Reconfigurable Integrated Circuits for ReImagine

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Flexibility of Digital Pixel Architectures

Different IR Imaging Modalities Enabled by MITLL DFPA

Wide Area Imaging

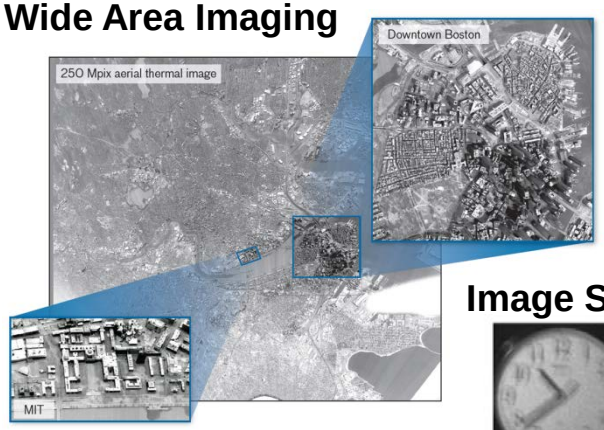
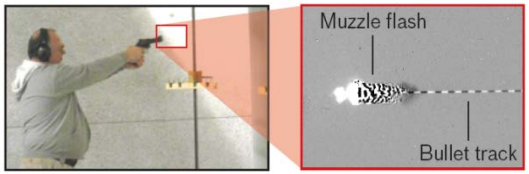


Image Stabilization

2D Convolutions

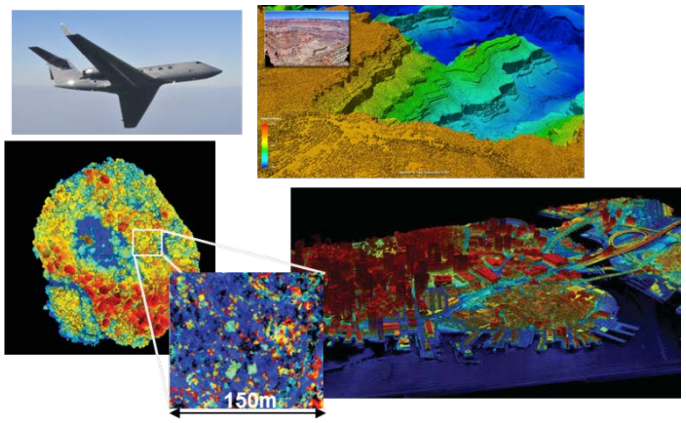
Fast Temporal Processing



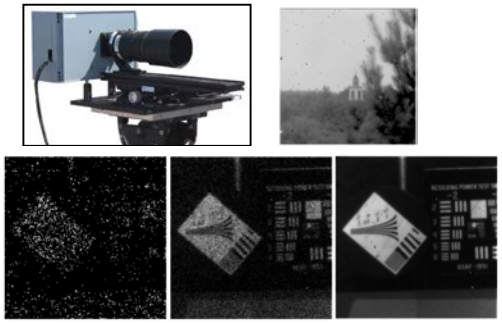
**DFPA = Digital Focal Plane Array*

Variety of Applications Enabled by MITLL Digital Pixels and Gm APDs

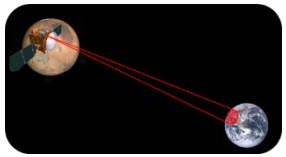
3D Ladar



Photon Counting Imaging



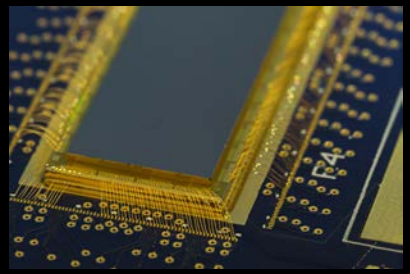
Optical Communications



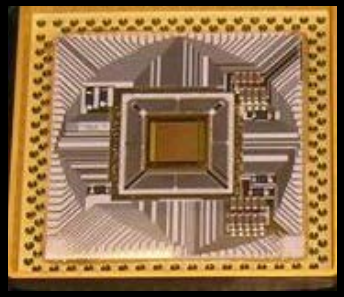
**Gm APD = Geiger Mode Avalanche Photodiode*

Digital ROICs Demonstrated by MITLL

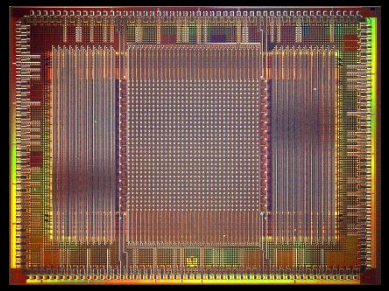
Digital Focal Plane Arrays



Gm APD Photon Counters



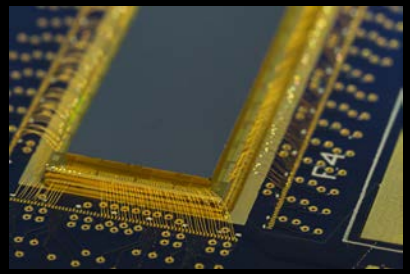
Gm APD Photon Timers



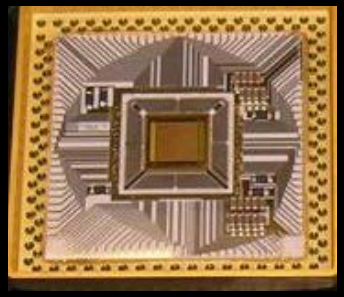
- **Digital Readout Integrated Circuit (ROIC) characteristics**
  - **ROICs are hybridized to an array of diodes (type of diode varies)**
  - **In-pixel digitization**
  - **All digital readout**
  - **Standard foundry CMOS process**
  - **Similar backend digital building blocks**

Digital ROICs Demonstrated by MITLL

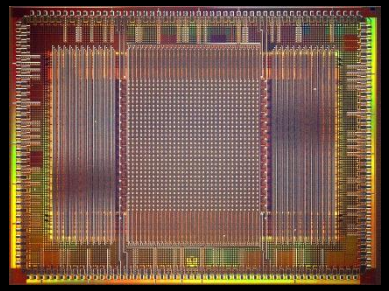
Digital Focal Plane Arrays



Gm APD Photon Counters



Gm APD Photon Timers



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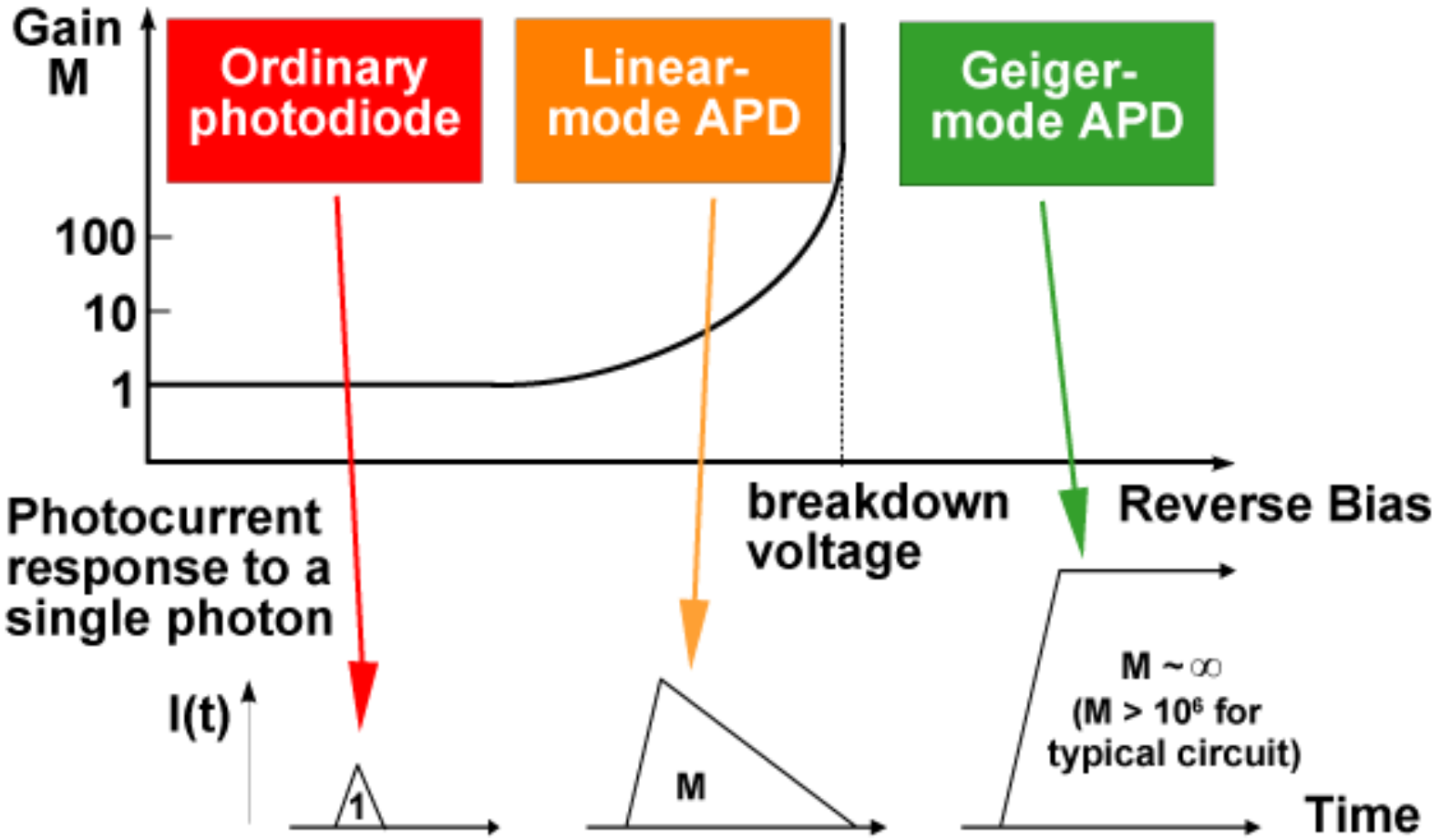
Key difference: How ROIC interfaces to diode and performs digitization

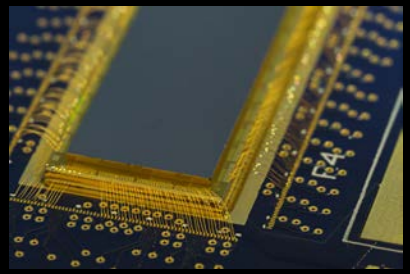
Photodiode Modes of Operation



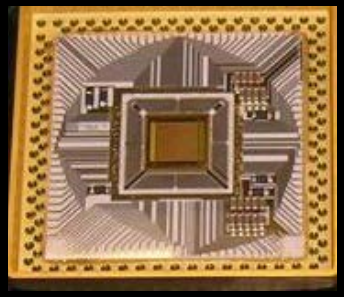
Each type of photodiode requires a different type of ROIC front-end circuit

In-pixel Digitization Methods

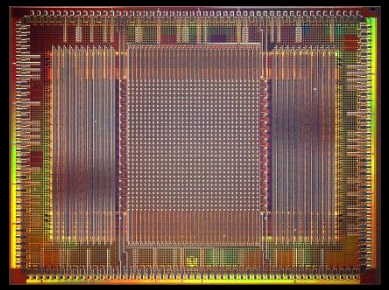
Digital Focal Plane Arrays



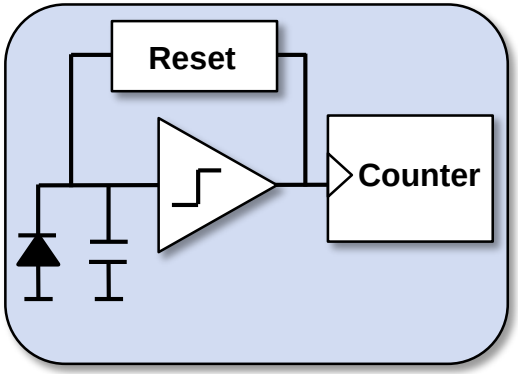
Gm APD Photon Counters



Gm APD Photon Timers

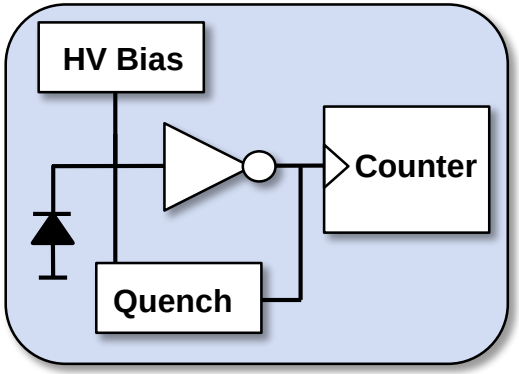


DFPA Pixel



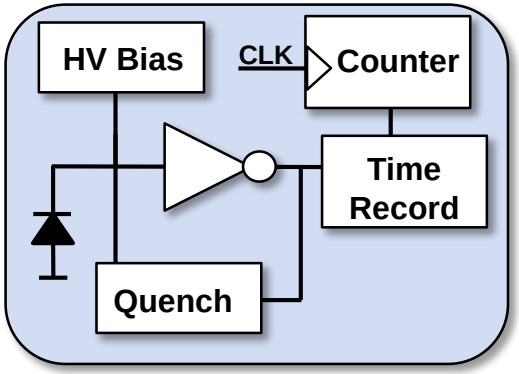
Count # of times capacitor fills up

Photon Counter Pixel



Count # of "Events"

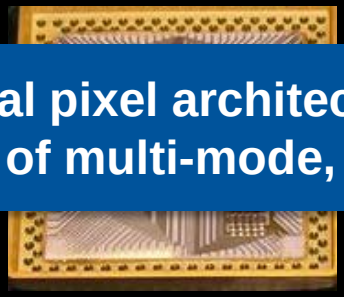
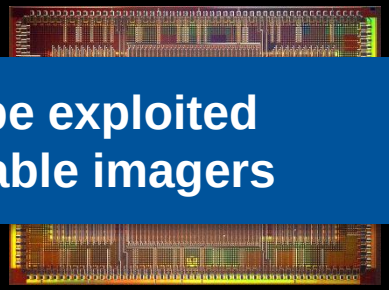
Photon Timing Pixel



Record Time of an "Event"

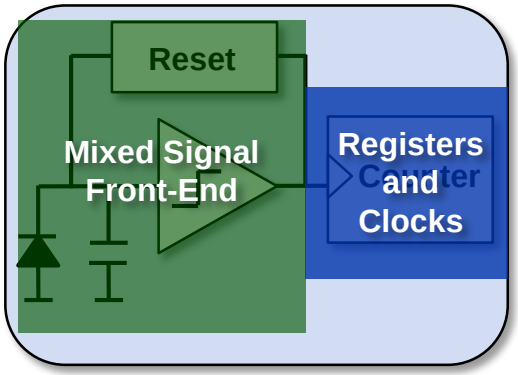
In-pixel Digitization Methods

Digital Focal Plane Arrays | **Gm APD Photon Counters** | **Gm APD Photon Timers**

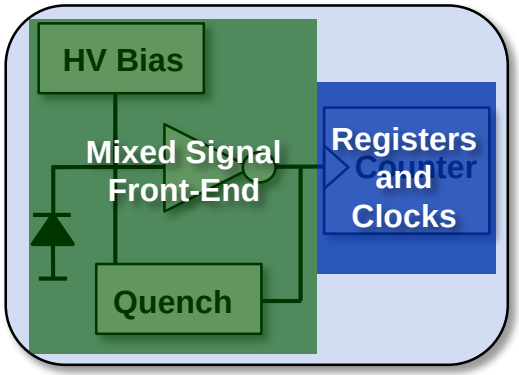
Commonality of digital pixel architectures can be exploited to enable a new class of multi-mode, reconfigurable imagers

DFPA Pixel



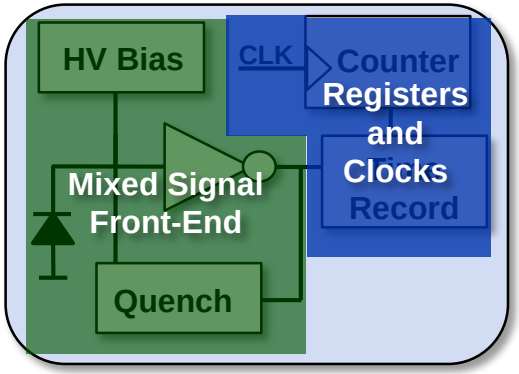
Count # of times capacitor fills up

Photon Counter Pixel



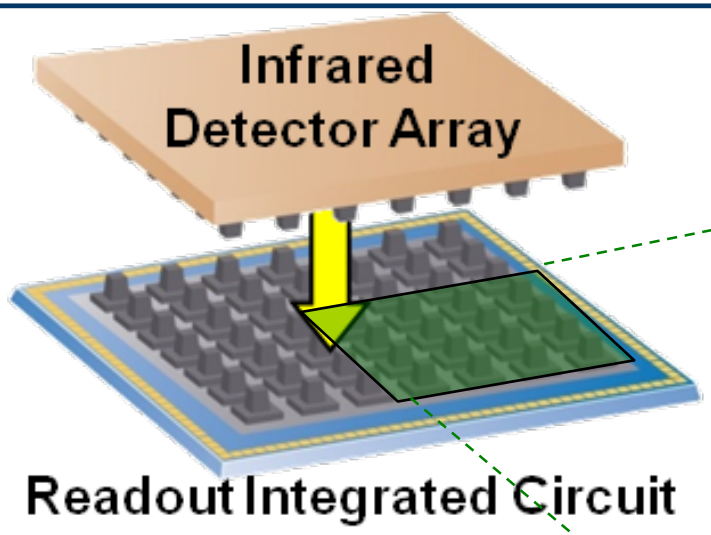
Count # of "Events"

Photon Timing Pixel

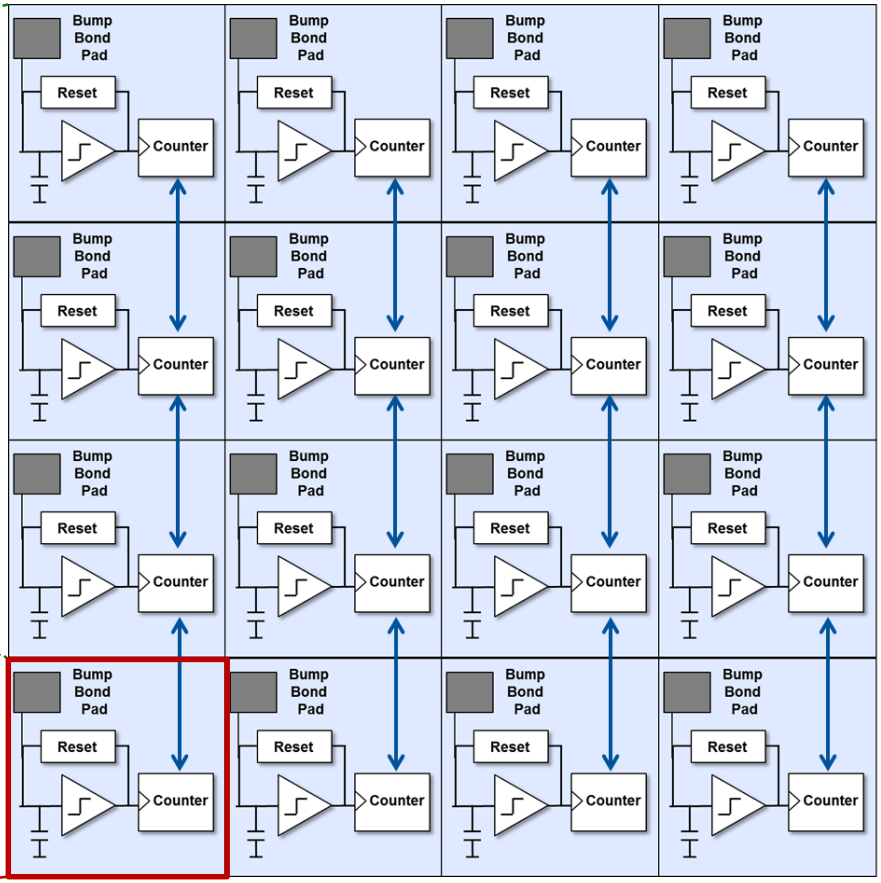


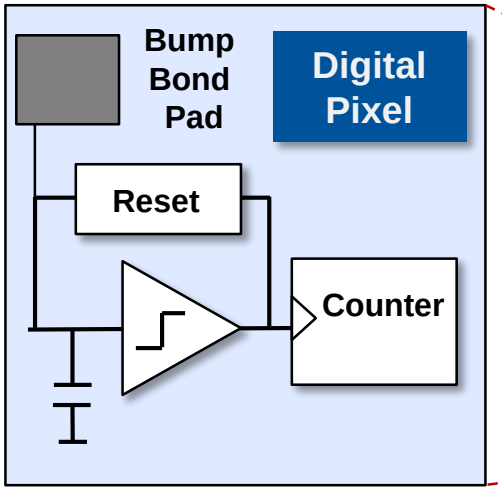
Record Time of an "Event"

MITLL Digital Focal Plane Array Architecture



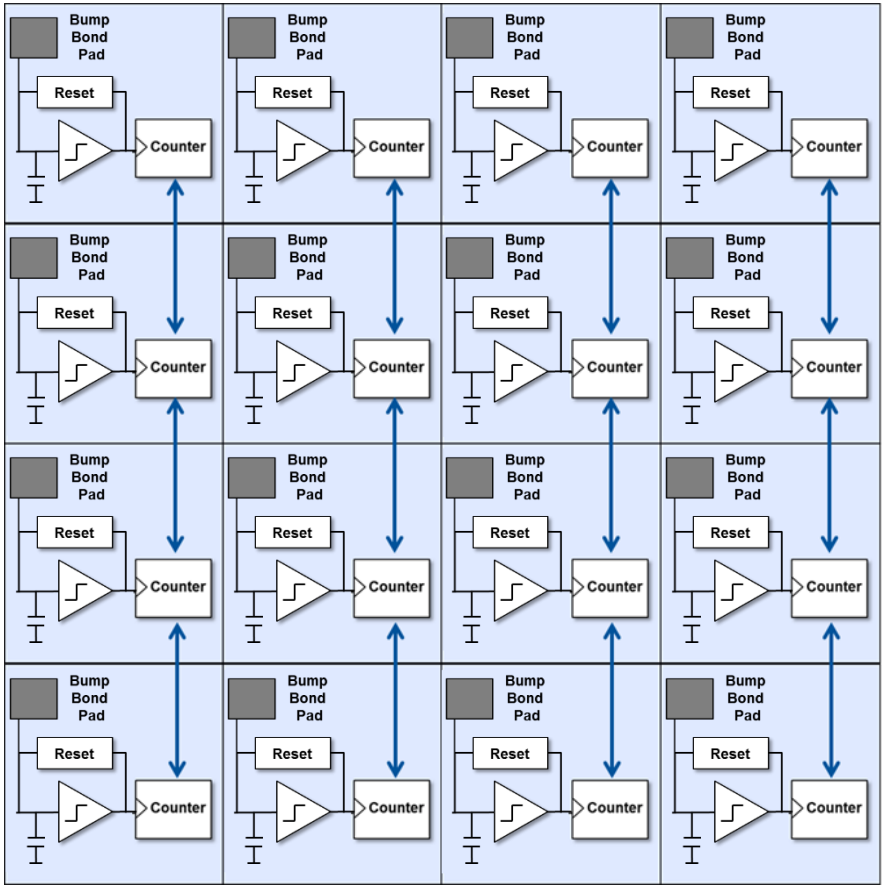
Digital Pixel Array





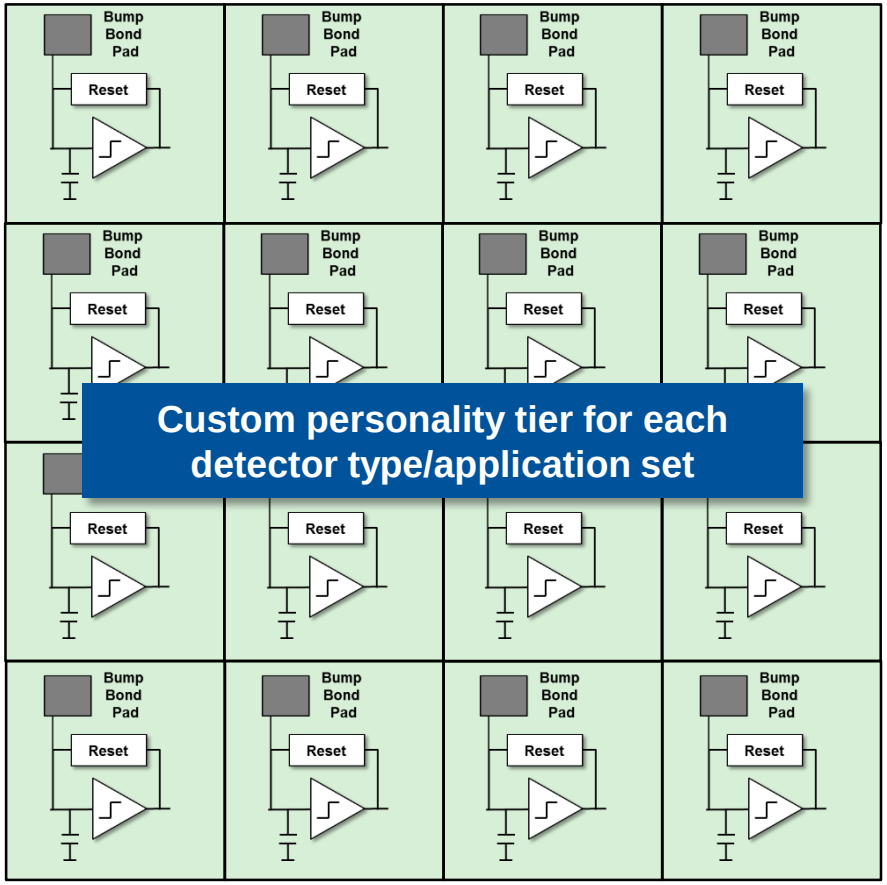
ReImagine 3D ROIC Approach

Digital Pixel Array

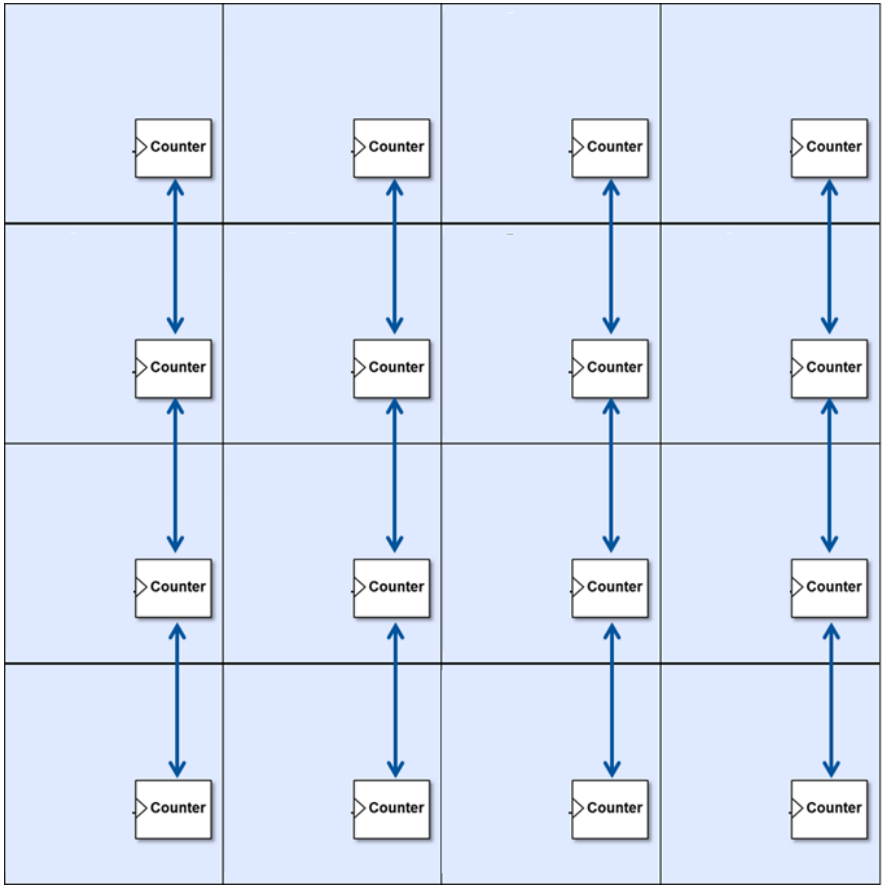


ReImagine 3D ROIC Approach

Tier 2 Personality Tier



Tier 1 Digital IC

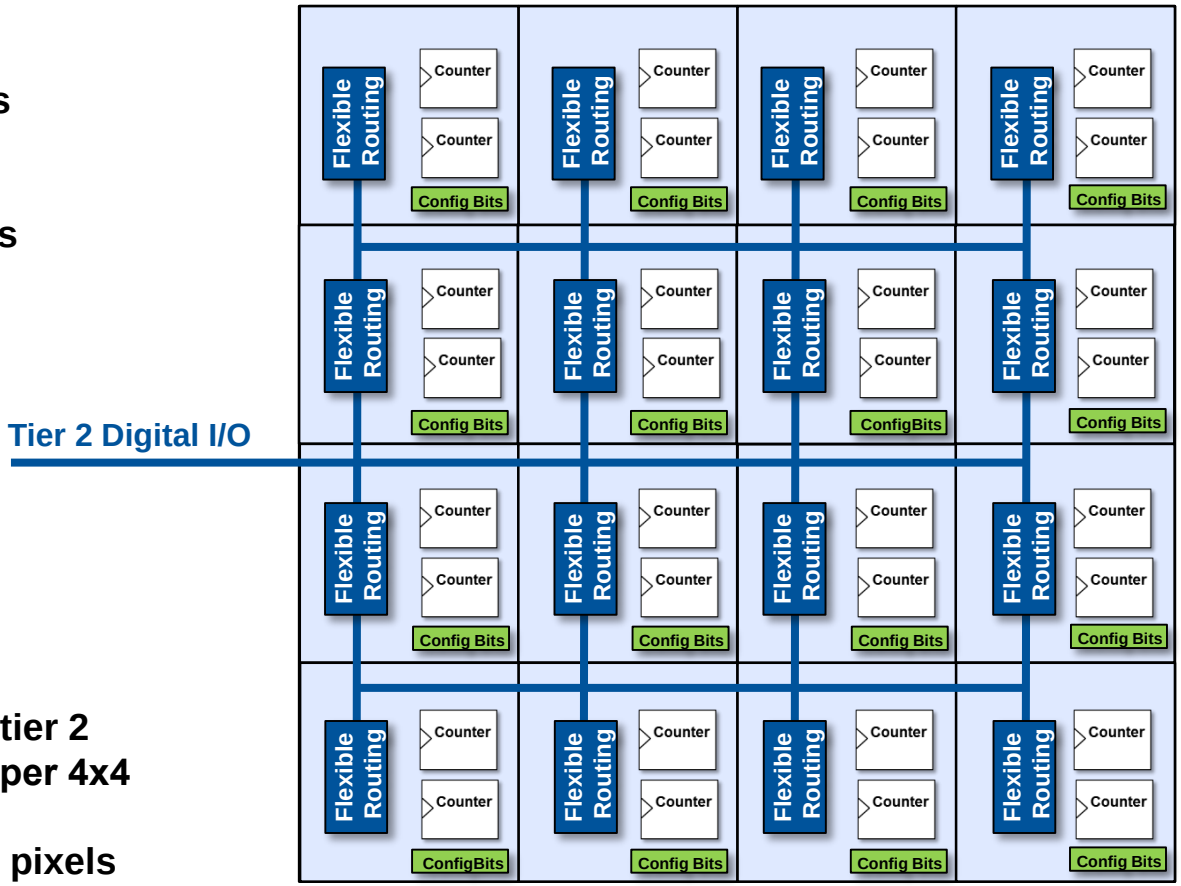


ReImagine 3D ROIC Approach

Gen 1 Architecture Concepts

1. Add additional counters
   - 8-bit register building blocks
   - ≥ 16 bits per pixel
2. Add counter configuration options
   - Count up/count down
   - Timing
   - Serial shift left/right
   - Orthogonal shift/route
3. Group pixels in to sub-arrays
   - Dynamic resource sharing within 4x4 sub-array
4. Add flexible routing
   - Digital inputs from pixels in tier 2
   - ≥ 1 bidirectional I/O to tier 2 per 4x4 sub-array
   - Orthogonal routing between pixels
   - Support for different pitch arrays

Tier 1 Digital IC



ReImagine 3D ROIC Approach

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   Example Configurations:
   - 16 pixels/16 bits
   - 4 pixels/64 bits
   - 1 pixel/256 bits
   - 12 pixels/8 bits and 4 pixels/40 bits
4. Add flexible routing
   - Digital inputs from pixels in tier 2
   - ≥ 1 bidirectional I/O to tier 2 per 4x4 sub-array
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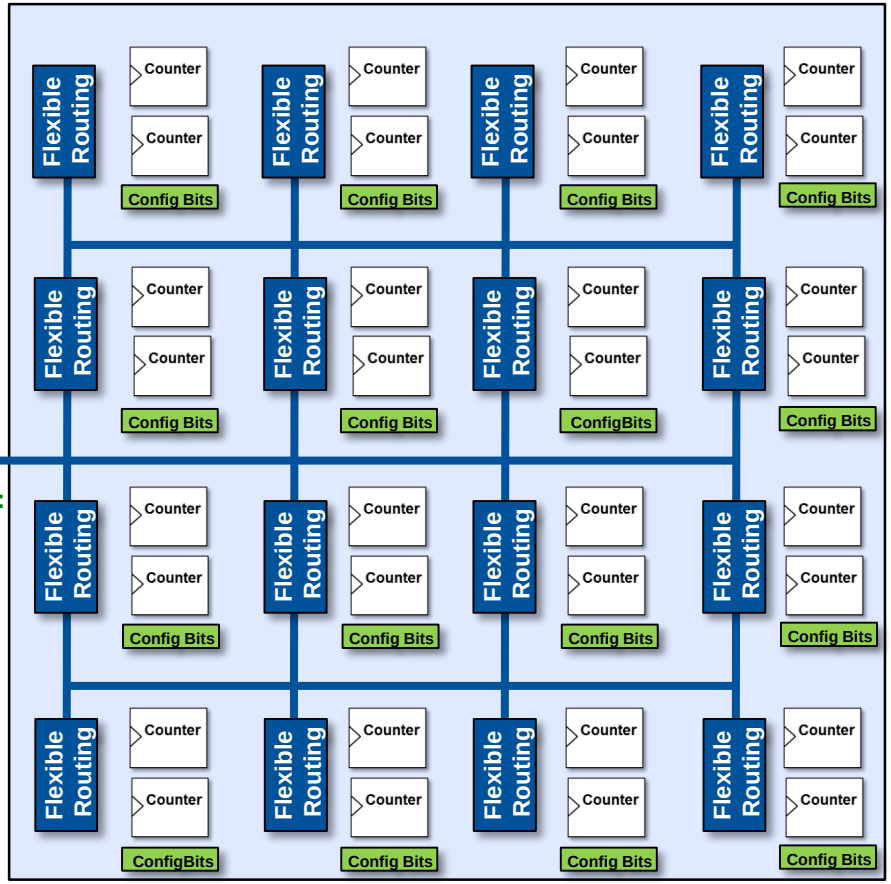
Tier 1 Digital IC

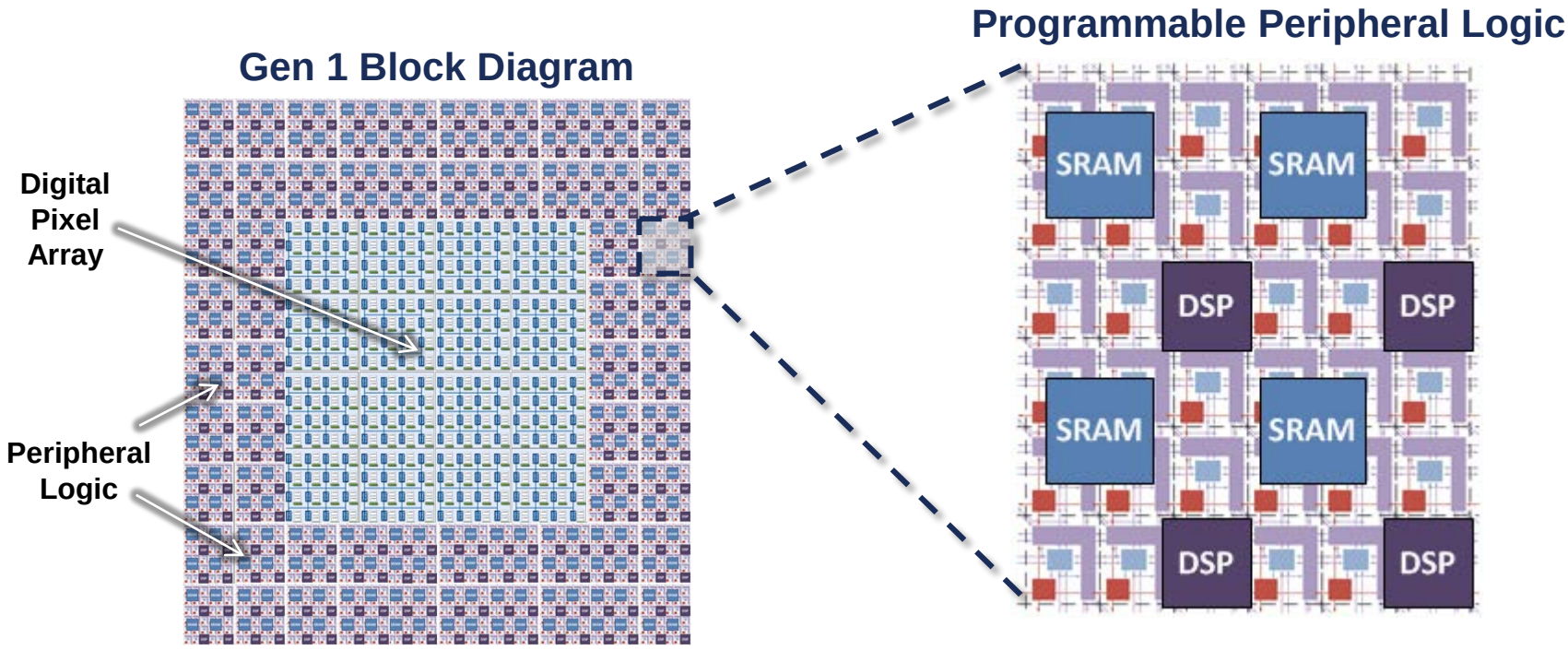


Notional Device Specification

Gen 1 Notional Characteristics

Criterion	Gen 1
Pixel Format	640 x 512
Pixel Pitch	≥ 10 µm
Operating Temperature	77 – 300 K
Minimum Tier 1-2 Interconnect Pitch	5 µm
Digital Registers/Pixel	≥ 16 bits
Pixel Configuration	• 8 bits per counter, independently configurable • Count up/down or timing • Serial shift left/right • Orthogonal data shift/route • Resource configuration per 4x4 pixel sub-array
Tier 2 Interface	≥ 1 bidirectional I/Os per 4x4 pixel sub-array
Routing	4 reconfigurable routing channels per 4x4 pixel sub-array
Peripheral Logic	• ≥ 10k look up tables • ≥ 64 DSP blocks • ≥ 1 MB memory

FPGA-like Resources and Programming



- **Pixel array will be surrounded by banks of reconfigurable logic resources**
- **Reconfigurable periphery and pixel array circuitry programmed through FPGA based synthesis and place and route tools**
  - **Tools consist of open source FPGA CAD tools and government furnished software from MITLL as well as a library of Verilog models of ReImagine digital resources**

Summary

- **MITLL leveraging extensive background in digital pixels to develop next generation reconfigurable integrated circuits for ReImagine**
- **Gen 1 IC will provide arrays of dynamically reconfigurable counter resources surrounded by peripheral programmable logic**
- **Gen 2 IC will expand and Gen-1 concepts and replace some of the counter resources in the pixel array with more complex digital blocks (e.g. memories, adders, multipliers, etc)**
- **Reconfigurable ICs will be programmed through a combination of open source FPGA CAD tools and government-furnished software from MITLL**