Stress Testing of Semiconductor Switches for PV Inverter Applications at Sandia National Laboratories

Utility-Scale Grid-Tied PV Inverter Reliability Workshop

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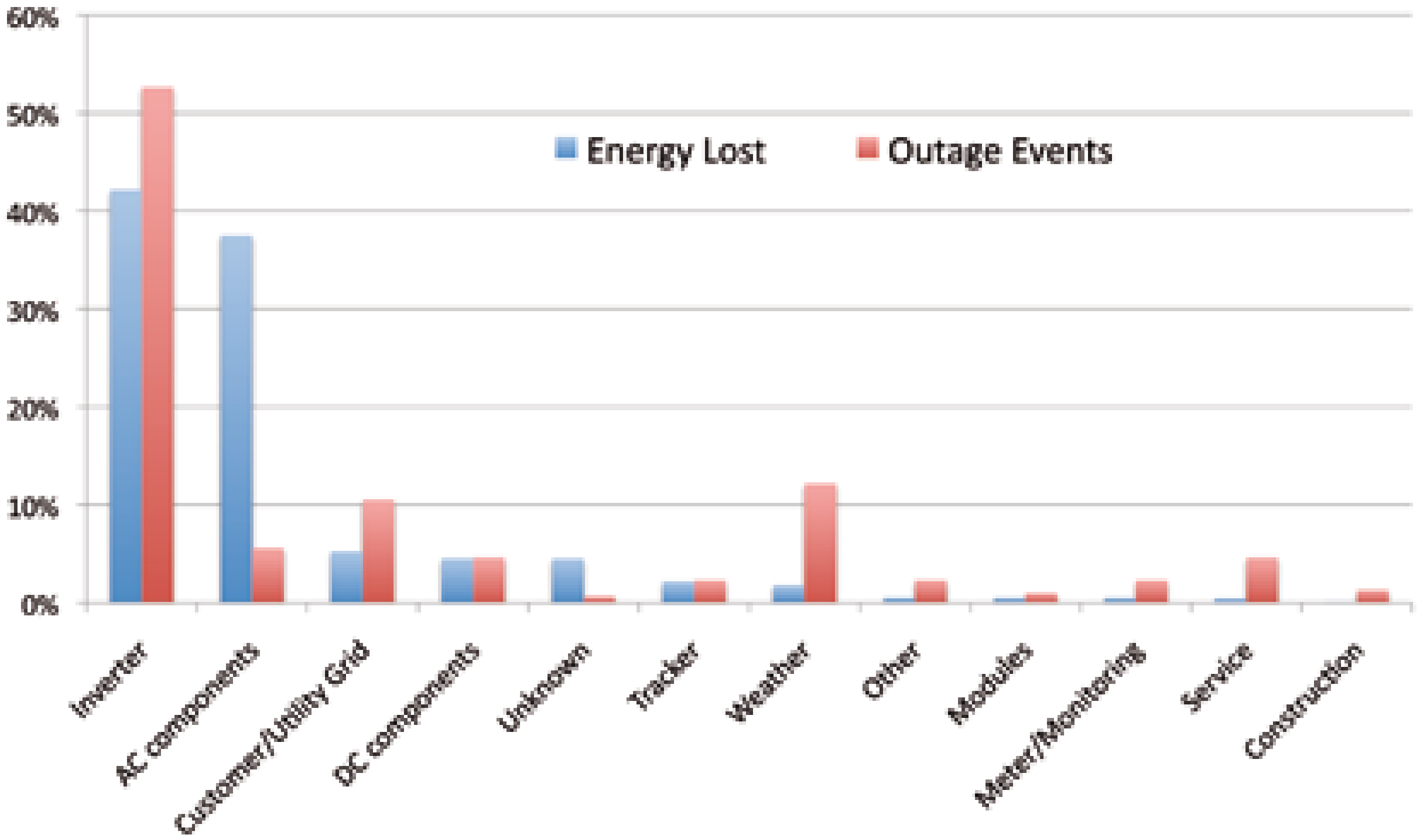
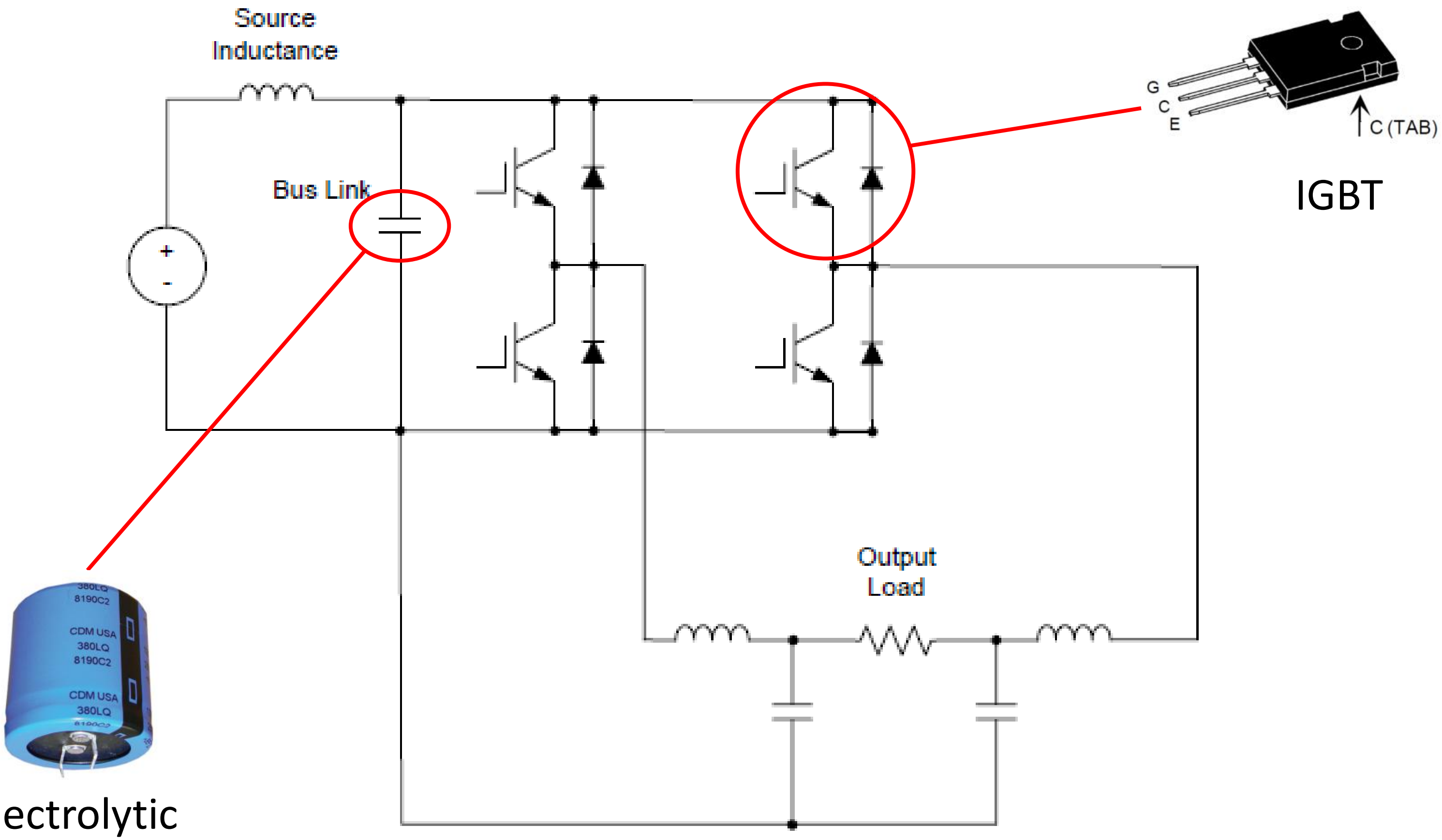
Is the inverter the least reliable component of the PV system?



Source: Photovoltaics International pp. 173-179
PV International Edition 5 (Sep. 16, 2009)

Basic inverter circuit topology (single-phase H-bridge)

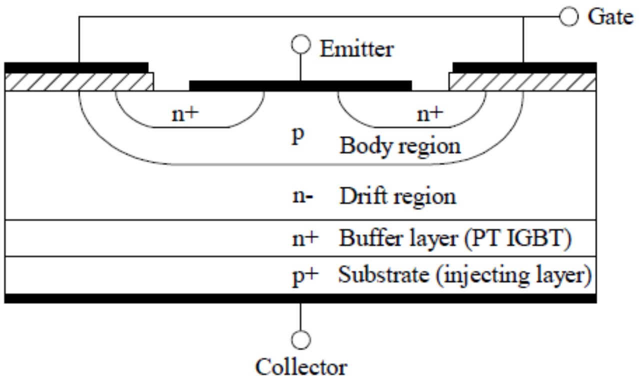


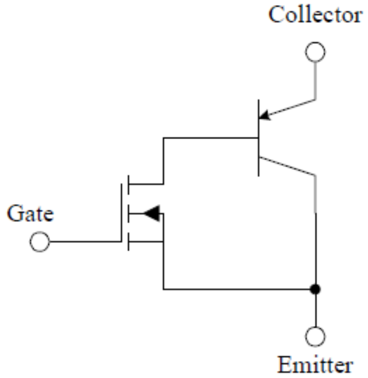
IGBT

Electrolytic capacitor

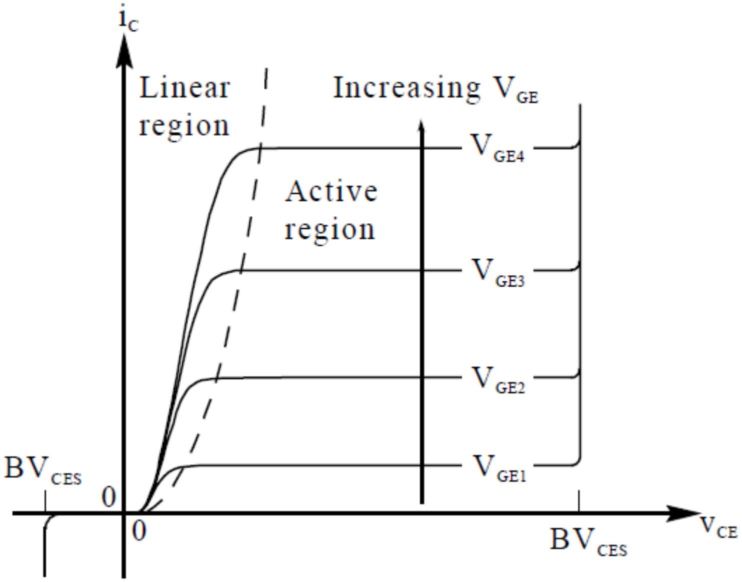
Other critical components?

Semiconductor switch: Insulated-Gate Bipolar Transistor (IGBT)





- Hybrid MOS-bipolar structure
- Main conduction is through the bipolar device with the base current controlled by the MOS device
- Allows for very high collector currents coupled with high gate impedance
- Switching tends to be slower than power MOSFET due to minority carrier storage in base region
- Unlike power MOSFET, minimal reverse current



Drawings from Advanced Power Technology Application Note APT0201 (July 2002)

IGBT Device Reliability

- IGBT is repeatedly subjected to alternating cycles of ON state (high current / low voltage) and OFF state (low current / high voltage)

- During switching, the device is briefly (few μs) subjected to a transition during which it experiences very high power (high current / high voltage)

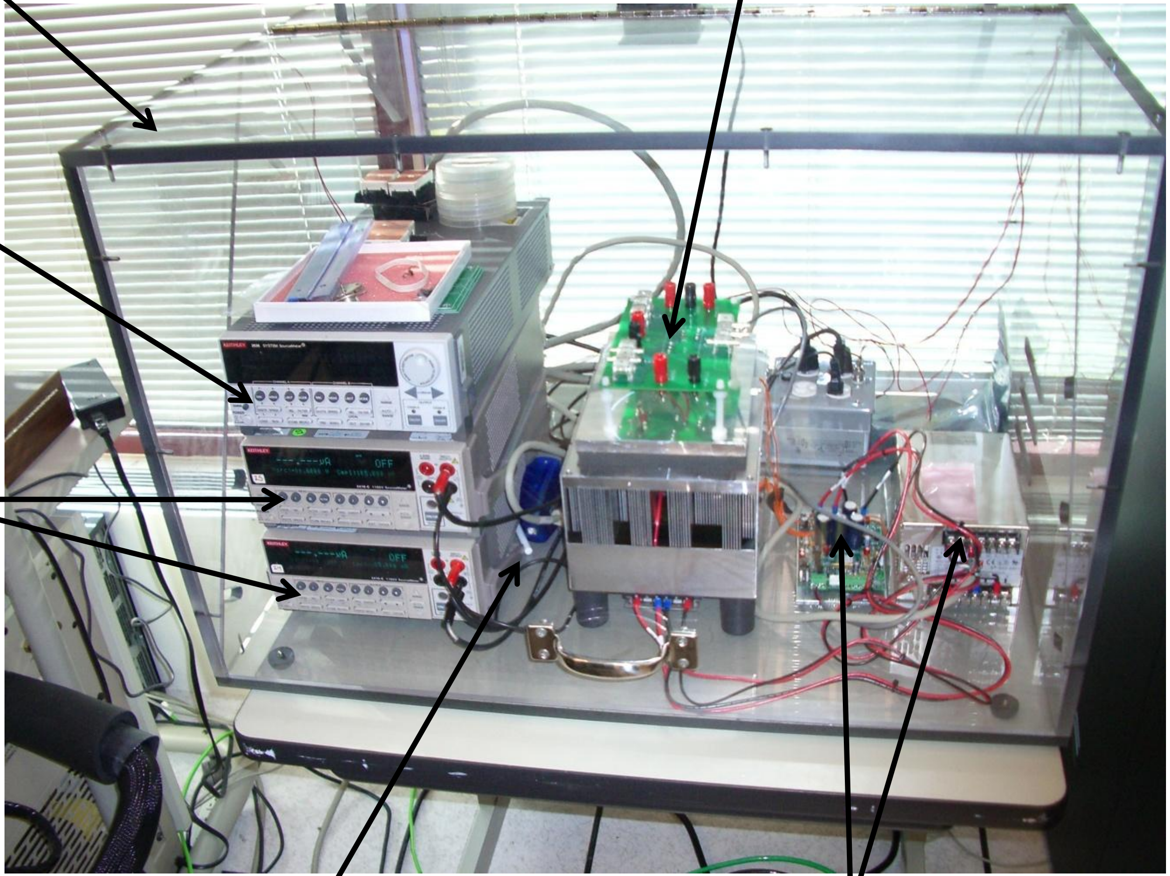
- High power generates lots of heat; improper heat-sinking may degrade device lifetime and / or cause catastrophic failure

- Inverter may need to operate in hot environments, and may also be subject to wide swings in operating temperature

- Si- based IGBT is a fairly mature but is subject to degradation mechanisms that are common to all Si-based devices (e.g. SiO_2 gate breakdown)

- Our initial testing has been focused on high current / low voltage stress condition

Experimental set-up



Safety interlock box

Sample mount

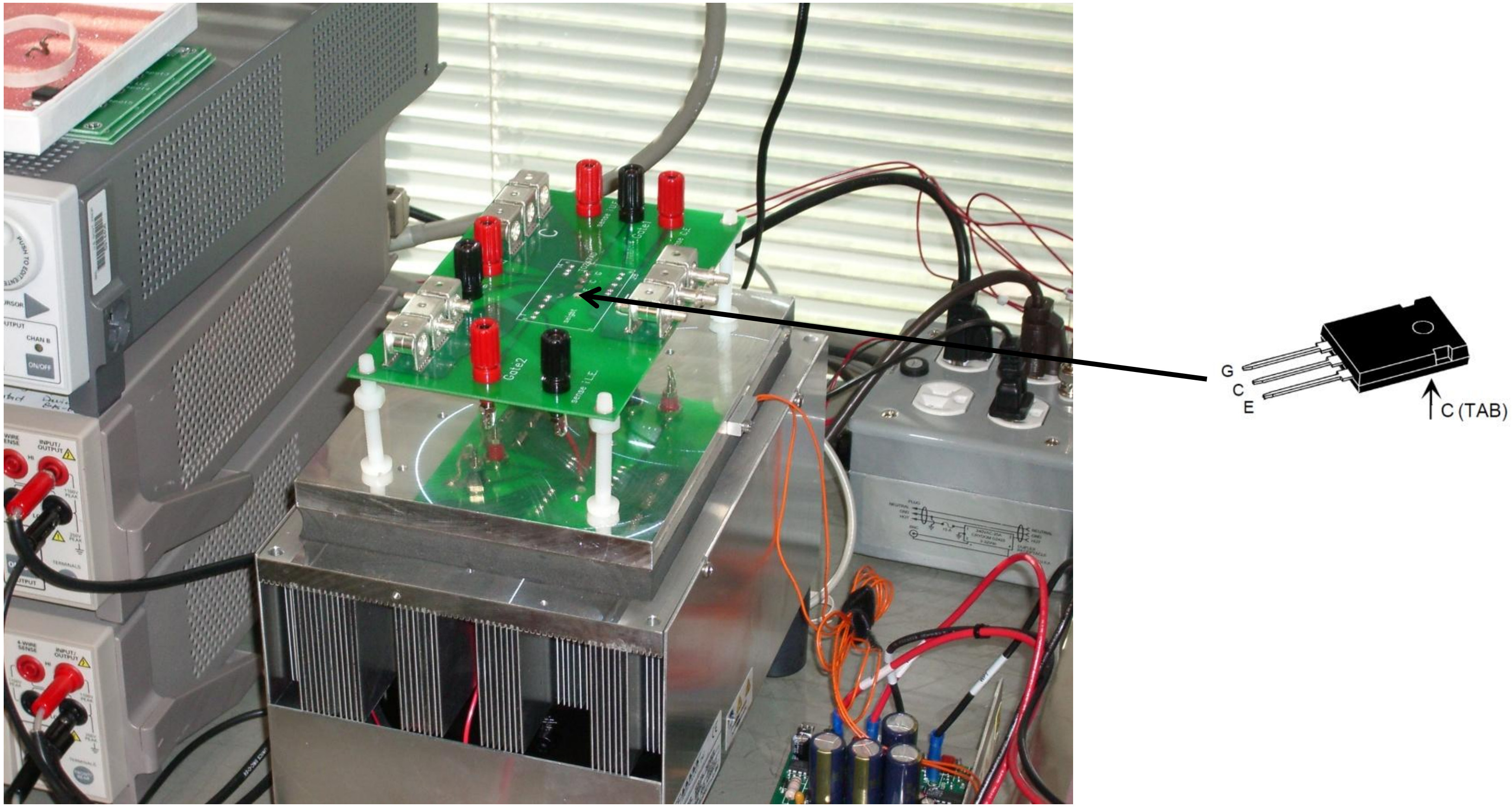
Dual-channel High-resolution SMUs (gate current, etc.)

High-voltage (1100 V each) SMUs for off-state stressing

Heating / cooling plate

Heating / cooling plate power supply and control

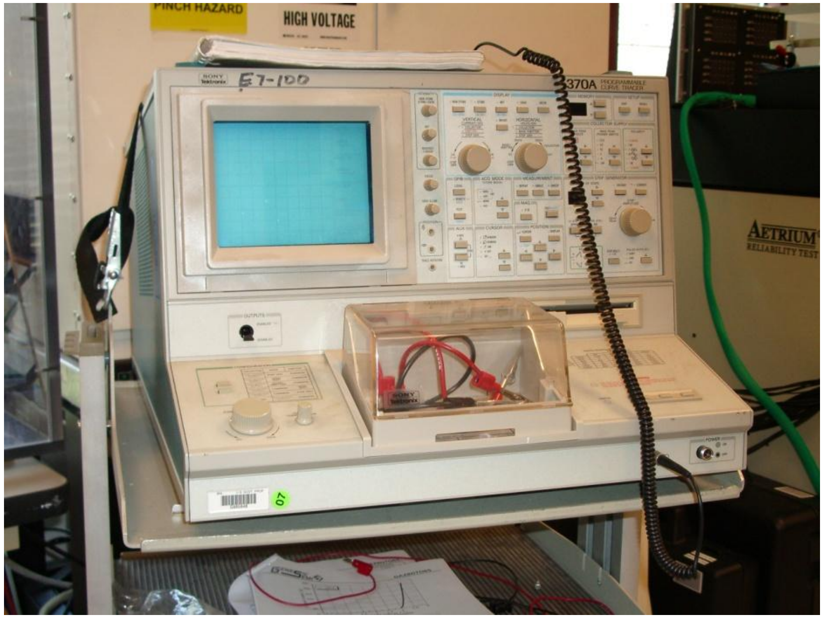
Sample mounting



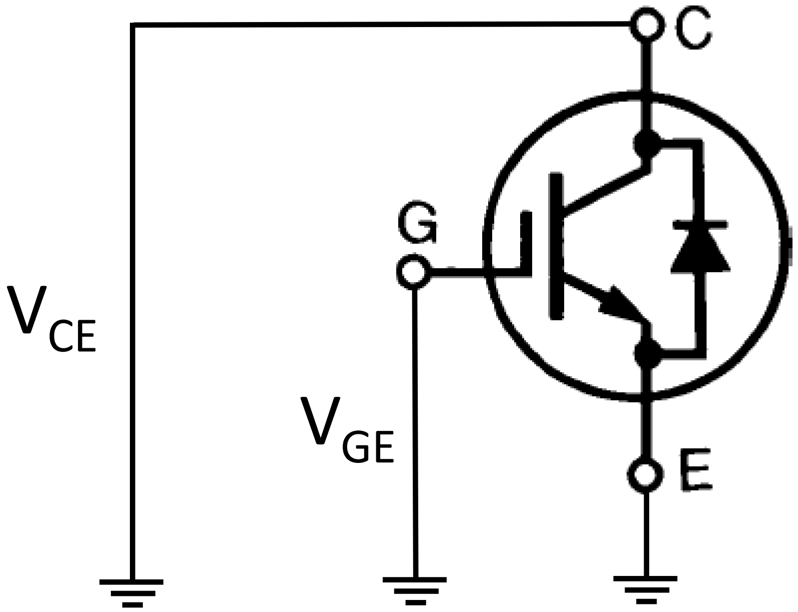
Stress / measure equipment

3200 W power supply
(400 A, 8 V)

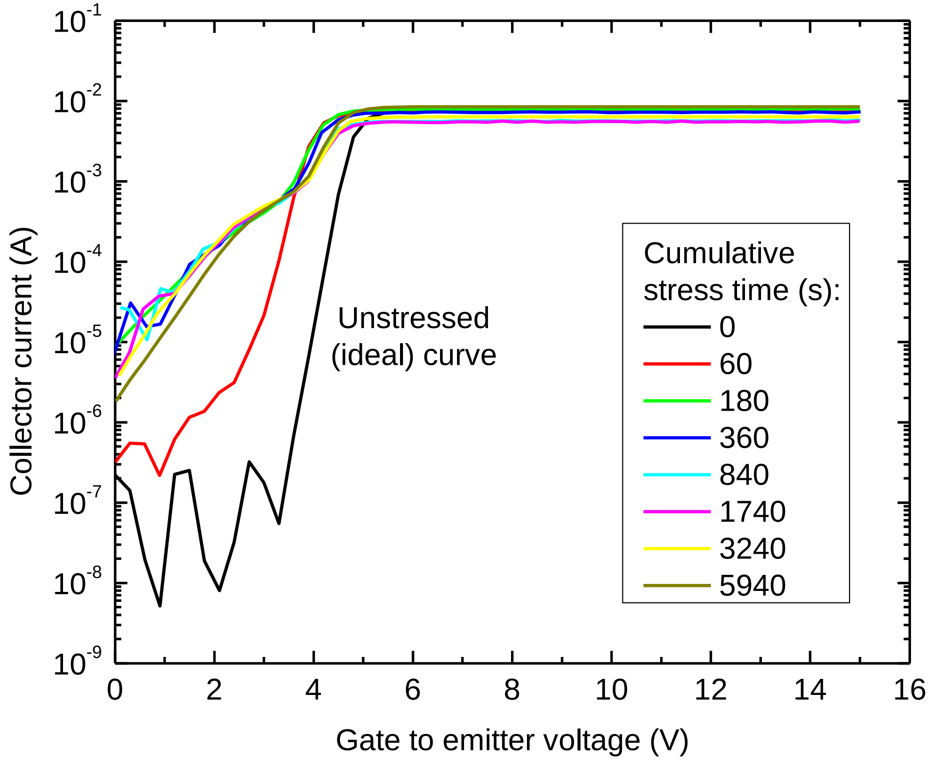
Curve tracer



Bias configuration for IGBT stress-measure experiments



Experiment #1 (25°C stress)



600 V, 60 A device found in several inverters that we examined

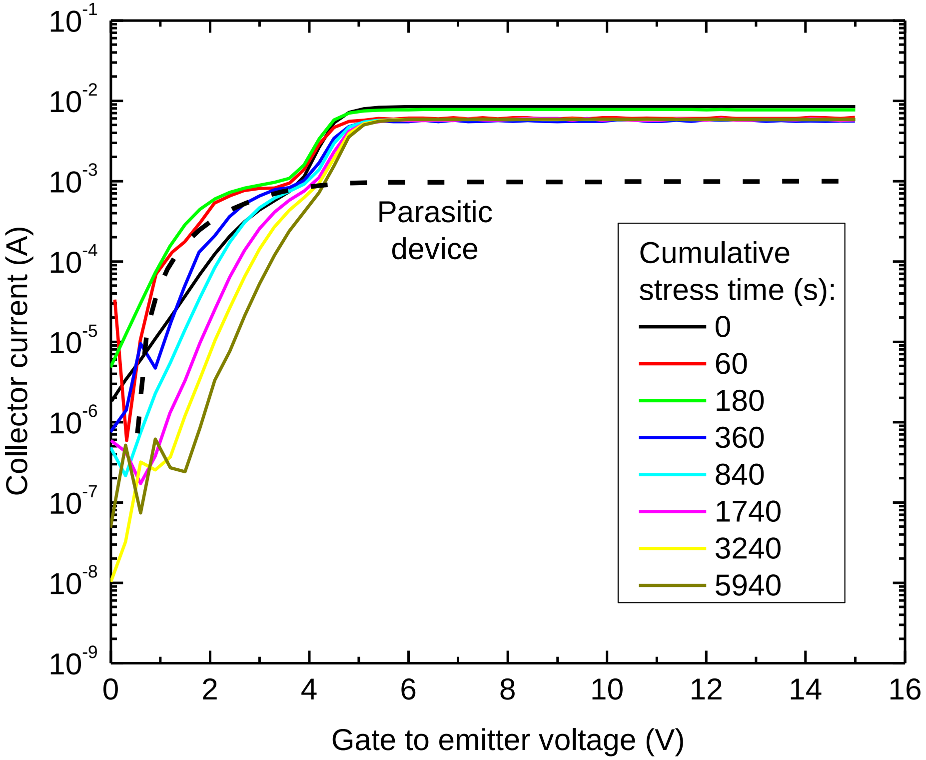
Fast initial degradation in sub-threshold region, appears to saturate; not much degradation in on-state characteristics

Degradation not observed on all samples tested (a few samples measured so far)

1. Measure I_C-V_{GE} curve for fixed V_{CE} = 1 V at 25°C
2. Stress device using V_{GE} = 20 V, V_{CE} = 2 V at 25°C; $I_C \approx 38$ A
3. Repeat

Experiment #2 (100°C stress)

Use the same device as the previous experiment



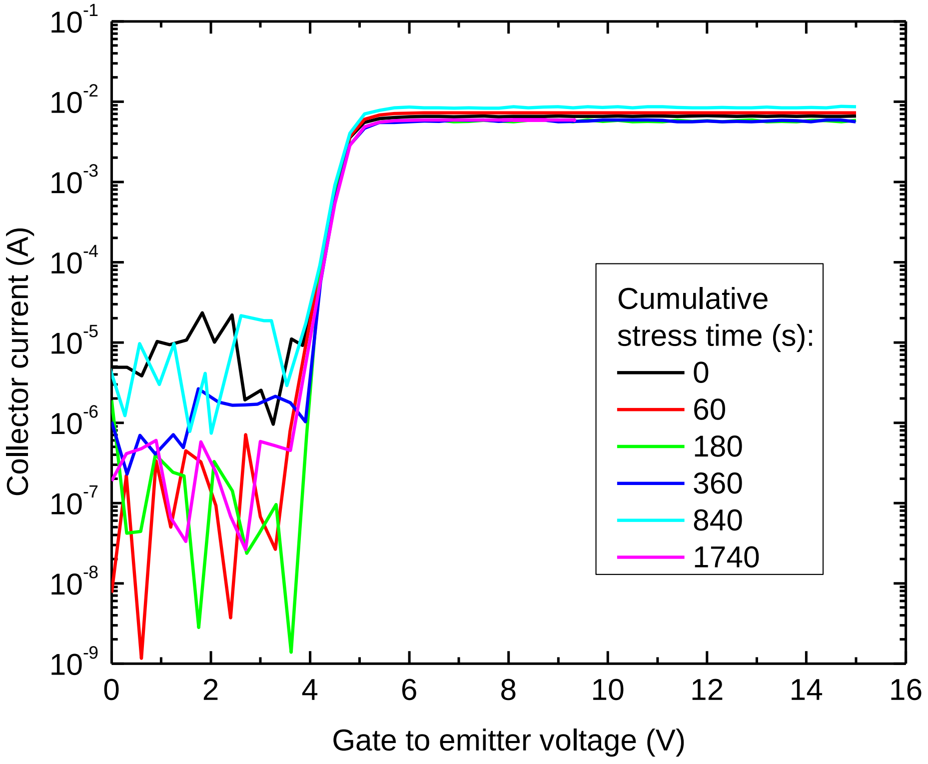
High-temperature stress appears to anneal out the damage from the low-temperature stress

Is change in IV curve due to introduction of parasitic device?

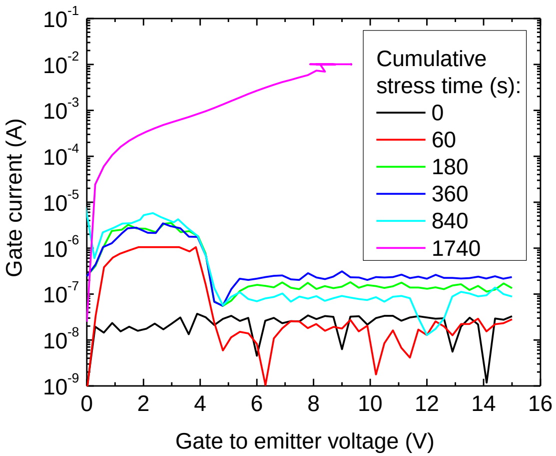
1. Measure I_C-V_{GE} curve for fixed V_{CE} = 1 V at 25°C
2. Stress device using V_{GE} = 20 V, V_{CE} = 2 V at 100°C; $I_C \approx 38$ A
3. Repeat

Experiment #3 (100°C stress)

Use a fresh device

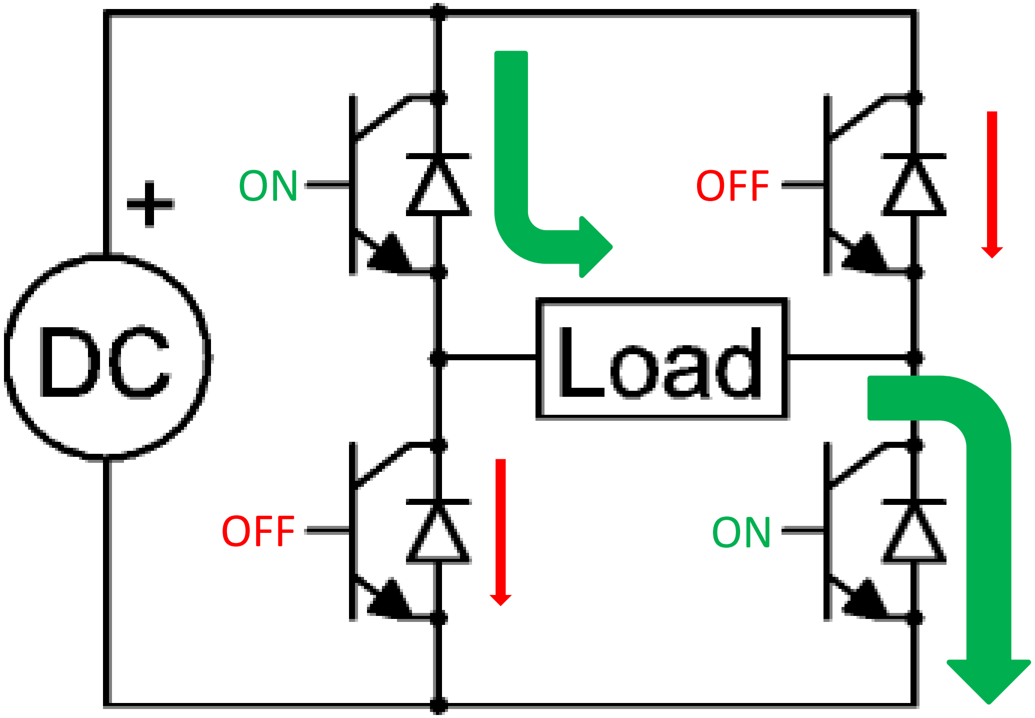


Minimal degradation when stressed at high temperature; results suggestive of hot-carrier damage in the MOS part of the device; but gate current becomes worse at high T (different failure mechanism)



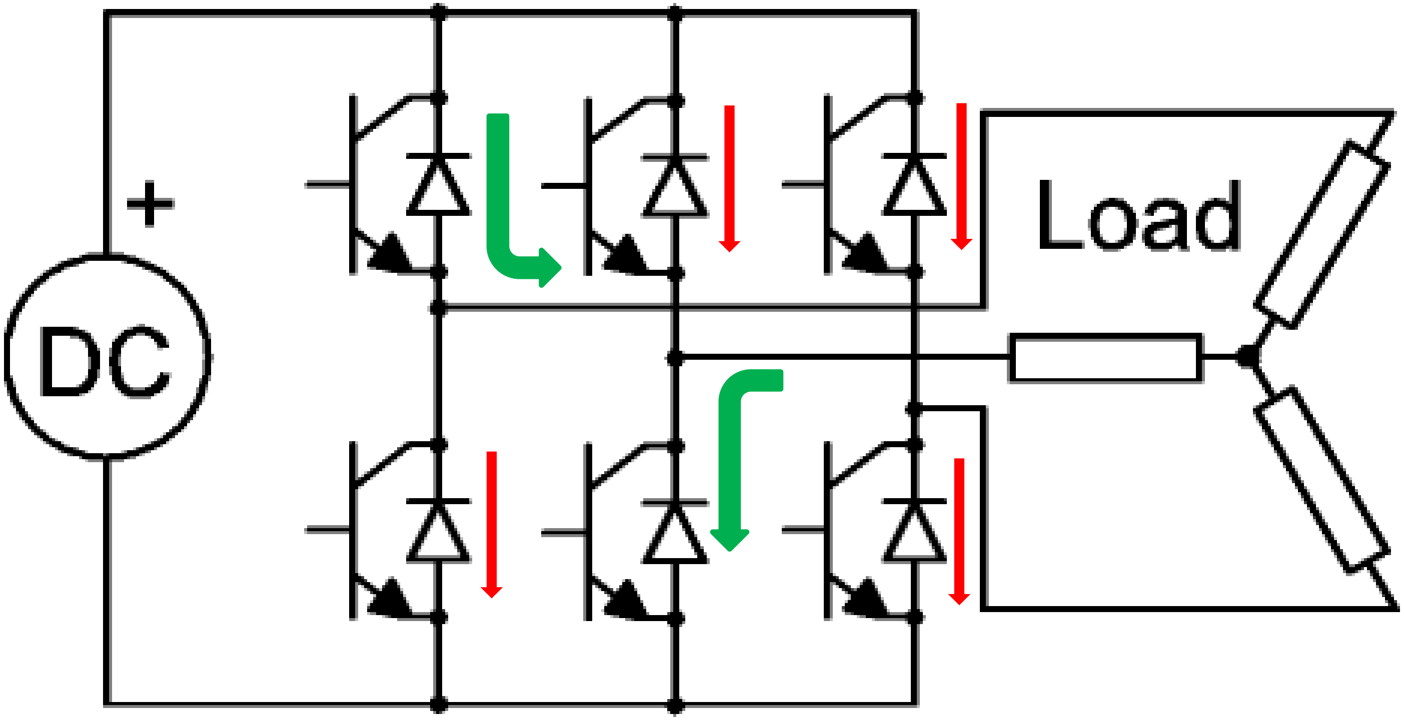
1. Measure I_C-V_{GE} curve for fixed V_{CE} = 1 V at 25°C
2. Stress device using V_{GE} = 20 V, V_{CE} = 2 V at 100°C; $I_C \approx 38$ A
3. Repeat

Possible impact on inverter performance



- OFF-state leakage current may result in loss of power delivered to load
- Need to evaluate devices at much higher V_{CE}
- Planning SPICE modeling to determine impact on inverter efficiency

Same concept applies to three-phase inverter

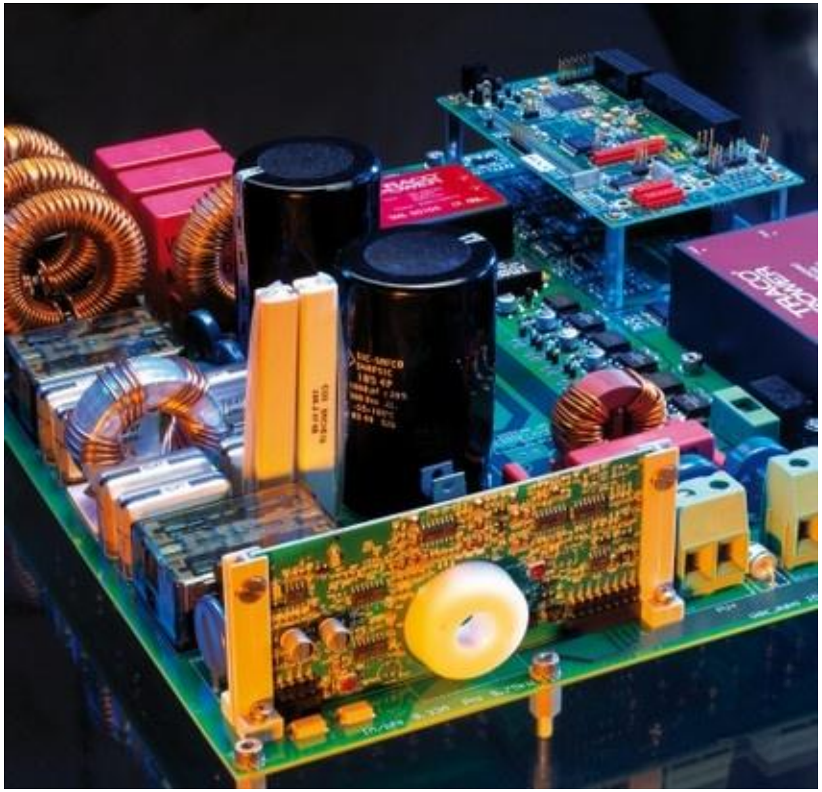


IGBT monitoring inside inverter

- Plan is to monitor IGBT properties inside working inverter to compare degradation to device-level testing

- Several inverters have been purchased, currently setting up (planning to use solar simulator as DC source)

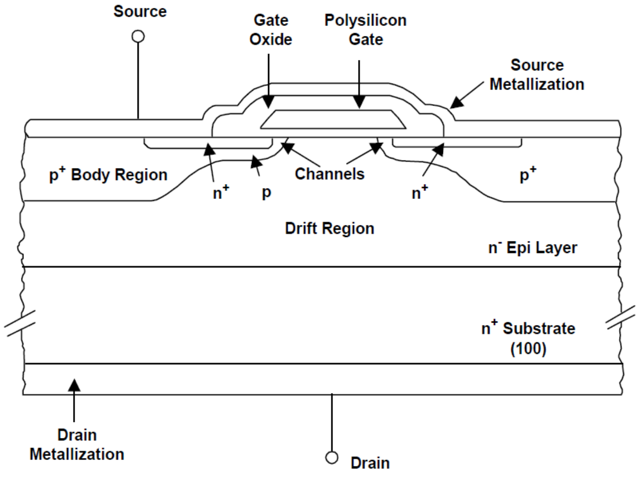
"Post-Silicon" device reliability for power electronics

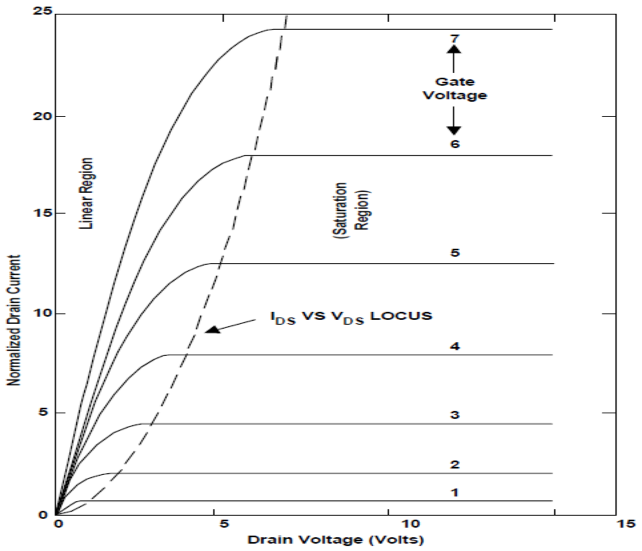


- Record-efficiency inverter has been demonstrated using SiC MOSFETs

- We have done reliability testing on the same MOSFET used in the inverter

SiC power MOSFET

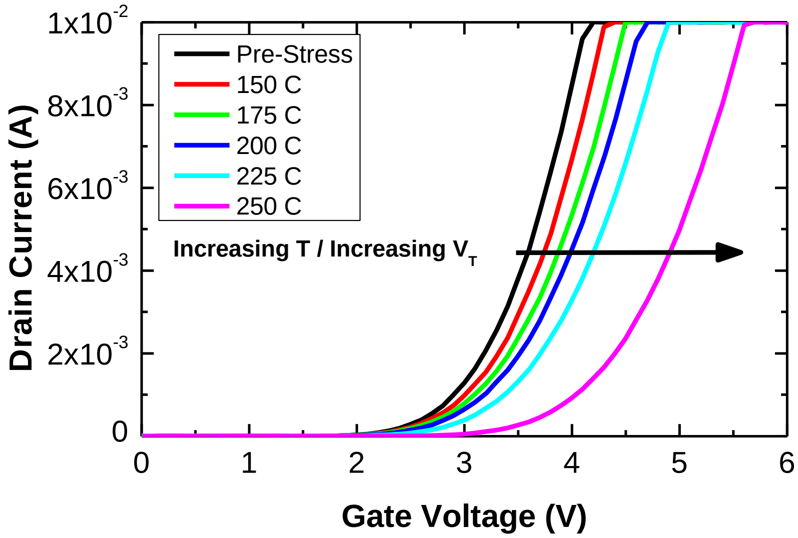


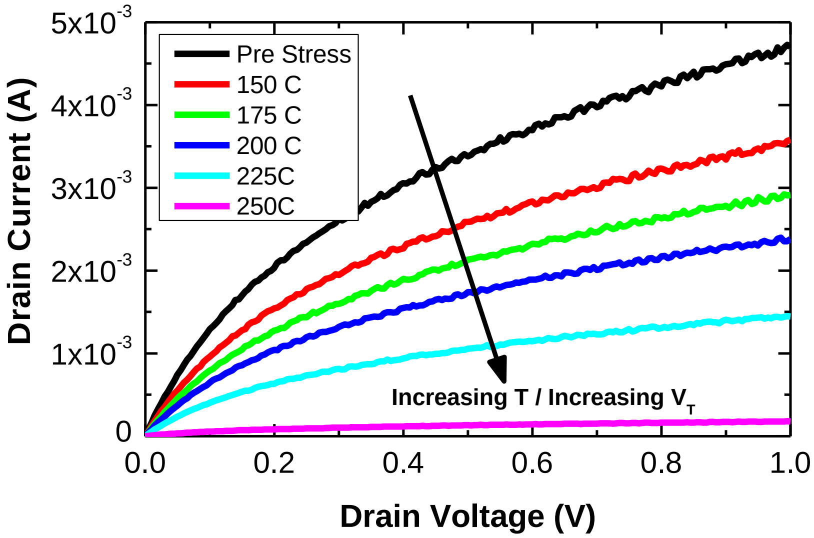


Drawings from International Rectifier, “Power MOSFET Basics”

- SiC has many intrinsic material advantages over Si for power devices
  - Large bandgap (low intrinsic carrier concentration at high T)
  - High breakdown field strength (avalanche breakdown)
  - High thermal conductivity
- But it is a much less mature technology and is thus less reliable
  - SiO_2 gate oxide reliability
  - SiC material defects (μ-pipes), stacking faults

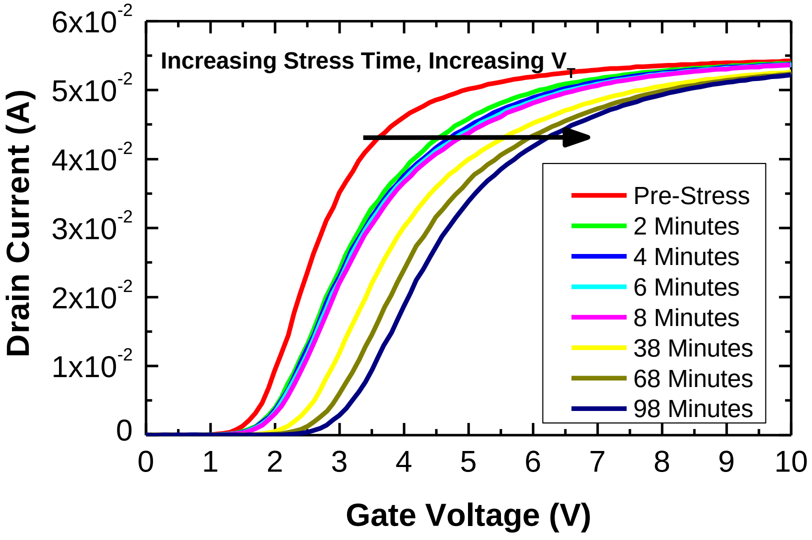
n-channel SiC MOSFET BTS experiment #1

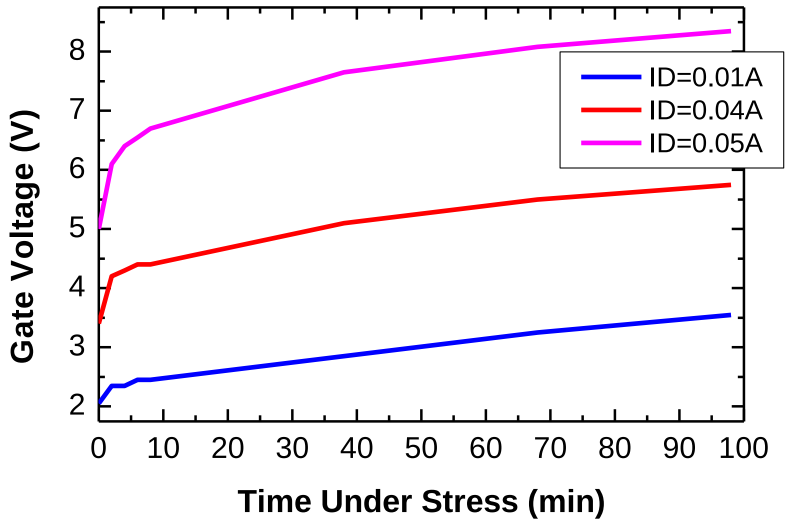




- Measured I_D-V_G (V_D = +1 V) and I_D-V_D (V_G = +4 V) curves at room T
- Heated sample to temperature indicated and applied +20 V gate voltage for 7 minutes
- Cooled back to room temperature and I_D-V_G, I_D-V_D curves were re-measured
- Process was repeated for various stress temperatures
- Positive V_T shift suggests presence of negative charge in oxide, perhaps injected from n-channel during stress
- Decrease in current for fixed bias degrades ON-state performance of device

n-channel SiC MOSFET BTS experiment #2





- Sample heated to 225°C and I_D-V_G curve measured (V_D = +1 V)
- Gate stress of +20 V applied for time indicated
- I_D-V_G curve re-measured at 225°C
- Process was repeated for various additional stress times
- Increase in V_T is again observed and will degrade ON-state performance of switch, resulting in less power delivered to load

Continuing work

- Stressing of Si-based IGBTs under various conditions
  - High current, high voltage, transient high power

- Monitoring of IGBTs in actual inverters and comparison to device-level testing

- Modeling of device lifetime and failure mechanisms for inclusion in inverter and system reliability models

- "Post-Si" device studies (SiC, GaN) for future power electronics needs
  - Basic defect studies and reliability physics
  - Device modeling

- Stress testing of electrolytic bus capacitors

- **Goal is to establish unbiased, standardized test procedures and reliability / efficiency models for industry**