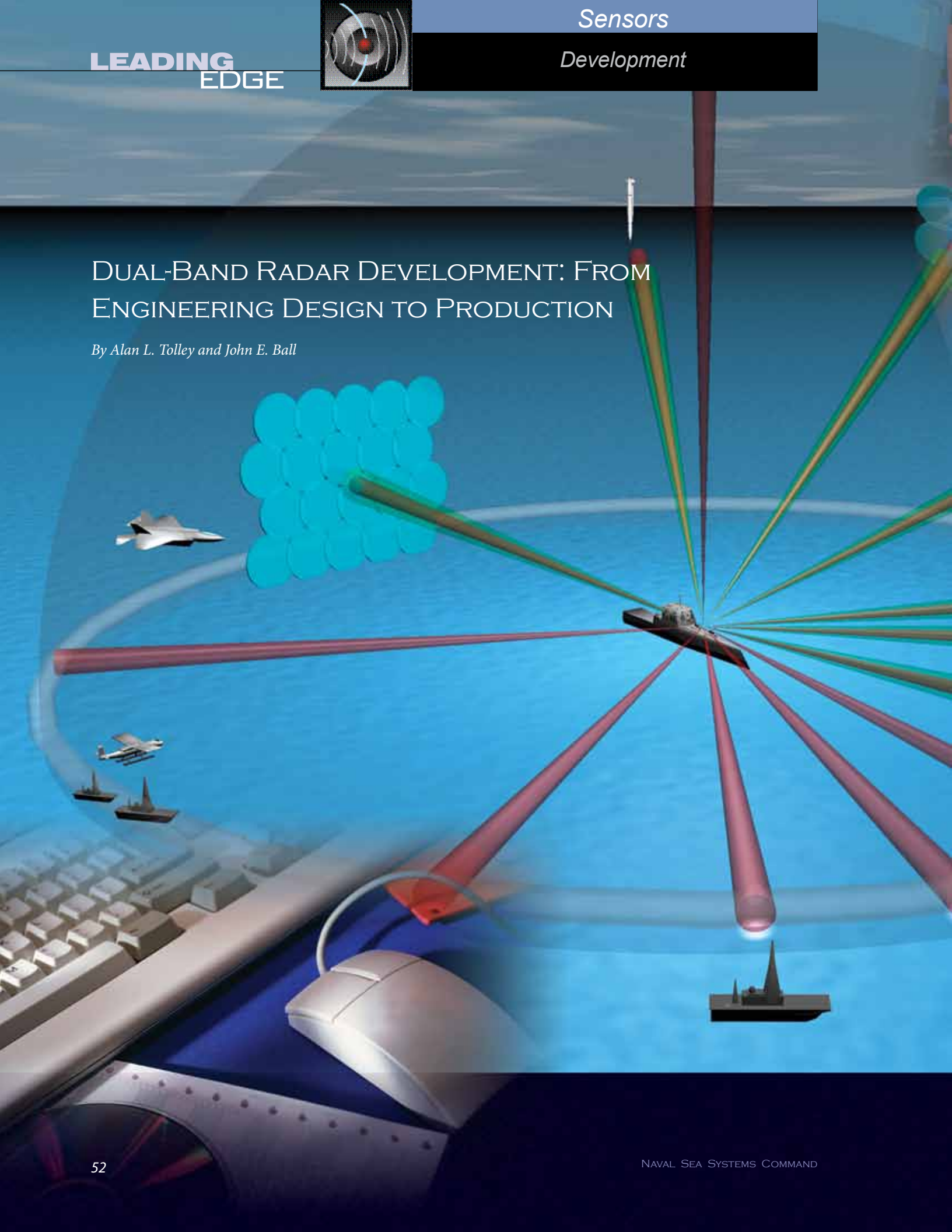
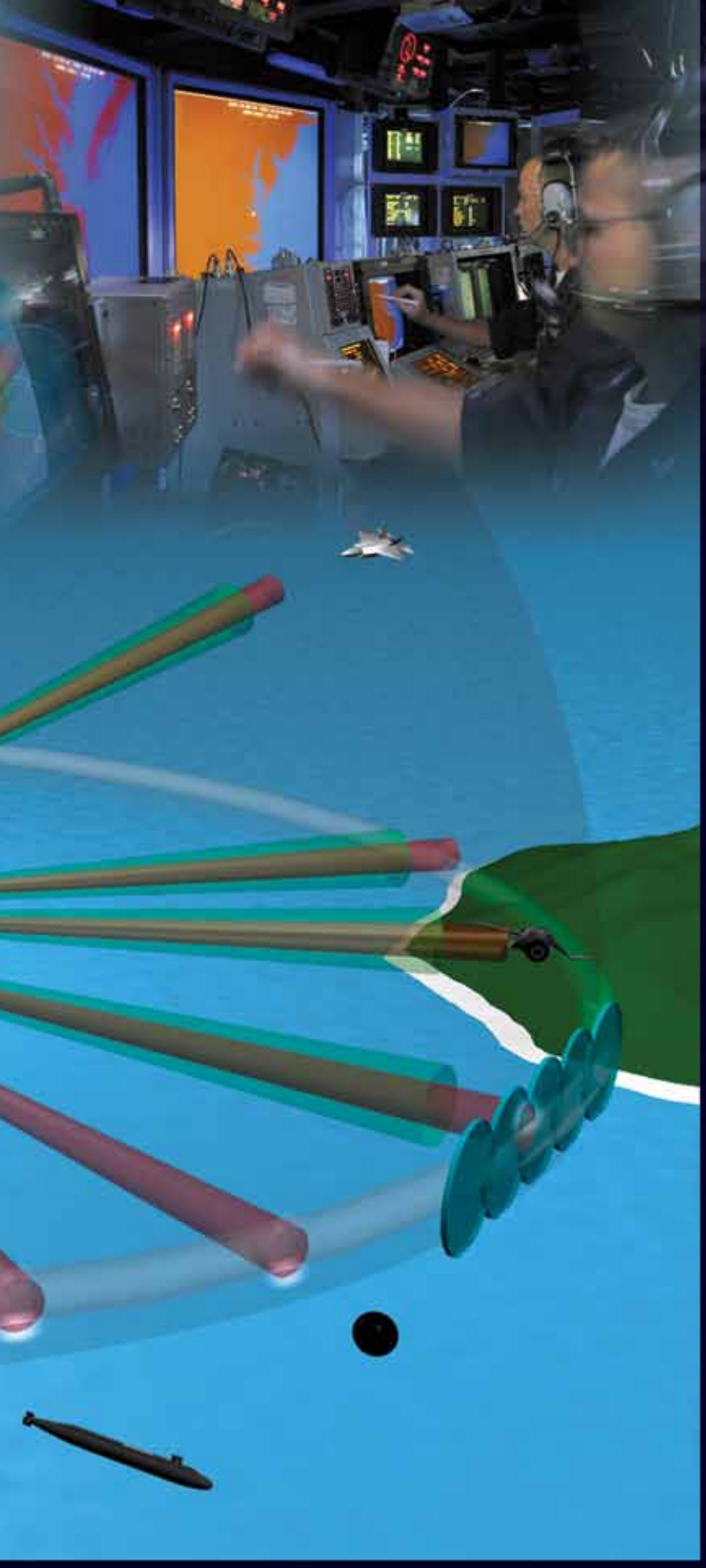
# Dual-Band Radar Development: From Engineering Design to Production

*By Alan L. Tolley and John E. Ball*







## Overview

The Dual-Band Radar (DBR) Suite is a U.S. Navy program. The suite consists of two radars integrated with a common controller and single interface to the combat system. The DBR radar acts according to combat-system-supplied doctrine, which effectively removes the need for an operator to run the radar, look at a radar display, and make tactical decisions. The radar not only provides fast reaction times, but also removes much of the potential for operator error in threat response.

The radars operate at X-band and S-band, and utilize active array technology, a first for the U.S. surface Navy. The DBR is scheduled for Initial Operational Capability (IOC) in 2014 aboard DDG 1000. The DBR will also be installed aboard USS *Gerald R. Ford* (CVN 78), the lead ship of the CVN 21 program. The DBR program started in 1999 with a contract award for the AN/SPY-3 Multifunction Radar (X-band) to Raytheon. Raytheon recently installed engineering development models (EDMs) of both the X-band and the S-band radars at the DDG 1000 Wallops Island Engineering Test Center (WIETC). Testing on AN/SPY-3 and the S-band Volume Search Radar (VSR) is currently underway. This paper summarizes the effort of transitioning from engineering design to production, discusses the upcoming combat-system integration challenges, and highlights the advantages of the integrated DBR system to the Navy.

## System Architecture and Description

The DBR suite is composed of two radars: the AN/SPY-3 Multifunction Radar (an X-band radar) and the VSR (an S-band radar) and contains a central resource manager for both radars. The DBR is connected to the combat system via a single interface. A block diagram of the DBR system is shown in Figure 1. The AN/SPY-3 primarily focuses on horizon search, low-altitude tracking, and missile support (illumination, uplink, and downlink), while the VSR is primarily responsible for volume search and tracking.

The design goals of DBR are to:

- Operate in harsh littoral environments, which often include potentially high-clutter areas, as well as land-based jamming
- Provide automated ship self-defense capabilities against air and surface targets, including low-flying missiles
- Provide robust multimission radar
- Provide advanced electronic protection (EP) capabilities

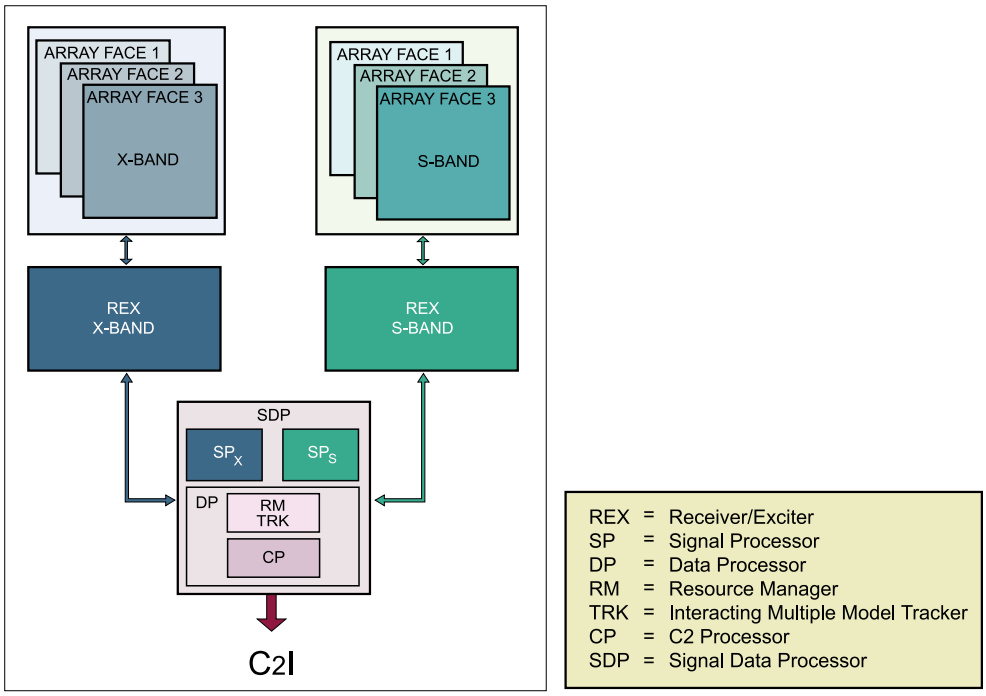



**Figure 1.** DBR Block Diagram

The AN/SPY-3 consists of three active arrays and the Receiver/Exciter (REX) cabinets above-decks and the Signal and Data Processor (SDP) subsystem below-decks. The VSR has a similar architecture, with the beamforming and narrowband down-conversion functionality occurring in two additional cabinets per array. A central controller (the resource manager) resides in the Data Processor (DP). The DBR is the first radar system that uses a central controller and two active-array radars operating at different frequencies.[1]

The DBR gets its power from the Common Array Power System (CAPS), which comprises Power Conversion Units (PCUs) and Power Distribution Units (PDUs). The DBR is cooled via a closed-loop cooling system called the Common Array Cooling System (CACS). The power and cooling systems are not shown in Figure 1.

The X-band has, in general, favorable low-altitude propagation characteristics, which readily support the horizon search functionality of the AN/SPY-3. A large operating bandwidth is required to mitigate large propagation variations due to meteorological conditions (i.e., evaporative ducting). The X-band arrays are smaller and lighter than the S-band arrays. This allows the X-band radar to be positioned higher, which results in improved performance in low-flyer detection and tracking.[2] The VSR provides a high-power-aperture product (the power-aperture product is a figure of merit of radar systems, the product of the total average radar transmitted power and the antenna area), and sufficiently small beam widths to support accurate target tracking. The VSR's primary role is to perform the volume search function.

The AN/SPY-3 and the VSR are both advanced, solid-state, active phased-array radars. Solid-state arrays offer several advantages:

- Lower transmit and receive losses relative to passive arrays
- Higher operational availability
- Graceful transmit degradation versus a single transmitter system[2]

The REX consists of a digital and an analog portion. The digital portion of the REX provides system-level timing and control. The analog portion contains the exciter and the receiver. The exciter is a low-amplitude and phase noise system that uses direct frequency synthesis. The radar's noise characteristics support the high clutter cancellation requirements required in the broad range of maritime operating environments that DBR will likely encounter. The direct frequency synthesis allows a wide range of pulse repetition frequencies, pulse widths, and modulation schemes to be created. The receiver has high dynamic range to support high clutter levels caused by close returns from range-ambiguous Doppler

waveforms. The receiver has both narrowband and wideband channels, as well as multichannel capabilities to support monopulse processing and sidelobe blanking. The receiver generates digital data and sends the data to the signal processors.

The DBR uses IBM commercial off-the-shelf (COTS) supercomputers to provide control and signal processing. DBR is the first radar system to use COTS systems to perform the signal processing. Using COTS systems reduces development costs and increases system reliability and maintainability. Referencing Figure 1, the high-performance COTS servers perform signal analysis using radar and digital signal-processing techniques, including channel equalization, clutter filtering, Doppler processing, impulse editing, and implementation of a variety of advanced electronic protect algorithms. The IBM supercomputers are installed in cabinets that provide shock and vibration isolation. The DP contains the resource manager, the tracker, and the command and control processor, which processes commands from the combat system.

The DBR utilizes a multitier, dual-band tracker, which consists of a local X-band tracker, a local S-band tracker, and a central tracker. The central tracker merges the local tracker data together and directs the individual-band trackers' updates. The X-band tracker is optimized for low latency to support its mission of providing defense against fast, low-flying missiles, while the VSR tracker is optimized for throughput due to the large-volume search area coverage requirements.

The combat system develops doctrine based on the current tactical situation and sends the doctrine to the DBR. The combat system also has control of which modes the radar will perform. Unlike previous-generation radars, the DBR does not require an operator and has no manned display consoles. The system uses information about the current environment and doctrine from the combat system to make automated decisions, not only reducing reaction times, but also reducing the risks associated with human error. The only human interaction is for maintenance and repair activities.

The DBR supports the modes of operation as shown in Figure 2. The primary modes for AN/SPY-3 are horizon search/track while scan, surface search/navigation, periscope detection and discrimination, and environmental mapping. During engagements, AN/SPY-3 also performs precision

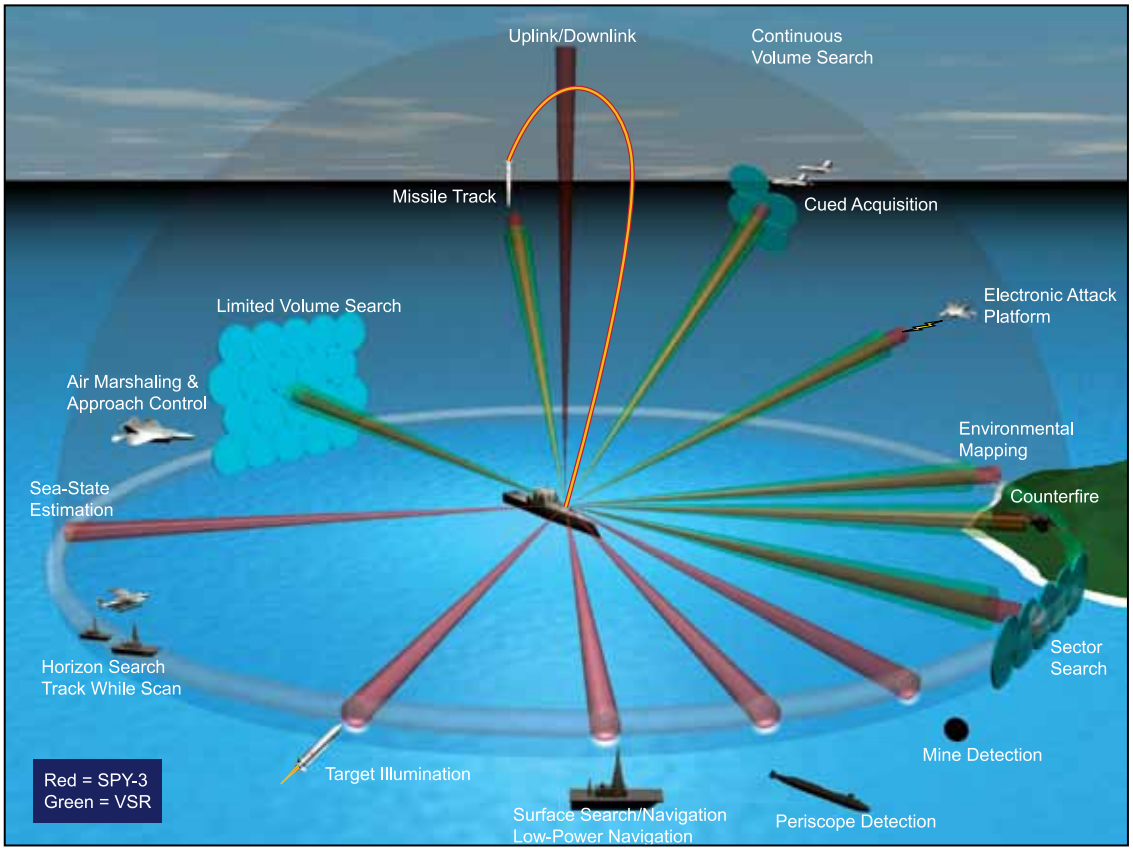



**Figure 2.** DBR Operating Modes

tracking, ownship missile tracking, missile communications, and target illumination. The primary mode of operation for VSR is continuous volume search, precision tracking, and environmental mapping. Several modes can be performed by either band as directed by the resource manager, such as limited volume search, precision tracking, or cued acquisition. This allows the radar flexibility if one of the bands is taxed due to other modes being performed, such as when the AN/SPY-3 is performing illuminations.

Previously, the Navy utilized separate radar systems for air traffic control (ATC), target illumination, target tracking, surface search and navigation, missile tracking, and environmental mapping. The DBR suite integrates these functions into one system, providing a robust and effective solution for the Navy. An integrated system has several advantages over a collection of separate systems—lower cost, lower weight, lower ship space required, and most importantly, less manning is required.

## Engineering Development Model (EDM) Integration & Test

The DBR integration and test effort has been separated into two parallel efforts. The first effort focuses solely on AN/SPY-3, whose development started much earlier than VSR. The second effort focuses solely on integrating VSR. Both systems continue to be integrated and tested separately at Wallops Island until late 2009, when both systems will be integrated to form the DBR.

### *AN/SPY-3 Integration and Test*

This section discusses the integration and testing at Wallops Island on the Self-Defense Test Ship (SDTS), and at the Surface Warfare Engineering Facility (SWEF).

### *Wallops Island Land-Based Testing*

The AN/SPY-3 Development Contract, awarded to Raytheon in 1999, produced an EDM that was installed at Wallops Island, Virginia, in 2003. This installation is shown in Figure 3. At this location, the AN/SPY-3 EDM System was integrated, and full-power radiation was achieved for the first time. Previous subsystem integration activities were limited to single-element radiation inside a near-field range. As the system matured, the effort transitioned from a hardware verification activity to a system functionality test program, which specifically focused on the Air Search and Track functionality. The test program adopted an incremental strategy that began with tracking low-cost targets (e.g., Learjets) and culminated with testing against target drones.

### *Self-Defense Test Ship (SDTS) Testing*

After completing the land-based testing in 2005, the AN/SPY-3 system was shipped to Port Hueneme, California, to be installed upon the SDTS, the decommissioned USS *Paul F. Foster* (DD 964). Figure 4 shows the SDTS and identifies the location of the AN/SPY-3 radar on the ship. The test objectives remained similar, but these tests were conducted in an operational environment with ship-motion and land-clutter backgrounds. The AN/SPY-3 completed its testing program in 2006 but remained on the SDTS until 2008 to observe Ship Self-Defense System (SSDS) testing. The testing, completed while installed on the SDTS, was essential to production decisions and gave insight into the operational environment.

### *VSR Integration & Test*

The VSR development produced an EDM that was installed in the SWEF located at Port Hueneme, California, in 2007. This installation is shown in Figure 5. This test period focused on hardware characterization, including measurements of Effective Isotropically Radiated Power (EIRP) and system stability. (EIRP is a figure of merit for antenna systems and is a way to compare the radiated power of antennas.) In 2008, the system was shipped to Wallops Island, Virginia, to be installed in the WIETC, shown in Figure 6.

**Figure 3.** AN/SPY-3 Wallops Island Installation


**Figure 4.** AN/SPY-3 Self-Defense Test Ship Installation


**Figure 5.** VSR Surface Warfare Engineering Facility Installation

**Figure 6.** Dual-Band Radar Wallops Island Engineering Test Center Installation

## Platform Integration

The DBR is being integrated into both the *Zumwalt*-class destroyer and the *Ford*-class aircraft carrier. Each platform introduces its own set of design considerations, which range from prime power type to sensor priority differences. The examples listed in this section are not intended to be complete; they represent only a sampling of the platform design considerations for both *Zumwalt* and *Ford*.

### *DDG 1000* Zumwalt-*Class Destroyer*

The physical arrangement of the sensors in the *Zumwalt* deckhouse is illustrated in Figure 7. To accommodate integration into the *Zumwalt* class, the DBR design has been uniquely influenced in the areas of prime power type, array structure, and VSR radome design. With the introduction of the Integrated Power System (IPS) for *Zumwalt*, the 440-VAC EDM design was changed to accommodate the ship-power-supplied 4160 VAC. The CAPS design is being updated to accommodate the voltage change.

### *CVN 78* Gerald R. Ford-*Class Aircraft Carrier*

The physical arrangements of the sensors in the *Ford*-class island are illustrated in Figure 8. To accommodate integration into *Ford* class, the DBR design has been uniquely influenced in the areas of prime power type and sensor priorities. Similar to the design changes in *Zumwalt*, *Ford* class will supply CAPS with 13.8 kVAC. Design updates to CAPS are in process to accommodate this change.

In addition to being the primary antiair warfare (AAW) sensor for the *Ford* class, DBR is also the primary ATC sensor. To accommodate this added functionality, DBR has added a short-range search fence to the baseline functionality set that runs concurrently with other functionalities, such as long-range volume search and track, horizon search and track, etc. To date, the combat system and ATC mission areas have had dedicated sensors on aircraft carrier platforms. The concept of sharing the DBR across mission areas is a new concept and requires careful consideration of how the system is integrated.

## Future Challenges

In order to successfully deliver the DBR to the fleet, a number of activities will be accomplished over the next several years, including the completion of the radar integration and test program. Results from testing to date—along with

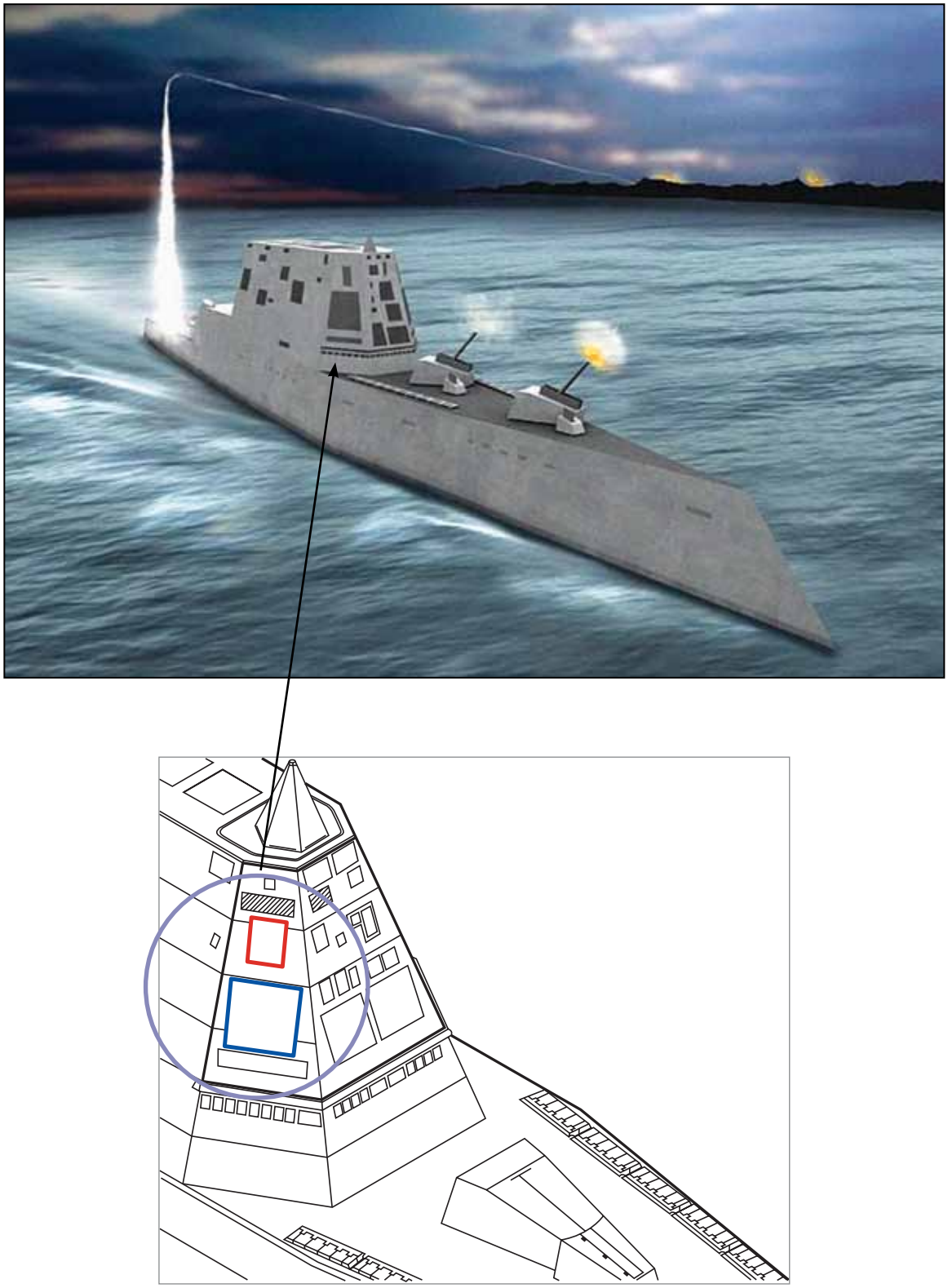


**Figure 7.** DDG 1000 USS *Zumwalt* DBR Installation Drawing—AN/SPY-3 is shown in red, and VSR is shown in blue.

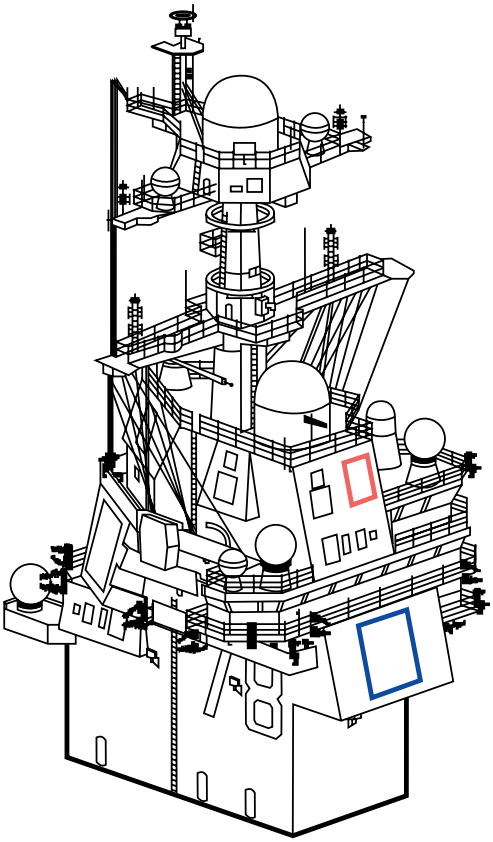


**Figure 8.** CVN 78 DBR Installation Drawing—AN/SPY-3 is shown in red, and VSR is shown in blue.

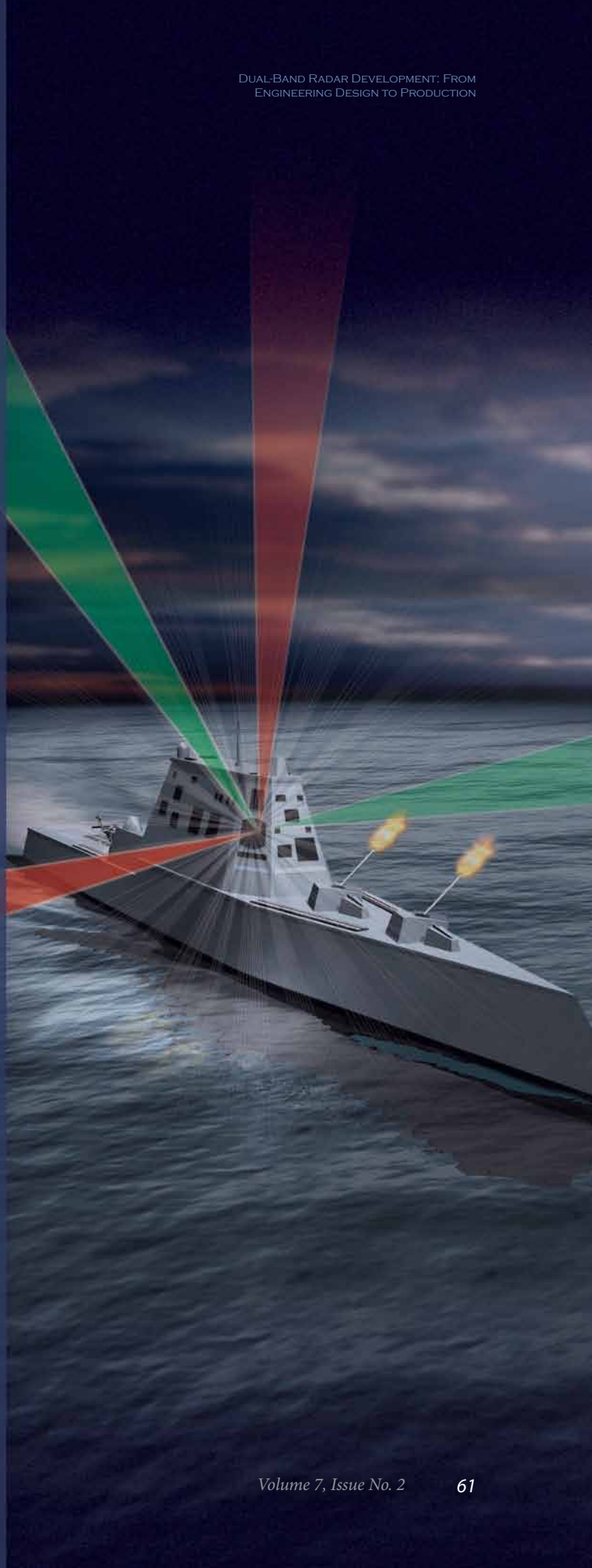
cost reduction, risk mitigation, and production activities—have been incorporated into the production designs. The DBR has entered the beginning stages of production, and the challenges of producing units in sufficient quantity will continue as this transition from prototype to production occurs. Combat-system integration activity for both *Zumwalt* and *Ford* class is a significant future activity. The combat-system integration activity will not be limited to connectivity of the system but to also collaboratively work with the combat system(s) to ensure that the advanced capability introduced by DBR is fully integrated into the combat system.

## Conclusions

The DBR is a highly integrated system, providing the Navy with a powerful volume and surface-search radar system. The DBR is the first radar to use COTS supercomputers to perform signal-processing functions, providing a cost-effective, robust solution. The DBR is also the first dual-band, active-array radar suite with a central controller, providing advanced capabilities and flexibility to the Navy. The DBR acts automatically using combat-system-supplied doctrine, and DBR does not need a dedicated operator. This system reduces system-level reaction times and removes much of the potential for operator error in threat response, compared to previously fielded Navy radar systems. This results in reduced operating costs and fewer chances for human error. The DBR is designed with graceful degradation wherever possible, providing both reduced operating costs and a robust system for the Navy. The MFR and VSR radars are currently being tested, and integration with the combat systems is planned in the future.

## References

1. DDG 1000 Dual-Band Radar (DBR), Raytheon Company, 30 Aug 2005.
2. Fontana, W. J., and K. H. Krueger, "AN/SPY-3: The Navy's Next-Generation Force Protection Radar System," *Proceedings of the 2003 IEEE International Symposium on Phased Array Systems and Technology*, pp. 594–603, 14–17 Oct 2003.



# International Treaty Verification: Cobra Judy Replacement Program

*By Penny Moran and Chris Reasonover*

**Figure 1.** Cobra Judy Aboard USNS *Observation Island*

The Cobra Judy radar system provides long-dwell, foreign ballistic-missile data collection in support of international treaty verification. Cobra Judy, aboard U.S. naval ship (USNS) *Observation Island* (shown in Figure 1), has been in service for many years, with the ship now over 56 years old. Consequently, both the system and the ship are in need of replacement.

*Cobra Judy Phased Array Radar*

The Cobra Judy Replacement (CJR) Program includes the design, development, and acquisition of a functional replacement ship and mission equipment (ME) suite for the current Cobra Judy and USNS *Observation Island*. The CJR's treaty verification mission will remain the same as the system it replaces, and it will continue to provide worldwide, high-quality, high-resolution, multiwavelength radar data. The systems aboard the replacement ship will include high-power, instrumentation-class, X-band and S-band phased-array radars and the necessary ancillary equipment to support the mission. A close-up of Cobra Judy S-band phased array and X-band dish antenna is shown in Figure 2. The X-band radar and its antenna dimensions are shown in Figure 3, with the array halves being test-fit for the X-band array shown in Figure 4.

Both the X-band and S-band radars will employ a variety of waveforms and bandwidths to provide operational flexibility and high-quality data collection. The X-band radar will provide very high-resolution data on particular objects of interest, while the S-band radar will serve as the primary search-and-acquisition sensor and will be capable of tracking and collecting data on a large number of objects in a multitarget complex. The S-band antenna dimensions are shown in Figure 5, with an overall size very similar to the X-band antenna.

A common back end (CBE) will handle all controls and signal processing for both X- and S-band arrays. The CBE includes:

- Displays
- Processing Software and Equipment
- Communication Suite
- Weather Equipment

**Figure 2.** Close-Up of Cobra Judy S-Band Phased Array and X-Band Dish Antenna

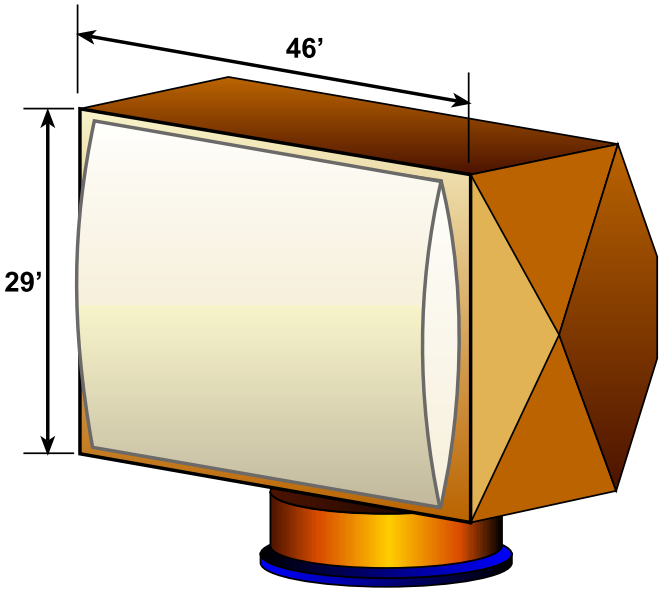



**Figure 3.** X-Band Antenna


**Figure 4.** Test-Fit for Upper and Lower Halves of the X-Band Array

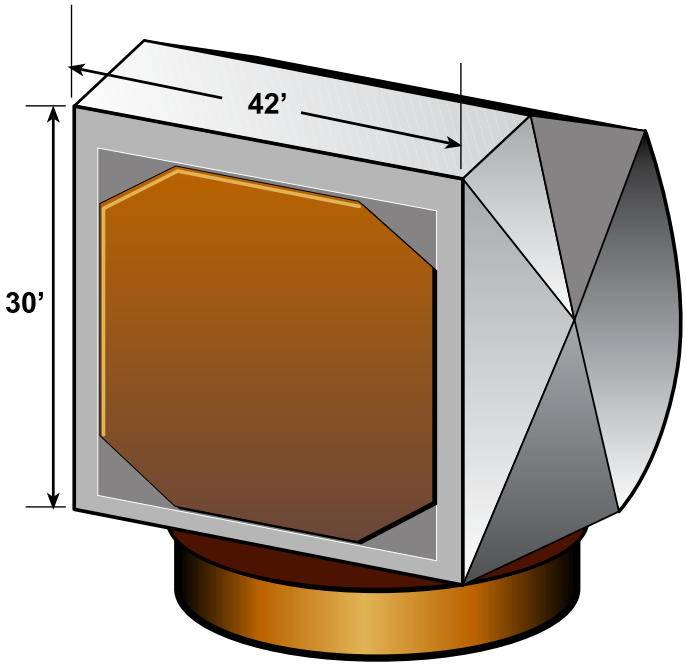



**Figure 5.** S-Band Antenna

Centralizing the software and processing equipment maximizes code reuse between the two radars and reduces overall cost for the system. Many of the CBE components are designed to be common, modular, and open between the two radars. The CBE will also be equipped with various simulation and test modes to support maintenance and training. The CBE is depicted in Figure 6.

Raytheon Integrated Defense Systems (Raytheon IDS) is developing the X-band radar and CBE ME, with Northrop Grumman Electronic Systems (as a directed subcontractor) developing the S-band antenna, pedestal, and antenna servo control system. The CJR ME suite will be installed on a T-AGM 25 platform specially outfitted for the mission, as shown in the artist's concept in Figure 7. The ship is being constructed by VT Halter Marine in Pascagoula, Mississippi. When ship construction is complete, it will move to Ingleside, Texas, for installation of ME, including the heavy-lift operations of installing the pedestals and arrays. Like the current USNS *Observation Island*, the new ship—recently named USNS *Howard O. Lorenzen*—will be a white-hull, noncombatant. CJR's initial operational capability (IOC) is set for 31 December 2012.

Engineers at the Naval Surface Warfare Center (NSWC) Dahlgren helped to lead design efforts and continue to support development and testing by leveraging core technical capabilities in:

- Requirements Development and Validation
- Systems Engineering
- Software Development
- Safety and Environmental
- Electromagnetic Interference / Electromagnetic Compatibility (EMI/EMC)
- Human-Systems Integration (HSI)

Requirements development included managing a diverse technical team made up of both government and contracted engineering-support personnel, while requirements validation was realized through in-house modeling and simulation (M&S). These and other efforts included both direct program office leadership roles and specialized engineering support at the working level.

Recognized for its rigorous radar systems engineering, NSWC Dahlgren was appointed as the lead or deputy in several of the program office's integrated product teams (IPT) from the program's start. As the X-band IPT lead, NSWC Dahlgren was responsible for developing key requirements, monitoring functional requirement allocations, and maintaining oversight through design and manufacturing. NSWC Dahlgren also supported the S-band IPT as deputy lead and developed many of its key requirements. Both IPTs leveraged NSWC Dahlgren's expertise in radio frequency (RF) propagation to develop operational performance requirements for both radars under a range of environmental conditions.

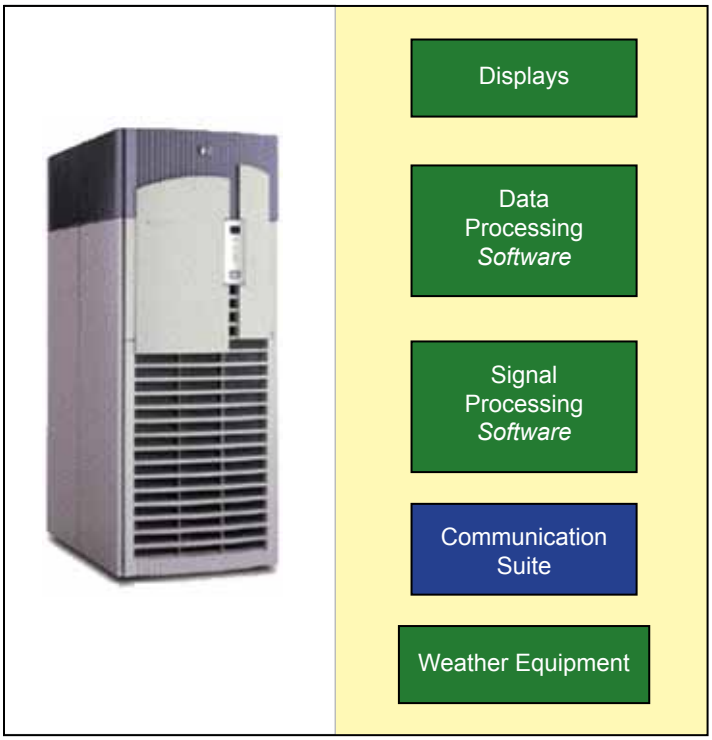



**Figure 6.** Common Back End (CBE)

As the CBE IPT lead, NSWC Dahlgren led and continues to oversee development of the software that will integrate the X- and S-band radars. Early in the program, NSWC Dahlgren engineers maintained a constant presence at Raytheon IDS to participate in the software development process and to collect metrics for the program office. This allowed for early detection, reporting, and resolution of software development issues. NSWC Dahlgren also led the CJR Operations IPT. This role required frequent site visits to all subcontractors to witness manufacturing and developmental testing of the ME, which included construction and factory acceptance testing of the antenna pedestal, antenna backstructure, X-band array plates, cooling equipment, and power equipment.

NSWC Dahlgren further served as the deputy lead in the Integration and Test IPTs and continues to serve as deputy lead for integration. As the Test IPT deputy, NSWC Dahlgren reviewed test plans and procedures, witnessed factory acceptance and specification sell-off testing, and interfaced with both the Navy and Air Force operational test agencies to write the Test

**Figure 7.** Artist's Concept for USNS *Howard O. Lorenzen*

and Evaluation Master Plan (TEMP), further coordinating approval through the Navy, Air Force, and Office of the Secretary of Defense (OSD). The Test IPT deputy also chaired the M&S accreditation board, which imposed a rigorous verification, validation, and accreditation (VV&A) process to prime contractor-proposed models to be used for final requirements sell-off. As the Integration IPT deputy, NSWC Dahlgren served as the government liaison between the program office and Raytheon IDS to coordinate witnessing of developmental tests in support of requirement sell-off and to maintain sell-off evidence for government acceptance. NSWC Dahlgren engineers also developed the sign-off process for the program office.

NSWC Dahlgren additionally served the CJR program office in a number of unique and important areas outside of the IPT lead and deputy roles. Early in the program, NSWC Dahlgren served as a liaison between ME and ship requirements development, subsequently participating in the ship source selection process as the program office's representative and ME expert. NSWC Dahlgren was also a major contributor to the milestone B/C documents, such as the acquisition plan, acquisition strategy, integrated logistics support plan, systems engineering plan, and the TEMP. In addition, NSWC Dahlgren engineers drafted the initial security class guide for the program office and participated in the final contract negotiation with Raytheon IDS.

Other engineering support included the CJR Principal For Safety (PFS), environmental compliance analysis, EMI/EMC studies, and HSI reviews. As PFS, NSWC Dahlgren served as the CJR Program liaison to the Weapon System Explosives Safety Review Board (WSESRB). Once the PFS role was completed, NSWC Dahlgren continued as the lead for safety on the program. NSWC Dahlgren also performed analyses to confirm CJR's compliance with international pollution control standards. One goal of these analyses was to verify the ME's ability to endure the corrosive environment produced by a maritime environment and ship stack gases. NSWC Dahlgren was also responsible for all EMI/EMC topside studies. The EMI/EMC study included analysis to minimize co-site interference between the two radars and the between the radars and communications suite, as well as the ship's navigation and safety systems. This analysis included investigation and mitigation of potential issues with off-board RF emitters. Furthermore, NSWC Dahlgren was, and continues to be, the lead for dealing with domestic and international frequency spectrum management among CJR, the operational Navy, and all other potential sources of interference.

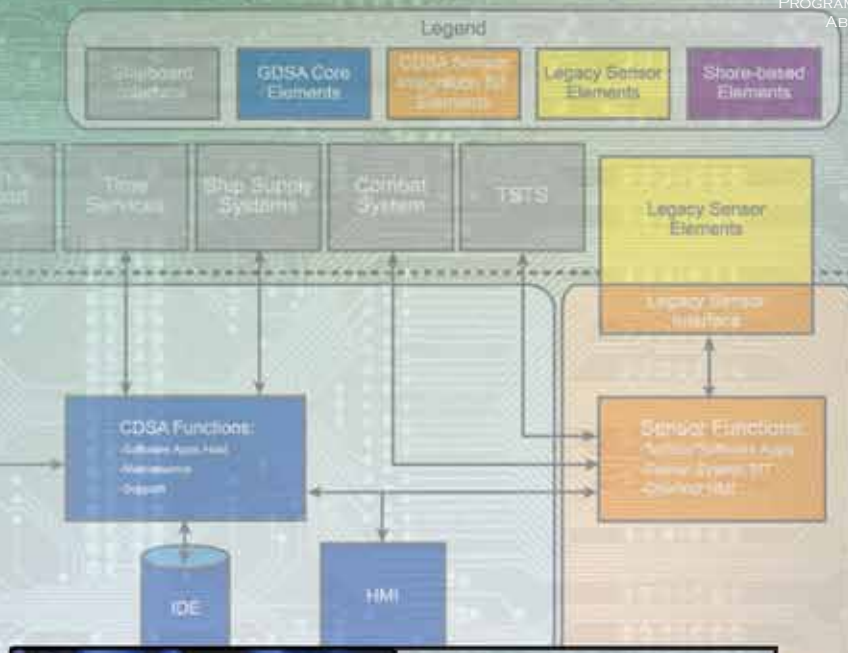
One of NSWC Dahlgren's more critical engineering support roles is to serve as the government clearinghouse for all CJR contract deliverables and working documents by hosting both unclassified and classified websites. These websites enable document and data sharing day and night across multiple sites, thereby facilitating the timely turnaround of documents, comments, and analysis products. These websites additionally provide a common, controlled document repository for all CJR data supporting government and industry.

In replacing the aging Cobra Judy and USNS *Observation Island*, the Navy, NSWC Dahlgren, and the Air Force are ensuring that CJR will succeed in performing the critical mission of international treaty verification over the coming decades.

*Cobra Judy Phased Array Radar*

# Program Executive Office Integrated Warfare Systems Above Water Sensor Directorate Common Digital Sensor Architecture Design Initiatives

*By John Schofield*


Legend
GDSA Core Elements
Legacy Sensor Elements
Shore-based Elements
Time Services
Ship Supply Systems
Combat System
TSTS
Legacy Sensor Elements
CDSA Functions:
Sensor Functions:
IDE
HMI



The Program Executive Office Integrated Warfare System above Water Sensor Directorate (PEO IWS 2.0) initiated the Common Digital Sensor Architecture (CDSA) project to address long-term reliability, maintainability, and availability (RMA) issues associated with deployed above-water sensors caused by systemic obsolescence. The Naval Surface Warfare Center (NSWC) Crane Division was tasked by PEO IWS 2.0 to lead the CDSA project to assist with the alignment of sensor support solutions and the development of the support infrastructure to achieve and sustain operational effectiveness of sensor systems. Through the successful implementation of the CDSA effort, PEO IWS 2.0 is providing a means to eliminate sensor-unique reengineering efforts; provide stability for out-year funding requirements; and consolidate contracts, engineering, and support efforts.

The CDSA project is divided into three primary efforts: CDSA Core, Shore-Based Product Data Management (PDM), and a CDSA Sensor Integration Kit. The CDSA functional block diagram, contained in Figure 1, illustrates the interaction of CDSA functional elements.

The CDSA Core comprises common shipboard elements consisting of human-machine interface (HMI), maintenance and support functions, an integrated data environment (IDE), a sensor tactical host function, and standardized interfaces. The CDSA Core provides a common sensor look, touch, and feel, while eliminating processes that drive knowledge and skill requirements. Additionally, the CDSA Core automates the maintenance and supply support process; integrates technical and support data to eliminate advanced training requirements; captures accurate RMA sensor data; and provides a common development platform, enabling a reduction to manpower, personnel, and training costs. A common architecture and accurate RMA data enable the Navy support community to effectively implement and manage a support strategy to achieve and sustain operational effectiveness objectives.

The Shore-Based PDM provides the capability to collect, process, and manage all relevant system

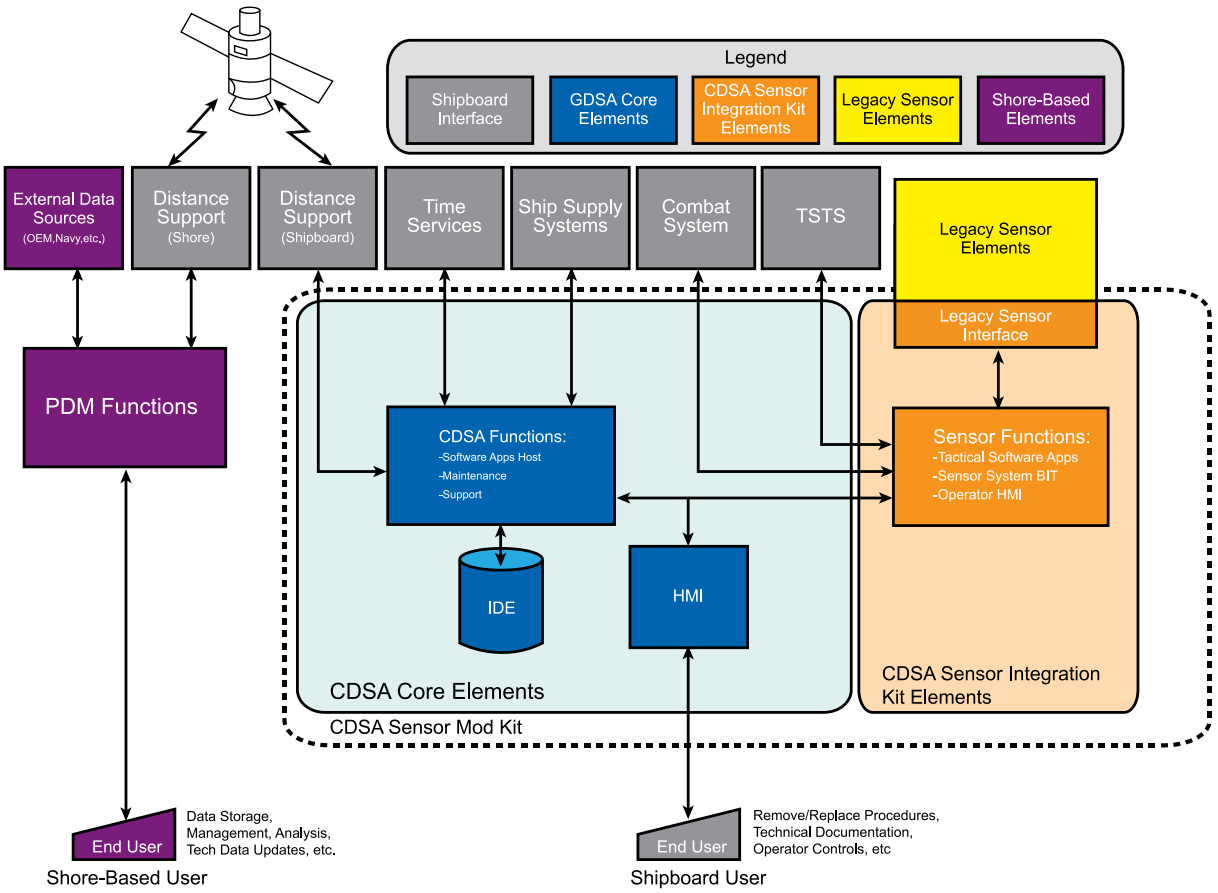



**Figure 1.** Common Digital Sensor Architecture Functional Block Diagram

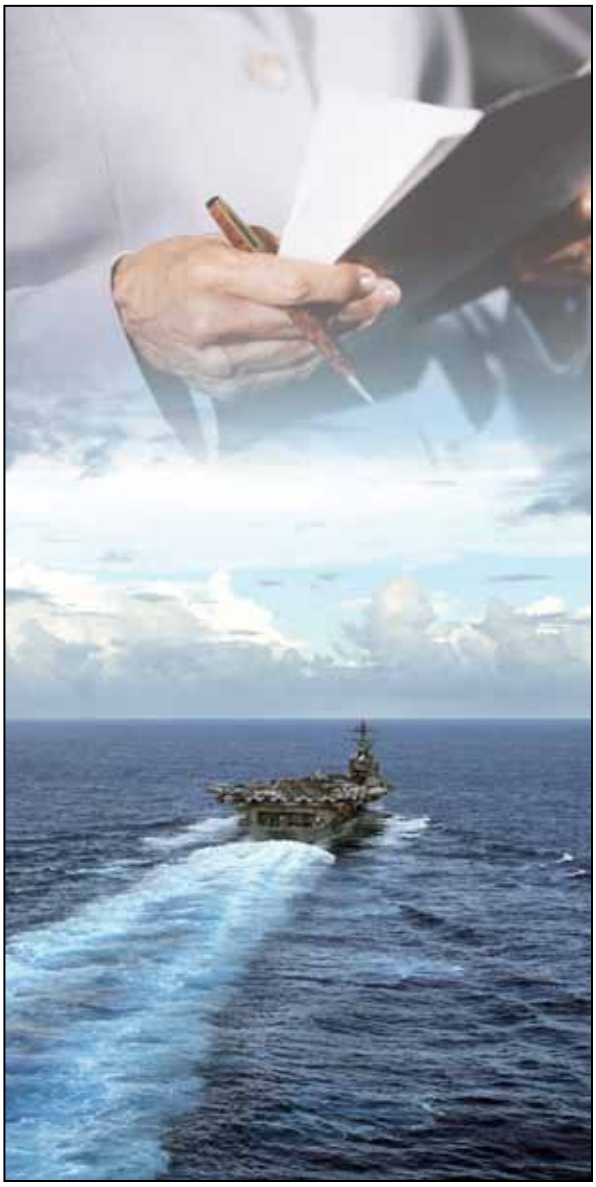
data required to implement an effective sustainment strategy across all designated Above-Water Sensors' life cycles. The PDM also provides the capability to synchronize and extract data from ship to shore through utilization of existing Navy Distance Support architecture.

The Sensor Integration Kit includes the hardware and software components required to integrate the CDSA Core into the sensor system. The integration of CDSA transitions sensor applications' execution to general-purpose processors, and introduces and expands full system built-in-test and built-in-measurement designs to achieve sensor supportability requirements.

The CDSA design effort establishes a common modular architecture using Navy Open Architecture guidelines, standardized interfaces, and common hardware. The alignment of technical architectures across sensor systems enables synchronization of efforts across sensor systems. The development of portable sensor applications reduces the risk of technology refresh and technology insertion in the out years. In addition, the CDSA design effort reduces system maintenance requirements, required shipboard technical skills, and workload requirements. Maintenance requirements are reduced by expanding the sensor self-monitoring capability by embedding all required technical information into the system and by providing a design solution that eliminates the requirements for pipeline training, technical training equipment, and technical manuals. The ultimate goal is to design the CDSA such that an apprentice-level technician can maintain the system. This would enable the same technician to maintain multiple sensor systems.

Another objective of the CDSA project is to establish a common set of support measures of effectiveness (operational availability, ownership cost) and then manage logistics support to these measures in an IDE, which is critical to providing a common life-cycle support strategy. Visibility into sensor systems to accurately report and assess RMA of the system is critical in meeting fleet requirements and in addressing and sustaining fleet needs. Standardization and the accessibility of accurate data is the key enabler. Not only does standardization and accessibility of sensor data allow for a network of integrated sensors, it also provides visibility to assess the effectiveness of the support solution.

In summary, to PEO IWS 2.0, CDSA provides a common core capability supporting improved operability and maintainability, as well as providing accurate RMA data to monitor sensor support solutions. This approach provides continuous visibility into the system to identify where program resources should be invested. For the fleet, CDSA provides an integrated support solution that sustains operational availability within affordable cost. For the technical community, CDSA provides a modular software-centric and net-centric system to act as a transition platform for technology. For the supply support community, CDSA provides RMA data to perform supply chain management to ensure that support strategy sustains system operational availability at cost.




# International Programs

*By Michael Madatic*

Entering the 21st century, the U.S. has come to deal with the reorganization of Russia and the growth of China, as well as smaller rogue states. As part of an active foreign policy, the Navy has pursued international cooperative efforts to meet shared maritime interests. The Naval Surface Warfare Center (NSWC) Dahlgren has been committed to advancing radar projects both within the Department of Defense (DoD) and alongside allied nations over the last several years. And like the U.S. Navy, navies of the U.K. and Australia are fielding advanced active phased array radars.

## U.K./U.S. Advanced Radar Technology Integrated System Test Bed (ARTIST)

The U.S. and U.K. are cooperatively conducting research and development of advanced maritime active phased array radars to support future maritime radars or upgrades to existing systems. Specifically, the U.S. and U.K. are developing and testing two advanced phased array radar demonstrators under the ARTIST program. Technologies to be applied include adaptive active digital array, signal-processing, digital beamforming, high-range resolution integration techniques, and radar controls. Testing will begin in the spring of 2010 at Wallops Island, Virginia.

The U.K. has invested heavily in the development of digital array architecture (i.e., analog-to-digital conversion), as well as digital beamforming techniques through critical experiments and algorithm development over the past 20 years. These technologies included the construction of an active S-band radar demonstrator and corresponding radar controls, including the advanced signal-processing and beamforming techniques. These developments were initially conducted by the U.K. under the Multifunctional Electronically Scanned Adaptive Radar (MESAR) I and II programs. By establishing a cooperative program with the U.K., an existing and proven technology can be expanded upon by the U.S. Navy for the development of next-generation radars.

U.S./U.K. ARTIST cooperation provides risk reduction and facilitates the potential use by the U.S. of advanced digital phased array developments for air and missile defense radars. The ARTIST program also provides risk reduction to the U.K. development of the SAMPSON radar. The technologies being developed under the ARTIST program, when combined, will provide a vast improvement to today's sea-based radar systems. A depiction of the SAMPSON Radar is shown in Figure 1.

Benefits from these bilateral cooperative efforts are many and include:

**Figure 1.** Sampson Radar

- The incorporation of the U.K.'s technological resources (industry/laboratories) and cost sharing of technology maturation are common to both nations.
- Advanced U.K. digital radar technology permits optimization of U.S.-developed high-powered phased array radar.
- The U.K. contribution will provide enhanced and specialized digital adaptive beamforming, thereby reducing the U.S. investment required to fulfill U.S. Navy requirements.
- The output of this cooperative research and development effort represents a quantum increase in adaptive nulling, clutter rejection, and sidelobe cancellation capability over current U.S. analog-based radars.
- The program's resulting critical technologies can be matured in the near term and introduced into new radar designs or as an upgrade backfit to existing radars.
- Cooperation accelerates development schedules while providing significant cost avoidance through cross-capture of complementary and previously completed nonrecurring engineering.

British Aerospace Systems, Qinetiq, and Roke Manor Research are developing the U.K. version of the ARTIST test bed. Lockheed Martin is developing the U.S. version of the ARTIST test bed (see Figure 2). Roke Manor (U.K.) is also a key partner contributing to the development of a distributed receiver (see Figure 3), while BAE is providing the narrow-band, medium-band exciter to the U.S. ARTIST.

## Australia/U.S. Phased Array Radar (AU.S.PAR)

In the late 1990s, the Royal Australian Navy (RAN) invested in the development of a solid-state radar system for potential application as a midlife upgrade to the Australian Navy's ANZAC-class ships. This Australian radar development and demonstration effort, termed CEAFAR, was of interest to the U.S. since the resulting radar was one of the first fully functioning S-band solid-state radars in the world. The specific radar that the Australians developed was an engineering development model (EDM) containing two faces of a planned six-face system and low-power transmit/receive (T/R) modules. The Australian EDM system was installed on a RAN ship and completed a very successful at-sea test program. Since the completion of the at-sea test demonstration, the RAN

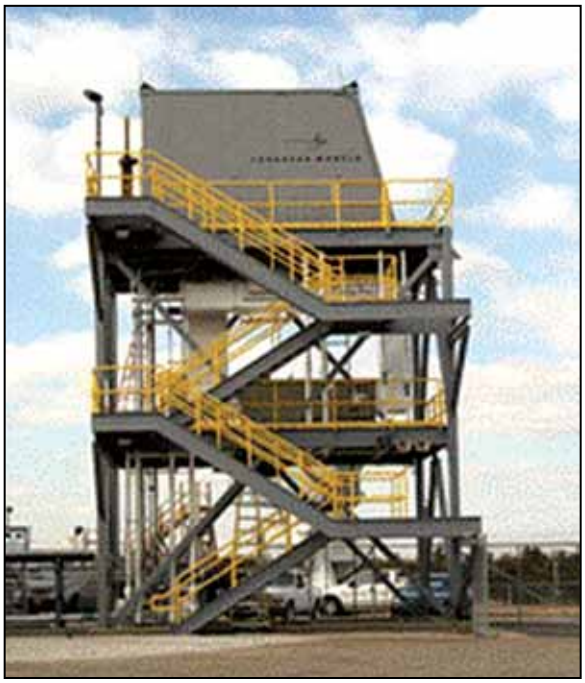


**Figure 2.** Lockheed Martin ARTIST Test Bed

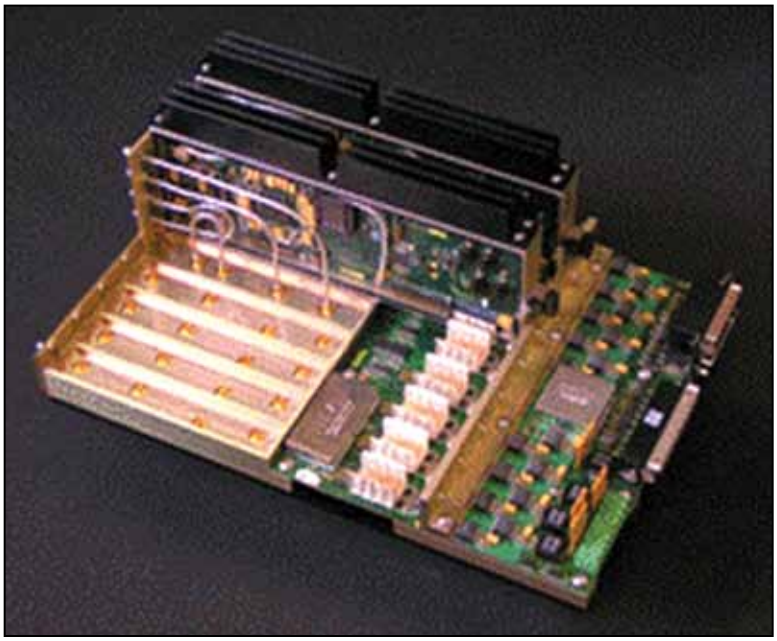


**Figure 3.** Roke Manor Receiver

approved the midlife upgrade to the ANZAC Class that included procurement of 10 CEAFAR systems from CEA Technologies, Pty, Ltd. A photo of CEAFAR is shown in Figure 4.

In March 2002, under the direction of John J. Young, Jr., then Assistant Secretary of the Navy for Research, Development, and Acquisition, PEO IWS 2.0 (Above-Water Sensors) sent a team of engineers and scientists to Australia to investigate the CEAFAR technology and consider the potential application to future U.S. radar developments. The U.S. team verified that the technology was innovative and realized that the Australian methods for development and manufacturing were very different than those employed by U.S. industries. The U.S. Navy quickly concluded that the U.S. could gain from cooperation with the Australian CEAFAR solid-state radar technology development.

Maritime solid-state radars are generally manufactured on a single faceplate. The single faceplate provides a very rigid structure to hold the radiating elements, with structure flatness requirements as small as 10 mils across the entire aperture. Each face of a solid-state radar typically has an off-array power system, receiving system, and a signal-processing system, all controlled with a digital computer.

In the case of CEAFAR, a process to segment the aperture was developed, allowing a radar to be built from small building blocks (about 12 inches by 12 inches) to the full size required. Each building block is called a tile. The tile includes the receive system and the signal-processing system. The unique Australian tile concept significantly simplifies the manufacturing process of the antenna.

The U.S. and Australian governments ratified the Australia–U.S. Phased Array Radar (AU.S.PAR) Project Arrangement (PA) in April 2005 to develop a medium-power and a high-power version of the tile concept. The high-power version was subsequently cancelled in 2007 due to poor power amplifier performance. The U.S. interests in the cooperative project are focused in five key technology areas for the medium-power project:

1. ***Segmented Aperture***—Understand the process involved in building a large array from small building blocks
2. ***Calibration Methodology***—Examine the process used to calibrate a segmented aperture.
3. ***Pulse-Modulated Power Supply***—Develop an efficient and inexpensive power supply to be used in the tile concept

**Figure 4.** CEA-FAR Onboard HMAS *Arunta*

4. ***Field-Programmable Gate Arrays (FPGA)-Based High Throughput Signal Processing***—Develop a field-programmable gate array base signal-processing system embedded in the tile.
5. ***Vector Modulator Beam Steering***—Develop a beam-steering capability based on vector modulators that allow steering during transmitted pulses.

The medium-power version of the tile concept commenced test in June 2006.

The Australian company, CEA Technologies, Pty, Ltd, is responsible for the development of all aspects of the AU.S.PAR project. Each of the key technology efforts identified above is jointly developed via cost sharing and is thus usable by both countries. There is no U.S. industry directly involved in the AU.S.PAR project; however, Northrop Grumman has invested heavily in CEA Technologies.

## International Program Transition

A key concern of international programs is the ability to transition individual developments into radar programs within each country. If a cooperative program produces a new design, develops a new algorithm, or improves the state of knowledge in a particular technology, it is important that these developments migrate to appropriate radar programs. For research-based projects that are risk-reduction efforts, it may well be concluded that the technology is not the right technology to be inserted into a subsequent development effort. This is also valid output from such projects.

For the ARTIST program, the transition path has already had some success in both the U.S. and the U.K. The U.K. continues with the required development for the SAMPSON radar. To a large degree, the digital technologies of the ARTIST program are already integrated with the SAMPSON radar. Within the U.S., the transition is much more subtle. Lockheed Martin is developing the midlife upgrade of the SPY-1 system and, as part of this design upgrade, the receiver components can be traced to the ARTIST program.

The AU.S.PAR program also has celebrated some success. The tile design and manufacturing process, as well as the associated calibration techniques, are a product of the CEAFAR program. The CEAFAR radar system is destined to be implemented in the midlife upgrade of the ANZAC destroyers. The U.S. has not yet transitioned the technology gains to date; however, each technology is undergoing evaluation for future new radar developments.

Clearly, warfighters representing allied countries benefit tremendously by participating in cooperative research and development programs. These navies benefit not only by having more powerful and more capable radar systems, but international compatibility and interoperability among these systems improves considerably as well.

# Rapid Prototyping of Radar Signal Processing

*By David Leas*

Military sensors employ signal processors to take raw information gathered by the sensors to produce data that can be used by warfighters to gain battlespace awareness. Signal-processing algorithms are typically mathematically intensive, and thus, are the most computationally challenging algorithms seen in military systems. Additionally, the quality of battlespace awareness achieved is often directly related to the complexity built into the signal processor.

Traditionally, the most demanding sensor signal-processing applications have been hosted in hardware-based processing systems. These hardware-based solutions were often constructed using application-specific integrated circuits (ASICs) that required a very high initial investment cost for nonrecurring engineering. This resulted in designs that were prone to obsolescence due to the limited availability of the components over the long life spans of the military system. Recently, the Navy has begun to use digital devices known as field-programmable gate arrays (FPGAs) in radar and electronic warfare sensor signal-processing applications previously solvable only with ASIC-based solutions. Unlike ASICs, FPGAs allow the creation of digital logic that is reprogrammable. Hardware using these devices thereby has flexibility similar to software, which allows the developer to test and upgrade algorithms without the expense and risk associated with fabricating a custom chip each time a change needs to be made. The downside of this flexibility, however, is that in addition to the design challenges inherent in creating hardware, FPGA development adds many of the difficulties found in software development.

Typically, FPGA designs have been developed using a hardware description language (HDL) such as VHDL (Very High-Speed Integrated Circuit (VHSIC) Hardware Description Language). This code needs to be validated for functionality and syntax in a way very similar to conventional software. However, unlike software, in order to validate the design, a tool called an HDL simulator needs to be employed. An HDL simulator uses a special piece of HDL code called a test bench to stimulate the system under test, which allows the simulated system outputs to be validated. After functional validation, the code created with this process is then synthesized to a form suitable for implementation of the design as digital logic in the FPGA.

As an alternative to conventional VHDL design for FPGAs, the vendor Xilinx has created the System Generator for Digital Signal Processing (DSP) development tool that allows for creation of FPGA designs in the Mathwork's Simulink environment. Simulink is a tool that allows for the graphical creation of algorithms using block diagrams known as blocksets and for the subsequent simulation of the designs to ensure proper functionality. Another important feature of Simulink is its link with Mathwork's MATLAB environment. MATLAB is the most widely used tool to model military and commercial signal-processing algorithms and has become the de facto standard for DSP design. The integration of MATLAB with Simulink allows the developer to use code and tools created in MATLAB to stimulate and analyze algorithms developed in Simulink.

The System Generator tool creates functional VHDL code from the Simulink environment using a special blockset developed by Xilinx. Being integrated into Simulink, it allows the developer to test and examine designs through the integration with MATLAB. The developer is able to inject test vectors into the system from the MATLAB workspace and export system outputs to the MATLAB workspace. This ability facilitates a much faster design cycle by moving much of the testing that is normally done with VHDL test benches and simulators to validate functionality of VHDL code to testing in the Simulink/MATLAB environment. By way of illustration, Figure 1 shows a small System Generator design of a component known as a digital down converter that is used in many radar and electronic warfare signal-processing systems.

The System Generator design flow takes advantage of the tight integration of Simulink and MATLAB to realize time savings in the development and validation of FPGA algorithms. A baseline software simulation in MATLAB of the desired system functionality is created that is used to compare with the output of the System Generator model. As each subsystem is completed in Simulink using the System Generator blockset, it can immediately be verified against the MATLAB simulation of the system by replacing the portion of the simulation code representing the subsystem with the Simulink subsystem itself. The close integration of the System Generator and MATLAB allows for this rapid validation. Upon the completion and validation of all the subsystems, the full system can be integrated and validated against the original simulation.

After the system is finished and verified in Simulink, it is then converted into VHDL using

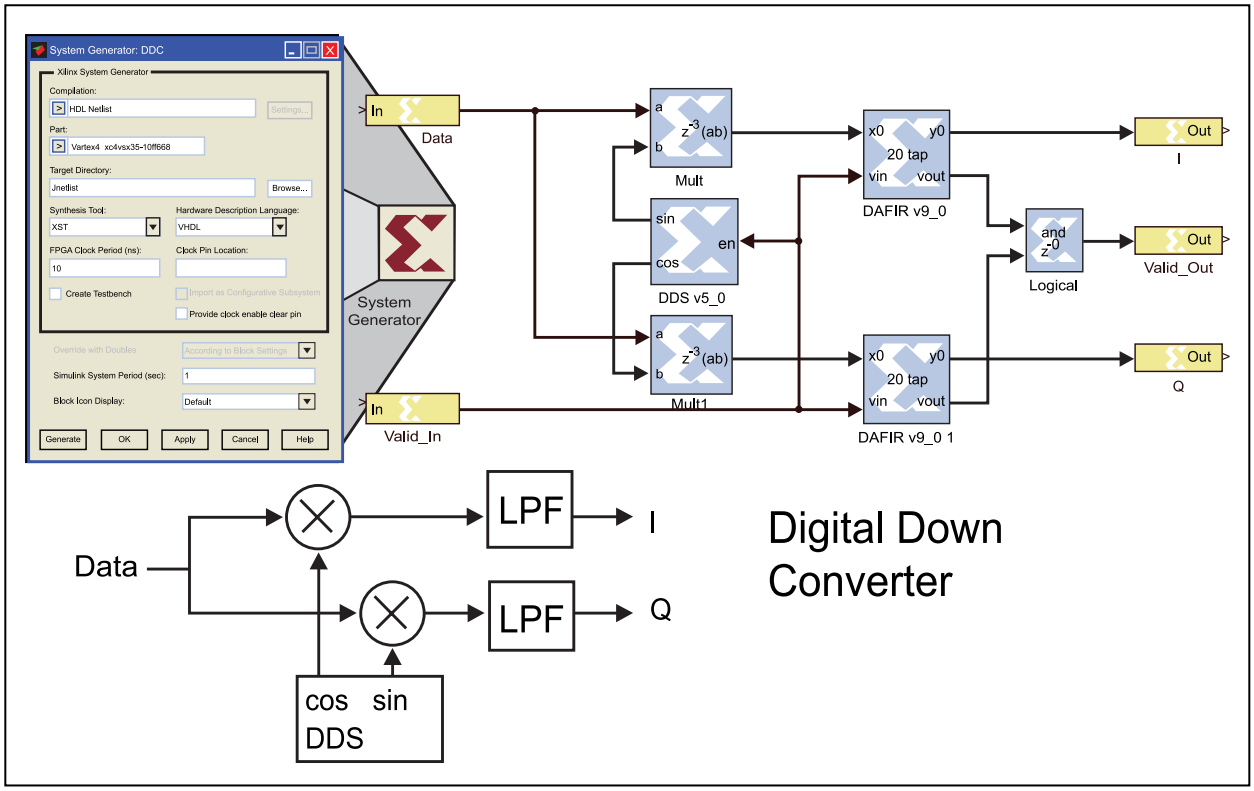



**Figure 1.** System Generator Design of a Digital Down Converter

the System Generator tool. The VHDL created is chip-specific to the part specified in the System Generator tool. This means that the code generated will work only on the specific Xilinx chip; however, it is highly optimized for that chip. The targeted chip can be changed and the code regenerated at any time, which helps to avoid obsolescence issues. Once the VHDL code is generated, some minor work is frequently required to integrate the System Generator portions of the design with the rest of the system. The System Generator design flow is shown in Figure 2.

The use of the System Generator has resulted in significant improvements in the development time of several systems and has enabled a much faster verification cycle for those systems. One of the systems developed using this tool was a signal processor for a low-power, low-cost frequency-modulated continuous-wave (FMCW) radar. A system block diagram of the radar signal processor is shown in Figure 3.

The initial system required approximately 2 weeks of development time to complete, with an additional 2 weeks of development time for the system modifications and refinements. The hardware used for the development was a low-cost development board from Xilinx shown in Figure 4; the output of the signal processor, displayed on an oscilloscope, is shown in Figure 5.

The use of the System Generator allowed for subsystems to be tested as they were developed by integrating them within a MATLAB simulation of the signal processor and comparing the results to the simulation alone. If the design were implemented using conventional FPGA design tools, it is estimated that the design process would have taken 6 to 8 weeks to achieve initial capability.

The primary benefit of using the System Generator is the rapid development time. With its close integration with MATLAB, much of the verification of the system can be done more quickly than if done in VHDL. The use of specific blocks to implement functions also results in efficient code optimized by the chip vendor for use on their hardware. The use of the System Generator shortens the development time of FPGA-based signal-processing algorithms significantly. On this project, development time was shortened by a factor of three, as compared to traditional design techniques, thus allowing systems to be more rapidly fielded and upgraded to meet the needs of the warfighter.

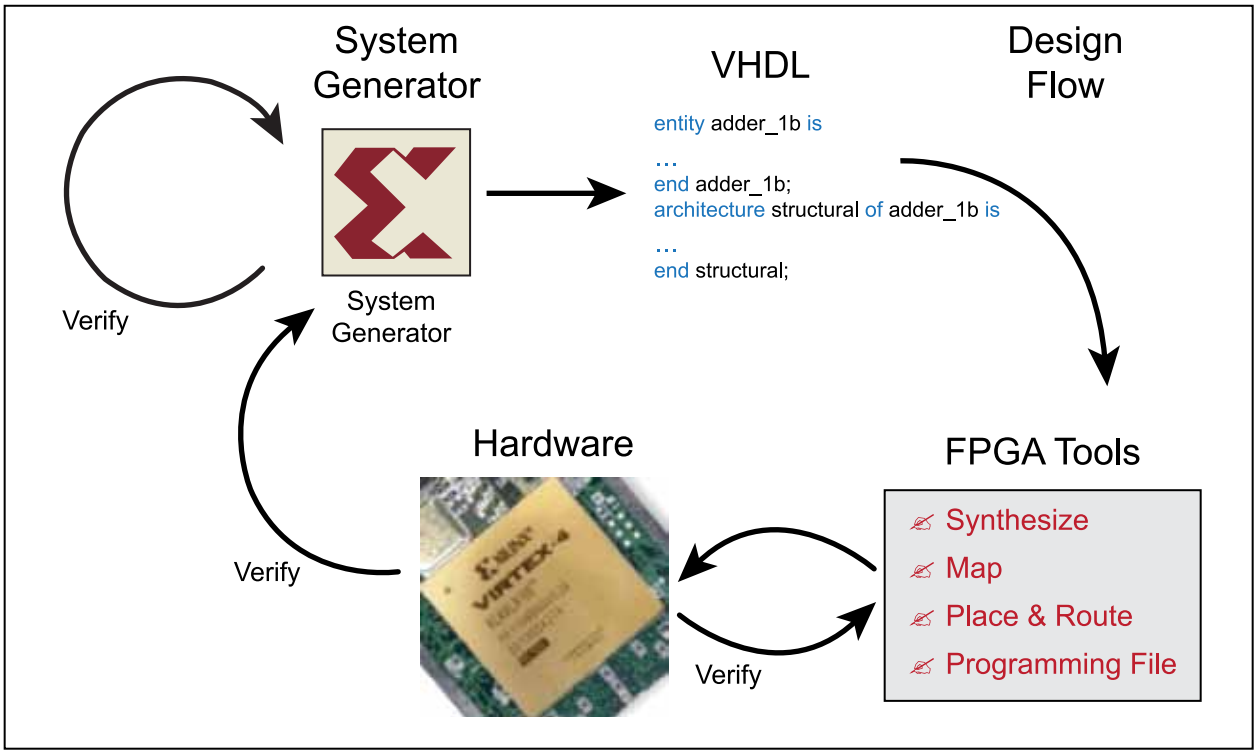



**Figure 2.** Design Flow Using System Generator

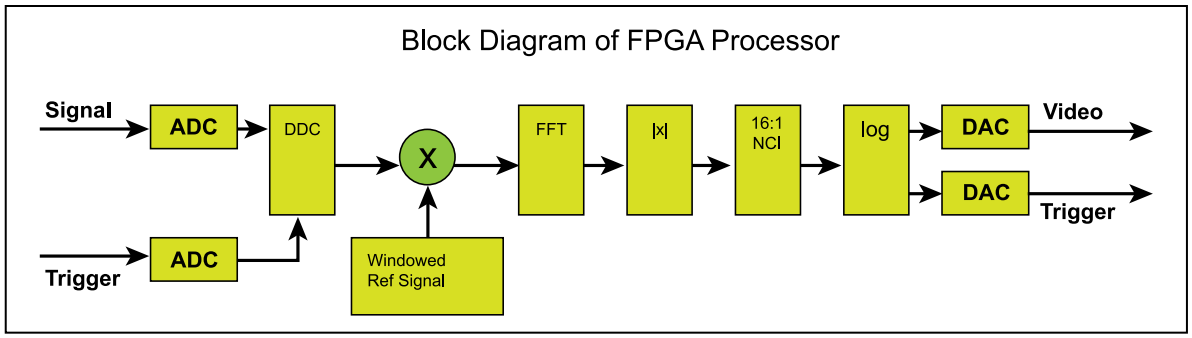



**Figure 3.** Block Diagram of FMCW Radar Signal Processor

**Figure 4.** Hardware Platform Used for the FMCW Radar Signal Processor

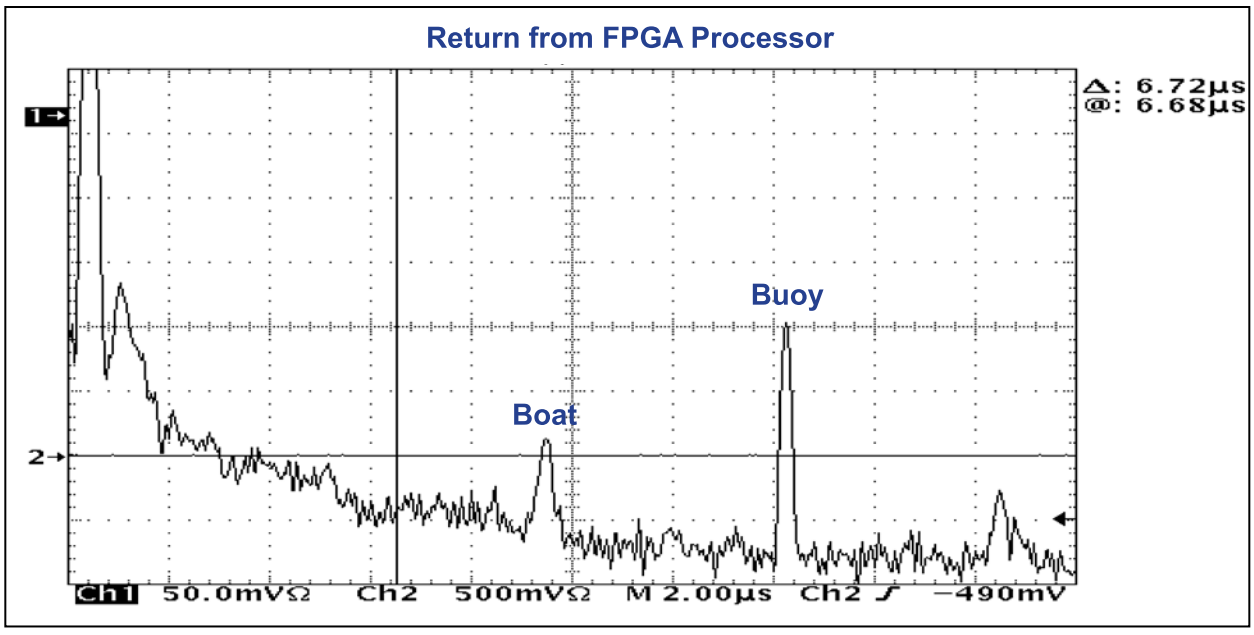



**Figure 5.** Radar Video Output of FMCW Radar Signal Processor

# The AN/SPS-74 Periscope Detection Radar System

*By Ian Barford, Mark Tadder, and Christopher Gorby*


Over the last decade, the Navy's focus has increasingly shifted from open-ocean operations to littoral warfare. As the performance of the Navy's traditional antisubmarine warfare (ASW) sensors (passive and active sonar systems) degrades in the littoral environment, alternative ASW sensors, such as periscope detection radars, are required to provide effective ASW capability in these regions. In response to the U.S. Fleet Forces Command (USFFC) Integrated Priority Capabilities List (IPCL), a rapid-deployment capability periscope detection radar system program was initiated in August 2006. The AN/SPS-74 Radar System (see Figure 1) is currently undergoing test and evaluation at the Navy's Acoustic Test and Evaluation Center on Andros Island, Bahamas. It is also being installed in USS *George Washington* (CVN 73). This article describes the AN/SPS-74 periscope detection radar system program and provides an overview of the design features that permit the detection, discrimination, and declaration of periscopes in challenging environmental conditions.

Since the mid-1990s, the Navy has sought to develop a ship-based periscope detection capability. A developmental brassboard system has been periodically deployed and extensively tested since 1996 under the Office of Naval Research (ONR) Advanced Radar Periscope Detection & Discrimination (ARPDD) program. The ARPDD system consists of an AN/APS-137 airborne radar modified to interface with a developmental discrimination and post-processing computer system. After rigorous testing, it was determined that the experimental ARPDD system provided acceptable periscope detection and false-alarm rates. After receiving priority on the USFFC IPCL, an advanced technology demonstration (ATD) development effort was initiated by the Navy's Program Executive Office for Integrated Warfare Systems (PEO IWS). The AN/SPS-74(V) Rapid Development Capability (RDC) program was initiated in 2006 to develop and field an affordable, integrated radar and post-processing system that replicates the performance capability of the ARPDD system by porting ARPDD capability elements to an open-architecture (OA)/commercial off-the-shelf (COTS) environment.

The AN/SPS-74(V)1 Radar System, shown in Figure 2, is an X-band, narrow-beam, high scan rate, high processing capacity, periscope detection and discrimination radar that rapidly scans the sea surface over a full 360 degrees in azimuth. The radar's primary function is to provide periscope declarations to the shipboard combat system

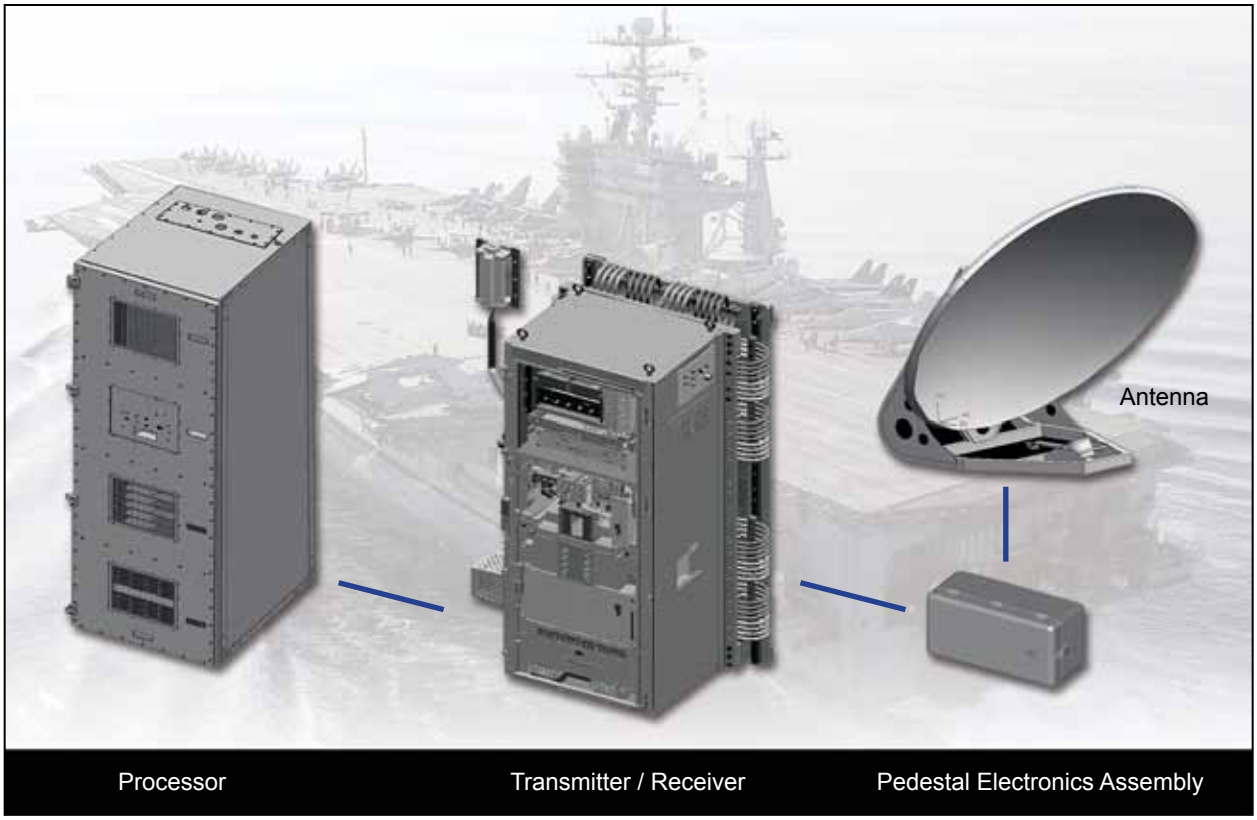



**Figure 1.** AN/SPS-74 Radar System

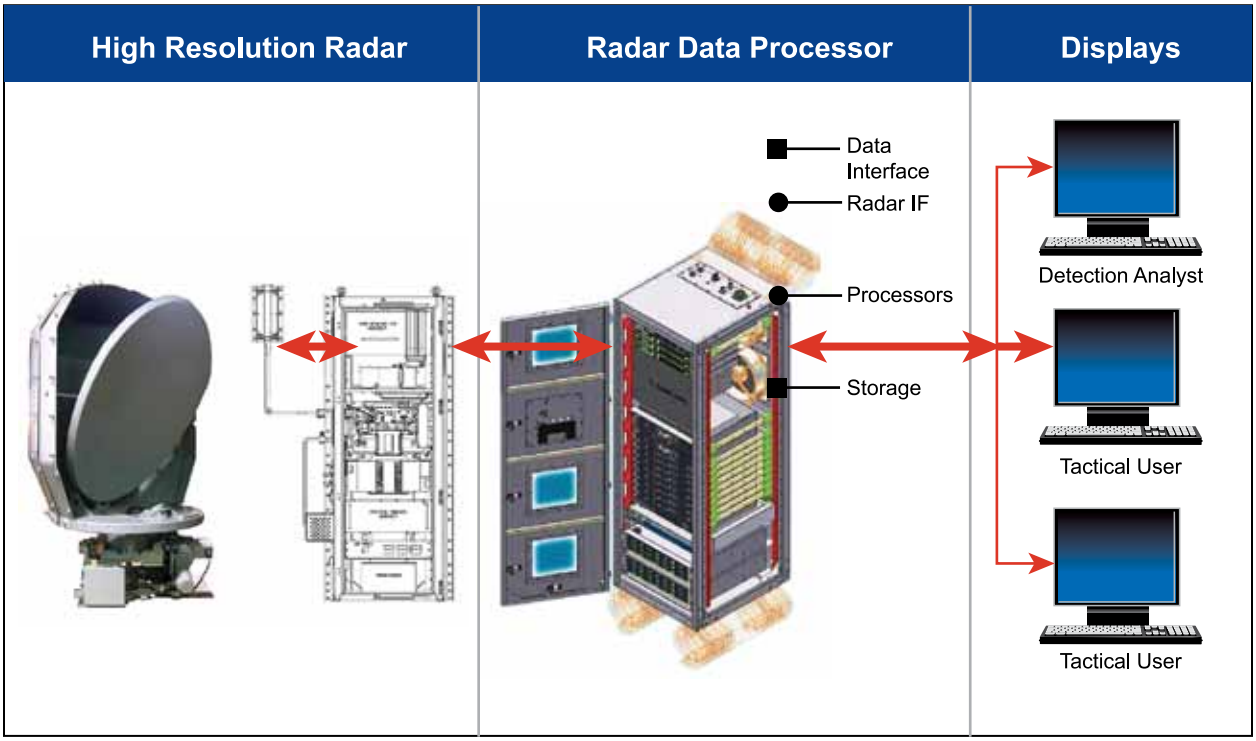



**Figure 2.** AN/SPS-74(V)1 Radar System

by detecting and discriminating periscopes in sea clutter. The system introduces a new high-resolution radar consisting of a modern ultra-wide bandwidth receiver, a high-reliability transmitter, and a 300-rpm scanning antenna. The radar data processor features very high throughput data processing using COTS processors.

Detection of periscopes is especially challenging since they are often hidden or obscured by ocean waves and because they may be exposed only for a short time. On every scan, the radar passes information to the high-performance data processor for immediate isolation of potential periscope targets from clutter. Using proven algorithms from the ARPDD program, the data processor processes potential periscope target data with a multifeature discriminator function and then provides automatic target alerts to the operator.

The radar digital display provides an ocean surface picture with rapid-classification aids that help the AN/SPS-74 radar operator make an informed decision regarding classification of detected targets as shown in Figure 3. The radar system is required to meet the challenging system specifications for the detection and classification of submarine periscopes. This system is required to unambiguously display any possible submarine periscope detection data while also displaying very little ocean-generated clutter return. Detecting and reporting false alerts is required to be kept to a minimum in all types of sea states.

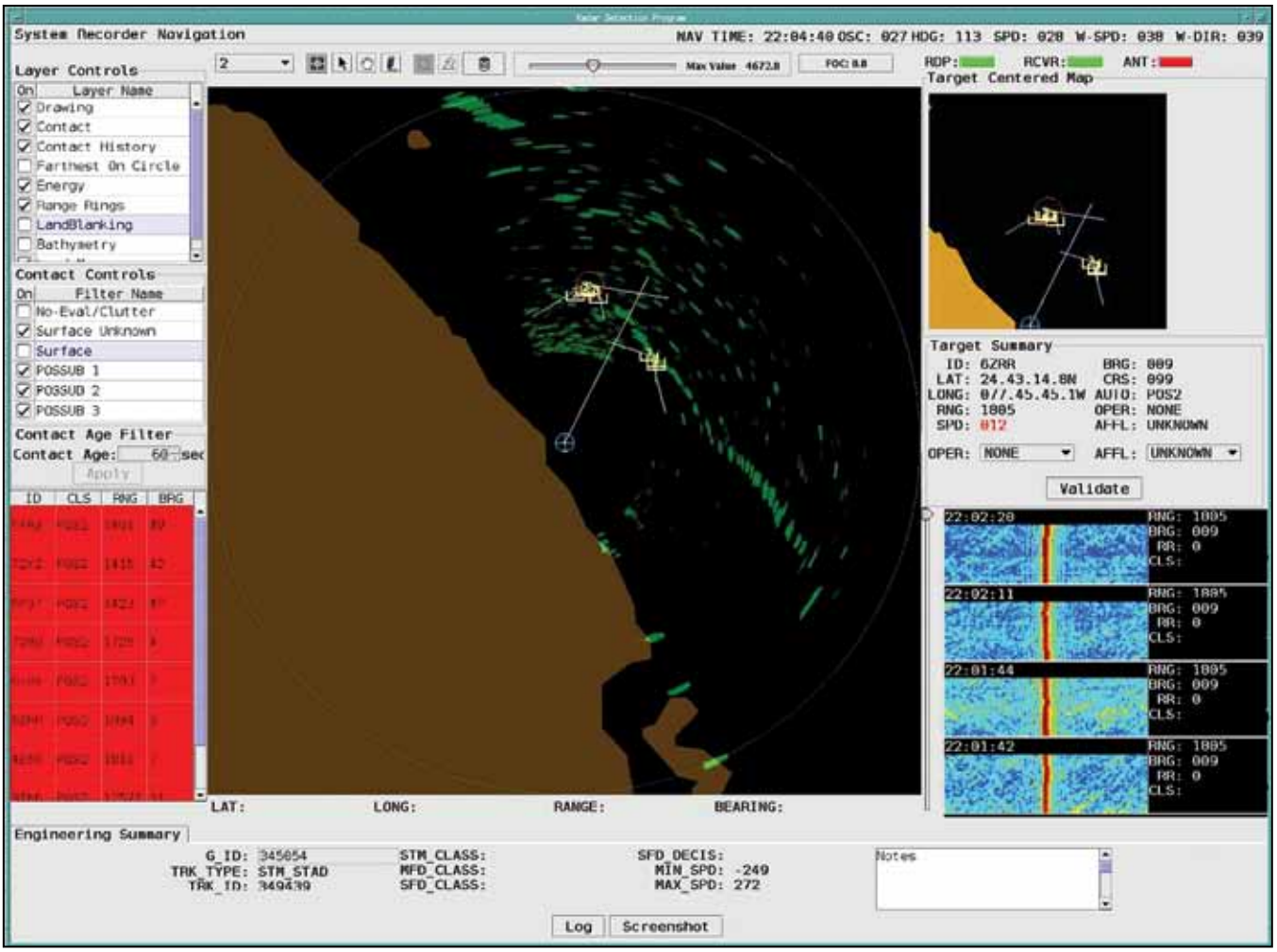



**Figure 3.** Periscope Detection and Discrimination Display

The AN/SPS-74 radar system is currently undergoing extensive test and evaluation at the Navy's Atlantic Undersea Test and Evaluation Center (AUTEC) on Andros Island in the Bahamas (see Figure 4). This location was chosen for its close proximity to deep water, which allows for submarines to enter and exit with ease. The antenna is installed on a platform at a height that is consistent with the intended installation location on aircraft carriers. Since April 2008, the AN/SPS-74 test team has conducted test events in which submarines and submarine-like targets have performed scripted mission scenarios. Using the data from these test events, radar engineers have optimized the system discrimination and classification parameters to meet the stringent system requirements.

PEO-IWS plans to acquire eleven AN/SPS-74(V) systems, with ten systems slated for installation in U.S. Navy aircraft carriers and one system designated for installation at the Naval Surface Warfare Center (NSWC) land-based test site at Oceana Naval Air Station, Dam Neck Annex, Virginia Beach, Virginia. The system is also under consideration for future application aboard surface combatant ships. In support of the PEO-IWS, radar engineers from the NSWC Divisions at Dahlgren, Virginia; Port Hueneme, California; and Crane, Indiana have worked closely with the Naval Research Laboratory (NRL), Johns Hopkins University/Applied Physics Laboratory (JHU/APL), Northrop Grumman Corporation, and Three Phoenix Corporation to achieve program objectives.

**Figure 4.** AN/SPS-74 Radar Installation at the AUTEC Test Site