Field-Programmable Gate Array Research Speeds HPC "up to 100X"

Presented by

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SC07

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Explore FPGAs for future ORNL HPC

Why HPC vendors offer FPGAs

sgi Virtex4 FPGA blades "accelerate mission-critical applications > 100X."

CRAY THE SUPERCOMPUTER COMPANY Steve Scott, CTO HPCWire 24/3/2006

"*After exhaustive analysis, Cray concluded that, although multi-core commodity processors will deliver some improvement, exploiting parallelism through a variety of processor technologies using scalar, vector, multithreading and* ***hardware accelerators*** *(e.g.,* ***FPGAs*** *or ClearSpeed co-processors) creates the greatest opportunity for application acceleration.*"

ORNL benefit: Exceed petaflops and reduce power

Contents

- Background: Why FPGAs?
- ORNL success: FPGA systems, tools and up to 100X speedup
- Partners: XILINX Research Lab, UT, SRC, mitrion, CRAY, sgi

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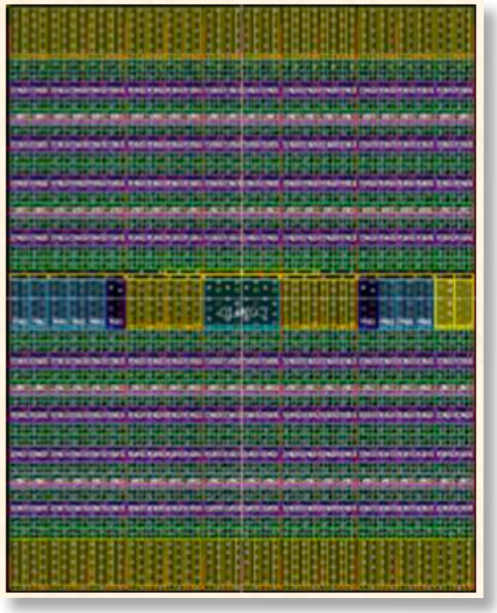
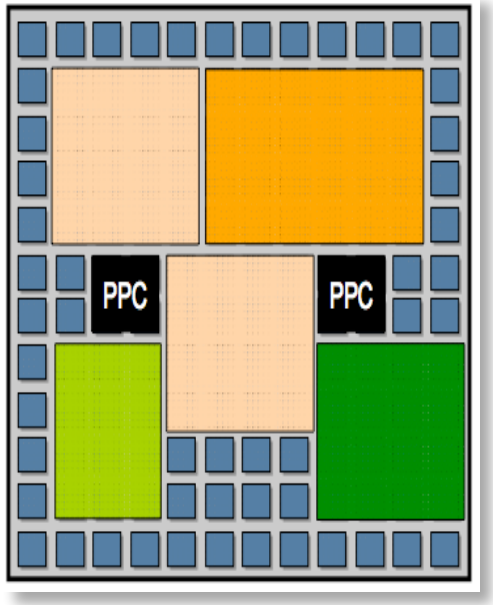
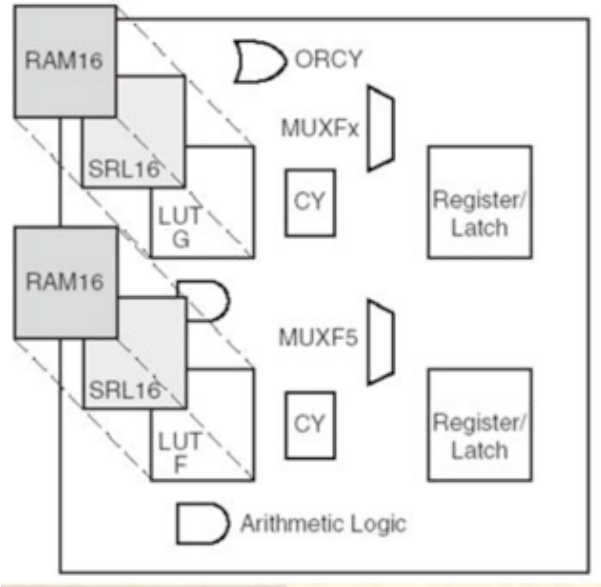
What's an FPGA? Your "custom chip"







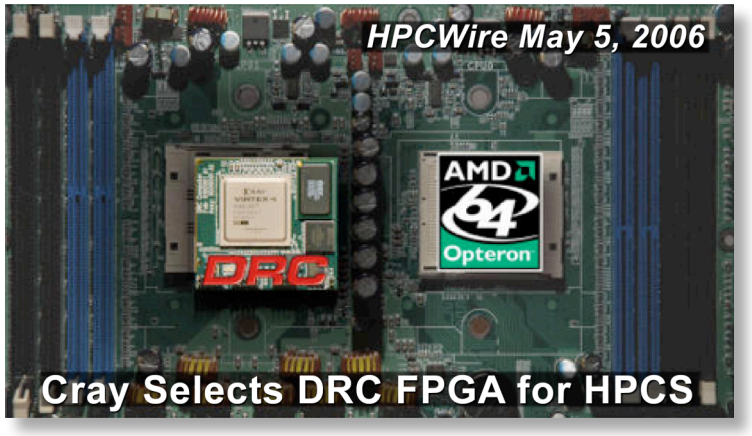
FPGA Logic slice

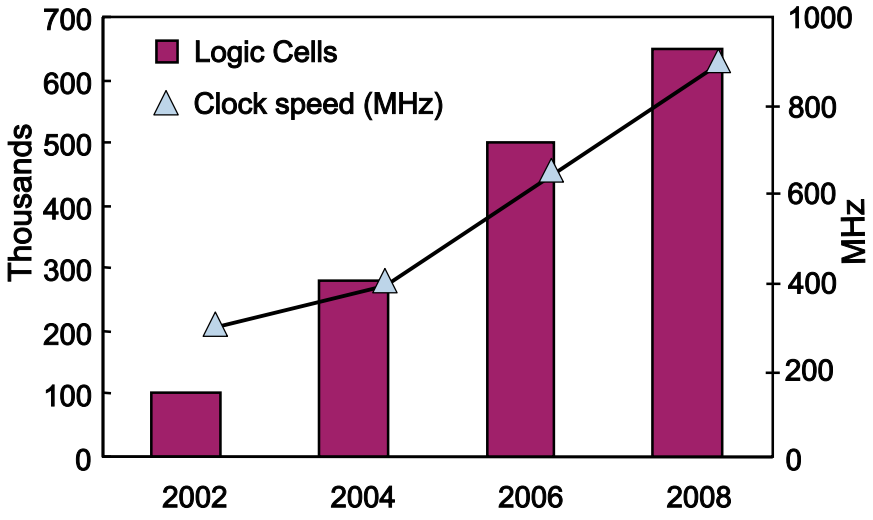
Xilinx Virtex4 FPGA: 25K slices (miniCPUs)

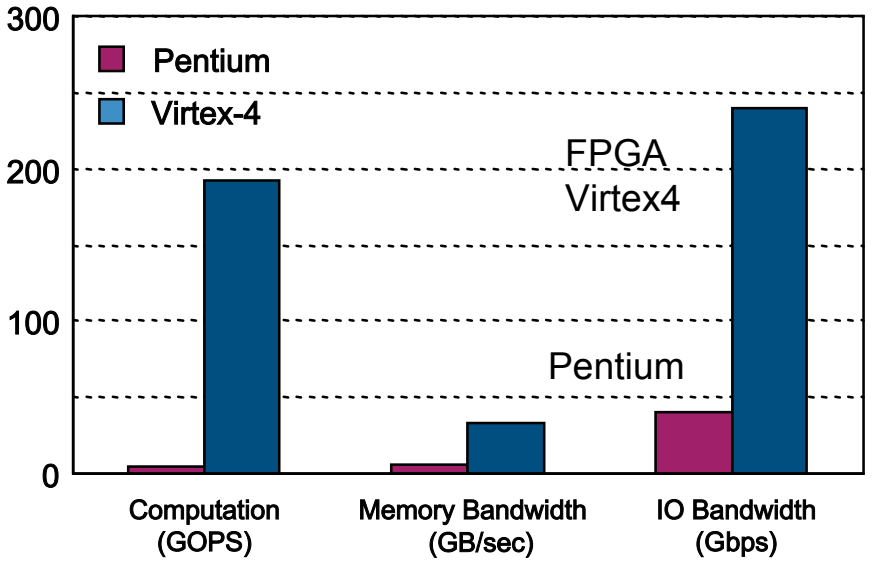
- Logic array: user-tailored to application
- On-chip RAM, multipliers and PowerPCs
- Gigabit transceivers/DSP blocks => FastIO/precision
- 100–1000 operations/clock cycle

Why FPGAs?

- Performance—optimal silicon use (maximize parallel ops/cycle)
- Rapid growth—cells, speed, I/O
- Power—1/10th CPUs
- Flexible—tailor to application

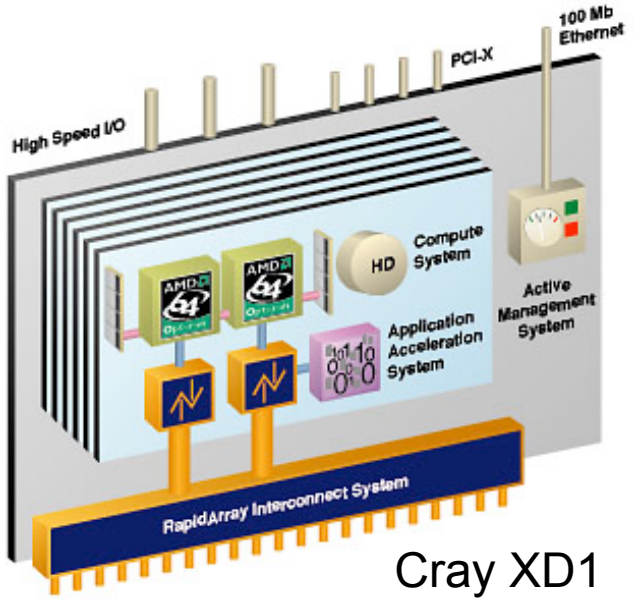




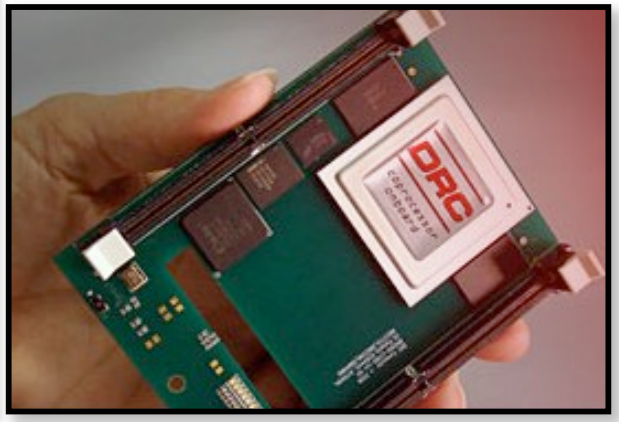


ORNL FPGA hardware/tools

- SRC-6 (Carte), Digilent (Viva, VHDL), Nallatech (Viva)
- Cray XD1 (MitrionC, VHDL): 6 FPGAs + 144 Opterons
- SGI RASC-Altix/Virtex4s (MitrionC)
- CHiMPS (Bee2 => Cray XD1 => DRC => XT4)

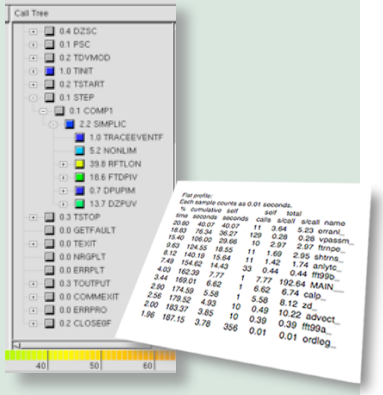


Cray XD1

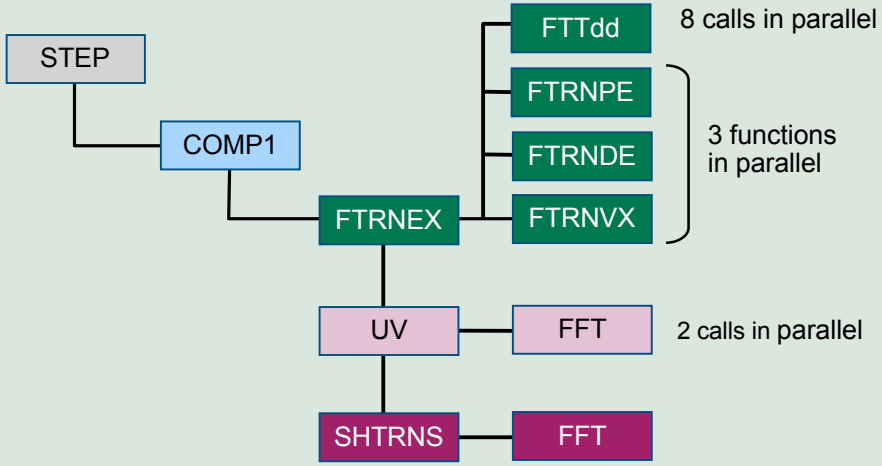


Ported HPC code spectral transform shallow water model (STSWM) **to FPGAs**

Profile

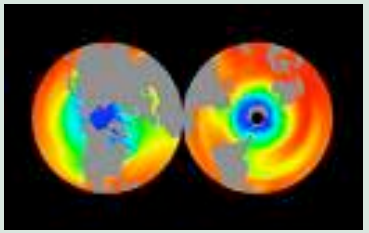


Find parallelism: 80% FFTs



Goal

More GF/$ GF/Watt



Model faster

Exploring programming options

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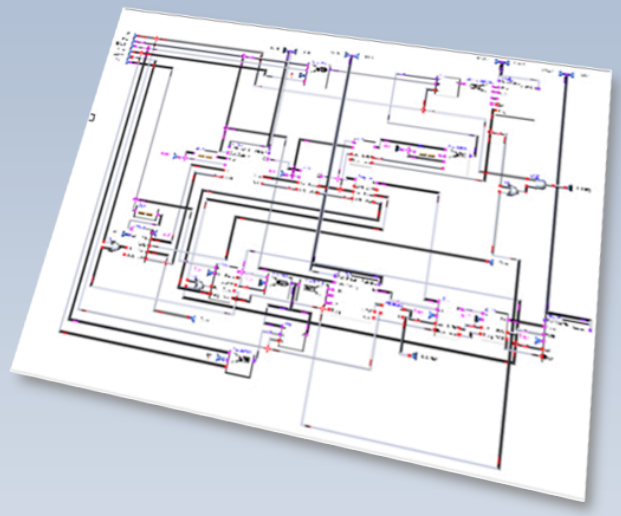
Gauss matrix solver



Viva: Graphical icons—3-dimensional

Compiler, simulator, and debugger

MitrionC: Text/flow—1-dimensional

+ Carte/SRC, CHiMPS-VHDL/Xilinx , DSPlogic

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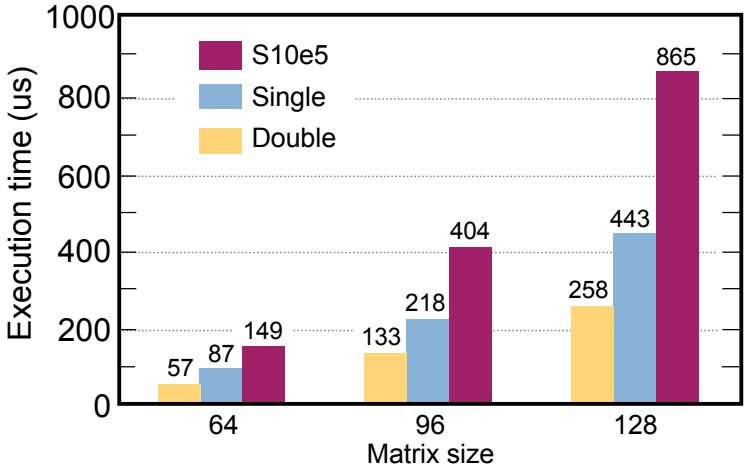
37X* LU decomposition speedup
10X for matrix equation solver



Design	Double FP	Single FP	S10e5
PE Amount	8	16	32
Max size	128	256	256
Achievable frequency	120 MHz	150 MHz	150 MHz
Slices	27,005 (57%)	14,792 (59%)	14,730 (62%)
BRAMs	68 (29%)	129 (55%)	65 (28%)
MULT18X18	128 (55%)	64 (27%)	32 (13%)

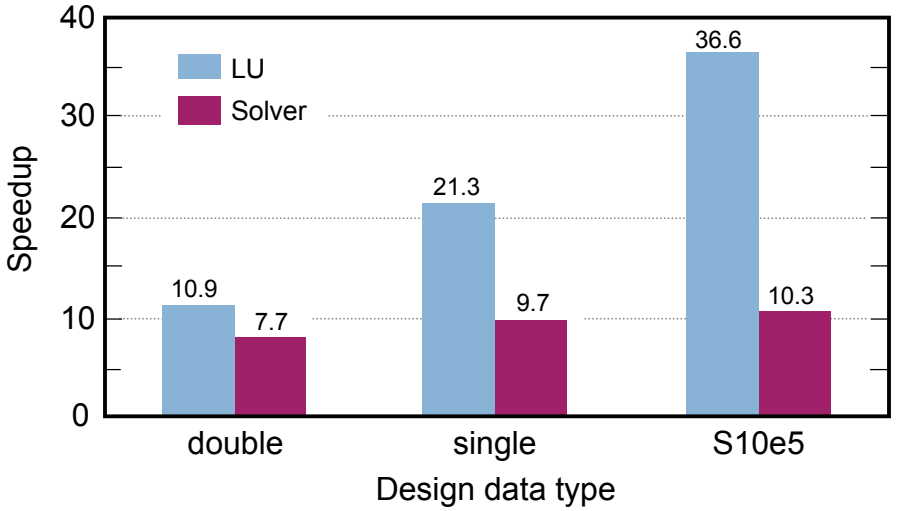
Benefits:

High performance of LP arithmetic

High precision accuracy

Speedup increases with matrix size

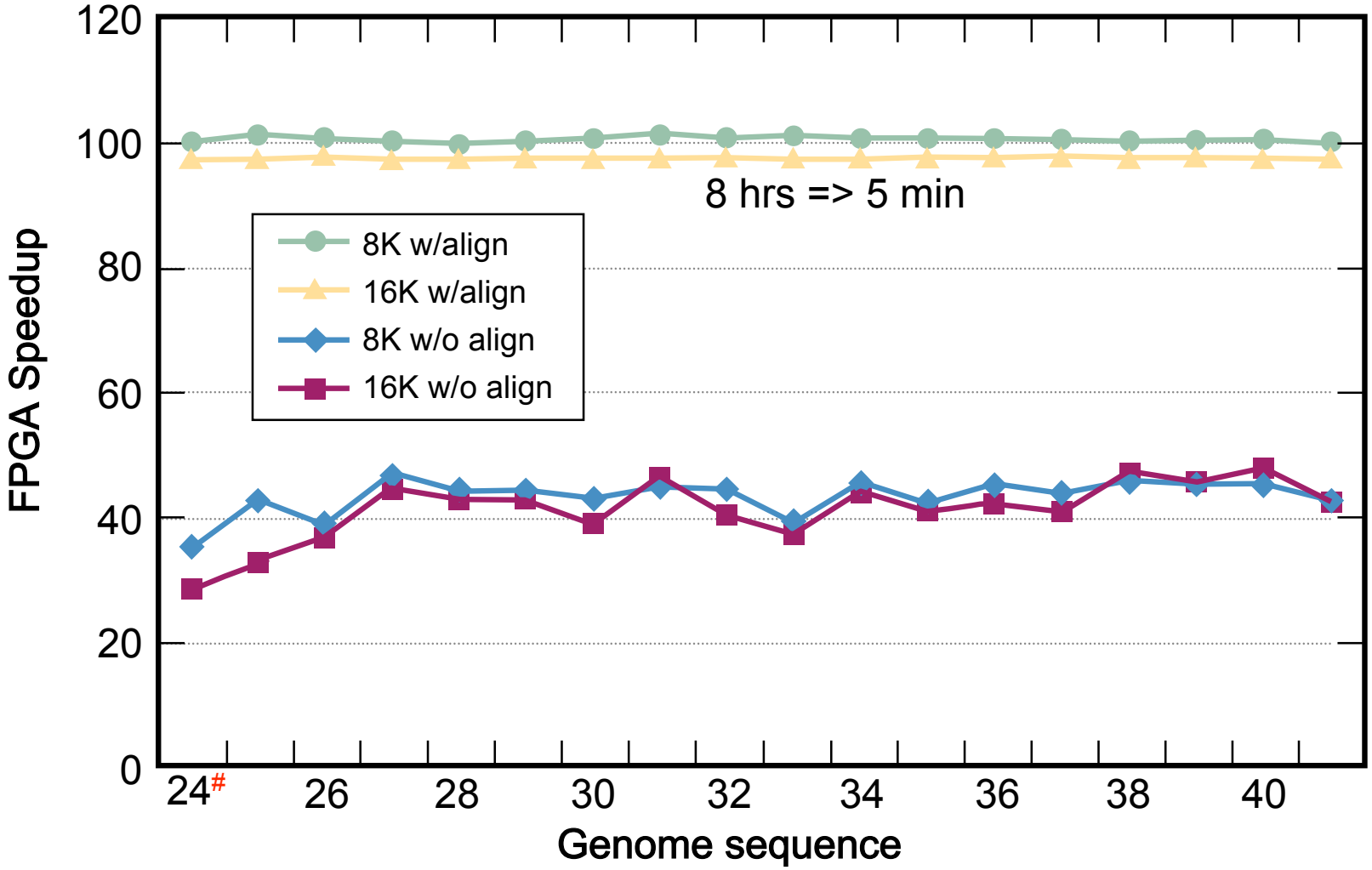
(as LU dominates calculations)



First mixed-precision LU and solver for FPGAs

*FPGA vs 2.2 GHz Opteron

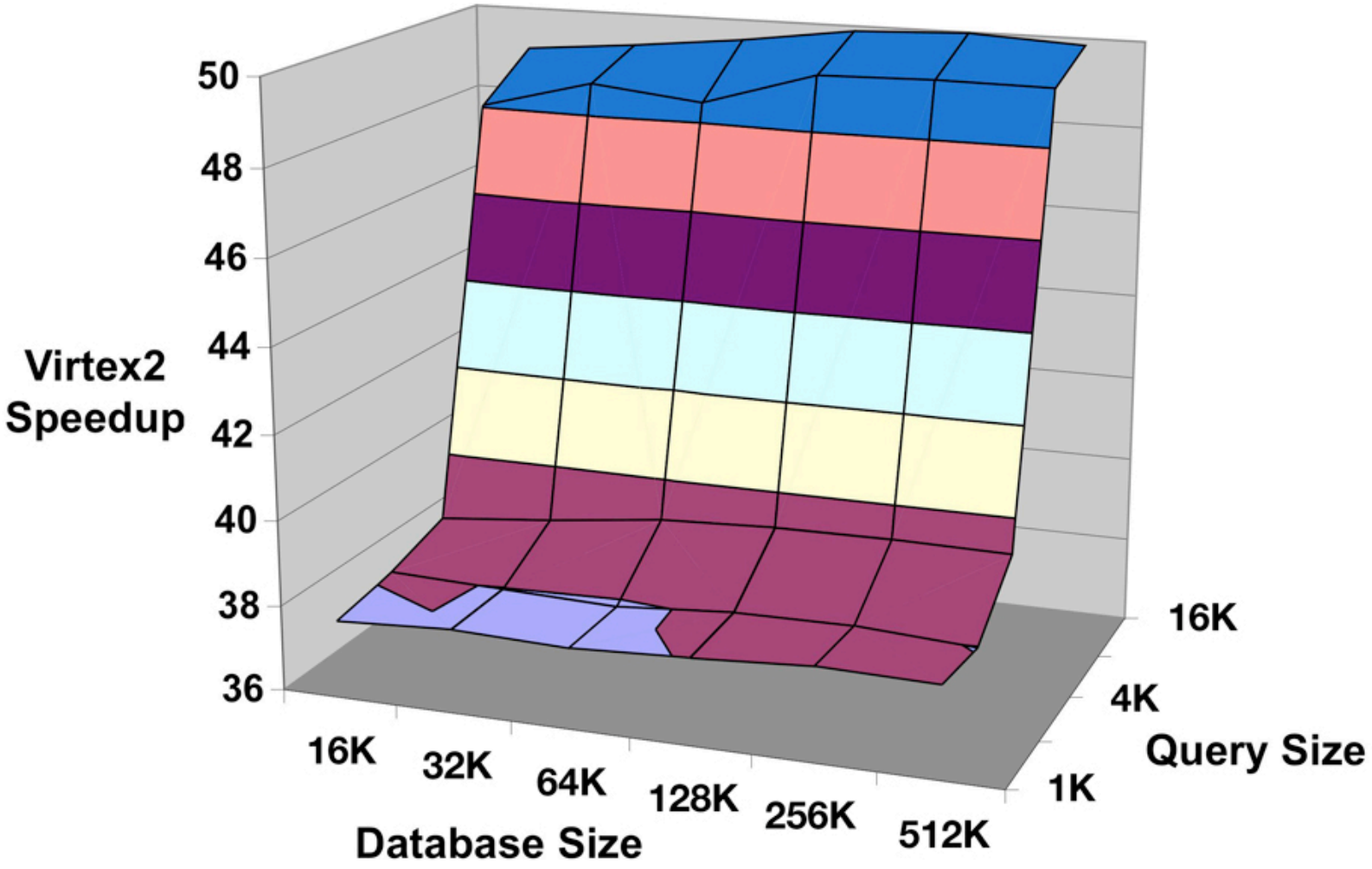
100X* DNA sequence speedup
Bacillus anthracis human DNA comparison



*Virtex-4 FPGA vs 2.2 GHz Opteron on Cray XD1

24= Sequence AE17024

FPGA speedup grows with query size



Summary

- ORNL FPGA research:
  - Increasing HPC relevence
  - FPGA systems: Cray, SRC, Nallatech, Digilent, SGI
  - Compilers: Mitrion-C, Carte, Viva, DSPlogic, CHiMPS
  - Speedup: 10X eqn soln, 100X DNA sequencing
  - Partners: Xilinx, UT, Mitrion, Cray, SGI
- Next: Explore DRC, more FPGAs and CHiMPS

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