

The HPC Challenge (HPCC) Benchmark Suite

Presented by

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The MathWorks, Inc.

<http://icl.cs.utk.edu/hpcc/>



HPCC: Components



$$Ax=b$$

1. HPL (High Performance LINPACK)

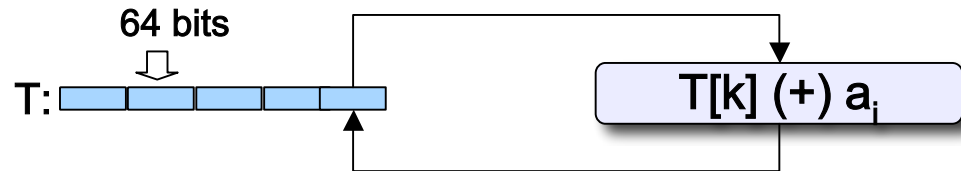
name	kernel	bytes/iter	FLOPS/iter
COPY:	$a(i) = b(i)$	16	0
SCALE:	$a(i) = q*b(i)$	16	1
SUM:	$a(i) = b(i) + c(i)$	24	1
TRIAD:	$a(i) = b(i) + q*c(i)$	24	2

2. STREAM

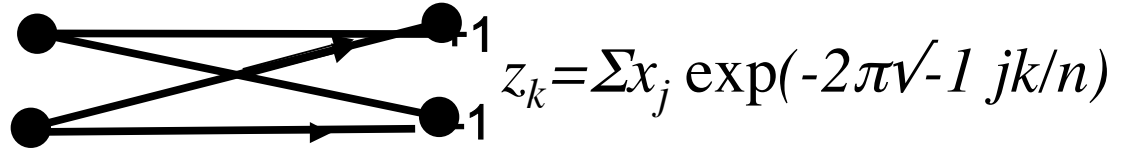
3. PTRANS

$$A \leftarrow A^T + B$$

4. RandomAccess



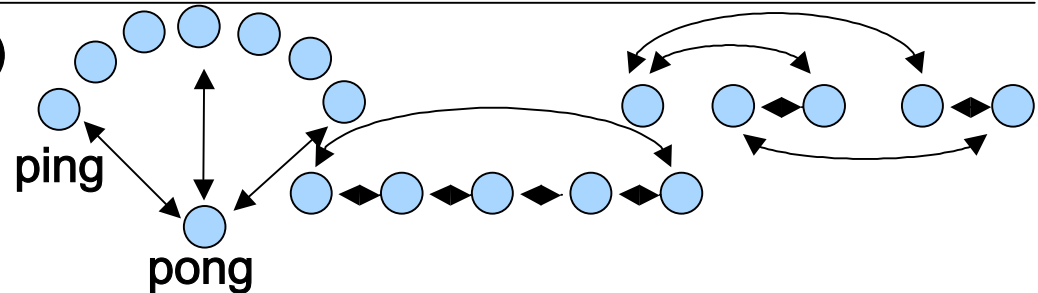
5. FFT



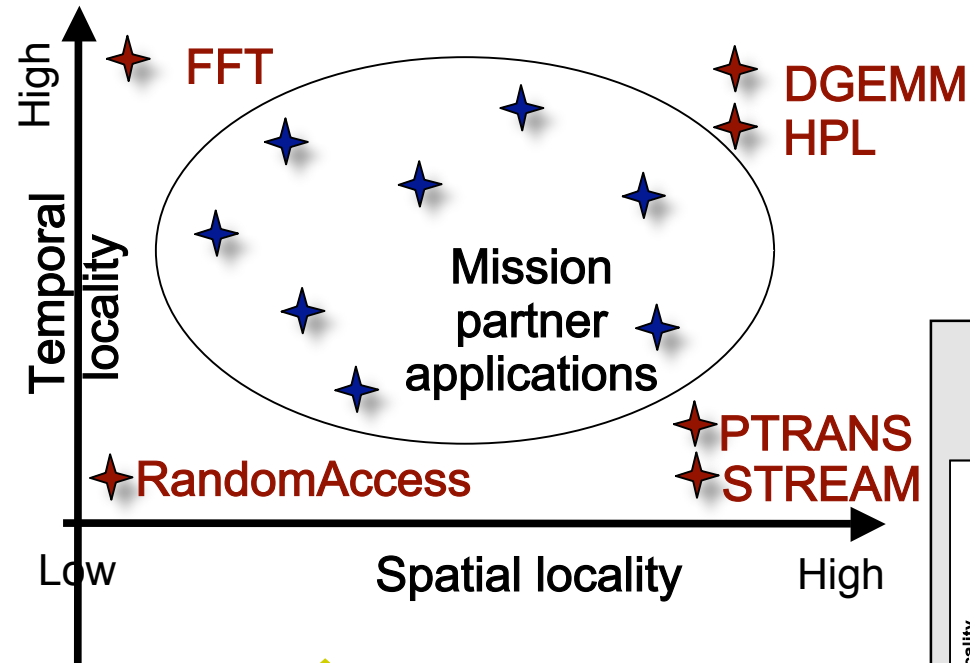
6. Matrix-matrix multiply

$$C \leftarrow s*C + t * A*B$$

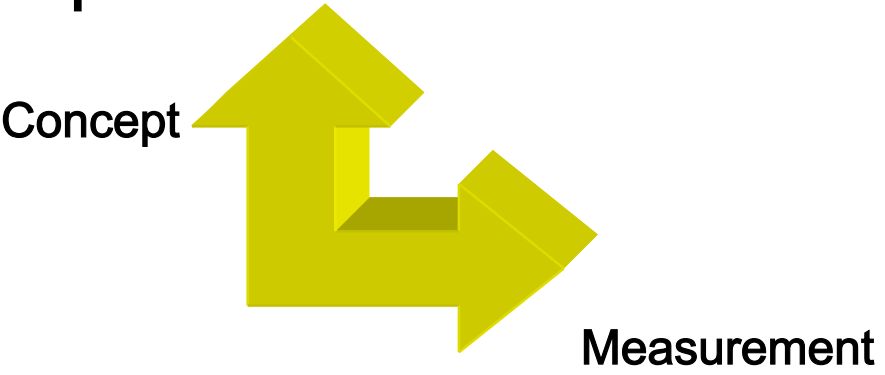
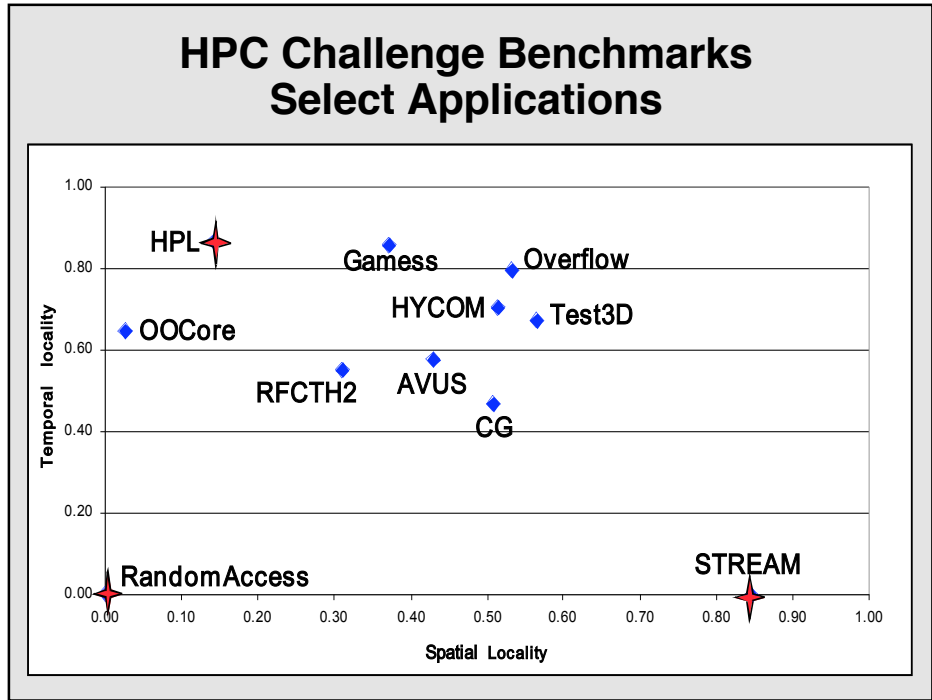
7. b_eff (effective bandwidth/latency)



HPCC: Motivation and measurement

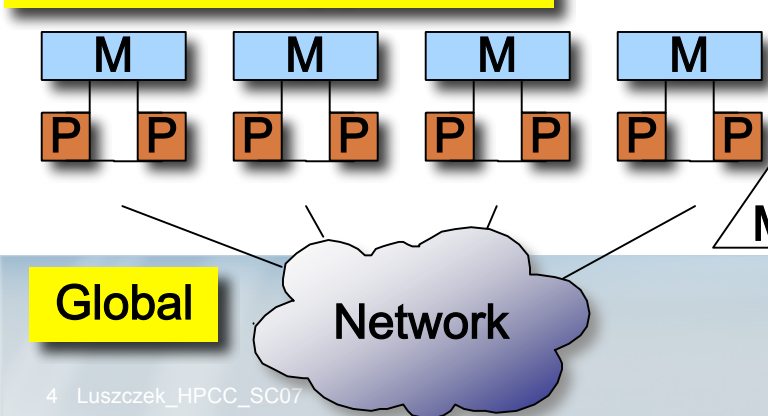
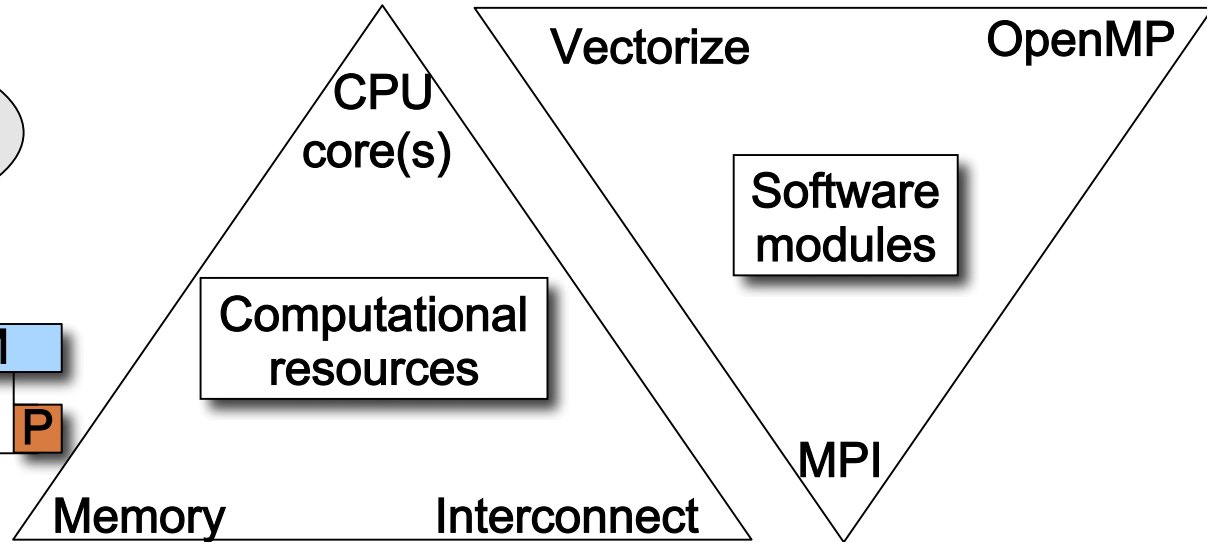
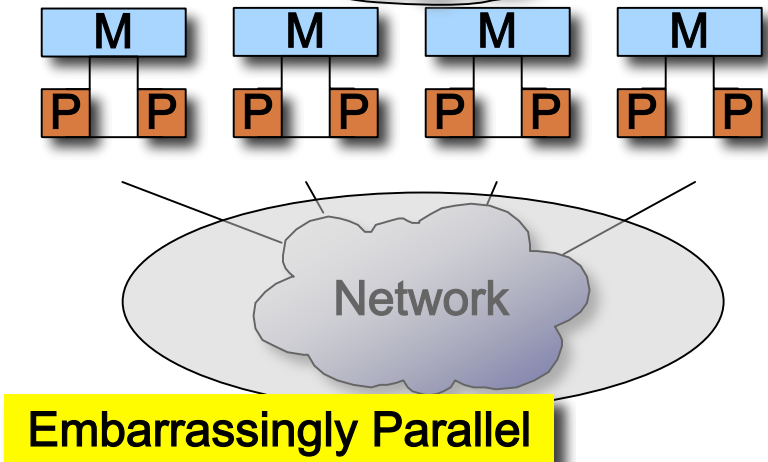
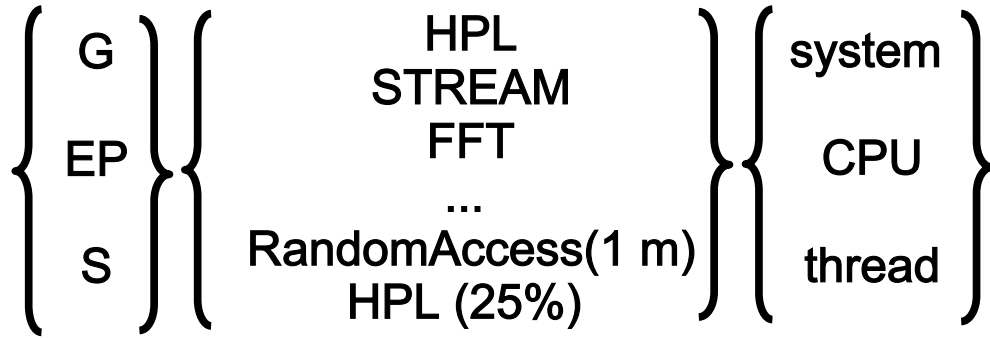
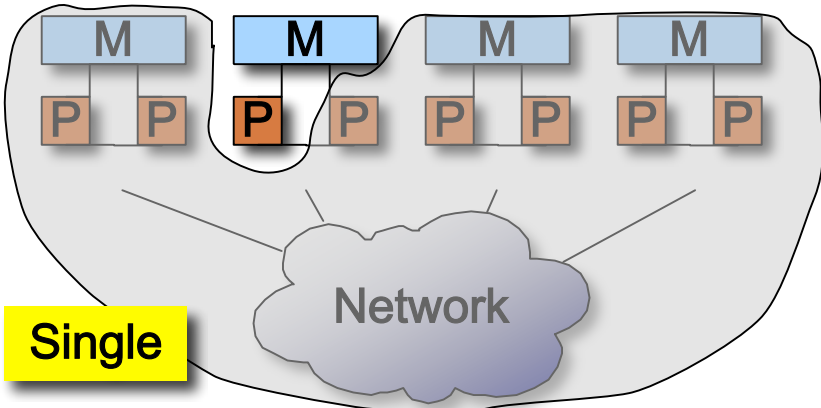


Generated by PMaC @ SDSC



Spatial and temporal data locality here is for one node/processor - i.e., locally or "in the small."

HPC: Scope and naming conventions



HPC: Hardware probes

HPC Challenge Benchmark

- Top500: solves a system

$$Ax = b$$

- STREAM: vector operations

$$A = B + s \times C$$

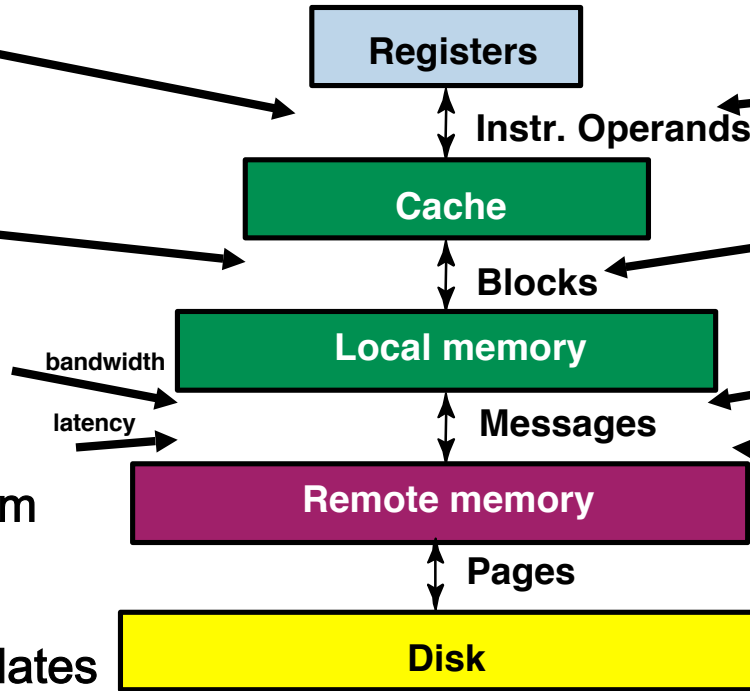
- FFT: 1D fast Fourier transform

$$Z = \text{FFT}(X)$$

- RandomAccess: random updates

$$T(i) = \text{XOR}(T(i), r)$$

Corresponding Memory Hierarchy



HPCS Performance Targets (improvement)

2 Petaflops
(8x)

6.5 Petabytes
(40x)

0.5 Petaflops
(200x)

64,000 GUPS
(2000x)

- HPCS program has developed a new suite of benchmarks (HPC Challenge).
- Each benchmark focuses on a different part of the memory hierarchy.
- HPCS program performance targets will flatten the memory hierarchy, improve real application performance, and make programming easier.

HPCC: Official submission process

1. Download

2. Install

3. Run

4. Upload results

5. Confirm via @email@

6. *Tune*

7. *Run*

8. *Upload results*

9. *Confirm via @email@*

Prerequisites:

- C compiler
- BLAS
- MPI

Provide detailed installation and execution environment.

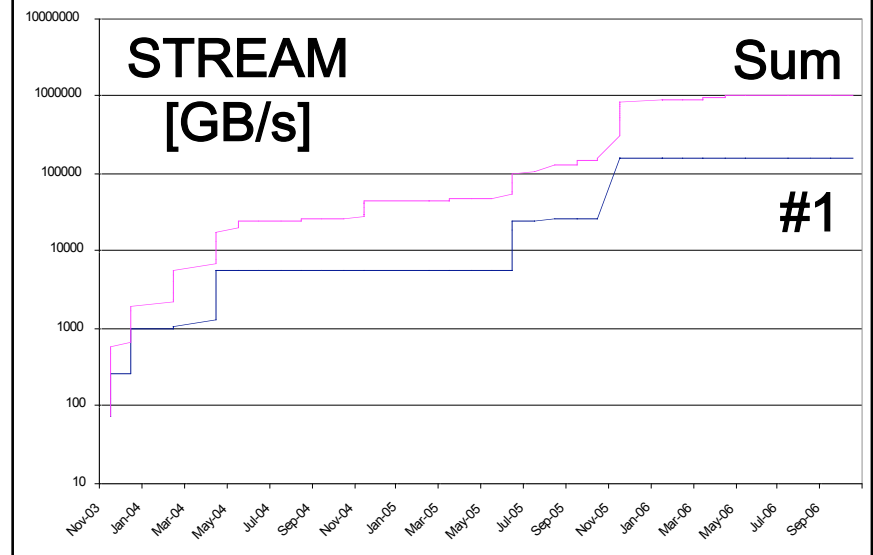
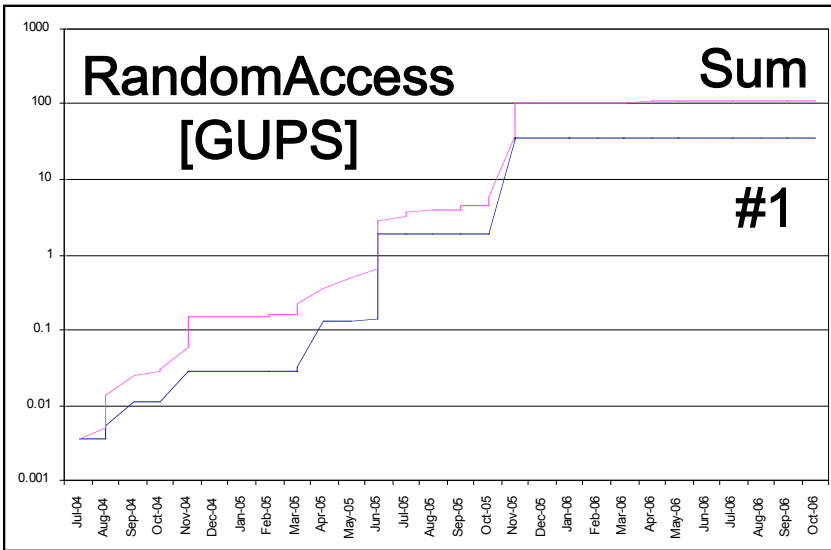
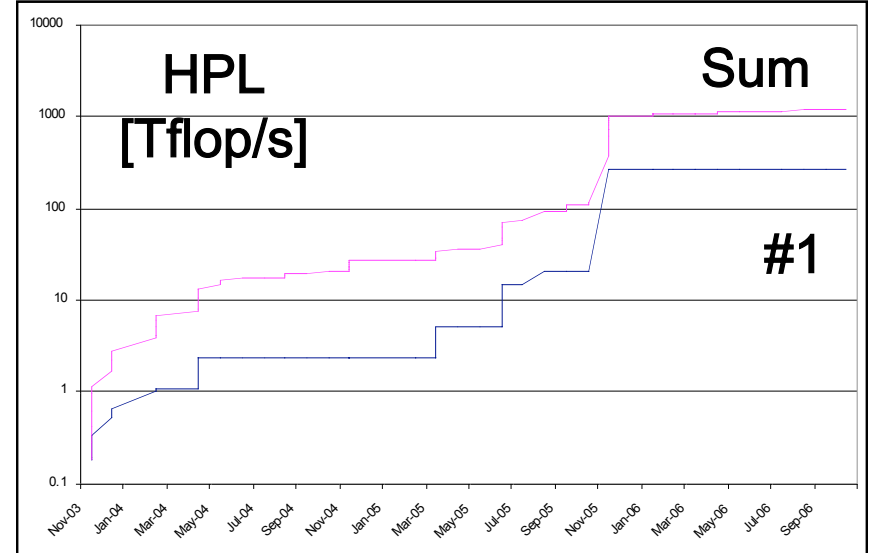
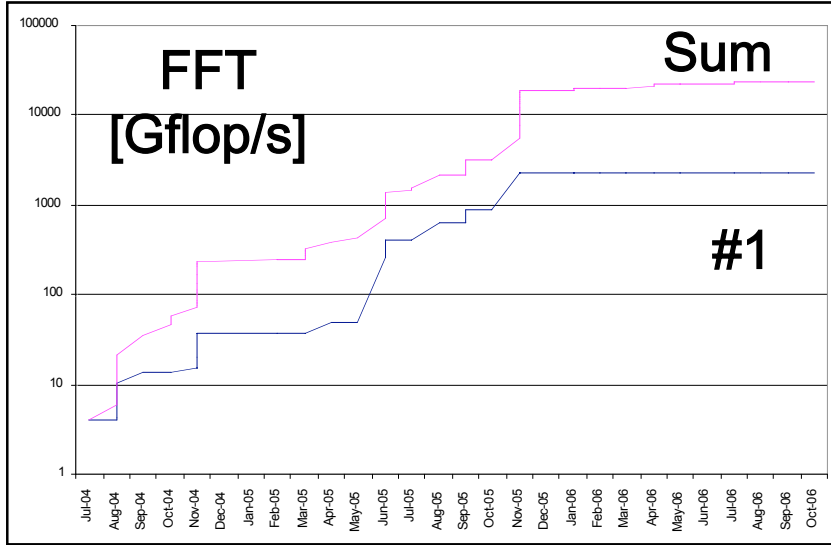
- Only some routines can be replaced.
- Data layout needs to be preserved.
- Multiple languages can be used.

Optional

Results are immediately available on the Web site:

- Interactive HTML
- XML
- MS Excel
- Kiviat charts (radar plots)

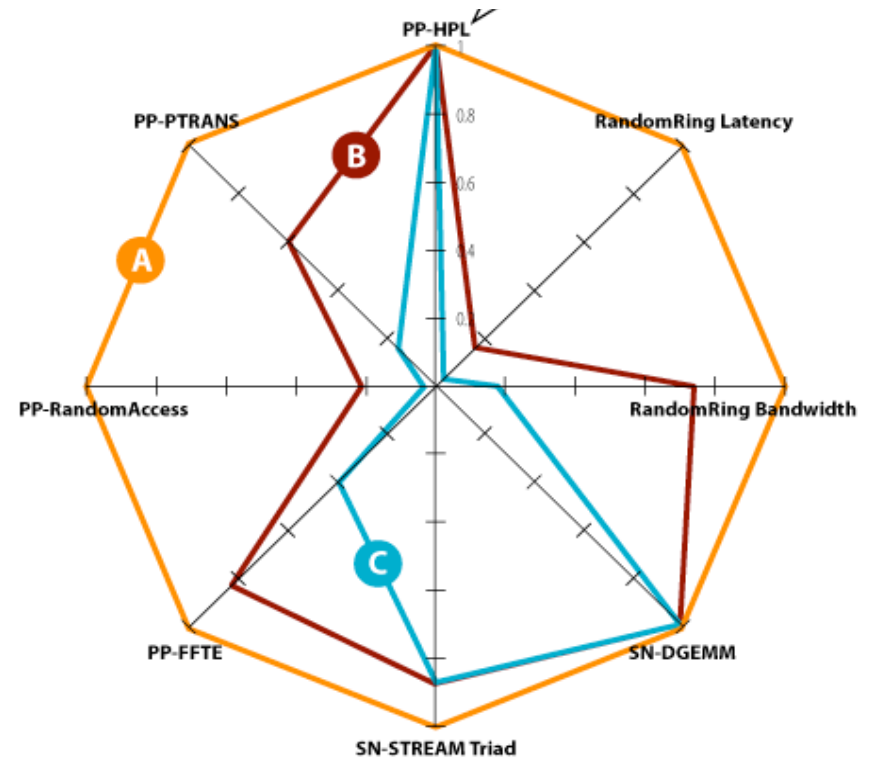
HPCC: Submissions over time



HPCC: Comparing three interconnects

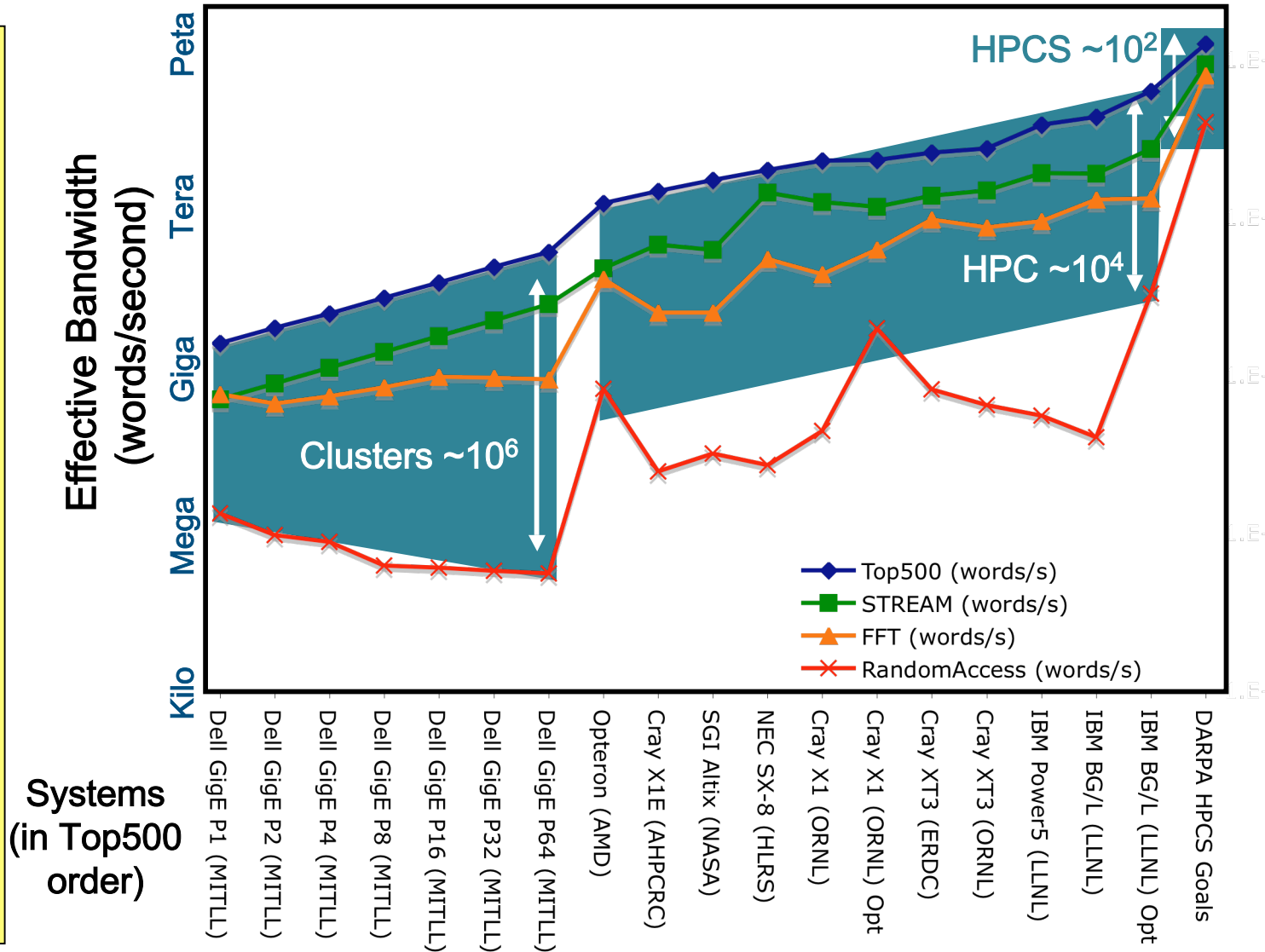
- 3 AMD Opteron clusters
 - Clock: 2.2 GHz
 - 64-processor cluster
- Interconnect types
 - A. Vendor
 - B. Commodity
 - C. GigE
 - G-HPL
 - Matrix-matrix multiply
- Cannot be differentiated based on
 - G-HPL
 - Matrix-matrix multiply
- Available on HPCC Web site
 - <http://icl.cs.utk.edu/hpcc/>

Kiviat chart (radar plot)



HPCC: Analysis of sample results

- All results in words/second
- Highlights memory hierarchy
- Clusters
 - Hierarchy steepens
- HPC systems
 - Hierarchy constant
- HPCS goals
 - Hierarchy flattens
 - Easier to program



HPCC: Augmenting June TOP500

TOP500 rating

Data provided by HPCC database

Rank	Name	Rmax	HPL	PTRANS	STREAM	FFT	GUPS	Lat.	b/w
1	BG/L	280.6	259.2	4665.9	160	2311	35.47	5.92	0.16
2	BGW (*)	91.3	83.9	171.5	50	1235	21.61	4.70	0.16
3	ASC Purple	75.8	57.9	553.0	44	842	1.03	5.11	3.22
4	Columbia (*)	51.9	46.8	91.3	21	230	0.25	4.23	1.39
5	Tera-10	42.9							
6	Thunderbird	38.3							
7	Fire x4600	38.18							
8	BlueGene eServer	37.33							
9	Red Storm	36.2	33.0	1813.1	44	1118	1.02	7.97	1.15
10	Earth Simulator	35.9							

Contacts

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**INNOVATIVE COMPUTING
LABORATORY**

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