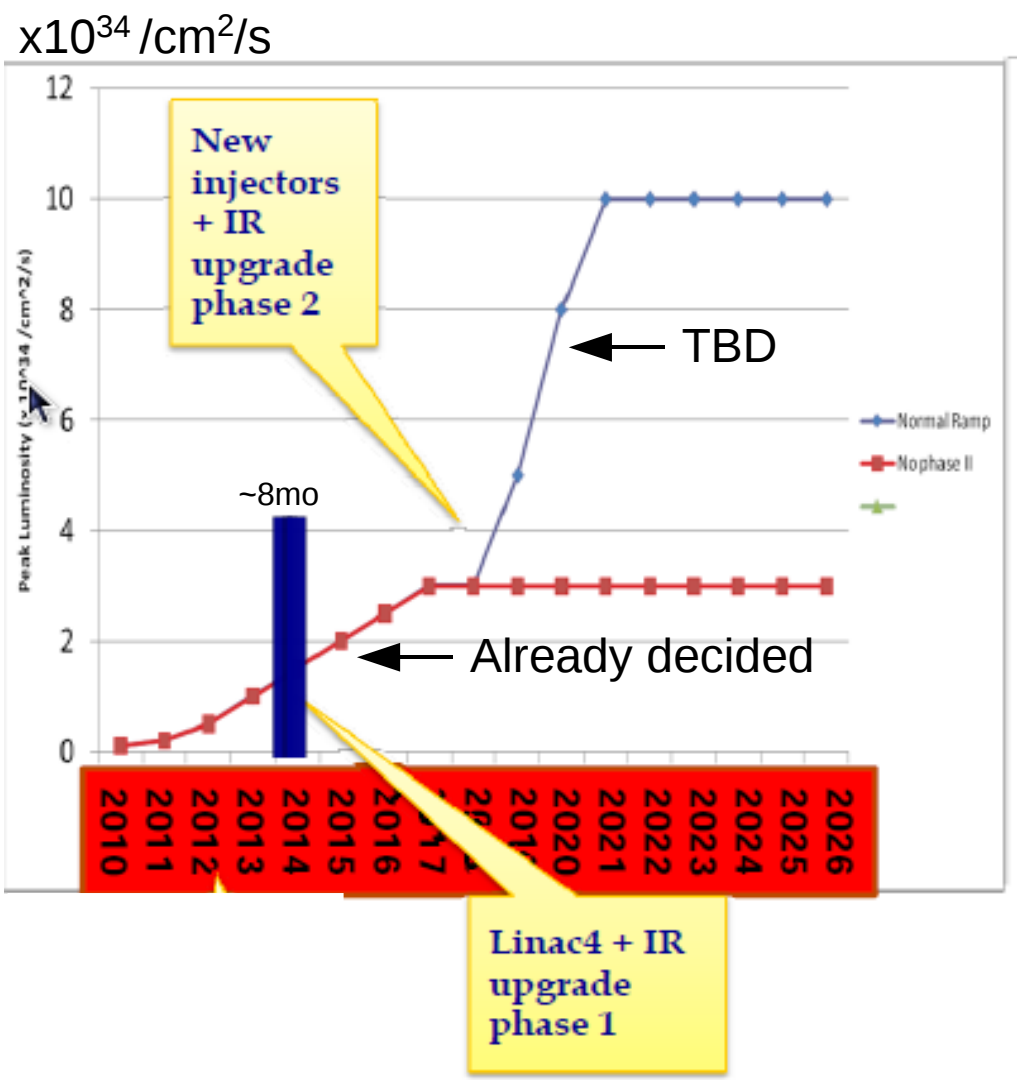
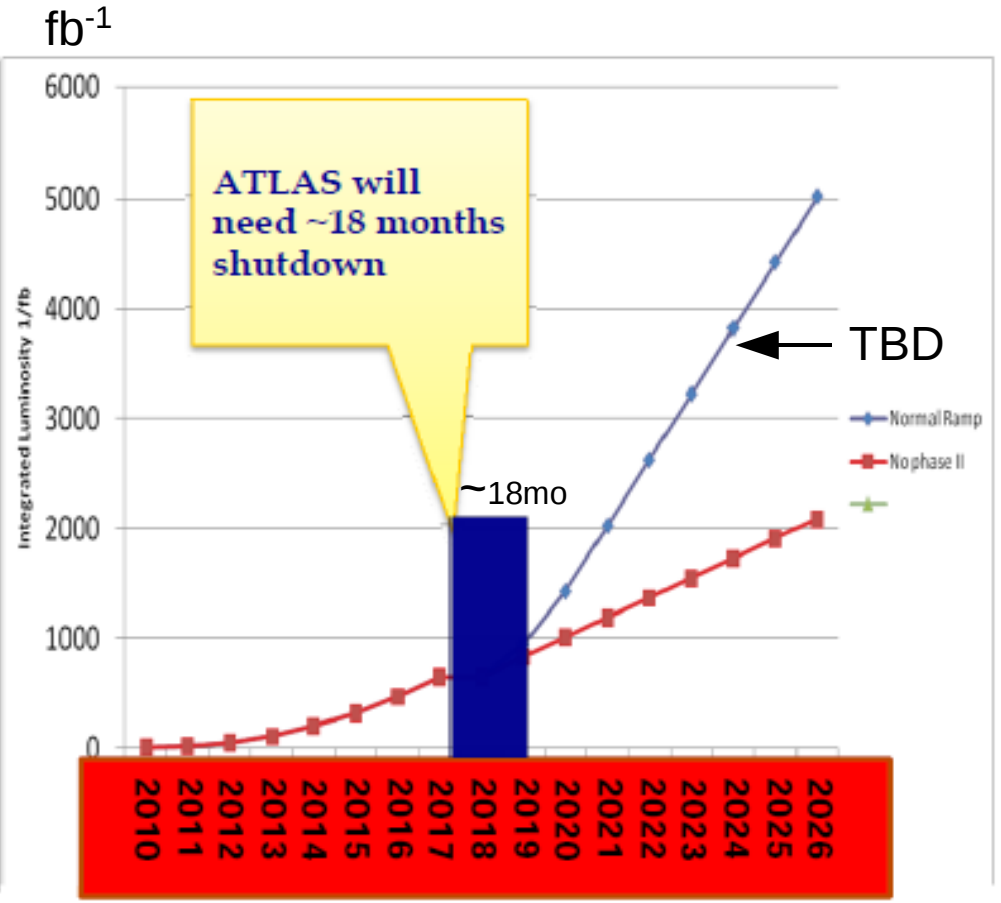
ATLAS Upgrades for High Luminosity

Fermilab, July 7, 2009

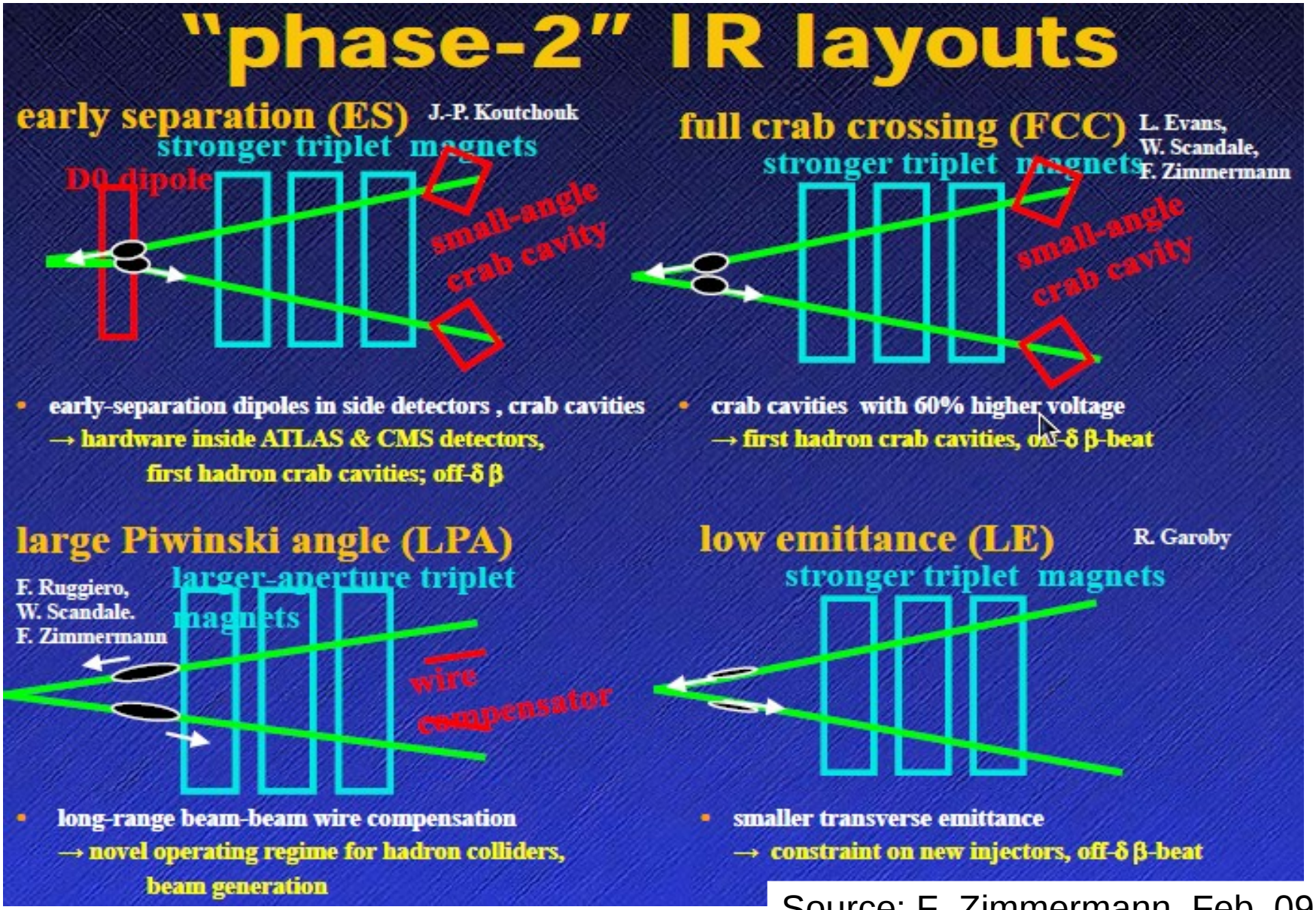
M. Garcia-Sciveres

LHC plans


x10^34 /cm^2/s
New injectors + IR upgrade phase 2
TBD
~8mo
Already decided
Linac4 + IR upgrade phase 1
Normal Ramp
No phase II
Peak Luminosity (x10^34 /cm^2/s)
0
2
4
6
8
10
12
2010
2011
2012
2013
2014
2015
2016
2020
2021
2022
2023
2024
2025
2026

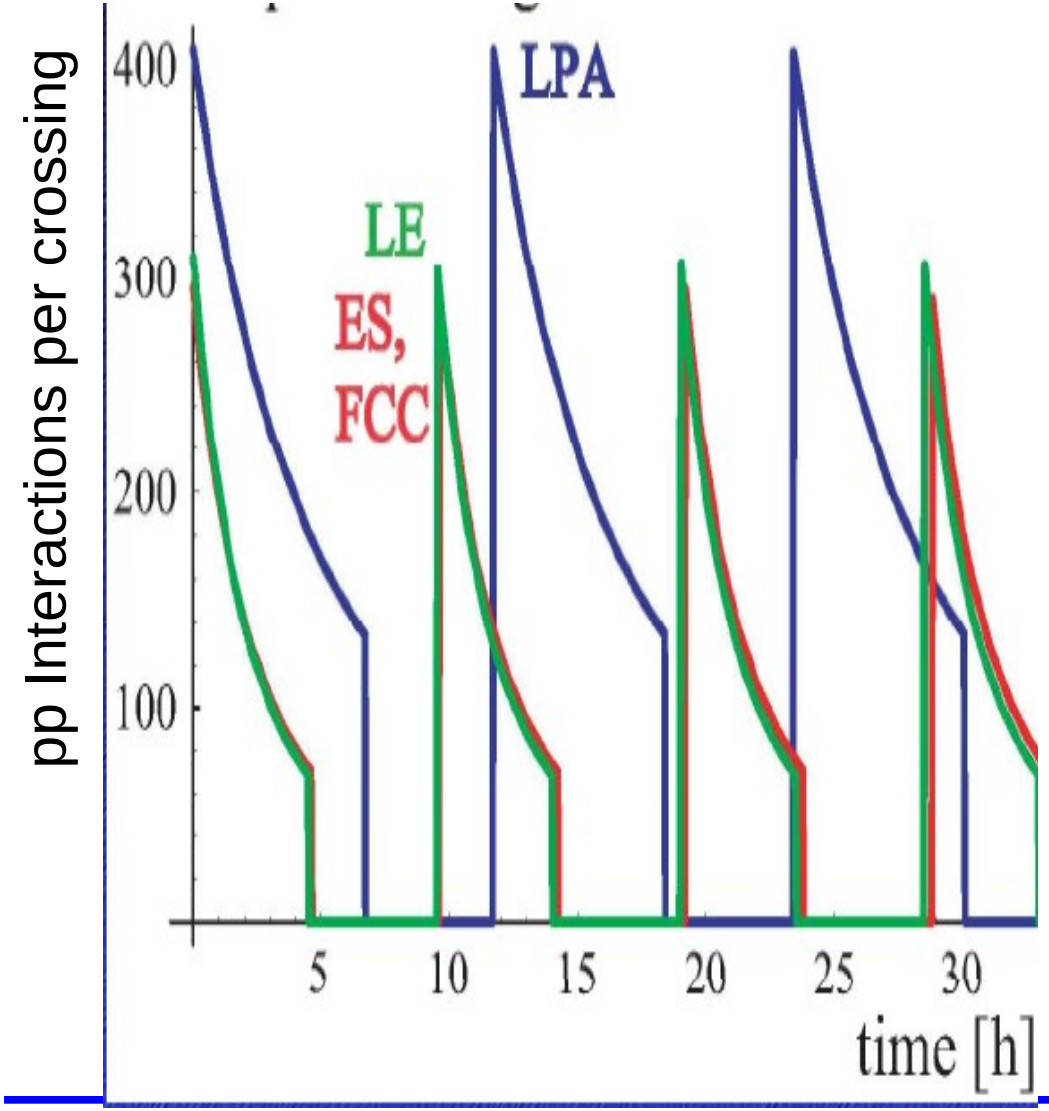

fb^-1
ATLAS will need ~18 months shutdown
TBD
~18mo
Normal Ramp
No phase II
Integrated Luminosity 1/fb
0
1000
2000
3000
4000
5000
6000
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026

Several beam options for phase II

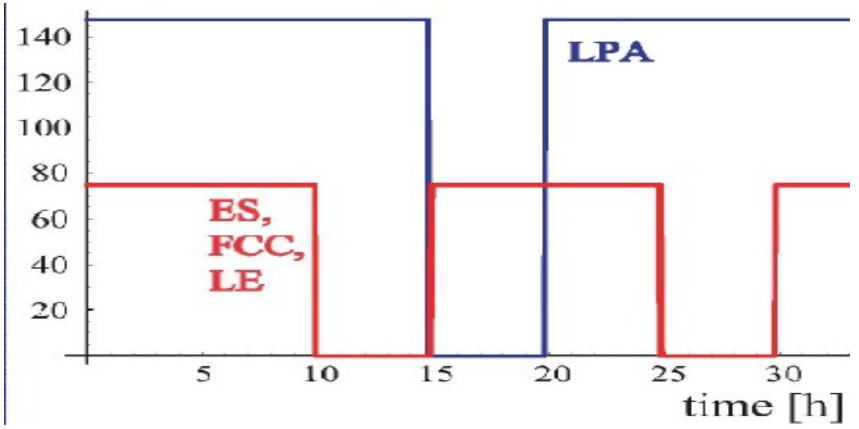


Source: F. Zimmermann, Feb. 09

Beam options affect hit rates, but not total radiation dose



Same beam options with perfect luminosity leveling.
Only 20% lower integrated L due to longer beam lifetime.



ATLAS upgrade plans

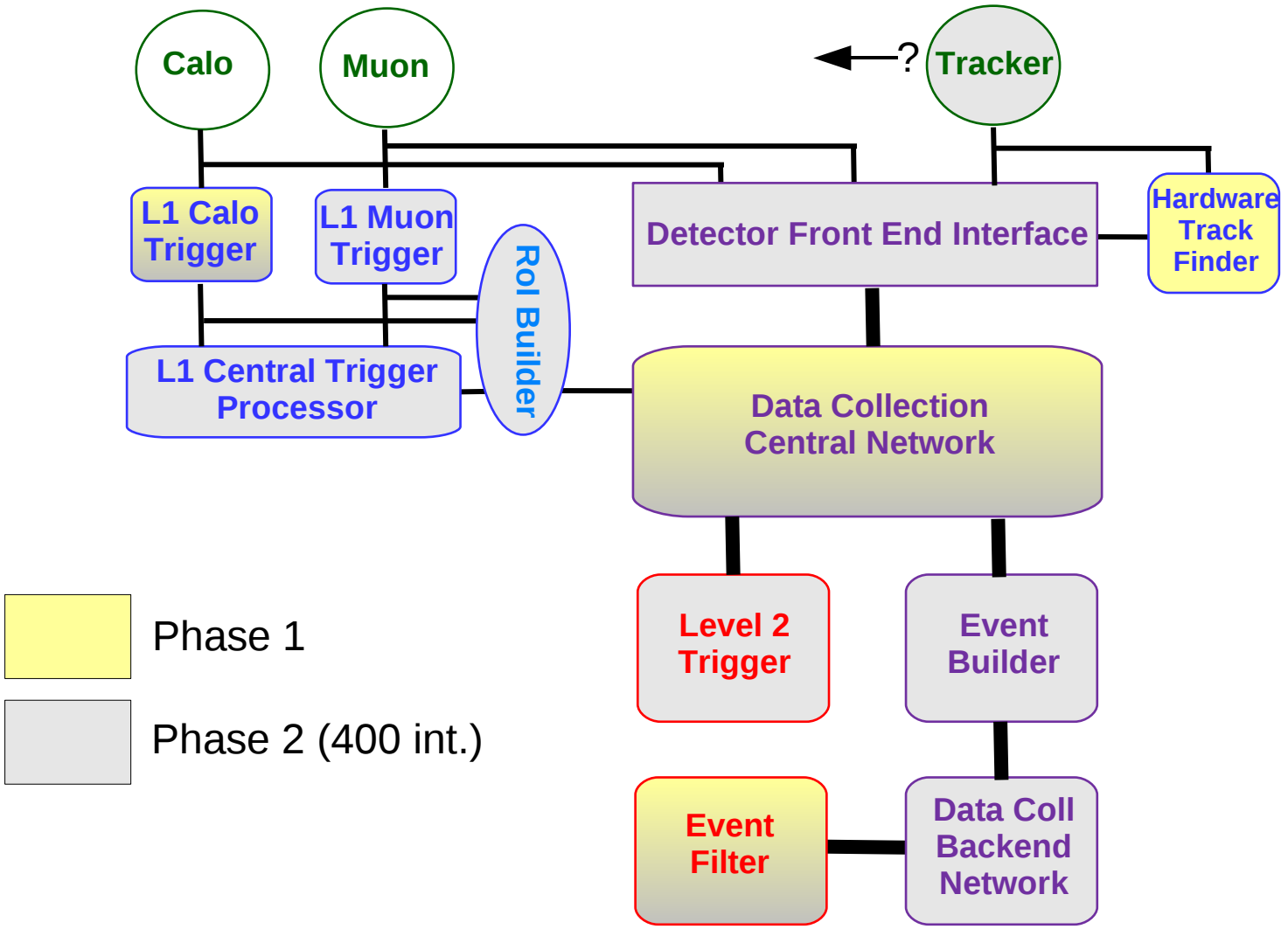
- Phase 1:
  - Trigger / DAQ
    - Moderate upgrades
  - Pixels
    - Our version of L0(0)
  - Muons
    - Restore de-scoped forward elements

- Phase 2:
- If worst case of 400 int./xing
  - Trigger / DAQ
    - Major upgrade
  - Muons
    - Possibly new forward chambers
  - Lar calorimeters
    - Electronics in barrel
    - New forward elements
  - Tile calorimeters
    - Electronics
  - Inner tracker
    - Full replacement

Underlined elements needed even if no Phase 2 or perfect luminosity leveling

Trigger/DAQ is the first thing to upgrade

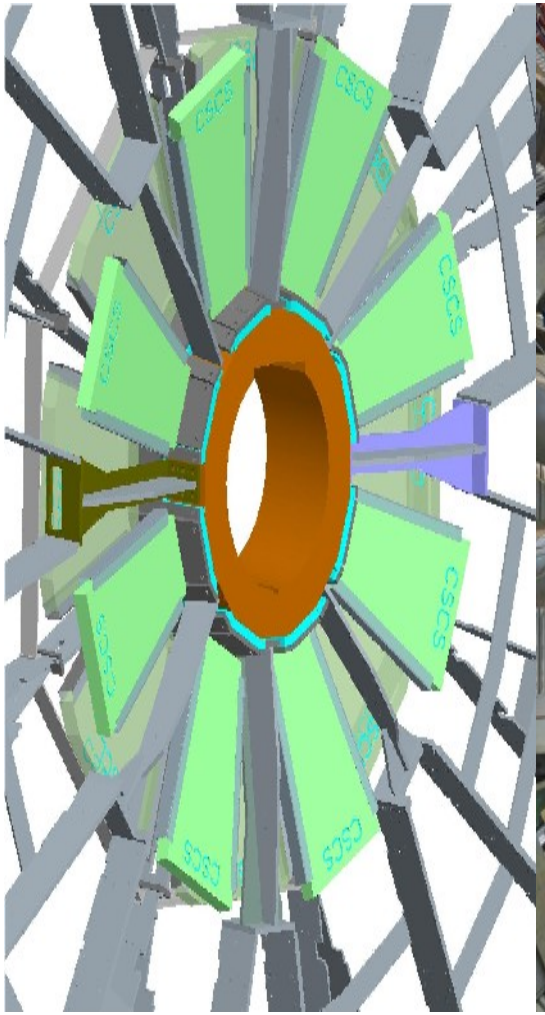
Higher interaction rate with same rate to tape. Bigger events due to pile-up.

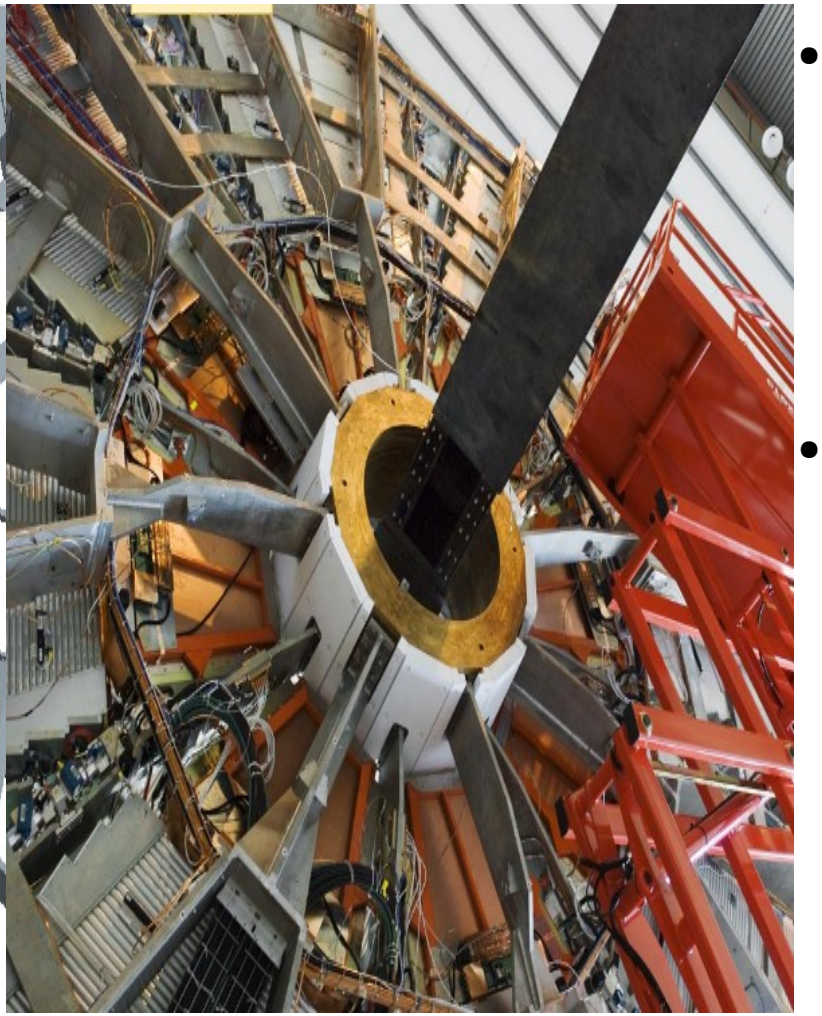


Phase 1 other than TDAQ

- Muons
  - Forward Cathode Strip Chambers (CSC) were de-scoped from 8 layers to 4 layers in present detector
  - Present CSC system looks marginal at $3x10^{34}$.
  - But, muon performance is background driven, not signal driven. Large uncertainty on rates. X5 safety factor used in design. Won't really know what is needed until after some running.
- Pixels
  - Pixel performance is signal driven, background irrelevant.
  - At $3x10^{34}$ present inner layer is inefficient
  - Radiation damage after 300-500 fb^{-1} is significant at inner layer
  - Additional degradation due to accumulated failures may have big impact on physics.

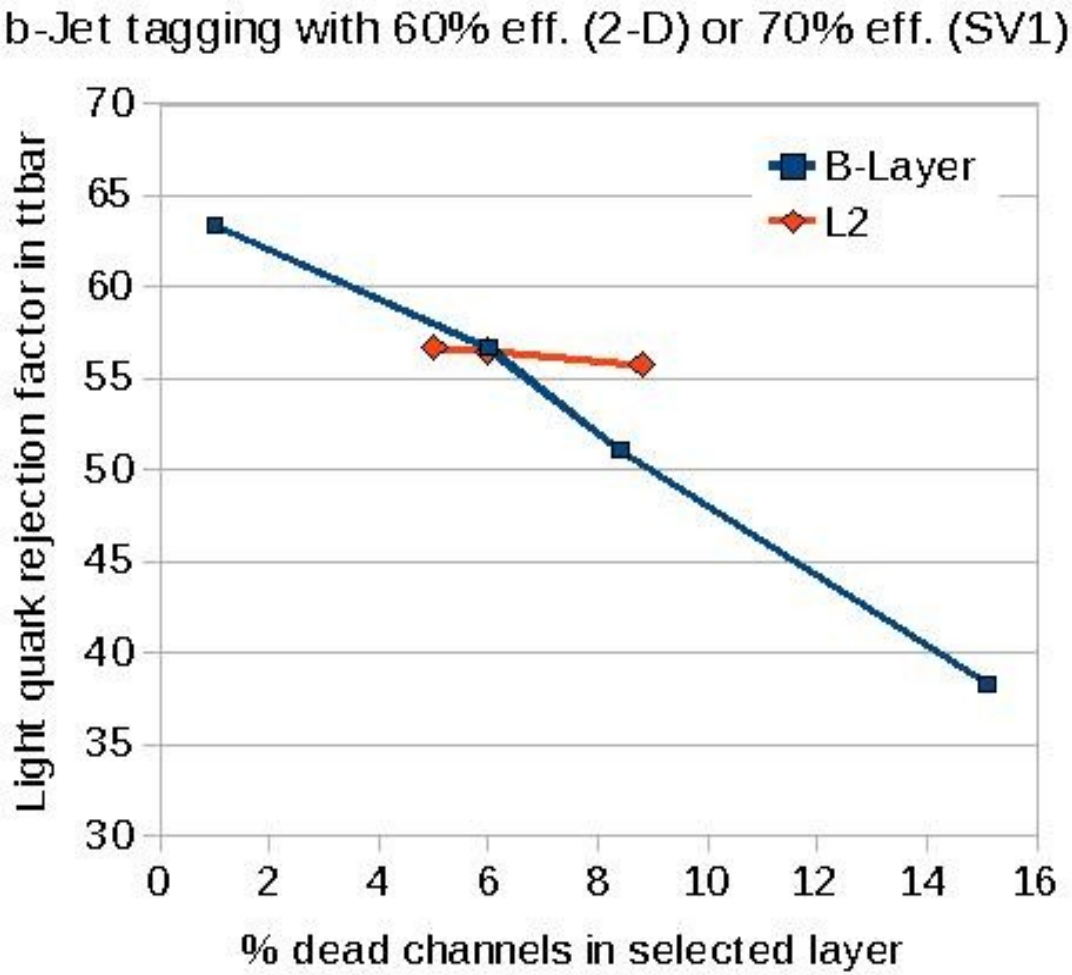
Phase I CSC



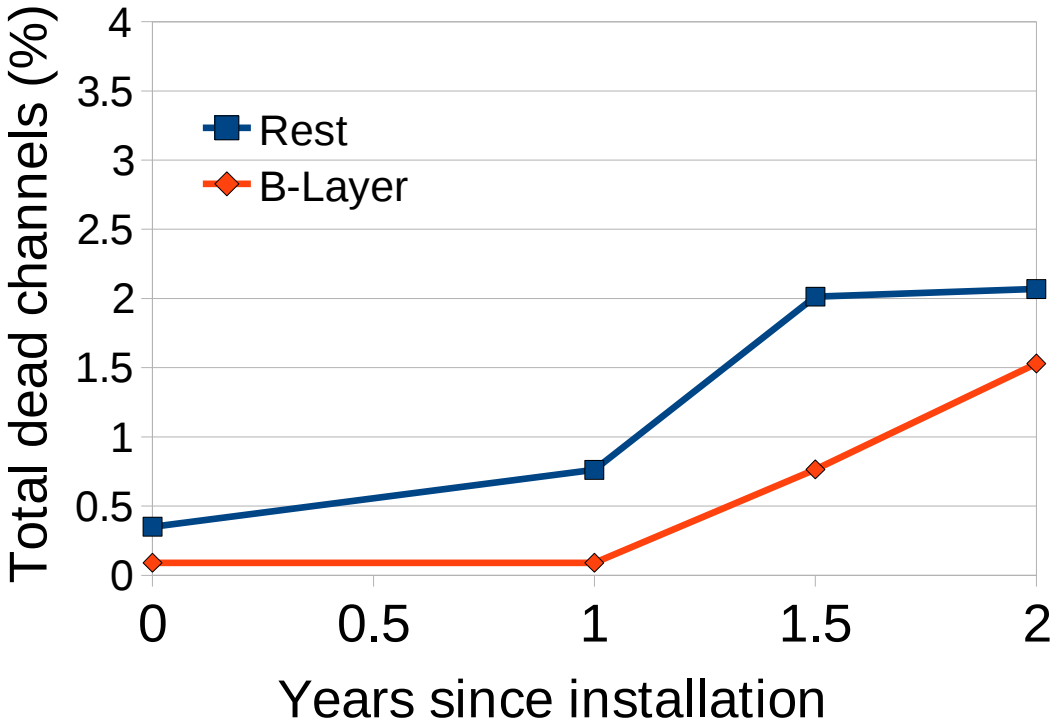


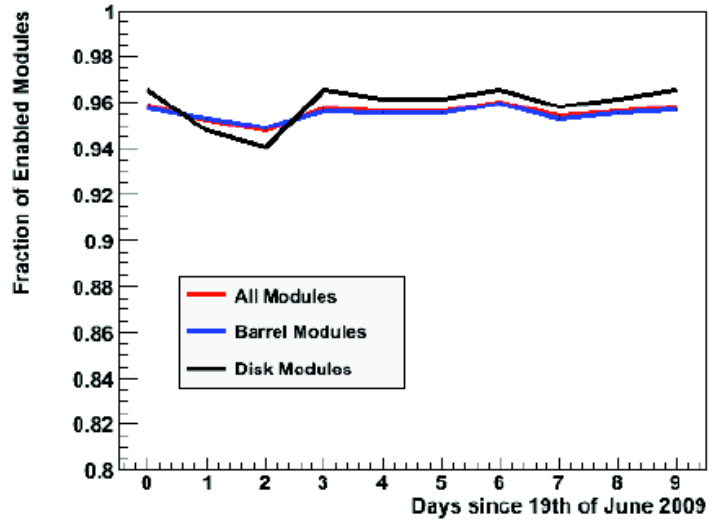
- Could use same technology, but installation difficult (ship in a bottle assembly)
- R&D into new technologies that would also work for phase II
  - eg. Micromegas

Physics impact of dead pixels



State of present pixel detector



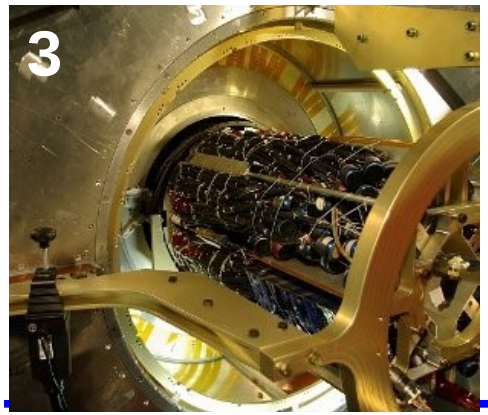


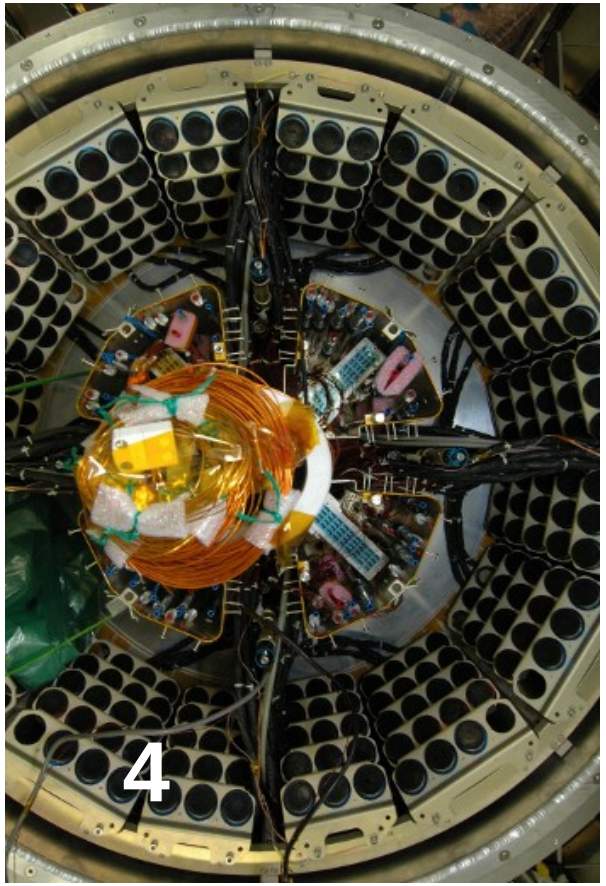
June 09 cosmic run pixel live fraction

- On-detector faults (no access for repair is possible)
- Excludes leaks in cooling circuits, which so far all can be operated

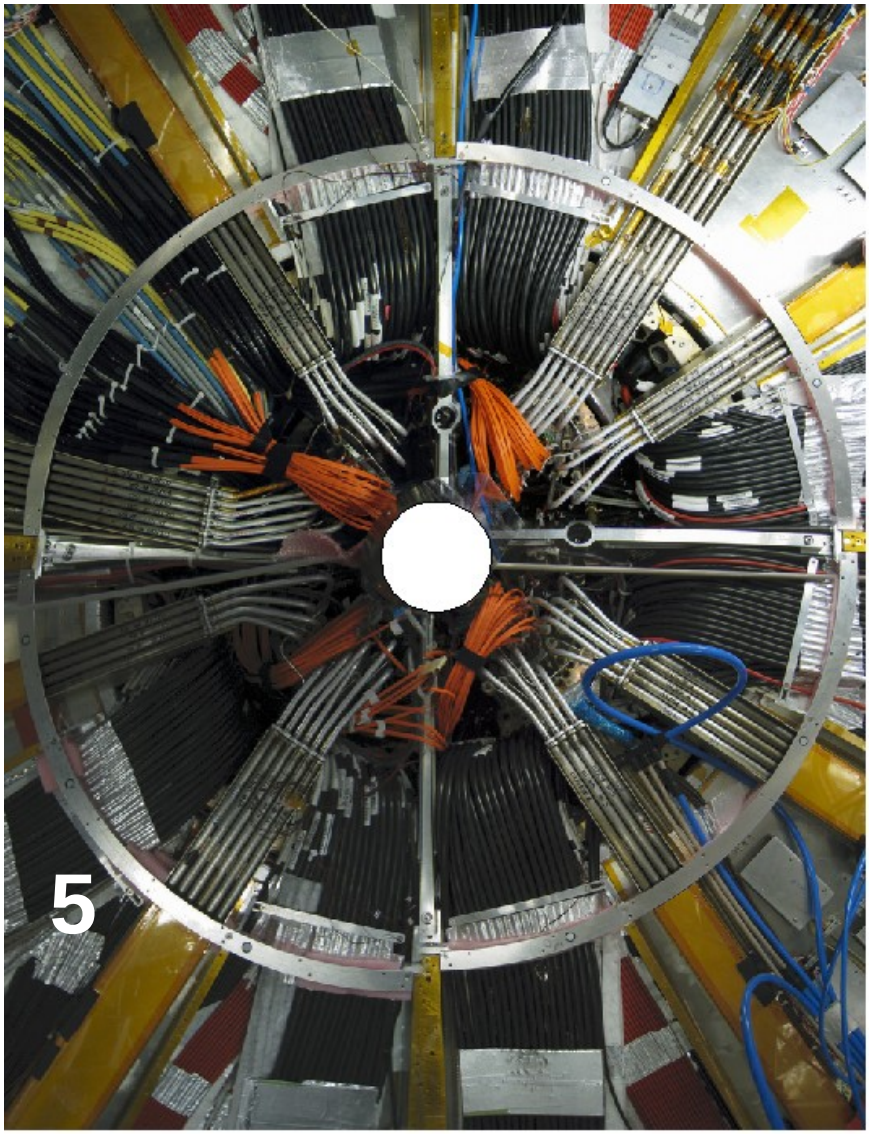
ATLAS pixels are inaccessible.

- Long installation/removal time.
- Must break accelerator vacuum.

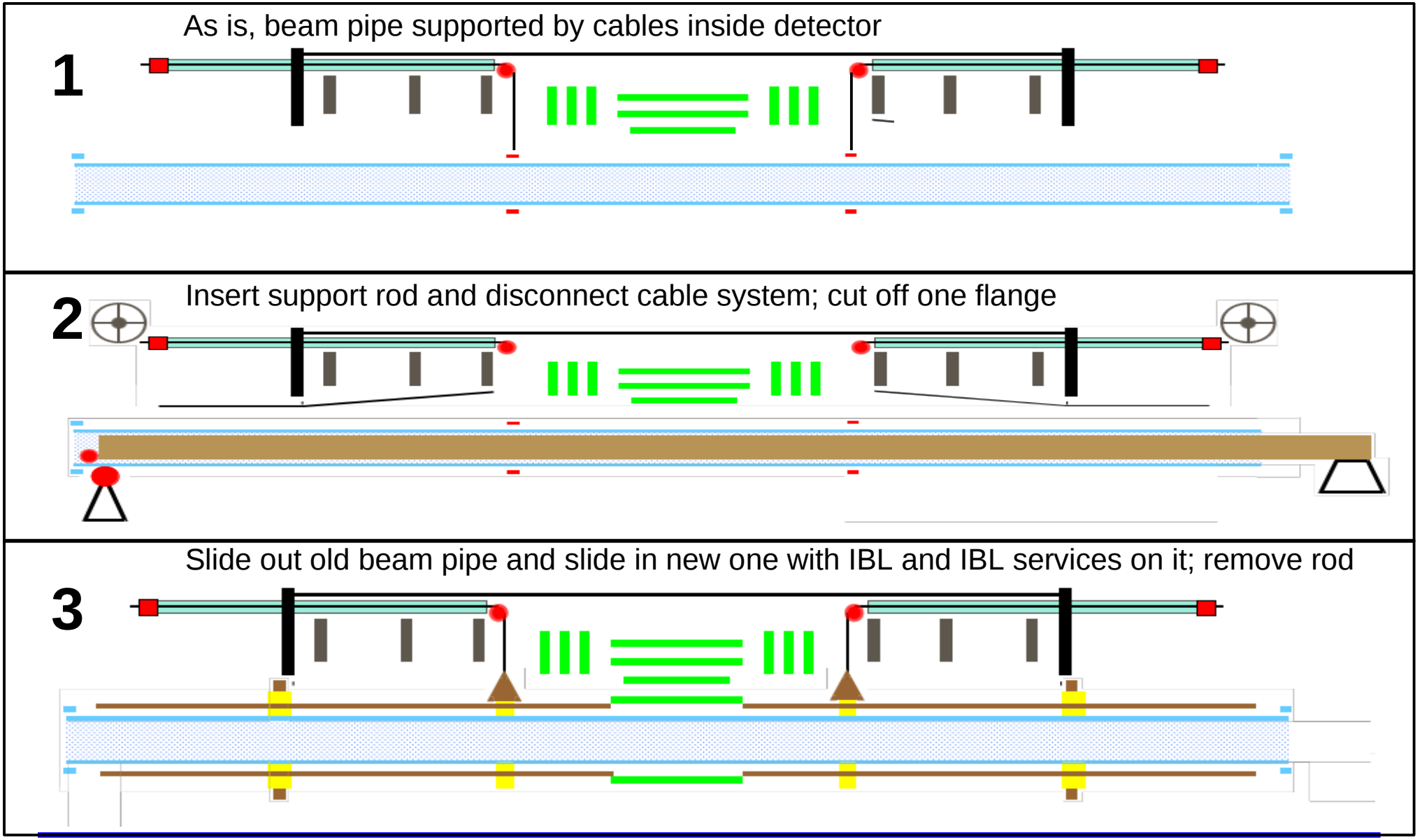




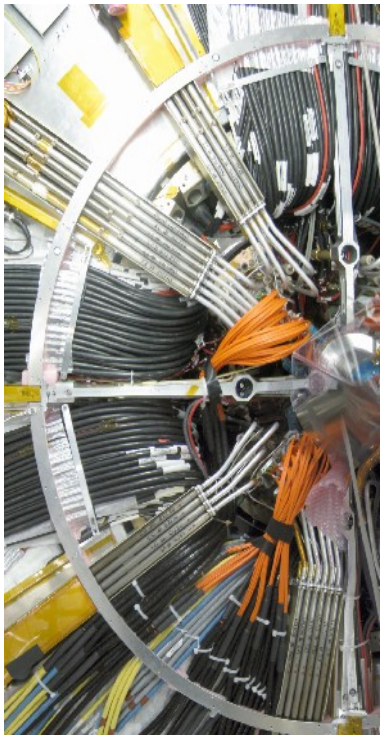
10 weeks



IBL concept

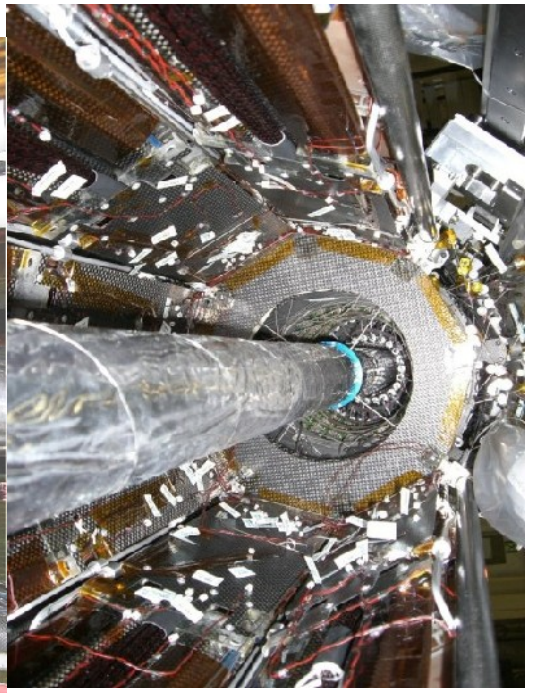

As is, beam pipe supported by cables inside detector
1
Insert support rod and disconnect cable system; cut off one flange
2
Slide out old beam pipe and slide in new one with IBL and IBL services on it; remove rod
3

A trip along the beam pipe



Z=-4m,
view towards IP

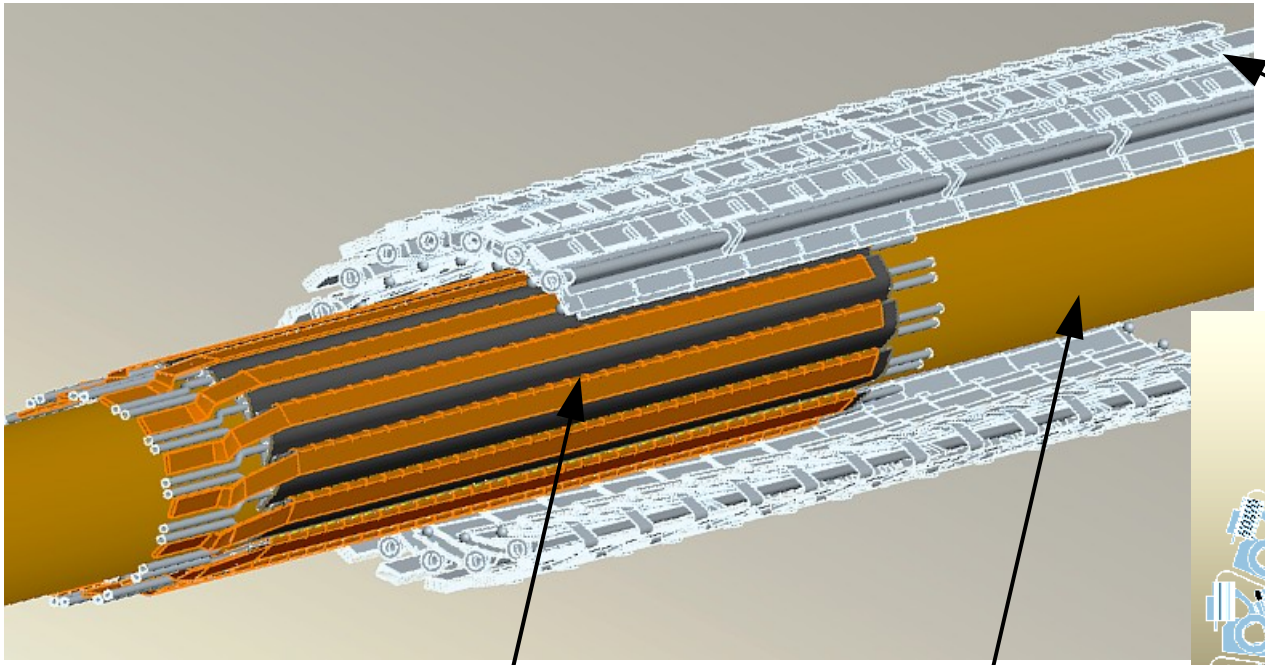
Z=-3m,
Section



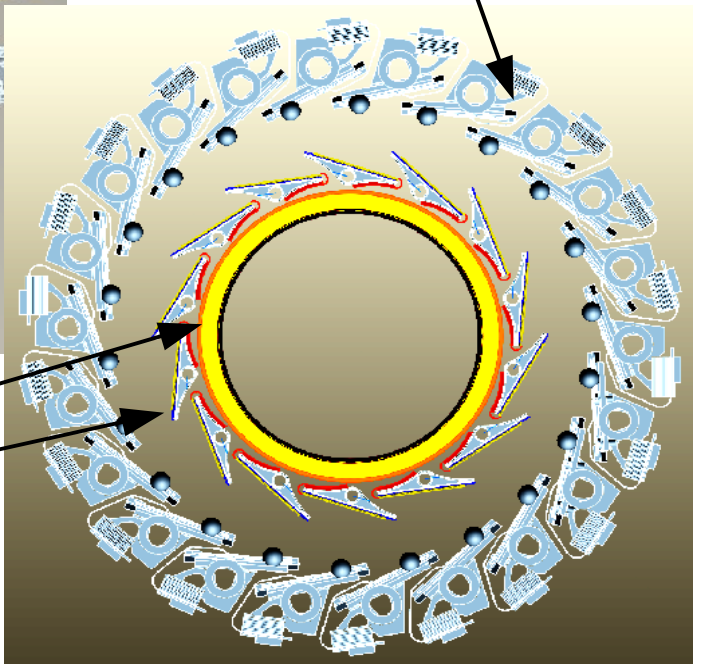
Z=-2m,
towards IP

Z=-1.4m,
towards IP

IBL design



Existing B-layer



New beam pipe

IBL mounted on beam pipe

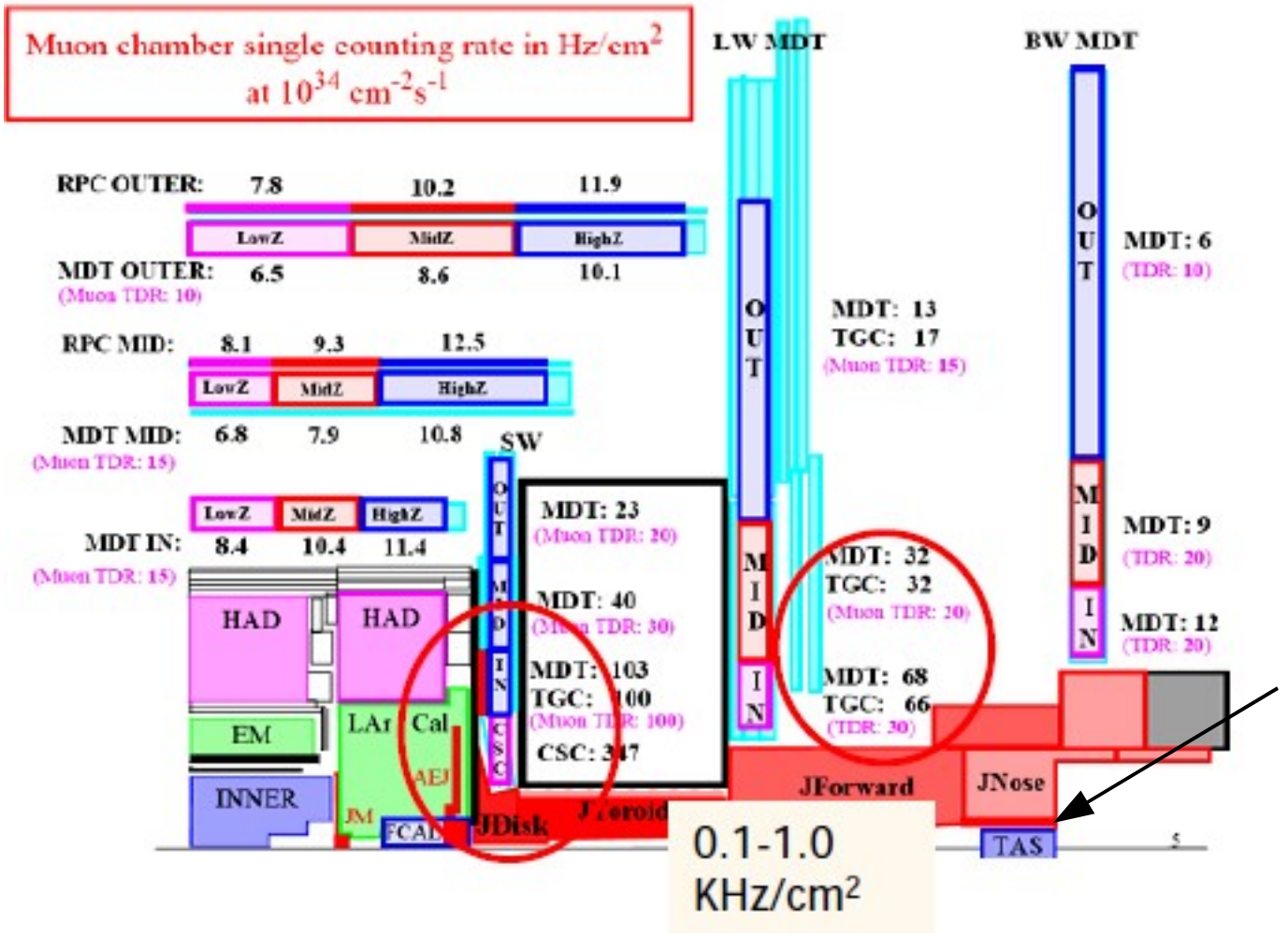
Smaller profile thanks to new chip format (FE-I4) and new mechanical structures.
New sensors with higher radiation tolerance
Smaller pixels and new readout architecture for higher rate operation

Phase 2

Phase 2 other than TDAQ

- High background areas in muon system
  - need shielding and / or new chambers
- LAr electronics
  - Rate, I/O, radiation damage
- Tile calorimeter electronics
  - Rate, radiation damage
- Completely new inner detector
  - Existing detector projected to be significantly damaged by start of phase 2
  - Need to replace regardless of beam scenario
- Letter of intent describing full scope is planned for Spring '10

Muon backgrounds



In Phase 2

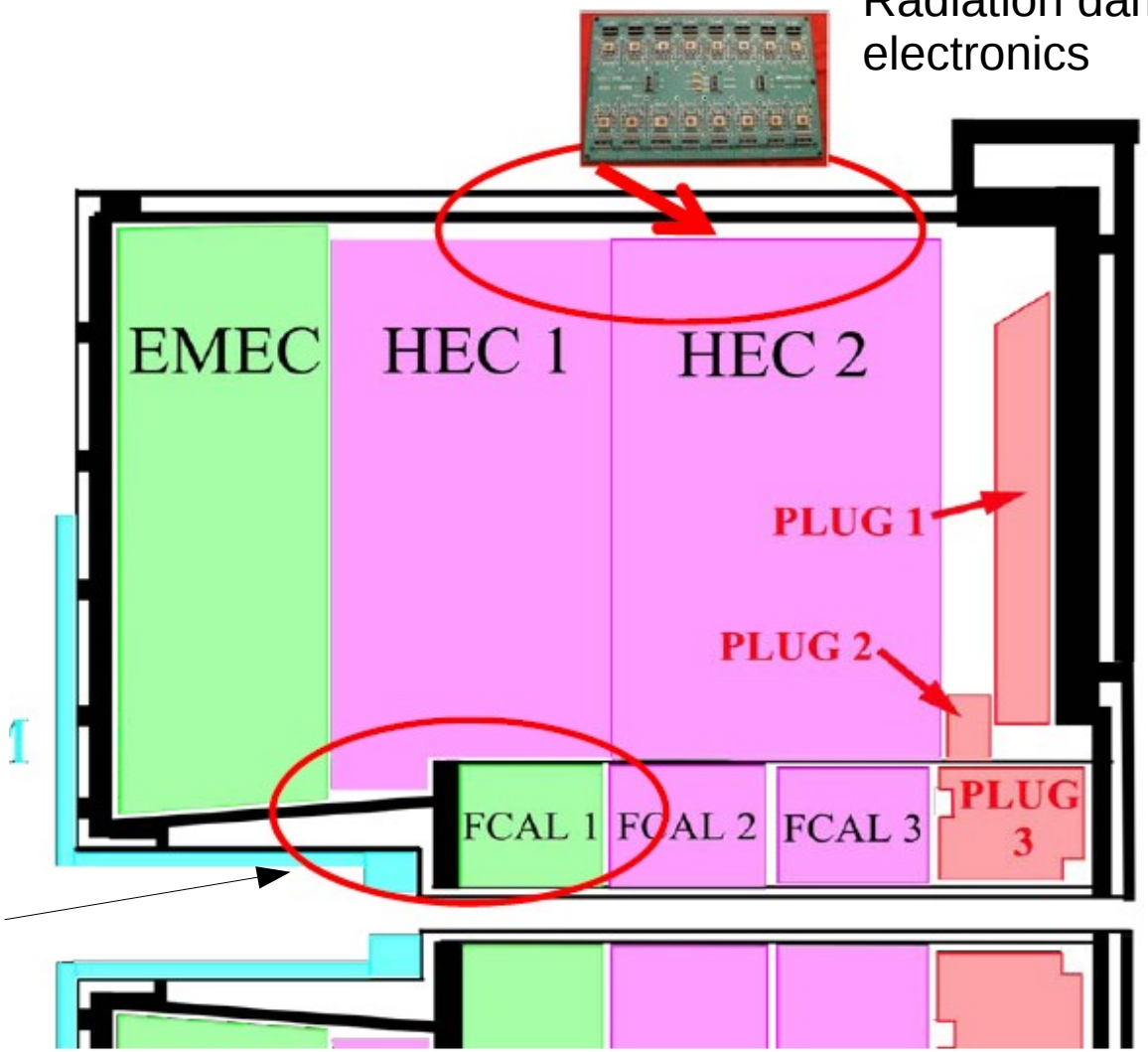
Moderator could be added in a few places

Shielding configuration could be optimized here

Considering all Be beam-pipe through ATLAS

Liquid Argon concerns

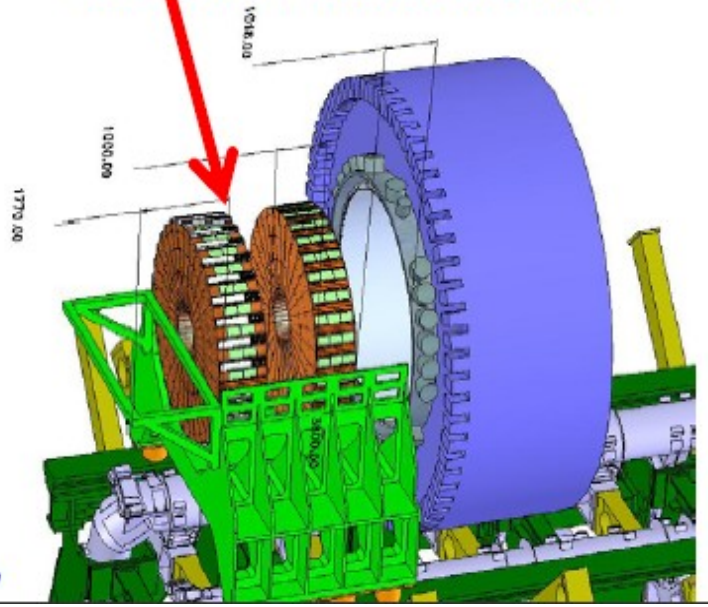
Radiation damage to electronics

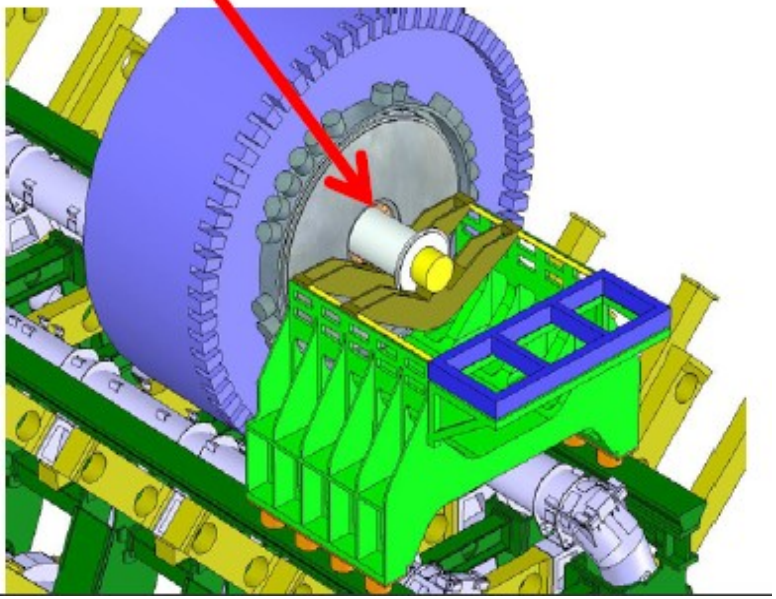


Boiling of LAr at very
High hit rates.
Signal drops quickly

FCAL options

- Option1
  - HEC cold electronics to be replaced,
  - Cold FCal replaced by a new one.
- Option 2
  - HEC cold electronics does not need to be replaced,
  - Cold FCal replaced by a new one, large cold cover needs to be removed.
    (If FCal cabling is modified, large cold cover may not need to be removed.)
- Option 3
  - HEC cold electronics does not need to be replaced,
  - Mini-FCal in front of cold Fcal



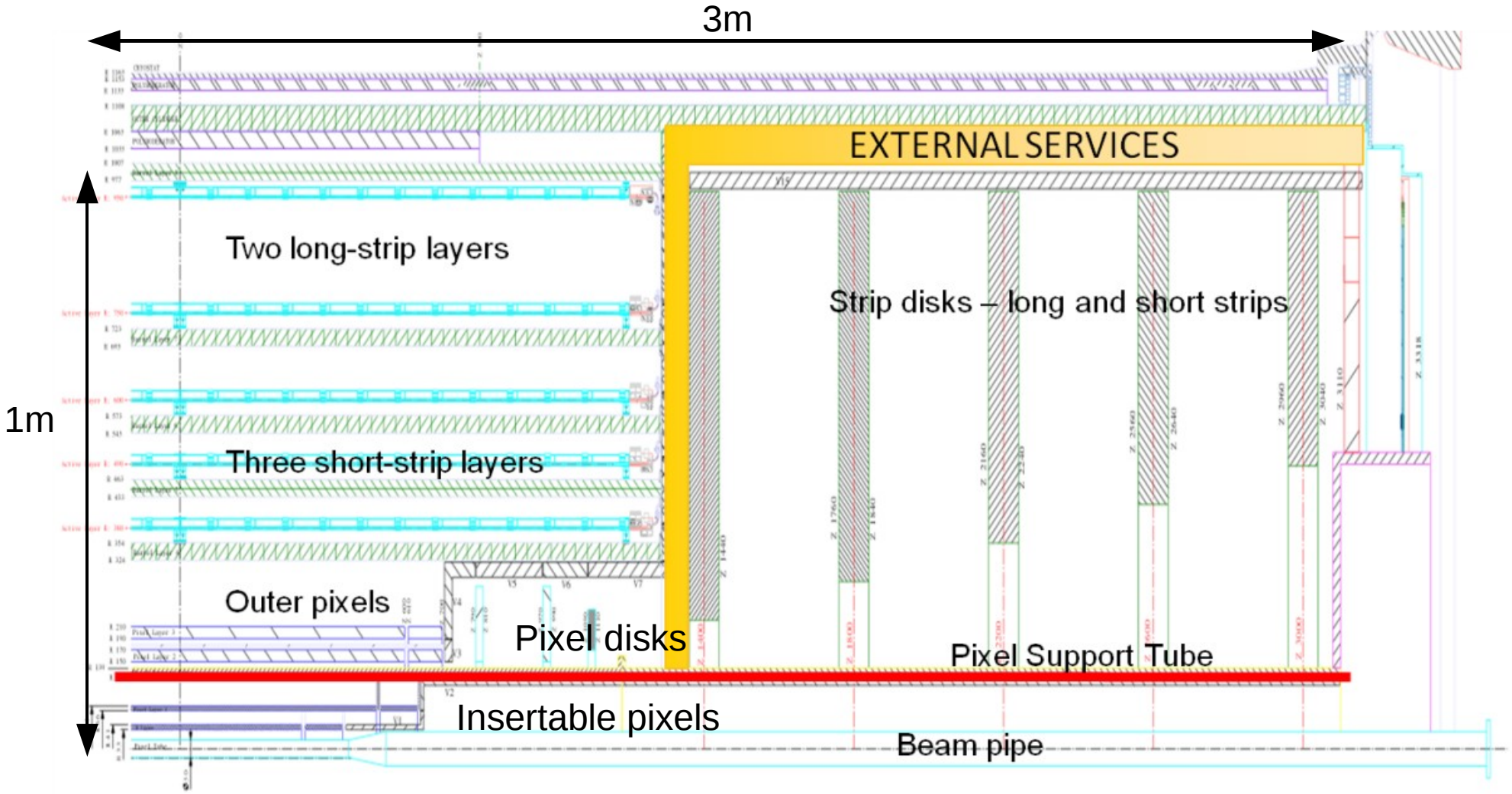


06/17/2009 M.Nessi - CERN

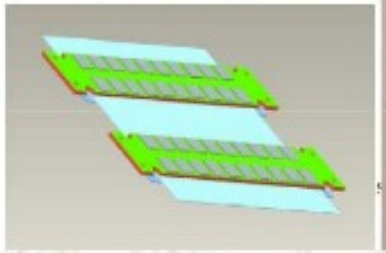
Inner detector

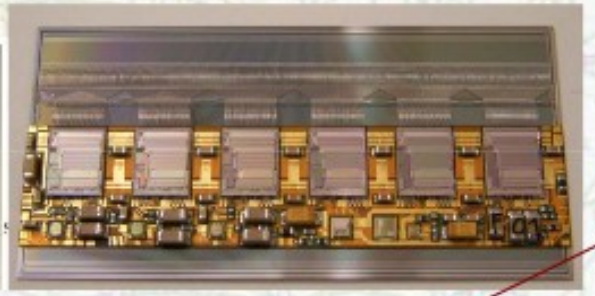
- After about 700fb^{-1} must replace entire inner detector due to radiation damage, regardless of ensuing luminosity profile
- Baseline is an all silicon tracker with same or better physics performance as now, but with up to 400 interactions / crossing and 3000fb^{-1} accumulated.
- Many baseline choices depend on requirements that may change. Design will need to adapt when this happens.
  - Most salient example is trigger requirements.
  - Different trigger options under consideration.
- Detector is mechanically 2 regions:
  - Main detector, which includes 2 or 3 pixel layers and disks.
  - Insertable pixels: innermost 2 layers.

Current working layout for tracker

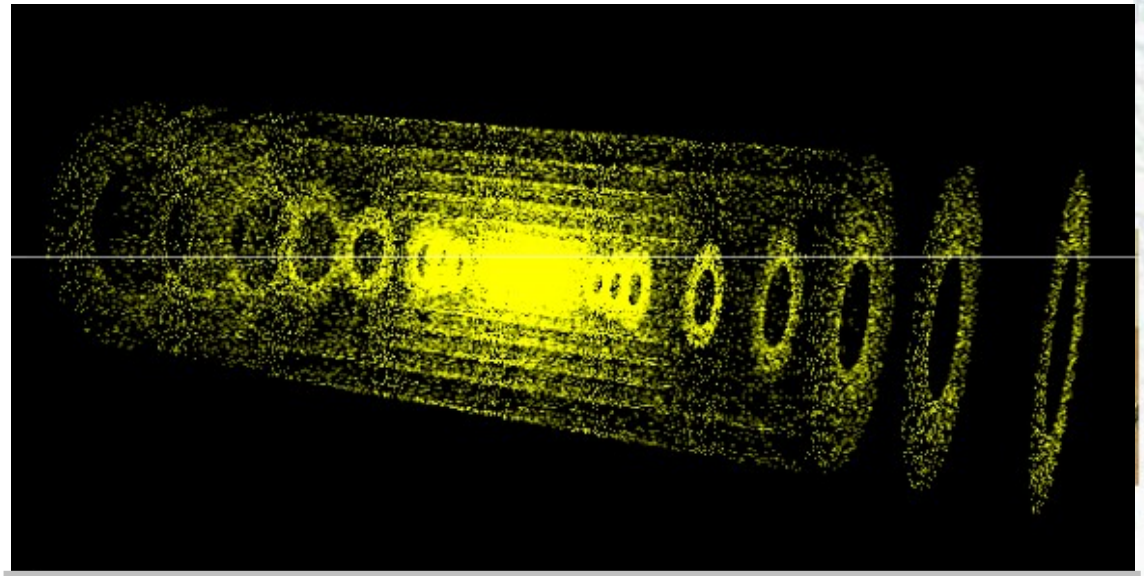


Strip elements

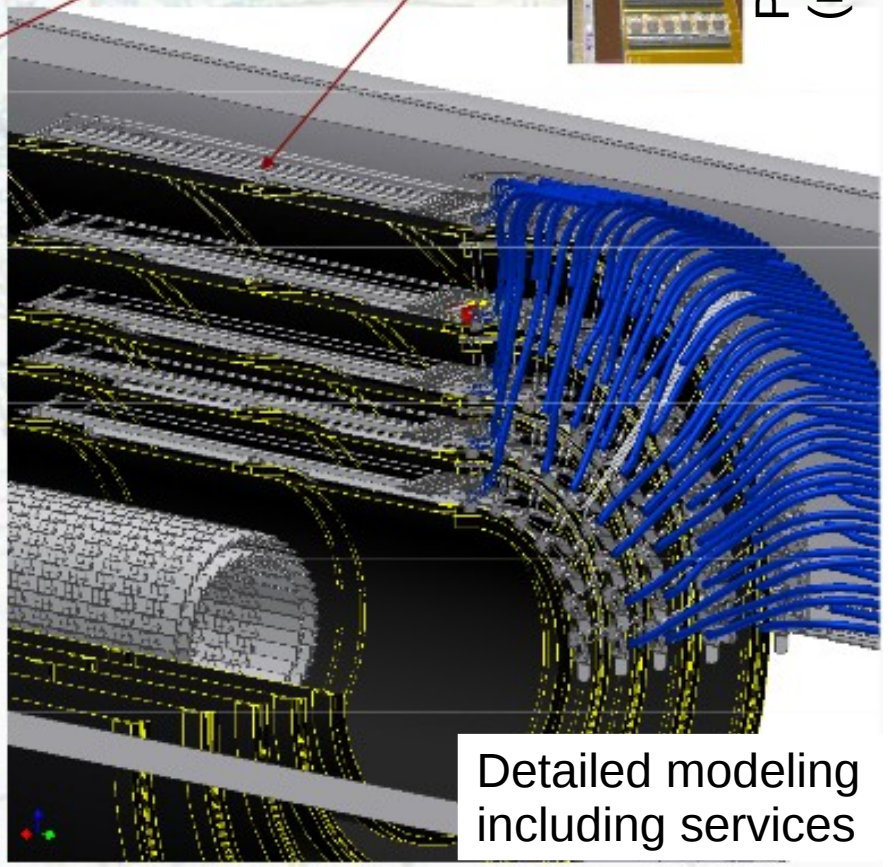




Prototype stave
(more later)

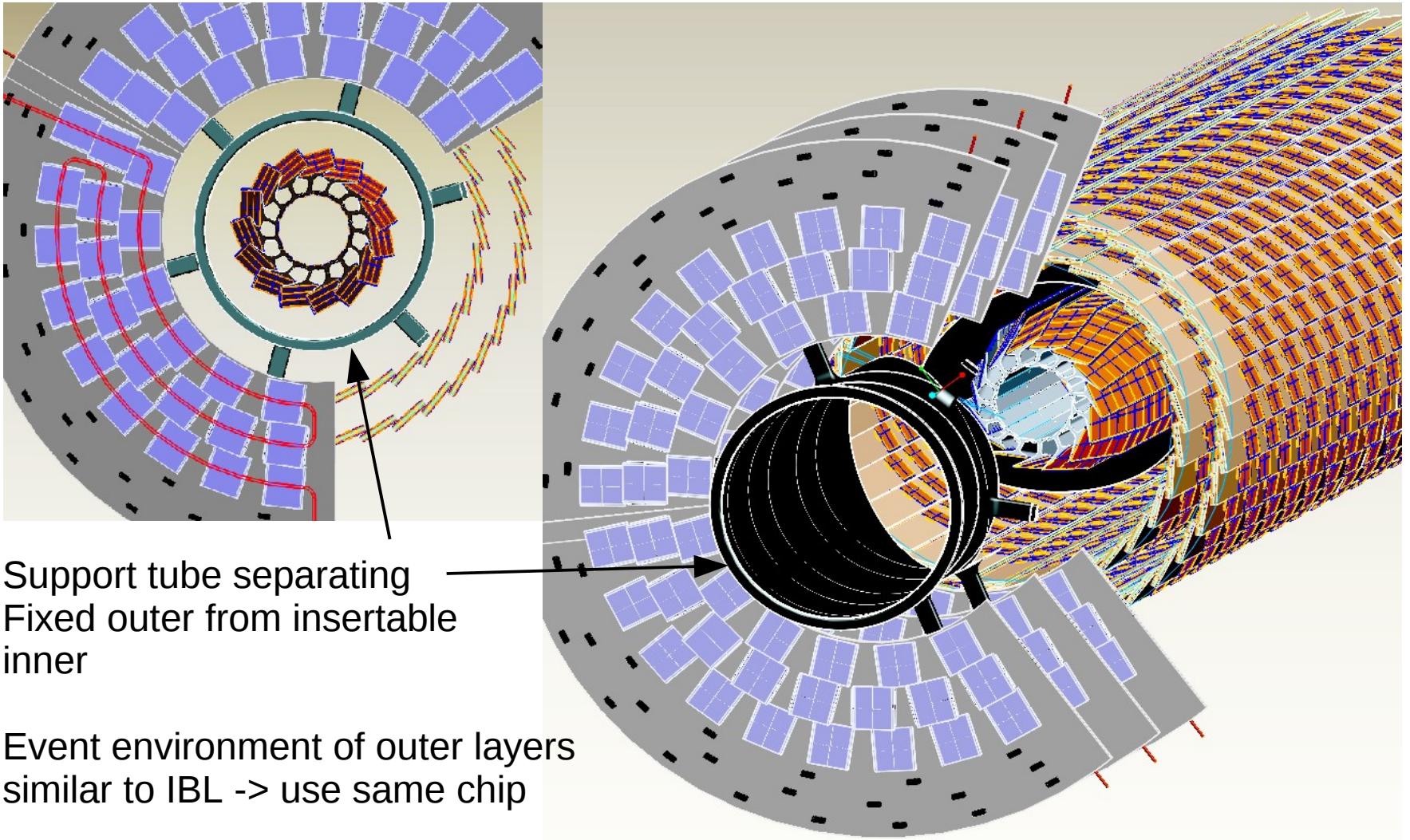


Hits from 400 interactions with detector material



Detailed modeling including services

Pixel elements



Support tube separating Fixed outer from insertable inner

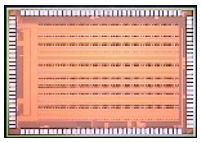
Event environment of outer layers similar to IBL -> use same chip

Phase 2 main tracker enabling technologies

- Higher voltage, more radiation tolerant, cheaper (n on p) planar sensors (both strips and pixels)
- Large format (FE-I4) pixel readout chip for cheaper large area pixels
- New (possibly larger format) ABCnext strip readout chip
- GBT data multiplexer & optical link
- High bandwidth, low mass micro-twinax
- Serial power distribution and/or DC-DC conversion
- Electro-mechanical integrated staves & disks (both strips and pixels)
- New high thermal conductivity, low mass carbon foam
- CO_2 evaporative cooling
- Trigger stave? TBD

FE-I4

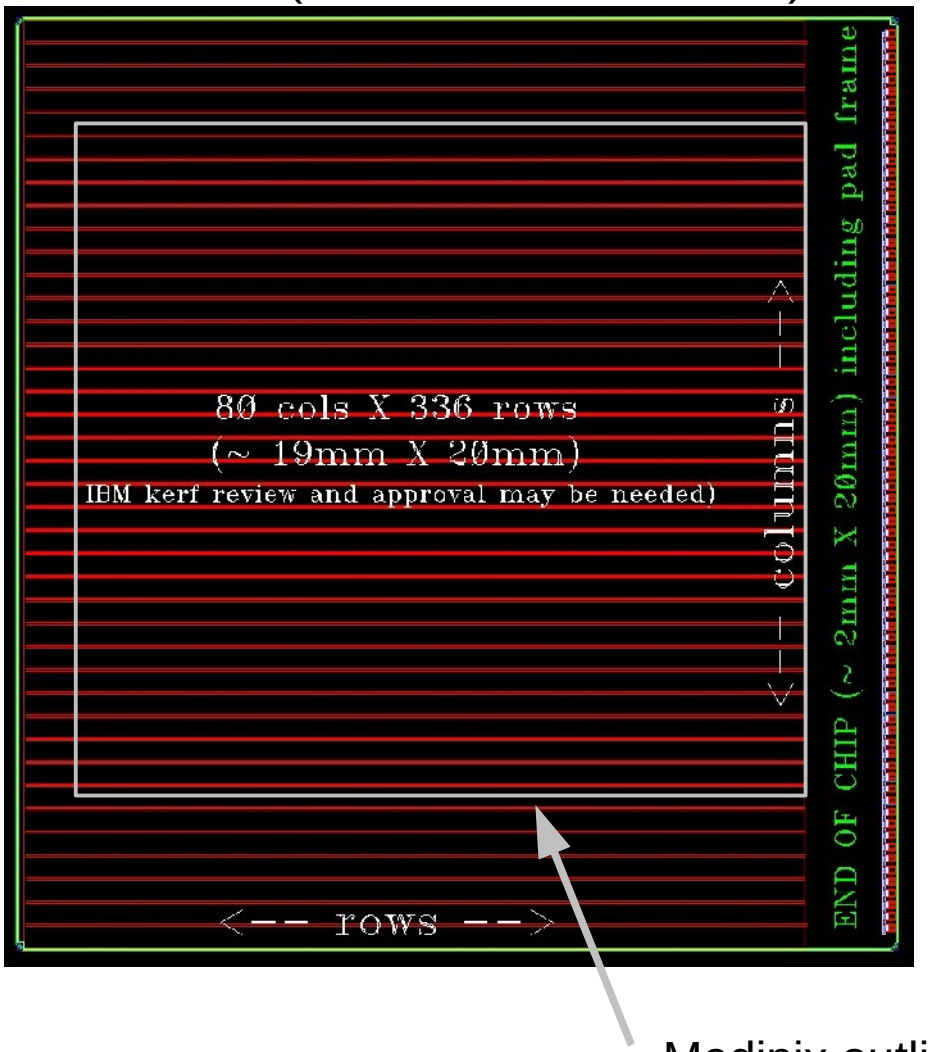
50u x 250u pixel
130nm feature size, ~100M transistors
<1% Inefficiency at IBL max. luminosity
Built-in x2 DC-DC and linear regulators
Lower current per unit area than FE-I3
Rad hard to >200MRad



FE-I4 analog demonstrator (2008)

FE-I3 (present detector)
50u x 400u pixel

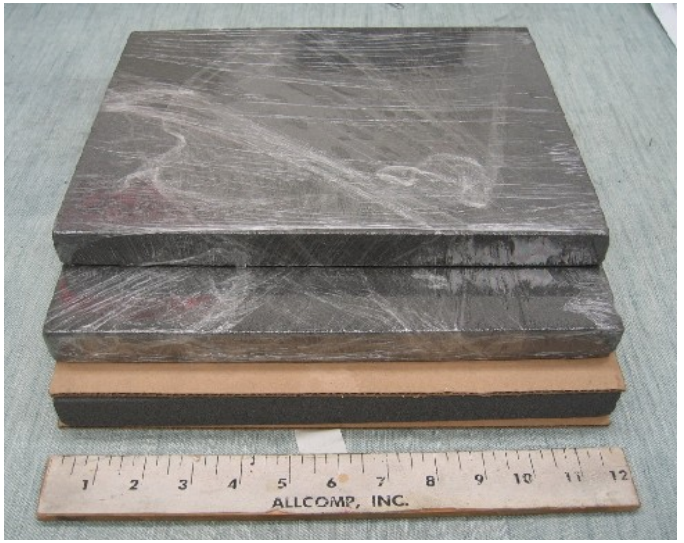
FE-I4 (to be submitted Fall 09)

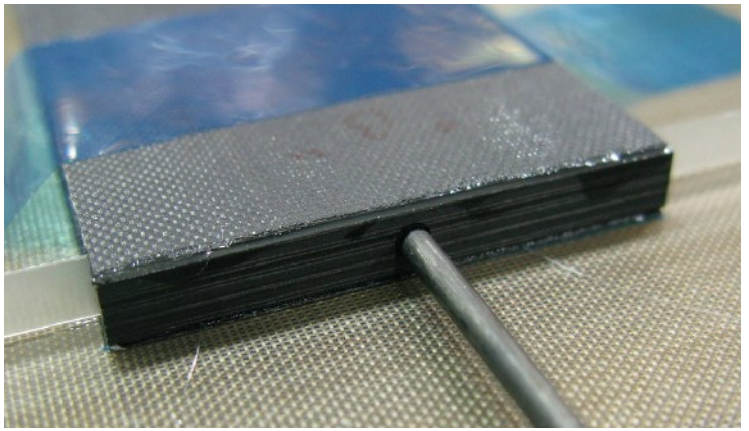


Medipix outline

High thermal conductivity, low mass foam

- Comes from Allcomp, Inc. (with SBIR support)
- Latest version has ρ ~ 0.2 g/cc and K ~ 20-25 W/m/K
- Made in blocks 1”x1”x12”
- Nominal pore per inch is 100 but can tune





Pixel stave core with Ti pipe

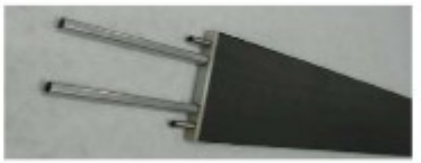
Integrated stave – strip format

60 cm, 9 cm strip, 6 segments/side, based upon CDF Run2b architecture

Stave-06

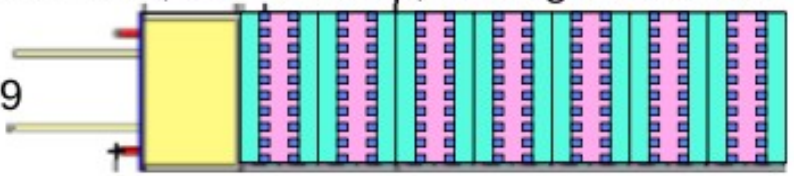
1 meter, 3 cm strip, 30 segments/side 192 Watts, ~2.4 % Xo

Stave-07



1.2 meter, 2.5 cm strip, 48 segments/side ~250-300 Watts 1.7 – 2.4 % Xo

Stave-09



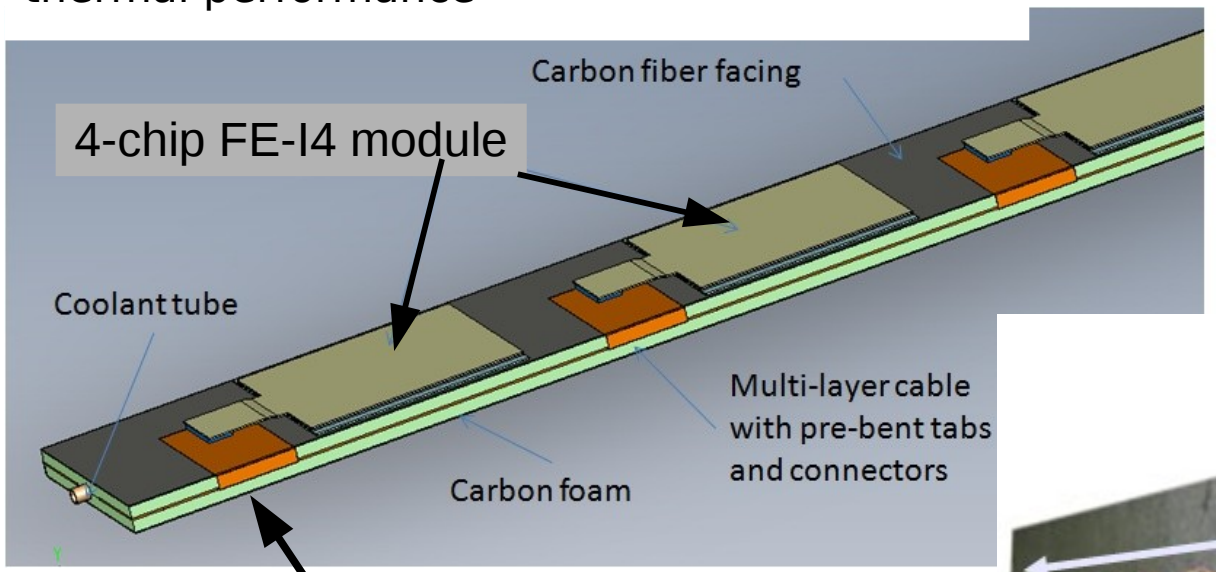
etc, etc, etc…. ATLAS design

Trigger Stave

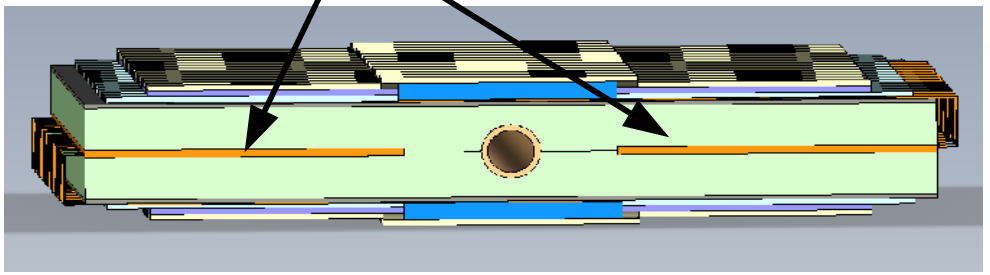
etc….

Integrated stave – pixel format

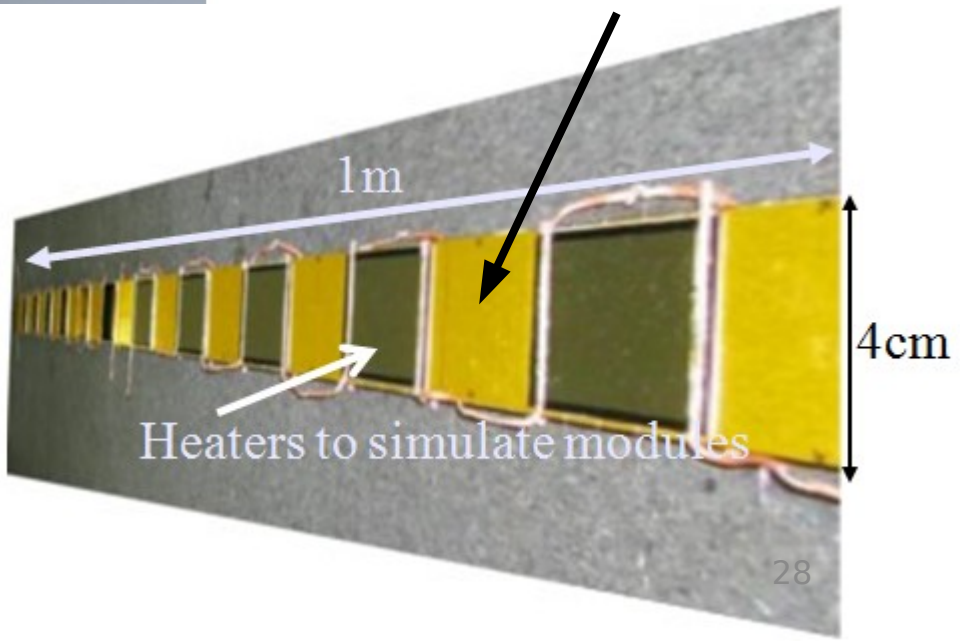
Current buried cable design with better thermal performance



Cable (~ 0.5mm thick)

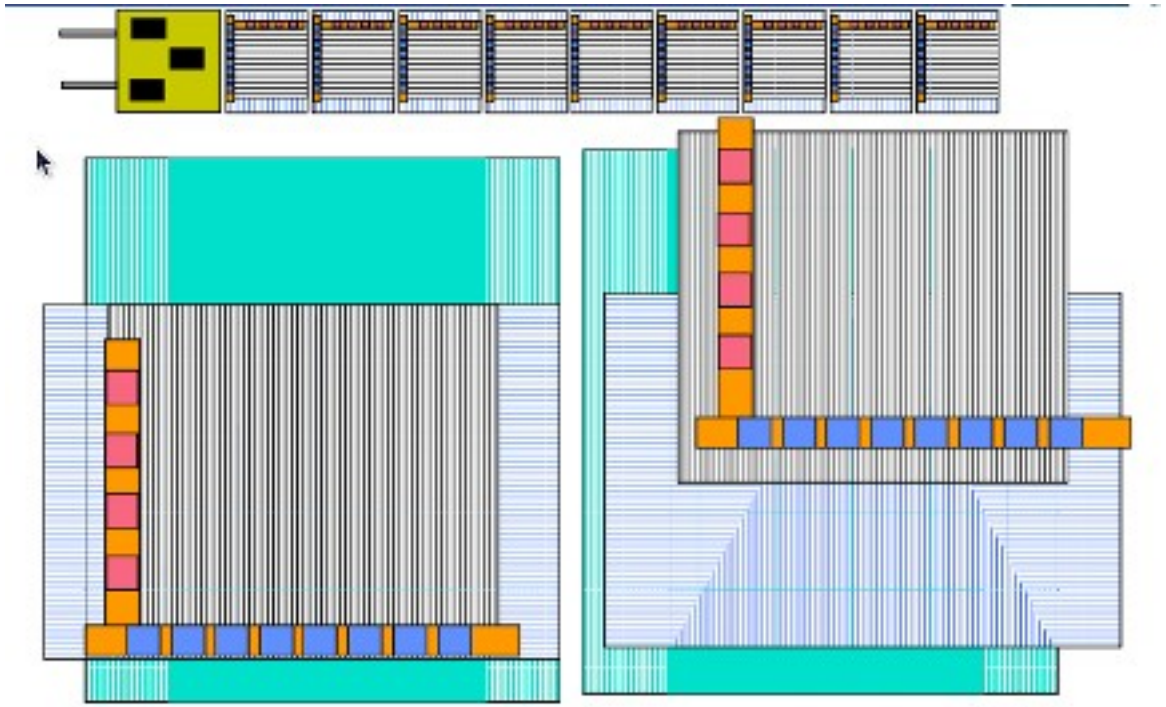


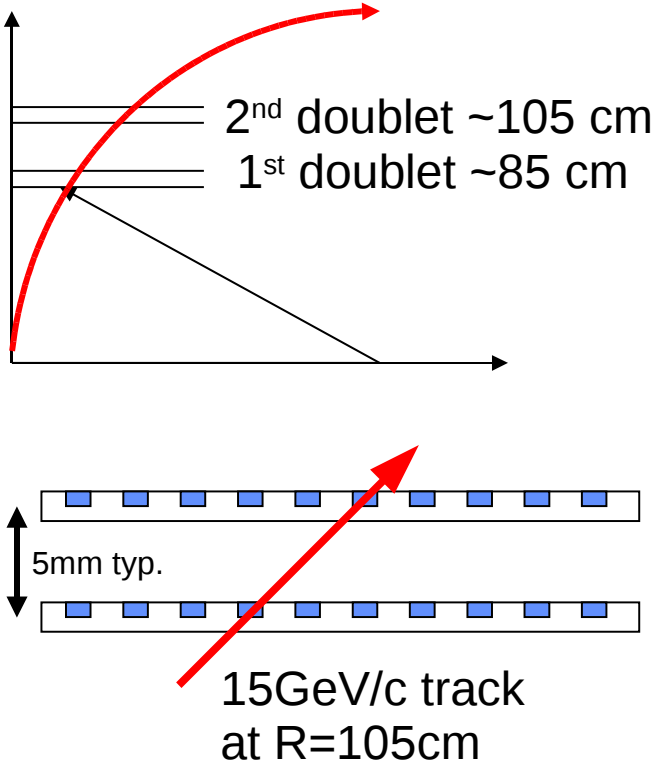
First thermal prototype Bus cable (similar concept to silicon strip staves) glued on top of mechanical stave



“Trigger layer” option

- A regular stave uses hits from both sides to determine phi and Z (from stereo angle)
  - 2 data points and 2 DOF. Calculation of Z is done off-line
- A trigger stave uses hits from both sides to determine phi and incidence angle (no stereo possible)

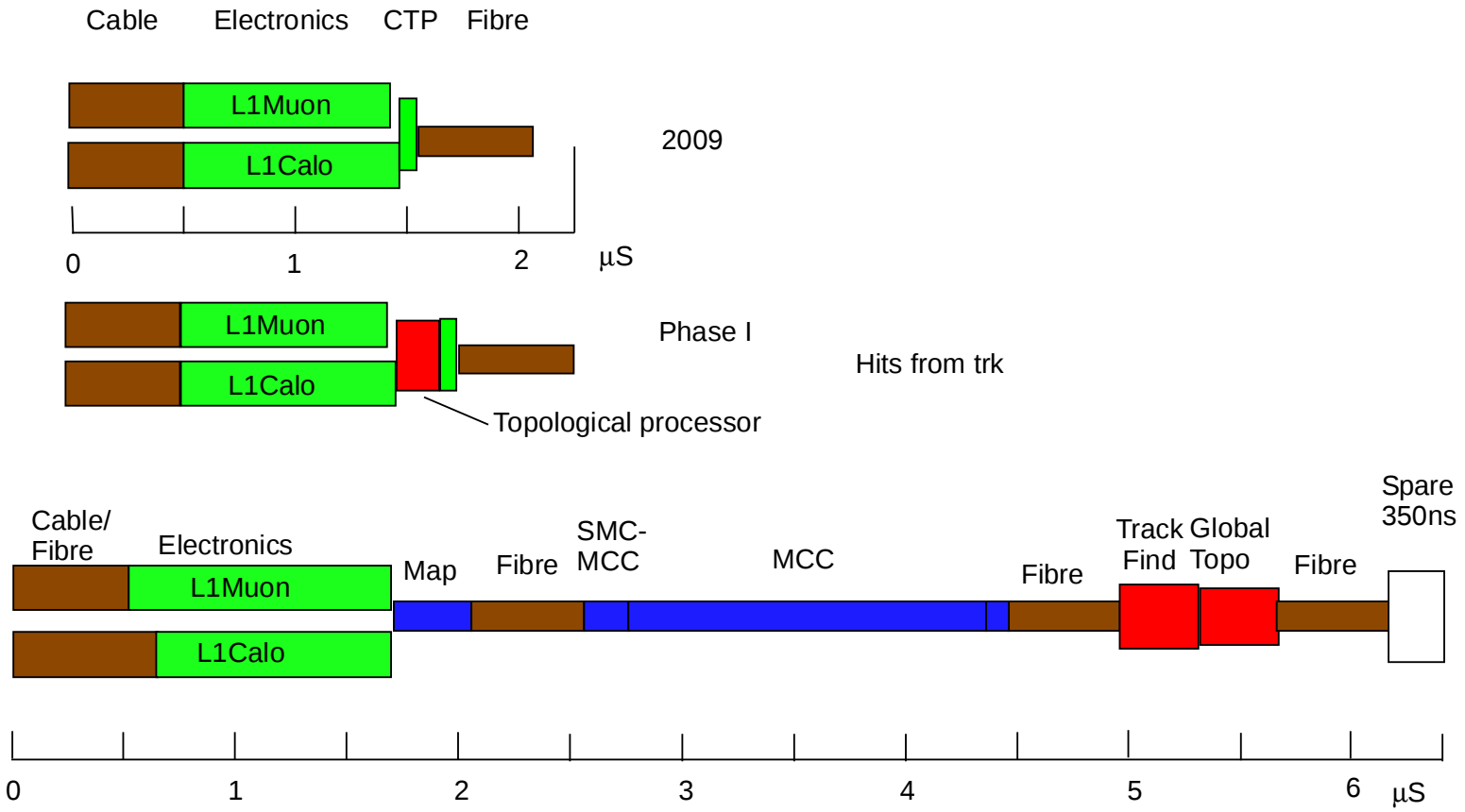




Track Trigger options

- As interaction rate increases, but data-to-tape rate stays the same, a better and better hardware trigger is needed.
  - Hardware because the data output bandwidth to LVL2 cannot increase arbitrarily.
- Adding track primitives to LVL1 can improve muons, electrons, potentially others
- OR, one can go to a 2-level hardware trigger, where only the 2nd level has track information
  - Presently favored approach by ATLAS trigger group
  - The data output bandwidth problem is solved by only reading regions of interest into the trigger
  - This does require longer latency for reading all data from the detector- OK if electronics will be replaced anyway.

Increase of trigger latency

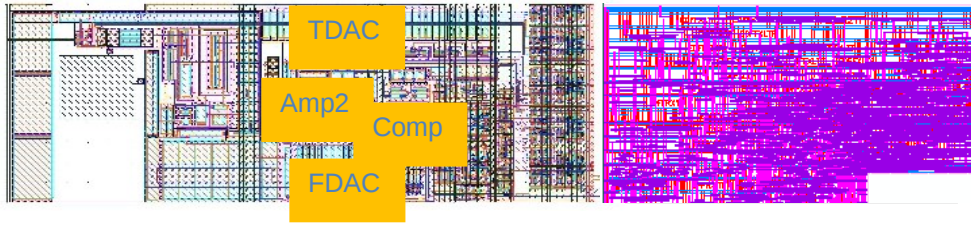


Insertable pixels enabling technologies

- Higher radiation tolerance sensors:
  - 3D, very high voltage planar, diamond.
- A further generation of pixel chip beyond FE-I4:
  - Smaller pixels to keep low occupancy
  - Cope with higher data rate with >99% efficiency
  - Could be 3-D integration, 65nm...
- A further generation of data multiplexer & optical link: Need >10Gb/s per unit.
- Cooling, foam, power distribution, as for main tracker.
- Carbon cooling pipe and/or still lower mass structures

Pixel size and event data memory

FE-I3, 4 bits / pixel



FE-I4, 20 bits / pixel

Does not scale with feature size

Scales with feature size

?

Beyond FE-I4, ~30 bits / pixel

Conclusions 1/2

- 2 phase detector upgrade path to cope with luminosity increases
- Trigger/DAQ upgrades in each phase a given
- Main instrument upgrades for phase 1 are IBL and forward muons (depending on actual backgrounds)
- TDR for Phase I and Letter of Intent for Phase II planned for next year.
- Significant work in all parts of the detector needed to reach 400 interactions per crossing

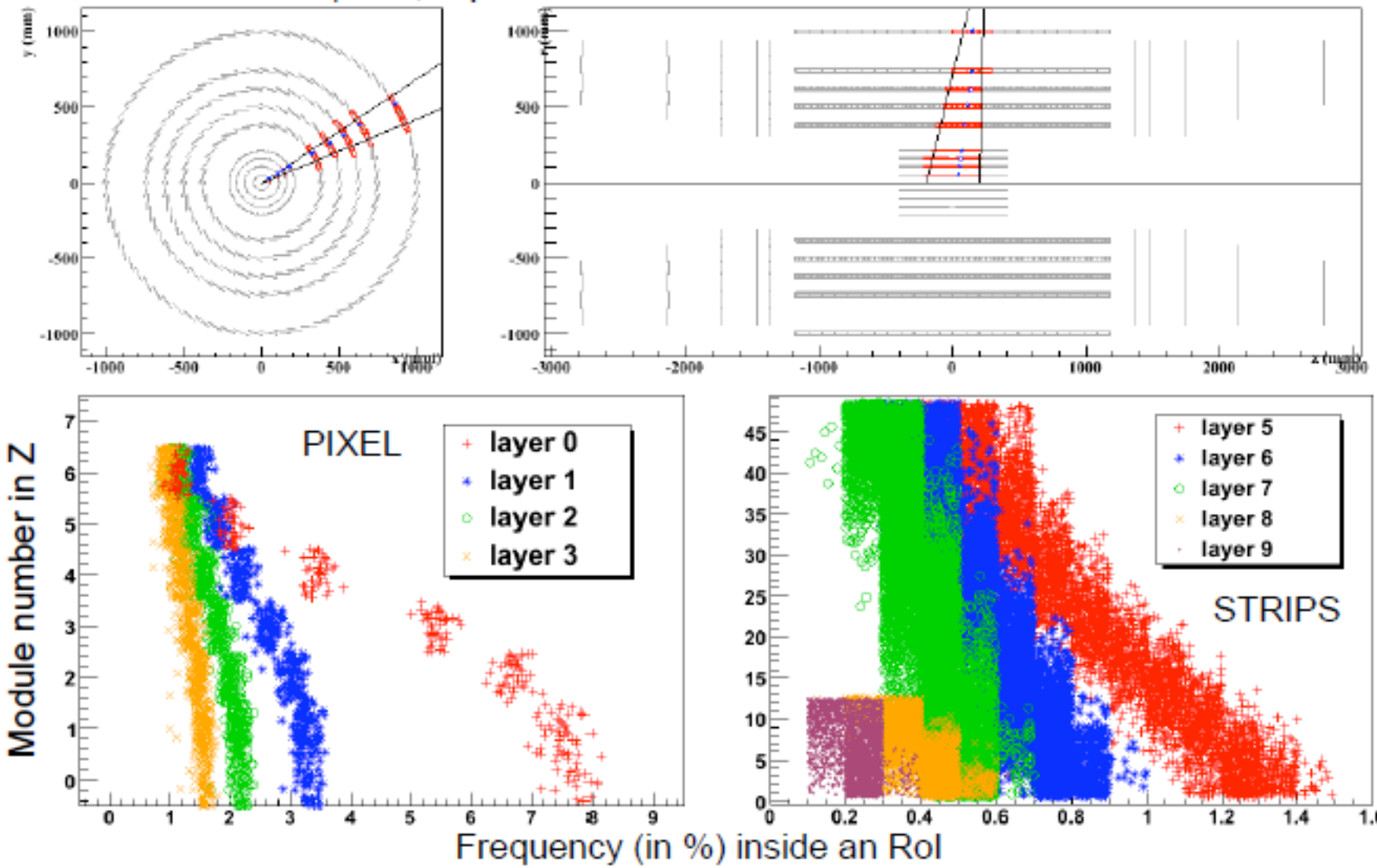
Conclusions – Phase 2 tracker

- 40M strips + 400M pixels outer, 100M pixels inner.
- Most main tracker enabling technologies already available or in advanced stages of R&D
  - Trigger layers an exception, but not required in baseline.
- Many technologies needed for insertable pixels are not yet there. Significant R&D still needed.

BACKUP

Regional Readout studies

RoI: Δϕ=0.2, Δη=0.2 at Calo Δz=40cm at beamline



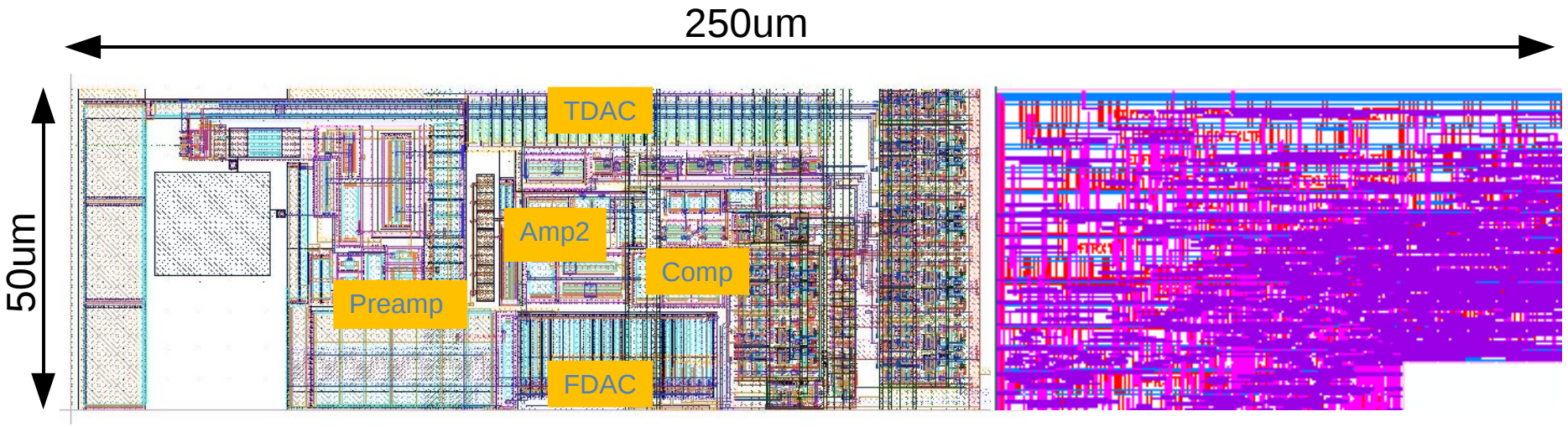
Some new features in FE-I4

- Biggest chip in HEP to date
  (Lower cost for large area pixels)
- Greater fraction of the footprint devoted to pixel array
  (=> move the memory inside the array)
- Lower power
  (=> don't move the hits around unless triggered)
- Able to take higher hit rate
  (=> store the hits locally and distribute the trigger)

Region architecture

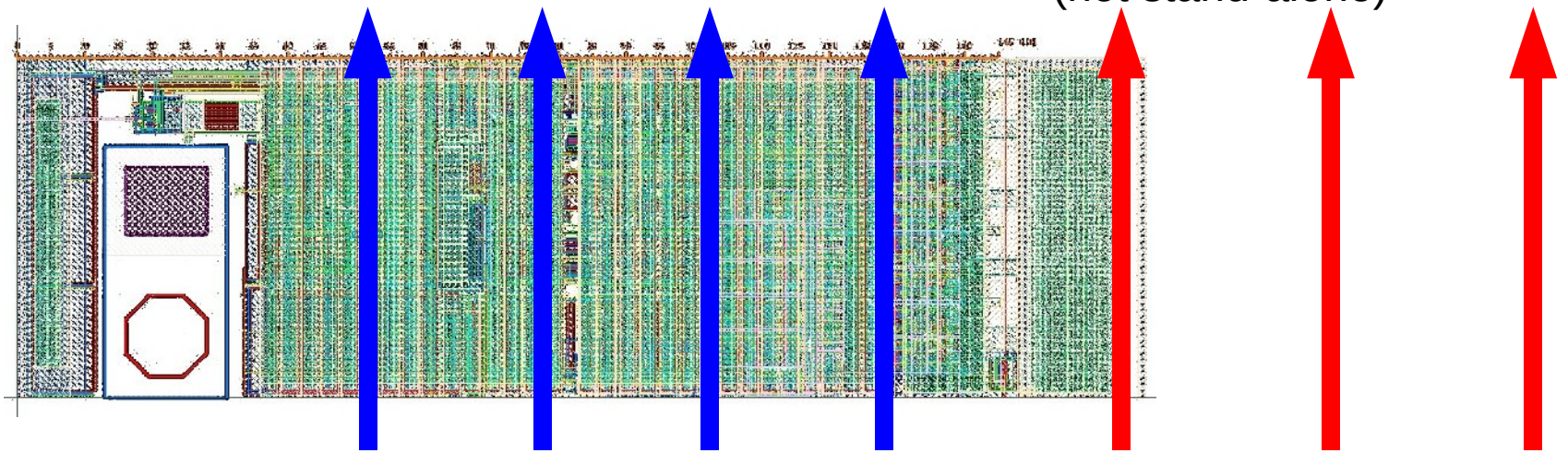
- Still able to resolve the hits at higher rate
  (=> smaller pixels and faster recovery time)
- No need for extra module control chip
  (=> significant digital logic logic blocks on array periphery)

FE-I4 Pixel Layout



Custom layout.

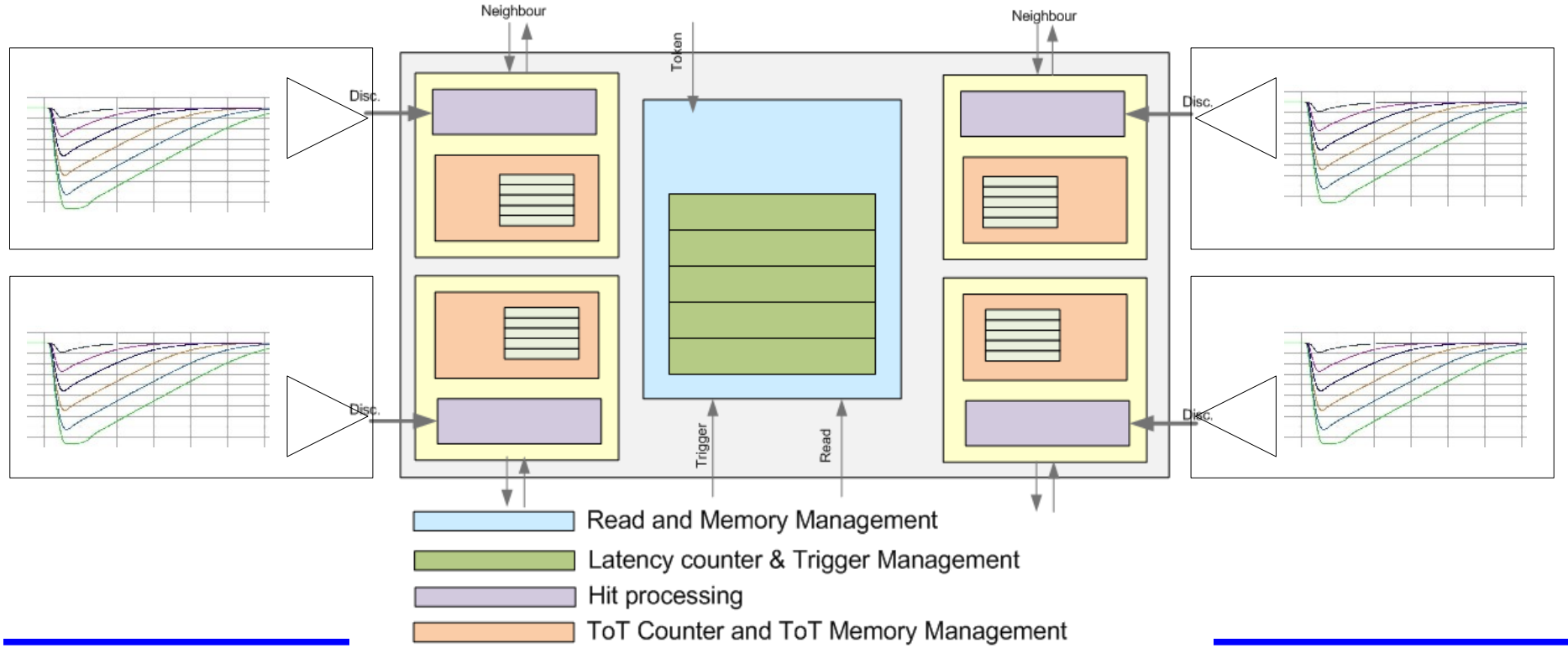
Part of synthesized region
(not stand-alone)



Power distribution and shield on top metals. Only vertical - no analog/digital crossing

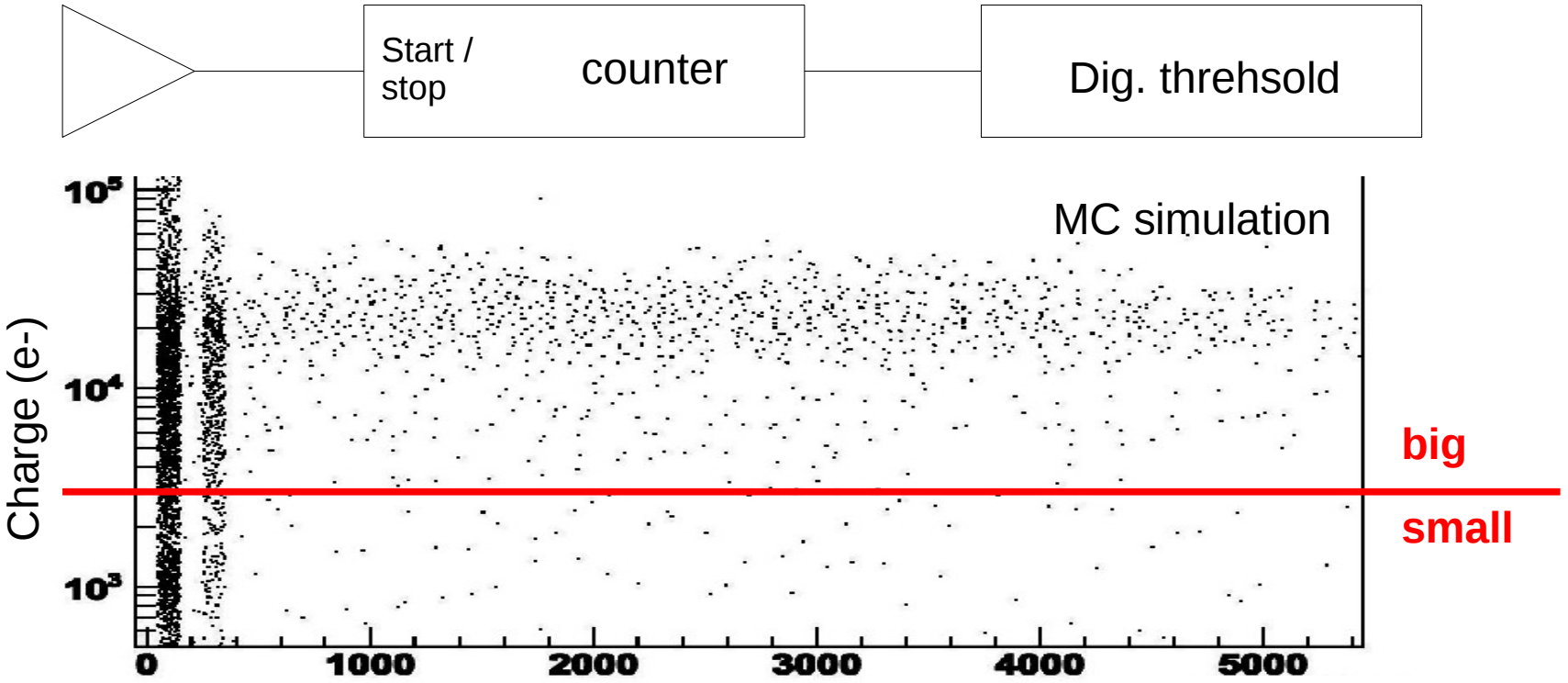
FE-I4 region

- 4 analog pixels, each ending with a comparator output (ADC function).
- One common digital region synthesized as one block.
- 5-deep TOT value memory for each pixel, but shared trigger latency counters.
- If 1 pixel is hit, 1 counter starts. If 2,3,4 pixels are hit, also only 1 counter starts.
- No region dead time (pixel A hit this crossing and B hit next crossing is OK)

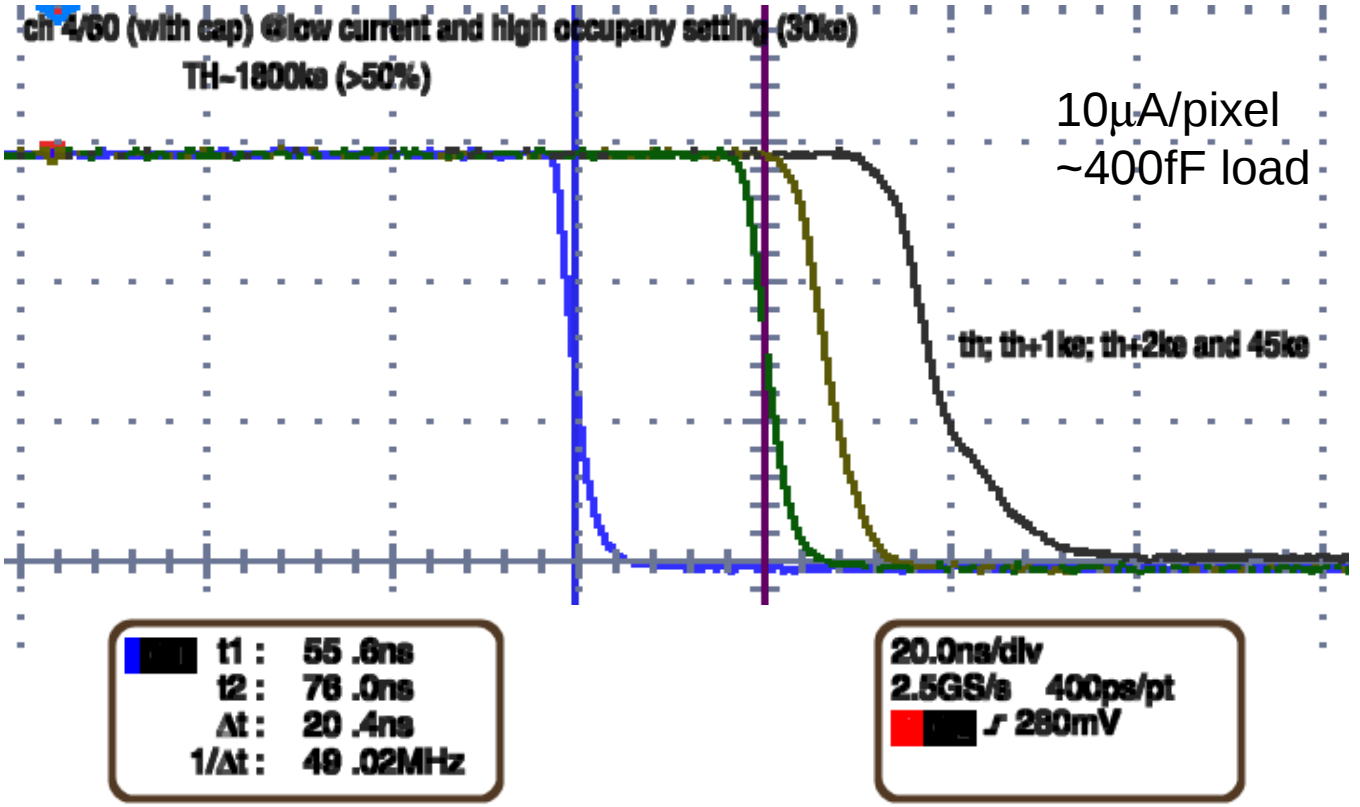


Hit association

- Recall claim “higher current to improve time-walk not needed”
- Because we use a digital threshold with association of “small hits” by proximity, not time.
  - Large hits are in time
  - Small hits are close to large hits



Time-walk



- Can be reduced by increasing analog current
- But there is no need (see later)

Analog pixel

Design:

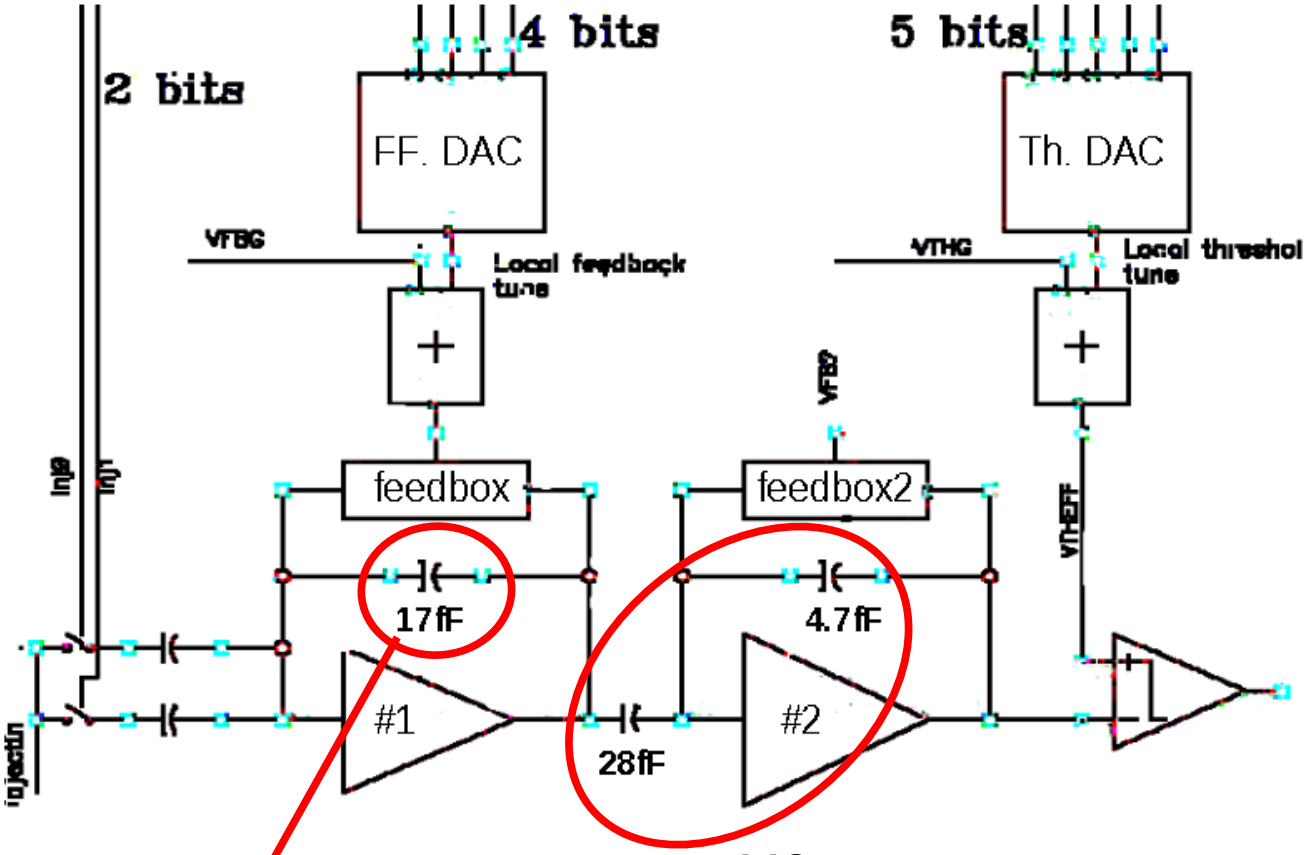
1.2V – 1.5V

5µA – 17µA

Baseline:

10µA @ 1.4V

Same as present detector nominal per unit area



~4MIP
dynamic range

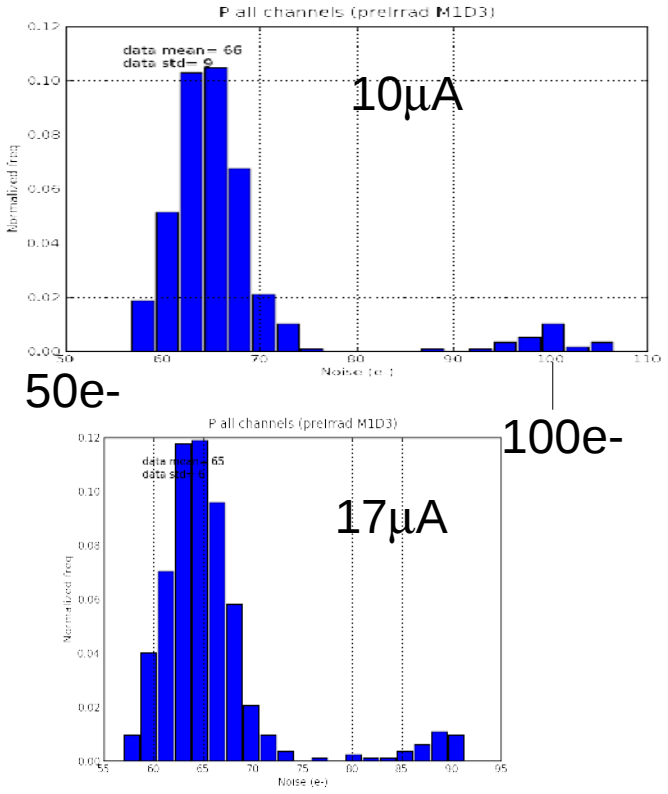
X6
No shaping

Noise Performance

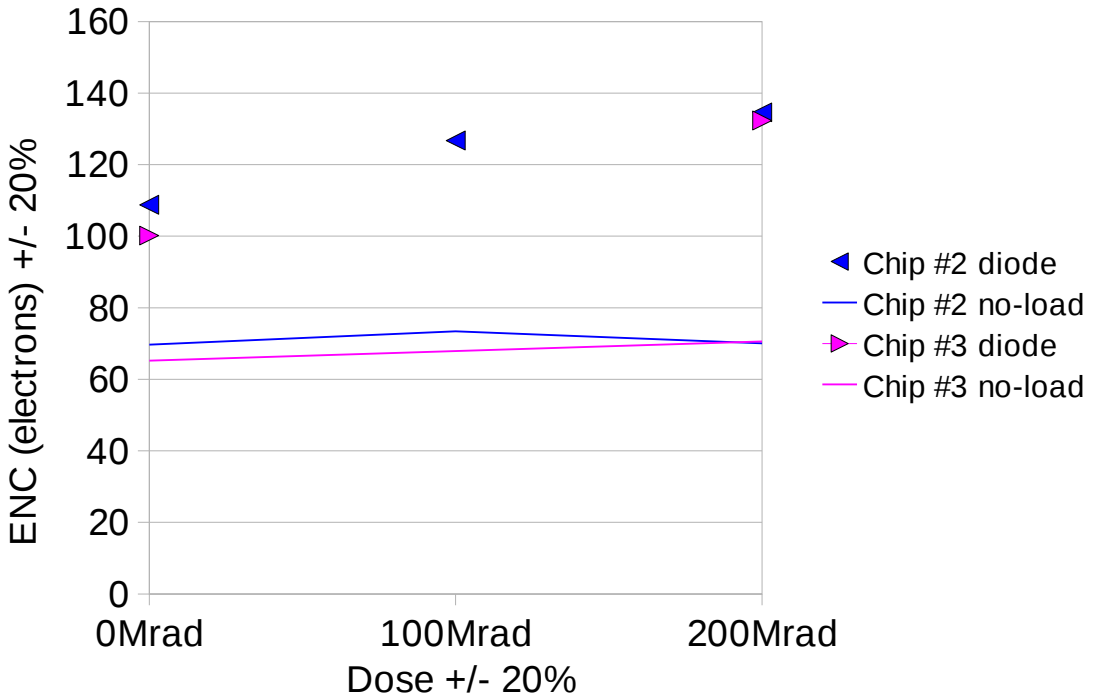
(measured in pixel array test chip)

Noise

unloaded ~400fF



Irradiation:
Loaded channels increased ~20%,
But load is a diode!
The load itself changes with radiation
No bump-bonded assemblies yet.



Functional simulations (example)