EDGELESS DETECTORS FOR HIGH ENERGY PHYSICS APPLICATIONS

Dr. Juha Kalliopuska

Business from technology

Outline

- VTT in brief
- Facilities and process resources
- 3D detector process
- Edgeless detector prototypes on 6” SOI Wafer
    - Wafer layout, fabrication process & motivation
    - Different designs: p-on-n and n-on-n
    - Handle wafer removal and packaging
- Detector characterization
    - Strip detectors: CV, IV and Breakdown voltage
    - Pixel detector: IV, X-ray source and tube images
- VTT’s process capabilities for advanced detectors
- Summary

VTT in brief

Customer sectors

- Biotechnology, pharmaceutical and food industries
- Electronics
- Energy
- ICT
- Real estate and construction
- Machines and vehicles
- Services and logistics
- Forest industry
- Process industry and environment

Focus areas of research

- Applied materials
- Bio- and chemical processes
- Energy
- Information and communication technologies
- Industrial systems management
- Microtechnologies and electronics
- Technology in the community
- Business research

- Turnover 245 M€
- Personnel 2,700
- 77% with higher academic degree
- 6,200 customers
- Established 1942
- VTT has been granted ISO9001:2000 certificate.

VTT's operations

Research and Development ■ Strategic Research ■ Business Solutions ■ Ventures ■ Expert Services ■ Corporate Services

Public decision makers, financiers and R&D performers

Parliament of Finland

Council of State

Research and Innovation Council

Ministry of Education

- Academy of Finland
- Universities

Ministry of Employment and the Economy

- Tekes, the Finnish Funding Agency for Technology and Innovation
- VTT

Other ministries and research institutes

- Sitra, the Finnish Innovation Fund
- Finnvera
- Finpro
- Finnish Industry Investment Ltd

TE-Centres

VTT SERVICES

MICRONOVA CLEANROOMS

Main Cleanroom Characteristics

Total Area	2 600 m^2
Cleanroom Classification (in clean bays)	ISO 4…ISO 6 (10…1000)
Temperature	21 °C ± 0,5 °C
Relative humidity	45 % ± 5%

Clean bay - Service chase type
Ventilation based on filter fan units
Raised perforated floor
Subfab with technical support areas

Labs with built-in Cleanrooms

Micropackaging lab - dicing saws, wire bonding

SubTech lab - Ion implantation, CMP, backgrinder, wafer bonder

Process equipment is mainly for 150 mm wafer size, but some processes can be performed also on 200 mm wafers

Equipments

Furnace:

- oxidation, LTO, TEOS, Nitride, doped and undoped polysilicon
- 2 Centrotherm furnace stacks

Lithography:

- Contact aligners – MA150 and MA6 (bottom side alignment), MA200
- E-beam writing – Zeiss LEO 1560
- Step and Stamp Imprint Lithography – Suss MicroTec NPS 300
- i-line stepper, Canon FPA 2500i3
- Resist/development tracks, Suss ACS 200 and AIO Duna 700

Dry etching

- Etchers for silicon oxide, nitride, metals - LAM 4520/4420/9600
- Deep silicon etching - Aviza Omega i2L and STS ASE
- Silicon oxide ICP etching – STS AOE
- RIE – Oxford 80Plus
- Plasma strippers (PRS 800/801), microwave asher (Aura 1000), wet ozone stripping

Ion Implantation

- Medium current, 200 keV, P, As, B – Eaton NV8200-P

Equipments

Sputtering: AlSi, Mo, TiW, Si - Provac LLS 801

PECVD: Silicon oxide and nitride, incl. TEOS-process

Electroplating:
- Ni, Cu, SnAg, SnPb and SnBi – RENA and home-built plating systems

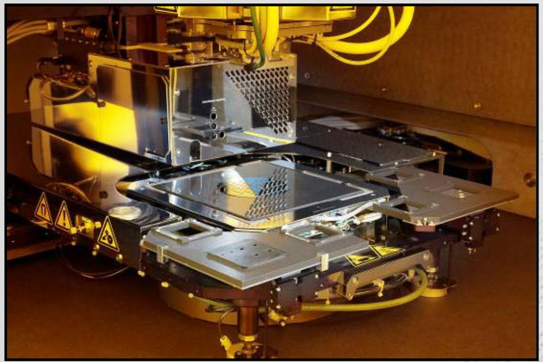
Flip-chip bonding: 2 Suss MicroTec FC150 bonders

Dicing: Disco DFD 651 and Loadpoint uAce-352

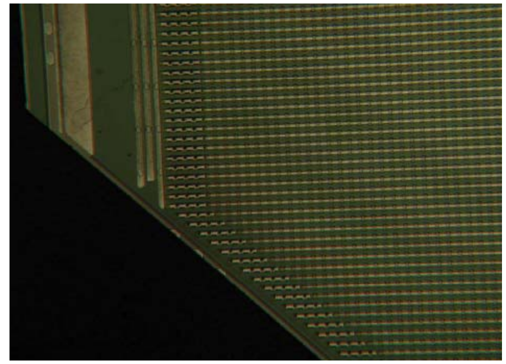
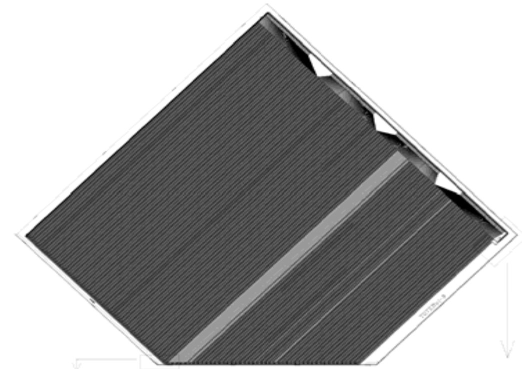
Fusion wafer bonding: EVG 5201S and EV 801 (non-IC materials)

Backgrinding (wafer thinning): Strasbaugh 7AF

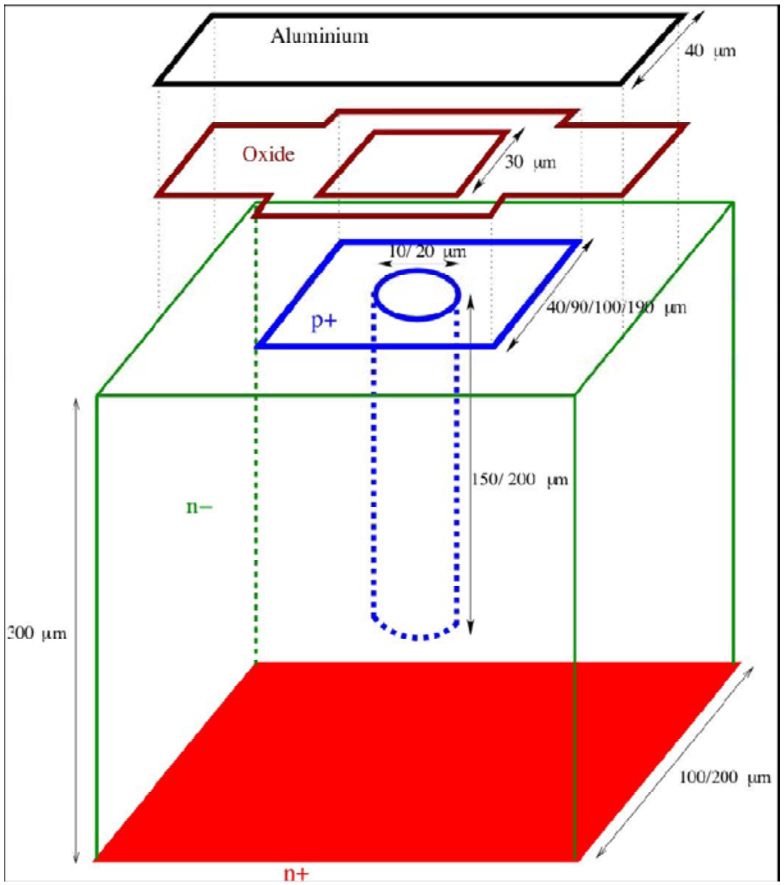
Polishing and planarization: Strasbaugh 6DS-SP



VTT’s 3D DETECTORS

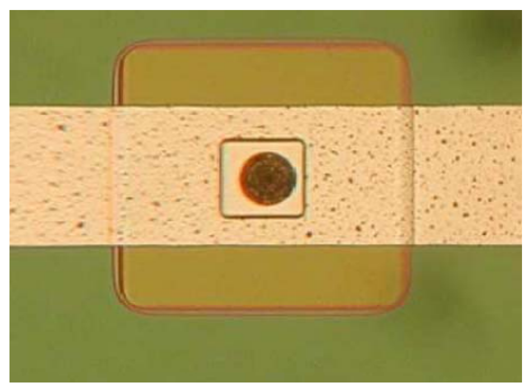
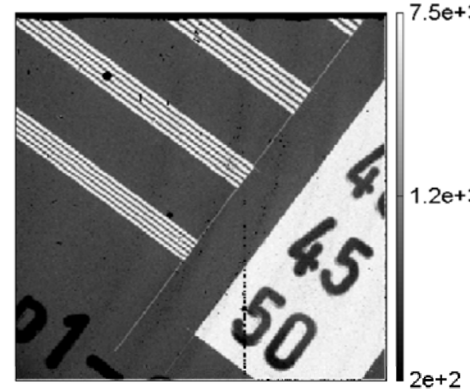



Pixel element of a strip detector



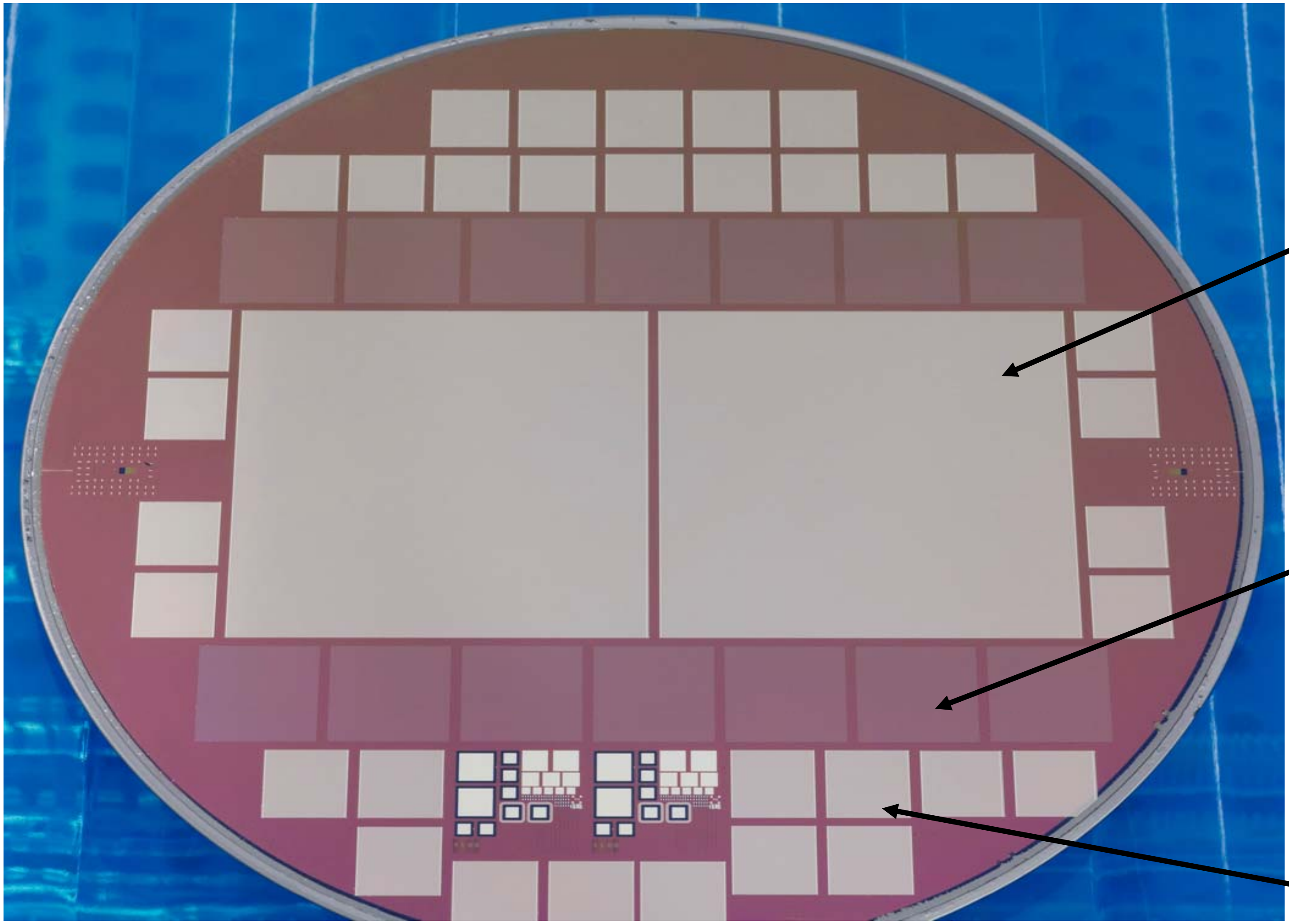
PROPERTIES

- GOOD SPATIAL RESOLUTION
- TUNABILITY OF THE VERTICAL DOPING PROFILES
- SMALL DEPLETION VOLTAGE
- LARGE AREA STRIP AND PIXEL DETECTORS DEMONSTRATED (~10 cm^2)
- SAME TECHNOLOGY FOR VERTICAL I/O’s & EDGELESS DETECTORS

Pixel of a 3D strip detector and X-ray image taken with a 3D detector coupled to the Medipix2

EDGELESS DETECTORS on 6” (150 mm) SOI WAFER



Main edgeless strip detectors

- *5 x 5 cm²*
- *DC & FOXFET*
- *50 μm edge distance*

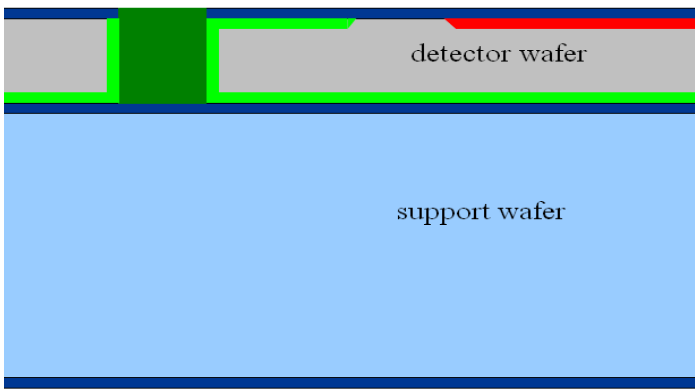
Medipix 2 edgeless pixels

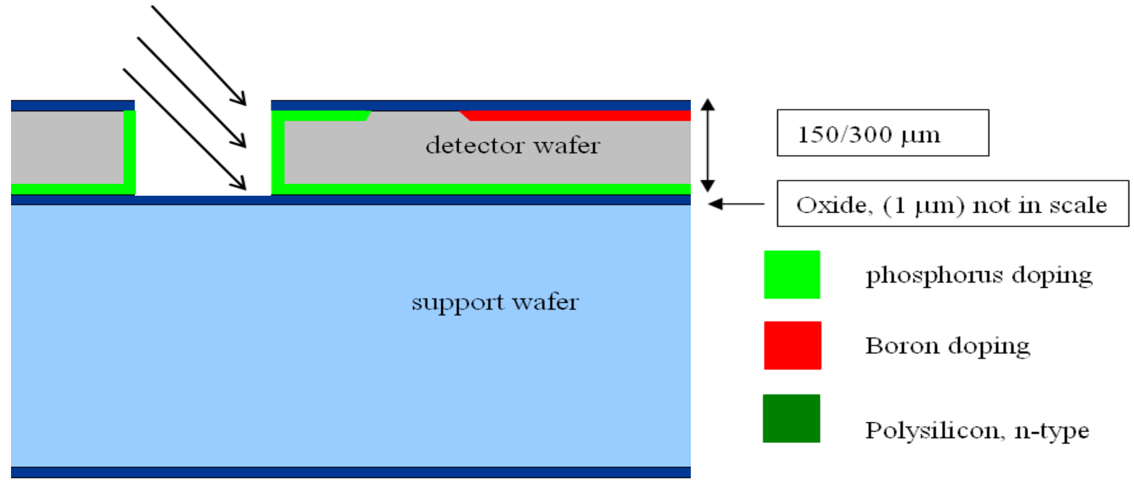
- *1,4 x 1,4 cm²*
- *20 & 50 μm edge distance*

Baby edgeless strip detectors

- *1 x 1 cm²*
- *DC, PT & FOXFET*
- *20, 50 & 100 μm edge distance*

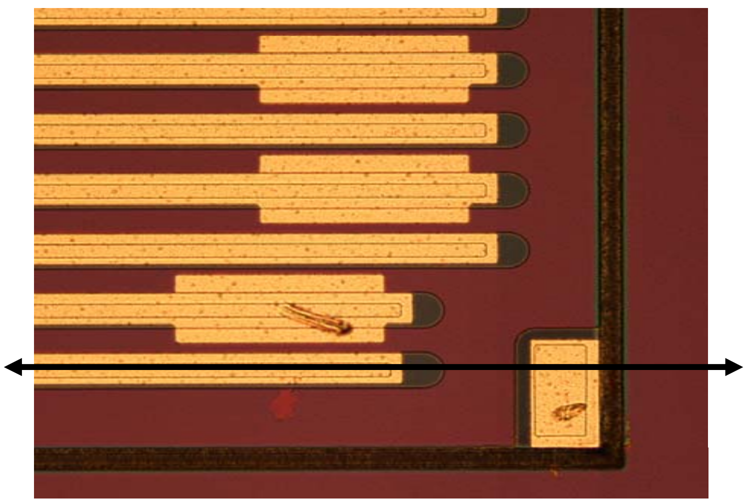
VTT's edgeless fabrication process

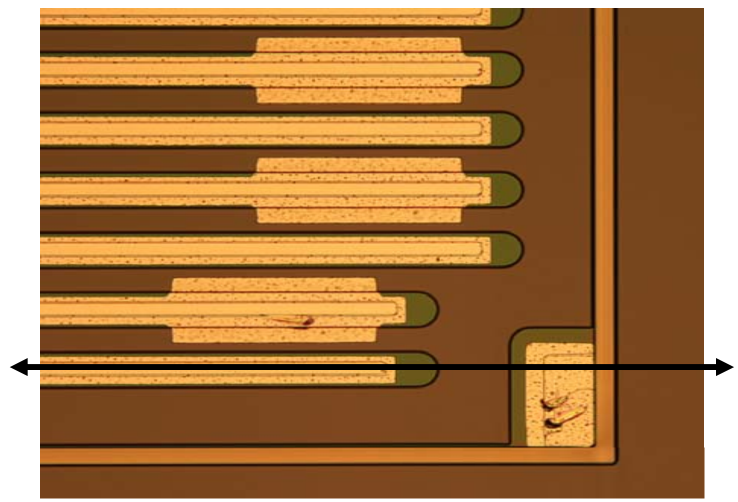




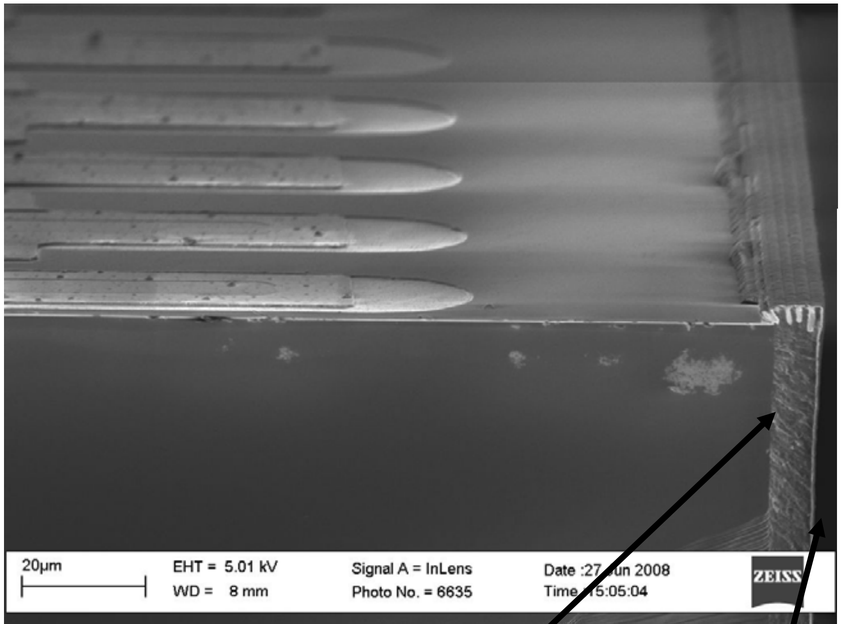
Poly process, p-on-n

Edge implantation, p-on-n

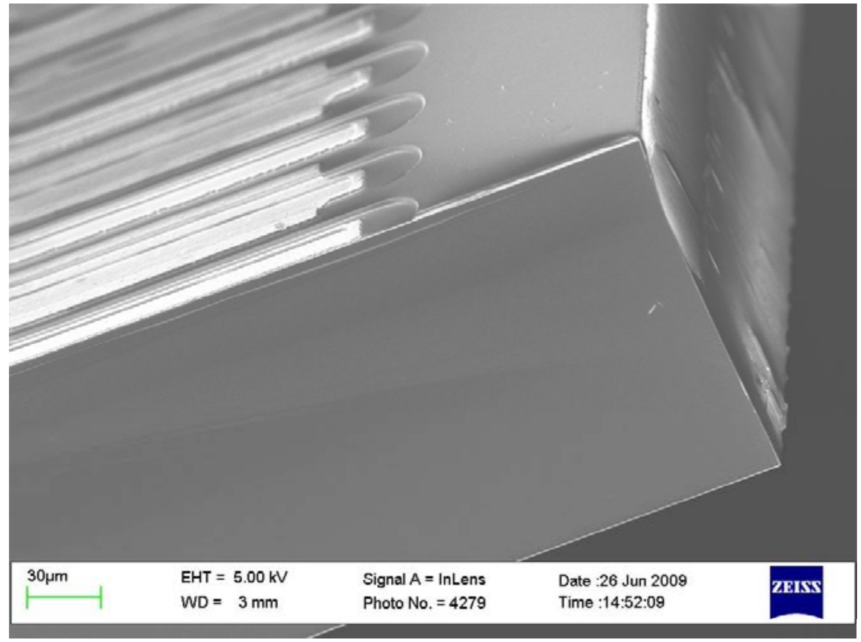


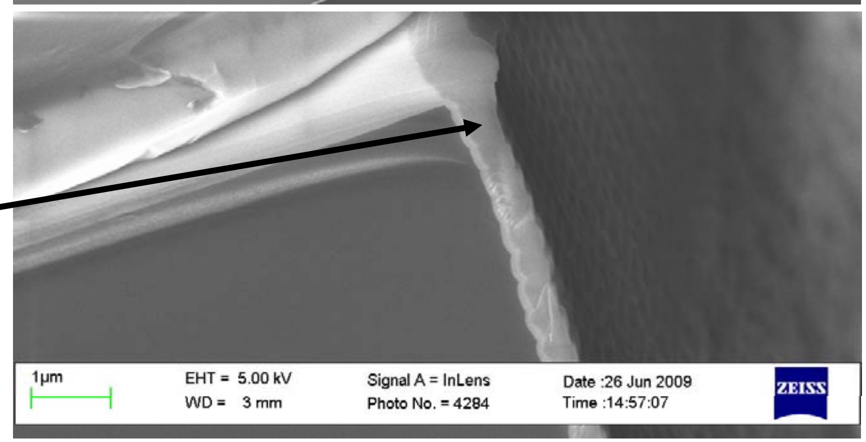


Poly process



Edge implantation





6 um inactive polysilicon

500 nm oxide

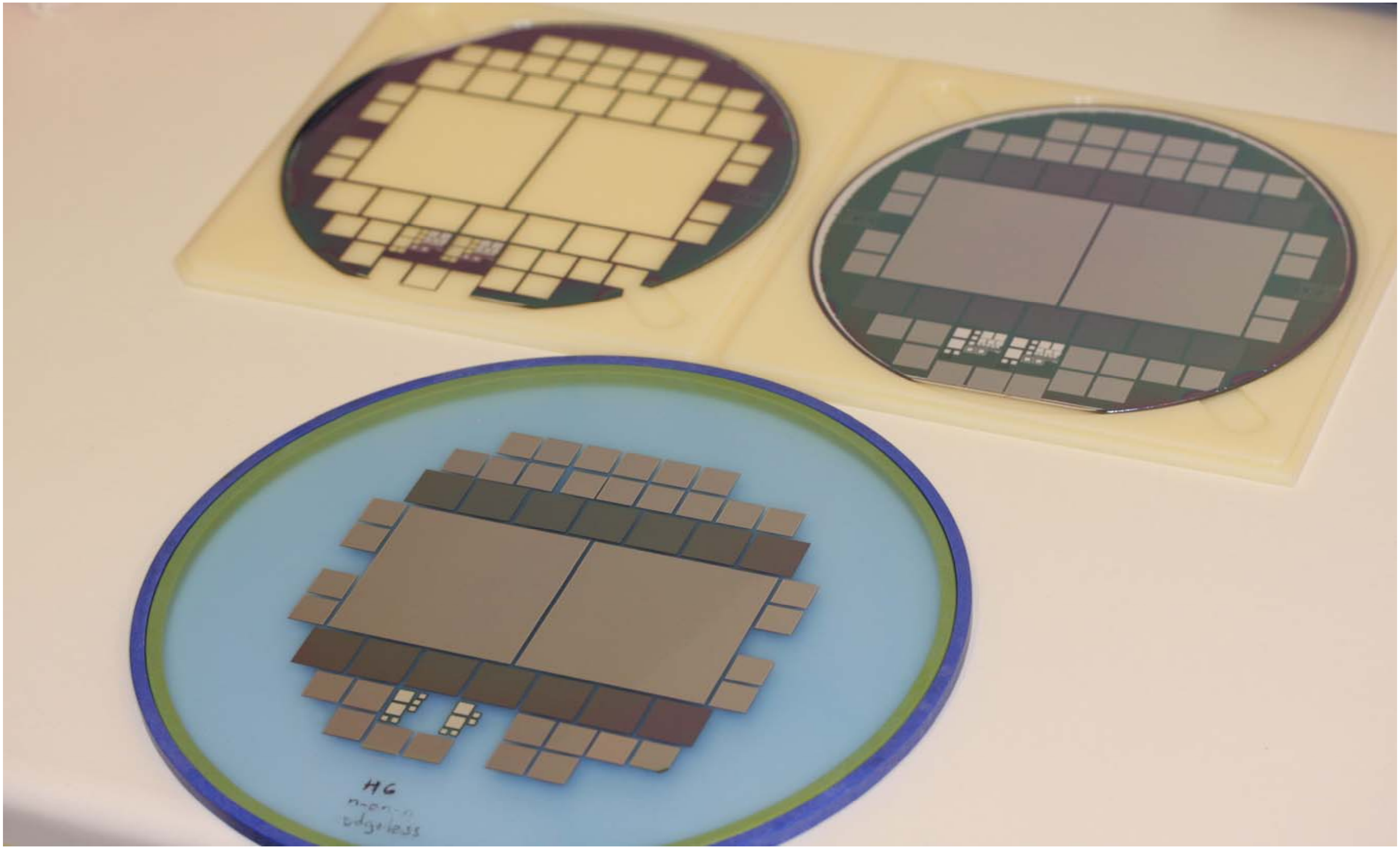
3D PROCESSING WITH POLYSILICON FILLING

- Filling of the trenches is a slow process
- ~50% of total process equipment time in furnace
- Bowing of 6” wafers due to the polysilicon growth (~0.5 mm)
- Difficulties in lithography, planarization and ion implantation
- Wafers brittle -> increased possibility of wafer cracking
- Slow planarization process required
- Detector edge cracking after the support removal
- Physical inactive edge region ~5-10 µm

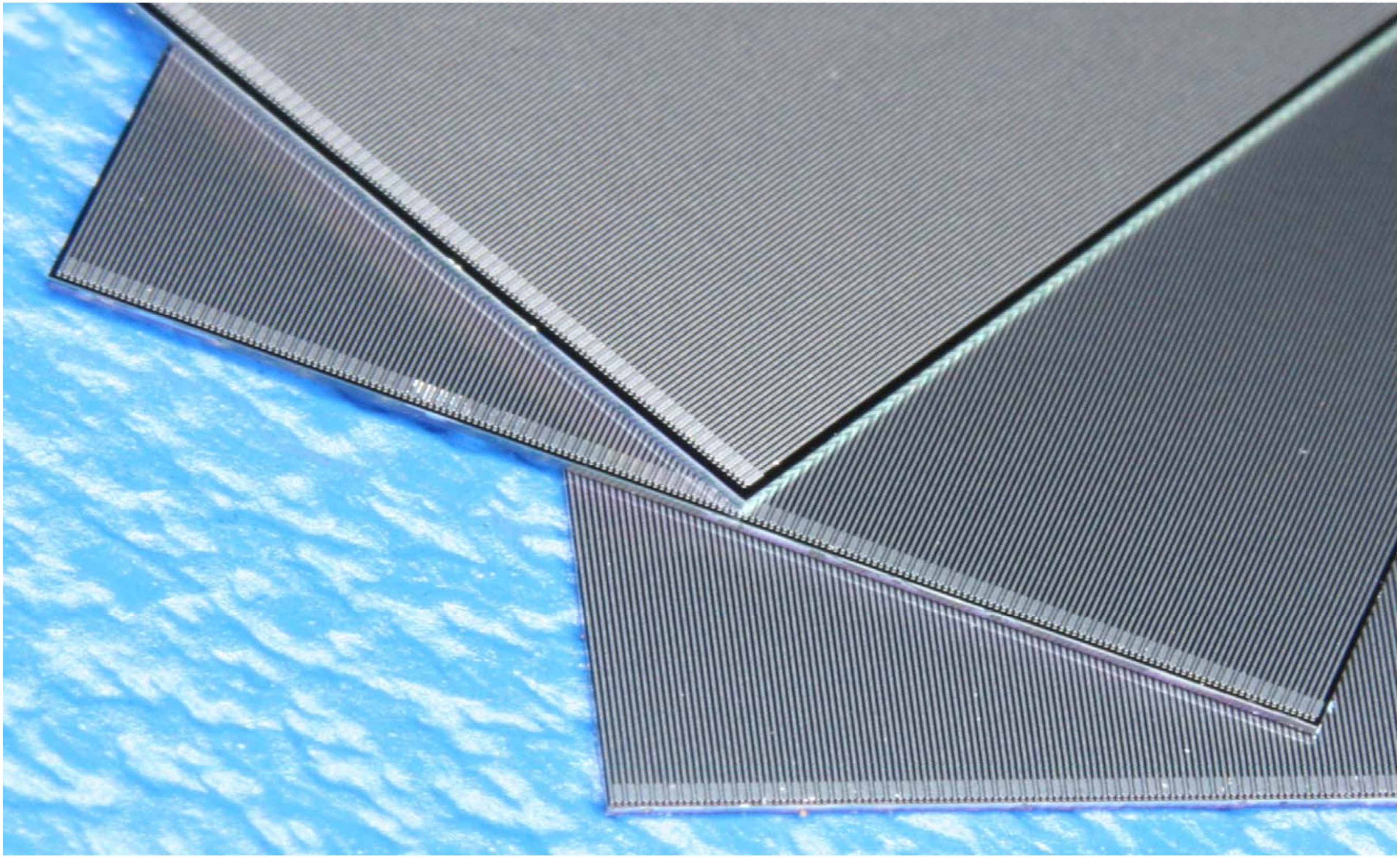
3D PROCESSING WITH ALTERNATIVE PROCESS

- No need for polysilicon filling, planarization and separate ICP dicing
- Fast process and no bowing of the wafer
- Detector edges sustain handling – no edge cracking
- Physical inactive edge region <1 µm
- Requires non-planar lithography -> readiness available at VTT

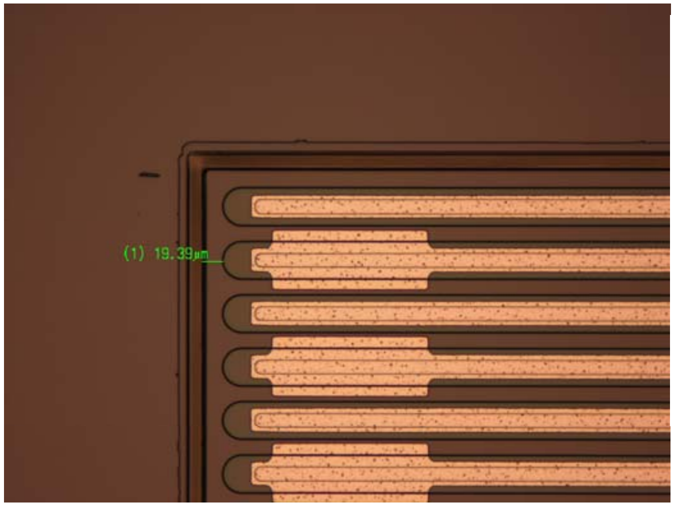
Handle wafer removal

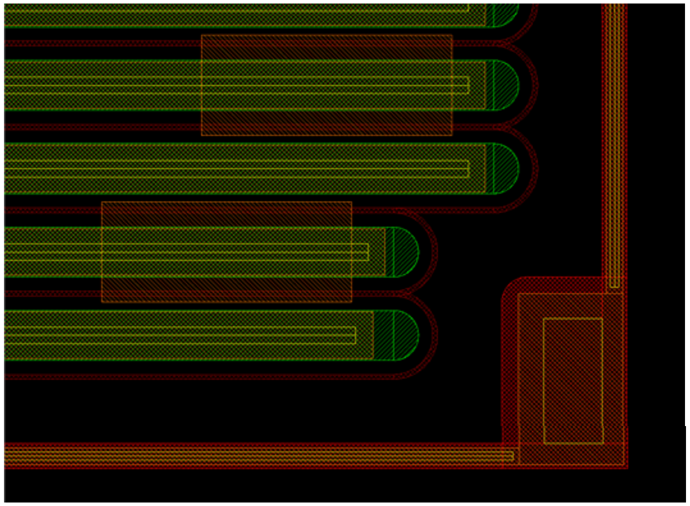


Edgeless strip detectors

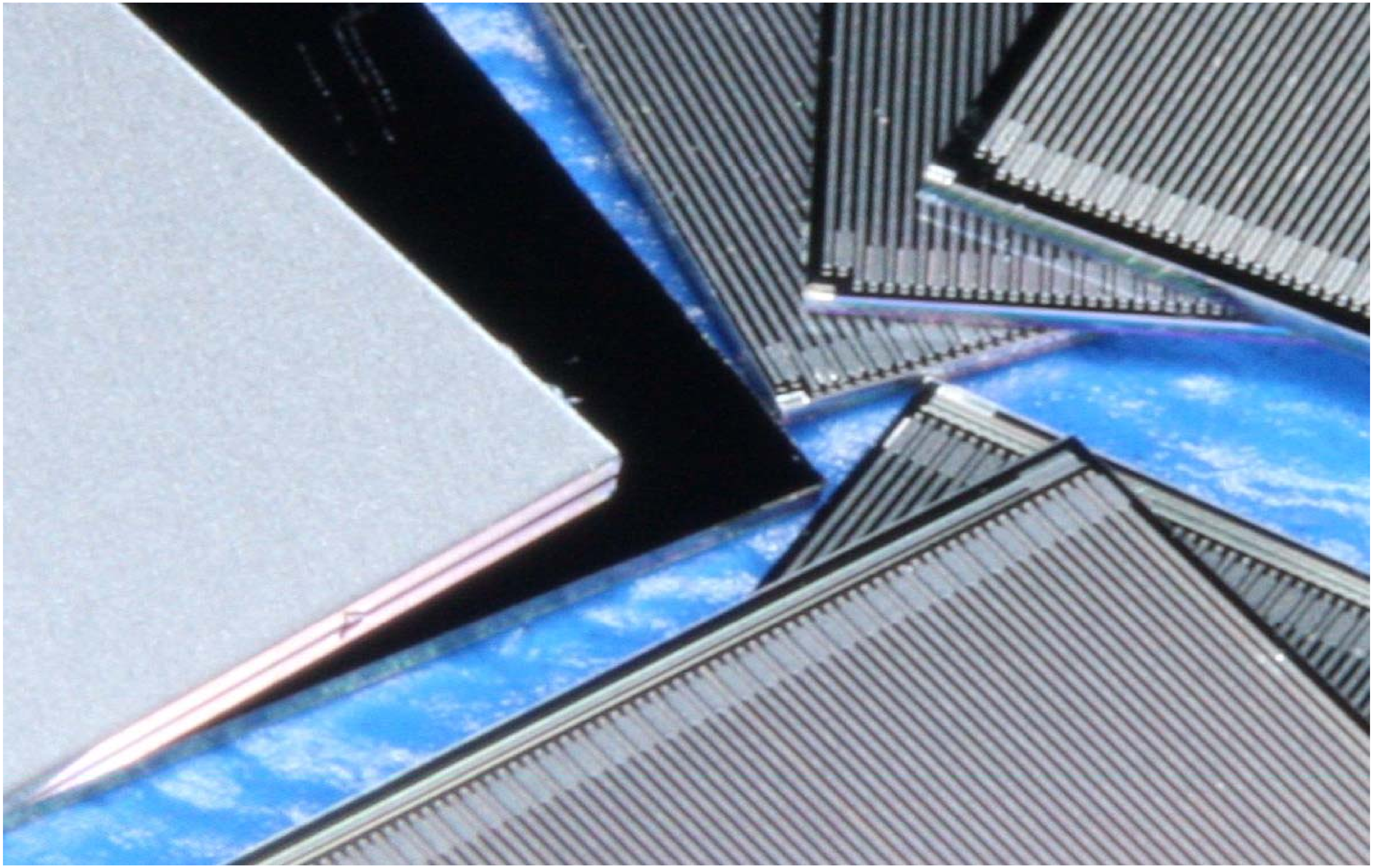


DC-coupled strip desings & n-on-n layout



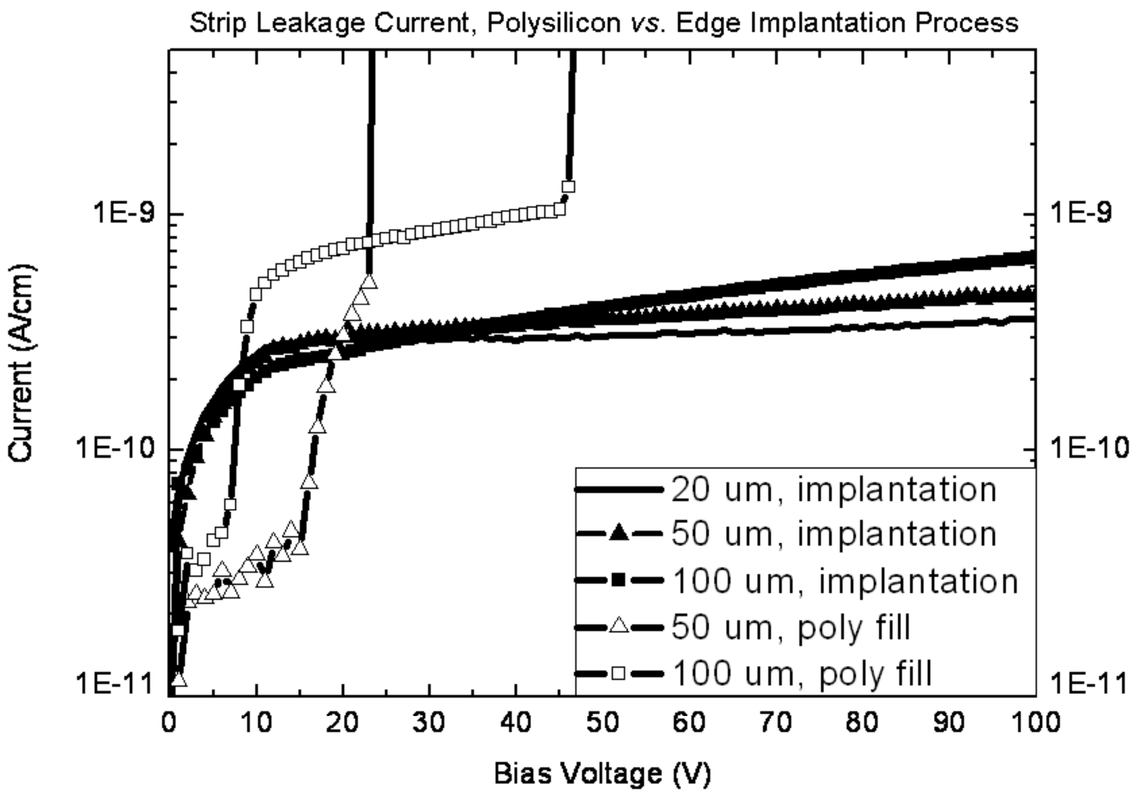


Edgeless strip detectors



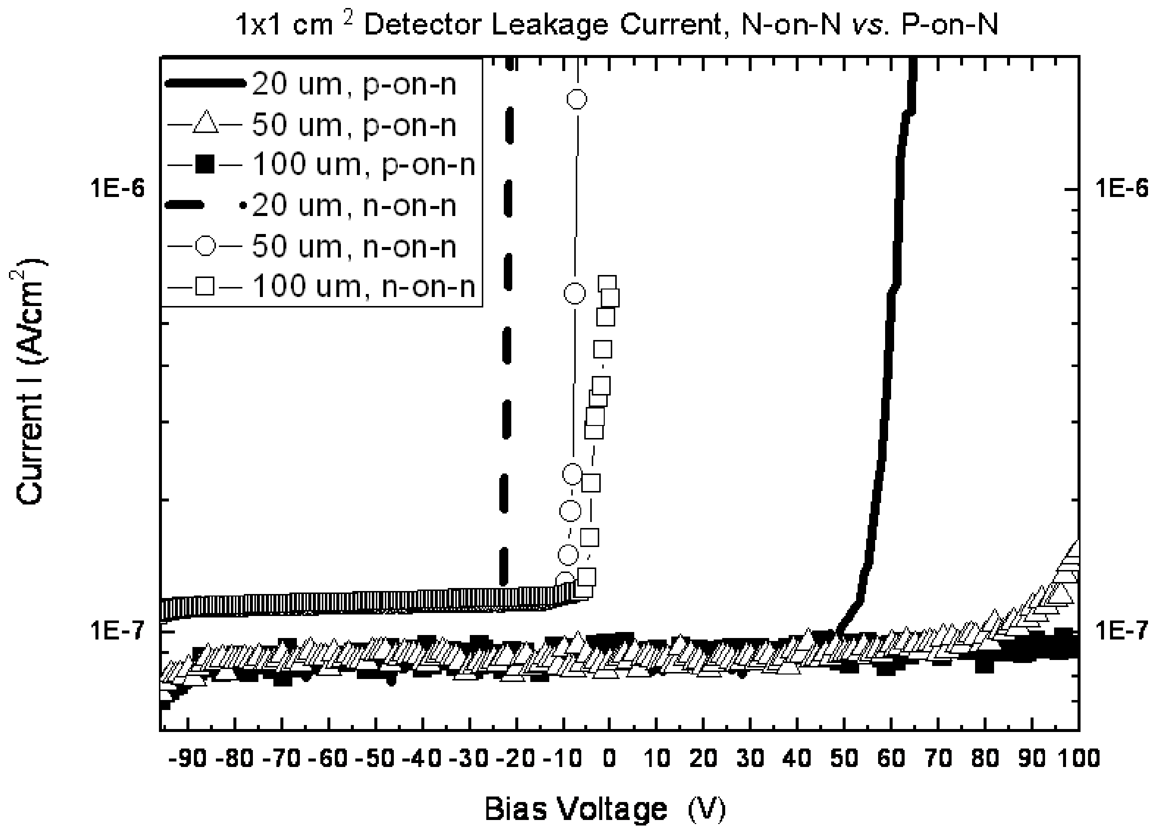
Strip leakage current: p-on-n implantation vs. poly

- Low leakage currents for both process approaches
- Very early breakdown voltages for poly filling
- Leakage current depends on the active edge distance



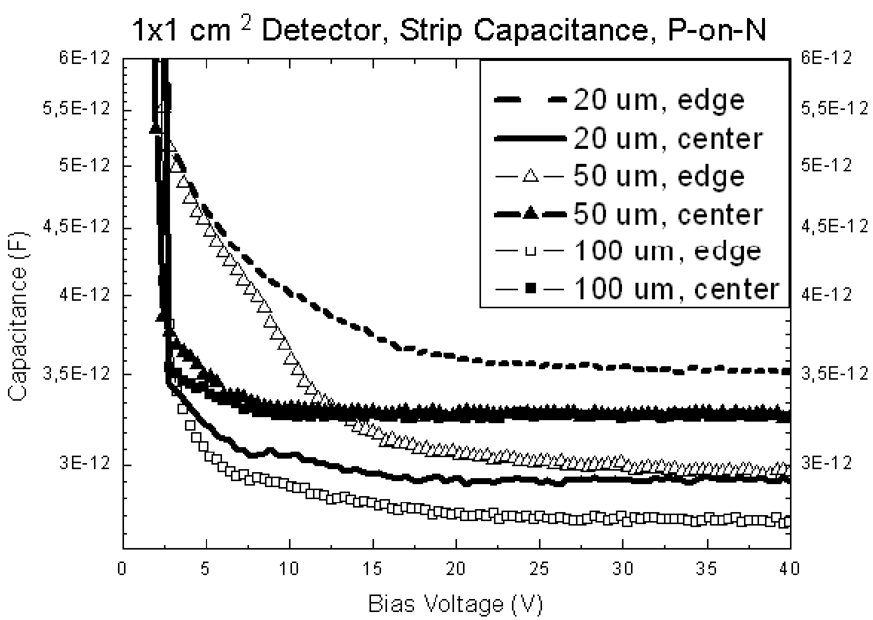
Leakage current and breakdown: p-on-n and n-on-n

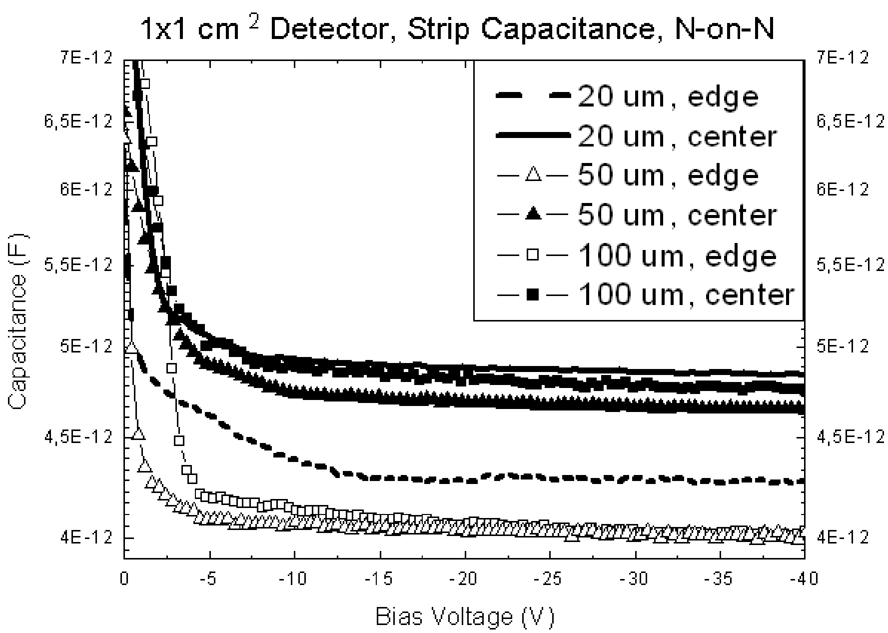
- p-on-n: 50 - 70 nA/cm^2 & breakdown at 145 - (>200 V)
- n-on-n: 116 - 118 nA/cm^2 & breakdown at 75 - 95 V



Strip capacitance and depletion: p-on-n and n-on-n

- Front-to-backplane depletion 7 V (p-on-n) and 4 V (n-on-n)
- p-on-n: 550 – 700 pF/cm^2 and full depletion 25 - 40 V
- n-on-n: 800 – 960 pF/cm^2 and full depletion 13 - 25 V

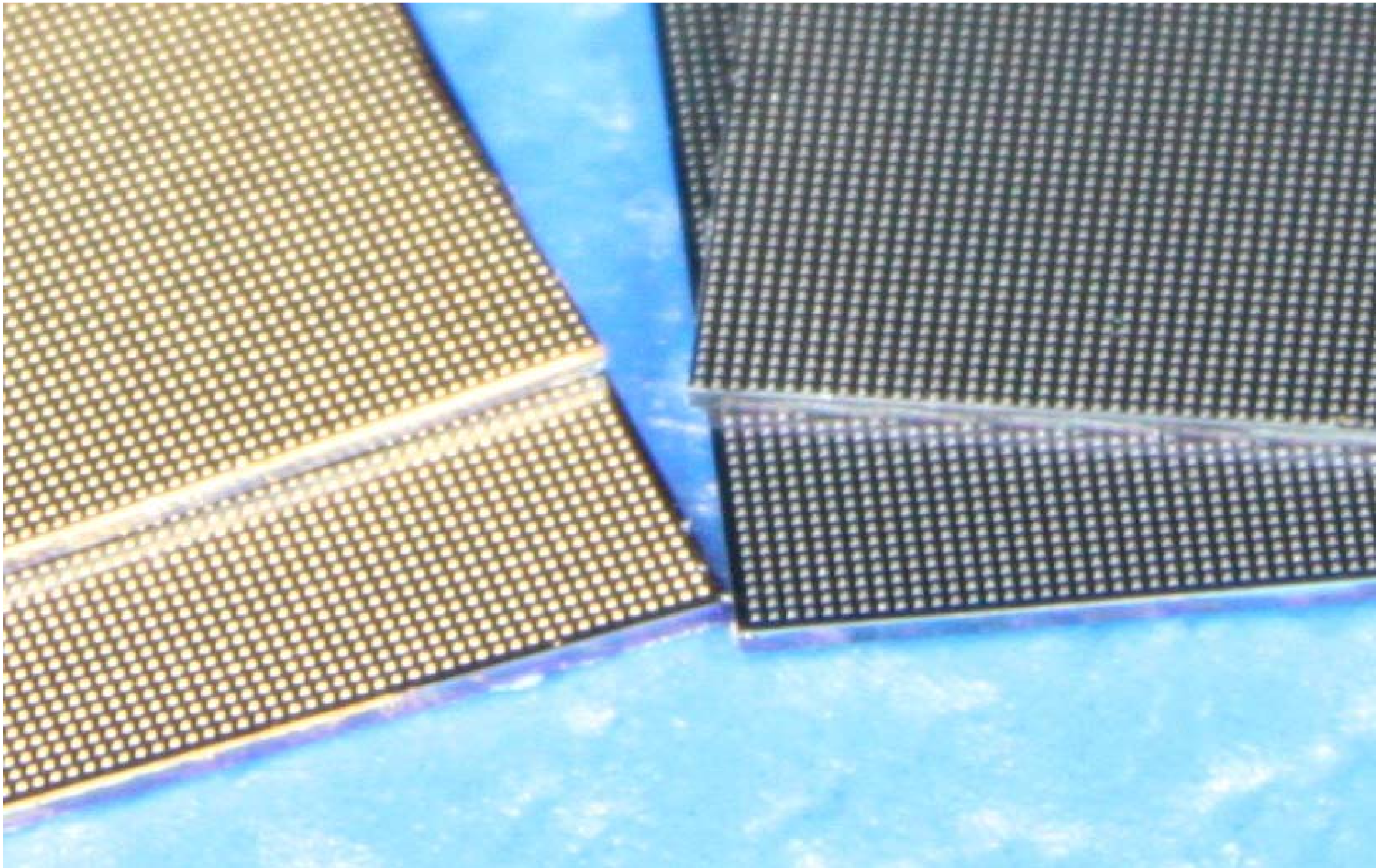




Characteristics of 150 um thick edgeless strip detectors

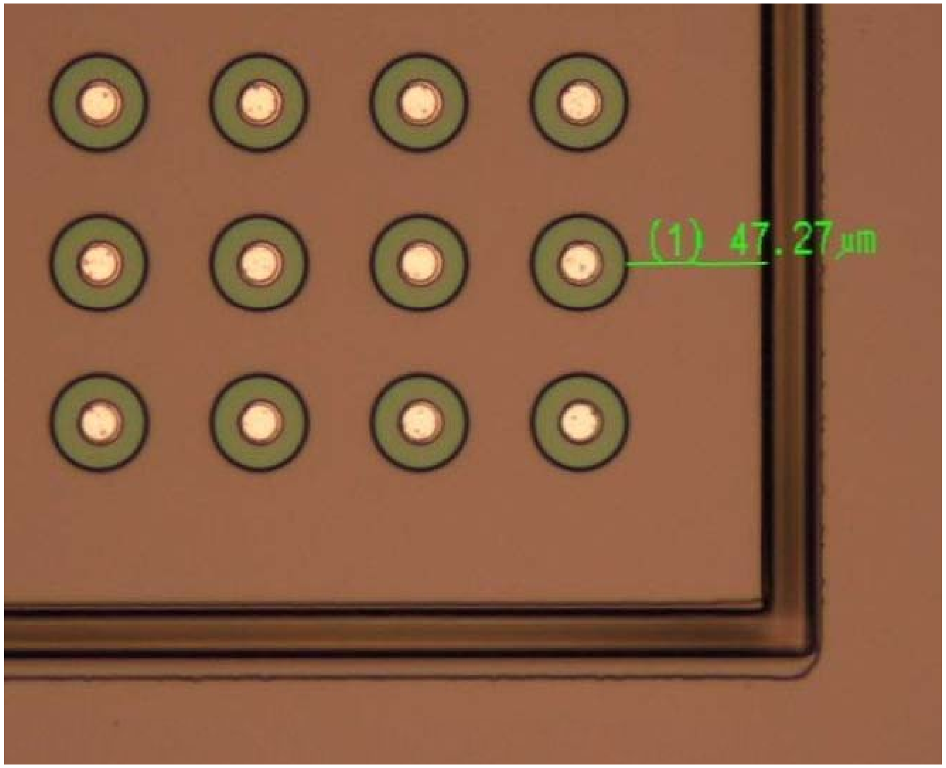
Edge distance	*20 μm*		*50 μm*		*100 μm*	
polarity	*p-on-n*	*n-on-n*	*p-on-n*	*n-on-n*	*p-on-n*	*n-on-n*
Full depletion voltage	~25 V	~13 V	~35 V	~16 V	>40 V	~25 V
IV @ 40 V (nA/cm^2)	50-59	118	58-68	116	66-70	117
CV @ 40 V (pF/cm^2)	580-620 705 (edge)	940-960 855	652-665 593 (edge)	930-950 800	650-655 543 (edge)	937-955 805
Breakdown voltage	~145 V	~75 V	~180 V	~90 V	>200 V	~95 V

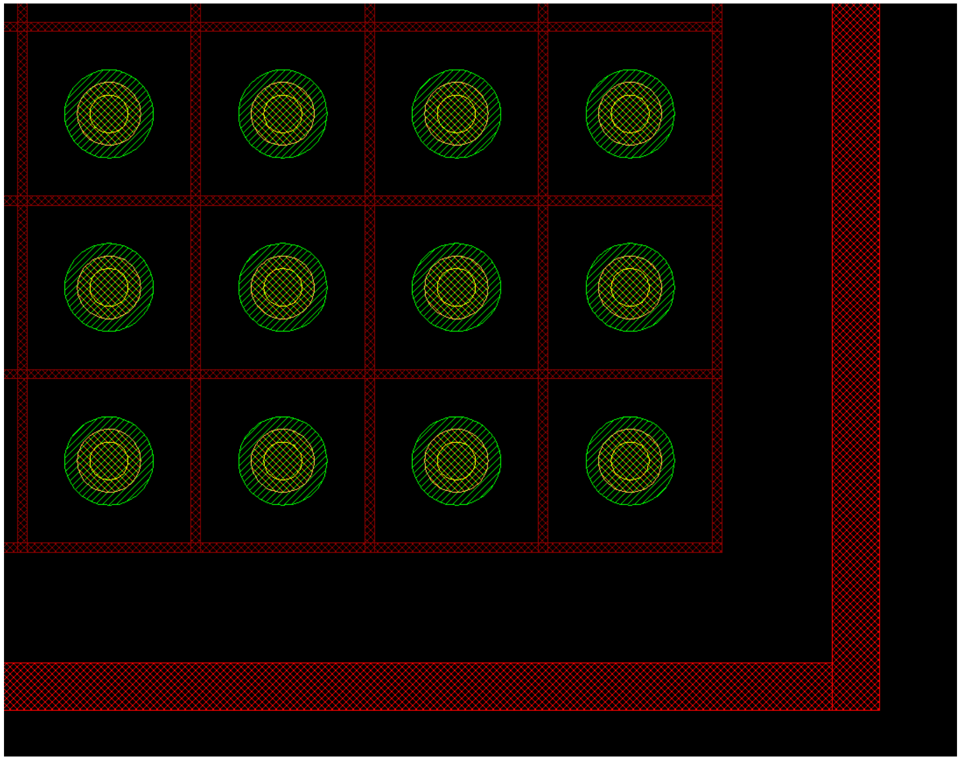
Edgeless pixel detectors



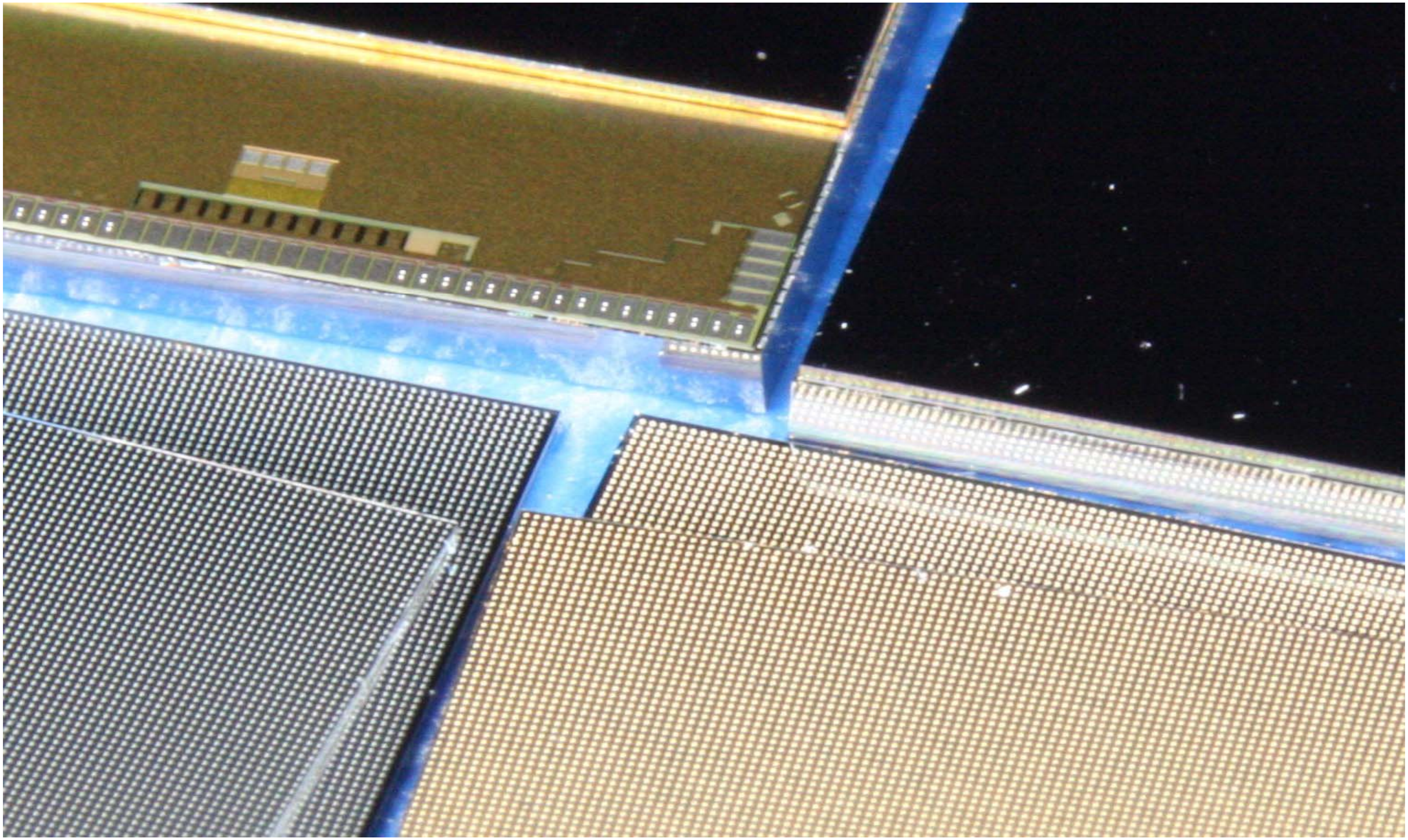
Medipix2 pixel desing & n-on-n layout

- Pixel pitch of 55 µm
- Active edge distances 20 and 50 µm
- UBM service available from subcontractor





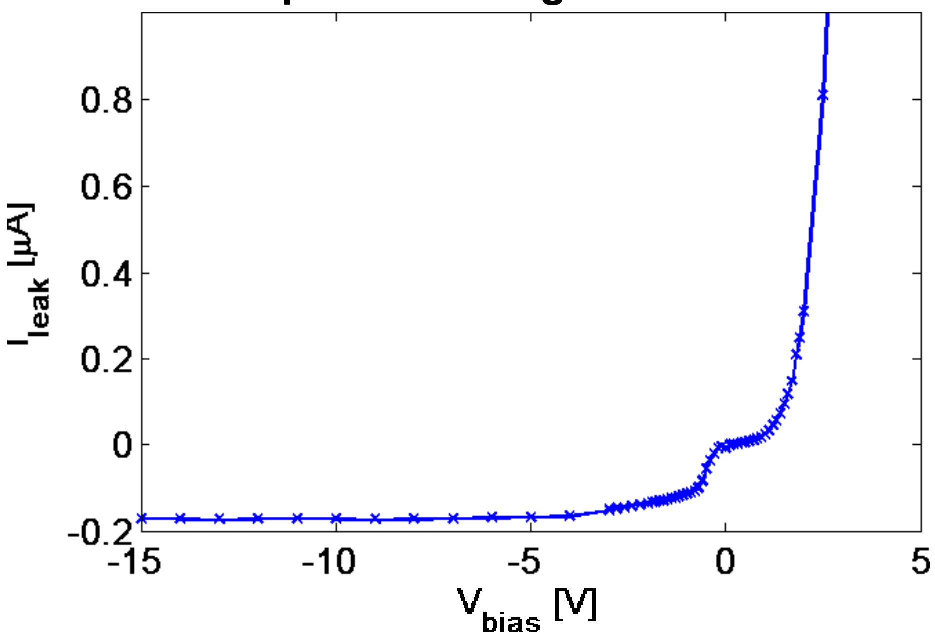
Flip-chip bonding to Medipix2



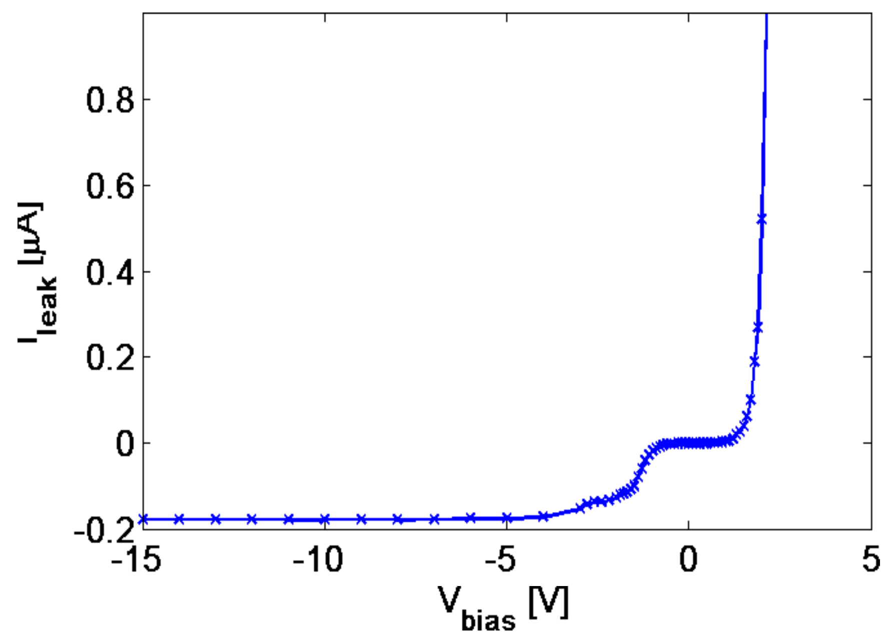
Medipix2 n-on-n pixel detector: leakage current

- Detector biased from backside
- Active edge distances of 20 and 50 µm
- Leakage currents: 88 nA/cm^2 and 90 nA/cm^2
- No breakdown observed below 70 V

20 µm active edge distance



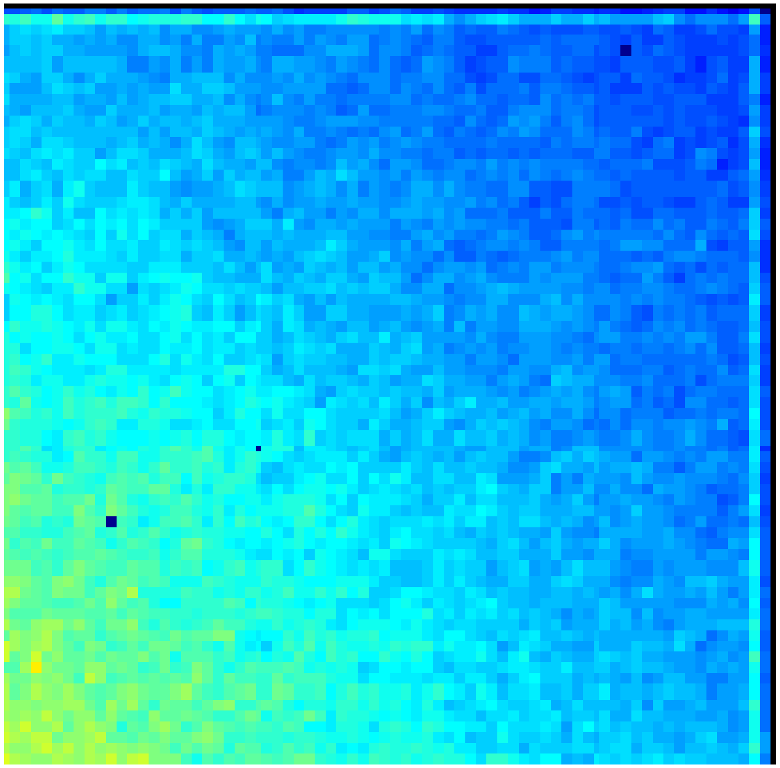
50 µm active edge distance



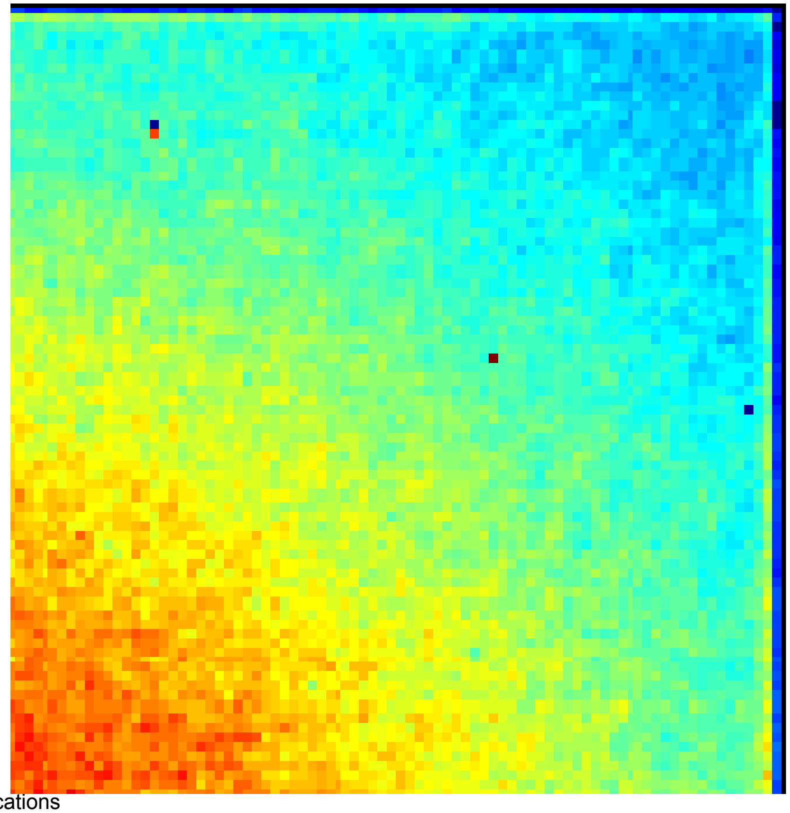
Medipix2 n-on-n pixel detector: radiation source images

- Good flip-chip bonding yield
- Fe55 (γ), Cd109 (γ) and Sr90 (e^-) for 300 s at -15V bias
- Second to the edge row has highest count rate

20 µm active edge distance



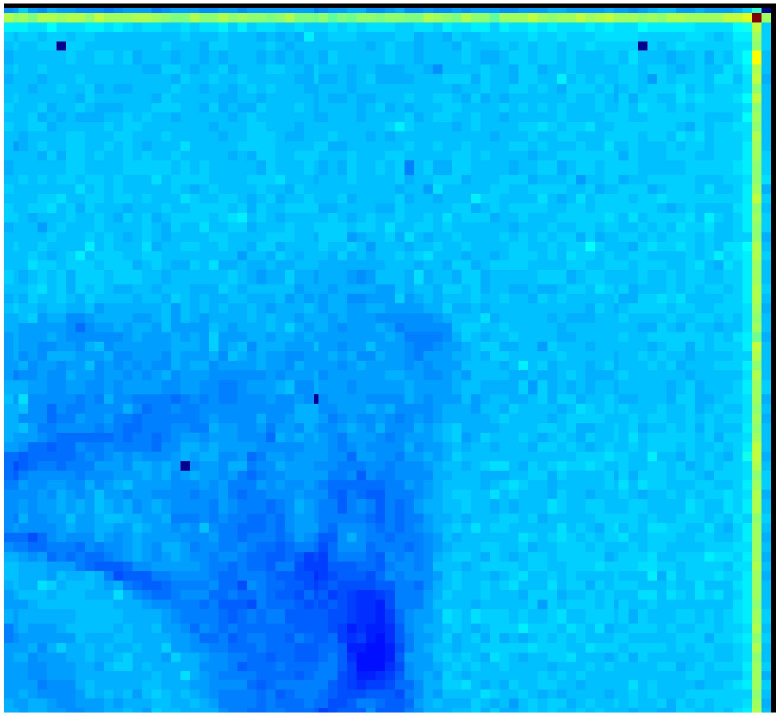
50 µm active edge distance



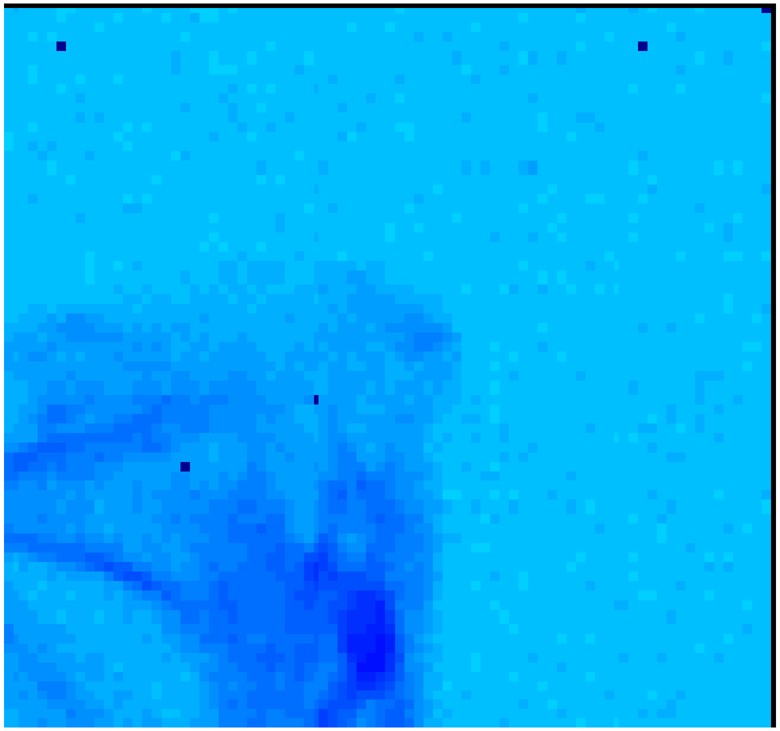
Medipix2 n-on-n pixel detector: X-ray tube images

- 20 µm active edge distance detector at -15V bias
- W-tube with 30 keV, 10 mA and 2.2 mm Al filtering
- Flat band correction improves the image at the edge

Uncorrected image



Flat-field corrected



VTT's process capabilities for advanced detectors

- Operator time 48-54% of the equipment time -> parallel batch processing
- Delivery time includes possible UBM process and handle wafer removal
- Add 1 month to the delivery time for the prototype process

	DC STRIP (realized)	EDGELESS POLY (realized)	EDGELESS IMPLANTATION (realized)	NEW EDGELESS IMPLANTATION (estimate)	FULL 3D EDGELESS POLY (estimate)
PROCESS TIME (h)	**108** (2-3 WEEKS)	**511** (10-11 WEEKS)	**305** (6-7 WEEKS)	**276** (5-6 WEEKS)	**356** (7-8 WEEKS)
PROCESS STEPS	59	118	119	109	152
BOTTLE NECKS (% OF THE PROCESS TIME)	LITHOGRAPHY 23% FURNACE 20%	FURNACE 46% DRY ETCH 13% PLANARIZATION 12 %	LITHOGRAPHY 23% FURNACE 20%	FURNACE 21% LITHOGRAPHY 18%	FURNACE 27% DRY ETCH 20%
DELIVERY TIME	***1 MONTH***	***3-4 MONTHS***	***2-3 MONTHS***	***2 MONTHS***	***3 MONTHS***

Summary

- First prototypes p-on-n and n-on-n edgeless detectors have been fabricated
  - Breakdown and depletion voltage increase with the active edge distance
  - Leakage current increases with the active edge distance
  - Capacitance increases for the p-on-n with the active edge distance but decreases for the strip closest to the edge
  - For the n-on-n the capacitance is almost independent on the edge design
  - Good uniformity observed within the strips and pixels
  - Second to the edge pixels collect more charge
  - Physical edge activity of ~1 μm and no edge cracking
- VTT has capability to produce and deliver edgeless and full 3D edgeless detectors in 2-4 months.
  - Three edgeless prototype processes done (1 poly & 2 edge implantation)
  - Good understanding of the edgeless 3D process and non-planar lithography
- Further work in edgeless detector characterization: radiation hardness, edge activity determination and beam tests.


VTT creates business from technology