DEPFET pixels for the ILC vertex detector

M.Trimpl

DEPFET – collaboration:

MPI/MPE Munich

L.Andricek, P.Lechner, H.G. Moser, R.H.Richter, L.Strüder, G.Lutz, J.Treis

U Mannheim

P.Fischer, F.Giesen, C.Kreidel, I.Peric

U Bonn

M.Koch, R.Kohrs, H.Krüger, P.Lodomez, L.Reuen, C.Sandow, M.Trimpl, E.v.Törne, J.J.Velthuis, N.Wermes

U Prague

Z.Doležal, P Kodyš, D.Scheirich

U Aachen

L.Feld, W.Karpinski, K.Klein

outline

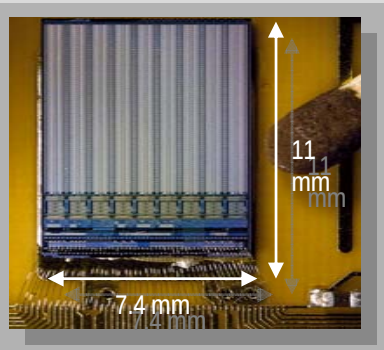
- **Introduction**: ILC project, vtx-d and requirements
- **DEPFET technology**:

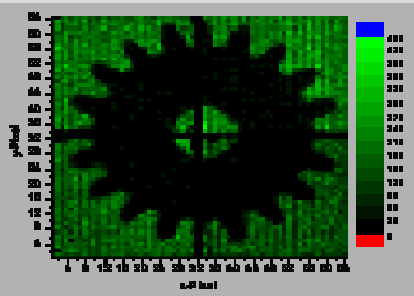
  principle, present production and thinning approach
- **Sensor characterization**: clear, rad. tolerance
- **Overview**: ILC DEPFET-System
- **R/O - electronics** (CURO- FE):

  architecture, circuit realization and results
- **Results** with present system (lab, beam test)
- Summary and Outlook

Activities in the SILAB

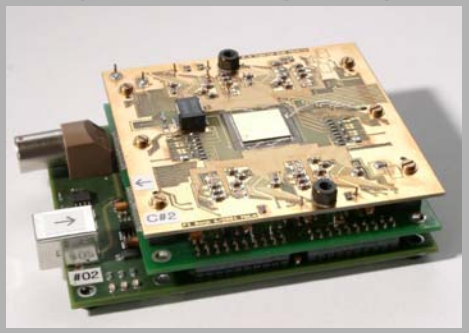
ATLAS pixels





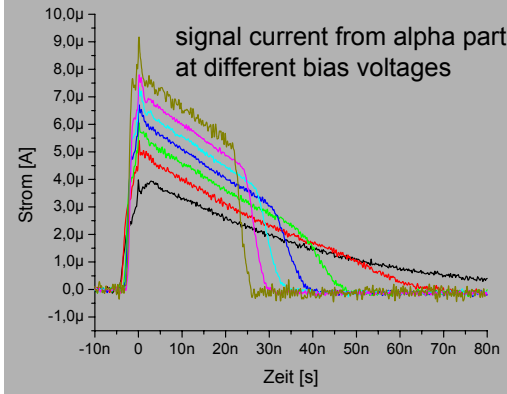
CdTe
2x2 module

X-Ray Imaging



SILAB
Silizium Labor Bonn

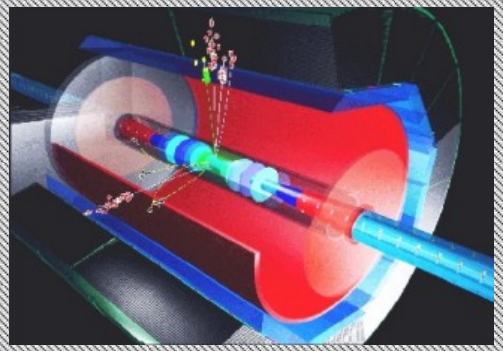
large experience in
ASIC design and
detector instrumentation

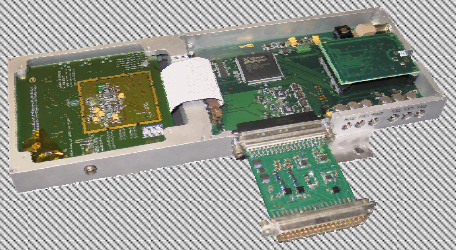


new materials

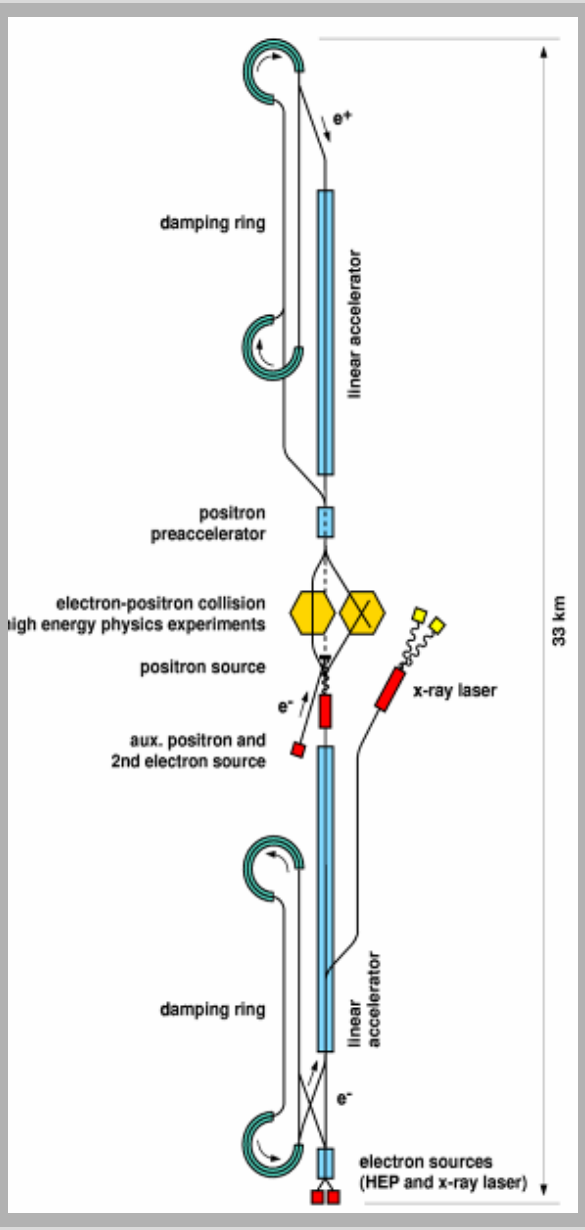
TCT –
transient
current
technique

DEPFET ILC vtx-d





International Linear Collider



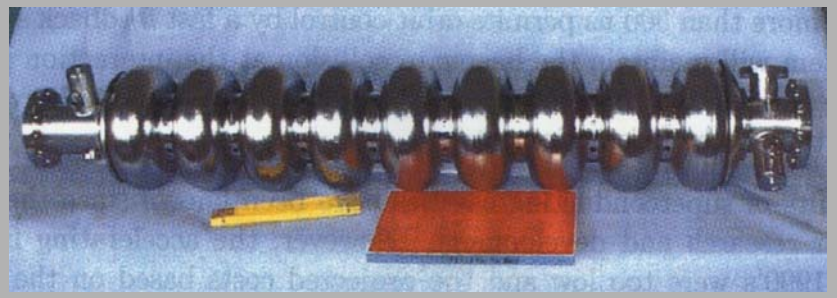
- design phase: ILC - TDR 2007, starting 2017 ?
- 3 detector concepts: LDC (TESLA), SiD, GLD
- precision measurements: $\delta(1/p) = 5 \cdot 10^{-5}$ / GeV (1/10 LEP, LHC)

e^+ e^- defined initial state

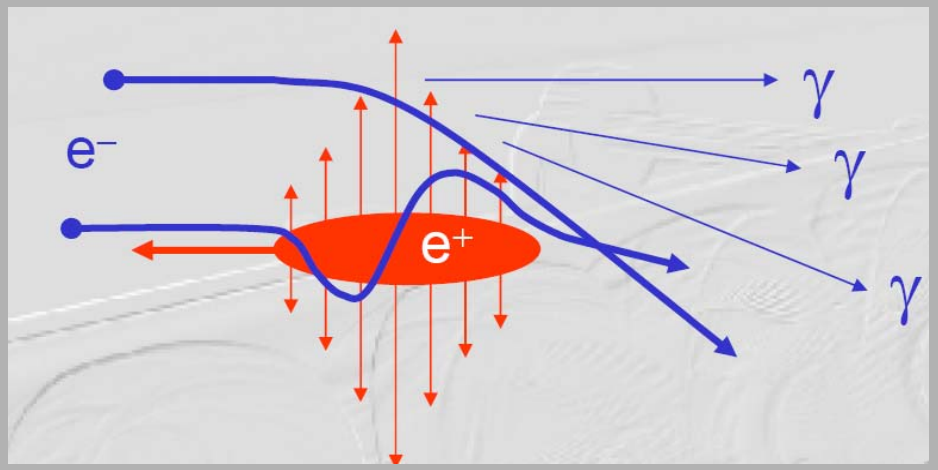
- luminosity $L = 3 \cdot 10^{34}\ cm^{-2}\ s^{-1}$, E_{CM} up to 1 TeV
- linear accelerator

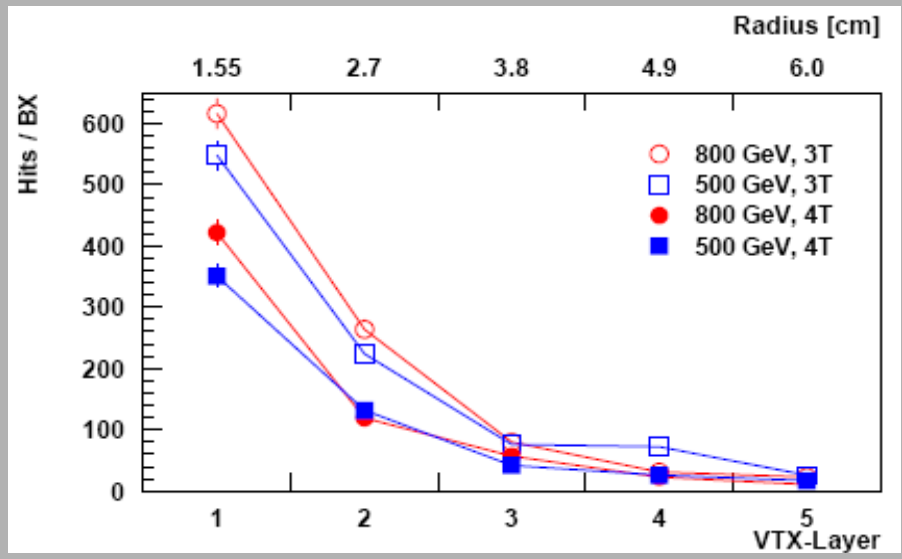
  → no synchrotron-radiation : $\Delta E_{sync} \propto E^4/m^4$

- superconducting accelerating cavities (>25MV/m):



Beamstrahlung (e^+e^- Pairs)



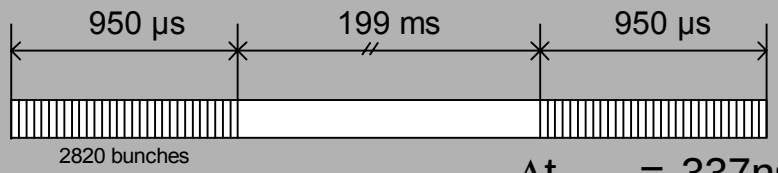


[C.Hensel]

$$\delta_{BS} = \frac{\Delta E}{E} \propto \frac{E_{cm}}{\sigma_z}\left(\frac{N}{\sigma_x^* + \sigma_y^*}\right)^2$$

layer 1: 0.05 hits / mm^2 / BX

bunch structure:



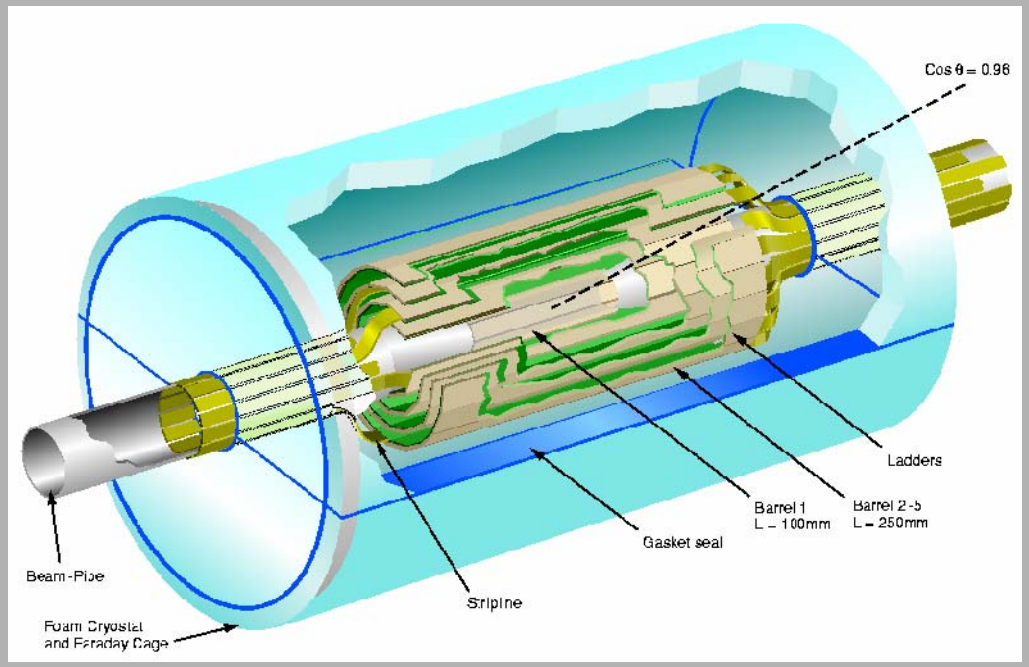
Δt_{bunch} = 337ns

5Hz repetition rate

occupancy: 20% (readout once !!)

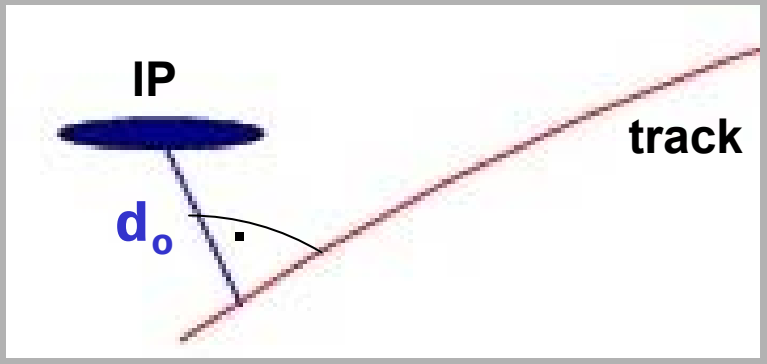
R/O: 50µs (20x per bunch train)

ILC Vertex Detector (LDC)



- 5 layers, r: 15mm ... 60mm
- pixel size: 20-30 µm, spatial resolution of a few µm
- module: ~ 13 x 100 mm^2, 22 x 250 mm^2
- overall ~ 1GPixel
- thin sensors d=50µm: 0.1% X_0 per layer
- low power consumption (simple gas cooling)
- radiation tolerance: 200 kRad (5 years)

Impact Parameter Resolution (d_o)



$$\sigma = \sqrt{a^2 + \left(\frac{b}{p\sin^{\frac{3}{2}}\theta}\right)^2}$$

$a < 5\,\mu m$ (point precision)

$b < 10\,\mu m$ (multiple scattering)

<p> = 1...2 GeV

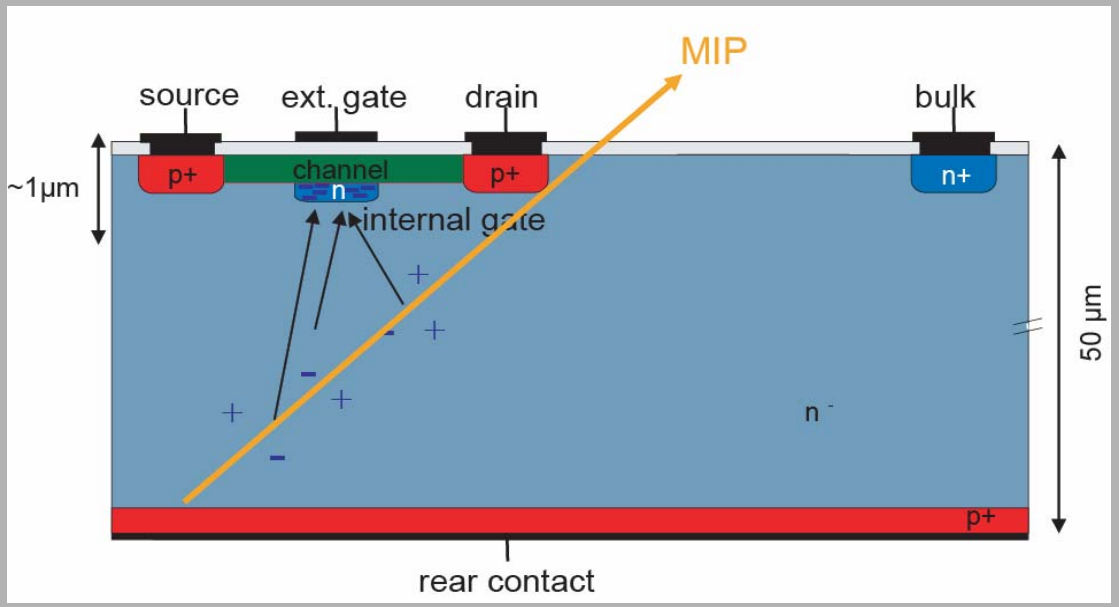
b : 300µm

c, τ : 75µm

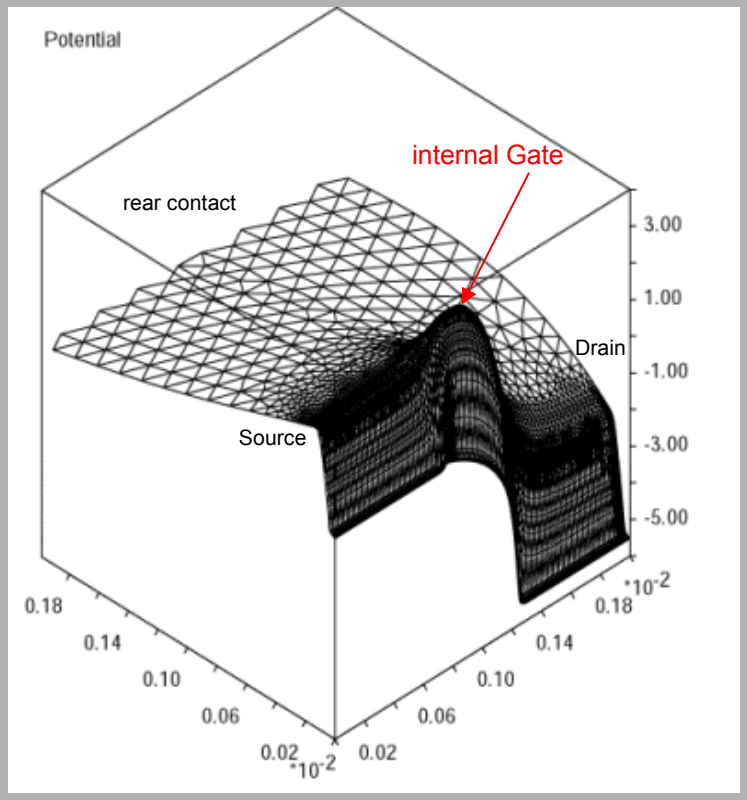
Technologies:
- **CCDs / ISIS**
- **MAPS/CMOS**
- **DEPFET**

DEPFET principle of operation

principle



potential distribution:



[TeSCA-Simulation]

- FET-Transistor integrated in pixel (first amplification)
- charge generation in whole substrate (d=50µm, **ENC=100e⁻**: S/N > 40)
- charge collection due to electric field
- figure of merit: internal gain ($g_q = \Delta I_D / \Delta q$)

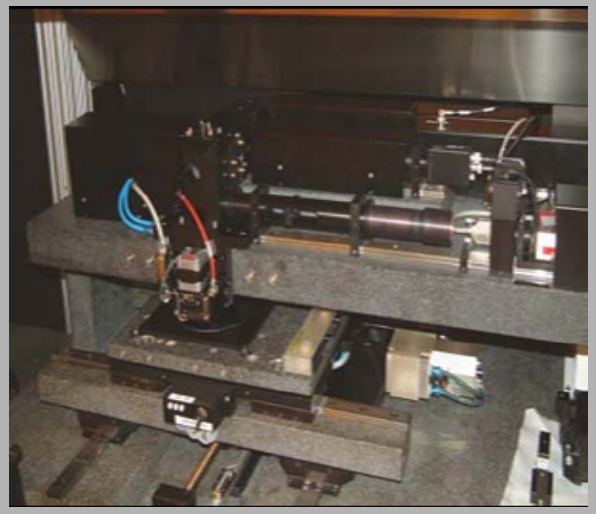
DEPFET Fabrication

design, fabrication and testing
of DEPFETs at the **HLL MPI Munich**:

- 800m^2 clean room (class 1),
- 6“ process line,
- min. feature size 1.5µm

HLL located at the Siemens plant
in Neu-Perlach (founded 1992)

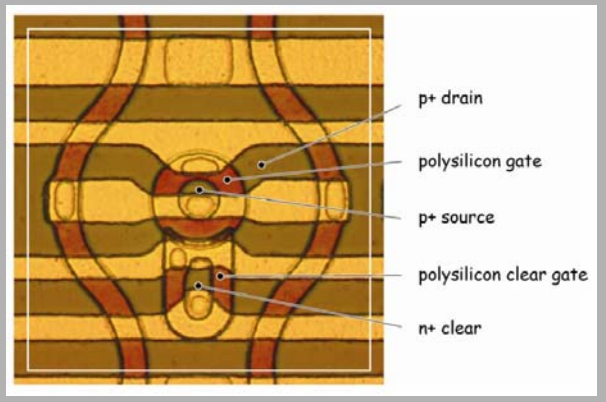
direct wafer writer (UV laser):

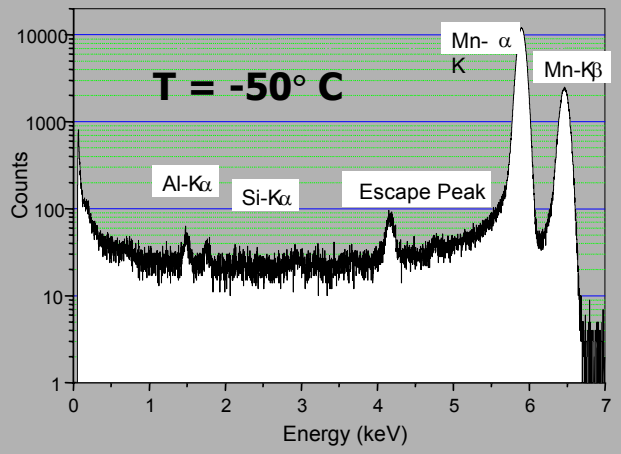


DEPFET Applications

XEUS pixels on same PXD4 wafer run as ILC

XEUS – The X-Ray Evolving Universe Spectroscopy Mission	ILC
imaging spectroscopy **Xray astronomy**	**particle tracking** **HEP**
7.68 x 7.68 cm² 1024 x 1024 pixels 1 MPix	1.3 x 10 cm² (x 8) 520 x 4000 pixels (x 8) 1GPix
75 µm	**25 µm**
300 ... 500 µm	**50 µm**
< 4 el. ENC	~100 el. ENC
1.2 ms **2.5 µs**	**50 µs / frame** **50 ns / line**



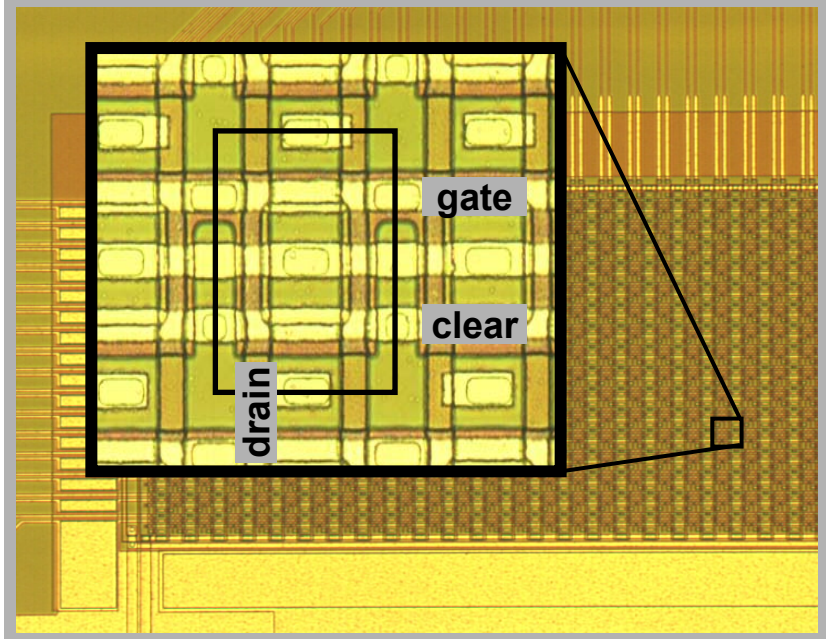


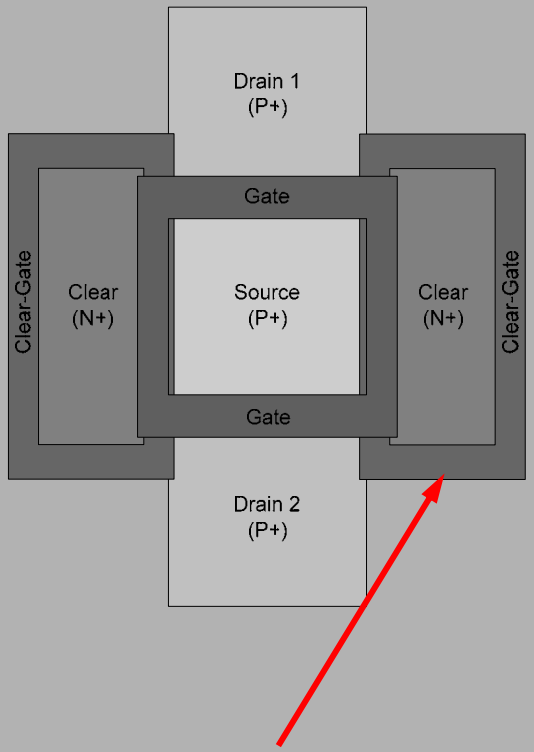
energy resolution:
126 eV FWHM @ Fe^{55} - k_α line
corresponding to **4.9 e^- ENC**

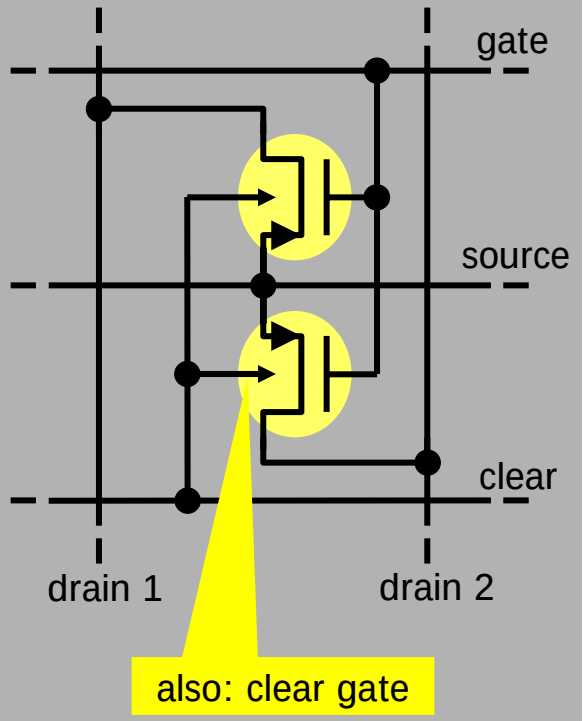
sensor production for the ILC

fabricated: matrices with up to 128x64 pixel, 450µm thick

linear double pixel structures (22x36 µm² pixels) (high density layout)



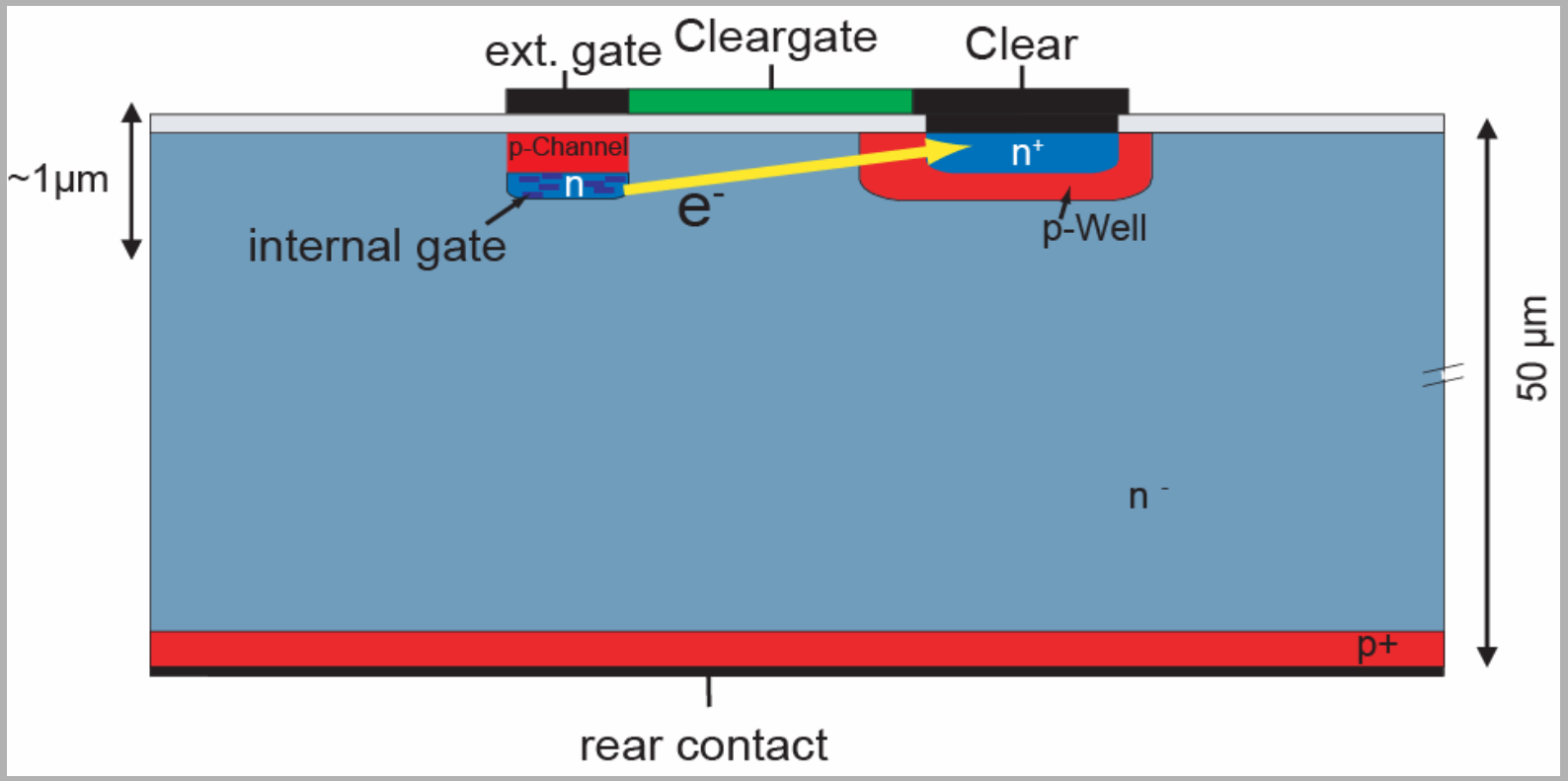




- **new production** started recently 03/2006:
- matrices up to 512x512 pixel
- full ILC length column & row test structures

special **clear gate**
to support clear operation

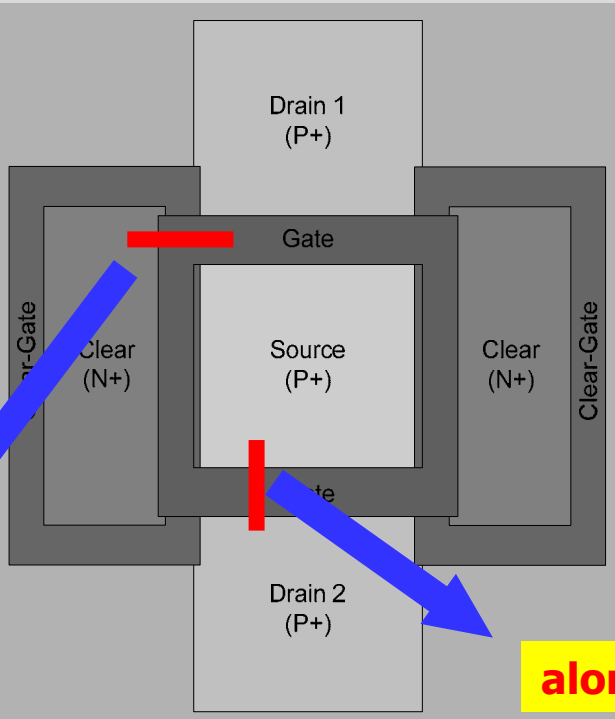
DEPFET clear operation



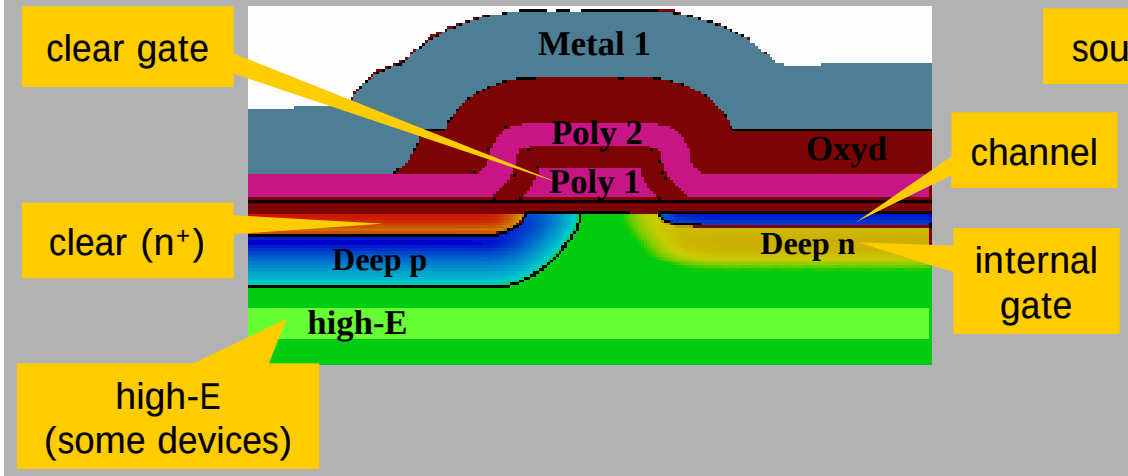
- remove charge via „clear“ contact
- remove all charge → complete clear
  no „reset-noise“, needed at the ILC

DEPFET clear operation (details)

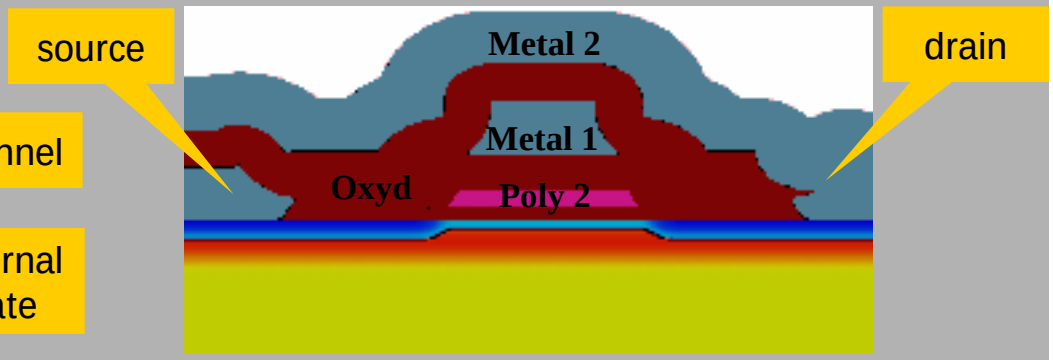
- **'clear gate'** to lower the clear barrier
  Clocked and **static** operation possible
- deep **high-E** n-implantation in some devices
  to lower clear voltages



perpendicular to channel

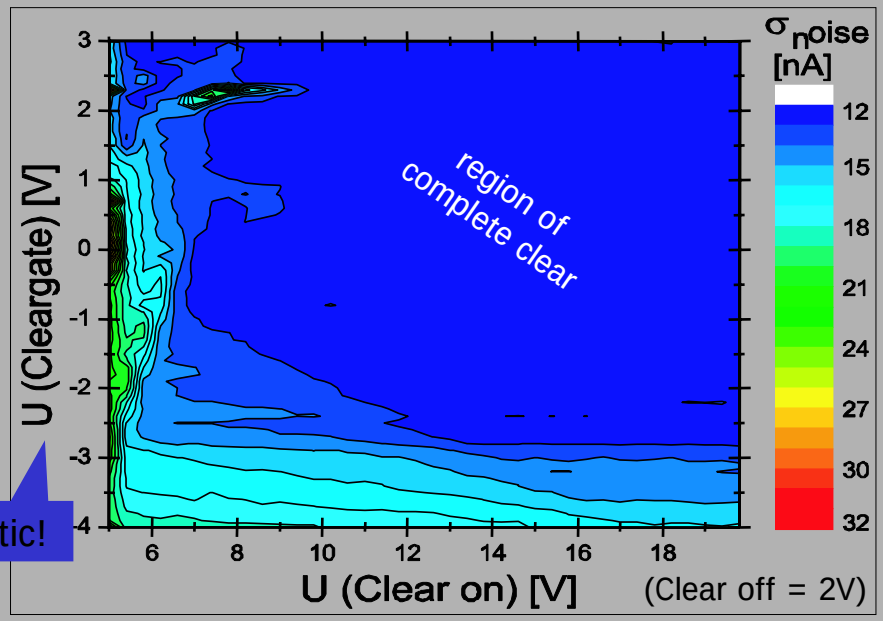


along the channel



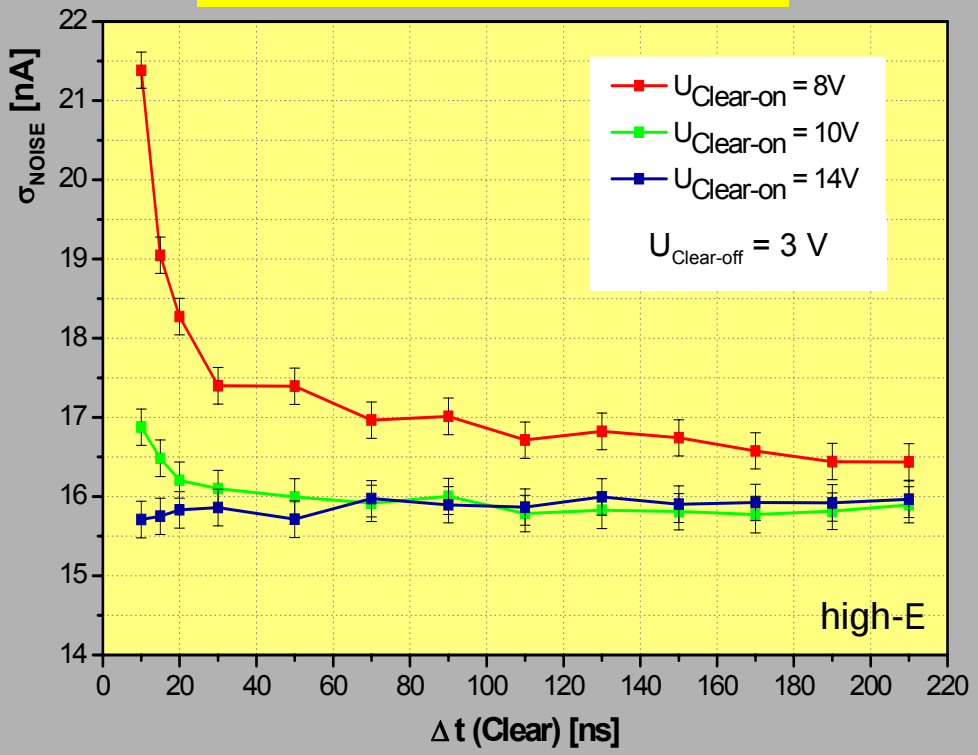
clear efficiency

- Measurements on mini matrix devices
- 'noise' becomes minimal if clearing is complete!



- complete clear achieved with static clear gate!
- required voltages small (5 – 7 V) – important for future SWITCHER!
- clear (gate) operation does not decrease after irradiation (1MRad)

Complete clear in only 10 ns:



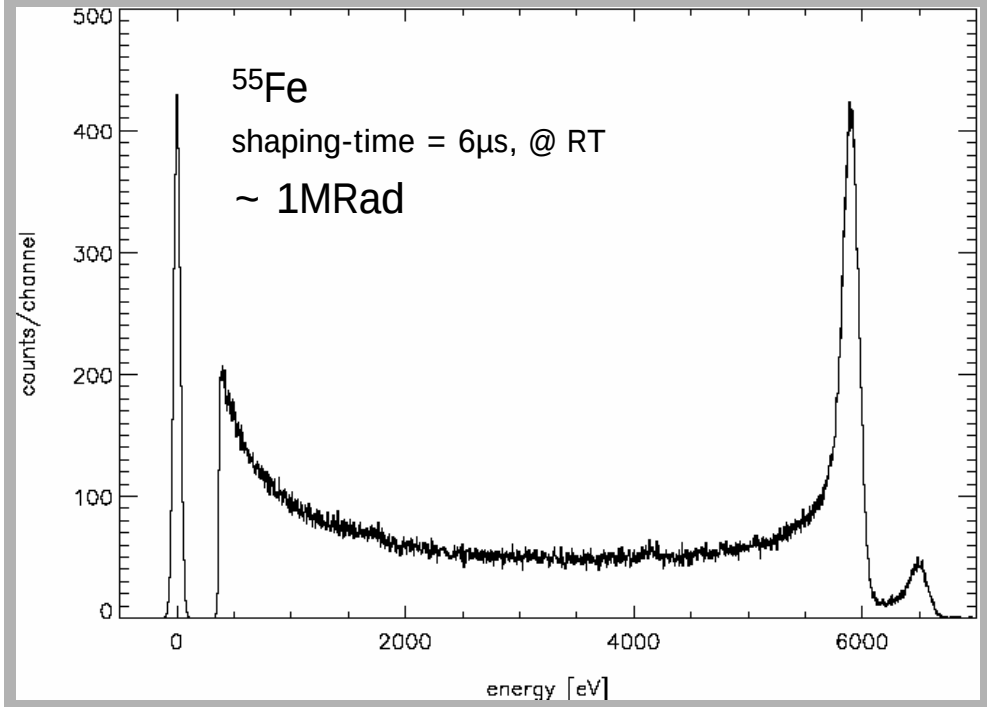
- various designs (high-E, no high-E)
- geometries (length of clear gate)
- operating conditions (static or clocked clear gate)

[C.Sandow, Bonn]

radiation tolerance: sensor

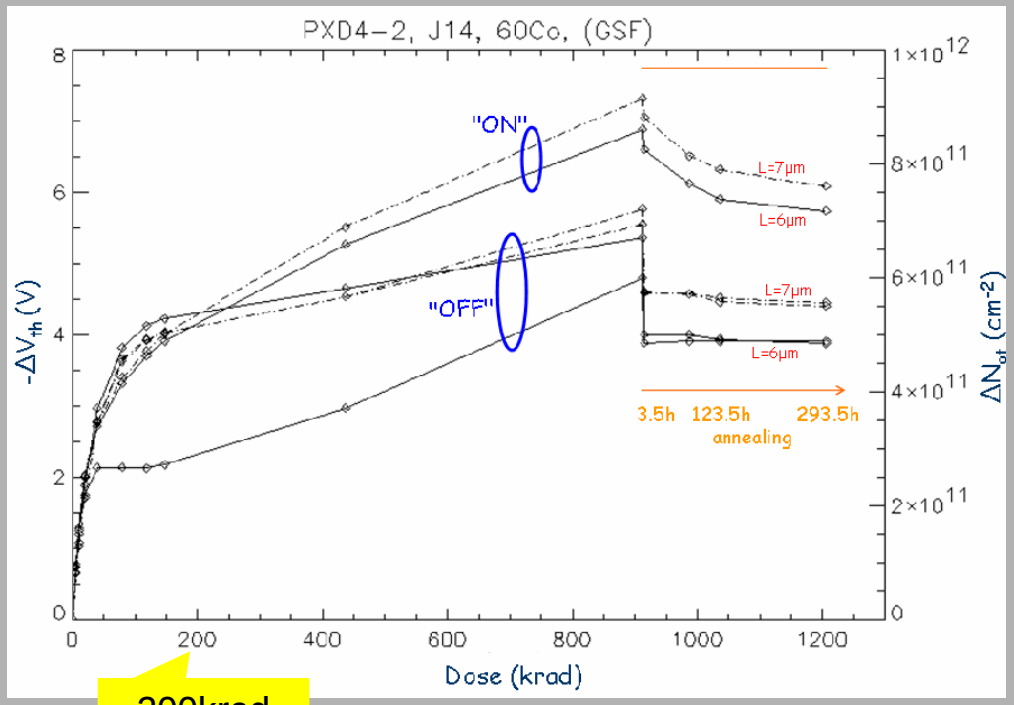
irradiation up to 1MRad using ^{60}Co

single pixel spectrum



from iron-peak: ENC ~ 15 e$^-$
(comparable with preirrad. structures)

shift of threshold voltage of MOSFETs
(oxide thickness ~200nm)



200krad

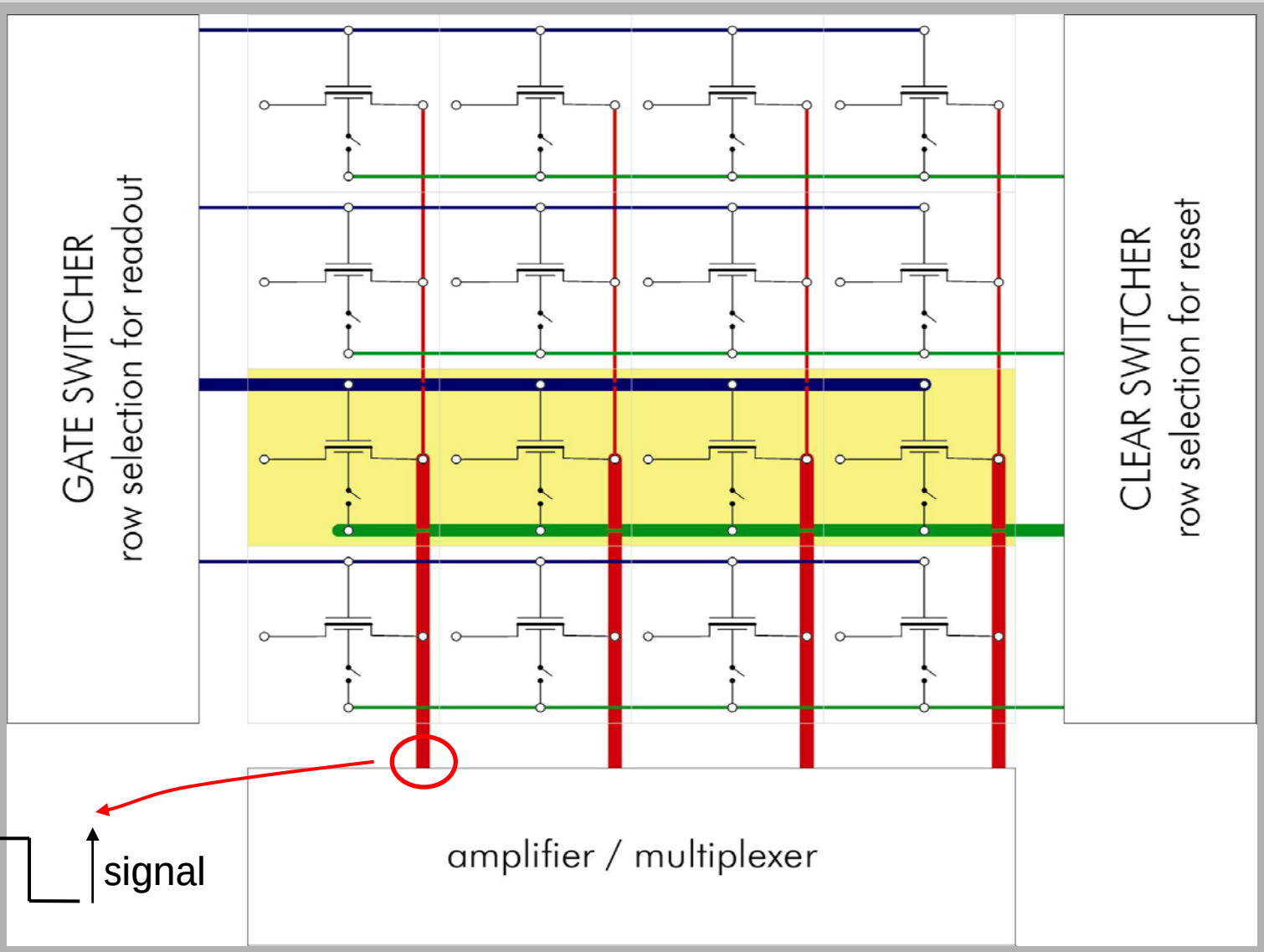
- **shift**: - 4...- 6 V
- saturation after 200 kRad

[L.Andricek, MPI Munich]

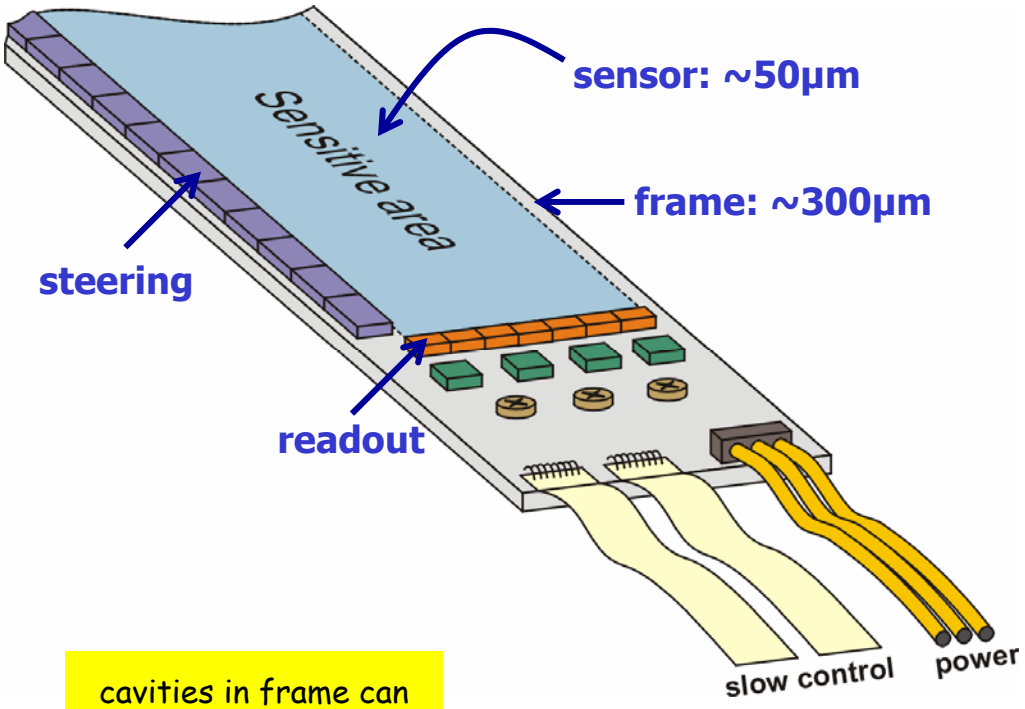
matrix operation

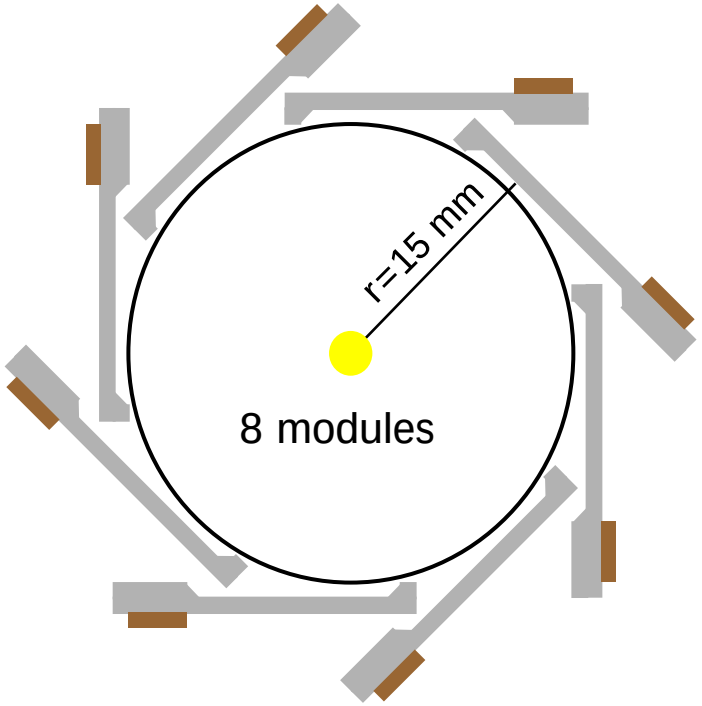
- **low power consumption,**
- **low multiple scattering**

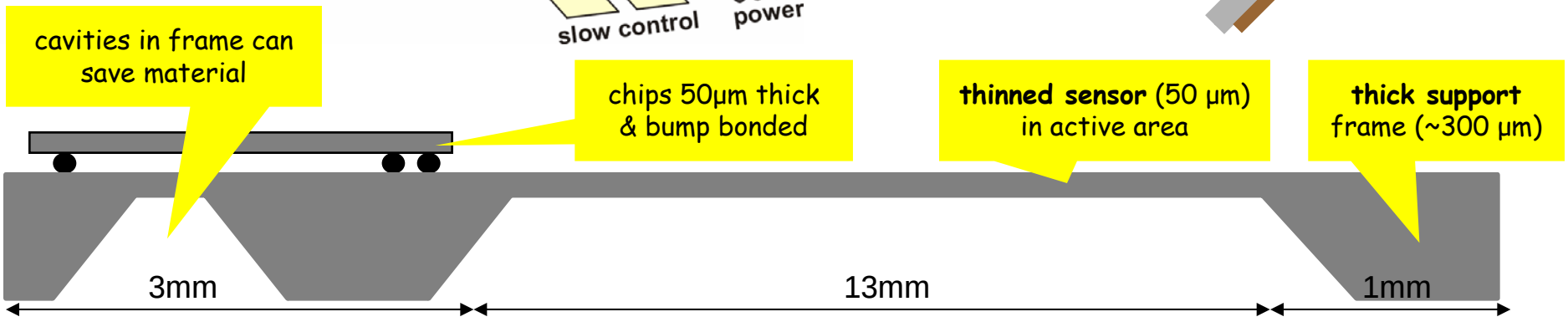
but line rate:
≥ 20MHz



ILC - DEPFET module (L1)

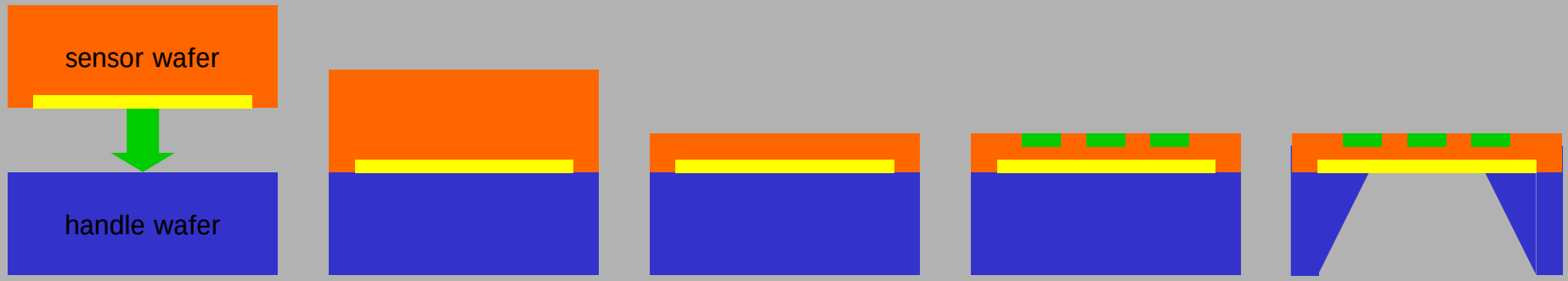






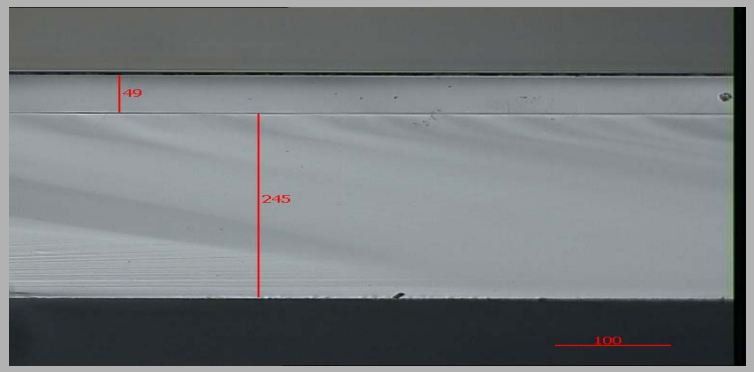
material budget (1st layer, incl. steering chips and frame) ~ 0.11 %X_0

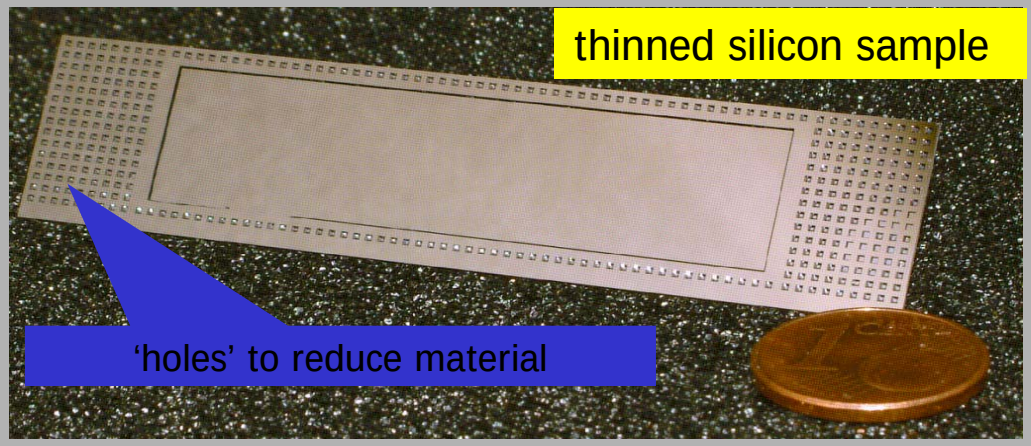
Producing thin DEPFETs



1. implant backside on sensor wafer
2. bond wafers with SiO_2 in between
3. thin sensor side to desired thick.
4. process DEPFETs on top side
5. etch backside up to oxide/implant

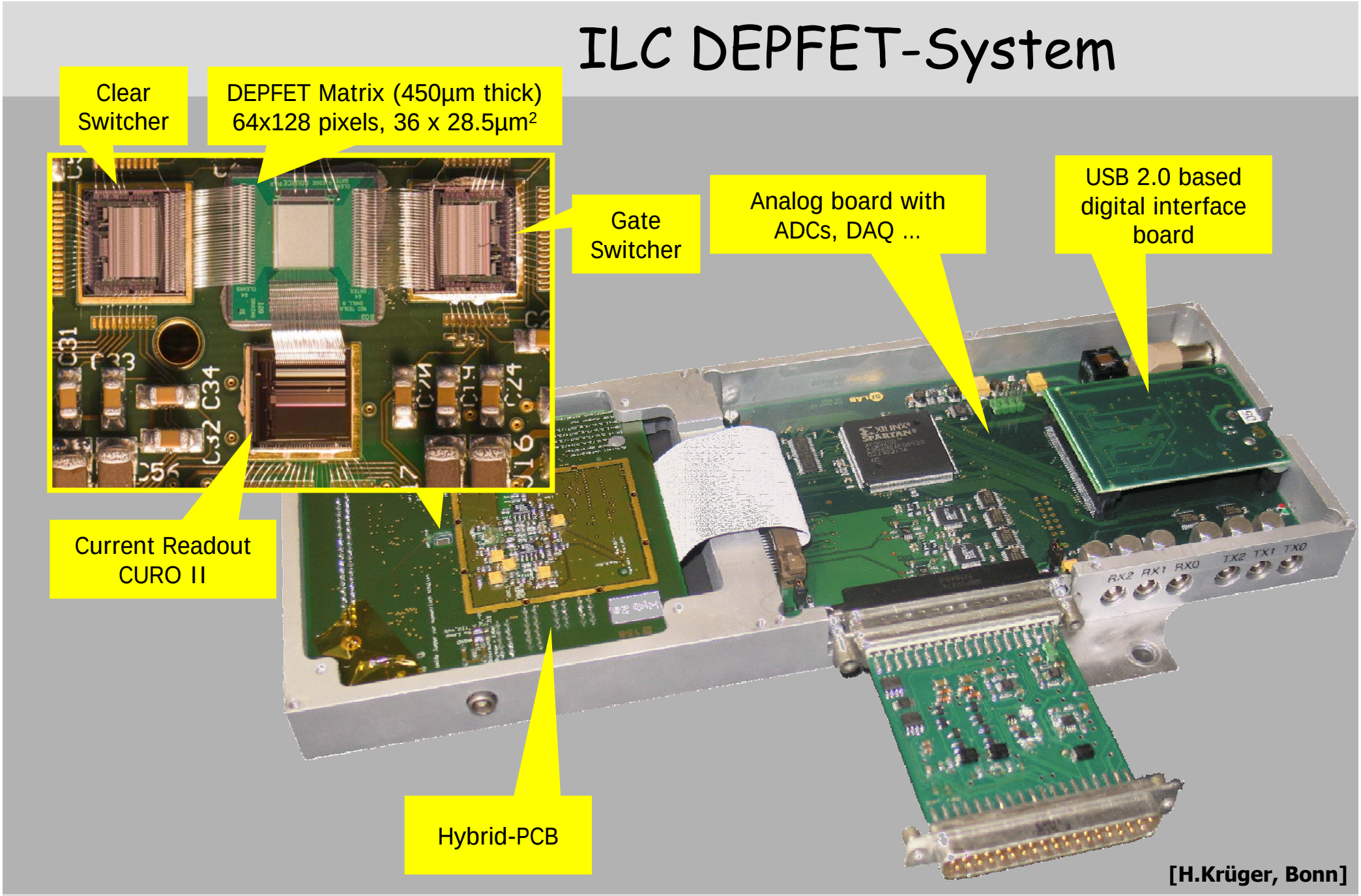
wafer bonding:





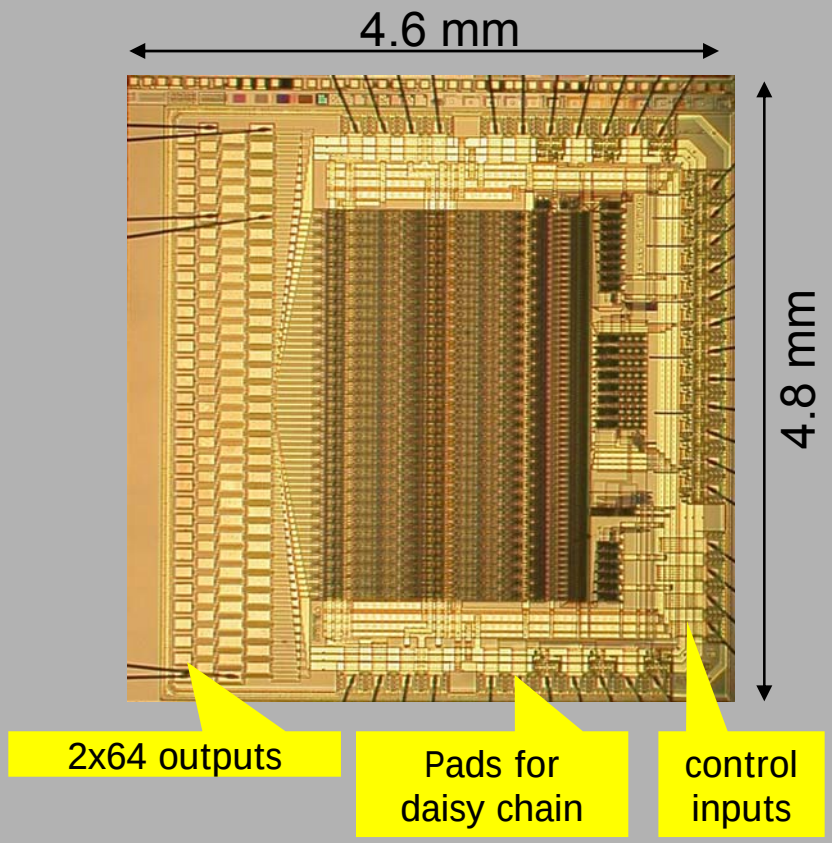
[L.Andricek, MPI Munich]

ILC DEPFET-System



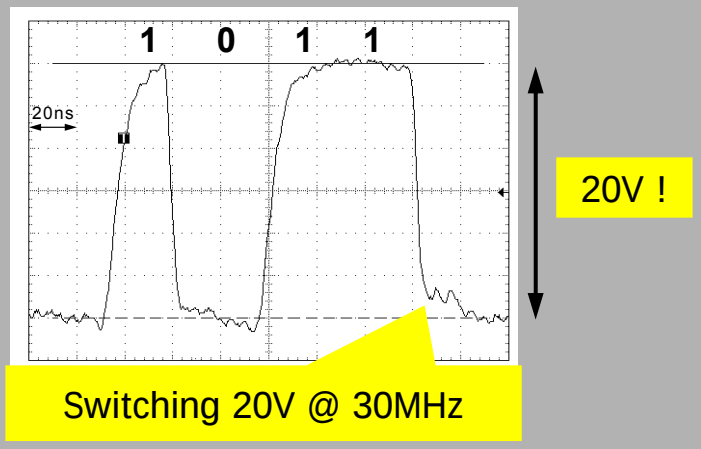
[H.Krüger, Bonn]

steering chip SWITCHER



Features:

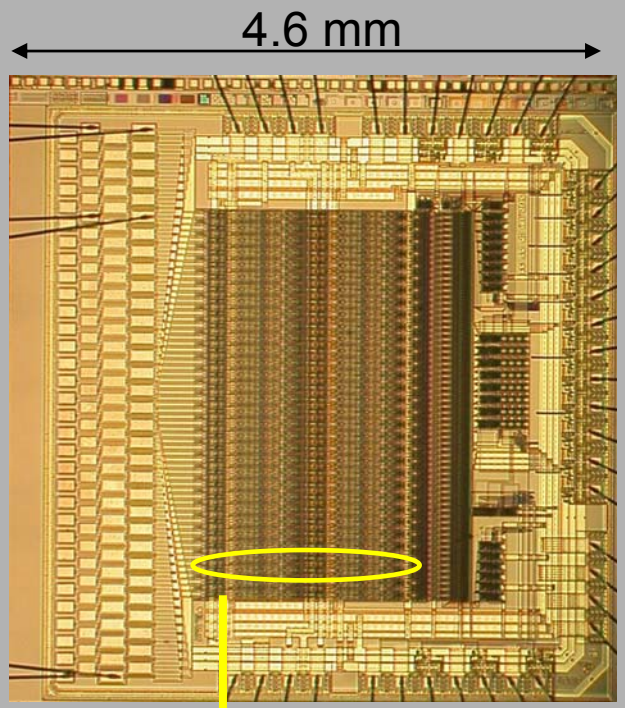
- **produced 1/2003**
- **2 x 64 channels ('A' and 'B')**
- switches up to 25 Volts
- **ground levels arbitrary**
- internal sequencer **(flexible pattern)**
- **daisy chaining of several chips for modules possible**
- **0.8 µm AMS HV – technology**
- radiation tolerance may be problematic!



- functionality proven ✓
- **RAM & sequencer (digital) tested up to 80 MHz**
- power consumption ~ 1mW / channel @ 30MHz

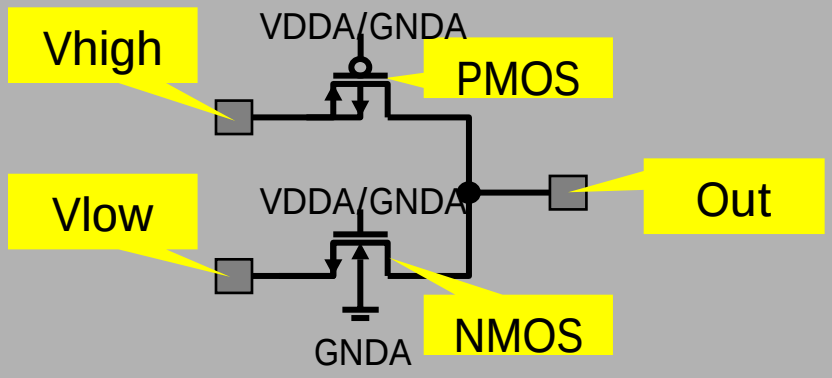
[I.Peric, Mannheim]

SWITCHER: speed

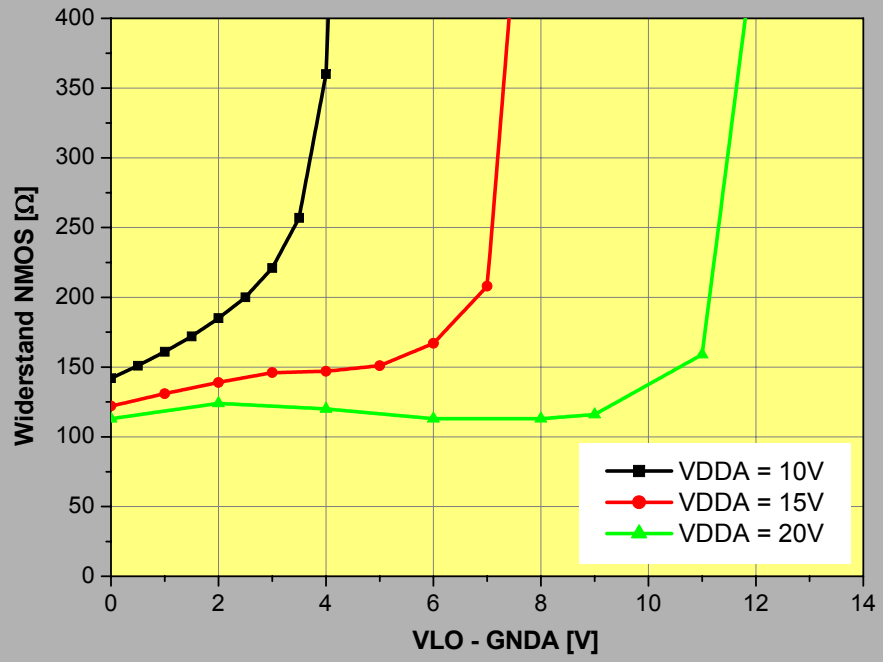


[I.Peric, Mannheim]

>50% Layout size !



nmos (Vlow):



typical value: **< 200 Ω**

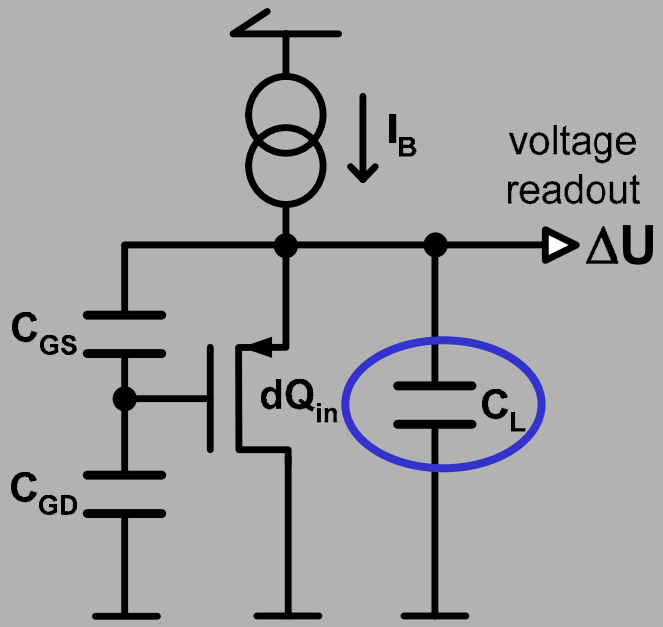
C_{row}=15pF

→ τ = 3ns

(fast steering !)

DEPFET readout: drain vs source

source (follower) R/O

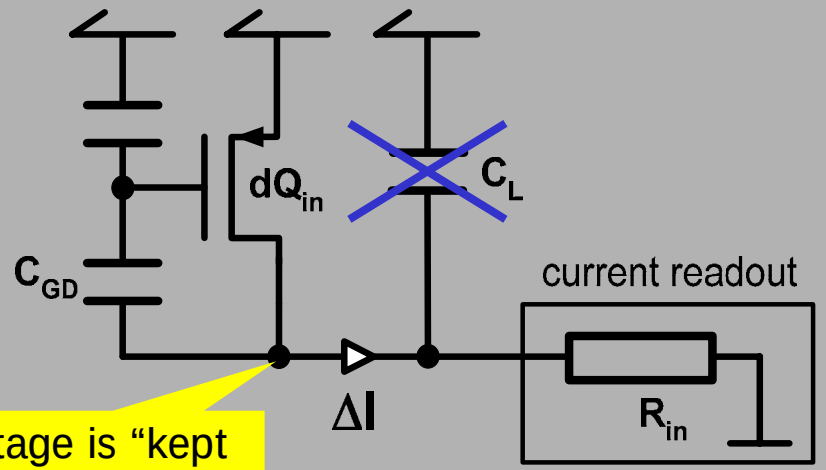


- constant bias current I_B provided
- charge in internal gate translates into source voltage node change

$$\tau = 2.2 \times \frac{C_L\,(1+C_{gs}/C_{gd})}{g_m} \approx \mu s$$

no option for ILC

drain R/O



voltage is "kept constant"

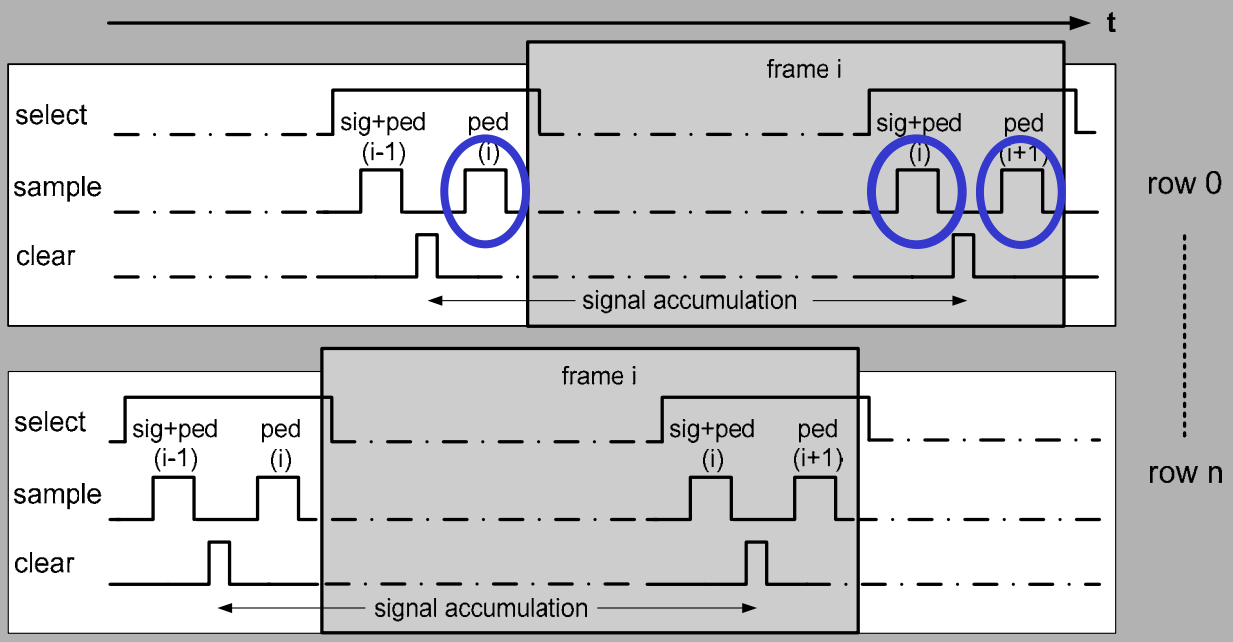
- keep V_{DS} constant, measure I_{Drain} directly
- fast response: limited by RC time of R_{in} (CURO) and C_L

→ few ns @ C_L =40pF

readout mode @ ILC

ILC: no „trigger“ → hit detection / 0-suppression in readout chip

„rolling shutter“



advantage:

- 0-suppression while processing one row

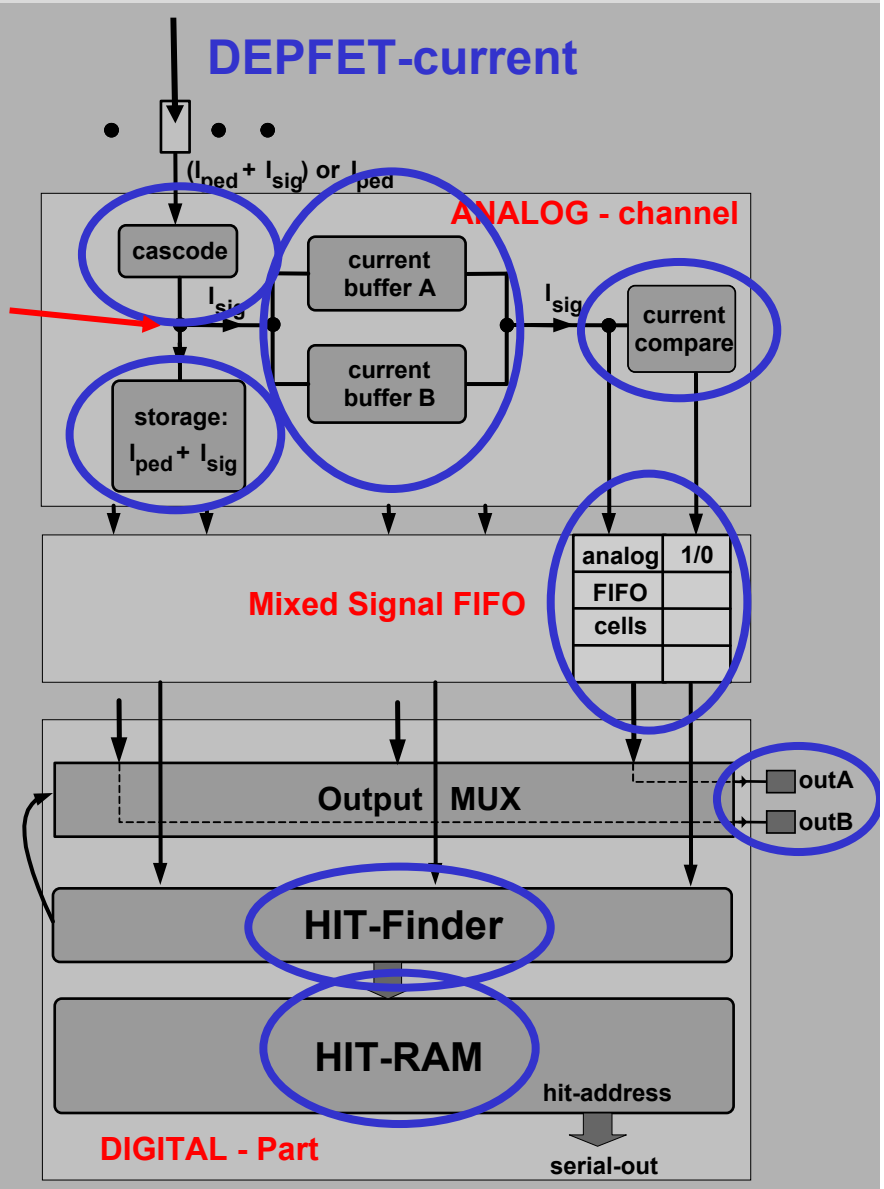
- fast CDS (suppresses 1/f noise)

needed: - complete „clear“ (demonstrated !)

overview: CURO-Architecture

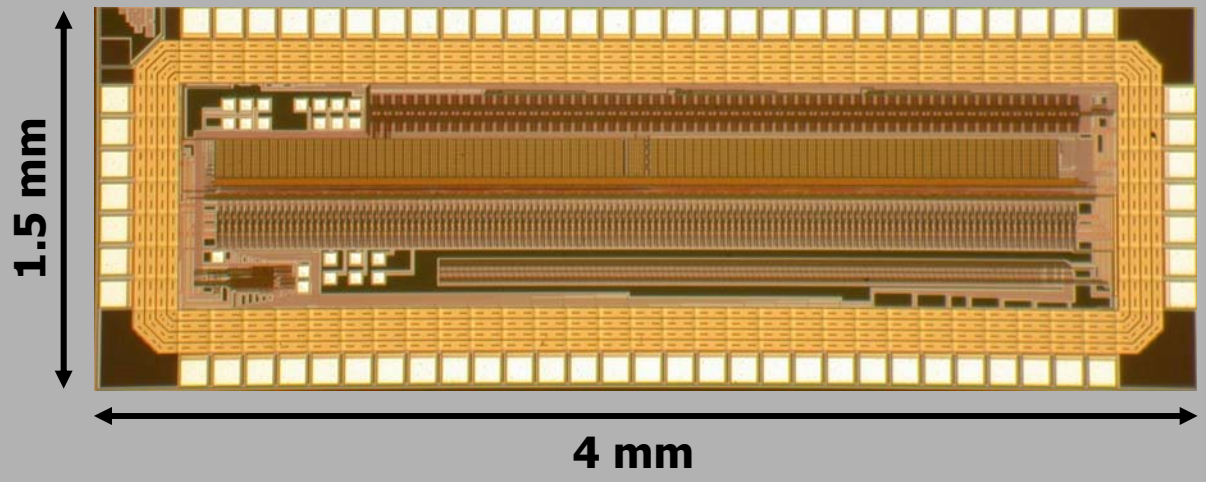
CURO – **CU**rrent **R**ead**O**ut

- current based readout
  → **low input impedance by regulated cascode**
- **pedestal + signal** is stored in **current memory cell**
- **pedestal current** is subtracted at input node **after reset** (fast CDS)
- **signal current** buffered (alternating) in **2 cells**
  → hit-identification, **FIFO storage**
- FIFOs **digital part** is scanned by **HIT-Finder**
- Hit-Finder finds up to 2 hits per cycle:
  - **analog currents** to outA, outB
  - **digital hit position** stored in HIT-RAM



CURO I (testchip)

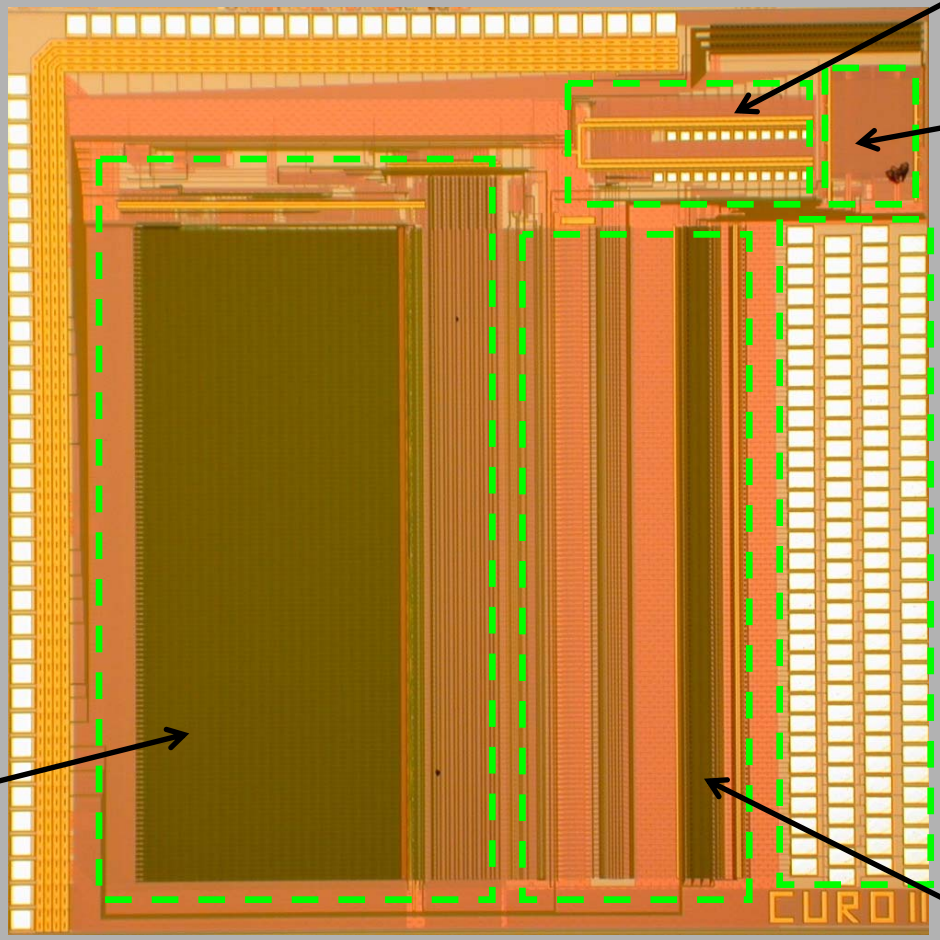
- TSMC 0.25µm
- 5metal layer
- contains all building blocks of CURO-Architecture
- radiation tolerant layout rules with annular nmos
- 05/2002



r/o concept proven !

CURO II

- TSMC 0.25µm
- 5 metal layer
- 4.5 x 4.5 mm^2
- 11/2003



steering unit:
~ 20 steering signals

12x **8bit DACs**
Biasing, test currents, thresholds

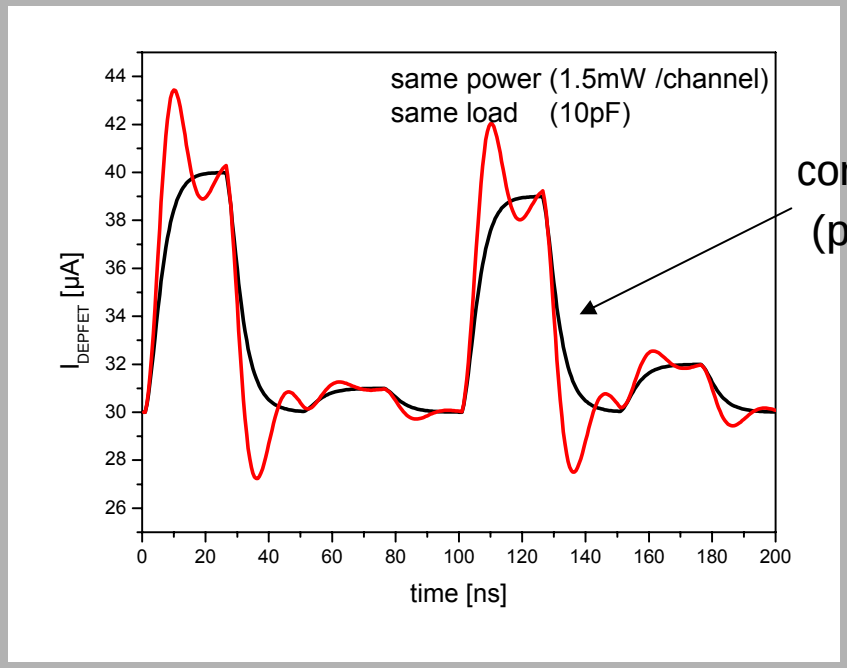
pads (communication):
fast signals: LVDS

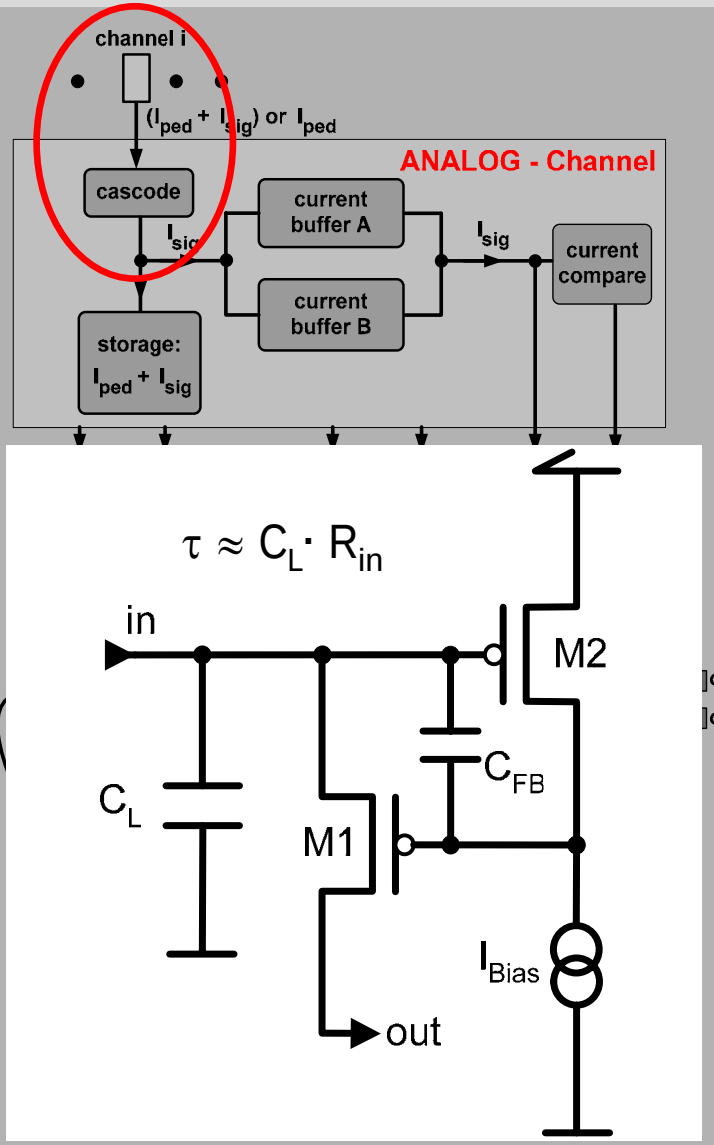
128 input channel
(DEPFET - Matrix)

digital part:
Hit-Finder,
RAM, FIFO

analog part:
current memory cells,
comparator

input cascode





$$\nu_{gr} = \frac{g_{m2}}{2\pi\, C_L}$$

higher $\mathbf{g_m}$ by higher $\mathbf{I_{Bias}}$ → **speed** vs. **power**

present-matrices : 7.5pF; final ILC-matrices: ≈ 40pF !!

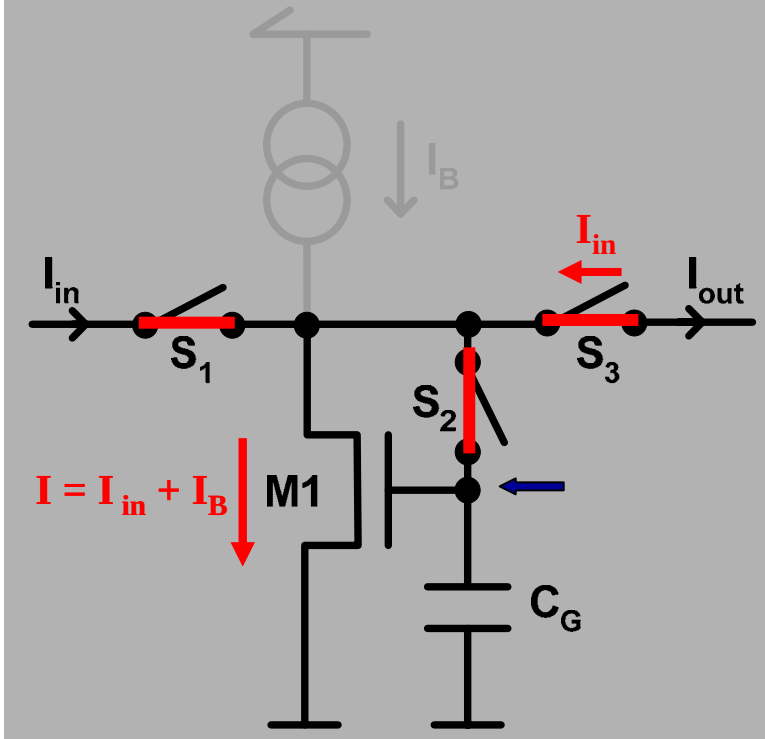
CUROIIb: power down feature

IBias = **1µA** static operation → **fix input potential**

500µA → high speed operation

cascode compensates load capacitance

current memory cell (principle)



[Hughes/Toumazou]

(use of cascode techniques !)

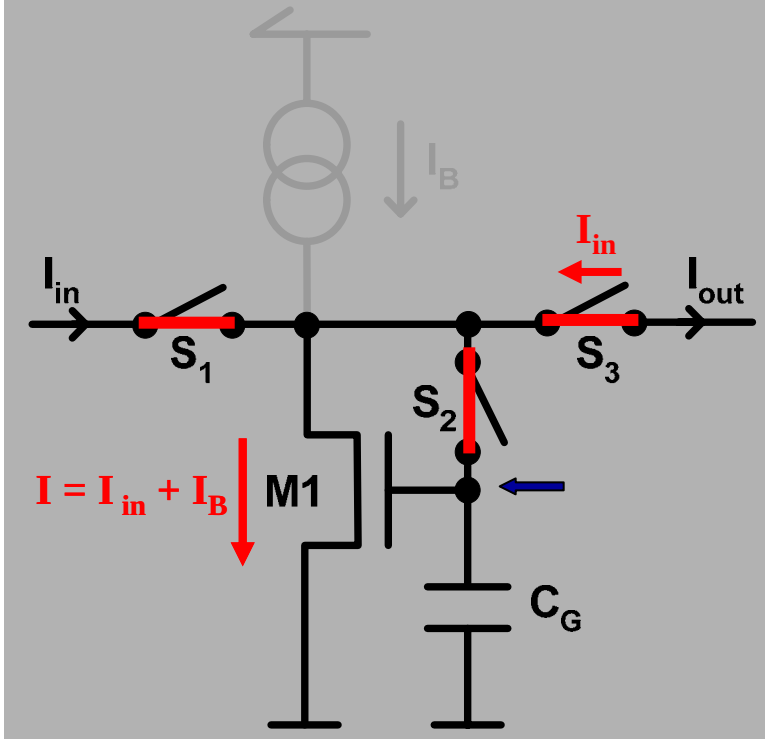
store current ??

charge: input (S1) and sample-switch (S2) closed
→ charge gate-capacitance of M1

sample: open input (S1) and sample-switch (S2)
→ voltage at capacitance „same“
→ current „same”

transfer: close output-switch (S3)
(right after “sampling”)
→ $I_{out} = - I_{in}$ at output node

current memory cell (advantages)

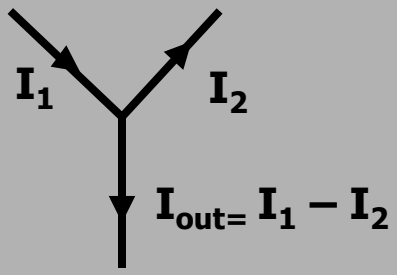


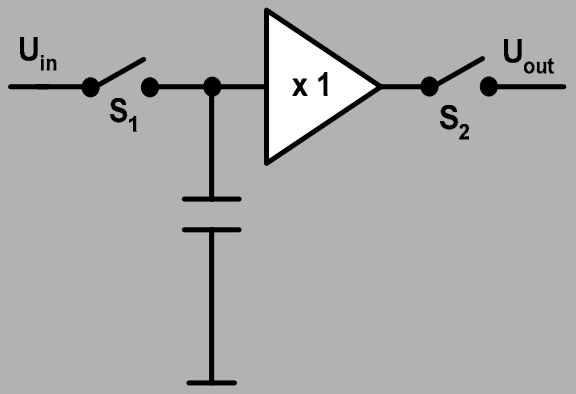
[Hughes/Toumazou]

(use of cascode techniques !)

advantages:

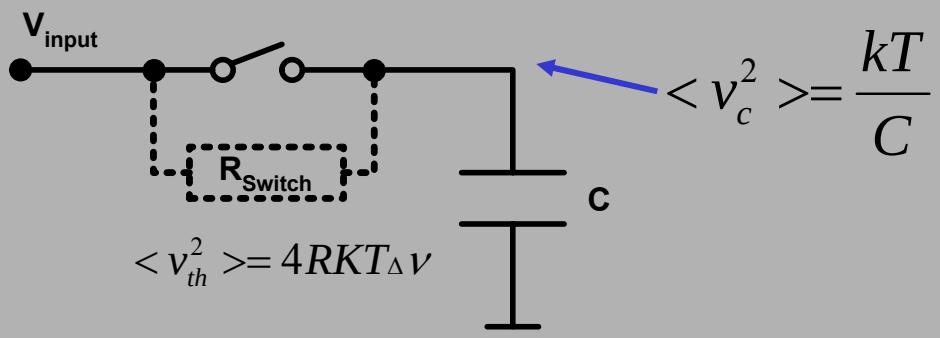
- high dynamic range (with reduced supply voltage)
- precise current subtraction easy
- drivers not needed





noise vs. time response

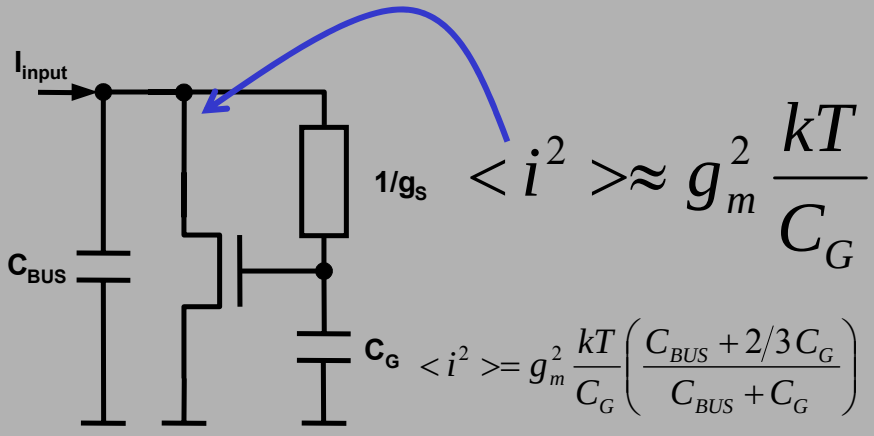
noise contribution



$$< v_c^2 >= \frac{kT}{C}$$

$$< v_{th}^2 >= 4RKT\Delta\nu$$

(independent of R)

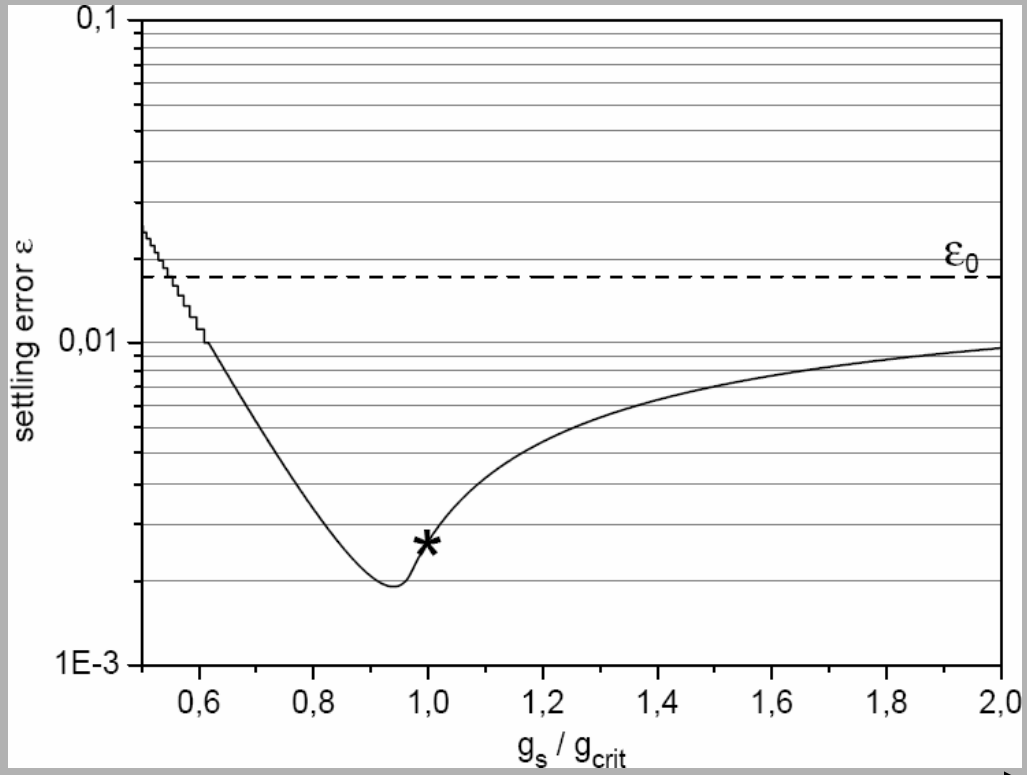


$$< i^2 >\approx g_m^2 \frac{kT}{C_G}$$

$$< i^2 >= g_m^2 \frac{kT}{C_G}\left(\frac{C_{BUS} + 2/3 C_G}{C_{BUS} + C_G}\right)$$

- g_m small, C_g large, C_{BUS} minor importance

time response

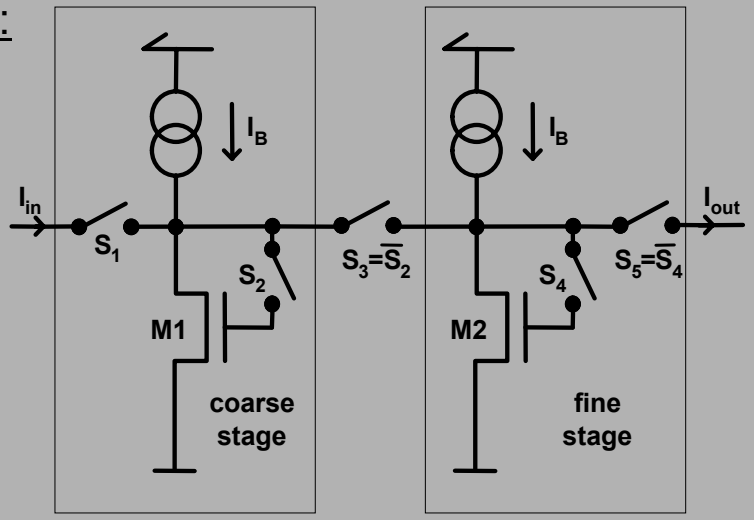


$$\tau = \frac{C_G + C_{BUS}}{g_m}$$

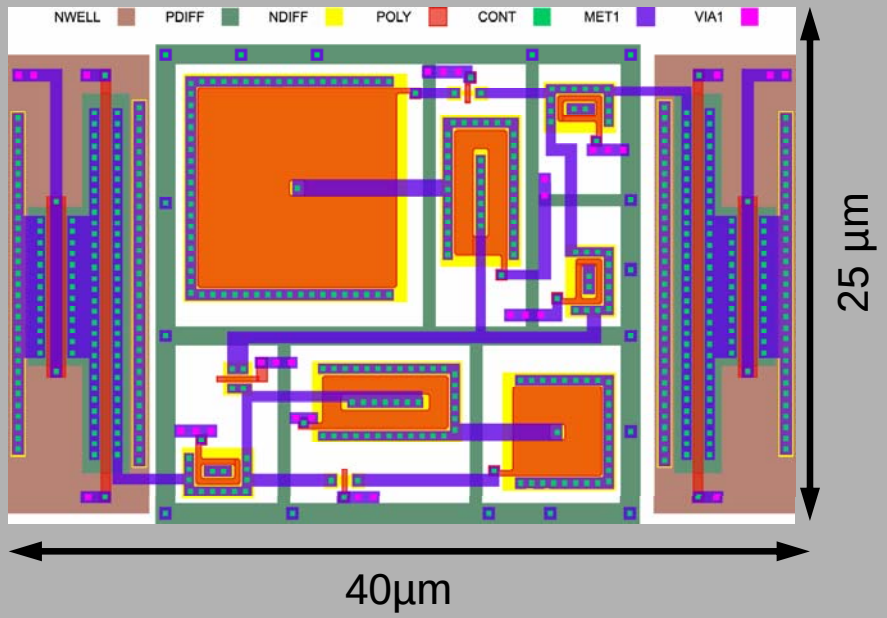
- **switch optimizes time response**
- **noise vs. bandwidth**
- **minimize bus capacitance**

two stage sampling cell

schematic:



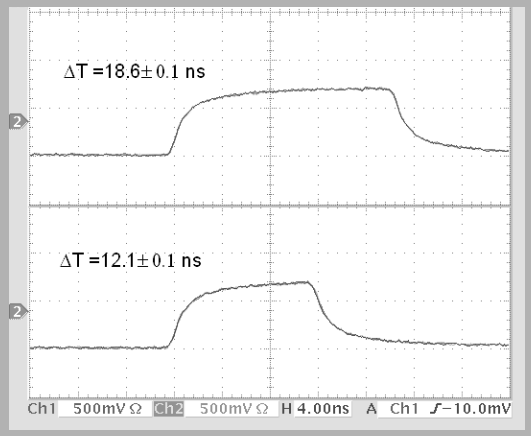
layout:



(+) improves linearity
(non-linearity due to charge injection)

(-) more complex steering ! (all signals generated „on-chip“)

coarse sampling:



different designs:
coarse stage: fast, noise does not contribute
fine stage: „slower“, optimized for noise

calculated noise: ~ 25nA, bandwidth: 50MHz

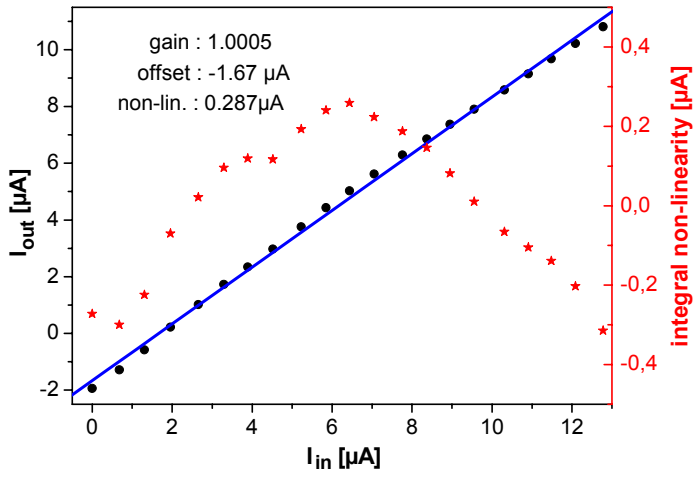
Linearity + Pedestal Subtraction

all analog measurements @ 24MHz line rate (sampling with 48MHz)

- linearity:

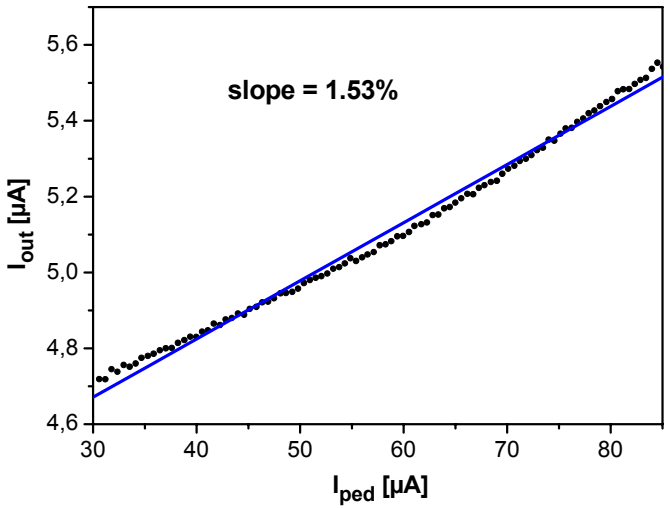
transfer gain:
1.00± 0.01

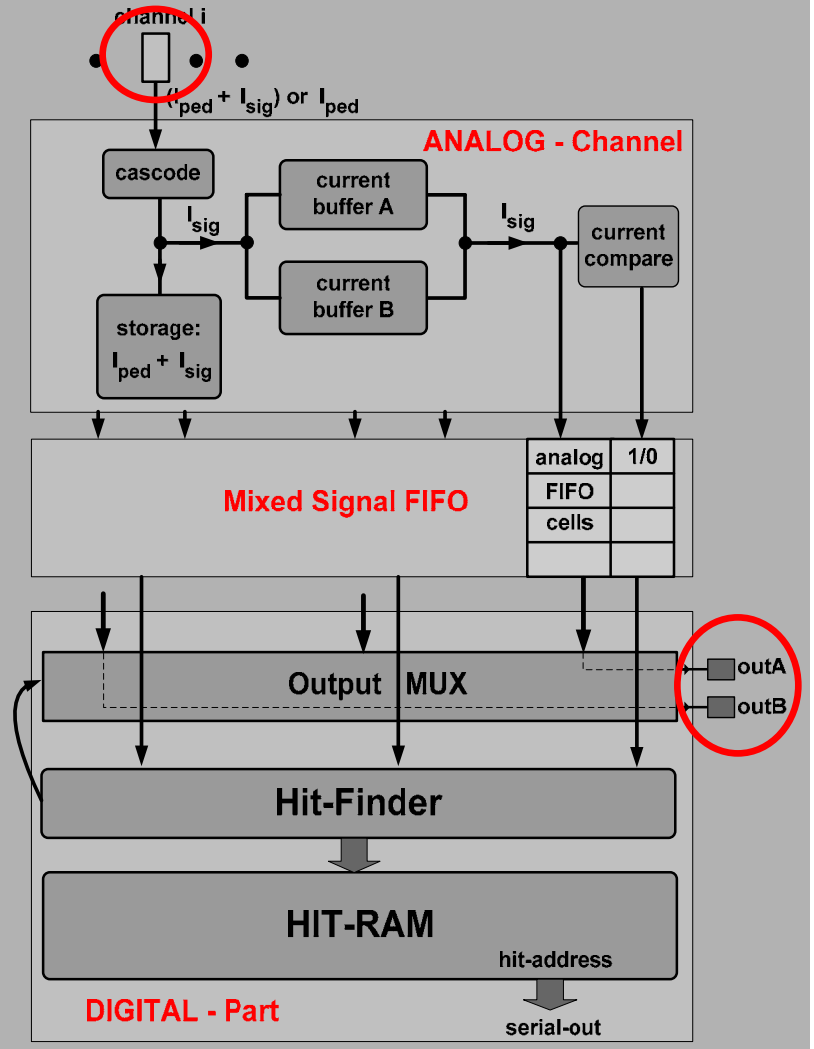
INL= 2,3 %
(**I**ntegral **N**on **L**inearity)



- pedestal subtraction:

e.g.
5µA (10%)
pedestal dispersion
→ **75nA** after
pedestal subtraction





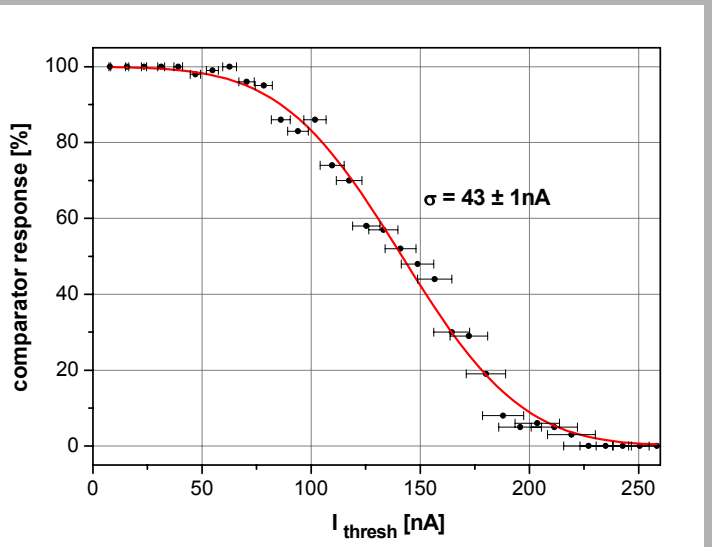
Noise & Dispersion

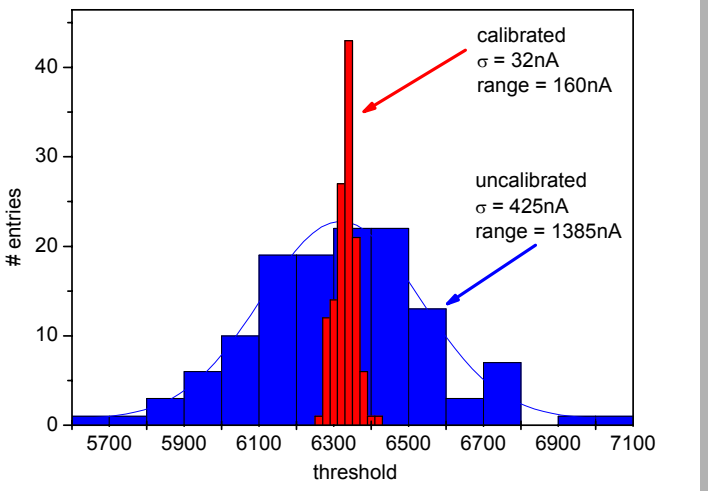
- noise:

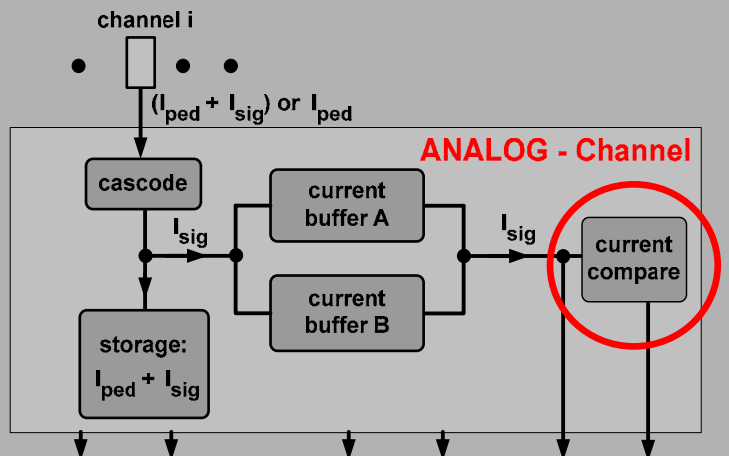
  DEPFET r/o with CURO:

  ENC ~ 90e$^-$

  (g_q=500pA/e$^-$)



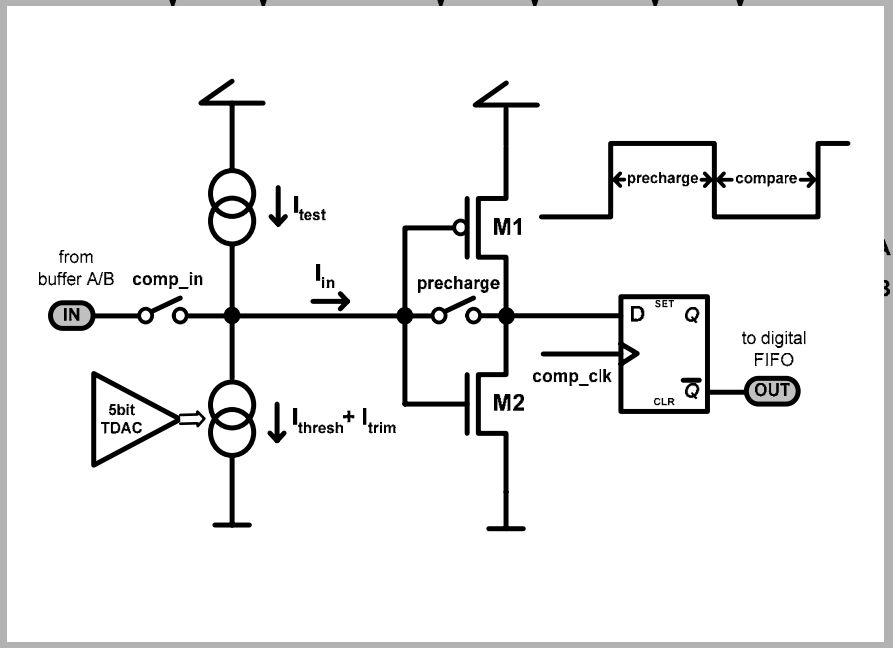




- Dispersion:

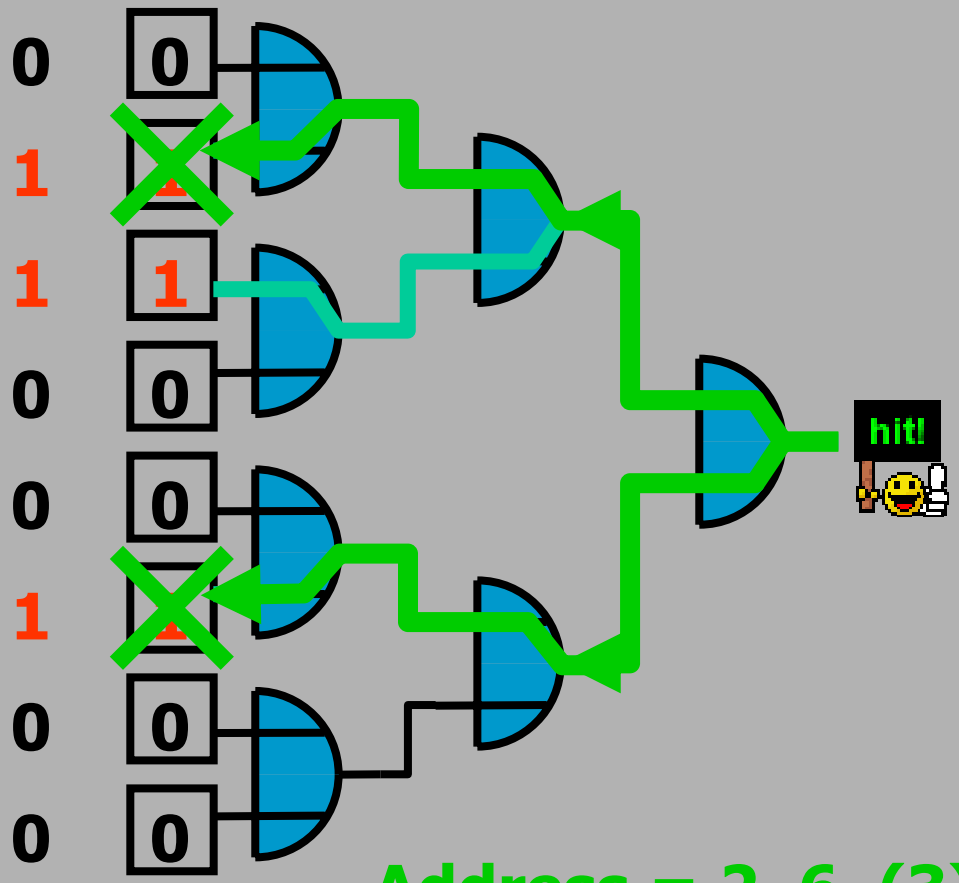
  σ ~ 35nA

  after calibration dispersion < noise



fast 0 - suppression

Hit-Finder:



Address = 2, 6, (3)

[P.Fischer]

parallel tree architecture

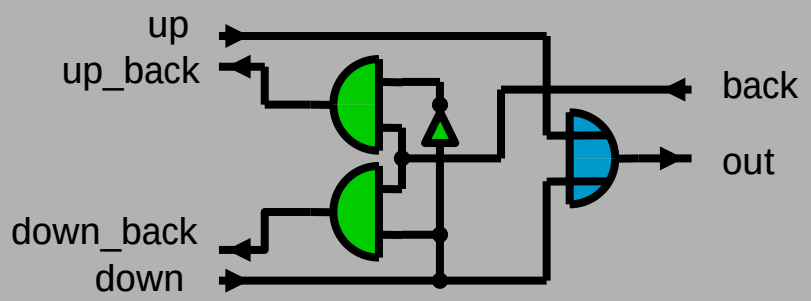
- finds up to 2 hits per clock cycle
- propagation delay:

$_2\log(\#\text{channels}) = 7$ only !

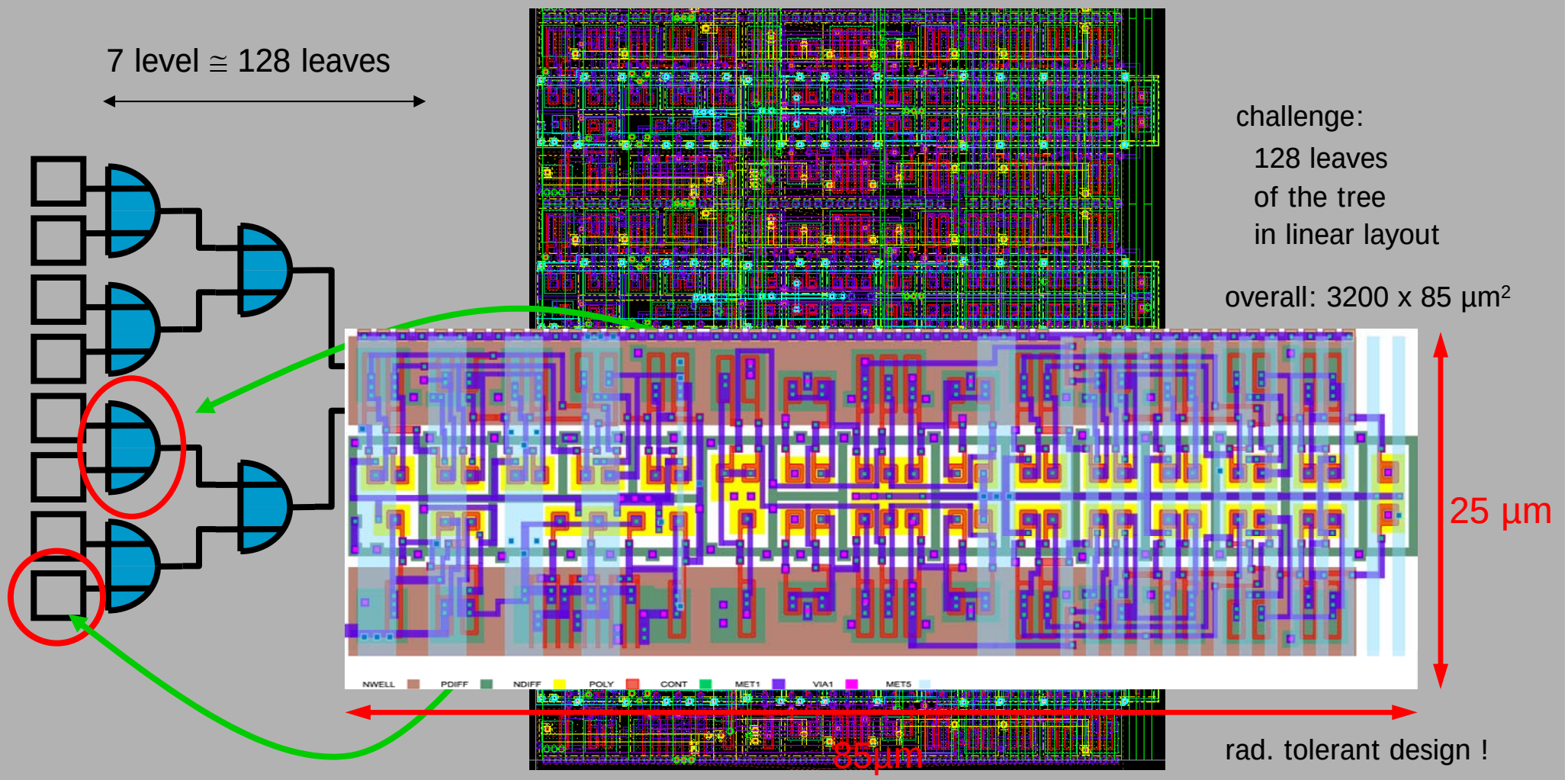
serial hit finding

- clock > 2 GHz needed
- „aggressive“ even with 0.09 µm !

leaf („lower“ part)

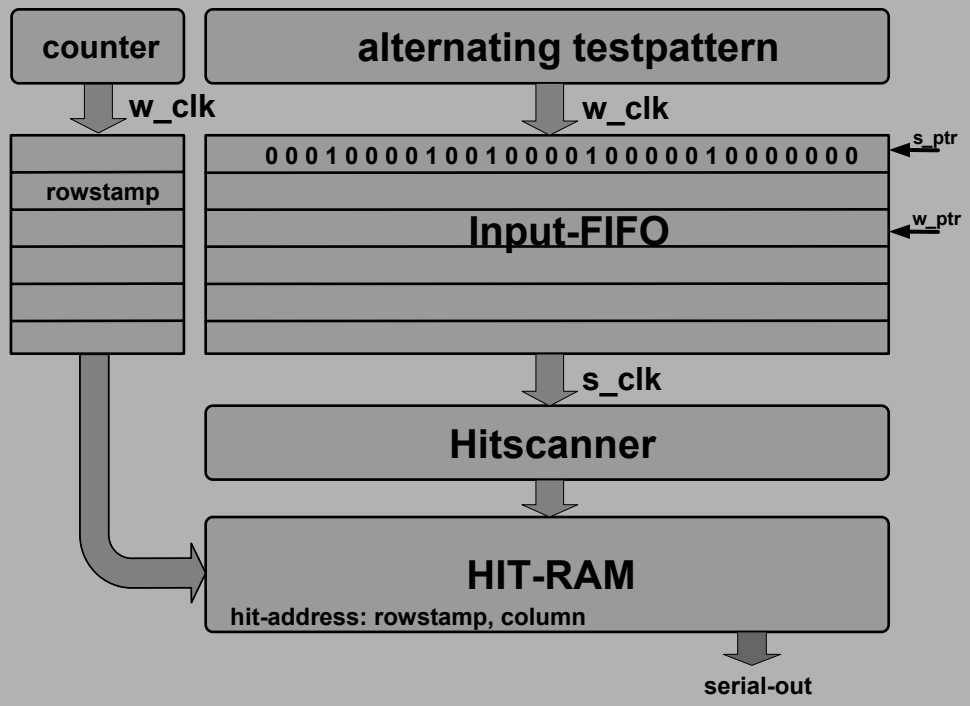


Hit-Finder: Layout



CURO II measurements (cont'd)

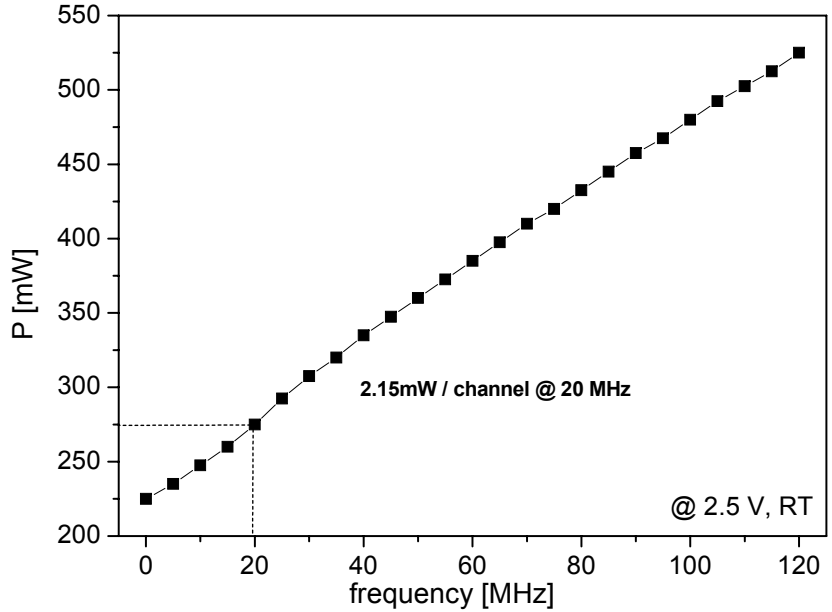
digital tests:



expected mean rate (1. layer):
1-2 hits @ 20MHz

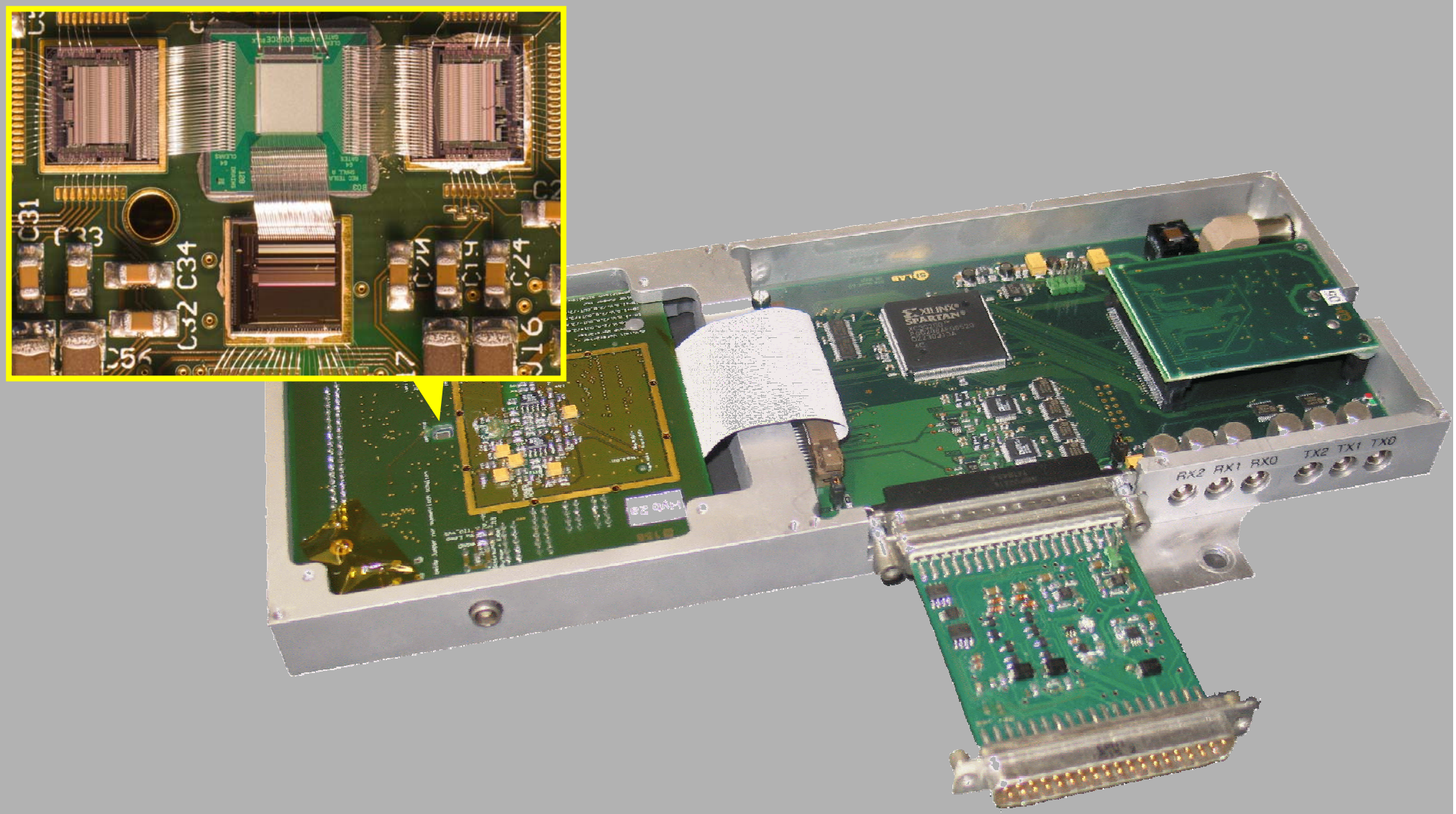
works fine up to: 110MHz

total power consumption:



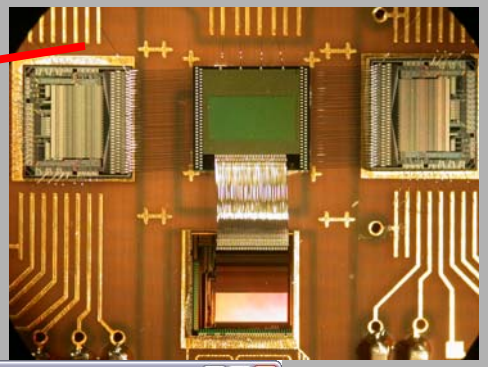
→ 250W for whole vtx-d
(continuous operation)
bunch structure 1 :199
→ **pulsed mode (1:30) ~ 10W**

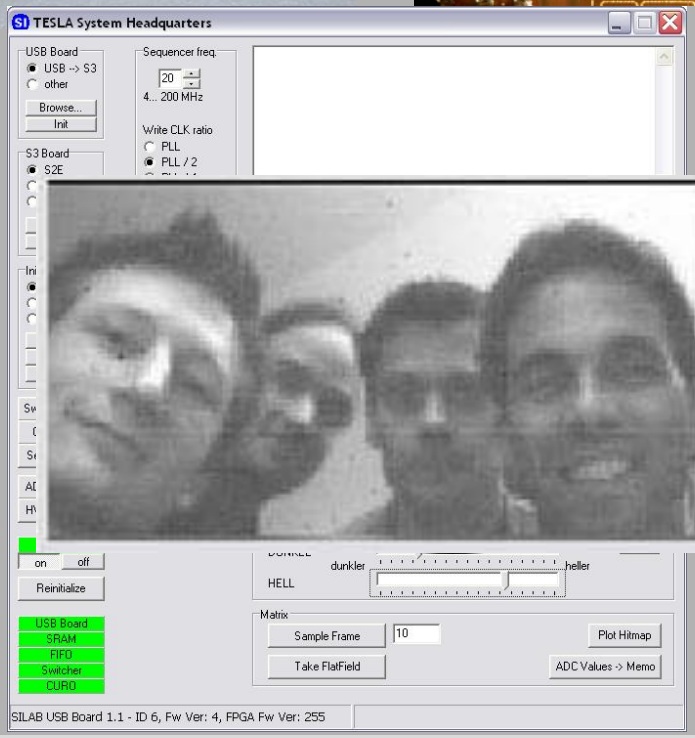
System Measurements

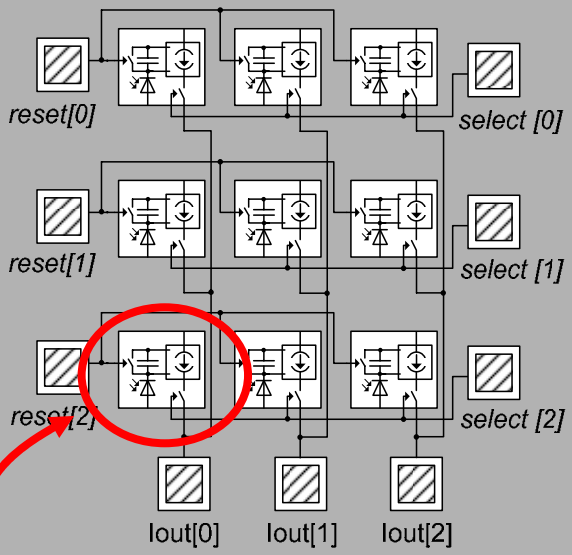


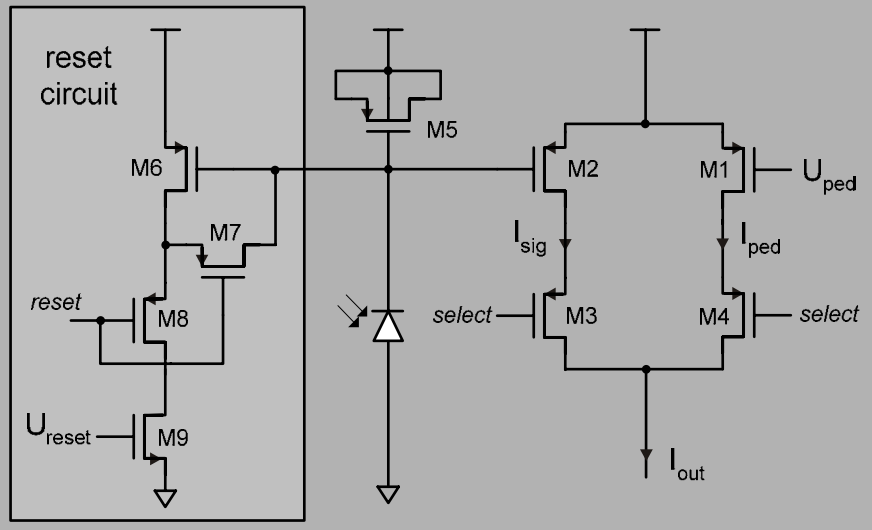
CMOS matrix

Hybrid with CMOS-Imager Matrix in AMS 0.35µm



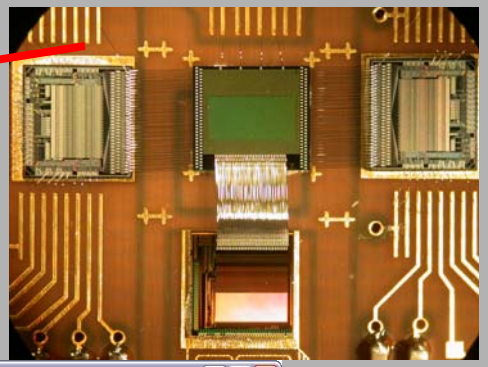


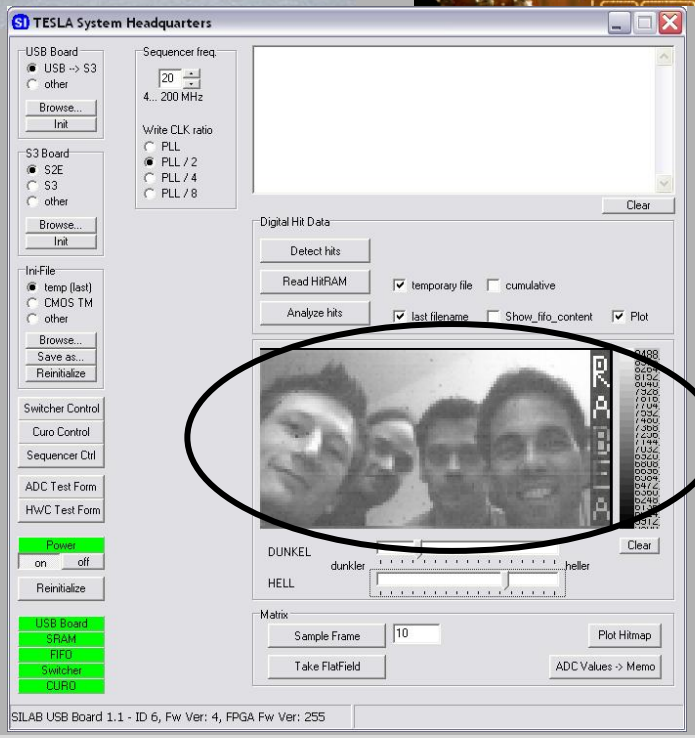




zero suppressed r/o (CMOS matrix)

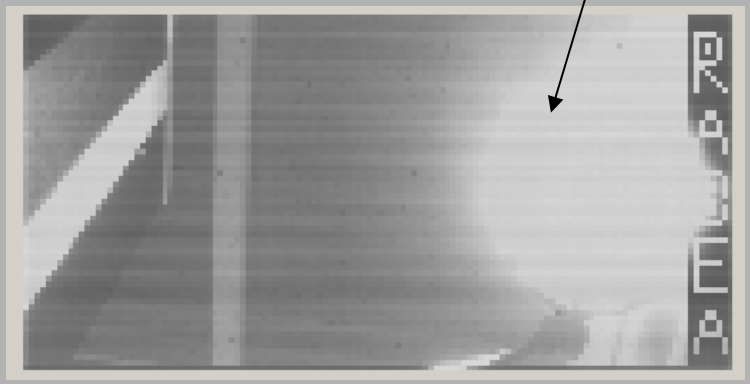
Hybrid with CMOS-Imager Matrix in AMS 0.35µm



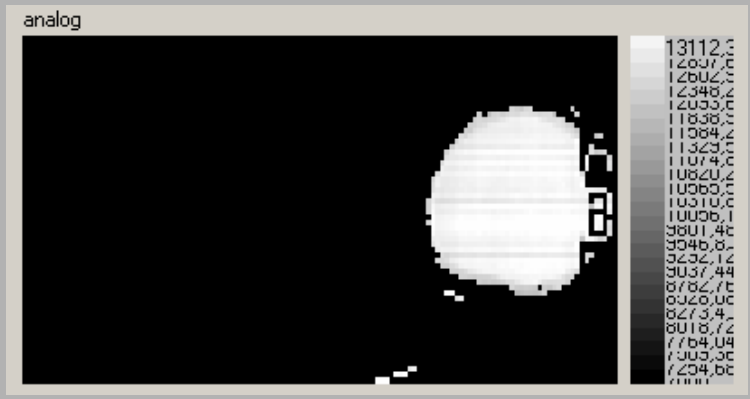


full analog frame

lightspot of a desk lamp



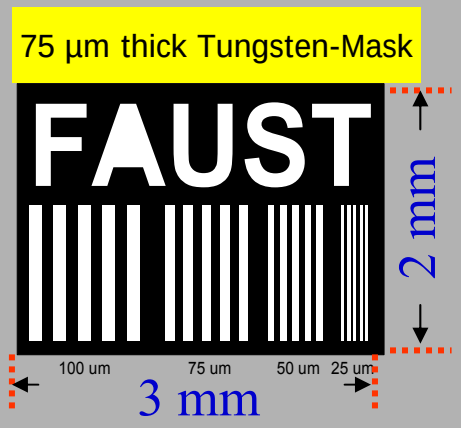
zero suppressed analog readout



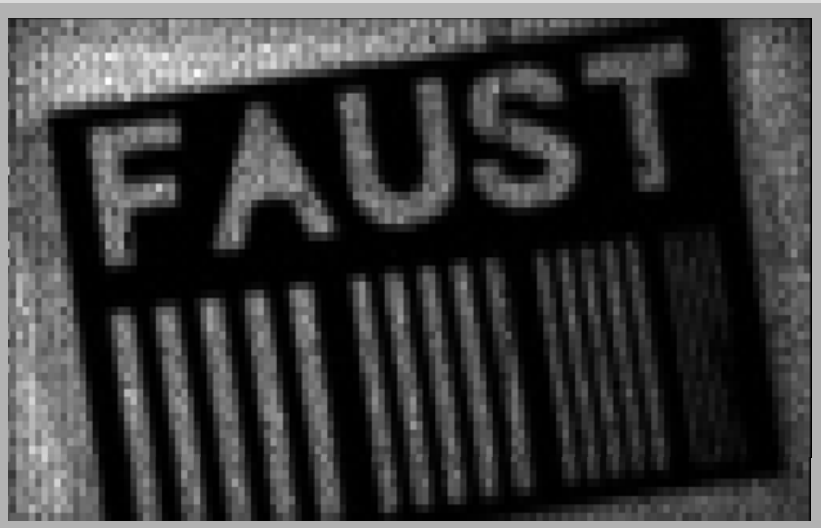
zero suppressed matrix r/o works
next CURO: neighbor logic

[R.Kohrs, Bonn]

ILC DEPFET-System in the lab

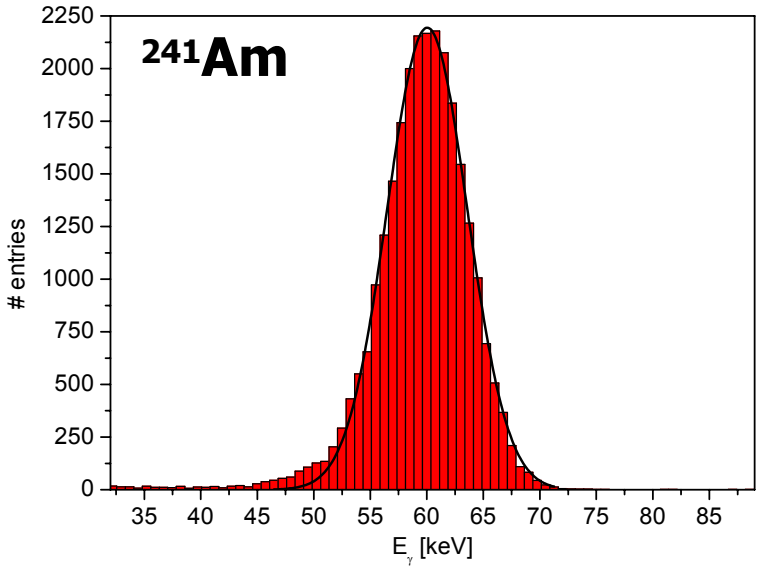


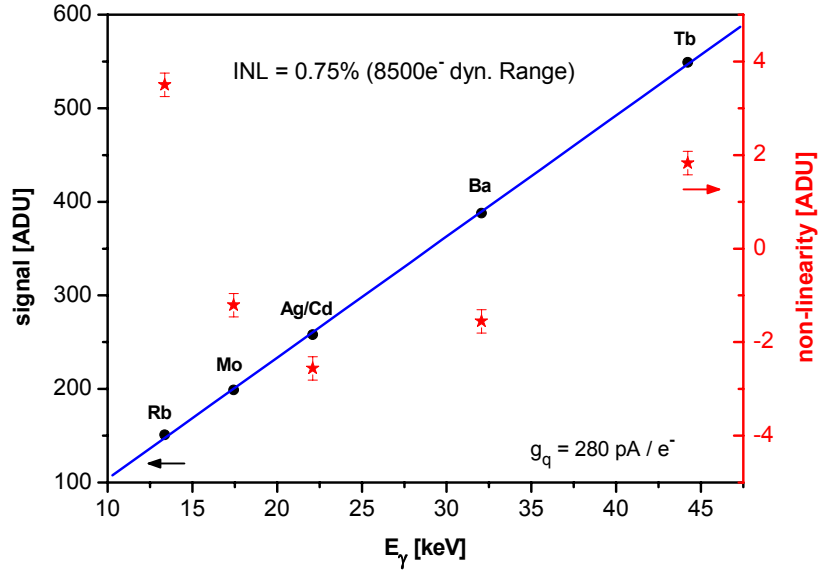
irradiation with ^{55}Fe
(6keV γ, 1700 e$^-$)



system performance:

- **speed:** line rate ~2 MHz
- **noise:** 220 e$^-$ (from noise peak)





Integral-**N**on-**L**inearity = 0.75% for 8500e$^-$

noise contributions: system

- Sensor
  - (shot noise) 8e⁻ (50µs), 45e⁻ (current r/o)
  - (1/f noise) 1.6e⁻ (after CDS)
  - (thermal noise) 26e⁻ (after CDS)
- SWITCHER (kT/C) 0.92nA 3.3e⁻
- CURO (sampling) 45nA **160e⁻**
- External transamp. 26.5nA **94e⁻**

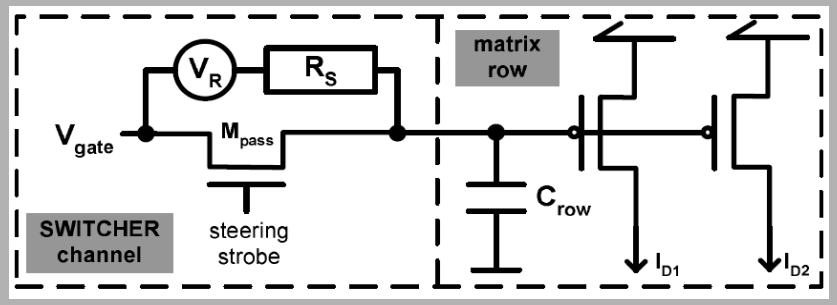
total: **~190e⁻** (measured **~220e⁻**) ...

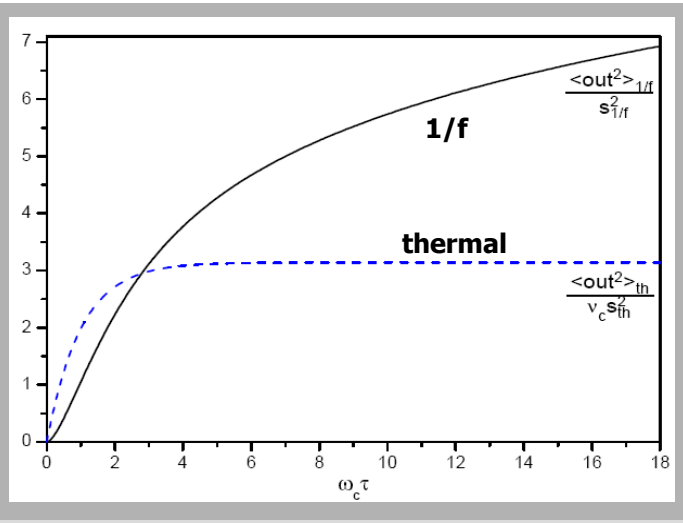
noise after CDS

$$\langle \mathrm{ENC}_{1/f}^2 \rangle = a_{1/f} \frac{g_m^2}{g_q^2} \cdot 2 \int_0^\infty \frac{1-\cos(2\pi\nu_c\tau \cdot x)}{x\,(1+x^2)}\,dx \qquad x = \nu/\nu_c$$

$$\langle \mathrm{ENC}_{th}^2 \rangle = 4kT \frac{2}{3} \frac{g_m}{g_q^2} \nu_c \pi \left(1 - e^{-2\pi\nu_c\tau}\right)$$

switching noise:



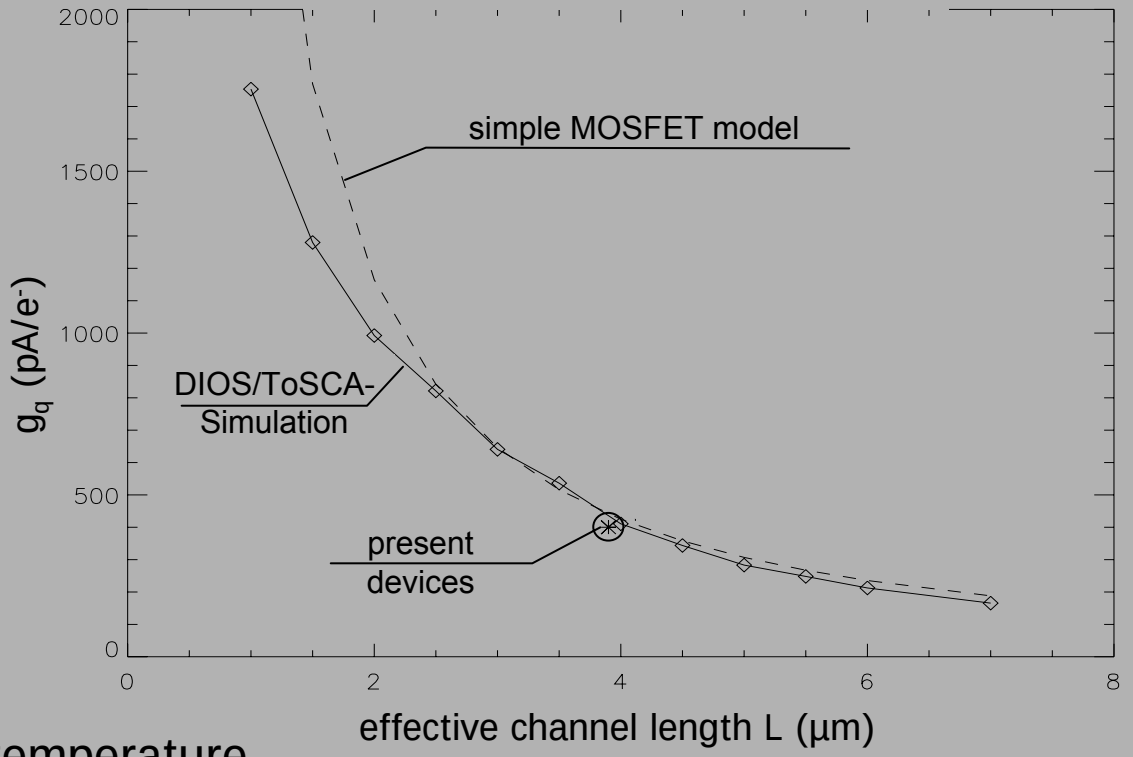


scaling potential of the DEPFET

influence of internal amplification:

$S/N \sim g_q$

(when noise is dominated by readout chain)

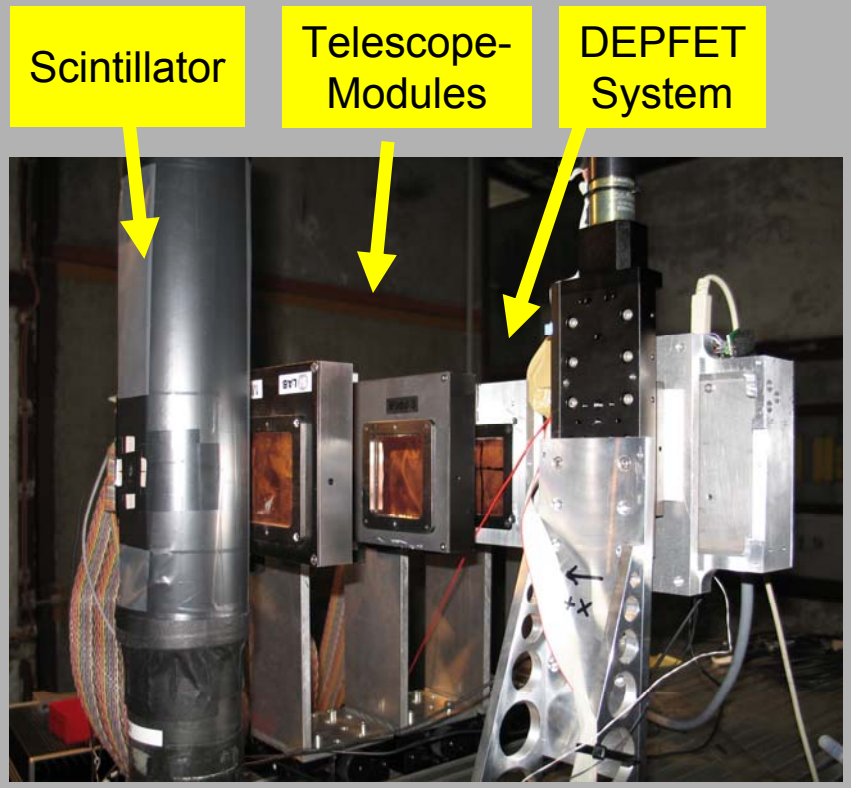


noise improvement:

- ILC operation lower than room temperature
- redesign of CURO
- new DEPFET sensors (higher g_q)

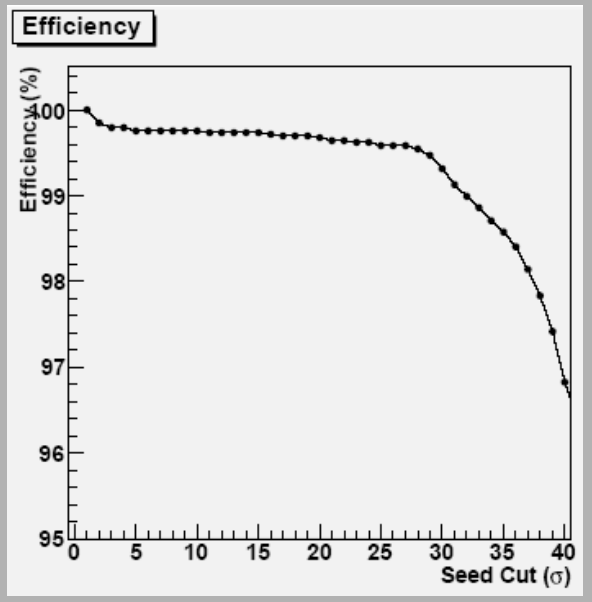
→ ENC = 100 e$^-$ achievable

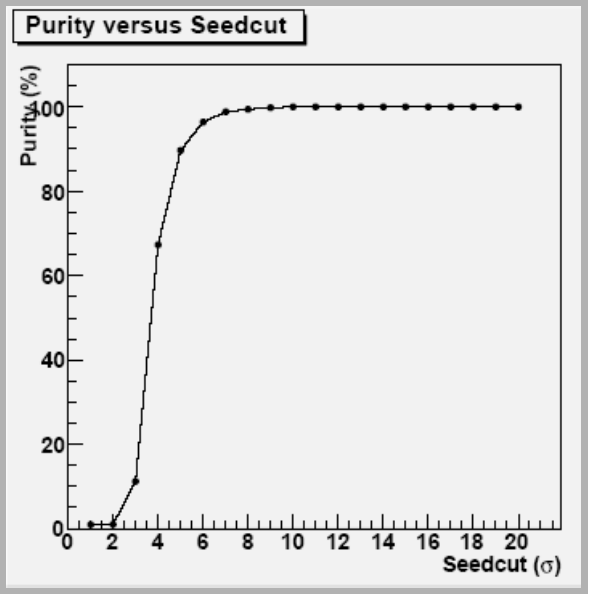
Test Beam Results

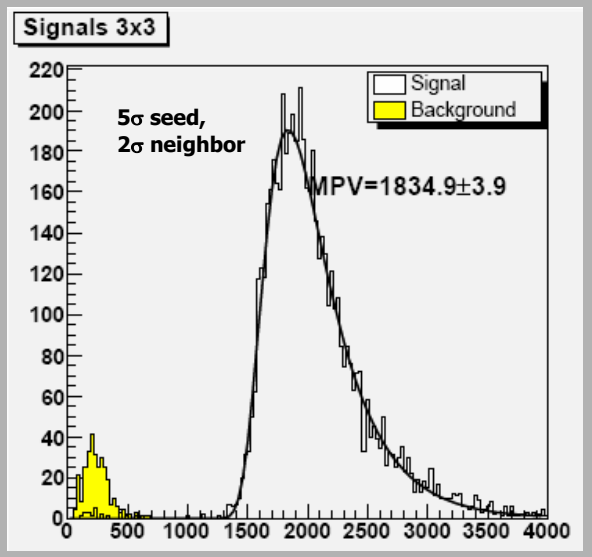


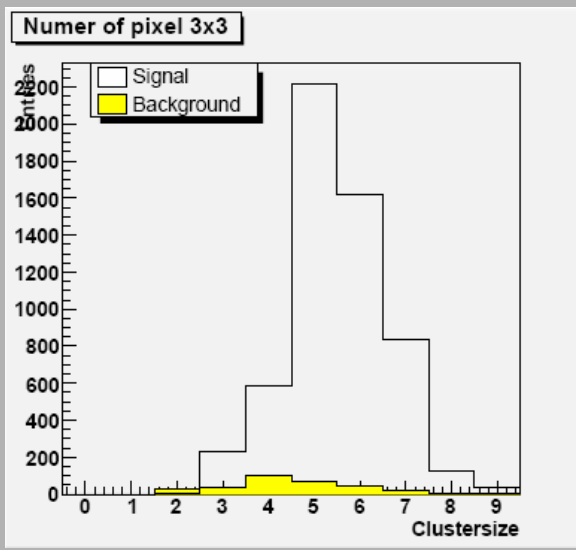
- Beam T24 @ DESY, Electrons @ 6 GeV
- Reference telescope: 4 Si-strip planes

- noise ~ 16 ADU
- **S/N ~110 (450µm sensors !)**
- position resolution:
  CERN test beam in August 2006









[J.J. Velthuis, Bonn]

summary

- **DEPFET pixel based vtx-d presented**
  - features: high S/N due to fully depleted bulk
  - present production (~30x30µm² pixels, matrices: 128x64 pixels, 450µm thick)
  - clear, radiation tolerance demonstrated, thinning concept established

- **Readout ASIC (CURO) using current mode techniques:**
  - pedestal subtraction, fast CDS, on chip hit-detection and 0-suppression

- **CURO II performance:**
  - noise: < 45nA $\rightarrow$ ~ 160 e^- (g_q=280pA/e^-) / 90e^- (g_q=500pA/e^- $\cong$ design value)
  - analog speed: 24 MHz line rate (48MSPS) , sufficient for ILC !
  - hit-identification and 0-suppression : > 100MHz , sufficient for ILC !

- **ILC-DEPFET-System:**
  - operated at ≈ 2MHz line rate, noise: 220e^-
  - 6GeV e^- test beam at DESY: S/N ~ 110 (450µm sensors)

outlook

System:

- increase system **speed** (2MHz → 20MHz !!)
- reduce **noise** (190e^- possible, next system should achieve <100e^-)
- beam test @ **CERN** -> spatial resolution and establish pixel telescope

CURO IIb:

- on-chip **common mode computation/correction** (easy with currents)
- cluster logic (keeping at least the closest neighbor)
- improve **input cascode** (readout larger matrices)
- implement (fast) **power down feature** (pulsed mode configuration)
- on chip **ADC** (IP from nordic semiconductor)

New sensors:

- 512x512 matrices, 25x25µm^2
- production of **thin DEPFETs** (longer time scale)

references

References

CURO / System: „Design of a current based readout chip and development of a DEPFET pixel prototype system for the ILC vertex detector“, PhD thesis, M.Trimpl, http://hss.ulb.uni-bonn.de/diss_online

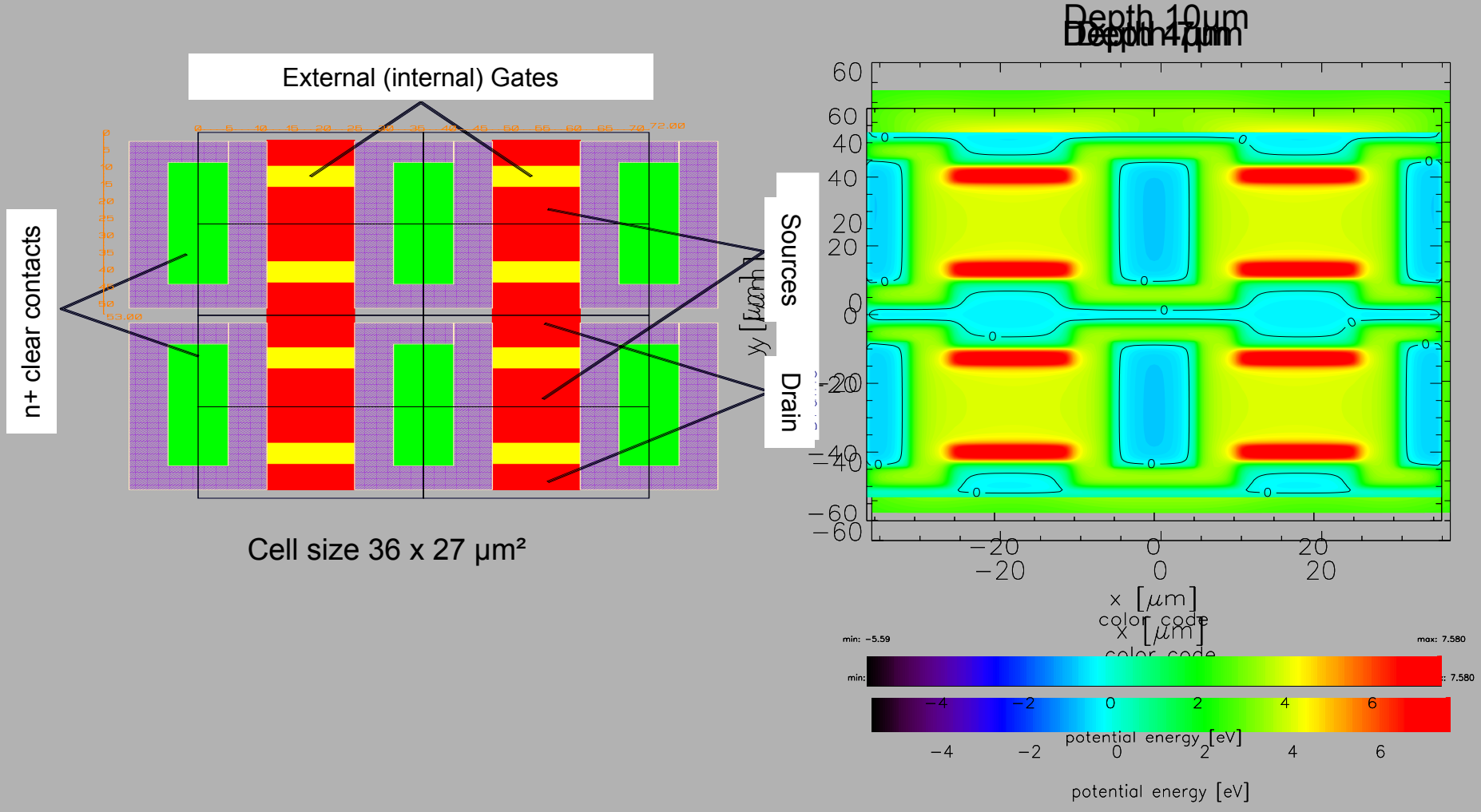
Thinning: „Processing of ultra thin silicon sensors for future linear collider experiments“, L.Andricek et al., IEEE TNS (51), No3, pp.1117-1120

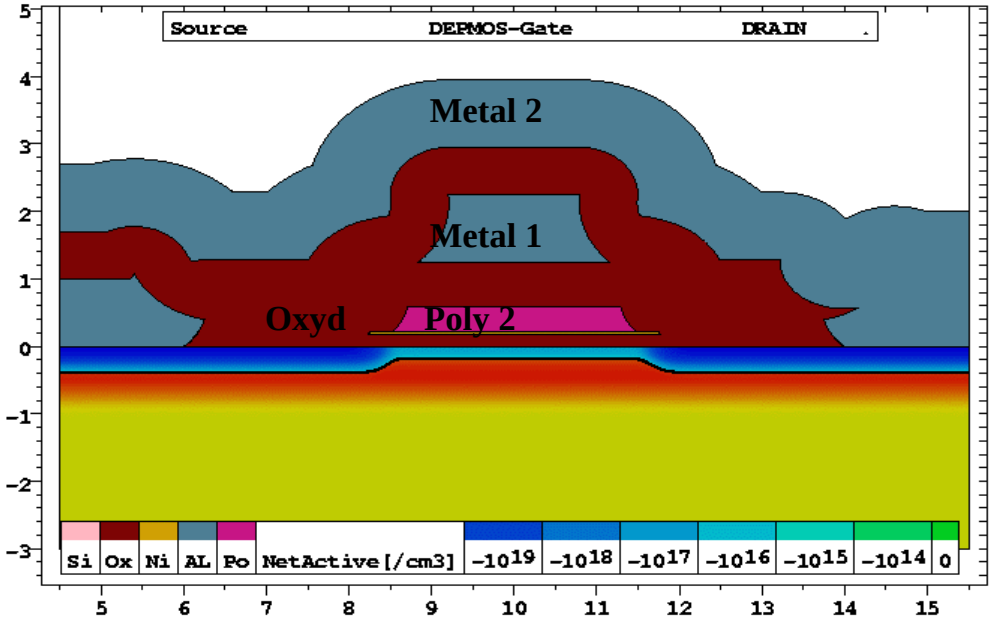
Sensor: „Design and Technology of DEPFET Pixel Sensors for Linear Collider Applicatons“, R.H.Richter, NIM A511, pp.250-256

Rad Tolerance: „The MOS-type DEPFET Pixel Sensor for the ILC Environment“, L.Andircek et al., Pixel 2005, submitted to NIM (A)

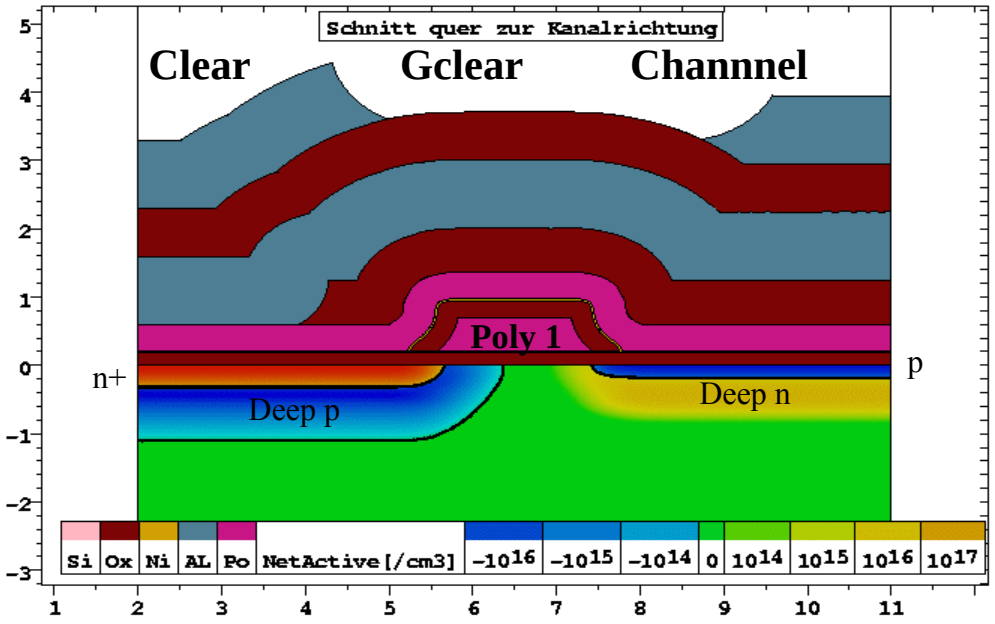
Potential during collection - 3D Poisson equation (Poseidon)

(50µm thick Si, $N_B=10^{13}cm^{-3}$, V_{Back}=-20V)

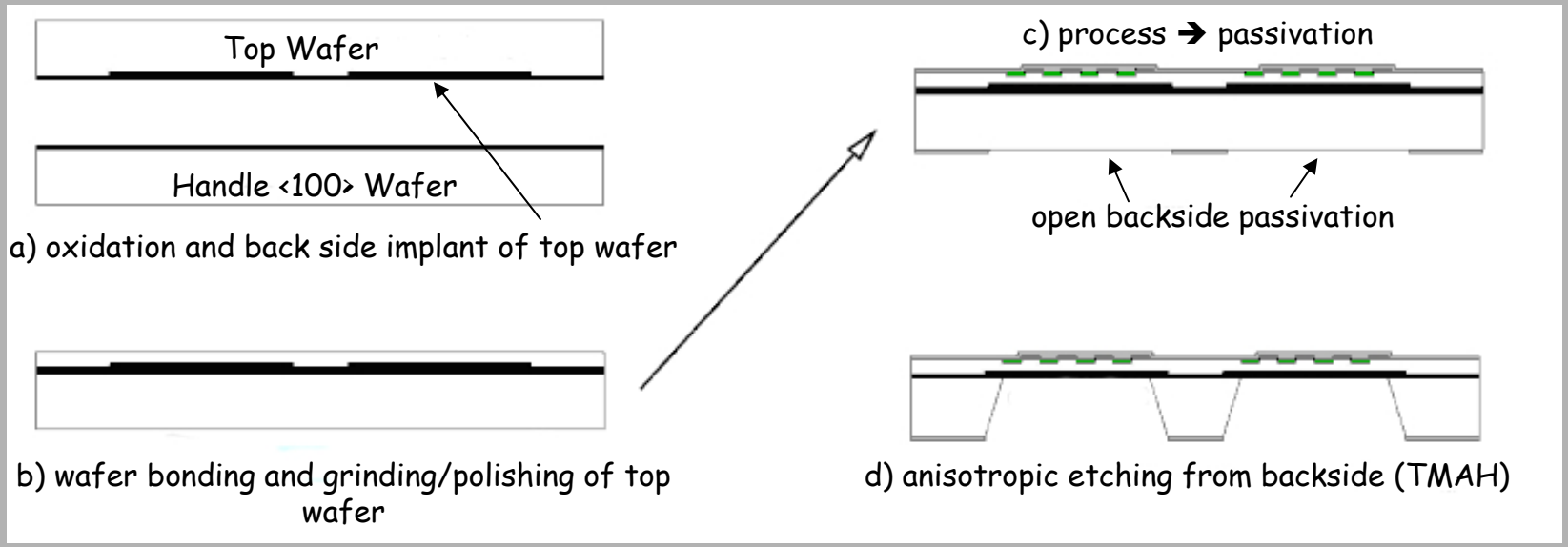




Along the channel

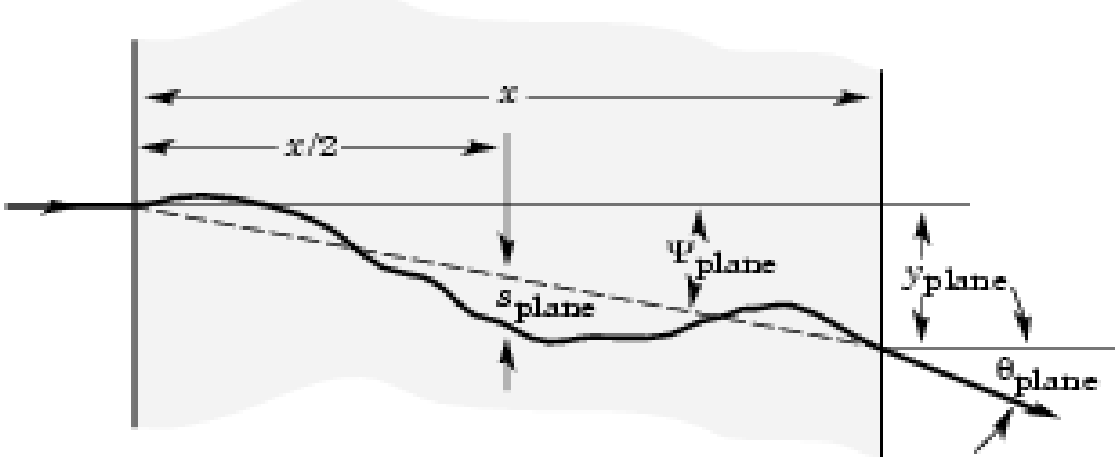


Perpendicular to the channel


Top Wafer
Handle <100> Wafer
a) oxidation and back side implant of top wafer
b) wafer bonding and grinding/polishing of top wafer
c) process ➔ passivation
open backside passivation
d) anisotropic etching from backside (TMAH)

Multiple Scattering

- During passage through matter Coulomb scattering on nuclei⇒deviation from original track

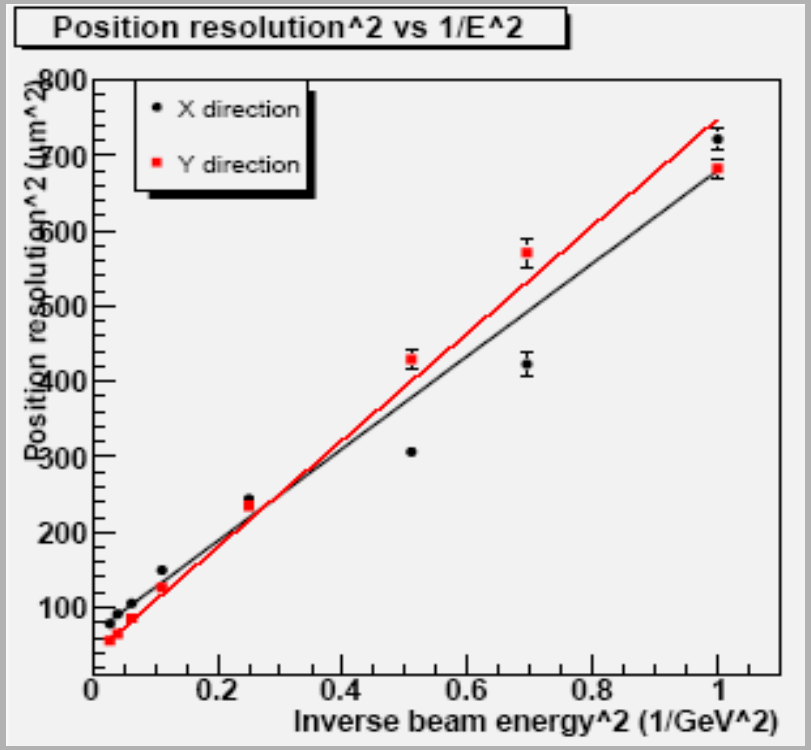


- Deflect $\theta_0 = \frac{13.6\ MeV}{\beta cp} z\sqrt{x / X_0}\left[1 + 0.038 \ln\left(x / X_0\right)\right]$

Uncertainty in predicted position

$$\sigma^2_{tot} = \sigma^2_{DEPFET} + \sigma^2_{intrinsic\ telescope} + \sigma^2_{multiple\ scattering}$$

- Remember: $\sigma_{MS}^2 \sim 1/E_{tot}^2$
- Using these scans both errors can be estimated and corrected for assuming:
  - Resolution proportional to pitch
  - Telescope performance equal in X and Y
- Note:
  - August: error MS + intr=8-9µm
  - January: error MS + intr≈6.2μm
  - (Daniel: 6.94μm)



Position resolutions

Hybrid	X_{CoG}^{corr}	Y_{CoG}^{corr}	X_{η}^{corr}	Y_{η}^{corr}
2A	6.2	3.0	5.3	3.2
1A	5.8	4.2	5.2	4.0
1B	5.8	5.1	5.5	5.1
Mun1	7.5	4.9	6.6	4.6
GCG	6.2	3.8	5.2	4.6

- Note that these values are estimated. Expected to be better. However, subtracting 6.2 or 6.9 make huge difference.
- η-distributions in Y asymmetric, magnitude depending on seed odd or even

Estimated Power Dissipation

- For V_{Drain} = 5V and I_{Drain} = 100µA (conservative values): P_{DEPFET} = 0.5mW per *active* device

- **Layer1** (8 Modules x 2 sides x 512 = 8192 pixels), duty cycle = 1/200 (idealistic case):

Sensor:	only active pixels dissipate power	⇒ 8192 x 0.5mW / 200 = **20 mW**
SWITCHER:		6.3mW per active channel at 50MHz (measured)
	⇒ 16 x 6.3mW / 200	= **0.5 mW**
CURO:	5 mW / channel (extrapolated)	⇒ 8192 x 2.8mW / 200 = **220 mW**
		Sum: ~ 240 mW

- Scaling up from 18.7 Mpixels (L1) to ~493 Mpixels for **5 layers** gives: **Total:~6.3 W**
- **Note:** Largest dissipation (CUROs) is outside active area where cooling is less problematic!
- This calculation assumes that all chips can be switched into a stand-by mode with ~zero power dissipation between bunch trains. This feature must be included in future chip versions.
- given a safety margin **total power still < 10W**