The DEPFET Active Pixel Sensor as Vertex Detector for the ILC

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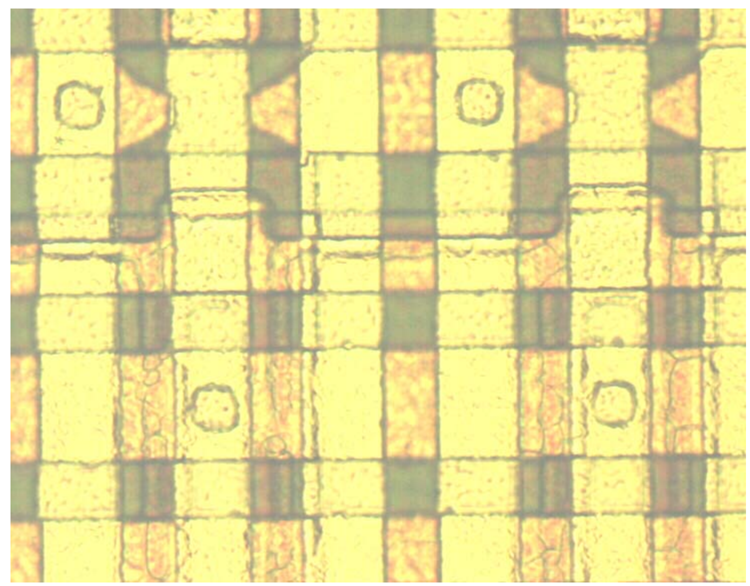
DEPFET collaboration:

Bonn, Mannheim, MPI, Aachen, Prague, Karlsruhe, Valencia, (LBNL)

- **ILC Vertex Detector**
- **MPI Semiconductor Laboratory**
- **DEPFET Principle**
- **Performance**
- **Radiation Hardness**
- **Matrix Operation**
- **Support ASICs**
- **Testbeam results**
- **Module Concept**
- **Power Consumption**
- **Simulation Studies**
- **Conclusions**



Research techniques seminar
Fermilab
June 6 2006

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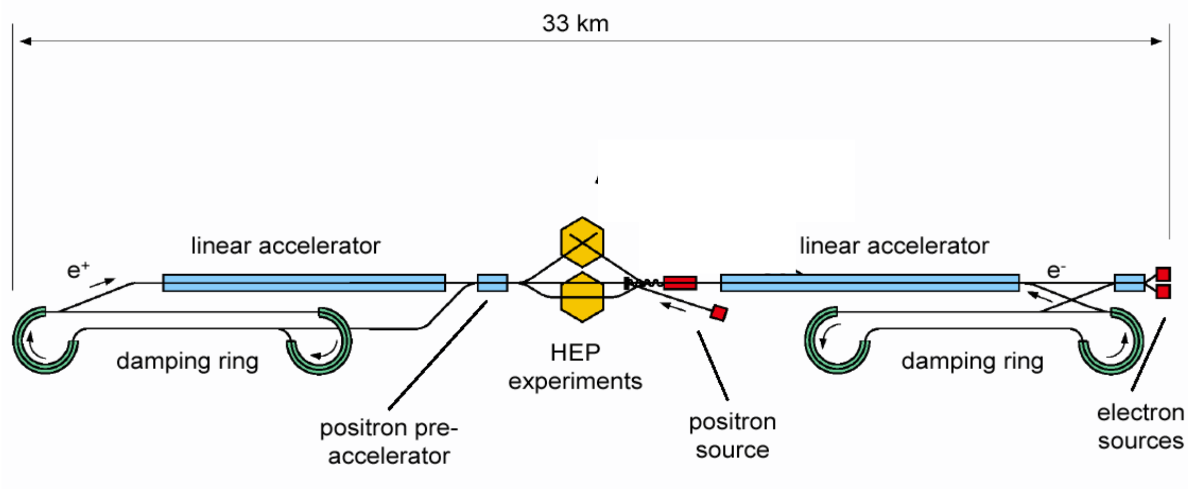
The Linear Collider Project



- 200 GeV < $\sqrt{s}$ < 500 GeV (possibility of upgrade to 1 TeV)
- Integrated luminosity ~ 500 fb^{-1} in 4 years
- Start in 2015 ?
- Needs an excellent vertex detector: b- and c- tacking, Vertex charge reconstruction
- Impact parameter resolution: 5 μm $+^2$ 10 μm/(p $\sin^{2/3}\Theta$) (p in GeV/c)
  - needs small pixels (~25 x 25 μm^2)
  - minimal scattering material: ~0.1% X_0/layer (= 100 μm silicon!)

Linear Collider Vertex Detector

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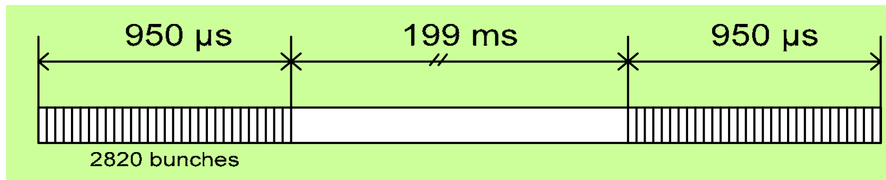
ILC time structure:

2820 bunches spaced by 337 ns
199 ms between trains (1/200 duty cycle)



Background (Beamstrahlung):

140,000 e+e- pairs/BX

0.03 hits/mm^2/BX (at R=15mm, B=4T)

Bunch train: (x 2820) => 85 hits/mm^2/BT

At least 20 readout cycles/BT to keep occupancy low

Need 50 MHz line rate for pixel matrix readout

Radiation: 100krad in 5 years (at 15 mm radius)

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Three Detector Concepts

SiD

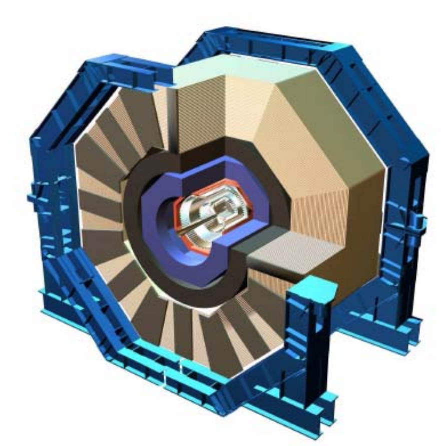
-: small radius, high B field
-: few track meas. points
with high res. (Si)
-: Si-W Calorimetry
-: VTX: r_{min}=1.4 cm

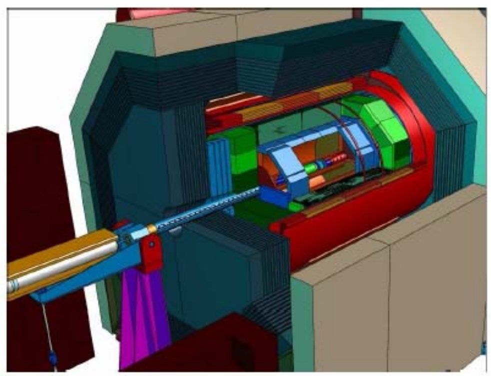
LDC

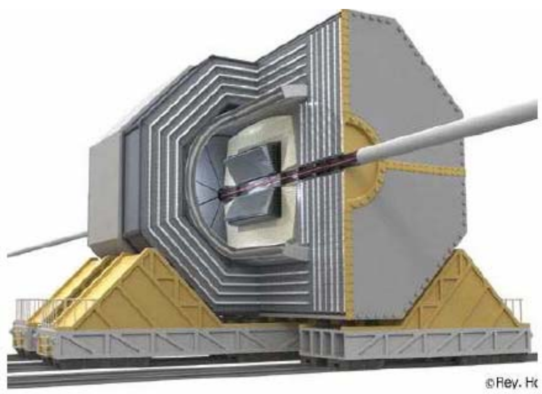
-: med. radius, med. B field
-: many track meas. points
with med. res. (TPC)
-: Si-W Calorimetry
-: VTX: r_{min}=1.5 cm

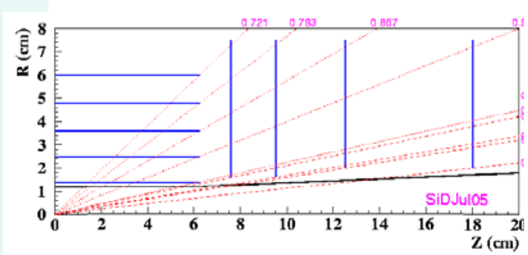
GLD

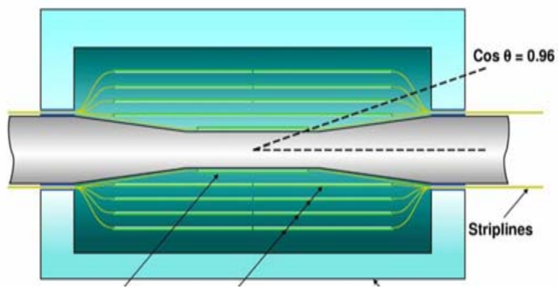
-: large radius, low B field
-: many track meas. points
with med. res. (TPC)
-: Sci.-W Calorimetry
-: VTX: r_{min}=1.7 cm

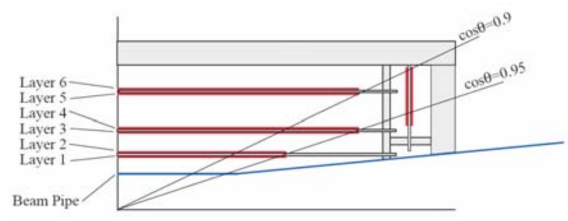












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Pixel Vertex Detector at the ILC

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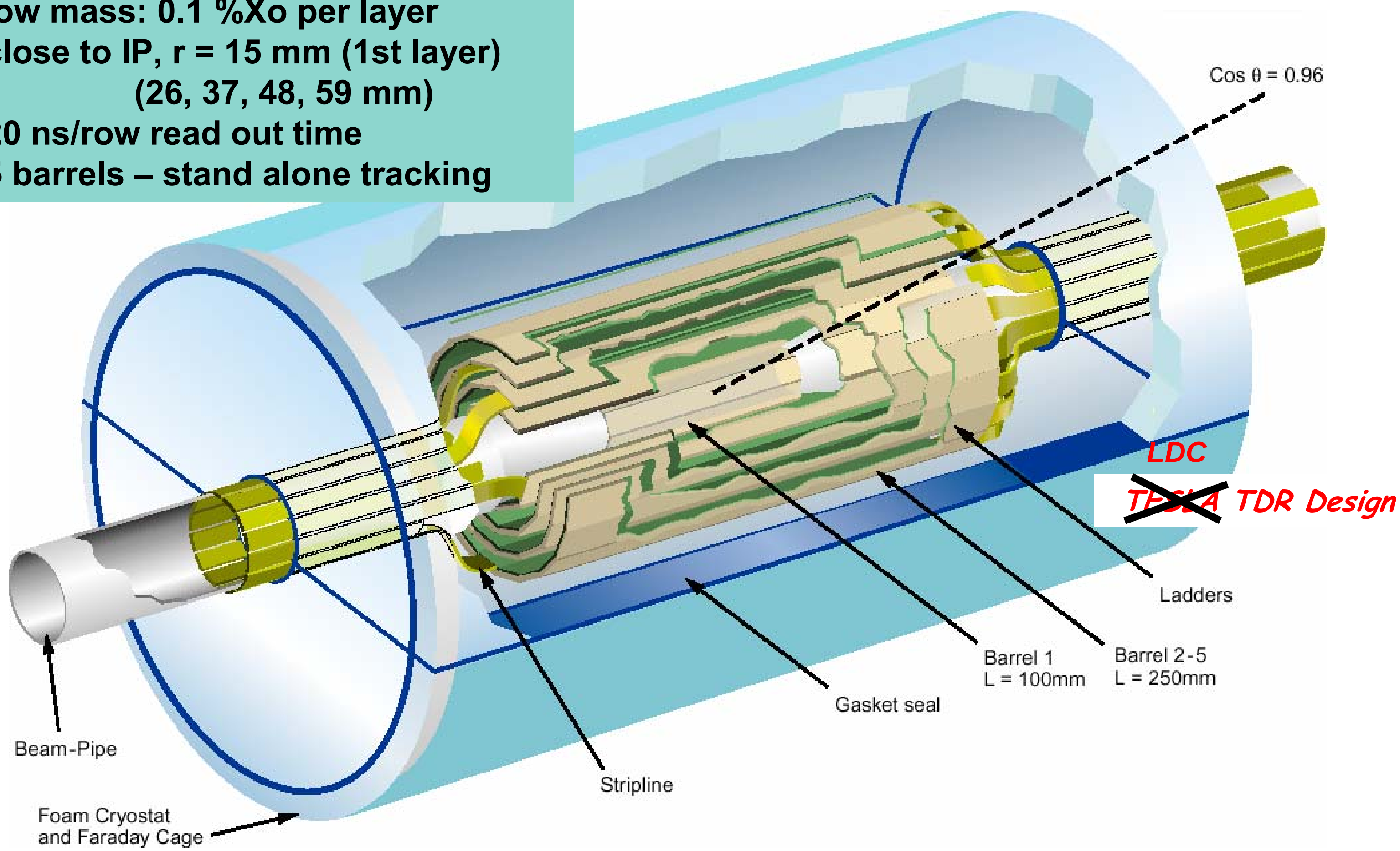
- pixel size: 20-30 µm
- low mass: 0.1 %Xo per layer
- close to IP, r = 15 mm (1st layer)
  (26, 37, 48, 59 mm)
- 20 ns/row read out time
- 5 barrels – stand alone tracking



1st layer module: 100x13 mm², 2nd-5th layer : 125x22 mm² → Σ120 modules

Several Sensor Concepts: CCDs, MAPs, SOI, DEPFETs

MPI Semiconductor Laboratory (Halbleiterlabor: HLL)

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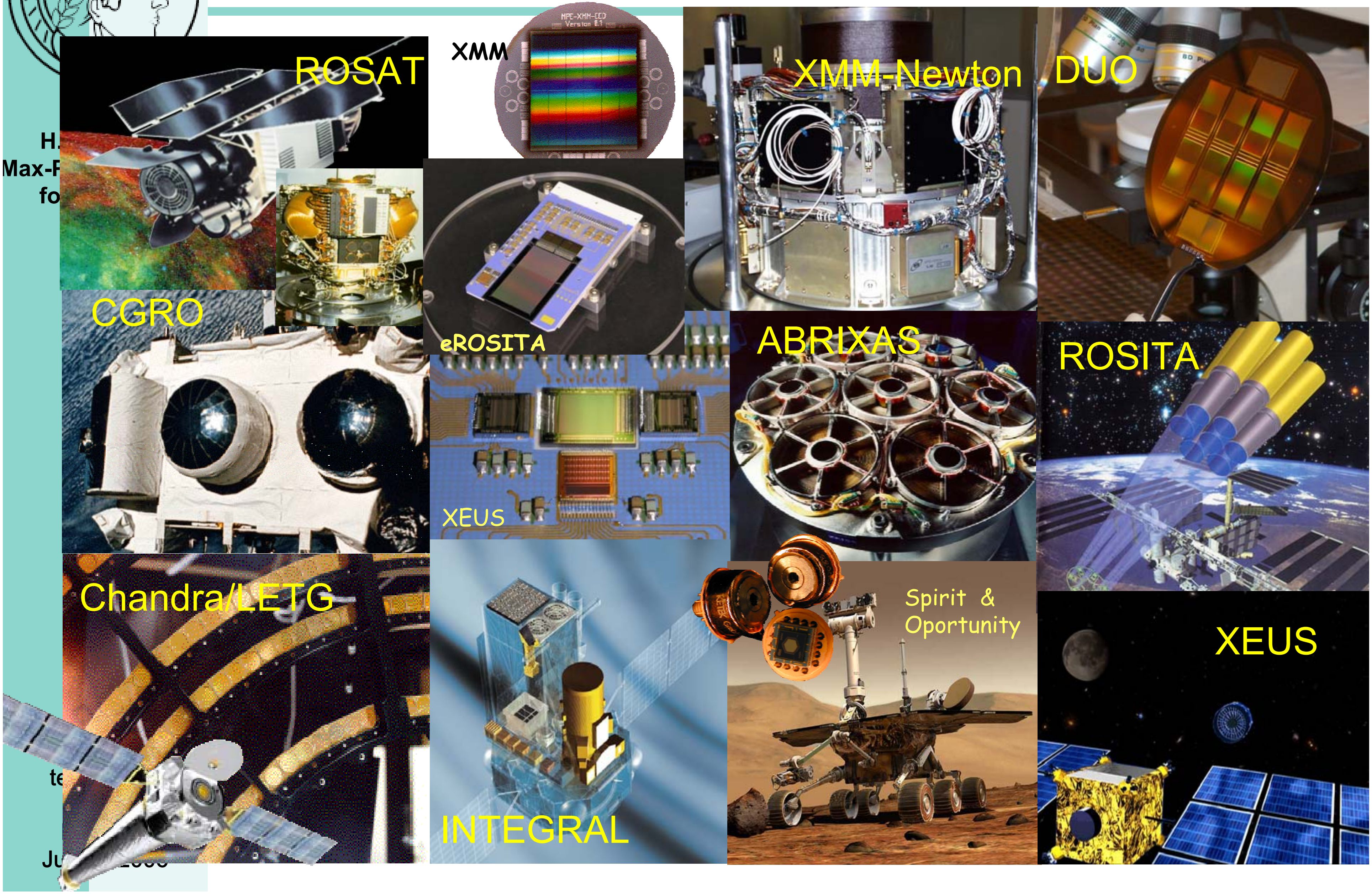
Common project of the:

Max-Planck-Institut fuer Physik (Werner Heisenberg Institut), Munich

Max-Planck-Institut fuer extraterrestrische Physik, Garching

Founded in 1992, since 2000 located in the Siemens plant in Neu-Perlach, Munich

Scientific activities of the MPE



MPI für Physik Projects
(Werner-Heisenberg-Institut für Physik)

H.
Max-P
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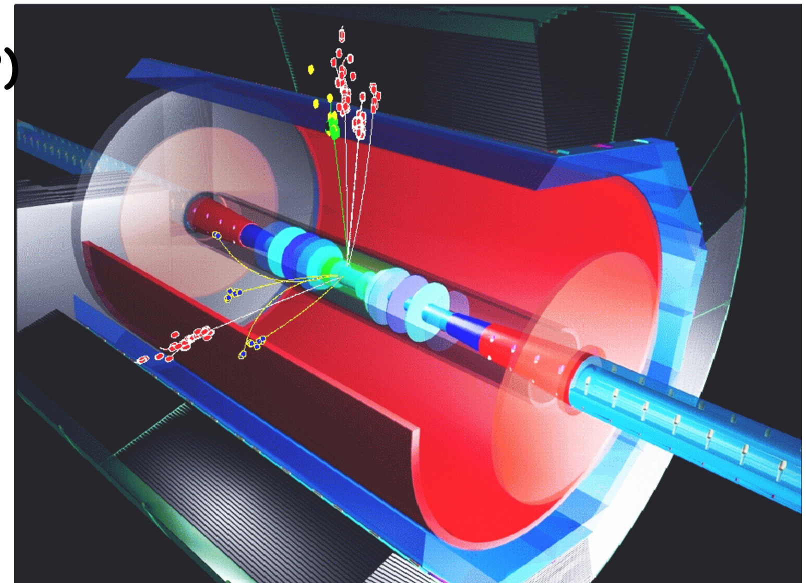
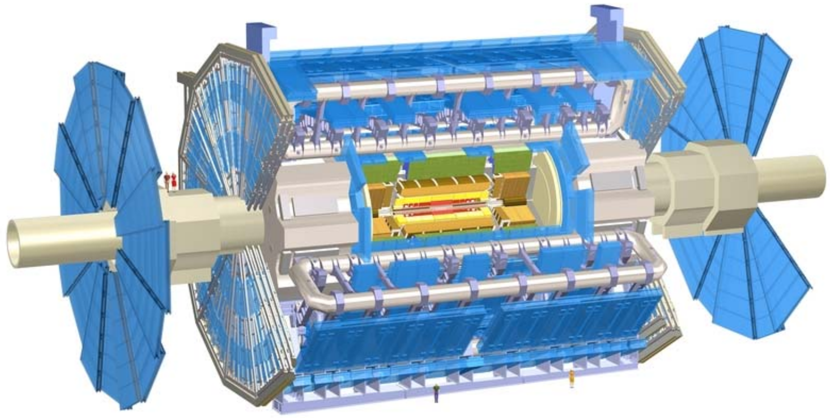
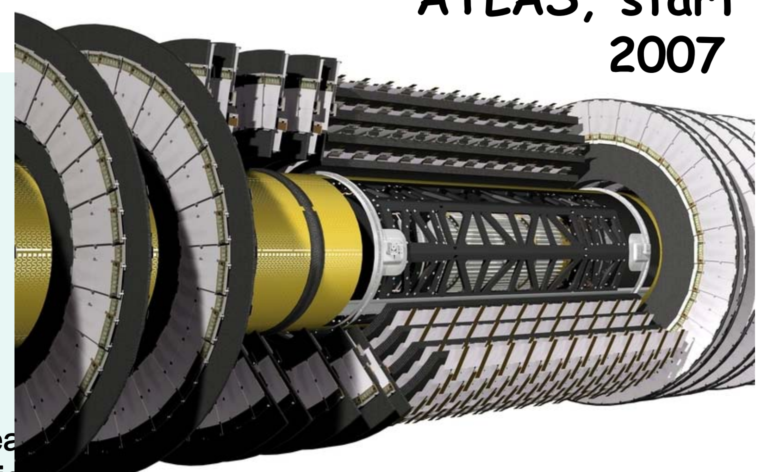
ILC, start in 2016 (?)





ATLAS, start in 2007



MAGIC, operational todate

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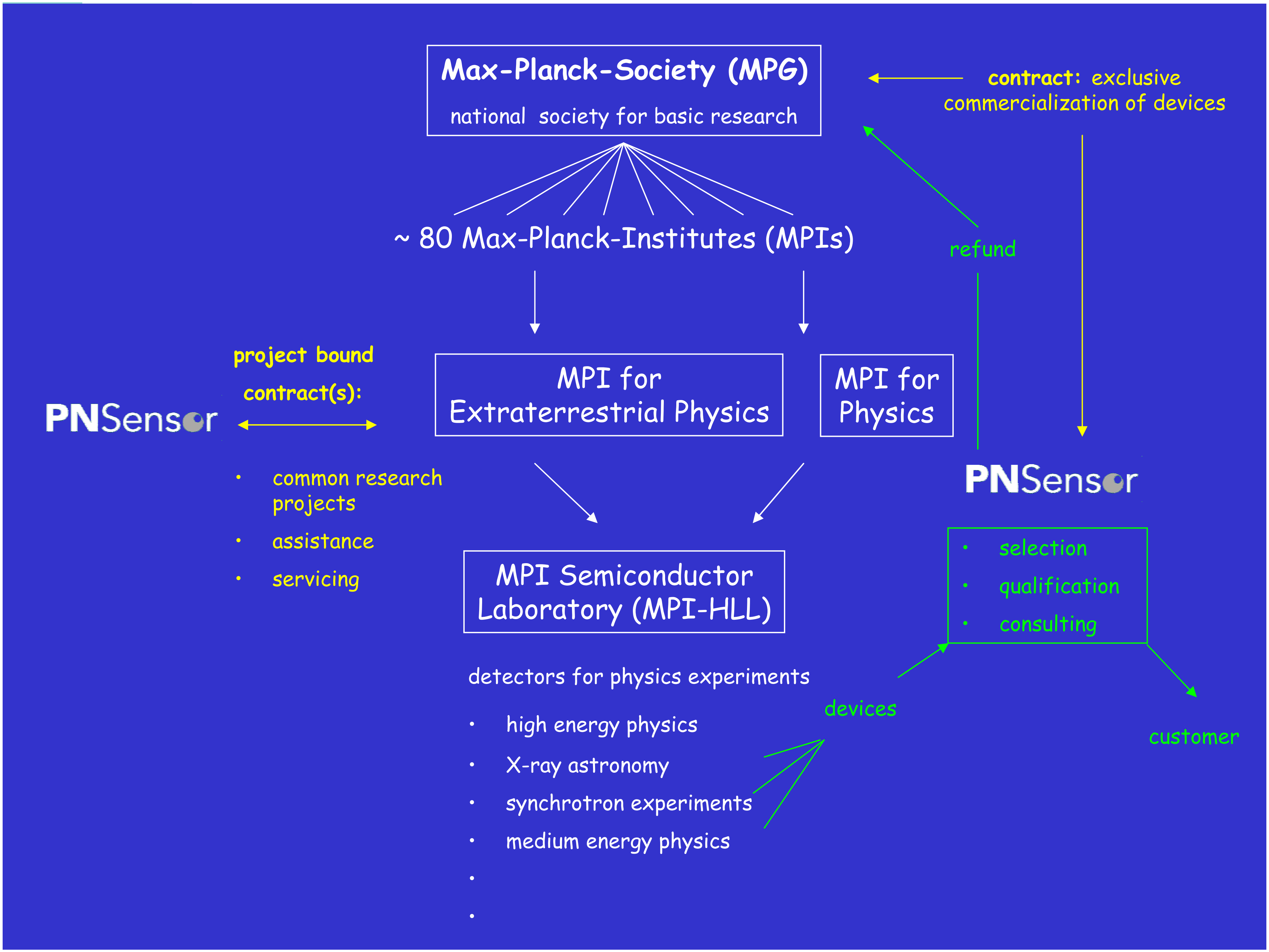
Max-Planck-Society (MPG)
national society for basic research
contract: exclusive commercialization of devices
~ 80 Max-Planck-Institutes (MPIs)
refund
project bound contract(s):
PNSensor
MPI for Extraterrestrial Physics
MPI for Physics
common research projects
assistance
servicing
PNSensor
selection
qualification
consulting
MPI Semiconductor Laboratory (MPI-HLL)
detectors for physics experiments
high energy physics
X-ray astronomy
synchrotron experiments
medium energy physics
devices
customer

Complete Design and Manufacturing Chain

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- Facilities for Layout and Simulation of Semiconductor Devices
- Production of Silicon Detectors
- Mounting and Tests

- Special Features:

- Processing of ultra-pure silicon wafers (10^{12} impurites/cm^3)
- Double sided wafer processing
- Wafer scale detectors (up to 50 cm^2 area)

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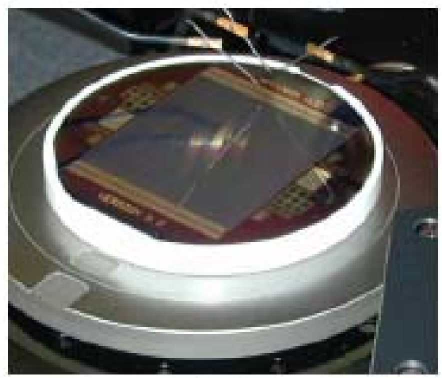
HLL Facilities

800 m^2 cleanroom up to class 1 ...

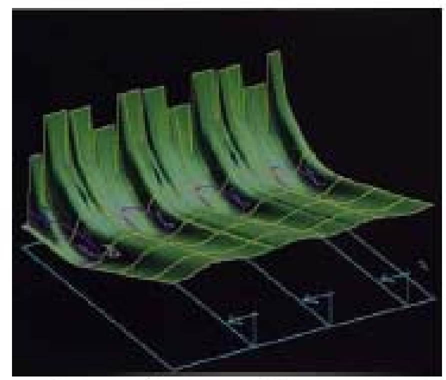
... with modern, custom made equipment ...

... for a full 6" silicon process line

mounting & bonding

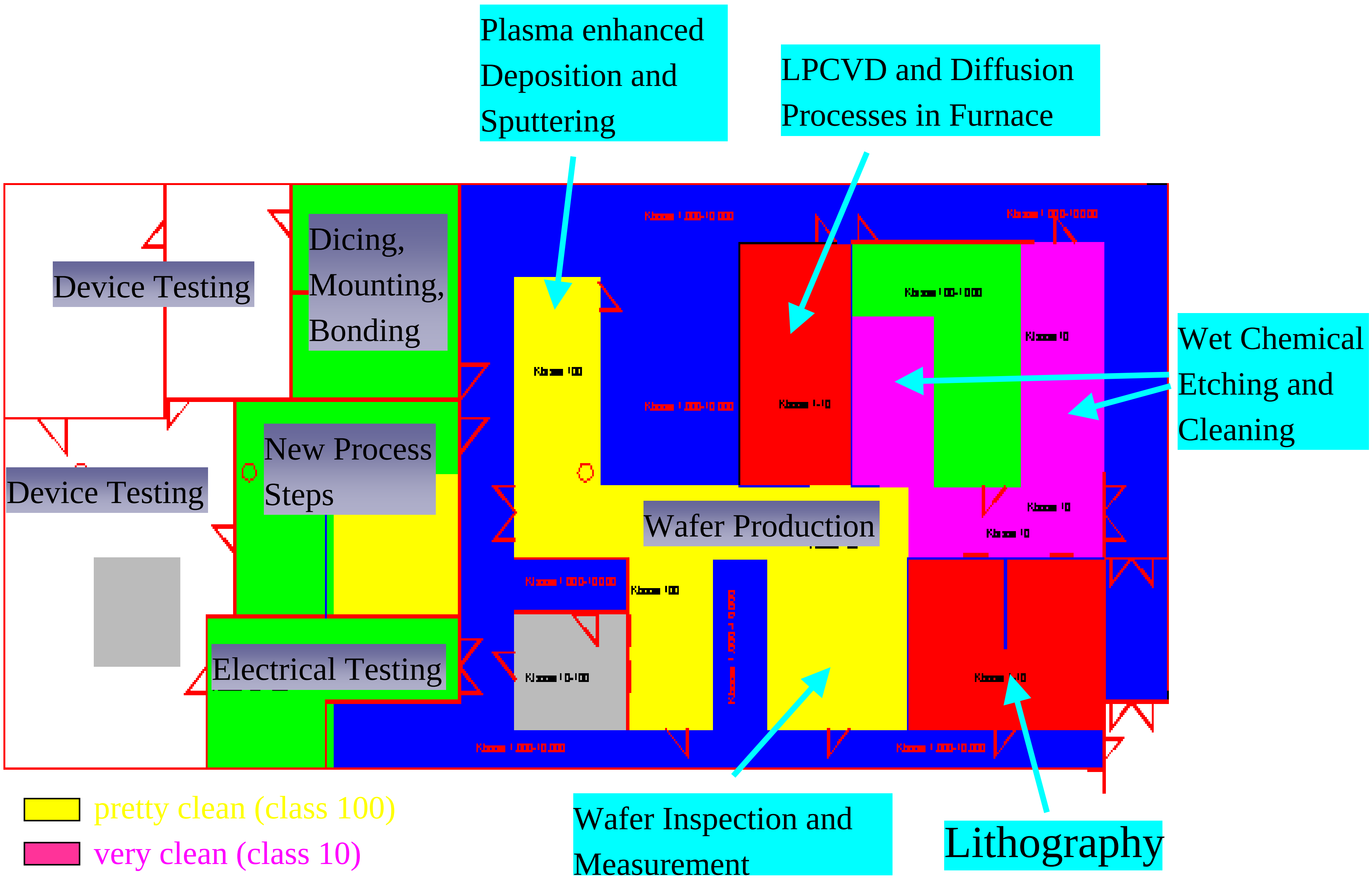


test & qualification



simulation, layout & data analysis

Inside the HLL



- pretty clean (class 100)
- very clean (class 10)
- as clean as you get (class 1)
- medium clean (class 1.000 – 10.000)

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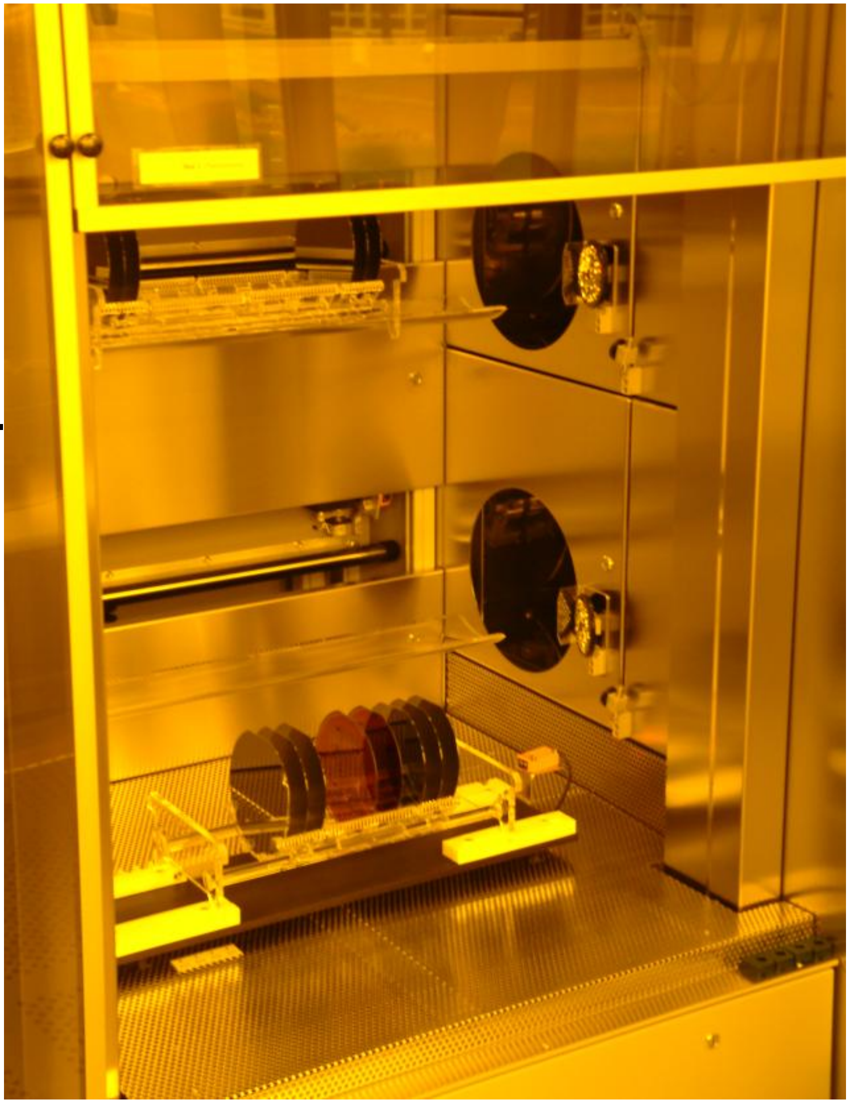
Oxidation

During „thermal oxidation“, the wafer surface ist transformed from Si to SiO_2.

Oxidation takes place in a furnace @ 1050 °C in a pure O_2 athmosphere.

• The highest temperature of all process steps
• SiO_2 provides passivation for further steps

=> the most important step for final leakage current level.



Lithography

Wafers are covered with photoresist, exposed to UV-light and developed.

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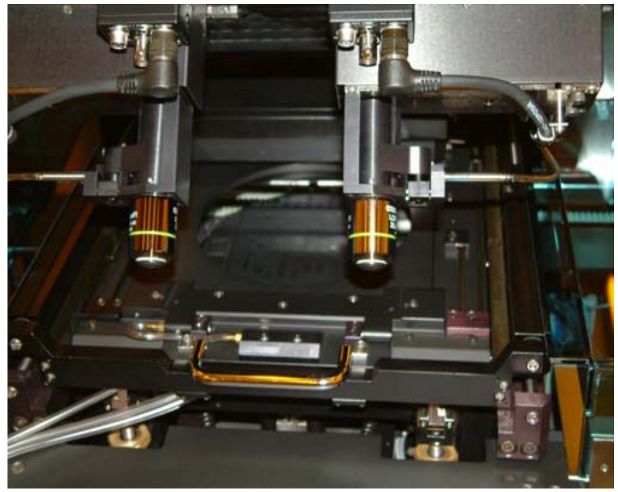
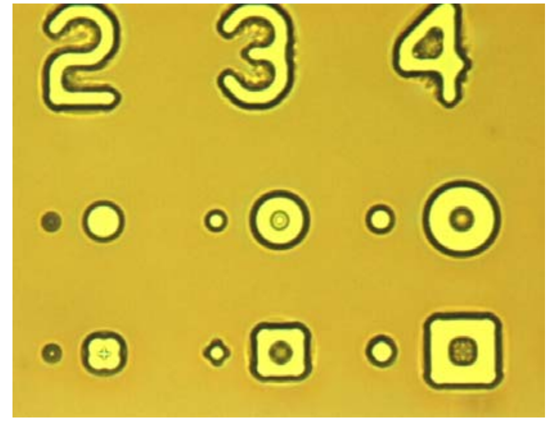
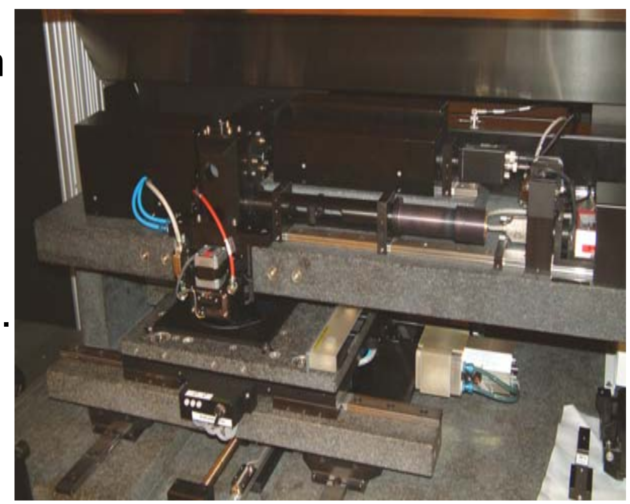
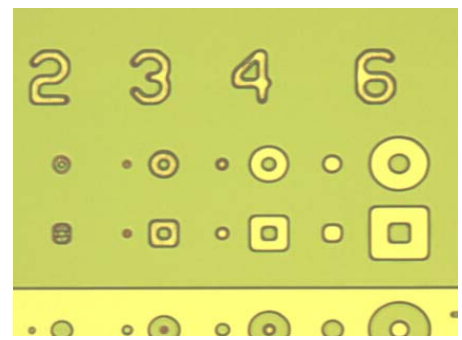
Projection of wafer **mask** in proximity distance (15ym). Minimum feature size (3µm) is set by diffraction effects.

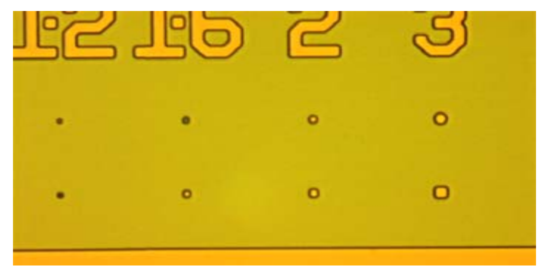




Direct writing of design data:
A focused UV laser beam is scanned with acusto-optic modulators. Minimum feature size (1,5µm) given by spot diameter.







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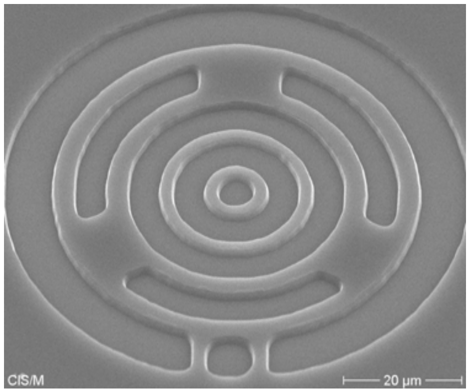
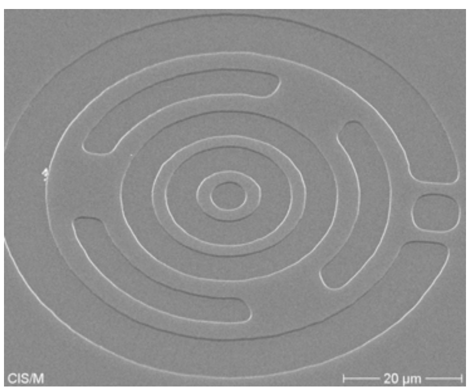
Structuring of deposited layers

Transfer of lithographic pattern

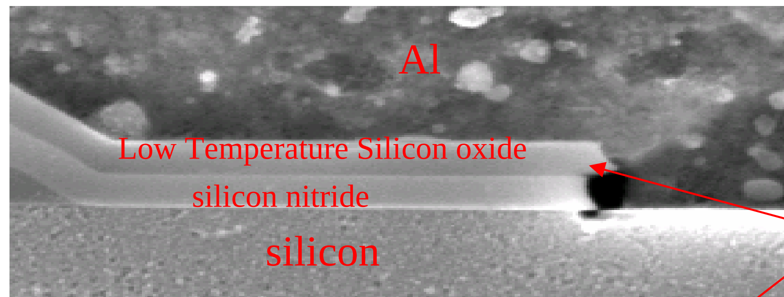


developed photoresist on top of Oxide

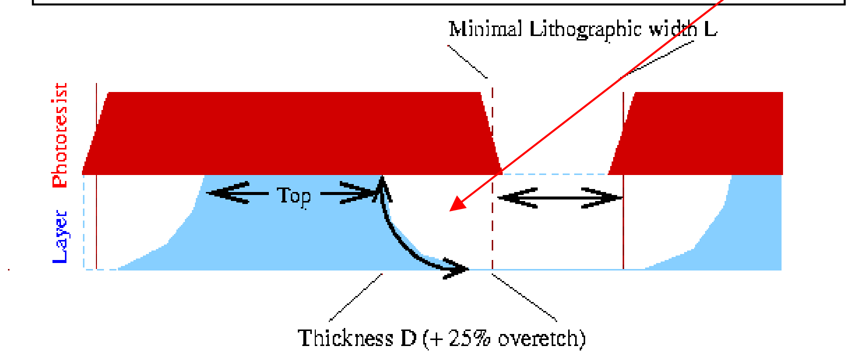


Oxide etched, photoresist removed

Wet chemical etching (opposite to plasma etching) avoids radiation damage, but:
=> Isotropic etching sets a limit for small structures



Structuring of silicon nitride with LTO layer as mask



Minimum pitch = Top+2,5 D+L

Deposition of additional layers

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Deposition of :

- Silicon oxide (LTO) (from SiH_4+O_2 @ 400 °C)

-**Silicon nitride** (from SiH_2Cl_2+NH_3 @ 730 °C)

- insulation layers

by Low Pressure Chemical Vapor Deposition

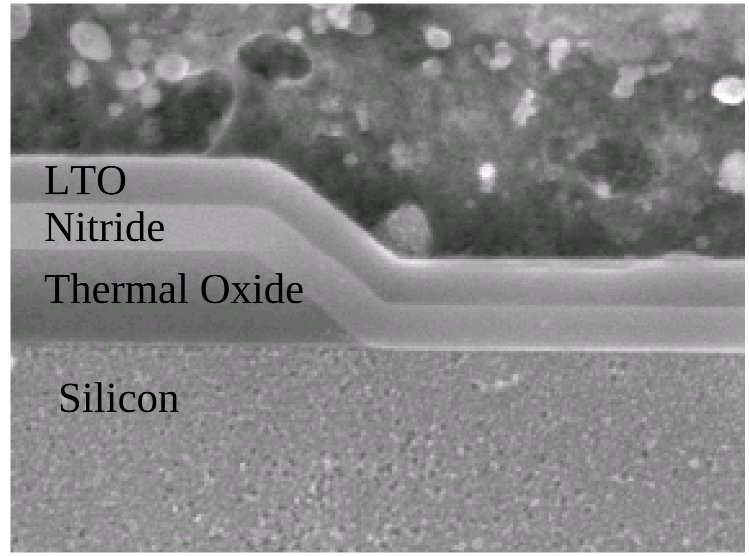
Polysilicon deposited by LPCVD (SiH_4 @ 570°C)

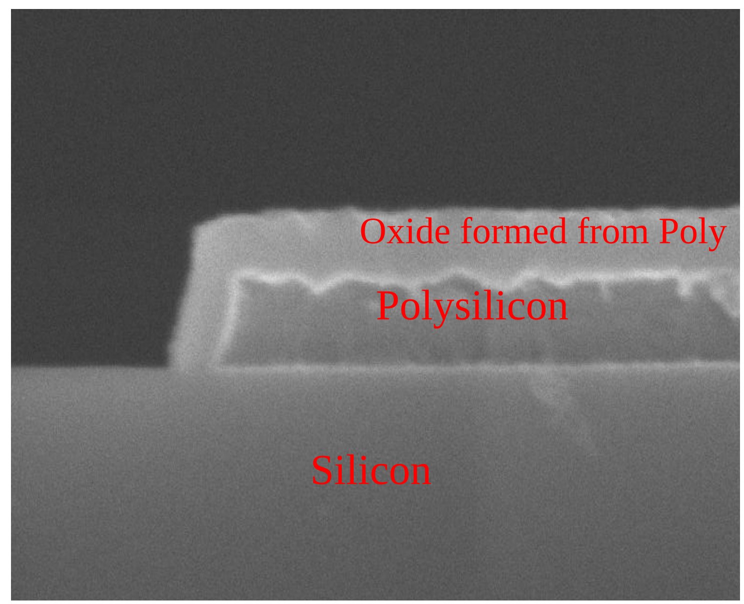
-conductivite (after Ion implant)

-structured polysilicon can be oxidised and forms a dense **self-aligned insulation** layer.

Aluminium deposited by plasma sputtering off a high purity target.

Double poly and double metal processes available





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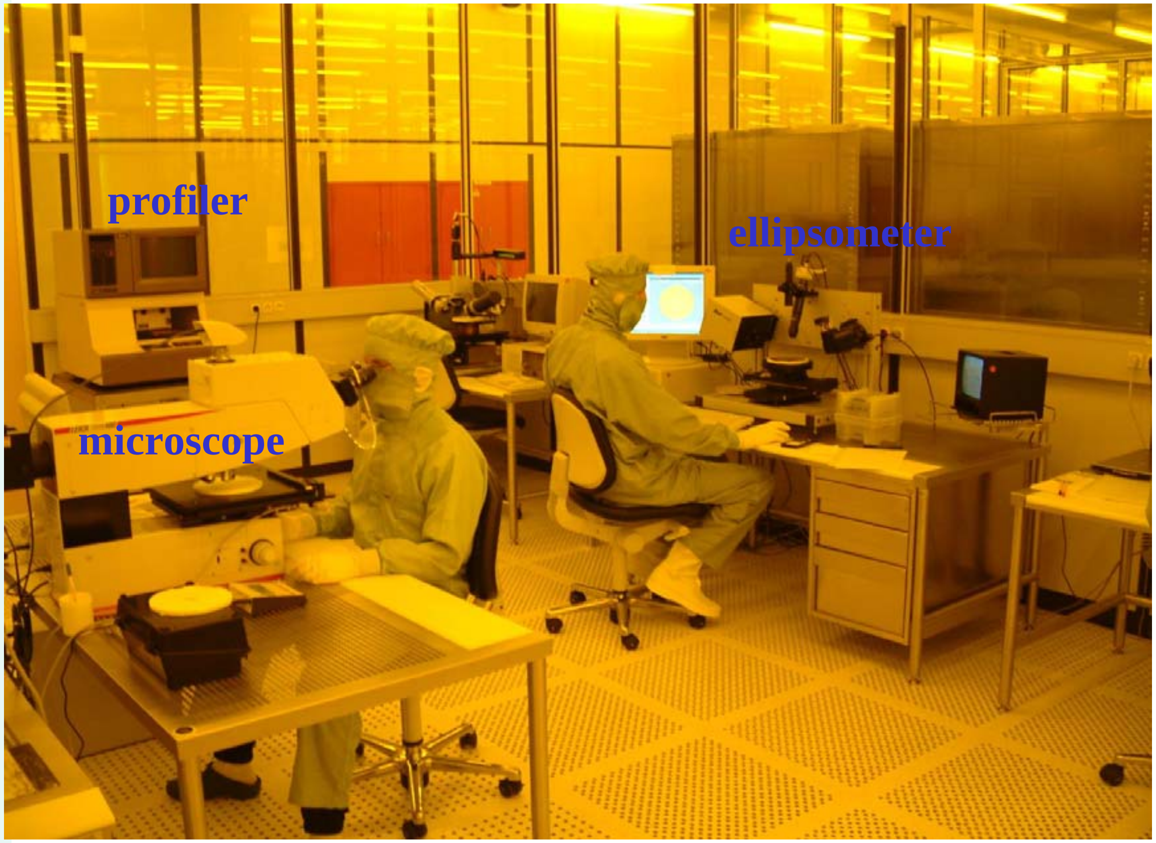
Quality control

- Extensive <u>Inspection</u> by **optical microscopy**
- Measurement of <u>layer thickness</u> by **ellipsometry** and stylus-**profilers**
- <u>Particle detection</u> on deposited layers by **light scattering**



Done externally:
REM, **AFM**,
VPD, **SIMS**,
chemical analysis

Chip separation and mounting

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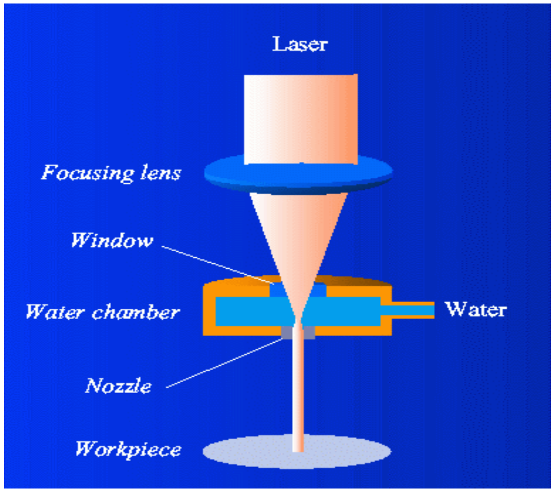
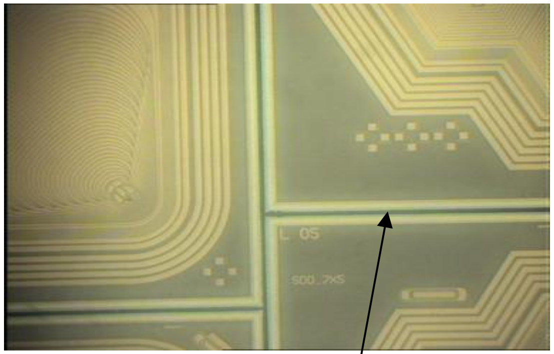


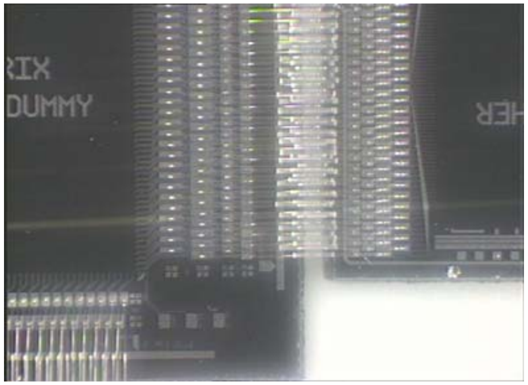
Principle of **Water guided Laserbeam**

Automatic Wedge bonder



75 μm wide Scribeline on diced wafer.

Laserbeam can cut **any shape**



Bonded chip (4 rows staggered)

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From Design to Reality

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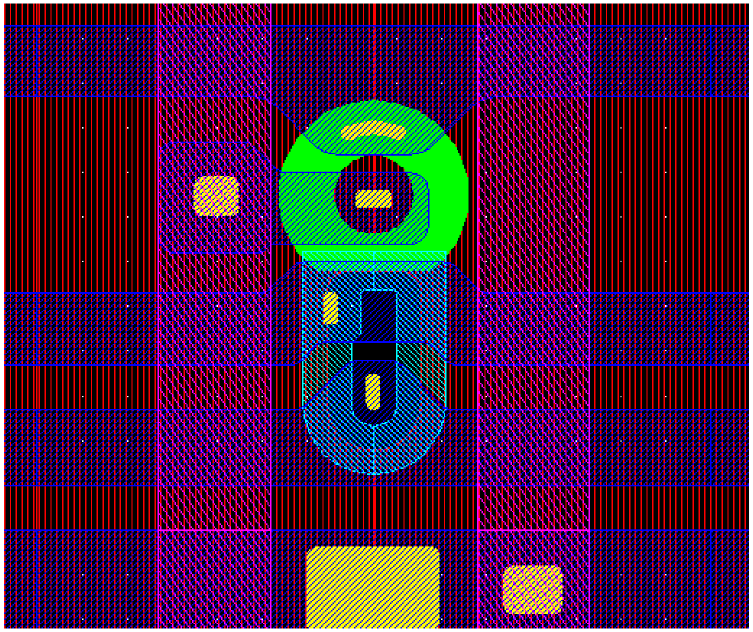
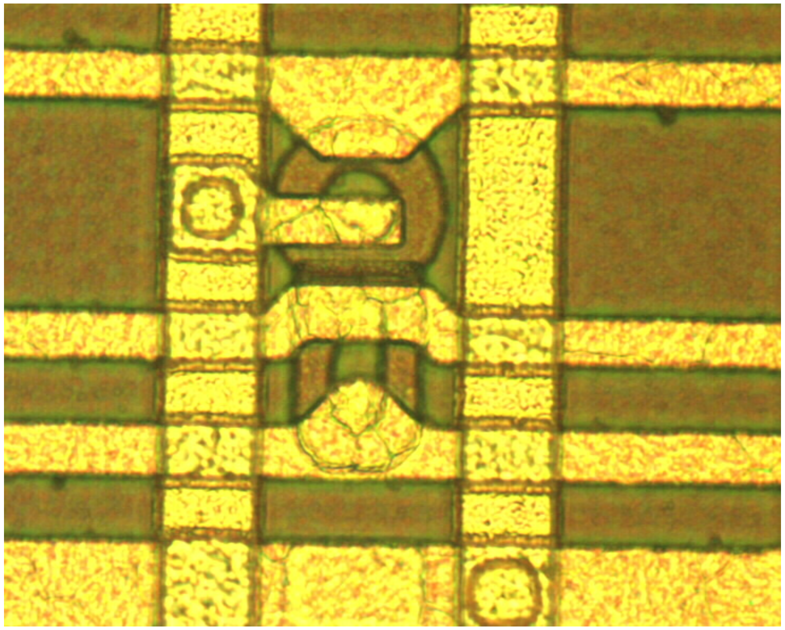
Layout of a DEPFET Active Pixel Sensor Cell
& same cell after processing



APS mask design (single cell)



APS cell finished

The DEPFET active pixel sensor

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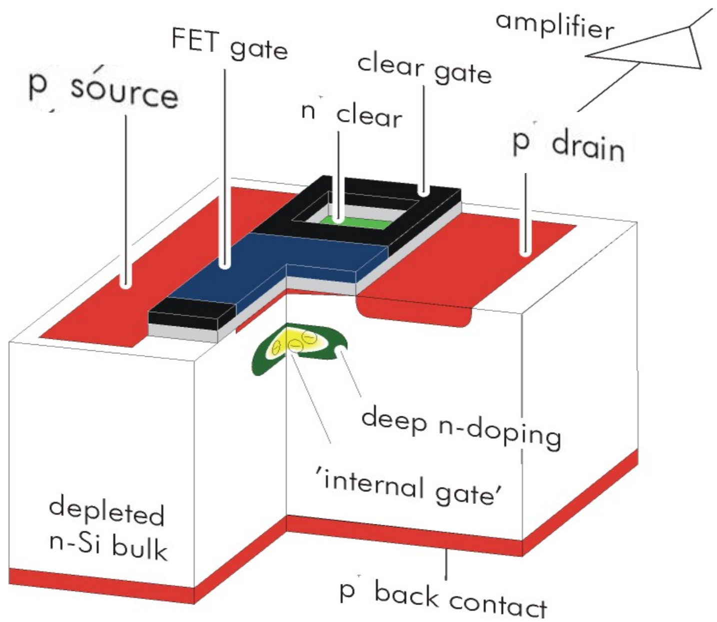

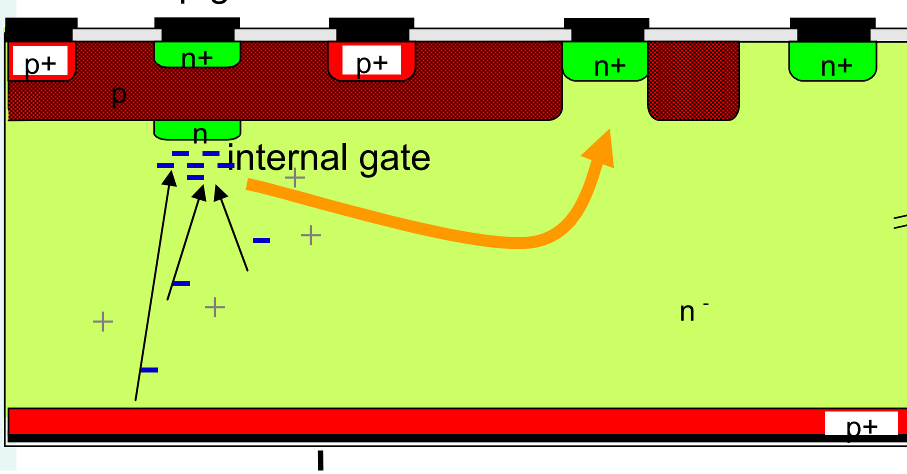

Depleted Field EffectTransistor

- Charge generated in fully depleted bulk
- Fast charge collection by drift underneath the transistor channel
- Modulates the transistor current (350 pA/e for ILC layout)
- Combined function of sensor and amplifier
- Low capacitance and low noise (10-20 fC)
- Signal charge remains undisturbed by readout
- Internal storage
- Complete clearing of signal charge
- No reset noise

Matrix operation

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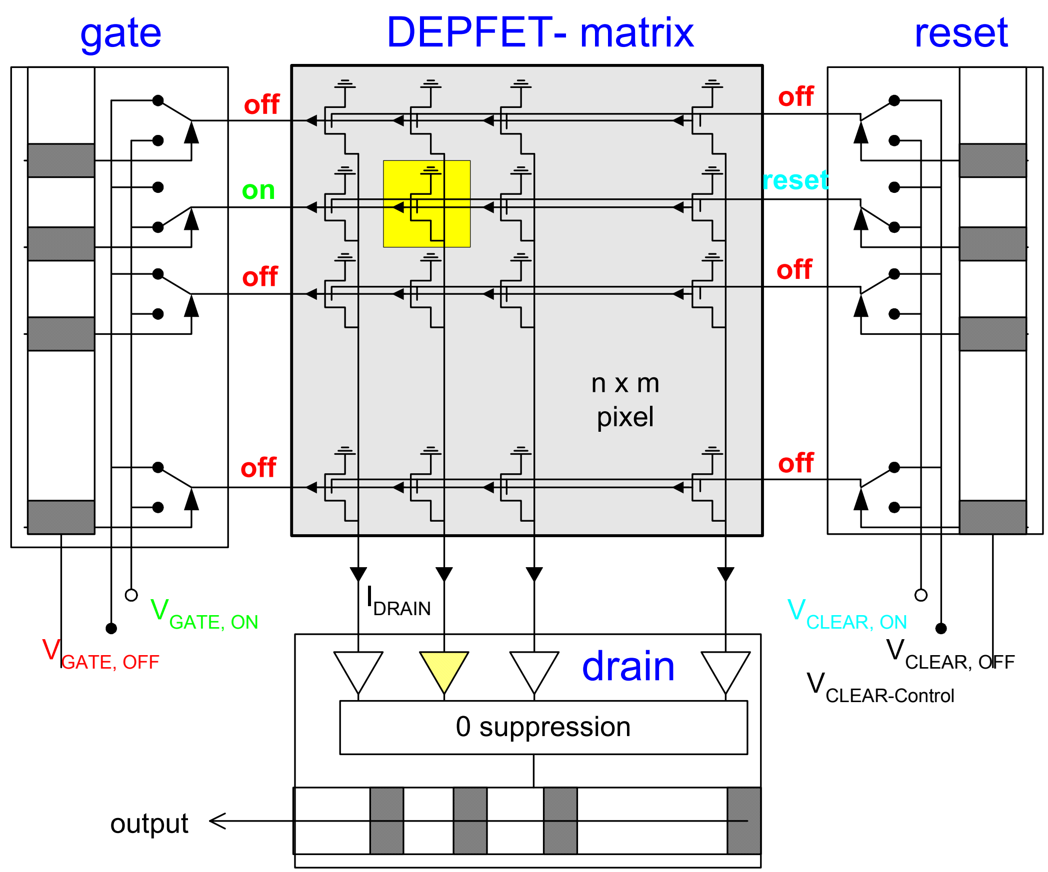

o **Charge collection in "OFF" state of the transistor**
o **Select one row via external gates and measure pedestal + signal current**
o **Reset that row and measure pedestal currents …..**

Only one single row active at a time and dissipating power
However, sensor is sensitive even if DEPFET is OFF!

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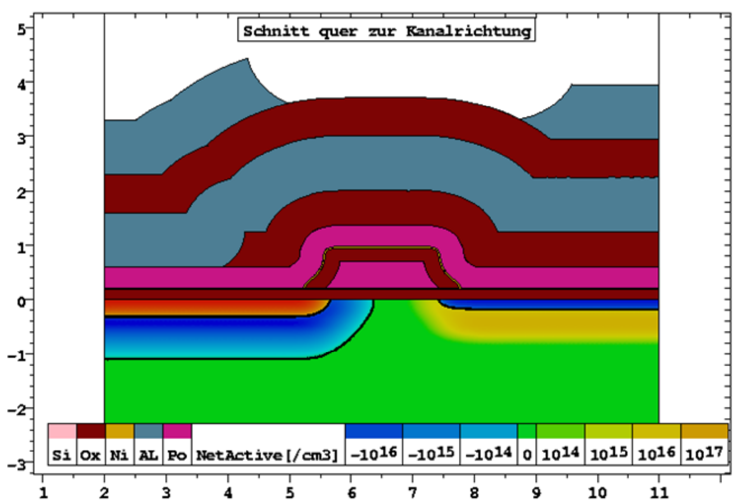
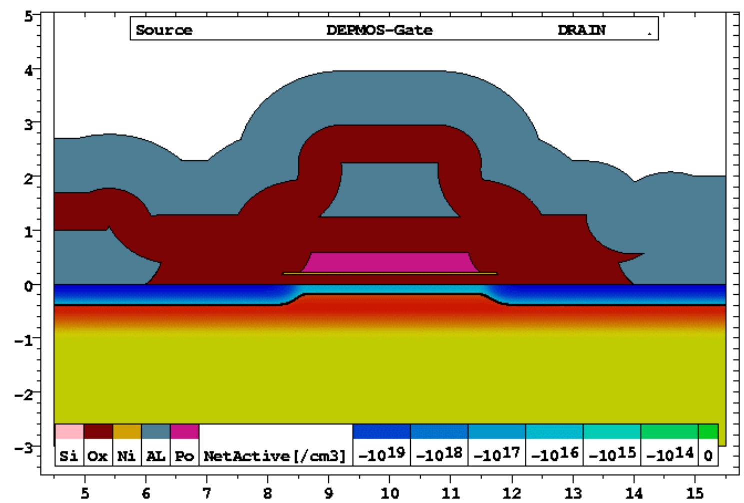
PXD4 - DEPFET: Two projects on one wafer

	ILC	*XEUS*
purpose	particle tracking	imaging spectroscopy
sensor size	1.3 x 10 cm², 2.2 x 12.5 cm²	7.68 x 7.68 cm²
pixel size	25 µm	75 µm
sensor thickness	50 µm	300 ... 500 µm
noise	~ 100 el. ENC	4 el. ENC
Readout time per row	20 ns	2.5 µs





Double metal, double poly process

The XEUS mission (2015)

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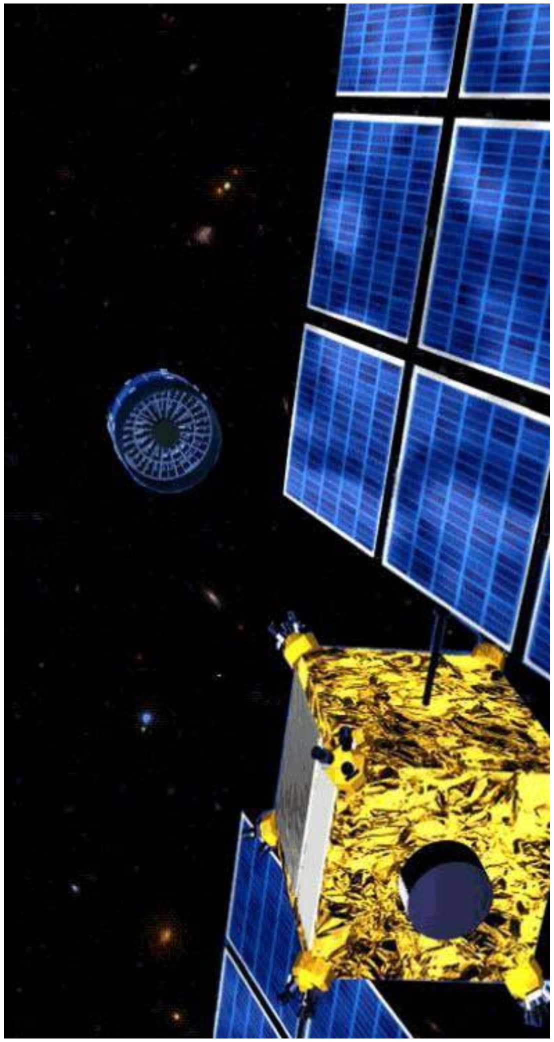
Mission concept:

- X-ray telescope consisting of two satelites, mirror (MSC) and detector (DSC) spacecraft
- Formation flight; active control of focal length with 1 mm^3 accuracy
- Replacement of DSC possible
- Increase of mirror surface from 6 m^2 to 30 m^2 possible
- Total mission lifetime ca. 25 yrs.
- 2 mirror technologies in discussion: Slumped glass / ESA high precision pore optics

Parameter	Specification (goal)
Energy range	0.05 -30 keV
Telescope focal length	50 m
Mirror area	6 m^2 (MSC 1) 30 m^2 (MSC 2)
Fields of view	5' (WFI) 1' (NFI)
Energy resolution @ C-Ka	50 eV (WFI), 2 eV (NFI)
Energy resolution @ Mn-Ka	125 eV (WFI), 5 eV (NFI)



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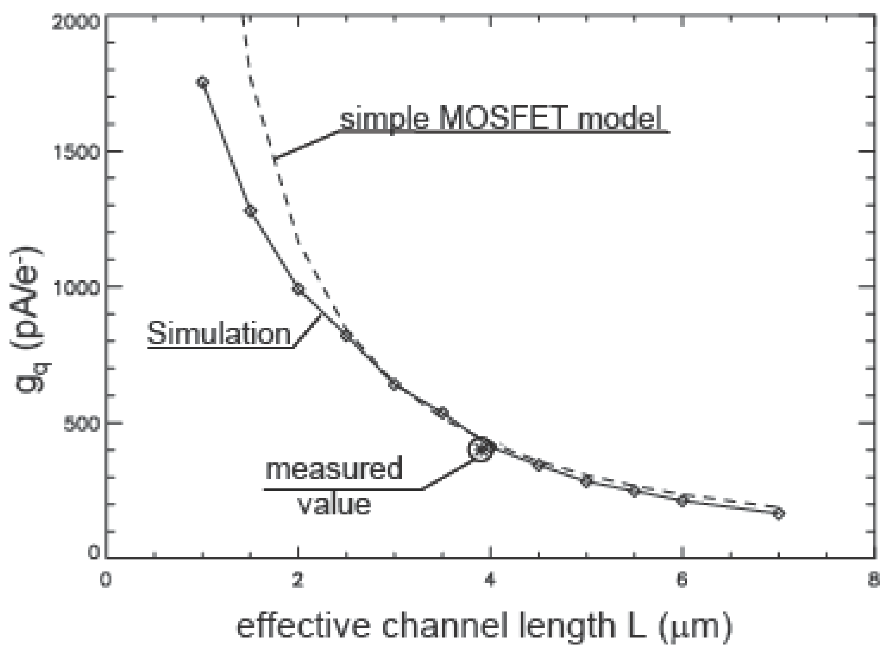
Lab Measurements

transconductance of the internal gate

$$g_q = \frac{dI_D}{dQ} = -\frac{\mu_p}{L^2}(V_{GS} - V_{th})$$



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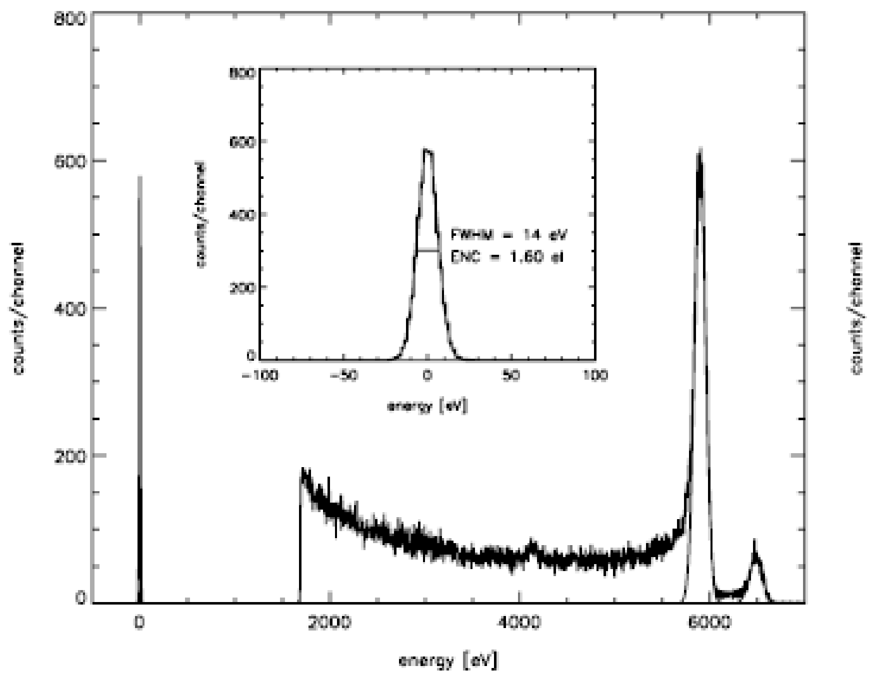
Lab Measurements

Low intrinsic noise

demonstrated by spectroscopic measurements with single pixels:

1.6 el rms noise

(at room temperature, 10 μs shaping time)



Fe^{55} spectrum

Clear (Reset)

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DEPFET Matrix Mode

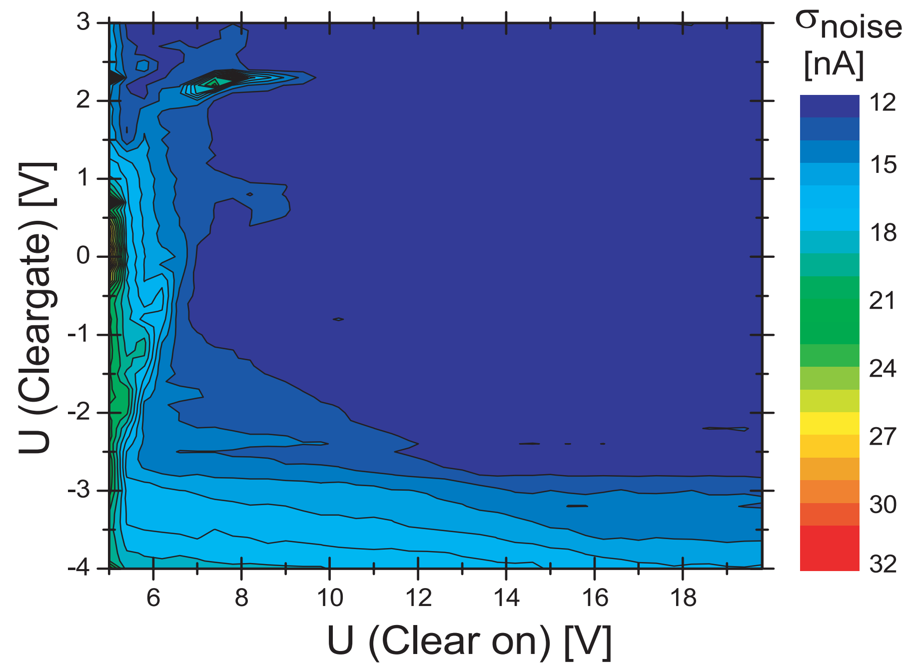
Accumulate
Read (1)
Clear
Read (2)
Accumulate

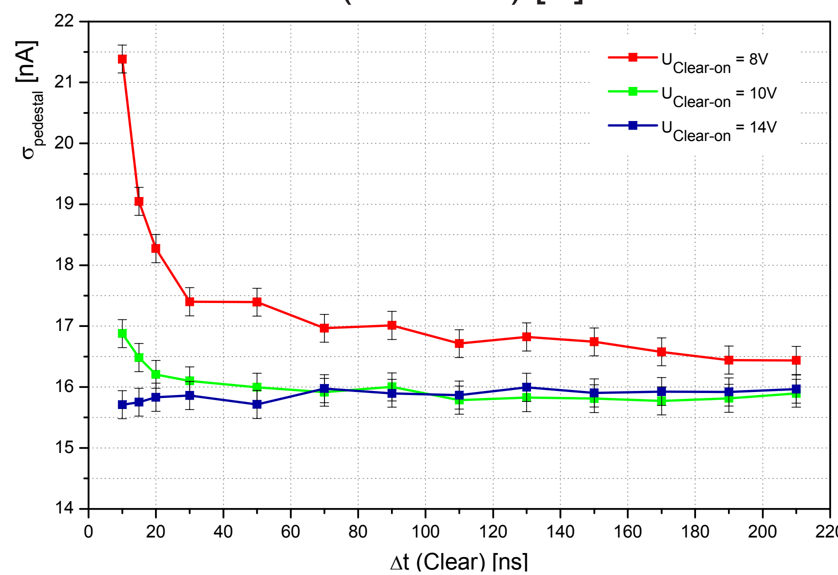
Signal = Read(1) – Read(2)
(Correlated sampling, pedestal suppression)

Clear efficiency important:
Depends on:
Clear contact voltage
Clear gate voltage

Incomplete clear reduces signal and adds noise

Complete clear in wide parameter range
Clearing time < 10ns achieved





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Radiation Hardness

Bulk damage: mainly by neutrons from calorimeters -> negligible

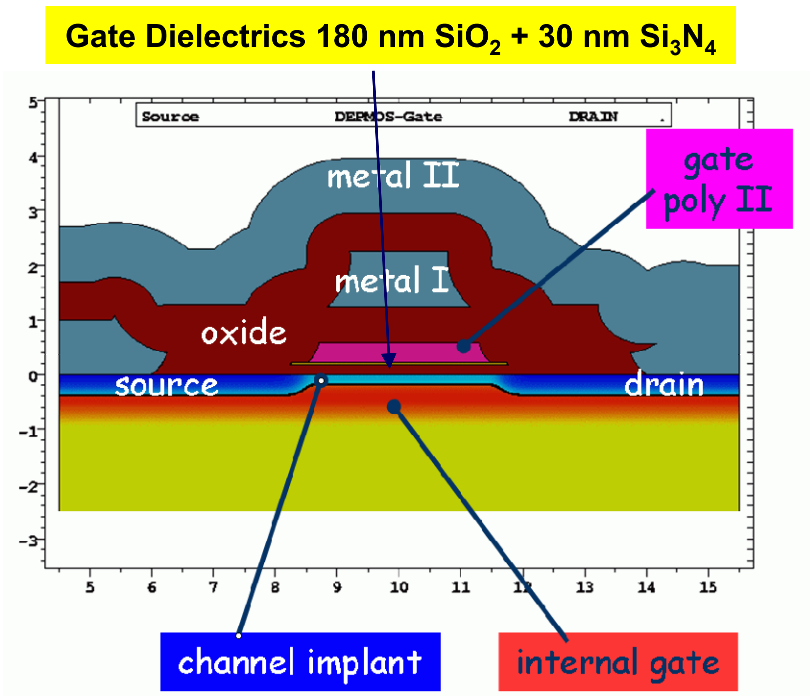
Oxide damage due to charged particles: 100 kRad in 5 years at 15mm

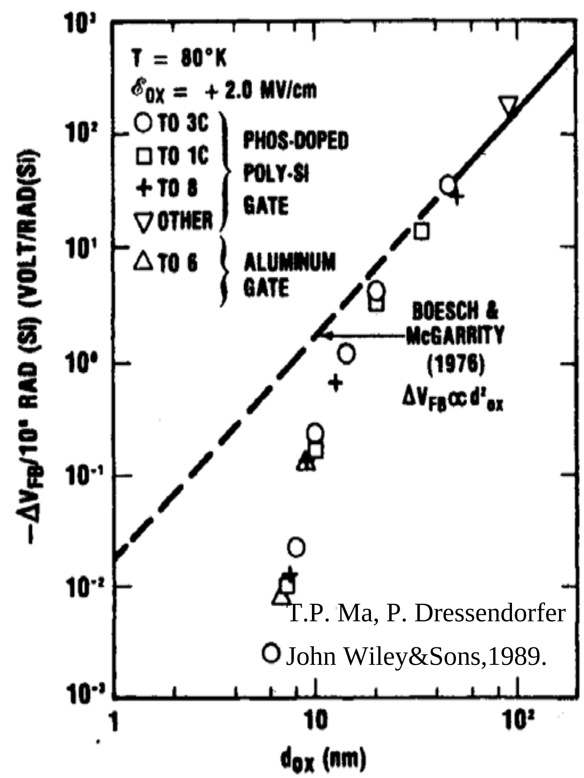
1. **positive oxide charge and positively charged oxide traps have to be compensated by a more negative gate voltage:**

   negative shift of the theshold voltage

2. **increased density of interface traps:**

   higher 1/f noise and reduced mobility (g_m)





Radiation Hardness

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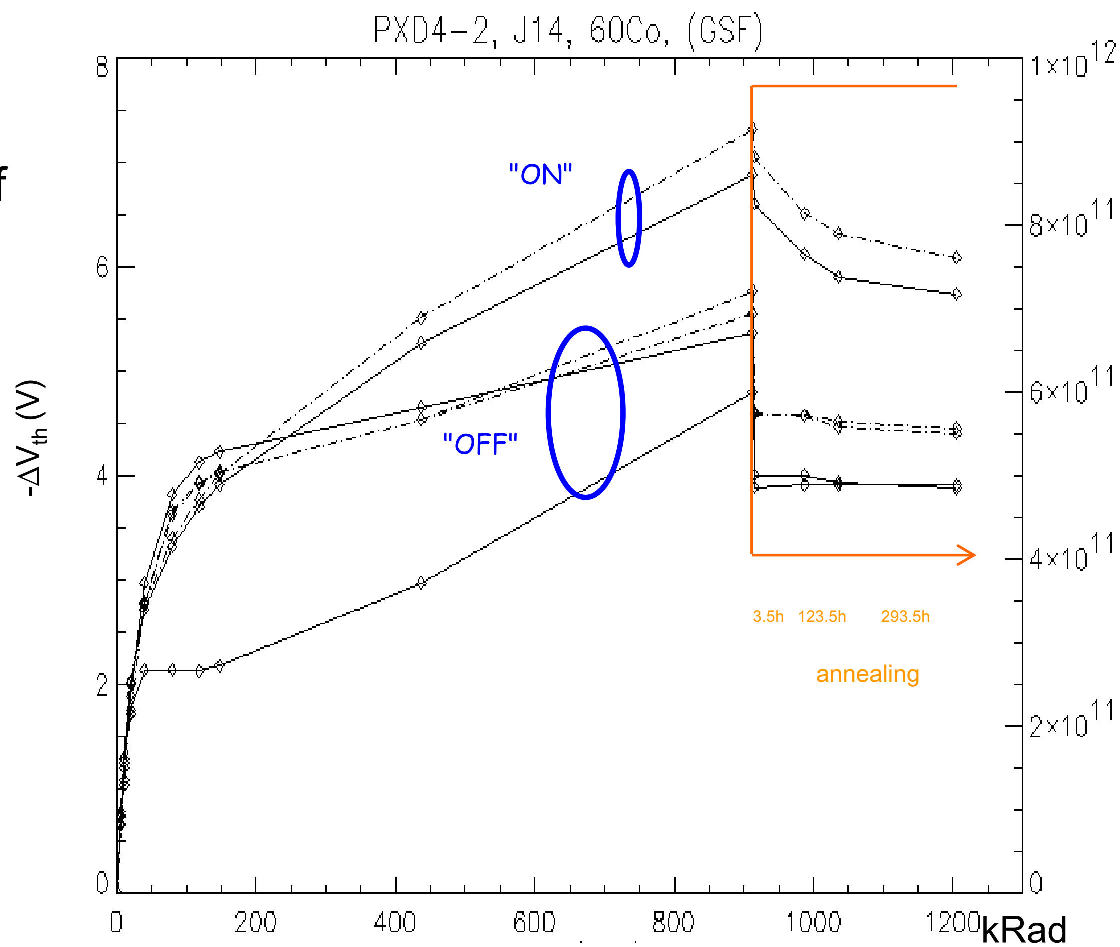
Irradiations on DEPFET teststructures (Co^{60} at GSF, Munich)

a) Irradiation in off state (gate voltage off)
b) Irradiation in on state (gate voltage on)

In ILC: DEPFET off most of the time (1000/1)

Threshold shift reasonably small ~ 4V

Can be compensated!



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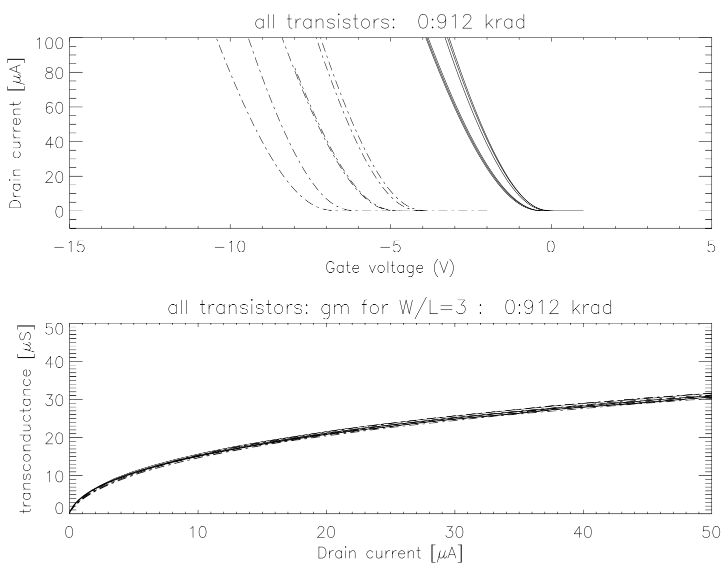
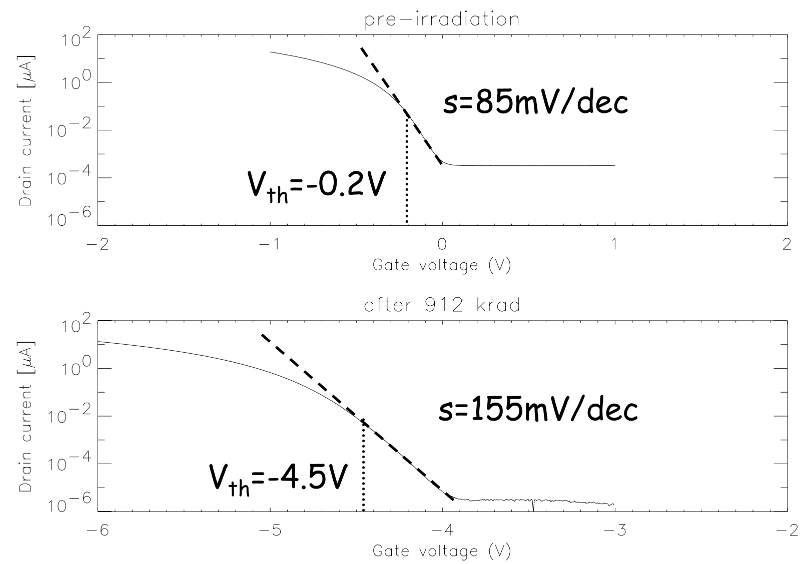
Transconductance and subthreshold slope





No change of the transconductance g_m

$$N_{it} = \frac{C_{ox}}{kT} \cdot \ln(10) \cdot \left(s_{D2} - s_{D1}\right)$$

Charge amplifcation:

Before irrad.: g_q = 350 pA/e

At 912 krad: g_q = 335 pA/e

300 krad → $N_{it} \approx 2 \cdot 10^{11}$ cm^{-2}

912 krad → $N_{it} \approx 7 \cdot 10^{11}$ cm^{-2}

Leakage current:

Before irrad: 5-22 fA

912 krad: 156 fA (~ 1 e/μs)

Literature:
After 1Mrad 200 nm (SiO_2):
$N_{it} \approx 10^{13}$ cm^{-2}

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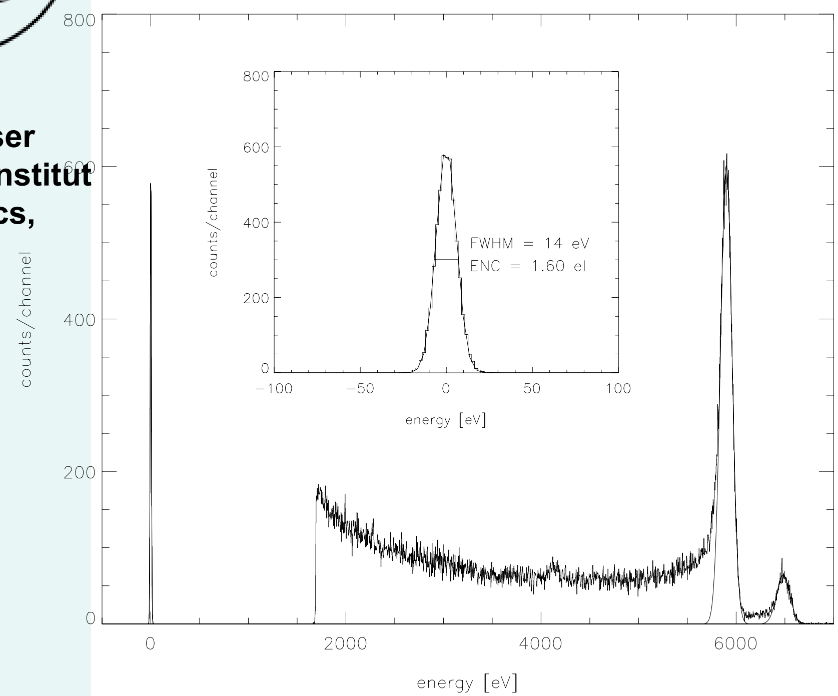
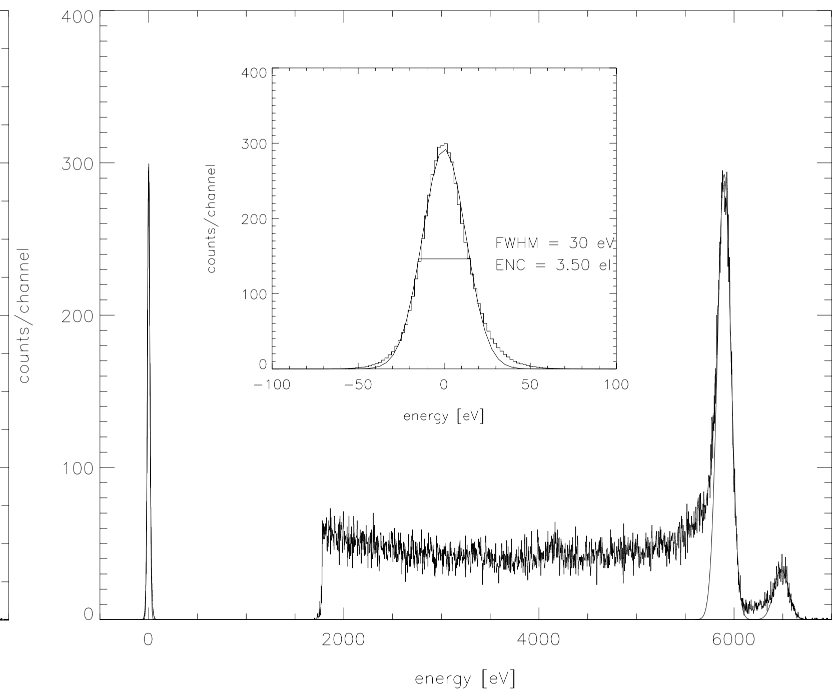
^{55}Fe Spectrum (single pixel)





non-irradiated

V_{thresh}≈-0.2V, V_{gate}=-2V
I_{drain}=41 μA
time cont. shaping τ=10 μs

Noise ENC=1.6 e^- (rms)

at T>23 degC

912 krad ^{60}Co

V_{thresh}≈-4.0V, V_{gate}=-6.0V
I_{drain}=40 μA
time cont. shaping τ=10 μs

Noise ENC=3.5 e^- (rms)

at T>23 degC

Noise vs. shaping time τ

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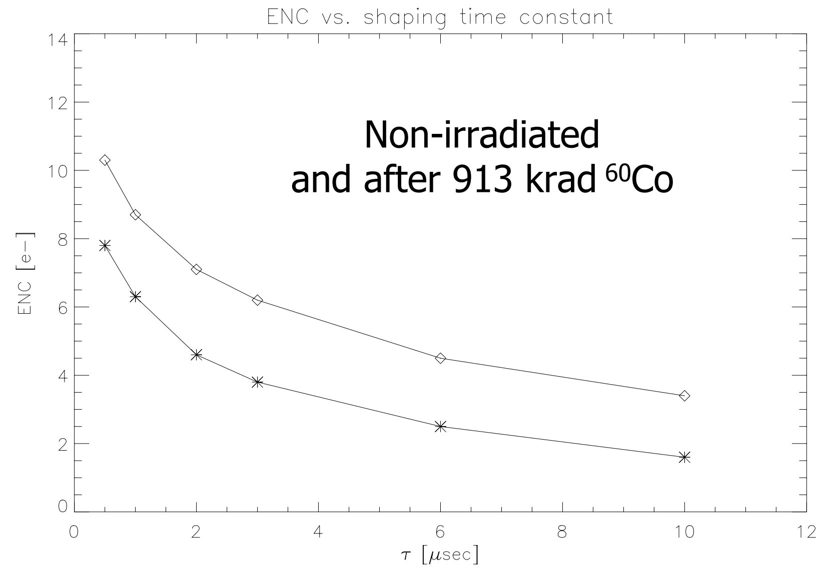
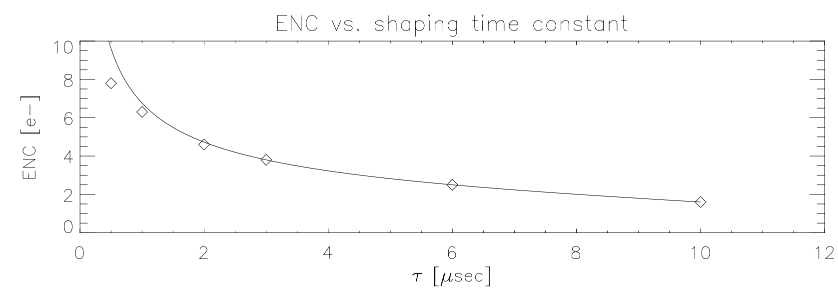
$$ENC = \sqrt{\alpha \frac{2kT}{g_m} C_{tot}^2 A_1 \frac{1}{\tau} + 2\pi a_f C_{tot}^2 A_2 + q I_L A_3 \tau}$$

Thermal noise

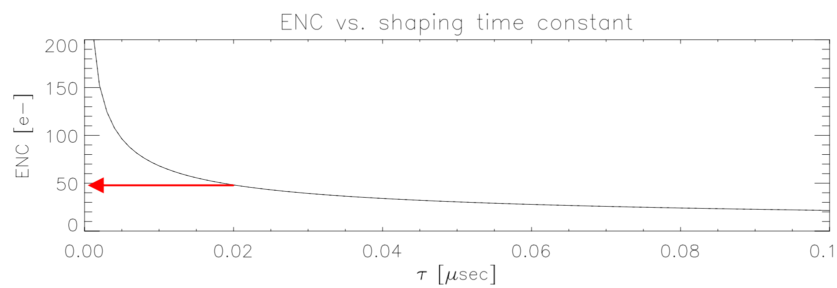
1/f noise

Leakage current





Fit and extrapolate to 20ns
(Bandwidth at ILC)



Expect:	~ 50 e noise
Calculation:	~ 36 e noise

DEPFET Matrix Test System

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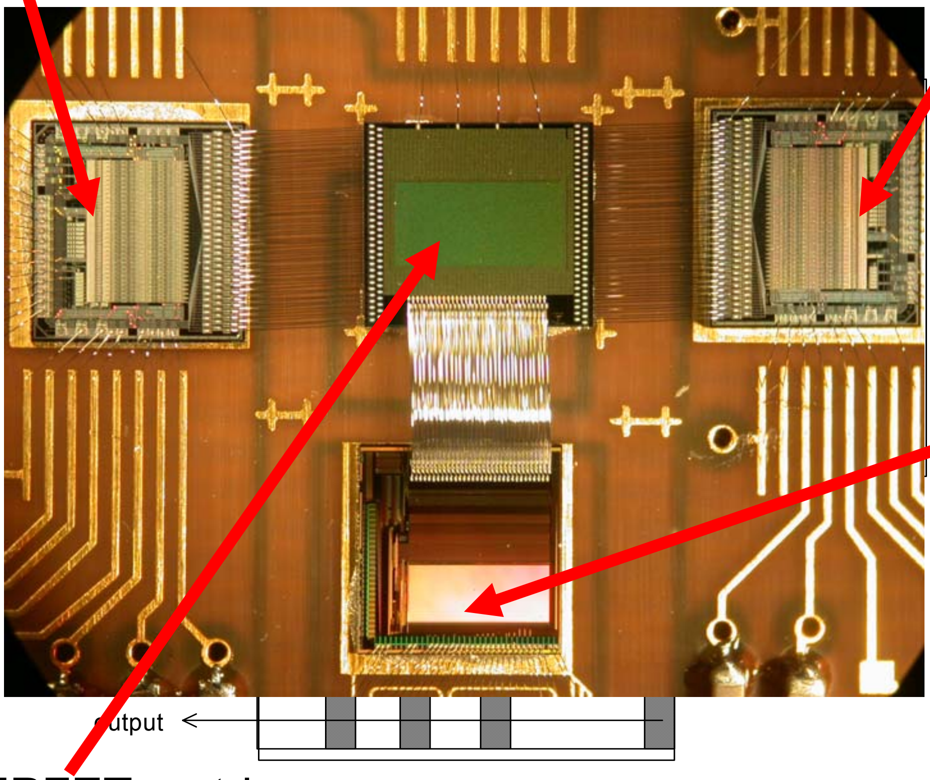
Switcher I: selects rows for readout (switch external gate)

Switcher II: clears rows



Curo II readout chip
128 channel current amplifier for column readout
Internal pipeline & 0-suppression

DEPFET matrix
64x128 pixels
28.5x36 μm^2

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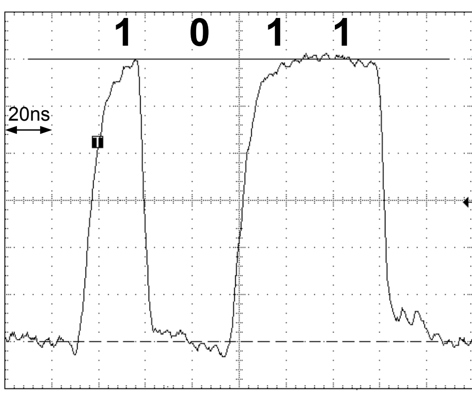
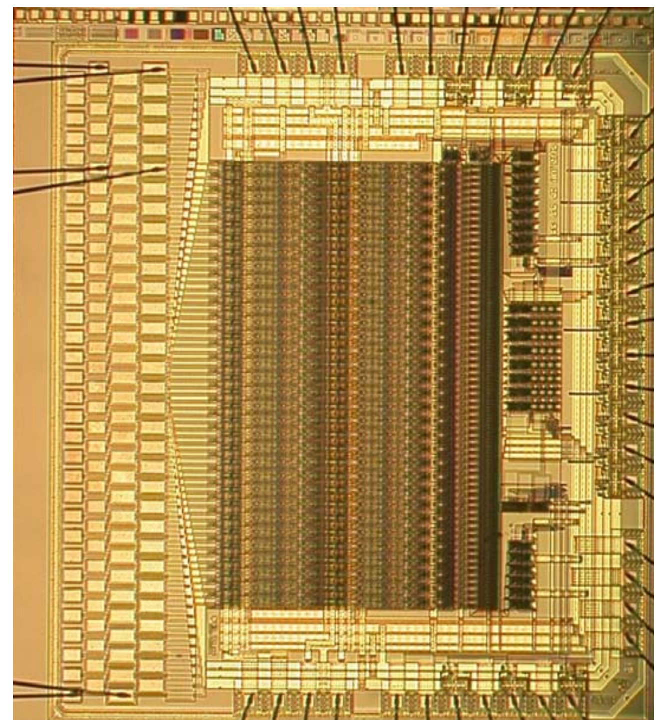
Support ASICs: Switcher

Switcher: provides gate and clear signals

- **64 channels** with **2 analog MUX** outputs (‘A’ and ‘B’)
- Can switch up to **25 V**
- **digital control ground + supply floating**
- **fast internal sequencer** for programmable pattern (operates up to 80MHz)
- Present dissipation: **1mW/channel @ 30MHz**
- 0.8µm AMS HV technology



$\Delta U = 20V$ $\nu = 30$ MHz



Research techniques seminar
Fermilab
June 6 2006

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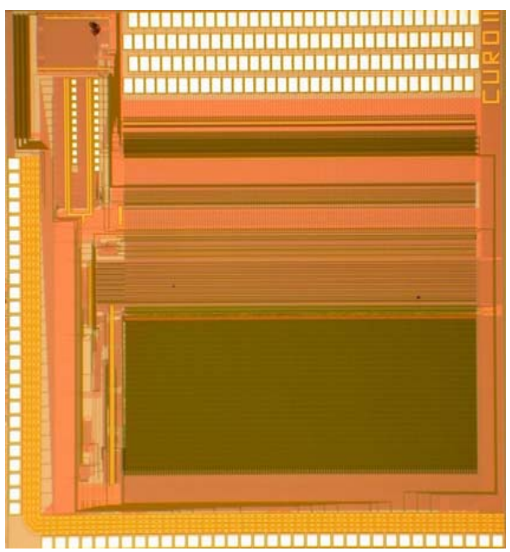
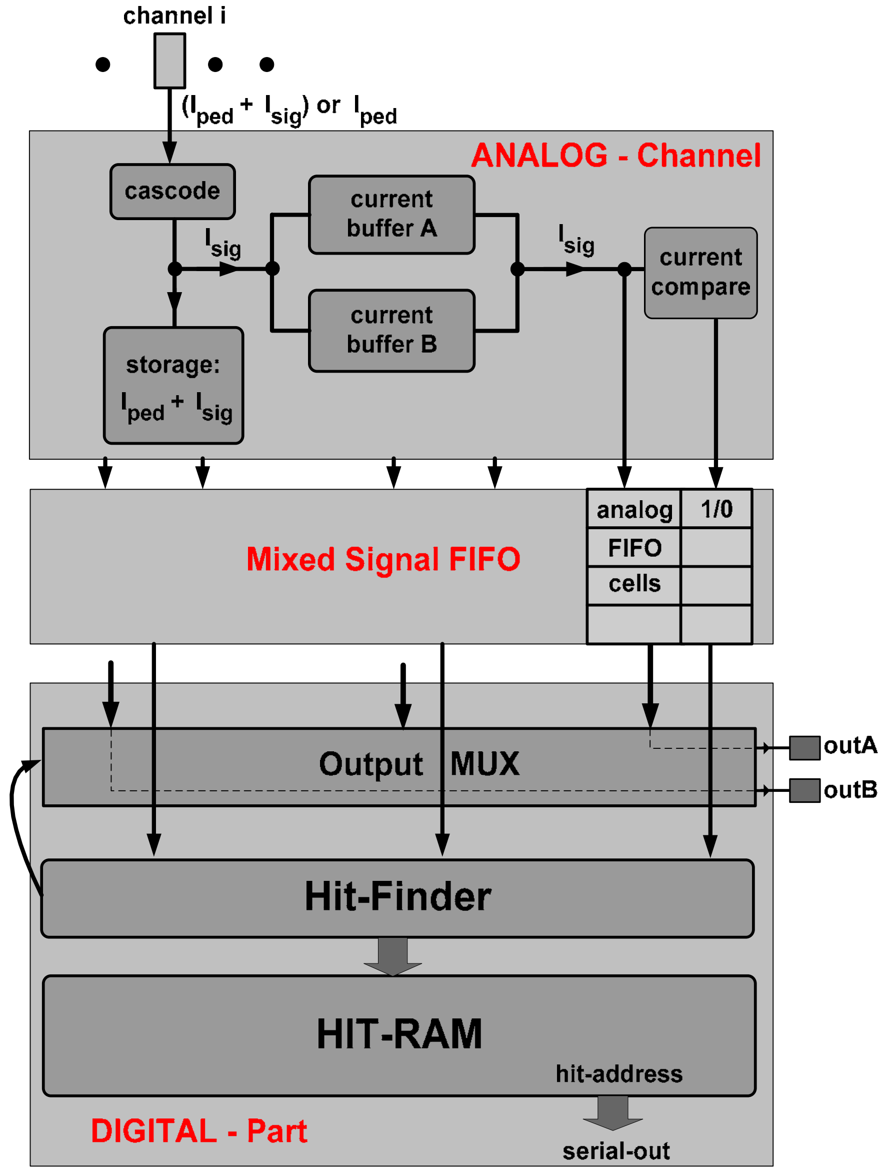
Support ASICs: Curo

CURO: 128 channel readout chip

- On-chip **pedestal subtraction** (correlated double sampling)
- Real time **hit finding** and **zero suppression**
- Hit addresses store in on-chip RAM
- 0.25µm CMOS technology
- **Row rate of 25 MHz has been achieved**





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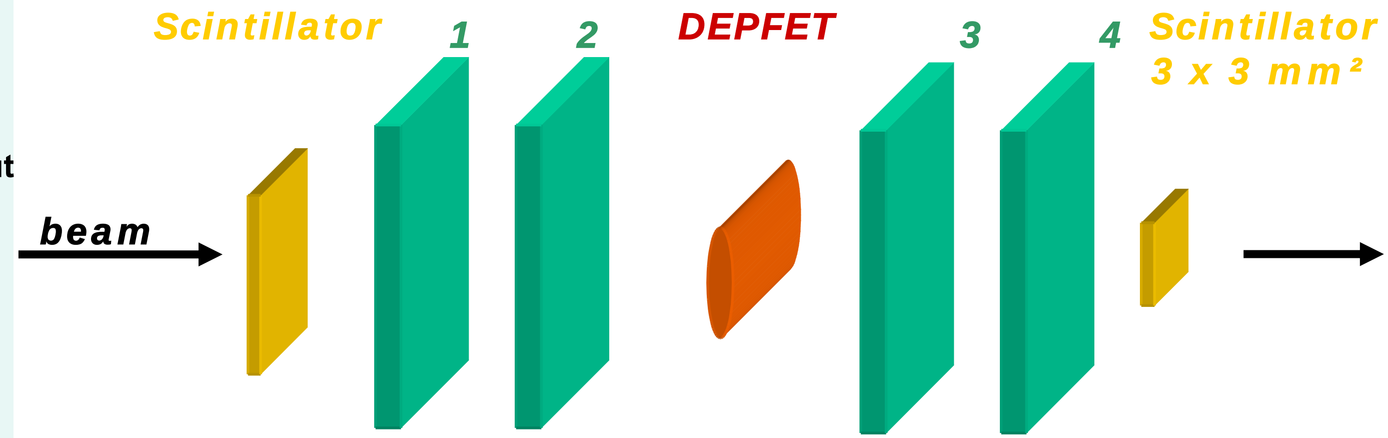
Testbeam



DESY test beam with 6 GeV e-

Bonn ATLAS telescope system:

- double sided strip detectors, 300µm
- pitch 50 µm

DEPFET:

- 128x64 (28.5x36 μm^2)
- 450 µm thick
- Row rate time 13.4µs (limited by DAQ)
- sample-clear-sample: 300ns

Noise & Cluster Calculation

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noise calculation:

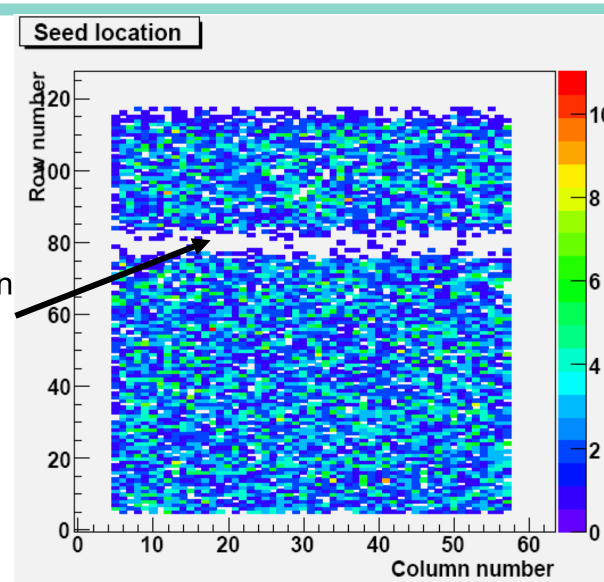
signal distribution after pedestal and common mode correction & hit removal

16.3 ADU → ENC: ~300 e$^-$

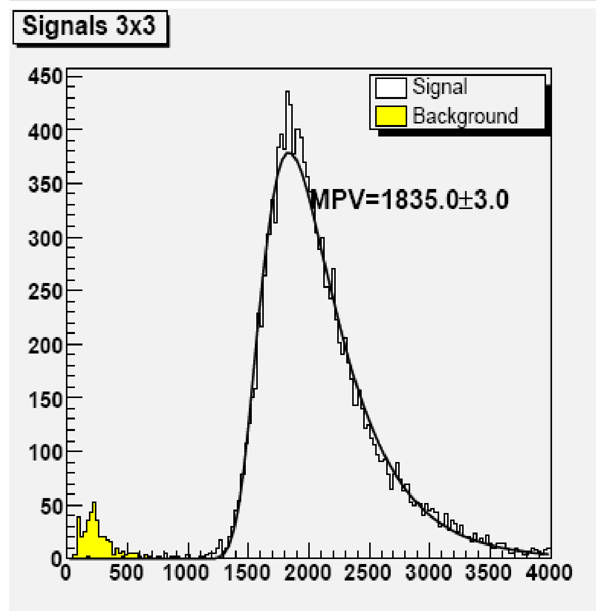
cluster finding:

5σ seed threshold,
2σ neighbor threshold in given ROI

steering line short in matrix layout (no LVS…)



cluster size	MPV [ADU]
3 x 3	1835
5 x 5	1850
7 x 7	1868



signal confined in 3 x 3 pixel clusters

S/N = 112 (450 µm substrate)

Noise dominated by systems noise (pickup)

Front end noise ~ 100 e (estimated)

Uncertainty in Predicted Position

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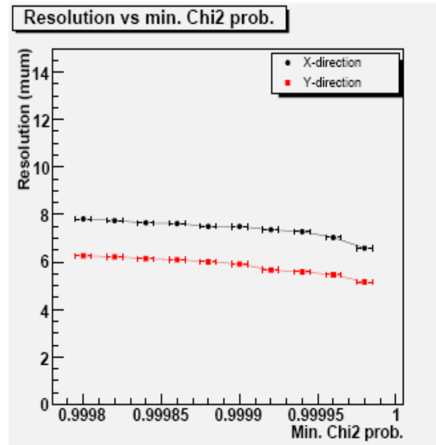
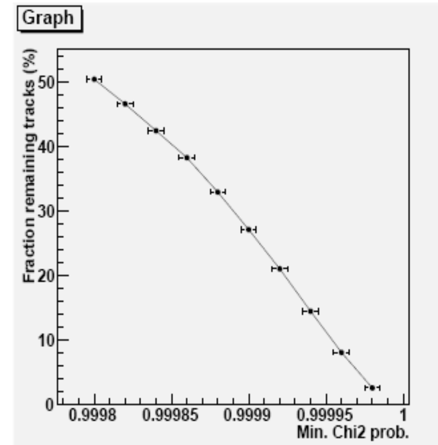
6 GeV e$^-$ beam @ DESY ➔ multiple scattering limited position resolution

apply χ^2-cut on fitted racks:

- does not improve too much (compact setup)

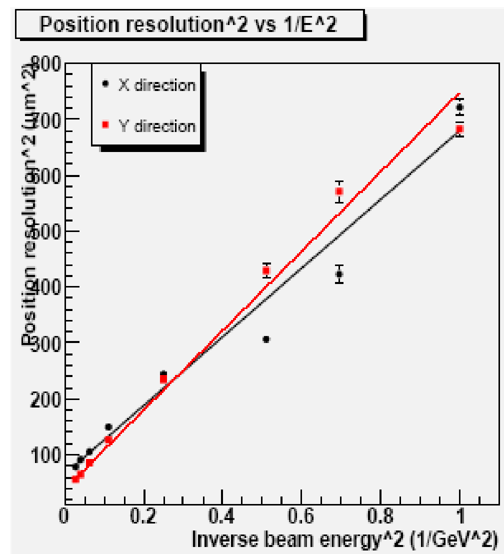
better:





scan beam energy to estimate true resolution:

Detector	X-Resolution (μm)	Y-Resolution (μm)	X-η_{est}	Y-η_{est}
Hybrid 2A	8.1±0.1	7.1±0.1	5.3	3.2
Hybrid 1A	8.0±0.1	7.5±0.1	5.2	4.0
Hybrid 1B	8.2±0.1	8.1±0.1	5.5	5.1
Hybrid Mun1	9.0±0.1	7.8±0.1	6.6	4.6
Hybrid GCG	8.0±0.1	7.8±0.1	5.2	4.6



Still ~ 4 μm uncertainty (telescope resolution)
Testbeam at CERN planned

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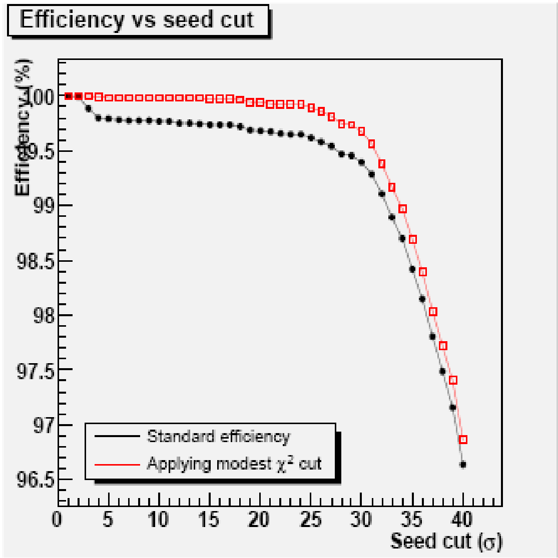
Efficiency & Purity

Efficiency = #good clusters/#good tracks

- 5σ seed cut

➔ efficiency > 99.9%

Hybrid	No (%)	Wrong (%)	Eff (%)	No (%)	Wrong (%)	Eff (%)
Hyb2A	0.038	0.209	99.75	0.021	0.021	99.96
HybMun1	0.040	0.373	99.63	0	0.022	99.98
Hyb1B	0.046	0.137	99.82	0.025	0	99.97
Hyb1A	0.010	0.251	99.74	0.012	0	99.99
HybCGC	0.031	0.187	99.78	0.018	0	99.98



Purity = #good clusters/#all clusters

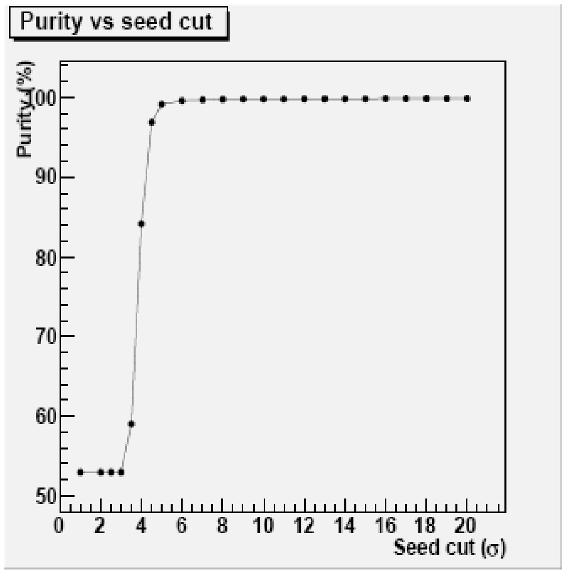
- problem: long integration time causes ~15% double hits

→ look for clusters in inverted frames

- still problem: out of time events (events between clear and 2. sample)

→ correct for them

➔ Purity ~ 100%



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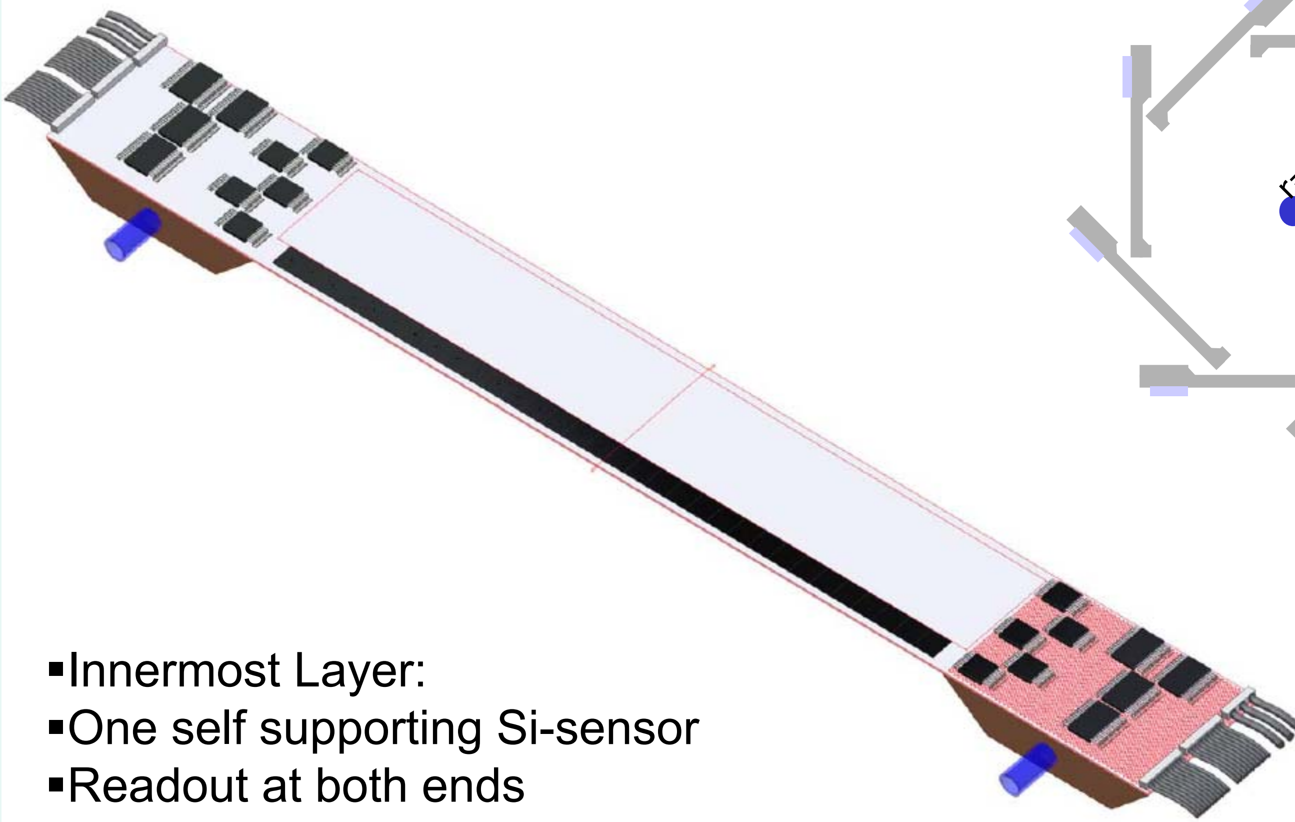
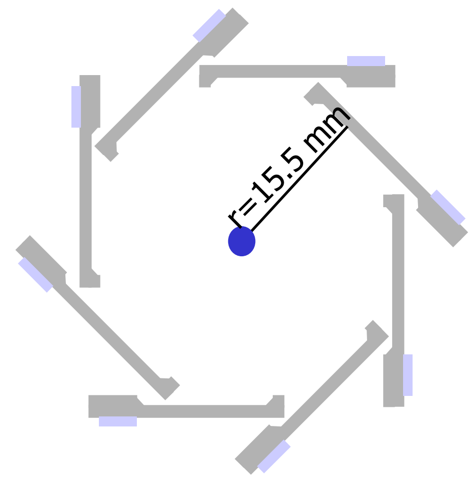
Module Concept & Material Budget





- Innermost Layer:
- One self supporting Si-sensor
- Readout at both ends
- Sensitive area thinned to 50 μm
- Support frame not thinned (300 μm)
- Thinned (50 μm) ASIC bump bonded

Processing thin detectors (50 μm)

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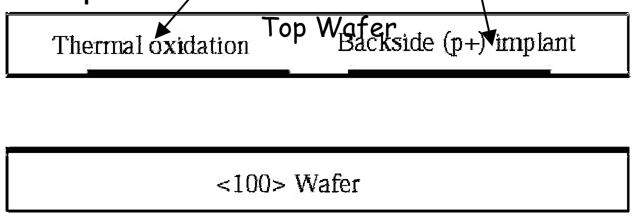
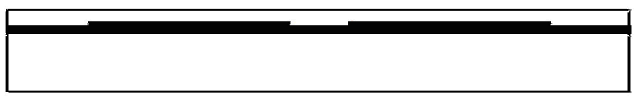
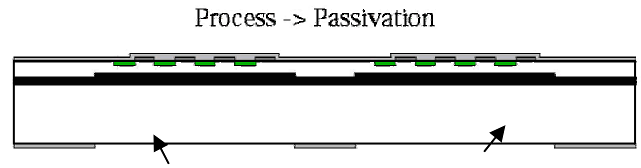
a) oxidation and back side implant of top wafer

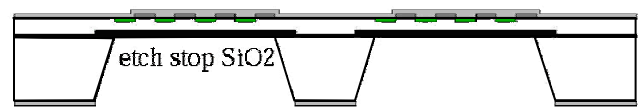




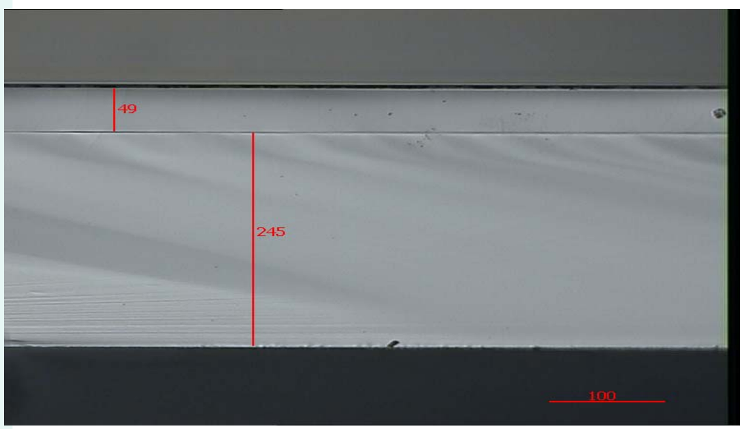
c) process ➔ passivation



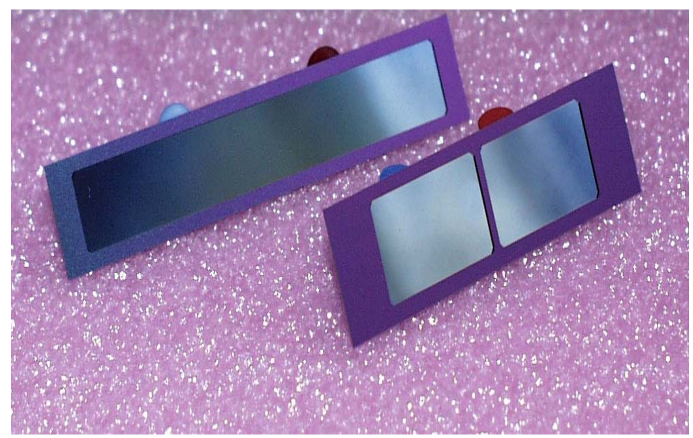
open backside passivation



b) wafer bonding and grinding/polishing of top wafer



d) deep etching opens "windows" in handle wafer



Successfully tested with MOS diodes (keep low leakage current ~ 800 pA/cm^2)

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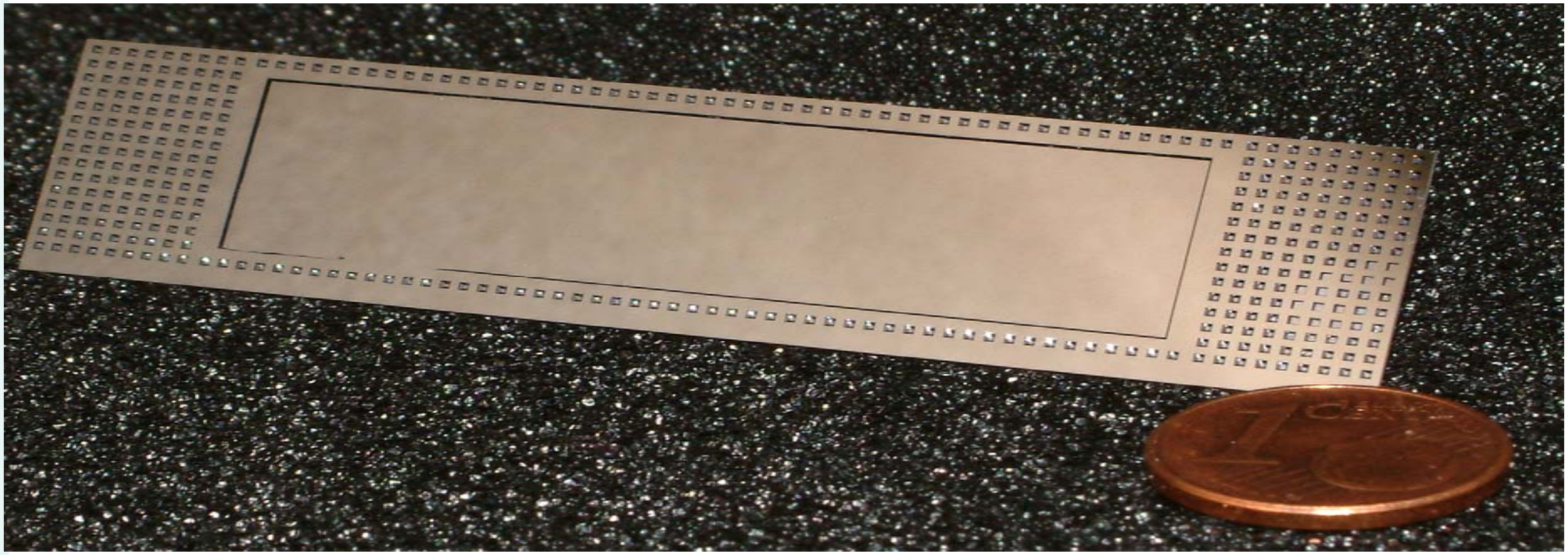
Material Budget

Estimated Material Budget (1st layer):

Pixel area:	**100x13 mm^2, 50 µm:**	**0.05% X_0**
steer. chips:	**100x2 mm^2, 50 µm:**	**0.008% X_0**
(perforated) frame :	**100x4 mm^2, 300 µm:**	**0.05% X_0**
_		**0.11%X_0**



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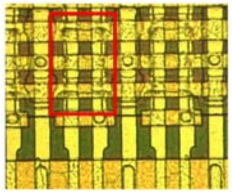
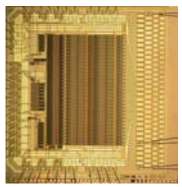
Module Concept/Power Consumption

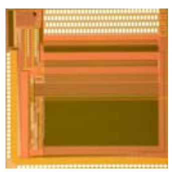
DEPFET Matrix:	power per active pixel:	50 mW
	only one row active:	0.5-0.8 W/row
	duty cycle:	1/200
	5 layer detector:	0.5 W



Switcher:	power per active row:	6.3 mW
	duty cycle:	1/200
	5 layer detector	4 mW



CURO:	power/channel (50MHz)	2.8 mW
	duty cycle:	1/200
	5 layer detector:	2.6 W



Total:		3.1 W

Only 0.5 W in active area (no cooling of sensors needed)
Only 2.6 W at the end flanges
Low power consumption further reduces material needs

Simulations

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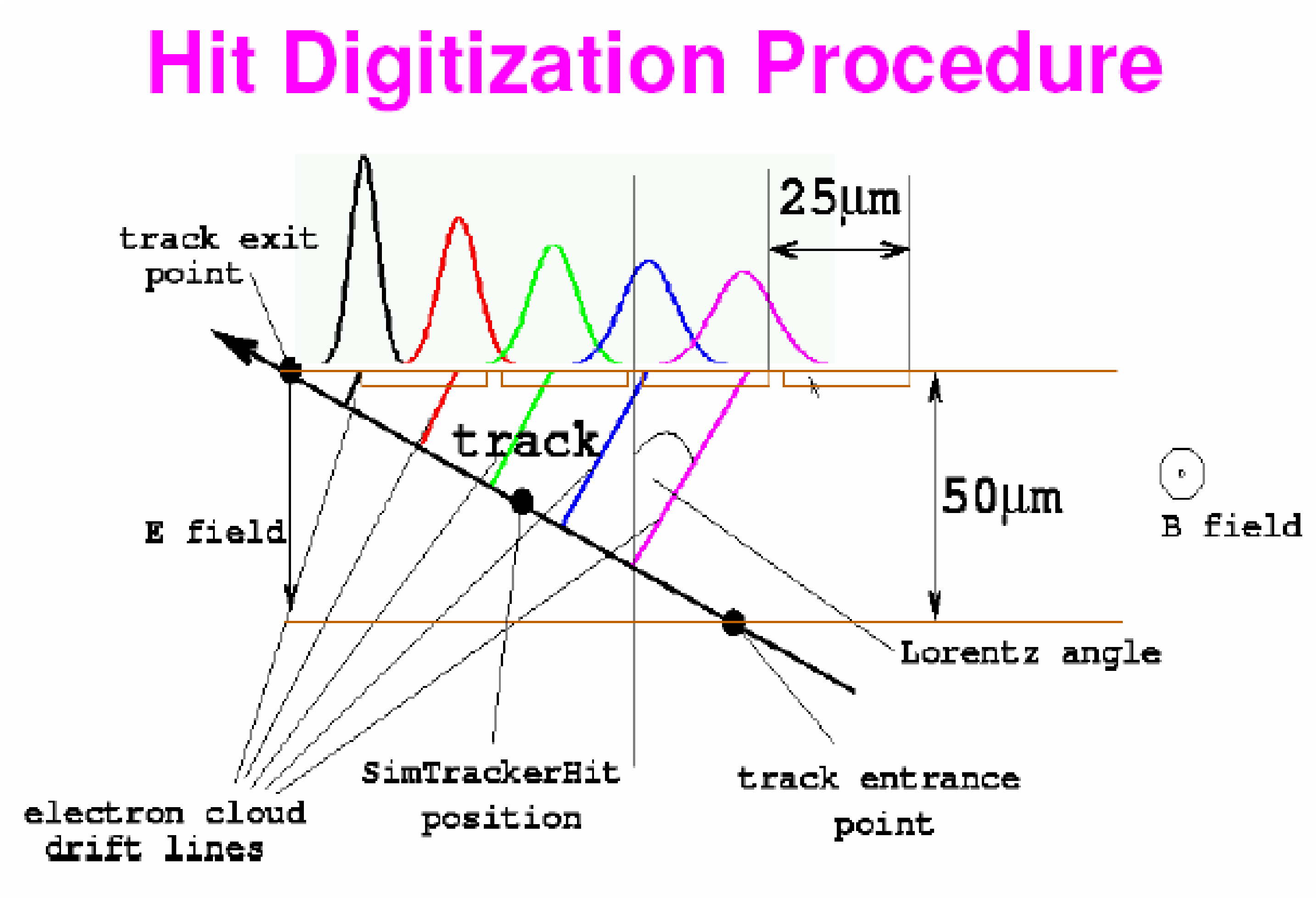
DEPFET module implemented in LDC Geant4 simulations tools (MOKKA) (A. Raspereza)



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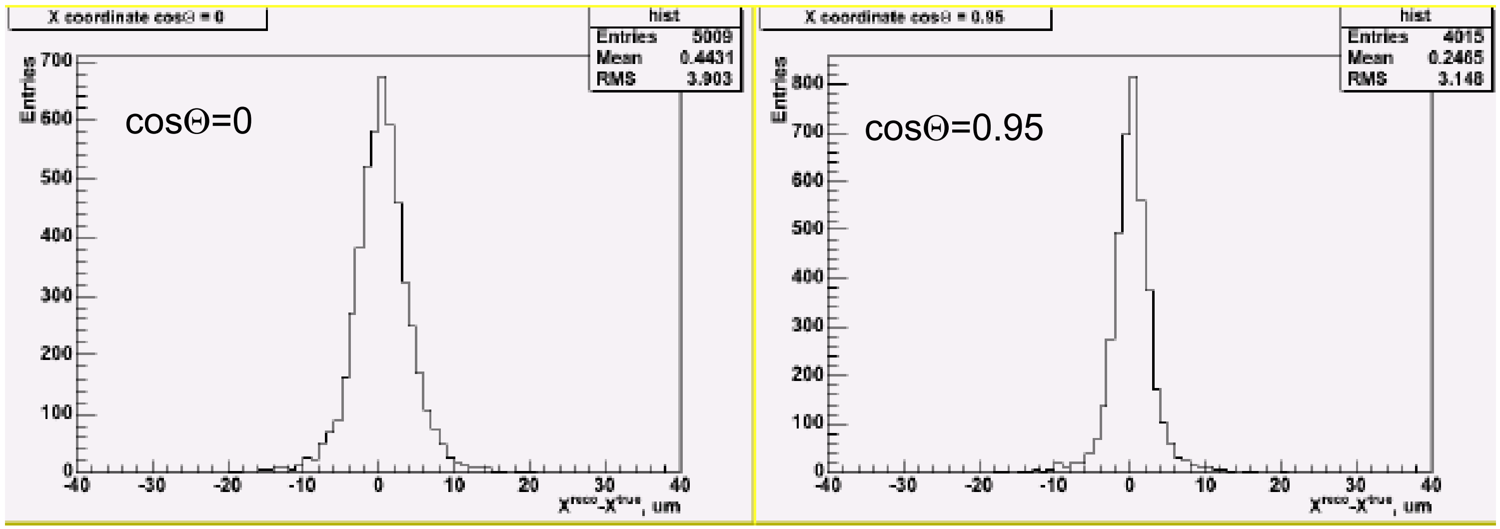
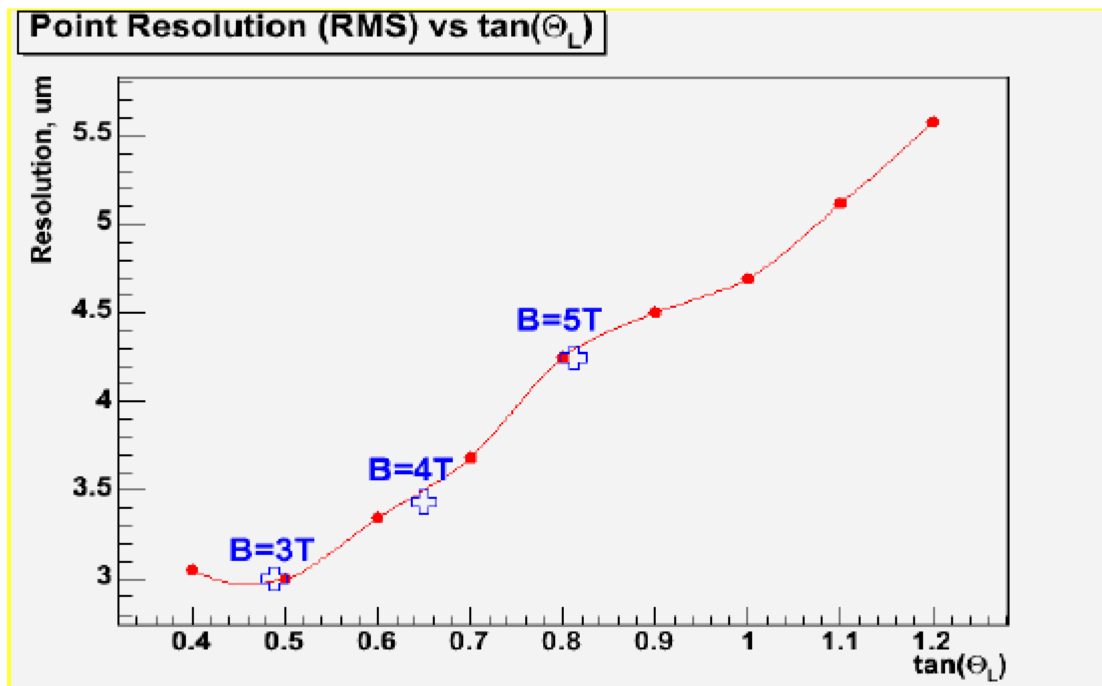
Resolution: R-Phi



Nominal resolution
3.4 μm (RMS)
-Normal incidence
-B=4T (LDC)
-(25 μm)^2 pixel
-50 μm thickness

-Depends slightly on B (Lorentz angle)



Resolution: z

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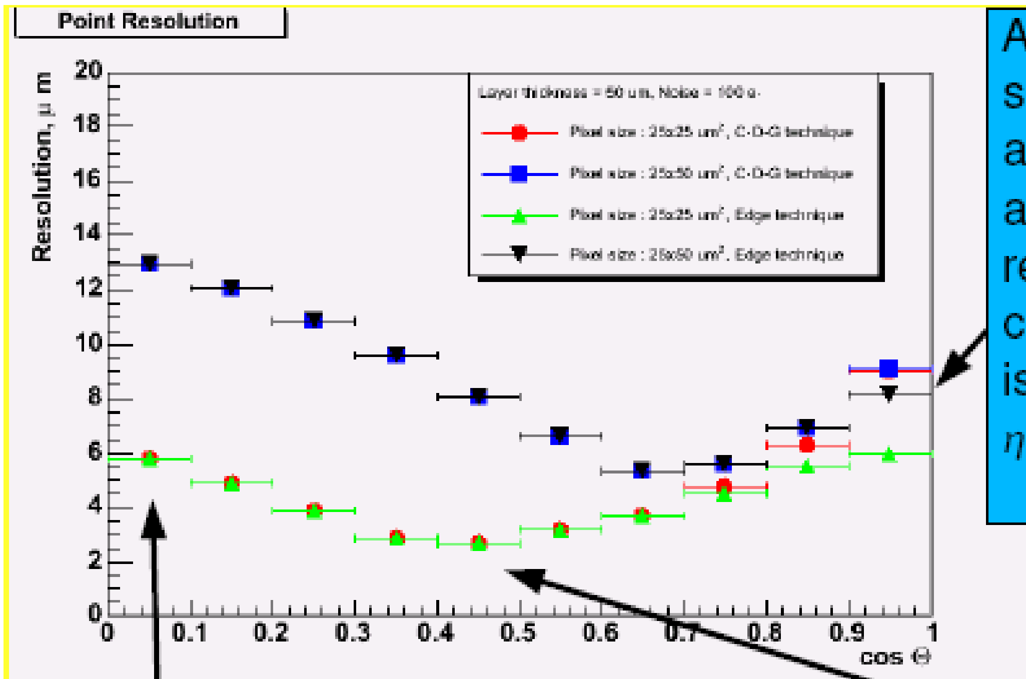

At shallow angles cluster size gets extremely large and simple centre-of-gravity approach yeilds poor resolution due to inter-pixel charge fluctuations. Resolution is improved by means of η-algorithm (edge-technique)

In many cases at normal incidence only one row is fired :
resolution is limited by pixel size

When track is inclined more than one row is fired -> resolution gets better

Impact Parameter Resolution (D_0)

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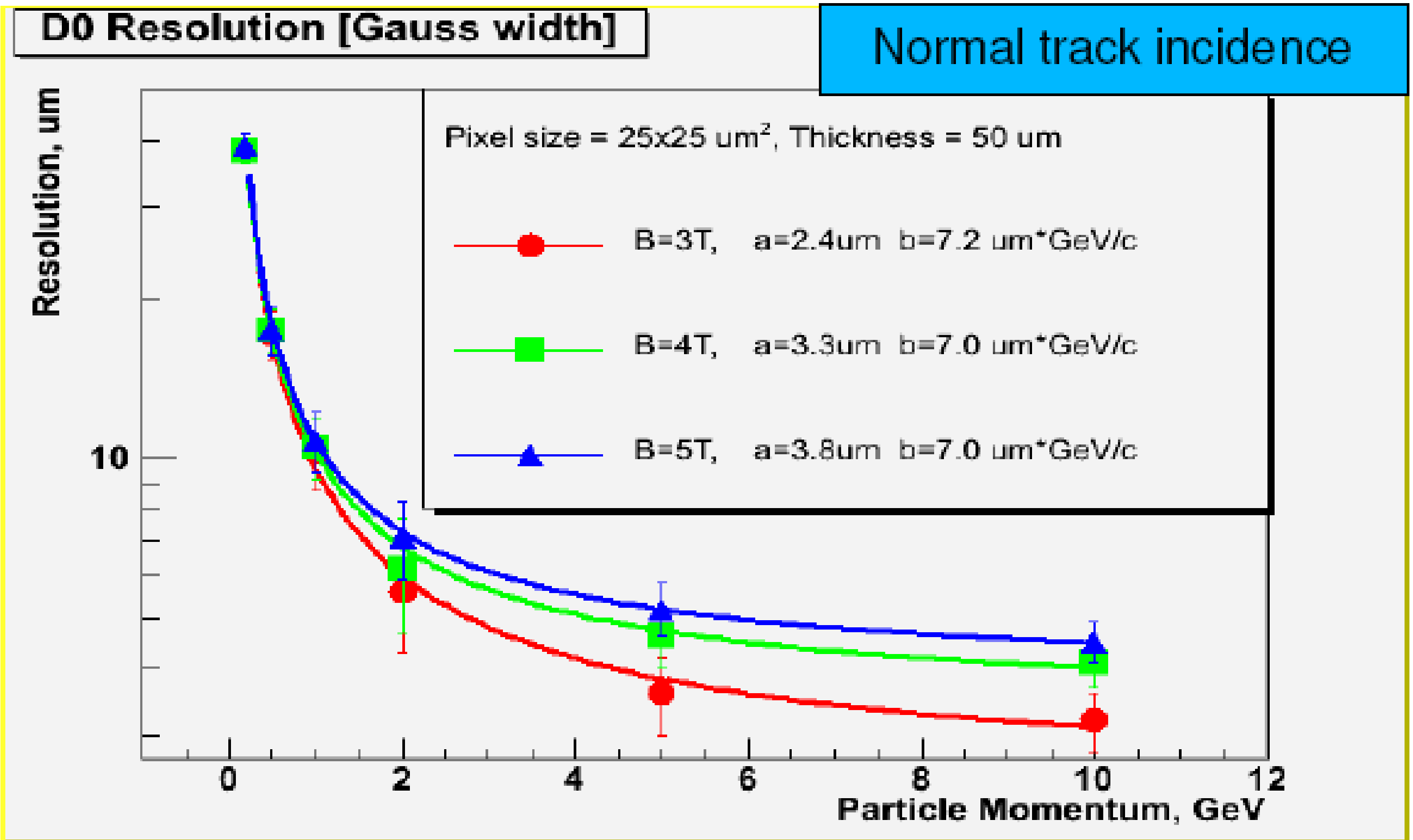

Required: 5 μm +² 10 μm/(p sin2/3Θ) (p in GeV/c)

a < 5 μm   b < 10 μm

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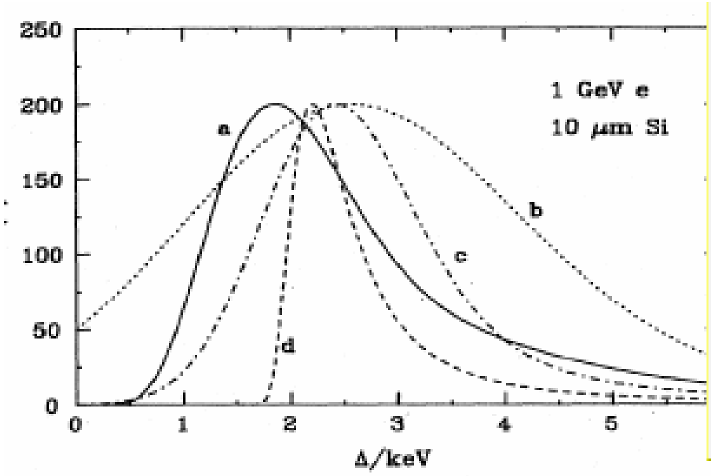
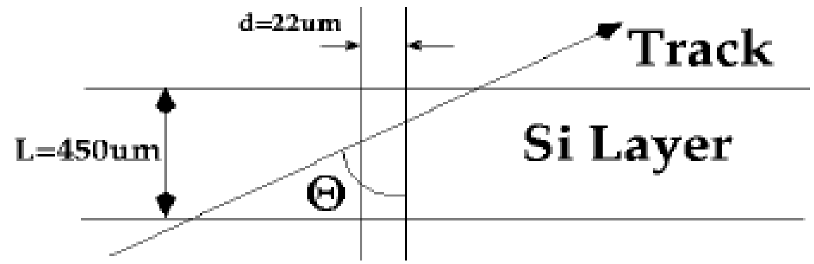
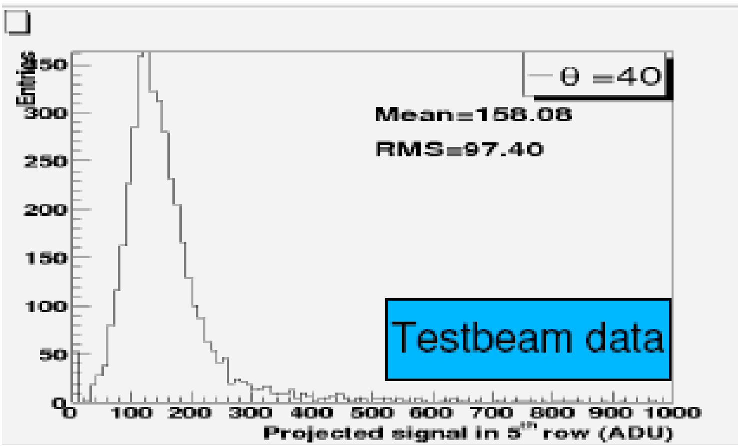
GEANT4 for thin Si-Layers

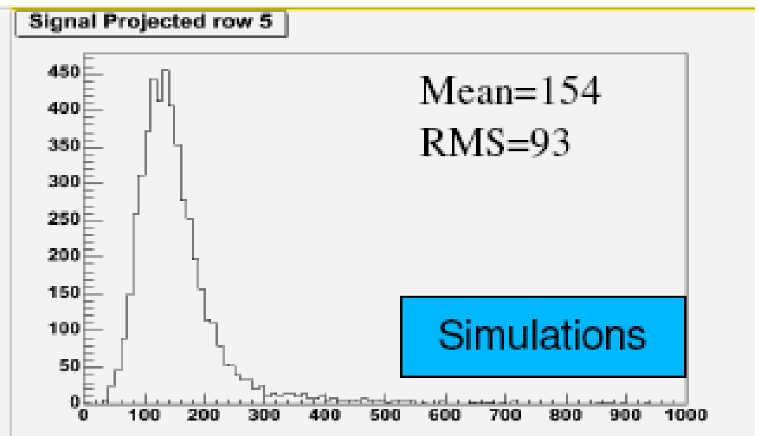


H.Bichsel Rev. Modern Physics 60-3 (1998)



Probe layer thickness of ~ 30 μm using inclined tracks





Very good agreement of GEANT4 simulations and testbeam data

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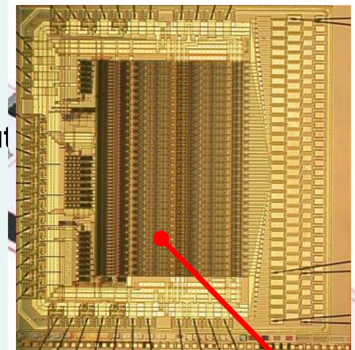
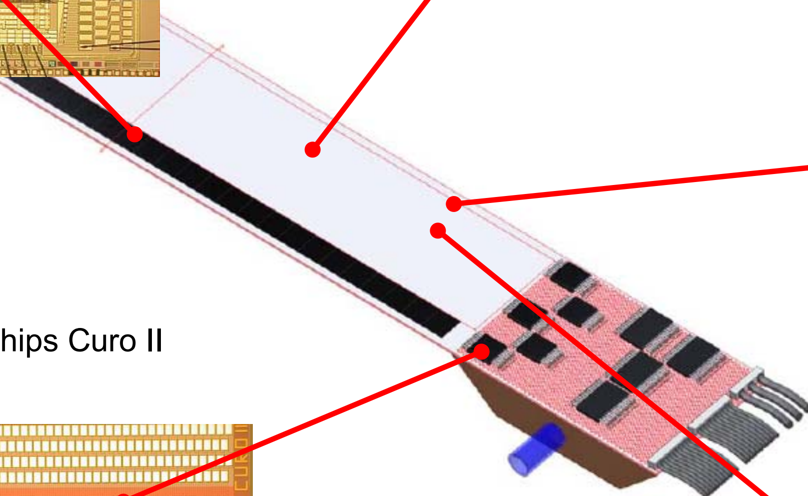
Munich

Project Status - in Summary

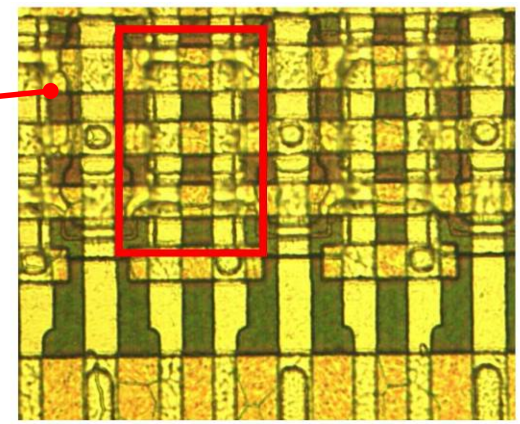
✓ steering chips Switcher II



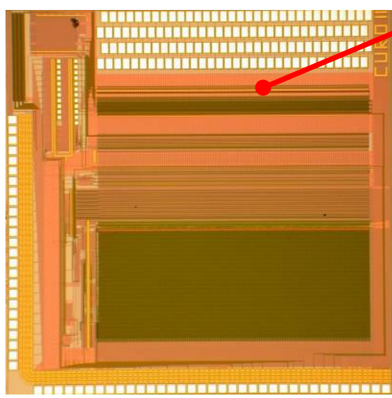
✓ thinning technology

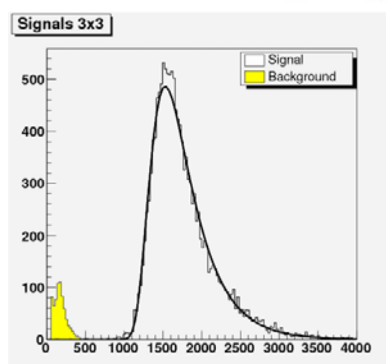


✓ double metal/double poly technology

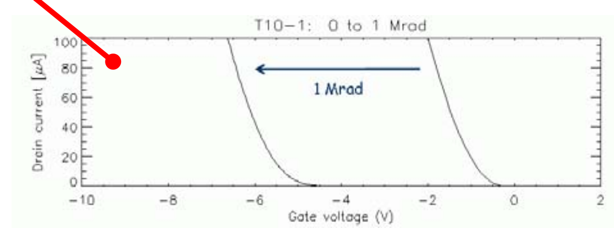


✓ r/o chips Curo II





✓ tolerance against ion. radition



✓ beam test

Research
techniques
seminar
Fermilab
June 6 2006

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Munich

Conclusions

- DEPFET technology established (double metal/double poly)
- Low intrinsic noise and complete clear demonstrated
- Thinning technology established
- Radiation tolerance up to 1 Mrad demonstrated
- Readout and control ASICs developed and produced
- Successful operation in beam test

Advantages for ILC Operation:

- Signal generation and collection in depleted bulk
  - large and fast signal
- First amplification step integrated
  - low noise
- RAM addressing of pixels (no charge transfer)
  - fast readout, radiation tolerant
- Power dissipation only during readout cycle
  - low power
- Wafer scale arrays (6”) possible
  - simple modules, less material
- Inhouse development & fabrication
  - complete control of design & technology

Next Steps

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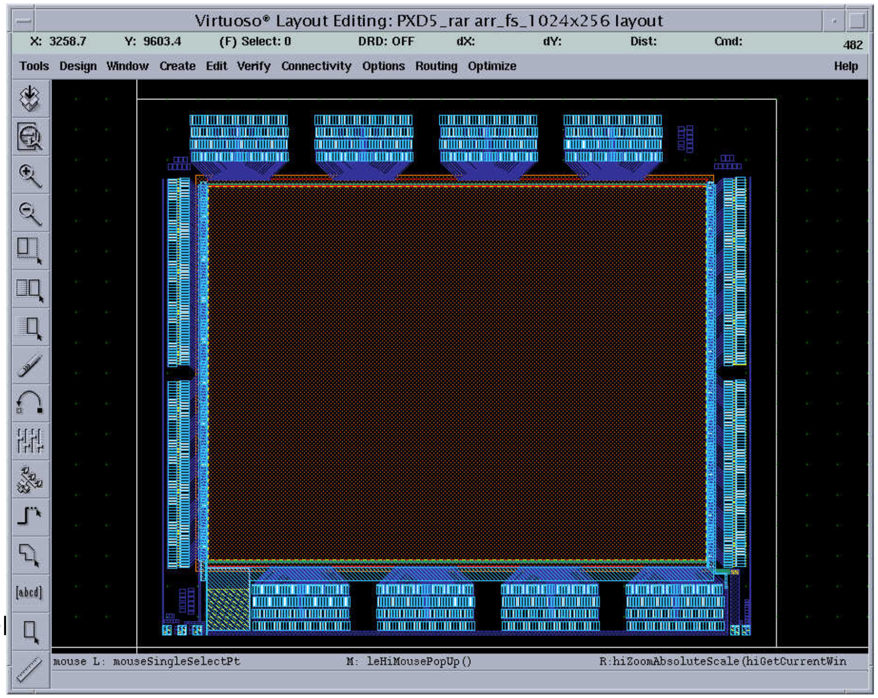
New DEPFET production (larger matrices), in production
New CURO (more features, better matching to g_q)
Rad-hard Switcher

512 x 512 matrix
pixel size: 32 x 24 µm²
array size: 16.38 x 12.29 mm²
chip size: 21 x 20 mm²

Also: 128 x 2048 matrix
pixel size (24 µm)²
5 cm length



Open for new "collaborators"

- **No MOU**
- **No spokesperson/project manager**
- **No steering committee**
- **A lot of work to do**

If you are interested to work with DEPFETs, contact us

- **http://www.depfet.org**

The competitors.... See https://wiki.lepp.cornell.edu/wws/bin/view/Projects/VtxProjects

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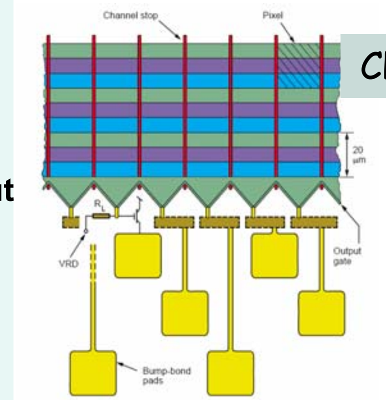
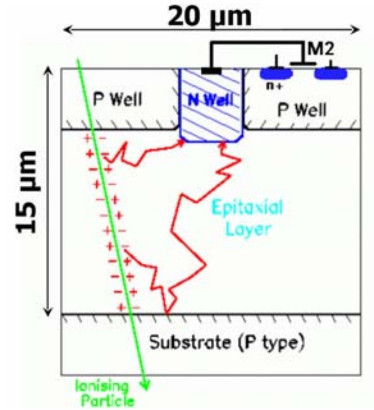
CP-CCD

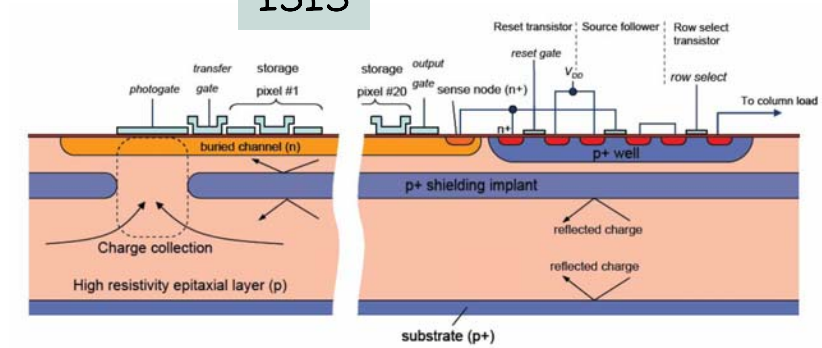


charge coll. in epi. layer

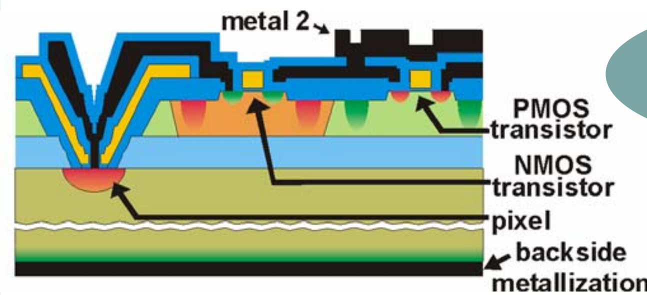
CMOS MAPS in various "flavours"



ISIS

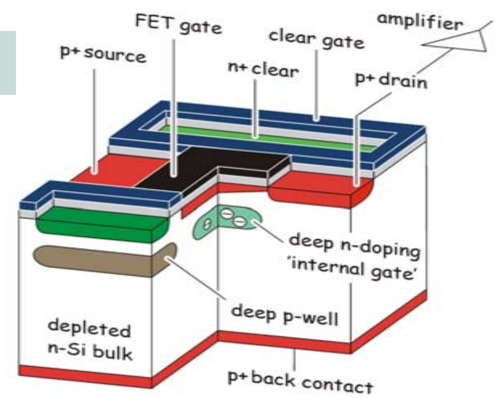


SOI Sensors



charge coll. in fully depl. bulk

DEPFET



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Alternatives/Competitors

Hybrid Pixels: Pixel detector with bump-bonded electronics (e.g. ATLAS/CMS pixels):

problems: power and material!

CCDs: used very successfully in SLD

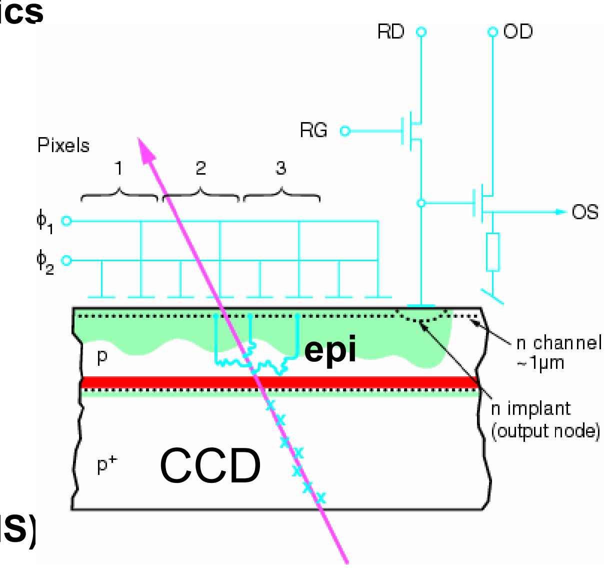
problems: power, speed

=> continuous shifting

=> time distance relation

=> radiation hardness (transfer efficiency)

promising concept: internal storage pixels (ISIS)



MAPS: Monolithic Active Pixel Senors:

intergrated CMOS electronics

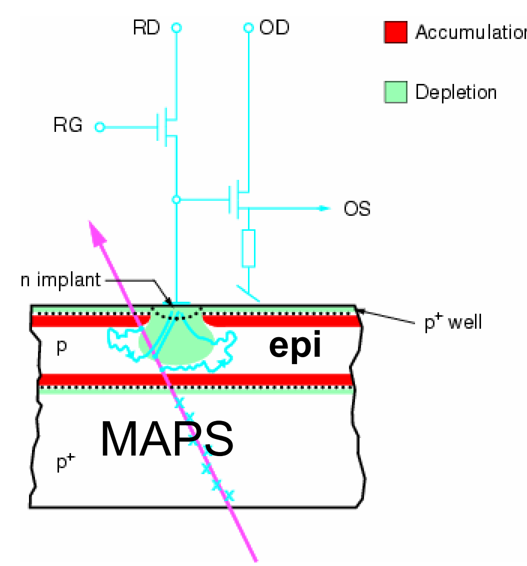
uses "standard" CMOS:

complex signal processing possible (0-suppression, pipeline)

problems: speed, cross-talk, power

CMOS process: small, slow and diffusing signal from thin (~15 µm) partially depleted epi-layer

Small sensor chips (yield problem), recticles



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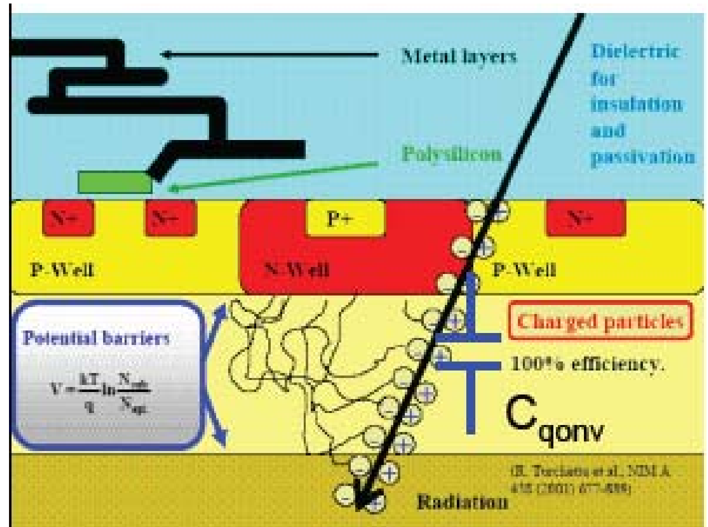
Alternatives/Competitors: MAPS

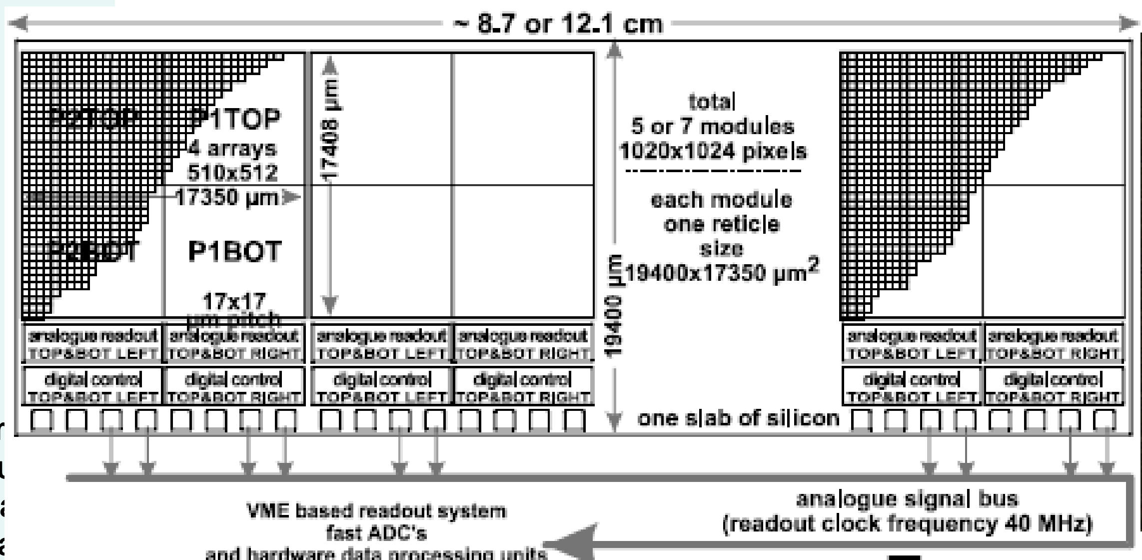
N-well used for signal collection
Only p-well possible for processing

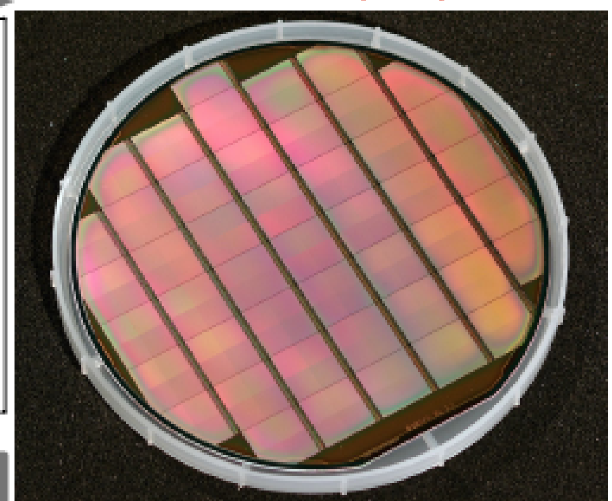
N- & p-well only in periphery

Successful prototypes
S/N: 20/1
Resolution < 2 μm
However: signal distributed over many pixels

Speed: not yet to LHC specs (inner layer)
Power: ?????







TRANSVERSE LADDER READOUT

Alternatives/Competitors: CCD

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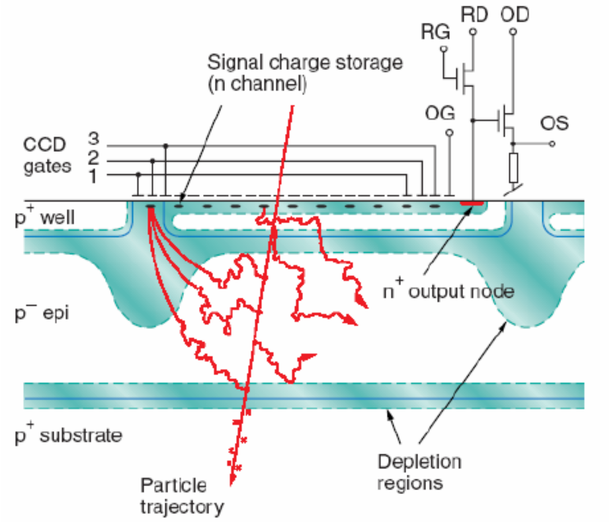
CCDs with double column parallel reaout
25 MHz with 1.9 V !!!
Noise: 60 e-

Radiation damage?
Wafer scale devices?

New concept: ISIS CCDs

In situ storage of ~ 20 “events”
Exists for high speed optical cameras

Immune to noise pickup from beam (SLD lession)



Why *whisper* just when an express train roars through the station?
(Chris Demerell)

An (un)biased comparisson....

	Resolution 5µm	Material budget ≤ 0.1% X_0	r/o speed 50µs/frame	Power consumpt.	Rad. tolerance γ, n	Remarks
CP-CCD	4.2µm + + (expectation)	+ R&D, comp. Ladder	25MHz done + R&D	V_{clk}≈2V + R&D	- (n) low T op.	rad. tolerance may be the limiting factor
CMOS MAPS	2µm +++ But at high speed?	+ R&D, comp. Ladder	R&D !	+	+ γ,n but with non std. techno.	large devices? d_{epi}?
SOI Sensors	No clear concept for the ILC. Feasibility shown, looking for industrial partners to continue.					
DEPFET	Like CCD + + (expectation)	+ R&D, all-silicon module	+ all comp. Ok, system test? R&D!	+ +	γ: + n: ?, but expect Ok!	no show stoppers so far.... ☺
HAPS (ATLAS&CMS)	7µm (-)	- -	+ +	- -	+ +	Backup solution