Implementation of Active Sonar Signal Detection Algorithms On Reconfigurable Computing Platforms Using Integer Fourier Transform Techniques

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Abstract

To maintain dominance in maritime sensing, there is a continuing need to develop innovative approaches for near real-time remote detection of underwater threats and targets. The Office of Naval Research (ONR) focuses its Science and Technology (S&T) programs in the areas of Battlespace Environment (BSE), Anti-Submarine Warfare (ASW), and Mine Warfare (MIW). This project investigates the detection, localization, and classification of underwater targets using Matched Filter (MF) active sonar signal processing techniques via Integer Fourier Transform (IntFFT). MF is central to sonar signal processing. The output of the MF gives a measure of how well the hypothesized signal matches the received signal as functions of a set of parameters, usually the range and velocity of targets. The focus of this research effort is to demonstrate the use of integer FFT to carry out key computations for active sonar processing used for underwater echo-location, namely MF bank implementations for broadband transmit waveforms. MatLab is used for code development, and Simulink model is developed for each project element.

Background

- Echolocation is used for tactical operations
- Matched filter is at the heart of sonar signal processing
- FFT mines frequency information from noisy signals
- Decision theory is used in complex scenarios
- Integer arithmetic reduces computational load

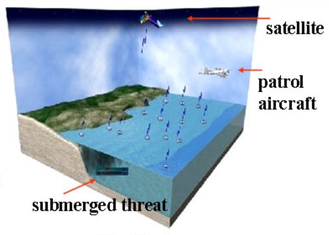
Research Objectives

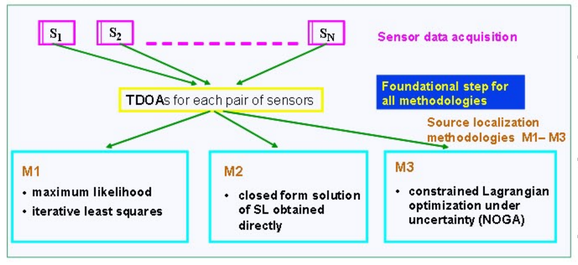
- Implement Matched Filter (MF) for underwater target identification and tracking
- Simulate hypothesized scenario involving multiple sensors
  - Sensors collect time delayed signals echoing from targets underwater
- Implement Cooley-Tukey FFT in Simulink using Integer arithmetic for complex number multiplications (CT IntFFT)
- Run simulation, collect, and analyze data
- Implement algorithms on FPGA

Motivations

- Simulated network of sensors observing same signal with varying time delay of arrival (TDOA) are used to characterize target position and motion
- Correlation is a subtractive operation that estimates time delay of arrival of two signals
- Correlation operation can be carried out in the time domain
  - Process is usually performed in frequency domain for real time analysis

- Sensor matrix composed of randomly placed Sonobuoys
- Sonobouys - passive omni-directional sensors collecting data from underwater
  - Provide sound pressure measurements
  - Provide signal derived from targets
- Self-localizing Sonobuoys field offers unique mode of underwater target detection
  - Deployment flexibility, signal acquisition speed, focused ranging and capability for Netcentric information fusion





- Multiple sensors collect attenuated signal containing noise or interference
- Signal acquired in time domain
  - FFT converts to frequency domain
- Inverse FFT of cross power spectrum gives cross correlation
- Cross Correlation gives time delay of arrival (TDOA) estimate

$$1^{st}\ Sensor: x(t) = s(t) + n_1(t)$$

$$2^{nd}\ Sensor: y(t) = \alpha s(t+\tau) + n_2(t)$$

$$MF\ Output\ R_{xy}(\tau) = E[x(t)y(t-\tau)] \qquad \hat{R}_{x,y}(\tau) = \int_{-\infty}^{\infty} \hat{G}_{x,y}(f)\exp^{j2\pi f\tau}\,df$$

$$\hat{R}_{x,y}(t) = \frac{1}{T-\tau}\int x(t)y(t-\tau)dt$$

A. Cooley-Tukey IntFFT

- Fourier Transform (FT) converts of continuous time signal from time domain to frequency domain
- Discrete Time Fourier Transform (DTFT) - FT for discrete time signals
  - Function of continuous frequencies
- Discrete Fourier Transform (DFT) - similar to DTFT
  - Discrete representation of the frequency content of the signal
- Fast Fourier Transform (FFT) - family of fast algorithms to compute the DFT
  - Most take roots from Cooley-Tukey FFT algorithm
- Cooley-Tukey algorithm outlines efficient algorithm
  - Minimizes number of operations required to compute DFT

$$X_{(m_2,m_1)} = \sum_{k_0=0}^{r-1}\sum_{k_1=0}^{N_1-1} x_{(k_1,k_0)} W_N^{(m_2 m_0 N_1 + k_1 m_0)}$$

$$= \sum_{k_0=0}^{r-1}\left[W_N^{(m_0 k_0)}\left\{\sum_{k_1=0}^{N_1-1} x_{(k_1,k_0)} W_{N_1}^{(m_2 k_1)}\right\}\right] W_N^{(m_2 m_0 N_1)}$$

$$= \sum_{k_0=0}^{r-1}\left[W_N^{(m_0 k_0)}\left\{\sum_{k_1=0}^{N_1-1} x_{(k_1,k_0)} W_{N_1}^{(m_2 k_1)}\right\}\right] W_r^{(m_0 k_0)}$$

Figure 1. CT FFT algorithm

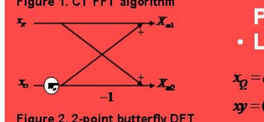


Figure 2. 2-point butterfly DFT

$$a^2 + b^2 = 1$$
$$x_Q = a_Q + jb_Q$$
$$|x_Q| \neq 1,\ for\ a, b < 1$$
$$\frac{1}{x_Q} = \frac{a_Q}{|x_Q|^2} - j\frac{b_Q}{|x_Q|^2}$$

Figure 3. Violation of PR OF DFT

$$x_Q = a_Q + jb_Q;\ y_Q = c_Q + jd_Q$$
$$xy = (ac - bd) + j(ad - bc)$$
$$= [1\ \ j]\begin{bmatrix} a & -b \\ b & a \end{bmatrix}\begin{bmatrix} c \\ d \end{bmatrix} = [1\ \ j]\,\Re\begin{bmatrix} c \\ d \end{bmatrix}$$
$$\Re = \begin{bmatrix} a & -b \\ b & a \end{bmatrix} = \begin{bmatrix} 1 & \frac{a-1}{b} \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 \\ b & 1 \end{bmatrix}\begin{bmatrix} 1 & \frac{a-1}{b} \\ 0 & 1 \end{bmatrix}$$

Figure 4. Lifting scheme For PR OF DFT

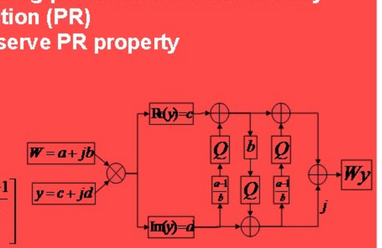


Figure 5. Data flow of Lifting scheme operation

- Computational requirement and power consumption can be high in embedded processing
  - Complex number multiplication use floating point arithmetic
- Integer FFT uses only integer arithmetic
- Quantization of floating point numbers can destroy Perfect Reconstruction (PR)
- Lifting scheme preserve PR property

B. Matched Filter

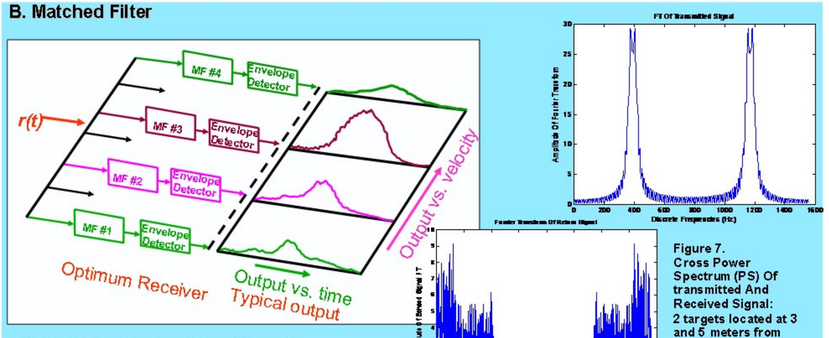


Figure 6. Schematics of a Matched Filter bank

Figure 7. Cross Power Spectrum (PS) Of transmitted And Received Signal: 2 targets located at 3 and 5 meters from source

- MF - bank of correlation filters
  - Each filter tuned to particular Doppler frequency
- MF - design maximizes signal to noise ratio of noisy signal
- MF - used in radar and underwater targets location and tracking

Reconfigurable Computing Via FPGA

- Emergence of high capacity reconfigurable devices ignited a revolution in general purpose processing
- Possible to tailor and dedicate functional units and interconnects to take advantage of application dependent dataflow
- Early research in this area of reconfigurable computing has shown encouraging results
  - 10-100X computational density and reduced latency over more conventional processor solutions
- FPGA is type of logic chip
  - Programmable Logic Device (PLD) is generally limited to hundreds of gated
  - FPGA supports thousands of gates

Xilinx ExtremDSP™ Hardware

- 500MHZ clocking multi-gigabit serial I/O
- 256 GMAC digital signal processing
- 450 MHZ PowerPC tm processors with H/W acceleration
- Highest logic integration
- 200,000 logic cells
- Reduced power consumption
- Achieved performance goals while staying within your power budget

Figure 8. Virtex 4 ExtremDSP™ Development Board

Power Consumption in FPGA

- Latest data shows Xilinx virtex-4 FPGA may consume less than 1/10th power of competing FPGAs
- Power consumption depends on application and FPGA floor planning
- Significant power reduction in virtex-4 is achieved through unique power-saving configuration circuitry and the use of 90nm triple-oxide technology
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- Power consumption advantage inherent to virtex-4 FPGAs reduce system power supply and cooling loads, improving long-term system reliability and lowering total system costs
- Power consumption estimation is complicated and depends on hardware design

Conclusion and Future Research

- Matched Filter was implemented
- Lifting scheme was used in combination of Cooley-Tukey algorithm to obtain integer FFT
- Hypothesized scenario was simulated with various target ranges and speeds
- Algorithm is being implemented on FPGA boards
- Computer and FPGA simulations results will be compared

Figure 9. Virtex 4 ExtremDSP™ Development Board In Lab

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