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In order to maintain dominance in maritime sensing, there is a continuing need to develop innovative approaches for near real-time remote detection of underwater threats and targets. The Office of Naval Research (ONR) focuses its Science and Technology (S&T) programs in the areas of Battlespace Environment (BSE), Anti-Submarine Warfare (ASW), and Mine Warfare (MIW). This project addresses the technical challenges put forth by ONR by investigating the detection, localization, and classification of underwater targets using Matched Filter (MF) active sonar signal processing techniques via integer Fourier Transform. MF is central to sonar signal processing. Fundamentally, the MF is a correlator, which compares the received signal with a hypothesized signal. The output of the matched filter gives a measure of how well the hypothesized signal matches the received signal as functions of a set of parameters, usually the range and velocity of targets. A matched filter isolates a signal in signal space as a space array isolates a direction in real space. Modern day sonar platforms employ a bank of matched filters, the i^{th} of which is tuned to a particular Doppler frequency.

The focus of this research effort is to demonstrate the use of integer FFT to carry out key computations for active sonar processing used for underwater echo-location, namely MF bank implementations for broadband transmit waveforms. This project also delineates physical implementation of this system for real-time deployment and integrated expansion on complex structures. Hardware implementation is done on reconfigurable computing platforms such as the Field Programmable Gate Array (FPGA) board. The Discrete Fourier Transform (DFT), one of the fundamental operations in digital signal processing (DSP) is a significant component of this project, and it is given special attention for hardware implementation. The Integer Fast Fourier Transform, or simply Integer FFT, algorithm is used to approximate the DFT. The Integer FFT lessens the computational complexity of the algorithm by using only bit shifting and additions and no multiplication, while allowing for a perfect reconstruction of the original signal. This elimination of multiplication in the DFT algorithm alleviates and provides for an adaptable power requirement of the hardware. Finally, simulation is conducted to test and collect data used in parameter characterization and signal analysis.

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