Analog-to-Digital Conversion Using Custom CMOS Analog Memory for the EOS Time Projection Chamber

K.L. Lee, A.A. Arthur, R.W. Jones, H.S. Matis, M. Nakamura,
S.A. Kleinfelder, H.G. Ritter and H.H. Wieman

Lawrence Berkeley Laboratory
University of California
Berkeley, CA 94720

Abstract

The multiplexing scheme of custom CMOS analog memory integrated circuits, 16 channels x 256 cells, into analog to digital converters (ADC's) to handle 15,360 signal channels of a time projection chamber detector system is described. Primary requirements of this system are high density, low power and large dynamic range. The analog memory device multiplexing scheme was designed to digitize the information stored in the memory cells. The digitization time of the ADC's and the settling times for the memory unit were carefully interleaved to optimize the performance and timing during the multiplexing operation. This kept the total number of ADC's, a costly and power consuming component, to an acceptable minimum.

I. INTRODUCTION

There are 15,360 signal channels in the Equation of State (EOS) time projection chamber (TPC) detector [1]. To minimize the large number of cables which might otherwise be required, multiplexing and digitization is performed directly on the detector before sending information elsewhere for further processing. Low power, high density front end electronics were designed to meet the cooling and space requirements. The switched capacitor array (SCA) analog memory integrated circuit helped meet these objectives. The SCA is described in reference 2. This paper describes the SCA operation and multiplexing scheme employed to meet our design goals.

II. SCA TIMING OPERATION

A simplified block diagram Fig. 1 shows 1 of 16 memory banks driven by common internal logic circuits. There are three phases of operation for each data acquisition cycle: 1) initialization, 2) write, and 3) read. Figs. 2(a) and (b) shows a simplified timing diagram for one acquisition cycle.

A. Initialization

Dynamic shift registers are used as pointers to select individual memory cells in the SCA, but they do not retain their pointing capabilities except for a short time. Due to the nature of dynamic shift registers, keeping the capacitor memories in the shift register in a known state while waiting for an event trigger requires "zipping", a 300 ns operation which turns on all switches to all memory cells. Zipping is accomplished by holding both Clk-1 and Clk-2 high while holding the shift register data input high. All memory cell

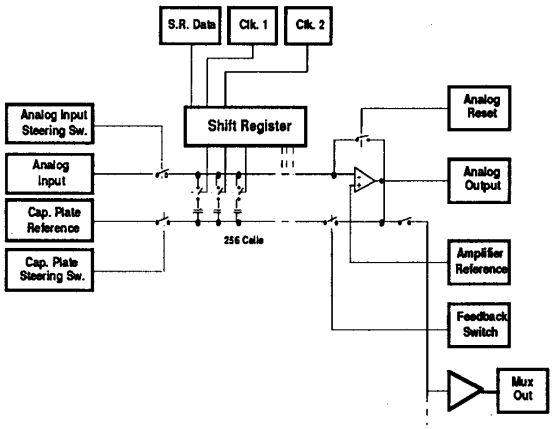


Fig. 1 Simplified SCA Circuit, one of 16 memory banks.

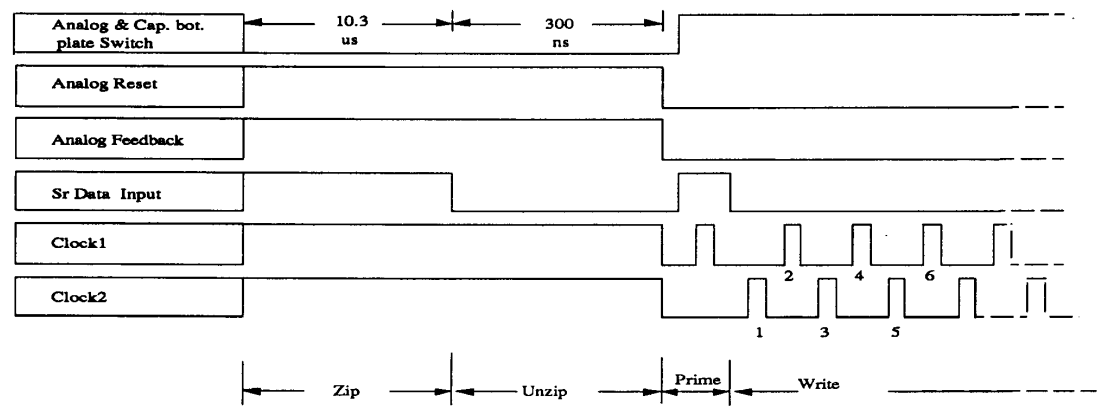
capacitors are then reset to zero by having turned on the analog reset and feedback switches. This requires an additional 10 μs for all capacitors to fully discharge. Thus, a 10.3 μs minimum holdoff time is required after an abort or a write cycle followed by a readout cycle. All during the above operation, the SCA analog input and capacitor bottom plate switches are opened.

B. Write

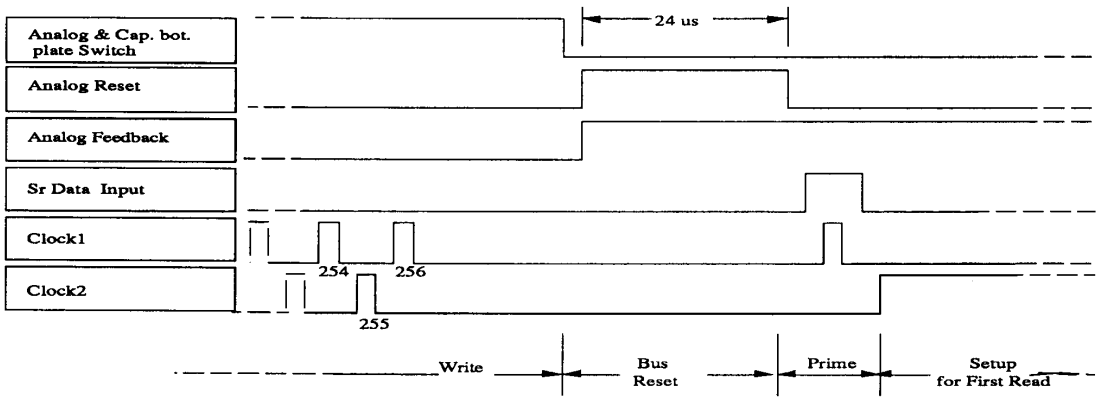
Upon the arrival of an event trigger, an "unzipping" period of 300 ns is required before the analog reset and analog feedback switches are opened prior to a write cycle. Unzipping restores all bits to "zero" state at all locations in the shift register. This is accomplished by holding both Clk-1 and Clk-2 high while holding the shift register data input low.

The analog input and capacitor bottom plate switches are then closed. A "prime" bit which brackets the Clk-1 pulse loads the dynamic shift register with a "one" in the first bit in the shift register. Set-up and hold requirements must be observed. The first cell is written into on the following Clk-2 pulse.

An additional 128 pulses for both Clk-1 and Clk-2 are required during write to run the prime bit off the end of the shift register after the prime bit is introduced. Clk-1 and Clk-2 are interleaved to produce a total of 256 additional clock pulses.



(a) Initialization and Write



(b) Setup for first Read

Figs. 2 (a) and (b) Simplified SCA timing diagram(waveform timebase not drawn to scale)

This procedure is necessary to guarantee that no "ones" are left in the shift register or else two cells could be addressed simultaneously during readout which will give erroneous results.

C. Read

After writing in data, the analog input and capacitor bottom plate switches are opened. The analog reset switch on the SCA output op-amp of each individual channel is closed for a 24 μs period in order to insure that the op-amp output is driven to a known voltage, i.e. Vref. This minimizes the possibility of a negatively charged capacitor from being driven into the substrate. The feedback switch can now be closed and the analog reset switch opened to start the readout cycle. A "prime" bit which brackets the Clk-1 pulse is loaded into the shift register to initiate a pointer to commutate each memory cell to the output amplifier.

After each cell is read, the analog reset switch is turned on to discharge the capacitor and restore the common analog input line to the reference voltage. Clk-1 and Clk-2 continue to toggle until all memory is read.

III. 60 CHANNEL MULTIPLEX MODULE

The simplified block diagram in Fig. 3 shows a basic 60 channel multiplex module consisting of four SCAs each buffered by an output amplifier, a sample and hold circuit, and a 12 bit ADC, an AD671. Only 15 of the 16 available analog channels are used from each SCA, making a total of 60 channels per module.

There are 256 identical modules in the system all logically driven in parallel. Simplified timing diagram of a 60 channel multiplex module is shown in Fig. 4.

A general description of the multiplexing sequence as used in the EOS TPC system is as follows.

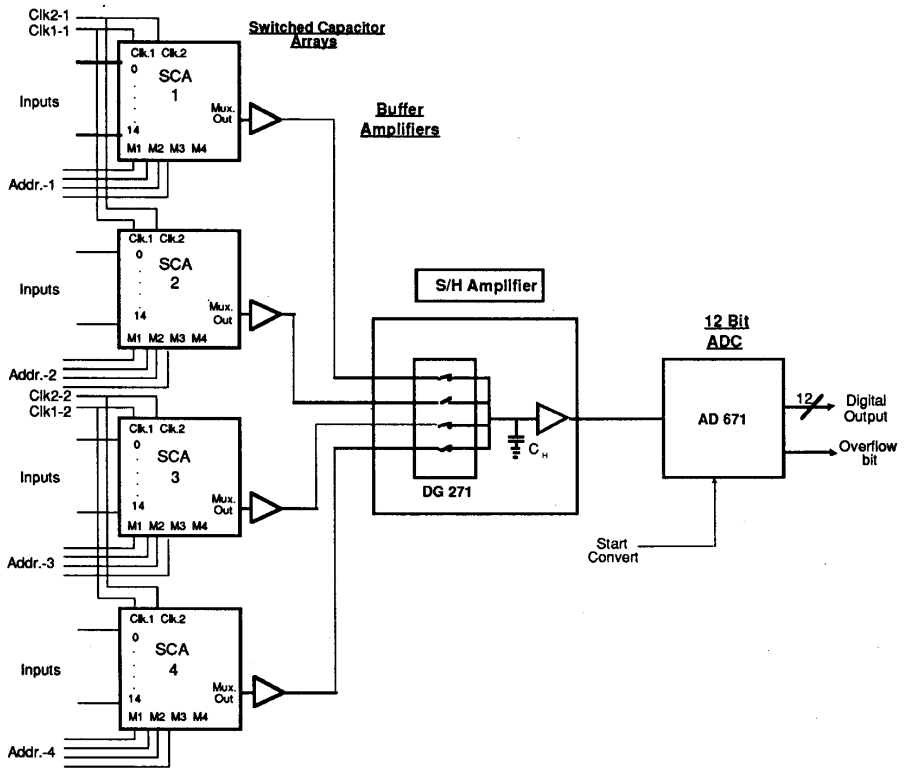


Fig. 3 Simplified block diagram of a 60 channel SCA multiplex module.

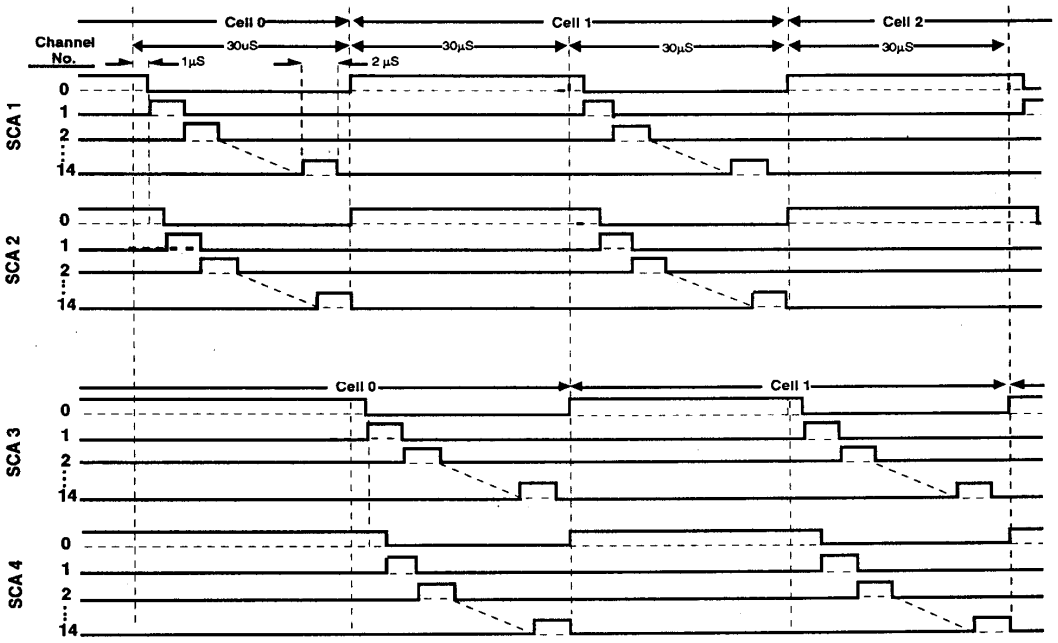


Fig. 4 Simplified timing diagram of a 60 channel SCA multiplex module.

SCA1 and SCA2 are alternately sampled in 1 μs periods until all 15 channels of each SCA have been digitized. This operation takes 30 μs. Multiplexing is then performed on SCA3 and SCA4 in the same manner. In the same time frame that SCA3 and SCA4 are sampled and digitized, SCA1 and SCA2 shift new analog data to their respective outputs. This overlapping process allows 30 μs for the individual SCA output amplifiers to settle before their next sampling. Toggling between pairs of SCAs continues until all of the memory cells have been processed.

Figure 5 shows in detail the circuit of an SCA output buffer amplifier. The AD843 op-amp provides a voltage gain of 2.8 with low impedance drive to the sample and hold switch, and compensation for SCA output offset. LT1029 provides a high stability voltage reference source to the input buffer amplifier and the associated SCA.

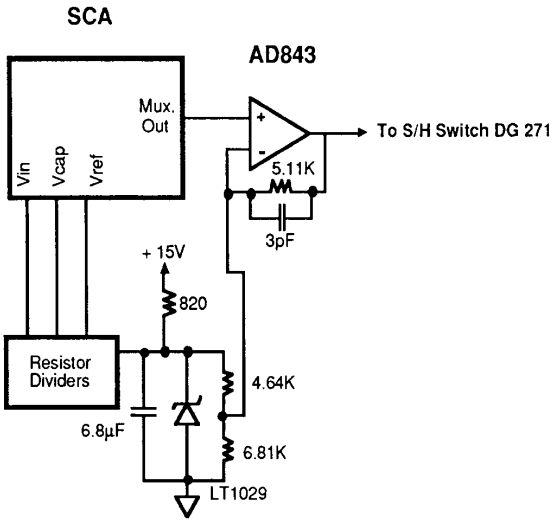


Fig. 5 SCA output buffer amplifier.

IV. PERFORMANCE RESULTS

An SCA test stand was constructed incorporating the multiplex ADC circuit design, and checked out successfully. Test measurements can be made accurately at the full 12 bit resolution of the ADC.

Digital data from the test stand is transmitted to a Macintosh computer via CAMAC interface. There, the raw data is stored in a permanent file and then processed for display or printed out. Table I gives the test results of the SCA ADC multiplex circuit.

The test stand was used to test newly packaged SCAs to select the approximately 1150 devices needed for the system. Critical parameters of each SCA are tested and resultant data stored for analysis at a later time.

Table I

SCA ADC Multiplex Test Results

Analog signal dynamic range	2800:1
Noise referred to SCA input	0.6 mV rms
Non-linearity	< 5%
Crosstalk @ 1 MHz sine wave	< 1%

IV. CONCLUSION

Operating at a signal sampling frequency of 10 MHz, performance results of the SCA multiplex ADC circuit met design objectives. The circuit does not introduce significant noise or signal distortion. The multiplex scheme achieved a conversion rate of 1 MHz per ADC for a total of 256 MHz system conversion rate.

VI. ACKNOWLEDGEMENTS

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VII. REFERENCES

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[2] S.A. Kleinfelder, "A 4096 Cell Switched Capacitor Analog Waveform Storage Integrated Circuit", IEEE Trans. Nucl. Sci., NS-37, No. 3, pp 1230-1236, June 1990.