

2008 R&D 100 Award Entry Form

The logo for xyce features the word "xyce" in a bold, blue, sans-serif font with a 3D effect. A white, curved swoosh element starts from the left, loops over the top of the 'x', and then curves down and to the right, ending near the 'e'. To the right of the 'e' is a small "TM" trademark symbol. Below the main logo, the text "PARALLEL ELECTRONIC SIMULATOR" is written in a smaller, white, sans-serif font. At the bottom of the logo area, the version number "4.0.2" is displayed in a large, white, sans-serif font.

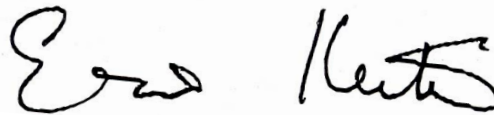
xyceTM
PARALLEL ELECTRONIC SIMULATOR
4.0.2

Submitting Organization

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AFFIRMATION: I affirm that all information submitted as a part of, or supplemental to, this entry is a fair and accurate representation of this product.



Eric R. Keiter

Joint Entry

No

Product Name

Xyce™ 4.0.2.

Brief Description

Xyce 4.0.2 is a massively parallel analog circuit simulator. While designed to be compatible with existing commercial circuit simulators, it has been designed from the ground up to be distributed-memory parallel.

**Date When First Marketed
or Available**

Xyce became available from Sandia in 2007 on a case-by-case basis for commercial and research licenses. Additionally, Xyce will be part of a commercial electronic design automation (EDA) product in the coming year. Fastrack Design, Inc (www.fastrack-design.com), San Jose, CA, has licensed the Xyce Parallel Electronic Simulator technology from Sandia National Laboratories. This transfer of the unique technologies within Xyce to the U.S. marketplace will benefit the domestic economy, and have a have large impact on the EDA industry.

Xyce™ 4.0.2

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Product Price

Xyce 4.0.2 is available for both research and commercial licenses. Fees are determined on a case-by-case basis.

Patents/Patents Pending

No



Xyce™ 4.0.2

Primary Function

Xyce, which has been under development at Sandia National Laboratories since 1999, is capable of accurately simulating circuits of millions of circuit elements on hundreds of processors.

What does Xyce™ 4.0.2 do?

Sandia National Laboratories' (Sandia) Xyce Parallel Circuit Simulator is the world's first massively parallel analog circuit simulator. Circuit simulation has been a major component of the electronics industry for over 30 years, and is the basis for the large electronic design automation (EDA) industry. Xyce, which has been under development at Sandia since 1999, is capable of accurately simulating circuits of millions of circuit elements on hundreds of processors. This unprecedented capability has transformed electrical design and analysis within Sandia. Primarily funded by the Department of Energy's Advanced Simulation and Computing (ASC), the mission for Xyce has been to help with nuclear weapon system design and qualification. With the elimination of underground nuclear testing and declining defense budgets, science-based stockpile stewardship requires increased reliance on high-performance modeling and simulation of weapon systems. Xyce's application in this context has been to help certify large electrical systems (including integrated circuits) in the presence of radiation and other hostile effects. Xyce will soon have a similar impact on the electronics industry, although the driver in industry will be integrated circuit (IC) feature size rather than radiation.

In 1965, Intel co-founder Gordon Moore made the observation that the number of transistors that can be inexpensively placed on an integrated circuit doubles approximately every two years. This trend has continued into the twenty-first century, and, as a result, there are modern, commercial integrated circuits consisting of over 100 million transistors. Correspondingly, the size of each transistor in such circuits has shrunk dramatically. Modern technologies now make use of transistors that are as small as 45 nanometers. Important physical effects, such as parasitic resistance and capacitance in transistors and electrical interconnects, were easily manageable for larger transistors but have become much more challenging in the nanometer regime.

As IC feature sizes shrink (<90 nm technology), the relationship between IC design and IC manufacturing has fundamentally changed. For newer technologies, it has been increasingly difficult to implement the intended IC design and achieve good product yield because designs

Xyce™ 4.0.2

Primary Function

Xyce has been completely redesigned and is a unique capability. By doing a complete redesign, it was possible to create a code that is parallel in the most general sense, relying on a message-passing implementation that allows it to run efficiently on the largest possible number of computing platforms, including serial, shared-memory, and distributed-memory.

can no longer be adequately verified using traditional digital simulation technologies. Instead, more accurate analog circuit simulation methods (i.e., SPICE¹) have to be used. However, most commercial ICs are too large to be simulated via traditional circuit simulators, as commercial (SPICE-based) simulators are serial-only and rely on direct solvers for their linear solution. As a result, commercial circuit simulators scale very poorly beyond 100K unknowns. Generally, the number of unknowns required for a circuit simulation is in the same ballpark as the number of unique components of a circuit. For example, a two-million transistor circuit will generally require the solution of approximately two million independent variables. Circuits of this size are well beyond the capability of direct solvers, and, as a result, well beyond the capability of traditional SPICE-based circuits. Thus, there exists a strong need for a "SPICE-accurate" simulation capability that can also scale to millions of devices. The Xyce circuit simulator has the key solver and parallel technology to help fill this gap.

Xyce is similar to SPICE in that it is an analog circuit simulator, and solves the same basic set of Kirchoff law equations. Additionally, it is compatible with most SPICE-based simulators in that it supports the same device (physics) models as well as the same style of input deck. However, Xyce has been completely redesigned and is a unique capability. By doing a complete redesign, it was possible to create a code that is parallel in the most general sense, relying on a message-passing implementation that allows it to run efficiently on the largest possible number of computing platforms, including serial, shared-memory, and distributed-memory. Examples of these platforms include exotic platforms, such as Sandia's NNSA/ASC RedStorm machine, which is a 12,000 node, 124 TeraFlop computer, and cluster-based machines such as Sandia's Thunderbird. Less exotic parallel platforms (e.g., Beowulf clusters), as well as common commercial desktop machines (e.g., Linux, OSX, and Windows) are supported as well.

Careful attention has been paid to the specific nature of circuit-simulation problems to ensure that optimal parallel efficiency is

¹ SPICE=Simulation Program with Integrated Circuit Emphasis. SPICE was originally developed at the University of California-Berkeley in the 1970s, and has been the basis for most commercial circuit simulators.

Primary Function

achieved as the number of processors grows. Parallel circuit simulation is particularly challenging, in part because circuit simulation can be described as a set of differential equations distributed over an arbitrary network. The network (or circuit) is arbitrary in that any component in a circuit schematic could, in theory, be connected to any other component. This makes a circuit-simulation problem very difficult to distribute in parallel, as there are fewer constraints on parallel communication costs. In contrast, mesh-based simulators (which comprise many of the massively parallel simulators in existence) can rely on a greater degree of data locality, thus keeping communication costs low.

Despite these challenges, Xyce has demonstrated scalable performance to circuits consisting of millions of devices and has been applied to a large number of "real" (i.e., non-ideal) engineering problems. To date these have primarily been ICs from the nuclear weapon community, but more recently have included technology circuits from the commercial world as well. Doing so required the development of new solver technologies, including the application of novel preconditioned iterative solvers, as well as new continuation methods for circuits and advanced time-integration technologies.

How does it do it?

The Xyce team has chosen to emphasize a modular development approach and in doing so has collaborated closely with the Trilinos solver group at Sandia National Laboratories. The Trilinos Project is an effort to develop algorithms and enabling technologies within an object-oriented software framework for the solution of large-scale, complex, multi-physics engineering and scientific problems. As such, the use of the Trilinos library has been crucial for Xyce development. The guidelines for Xyce development have been:

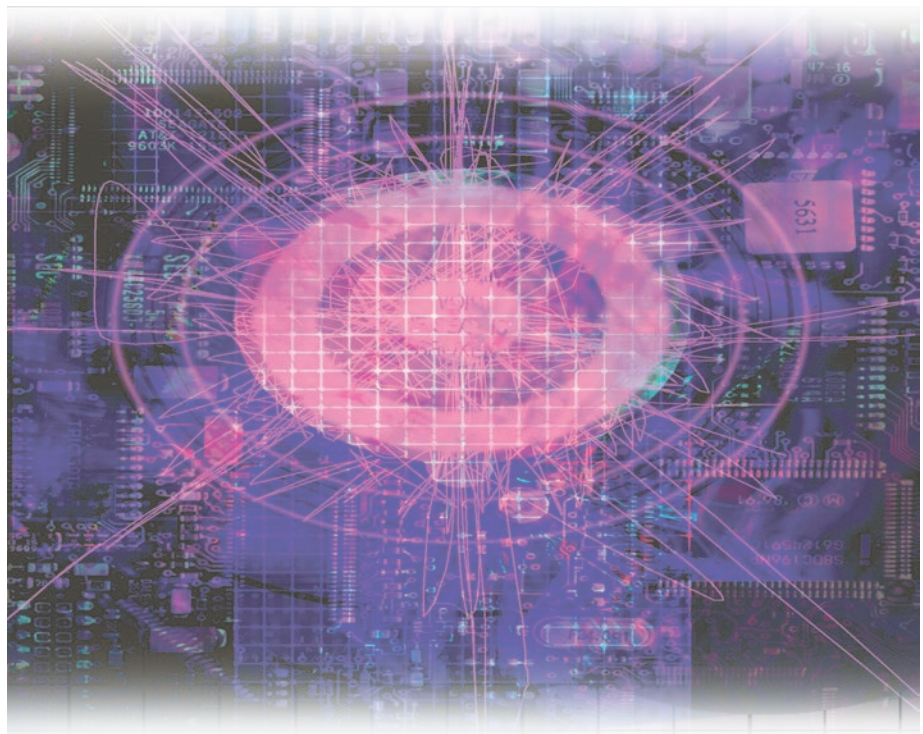
1. Compatibility with industry standard simulators. This includes input file (netlist) compatibility, as well as support for the full set of industry standard transistor models.
2. Modular, object-oriented C++ design.

Primary Function

Prior to Xyce's development, the conventional wisdom was that the circuit matrices were too poorly conditioned for iterative solvers to be of use. However, the Xyce project has demonstrated this conventional wisdom to be incorrect.

3. Designed "from-the-ground-up" to be distributed memory, message-passing (MPI-based) implementation. This is the most flexible parallel implementation possible, and allows Xyce to be ported to a wide variety of parallel platforms, from high-end supercomputers to relatively modest compute clusters.
4. Modern solver technologies, applied in a modular flexible manner. This allows Xyce to provide a variety of linear, nonlinear, continuation, and time-integration capabilities, which can be mixed and matched as appropriate to the problem.
5. Focus on preconditioned iterative linear solvers for circuit simulation.

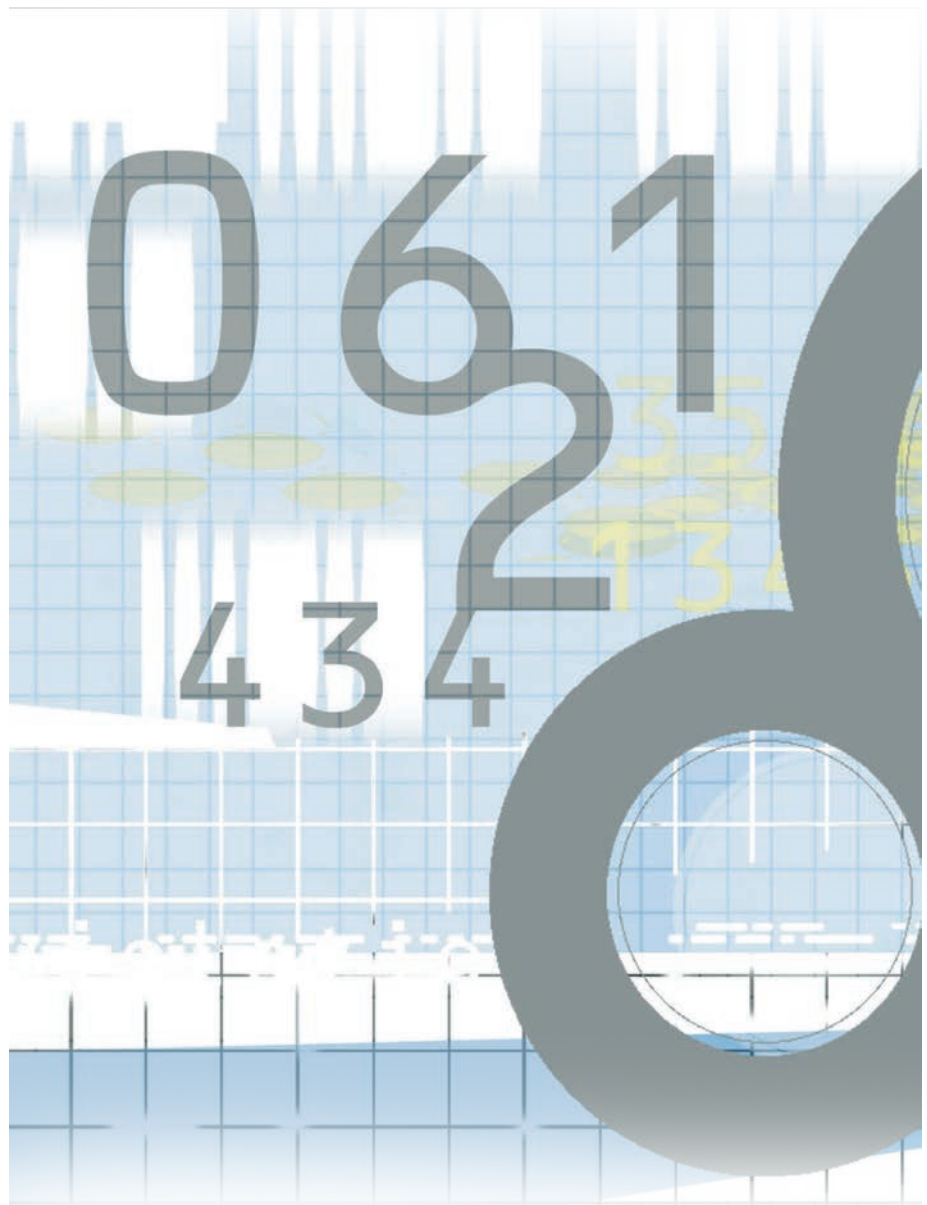
The application of iterative linear solvers to circuit simulation is a particularly differentiating feature of Xyce. Most circuit simulators rely entirely on direct (Gaussian elimination-based) matrix solvers. However, direct solvers typically perform poorly for larger problems, and have prohibitive communication costs for parallel simulation, so parallel simulators have always relied on iterative methods. Prior to Xyce's development, the conventional wisdom was that the circuit matrices were too poorly conditioned for iterative solvers to be of use. However, the Xyce project has demonstrated this conventional wisdom to be incorrect.



Xyce™ 4.0.2

Competition

The EDA industry is a very large and mature industry. According to the Gartner DataQuest EDA market analysis report, the SPICE simulation market is approximately \$370 million and expected to grow to about \$550 million in 2009. Not surprisingly, there are a large number of commercial as well as free circuit simulators. What follows in the Comparison Matrix is (by necessity) a partial list.



Comparison Matrix

Company	Product	Version	Language	Status	Parallel capability	Matrix solver	Capacity
Sandia National Labs	Xyce	4.0.2	C++	Commercial and research licenses	Distributed memory parallel (MPI)	Direct and iterative solver options	10-100 million unknowns
Cadence/Orcad	PSpice	9.1	C	Commercial	Serial only	Direct only	400,000 unknowns
Synopsys	HSpice	2007.09	C	Commercial	Serial only	Direct only	400,000 unknowns
Silvaco	SmartSpice	N/A	C	Commercial	Limited parallel, multi-threaded capability (not distributed memory)	Direct and iterative solver options	8 million unknowns
Berkeley	Spice	3f5	C	Open source (BSD License)	Serial only	Direct only	50,000 unknowns

Xyce Improvements over Competition

Primarily, Xyce is superior to its competitors due to its parallel implementation, and its resulting capacity for very large problem sizes. Currently, the industry has no similar capability in terms of problem size. Xyce's iterative matrix solver technology has been key to this improvement. The closest competitor is possibly SmartSpice, but its parallel implementation is limited to a multi-threading approach, and is much more limited than Xyce in terms of problem size. Xyce is the only circuit simulation tool that is capable of simulating full IC systems without resorting to simplifications that compromise accuracy.

Xyce has solved a number of circuits that are beyond the capability of any other circuit simulator. As early as 2003, Xyce was able to simulate successfully the largest analog circuit ever simulated [see Appendix items 1, 2]. Xyce solved a 14,336,000-device circuit problem using 1024 processors of Lawrence Livermore National Laboratory's Application Specific Integrated Circuit (ASIC) ASCI White IBM computer.

Also, beginning in 2003, Xyce was used to perform a parallel simulation of the Permafrost ASIC for the W76-1 weapon [see Appendix item 3]. This ASIC contained in excess of 200,000 MOSFET transistors, modeled by the BSIM3 MOSFET analog model. In addition to Xyce's parallel capability, this simulation also required the use of a new BSIM3-specific homotopy algorithm, a feature unique to Xyce among circuit simulation codes. This new algorithm was crucial in the ability to perform this calculation and is not available in any commercial simulator. Xyce has subsequently applied to similar ASIC circuits, up to (> 1 million) device ASICs, none of which can be simulated in any commercial tool.

Principal and Other Applications

The original impetus for Xyce was to provide an analysis and qualification tool for electrical circuits from nuclear weapon designs. To date this has been its principal application within Sandia. However, Xyce is designed to be 100 percent compatible with existing circuit simulators, and thus is applicable to a wide range of electrical circuit applications. These include, but are not limited to, memory circuit, ASICs, field-programmable gate arrays, RF digital, RF analog, and various system-on-a-chip applications. Circuit simulation is a key part of electrical design cycles and is used in both the pre-and post-layout stages. As noted, Xyce is unique in its capability to simulate very large (> 1 million device) circuits. This capability was critical for Xyce to be utilized to generate evidence used in the W76-1 qualification, which concluded in 2006. Furthermore, Xyce will be used in the analysis and qualification of future weapon systems.

In addition to traditional circuit simulation, Xyce has also been applied to a variety of non-circuit applications, most notably biological simulation as well as MEMS (microelectromechanical systems) simulation [see Appendix item 6]. Being a network simulator, it is theoretically capable of simulating any problem that can be represented as a system of ordinary differential equations distributed across an arbitrary network.



Xyce™ 4.0.2

Summary

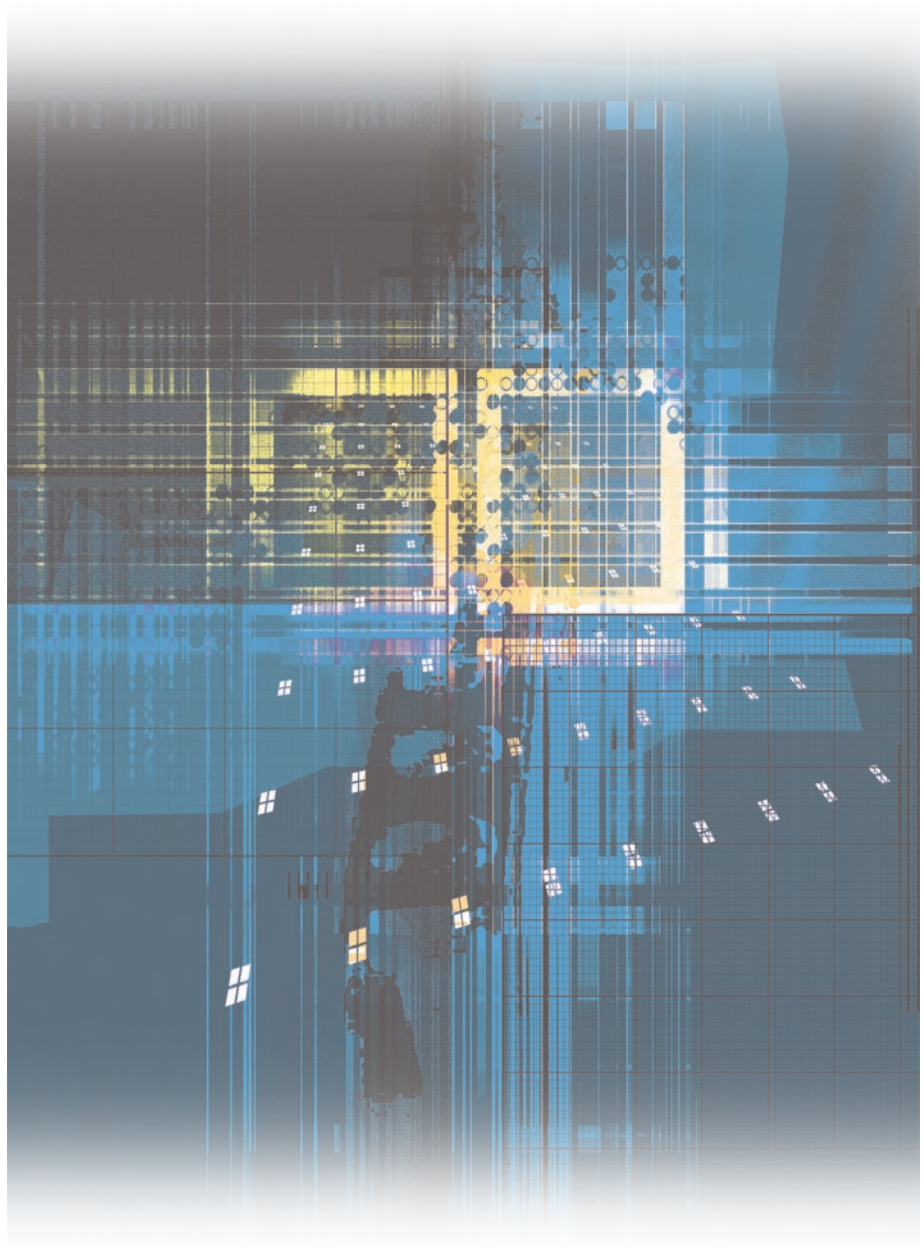
Despite the circuit simulation community being very mature and competitive, the Xyce circuit simulator is a unique and groundbreaking capability that is well-poised to meet the future needs of the electrical design world. As noted previously, the electronics industry is in a transition phase. Feature sizes have shrunk to a point where verifying designs via simulation is crucial yet much more difficult. Previous generations of IC have been verified and tested using digital and/or hierarchical simulation techniques and these are no longer adequate for modern feature sizes. Xyce is the only circuit simulation tool capable of simulating circuits in the >10 million device range and is thus uniquely positioned to impact this community. Xyce is able to accomplish this because of several unique features:

1. Efficient distribution and load balance of a network problem in parallel.
2. The effective use of preconditioned iterative solvers for circuits, which were previously thought to be impossible for circuits.
3. A truly parallel design based on message-passing implementation.

The design of Xyce has preceded industry trends, and as such will be in a position to uniquely impact the electrical design community. Xyce is the only truly parallel circuit simulator in the world because parallel circuit simulation is such a challenging problem.

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Appendices

1. "Sandia's Homegrown Xyce Software Gains Notice in World of Modeling Electrical Circuits," *Sandia Lab News*; June 13, 2003.
2. "Largest Full, Analog Circuit Ever Run," *Xyce News Note*; May 25, 2003.
3. "Xyce™ Parallel Simulation of the Permafrost ASIC," *ASIC Xyce News Note*; Oct.17, 2003.
4. "Fast Computation of Electrical Circuits: Speeding Up Charging Circuit Simulation," *MPDE Xyce News Note*; June 2004.
5. "Xyce™ Simulation of the Spock ASIC," *Xyce News Note*; May 10, 2004.
6. "New Xyce Capability Demonstrated: Integrated Electro-Mechanical System Simulation," *MEMS Xyce News Note*; May 31, 2006.

1. "Sandia's Homegrown Xyce Software Gains Notice in World of Modeling Electrical Circuits," *Sandia Lab News*; June 13, 2003.

EXCERPT

Sandia's homegrown Xyce software gains notice in world of modeling electrical circuits

Xyce ran the largest analog full circuit simulation ever in May experiment

By Chris Burroughs

Sandia's homegrown four-year-old Xyce™ software is gaining notice in the world of modeling electrical circuits.

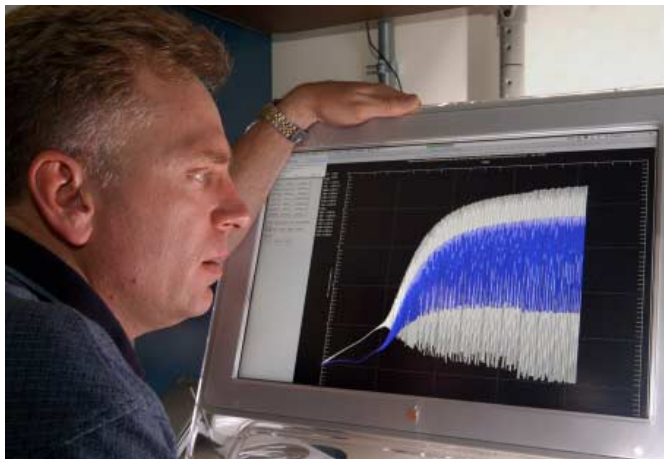
Late last month the electric circuit simulation code ran a 14,336,000-analog-device problem, using 1,024 processors of Lawrence Livermore's ASCI (Accelerated Strategic Computing Initiative) White IBM computer. It is believed to be the largest analog circuit simulation ever done, and it was conducted on the largest number of concurrent processors ever used for circuit simulation.

The accomplishment was part of a scaling study in support of an ASCI milestone, and the developers are convinced they can build a simulation code that can model even faster.

An interdisciplinary team from Depts. 9233, 8205, and 1734 began work on Xyce in July 1999 to develop an electrical modeling code that better meets Sandia's needs. Currently, Sandia's circuit simulation community relies mainly on a commercial code, PSpice (note the rhyming with Xyce), which operates sequentially, and hence, not as rapidly for large-scale circuit problems. Furthermore, Xyce gives Sandia the ability to simulate circuit problems of unprecedented size.

"We had our specific needs — like some of our device models have to support environmental effects [e.g., radiation], which no commercial cir-

(Continued on page 4)



SCOTT HUTCHINSON studies a computer simulation of a voltage waveform from an oscillator circuit. (Photo by Randy Montoya)

Happy birthday SSTP



Five years and 14 tenants after its first groundbreaking, Sandia Science and Technology Park, a unique public/private economic development initiative based just outside the Eubank gate in Albuquerque, celebrated its fifth anniversary. See story on page 5.

Tool to help Protective Force determine who may enter access points during off-hours

By Chris Burroughs

In the next few weeks a new tool will be provided to Sandia's Protective Force that will allow its members to better monitor who can and cannot enter certain restricted/controlled access points during weekends and off hours.

The ProForce will be able to look up a specific restricted/controlled access point through a computer access program, called Web-enabled Custodian-controlled Access Tool (WebCAT), and verify who is authorized inside the area.

"Right now, in most cases, if the ProForce receives a call to let someone in a controlled lab or into a Q-only hallway, for example, he or she doesn't know if the person is authorized to be there during off hours," says Janet Ahrens, Manager of Electronics Security Dept. 3112. "The ProForce will have to call the building or site manager to find out."

This situation has arisen because of the increased use of card readers throughout the Labs that allow only certain people in restricted/controlled access areas. Since 1996 more than 700 card readers have been installed at main access points to tech areas and in restricted points in buildings. Most of the time when a person swipes to enter a controlled area, he or she is admitted

(Continued on page 4)

Sandia Lab News

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Managed by Lockheed Martin for the National Nuclear Security Administration



Six-lab nuclear energy action plan has Sandia as systems integrator

Goal: Increase use of nuclear power, hydrogen fuels; reduce waste

By Will Keener

A joint presentation by six DOE laboratory directors in May to Deputy Secretary of Energy Kyle McLarlow has resulted in a step ahead for a Nuclear Energy action plan, proposed by the group. The plan calls for activities on the part of all six laboratories, with Sandia acting in an integrating capacity, reports Sandia President C. Paul Robinson.

"Basically, we found that we were pushing on an open door," says Paul of the meeting. "The Administration's Energy Plan already emphasizes nuclear energy (based on its competitive costs and zero carbon emissions) and the move to a hydrogen economy for transportation fuels. Our proposal integrates these two."

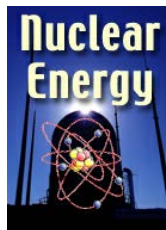
The action plan suggests an emphasis in some higher temperature reactors that can effi-

ciently produce hydrogen, Paul explains. "Thus we can speed the time to transition." McLarlow told the gathered group of laboratory representatives that the White House may also want to review the ideas in the action plan.

Last summer Sandia joined with Argonne, Idaho National Engineering and Environmental, Oak Ridge, Lawrence Livermore, and Los Alamos national laboratories in signing an agreement aimed at enabling nuclear power to play a global role in the 21st century. The action plan, which sets out specific dates and goals, is a product of that agreement.

"Sandia has offered to the rest of the labs our experience and expertise as 'system integrators' for this effort," Paul says. Each lab in the partnership has expertise in particular areas of nuclear technology that it will bring to the table, Paul adds, "but we thought that what was most

(Continued on page 6)



3 Truman lecture by WSJ reporter Carla Robbins touches upon US role and image overseas

6 Sandia, Kurchatov laboratory directors sign MOU to advance nuclear energy, related technologies

2. "Largest Full, Analog Circuit Ever Run," *Xyce News Note*; May 25, 2003.

EXCERPT

Xyce™ News Note

Xyce™ Parallel Electronic Simulator

News Note

Largest Full, Analog Circuit Ever Run*

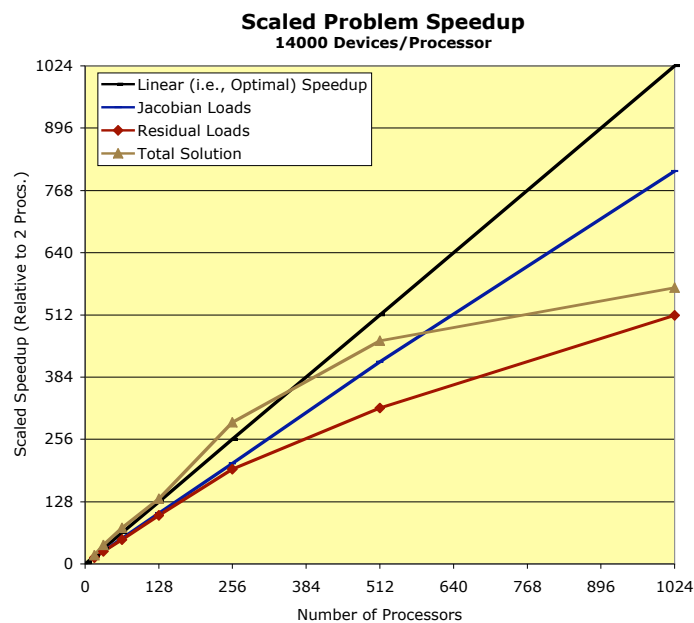


Figure 1. Scaled speedup for nonlinear transmission line problem. NOTE: the scaled-speedup numbers are with respect to two-processors, the smallest number used for the study. Also, the "Total Solution" scaling includes the effects of problem-dependent algorithmic scaling.

* To the best of the team's knowledge of the available literature.

On May 25th, 2003, the Xyce™ team at Sandia National Laboratories ran a 14,336,000 device circuit problem using 1024 processors of Lawrence Livermore's ASCI White IBM computer. To the best of the team's ability to determine, this is the largest full, analog circuit simulation ever run *and* it was run on the largest number of concurrent processors ever used for circuit simulation. This simulation resulted in a linear system of approximately 6,000,000 unknowns that were solved using Sandia's Trilinos solver toolkit (the AztecOO Krylov

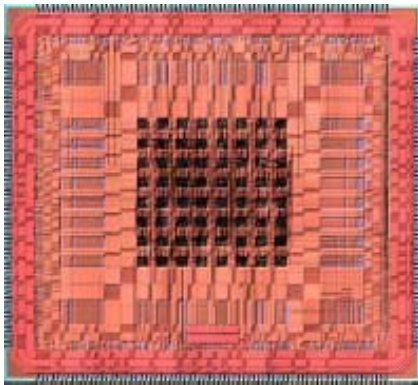
3. "Xyce™ Parallel Simulation of the Permafrost ASIC," *ASIC Xyce News Note*; Oct.17, 2003.

EXCERPT

Xyce™ News Note
10/17/03



Xyce™ Parallel Simulation of the Permafrost ASIC



On September 17th, 2003, the Xyce™ team at Sandia National Laboratories demonstrated the efficacy of its modern solution methods by performing a parallel simulation of the W76-1 Permafrost Application Specific Integrated Circuit (ASIC). This ASIC contained in excess of 200,000 MOSFET transistors, modeled by the BSIM3 MOSFET analog model. Notable in this simulation is the use of a new *homotopy* algorithm, provided by the NOX/LOCA library (part of the Trilinos solver suite) and a *homotopy-enabled* BSIM3 model - two new features unique to Xyce among circuit simulation codes - that were crucial in the ability to perform this calculation. This demonstrated capability is critical to the future

electrical modeling and simulation needs at Sandia where environmental effects on critical electrical components can now be simulated.

The ASIC device is a digital circuit which is key to understanding the difficulty associated with this calculation. As part of performing a transient simulation of this digital circuit, the initial conditions or the so-called *DC Operating Point* (DCOP) must first be determined. However, there are many potential "states" that the circuit may adopt for the DCOP and this non-uniqueness of the solution presents extreme difficulties for both the nonlinear and linear solution methods. In fact, it is often extremely difficult if not impossible to determine the DCOP for these circuits using conventional Newton-based approaches. Nevertheless, using the new homotopy approach dramatically transforms the DCOP calculation into a much more tractable problem allowing for the use of parallel Krylov iterative methods for the underlying

4. "Fast Computation of Electrical Circuits: Speeding Up Charging Circuit Simulation," *MPDE Xyce News Note*; June 2004.

Fast Computation of Electrical Circuits: Speeding Up Charging Circuit Simulations

Researchers at Sandia National Laboratories have achieved a 600 times speed up over a traditional simulation for a highly oscillatory charging circuit. This advance represents a big step forward in simulating highly oscillatory circuits. These circuits typically have relatively slow behavior mapped on to very fast oscillations which consequently require huge computational integration times to solve. Applications include: communication circuits, charging circuits, trigger circuits and oscillators. These circuits represent critical sub-components of more sophisticated systems, are often quite small in size, and yet take very long to simulate. Until now, advanced analysis of these circuits, e.g. optimization and sensitivity calculations, have not been possible due to the huge overhead in simulation.

Sandia researchers have applied new research ideas in Multiple-Time Partial Differential Equations (MPDE) to achieve these results. The main idea behind MPDE algorithms is to introduce two artificial time variables. The first variable represents the highly oscillatory behavior of the circuit and the second represents the relatively slow behavior. This decouples the different rates of change in the problem and allows for considerable savings in integration. This new approach not only provides substantial speed-up but also

allows for coarse design based simulations of these circuits, which were simply not possible before. This new algorithm is being implemented in **Xyce**, Sandia's large scale parallel circuit simulator, and will soon be available to designers.

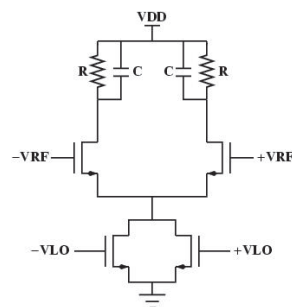


Figure 1: Balanced CMOS down-conversion mixer that was simulated for this speed-up comparison. The lower pair of MOSFETs generates a current that doubles the LO frequency and the upper pair forms a differential pair. The circuit implements multiplications of the RF and LO signals. The LO signal is a 450Mhz sinusoid modulated by a 2.5kHz sinusoid. The RF signal is a 900MHz carrier modulated by a bit-stream at 10kbps.

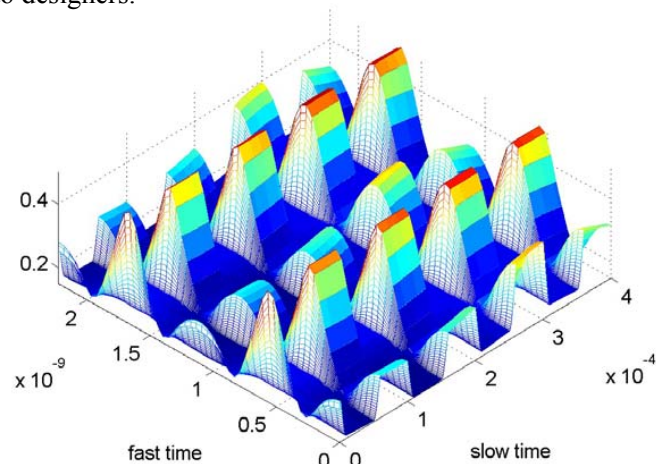


Figure 2: MPDE solution for the voltage at the drains of the upper MOSFETs.

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5. "Xyce™ Simulation of the Spock ASIC," Xyce News Note; May 10, 2004.

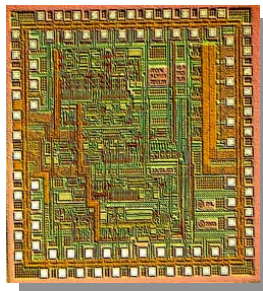
Xyce™ News Note

5/10/04



Xyce™ Simulation of the Spock ASIC

In November 2003, the Xyce™ (<http://www.cs.sandia.gov/Xyce>) team at Sandia National Laboratories further demonstrated the power of its modern solution methods



by performing a simulation of the W80-3 SA3989 (A.K.A. Spock) Firing-Set Application Specific Integrated Circuit (ASIC). The chip is being designed and manufactured by the MDL for the W80-3 Firing Set. This ASIC is a mixed-signal multi-function DC-to-DC power supply controller chip; it is comprised of approximately 4500 transistors; and is fabricated in the MDL CMOS6R radiation hardened process.

Steve Dunlap, the ASIC designer, used Xyce™ as a tool in his design and states that:

"Instrumental in the successful design of the SA3989 was the ability to conduct a pad-to-pad simulation of the part prior to manufacture, this insures that major design blocks internal to the ASIC interoperate correctly. Because of the analog components, size of the chip and its complexity the currently used design tools—PSPICE in particular—were not capable of performing this simulation. Attempts were made to run the pad-to-pad simulation on PSPICE, one simulation ran for 5 days on 550 MHz PC and only completed 30% before it failed. Interestingly, not only did the simulation fail to complete but upon examination of the data it was discovered that the simulation had produced erroneous output due to accumulated errors. Xyce™ was employed for the same purpose of performing a pad-to-pad simulation. Xyce™ required a great deal of custom "tweaking" but was able to complete the simulation, giving the designer greater confidence that the design would work as intended therefore reducing design cycles and consequently costs."

Appendix

6. "New Xyce Capability Demonstrated: Integrated Electro-Mechanical System Simulation," *MEMS Xyce News Note*; May 31, 2006.

EXCERPT

XYCENEWSNOTE

May 31, 2006

Xyce is a scalable, analog network (e.g., circuit) simulator developed by Sandia under ASC funding to support large-scale advanced circuit simulations and analysis for problems critical to Sandia's nuclear weapons mission.



New Xyce capability demonstrated: integrated electro-mechanical system simulation

Department 1437 - Electrical & Microsystems Modeling

Overview

In May 2006, the Xyce™ (<http://www.cs.sandia.gov/Xyce>) team at Sandia National Laboratories, led by Eric Keiter, further demonstrated the flexibility and power of the Xyce application code. Specifically, the team built upon the code's general integrated-network solution engine by incorporating a theoretical, yet realistic, compact-model of a Micro-Electro-Mechanical System (MEMS) switch into its model library and simulating its switching behavior as driven by a digital signal.

The demonstration switch model in Xyce, implemented by Richard Schiek, is based on a two-ODE (Ordinary Differential Equation) description

of a MEMS switch that is intended for demonstration purposes only and does not represent any MEMS device currently being designed or built by Sandia. Instead, this model and its integration within Xyce demonstrates a "proof-of-principle" that will show the way forward for further R&D for Xyce and the development of partnerships between Centers 1400 and 1700. Overall, the goal is to provide a systems-level simulation capability representing the integrated electro-mechanical behavior for design and analysis that will have a real impact on MEMS designs at Sandia for critical national security missions.

The Xyce code has been under development for several years as a key ASC application for modeling analog circuits at high levels of integration and in

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