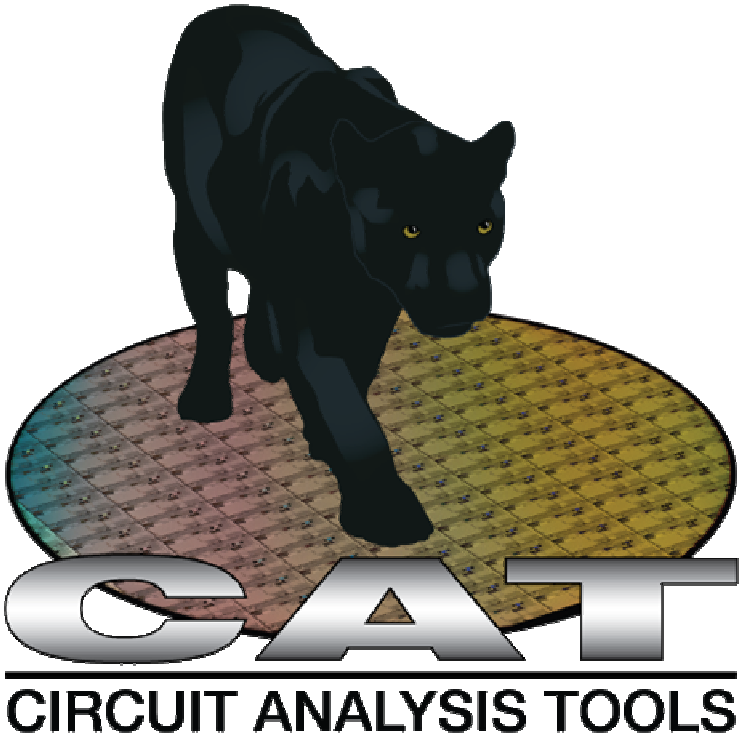
Welcome to the Circuit Analysis Tools Proposers' Day

8:30 – 8:35	Introductory Remarks	Dr. William Vanderlinde CAT Program Manager
08:35 – 9:00	IARPA Overview	Dr. Timothy Murphy IARPA Deputy Director
9:00 – 10:45	CAT Overview	Dr. William Vanderlinde CAT Program Manager
10:45 – 11:00	Contracting Overview	Dr. Dev Palmer ARO Contracting Officer's Representative
11:00 – 11:15	Break	
11:15 – 12:15	Proposers' Presentations	(Government not present)
12:15 – 12:30	Administrative Remarks	Dr. William Vanderlinde CAT Program Manager
12:30 – 1:45	Lunch Break – On your own (Gov't Representatives Depart)	
1:45 – 4:00	Posters and Teaming Discussions	



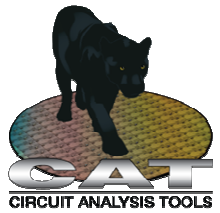
Circuit Analysis Tools (CAT) Proposers' Day
IARPA-BAA-09-09 Overview

Dr. William Vanderlinde

Program Manager

24 July 2009

Disclaimer



- This presentation is provided solely for information and planning purposes.
- The Proposers' Day Conference does not constitute a formal solicitation for proposals or proposal abstracts.
- Nothing said at Proposers' Day changes the requirements set forth in a BAA.
- Any conflict between what is said at Proposers' Day and what is in a BAA will be resolved in favor of the BAA.

Goals of Proposers' Day

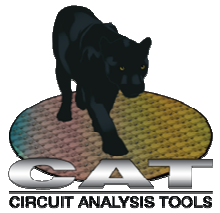
- **Familiarize participants with IARPA's interest in Circuit Analysis Tools – Please provide feedback, this is your chance to alter the course of events.**

- **Foster discussion of synergistic capabilities among potential program participants, AKA teaming. Take a chance, someone might have a missing piece of your puzzle.**

Today's Topics

- Program Overview – background and overall goals
- Program Metrics, Milestones and Reporting
- Award Information – how is the program structured
- Eligibility Information – who can propose
- Proposal Review Information – how your proposal is evaluated

- Question periods will be sprinkled throughout



CAT Program Proposers' Day

PROGRAM OVERVIEW

CAT Program Overview

- Improve fundamental tools for:
  - failure analysis
  - fault isolation
  - de-bugging
- Meet the challenges of:
  22 nm technology node and beyond
  stacked chip and other advanced packages
- Our goals are similar to those in the SEMATECH's IC Failure Analysis Council's gap analysis report
- We are looking for *large* improvements in tool technology – four generations of Moore's Law

CAT Program Thrust Areas

1. Circuit Edit – physical modification through deposition and removal of material.

2. Logic Analysis refers to the functional testing of a circuit to include logic states and timing of individual transistors and internal nodes of an integrated circuit.

3. Fault Isolation refers to localization of defects in an integrated circuit to include shorts, opens, and failed transistors (either hard or soft failures.)

4. Fast Imaging refers to tools capable of imaging minimum size circuit features on an entire silicon die, either a partially processed die or complete die with layers removed.

Program Phases

- Two (2) Phases over four (4) years:
  - Each Phase will build upon specific technical goals that must be achieved to proceed to the next, culminating in a final set of application demonstrations.
- Phase 1 high level goals (24 months): Laboratory Demonstration Platform
  - Design, fabricate, and test laboratory scale system
  - Demonstrate Phase 1 metrics
- Phase 2 high level goals (24 months): Prototype System
  - Design, fabricate, and test prototype system
  - Optimize performance of prototype system
  - Demonstrate Phase 2 metrics
  - Demonstrate Reliability and Reproducibility metrics
  - Demonstrate applications

Table 1: Circuit Edit Metrics

Circuit Edit Objective	Figure of Merit	State-of-the-art (45 nm node)	Phase 1 (22 nm node)	Phase 2 (11 nm node)
Metal Deposition	Line width	100 nm	45 nm	20 nm
	Rewire Pitch	200 nm	90 nm	40 nm
	Resistivity	400 μΩcm	200 μΩcm	80 μΩcm
	R_c to metal	300 Ω	150 Ω	60 Ω
Dielectric Deposition	Resistivity	10^9 Ωcm	10^{10} Ωcm	10^{11} Ωcm
Via Milling	Placement Accuracy	75 nm	34 nm	15 nm
	Aspect Ratio	5:1	8:1	10:1
	Endpoint in metal through dielectric[a] (10% M1)	30 nm	15 nm	6 nm
	Endpoint in metal through bulk Si[a] (10% M1)	30 nm	15 nm	6 nm
	Endpoint in dielectric through metal[a] (10% ILD)	30 nm	15 nm	6 nm
Reproducibility[b]	Fraction of working parts	90%	----	4 of 5
Reliability[b]	Temperature range with ≥75% reliability	Room Temperature	----	-50˚C to 125˚C

[a] In specified aspect ratio hole

[b] For structures incorporating metal, dielectrics and vias

Table 2: Fault Isolation Metrics

	Fault Isolation Objective	Figure of Merit	State-of-the-art (45 nm node)	Phase 1 (22 nm node)	Phase 2 (11 nm node)
Front-side Analysis	SRAM	Probing	6 probes	13 probes in 1 μm^2 box	13 probes in 0.25 μm^2 box
		Beam damage[a]	< 0.05 V Threshold voltage shift	< 0.03 V Threshold voltage shift	< 0.02 V Threshold voltage shift
		Stability (time in steady contact)	15 min	15 min	15 min
		Setup time	---	---	<10 min
	General probing	Minimum set of materials to be probed	Cu, Al, W, poly	Cu, Al, W, poly, NiSi	Cu, Al, W, poly, NiSi
	Probing preparation	Front-side delayering	planar to 40 nm over 4x4 mm	planar to 10 nm over 4x4 mm	planar to 5 nm over 4x4 mm
		Reproducibility	---	---	95%
Back-side Analysis	Optical[b] localization	Resolution (lateral)	300 nm	150 nm	80 nm
		Localization Accuracy[c]			80%
	Die level back-side thinning[d]	Thickness	20 µm	10 µm	1 µm
		Flatness over 4 cm^2	5 µm	2 µm	0.5 µm
		Surface roughness	5 nm RMS	3 nm RMS	2 nm RMS
		Reproducibility	---	---	95%
Stacked Chip Analysis	Localization of current / signals	Z (vertical)	30 µm	10 µm	< 1 µm
		X-Y (lateral[e])	6 µm	4 µm	3 µm
		Current level detection[f]	1 mA	10 µA	1 µA
		Scan time for 1 mm^2 area[f]	15 min	20 min	<30 min
		Differentiate chips[g]	2 chips of different technologies	3 chips[d]	5 chips[d]
		Localization Accuracy[c]			80%
	Re-packaging	Stacked chip separation	None	3 chips	5 chips
		Rewiring	None	3 chips	5 chips
		Reliability[h]			80%

Table 2: Fault Isolation Metrics

	Fault Isolation Objective	Figure of Merit	State-of-the-art (45 nm node)	Phase 1 (22 nm node)	Phase 2 (11 nm node)
Front-side Analysis	SRAM	Probing	6 probes	13 probes in 1 μm^2 box	13 probes in 0.25 μm^2 box
		Beam damage[a]	< 0.05 V Threshold voltage shift	< 0.03 V Threshold voltage shift	< 0.02 V Threshold voltage shift
		Stability (time in steady contact)	15 min	15 min	15 min
		Setup time	---	---	<10 min
	General probing	Minimum set of materials to be probed	Cu, Al, W, poly	Cu, Al, W, poly, NiSi	Cu, Al, W, poly, NiSi
	Probing preparation	Front-side delayering	planar to 40 nm over 4x4 mm	planar to 10 nm over 4x4 mm	planar to 5 nm over 4x4 mm
		Reproducibility	---	---	95%

[a] For probing coupled with SEM imaging

Table 2: Fault Isolation Metrics

	Fault Isolation Objective	Figure of Merit	State-of-the-art (45 nm node)	Phase 1 (22 nm node)	Phase 2 (11 nm node)
Back-side Analysis	Optical[b] localization	Resolution (lateral)	300 nm	150 nm	80 nm
		Localization Accuracy[c]			80%
	Die level back-side thinning[d]	Thickness	20 µm	10 µm	1 µm
		Flatness over 4 cm^2	5 µm	2 µm	0.5 µm
		Surface roughness	5 nm RMS	3 nm RMS	2 nm RMS
		Reproducibility	---	---	95%

[b] Optical here makes broad reference to all photonic based fault isolation approaches and resolution refers to the ability to resolve adjacent features and not simply the ability to localize peak signals with high accuracy.

[c] Localization accuracy refers to the ability to correlate a defect through physical deprocessing results with the signature obtained from the fault isolation tool.

[d] Circuit electrically intact

Table 2: Fault Isolation Metrics

	Fault Isolation Objective	Figure of Merit	State-of-the-art (45 nm node)	Phase 1 (22 nm node)	Phase 2 (11 nm node)
Stacked Chip Analysis	Localization of current / signals	Z (vertical)	30 µm	10 µm	< 1 µm
		X-Y (lateral[e])	6 µm	4 µm	3 µm
		Current level detection[f]	1 mA	10 µA	1 µA
		Scan time for 1 mm^2 area[f]	15 min	20 min	<30 min
		Differentiate chips[g]	2 chips of different technologies	3 chips[d]	5 chips[d]
		Localization Accuracy[c]			80%
	Re-packaging	Stacked chip separation	None	3 chips	5 chips
		Rewiring	None	3 chips	5 chips
		Reliability[h]			80%

[c] Localization accuracy refers to the ability to correlate a defect through physical deprocessing results with the signature obtained from the fault isolation tool.

[e] At 30 µm working distance

[f] At conditions to meet vertical and lateral resolutions (and current for scan time)

[g] Same and different technologies (eg. 3 stacked SRAMs or stacked logic and analog devices). Each die has minimum thickness of 10 µm. Imaging should be able to differentiate current / signals on each die.

[h] Reliability of technique to separate devices and repackage them without losing the ability to localize the defect (i.e. device retains same or similar electrical defect signature). Metric given as percent of parts successfully repackaged.

Table 3: Logic Analysis Metrics

Logic Analysis Objective	Figure of Merit	State-of-the-art (65 nm node)	Phase 1 (32 nm node)	Phase 2 (16 nm node)
Static and dynamic logic analysis	Sensitivity	1 hour @ 0.8V	1 hour @ 0.65V (improved 10x)	1 hour @ 0.5V, (improved 100x)
	Lateral resolution	250 nm	130 nm	60 nm
	Reproducibility[a]	---	---	99%
Sample prep	Back-side thinning	1 µm over 1 mm^2	0.3 µm over 10 $µm^2$	0.1 µm over 1 $µm^2$
	Reproducibility	---	---	95%

[a] Ability of technique to obtain the same results from repeated measurements with variations in signal intensity < 10%. Each measurement needs to include sample setup.

Table 4: Fast Imaging

Fast Imaging (tool does not need to be an SEM)				
Objective	Figure of Merit	State-of-the-art (45 nm node)	Phase 1 (45 nm node)	Phase 2 (22 nm node)
Image acquisition speed	Imaging time[a]	140,000 min	1,400 min (improved scan rate 100x)	1,400 min (improved scan rate 400x)
	Reproducibility[b]	---	---	99%
Die level front-side planar delayering[c]	Flatness over 1 cm^2	1 µm	1 µm	0.5 µm
	Surface roughness	5 nm RMS	3 nm RMS	2 nm RMS
	Minimum set of materials to be delayered	Al, Cu, SiO_2	Al, Cu, SiO_2, low-k	Al, Cu, SiO_2, low-k
	Method	Manual	Manual	Automatic
	Reproducibility	---	---	95%

[a]To image a 1 cm^2 area with a pixel density of 8 pixels per line width and signal to noise ratio of 20:1. Note that in Phase 2, the improvement is through imaging smaller feature sizes, while keeping the total scan time the same. This results in an effective increase in scanning rate of 400x more than state-of-the-art.

[b]Image quality (signal-to-noise and resolution) is reproducible within 10% for 99% of measurements on the same device.

[c]Underlying circuit electrically intact

More on Metrics

- **Program Metrics:**
  - **Evaluate the effectiveness of proposed solutions in achieving the stated program objectives.**
  - **Determine whether satisfactory progress is being made to warrant continued funding of the program.**
  - **Bound the scope of effort, while affording maximum flexibility, creativity, and innovation in proposing solutions to the stated problems.**
  - **Proposer may suggest that one or more metrics are not suitable. If so, the reasoning should be fully explained, and an alternate metric suggested as appropriate. Overly conservative metrics will adversely affect a proposal's score.**
  - **Proposers may suggest additional metrics.**

Waypoints

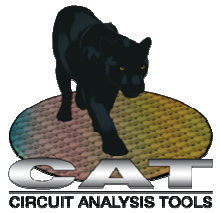
Months after Program Start*	Waypoint Description	Metric	Intent
1-2 months	Kickoff site visits (At Contractor)	Start-up progress: Staffing, equipment and resource readiness; approach and schedule confirmation	Mutual understanding of project plan and effective project start
7 months (Nov 2010)	Program Workshop (At ISTFA)	Attendance and Presentation	Cross-fertilization between program performers; strengthen collaborative relations; gain insights into extant approaches to analysis techniques
10 months	Program Review (DC Area)	Progress and schedule	Funding continuance

***For 2nd, 3rd, and 4th year waypoints add 12 months, etc.**

Reporting

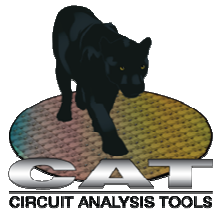
Mandatory Reports

- Monthly Financial Report (spreadsheet)
- Monthly Technical Report (1 Page)
- Quarterly Technical Report (PowerPoint Slides)
- Annual Report
- Final Contract Report



CAT Program Proposers' Day

Questions?



CAT Program Proposers' Day

Proposals

Schedule

- White Papers due 30 days after BAA published. *White papers are optional but highly encouraged*
- White Paper feedback to offerors within 30 days.
- Full Proposals due 90 days after BAA is published.
- Awards announced ~ 180 days after BAA published.

Once the BAA is released, questions can only be answered in writing on the program website.

Proposal Format

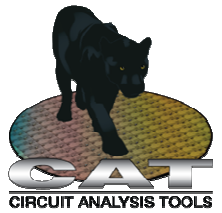
- **Volume 1 -- Technical and Management Proposal (Maximum 30 pp.)**
  - **Section 1 – Cover Sheet and Transmittal Letter**
  - **Section 2 – Summary of Proposal**
  - **Section 3 – Detailed Proposal**
  - **Section 4 – Additional Information**

- **Volume 2 – Cost Proposal (No page limit)**
  - **Section 1 – Cover**
  - **Section 2 – Detailed Estimated Cost Breakdown**

White papers consist of Volume 1, Sections 1 & 2. (Maximum 10 pp.)

Proposals must conform to page limits!!!

Proposals



- **Programmatic issues that should be discussed in the proposal:**
  - **Team's current technical capabilities.**
  - **Key resources needed which are not currently available to the team, such as capital equipment and special expertise. Teaming will likely play an essential role in providing special expertise.**
  - **A teaming plan along with the roles and responsibilities of each member of the research team.**
  - **End of Phase and some intermediate milestones are set, but it is expected that other intermediate milestones that are on the critical path of the proposed approach will be proposed.**
  - **A schedule of all milestones including a clearly charted description of the various risk mitigation strategies that will be undertaken to achieve the important (particularly end of phase) milestones.**

Teaming

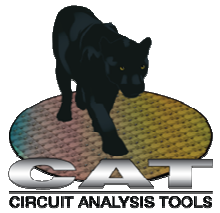
- **Because of the many challenges in designing, fabricating, and testing greatly improved circuit analysis tools, both depth and diversity will be beneficial for overcoming these challenges.**
  - **Completeness – teams should not lack any capability necessary for success, *e.g.* should not rely upon results from the community at large, or some enabling technology to be developed elsewhere.**
  - **Tightly knit teams**
    - **Clear, strong management, single point of contact**
    - **No loose confederations**
    - **Each team member should be contributing significantly to the program goals. Explain why each member is important, *i.e.* if you didn't have them, what wouldn't get done?**
    - **No teaming for teaming's sake.**
- **Remember, you may be very accomplished, but can you do it all?**

Award Plan

- 4-year Program starting Spring 2010
  - Base Period - 12 months
  - Option Year 1 - 12 months
  - Option Year 2 - 12 months
  - Option Year 3 - 12 months

- Criteria for awarding option years: success against previous year's goals, funds availability, and IARPA priorities. Award of option years is at the sole discretion of the Government.

- Multiple awards anticipated, depending upon
  - quality of the proposals received
  - availability of funds



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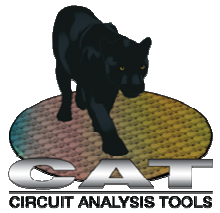


CAT Program Proposers' Day

Eligibility Information

Eligibility Information

- Collaborative efforts/teaming strongly encouraged
  - Content, communications, networking, and team formation - responsibility of proposers
- Foreign organizations and/or individuals may participate
  - Must comply with Non-Disclosure Agreements, Security Regulations, Export Control Laws, etc, as appropriate
- Other Government Agencies, Federally Funded Research and Development Centers (FFRDCs), University Affiliated Research Centers (UARCs), and any other similar type of organization that has a special relationship with the Government, that gives them access to privileged and/or proprietary information, or access to Government equipment or real property, are not eligible to submit proposals under this BAA or participate as team members under proposals submitted by eligible entities.
- If you wish to utilize any resources from these organizations, please let me know ASAP. If IARPA determines that the resources are unique and do not exist in the private sector, IARPA will attempt to work directly with that organization to arrange for that capability to be made available to all program participants who might benefit.

Test chips

- Test chips for demonstration of metrics and overall capability will be developed during the beginning of the program with the assistance of a Government partner.

- Offerors should budget in their proposals for test chips required for tool development.

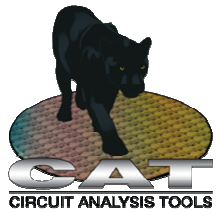
CAT Program Proposers' Day

Proposal Review Information

Evaluation Criteria

- **Evaluation criteria in descending order of importance are:**
  - **Overall Scientific and Technical Merit**
  - **Effectiveness of Proposed Work Plan**
  - **Relevance to CAT Program Goals**
  - **Relevant Experience and Expertise**
  - **Cost Realism**
- **All responsive proposals will be evaluated by a board of qualified government reviewers. Each proposal will be evaluated by at least three reviewers.**

Point of Contact



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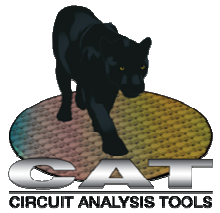
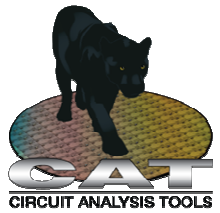


CAT Program Proposers' Day

Thank You!

Any Final Questions?



Look for the CAT BAA sometime in the next few weeks

http://www.iarpa.gov/solicitations.html