OFFICE OF THE DIRECTOR OF NATIONAL INTELLIGENCE

Trusted Integrated Chips (TIC)
Safe and Secure Operations Office

LEADING INTELLIGENCE INTEGRATION

Dennis L. Polla, Ph.D.
Acting Director SSO
TIC Proposers' Day
27 July 2011

TIC Program Proposers' Day Agenda

8:30am – 8:45am	*IARPA Overview and Remarks*	Dr. Dennis Polla SSO Office Director	Atrium Ballroom
8:45am – 9:15am	*DARPA TRUST and IRIS Programs*	Dr. Carl McCants DARPA Program Manager	
9:15am – 10:15am	*TIC Program Overview*	Dr. Dennis Polla SSO Office Director	
10:15am – 10:45am	*Break*		
10:45am – 11:15am	*TIC Program Questions & Answers*	Dr. Dennis Polla SSO Office Director	Atrium Ballroom
11:15am – 11:45am	*Contracting*	Ms. Sarah Wiley IARPA Contracting Officer	
11:45am – 1:00pm	*Lunch*		
1:00pm – 2:00pm	*Proposers' 5-minute Capability Presentations*	Attendees (**No Government**)	Atrium Ballroom
2:00pm – 5:00pm	*Proposers' Networking and Teaming Discussions*	Attendees (**No Government**)	Margaret Brent (2nd Fl, Room 2112)
1:00pm – 4:30pm	*Proposers' 10-minute Side-bars (Optional)*	Non-USG Affiliated Attendees	Thurgood Marshall (2nd Fl, Room 2113)

Disclaimer

- This presentation is provided solely for information and planning purposes.
- The Proposers' Day Conference does not constitute a formal solicitation for proposals or proposal abstracts.
- Nothing said at Proposers' Day changes the requirements set forth in a BAA.
- BAA supersedes anything presented or said at the Proposers' Day by IARPA.

Proposers' Day Goals

- **Familiarize participants with IARPA's interest in secure and reliable chip fabrication – Please ask questions & provide feedback; this is your chance to alter the course of events.**
- **Foster discussion of synergistic capabilities among potential program participants; identification of teaming opportunities.**

Trusted Integrated Chips (TIC) Motivation

- Large integrated circuit foundries now dominate the world's production of high performance integrated circuits.
- Fabless companies have emerged as high-value designers leaving fabrication to foundries.
- TSMC, Global Foundry Solutions, UMC, and SMIC are the world's largest foundries competing on performance, cost, delivery, systems integration, and yield.
- US policies and approaches to ensuring our access to safe and secure integrated chips (ICs) are not keeping up with the explosive domination/capabilities of world foundries.
- The US must have open access to obtain the highest performance integrated circuits and systems chips.

Trusted Integrated Chips (TIC) Overview

Vision:

- Ensure the U.S. Intelligence Community can obtain the highest performance possible in integrated circuits which are often derived from commercial foreign foundries, not just through U.S. trusted foundries.
- Obtain near 100% assurance that designs are safe and secure – not compromised with malicious circuitry.
- Ensure security of designs, capability, and performance while simultaneously protecting intellectual property.
- Realize secure systems combining advanced CMOS with higher value chips.

Goal:

- Develop new approaches to chip fabrication to assure security and intellectual property protection of chips manufactured by off-shore foundries.

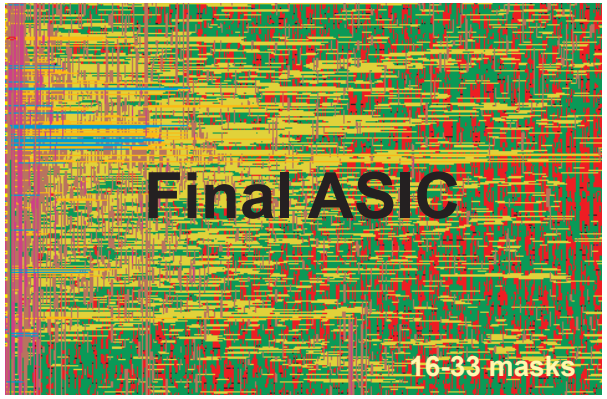
Approach:

- Protection of circuit/systems designs.
- Split-Manufacturing: Front-End-of-Line (FEOL) at a world-class foundry followed by Back-End-of-Line (BEOL) metallization at a U.S. secure facility.

Split Manufacturing Concept

Offshore-produced raw material

Trusted metallizations

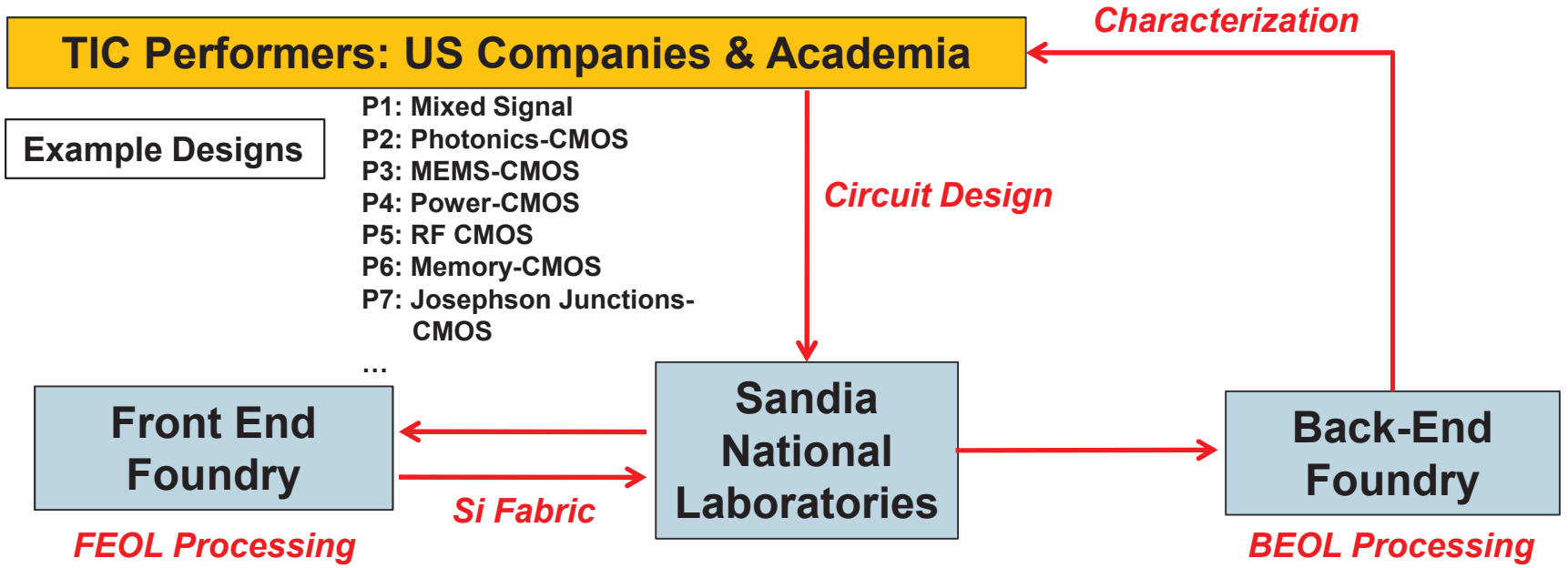


Safe and Secure ASIC

- Security assurance
- IP protection
- Cost-volume trade-offs may even enable superior reliability and performance as compared to commercial products

L. Pileggi, CMU

Government Provided Capabilities Available to Offerors



- Foundry design rules will be available to performers for FEOL and BEOL processing.
- Sandia National Laboratories will coordinate submitted circuit designs for FEOL and BEOL processing.
- The completed wafers or die will be sent back to performers for characterization.

Program Objective (TIC)

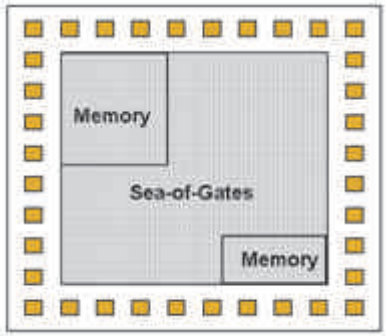
- **Attain state-of-the art performance and near absolute security assurance in integrated circuits derived from world-class commercial foundry operations**
  - Best performance derived from advanced semiconductor nodes
  - Access to commercial manufacturing innovation and timely delivery
  - Assurance that sensitive designs are not disclosed to our adversary
  - Assurance that no malicious circuitry has been fabricated in our chips
  - Reliability assurance

- **Back-End-Of-Line (BEOL) processing (integrated circuit fabrication up to the point of metallization or first metallization by foundry with remaining metallization steps taking place in a secure facility in the USA**
  - Design intention in not disclosed
  - Malicious circuits are either detected or simply not powered

- **Program seeks**
  - Demonstration of split-manufacturing concept applied to high performance chips
  - Obfuscation of design intent
  - Security of designs and assurance against malicious circuits

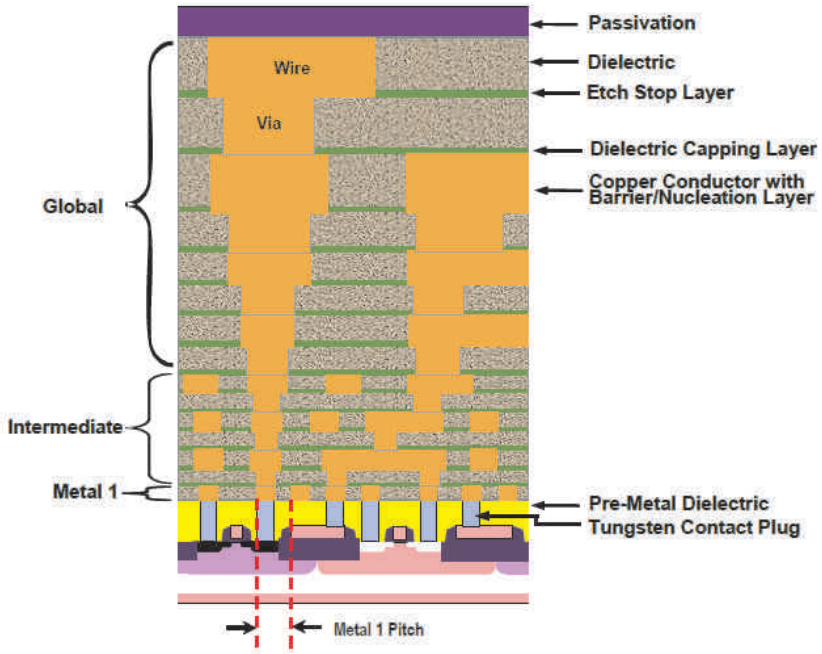
Split Manufacturing for Security and Performance

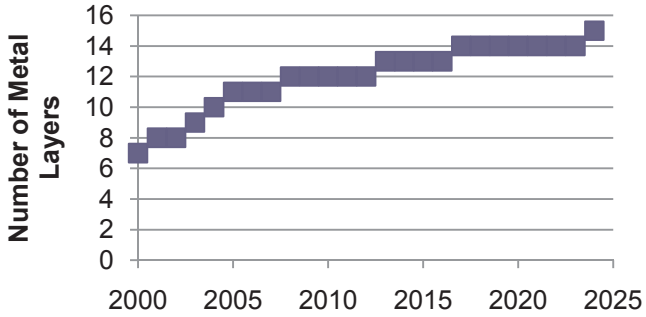
- Standard cell designs could be partially fabricated off-shore to obfuscate much of the design intent and IP (intellectual property)
  - Minimal circuit-level design IP may be disclosed
- Gate arrays and "Si fabrics" would not disclose any IP or intent
  - Off-shore design would be just a raw material that is more easily inspected for faults and trojan horses
  - But there is a significant design quality compromise



- Nanoscale patterning trends make split-fabrication more effective
  - Construct an application-specific FEOL "array" of devices off-shore that can be customized at a trusted U.S. facility
  - Low volume trusted fabrication solutions for BEOL could be used to create ICs that are superior to those from off-shore commercial fab alone
  - Regular FEOL patterns represent raw material that can be thoroughly inspected for faults and insertion of nefarious circuitry

Split Manufacturing Challenge



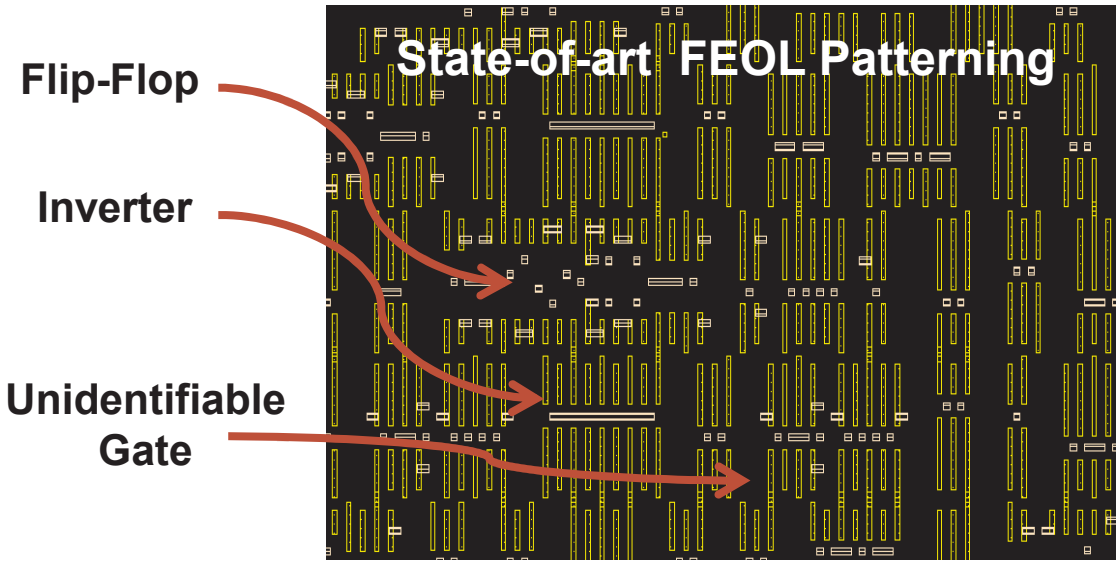


SIA Roadmap 2010

- **The semiconductor layer (FEOL) lithography node is set by the critical dimension (CD)**
  - **Usually the gate length of the MOSFET**
- **State-of-the art ICs have up to 12 layers of copper interconnect (BEOL)**
  - **Number of layers will continue to increase**
- **First metal layer is at node pitch**
  - **Intermediate metal layers are at 1.5 times node pitch**
  - **Global layers are 2 times node pitch to 2 microns**
  - **Same level of fab capability is needed at first layers of BEOL as FEOL**

FEOL Circuit Obfuscation

- **Indistinguishable *and* area efficient SRAM and logic patterns are currently unlikely**
- **But creating slightly more generic logic patterning provides additional security to reverse engineering and silent fault insertion**
- **Investigate design/security trade-off of increased generic logic patterning**



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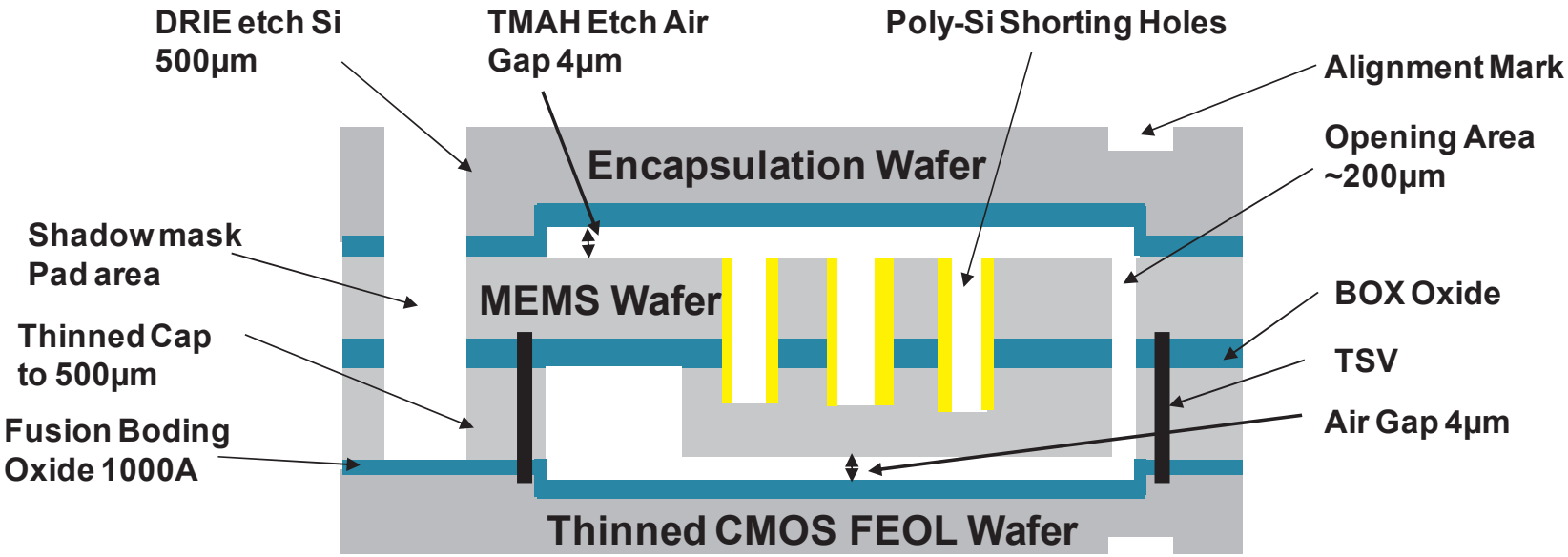
Example: 3D MEMS BEOL Integration and Packaging



Challenges:

- 3-wafer fusion bonding to SOA FEOL CMOS
- Vertical DRIE profile for large open area
- Notching for small area DRIE etching
- Metallization for multi-step height structures

Nanyang Technological University
DARPA N/MEMS S&T Fundamentals
Prof. Holden Li

Circuit Verification

- **New verification methods that ensure that no malicious circuitry has been added during fabrication. These methods are anticipated and set at the time of fabrication.**

- **New ideas that are different from those being explored in other federal research programs such as DARPA TRUST and DARPA IRIS programs are encouraged.**

Focus Areas

Thrust Area	Description
1. Secure Split-Manufacturing	Development of split-manufacturing processes in which a FEOL process defines transistor building blocks up to the point of the first or second metallization followed by a BEOL process in which remaining metallizations are carried out in secure trusted facilities in the U.S. Initially, a conservative node (e.g., 130 nm-node) will be selected in Phase I with continued improvement in Phases II and III.
2. FEOL Circuit Obfuscation	Circuit obfuscation methods whereby the intent of digital and analog functions and their associated building blocks are disguised in their function within the FEOL process.
3. Circuit Verification	New verification methods that ensure that no malicious circuitry has been added during fabrication. New ideas that are different from those being explored in other federal research programs such as DARPA's TRUST and IRIS programs are encouraged.
4. 3-D Fabrication	New approaches to 3-D fabrication at significant semiconductor manufacturing nodes. These include new transistor/circuit designs and creative stacking methods such as those which may be required for integrated MEMS and III-V-on-Si chips.

Key Technical Challenges

- **Split-Manufacturing: BEOL processing on FEOL silicon fabrics at SOA manufacturing nodes with BEOL metallization**
- **Circuit obfuscation approaches**
- **Virtually 100% assurance against compromised circuits**
- **3D processing and integration at challenging nodes**

Out of Scope

- **Processes carried out on < 200 mm wafers or >0.25 μm design rules.**
- **Non-scalable designs.**
- **Processes that do not drive ultimate CMOS performance per Semiconductor Industry Roadmap.**
- **Obfuscation, characterization, or trust verification efforts that are not integrated in a chip-producing split-end manufacturing approach.**

Program Phases

	Duration	Description
Phase I Base Period	**18 months**	• **Develop the proposed design, process or packaging** • **Demonstrate the feasibility of the proposed technologies**
Phase II Option Period 1	**15 months**	• **Scale the technologies to the intermediate technology node** • **Implement and demonstrate at this node**
Phase III Option Period 2	**15 months**	• **Scale the technologies to the final program technology node** • **Implement and demonstrate at this node**

Notes:

1. The TIC Program is anticipated to be 4 years in duration.
2. Phases become more difficult as the development technologies scale to address more advanced technology nodes:
    - The secure split-manufacturing development will start, for example, with the 130 nm-node in Phase 1 and subsequently move toward the 22 nm-node in Phase III.
    - 3D processing will similarly address increasing more complex integrated structures such as high-performance integrated circuits and integrated systems such as MEMS, photonics-on-Si, etc.
3. Each phase must satisfy specific technical goals before proceeding to the following phase.

Example Performance Goals

Metric	Phase I Base Period	Phase II Option Period 1	Phase III Option Period 2
BEOL: Process - 130nm process - 65nm process - 32/28/22nm process	Density > 50%	Density > 90%	Density = 100%
BEOL: Nanoscale Patterning - 130nm metallization - 28/22nm metallization - 12nm metallization	Density > 50%	Density > 90%	Density > 150%
FEOL Obfuscation - Logic/memory obs. - Analog/digital obs.	 Density > 50% Density > 50%	 Density > 90% Density > 90%	 Density = 100% Density = 100%
3D Processing - 3D IC Obfuscation - 3D MEMS - 3D III-Vs-on-Si	 Speed > 1X S/N > 1X	 Speed > 1X S/N > 2X	 Speed > 1.5X S/N > 10X Speed > 2X
Verification - 130nm process - 65nm process - 32/28/22nm process	Speed > 1X	Speed > 1X	Speed > 2X

Note: These are example performance goals provided as reference. Offerors must propose aggressive quantitative metrics specific to the technologies and application interests proposed and intermediate quantifiable milestones for monitoring and measuring the program progress.

Example Major Milestones

Milestone Description	Months after Program Start	Metric	Deliverable
Phase 1 (Base Period, 18 months)			
1) Concept design and/or feasibility study - completion	3 months	---	Report
2) First iteration design, fab and test of circuit demo vehicle (CDV) at the starting technology node	11 months	Performance meets or exceeds Phase 1 waypoint metrics	Test Report Test Chips
3) Second iteration design, fab and test of CDV at the starting technology node	18 months	Performance meets or exceeds Phase 1 metrics	Test Report Test Chips
Phase 2 (Option Period 1, 15 months)			
4) First iteration design, fab and test of CDV scaled at the intermediate technology node	26 months	Performance meets or exceeds Phase 2 waypoint metrics	Test Report Test Chips
5) Second iteration design, fab and test of CDV scaled at the intermediate technology node	33 months	Performance meets or exceeds Phase 2 metrics	Test Report Test Chips
Phase 3 (Option Period 2, 15 months)			
6) First iteration design, fab and test of CDV scaled at the leading-edge technology node	41 months	Performance meets or exceeds Phase 3 waypoint metrics	Test Report Test Chips
7) Second iteration design, fab and test of CDV scaled at the leading-edge technology node	48 months	Performance meets or exceeds Phase 3 metrics	Test Report Test Chips

Test and Evaluation

- **Participants will characterize the chips produced in the TIC program.**

- **Sandia National Laboratories will perform minimal characterization of test transistors and circuits.**

Proposal Guidance

- **Your proposal should include a full discussion of the technical approach that will be used to meet the program goals.**
- **Programmatic issues to be addressed in the proposal:**
  - **Your team's current technical capabilities**
  - **Key resources needed (not currently available to your team), to include capital equipment and special expertise (teaming will likely play an essential role in providing special expertise). The risk in acquiring these key resources, and mitigation strategies, should be indicated as well**
  - **A teaming plan along with the roles and responsibilities of each member of the research team**
  - **End of phase and some intermediate milestones are set, but it is expected that other intermediate milestones that are on the critical path of the proposed approach will be offered**
  - **A schedule of all milestones including a clearly charted description of the various risk mitigation strategies that will be undertaken to achieve program goals**

Eligibility Information

- **Other Government Agencies, Federally Funded Research and Development Centers (FFRDCs), University Affiliated Research Centers (UARCs), and any other similar type of organization that has a special relationship with the Government, that gives them access to privileged and/or proprietary information or access to Government equipment or real property, are not eligible to submit proposals under this BAA or participate as team members under proposals submitted by eligible entities**
- **Only U.S. organizations or institutions may prime and submit proposals to the Trusted Integrated Chips (TIC) BAA. Additionally, at least twenty percent (20%) of the principals of the team (as measured by FTEs) must be from U.S. organization(s) or institution(s). Foreign participants and/or individuals may participate to the extent that such participants comply with any necessary Non-Disclosure Agreements, Security Regulations, Export Control Laws and other governing statutes applicable under the circumstances. Proposers are expected to ensure that the efforts of foreign participants do not either directly or indirectly compromise the laws of the United States, nor its security interests. As such, proposers should carefully consider the roles and responsibilities of foreign participants as they pursue teaming arrangements in response to the TIC BAA.**

Proposal Evaluation Criteria

- **Overall Scientific and Technical Merit**
- **Effectiveness of Proposed Work Plan**
- **Relevance to IARPA Mission and TIC Program Goals**
- **Relevant Experience and Expertise**
- **Cost Realism**

Evaluation criteria will appear in the BAA.

Teaming

- **Because of the many challenges presented by this program, both depth and diversity will be beneficial.**
  - **Throughput: Consider all that you will need to do, all the ideas you will need to test. Make sure you have:**
    - **Enough people and expertise to do the job**
    - **Sufficient resources to follow critical path while still exploring alternatives – risk mitigation**
  - **Completeness: teams should not lack any capability necessary for success, e.g., should not rely on enabling technology to be developed elsewhere.**
  - **Tightly knit teams**
    - **Clear, strong, management; single point of contact**
    - **Each team member should be contributing significantly to the program goals. Explain why each member is important, i.e., if you didn't have them, what wouldn't get done?**
    - **No teaming for teaming sake**

Schedule

- **Full Proposals are due ~45 days after BAA is published.**
- **Once the BAA is released, questions can only be answered in writing on the program website.**

Additional Information

- **Email: dni-iarpa-baa-11-09@ugov.gov with additional questions**
- **TIC BAA will be posted on FedBizOpps website (www.fedbizopps.gov)**
- **Q&As will appear after the BAA. See http://www.iarpa.gov/solicitations_tic.html**

TIC Summary

a) Prove that Secure IC Technology can be realized through a Front-End (FEOL) / Back-End of Line (BEOL) Split-Manufacturing Process.

b) Enable the U.S. government and their contractors to have access to world-class integrated circuit foundry manufacturing facilities.

c) Ensure security of designs, design intent, and performance capabilities.

d) Drive a U.S. model for both national security protection and IP protection.

e) Ensure the security of the chips we use in our networked world.

f) Develop multi-functional systems containing the highest performance Si CMOS.

TIC Program Proposers' Day

Questions?