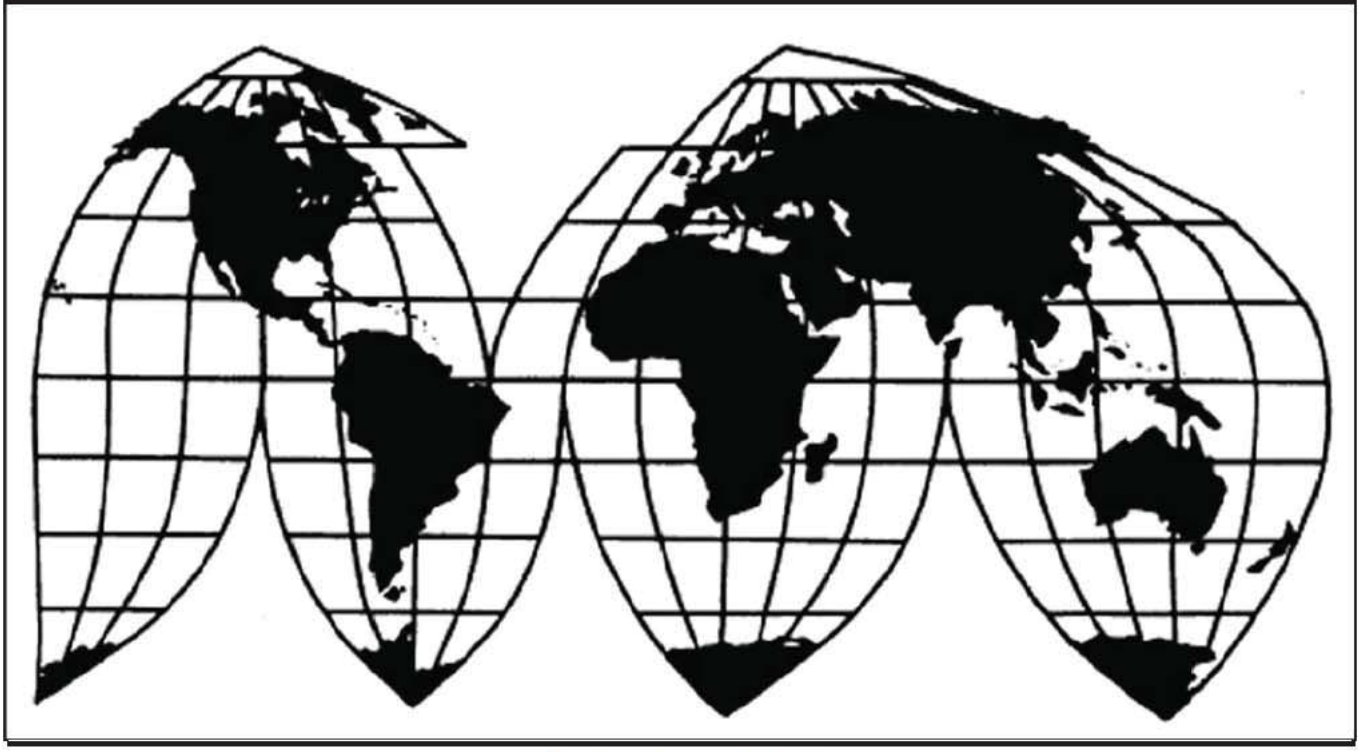
In the Matter of

CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS, MEDIA PLAYERS, AND CAMERAS

Investigation No. 337-TA-709

Publication 4330 **June 2012**

U.S. International Trade Commission



Washington, DC 20436

U.S. International Trade Commission

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UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C. 20436

In the Matter of **CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS, MEDIA PLAYERS, AND CAMERAS**	**Investigation No. 337-TA-709**

NOTICE OF COMMISSION DETERMINATION NOT TO REVIEW A FINAL DETERMINATION OF NO VIOLATION OF SECTION 337; TERMINATION OF THE INVESTIGATION

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has determined not to review the final initial determination ("ID") issued by the presiding administrative law judge ("ALJ") on April 4, 2011, finding no violation of section 337 in the above-captioned investigation.

FOR FURTHER INFORMATION CONTACT: Jia Chen, Office of the General Counsel, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 708-4737. Copies of non-confidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 205-2000. General information concerning the Commission may also be obtained by accessing its Internet server at *http://www.usitc.gov*. The public record for this investigation may be viewed on the Commission's electronic docket (EDIS) at *http://edis.usitc.gov*. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on (202) 205-1810.

SUPPLEMENTARY INFORMATION: The Commission instituted this investigation on March 29, 2010, based on a complaint filed by Freescale Semiconductor, Inc. of Austin Texas. 75 *Fed. Reg.* 16837 (Mar. 29, 2010). The complaint alleged violations of Section 337 of the Tariff Act of 1930 (19 U.S.C. § 1337) in the importation into the United States, the sale for importation, and the sale within the United States after importation of certain integrated circuits, chipsets, and products containing same including televisions, media players, and cameras by reason of infringement of certain claims of U.S. Patent Nos. 5,467,455 ("the '455 patent"), 5,715,014, and 7,199,306. The complaint, as amended, named the following respondents:

Panasonic Corporation of Osaka, Japan; Panasonic Corporation of North America of Secaucus, New Jersey; Funai Electric Co., Ltd. of Osaka, Japan, Funai Corporation, Inc. of Rutherford, New Jersey Funai (collectively "Funai"); JVC Americas Corp. of Wayne, New Jersey; Victor Company of Japan Limited of Yokohama, Japan; Best Buy Purchasing, LLC, Best Buy.Com, LLC, Best Buy Stores, L.P., all of Richfield, Minnesota (collectively "Best Buy"); B&H Foto & Electronics Corp. of New York, New York; Huppin's Hi-Fi Photo & Video, Inc. of Spokane, Washington; Buy.com Inc. of Aliso Viejo, California; QVC, Inc. of West Chester, Pennsylvania; Crutchfield Corporation of Charlottesville, VA. Only Funai, Best-Buy, and Wal-Mart remain as respondents, and only the '455 patent is currently at issue.

On April 4, 2011, the presiding ALJ issued a final ID finding no violation of section 337 by respondents Funai, Best-Buy and Wal-Mart. The ALJ concluded that none of the accused products infringe the '455 patent because the third-party documents relied on by complainant to show infringement were entitled to no evidentiary weight. The ALJ further concluded that otherwise all of the elements for proving a violation were shown and that respondents have not established that the '455 patent is invalid under 35 U.S.C. § 102 for anticipation, under 35 U.S.C. § 103 for obviousness, or under 35 U.S.C. § 112 for failure to comply with the written description requirement. On April 28, 2011, complainant filed a petition for review of the ID. On the same day, respondents filed a contingent petition seeking review only if the Commission otherwise determined to review the ID.

Having examined the record of this investigation, including the ALJ's final ID and the submissions of the parties, the Commission has determined not to review the ID.

The authority for the Commission's determination is contained in section 337 of the Tariff Act of 1930, as amended (19 U.S.C. § 1337), and in sections 210.42-46 and 210.50 of the Commission's Rules of Practice and Procedure (19 C.F.R. §§ 210.42-46 and 210.50).

By order of the Commission.

James R. Holbein
Secretary to the Commission

Issued: June 6, 2011

CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS, MEDIA PLAYERS, AND CAMERAS **337-TA-709**

CERTIFICATE OF SERVICE

I, James Holbein, hereby certify that the attached has been served by hand upon the Office of Unfair Import Investigations and the following parties as indicated, on _____June 6, 2011_____.

James Holbein, Secretary
U.S. International Trade Commission
500 E Street, SW
Washington, DC 20436

On Behalf of Complainant Freescale Semiconductor, Inc.:

Alan D. Albright, Esq.
BRACEWELL & GIULIANI LLP
111 Congress Avenue, Suite 2300
Austin, Texas 78701

( ) Via Hand Delivery
( ) Via Overnight Mail
(X) Via First Class Mail
( ) Other: _____

On Behalf of Respondent Wal-Mart Stores, Inc.:

Janine A. Carlan, Esq.
ARENT FOX LLP
1050 Connecticut Ave., NW
Washington, DC 20036

( ) Via Hand Delivery
( ) Via Overnight Mail
(X) Via First Class Mail
( ) Other: _____

On Behalf of Respondents Funai Electric Co., Ltd.; Funai Corporation, Inc.; Best Buy Purchasing, LLC; BestBuy.com, Inc.; Best Buy Stores, L.P.:

Paul Devinsky, Esq.
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600 13th Street. NW. 2th Floor
Washington. D.C. 20005-3096

( ) Via Hand Delivery
( ) Via Overnight Mail
(X) Via First Class Mail
( ) Other: _____

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	
CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS, MEDIA PLAYERS, AND CAMERAS	Inv. No. 337-TA-709

Final Initial and Recommended Determinations

This is the administrative law judge's Final Initial Determination under Commission rule 210.42. The administrative law judge, after a review of the record developed, finds inter alia that there is jurisdiction and that there is no violation of section 337 of the Tariff Act of 1930, as amended.

This is also the administrative law judge's Recommended Determination on remedy and bonding, pursuant to Commission rules 210.36(a) and 210.42(a)(1)(ii). Should the Commission find a violation, the administrative law judge recommends the issuance of limited exclusion orders barring entry into the United States of infringing integrated circuits, chipsets and products containing same including televisions, media players, and cameras as well as the issuance of appropriate cease and desist orders. The imposition of any bond during the Presidential Review period is not recommended.

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ABBREVIATIONS

CBr	Complainant's Post Hearing Brief
CRBr	Complainant's Post Hearing Reply Brief
CPFF	Complainant's Findings of Fact
CRFF	Complainant's Rebuttals to Respondents' Findings of Fact
RBr	Respondents' Post Hearing Brief
RRBr	Respondents' Post Hearing Reply Brief
RFF	Respondents' Findings of Fact
RRFF	Respondents' Rebuttal Findings of Fact
SBr	Staff's Post Hearing Brief
SRBr	Staff's Post Hearing Reply Brief
SRFF	Staff's Responses to Respondents' Findings of Fact

OPINION

I. Procedural History

By notice dated March 29, 2010, the Commission instituted an investigation, pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, to determine inter alia (a) whether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain integrated circuits, chipsets, or products containing same including televisions, media players, or cameras that infringe one or more of claims 1, 8-10, 22, and 26 of U.S. Patent No. 5,467,455 ('455 patent), claims 1 and 10 of U.S. Patent No. 5,715,014 ('014 patent), and claims 1, 6, 11, and 13-16 of U.S. Patent No. 7,199,306 ('306 patent).

The complaint, relating to the investigation, was filed with the Commission on March 1, 2010, under section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, on behalf of Freescale Semiconductor, Inc. (Freescale). A letter supplementing the complaint was filed on March 18, 2010. The complainant requested that the Commission institute an investigation and, after the investigation, issue an exclusion order and cease and desist orders. The following were named in the notice of investigation as respondents and were served with the complaint: Panasonic Corporation, Panasonic Semiconductor Discrete Devices Co., Ltd. (PSDD) and Panasonic Corporation of North America; Funai Electric Co., Ltd. and Funai Corporation, Inc. (Funai); JVC Kenwood Holding, Inc. (JVC); Victor Company of Japan Limited (Victor); JVC Americas Corp. (JVC); Best Buy Co., Inc. (Best Buy); B & H Foto & Electronics Corp. (B&H); Huppin's Hi-Fi Photo & Video, Inc. (Huppin's); Buy.com Inc. (Buy); Liberty Media Corporation (Liberty); QVC, Inc. (QVC); Crutchfield Corporation; (Crutchfield); Wal-Mart Stores, Inc. (Wal-Mart); and Computer Nerds International, Inc. (Computer Nerds).

By notice dated April 22, 2010, the investigation was permanently reassigned to the undersigned.

Order No. 2, which issued on April 2, 2010, set a sixteen month target date of August 2, 2011, which meant that any final initial determination on violation should be filed no later than Monday April 4, 2011.[1]

On July 8, 2010, Order No. 10 granted complainant's motion for leave to amend its complaint to (1) correct clear typographical errors; (2) replace one respondent, viz. Best Buy, whose counsel has represented that it does not sell for importation, import, or sell after importation any accused products and has provided an identification of substitute parties, viz. Best Buy Purchasing, LLC, Best Buy.com, Inc. and Best Buy Stores, L.P. that should be added in Best Buy's place; and (3) add additional dependent claim 2 of the '306 patent and, with respect to (2) supra, correct the Notice of Investigation.

On August 3, 2010, Order No. 15 granted complainant's motion for termination of the investigation as to respondents PSDD and JVC. The Commission non-reviewed Order No. 15 on September 2, 2010.

On September 30, 2010, Order No. 20, granted complainant's motion for leave to amend its complaint and the notice of investigation to: (1) change the name of one respondent from BestBuy.com, Inc. to BestBuy.com, LLC; (2) correct the addresses of BestBuy.com, LLC and Best Buy Purchasing, LLC; and (3) terminate one respondent, namely Liberty, whose counsel had represented that it does not sell for importation, import, or sell after importation any accused products. The Commission non-reviewed Order No. 20 on October 21, 2010.

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[1] The notice of publication was published on April 2, 2010 (75 Fed. Reg. 16,837).

Order No. 33, which issued on January 5, 2011, granted complainant's motion that it has satisfied the requirements of 19 U.S.C. § 1337 (a)(3) in that a domestic industry based on licensing activities exists in the United States for each of the patents in issue in this Investigation, viz. the '455 patent, the '014 patent and the '306 patent. The Commission non-reviewed Order No. 33 on February 4, 2011.

Order No. 34, which issued on January 5, 2011, granted a motion of certain respondents for summary determination of non-infringement of claim 1 of the '306 patent. The Commission, in a notice dated February 7, 2011 extended the date for determining whether to review Order No. 34 by sixty (60) days to April 11, 2011.

The administrative law judge did not conduct a "tutorial." However Order No. 36, which issued on January 13, 2011 and was considered an "education vehicle" for the administrative law judge, required submissions from complainant, respondents and the Commission Investigative Staff (staff) with said order making reference to the prehearing briefs of respondents and the staff and posing, inter alia, the following question for respondents:

> 35. Referring to the '455 patent and respondents' invalidity assertions of the asserted claims on prior art, as the staff argued (SPre at 70-71) respondents allege some ten separate anticipatory prior art references for the asserted claims and further assert over 40 different permutations of prior art combinations as invalidating under section 103, including combinations of prior art that are also alleged to anticipate. Moreover in fn 31 the staff in its SPre argued that besides being unreasonably large in number, the invalidity assertions in respondents' pre-hearing brief also suffer from a dearth of detail. The administrative law judge agrees. The respondents are put on notice that, in response to this question, unless respondents supplement their prior art invalidity arguments with specific facts, said arguments will be stricken from the RPre and respondents will not be permitted to present said arguments at the evidentiary hearing. Respondents' supplementation, in response to this question, should factually address each of the assertions raised in CPre

> at 425-78 and in CSPre at 17-21. Merely as an illustrative example, respondents are directed to the statements of complainant regarding Gist (CPre at 427-34). For example do respondents agree that in Gist there is a separate integrated circuit for the bus interface circuits, apart from whatever integrated circuit may also be part of the device or module. If respondents do not agree, respondents should make specific reference to exhibits in support. A reference to charts will carry no weight. On this point, the staff in its fn 31 has represented that respondents' expert on the '455 patent even testified that the reader of charts had to "infer" which claim elements were where in the prior art references. Such testimony, if made at the evidentiary hearing, will not meet the clear and convincing standard that respondents must meet in invalidating claims over prior art. As additional examples of the inadequacy of the portion of RPre relating to the alleged invalidity of the asserted claims of the '455 patent, respondents argued (RPre at 178) that "as detailed in RX-0635, each and every element of claims 1, 8, 9, 10, 22 and 26 of the '455 patent are found explicitly or inherently in the teachings of the Gist patent." Similar language, on anticipation with respect to other art is found at RPre 180, 181, 182, 183, 185, 186, 187. Like language, as to obviousness is found at RPre at 191, 192, 194, 195, 197, 198, 199, 201, 202.

(Order No. 36 at 7.) Said Order 36 required filings from complainant and the respondents by January 21, 2011, reply submissions from said parties by January 27, 2011, submission from the staff by January 31, 2011 and further reply submissions from the private parties by Febuary 2, 2011.

Order No. 37, which issued on January 13, 2011, directed the private parties to report regarding any settlement. Order No. 38, which issued on January 20, 2011, allowed complainant and respondents Funai to conduct the settlement conference required by Order No. 37 before February 1, 2011 in Japan without a representative from the staff present.

Order No. 40, which issued on January 24, 2011, granted the motion of complainant, respondents Panasonic Corporation and Panasonic Corporation of North America (Panasonic), JVC, Victor, Funai, except as to products of Funai that incorporate Zoran ICs, and the remaining

respondents (retailer respondents) to suspend all upcoming deadlines through January 28, 2011 with respect to Panasonic, JVC, and all retailer respondents, except as to products of Funai that incorporate Zoran ICs.

Order No. 41 which issued on Januay 28, 2011, granted complainant's motion to suspend the procedural schedule and evidentiary hearing indefinitely as to respondents Panasonic, Victor, JVC, Crutchfield,[2] Huppin's and Computer Nerds, based on a Memorandum of Understanding (MOU) between complainant and Panasonic as to covered products and parties.

Order No. 42, which issued on January 28, 2011, granted Motion No. 709-73 of complainant and respondents Funai to the extent that the prehearing conference and hearing was to commence on February 7, 2011 and continue on February 8 and 9 as requested by the private parties. A request to modify ground rule 19(x) to permit the exchange of demonstratives no later than twenty-four hours before they were proposed to be used at the hearing was denied.

Order No. 43, which issued on February 4, 2011, related to a stipulation involving importation and Funai and said Order was superceded by Order No. 49, which included a stipulation identical to the Order 43 stipulation but which also includeed citations to certain exhibits. Order No. 44, which also issued on February 4, 2011, related to a stipulation involving respondent Wal-Mart while Order No. 45, which also issued on February 4, 2011, related to a stipulation involving respondents Best Buy Purchasing, LLC, Best Buy.com, LLC, and Best Buy Stores, L.P. Order No. 46 and Order No. 47 which also issued on February 4, 2011 related to

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[2] In a telephone conversation on January 28, 2011 between the attorney adviser and complainant's counsel, and also in an email from complainant's counsel to the attorney advisor, it was represented that respondent B & H Foto & Electronics Corp. is not to be suspended from the investigation, but respondent Crutchfield should be suspended.

stipulations involving respondent QVC, Inc. and respondent B&H, respectively.

Order No. 48, which issued on February 7, 2011, terminated the investigation as to respondents Victor, JVC, B & H, Huppins, Buy, QVC, Crutchfield, and Computer Nerds (Released Respondents) on the basis of withdrawing complainant's claims against said Released Respondents. On February 28, 2011, the Commission non-reviewed Order No. 48. On March 2, 2011, Order No. 50 issued which terminated the investigation as to respondents Panasonic based on a settlement and licensing agreement that resolved the proceeding against said respondents. It also terminated the investigation as to the '306 patent, the '014 patent and claims 1, 8, 22 and 26 of the '455 patent. Hence, only claims 9 and 10 of the '455 patent are in issue in this investigation.

Arguments on several motions in limine were heard on February 3, 2011. A prehearing conference was conducted on February 7, 2011. At said conference, rulings were made on said motions in limine. (Tr. at 33-53.)

A three day evidentiary hearing was conducted on February 7, 8, and 9. The only respondents that participated in the hearing were Funai Electric Co., Ltd., Funai Corporation, Inc., Wal-Mart Stores, Inc., Best Buy Purchasing, LLC, BestBuy.Com, LLC and Best Buy Stores, L.P. Post hearing submissions have been filed.[3] This matter is now ready for decision.[4]

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[3] The staff did not file any rebuttal findings to complainant's proposed findings.

[4] Respondents in their RBr at 50-54 requested that the administrative law judge "reverse his ruling striking Mr. McAlexander's testimony [citing 800:10-814:10; 868:11-892:15; 904:24-913:15]." A motion for reconsideration requires more than simply rearguing points made at the evidentiary hearing. Rather there are only three possible grounds for any motion for reconsideration: "(1) an intervening change in controlling law, (2) the availability of new evidence not previously available, and (3) the need to correct a clear error of law or prevent manifest injustice." Atkins v. Marathon LeTourneau Co., 130 F.R.D. 625, 626 (S.D. Miss. 1990)

The Final Initial and Recommended Determinations are based on the record compiled at the hearing and the exhibits admitted into evidence. The administrative law judge has also taken into account his observation of the witnesses who appeared before him during the hearing. Proposed findings of fact submitted by the parties not herein adopted, in the form submitted or in substance, are rejected as either not supported by the evidence or as involving immaterial matters and/or as irrelevant. Certain findings of fact included herein have references to supporting

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(citing Natural Resources Defense Council v. United States Envtl. Protection Agency, 705 F. Supp. 698, 702 (D.D.C. 1989)). See also Bulley v. Fid. Fin. Servs. of Miss., Inc., 2000 U.S. Dist. LEXIS 13481, 4-5 (S.D. Miss. Sept. 8, 2000); In re King, 2005 Bankr. LEXIS 2896 (Bankr. S.D. Ohio July 15, 2005) ("To constitute 'newly discovered evidence,' the evidence must have been previously unavailable." GenCorp, Inc. v. Am. Int'l Underwriters, 178 F.3d 804, 834 (6th Cir. 1998)(citations omitted).) "As a general principle, motions for reconsideration are granted if the moving party demonstrates: (1) a clear error of law; (2) newly discovered evidence that was not previously available to the parties; or (3) an intervening change in controlling law." Owner-Operator Indep. Drivers Assn v. Arctic Express, Inc., 288 F. Supp. 2d 895, 900 (S.D. Ohio 2003)(citing GenCorp, 178 F.3d at 834). "Motions for reconsideration do not allow the losing party to 'repeat arguments previously considered and rejected, or to raise new legal theories that should have been raised earlier.'" Id., internal citation omitted. The administrative law judge finds that respondents did not establish any of said grounds for a motion for reconsideration. In addition Commission rule 210.15, which relates to motions, was not followed. Thus on procedural grounds, respondents request that the administrative law judge reverse any rulings striking McAlexander's testimony is denied.

Complainant in its CBr at 111, 114 and 118 moved to strike certain of McAlexander's trial testimony. However Commission rule 210.15 was not followed. Hence said motion is also denied on procedural grounds.

Respondents also in their post-hearing submissions requested that "Section IV.A.6 of Freescale's Post-hearing Brief, and CPFF 263-325, be struck, pursuant to Order no. 42..." (RRBr at 50, n. 30) on the ground that complainant's "new argument" was not disclosed in complainant's pre-hearing brief or in Subramanian's expert report. (Id.) However Commission rule 210.15 was not followed. Hence said request is denied.

Respondents in addition in their RFF made reference to numerous motions to strike e.g. ROCPFF 297, which reads "Move to strike... Attorney argument proffered as finding of fact." Because Commission rule 210.15 was not followed, said motions are denied.

evidence in the record. Such references are intended to serve as guides to the testimony and exhibits supporting the finding of fact. They do not necessarily represent complete summaries of the evidence supporting said findings.

II. Jurisdiction Including Parties And Importation

Section 337 of the Tariff Act of 1930, as amended, declares unlawful the importation into the United States, the sale for importation, or the sale within the United States after importation by the owner, importer, or consignee, of articles that infringe a valid and enforceable United States patent if an industry in the United States relating to the articles protected by the patent exists or is in the process of being established. See 19 U.S.C. §§ 1337 (a)(1)(B)(i) and (a)(2). Section 337 also provides that the Commission shall investigate alleged violations of said section and is empowered to hear and decide actions involving alleged unfair acts under the Section. See Certain Steel Rod Treating Apparatus, Inv. No. 337-TA-97, Commission Opinion, 215 U.S.P.Q. 229, 231 (June 30, 1981). Section 337 proceedings are in rem, making in personam jurisdiction unnecessary. However due process requires that the notice of investigation be provided to persons with an interest in the property at issue in a manner reasonably calculated to inform them of the pendency of an action so that they may have an opportunity to appear and defend their interests. Id. at 232, Certain Ammonium Octamolybdate Isomers, Inv. No. 337-TA-477, Init. Det. at 8 (May 15, 2003).

For identification of the private parties in this invesgitation, see Section XIII, FF1-9. With regard to importation, the private parties have entered into several stipulations concerning, for example, the importation requirement and domestic inventory of accused products. See Order No. 49 (Feb. 9, 2011), Order No. 44 (Feb. 4, 2011), and Order No. 45 (Feb.4, 2011). Hence the

Commission possesses subject matter jurisdiction.

Respondents have participated in the evidentiary hearing in this investigation and have not pleaded an affirmative defense of lack of personal jurisdiction. See Certain SteelRod Treating Apparatus, Inv. No. 337-TA-97, Order No. 13 (May 8, 1981) (noting that failure to consolidate threshold procedural matters in a timely manner constitutes waiver), aff'd on other grounds, Commission Memorandum Opinion at 3 (June 29, 1981). Hence the Commission also possesses personal jurisdication.

III. Technology In Issue

The parties have stipulated to the following general overview of technology in issue (JX-2):

> 1. The technology at issue relating to the '455 patent involves, inter alia, bus termination circuitry that may be enabled or disabled to reduce unwanted signal reflection on a bus. A bus may be used to transmit signals between two or more devices (e.g., a memory device, communication device, interface device or peripheral device). Depending on the direction of the signal, a given device may be a sender or a receiver. A bus on which signals may be transmitted in either direction is known as a "bidirectional" bus.
>
> 2. Signal reflection may occur when the load impedance of the receiver does not match the characteristic impedance of the conductive path, e.g., wiring between two devices on a printed circuit board connected by a bus or one or more conductive traces. When the impedance of the receiving device and the conductive path are not matched, the signal partially bounces off or "reflects" from the receiver.
>
> 3. Signal reflection interferes with the transmitted signal which may cause transmission of signals to the conductive path to be slowed and/or altered in amplitude. A reduction in signal reflection, therefore, allows a more rapid signal propagation. on the conductive path. Signal reflection can be reduced by using termination such as adding an impedance at or near the receiving end of a conductive path.

4. Among the methods of terminating a conductive path, known at the time of the '455 patent's filing, was through the addition of a resistor at or near the receiving end. Other known methods included adding a capacitor, a PN junction, a diode, a resistive device, an inductor, an N channel transistor, a P channel transistor, a junction field effect transistor (JFET), a metal oxide semiconductor transistor (MOSFET), a bipolar device, a Bi-CMOS device, a current source, a voltage source, or any other like termination component or circuit to the receiving end of the conductive path. Permanently connected termination circuitry usually caused increased power consumption.

5. The '455 patent describes determining whether, for example, a data processor will be receiving data or sending data external to the processor. In one embodiment of the '455 patent, the disclosed termination circuitry is enabled if the data processor is receiving data from the bus in order to reduce signal reflection when the processor is receiving a signal from the bus. The disclosed termination circuitry is disabled if the data processor is sending data to the bus. The '455 patent calls this "dynamic termination." When the data is incoming, i.e., the data processor is receiving, the termination circuitry is enabled. When the data is outgoing, i.e., the data processor is transmitting, the termination circuitry is disabled.

6. In one embodiment of the '455 patent discloses that a control signal is used to enable the disclosed termination circuit. The enabled termination circuit electrically "couples" a circuit component to the bidirectional bus. The circuit component, when "coupled" to the bus, provides termination to the bus. When the control signal is not asserted, the disclosed circuit component is not electrically "coupled" to the bidirectional bus.

7. In one embodiment, the '455 patent also discloses that a series of control signals may be used to activate multiple termination circuits within a given device. When a given control signal is sent, the termination circuit responding to that control signal electrically couples the respective termination circuit component to the bidirectional bus. In this way, the '455 patent discloses the ability to adjust the termination impedance that is "coupled" and "decoupled" from the bus by selectively enabling one or more of the termination circuits.

IV. Experts

Vivek Subraramanian was qualified at the hearing as complainant's expert in the field of

electrical engineering and integrated circuits. (Tr. at 21.) Joseph C. McAlexander III was qualified at the hearing as respondents' expert in the field of electrical engineering and integrated circuits. (Tr. at 647.)

V. Person of Ordinary Skill

The level of ordinary skill in the art of the '455 patent is at least a Bachelor of Science degree in electrical engineering or equivalent, with a few years of experience, particularly focused on issues related to memories and memory systems such as described in the "Background Of The Invention" section of the '455 patent. (JX-1; Subramanian, Tr. at 122-3, McAlexander, Tr. at 673.)

VI. Claims in Issue

Asserted claim 9 of the '455 patent states:

> A data processor within an integrated circuit package comprising:
>
> an execution unit internal to the data processor;
>
> a plurality of external pins connected to the integrated circuit package, the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus;
>
> a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one bus termination circuit, the plurality of bus termination circuits providing data to or receiving data from the execution unit, each bus termination circuit in the plurality of bus termination circuits having an input for receiving a control signal;
>
> a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one

circuit component from the bus.

(JX-1 at 10:26-52.)

Asserted claim 10 of the '455 patent states:

> The data processor of claim 9 wherein the at least one circuit component is a circuit component selected from a group consisting of: a capacitor, a diode, a resistor, a transistor, a voltage source, a current source, an electrical short circuit, and an inductor.

(JX-1 at 10:53-57.)

VII. Claim Construction

The claims of a patent define the invention to which the patentee is entitled the right to exclude. Phillips v. AWH Corp., 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (Phillips). The words of a claim are generally given their ordinary and customary meaning. Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996). The ordinary and customary meaning of a claim term is the meaning the term would have to a person of ordinary skill in the art at the time of the invention, i.e., constructively the effective filing date of the patent application. Phillips, 415 F.3d at 1313. The ordinary meaning of a claim term as understood by a person of ordinary skill in the art may in some circumstances be readily apparent to laymen. See Brown v. 3M, 265 F.3d 1349, 1352 (Fed. Cir. 2001). However, "[w]hen the parties present a fundamental dispute regarding the scope of a claim term, it is the court's duty to resolve it." O2Micro Int'l Limited v. Beyond Innovation Technology Co., 521 F.3d 1351, 1362 (Fed. Cir. 2008). When giving a claim term meaning, "the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." Phillips, 415 F.3d at 1313. In construing the claims, the court should also consider "the patent's prosecution history, if it is in evidence."

Markman v. Westview Instruments, Inc., 52 F,3d 967, 976, 980 (Fed. Cir. 1995).

While information extrinsic to the patent and its prosecution history may be considered, it is often "less reliable than the patent and its prosecution history." Phillips, 415 F.3d at 1318 (noting that litigation-derived expert reports and testimony are especially suspect). "[E]xpert testimony at odds with the intrinsic evidence must be disregarded." Network Commerce, Inc. v. Microsoft Corp., 422 F.3d 1353, 1361 (Fed. Cir. 2005) (holding that unsupported conclusions concerning patent claims provide little support for suggested claim construction). Not all extrinsic information, however, must be disregarded. For example:

> [i]n some cases, the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words. See Brown v. 3M,265 F.3d 1349, 1352 (Fed Cir. 2001) (holding that the claims did "not require elaborate interpretation"). In such circumstances, general purpose dictionaries may be helpful.

Phillips 415 F.3d at 1314. However, in many cases that give rise to litigation, determining the ordinary and customary meaning of a claim requires examination of terms that have a particular meaning in a field of art. Because the meaning of a claim term as understood by persons of skill in the art is often not immediately apparent, and because patentees frequently use terms idiosyncratically, the court looks to those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean. Id. Those sources include the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art. See Gemstar-TV Guide Int'l, Inc. v. Int'l Trade Comm'n, 383 F.3d 1352, 1364 (Fed. Cir.2004); Vitronics, 90 F.3d at 1582-83; Markman, 52 F.3d at 979-80.

At issue are claims 9 and 10 of the '455 patent.

A. The claimed phrases "circuit" and "circuitry"

The claimed phrase "circuit" appears in asserted claim 9. The phrase "circuitry" does not appear in either asserted claim 9 or 10.

Complainant argued that neither of these claimed phrases need to be construed, as its expert testified that there was no difference or contradiction between the parties proposed plain and ordinary meanings. (CBr at 57.) Complainant further argued that, to the extent the administrative law judge deems a construction to be necessary, "circuit" and "circuitry" should both be construed as an "assemblage of electronic elements." (CBr at 57.)

Respondents argued that complainant and respondents agreed that said claimed phrases should be given their plain and ordinary meaning, which respondents assert is "an interconnection of circuit elements," in accordance with the specification. (RBr at 70.) Respondents further argued that complainant's expert opined that there was no substantive difference between complainant's construction, which is an "'assemblage' of elements," and respondents' construction. (RBr at 70.)

The staff argued that the claimed phrase "circuit" should be accorded its plain meaning, as there is no dispute. (SBr at 12.)

As circuitry is no longer a claimed phrase and the parties agree that neither "circuit" nor "circuitry" need to be construed, and that the exact definition does not substantively affect issues in this investigation, the administrative law judge accords these terms their plain and ordinary meaning, which he will take to be an assemblage of electronic elements, i.e. complainant's construction instead of respondents' construction, because respondents use a term to be defined

(viz. circuit) in the definition of that term, which is to be avoided. The administrative law judge does, however, understand that there is no substantive difference between the definitions of respondents and complainant.

B. The claimed phrase "circuit component"

This claimed phrase is in asserted claims 9 and 10.

Complainant argued that there is no longer a dispute as to the claimed phrase in issue; that respondents did not present any construction for it at the hearing beyond plain and ordinary meaning; and that complainant has no objection to staff's construction, which is "circuit element that provides an impedance for termination." (CBr at 19-20.)

Respondents argued that all parties agree that the proper construction for the claimed phrase is "a circuit element that provides impedance for termination." (RBr at 54.)

The staff argued that said claimed phrase should be construed as "circuit element that provides an impedance for termination." (SBr at 9.)

The parties assert that the term "circuit component" should be understood to mean "circuit element that provides impedance for termination." (RFF 159 (undisputed).) Claim 9 reads in relevant part:

> to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus.

(JX-1 at 10:47-52 (emphasis added).) Thus, the circuit component must reduce signal reflection on the bus. The specification also discloses:

> The termination circuit contains one or more circuit components which when coupled to the data line reduce reflection or change line

> impedance on the bi-directional external bus 17 when data is being received by the device 10. The circuit components may include one or more of a capacitor, a PN junction, a diode, a resistor, a resistive device, an inductor, an N channel transistor, a P channel transistor, a junction field effect transistor (JFET), a metal oxide semiconductor transistor (MOSFET), a bipolar device, a Bi-CMOS device, a current source, a voltage source, any other like termination component, or a circuit comprising one or more of the circuit elements listed above.

(JX-1 at 4:28-40 (emphasis added).) Thus, the specification discloses that a circuit component changes impedance on the bus. Based on the intrinsic evidence cited, supra, the administrative law judge finds that a "circuit component" is an element of a circuit, viz., "an assemblage of electronic elements," as defined, supra, that provides impedance for termination, which finding is consistent with the agreement, supra, of the parties.

C. The claimed phrase "bus termination circuit"

This claimed phrase is in asserted claim 9.

Complainant argued that "bus termination circuit" should be construed to mean "circuitry for signal termination that is selectively enabled or disabled in response to a control signal whose assertion is based, at least in part, on the direction of data signals on the bus." (CBr at 10.) Complainant further argued that its construction is supported by the intrinsic evidence, including the summary of the invention, the rest of the specification, and even the title of the patent. (CBr at 10.) Complainant further argued that each embodiment disclosed in the '455 patent includes the direction of data in the determination of enabling the termination circuitry. (CBr at 11.)

Respondents argued that this claim phrase should be construed as "circuitry for signal termination that is selectively enabled or disabled in response to a control signal." (RBr at 58.) Respondents further argued that the language of claim 9 shows that a bus termination circuit can

be operated by use of a single control signal (RBr at 59); that the use of directional control signals is only an embodiment of the '455 patent, not the invention; and that the termination circuits described in the '455 patent are not limited to circuits that must be enabled or disabled based on data directionality. (RBr at 60-61.)

The staff argued that "bus termination circuit" means "circuitry for signal termination that is selectively enabled or disabled in response to [a] control signal whose assertion is based, at least in part, on the direction of data signals on the bus." (SBr at 9.)

The language of asserted claim 9 reads in relevant part:

> a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one bus termination circuit, the plurality of bus termination circuits providing data to or receiving data from the execution unit, each bus termination circuit in the plurality of bus termination circuits having an input for receiving a control signal; and
>
> a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus.

(JX-1 at 10: 33-52 (emphasis added).) Thus, pursuant to the language of the claim, each bus termination circuit has an input for receiving a control signal, which control signal determines if the bus termination circuit couples or decouples "at least one circuit component." Further, the parties agree that a bus termination circuit is, at least, "circuitry for signal termination that is selectively enabled or disabled in response to a control signal..." See, supra. Respondents

disagreed, however, that the assertion of said control signal is "based, at least in part, on the direction of data signals on the bus", as contended by complainant and the staff. (RBr at 60.)

The plain language of the claim does not directly require that the control signal be asserted based on the direction of data signals on the bus; i.e., whether the bus termination circuits are "providing data to or receiving data from" the execution unit. Asserted claim 9, however, does require that when the control signal is asserted, the bus termination circuit "couple at least one circuit component to the bus to reduce signal reflection on the bus..." and when the control signal is deasserted, that the bus termination circuit "decouple at least one circuit component from the bus."

With reference to the specification, the Summary of the Invention states that:

> The previously mentioned disadvantages are overcome and other advantages achieved with the present invention. In one form, the present invention comprises a method for determining whether to enable termination circuitry within a data processor. A bus transfer begins through a bus coupled between the data processor and a device external to the data processor. A determination is made as to whether the data processor is receiving data or sending data external to the processor. The termination circuitry is enabled if the data processor is receiving data from the bus in order to reduce signal reflection on the bus. The termination circuitry is disabled if the data processor is sending data through the bus.

(JX-1 at 1:44-57 (emphasis added).) Thus, signal reflection is only a problem when receiving data from the bus. Moreover, in describing the preferred embodiment, the '455 patent reads:

> In general, the apparatus and method illustrated herein is designed to dynamically enable the proper termination inside a receiver at the end of the bi-directional bus. The proper termination is dynamically connected to the bus only when data is being received in order to reduce signal reflection on the bus (i.e. transmission line effects) and allow for a more rapid operational speed. This dynamic bus termination requires a control signal which indicates to the receiving device the current drive direction

> of the bus (i.e., is data being read from the device or is data being written to the device). When this control signal indicates the bus has a voltage and/or current which is being driven into the receiving device, the receiving device turns on its termination devices to dampen the incoming signal so no reflections are sent back down the bus (transmission line). When the control signal indicates the bus is not being driven into the receiving device the receiving device's terminators are turned off to reduce the load on the bus and power dissipation of the bus.
>
> * * *
>
> Specifically, the apparatus and method illustrated herein provides the ability to dynamically terminate a bi-directional bus depending on the current bus drive direction.

(JX-1 at 2:53 - 3:4, 3:44-46 (emphasis added).) Thus, as seen in the preferred embodiment, termination circuitry is enabled if the data processor is receiving data from the bus in order to reduce signal reflection. Moreover, the purpose of the invention as stated in the Field of the Invention section of the '455 patent is that the "present invention relates generally to data processors, and more particularly, to dynamic termination of conductive bus lines to avoid signal reflection." (JX-1 at 1:6-8 (Field of the Invention).) Therefore, based on the language of asserted claim 9 and the specification, the administrative law judge finds that "signal reduction" is a requirement of asserted claim 9, and signal reduction only occurs when data is being received by the execution unit. Hence, the administrative law judge finds that a "bus termination circuit" is circuitry for signal termination that is selectively enabled or disabled in response to a control signal whose assertion is based, at least in part, on the direction of data signals on the bus.

Respondents argued that the second paragraph of the Summary of the Invention shows that "another form" of the invention exists that does not require the control signal be asserted based on the direction the data is flowing, and further rely on Fig. 8 and related text as showing an

embodiment that likewise does not have that requirement. (RBr at 60-61, RRBr at 27-28.) Said second paragraph, however, restates the invention as an apparatus, as opposed to the first paragraph of the summary, which describes a method. Moreover, regarding Fig. 8 and the related text in the specification, Fig. 8 relates back to Fig. 5 and the "present invention." (See JX-1 at 2: 38-41 ("FIG. 8 illustrates, in a block diagram, yet another inter-connection of the plurality of independently-enabled bus termination circuits of FIG. 5 in accordance with the present invention.").) Fig. 5 asserts or deasserts bus termination based on a control signal as does Fig. 1 in accordance with the present invention, which is consistently described as being asserted based on the direction the data is flowing. Also, as the administrative law judge has found, supra, the language of asserted claim 9 requires that a bus termination circuit "couple at least one circuit component to the bus to reduce signal reflection on the bus..." and that said signal reflection only occurs when data is being received.

D. The claimed phrase "execution unit"

This claimed phrase is in asserted claim 9.

Complainant argued that this term should be construed in accordance "with the meaning used in the specification, which is 'a portion of an integrated circuit at least partially software driven by microcode and/or nanocode.'" (CBr at 9.) Complainant further argued that "execution unit" did not have a commonly used meaning at the time of the '455 invention, and no other explanation in the specification exists. (CBr at 9; see also CPFF 133.)

Respondents argued that an "execution unit" is "a portion of an integrated circuit that executes commands and instructions." (RBr at 54.) Respondents further argued that the specification lists an execution unit as one of several possible integrated circuits, and thus that

complainant is attempting to read a limitation from the specification into the claim (RBr at 55) and that a person of ordinary skill in the art at the time the asserted '455 patent was filed would have understood "execution unit" to be a portion of a processor that executed computer instructions. (RBr at 56.)

The staff argued that an "execution unit" should be "a portion of an integrated circuit that executes commands or instructions." (SBr at 9.) The staff further argued that there is no support in the intrinsic record for mandating "at least partially software driven by microcode and/or nanocode" as argued by complainant. (SBr at 9.)

The claimed phrase, "execution unit" as found in asserted claim 9 is merely described as follows:

> "an execution unit internal to the data processor ... the plurality of bus termination circuits providing data to or receiving data from the execution unit...

(JX-1 at 10:28, 10:37-39.)[5] Thus, all that can be determined from the claim language is that the execution unit is contained by the data processor, and can send and receive data.

In the specification, the paragraph which mentions an execution unit reads:

> The invention can be further understood with reference to the FIGS. 1-7. FIG. 1 illustrates a data processing system. The data processing system has a device 10 and a device 12 (referred to also as communication devices since they communicate to one another). Generally, device 10 and device 12 are each integrated circuits. For example, either device 10 or device 12 may be a memory device (such as a SRAM, a DRAM, a EEPROM device, an EPROM device, a flash device, and the like), an interface device, any peripheral device, a DMA device, a communication device, a timer, analog circuitry, a microprocessor, a pipelined execution device, an application specific integrated circuit

[5] The claimed phrase "execution unit" also appears in non-asserted claim 14 of the '455 patent, using substantially the same language as asserted claim 9. (JX-1 at 11:13, 11:19-21.)

> (ASIC) device, a programmable logic array (PLA), hard-wired logic, an execution unit at least partially software driven by microcode and/or nanocode, a plurality of execution devices, a digital signal processor (DSP), a computer, a data processor, a central processing unit (CPU), and integrated circuit, and/or the like.

(JX-1 at 3:64-11:14 (emphasis added).) Thus, an execution unit is listed as an example of an integrated circuit, and could be used as either device 10 or device 12 in Fig. 1. Device 10 is later described "[t]he enable signal, in general, is in one logic state if a data is incoming to the device 10 and is deasserted when data is being sent out from the device 10." (JX-1 at 4:44-45.) Hence, an execution unit is further seen to be a device that can send and receive data. Moreover, the parties agree that an "execution unit" is a portion of an integrated circuit. (See, supra.) The administrative law judge finds nothing in the specification that defines an execution unit, except to the extent that it is capable of performing certain functions.

Based on the foregoing, the administrative law judge finds that an "execution unit" is "a portion of an integrated circuit that executes commands or instructions."

E. The claimed phrase "the plurality of bus termination circuits providing data to or receiving data from the execution unit..."

This claimed phrase is in asserted claim 9.

Complainant argued that the language "providing data to or receiving data from..." in the claimed phrase in issue should be accorded its plain and ordinary meaning. (CBr at 24.) Complainant further argued that respondents' requirement of active participation of the bus termination circuit is not warranted; that the word "providing" is used in the specification in ways that do not support respondents' construction; and that there is no support for respondents' assertion that claim 9 is described solely by Fig. 8. (CBr at 24-26.) With respect to the word

"or," complainant argued that, when reading the entirety of claim 9, it is clear that because the claim requires bi-directional communication, the bus termination circuits must be able to both provide and receive data. (CRBr at 55.)

Respondents argued that the word "providing" should be accorded its plain meaning of "to pass" or "to supply" and that complainant agreed. (RBr at 65.) Further, respondents argued that "providing" must also require that a bus termination circuit actively participate in the exchange of data to and from the "execution unit"(RBr at 68) and that the specification in describing Fig. 8 shows that "the drafter of the specification correctly uses the verb 'provide' in connection with the 'assertion' of an enable signal, an active step..." (RBr at 66-67.) With respect to the word "or," respondents argued that although the parties all agreed that or should be given its plain and ordinary, complainant asserted at the hearing that "or" is the same as "and," and respondents further argued that the Federal Circuit has rejected such an interpretation and that complainant has demonstrated no valid reason to depart from using "or" in the disjunctive. (RBr at 68-69.)

The staff argued that nothing in the intrinsic record mandates the "narrow construction proposed by Mr. McAlexander and Respondents to require 'active' participation by the termination circuits" and therefore that this claim phrase should be accorded its ordinary meaning. (SBr at 11.)

The parties all agree that the plain and ordinary meaning of "providing" includes "supplying" and that the plain and ordinary meaning of "receiving" includes "taking" or "getting." (CBr at 24; RBr at 65; RRBr at 41, n. 25; SBr at 11.) Asserted claim 9 reads in relevant part:

> an execution unit internal to the data processor;

> a plurality of external pins connected to the integrated circuit package, the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus;
>
> a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one bus termination circuit, the plurality of bus termination circuits providing data to or receiving data from the execution unit, each bus termination circuit in the plurality of bus termination circuits having an input for receiving a control signal;

(JX-1 at 28-41 (emphasis added).) Thus, a bus termination circuit is connected to an external pin and the execution unit. As the language of the claims indicates, the bus termination circuit either provides (or supplies) data to, or receives (or takes or gets) data from the execution unit. Since the bus termination circuit is connected to an external pin and the execution unit, which execution unit is internal to the data processor, and the language of asserted claim 9 states "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor...," the administrative law judge finds that it is a requirement of the claim that the bus termination unit can both provide and receive data; not do only one or the other. With respect to "providing," nothing in the claim language indicates the manner that said data is provided.

With respect to the specification, although the words "provide," "provides," and "providing" are used therein, the administrative law judge has found no use of those words relating to the bus termination circuit's communication with an execution unit or the data processor. Thus, Figs. 1, 2, and 5 are block diagrams that show data entering and leaving the "dynamic bus termination circuit 14." (See, inter alia, JX-1 at 4:15-20 (describing Fig. 1); JX-1 at 7:9-11 (stating that elements of Fig. 1 which are analogous to elements in Fig 5 are identically labeled).) It is noted that in Figs. 1 and 5, in device 10, there is a "bi-directional bus 13,"

represented by a double-headed arrow, connectng "dynamic bus termination circuit 14" to the "bi-directional bus" 17 and a double-headed arrow labeled "DATA" connecting dynamic bus termination circuit 14 to a "data unit" 18. In Fig. 2, bi-directional bus 17 is connected to a double-headed arrow which is drawn through bus termination circuit 14. Therefore, the administrative law judge finds that the specification supports and further explains the limitation in asserted claim 9 requiring that the bus termination circuit be capable of either providing or receiving data. With the exception of what occurs when the bus termination circuit must reduce signal reflection, neither the claims nor the specification put any further restriction on what the bus termination circuit must do when it provides or receives data to or from the execution unit. Hence, the administrative law judge accords the claimed phrase "providing data to or receiving data from" its plain meaning, i.e. "the plurality of bus termination circuits supplying data to or getting data from the execution unit," as defined herein.[6]

Respondents argued that the claim term "providing" should be accorded its plain meaning. (RBr at 68.) Respondents further argued that, to the extent it requires interpretation, it "means a bus termination circuit that actively participates in the exchange of data to and from the 'execution unit'" (RBr at 68), which is inconsistent with the argument that the term would be understood by a person of ordinary skill in the art to have its plain meaning. (Compare RBr at 65 (""providing' should be construed according to its plain and ordinary meaning..." with RBr at 66 ("the drafter of the specification correctly uses the verb 'provide' in connection with the 'assertion' of an enable signal..."); also compare RBr at 65 ("The term 'providing' is not a highly

[6] The claimed phrases "bus termination circuit" and "execution unit," referred to here, are separately construed

technical term. Rather, it is a prosaic term.") with RBr at 65 ("Most significant here is that the term 'providing' is used in connection with the description of a second embodiment...").)

Referring to respondents' argument that the claimed phrase "providing" requires active participation in the exchange of data, the bus termination circuit is required to both provide and receive data, as found, supra. In a separate limitation, the bus termination circuit as recited in claim 9 of the '455 patent is required to perform signal reduction. (See Section C, supra, (finding that a bus termination circuit performs signal reduction when data is being received by the execution unit).) Thus, claim 9 requires the bus termination circuit to perform some action when receiving data, but requires no action when "providing" data in a prior limitation. The administrative law judge finds nothing in the claim language which associates "providing" with any activity. Respondents make further reference to the specification at, inter alia, JX-1 at 1:66-2:2 ("The circuitry for terminating has a second input/output terminal for providing or receiving data from internal to the communication device.") and argued that the cited portion of the specification "clearly describes a structure, the 'second input/output terminal' that must perform an act, i.e., 'provid[e] or receiv[e] data from internal to the communication device." However, the cited portion of the specification does not relate to the claimed phrase at issue. Further, the administrative law judge has found nothing in the specification, including the citation by respondents, supra, that supports the argument that the plain meaning of the word "providing" requires "active participation."

F. The claimed phrase "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus"

This claimed phrase is in asserted claim 9.

Complainant argued that the parties agreed that this claimed phrase should be accorded its plain and ordinary meaning, but that the parties disagreed as to what that meaning is; that respondents' interpretation that external bus must be between the plurality of external pins and the data processor which is internal to the integrated circuit is not supported by the plain language of the claims; that the logic bits must travel to and from the data processor "via an external bus," consistent with common sense and the specification; that respondents' interpretation is admittedly nonsensical and thus can only be correct if the claim is "susceptible to only one reasonable interpretation" (emphasis in original) but that the grammar here does not require that result; and respondents' interpretation is unsupported in the specification. (CBr at 20-24.) Complainant further argued that if this claimed phrase needs to be construed, it should be "the plurality of external pins used to bidirectionally communicate logic bits traveling to and from the data processor via an external bus." (CBr at 20.)

Respondents argued that the parties agree that the word "via" should be construed according to its plain meaning of "by way of" or "through"; that the claimed phrase in issue is unambiguous and therefore the specification need not be consulted with respect to its interpretation; that basic grammar "requires that the logic bits travel from the external pins, through the external bus, and then onto the data processor (and vice versa)." (RBr at 61.) Respondents further argued that complainant's construction parses and shifts clauses "in a manner inconsistent with the unambiguous language of the limitation as written. (RBr at 62.)

The staff argued that this claimed phrase should be construed as "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor, the logic bits traveling to and from the data processor via an external bus." (SBr at 10.)

Although the private parties both depend on "plain and ordinary meaning," their interpretation differs. Thus, there is a dispute between the parties. The preamble of the asserted claim reads: "A data processor within an integrated circuit package comprising...," meaning that the data processor is within an integrated circuit. The full language of the limitation containing the claimed phrase at issue reads:

> a plurality of external pins connected to the integrated circuit package, the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus...

(JX-1 at 10:30-34.) Thus, pursuant to said language, the "external pins" are a part of the data processor and are connected to the integrated circuit package. Said language also discloses that said external pins are used to communicate logic bits "to and from the data processor." What the data processor is communicating with, precisely, is not specified, except that it must be within the integrated circuit package. The claimed phrase at issue also indicates that communication with the integrated circuit package is "via an external bus." The parties agreed that an understanding of "via" as "by way of" or "through" is consistent with the specification of the '455 patent. (RFF 186 (undisputed).)

With respect to the specification, the Summary of the Invention reads in relevant part:

> A bus transfer begins <u>through a bus coupled between the data processor and a device external to the data processor</u>. A determination is made as to whether the data processor is receiving data or sending data external to the processor. The termination circuitry is enabled if the data processor is receiving data from the bus in order to reduce signal reflection on the bus. The termination circuitry is disabled if the data processor is sending data through the bus.

(JX-1 at 1:49-57 (emphasis added).) Thus, the bus is described as being the means of communication between the data processor and an external device. Fig. 1 and the related text in

the specification describe a dynamic bus termination circuit 14 attached to an external integrated circuit data pin, which is in turn attached to an external bus 17. (See, inter alia, JX-1 at Fig. 1; JX-1 at 4:15-17 ("The device 10 has a dynamic bus termination circuit 14 connected via at least one conductor or a bi-directional bus 13 to one or more external integrated circuit data pins."); JX-1 at 4:28-31 ("The termination circuit contains one or more circuit components which when coupled to the data line reduce reflection or change line impedance on the bi-directional external bus 17 when data is being received by the device 10.").) Based on the foregoing intrinsic evidence including the specification, the administrative law judge finds that the claimed phrase in issue should be construed as "a plurality of external pins used to bidirectionally communicate logic bits from the data processor, the logic bits traveling to and from the data processor via an external bus."

Respondents have argued that the claim language is unambiguous and therefore the specification is "irrelevant to the understanding of the claim term." (RRBr at 39 (emphasis in original); see also RBr at 63.) For support, respondents cite Chef America, Inc. v. Lamb-Weston, Inc., 358 F.3d 1371, 1374 (Fed. Cir. 2004) ("where as here, the claim is susceptible to only one reasonable interpretation, the canons of claim construction [] are inapposite, and we must construe the claims based on the patentee's version of the claim as he himself drafted it.") (Chef America). In Chef America, the claim language at issue was "heating the resulting batter-coated dough to a temperature in the range of about 400 degrees F. to 850 degrees F." The central dispute was over whether or not the word "to" could be read as "at," despite the fact that there was no special definition in the specification of "to." The Court found that the patentee had specifically chosen the word "to" during prosecution. Id. at 1374. Also, in that case, Chef

America's baking expert could not explain why a person of ordinary skill in the art would read "to" as "at," but depended on the fact that it was well known that if the dough itself was heated to that temperature, instead of at that temperature (i.e., in an oven heated to that temperature) an unusable product would result. Chef America at 1375. In summary, it was a single word at issue, which word was specifically chosen by the patentee with no special meaning defined in the specification. In contrast, in this investigation, where the private parties purport to depend on the plain and ordinary meaning (instead of a changed meaning), the meaning of specific words is not at issue as it was in Chef America, and there is a dispute as to how the claim phrase taken as a whole is interpreted. (RBr at 61-62; CBr at 20-21; SBr at 10-11.)

G. The claimed phrases "couple" and "decouple"

The claimed phrases are in asserted claim 9.

Complainant argued that the parties agree that "couple" and "decouple" should be construed as "to electrically connect to" (CPFF 127 (undisputed)) and "electronically disconnect from" (or "not electrically connect[ed] to") (CPFF 128 (undisputed); CBr at 27.) Complainant further argued that the way that respondents apply that construction is unsupported and illogical. (CBr at 27-32.)

Respondents argued that the parties agreed that "couple" means"electrically connected to" and "decouple" means "not electrically connected to." (RBr at 70.) Respondents further argued that complainant is now arguing for a new construction of decouple meaning "complete[] an electrical circuit to reduce signal reflection on the bus..." (RRBr at 50); that such an interpretation imports a limitation from the specification into the claim (RRBr at 51); and that there is no support in the specification for complainant's "new" construction (RRBr at 51-52).

The staff argued that "couple" and "decouple" mean, respectively, "to electrically connect [to]" and "to electrically disconnect [from]." (SBr at 11-12.)

The claimed phrase "couple" or "coupled"occurs within two elements of asserted claim 9, while the claimed phrase "decouple" occurs once in the last element of asserted claim 9. Specifically, a bus termination circuit "coupled" to an external pin (JX-1 at 10:35-37); a conductor coupled to "each input of each of the bus termination circuits." (JX-1 at 10:42-44) and a circuit component coupled to the bus (JX-1 at 10:47-48), and then decoupled from the bus. (JX-1 at 10:51-52.) Thus, some connection allowing communication is apparent.

As per the Summary of the Invention:

> A bus transfer begins through a bus coupled between the data processor and a device external to the data processor.
>
> * * *
>
> the invention comprises a data processing system having a communication device having at least one external pin connected external to the communication device. The at least one external pin is coupled to receive data from external to the communication device and transmit data external to the communication device. The communication device has circuitry for terminating. The circuitry for terminating has a first input/output terminal coupled to the at least one external pin via at least one data line. The circuitry for terminating has a second input/output terminal for providing or receiving data from internal to the communication device. The circuitry for terminating has an input for receiving an enable signal and has one or more termination component(s). The enable signal couples the termination component to the at least one termination pin when the enable signal is asserted, and decouples the termination component from the at least one termination pin when the enable signal is deasserted.

(JX-1 at 1:49-51, 1:58-2:8 (emphasis added).) Based on the foregoing, "couple" means that there must be a sufficient connection for communication to occur. The specification also discloses:

> The termination circuit contains one or more circuit components which when coupled to the data line reduce reflection or change line impedance on the bi-directional external bus 17 when data is being received by the device 10.

(JX-1 at 4:28-31 (emphasis added).) Thus it is seen that when coupled to the external bus, the circuit components are expected to have a definitive affect on the external bus.

Later, the specification reads:

> A circuit component 104, used to dynamically reduce signal reflection, has a first terminal connected to the emitter of transistor 102 and a second terminal connected/coupled to the bus 17 (output buffers, input buffers, and input/output (I/O) buffers, as needed, are not specifically illustrated in FIGS. 1-2). The transistor 108 has an emitter connected to a ground potential, a collector, and a base connected to the enable signal. A component 106, similar to component 104, has a first terminal connected/coupled to the bus 17 and a second terminal connected to the collector of transistor 108.

(JX-1 at 6:2-12 (emphasis added).) Thus, the specification uses the word "coupled" as synonymous with "connected."

Based on the foregoing, the administrative law judge accepts the party's agreed-to language; i.e., that "couple" means "electrically connect to" and "decouple" means "electrically disconnect from."[7]

In their briefs, the private parties have made several arguments related to the particular use of the claimed phrases "couple" and "decouple" with respect to the "at least one circuit component." (CBr at 27-32; RRBr at 49-57.) Thus, the parties appear to be attempting to interpret the entire claim limitation rather than just the claimed phrases "couple" and "decouple."

---

[7] Whether an accused product practices the claimed element; i.e., actually couples and decouples a circuit component as per the claim construction herein, is a question of infringement, not claim construction.

Specifically, complainant argued that decoupling is the opposite of coupling; that the claim limitation expressly requires that "electrically connecting the termination circuitry completes an electric circuit 'to reduce signal reflection on the bus...'"; and that electrically disconnecting must break the electrical circuit. (CBr at 28-29.) Respondents argued that complainant is importing a limitation that "coupled" must mean "complete[] an electrical circuit to reduce signal reflection on the bus..."; and that complainant has pointed to nowhere in the specification that justifies its reading "that when the circuit component in Figure 2 is 'floating' (a term which is mentioned nowhere in the '455 patent but one that used often by Dr. Subramanian in the hearing... the component is somehow 'decoupled'..."(RRBr at 52.) The staff argued that the private parties "have different understandings of what it means to be electrically connected to and disconnected from..."; however, it supported the agreed-upon construction. (SBr at 11-12.)

The claim element at issue reads:

> a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus.

(JX-1 at 10:42-52.) Thus, said claim element, supra, taken as a whole, requires that the "at least one circuit component" be coupled to the bus "to reduce signal reflection on the bus" when a control signal is asserted, and said circuit component must be decoupled when said control signal is deasserted. Thus, the circuit component must be electrically disconnected from the bus, such that it, inter alia, can no longer reduce signal reflection on the bus. The administrative law judge

finds that this reading is supported in multiple sections of the specification. (See, inter alia, JX-1 at 1:53-55 ("The termination circuitry is enabled if the data processor is receiving data from the bus in order to reduce signal reflection on the bus."); JX-2 at 2:4-8 ("The enable signal couples the termination component to the at least one termination pin when the enable signal is asserted, and decouples the termination component from the at least one termination pin when the enable signal is deasserted."); JX-2 at 2:63-3:4; 5:5-20; 6: 20-22, 40-45; 7:21-26.)

VIII. Zoran Datasheets And Schematics

At the evidentiary hearing on February 8, 2011, complainant requested admission of certain third party Zoran Corporation (Zoran)[8] documents including datasheets CX-1411C, CX-1412C, CX-1413C, and CX-1414C and schematics CX-1417C. The respondents objected to the admissibility of said documents. (See Tr. at 603-6.) In arguing for the admissibility of said documents, counsel for complainant indicated that complainant would not be able to prove infringement by a preponderance of the evidence if said documents were not admitted:

> JUDGE LUCKERN: Let me ask you this question: I haven't decided what I'm going to do, I don't know what I'm going to do, but if I kept them out and struck them and all the testimony that goes along with it, would you still believe that you could show infringement by a preponderance of the evidence?
>
> MR. HOFFMAN: No, Your Honor, we would not be able to.

(Tr. at 601.) Said exhibits are said datasheets CX-1411C, CX-1412C, CX-1413C, and CX-1414C and schematics CX-1417C, which complainant asserted show the relevant functionality of accused products. The administrative law judge overruled respondents' objection, admitted said exhibits, and encouraged the parties to present arguments in the post-hearing briefs, findings of

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[8] Zoran is a third-party that provides certain integrated circuit chips to Funai, and said integrated circuit chips are incorporated into the accused Funai products. (See CBr at 38.)

fact, and rebuttal findings of fact regarding the weight, if any, the administrative law judge should give to said exhibits in making a determination on infringement.[9] (See Tr. at 626-7.)

Complainant argued that the schematics in CX-1417C represent the accused products because said schematics were provided by Zoran with the { } in response to a subpoena. (CBr at 38-9.) Complainant further argued that "the undisputed facts establish a prima facie case and a presumption that the Zoran documents are authentic and reliable evidence upon which the Chief Judge should properly rely." (CBr at 44.) Complainant also argued that respondents' arguments "are predicated on Zoran failing to comply with the subpoena in its production" and respondents have not set forth "any affirmative facts to rebut the presumption that is supported by the undisputed facts." (CBr at 48, 53.)

Respondents Funai have argued that the administrative law judge should give no weight to the third-party Zoran documents complainant Freescale relies upon in its infringement case. (RBr at 16.) Funai contended that the Zoran documents were not properly authenticated or shown to be reliable and representative of the circuits used in Funai products. (RBr at 17.) Specifically, Funai noted that complainant Freescale's expert Subramanian did not examine actual Zoran circuits or Funai products. They further contended that their expert "McAlexander testified, and Dr. Subramanian acknowledged, that there is nothing in or about the Zoran documents that indicates that they are final documents or correspond to specific manufactured products, let alone

---

[9] With respect to the administrative law judge's findings on infringement in Section IX infra, the administrative law judge in Section IX has found that based on the statement of complainant's counsel and a review of said Zoran documents as found in Section VIII, complainant has failed to prove infringement by a preponderance of the evidence because all of said Zoran datasheets CX-1411C, CX-1412C, CX-1413C, and CX-1414C are found unreliable as evidence of the composition of the accused products and because said Zoran schematics CX-1417C are also found unreliable as evidence of the composition of the accused products.

the accused integrated circuits in the Respondents' products." (RBr at 16-7.) Funai also noted that the administrative law judge granted a request by complainant Freescale to extend the discovery deadline with respect to obtaining additional discovery from Zoran, but Freescale did not depose Zoran, seek an affidavit from Zoran regarding Zoran documents, or move to have the Zoran subpoena enforced. (RBr at 17-8.) Funai further argued that Freescale cannot rely on the fact that the documents in issue were produced in response to a subpoena to establish that the documents are reliable because "the documents bear indicia of unreliability." (RBr at 29-31.)

The staff argued that the documents at issue are reliable and the testimony regarding the documents should be given full weight because the documents "were produced by Zoran in response to a subpoena issued by the Chief Judge; the subpoena asked for schematics for parts used in the accused Funai products; and the schematics were produced by Zoran with the

{

} (SBr at 17.) The staff also argued that respondents' assertions regarding the documents in issue should be rejected because their argument is legally unsupported and relies on speculation and attorney argument. (SBr at 17; SRBr at 3.)

Complainant bears the burden of proving infringement by a preponderance of the evidence, and with that burden complainant bears the burden of proving the composition of the accused products. Ultra-Tex Surfaces, Inc. v. Hill Brothers Chemical Co., 204 F.3d 1360, 1364 (Fed. Cir. 2000). Complainant must provide sufficient evidence to show infringement before the burden shifts to the accused infringer to offer contrary evidence. See L&W, Inc. v. Shertech, Inc., 471 F.3d 1311, 1318 (Fed. Cir. 2006). However, said evidence must show infringement for each accused device and the complainant cannot rely on an assumption that all of the accused products include similar structure to shift the burden to the accused infringer. See Id.

Further, Commission precedent indicates that admitted evidence may be given no weight in making a final initial determination on infringement where said admitted evidence is unreliable or insufficient to show the composition of the accused products. See Certain Sucralose, Sweeteners Containing Sucralose, And Related Intermediate Compounds Thereof, Inv. No. 337-TA-604, Commission Opinion at 90-93 (April 28, 2009) (affirming non-infringement determination of the administrative law judge based in part on unreliability of admitted evidence) (Sucralose); Certain Nor And Nand Flash Memory Devices And Products Containing Same, Inv. No. 337-TA-560, Initial Determination at 40-46 (June 1, 2007) (Non-review by Commission on July 13, 2007) (finding admitted evidence unreliable and giving said evidence and testimony related to said evidence no weight). In Sucralose, complainant relied on its employee's testimony regarding third party test results to prove infringement by a defaulting party. However, the administrative law judge found said testimony insufficient and unreliable to prove infringement because "no one who conducted the tests was called to testify regarding the methodology used or the reliability of the results," and the Commission affirmed. Sucralose, Comm. Op. at 90-3.

It is undisputed that all the Zoran documents in issue were produced by Zoran in response to a subpoena propounded by complainant and requesting documents related to Zoran part numbers disclosed by Funai as being incorporated into Funai accused products. (CPFF 481-484 (undisputed).) Regarding the Zoran datasheets, the titles of the datasheets include the text { }(CX-1411C; CX-1412C; CX-1413C; CX-1413C.) Each of those SupraHD identifiers relates to Zoran chips which Funai has admitted are in the accused products. (See CX-1411C at Zoran 000376; CPFF 483 (undisputed); CPFF 484 (undisputed).) Further, complainant's expert Subramanian testified

regarding the link between the datasheets and the Zoran chips in the accused products:

{

}

(Tr. at 193-194 (emphasis added).)

The administrative law judge finds that there is a link between the datasheet exhibits, viz. CX-1411C, CX-1412C, CX-1413C, and CX-1414C, and the Zoran chips present in the accused products because the datasheets consistently correlate "SupraHD" parts to Zoran part numbers present in the accused products. (See CX-1411C at Zoran 000376; CX-1412C at Zoran 000542; CX-1413C at Zoran 000677; CX-1414C at Zoran 000873; CPFF 483 (undisputed); CPFF 484 (undisputed).) For example, {

}

(CX-1414C at Zoran 000873.) Similarly, CX-1411C includes the list:

{

}

(CX-1411C at Zoran 000376.)

However, despite said link, each of said datasheets has the language on the first page,

{

} (CX-

1411C, CX-1412C, CX-1413C, CX-1414C.) Regarding said text on the datasheets,

complainant's expert Subramanian testified:

{

}

(Tr. at 542-543 (emphasis added).) Thus, Subramanian testified that {

} but concluded that they represented what is included in the accused products

because the datasheets were produced in response to a subpoena. Further, the title pages of these datasheets include the dates{

} (CX-1414C). Regarding the dates on said datasheets, Subramanian testified:

{

}

{

}

(Tr. at 538-545 (emphasis added).) Thus, the administrative law judge finds that Subramanian admitted that "more recent ones ... were not provided in response to the subpoena" and relied upon the fact that said datasheets were produced pursuant to a subpoena to indicate that said datasheets were final documents that accurately reflected the composition of the accused products. Based on the foregoing, the administrative law judge finds that the sponsoring witness for said datasheets, viz. Subramanian, could provide no details regarding how the datasheets were created or the origin of certain information contained therein and relied primarily on the fact that said datasheets were produced pursuant to a subpoena in concluding that the technical

information contained therein accurately represented the composition of the accused products. He further finds that Subramanian has based his conclusions regarding the reliability of the datasheets on the legal conclusion that because the datasheets were produced in response to a subpoena they are presumed reliable. However, Subramanian, who is not an attorney, testified only as an expert in the field of "electrical engineering and integrated circuits." (Tr. at 121.)

Further, complainant's expert Subramanian, as seen from his following testimony, testified that his infringement analysis as it relates to CX-1411C, CX-1412C, CX-1413C, and CX-1414C is the same for each of these documents, which indicates that the relevant parts of these documents did not significantly change from {

}

(Tr. at 211-215 (emphasis added).) In addition, the administrative law judge finds the datasheet pages relied upon by Subramanian in his infringement analysis contain {

}

However, Subramanian, as found supra, could not provide any details regarding the origin of the information contained in said datasheets and based his conclusion that the technical information contained therein was the final information representing the contents of the actual Zoran integrated circuits in the accused products solely on the fact that said datasheets were produced in response to a subpoena. Further, the administrative law judge finds that complainant produced no other evidence beyond the testimony of Subramanian to establish the finality and reliability of said datasheets, and he further finds that the record does not contain any corroborating evidence to establish their finality other than certain consistencies among said datasheets, which only indicates that certain information in said datasheets may be final. Significantly, he finds complainant, who has the burden to establish infringement, presented nothing from Zoran, from which said datasheets originated, explaining the defects, supra, in said datasheets CX-1411C, CX-1412C, CX-1413C, and CX-1414C.[10] Thus, he finds that said datasheets are unreliable as evidence of the contents of the accused products. Accordingly, said datasheets and testimony regarding the technical information contained in said datasheets will not be given any weight in making a final determination on infringement.

Regarding the Zoran schematics CX-1417C, like said datasheets, it is undisputed that said

---

[10] It is a fact that complainant did not depose Zoran. However, it is also a fact that the administrative law judge issued a subpoena ad testificandum and duces tecum to Zoran Corporation as early as July 9, 2010, nearly six months before the beginning of the evidentiary hearing. (EDIS Docket Document ID No. 444564.) Further, in Order No. 19, the administrative law judge extended the fact discovery deadline to October 8, 2010 to allow, inter alia, complainant to complete discovery with respect to Zoran "including concluding document production and providing a witness to testify." (Order at 1.) Said extension of discovery occurred approximately four months before the beginning of the evidentiary hearing.

schematics were produced pursuant to a subpoena. (CPFF 481-484 (undisputed).) It is also undisputed that the first page of the exhibit containing schematics (CX-1417C) includes the { } (RFF 53 (undisputed in relevant part).) Regarding the relevance {

}

(Tr. at 159 (emphasis added).) Thus, the administrative law judge finds that Subramanian relied on the fact that the schematics were produced pursuant to a subpoena to show that the handwritten notation was accurate and the schematics in the exhibit (CX-1417C) represented the circuitry present in the accused products. Subramanian further testified that without the handwritten notation he would not be able to relate the schematics to any particular Zoran part number:

> Q. And just to be clear, from Judge Luckern's point, without the hand scrawl, without the hand notations, you have no way to associate any wiring or functionality in a schematic to any particular part, correct?
>
> A. To any single part?
>
> Q. Any single part, correct?
>
> A. Yes, I agree. I would only be able to associate it collectively, to the list of parts on the subpoena, but not to any single part.

(Tr. at 424-425 (emphasis added).) Subramanian further testified regarding the handwritten notation:

Q. You just don't know who put that scrawl there?
A. I think I already said that. That's correct.

Q. Do you know why whoever did it, did it? Do you know?

A. I believe so. I believe they put it on there to indicate the family that it's from.

Q. That's your belief. I'm asking you a different question. Do you know why the person who put it there put it there?

A. Beyond my belief, I have no additional basis for saying that.

Q. So you just don't know why that person, you don't know who it is, you don't know why they put it there?

A. I do not know who it is. I have a belief as to why it is there, but beyond that, I have no other basis.

(Tr. at 414-415 (emphasis added).) Thus, the administrative law judge finds that Subramanian testified that he has no personal knowledge regarding who placed the handwritten notation on CX-1417C or why it was place there, and he further finds that Subramanian did not provide any corroborating information regarding the technical content of the schematics. Moreover, beyond the testimony of Subramanian, complainant did not provide any other evidence regarding who wrote the handwritten notation, why it was written, or when it was written.

Further regarding the schematics in CX-1417C labeled {

}

(Tr. at 532-534 (emphasis added).) Thus, the administrative law judge finds with respect to the relevance of the schematics CX-1417C that Subrmanian relied on the fact that said schematics were produced in response to a subpoena while acknowledging {

}

(Tr. at 547-550 (emphasis added).) Thus, the administrative law judge finds that Subramanian,

{

}

Further, Subramanian testified that information regarding {

} Thus, he testified:

> THE WITNESS: I understand, Your Honor. When you design a new circuit, the circuit complexity, in many cases, can get quite large, and as a result, humans make errors.
>
> So commonly, there are both computer based checks, and I'll explain what that means, as well as person based checks, and the person based checks will mean you will sit down with the rest of your design team, and you'll present what you've done, and they will look at it, and they'll give you suggestions, or they might say, well, watch out for this problem or not.
>
> The computer based checks are, they'll run circuit simulations, confirm that the circuits have the behavioral patterns that you expect them to have, and then there'll be some sort of version control database maintained that'll say that this particular version of the design, arbitrarily, version 1.6, has past the checks.
>
> Those version control databases do not, however, have to be in the same database as the schematics.

(Tr. at 546-547 (emphasis added).) However, the administrative law judge finds that neither complainant nor Subramanian have provided any evidence of another database or other corroborating evidence showing that said schematics have been {

}

(Tr. at 551-553 (emphasis added).) The administrative law judge finds that Subramanian again relied on the fact that said schematics were produced pursuant to a subpoena as the only evidence that they represent the circuitry in the accused products despite the {

}

Regarding the { } listed on the pages of CX-1417C, Subramanian testified:

{

}

(Tr. at 536-537 (emphasis added).) Thus regarding dates, Subramanian is "positive" because the schematics were produced in response to a subpoena.

Based on the foregoing, the administrative law judge finds that the contents of the schematics are unreliable insofar as they do not bear any indicia of finality; the record does not

contain any corroborating evidence to establish their finality; and the sponsoring witness could provide no details whatsoever concerning how the document was created or the origin of the technical information contained therein. Accordingly, the administrative law judge finds that said schematics are not reliable evidence of the composition of the accused products and said exhibit along with the testimony regarding said exhibit will not be given any weight in making a final determination on infringement.

Complainant and the staff each argued that the schematics in exhibit CX-1417C are reliable evidence of the circuitry present in the accused products because the schematics were produced in response to a subpoena. (See CBr at 49; SBr at 17.) To support said argument, complainant asserted that the schematics were provided by Zoran through Zoran's counsel and produced as received and the{ } shows the "schematics produced by Zoran correlate precisely to the schematics requested by Complainant in its subpoena." (CBr at 50.) Complainant concluded that "[t]hese facts support a prima facie case that the Zoran schematics are reliable evidence of the Zoran integrated circuits," and "[i]t is more likely that (sic) not that the schematics are exactly what they purport to be: Zoran schematics for the integrated circuit part numbers requested in the subpoena and that are listed on the Zoran schematics themselves." (CBr at 51.) Complainant further concluded that these facts created a "presumption that the Zoran documents are authentic and reliable evidence," and respondents have not identified any facts to rebut this presumption. (CBr at 44.)

Significantly however, neither complainant nor the staff cited to any law establishing that documents produced pursuant to a third-party subpoena are inherently reliable or establish a "prima facie" case that said documents are reliable creating a presumption that must be rebutted by respondents, and the administrative law judge has found no law supporting said arguments.

To the contrary, in U.S. v. Sutton the court stated:

> Next, documents produced by a third party, ... by subpoena or otherwise-regarding which the defendants have had no right to cross-examination, will probably not be received in evidence unless during the trial, an appropriate witness should provide the necessary predicate for the document to be admitted and thereby affording the defendants the right of cross-examination.

795 F.2d 1040, 1056 (Temp. Emer. Ct. App. 1986) (emphasis added). Moreover, complainant has produced no evidence regarding, with reference to the schematics CX-1417C,{ } beyond the fact that said schematics were produced in response to a subpoena, as found supra. Further, as found supra, CX-1417C includes { } suggesting it is not a final version of a schematic and complainant produced no corroborating evidence establishing the finality of said schematics. Significantly, like the datasheets in issue, the administrative law judge finds complainant, who has the burden to establish infringement, presented nothing from Zoran explaining the defects, supra, in said schematics CX-1417C.

IX. Infringement

At issue is whether complainant established, by a preponderance of the evidence, that the accused products infringe claims 9 and 10 of the asserted '455 patent.

Complainant has admitted, as found, supra, in Section VIII, that its infringement contentions rely on, inter alia, CX-1411, CX-1412, CX-1413, CX-1414, and CX-1417, viz. the Zoran datasheets and the Zoran schematics. As found supra, the administrative law judge has not accorded any weight to said Zoran datasheets and schematics or the related testimony. Thus, he finds that complainant has failed to show that the accused products infringe the asserted claims of the '455 patent. However, for the sake of the infringement analysis, the administrative law judge will, in this section, assume, arguendo, that each of the Zoran datasheets, the Zoran

schematics, and related testimony are accorded weight and will make findings as to whether there is infringement under said assumption.[11]

A. Accused Products

Complainant accused certain models of Funai televisions using integrated circuits manufactured by third party Zoran. (CBr at 34.) Specifically, the Zoran integrated circuits, or chips, are in the { } (CBr at 34.) The specific models of Funai televisions that complainant accuses of including chips from Zoran are on the following chart, where the Funai model numbers follow the colon on each bullet point:

{

}

[11] Respondents also have generally objected to complainant not having examined either the commercial end products (particular models of Funai televisions) accused of infringement, nor the specific Zoran IC chips alleged to be the basis for complainant's infringement allegations. (See, inter alia, RRCPFF 719; RRCPFF 720; RRCPFF 723.) The administrative law judge rejects this argument, and finds, despite the lack of reliable documentation in this investigation, that where reliable documentation does exist, said reliable documentation is sufficient to show how products work such that examination of physical products is not necessary to prove infringement. See Monsanto Co. v. David, 516 F.3d 1009, 1015-1016 (Fed. Cir. 2008) ("an expert need not have obtained the basis for his opinion from personal perception").

(CBr at 37.) Complainant argued that, for the purpose of determining infringement of asserted claims 9 and 10, the "analysis and result is the same for each of the Accused Funai Zoran ICs." (CBr at 63.) Because the accused products are goods that include a component that is alleged to infringe the asserted patent, complainant must show that said component infringes and that said component is installed in the accused products.

With respect to whether the alleged infringing components, i.e. the Zoran chips, are installed in the accused products, the respondents do not dispute that the accused products contain Zoran chips with the model numbers:{

} (See CPFF 114; ROCPFF 114A; CX-122C at 9-10.) Thus, the administrative law judge finds that said components, viz. the Zoran chips, are installed in said accused products, viz. the Funai model numbers listed supra.

B. The claim limitation "A data processor within an integrated circuit package comprising..."

Complainant argued that, based on the Zoran hardware datasheets CX-1411C, CX-1412C, CX-1413C, and CX-1414C, that the Zoran chips are integrated circuits. (CBr at 65-67.) Further, complainant argued, with reference to said datasheets, that the accused products contain a Zoran integrated circuit that is a data processor, as it has a CPU and other components that process data. (CBr at 67.)

Respondents presented no substantive counterargument, instead relying on their conclusion that CX-1411C - 1414C are "neither probative nor reliable." (CPFF 712; ROCPFF 712; RRCPFF 712.)

The staff argued that "each and every limitation of claim 9 of the '455 patent as correctly construed is literally present in the Zoran chips incorporated in the accused Funai products." (SBr at 18.)

Each of the Zoran chips at issue in this investigation are described in a datasheet as being { {

} CX-1412C at ZORAN 542; CX-1413C at ZORAN 677; CX-1414C at ZORAN 873.) Complainant's expert testified that "IC" means integrated circuit. (Tr. at 238; see also CPFF 673 (undisputed in relevant part).) Said datasheets show that the Zoran chips are integrated circuits. (CPFF 653, 654, 655 (all undisputed in relevant part).) Further, the datasheets show that the Zoran chips at issue have a data processor within an integrated circuit package. (CPFF 712 (undisputed in relevant part).) Respondents have not substantively rebutted complainant's arguments with respect to the preamble of claim 9 of the '455 patent. In fact, respondents' expert McAlexander testified that said chips do contain a data processor. (ROCPFF 716 (citing Tr. at 1029, 1030-32).) Thus, assuming, arguendo, that said Zoran datasheets CX-1411C, CX-1412C, CX-1413C, and CX-1414C are accorded weight, the administrative law judge finds that the Zoran chips at issue do practice the preamble of claim 9 of the '455 patent; that is, they are integrated circuits that contain a data processor.

C. The claim limitation "an execution unit internal to the data processor..."

Complainant argued that the accused products practice this claim limitation under either party's construction of "execution unit." (CBr at 68.) Specifically, complainant argued that the Zoran chips have an internal CPU; that a {

} (CBr at 68); that the Zoran chips all execute Application software; that since each of the chips runs firmware, they meet this claim limitation; and that

respondents' and staff's constructions are broader than complainant's construction. (CBr at 68-70.)

Respondents argued that the evidence relied on by complainant is insufficient to show that the Zoran chips practice this claim element (RRBr at 65-67; see also, e.g., ROCPFF 719; RRCPFF 719) and that complainant has not shown that any execution unit in the Zoran IC chips is driven by microcode and/or nanocode, as required by complainant's claim construction. (RRBr at 65-68.)

The staff argued that "each and every limitation of claim 9 of the '455 patent as correctly construed is literally present in the Zoran chips incorporated in the accused Funai products." (SBr at 18.)

The administrative law judge has found, supra, that an "execution unit" is "a portion of an integrated circuit that executes commands or instructions." He also has found, supra, that the Zoran chips are integrated circuits and have a data processor. The datasheets show that each of the Zoran chips{ } (CX-1411C at ZORAN 375, 377; CX-1412C at ZORAN 541, 542, 544, 548; CX-1413C at ZORAN 669, 670; CX-1414C at ZORAN 865, 874; see also CPFF 719 (undisputed in relevant part).) Respondents' expert McAlexander testified that "there is an execution unit inside of chips because, if they do any processing at all, they will have the most rudimentary form of an execution unit based on my definition." (Tr. at 1035.) Based on the foregoing, and assuming, arguendo, that the Zoran datasheets are accorded weight, the administrative law judge finds that complainant has shown that the Zoran chips at issue practice this limitation of claim 9 of the '455 patent at issue.

D. The claim limitation "a plurality of external pins connected to the integrated circuit package, the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus..."

Complainant argued that this limitation has two clauses and only the second, viz. "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus..." is disputed; that there is no dispute that each of the Zoran chips at issue have a plurality of external pins connected to the integrated circuit package; and that under complainant and the staff's construction of the second clause, the Zoran chips practice this element. (CBr at 71-75.) Specifically, complainant argued that both complainant's expert Subramanian and respondents' expert McAlexander agreed that the Zoran integrated circuits have "a plurality of external pins connected to the integrated circuit package," and that the external pins are formed by ball connectors on the Zoran chips, which are shown in images in each of the Zoran datasheets. (CBr at 71-72.) Complainant further argued that {

} and that McAlexander agreed that based on the datasheets the Zoran parts meet this claim element under complainant and staff's interpretation. (CBr at 75-77.)

Respondents argued that "the proper grammatical understanding of this unambiguous claim term... requires that the logic bits travel from the external pins, through the external bus, and then onto the data processor," and that it is undisputed that the Zoran schematics do not depict such a configuration. (RBr at 82.) Respondents did not present any non-infringement arguments based on complainant and the staff's interpretation of this claim term beyond relying on their conclusion that the datasheets CX-1411C - 1414C are unreliable. (RRBr at 71-72.)

The staff argued that "each and every limitation of claim 9 of the '455 patent as correctly

construed is literally present in the Zoran chips incorporated in the accused Funai products." (SBr at 18.)

The administrative law judge has found, supra, that the Zoran chips are integrated circuits and have a data processor. The Zoran datasheets show that each of the Zoran chips at issue include{

} practice the limitation "a plurality of external pins connected to the integrated circuit package." (CX-1411C at ZORAN 519; CX-1412C at ZORAN 642; CX-1413C at ZORAN 836; CX-1414C at ZORAN 1012; CPFF 740 (undisputed in relevant part); CPFF 741 (undisputed in relevant part); CPFF 742 (undisputed in relevant part); CPFF 743 (undisputed in relevant part); CPFF 744 (undisputed in relevant part).) Regarding the remainder of this claim limitation, the administrative law judge has found, supra, that the claimed phrase in issue should be construed as "a plurality of external pins used to bidirectionally communicate logic bits from the data processor, the logic bits traveling to and from the data processor via an external bus." The datasheets show that{

} (CX-1411C at ZORAN 459; CX-1412C at ZORAN 599; CX-1413C at ZORAN 769; CX-1414C at ZORAN 956; CPFF 757 (undisputed in relevant part); CPFF 758 (undisputed in relevant part); CPFF 760 (undisputed in relevant part).) The datasheets also show {

} (CX-1411C at ZORAN 467; CX-1413C at ZORAN 778; CX-1414C at ZORAN 953; CPFF 762 (undisputed in relevant part); CPFF 763 (undisputed in relevant part).) Based on the foregoing, and assuming, arguendo, that the Zoran datasheets are accorded weight, the administrative law judge finds that complainant has shown that the Zoran chips at issue practice

this limitation of claim 9 of the '455 patent.

E. The claim limitation "a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one bus termination circuit, the plurality of bus termination circuits providing data to or receiving data from the execution unit, each bus termination circuit in the plurality of bus termination circuits having an input for receiving a control signal; and..."

Complainant argued that each of the Zoran chips has the claimed plurality of bus termination circuits, under any party's construction. (CBr at 77.) Specifically, complainant argued that the Zoran hardware datasheets specify {

} (CBr at 78.) Complainant also relies on the schematics for further details. (CBr at 79-88.) Complainant further argued that Zoran chips have a CPU which is an execution unit and {

} (CBr at 94.)

Respondents argued that complainant has failed to show that this claimed phrase is practiced by the Zoran chips under complainant's construction, because the alleged control signal is{

} (RRBr at 78-80.)

The staff argued that "each and every limitation of claim 9 of the '455 patent as correctly construed is literally present in the Zoran chips incorporated in the accused Funai products." (SBr at 18.)

The administrative law judge has found, supra, that a "bus termination circuit" is circuitry for signal termination that is selectively enabled or disabled in response to a control signal whose

assertion is based, at least in part, on the direction of data signals on the bus. The administrative law judge has also found, supra, that the claimed phrase "providing data to or receiving data from" is accorded its plain meaning, i.e. "the plurality of bus termination circuits supplying data to or getting data from the execution unit."

The Zoran datasheets specify that the Zoran chips at issue have {

} (CPFF 781 (undisputed in relevant part); see also, CPFF 788, 789, 790, 792, 793, 794, 794796, 797 (all undisputed in relevant part).) Thus, CX-1417 depicts a plurality of termination circuits. (See CPFF 798 (undisputed in relevant part).) Also, respondents' expert McAlexander testified that the Zoran schematics showed chips with "a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one

bus termination circuit." (Tr. at 358.)

With respect to "the plurality of bus termination circuits providing data to or receiving data from the execution unit," each of the Zoran chips at issue has {

} (CPFF at 812 (undisputed in relevant part).) In said chips, the CPU is the execution unit, and { } (CPFF at 814, 815 (undisputed in relevant part).) The Zoran datasheets show that {

} (CX-1411 at ZORAN 375; CX-1412C at ZORAN 541; CX-1413C at ZORAN 669; CX-1414C at ZORAN 865; see also CPFF 816, 817 (undisputed in relevant part).)

Regarding the claim element phrase "each bus termination circuit in the plurality of bus termination circuits having an input for receiving a control signal," the bus termination circuits in the Zoran chips each have{ } (CPFF 830 (undisputed in relevant part); CX-1417C at ZORAN 1042.)

Based on the foregoing, and assuming, arguendo, that the Zoran datasheets and Zoran schematics are accorded weight, the administrative law judge finds that the Zoran chips practice the limitation at issue.

Respondents have argued that {

} Thus, the administrative law

judge rejects respondents' argument.

F. The claim limitation "a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus."

Complainant argued that each of the Zoran chips has a control signal that turns transistors on or off. (CBr at 94.) Complainant further argued that the Zoran datasheets and schematics show the claimed coupling and decoupling in response to the assertion or deassertion of a control signal. (CBr 98-99.)

Respondents argued that the circuit components which both parties agree are the resistors shown in the Zoran schematics are never "decoupled" from the bus. (RBr at 71-72.)

The staff argued that decoupling does not require a switch or transistor between the resistors and the bus, and thus the Zoran chips do practice this limitation. (SBr at 20.)

The administrative law judge has found, supra, that "couple" means "electrically connect to" and "decouple" means "electrically disconnected from." The Zoran schematics CX-1417C show that each {

}(CX-1417C at ZORAN 1042; see also CPFF 855 (undisputed in relevant part).) The administrative law judge has found, supra, that the circuit component must be electrically disconnected from the bus, such that it, inter alia, can no longer reduce signal reflection on the bus. He finds that turning off a transistor causing a resistor to no longer reduce signal reflection on a bus meets that definition. Based on the foregoing, and assuming, arguendo, that the Zoran datasheets and Zoran schematics are accorded weight the administrative law judge finds that the Zoran chips practice the limitation at issue.

G. Asserted Claim 10, "The data processor of claim 9 wherein the at least one circuit component is a circuit component selected from a group consisting of: a capacitor, a diode, a resistor, a transistor, a voltage source, a current source, and electrical short circuit, and an inductor.

The administrative law judge has found in Section F, supra, that the schematics show a

{ }

(CX-1417C at ZORAN 1042; see also CPFF 854 (undisputed in relevant part); RRCPFF 854A.) A { } is listed as one of the group of possible circuit components which satisfies claim 10. Based on the foregoing, and assuming, arguendo, that the Zoran datasheets and Zoran schematics are accorded weight the administrative law judge finds that the Zoran chips practice the limitation at issue.

H. Conclusion

Thus, based on the foregoing, the administrative law judge finds that, were the Zoran datasheets and schematics accorded weight, the accused products would infringe asserted claims

9 and 10 of the '455 patent.

X. Validity

A. Prior Art

Respondents argued that asserted claims 9 and 10 of the '455 patent are anticipated by U.S. Patent No. 3,832,575 (Dasgupta) (RX-532). (RBr at 85-95.) It is further argued that said claims would have been obvious considering Dasgupta in view of certain secondary references. (RBr at 99-121.)[12]

Complainant argued that respondents did not present any evidence that asserted claims 9 and 10 are invalid as anticipated by any prior art reference; that Dasgupta does not anticipate said claims; and that the asserted claims are not obvious. (CBr at 102-22.)

The staff argued that no evidence of invalidity under 35 U.S.C. § 102 was presented by respondents and that the evidence did not clearly and convincingly show that claims 9 or 10 are invalid under 35 U.S.C. § 103 because no combination of references rendered obvious the claimed data processing within an integrated circuit package having the claimed plurality of bus termination circuits in issue, citing Subramanian, Tr. at 1085-1097. (SBr at 24.)

1. Anticipation

Section 102 of Title 35 sets forth the novelty conditions that must be satisfied to obtain a valid U.S. patent. If every limitation of a patent claim is satisfied by a single item of prior art, it is "anticipated" and, hence, invalid under § 102 for lack of novelty. Karsten Mfg. Corp. v. Cleveland Golf Co., 242 F.3d 1376, 1383 (Fed. Cir. 2001). Thus to invalidate a patent by anticipation, a prior art reference normally needs to disclose each and every

[12] Although initially in response to the complaint it was alleged that the '455 patent was unenforceable, respondents abandoned that defense in their pre-hearing statement. (CPFF 1101, CPFF 1102 (both undisputed).)

limitation of the claim. Standard Havens Prods., Inc. v. Gencor Indus., Inc., 953 F.2d 1360, 1369 (Fed. Cir. 1991). However, a prior art reference may anticipate when a claim limitation or limitations not expressly found in that reference are nonetheless inherent in it. Id. Accordingly, under 35 U.S.C. § 102 a claim is anticipated "if each and every limitation is found either expressly or inherently in a single prior art reference." Celeritas Techs. Ltd. v. Rockwell Int'l Corp., 150 F.3d 1354, 1361 (Fed. Cir. 1998). Anticipation is a question of fact, including whether or not an element is inherent in the prior art. In re Schreiber, 128 F.3d 1473, 1477 (Fed. Cir. 1997). Under the principles of inherency:

> [t]o serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill

Continental Can Co. USA, Inc. v Monsanto Co., 948 F.2d 1264, 1268 (Fed. Cir. 1990) (emphasis added). At the hearing, there was no evidence in the record that the asserted claims are invalid as anticipated by any prior art reference, nor did respondents' technical expert McAlexander, offer any opinion relating to respondents' anticipation defense.[13] Moreover to the extent that respondents argued that the asserted claims are anticipated by Dasgupta, it is undisputed that Dasgupta does not explicitly or inherently disclose every element of asserted claims 9 and 10. Thus McAlexander testified:

> Q. And you admitted in your deposition on Sunday that Dasgupta does not teach the providing data to or receiving data from the execution unit limitation of Claim 9 explicitly, correct?

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[13] Respondents in their post hearing submissions rely on testimony of McAlexander at the evidentiary hearing that was stricken at said hearing. Respondents in their RBr at 50 requested that the administrative law judge "reverse his ruling striking Mr. McAlexander's testimony." Said request has been denied. See Section I (Procedural History), supra.

A. By explicit you mean the entirety of that providing to and the - - both?

Q. Yes, sir.

A. Yes, I said that it does not do both.

Q. And so since that is not taught by Dasgupta –

A. Right.

Q. - - you have to find teaching of that element in another reference and testify as to the reason why a person of ordinary skill in the art in 1993 would have combined those two references to disclose that element; is that fair?

A. That's fair.

(Tr. at 1062-63.)

With respect to the Dasgupta patent, it discloses a "Data Bus Transmission Line Termination Circuit" that is formed on the "same integrated circuit chip as the receiver circuit." (CPFF 1007 (undisputed); RX-532 at Abstract.) In each of the disclosed embodiments, Dasgupta shows a "receiver circuit," without any description of its function or application. (RX-532 at Figs. 4-8; 4:29-9-46.) None of the embodiments in Dasgupta disclose either transmit circuitry or a transmit path for data. (CPFF 1009 (undisputed).) Accordingly, the administrative law judge finds that the data bus connected to the integrated circuits described therein is uni-directional. (RX-532 at Figs. 1, 3-8; 3:57-9:46.) Because Dasgupta describes only the receive path, it does not disclose "the control signal.. .to couple at least one circuit component to the bus".

Dasgupta further discloses termination circuitry generically for use within an integrated circuit that contains a "receiver circuit." (CPFF 1007 (undisputed); RX-532 at Abstract, Figs. 3-8.) According to its Abstract:

> The termination circuit is preferably formed on the same integrated circuit chip as the receiver circuit so as to be located adjacent the

> effective end of the total transmission line including the portion extending from the data bus proper through the connections and conductors of the board, card, module and chip to the receiver circuit on the chip.

(RX-532 at Abstract.) Each of the drawings in Dasgupta illustrating the inventive embodiments (Figs. 3-8) contains a block labeled either "receiver circuit" or "RC1 " through "RC6." (CPFF 1011 (undisputed); RX-532 at Figs. 3-8.) At the hearing, neither respondents nor their expert provided any evidence that Dasgupta discloses the claimed term "plurality of bus termination circuits" as that term has been construed by the administrative law judge, supra. Furthermore, McAlexander never identified anything in Dasgupta corresponding to the "execution unit internal to the data processor" limitation of claim 9. To the contrary, the administrative law judge finds that the generic "receiver circuit" shown in Dasgupta meets neither the "data processor within an integrated circuit package" nor the "execution unit internal to the data processor" limitations of claim 9. Moreover because the disclosure of Dasgupta is directed only to termination of the receiver circuitry within an integrated circuit, the data bus shown is uni-directional. (RX- 532 at Figs. 1, 3-8; 3:57-9:46.) At the hearing, neither the respondents nor their technical expert provided any evidence or expert opinion that Dasgupta inherently or explicitly disclosed an external bus "used to bidirectionally communicate logic bits to and from the data processor." To the contrary respondents' expert merely stated: "[t]his chip will be packaged, it's the way it was done circa 1974, so this packaged present invention chip would have external pins, and the external pins were used to bi-directionally communicate logic bits to and from the data processor via an external bus." (McAlexander, Tr. at 905:7-12).[14]

Regarding the language of claim 9 "the plurality of bus termination circuits providing data

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[14] This testimony was not stricken. See Tr. at 905-07.

to or receiving data from the execution unit," respondents' expert admitted that Dasgupta does not teach "the plurality of bus termination circuits providing data to or receiving data from the execution unit" limitation of claims 9 and 10. (McAlexander, Tr. at 1062-63.) Referring to the claimed language "the plurality of bus termination circuits" the "bus termination circuit" in claim 9 "is selectively enabled or disabled in response to a[n] control signal whose assertion is based, at least in part, on the direction of data signals on the bus," as found by the administrative law judge supra. The administrative law judge finds that Dasgupta does not disclose "bus termination circuits" that meet this limitation, because Dasgupta illustrates only the receiver and receive path for data in an integrated circuit. (RX- 532 at Figs. 1, 3-8; 3:57- 9:46.) Therefore, he finds that Dasgupta does not teach bus termination that is selectively enabled or disabled based on whether the integrated circuit is receiving or transmitting data.

Based on the foregoing, the administrative law judge finds that respondents have not meet their burden of proving, by clear and convincing evidence, that asserted claim 9 and asserted claim 10, which is dependent on said claim 9, are anticipated by Dasqupta.

2. Obviousness

At the hearing, respondents contended that claims 9 and 10 of the '455 patent were rendered obvious by four combinations of two references: the Dasgupta patent (RX-532) in view of a Gist patent (RX-243), Dasgupta in view of a Gabara patent (RX-13), Dasgupta in view of a Lauffer patent (RX-238) and Dasgupta in view of a Work patent (RX-21). (CPFF 1019.) The administrative law judge finds that respondents have failed to meet their burden of proving, by clear and convincing evidence, that any of those combinations renders claims 9 and 10 obvious.

Respondents have the burden to overcome the presumption that the asserted claims of the '455 patent are valid. Tech. Licensing Corp v Videotek, Inc., 545 F.3d 1316 (2008). The burden

of persuasion never shifts to complainant. Id. Rather, the risk of "decisional uncertainty" remains on the party or parties asserting invalidity. Id. Thus, it is respondents' burden to prove by clear and convincing evidence that any of the alleged prior art references, alone or in combination, render obvious asserted claims 9 and 10 of the '455 patent. See PharmaStem Therapeutics, Inc. v. ViaCell, Inc., 491 F.3d 1342, 1360 (Fed. Cir. 2007) (stating, "the burden falls on the patent challenger to show by clear and convincing evidence that a person of ordinary skill in the art would have had reason to attempt to make the composition or device, or carry out the claimed process, and would have had a reasonable expectation of success in doing so."). Failure to do so means that respondents lose on this point. Tech. Licensing, 545 F.3d at 1327.

Included within the presumption of validity is a presumption of non-obviousness. Structural Rubber Prods. Co. v. Park Rubber Co., 749 F.2d 707, 714 (Fed. Cir. 1984). Regarding non-obviousness, the patent statute dictates that a person is not entitled to a patent if the differences between the claimed invention and the prior art "are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. §103; see also Net MoneyIN, Inc. v. VeriSign, Inc., 545 F.3d 1359, 1371 (Fed. Cir. 2008) (stating, "differences between the prior art reference and a claimed invention, however slight, invoke the question of obviousness, not anticipation.").

The ultimate determination of whether an invention would have been obvious is a legal conclusion based on underlying findings of fact. In re Dembiczak, 175 F.3d 994, 998 (Fed. Cir. 1999). The underlying factual inquiries relating to non-obviousness include: 1) the scope and content of the prior art; 2) the level of ordinary skill in the art; 3) the differences between the claimed invention and the prior art; and, 4) secondary considerations of non-obviousness, such as long-felt need, commercial success, and the failure of others. See Graham v. John Deere Co., 383

U.S. 1, 17 (1966).

Obviousness may be based on any one of the alleged prior art references or a combination of the same, and what a person of ordinary skill in the art would understand based on his knowledge and said references. If all of the elements of an invention are found, then:

> [A] proper analysis under § 103 requires, inter alia, consideration of two factors: (1) whether the prior art would have suggested to those of ordinary skill in the art that they should make the claimed composition or device, or carry out the claimed process; and (2) whether the prior art would also have revealed that in so making or carrying out, those of ordinary skill would have a reasonable expectation of success. Both the suggestion and the reasonable expectation of success must be founded in the prior art, not in the applicant's disclosure.

Velander v. Garner, 348 F.3d 1359, 1363 (Fed. Cir. 2003) (emphasis added) (internal citations omitted). Further, the critical inquiry in determining the differences between the claimed invention and the prior art is whether there is a reason to combine the prior art references. See C.R. Bard v. M3 Sys., 157 F.3d 1340, 1352 (Fed. Cir. 1998). For example:

> [A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.

KSR Int'l Co. v. Teleflex, Inc., 550 U.S. 398, 418-19 (2007) (emphasis added) (KSR). However, the Supreme Court has rejected a "rigid approach," regarding a patent challenger's obligation to demonstrate a "teaching, suggestion, or motivation to combine" in the prior art. Id. at 419-22. The Court stated that:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. Sakraida and Anderson's-Black Rock are illustrative-a court must ask whether the improvement is more than the predictable use of prior art elements according to their established function.
>
> Following these principles may be more difficult in other cases than it is here because the claimed subject matter may involve more than the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement. Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. To facilitate review, this analysis should be made explicitly. See In re Kahn, 441 F.3d 977, 988 (CA Fed. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusions of obviousness"). As our precedents make clear, however, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

Id. at 417-18 (emphasis added). Further, a suggestion to combine may come from the prior art, as filtered through the knowledge of one skilled in the art. See Certain Lens-Fitted Film Pkgs., Inv. No. 337-TA-406, Order No. 141 at 6 (May 24, 2005). "[I]n many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." KSR, 550 U.S. at 420-21.

At the outset, the administrative law judge finds that none of the combinations advanced

by respondents contain all the elements of claims 9 and 10. Thus in their response filed January 21, 2011 to Question 35 of Order No. 36, respondents identified three limitations in claim 9 that were allegedly present in the Gist, Gabara, Lauffer, and Work references, such that when combined with Dasgupta, each of those combinations would render claims 9 and 10 obvious. See response to Q35. Said three limitations in respondents' obviousness combinations with Dasgupta were (1) the termination circuit within a data processor; (2) a bi-directional bus; and (3) decoupling the circuit component from the bus. (Id.) However the administrative law judge finds that Dasgupta is missing more than these three limitations. See supra. Hence even if said four secondary references combined with Dasgupta disclosed those three limitations, none of the combinations disclose all limitations of claims 9 and 10. See infra. In addition, as seen infra, the administrative law judge finds that respondents failed to prove that the asserted claims are obvious because they have not established why a person of ordinary skill in the art at the time the '455 patent application was filed would have combined any of the references in the manner asserted by respondents.[15]

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[15] Respondents' expert McAlexander did provide the following testimony as to the alleged combinations:

> Q. Please explain your opinion with regard to whether one of ordinary skill in the art at the time of the Gay '455 patent invention would have found it obvious to combine any one of Work RX-021, Lauffer RX-238, Gabara, RX-013, or Gist, RX-243, to the teachings of Dasgupta, and please explain your answer.
>
> A. It is my opinion that one of skill in the art at the time of the invention of the Gay patent would have found that any one of the combinations of Dasgupta, in view of Gabara, Gist, Work, or Lauffer, would have found the -- with respect to the termination circuit, would have found that element obvious.

(Tr. at 971-72.) Said testimony is found to be merely conclusory.

a. Dasgupta With Gist

Regarding the combination of Dasgupta in view of the Gist patent (RX-243) the administrative law judge finds that said combination does not contain at least the following limitations: (1) "a data processor within an integrated circuit package"; (2) "an execution unit internal to the data processor"; (3) "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus"; (4) "a plurality of bus termination circuits"; and (5) "the plurality of bus termination circuits providing data to or receiving data from the execution unit." Referring to said limitation (1), Fig. 1 from Gist is a system-level diagram of computer system 10, comprised of CPUs 12 and 14, memory modules 16, 18, 20 and 22, and I/O modules 24, 26 and 28, each connected to system bus 30. (CPFF 1020 (undisputed); RX-243 at 4:57-66; Fig. 1.) The components 12-28 of Fig. 1 are called both "devices" and "modules" throughout the specification, and never called integrated circuits. (CPFF 1021 (undisputed); RX-243 at 4:57-28:50.) Each CPU, memory, and I/O module in Gist has a bus interface circuit, for example, interface 14a in CPU module 14. (CPFF 1023 (undisputed).) The bus interface circuit terminates the system bus, among other things. (CPFF 1024 (undisputed).) Within each device, e.g., CPU 14, there is a line separating the bus interface circuit (here 14a) from the rest of the device, indicating that the bus interface circuit is a distinct portion of the device. (RX-243-Fig. 1)

When asked to explain the relevance of Gist "to the issue of termination circuitry within a data processor," respondents' expert McAlexander answered:

> Figure 1 of Gist shows multiple different units, such as CPUs, which are labeled at the bottom right corners 12 and 14, communicating bi-directionally to a bi-directional bus 30, and then if we look further in Figure 3, Figure 3 represents a circuit that is included in each one of 12 and 14 CPU, and you will see in Figure 3 that the - at the top corner is labeled I/O, and that is the

> connection point to the I/O or the input/output to the data bus 30.
>
> And then you will notice that, inside of the box labeled 40, which is a - labeled in a previous figure. This shows both a driver and a receiver. A driver drives data to the bus, a receiver receives data from the bus, and to the left of these two blocks, driver and receiver, is a smaller block called 42, which is termination, so this is a termination circuit that is electrically connected to the bi-directional bus.

(Tr. at 953-54.) As seen from the foregoing, respondents' expert failed to specifically identify a disclosure of the "data processor within an integrated circuit package" in Gist. Moreover complainant's expert Subramanian explained that within those CPU modules in Gist the bus termination circuitry is contained in an application specific integrated circuit (ASIC) that is separate from the CPU integrated circuit. (Tr. at 1087-89; RX-243 at 5.) Subramanian further explained that Gist discloses that the ASIC is located in the bus interface circuitry portion 12a of CPU module 12, as an example, separate from the CPU integrated circuit that would contain a data processor. (Tr. at 1089.) Gist further teaches that the bus interface circuit for each module or device includes the ASIC containing the bus termination circuitry. (CPFF 1030 (undisputed).) Gist also teaches that the ASIC includes bus interface cells 40, each of which contains driver 70, receiver 90, and termination circuit 42. (RX-243 at 5:15-44.) Significantly Gist does not disclose that the ASIC contains either a data processor or an execution unit internal to the data processor. (RX-243 at 5:15-44.) Neither respondents nor their expert referred to the ASIC teaching of the Gist patent. (CPFF 1033 (undisputed).) Hence because Gist teaches there is a separate integrated circuit for the bus interface circuits, apart from whatever integrated circuit may also be part of the device or module, the administrative law judge finds that Gist does not disclose the "data processor within an integrated circuit package" which also contains the "plurality of bus termination circuits" as recited in claim 9.

Regarding the claimed language "an execution unit internal to the data processor," because the termination circuitry disclosed in Gist is contained within an application specific integrated circuit (ASIC), not as part of a data processor within an integrated circuit package as required by claim 9 (see RX-243 at 5:15-44), it necessarily follows that Gist does not teach "an execution unit internal to the data processor." Moreover at the hearing, neither respondents nor their expert provided any evidence regarding this limitation in Gist.

Regarding the claimed language "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus," because the termination circuitry disclosed in Gist is contained within an application specific integrated circuit (ASIC), not as part of a data processor within an integrated circuit package as required by claim 9 (RX-243 at 5:15-44), the administrative law judge finds that Gist does not teach "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus" under the administrative law judge's construction of said language. At the hearing, respondents' expert did identify system bus 30 in Gist as the "bi-directional bus" in claim 9. (CPFF 1035 (undisputed).) However system bus 30 in Gist is connected to the ASIC within the bus interface circuit of each module (RX-243 at 4:57-5:44) not to the integrated circuit containing the data processor, as required in asserted claim 9. (CPFF 1036 (undisputed).)

Regarding the claimed language "a plurality of bus termination circuits," the administrative law judge has found that "bus termination circuit" in claim 9 "is circuitry for signal termination that is selectively enabled or disabled in response to a control signal whose assertion is based, at least in part, on the direction of data signals on the bus." At the hearing, respondents' expert did not apply said construction to Gist. (CPFF 1038 (undisputed).) Moreover there is no evidence

that Gist meets said claimed language as construed by the administrative law judge.

Referring to the claimed language "the plurality of bus termination circuits providing data to or receiving data from the execution unit" respondents did not address said limitation in the combination of Dasgupta with Gist in their response filed January 21, 2011 to Question 35 posed in Order No. 36. In any event, neither respondents nor their expert have proven that Gist meets said limitation under any party's construction. As found supra, Gist discloses that the termination circuitry is contained within an application specific integrated circuit (ASIC), not a data processor integrated circuit. (RX-243 at 5:15-44.) Accordingly, the administrative law judge finds that there is also no "execution unit" in the same integrated circuit as the termination circuitry, as required by claim 9, and therefore the termination circuitry is not capable of "providing data to or receiving from" an execution unit that is located in another integrated circuit.

In addition, the administrative law judge finds that, during the hearing, neither respondents nor their expert McAlexander provided evidence in the record as to why a person of ordinary skill in the art at the time the '455 patent was filed would have combined the Dasgupta and Gist references to render claims 9 and 10 obvious. Respondents have therefore not met their burden, by clear and convincing evidence, to demonstrate that a person of ordinary skill in the art would have combined Dasgupta and Gist in the manner claimed.

b. Dasgupta With Gabara

Referring to the combination of Dasgupta in view of the Gabara patent (RX-13) the administrative law judge finds that said combination does not contain at least the following limitations: (1) "a data processor within an integrated circuit package"; (2) "an execution unit internal to the data processor"; (3) "the plurality of external pins used to bidirectionally

communicate logic bits to and from the data processor via an external bus"; (4) "a plurality of bus termination circuits"; and (5) "the plurality of bus termination circuits providing data to or receiving data from the execution unit." Thus at the hearing, neither respondents nor their expert provided any evidence regarding said limitation (1). Respondents in ROCPFF 1043 refer to the following testimony of McAlexander:

> Q. Finally, with regard to Gabara, RX-013, you mentioned that as a secondary reference with regard to termination circuitry within a data processor as well, I believe?
>
> A. That is correct.
>
> Q. And could we get- it's on the screen.
> Could you please explain the relevant teachings of Gabara, insofar as that issue is concerned?
>
> A. Yeah, Gabara shows, in Figure 2 on RX-13-2, several blocks, I'll focus on block 20, which is a digital impedance block, and the digital impedance is controlled by Sn, and that is an input signal that controls the application or disassociation of decoupling of the digital impedance from the bus.
>
> Q. And that is all within a termination circuit within a data processor?
>
> A. Yes.
>
> Q. And could you explain how one of ordinary skill in the art would apply the teachings of Gabara in terms of the termination circuitry within the data processor to Dasgupta, please?
>
> A. Yes. The Dasgupta reference shows selective assertion or deassertion of a control signal in order to permit signal termination or to decouple the termination component :from the bus. And as shown also, here in Gabara is a digital impedance circuit that is selectively activated or deactivated, coupled or decoupled to the bus based upon the input voltage level of the control signal Sn.

(Tr. at 968-969.) Said testimony does not show that Gabara teaches said limitation (1). Moreover complainant's expert Subramanian provided his opinion that Gabara does not teach the "data processor within an integrated circuit package" limitation:

Q. Do you have an opinion as to whether Gabara teaches a bi-directional data bus?

A. I do. It is my opinion that Gabara does not teach a bi-directional data bus. It does not teach a bi-directional data bus because the disclosures within Gabara have separate transmit and receive connections, most of Gabara deals purely with transmit, and it's only dealing with output impedance, not with matching. It's dealing with the drivability and the output.

There's separate disclosure related to receive which is identified as being different circuitry, so it's completely separated. There's no bi-directional bus disclosure.

(Tr. at 1095.)

Referring to the claimed language "an execution unit internal to the data processor" (limitation (2)), respondents' expert McAlexander testified:

Q. Finally with regard to Gabara, RX-013, you mentioned that as a secondary reference with regard to termination circuitry within a data processor as well, I believe?

A. That is correct.

Q. And could we get -- it's on the screen.

Could you please explain the relevant teachings of Gabara, insofar as that issue is concerned?

A. Yeah, Gabara shows, in Figure 2 on RX-13-2, several blocks, I'll focus on block 20, which is a digital impedance block, and the digital impedance block is controlled by Sn, and that is an input signal that controls either the application or disassociation or decoupling of the digital impedance from the bus.

Q. And that is all within a termination circuit within a data processor?

A. Yes.

Q. And could you please explain how you believe one of ordinary skill in the art would apply the teachings of Gabara in terms of the termination circuitry within the data processor to Dasgupta, please?

A. Yes. The Dasgupta reference shows selective termination, either

assertion or deassertion of a control signal in order to permit signal termination or to decouple the termination component from the bus.

And as shown also, here in Gabara is a digital impedance circuit that is selectively activated or deactivated, coupled or decoupled to the bus based upon the input voltage level of the control signal Sn.

Q. And is it your belief that a person of ordinary skill in the art at the time of the Gay invention, the '455 patent, would have found that combination to have been obvious?

A. In my opinion, yes.

(Tr. at 968-9.) Said testimony does not disclose "an execution unit internal to the data processor."

As for the claimed language "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus" (limitation (3)), the administrative law judge construed such language as "a plurality of external pins used to bidirectionally communicate logic bits from the data processor, the logic bits traveling to and from the data processor via an external bus." (See Section VII.F, supra.) At the hearing, respondents' expert McAlexander testified:

Q. Mr. McAlexander, were there any other references that you relied upon in order to combine with Dasgupta with regard to the bi-directionality issue?

A. Yes, Gabara.

* * *

Q. Could we have Gabara [RX-13] up?

Mr. McAlexander, could you please explain the relevant teachings of Gabara, as you understand it, to the issue of bi-directionality and how it would be combined with Dasgupta?

A. The circuit that's shown in 100 is selectively applied or decoupling impedance, for the purpose of impedance matching to the bus, and

the pin that's shown in 10 is connected to an external bus which is 200. The patent specification specifies that this particular pin can be either to a uni-directional or a bi-directional. It could be for input and output.

Q. And can you please explain how you would combine that with the Dasgupta reference?

A. This patent would then show that this termination component is linked -- electrically connected to a bi-directional bus and, therefore, would permit both the input of data from the bus and the output of data to the bus.

(Tr. at 947-48.) The administrative law judge finds that said testimony does not show that Gabara refers to an external bus connected to an integrated circuit, let alone a bi-directional bus connected to an integrated circuit. Moreover, as complainant's expert, Subramanian, testified, Gabara does not disclose a bi-directional bus, and further explained that Gabara teaches modifying the impedance of an output terminal. See supra.

Referring to the claimed language "bus termination circuit" in claim 9, the administrative law judge has construed said language as "circuitry for signal termination that is selectively enabled or disabled in response to control signal whose assertion is based, at least in part, on the direction of data signals on the bus." At the hearing, respondents' expert did not apply this construction to Gabara.

In addition to the foregoing, at the hearing neither respondents nor their expert McAlexander provided evidence in the record as to why a person of ordinary skill in the art, at the time the '455 patent was filed, would have combined the Dasgupta and Gabara references to render claims 9 and 10 obvious. Respondents refer to testimony of their expert (Tr. at 968-9, supra), which the administrative law judge has found inadequate. See supra.

c. Dasgupta With Lauffer

At the hearing, and with regard to the combination of Dasgupta with Lauffer, neither

respondents nor their expert McAlexander provided any evidence regarding the claimed language "a data processor within an integrated circuit package." Respondents expert did testify:

Q. And get Lauffer [RX-238] up, please.

Would you please explain the relevant teachings of Lauffer, insofar as they relate to the termination circuitry within a data processor limitation?

A. The termination -- if I may use this, the termination circuit is shown inside of the device labeled 10 on the left side of the screen, and the component -- termination component is the resistor that's labeled R sub t -- looks like t1, that is in the bottom right corner of the dashed box labeled 10.

And the transistor, which selectively couples Rt1, the component to the data bus, or decouples, such that Rt1 is not electrically connected, that functionality is performed by transistor 38. So the combination of 38 and Rt1provide the termination circuit that is connected, selectively connected or disconnected from the termination line, which is labeled as 14.

Q. And is that within the data processor?

A Yes. In fact, if we look at the CMOS, it has CMOS transmit and receive circuit, which is labeled in box -- looks like 16, I believe.

Q. I believe it's 10.

A. No, the CMOS transmit and receive circuit is in block 16, and the control of that shown like, for instance, T/r line 50, there would be a rudimentary execution unit that would provide the control logic for that, so it is within a data processor.

Q. And how, in your opinion, would one of ordinary skill in the art have used the teachings from Lauffer RX-238 in connection with Dasgupta, insofar as the termination circuitry within the data processor element is concerned?

A. Well, as I mentioned before, Dasgupta teaches the -- teaches termination circuit, and Lauffer also has a termination circuit arranged in the same way as Dasgupta, where the switch -- the transistor provides the coupling and decoupling of the resistor component from the bus in a like manner, as what I described earlier in Dasgupta, and Lauffer expressly teaches the

bi-directional aspects. So this is an input/output termination circuit.

(Tr. at 966-68.) However as complainant's expert Subramanian testified:

Q. Thank you. Could I have RX-238 in evidence, the Lauffer patent at Figure 1.

Do you have an opinion as to whether Lauffer teaches a data processor within an integrated circuit package?

A. I do. It is my opinion that Lauffer, the Lauffer patent 827 does not teach a data processor with[in] an integrated circuit package.

In particular, if we look at the Lauffer patent, specifically all it deals with is a CMOS transceiver device that is not a data processor. There is no execution unit within it. It does not meet the requirements of Claim 9.

(Tr. at 1095-96 (emphasis added.).)

Referring to the claimed language "an execution unit internal to the data processor" respondents' expert McAlexander testified that "there would be a rudimentary execution unit that would provide the control logic for that, so it is within a data processor." (Tr. at 966-68, supra.) However as complainant's expert Subramanian testified, Lauffer does not teach the "execution unit internal to the data processor" limitation. See supra.

Referring to the claimed language "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus," at the hearing, respondents' expert identified a bi-directional bus in Fig. 1 of Lauffer. (CPFF 1061 (undisputed).) Lauffer does not, however, disclose a data processor within an integrated circuit package, and accordingly does not show any path to "bidirectionally communicate logic bits to and from the data processor" as required by claim 9.

Referring to the claimed phrase "a plurality of bus termination circuits" under the administrative law judge construction, which is substantially the same as the proposed

construction of the complainant and the staff, at the hearing, respondents' expert did not apply this construction to Lauffer. (CPFF 1062 (undisputed).) Accordingly, there is no evidence that Lauffer meets this element under said construction.

In addition, at the hearing, neither respondents nor their expert McAlexander established why a person of ordinary skill in the art at the time the '455 patent was filed would have combined the Dasgupta and Lauffer references to render claims 9 and 10 obvious. While respondents' expert did testify:

> Q. And how, if at all, would one of ordinary skill in the art use that teaching or apply that teaching to Dasgupta?
>
> A. Dasgupta has a data bus. This, in combination, with Lauffer indicates a bi-directional bus.

(Tr. at 949), the administrative law judge does not find said testimony indicates why a person of ordinary skill in the art would combine Dasgupta with Lauffer.

d. Dasgupta With Work

The administrative law judge finds that the combination of Dasgupta in view of the Work patent (RX-21) does not render obvious claims 9 and 10 of the '455 patent because it is does not contain at least the following limitations: (1) "a data processor within an integrated circuit package"; (2) "an execution unit internal to the data processor"; (3) "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus"; (4) "a plurality of bus termination circuits"; (5) "the plurality of bus termination circuits providing data to or receiving data from the execution unit"; and (6) "the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus."

At the hearing, neither respondents nor their expert McAlexander provided adequate

evidence regarding said limitations in the combination of Dasgupta with Work. Respondents' expert testified:

Q. Can we please put up Work RX-021? Mr. McAlexander, could you please explain the relevant teachings of Work, insofar as they relate to the bi-directional bus issue?

A. With Work -- I'll use the pointer. Work, on the face page of Figure 1, is a data processing chip that communicates with various components, but on the right side, there is a section, a circuit group that's called programmable line driver receivers. Driver receivers says that it both drives and receives, and the double-headed arrow line that's just immediately to the right of that, communicating with the external peripheral equipment, is identified by Work as a bi-directional bus.

* * *

Q. Okay. And finally, with regard to the termination circuitry within a data processor -- I'd like to put up Work, RX-021.

Mr. McAlexander, you made reference to Work as a possible secondary reference. Can you please explain its relevance to the issue of termination circuitry within a data processor?

A. The termination circuitry within theWork reference is shown as R sub 1 and R sub 2. These are termination circuits that are applied to the bus, which is labeled 216, they're connected to the internal bus 216, and then to a pad which goes external to the chip.

Q. And so is it fair to say that the termination circuitry within -- the termination circuitry of Work is within the data processor?

A. Yes.

Q. And what would be the -- I'm sorry -- and how would you purport to combine any teachings of Work, insofar as the termination circuitry within the data processor is concerned to Dasgupta?

A. What this reference shows -- teaches is the use of the termination circuit in association with a bi-directional bus 216.

That's borne out by the input and output buffers labeled I sub n and O-U-T that are attached to the left of that highlighted, green highlighted bus.

And the pullup resistor program in circuit 88, pulldown resistor

program in circuit 90 that's shown in the bottom two boxes of Figure 5, show selective resistance that can be programmed and allows the user of this type of device to selectively program the resistances to be high impedance or low impedance.

* * *

Q. Please explain your opinion with regard to whether one of ordinary skill in the art at the time of the Gay '455 patent invention would have found it obvious to combine any one of Work RX-021, Lauffer RX-238, Gabara, RX-013, or Gist, RX-243, to the teachings of Dasgupta, and please explain your answer.

A. It is my opinion that one of skill in the art at the time of the invention of the Gay patent would have found that any one of the combinations of Dasgupta, in view of Gabara, Gist, Work, or Lauffer, would have found the -- with respect to the termination circuit, would have found that element obvious.

(Tr. at 949-50, 969-71.) Work however does not teach the "data processor within an integrated circuit package" limitation. As complainant's expert testified:

Q. And lastly, RX-21 in evidence, the Work patent. Could I have Figure 1, please.

Do you have an opinion as to whether the Work patent discloses a data processor with an integrated circuit package?

A. I do. It is my opinion that the Work patent does not disclose a data processor within an integrated circuit package.

Specifically, the disclosure of the Work patent, and indeed it shows up in the title itself and specifically in Figure 1, is related to a peripheral controller, and the peripheral controller does not meet the requirements of being a data processor with an integrated circuit package. It does not provide the execution unit, et cetera, that is required by Claim 9 of the '455 patent.

(Subramanian, Tr. at 1096-97.)

Moreover, referring to the claimed language "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus" the administrative law judge construed the language substantially as complainant and staff construed it. See supra. At the hearing, respondents' expert McAlexander identified a bi-directional bus in

Work. (CPFF 1070 (undisputed).) McAlexander did not, however, identify an external bus that is "used to bidirectionally communicate logic bits to and from the data processor," consistent with the construction of complainant and the staff.

With respect to the claimed language "a plurality of bus termination circuits," the administrative law judge's construction is substantially identical to the complainant and staff's proposed constructions. At the hearing, respondents' expert did not apply this construction to Work. (CPFF 1072 (undisputed).)

Referring to the claimed language "the plurality of bus termination circuits providing data to or receiving data from the execution unit," neither respondents nor their expert McAlexander established that Work meets said the limitation.

With regard to the claimed language "the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus," at the hearing, respondents' expert testified that he was not relying on Work for the "decouple" teaching to combine with Dasgupta. (CPFF 1075 (undisputed).)

In addition at the hearing, neither respondents nor their expert McAlexander provided adequate evidence in the records as to why a person of ordinary skill in the art at the time the '455 patent was filed would have combined the Dasgupta and Work references to render claims 9 and 10 obvious. (CPFF 1076.)

Based on the foregoing, the administrative law judge finds that respondents have not established by clear and convincing evidence that claims 9 and 10 of the '455 patent are obvious in view of any of the alleged combinations.

B. Lack Of Written Description

Respondents argued that the unambiguous language of the limitation of claim 9, viz.

"plurality of external pins . . . used to bidirectionally communicate logic bits to and from a data processor via an external bus" requires that data be passed from the external pins to the data processor by way of an external bus, and to the external pins from the data processor by way of an external bus; that there is no embodiment disclosed in the '455 patent that reads on this limitation; and that therefore claim 9 and dependent claim 10 of the '455 patent are invalid for lack of written description. (RBr at 122.)

Complainant argued that the parties dispute that the meaning of the limitation "plurality of external pins . . . used to bidirectionally communicate logic bits to and from a data processor via an external bus" is unambiguous, and that under complainant's and staff's interpretation, this element is consistent with all disclosed embodiments of the '455 patent. (CRBr at 95.)

As the Federal Circuit stated "[a] patent is presumed valid, and the burden of persuasion to the contrary is and remains on the party asserting invalidity." Ralston Purina Co. v. Far-Mar-Co, Inc., 72 F.2d 1570, 1573 (Fed. Cir. 1985). "In addition, the party asserting invalidity also bears the initial procedural burden of going forward to establish the legally sufficient prima facie case of invalidity." Id. "A party asserting invalidity based on 35 U.S.C § 112 bears no less a burden and no fewer responsibilities than any other patent challenger." Id. at 1574.

The written description requirement of section 112 is a question of fact. Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1565 (Fed. Cir. 1991). It asks whether the disclosure in an application as originally filed "reasonably conveys to the artisan that the inventor had possession at that time of the later claimed subject matter." In re Kaslow, 707 F.2d 1366, 1375 (Fed. Cir. 1983). To comply with the written description requirement, "the specification need not describe the claimed subject matter in exactly the same terms as used in the claims; it must simply indicate to persons skilled in the art that as of the [filing] date the applicant had invented what is now claimed." All

Dental Prodx, LLC v. Advantage Dental Prods., Inc., 309 F.3d 774, 779 (Fed. Cir. 2002) (quoting Eiselstein v. Frank, 52 F.3d 1035, 1038 (Fed. Cir. 1995)); see also In re Wilder, 736 F.2d 1516, 1520 (Fed. Cir. 1984) ("It is not necessary that the claimed subject matter be described identically"). The administrative law judge has found in Section VII F supra that the parties dispute the meaning of the limitation "plurality of external pins . . . used to bidirectionally communicate logic bits to and from a data processor via an external bus," that said limitation when properly construed means" a plurality of external pins used to bidirectionally communicate logic bits to and from a data processor via an external bus" and that the specification of the '455 patent supports said construction. Hence he finds that respondents have not established, by clear and convincing evidence, that asserted claims 9 and 10 of the '455 patent fail to meet the written description requirement of 35 U.S.C. § 112 ¶ 1.

XI. Remedy

In investigations in which a violation of Section 337 is found, the Commission may issue either a limited exclusion order or a general exclusion order and, if appropriate, cease and desist orders. See 19 U.S.C. §§ 1337(d) and (f). In this investigation, complainant Freescale seeks a limited exclusion order directed to the products of those respondents found to be infringing. (CBr at 127-8.) Freescale also seeks cease and desist orders. (Id. at 138-9.)

If there is a violation of Section 337, the staff believes that a limited exclusion order against the respondents found to infringe would be the appropriate recommendation. (SBr at 25.) With regard to cease and desist orders, the staff argued that respondents have stipulated as to their domestic inventories of infringing products, and that those inventory levels are commercially significant, citing e.g., Order No. 49, Exhibit A at ¶ 6{

} and Order Nos. 44 and 45. Thus, the staff argued that cease

and desist orders also would be an appropriate recommendation as to each of the respondents.

Respondents argued that the record demonstrates that no finding of a violation of § 337 is warranted in this investigation, and hence neither a limited exclusion order nor any cease-and-desist order should be recommended. It is further argued that in the event a finding of violation of § 337 is made, it is clear that neither an exclusion order nor a cease-and-desist order is warranted under the prevailing facts and circumstances, relying on Certain Erasable Programmable Read-Only Memories Components Thereof Products Containing Such Memories, and Processes For Making Such Memories (EPROMs), Inv. No. 337-TA-276, Comm'n Op. (May 1989), USITC Pub. 2196 aff'd sub nom. Hyundai Elec. Indus. Co. v. U.S. Intl trade Comm'n, 899 F.2d 1204 (Fed. Cir. 1990) (EPROMs).

The Commission has broad discretion in selecting the form, scope, and extent of a remedy in Section 337 proceedings. Certain Integrated Circuit Telecommunication Chips, Inv. No. 337-TA-337, Comm'n Op. at 21 (August 3, 1993). Pursuant to its statutory authority found at 19 U.S.C. § 1337 (d), the Commission may exclude from importation goods and products that form the basis for a finding of a violation of Section 337 which includes products that have been found to infringe the patents-in-suit directly, contributorily or by inducement after importation has occurred. 19 U.S.C. § 1337(d); Certain Flash Memory Circuits, Inv. No. 337-TA-382, Comm'n Op. at 26 (June 26, 1997) ("The Commission has the authority to enter an exclusion order, a cease and desist order, or both."). Indeed, absent special circumstances, the statute requires such exclusion:

> If the Commission determines ... that there is a violation of this section, it shall direct that the articles concerned ...be excluded from entry into the United States, unless, after considering the public health and welfare, competitive conditions in the United States economy, the production of like or directly competitive articles in the United States, and United States consumers, it finds

that such articles should not be excluded from entry.

19 U.S.C. § 1337(d). Hence, a remedy excluding respondents' infringing products from entry is mandatory if a violation of Section 337 is found, unless the Commission finds that public interest factors militate against such remedy.

Section 337(f) also permits the Commission to issue, in lieu of, or in addition to, an exclusion order, a cease and desist order directing persons found to have violated Section 337 to cease and desist from engaging in the unfair methods or acts involved. 19 U.S.C. § 1337(f). Cease and desist orders are warranted with respect to respondents that maintain commercially significant U.S. inventories of the infringing product. See, e.g., Certain Crystalline Cefadroxil Monohydrate, Inv. No. 337-TA-293, USITC Pub. 2391 at 37-42 (June 1991). The Commission has the authority to issue cease and desist orders where a respondent has a sufficient inventory of infringing goods in the United States. Certain NAND Flash Memory Circuits, Inv. No. 337-TA-526, 2005 ITC Lexis 859, Init. Determ. at *255 (Oct. 19, 2005) (citing Certain Plastic Encapsulated Integrated Circuits, Inv. No. 337-TA-315, U.S.I.T.C. Pub. No. 2574, Comm'n Op. at 37 (November 1992)).

Cease and desist orders are directed at a specific respondent in order to prevent the sale, distribution and other use of products that have already been imported into the United States prior to the entry and implementation of any exclusion order. Certain Curable Fluoroelastomer Compositions, Inv. No. 337-TA-364, Notice of Issuance of Limited Exclusion Order and Cease and Desist Order, 1995 WL 1049682 (Mar. 16, 1995). Cease and desist orders can preclude any activity "reasonably related to the importation of infringing products." Certain Hardware Logic Emulation Systems, Inv. No. 337-TA-383, Comm'n. Op. on Remedy, the Public Interest, and Bonding, 1998 WL 307240 (Feb. 28, 1998). Typical cease and desist orders enjoin a respondent

from selling, marketing, distributing and advertising its infringing products, as well as any solicitation of U.S. agents and distributors for the purpose of selling, marketing, distributing, and advertising infringing products. See Certain Electrical Connectors and Products Containing Same, Inv. No. 337-TA-374, Comm'n Cease and Desist Order, 1996 WL 1056313 (May 3, 1996).

At the outset, in issue is whether the requested relief is amenable to an EPROMs analysis. The Commission, in EPROMs, Comm'n Op. at 124-26, 136 identified the following relevant factors to be considered in determining whether an exclusion order should extend to downstream products:

> (1) the value of the infringing articles compared to the value of the downstream products in which they are incorporated;
>
> (2) the identity of the manufacturer of the downstream products, i.e., whether it can be determined that the downstream products are manufactured by the respondent or by a third party;
>
> (3) the incremental value to the complainant of the exclusion of downstream products;
>
> (4) the incremental detriment to respondents of exclusion of such products;
>
> (5) the burdens imposed on third parties resulting from exclusion of downstream products;
>
> (6) the availability of alternative downstream products that do not contain the infringing articles;
>
> (7) the likelihood that the downstream products actually contain the infringing articles and are thereby subject to exclusion;
>
> (8) the opportunity for evasion of an exclusion order that does not include downstream products; and
>
> (9) the enforceability of an order by Customs; and any other factors the Commission determines to be relevant.

See also Certain Liquid Crystal Display Modules, Products Containing Same, and Methods Using the Same, Inv. No. 337-TA-634, Comm. Op. at 4 (Nov. 24, 2009) (adopting Judge's analysis of EPROMs factors).

Complainant Freescale contended that its requested relief is not amendable to an EPROMs analysis. (CBr at 130.) The staff disagrees. (SRBr at 6.) Respondents argued that the EPROMs factors are appropriately applied in this investigation and while complainant addressed the EPROMs factors, the factors weigh against an exclusion order. (RRBr at 120-22.)

The administrative law judge finds that complainant Freescale's requested relief for an exclusion order is amendable to an EPROMs analysis. As the Commission stated in EPROMs:

> "[T]he Commission may, in issuing [limited] exclusion orders, . . . balance the complainant's interest in obtaining complete protection from all infringing imports by means of exclusion of downstream products against the inherent potential of even a limited exclusion order, when extended to downstream products, to disrupt legitimate trade in products which were not themselves the subject of a finding of violation of section 337."

EPROMs, Comm'n Op. at 125. As is clear from said quote, the point of an EPROMs analysis is to balance a complainant's interest in obtaining relief from all infringing imports against the disruption of legitimate trade in products not themselves the subject of a finding of violation of section 337. Thus, if respondents Funai manufactured or imported into the United States automobiles that incorporated the Zoran ICs, it is certainly questionable whether Freescale could obtain an order excluding those Funai automobiles because those automobiles "were not themselves the subject of a finding of violation of section 337," and the administrative law judge sees a big difference between automobiles and televisions and the importation on the one hand of automobiles and on the other hand televisions. There is certainly a large price differential. On the other hand, with regard to the Funai televisions that were the subject of this investigation and

which do incorporate the Zoran ICs, the administrative law judge finds no plausible argument that exclusion of those televisions would "disrupt legitimate trade." Also while complainant argued that the products that it seeks to be excluded are not "downstream products" but are Funai's "own infringing products" (CBr at 129) case law indicates that products containing an allegedly infringing product are "downstream" products. See Kyocera Wireless Corp. v. Int'l Trade Comm'n, 545 F.3d 1340, 1358 (Fed. Cir. 2008); see also Hyundai Elecs. Indus. Co. v. United States ITC, 899 F.2d 1204, 1206 (Fed. Cir. 1990).

Referring to the EPROMs factors and regarding the first EPROMs factor, viz. the value of infringing articles compared to the value of downstream products, while there is no evidence that the infringing Zoran integrated circuits per se are imported,{

} Funai televisions that are imported. As complainant's expert Subramanian testified:

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}

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}

(Tr. at 170, 195-96, 269-70 (emphasis added).)

Respondents argued that the complaint did not accuse Zoran integrated circuits or products containing Zoran integrated circuits of infringing any patent owned by Freescale, and Zoran integrated circuits were not mentioned at any point in the complaint. (RFF 2.) However, contrary to respondents' argument, the administrative law judge and the Commission in this investigation decided on multiple occasions that Funai products containing Zoran integrated circuits were within the scope of accused products described in Freescale's initial complaint. (See Order No. 8; Order No. 10; Order No. 11; Order No. 12; Order No. 13; Aug. 8, 2010 Notice Of Comm'n Det. Not to Review Init. Determ'n Granting Motion to Amend Complaint.) In addition, in response to Freescale's motion which resulted in Order No. 8, Funai had argued that the scope of this investigation is limited exclusively to ICs manufactured by Panasonic. (Order No. 8 at 3-5.) Also in Order No. 8, the administrative law judge rejected Funai's argument and compelled Funai to provide discovery on all of its accused products, including those that contain ICs manufactured by parties other than Panasonic. (Order No. 8 at 10-16 (ordering Funai to "respond to Freescale ... with respect to all products that Funai sells for importation, imports, or sells after importation

within the United States that contain an accused integrated circuit, regardless of the manufacturer of said integrated circuit").) In addition, respondents moved on June 25, 2010 to amend or clarify the notice of investigation to exclude, inter alia, Funai products containing non-Panasonic ICs from the scope of accused products. (Order No. 11 at 1-2.) In denying that motion in Order No. 11, the administrative law judge noted that the same issue was considered, and expressly rejected, in Order No. 8. (Order No. 11 at 5-6 ("Significantly, the administrative law judge found (in Order No. 8) that, contrary to Panasonic, Funai, and JVC's assertion, the 'integrated circuits' and 'chipsets' at issue in this investigation are not limited to those manufactured by Panasonic." and "[a]ccordingly, the administrative law judge found that Panasonic, Funai, and JVC's products fall within the scope of this investigation and a limited exclusion order in this investigation may properly cover said products, regardless of who is the manufacturer of the accused integrated circuit contained within such products.").) On July 16, 2010 respondents filed a motion for interlocutory review of Order No. 11 which motion for interlocutory review was denied. (Order No. 12.) On July 16, 2010, respondents filed a petition for Commission review of Order No. 10's initial determination granting Freescale's motion to amend the complaint. (See Order No. 13 at 1 (describing respondents' motion to stay pending Commission review of Order No. 10).) The Commission denied respondents' petition to review Order No. 10. (Aug. 8, 2010 Notice Comm'n Det. Not to Review Init. Determ'n Granting Motion to Amend Complaint.) Thus the administrative law judge rejects respondents' argument that Zoran integrated circuits or products containing said circuits are not in issue in this investigation and further finds that EPROMs factor 1 supports exclusion of Funai's downstream products.

Regarding EPROMs factor 2, viz. the identity of the manufacturer of the downstream products, i.e., whether it can be determined that the downstream products are manufactured by

the respondents or by a third party, the administrative law judge finds that it supports exclusion of Funai's downstream products because the Funai respondents are named respondents and import televisions.

Regarding EPROMs factor 3, viz. the incremental value to the complainant of the exclusion of downstream products, and factor 8, viz. the opportunity for evasion of an exclusion order that does not include downstream products, the administrative law judge finds that said factors support exclusion because if Funai's products are not excluded, Freescale would be denied any effective relief, as there is no evidence that the Funai respondents import infringing integrated circuits by themselves. As for factor 5, viz. the burdens imposed on third parties resulting from exclusion of downstream products, he finds that the burden would be non-existent because the order excluding Funai's downstream products would apply only to respondents Funai, not to any third-party. Referring to factor 6, viz. the availability of alternative downstream products that do not contain the infringing articles, said factor is also found to support exclusion of said Funai's downstream products because Freescale has licensed the '455 patent to several entities, including Panasonic, who can import their products irrespective of any exclusion order that may issue against Funai's products.

As for factor 7, viz. the likelihood that the downstream products actually contain the infringing article and are thus subject to exclusion, identification of the Funai products that contain the infringing chips can be done. Thus at the hearing, complainant's expert Subamanian testified as to the specific Funai products that contain the infringing chips referring to CX-122C, pages 9 and 10. Also Funai has stipulated that "the brand names listed in [CX-80C, CX-122C, and CX-164C] are the names used on packaging or crates of the products listed in response to those interrogatories during importation into the United States." (CPFF 1190 (undisputed).)

Additionally, there is no evidence that such products are assembled in the United States. (CPFF 1191 (undisputed).)

Referring to factor 9, viz. the enforceability of an order by Customs with respect to the Funai products that incorporate infringing chips, the infringing chips are found in specific products produced by Funai. (Subramanian, Tr. at 169-173.) Also as found supra, Funai has stipulated that the brand names listed in CX-80C, CX-122C, and CX-164C are the names used on packaging or crates of the products listed in response to those interrogatories during importation into the United States. Thus Customs can identify the Funai televisions based on said brand names.

Referring to the foregoing and based on the EPROMs factors, the administrative law judge finds that a limited exclusion order directed to respondents' products that incorporate the infringing integrated circuits would be appropriate.

With regard to any cease and desist order, respondents Funai have stipulated that {

} after they had been imported, sold for importation, or sold after importation into the United States. (Order No. 49, Exhibit A at ¶¶ 5-6.) Thus the administrative law judge recommends appropriate cease and desist orders be issued against the respondents.

XII. Bond

Complainant argued that the Commission should require a 100% bond. (CBr at 139-44.)

Respondents argued that no bond should be imposed during any Presidential period and that complainant apparently is under the "misimpression that no evidence on bonding is necessary and that a 100% bond is essentially automatic." (RBr at 130-31.)

The staff argued that it appears that complainant Freescale did not pursue evidence

regarding the pricing of respondents' accused products, that notwithstanding complainant's decision not to seek said information from respondents, Freescale seeks a bond in the amount of 100% of the entered value of any infringing product; that in light of Freescale's failure to pursue relevant discovery on the issue of what constitutes an appropriate bond, it has failed to carry its burden of proving that a 100% bond should be imposed, citing Certain Rubber Antidegradants, Components Thereof, and Products Containing Same, Inv. No. 337-TA-533, Comm'n Op., 2006 ITC LEXIS 591, at *59 (July 21, 2006); that in addition Freescale has not shown that it is entitled to a bond of 100% of entered value, at least because there is evidence that tends to establish a reasonable royalty, citing Certain Stringed Musical Instruments and Components Thereof, Inv. No. 337-TA-586, Final Initial and Recommended Determination, 2007 ITC LEXIS 1226, at *47-48 & n.116 (Dec. 3, 2007) (reviewed on other grounds); and that none of said evidence (in the form of license agreements) was presented or admitted at the evidentiary hearing. Thus, the staff argued that no bond should be imposed.

Section 337(j)(3) provides for the entry of infringing articles upon the payment of a bond during the sixty-day Presidential review period. 19 U.S.C. § 1337(j)(3). Any bond is to be set at a level sufficient to "offset any competitive advantage resulting from the unfair method of competition or unfair act enjoyed by persons benefiting from the importation." Certain Dynamic Random Access Memories, Components Thereof and Products Containing Same, Inv. No. 337-TA-242, Commission Opinion on Violation, Remedy, Bonding and the Public Interest, USITC Pub. No. 2034, 1987 WL 450856 (U.S.I.T.C.) at 38 (1987). When reliable price information is available, the Commission has set a bond by eliminating the price differential between the domestic and the imported infringing product. Certain Digital Satellite System (DSS) Receivers and Components Thereof, Inv. No. 337-TA-392, Final Initial and

Recommended Determination on Remedy and Bonding, U.S.I.T.C. Pub. No. 3418, 2001 WL 535427 (U.S.I.T.C.) at 336 (April 2001). Where reliable price information is not available, Commission precedent establishes that the bond should be set at 100%. Certain Semiconductor Memory Devices and Products Containing Same, ITC Inv. No. 337-TA-414, Recommended Determination on Remedy and Bonding, 1999 WL 1267282 (U.S.I.T.C.) at 6 (December 13, 1999).

While complainant Freescale has argued that it has "identified a wide range of products that infringe the '455 patent, and a wide range of prices for these products"(CRBr at 103), a bond set at 100% is levied only when reliable price information is not available. See Certain Flash Memory Circuits and Products Containing Same, Inv. No. 337-TA-382, USITC Pub. No. 3046, Comm'n Op. at 26-27 (July 1997) (100% bond imposed only when price comparison was not practical because the parties sold products at different levels of commerce, and the proposed royalty rate appeared to be de minimis and without adequate support in the record.). However there are indications that reliable price information may have been available to complainant Freescale. For example, and merely as an illustration, as recited in the Procedural History, supra, Order No. 50 terminated the investigation as to certain respondents based on a settlement agreement and licensing agreement relating to each of the '306 patent, the '014 patent and certain claims of the '455 patent. Complainant, in arguing for a 100% bond and in spite of said licensing agreement, made no attempt to argue that any such licensing agreement would not establish a reasonable royalty for claims 9 and 10 of the '455 patent.

Based on the foregoing, the administrative law judge denies complainant's request for a bond set at 100% and further recommends that no bond be set.

XIII. Additional Findings

1. Complainant Freescale Semiconductor, Inc. (Freescale) is a Delaware corporation with its headquarters located at 6501 William Cannon Drive West, Austin, Texas. (Sept. 14, 2010 2nd Amd. Complaint at ¶ 5.)

2. Freescale was formed in 2004 as a result of the divestiture of the Semiconductor Products Sector of Motorola, Inc. (Sept. 14, 2010 2nd Amd. Complaint at ¶ 5.)

3. Respondent Funai Electric Co., Ltd. is a corporation organized under the laws of Japan, and maintains its principal place of business in Daito, Osaka, Japan. (Sept. 14, 2010 2nd Amd. Complaint at ¶ 62-69.)

4. Respondent Funai Electric Co., Ltd. is the world-wide parent corporation for Funai entities. (Sept. 14, 2010 2nd Amd. Complaint at ¶ 62-69.)

5. Respondent Funai Corporation, Inc. is a corporation organized under the laws of New Jersey, and maintains its principal place of business at 201 Route 17, Ste 903, Rutherford, New Jersey 07070. (Sept. 14, 2010 2nd Amd. Complaint at ¶ 62-69.)

6. Respondent Best Buy Purchasing, LLC is a Minnesota limited liability company having its principal place of business at 7601 Penn Avenue S., Richfield, Minnesota 55423. (Sept. 14, 2010 2nd Amd. Complaint at ¶ 90-95.)

7. Respondent Best Buy.Com, LLC is a Virginia limited liability company with its principal place of business at 7601 Penn Avenue S., Richfield, Minnesota 55423. (Sept. 14, 2010 2nd Amd. Complaint at ¶ 90-95.)

8. Respondent Best Buy Stores, L.P. is a Virginia limited partnership with its principal place of business at 7601 Penn Avenue S., Richfield, Minnesota 55423.

(Sept. 14, 2010 2nd Amd. Complaint at ¶ 90-95.)

9. Respondent Wal-Mart Stores, Inc. is a Delaware corporation having its principal place of business at 708 SW 8th Street, Bentonville, Arkansas 72716. (Sept. 14, 2010 2nd Amd. Complaint at ¶ 100-102.)

CONCLUSIONS OF LAW

1. The Commission has in personam and in rem jurisdiction.

2. There has been an importation of accused integrated circuits, chipsets, and products containing same including televisions, media players, and cameras into the United States which are the subject of the unfair trade allegations.

3. It has not been established that claims 9 and 10 of the '455 patent are invalid.

4. Complainant has failed to show that asserted claims 9 and 10 of the '455 patent are infringed.

5. Complainant has established a domestic industry.

6. The evidence establishes that there is no violation of section 337.

7. In the event a violation of section 337 is found, limited exclusion orders and cease and desist orders are recommended. However no bond is recommended.

ORDER

Based on the foregoing, and the record as a whole, it is the administrative law judge's Final Initial Determination that there is no violation of section 337 in the importation into the United States, sale for importation, and sale within the United States after importation of integrated circuits, chipsets, and products containing same including televisions, media players, and cameras. It is also the administrative law judge's recommendation, should a violation be found, that limited exclusion orders issue barring entry into the United States of infringing integrated circuits, chipsets, and products containing same including televisions, media players, and cameras and that appropriate cease and desist orders should issue. The administrative law judge does not recommend any bond.

The administrative law judge hereby CERTIFIES to the Commission his Final Initial and Recommended Determinations. The briefs of the parties, filed with the Secretary, are not certified, since they are already in the Commission's possession in accordance with Commission rules.

Further it is ORDERED that:

1. In accordance with Commission rule 210.39, all material heretofore marked in camera because of business, financial and marketing data found by the administrative law judge to be cognizable as confidential business information under Commission rule 201.6(a), is to be given in camera treatment continuing after the date this investigation is terminated.

2. Counsel for the parties shall have in the hands of the administrative law judge those portions of the final initial and recommended determinations which contain bracketed confidential business information to be deleted from any public version of said determinations, no later than April 18, 2011. Any such bracketed version shall not be served via facsimile on the administrative law judge. If no such bracketed version is received from a party, it will mean that the party has no objection to removing the confidential status, in its entirety, from these initial and recommended determinations.

3. The initial determination portion of the Final Initial and Recommended Determinations, issued pursuant to Commission rules 210.42(a) and 210.42-46, shall become the determination of the Commission, unless the Commission, shall have ordered its review of certain issues therein or by order has changed the effective date of the initial determination portion. The recommended determination portion, issued pursuant to Commission rule

210.42(a)(1)(ii), will be considered by the Commission in reaching a determination on remedy pursuant to Commission rule 210.50(a).

Paul J. Luckern
Chief Administrative Law Judge

Issued: April 4, 2011

CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS, MEDIA PLAYERS, AND CAMERAS **337-TA-709**

PUBLIC CERTIFICATE OF SERVICE

I, James R. Holbein, hereby certify that the attached **Public Version Final Initial and Recommended Determinations** has been served by hand upon the Office of Unfair Import Investigations, and the following parties as indicated, on

May 12, 2011.

James R. Holbein, Acting Secretary
U.S. International Trade Commission
500 E Street, SW
Washington, DC 20436

Complainant Freescale Semiconductor, Inc.:

( ) Via Hand Delivery
(X) Via Overnight Mail
( ) Via First Class Mail
( ) Other: _____

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For Respondents Funai Electric Co., Ltd; Funai Corporation, Inc.; Best Buy Purchasing, LLC; BestBuy.Com, Inc., Best Buy Stores, L.P. :

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(X) Via Overnight Mail
( ) Via First Class Mail
( ) Other: _____

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PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	
CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS, MEDIA PLAYERS, AND CAMERAS	Inv. No. 337-TA-709

Final Initial and Recommended Determinations

This is the administrative law judge's Final Initial Determination under Commission rule 210.42. The administrative law judge, after a review of the record developed, finds inter alia that there is jurisdiction and that there is no violation of section 337 of the Tariff Act of 1930, as amended.

This is also the administrative law judge's Recommended Determination on remedy and bonding, pursuant to Commission rules 210.36(a) and 210.42(a)(1)(ii). Should the Commission find a violation, the administrative law judge recommends the issuance of limited exclusion orders barring entry into the United States of infringing integrated circuits, chipsets and products containing same including televisions, media players, and cameras as well as the issuance of appropriate cease and desist orders. The imposition of any bond during the Presidential Review period is not recommended.

TABLE OF CONTENTS

ABBREVIATIONS

CBr	Complainant's Post Hearing Brief
CRBr	Complainant's Post Hearing Reply Brief
CPFF	Complainant's Findings of Fact
CRFF	Complainant's Rebuttals to Respondents' Findings of Fact
RBr	Respondents' Post Hearing Brief
RRBr	Respondents' Post Hearing Reply Brief
RFF	Respondents' Findings of Fact
RRFF	Respondents' Rebuttal Findings of Fact
SBr	Staff's Post Hearing Brief
SRBr	Staff's Post Hearing Reply Brief
SRFF	Staff's Responses to Respondents' Findings of Fact

OPINION

I. Procedural History

By notice dated March 29, 2010, the Commission instituted an investigation, pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, to determine inter alia (a) whether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain integrated circuits, chipsets, or products containing same including televisions, media players, or cameras that infringe one or more of claims 1, 8-10, 22, and 26 of U.S. Patent No. 5,467,455 ('455 patent), claims 1 and 10 of U.S. Patent No. 5,715,014 ('014 patent), and claims 1, 6, 11, and 13-16 of U.S. Patent No. 7,199,306 ('306 patent).

The complaint, relating to the investigation, was filed with the Commission on March 1, 2010, under section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, on behalf of Freescale Semiconductor, Inc. (Freescale). A letter supplementing the complaint was filed on March 18, 2010. The complainant requested that the Commission institute an investigation and, after the investigation, issue an exclusion order and cease and desist orders. The following were named in the notice of investigation as respondents and were served with the complaint: Panasonic Corporation, Panasonic Semiconductor Discrete Devices Co., Ltd. (PSDD) and Panasonic Corporation of North America; Funai Electric Co., Ltd. and Funai Corporation, Inc. (Funai); JVC Kenwood Holding, Inc. (JVC); Victor Company of Japan Limited (Victor); JVC Americas Corp. (JVC); Best Buy Co., Inc. (Best Buy); B & H Foto & Electronics Corp. (B&H); Huppin's Hi-Fi Photo & Video, Inc. (Huppin's); Buy.com Inc. (Buy); Liberty Media Corporation (Liberty); QVC, Inc. (QVC); Crutchfield Corporation; (Crutchfield); Wal-Mart Stores, Inc. (Wal-Mart); and Computer Nerds International, Inc. (Computer Nerds).

By notice dated April 22, 2010, the investigation was permanently reassigned to the undersigned.

Order No. 2, which issued on April 2, 2010, set a sixteen month target date of August 2, 2011, which meant that any final initial determination on violation should be filed no later than Monday April 4, 2011.[1]

On July 8, 2010, Order No. 10 granted complainant's motion for leave to amend its complaint to (1) correct clear typographical errors; (2) replace one respondent, viz. Best Buy, whose counsel has represented that it does not sell for importation, import, or sell after importation any accused products and has provided an identification of substitute parties, viz. Best Buy Purchasing, LLC, Best Buy.com, Inc. and Best Buy Stores, L.P. that should be added in Best Buy's place; and (3) add additional dependent claim 2 of the '306 patent and, with respect to (2) supra, correct the Notice of Investigation.

On August 3, 2010, Order No. 15 granted complainant's motion for termination of the investigation as to respondents PSDD and JVC. The Commission non-reviewed Order No. 15 on September 2, 2010.

On September 30, 2010, Order No. 20, granted complainant's motion for leave to amend its complaint and the notice of investigation to: (1) change the name of one respondent from BestBuy.com, Inc. to BestBuy.com, LLC; (2) correct the addresses of BestBuy.com, LLC and Best Buy Purchasing, LLC; and (3) terminate one respondent, namely Liberty, whose counsel had represented that it does not sell for importation, import, or sell after importation any accused products. The Commission non-reviewed Order No. 20 on October 21, 2010.

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[1] The notice of publication was published on April 2, 2010 (75 Fed. Reg. 16,837).

Order No. 33, which issued on January 5, 2011, granted complainant's motion that it has satisfied the requirements of 19 U.S.C. § 1337 (a)(3) in that a domestic industry based on licensing activities exists in the United States for each of the patents in issue in this Investigation, viz. the '455 patent, the '014 patent and the '306 patent. The Commission non-reviewed Order No. 33 on February 4, 2011.

Order No. 34, which issued on January 5, 2011, granted a motion of certain respondents for summary determination of non-infringement of claim 1 of the '306 patent. The Commission, in a notice dated February 7, 2011 extended the date for determining whether to review Order No. 34 by sixty (60) days to April 11, 2011.

The administrative law judge did not conduct a "tutorial." However Order No. 36, which issued on January 13, 2011 and was considered an "education vehicle" for the administrative law judge, required submissions from complainant, respondents and the Commission Investigative Staff (staff) with said order making reference to the prehearing briefs of respondents and the staff and posing, inter alia, the following question for respondents:

> 35. Referring to the '455 patent and respondents' invalidity assertions of the asserted claims on prior art, as the staff argued (SPre at 70-71) respondents allege some ten separate anticipatory prior art references for the asserted claims and further assert over 40 different permutations of prior art combinations as invalidating under section 103, including combinations of prior art that are also alleged to anticipate. Moreover in fn 31 the staff in its SPre argued that besides being unreasonably large in number, the invalidity assertions in respondents' pre-hearing brief also suffer from a dearth of detail. The administrative law judge agrees. The respondents are put on notice that, in response to this question, unless respondents supplement their prior art invalidity arguments with specific facts, said arguments will be stricken from the RPre and respondents will not be permitted to present said arguments at the evidentiary hearing. Respondents' supplementation, in response to this question, should factually address each of the assertions raised in CPre

> at 425-78 and in CSPre at 17-21. Merely as an illustrative example, respondents are directed to the statements of complainant regarding Gist (CPre at 427-34). For example do respondents agree that in Gist there is a separate integrated circuit for the bus interface circuits, apart from whatever integrated circuit may also be part of the device or module. If respondents do not agree, respondents should make specific reference to exhibits in support. A reference to charts will carry no weight. On this point, the staff in its fn 31 has represented that respondents' expert on the '455 patent even testified that the reader of charts had to "infer" which claim elements were where in the prior art references. Such testimony, if made at the evidentiary hearing, will not meet the clear and convincing standard that respondents must meet in invalidating claims over prior art. As additional examples of the inadequacy of the portion of RPre relating to the alleged invalidity of the asserted claims of the '455 patent, respondents argued (RPre at 178) that "as detailed in RX-0635, each and every element of claims 1, 8, 9, 10, 22 and 26 of the '455 patent are found explicitly or inherently in the teachings of the Gist patent." Similar language, on anticipation with respect to other art is found at RPre 180, 181, 182, 183, 185, 186, 187. Like language, as to obviousness is found at RPre at 191, 192, 194, 195, 197, 198, 199, 201, 202.

(Order No. 36 at 7.) Said Order 36 required filings from complainant and the respondents by January 21, 2011, reply submissions from said parties by January 27, 2011, submission from the staff by January 31, 2011 and further reply submissions from the private parties by Febuary 2, 2011.

Order No. 37, which issued on January 13, 2011, directed the private parties to report regarding any settlement. Order No. 38, which issued on January 20, 2011, allowed complainant and respondents Funai to conduct the settlement conference required by Order No. 37 before February 1, 2011 in Japan without a representative from the staff present.

Order No. 40, which issued on January 24, 2011, granted the motion of complainant, respondents Panasonic Corporation and Panasonic Corporation of North America (Panasonic), JVC, Victor, Funai, except as to products of Funai that incorporate Zoran ICs, and the remaining

respondents (retailer respondents) to suspend all upcoming deadlines through January 28, 2011 with respect to Panasonic, JVC, and all retailer respondents, except as to products of Funai that incorporate Zoran ICs.

Order No. 41 which issued on Januay 28, 2011, granted complainant's motion to suspend the procedural schedule and evidentiary hearing indefinitely as to respondents Panasonic, Victor, JVC, Crutchfield,[2] Huppin's and Computer Nerds, based on a Memorandum of Understanding (MOU) between complainant and Panasonic as to covered products and parties.

Order No. 42, which issued on January 28, 2011, granted Motion No. 709-73 of complainant and respondents Funai to the extent that the prehearing conference and hearing was to commence on February 7, 2011 and continue on February 8 and 9 as requested by the private parties. A request to modify ground rule 19(x) to permit the exchange of demonstratives no later than twenty-four hours before they were proposed to be used at the hearing was denied.

Order No. 43, which issued on February 4, 2011, related to a stipulation involving importation and Funai and said Order was superceded by Order No. 49, which included a stipulation identical to the Order 43 stipulation but which also includeed citations to certain exhibits. Order No. 44, which also issued on February 4, 2011, related to a stipulation involving respondent Wal-Mart while Order No. 45, which also issued on February 4, 2011, related to a stipulation involving respondents Best Buy Purchasing, LLC, Best Buy.com, LLC, and Best Buy Stores, L.P. Order No. 46 and Order No. 47 which also issued on February 4, 2011 related to

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[2] In a telephone conversation on January 28, 2011 between the attorney adviser and complainant's counsel, and also in an email from complainant's counsel to the attorney advisor, it was represented that respondent B & H Foto & Electronics Corp. is not to be suspended from the investigation, but respondent Crutchfield should be suspended.

stipulations involving respondent QVC, Inc. and respondent B&H, respectively.

Order No. 48, which issued on February 7, 2011, terminated the investigation as to respondents Victor, JVC, B & H, Huppins, Buy, QVC, Crutchfield, and Computer Nerds (Released Respondents) on the basis of withdrawing complainant's claims against said Released Respondents. On February 28, 2011, the Commission non-reviewed Order No. 48. On March 2, 2011, Order No. 50 issued which terminated the investigation as to respondents Panasonic based on a settlement and licensing agreement that resolved the proceeding against said respondents. It also terminated the investigation as to the '306 patent, the '014 patent and claims 1, 8, 22 and 26 of the '455 patent. Hence, only claims 9 and 10 of the '455 patent are in issue in this investigation.

Arguments on several motions in limine were heard on February 3, 2011. A prehearing conference was conducted on February 7, 2011. At said conference, rulings were made on said motions in limine. (Tr. at 33-53.)

A three day evidentiary hearing was conducted on February 7, 8, and 9. The only respondents that participated in the hearing were Funai Electric Co., Ltd., Funai Corporation, Inc., Wal-Mart Stores, Inc., Best Buy Purchasing, LLC, BestBuy.Com, LLC and Best Buy Stores, L.P. Post hearing submissions have been filed.[3] This matter is now ready for decision.[4]

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[3] The staff did not file any rebuttal findings to complainant's proposed findings.

[4] Respondents in their RBr at 50-54 requested that the administrative law judge "reverse his ruling striking Mr. McAlexander's testimony [citing 800:10-814:10; 868:11-892:15; 904:24-913:15]." A motion for reconsideration requires more than simply rearguing points made at the evidentiary hearing. Rather there are only three possible grounds for any motion for reconsideration: "(1) an intervening change in controlling law, (2) the availability of new evidence not previously available, and (3) the need to correct a clear error of law or prevent manifest injustice." Atkins v. Marathon LeTourneau Co., 130 F.R.D. 625, 626 (S.D. Miss. 1990)

The Final Initial and Recommended Determinations are based on the record compiled at the hearing and the exhibits admitted into evidence. The administrative law judge has also taken into account his observation of the witnesses who appeared before him during the hearing. Proposed findings of fact submitted by the parties not herein adopted, in the form submitted or in substance, are rejected as either not supported by the evidence or as involving immaterial matters and/or as irrelevant. Certain findings of fact included herein have references to supporting

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(citing Natural Resources Defense Council v. United States Envtl. Protection Agency, 705 F. Supp. 698, 702 (D.D.C. 1989)). See also Bulley v. Fid. Fin. Servs. of Miss., Inc., 2000 U.S. Dist. LEXIS 13481, 4-5 (S.D. Miss. Sept. 8, 2000); In re King, 2005 Bankr. LEXIS 2896 (Bankr. S.D. Ohio July 15, 2005) ("To constitute 'newly discovered evidence,' the evidence must have been previously unavailable." GenCorp, Inc. v. Am. Int'l Underwriters, 178 F.3d 804, 834 (6th Cir. 1998)(citations omitted).) "As a general principle, motions for reconsideration are granted if the moving party demonstrates: (1) a clear error of law; (2) newly discovered evidence that was not previously available to the parties; or (3) an intervening change in controlling law." Owner-Operator Indep. Drivers Assn v. Arctic Express, Inc., 288 F. Supp. 2d 895, 900 (S.D. Ohio 2003)(citing GenCorp, 178 F.3d at 834). "Motions for reconsideration do not allow the losing party to 'repeat arguments previously considered and rejected, or to raise new legal theories that should have been raised earlier.'" Id., internal citation omitted. The administrative law judge finds that respondents did not establish any of said grounds for a motion for reconsideration. In addition Commission rule 210.15, which relates to motions, was not followed. Thus on procedural grounds, respondents request that the administrative law judge reverse any rulings striking McAlexander's testimony is denied.

Complainant in its CBr at 111, 114 and 118 moved to strike certain of McAlexander's trial testimony. However Commission rule 210.15 was not followed. Hence said motion is also denied on procedural grounds.

Respondents also in their post-hearing submissions requested that "Section IV.A.6 of Freescale's Post-hearing Brief, and CPFF 263-325, be struck, pursuant to Order no. 42..." (RRBr at 50, n. 30) on the ground that complainant's "new argument" was not disclosed in complainant's pre-hearing brief or in Subramanian's expert report. (Id.) However Commission rule 210.15 was not followed. Hence said request is denied.

Respondents in addition in their RFF made reference to numerous motions to strike e.g. ROCPFF 297, which reads "Move to strike... Attorney argument proffered as finding of fact." Because Commission rule 210.15 was not followed, said motions are denied.

evidence in the record. Such references are intended to serve as guides to the testimony and exhibits supporting the finding of fact. They do not necessarily represent complete summaries of the evidence supporting said findings.

II. Jurisdiction Including Parties And Importation

Section 337 of the Tariff Act of 1930, as amended, declares unlawful the importation into the United States, the sale for importation, or the sale within the United States after importation by the owner, importer, or consignee, of articles that infringe a valid and enforceable United States patent if an industry in the United States relating to the articles protected by the patent exists or is in the process of being established. See 19 U.S.C. §§ 1337 (a)(1)(B)(i) and (a)(2). Section 337 also provides that the Commission shall investigate alleged violations of said section and is empowered to hear and decide actions involving alleged unfair acts under the Section. See Certain Steel Rod Treating Apparatus, Inv. No. 337-TA-97, Commission Opinion, 215 U.S.P.Q. 229, 231 (June 30, 1981). Section 337 proceedings are in rem, making in personam jurisdiction unnecessary. However due process requires that the notice of investigation be provided to persons with an interest in the property at issue in a manner reasonably calculated to inform them of the pendency of an action so that they may have an opportunity to appear and defend their interests. Id. at 232, Certain Ammonium Octamolybdate Isomers, Inv. No. 337-TA-477, Init. Det. at 8 (May 15, 2003).

For identification of the private parties in this invesgitation, see Section XIII, FF1-9. With regard to importation, the private parties have entered into several stipulations concerning, for example, the importation requirement and domestic inventory of accused products. See Order No. 49 (Feb. 9, 2011), Order No. 44 (Feb. 4, 2011), and Order No. 45 (Feb.4, 2011). Hence the

Commission possesses subject matter jurisdiction.

Respondents have participated in the evidentiary hearing in this investigation and have not pleaded an affirmative defense of lack of personal jurisdiction. See Certain SteelRod Treating Apparatus, Inv. No. 337-TA-97, Order No. 13 (May 8, 1981) (noting that failure to consolidate threshold procedural matters in a timely manner constitutes waiver), aff'd on other grounds, Commission Memorandum Opinion at 3 (June 29, 1981). Hence the Commission also possesses personal jurisdication.

III. Technology In Issue

The parties have stipulated to the following general overview of technology in issue (JX-2):

> 1. The technology at issue relating to the '455 patent involves, inter alia, bus termination circuitry that may be enabled or disabled to reduce unwanted signal reflection on a bus. A bus may be used to transmit signals between two or more devices (e.g., a memory device, communication device, interface device or peripheral device). Depending on the direction of the signal, a given device may be a sender or a receiver. A bus on which signals may be transmitted in either direction is known as a "bidirectional" bus.
>
> 2. Signal reflection may occur when the load impedance of the receiver does not match the characteristic impedance of the conductive path, e.g., wiring between two devices on a printed circuit board connected by a bus or one or more conductive traces. When the impedance of the receiving device and the conductive path are not matched, the signal partially bounces off or "reflects" from the receiver.
>
> 3. Signal reflection interferes with the transmitted signal which may cause transmission of signals to the conductive path to be slowed and/or altered in amplitude. A reduction in signal reflection, therefore, allows a more rapid signal propagation. on the conductive path. Signal reflection can be reduced by using termination such as adding an impedance at or near the receiving end of a conductive path.

4. Among the methods of terminating a conductive path, known at the time of the '455 patent's filing, was through the addition of a resistor at or near the receiving end. Other known methods included adding a capacitor, a PN junction, a diode, a resistive device, an inductor, an N channel transistor, a P channel transistor, a junction field effect transistor (JFET), a metal oxide semiconductor transistor (MOSFET), a bipolar device, a Bi-CMOS device, a current source, a voltage source, or any other like termination component or circuit to the receiving end of the conductive path. Permanently connected termination circuitry usually caused increased power consumption.

5. The '455 patent describes determining whether, for example, a data processor will be receiving data or sending data external to the processor. In one embodiment of the '455 patent, the disclosed termination circuitry is enabled if the data processor is receiving data from the bus in order to reduce signal reflection when the processor is receiving a signal from the bus. The disclosed termination circuitry is disabled if the data processor is sending data to the bus. The '455 patent calls this "dynamic termination." When the data is incoming, i.e., the data processor is receiving, the termination circuitry is enabled. When the data is outgoing, i.e., the data processor is transmitting, the termination circuitry is disabled.

6. In one embodiment of the '455 patent discloses that a control signal is used to enable the disclosed termination circuit. The enabled termination circuit electrically "couples" a circuit component to the bidirectional bus. The circuit component, when "coupled" to the bus, provides termination to the bus. When the control signal is not asserted, the disclosed circuit component is not electrically "coupled" to the bidirectional bus.

7. In one embodiment, the '455 patent also discloses that a series of control signals may be used to activate multiple termination circuits within a given device. When a given control signal is sent, the termination circuit responding to that control signal electrically couples the respective termination circuit component to the bidirectional bus. In this way, the '455 patent discloses the ability to adjust the termination impedance that is "coupled" and "decoupled" from the bus by selectively enabling one or more of the termination circuits.

IV. Experts

Vivek Subraramanian was qualified at the hearing as complainant's expert in the field of

electrical engineering and integrated circuits. (Tr. at 21.) Joseph C. McAlexander III was qualified at the hearing as respondents' expert in the field of electrical engineering and integrated circuits. (Tr. at 647.)

V. Person of Ordinary Skill

The level of ordinary skill in the art of the '455 patent is at least a Bachelor of Science degree in electrical engineering or equivalent, with a few years of experience, particularly focused on issues related to memories and memory systems such as described in the "Background Of The Invention" section of the '455 patent. (JX-1; Subramanian, Tr. at 122-3, McAlexander, Tr. at 673.)

VI. Claims in Issue

Asserted claim 9 of the '455 patent states:

> A data processor within an integrated circuit package comprising:
>
> an execution unit internal to the data processor;
>
> a plurality of external pins connected to the integrated circuit package, the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus;
>
> a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one bus termination circuit, the plurality of bus termination circuits providing data to or receiving data from the execution unit, each bus termination circuit in the plurality of bus termination circuits having an input for receiving a control signal;
>
> a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one

circuit component from the bus.

(JX-1 at 10:26-52.)

Asserted claim 10 of the '455 patent states:

> The data processor of claim 9 wherein the at least one circuit component is a circuit component selected from a group consisting of: a capacitor, a diode, a resistor, a transistor, a voltage source, a current source, an electrical short circuit, and an inductor.

(JX-1 at 10:53-57.)

VII. Claim Construction

The claims of a patent define the invention to which the patentee is entitled the right to exclude. Phillips v. AWH Corp., 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (Phillips). The words of a claim are generally given their ordinary and customary meaning. Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996). The ordinary and customary meaning of a claim term is the meaning the term would have to a person of ordinary skill in the art at the time of the invention, i.e., constructively the effective filing date of the patent application. Phillips, 415 F.3d at 1313. The ordinary meaning of a claim term as understood by a person of ordinary skill in the art may in some circumstances be readily apparent to laymen. See Brown v. 3M, 265 F.3d 1349, 1352 (Fed. Cir. 2001). However, "[w]hen the parties present a fundamental dispute regarding the scope of a claim term, it is the court's duty to resolve it." O2Micro Int'l Limited v. Beyond Innovation Technology Co., 521 F.3d 1351, 1362 (Fed. Cir. 2008). When giving a claim term meaning, "the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." Phillips, 415 F.3d at 1313. In construing the claims, the court should also consider "the patent's prosecution history, if it is in evidence."

Markman v. Westview Instruments, Inc., 52 F,3d 967, 976, 980 (Fed. Cir. 1995).

While information extrinsic to the patent and its prosecution history may be considered, it is often "less reliable than the patent and its prosecution history." Phillips, 415 F.3d at 1318 (noting that litigation-derived expert reports and testimony are especially suspect). "[E]xpert testimony at odds with the intrinsic evidence must be disregarded." Network Commerce, Inc. v. Microsoft Corp., 422 F.3d 1353, 1361 (Fed. Cir. 2005) (holding that unsupported conclusions concerning patent claims provide little support for suggested claim construction). Not all extrinsic information, however, must be disregarded. For example:

> [i]n some cases, the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words. See Brown v. 3M,265 F.3d 1349, 1352 (Fed Cir. 2001) (holding that the claims did "not require elaborate interpretation"). In such circumstances, general purpose dictionaries may be helpful.

Phillips 415 F.3d at 1314. However, in many cases that give rise to litigation, determining the ordinary and customary meaning of a claim requires examination of terms that have a particular meaning in a field of art. Because the meaning of a claim term as understood by persons of skill in the art is often not immediately apparent, and because patentees frequently use terms idiosyncratically, the court looks to those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean. Id. Those sources include the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art. See Gemstar-TV Guide Int'l, Inc. v. Int'l Trade Comm'n, 383 F.3d 1352, 1364 (Fed. Cir.2004); Vitronics, 90 F.3d at 1582-83; Markman, 52 F.3d at 979-80.

At issue are claims 9 and 10 of the '455 patent.

A. The claimed phrases "circuit" and "circuitry"

The claimed phrase "circuit" appears in asserted claim 9. The phrase "circuitry" does not appear in either asserted claim 9 or 10.

Complainant argued that neither of these claimed phrases need to be construed, as its expert testified that there was no difference or contradiction between the parties proposed plain and ordinary meanings. (CBr at 57.) Complainant further argued that, to the extent the administrative law judge deems a construction to be necessary, "circuit" and "circuitry" should both be construed as an "assemblage of electronic elements." (CBr at 57.)

Respondents argued that complainant and respondents agreed that said claimed phrases should be given their plain and ordinary meaning, which respondents assert is "an interconnection of circuit elements," in accordance with the specification. (RBr at 70.) Respondents further argued that complainant's expert opined that there was no substantive difference between complainant's construction, which is an "'assemblage' of elements," and respondents' construction. (RBr at 70.)

The staff argued that the claimed phrase "circuit" should be accorded its plain meaning, as there is no dispute. (SBr at 12.)

As circuitry is no longer a claimed phrase and the parties agree that neither "circuit" nor "circuitry" need to be construed, and that the exact definition does not substantively affect issues in this investigation, the administrative law judge accords these terms their plain and ordinary meaning, which he will take to be an assemblage of electronic elements, i.e. complainant's construction instead of respondents' construction, because respondents use a term to be defined

(viz. circuit) in the definition of that term, which is to be avoided. The administrative law judge does, however, understand that there is no substantive difference between the definitions of respondents and complainant.

B. The claimed phrase "circuit component"

This claimed phrase is in asserted claims 9 and 10.

Complainant argued that there is no longer a dispute as to the claimed phrase in issue; that respondents did not present any construction for it at the hearing beyond plain and ordinary meaning; and that complainant has no objection to staff's construction, which is "circuit element that provides an impedance for termination." (CBr at 19-20.)

Respondents argued that all parties agree that the proper construction for the claimed phrase is "a circuit element that provides impedance for termination." (RBr at 54.)

The staff argued that said claimed phrase should be construed as "circuit element that provides an impedance for termination." (SBr at 9.)

The parties assert that the term "circuit component" should be understood to mean "circuit element that provides impedance for termination." (RFF 159 (undisputed).) Claim 9 reads in relevant part:

> to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus.

(JX-1 at 10:47-52 (emphasis added).) Thus, the circuit component must reduce signal reflection on the bus. The specification also discloses:

> The termination circuit contains one or more circuit components which when coupled to the data line reduce reflection or change line

> impedance on the bi-directional external bus 17 when data is being received by the device 10. The circuit components may include one or more of a capacitor, a PN junction, a diode, a resistor, a resistive device, an inductor, an N channel transistor, a P channel transistor, a junction field effect transistor (JFET), a metal oxide semiconductor transistor (MOSFET), a bipolar device, a Bi-CMOS device, a current source, a voltage source, any other like termination component, or a circuit comprising one or more of the circuit elements listed above.

(JX-1 at 4:28-40 (emphasis added).) Thus, the specification discloses that a circuit component changes impedance on the bus. Based on the intrinsic evidence cited, supra, the administrative law judge finds that a "circuit component" is an element of a circuit, viz., "an assemblage of electronic elements," as defined, supra, that provides impedance for termination, which finding is consistent with the agreement, supra, of the parties.

C. The claimed phrase "bus termination circuit"

This claimed phrase is in asserted claim 9.

Complainant argued that "bus termination circuit" should be construed to mean "circuitry for signal termination that is selectively enabled or disabled in response to a control signal whose assertion is based, at least in part, on the direction of data signals on the bus." (CBr at 10.) Complainant further argued that its construction is supported by the intrinsic evidence, including the summary of the invention, the rest of the specification, and even the title of the patent. (CBr at 10.) Complainant further argued that each embodiment disclosed in the '455 patent includes the direction of data in the determination of enabling the termination circuitry. (CBr at 11.)

Respondents argued that this claim phrase should be construed as "circuitry for signal termination that is selectively enabled or disabled in response to a control signal." (RBr at 58.) Respondents further argued that the language of claim 9 shows that a bus termination circuit can

be operated by use of a single control signal (RBr at 59); that the use of directional control signals is only an embodiment of the '455 patent, not the invention; and that the termination circuits described in the '455 patent are not limited to circuits that must be enabled or disabled based on data directionality. (RBr at 60-61.)

The staff argued that "bus termination circuit" means "circuitry for signal termination that is selectively enabled or disabled in response to [a] control signal whose assertion is based, at least in part, on the direction of data signals on the bus." (SBr at 9.)

The language of asserted claim 9 reads in relevant part:

> a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one bus termination circuit, the plurality of bus termination circuits providing data to or receiving data from the execution unit, each bus termination circuit in the plurality of bus termination circuits having an input for receiving a control signal; and
>
> a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus.

(JX-1 at 10: 33-52 (emphasis added).) Thus, pursuant to the language of the claim, each bus termination circuit has an input for receiving a control signal, which control signal determines if the bus termination circuit couples or decouples "at least one circuit component." Further, the parties agree that a bus termination circuit is, at least, "circuitry for signal termination that is selectively enabled or disabled in response to a control signal..." See, supra. Respondents

disagreed, however, that the assertion of said control signal is "based, at least in part, on the direction of data signals on the bus", as contended by complainant and the staff. (RBr at 60.)

The plain language of the claim does not directly require that the control signal be asserted based on the direction of data signals on the bus; i.e., whether the bus termination circuits are "providing data to or receiving data from" the execution unit. Asserted claim 9, however, does require that when the control signal is asserted, the bus termination circuit "couple at least one circuit component to the bus to reduce signal reflection on the bus..." and when the control signal is deasserted, that the bus termination circuit "decouple at least one circuit component from the bus."

With reference to the specification, the Summary of the Invention states that:

> The previously mentioned disadvantages are overcome and other advantages achieved with the present invention. In one form, the present invention comprises a method for determining whether to enable termination circuitry within a data processor. A bus transfer begins through a bus coupled between the data processor and a device external to the data processor. A determination is made as to whether the data processor is receiving data or sending data external to the processor. The termination circuitry is enabled if the data processor is receiving data from the bus in order to reduce signal reflection on the bus. The termination circuitry is disabled if the data processor is sending data through the bus.

(JX-1 at 1:44-57 (emphasis added).) Thus, signal reflection is only a problem when receiving data from the bus. Moreover, in describing the preferred embodiment, the '455 patent reads:

> In general, the apparatus and method illustrated herein is designed to dynamically enable the proper termination inside a receiver at the end of the bi-directional bus. The proper termination is dynamically connected to the bus only when data is being received in order to reduce signal reflection on the bus (i.e. transmission line effects) and allow for a more rapid operational speed. This dynamic bus termination requires a control signal which indicates to the receiving device the current drive direction

> of the bus (i.e., is data being read from the device or is data being written to the device). When this control signal indicates the bus has a voltage and/or current which is being driven into the receiving device, the receiving device turns on its termination devices to dampen the incoming signal so no reflections are sent back down the bus (transmission line). When the control signal indicates the bus is not being driven into the receiving device the receiving device's terminators are turned off to reduce the load on the bus and power dissipation of the bus.
>
> * * *
>
> Specifically, the apparatus and method illustrated herein provides the ability to dynamically terminate a bi-directional bus depending on the current bus drive direction.

(JX-1 at 2:53 - 3:4, 3:44-46 (emphasis added).) Thus, as seen in the preferred embodiment, termination circuitry is enabled if the data processor is receiving data from the bus in order to reduce signal reflection. Moreover, the purpose of the invention as stated in the Field of the Invention section of the '455 patent is that the "present invention relates generally to data processors, and more particularly, to dynamic termination of conductive bus lines to avoid signal reflection." (JX-1 at 1:6-8 (Field of the Invention).) Therefore, based on the language of asserted claim 9 and the specification, the administrative law judge finds that "signal reduction" is a requirement of asserted claim 9, and signal reduction only occurs when data is being received by the execution unit. Hence, the administrative law judge finds that a "bus termination circuit" is circuitry for signal termination that is selectively enabled or disabled in response to a control signal whose assertion is based, at least in part, on the direction of data signals on the bus.

Respondents argued that the second paragraph of the Summary of the Invention shows that "another form" of the invention exists that does not require the control signal be asserted based on the direction the data is flowing, and further rely on Fig. 8 and related text as showing an

embodiment that likewise does not have that requirement. (RBr at 60-61, RRBr at 27-28.) Said second paragraph, however, restates the invention as an apparatus, as opposed to the first paragraph of the summary, which describes a method. Moreover, regarding Fig. 8 and the related text in the specification, Fig. 8 relates back to Fig. 5 and the "present invention." (See JX-1 at 2: 38-41 ("FIG. 8 illustrates, in a block diagram, yet another inter-connection of the plurality of independently-enabled bus termination circuits of FIG. 5 in accordance with the present invention.").) Fig. 5 asserts or deasserts bus termination based on a control signal as does Fig. 1 in accordance with the present invention, which is consistently described as being asserted based on the direction the data is flowing. Also, as the administrative law judge has found, supra, the language of asserted claim 9 requires that a bus termination circuit "couple at least one circuit component to the bus to reduce signal reflection on the bus..." and that said signal reflection only occurs when data is being received.

D. The claimed phrase "execution unit"

This claimed phrase is in asserted claim 9.

Complainant argued that this term should be construed in accordance "with the meaning used in the specification, which is 'a portion of an integrated circuit at least partially software driven by microcode and/or nanocode.'" (CBr at 9.) Complainant further argued that "execution unit" did not have a commonly used meaning at the time of the '455 invention, and no other explanation in the specification exists. (CBr at 9; see also CPFF 133.)

Respondents argued that an "execution unit" is "a portion of an integrated circuit that executes commands and instructions." (RBr at 54.) Respondents further argued that the specification lists an execution unit as one of several possible integrated circuits, and thus that

complainant is attempting to read a limitation from the specification into the claim (RBr at 55) and that a person of ordinary skill in the art at the time the asserted '455 patent was filed would have understood "execution unit" to be a portion of a processor that executed computer instructions. (RBr at 56.)

The staff argued that an "execution unit" should be "a portion of an integrated circuit that executes commands or instructions." (SBr at 9.) The staff further argued that there is no support in the intrinsic record for mandating "at least partially software driven by microcode and/or nanocode" as argued by complainant. (SBr at 9.)

The claimed phrase, "execution unit" as found in asserted claim 9 is merely described as follows:

> "an execution unit internal to the data processor ... the plurality of bus termination circuits providing data to or receiving data from the execution unit...

(JX-1 at 10:28, 10:37-39.)[5] Thus, all that can be determined from the claim language is that the execution unit is contained by the data processor, and can send and receive data.

In the specification, the paragraph which mentions an execution unit reads:

> The invention can be further understood with reference to the FIGS. 1-7. FIG. 1 illustrates a data processing system. The data processing system has a device 10 and a device 12 (referred to also as communication devices since they communicate to one another). Generally, device 10 and device 12 are each integrated circuits. For example, either device 10 or device 12 may be a memory device (such as a SRAM, a DRAM, a EEPROM device, an EPROM device, a flash device, and the like), an interface device, any peripheral device, a DMA device, a communication device, a timer, analog circuitry, a microprocessor, a pipelined execution device, an application specific integrated circuit

[5] The claimed phrase "execution unit" also appears in non-asserted claim 14 of the '455 patent, using substantially the same language as asserted claim 9. (JX-1 at 11:13, 11:19-21.)

> (ASIC) device, a programmable logic array (PLA), hard-wired logic, an execution unit at least partially software driven by microcode and/or nanocode, a plurality of execution devices, a digital signal processor (DSP), a computer, a data processor, a central processing unit (CPU), and integrated circuit, and/or the like.

(JX-1 at 3:64-11:14 (emphasis added).) Thus, an execution unit is listed as an example of an integrated circuit, and could be used as either device 10 or device 12 in Fig. 1. Device 10 is later described "[t]he enable signal, in general, is in one logic state if a data is incoming to the device 10 and is deasserted when data is being sent out from the device 10." (JX-1 at 4:44-45.) Hence, an execution unit is further seen to be a device that can send and receive data. Moreover, the parties agree that an "execution unit" is a portion of an integrated circuit. (See, supra.) The administrative law judge finds nothing in the specification that defines an execution unit, except to the extent that it is capable of performing certain functions.

Based on the foregoing, the administrative law judge finds that an "execution unit" is "a portion of an integrated circuit that executes commands or instructions."

E. The claimed phrase "the plurality of bus termination circuits providing data to or receiving data from the execution unit..."

This claimed phrase is in asserted claim 9.

Complainant argued that the language "providing data to or receiving data from..." in the claimed phrase in issue should be accorded its plain and ordinary meaning. (CBr at 24.) Complainant further argued that respondents' requirement of active participation of the bus termination circuit is not warranted; that the word "providing" is used in the specification in ways that do not support respondents' construction; and that there is no support for respondents' assertion that claim 9 is described solely by Fig. 8. (CBr at 24-26.) With respect to the word

"or," complainant argued that, when reading the entirety of claim 9, it is clear that because the claim requires bi-directional communication, the bus termination circuits must be able to both provide and receive data. (CRBr at 55.)

Respondents argued that the word "providing" should be accorded its plain meaning of "to pass" or "to supply" and that complainant agreed. (RBr at 65.) Further, respondents argued that "providing" must also require that a bus termination circuit actively participate in the exchange of data to and from the "execution unit"(RBr at 68) and that the specification in describing Fig. 8 shows that "the drafter of the specification correctly uses the verb 'provide' in connection with the 'assertion' of an enable signal, an active step..." (RBr at 66-67.) With respect to the word "or," respondents argued that although the parties all agreed that or should be given its plain and ordinary, complainant asserted at the hearing that "or" is the same as "and," and respondents further argued that the Federal Circuit has rejected such an interpretation and that complainant has demonstrated no valid reason to depart from using "or" in the disjunctive. (RBr at 68-69.)

The staff argued that nothing in the intrinsic record mandates the "narrow construction proposed by Mr. McAlexander and Respondents to require 'active' participation by the termination circuits" and therefore that this claim phrase should be accorded its ordinary meaning. (SBr at 11.)

The parties all agree that the plain and ordinary meaning of "providing" includes "supplying" and that the plain and ordinary meaning of "receiving" includes "taking" or "getting." (CBr at 24; RBr at 65; RRBr at 41, n. 25; SBr at 11.) Asserted claim 9 reads in relevant part:

> an execution unit internal to the data processor;

> a plurality of external pins connected to the integrated circuit package, the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus;
>
> a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one bus termination circuit, the plurality of bus termination circuits providing data to or receiving data from the execution unit, each bus termination circuit in the plurality of bus termination circuits having an input for receiving a control signal;

(JX-1 at 28-41 (emphasis added).) Thus, a bus termination circuit is connected to an external pin and the execution unit. As the language of the claims indicates, the bus termination circuit either provides (or supplies) data to, or receives (or takes or gets) data from the execution unit. Since the bus termination circuit is connected to an external pin and the execution unit, which execution unit is internal to the data processor, and the language of asserted claim 9 states "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor...," the administrative law judge finds that it is a requirement of the claim that the bus termination unit can both provide and receive data; not do only one or the other. With respect to "providing," nothing in the claim language indicates the manner that said data is provided.

With respect to the specification, although the words "provide," "provides," and "providing" are used therein, the administrative law judge has found no use of those words relating to the bus termination circuit's communication with an execution unit or the data processor. Thus, Figs. 1, 2, and 5 are block diagrams that show data entering and leaving the "dynamic bus termination circuit 14." (See, inter alia, JX-1 at 4:15-20 (describing Fig. 1); JX-1 at 7:9-11 (stating that elements of Fig. 1 which are analogous to elements in Fig 5 are identically labeled).) It is noted that in Figs. 1 and 5, in device 10, there is a "bi-directional bus 13,"

represented by a double-headed arrow, connectng "dynamic bus termination circuit 14" to the "bi-directional bus" 17 and a double-headed arrow labeled "DATA" connecting dynamic bus termination circuit 14 to a "data unit" 18. In Fig. 2, bi-directional bus 17 is connected to a double-headed arrow which is drawn through bus termination circuit 14. Therefore, the administrative law judge finds that the specification supports and further explains the limitation in asserted claim 9 requiring that the bus termination circuit be capable of either providing or receiving data. With the exception of what occurs when the bus termination circuit must reduce signal reflection, neither the claims nor the specification put any further restriction on what the bus termination circuit must do when it provides or receives data to or from the execution unit. Hence, the administrative law judge accords the claimed phrase "providing data to or receiving data from" its plain meaning, i.e. "the plurality of bus termination circuits supplying data to or getting data from the execution unit," as defined herein.[6]

Respondents argued that the claim term "providing" should be accorded its plain meaning. (RBr at 68.) Respondents further argued that, to the extent it requires interpretation, it "means a bus termination circuit that actively participates in the exchange of data to and from the 'execution unit'" (RBr at 68), which is inconsistent with the argument that the term would be understood by a person of ordinary skill in the art to have its plain meaning. (Compare RBr at 65 (""providing' should be construed according to its plain and ordinary meaning..." with RBr at 66 ("the drafter of the specification correctly uses the verb 'provide' in connection with the 'assertion' of an enable signal..."); also compare RBr at 65 ("The term 'providing' is not a highly

[6] The claimed phrases "bus termination circuit" and "execution unit," referred to here, are separately construed

technical term. Rather, it is a prosaic term.") with RBr at 65 ("Most significant here is that the term 'providing' is used in connection with the description of a second embodiment...").)

Referring to respondents' argument that the claimed phrase "providing" requires active participation in the exchange of data, the bus termination circuit is required to both provide and receive data, as found, supra. In a separate limitation, the bus termination circuit as recited in claim 9 of the '455 patent is required to perform signal reduction. (See Section C, supra, (finding that a bus termination circuit performs signal reduction when data is being received by the execution unit).) Thus, claim 9 requires the bus termination circuit to perform some action when receiving data, but requires no action when "providing" data in a prior limitation. The administrative law judge finds nothing in the claim language which associates "providing" with any activity. Respondents make further reference to the specification at, inter alia, JX-1 at 1:66-2:2 ("The circuitry for terminating has a second input/output terminal for providing or receiving data from internal to the communication device.") and argued that the cited portion of the specification "clearly describes a structure, the 'second input/output terminal' that must perform an act, i.e., 'provid[e] or receiv[e] data from internal to the communication device." However, the cited portion of the specification does not relate to the claimed phrase at issue. Further, the administrative law judge has found nothing in the specification, including the citation by respondents, supra, that supports the argument that the plain meaning of the word "providing" requires "active participation."

F. The claimed phrase "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus"

This claimed phrase is in asserted claim 9.

Complainant argued that the parties agreed that this claimed phrase should be accorded its plain and ordinary meaning, but that the parties disagreed as to what that meaning is; that respondents' interpretation that external bus must be between the plurality of external pins and the data processor which is internal to the integrated circuit is not supported by the plain language of the claims; that the logic bits must travel to and from the data processor "via an external bus," consistent with common sense and the specification; that respondents' interpretation is admittedly nonsensical and thus can only be correct if the claim is "susceptible to only one reasonable interpretation" (emphasis in original) but that the grammar here does not require that result; and respondents' interpretation is unsupported in the specification. (CBr at 20-24.) Complainant further argued that if this claimed phrase needs to be construed, it should be "the plurality of external pins used to bidirectionally communicate logic bits traveling to and from the data processor via an external bus." (CBr at 20.)

Respondents argued that the parties agree that the word "via" should be construed according to its plain meaning of "by way of" or "through"; that the claimed phrase in issue is unambiguous and therefore the specification need not be consulted with respect to its interpretation; that basic grammar "requires that the logic bits travel from the external pins, through the external bus, and then onto the data processor (and vice versa)." (RBr at 61.) Respondents further argued that complainant's construction parses and shifts clauses "in a manner inconsistent with the unambiguous language of the limitation as written. (RBr at 62.)

The staff argued that this claimed phrase should be construed as "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor, the logic bits traveling to and from the data processor via an external bus." (SBr at 10.)

Although the private parties both depend on "plain and ordinary meaning," their interpretation differs. Thus, there is a dispute between the parties. The preamble of the asserted claim reads: "A data processor within an integrated circuit package comprising...," meaning that the data processor is within an integrated circuit. The full language of the limitation containing the claimed phrase at issue reads:

> a plurality of external pins connected to the integrated circuit package, the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus...

(JX-1 at 10:30-34.) Thus, pursuant to said language, the "external pins" are a part of the data processor and are connected to the integrated circuit package. Said language also discloses that said external pins are used to communicate logic bits "to and from the data processor." What the data processor is communicating with, precisely, is not specified, except that it must be within the integrated circuit package. The claimed phrase at issue also indicates that communication with the integrated circuit package is "via an external bus." The parties agreed that an understanding of "via" as "by way of" or "through" is consistent with the specification of the '455 patent. (RFF 186 (undisputed).)

With respect to the specification, the Summary of the Invention reads in relevant part:

> A bus transfer begins <u>through a bus coupled between the data processor and a device external to the data processor</u>. A determination is made as to whether the data processor is receiving data or sending data external to the processor. The termination circuitry is enabled if the data processor is receiving data from the bus in order to reduce signal reflection on the bus. The termination circuitry is disabled if the data processor is sending data through the bus.

(JX-1 at 1:49-57 (emphasis added).) Thus, the bus is described as being the means of communication between the data processor and an external device. Fig. 1 and the related text in

the specification describe a dynamic bus termination circuit 14 attached to an external integrated circuit data pin, which is in turn attached to an external bus 17. (See, inter alia, JX-1 at Fig. 1; JX-1 at 4:15-17 ("The device 10 has a dynamic bus termination circuit 14 connected via at least one conductor or a bi-directional bus 13 to one or more external integrated circuit data pins."); JX-1 at 4:28-31 ("The termination circuit contains one or more circuit components which when coupled to the data line reduce reflection or change line impedance on the bi-directional external bus 17 when data is being received by the device 10.").) Based on the foregoing intrinsic evidence including the specification, the administrative law judge finds that the claimed phrase in issue should be construed as "a plurality of external pins used to bidirectionally communicate logic bits from the data processor, the logic bits traveling to and from the data processor via an external bus."

Respondents have argued that the claim language is unambiguous and therefore the specification is "irrelevant to the understanding of the claim term." (RRBr at 39 (emphasis in original); see also RBr at 63.) For support, respondents cite Chef America, Inc. v. Lamb-Weston, Inc., 358 F.3d 1371, 1374 (Fed. Cir. 2004) ("where as here, the claim is susceptible to only one reasonable interpretation, the canons of claim construction [] are inapposite, and we must construe the claims based on the patentee's version of the claim as he himself drafted it.") (Chef America). In Chef America, the claim language at issue was "heating the resulting batter-coated dough to a temperature in the range of about 400 degrees F. to 850 degrees F." The central dispute was over whether or not the word "to" could be read as "at," despite the fact that there was no special definition in the specification of "to." The Court found that the patentee had specifically chosen the word "to" during prosecution. Id. at 1374. Also, in that case, Chef

America's baking expert could not explain why a person of ordinary skill in the art would read "to" as "at," but depended on the fact that it was well known that if the dough itself was heated to that temperature, instead of at that temperature (i.e., in an oven heated to that temperature) an unusable product would result. Chef America at 1375. In summary, it was a single word at issue, which word was specifically chosen by the patentee with no special meaning defined in the specification. In contrast, in this investigation, where the private parties purport to depend on the plain and ordinary meaning (instead of a changed meaning), the meaning of specific words is not at issue as it was in Chef America, and there is a dispute as to how the claim phrase taken as a whole is interpreted. (RBr at 61-62; CBr at 20-21; SBr at 10-11.)

G. The claimed phrases "couple" and "decouple"

The claimed phrases are in asserted claim 9.

Complainant argued that the parties agree that "couple" and "decouple" should be construed as "to electrically connect to" (CPFF 127 (undisputed)) and "electronically disconnect from" (or "not electrically connect[ed] to") (CPFF 128 (undisputed); CBr at 27.) Complainant further argued that the way that respondents apply that construction is unsupported and illogical. (CBr at 27-32.)

Respondents argued that the parties agreed that "couple" means"electrically connected to" and "decouple" means "not electrically connected to." (RBr at 70.) Respondents further argued that complainant is now arguing for a new construction of decouple meaning "complete[] an electrical circuit to reduce signal reflection on the bus..." (RRBr at 50); that such an interpretation imports a limitation from the specification into the claim (RRBr at 51); and that there is no support in the specification for complainant's "new" construction (RRBr at 51-52).

The staff argued that "couple" and "decouple" mean, respectively, "to electrically connect [to]" and "to electrically disconnect [from]." (SBr at 11-12.)

The claimed phrase "couple" or "coupled"occurs within two elements of asserted claim 9, while the claimed phrase "decouple" occurs once in the last element of asserted claim 9. Specifically, a bus termination circuit "coupled" to an external pin (JX-1 at 10:35-37); a conductor coupled to "each input of each of the bus termination circuits." (JX-1 at 10:42-44) and a circuit component coupled to the bus (JX-1 at 10:47-48), and then decoupled from the bus. (JX-1 at 10:51-52.) Thus, some connection allowing communication is apparent.

As per the Summary of the Invention:

> A bus transfer begins through a bus coupled between the data processor and a device external to the data processor.
>
> * * *
>
> the invention comprises a data processing system having a communication device having at least one external pin connected external to the communication device. The at least one external pin is coupled to receive data from external to the communication device and transmit data external to the communication device. The communication device has circuitry for terminating. The circuitry for terminating has a first input/output terminal coupled to the at least one external pin via at least one data line. The circuitry for terminating has a second input/output terminal for providing or receiving data from internal to the communication device. The circuitry for terminating has an input for receiving an enable signal and has one or more termination component(s). The enable signal couples the termination component to the at least one termination pin when the enable signal is asserted, and decouples the termination component from the at least one termination pin when the enable signal is deasserted.

(JX-1 at 1:49-51, 1:58-2:8 (emphasis added).) Based on the foregoing, "couple" means that there must be a sufficient connection for communication to occur. The specification also discloses:

> The termination circuit contains one or more circuit components which when coupled to the data line reduce reflection or change line impedance on the bi-directional external bus 17 when data is being received by the device 10.

(JX-1 at 4:28-31 (emphasis added).) Thus it is seen that when coupled to the external bus, the circuit components are expected to have a definitive affect on the external bus.

Later, the specification reads:

> A circuit component 104, used to dynamically reduce signal reflection, has a first terminal connected to the emitter of transistor 102 and a second terminal connected/coupled to the bus 17 (output buffers, input buffers, and input/output (I/O) buffers, as needed, are not specifically illustrated in FIGS. 1-2). The transistor 108 has an emitter connected to a ground potential, a collector, and a base connected to the enable signal. A component 106, similar to component 104, has a first terminal connected/coupled to the bus 17 and a second terminal connected to the collector of transistor 108.

(JX-1 at 6:2-12 (emphasis added).) Thus, the specification uses the word "coupled" as synonymous with "connected."

Based on the foregoing, the administrative law judge accepts the party's agreed-to language; i.e., that "couple" means "electrically connect to" and "decouple" means "electrically disconnect from."[7]

In their briefs, the private parties have made several arguments related to the particular use of the claimed phrases "couple" and "decouple" with respect to the "at least one circuit component." (CBr at 27-32; RRBr at 49-57.) Thus, the parties appear to be attempting to interpret the entire claim limitation rather than just the claimed phrases "couple" and "decouple."

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[7] Whether an accused product practices the claimed element; i.e., actually couples and decouples a circuit component as per the claim construction herein, is a question of infringement, not claim construction.

Specifically, complainant argued that decoupling is the opposite of coupling; that the claim limitation expressly requires that "electrically connecting the termination circuitry completes an electric circuit 'to reduce signal reflection on the bus...'"; and that electrically disconnecting must break the electrical circuit. (CBr at 28-29.) Respondents argued that complainant is importing a limitation that "coupled" must mean "complete[] an electrical circuit to reduce signal reflection on the bus..."; and that complainant has pointed to nowhere in the specification that justifies its reading "that when the circuit component in Figure 2 is 'floating' (a term which is mentioned nowhere in the '455 patent but one that used often by Dr. Subramanian in the hearing... the component is somehow 'decoupled'..."(RRBr at 52.) The staff argued that the private parties "have different understandings of what it means to be electrically connected to and disconnected from..."; however, it supported the agreed-upon construction. (SBr at 11-12.)

The claim element at issue reads:

> a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus.

(JX-1 at 10:42-52.) Thus, said claim element, supra, taken as a whole, requires that the "at least one circuit component" be coupled to the bus "to reduce signal reflection on the bus" when a control signal is asserted, and said circuit component must be decoupled when said control signal is deasserted. Thus, the circuit component must be electrically disconnected from the bus, such that it, inter alia, can no longer reduce signal reflection on the bus. The administrative law judge

finds that this reading is supported in multiple sections of the specification. (See, inter alia, JX-1 at 1:53-55 ("The termination circuitry is enabled if the data processor is receiving data from the bus in order to reduce signal reflection on the bus."); JX-2 at 2:4-8 ("The enable signal couples the termination component to the at least one termination pin when the enable signal is asserted, and decouples the termination component from the at least one termination pin when the enable signal is deasserted."); JX-2 at 2:63-3:4; 5:5-20; 6: 20-22, 40-45; 7:21-26.)

VIII. Zoran Datasheets And Schematics

At the evidentiary hearing on February 8, 2011, complainant requested admission of certain third party Zoran Corporation (Zoran)[8] documents including datasheets CX-1411C, CX-1412C, CX-1413C, and CX-1414C and schematics CX-1417C. The respondents objected to the admissibility of said documents. (See Tr. at 603-6.) In arguing for the admissibility of said documents, counsel for complainant indicated that complainant would not be able to prove infringement by a preponderance of the evidence if said documents were not admitted:

> JUDGE LUCKERN: Let me ask you this question: I haven't decided what I'm going to do, I don't know what I'm going to do, but if I kept them out and struck them and all the testimony that goes along with it, would you still believe that you could show infringement by a preponderance of the evidence?
>
> MR. HOFFMAN: No, Your Honor, we would not be able to.

(Tr. at 601.) Said exhibits are said datasheets CX-1411C, CX-1412C, CX-1413C, and CX-1414C and schematics CX-1417C, which complainant asserted show the relevant functionality of accused products. The administrative law judge overruled respondents' objection, admitted said exhibits, and encouraged the parties to present arguments in the post-hearing briefs, findings of

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[8] Zoran is a third-party that provides certain integrated circuit chips to Funai, and said integrated circuit chips are incorporated into the accused Funai products. (See CBr at 38.)

fact, and rebuttal findings of fact regarding the weight, if any, the administrative law judge should give to said exhibits in making a determination on infringement.[9] (See Tr. at 626-7.)

Complainant argued that the schematics in CX-1417C represent the accused products because said schematics were provided by Zoran with the { } in response to a subpoena. (CBr at 38-9.) Complainant further argued that "the undisputed facts establish a prima facie case and a presumption that the Zoran documents are authentic and reliable evidence upon which the Chief Judge should properly rely." (CBr at 44.) Complainant also argued that respondents' arguments "are predicated on Zoran failing to comply with the subpoena in its production" and respondents have not set forth "any affirmative facts to rebut the presumption that is supported by the undisputed facts." (CBr at 48, 53.)

Respondents Funai have argued that the administrative law judge should give no weight to the third-party Zoran documents complainant Freescale relies upon in its infringement case. (RBr at 16.) Funai contended that the Zoran documents were not properly authenticated or shown to be reliable and representative of the circuits used in Funai products. (RBr at 17.) Specifically, Funai noted that complainant Freescale's expert Subramanian did not examine actual Zoran circuits or Funai products. They further contended that their expert "McAlexander testified, and Dr. Subramanian acknowledged, that there is nothing in or about the Zoran documents that indicates that they are final documents or correspond to specific manufactured products, let alone

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[9] With respect to the administrative law judge's findings on infringement in Section IX infra, the administrative law judge in Section IX has found that based on the statement of complainant's counsel and a review of said Zoran documents as found in Section VIII, complainant has failed to prove infringement by a preponderance of the evidence because all of said Zoran datasheets CX-1411C, CX-1412C, CX-1413C, and CX-1414C are found unreliable as evidence of the composition of the accused products and because said Zoran schematics CX-1417C are also found unreliable as evidence of the composition of the accused products.

the accused integrated circuits in the Respondents' products." (RBr at 16-7.) Funai also noted that the administrative law judge granted a request by complainant Freescale to extend the discovery deadline with respect to obtaining additional discovery from Zoran, but Freescale did not depose Zoran, seek an affidavit from Zoran regarding Zoran documents, or move to have the Zoran subpoena enforced. (RBr at 17-8.) Funai further argued that Freescale cannot rely on the fact that the documents in issue were produced in response to a subpoena to establish that the documents are reliable because "the documents bear indicia of unreliability." (RBr at 29-31.)

The staff argued that the documents at issue are reliable and the testimony regarding the documents should be given full weight because the documents "were produced by Zoran in response to a subpoena issued by the Chief Judge; the subpoena asked for schematics for parts used in the accused Funai products; and the schematics were produced by Zoran with the

{

} (SBr at 17.) The staff also argued that respondents' assertions regarding the documents in issue should be rejected because their argument is legally unsupported and relies on speculation and attorney argument. (SBr at 17; SRBr at 3.)

Complainant bears the burden of proving infringement by a preponderance of the evidence, and with that burden complainant bears the burden of proving the composition of the accused products. Ultra-Tex Surfaces, Inc. v. Hill Brothers Chemical Co., 204 F.3d 1360, 1364 (Fed. Cir. 2000). Complainant must provide sufficient evidence to show infringement before the burden shifts to the accused infringer to offer contrary evidence. See L&W, Inc. v. Shertech, Inc., 471 F.3d 1311, 1318 (Fed. Cir. 2006). However, said evidence must show infringement for each accused device and the complainant cannot rely on an assumption that all of the accused products include similar structure to shift the burden to the accused infringer. See Id.

Further, Commission precedent indicates that admitted evidence may be given no weight in making a final initial determination on infringement where said admitted evidence is unreliable or insufficient to show the composition of the accused products. See Certain Sucralose, Sweeteners Containing Sucralose, And Related Intermediate Compounds Thereof, Inv. No. 337-TA-604, Commission Opinion at 90-93 (April 28, 2009) (affirming non-infringement determination of the administrative law judge based in part on unreliability of admitted evidence) (Sucralose); Certain Nor And Nand Flash Memory Devices And Products Containing Same, Inv. No. 337-TA-560, Initial Determination at 40-46 (June 1, 2007) (Non-review by Commission on July 13, 2007) (finding admitted evidence unreliable and giving said evidence and testimony related to said evidence no weight). In Sucralose, complainant relied on its employee's testimony regarding third party test results to prove infringement by a defaulting party. However, the administrative law judge found said testimony insufficient and unreliable to prove infringement because "no one who conducted the tests was called to testify regarding the methodology used or the reliability of the results," and the Commission affirmed. Sucralose, Comm. Op. at 90-3.

It is undisputed that all the Zoran documents in issue were produced by Zoran in response to a subpoena propounded by complainant and requesting documents related to Zoran part numbers disclosed by Funai as being incorporated into Funai accused products. (CPFF 481-484 (undisputed).) Regarding the Zoran datasheets, the titles of the datasheets include the text { }(CX-1411C; CX-1412C; CX-1413C; CX-1413C.) Each of those SupraHD identifiers relates to Zoran chips which Funai has admitted are in the accused products. (See CX-1411C at Zoran 000376; CPFF 483 (undisputed); CPFF 484 (undisputed).) Further, complainant's expert Subramanian testified

regarding the link between the datasheets and the Zoran chips in the accused products:

{

}

(Tr. at 193-194 (emphasis added).)

The administrative law judge finds that there is a link between the datasheet exhibits, viz. CX-1411C, CX-1412C, CX-1413C, and CX-1414C, and the Zoran chips present in the accused products because the datasheets consistently correlate "SupraHD" parts to Zoran part numbers present in the accused products. (See CX-1411C at Zoran 000376; CX-1412C at Zoran 000542; CX-1413C at Zoran 000677; CX-1414C at Zoran 000873; CPFF 483 (undisputed); CPFF 484 (undisputed).) For example, {

}

(CX-1414C at Zoran 000873.) Similarly, CX-1411C includes the list:

{

}

(CX-1411C at Zoran 000376.)

However, despite said link, each of said datasheets has the language on the first page,

{

} (CX-

1411C, CX-1412C, CX-1413C, CX-1414C.) Regarding said text on the datasheets,

complainant's expert Subramanian testified:

{

}

(Tr. at 542-543 (emphasis added).) Thus, Subramanian testified that {

} but concluded that they represented what is included in the accused products

because the datasheets were produced in response to a subpoena. Further, the title pages of these datasheets include the dates{

} (CX-1414C). Regarding the dates on said datasheets, Subramanian testified:

{

}

{

}

(Tr. at 538-545 (emphasis added).) Thus, the administrative law judge finds that Subramanian admitted that "more recent ones ... were not provided in response to the subpoena" and relied upon the fact that said datasheets were produced pursuant to a subpoena to indicate that said datasheets were final documents that accurately reflected the composition of the accused products. Based on the foregoing, the administrative law judge finds that the sponsoring witness for said datasheets, viz. Subramanian, could provide no details regarding how the datasheets were created or the origin of certain information contained therein and relied primarily on the fact that said datasheets were produced pursuant to a subpoena in concluding that the technical

information contained therein accurately represented the composition of the accused products. He further finds that Subramanian has based his conclusions regarding the reliability of the datasheets on the legal conclusion that because the datasheets were produced in response to a subpoena they are presumed reliable. However, Subramanian, who is not an attorney, testified only as an expert in the field of "electrical engineering and integrated circuits." (Tr. at 121.)

Further, complainant's expert Subramanian, as seen from his following testimony, testified that his infringement analysis as it relates to CX-1411C, CX-1412C, CX-1413C, and CX-1414C is the same for each of these documents, which indicates that the relevant parts of these documents did not significantly change from {

}

(Tr. at 211-215 (emphasis added).) In addition, the administrative law judge finds the datasheet pages relied upon by Subramanian in his infringement analysis contain {

}

However, Subramanian, as found supra, could not provide any details regarding the origin of the information contained in said datasheets and based his conclusion that the technical information contained therein was the final information representing the contents of the actual Zoran integrated circuits in the accused products solely on the fact that said datasheets were produced in response to a subpoena. Further, the administrative law judge finds that complainant produced no other evidence beyond the testimony of Subramanian to establish the finality and reliability of said datasheets, and he further finds that the record does not contain any corroborating evidence to establish their finality other than certain consistencies among said datasheets, which only indicates that certain information in said datasheets may be final. Significantly, he finds complainant, who has the burden to establish infringement, presented nothing from Zoran, from which said datasheets originated, explaining the defects, supra, in said datasheets CX-1411C, CX-1412C, CX-1413C, and CX-1414C.[10] Thus, he finds that said datasheets are unreliable as evidence of the contents of the accused products. Accordingly, said datasheets and testimony regarding the technical information contained in said datasheets will not be given any weight in making a final determination on infringement.

Regarding the Zoran schematics CX-1417C, like said datasheets, it is undisputed that said

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[10] It is a fact that complainant did not depose Zoran. However, it is also a fact that the administrative law judge issued a subpoena ad testificandum and duces tecum to Zoran Corporation as early as July 9, 2010, nearly six months before the beginning of the evidentiary hearing. (EDIS Docket Document ID No. 444564.) Further, in Order No. 19, the administrative law judge extended the fact discovery deadline to October 8, 2010 to allow, inter alia, complainant to complete discovery with respect to Zoran "including concluding document production and providing a witness to testify." (Order at 1.) Said extension of discovery occurred approximately four months before the beginning of the evidentiary hearing.

schematics were produced pursuant to a subpoena. (CPFF 481-484 (undisputed).) It is also undisputed that the first page of the exhibit containing schematics (CX-1417C) includes the { } (RFF 53 (undisputed in relevant part).) Regarding the relevance {

}

(Tr. at 159 (emphasis added).) Thus, the administrative law judge finds that Subramanian relied on the fact that the schematics were produced pursuant to a subpoena to show that the handwritten notation was accurate and the schematics in the exhibit (CX-1417C) represented the circuitry present in the accused products. Subramanian further testified that without the handwritten notation he would not be able to relate the schematics to any particular Zoran part number:

> Q. And just to be clear, from Judge Luckern's point, without the hand scrawl, without the hand notations, you have no way to associate any wiring or functionality in a schematic to any particular part, correct?
>
> A. To any single part?
>
> Q. Any single part, correct?
>
> A. Yes, I agree. I would only be able to associate it collectively, to the list of parts on the subpoena, but not to any single part.

(Tr. at 424-425 (emphasis added).) Subramanian further testified regarding the handwritten notation:

Q. You just don't know who put that scrawl there?
A. I think I already said that. That's correct.

Q. Do you know why whoever did it, did it? Do you know?

A. I believe so. I believe they put it on there to indicate the family that it's from.

Q. That's your belief. I'm asking you a different question. Do you know why the person who put it there put it there?

A. Beyond my belief, I have no additional basis for saying that.

Q. So you just don't know why that person, you don't know who it is, you don't know why they put it there?

A. I do not know who it is. I have a belief as to why it is there, but beyond that, I have no other basis.

(Tr. at 414-415 (emphasis added).) Thus, the administrative law judge finds that Subramanian testified that he has no personal knowledge regarding who placed the handwritten notation on CX-1417C or why it was place there, and he further finds that Subramanian did not provide any corroborating information regarding the technical content of the schematics. Moreover, beyond the testimony of Subramanian, complainant did not provide any other evidence regarding who wrote the handwritten notation, why it was written, or when it was written.

Further regarding the schematics in CX-1417C labeled {

}

(Tr. at 532-534 (emphasis added).) Thus, the administrative law judge finds with respect to the relevance of the schematics CX-1417C that Subrmanian relied on the fact that said schematics were produced in response to a subpoena while acknowledging {

}

(Tr. at 547-550 (emphasis added).) Thus, the administrative law judge finds that Subramanian,

{

}

Further, Subramanian testified that information regarding {

} Thus, he testified:

> THE WITNESS: I understand, Your Honor. When you design a new circuit, the circuit complexity, in many cases, can get quite large, and as a result, humans make errors.
>
> So commonly, there are both computer based checks, and I'll explain what that means, as well as person based checks, and the person based checks will mean you will sit down with the rest of your design team, and you'll present what you've done, and they will look at it, and they'll give you suggestions, or they might say, well, watch out for this problem or not.
>
> The computer based checks are, they'll run circuit simulations, confirm that the circuits have the behavioral patterns that you expect them to have, and then there'll be some sort of version control database maintained that'll say that this particular version of the design, arbitrarily, version 1.6, has past the checks.
>
> Those version control databases do not, however, have to be in the same database as the schematics.

(Tr. at 546-547 (emphasis added).) However, the administrative law judge finds that neither complainant nor Subramanian have provided any evidence of another database or other corroborating evidence showing that said schematics have been {

}

(Tr. at 551-553 (emphasis added).) The administrative law judge finds that Subramanian again relied on the fact that said schematics were produced pursuant to a subpoena as the only evidence that they represent the circuitry in the accused products despite the {

}

Regarding the { } listed on the pages of CX-1417C, Subramanian testified:

{

}

(Tr. at 536-537 (emphasis added).) Thus regarding dates, Subramanian is "positive" because the schematics were produced in response to a subpoena.

Based on the foregoing, the administrative law judge finds that the contents of the schematics are unreliable insofar as they do not bear any indicia of finality; the record does not

contain any corroborating evidence to establish their finality; and the sponsoring witness could provide no details whatsoever concerning how the document was created or the origin of the technical information contained therein. Accordingly, the administrative law judge finds that said schematics are not reliable evidence of the composition of the accused products and said exhibit along with the testimony regarding said exhibit will not be given any weight in making a final determination on infringement.

Complainant and the staff each argued that the schematics in exhibit CX-1417C are reliable evidence of the circuitry present in the accused products because the schematics were produced in response to a subpoena. (See CBr at 49; SBr at 17.) To support said argument, complainant asserted that the schematics were provided by Zoran through Zoran's counsel and produced as received and the{ } shows the "schematics produced by Zoran correlate precisely to the schematics requested by Complainant in its subpoena." (CBr at 50.) Complainant concluded that "[t]hese facts support a prima facie case that the Zoran schematics are reliable evidence of the Zoran integrated circuits," and "[i]t is more likely that (sic) not that the schematics are exactly what they purport to be: Zoran schematics for the integrated circuit part numbers requested in the subpoena and that are listed on the Zoran schematics themselves." (CBr at 51.) Complainant further concluded that these facts created a "presumption that the Zoran documents are authentic and reliable evidence," and respondents have not identified any facts to rebut this presumption. (CBr at 44.)

Significantly however, neither complainant nor the staff cited to any law establishing that documents produced pursuant to a third-party subpoena are inherently reliable or establish a "prima facie" case that said documents are reliable creating a presumption that must be rebutted by respondents, and the administrative law judge has found no law supporting said arguments.

To the contrary, in U.S. v. Sutton the court stated:

> Next, documents produced by a third party, ... by subpoena or otherwise-regarding which the defendants have had no right to cross-examination, will probably not be received in evidence unless during the trial, an appropriate witness should provide the necessary predicate for the document to be admitted and thereby affording the defendants the right of cross-examination.

795 F.2d 1040, 1056 (Temp. Emer. Ct. App. 1986) (emphasis added). Moreover, complainant has produced no evidence regarding, with reference to the schematics CX-1417C,{ } beyond the fact that said schematics were produced in response to a subpoena, as found supra. Further, as found supra, CX-1417C includes { } suggesting it is not a final version of a schematic and complainant produced no corroborating evidence establishing the finality of said schematics. Significantly, like the datasheets in issue, the administrative law judge finds complainant, who has the burden to establish infringement, presented nothing from Zoran explaining the defects, supra, in said schematics CX-1417C.

IX. Infringement

At issue is whether complainant established, by a preponderance of the evidence, that the accused products infringe claims 9 and 10 of the asserted '455 patent.

Complainant has admitted, as found, supra, in Section VIII, that its infringement contentions rely on, inter alia, CX-1411, CX-1412, CX-1413, CX-1414, and CX-1417, viz. the Zoran datasheets and the Zoran schematics. As found supra, the administrative law judge has not accorded any weight to said Zoran datasheets and schematics or the related testimony. Thus, he finds that complainant has failed to show that the accused products infringe the asserted claims of the '455 patent. However, for the sake of the infringement analysis, the administrative law judge will, in this section, assume, arguendo, that each of the Zoran datasheets, the Zoran

schematics, and related testimony are accorded weight and will make findings as to whether there is infringement under said assumption.[11]

A. Accused Products

Complainant accused certain models of Funai televisions using integrated circuits manufactured by third party Zoran. (CBr at 34.) Specifically, the Zoran integrated circuits, or chips, are in the { } (CBr at 34.) The specific models of Funai televisions that complainant accuses of including chips from Zoran are on the following chart, where the Funai model numbers follow the colon on each bullet point:

{

}

[11] Respondents also have generally objected to complainant not having examined either the commercial end products (particular models of Funai televisions) accused of infringement, nor the specific Zoran IC chips alleged to be the basis for complainant's infringement allegations. (See, inter alia, RRCPFF 719; RRCPFF 720; RRCPFF 723.) The administrative law judge rejects this argument, and finds, despite the lack of reliable documentation in this investigation, that where reliable documentation does exist, said reliable documentation is sufficient to show how products work such that examination of physical products is not necessary to prove infringement. See Monsanto Co. v. David, 516 F.3d 1009, 1015-1016 (Fed. Cir. 2008) ("an expert need not have obtained the basis for his opinion from personal perception").

(CBr at 37.) Complainant argued that, for the purpose of determining infringement of asserted claims 9 and 10, the "analysis and result is the same for each of the Accused Funai Zoran ICs." (CBr at 63.) Because the accused products are goods that include a component that is alleged to infringe the asserted patent, complainant must show that said component infringes and that said component is installed in the accused products.

With respect to whether the alleged infringing components, i.e. the Zoran chips, are installed in the accused products, the respondents do not dispute that the accused products contain Zoran chips with the model numbers:{

} (See CPFF 114; ROCPFF 114A; CX-122C at 9-10.) Thus, the administrative law judge finds that said components, viz. the Zoran chips, are installed in said accused products, viz. the Funai model numbers listed supra.

B. The claim limitation "A data processor within an integrated circuit package comprising..."

Complainant argued that, based on the Zoran hardware datasheets CX-1411C, CX-1412C, CX-1413C, and CX-1414C, that the Zoran chips are integrated circuits. (CBr at 65-67.) Further, complainant argued, with reference to said datasheets, that the accused products contain a Zoran integrated circuit that is a data processor, as it has a CPU and other components that process data. (CBr at 67.)

Respondents presented no substantive counterargument, instead relying on their conclusion that CX-1411C - 1414C are "neither probative nor reliable." (CPFF 712; ROCPFF 712; RRCPFF 712.)

The staff argued that "each and every limitation of claim 9 of the '455 patent as correctly construed is literally present in the Zoran chips incorporated in the accused Funai products." (SBr at 18.)

Each of the Zoran chips at issue in this investigation are described in a datasheet as being { {

} CX-1412C at ZORAN 542; CX-1413C at ZORAN 677; CX-1414C at ZORAN 873.) Complainant's expert testified that "IC" means integrated circuit. (Tr. at 238; see also CPFF 673 (undisputed in relevant part).) Said datasheets show that the Zoran chips are integrated circuits. (CPFF 653, 654, 655 (all undisputed in relevant part).) Further, the datasheets show that the Zoran chips at issue have a data processor within an integrated circuit package. (CPFF 712 (undisputed in relevant part).) Respondents have not substantively rebutted complainant's arguments with respect to the preamble of claim 9 of the '455 patent. In fact, respondents' expert McAlexander testified that said chips do contain a data processor. (ROCPFF 716 (citing Tr. at 1029, 1030-32).) Thus, assuming, arguendo, that said Zoran datasheets CX-1411C, CX-1412C, CX-1413C, and CX-1414C are accorded weight, the administrative law judge finds that the Zoran chips at issue do practice the preamble of claim 9 of the '455 patent; that is, they are integrated circuits that contain a data processor.

C. The claim limitation "an execution unit internal to the data processor..."

Complainant argued that the accused products practice this claim limitation under either party's construction of "execution unit." (CBr at 68.) Specifically, complainant argued that the Zoran chips have an internal CPU; that a {

} (CBr at 68); that the Zoran chips all execute Application software; that since each of the chips runs firmware, they meet this claim limitation; and that

respondents' and staff's constructions are broader than complainant's construction. (CBr at 68-70.)

Respondents argued that the evidence relied on by complainant is insufficient to show that the Zoran chips practice this claim element (RRBr at 65-67; see also, e.g., ROCPFF 719; RRCPFF 719) and that complainant has not shown that any execution unit in the Zoran IC chips is driven by microcode and/or nanocode, as required by complainant's claim construction. (RRBr at 65-68.)

The staff argued that "each and every limitation of claim 9 of the '455 patent as correctly construed is literally present in the Zoran chips incorporated in the accused Funai products." (SBr at 18.)

The administrative law judge has found, supra, that an "execution unit" is "a portion of an integrated circuit that executes commands or instructions." He also has found, supra, that the Zoran chips are integrated circuits and have a data processor. The datasheets show that each of the Zoran chips{ } (CX-1411C at ZORAN 375, 377; CX-1412C at ZORAN 541, 542, 544, 548; CX-1413C at ZORAN 669, 670; CX-1414C at ZORAN 865, 874; see also CPFF 719 (undisputed in relevant part).) Respondents' expert McAlexander testified that "there is an execution unit inside of chips because, if they do any processing at all, they will have the most rudimentary form of an execution unit based on my definition." (Tr. at 1035.) Based on the foregoing, and assuming, arguendo, that the Zoran datasheets are accorded weight, the administrative law judge finds that complainant has shown that the Zoran chips at issue practice this limitation of claim 9 of the '455 patent at issue.

D. The claim limitation "a plurality of external pins connected to the integrated circuit package, the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus..."

Complainant argued that this limitation has two clauses and only the second, viz. "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus..." is disputed; that there is no dispute that each of the Zoran chips at issue have a plurality of external pins connected to the integrated circuit package; and that under complainant and the staff's construction of the second clause, the Zoran chips practice this element. (CBr at 71-75.) Specifically, complainant argued that both complainant's expert Subramanian and respondents' expert McAlexander agreed that the Zoran integrated circuits have "a plurality of external pins connected to the integrated circuit package," and that the external pins are formed by ball connectors on the Zoran chips, which are shown in images in each of the Zoran datasheets. (CBr at 71-72.) Complainant further argued that {

} and that McAlexander agreed that based on the datasheets the Zoran parts meet this claim element under complainant and staff's interpretation. (CBr at 75-77.)

Respondents argued that "the proper grammatical understanding of this unambiguous claim term... requires that the logic bits travel from the external pins, through the external bus, and then onto the data processor," and that it is undisputed that the Zoran schematics do not depict such a configuration. (RBr at 82.) Respondents did not present any non-infringement arguments based on complainant and the staff's interpretation of this claim term beyond relying on their conclusion that the datasheets CX-1411C - 1414C are unreliable. (RRBr at 71-72.)

The staff argued that "each and every limitation of claim 9 of the '455 patent as correctly

construed is literally present in the Zoran chips incorporated in the accused Funai products." (SBr at 18.)

The administrative law judge has found, supra, that the Zoran chips are integrated circuits and have a data processor. The Zoran datasheets show that each of the Zoran chips at issue include{

} practice the limitation "a plurality of external pins connected to the integrated circuit package." (CX-1411C at ZORAN 519; CX-1412C at ZORAN 642; CX-1413C at ZORAN 836; CX-1414C at ZORAN 1012; CPFF 740 (undisputed in relevant part); CPFF 741 (undisputed in relevant part); CPFF 742 (undisputed in relevant part); CPFF 743 (undisputed in relevant part); CPFF 744 (undisputed in relevant part).) Regarding the remainder of this claim limitation, the administrative law judge has found, supra, that the claimed phrase in issue should be construed as "a plurality of external pins used to bidirectionally communicate logic bits from the data processor, the logic bits traveling to and from the data processor via an external bus." The datasheets show that{

} (CX-1411C at ZORAN 459; CX-1412C at ZORAN 599; CX-1413C at ZORAN 769; CX-1414C at ZORAN 956; CPFF 757 (undisputed in relevant part); CPFF 758 (undisputed in relevant part); CPFF 760 (undisputed in relevant part).) The datasheets also show {

} (CX-1411C at ZORAN 467; CX-1413C at ZORAN 778; CX-1414C at ZORAN 953; CPFF 762 (undisputed in relevant part); CPFF 763 (undisputed in relevant part).) Based on the foregoing, and assuming, arguendo, that the Zoran datasheets are accorded weight, the administrative law judge finds that complainant has shown that the Zoran chips at issue practice

this limitation of claim 9 of the '455 patent.

E. The claim limitation "a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one bus termination circuit, the plurality of bus termination circuits providing data to or receiving data from the execution unit, each bus termination circuit in the plurality of bus termination circuits having an input for receiving a control signal; and..."

Complainant argued that each of the Zoran chips has the claimed plurality of bus termination circuits, under any party's construction. (CBr at 77.) Specifically, complainant argued that the Zoran hardware datasheets specify {

} (CBr at 78.) Complainant also relies on the schematics for further details. (CBr at 79-88.) Complainant further argued that Zoran chips have a CPU which is an execution unit and {

} (CBr at 94.)

Respondents argued that complainant has failed to show that this claimed phrase is practiced by the Zoran chips under complainant's construction, because the alleged control signal is{

} (RRBr at 78-80.)

The staff argued that "each and every limitation of claim 9 of the '455 patent as correctly construed is literally present in the Zoran chips incorporated in the accused Funai products." (SBr at 18.)

The administrative law judge has found, supra, that a "bus termination circuit" is circuitry for signal termination that is selectively enabled or disabled in response to a control signal whose

assertion is based, at least in part, on the direction of data signals on the bus. The administrative law judge has also found, supra, that the claimed phrase "providing data to or receiving data from" is accorded its plain meaning, i.e. "the plurality of bus termination circuits supplying data to or getting data from the execution unit."

The Zoran datasheets specify that the Zoran chips at issue have {

} (CPFF 781 (undisputed in relevant part); see also, CPFF 788, 789, 790, 792, 793, 794, 794796, 797 (all undisputed in relevant part).) Thus, CX-1417 depicts a plurality of termination circuits. (See CPFF 798 (undisputed in relevant part).) Also, respondents' expert McAlexander testified that the Zoran schematics showed chips with "a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one

bus termination circuit." (Tr. at 358.)

With respect to "the plurality of bus termination circuits providing data to or receiving data from the execution unit," each of the Zoran chips at issue has {

} (CPFF at 812 (undisputed in relevant part).) In said chips, the CPU is the execution unit, and { } (CPFF at 814, 815 (undisputed in relevant part).) The Zoran datasheets show that {

} (CX-1411 at ZORAN 375; CX-1412C at ZORAN 541; CX-1413C at ZORAN 669; CX-1414C at ZORAN 865; see also CPFF 816, 817 (undisputed in relevant part).)

Regarding the claim element phrase "each bus termination circuit in the plurality of bus termination circuits having an input for receiving a control signal," the bus termination circuits in the Zoran chips each have{ } (CPFF 830 (undisputed in relevant part); CX-1417C at ZORAN 1042.)

Based on the foregoing, and assuming, arguendo, that the Zoran datasheets and Zoran schematics are accorded weight, the administrative law judge finds that the Zoran chips practice the limitation at issue.

Respondents have argued that {

} Thus, the administrative law

judge rejects respondents' argument.

F. The claim limitation "a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus."

Complainant argued that each of the Zoran chips has a control signal that turns transistors on or off. (CBr at 94.) Complainant further argued that the Zoran datasheets and schematics show the claimed coupling and decoupling in response to the assertion or deassertion of a control signal. (CBr 98-99.)

Respondents argued that the circuit components which both parties agree are the resistors shown in the Zoran schematics are never "decoupled" from the bus. (RBr at 71-72.)

The staff argued that decoupling does not require a switch or transistor between the resistors and the bus, and thus the Zoran chips do practice this limitation. (SBr at 20.)

The administrative law judge has found, supra, that "couple" means "electrically connect to" and "decouple" means "electrically disconnected from." The Zoran schematics CX-1417C show that each {

}(CX-1417C at ZORAN 1042; see also CPFF 855 (undisputed in relevant part).) The administrative law judge has found, supra, that the circuit component must be electrically disconnected from the bus, such that it, inter alia, can no longer reduce signal reflection on the bus. He finds that turning off a transistor causing a resistor to no longer reduce signal reflection on a bus meets that definition. Based on the foregoing, and assuming, arguendo, that the Zoran datasheets and Zoran schematics are accorded weight the administrative law judge finds that the Zoran chips practice the limitation at issue.

G. Asserted Claim 10, "The data processor of claim 9 wherein the at least one circuit component is a circuit component selected from a group consisting of: a capacitor, a diode, a resistor, a transistor, a voltage source, a current source, and electrical short circuit, and an inductor.

The administrative law judge has found in Section F, supra, that the schematics show a

{ }

(CX-1417C at ZORAN 1042; see also CPFF 854 (undisputed in relevant part); RRCPFF 854A.) A { } is listed as one of the group of possible circuit components which satisfies claim 10. Based on the foregoing, and assuming, arguendo, that the Zoran datasheets and Zoran schematics are accorded weight the administrative law judge finds that the Zoran chips practice the limitation at issue.

H. Conclusion

Thus, based on the foregoing, the administrative law judge finds that, were the Zoran datasheets and schematics accorded weight, the accused products would infringe asserted claims

9 and 10 of the '455 patent.

X. Validity

A. Prior Art

Respondents argued that asserted claims 9 and 10 of the '455 patent are anticipated by U.S. Patent No. 3,832,575 (Dasgupta) (RX-532). (RBr at 85-95.) It is further argued that said claims would have been obvious considering Dasgupta in view of certain secondary references. (RBr at 99-121.)[12]

Complainant argued that respondents did not present any evidence that asserted claims 9 and 10 are invalid as anticipated by any prior art reference; that Dasgupta does not anticipate said claims; and that the asserted claims are not obvious. (CBr at 102-22.)

The staff argued that no evidence of invalidity under 35 U.S.C. § 102 was presented by respondents and that the evidence did not clearly and convincingly show that claims 9 or 10 are invalid under 35 U.S.C. § 103 because no combination of references rendered obvious the claimed data processing within an integrated circuit package having the claimed plurality of bus termination circuits in issue, citing Subramanian, Tr. at 1085-1097. (SBr at 24.)

1. Anticipation

Section 102 of Title 35 sets forth the novelty conditions that must be satisfied to obtain a valid U.S. patent. If every limitation of a patent claim is satisfied by a single item of prior art, it is "anticipated" and, hence, invalid under § 102 for lack of novelty. Karsten Mfg. Corp. v. Cleveland Golf Co., 242 F.3d 1376, 1383 (Fed. Cir. 2001). Thus to invalidate a patent by anticipation, a prior art reference normally needs to disclose each and every

[12] Although initially in response to the complaint it was alleged that the '455 patent was unenforceable, respondents abandoned that defense in their pre-hearing statement. (CPFF 1101, CPFF 1102 (both undisputed).)

limitation of the claim. Standard Havens Prods., Inc. v. Gencor Indus., Inc., 953 F.2d 1360, 1369 (Fed. Cir. 1991). However, a prior art reference may anticipate when a claim limitation or limitations not expressly found in that reference are nonetheless inherent in it. Id. Accordingly, under 35 U.S.C. § 102 a claim is anticipated "if each and every limitation is found either expressly or inherently in a single prior art reference." Celeritas Techs. Ltd. v. Rockwell Int'l Corp., 150 F.3d 1354, 1361 (Fed. Cir. 1998). Anticipation is a question of fact, including whether or not an element is inherent in the prior art. In re Schreiber, 128 F.3d 1473, 1477 (Fed. Cir. 1997). Under the principles of inherency:

> [t]o serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill

Continental Can Co. USA, Inc. v Monsanto Co., 948 F.2d 1264, 1268 (Fed. Cir. 1990) (emphasis added). At the hearing, there was no evidence in the record that the asserted claims are invalid as anticipated by any prior art reference, nor did respondents' technical expert McAlexander, offer any opinion relating to respondents' anticipation defense.[13] Moreover to the extent that respondents argued that the asserted claims are anticipated by Dasgupta, it is undisputed that Dasgupta does not explicitly or inherently disclose every element of asserted claims 9 and 10. Thus McAlexander testified:

> Q. And you admitted in your deposition on Sunday that Dasgupta does not teach the providing data to or receiving data from the execution unit limitation of Claim 9 explicitly, correct?

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[13] Respondents in their post hearing submissions rely on testimony of McAlexander at the evidentiary hearing that was stricken at said hearing. Respondents in their RBr at 50 requested that the administrative law judge "reverse his ruling striking Mr. McAlexander's testimony." Said request has been denied. See Section I (Procedural History), supra.

A. By explicit you mean the entirety of that providing to and the - - both?

Q. Yes, sir.

A. Yes, I said that it does not do both.

Q. And so since that is not taught by Dasgupta –

A. Right.

Q. - - you have to find teaching of that element in another reference and testify as to the reason why a person of ordinary skill in the art in 1993 would have combined those two references to disclose that element; is that fair?

A. That's fair.

(Tr. at 1062-63.)

With respect to the Dasgupta patent, it discloses a "Data Bus Transmission Line Termination Circuit" that is formed on the "same integrated circuit chip as the receiver circuit." (CPFF 1007 (undisputed); RX-532 at Abstract.) In each of the disclosed embodiments, Dasgupta shows a "receiver circuit," without any description of its function or application. (RX-532 at Figs. 4-8; 4:29-9-46.) None of the embodiments in Dasgupta disclose either transmit circuitry or a transmit path for data. (CPFF 1009 (undisputed).) Accordingly, the administrative law judge finds that the data bus connected to the integrated circuits described therein is uni-directional. (RX-532 at Figs. 1, 3-8; 3:57-9:46.) Because Dasgupta describes only the receive path, it does not disclose "the control signal.. .to couple at least one circuit component to the bus".

Dasgupta further discloses termination circuitry generically for use within an integrated circuit that contains a "receiver circuit." (CPFF 1007 (undisputed); RX-532 at Abstract, Figs. 3-8.) According to its Abstract:

> The termination circuit is preferably formed on the same integrated circuit chip as the receiver circuit so as to be located adjacent the

> effective end of the total transmission line including the portion extending from the data bus proper through the connections and conductors of the board, card, module and chip to the receiver circuit on the chip.

(RX-532 at Abstract.) Each of the drawings in Dasgupta illustrating the inventive embodiments (Figs. 3-8) contains a block labeled either "receiver circuit" or "RC1 " through "RC6." (CPFF 1011 (undisputed); RX-532 at Figs. 3-8.) At the hearing, neither respondents nor their expert provided any evidence that Dasgupta discloses the claimed term "plurality of bus termination circuits" as that term has been construed by the administrative law judge, supra. Furthermore, McAlexander never identified anything in Dasgupta corresponding to the "execution unit internal to the data processor" limitation of claim 9. To the contrary, the administrative law judge finds that the generic "receiver circuit" shown in Dasgupta meets neither the "data processor within an integrated circuit package" nor the "execution unit internal to the data processor" limitations of claim 9. Moreover because the disclosure of Dasgupta is directed only to termination of the receiver circuitry within an integrated circuit, the data bus shown is uni-directional. (RX- 532 at Figs. 1, 3-8; 3:57-9:46.) At the hearing, neither the respondents nor their technical expert provided any evidence or expert opinion that Dasgupta inherently or explicitly disclosed an external bus "used to bidirectionally communicate logic bits to and from the data processor." To the contrary respondents' expert merely stated: "[t]his chip will be packaged, it's the way it was done circa 1974, so this packaged present invention chip would have external pins, and the external pins were used to bi-directionally communicate logic bits to and from the data processor via an external bus." (McAlexander, Tr. at 905:7-12).[14]

Regarding the language of claim 9 "the plurality of bus termination circuits providing data

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[14] This testimony was not stricken. See Tr. at 905-07.

to or receiving data from the execution unit," respondents' expert admitted that Dasgupta does not teach "the plurality of bus termination circuits providing data to or receiving data from the execution unit" limitation of claims 9 and 10. (McAlexander, Tr. at 1062-63.) Referring to the claimed language "the plurality of bus termination circuits" the "bus termination circuit" in claim 9 "is selectively enabled or disabled in response to a[n] control signal whose assertion is based, at least in part, on the direction of data signals on the bus," as found by the administrative law judge supra. The administrative law judge finds that Dasgupta does not disclose "bus termination circuits" that meet this limitation, because Dasgupta illustrates only the receiver and receive path for data in an integrated circuit. (RX- 532 at Figs. 1, 3-8; 3:57- 9:46.) Therefore, he finds that Dasgupta does not teach bus termination that is selectively enabled or disabled based on whether the integrated circuit is receiving or transmitting data.

Based on the foregoing, the administrative law judge finds that respondents have not meet their burden of proving, by clear and convincing evidence, that asserted claim 9 and asserted claim 10, which is dependent on said claim 9, are anticipated by Dasqupta.

2. Obviousness

At the hearing, respondents contended that claims 9 and 10 of the '455 patent were rendered obvious by four combinations of two references: the Dasgupta patent (RX-532) in view of a Gist patent (RX-243), Dasgupta in view of a Gabara patent (RX-13), Dasgupta in view of a Lauffer patent (RX-238) and Dasgupta in view of a Work patent (RX-21). (CPFF 1019.) The administrative law judge finds that respondents have failed to meet their burden of proving, by clear and convincing evidence, that any of those combinations renders claims 9 and 10 obvious.

Respondents have the burden to overcome the presumption that the asserted claims of the '455 patent are valid. Tech. Licensing Corp v Videotek, Inc., 545 F.3d 1316 (2008). The burden

of persuasion never shifts to complainant. Id. Rather, the risk of "decisional uncertainty" remains on the party or parties asserting invalidity. Id. Thus, it is respondents' burden to prove by clear and convincing evidence that any of the alleged prior art references, alone or in combination, render obvious asserted claims 9 and 10 of the '455 patent. See PharmaStem Therapeutics, Inc. v. ViaCell, Inc., 491 F.3d 1342, 1360 (Fed. Cir. 2007) (stating, "the burden falls on the patent challenger to show by clear and convincing evidence that a person of ordinary skill in the art would have had reason to attempt to make the composition or device, or carry out the claimed process, and would have had a reasonable expectation of success in doing so."). Failure to do so means that respondents lose on this point. Tech. Licensing, 545 F.3d at 1327.

Included within the presumption of validity is a presumption of non-obviousness. Structural Rubber Prods. Co. v. Park Rubber Co., 749 F.2d 707, 714 (Fed. Cir. 1984). Regarding non-obviousness, the patent statute dictates that a person is not entitled to a patent if the differences between the claimed invention and the prior art "are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. §103; see also Net MoneyIN, Inc. v. VeriSign, Inc., 545 F.3d 1359, 1371 (Fed. Cir. 2008) (stating, "differences between the prior art reference and a claimed invention, however slight, invoke the question of obviousness, not anticipation.").

The ultimate determination of whether an invention would have been obvious is a legal conclusion based on underlying findings of fact. In re Dembiczak, 175 F.3d 994, 998 (Fed. Cir. 1999). The underlying factual inquiries relating to non-obviousness include: 1) the scope and content of the prior art; 2) the level of ordinary skill in the art; 3) the differences between the claimed invention and the prior art; and, 4) secondary considerations of non-obviousness, such as long-felt need, commercial success, and the failure of others. See Graham v. John Deere Co., 383

U.S. 1, 17 (1966).

Obviousness may be based on any one of the alleged prior art references or a combination of the same, and what a person of ordinary skill in the art would understand based on his knowledge and said references. If all of the elements of an invention are found, then:

> [A] proper analysis under § 103 requires, inter alia, consideration of two factors: (1) whether the prior art would have suggested to those of ordinary skill in the art that they should make the claimed composition or device, or carry out the claimed process; and (2) whether the prior art would also have revealed that in so making or carrying out, those of ordinary skill would have a reasonable expectation of success. Both the suggestion and the reasonable expectation of success must be founded in the prior art, not in the applicant's disclosure.

Velander v. Garner, 348 F.3d 1359, 1363 (Fed. Cir. 2003) (emphasis added) (internal citations omitted). Further, the critical inquiry in determining the differences between the claimed invention and the prior art is whether there is a reason to combine the prior art references. See C.R. Bard v. M3 Sys., 157 F.3d 1340, 1352 (Fed. Cir. 1998). For example:

> [A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.

KSR Int'l Co. v. Teleflex, Inc., 550 U.S. 398, 418-19 (2007) (emphasis added) (KSR). However, the Supreme Court has rejected a "rigid approach," regarding a patent challenger's obligation to demonstrate a "teaching, suggestion, or motivation to combine" in the prior art. Id. at 419-22. The Court stated that:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. Sakraida and Anderson's-Black Rock are illustrative-a court must ask whether the improvement is more than the predictable use of prior art elements according to their established function.
>
> Following these principles may be more difficult in other cases than it is here because the claimed subject matter may involve more than the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement. Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. To facilitate review, this analysis should be made explicitly. See In re Kahn, 441 F.3d 977, 988 (CA Fed. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusions of obviousness"). As our precedents make clear, however, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

Id. at 417-18 (emphasis added). Further, a suggestion to combine may come from the prior art, as filtered through the knowledge of one skilled in the art. See Certain Lens-Fitted Film Pkgs., Inv. No. 337-TA-406, Order No. 141 at 6 (May 24, 2005). "[I]n many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." KSR, 550 U.S. at 420-21.

At the outset, the administrative law judge finds that none of the combinations advanced

by respondents contain all the elements of claims 9 and 10. Thus in their response filed January 21, 2011 to Question 35 of Order No. 36, respondents identified three limitations in claim 9 that were allegedly present in the Gist, Gabara, Lauffer, and Work references, such that when combined with Dasgupta, each of those combinations would render claims 9 and 10 obvious. See response to Q35. Said three limitations in respondents' obviousness combinations with Dasgupta were (1) the termination circuit within a data processor; (2) a bi-directional bus; and (3) decoupling the circuit component from the bus. (Id.) However the administrative law judge finds that Dasgupta is missing more than these three limitations. See supra. Hence even if said four secondary references combined with Dasgupta disclosed those three limitations, none of the combinations disclose all limitations of claims 9 and 10. See infra. In addition, as seen infra, the administrative law judge finds that respondents failed to prove that the asserted claims are obvious because they have not established why a person of ordinary skill in the art at the time the '455 patent application was filed would have combined any of the references in the manner asserted by respondents.[15]

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[15] Respondents' expert McAlexander did provide the following testimony as to the alleged combinations:

> Q. Please explain your opinion with regard to whether one of ordinary skill in the art at the time of the Gay '455 patent invention would have found it obvious to combine any one of Work RX-021, Lauffer RX-238, Gabara, RX-013, or Gist, RX-243, to the teachings of Dasgupta, and please explain your answer.
>
> A. It is my opinion that one of skill in the art at the time of the invention of the Gay patent would have found that any one of the combinations of Dasgupta, in view of Gabara, Gist, Work, or Lauffer, would have found the -- with respect to the termination circuit, would have found that element obvious.

(Tr. at 971-72.) Said testimony is found to be merely conclusory.

a. Dasgupta With Gist

Regarding the combination of Dasgupta in view of the Gist patent (RX-243) the administrative law judge finds that said combination does not contain at least the following limitations: (1) "a data processor within an integrated circuit package"; (2) "an execution unit internal to the data processor"; (3) "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus"; (4) "a plurality of bus termination circuits"; and (5) "the plurality of bus termination circuits providing data to or receiving data from the execution unit." Referring to said limitation (1), Fig. 1 from Gist is a system-level diagram of computer system 10, comprised of CPUs 12 and 14, memory modules 16, 18, 20 and 22, and I/O modules 24, 26 and 28, each connected to system bus 30. (CPFF 1020 (undisputed); RX-243 at 4:57-66; Fig. 1.) The components 12-28 of Fig. 1 are called both "devices" and "modules" throughout the specification, and never called integrated circuits. (CPFF 1021 (undisputed); RX-243 at 4:57-28:50.) Each CPU, memory, and I/O module in Gist has a bus interface circuit, for example, interface 14a in CPU module 14. (CPFF 1023 (undisputed).) The bus interface circuit terminates the system bus, among other things. (CPFF 1024 (undisputed).) Within each device, e.g., CPU 14, there is a line separating the bus interface circuit (here 14a) from the rest of the device, indicating that the bus interface circuit is a distinct portion of the device. (RX-243-Fig. 1)

When asked to explain the relevance of Gist "to the issue of termination circuitry within a data processor," respondents' expert McAlexander answered:

> Figure 1 of Gist shows multiple different units, such as CPUs, which are labeled at the bottom right corners 12 and 14, communicating bi-directionally to a bi-directional bus 30, and then if we look further in Figure 3, Figure 3 represents a circuit that is included in each one of 12 and 14 CPU, and you will see in Figure 3 that the - at the top corner is labeled I/O, and that is the

> connection point to the I/O or the input/output to the data bus 30.
>
> And then you will notice that, inside of the box labeled 40, which is a - labeled in a previous figure. This shows both a driver and a receiver. A driver drives data to the bus, a receiver receives data from the bus, and to the left of these two blocks, driver and receiver, is a smaller block called 42, which is termination, so this is a termination circuit that is electrically connected to the bi-directional bus.

(Tr. at 953-54.) As seen from the foregoing, respondents' expert failed to specifically identify a disclosure of the "data processor within an integrated circuit package" in Gist. Moreover complainant's expert Subramanian explained that within those CPU modules in Gist the bus termination circuitry is contained in an application specific integrated circuit (ASIC) that is separate from the CPU integrated circuit. (Tr. at 1087-89; RX-243 at 5.) Subramanian further explained that Gist discloses that the ASIC is located in the bus interface circuitry portion 12a of CPU module 12, as an example, separate from the CPU integrated circuit that would contain a data processor. (Tr. at 1089.) Gist further teaches that the bus interface circuit for each module or device includes the ASIC containing the bus termination circuitry. (CPFF 1030 (undisputed).) Gist also teaches that the ASIC includes bus interface cells 40, each of which contains driver 70, receiver 90, and termination circuit 42. (RX-243 at 5:15-44.) Significantly Gist does not disclose that the ASIC contains either a data processor or an execution unit internal to the data processor. (RX-243 at 5:15-44.) Neither respondents nor their expert referred to the ASIC teaching of the Gist patent. (CPFF 1033 (undisputed).) Hence because Gist teaches there is a separate integrated circuit for the bus interface circuits, apart from whatever integrated circuit may also be part of the device or module, the administrative law judge finds that Gist does not disclose the "data processor within an integrated circuit package" which also contains the "plurality of bus termination circuits" as recited in claim 9.

Regarding the claimed language "an execution unit internal to the data processor," because the termination circuitry disclosed in Gist is contained within an application specific integrated circuit (ASIC), not as part of a data processor within an integrated circuit package as required by claim 9 (see RX-243 at 5:15-44), it necessarily follows that Gist does not teach "an execution unit internal to the data processor." Moreover at the hearing, neither respondents nor their expert provided any evidence regarding this limitation in Gist.

Regarding the claimed language "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus," because the termination circuitry disclosed in Gist is contained within an application specific integrated circuit (ASIC), not as part of a data processor within an integrated circuit package as required by claim 9 (RX-243 at 5:15-44), the administrative law judge finds that Gist does not teach "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus" under the administrative law judge's construction of said language. At the hearing, respondents' expert did identify system bus 30 in Gist as the "bi-directional bus" in claim 9. (CPFF 1035 (undisputed).) However system bus 30 in Gist is connected to the ASIC within the bus interface circuit of each module (RX-243 at 4:57-5:44) not to the integrated circuit containing the data processor, as required in asserted claim 9. (CPFF 1036 (undisputed).)

Regarding the claimed language "a plurality of bus termination circuits," the administrative law judge has found that "bus termination circuit" in claim 9 "is circuitry for signal termination that is selectively enabled or disabled in response to a control signal whose assertion is based, at least in part, on the direction of data signals on the bus." At the hearing, respondents' expert did not apply said construction to Gist. (CPFF 1038 (undisputed).) Moreover there is no evidence

that Gist meets said claimed language as construed by the administrative law judge.

Referring to the claimed language "the plurality of bus termination circuits providing data to or receiving data from the execution unit" respondents did not address said limitation in the combination of Dasgupta with Gist in their response filed January 21, 2011 to Question 35 posed in Order No. 36. In any event, neither respondents nor their expert have proven that Gist meets said limitation under any party's construction. As found supra, Gist discloses that the termination circuitry is contained within an application specific integrated circuit (ASIC), not a data processor integrated circuit. (RX-243 at 5:15-44.) Accordingly, the administrative law judge finds that there is also no "execution unit" in the same integrated circuit as the termination circuitry, as required by claim 9, and therefore the termination circuitry is not capable of "providing data to or receiving from" an execution unit that is located in another integrated circuit.

In addition, the administrative law judge finds that, during the hearing, neither respondents nor their expert McAlexander provided evidence in the record as to why a person of ordinary skill in the art at the time the '455 patent was filed would have combined the Dasgupta and Gist references to render claims 9 and 10 obvious. Respondents have therefore not met their burden, by clear and convincing evidence, to demonstrate that a person of ordinary skill in the art would have combined Dasgupta and Gist in the manner claimed.

b. Dasgupta With Gabara

Referring to the combination of Dasgupta in view of the Gabara patent (RX-13) the administrative law judge finds that said combination does not contain at least the following limitations: (1) "a data processor within an integrated circuit package"; (2) "an execution unit internal to the data processor"; (3) "the plurality of external pins used to bidirectionally

communicate logic bits to and from the data processor via an external bus"; (4) "a plurality of bus termination circuits"; and (5) "the plurality of bus termination circuits providing data to or receiving data from the execution unit." Thus at the hearing, neither respondents nor their expert provided any evidence regarding said limitation (1). Respondents in ROCPFF 1043 refer to the following testimony of McAlexander:

> Q. Finally, with regard to Gabara, RX-013, you mentioned that as a secondary reference with regard to termination circuitry within a data processor as well, I believe?
>
> A. That is correct.
>
> Q. And could we get- it's on the screen.
> Could you please explain the relevant teachings of Gabara, insofar as that issue is concerned?
>
> A. Yeah, Gabara shows, in Figure 2 on RX-13-2, several blocks, I'll focus on block 20, which is a digital impedance block, and the digital impedance is controlled by Sn, and that is an input signal that controls the application or disassociation of decoupling of the digital impedance from the bus.
>
> Q. And that is all within a termination circuit within a data processor?
>
> A. Yes.
>
> Q. And could you explain how one of ordinary skill in the art would apply the teachings of Gabara in terms of the termination circuitry within the data processor to Dasgupta, please?
>
> A. Yes. The Dasgupta reference shows selective assertion or deassertion of a control signal in order to permit signal termination or to decouple the termination component :from the bus. And as shown also, here in Gabara is a digital impedance circuit that is selectively activated or deactivated, coupled or decoupled to the bus based upon the input voltage level of the control signal Sn.

(Tr. at 968-969.) Said testimony does not show that Gabara teaches said limitation (1). Moreover complainant's expert Subramanian provided his opinion that Gabara does not teach the "data processor within an integrated circuit package" limitation:

Q. Do you have an opinion as to whether Gabara teaches a bi-directional data bus?

A. I do. It is my opinion that Gabara does not teach a bi-directional data bus. It does not teach a bi-directional data bus because the disclosures within Gabara have separate transmit and receive connections, most of Gabara deals purely with transmit, and it's only dealing with output impedance, not with matching. It's dealing with the drivability and the output.

There's separate disclosure related to receive which is identified as being different circuitry, so it's completely separated. There's no bi-directional bus disclosure.

(Tr. at 1095.)

Referring to the claimed language "an execution unit internal to the data processor" (limitation (2)), respondents' expert McAlexander testified:

Q. Finally with regard to Gabara, RX-013, you mentioned that as a secondary reference with regard to termination circuitry within a data processor as well, I believe?

A. That is correct.

Q. And could we get -- it's on the screen.

Could you please explain the relevant teachings of Gabara, insofar as that issue is concerned?

A. Yeah, Gabara shows, in Figure 2 on RX-13-2, several blocks, I'll focus on block 20, which is a digital impedance block, and the digital impedance block is controlled by Sn, and that is an input signal that controls either the application or disassociation or decoupling of the digital impedance from the bus.

Q. And that is all within a termination circuit within a data processor?

A. Yes.

Q. And could you please explain how you believe one of ordinary skill in the art would apply the teachings of Gabara in terms of the termination circuitry within the data processor to Dasgupta, please?

A. Yes. The Dasgupta reference shows selective termination, either

assertion or deassertion of a control signal in order to permit signal termination or to decouple the termination component from the bus.

And as shown also, here in Gabara is a digital impedance circuit that is selectively activated or deactivated, coupled or decoupled to the bus based upon the input voltage level of the control signal Sn.

Q. And is it your belief that a person of ordinary skill in the art at the time of the Gay invention, the '455 patent, would have found that combination to have been obvious?

A. In my opinion, yes.

(Tr. at 968-9.) Said testimony does not disclose "an execution unit internal to the data processor."

As for the claimed language "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus" (limitation (3)), the administrative law judge construed such language as "a plurality of external pins used to bidirectionally communicate logic bits from the data processor, the logic bits traveling to and from the data processor via an external bus." (See Section VII.F, supra.) At the hearing, respondents' expert McAlexander testified:

Q. Mr. McAlexander, were there any other references that you relied upon in order to combine with Dasgupta with regard to the bi-directionality issue?

A. Yes, Gabara.

* * *

Q. Could we have Gabara [RX-13] up?

Mr. McAlexander, could you please explain the relevant teachings of Gabara, as you understand it, to the issue of bi-directionality and how it would be combined with Dasgupta?

A. The circuit that's shown in 100 is selectively applied or decoupling impedance, for the purpose of impedance matching to the bus, and

the pin that's shown in 10 is connected to an external bus which is 200. The patent specification specifies that this particular pin can be either to a uni-directional or a bi-directional. It could be for input and output.

Q. And can you please explain how you would combine that with the Dasgupta reference?

A. This patent would then show that this termination component is linked -- electrically connected to a bi-directional bus and, therefore, would permit both the input of data from the bus and the output of data to the bus.

(Tr. at 947-48.) The administrative law judge finds that said testimony does not show that Gabara refers to an external bus connected to an integrated circuit, let alone a bi-directional bus connected to an integrated circuit. Moreover, as complainant's expert, Subramanian, testified, Gabara does not disclose a bi-directional bus, and further explained that Gabara teaches modifying the impedance of an output terminal. See supra.

Referring to the claimed language "bus termination circuit" in claim 9, the administrative law judge has construed said language as "circuitry for signal termination that is selectively enabled or disabled in response to control signal whose assertion is based, at least in part, on the direction of data signals on the bus." At the hearing, respondents' expert did not apply this construction to Gabara.

In addition to the foregoing, at the hearing neither respondents nor their expert McAlexander provided evidence in the record as to why a person of ordinary skill in the art, at the time the '455 patent was filed, would have combined the Dasgupta and Gabara references to render claims 9 and 10 obvious. Respondents refer to testimony of their expert (Tr. at 968-9, supra), which the administrative law judge has found inadequate. See supra.

c. Dasgupta With Lauffer

At the hearing, and with regard to the combination of Dasgupta with Lauffer, neither

respondents nor their expert McAlexander provided any evidence regarding the claimed language "a data processor within an integrated circuit package." Respondents expert did testify:

Q. And get Lauffer [RX-238] up, please.

Would you please explain the relevant teachings of Lauffer, insofar as they relate to the termination circuitry within a data processor limitation?

A. The termination -- if I may use this, the termination circuit is shown inside of the device labeled 10 on the left side of the screen, and the component -- termination component is the resistor that's labeled R sub t -- looks like t1, that is in the bottom right corner of the dashed box labeled 10.

And the transistor, which selectively couples Rt1, the component to the data bus, or decouples, such that Rt1 is not electrically connected, that functionality is performed by transistor 38. So the combination of 38 and Rt1provide the termination circuit that is connected, selectively connected or disconnected from the termination line, which is labeled as 14.

Q. And is that within the data processor?

A Yes. In fact, if we look at the CMOS, it has CMOS transmit and receive circuit, which is labeled in box -- looks like 16, I believe.

Q. I believe it's 10.

A. No, the CMOS transmit and receive circuit is in block 16, and the control of that shown like, for instance, T/r line 50, there would be a rudimentary execution unit that would provide the control logic for that, so it is within a data processor.

Q. And how, in your opinion, would one of ordinary skill in the art have used the teachings from Lauffer RX-238 in connection with Dasgupta, insofar as the termination circuitry within the data processor element is concerned?

A. Well, as I mentioned before, Dasgupta teaches the -- teaches termination circuit, and Lauffer also has a termination circuit arranged in the same way as Dasgupta, where the switch -- the transistor provides the coupling and decoupling of the resistor component from the bus in a like manner, as what I described earlier in Dasgupta, and Lauffer expressly teaches the

bi-directional aspects. So this is an input/output termination circuit.

(Tr. at 966-68.) However as complainant's expert Subramanian testified:

Q. Thank you. Could I have RX-238 in evidence, the Lauffer patent at Figure 1.

Do you have an opinion as to whether Lauffer teaches a data processor within an integrated circuit package?

A. I do. It is my opinion that Lauffer, the Lauffer patent 827 does not teach a data processor with[in] an integrated circuit package.

In particular, if we look at the Lauffer patent, specifically all it deals with is a CMOS transceiver device that is not a data processor. There is no execution unit within it. It does not meet the requirements of Claim 9.

(Tr. at 1095-96 (emphasis added.).)

Referring to the claimed language "an execution unit internal to the data processor" respondents' expert McAlexander testified that "there would be a rudimentary execution unit that would provide the control logic for that, so it is within a data processor." (Tr. at 966-68, supra.) However as complainant's expert Subramanian testified, Lauffer does not teach the "execution unit internal to the data processor" limitation. See supra.

Referring to the claimed language "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus," at the hearing, respondents' expert identified a bi-directional bus in Fig. 1 of Lauffer. (CPFF 1061 (undisputed).) Lauffer does not, however, disclose a data processor within an integrated circuit package, and accordingly does not show any path to "bidirectionally communicate logic bits to and from the data processor" as required by claim 9.

Referring to the claimed phrase "a plurality of bus termination circuits" under the administrative law judge construction, which is substantially the same as the proposed

construction of the complainant and the staff, at the hearing, respondents' expert did not apply this construction to Lauffer. (CPFF 1062 (undisputed).) Accordingly, there is no evidence that Lauffer meets this element under said construction.

In addition, at the hearing, neither respondents nor their expert McAlexander established why a person of ordinary skill in the art at the time the '455 patent was filed would have combined the Dasgupta and Lauffer references to render claims 9 and 10 obvious. While respondents' expert did testify:

> Q. And how, if at all, would one of ordinary skill in the art use that teaching or apply that teaching to Dasgupta?
>
> A. Dasgupta has a data bus. This, in combination, with Lauffer indicates a bi-directional bus.

(Tr. at 949), the administrative law judge does not find said testimony indicates why a person of ordinary skill in the art would combine Dasgupta with Lauffer.

d. Dasgupta With Work

The administrative law judge finds that the combination of Dasgupta in view of the Work patent (RX-21) does not render obvious claims 9 and 10 of the '455 patent because it is does not contain at least the following limitations: (1) "a data processor within an integrated circuit package"; (2) "an execution unit internal to the data processor"; (3) "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus"; (4) "a plurality of bus termination circuits"; (5) "the plurality of bus termination circuits providing data to or receiving data from the execution unit"; and (6) "the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus."

At the hearing, neither respondents nor their expert McAlexander provided adequate

evidence regarding said limitations in the combination of Dasgupta with Work. Respondents' expert testified:

Q. Can we please put up Work RX-021? Mr. McAlexander, could you please explain the relevant teachings of Work, insofar as they relate to the bi-directional bus issue?

A. With Work -- I'll use the pointer. Work, on the face page of Figure 1, is a data processing chip that communicates with various components, but on the right side, there is a section, a circuit group that's called programmable line driver receivers. Driver receivers says that it both drives and receives, and the double-headed arrow line that's just immediately to the right of that, communicating with the external peripheral equipment, is identified by Work as a bi-directional bus.

* * *

Q. Okay. And finally, with regard to the termination circuitry within a data processor -- I'd like to put up Work, RX-021.

Mr. McAlexander, you made reference to Work as a possible secondary reference. Can you please explain its relevance to the issue of termination circuitry within a data processor?

A. The termination circuitry within theWork reference is shown as R sub 1 and R sub 2. These are termination circuits that are applied to the bus, which is labeled 216, they're connected to the internal bus 216, and then to a pad which goes external to the chip.

Q. And so is it fair to say that the termination circuitry within -- the termination circuitry of Work is within the data processor?

A. Yes.

Q. And what would be the -- I'm sorry -- and how would you purport to combine any teachings of Work, insofar as the termination circuitry within the data processor is concerned to Dasgupta?

A. What this reference shows -- teaches is the use of the termination circuit in association with a bi-directional bus 216.

That's borne out by the input and output buffers labeled I sub n and O-U-T that are attached to the left of that highlighted, green highlighted bus.

And the pullup resistor program in circuit 88, pulldown resistor

program in circuit 90 that's shown in the bottom two boxes of Figure 5, show selective resistance that can be programmed and allows the user of this type of device to selectively program the resistances to be high impedance or low impedance.

* * *

Q. Please explain your opinion with regard to whether one of ordinary skill in the art at the time of the Gay '455 patent invention would have found it obvious to combine any one of Work RX-021, Lauffer RX-238, Gabara, RX-013, or Gist, RX-243, to the teachings of Dasgupta, and please explain your answer.

A. It is my opinion that one of skill in the art at the time of the invention of the Gay patent would have found that any one of the combinations of Dasgupta, in view of Gabara, Gist, Work, or Lauffer, would have found the -- with respect to the termination circuit, would have found that element obvious.

(Tr. at 949-50, 969-71.) Work however does not teach the "data processor within an integrated circuit package" limitation. As complainant's expert testified:

Q. And lastly, RX-21 in evidence, the Work patent. Could I have Figure 1, please.

Do you have an opinion as to whether the Work patent discloses a data processor with an integrated circuit package?

A. I do. It is my opinion that the Work patent does not disclose a data processor within an integrated circuit package.

Specifically, the disclosure of the Work patent, and indeed it shows up in the title itself and specifically in Figure 1, is related to a peripheral controller, and the peripheral controller does not meet the requirements of being a data processor with an integrated circuit package. It does not provide the execution unit, et cetera, that is required by Claim 9 of the '455 patent.

(Subramanian, Tr. at 1096-97.)

Moreover, referring to the claimed language "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus" the administrative law judge construed the language substantially as complainant and staff construed it. See supra. At the hearing, respondents' expert McAlexander identified a bi-directional bus in

Work. (CPFF 1070 (undisputed).) McAlexander did not, however, identify an external bus that is "used to bidirectionally communicate logic bits to and from the data processor," consistent with the construction of complainant and the staff.

With respect to the claimed language "a plurality of bus termination circuits," the administrative law judge's construction is substantially identical to the complainant and staff's proposed constructions. At the hearing, respondents' expert did not apply this construction to Work. (CPFF 1072 (undisputed).)

Referring to the claimed language "the plurality of bus termination circuits providing data to or receiving data from the execution unit," neither respondents nor their expert McAlexander established that Work meets said the limitation.

With regard to the claimed language "the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus," at the hearing, respondents' expert testified that he was not relying on Work for the "decouple" teaching to combine with Dasgupta. (CPFF 1075 (undisputed).)

In addition at the hearing, neither respondents nor their expert McAlexander provided adequate evidence in the records as to why a person of ordinary skill in the art at the time the '455 patent was filed would have combined the Dasgupta and Work references to render claims 9 and 10 obvious. (CPFF 1076.)

Based on the foregoing, the administrative law judge finds that respondents have not established by clear and convincing evidence that claims 9 and 10 of the '455 patent are obvious in view of any of the alleged combinations.

B. Lack Of Written Description

Respondents argued that the unambiguous language of the limitation of claim 9, viz.

"plurality of external pins . . . used to bidirectionally communicate logic bits to and from a data processor via an external bus" requires that data be passed from the external pins to the data processor by way of an external bus, and to the external pins from the data processor by way of an external bus; that there is no embodiment disclosed in the '455 patent that reads on this limitation; and that therefore claim 9 and dependent claim 10 of the '455 patent are invalid for lack of written description. (RBr at 122.)

Complainant argued that the parties dispute that the meaning of the limitation "plurality of external pins . . . used to bidirectionally communicate logic bits to and from a data processor via an external bus" is unambiguous, and that under complainant's and staff's interpretation, this element is consistent with all disclosed embodiments of the '455 patent. (CRBr at 95.)

As the Federal Circuit stated "[a] patent is presumed valid, and the burden of persuasion to the contrary is and remains on the party asserting invalidity." Ralston Purina Co. v. Far-Mar-Co, Inc., 72 F.2d 1570, 1573 (Fed. Cir. 1985). "In addition, the party asserting invalidity also bears the initial procedural burden of going forward to establish the legally sufficient prima facie case of invalidity." Id. "A party asserting invalidity based on 35 U.S.C § 112 bears no less a burden and no fewer responsibilities than any other patent challenger." Id. at 1574.

The written description requirement of section 112 is a question of fact. Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1565 (Fed. Cir. 1991). It asks whether the disclosure in an application as originally filed "reasonably conveys to the artisan that the inventor had possession at that time of the later claimed subject matter." In re Kaslow, 707 F.2d 1366, 1375 (Fed. Cir. 1983). To comply with the written description requirement, "the specification need not describe the claimed subject matter in exactly the same terms as used in the claims; it must simply indicate to persons skilled in the art that as of the [filing] date the applicant had invented what is now claimed." All

Dental Prodx, LLC v. Advantage Dental Prods., Inc., 309 F.3d 774, 779 (Fed. Cir. 2002) (quoting Eiselstein v. Frank, 52 F.3d 1035, 1038 (Fed. Cir. 1995)); see also In re Wilder, 736 F.2d 1516, 1520 (Fed. Cir. 1984) ("It is not necessary that the claimed subject matter be described identically"). The administrative law judge has found in Section VII F supra that the parties dispute the meaning of the limitation "plurality of external pins . . . used to bidirectionally communicate logic bits to and from a data processor via an external bus," that said limitation when properly construed means" a plurality of external pins used to bidirectionally communicate logic bits to and from a data processor via an external bus" and that the specification of the '455 patent supports said construction. Hence he finds that respondents have not established, by clear and convincing evidence, that asserted claims 9 and 10 of the '455 patent fail to meet the written description requirement of 35 U.S.C. § 112 ¶ 1.

XI. Remedy

In investigations in which a violation of Section 337 is found, the Commission may issue either a limited exclusion order or a general exclusion order and, if appropriate, cease and desist orders. See 19 U.S.C. §§ 1337(d) and (f). In this investigation, complainant Freescale seeks a limited exclusion order directed to the products of those respondents found to be infringing. (CBr at 127-8.) Freescale also seeks cease and desist orders. (Id. at 138-9.)

If there is a violation of Section 337, the staff believes that a limited exclusion order against the respondents found to infringe would be the appropriate recommendation. (SBr at 25.) With regard to cease and desist orders, the staff argued that respondents have stipulated as to their domestic inventories of infringing products, and that those inventory levels are commercially significant, citing e.g., Order No. 49, Exhibit A at ¶ 6{

} and Order Nos. 44 and 45. Thus, the staff argued that cease

and desist orders also would be an appropriate recommendation as to each of the respondents.

Respondents argued that the record demonstrates that no finding of a violation of § 337 is warranted in this investigation, and hence neither a limited exclusion order nor any cease-and-desist order should be recommended. It is further argued that in the event a finding of violation of § 337 is made, it is clear that neither an exclusion order nor a cease-and-desist order is warranted under the prevailing facts and circumstances, relying on Certain Erasable Programmable Read-Only Memories Components Thereof Products Containing Such Memories, and Processes For Making Such Memories (EPROMs), Inv. No. 337-TA-276, Comm'n Op. (May 1989), USITC Pub. 2196 aff'd sub nom. Hyundai Elec. Indus. Co. v. U.S. Intl trade Comm'n, 899 F.2d 1204 (Fed. Cir. 1990) (EPROMs).

The Commission has broad discretion in selecting the form, scope, and extent of a remedy in Section 337 proceedings. Certain Integrated Circuit Telecommunication Chips, Inv. No. 337-TA-337, Comm'n Op. at 21 (August 3, 1993). Pursuant to its statutory authority found at 19 U.S.C. § 1337 (d), the Commission may exclude from importation goods and products that form the basis for a finding of a violation of Section 337 which includes products that have been found to infringe the patents-in-suit directly, contributorily or by inducement after importation has occurred. 19 U.S.C. § 1337(d); Certain Flash Memory Circuits, Inv. No. 337-TA-382, Comm'n Op. at 26 (June 26, 1997) ("The Commission has the authority to enter an exclusion order, a cease and desist order, or both."). Indeed, absent special circumstances, the statute requires such exclusion:

> If the Commission determines ... that there is a violation of this section, it shall direct that the articles concerned ...be excluded from entry into the United States, unless, after considering the public health and welfare, competitive conditions in the United States economy, the production of like or directly competitive articles in the United States, and United States consumers, it finds

that such articles should not be excluded from entry.

19 U.S.C. § 1337(d). Hence, a remedy excluding respondents' infringing products from entry is mandatory if a violation of Section 337 is found, unless the Commission finds that public interest factors militate against such remedy.

Section 337(f) also permits the Commission to issue, in lieu of, or in addition to, an exclusion order, a cease and desist order directing persons found to have violated Section 337 to cease and desist from engaging in the unfair methods or acts involved. 19 U.S.C. § 1337(f). Cease and desist orders are warranted with respect to respondents that maintain commercially significant U.S. inventories of the infringing product. See, e.g., Certain Crystalline Cefadroxil Monohydrate, Inv. No. 337-TA-293, USITC Pub. 2391 at 37-42 (June 1991). The Commission has the authority to issue cease and desist orders where a respondent has a sufficient inventory of infringing goods in the United States. Certain NAND Flash Memory Circuits, Inv. No. 337-TA-526, 2005 ITC Lexis 859, Init. Determ. at *255 (Oct. 19, 2005) (citing Certain Plastic Encapsulated Integrated Circuits, Inv. No. 337-TA-315, U.S.I.T.C. Pub. No. 2574, Comm'n Op. at 37 (November 1992)).

Cease and desist orders are directed at a specific respondent in order to prevent the sale, distribution and other use of products that have already been imported into the United States prior to the entry and implementation of any exclusion order. Certain Curable Fluoroelastomer Compositions, Inv. No. 337-TA-364, Notice of Issuance of Limited Exclusion Order and Cease and Desist Order, 1995 WL 1049682 (Mar. 16, 1995). Cease and desist orders can preclude any activity "reasonably related to the importation of infringing products." Certain Hardware Logic Emulation Systems, Inv. No. 337-TA-383, Comm'n. Op. on Remedy, the Public Interest, and Bonding, 1998 WL 307240 (Feb. 28, 1998). Typical cease and desist orders enjoin a respondent

from selling, marketing, distributing and advertising its infringing products, as well as any solicitation of U.S. agents and distributors for the purpose of selling, marketing, distributing, and advertising infringing products. See Certain Electrical Connectors and Products Containing Same, Inv. No. 337-TA-374, Comm'n Cease and Desist Order, 1996 WL 1056313 (May 3, 1996).

At the outset, in issue is whether the requested relief is amenable to an EPROMs analysis. The Commission, in EPROMs, Comm'n Op. at 124-26, 136 identified the following relevant factors to be considered in determining whether an exclusion order should extend to downstream products:

> (1) the value of the infringing articles compared to the value of the downstream products in which they are incorporated;
>
> (2) the identity of the manufacturer of the downstream products, i.e., whether it can be determined that the downstream products are manufactured by the respondent or by a third party;
>
> (3) the incremental value to the complainant of the exclusion of downstream products;
>
> (4) the incremental detriment to respondents of exclusion of such products;
>
> (5) the burdens imposed on third parties resulting from exclusion of downstream products;
>
> (6) the availability of alternative downstream products that do not contain the infringing articles;
>
> (7) the likelihood that the downstream products actually contain the infringing articles and are thereby subject to exclusion;
>
> (8) the opportunity for evasion of an exclusion order that does not include downstream products; and
>
> (9) the enforceability of an order by Customs; and any other factors the Commission determines to be relevant.

See also Certain Liquid Crystal Display Modules, Products Containing Same, and Methods Using the Same, Inv. No. 337-TA-634, Comm. Op. at 4 (Nov. 24, 2009) (adopting Judge's analysis of EPROMs factors).

Complainant Freescale contended that its requested relief is not amendable to an EPROMs analysis. (CBr at 130.) The staff disagrees. (SRBr at 6.) Respondents argued that the EPROMs factors are appropriately applied in this investigation and while complainant addressed the EPROMs factors, the factors weigh against an exclusion order. (RRBr at 120-22.)

The administrative law judge finds that complainant Freescale's requested relief for an exclusion order is amendable to an EPROMs analysis. As the Commission stated in EPROMs:

> "[T]he Commission may, in issuing [limited] exclusion orders, . . . balance the complainant's interest in obtaining complete protection from all infringing imports by means of exclusion of downstream products against the inherent potential of even a limited exclusion order, when extended to downstream products, to disrupt legitimate trade in products which were not themselves the subject of a finding of violation of section 337."

EPROMs, Comm'n Op. at 125. As is clear from said quote, the point of an EPROMs analysis is to balance a complainant's interest in obtaining relief from all infringing imports against the disruption of legitimate trade in products not themselves the subject of a finding of violation of section 337. Thus, if respondents Funai manufactured or imported into the United States automobiles that incorporated the Zoran ICs, it is certainly questionable whether Freescale could obtain an order excluding those Funai automobiles because those automobiles "were not themselves the subject of a finding of violation of section 337," and the administrative law judge sees a big difference between automobiles and televisions and the importation on the one hand of automobiles and on the other hand televisions. There is certainly a large price differential. On the other hand, with regard to the Funai televisions that were the subject of this investigation and

which do incorporate the Zoran ICs, the administrative law judge finds no plausible argument that exclusion of those televisions would "disrupt legitimate trade." Also while complainant argued that the products that it seeks to be excluded are not "downstream products" but are Funai's "own infringing products" (CBr at 129) case law indicates that products containing an allegedly infringing product are "downstream" products. See Kyocera Wireless Corp. v. Int'l Trade Comm'n, 545 F.3d 1340, 1358 (Fed. Cir. 2008); see also Hyundai Elecs. Indus. Co. v. United States ITC, 899 F.2d 1204, 1206 (Fed. Cir. 1990).

Referring to the EPROMs factors and regarding the first EPROMs factor, viz. the value of infringing articles compared to the value of downstream products, while there is no evidence that the infringing Zoran integrated circuits per se are imported,{

} Funai televisions that are imported. As complainant's expert Subramanian testified:

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}

{

}

(Tr. at 170, 195-96, 269-70 (emphasis added).)

Respondents argued that the complaint did not accuse Zoran integrated circuits or products containing Zoran integrated circuits of infringing any patent owned by Freescale, and Zoran integrated circuits were not mentioned at any point in the complaint. (RFF 2.) However, contrary to respondents' argument, the administrative law judge and the Commission in this investigation decided on multiple occasions that Funai products containing Zoran integrated circuits were within the scope of accused products described in Freescale's initial complaint. (See Order No. 8; Order No. 10; Order No. 11; Order No. 12; Order No. 13; Aug. 8, 2010 Notice Of Comm'n Det. Not to Review Init. Determ'n Granting Motion to Amend Complaint.) In addition, in response to Freescale's motion which resulted in Order No. 8, Funai had argued that the scope of this investigation is limited exclusively to ICs manufactured by Panasonic. (Order No. 8 at 3-5.) Also in Order No. 8, the administrative law judge rejected Funai's argument and compelled Funai to provide discovery on all of its accused products, including those that contain ICs manufactured by parties other than Panasonic. (Order No. 8 at 10-16 (ordering Funai to "respond to Freescale ... with respect to all products that Funai sells for importation, imports, or sells after importation

within the United States that contain an accused integrated circuit, regardless of the manufacturer of said integrated circuit").) In addition, respondents moved on June 25, 2010 to amend or clarify the notice of investigation to exclude, inter alia, Funai products containing non-Panasonic ICs from the scope of accused products. (Order No. 11 at 1-2.) In denying that motion in Order No. 11, the administrative law judge noted that the same issue was considered, and expressly rejected, in Order No. 8. (Order No. 11 at 5-6 ("Significantly, the administrative law judge found (in Order No. 8) that, contrary to Panasonic, Funai, and JVC's assertion, the 'integrated circuits' and 'chipsets' at issue in this investigation are not limited to those manufactured by Panasonic." and "[a]ccordingly, the administrative law judge found that Panasonic, Funai, and JVC's products fall within the scope of this investigation and a limited exclusion order in this investigation may properly cover said products, regardless of who is the manufacturer of the accused integrated circuit contained within such products.").) On July 16, 2010 respondents filed a motion for interlocutory review of Order No. 11 which motion for interlocutory review was denied. (Order No. 12.) On July 16, 2010, respondents filed a petition for Commission review of Order No. 10's initial determination granting Freescale's motion to amend the complaint. (See Order No. 13 at 1 (describing respondents' motion to stay pending Commission review of Order No. 10).) The Commission denied respondents' petition to review Order No. 10. (Aug. 8, 2010 Notice Comm'n Det. Not to Review Init. Determ'n Granting Motion to Amend Complaint.) Thus the administrative law judge rejects respondents' argument that Zoran integrated circuits or products containing said circuits are not in issue in this investigation and further finds that EPROMs factor 1 supports exclusion of Funai's downstream products.

Regarding EPROMs factor 2, viz. the identity of the manufacturer of the downstream products, i.e., whether it can be determined that the downstream products are manufactured by

the respondents or by a third party, the administrative law judge finds that it supports exclusion of Funai's downstream products because the Funai respondents are named respondents and import televisions.

Regarding EPROMs factor 3, viz. the incremental value to the complainant of the exclusion of downstream products, and factor 8, viz. the opportunity for evasion of an exclusion order that does not include downstream products, the administrative law judge finds that said factors support exclusion because if Funai's products are not excluded, Freescale would be denied any effective relief, as there is no evidence that the Funai respondents import infringing integrated circuits by themselves. As for factor 5, viz. the burdens imposed on third parties resulting from exclusion of downstream products, he finds that the burden would be non-existent because the order excluding Funai's downstream products would apply only to respondents Funai, not to any third-party. Referring to factor 6, viz. the availability of alternative downstream products that do not contain the infringing articles, said factor is also found to support exclusion of said Funai's downstream products because Freescale has licensed the '455 patent to several entities, including Panasonic, who can import their products irrespective of any exclusion order that may issue against Funai's products.

As for factor 7, viz. the likelihood that the downstream products actually contain the infringing article and are thus subject to exclusion, identification of the Funai products that contain the infringing chips can be done. Thus at the hearing, complainant's expert Subamanian testified as to the specific Funai products that contain the infringing chips referring to CX-122C, pages 9 and 10. Also Funai has stipulated that "the brand names listed in [CX-80C, CX-122C, and CX-164C] are the names used on packaging or crates of the products listed in response to those interrogatories during importation into the United States." (CPFF 1190 (undisputed).)

Additionally, there is no evidence that such products are assembled in the United States. (CPFF 1191 (undisputed).)

Referring to factor 9, viz. the enforceability of an order by Customs with respect to the Funai products that incorporate infringing chips, the infringing chips are found in specific products produced by Funai. (Subramanian, Tr. at 169-173.) Also as found supra, Funai has stipulated that the brand names listed in CX-80C, CX-122C, and CX-164C are the names used on packaging or crates of the products listed in response to those interrogatories during importation into the United States. Thus Customs can identify the Funai televisions based on said brand names.

Referring to the foregoing and based on the EPROMs factors, the administrative law judge finds that a limited exclusion order directed to respondents' products that incorporate the infringing integrated circuits would be appropriate.

With regard to any cease and desist order, respondents Funai have stipulated that {

} after they had been imported, sold for importation, or sold after importation into the United States. (Order No. 49, Exhibit A at ¶¶ 5-6.) Thus the administrative law judge recommends appropriate cease and desist orders be issued against the respondents.

XII. Bond

Complainant argued that the Commission should require a 100% bond. (CBr at 139-44.)

Respondents argued that no bond should be imposed during any Presidential period and that complainant apparently is under the "misimpression that no evidence on bonding is necessary and that a 100% bond is essentially automatic." (RBr at 130-31.)

The staff argued that it appears that complainant Freescale did not pursue evidence

regarding the pricing of respondents' accused products, that notwithstanding complainant's decision not to seek said information from respondents, Freescale seeks a bond in the amount of 100% of the entered value of any infringing product; that in light of Freescale's failure to pursue relevant discovery on the issue of what constitutes an appropriate bond, it has failed to carry its burden of proving that a 100% bond should be imposed, citing Certain Rubber Antidegradants, Components Thereof, and Products Containing Same, Inv. No. 337-TA-533, Comm'n Op., 2006 ITC LEXIS 591, at *59 (July 21, 2006); that in addition Freescale has not shown that it is entitled to a bond of 100% of entered value, at least because there is evidence that tends to establish a reasonable royalty, citing Certain Stringed Musical Instruments and Components Thereof, Inv. No. 337-TA-586, Final Initial and Recommended Determination, 2007 ITC LEXIS 1226, at *47-48 & n.116 (Dec. 3, 2007) (reviewed on other grounds); and that none of said evidence (in the form of license agreements) was presented or admitted at the evidentiary hearing. Thus, the staff argued that no bond should be imposed.

Section 337(j)(3) provides for the entry of infringing articles upon the payment of a bond during the sixty-day Presidential review period. 19 U.S.C. § 1337(j)(3). Any bond is to be set at a level sufficient to "offset any competitive advantage resulting from the unfair method of competition or unfair act enjoyed by persons benefiting from the importation." Certain Dynamic Random Access Memories, Components Thereof and Products Containing Same, Inv. No. 337-TA-242, Commission Opinion on Violation, Remedy, Bonding and the Public Interest, USITC Pub. No. 2034, 1987 WL 450856 (U.S.I.T.C.) at 38 (1987). When reliable price information is available, the Commission has set a bond by eliminating the price differential between the domestic and the imported infringing product. Certain Digital Satellite System (DSS) Receivers and Components Thereof, Inv. No. 337-TA-392, Final Initial and

Recommended Determination on Remedy and Bonding, U.S.I.T.C. Pub. No. 3418, 2001 WL 535427 (U.S.I.T.C.) at 336 (April 2001). Where reliable price information is not available, Commission precedent establishes that the bond should be set at 100%. Certain Semiconductor Memory Devices and Products Containing Same, ITC Inv. No. 337-TA-414, Recommended Determination on Remedy and Bonding, 1999 WL 1267282 (U.S.I.T.C.) at 6 (December 13, 1999).

While complainant Freescale has argued that it has "identified a wide range of products that infringe the '455 patent, and a wide range of prices for these products"(CRBr at 103), a bond set at 100% is levied only when reliable price information is not available. See Certain Flash Memory Circuits and Products Containing Same, Inv. No. 337-TA-382, USITC Pub. No. 3046, Comm'n Op. at 26-27 (July 1997) (100% bond imposed only when price comparison was not practical because the parties sold products at different levels of commerce, and the proposed royalty rate appeared to be de minimis and without adequate support in the record.). However there are indications that reliable price information may have been available to complainant Freescale. For example, and merely as an illustration, as recited in the Procedural History, supra, Order No. 50 terminated the investigation as to certain respondents based on a settlement agreement and licensing agreement relating to each of the '306 patent, the '014 patent and certain claims of the '455 patent. Complainant, in arguing for a 100% bond and in spite of said licensing agreement, made no attempt to argue that any such licensing agreement would not establish a reasonable royalty for claims 9 and 10 of the '455 patent.

Based on the foregoing, the administrative law judge denies complainant's request for a bond set at 100% and further recommends that no bond be set.

XIII. Additional Findings

1. Complainant Freescale Semiconductor, Inc. (Freescale) is a Delaware corporation with its headquarters located at 6501 William Cannon Drive West, Austin, Texas. (Sept. 14, 2010 2nd Amd. Complaint at ¶ 5.)

2. Freescale was formed in 2004 as a result of the divestiture of the Semiconductor Products Sector of Motorola, Inc. (Sept. 14, 2010 2nd Amd. Complaint at ¶ 5.)

3. Respondent Funai Electric Co., Ltd. is a corporation organized under the laws of Japan, and maintains its principal place of business in Daito, Osaka, Japan. (Sept. 14, 2010 2nd Amd. Complaint at ¶ 62-69.)

4. Respondent Funai Electric Co., Ltd. is the world-wide parent corporation for Funai entities. (Sept. 14, 2010 2nd Amd. Complaint at ¶ 62-69.)

5. Respondent Funai Corporation, Inc. is a corporation organized under the laws of New Jersey, and maintains its principal place of business at 201 Route 17, Ste 903, Rutherford, New Jersey 07070. (Sept. 14, 2010 2nd Amd. Complaint at ¶ 62-69.)

6. Respondent Best Buy Purchasing, LLC is a Minnesota limited liability company having its principal place of business at 7601 Penn Avenue S., Richfield, Minnesota 55423. (Sept. 14, 2010 2nd Amd. Complaint at ¶ 90-95.)

7. Respondent Best Buy.Com, LLC is a Virginia limited liability company with its principal place of business at 7601 Penn Avenue S., Richfield, Minnesota 55423. (Sept. 14, 2010 2nd Amd. Complaint at ¶ 90-95.)

8. Respondent Best Buy Stores, L.P. is a Virginia limited partnership with its principal place of business at 7601 Penn Avenue S., Richfield, Minnesota 55423.

(Sept. 14, 2010 2nd Amd. Complaint at ¶ 90-95.)

9. Respondent Wal-Mart Stores, Inc. is a Delaware corporation having its principal place of business at 708 SW 8th Street, Bentonville, Arkansas 72716. (Sept. 14, 2010 2nd Amd. Complaint at ¶ 100-102.)

CONCLUSIONS OF LAW

1. The Commission has in personam and in rem jurisdiction.

2. There has been an importation of accused integrated circuits, chipsets, and products containing same including televisions, media players, and cameras into the United States which are the subject of the unfair trade allegations.

3. It has not been established that claims 9 and 10 of the '455 patent are invalid.

4. Complainant has failed to show that asserted claims 9 and 10 of the '455 patent are infringed.

5. Complainant has established a domestic industry.

6. The evidence establishes that there is no violation of section 337.

7. In the event a violation of section 337 is found, limited exclusion orders and cease and desist orders are recommended. However no bond is recommended.

ORDER

Based on the foregoing, and the record as a whole, it is the administrative law judge's Final Initial Determination that there is no violation of section 337 in the importation into the United States, sale for importation, and sale within the United States after importation of integrated circuits, chipsets, and products containing same including televisions, media players, and cameras. It is also the administrative law judge's recommendation, should a violation be found, that limited exclusion orders issue barring entry into the United States of infringing integrated circuits, chipsets, and products containing same including televisions, media players, and cameras and that appropriate cease and desist orders should issue. The administrative law judge does not recommend any bond.

The administrative law judge hereby CERTIFIES to the Commission his Final Initial and Recommended Determinations. The briefs of the parties, filed with the Secretary, are not certified, since they are already in the Commission's possession in accordance with Commission rules.

Further it is ORDERED that:

1. In accordance with Commission rule 210.39, all material heretofore marked in camera because of business, financial and marketing data found by the administrative law judge to be cognizable as confidential business information under Commission rule 201.6(a), is to be given in camera treatment continuing after the date this investigation is terminated.

2. Counsel for the parties shall have in the hands of the administrative law judge those portions of the final initial and recommended determinations which contain bracketed confidential business information to be deleted from any public version of said determinations, no later than April 18, 2011. Any such bracketed version shall not be served via facsimile on the administrative law judge. If no such bracketed version is received from a party, it will mean that the party has no objection to removing the confidential status, in its entirety, from these initial and recommended determinations.

3. The initial determination portion of the Final Initial and Recommended Determinations, issued pursuant to Commission rules 210.42(a) and 210.42-46, shall become the determination of the Commission, unless the Commission, shall have ordered its review of certain issues therein or by order has changed the effective date of the initial determination portion. The recommended determination portion, issued pursuant to Commission rule

210.42(a)(1)(ii), will be considered by the Commission in reaching a determination on remedy pursuant to Commission rule 210.50(a).

Paul J. Luckern
Chief Administrative Law Judge

Issued: April 4, 2011

CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS, MEDIA PLAYERS, AND CAMERAS **337-TA-709**

PUBLIC CERTIFICATE OF SERVICE

I, James R. Holbein, hereby certify that the attached **Public Version Final Initial and Recommended Determinations** has been served by hand upon the Office of Unfair Import Investigations, and the following parties as indicated, on

May 12, 2011.

James R. Holbein, Acting Secretary
U.S. International Trade Commission
500 E Street, SW
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Complainant Freescale Semiconductor, Inc.:

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