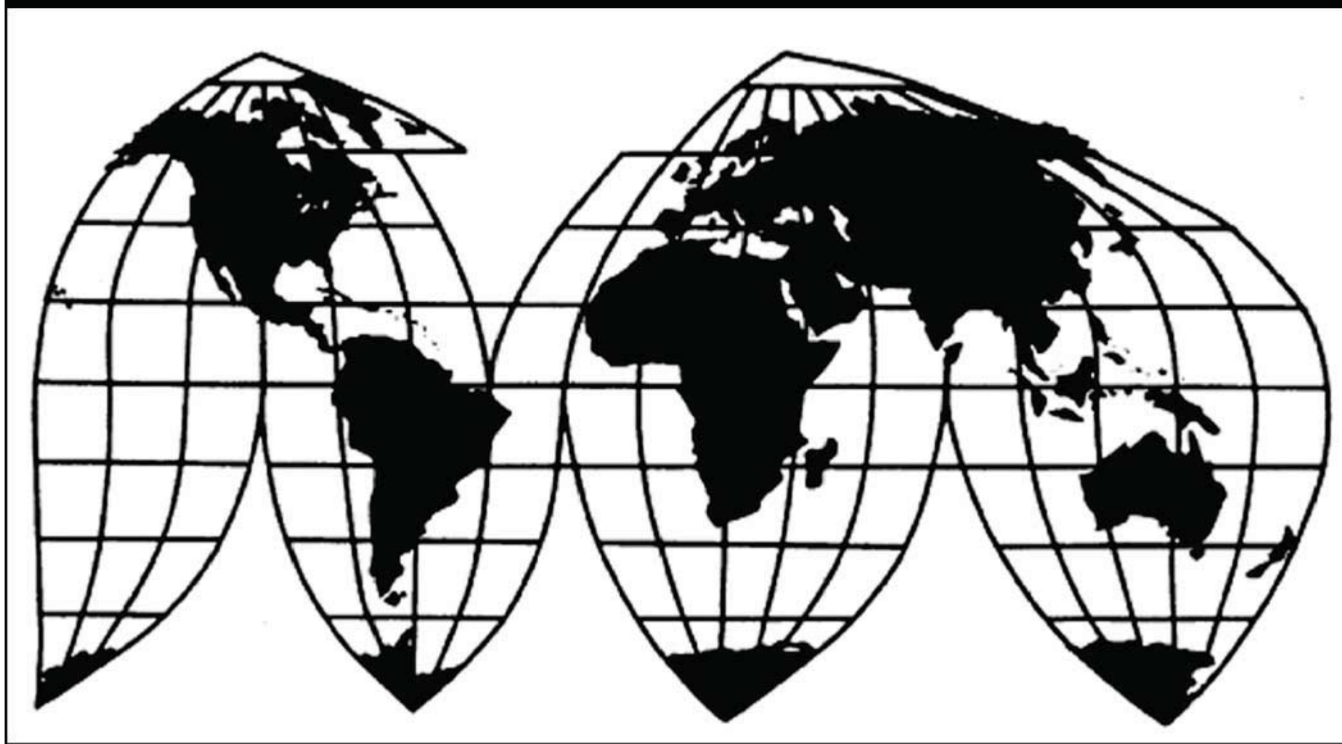
In the Matter of

Certain Semiconductor Chips with Minimized Chip Package Size and Products Containing Same (III)

Investigation No. 337-TA-630

Publication 4209 **December 2010**

U.S. International Trade Commission



Washington, DC 20436

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U.S. International Trade Commission

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Daniel R. Pearson, Vice Chairman
Deanna Tanner Okun
Charlotte R. Lane
Irving A. Williamson
Dean A. Pinkert

Address all communications to
Secretary to the Commission
United States International Trade Commission
Washington, DC 20436

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Publication 4209 **December 2010**

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C. 20436

In the Matter of **CERTAIN SEMICONDUCTOR CHIPS WITH MINIMIZED CHIP PACKAGE SIZE AND PRODUCTS CONTAINING SAME (III)**	**Investigation No. 337-TA-630**

NOTICE OF THE COMMISSION'S FINAL DETERMINATION OF NO VIOLATION OF SECTION 337; TERMINATION OF THE INVESTIGATION

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has determined that there has been no violation of section 337 of the Tariff Act of 1930, 19 U.S.C. § 1337, in this investigation, and has terminated the investigation.

FOR FURTHER INFORMATION CONTACT: Panyin A. Hughes, Esq., Office of the General Counsel, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 205-3042. Copies of non-confidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 205-2000. General information concerning the Commission may also be obtained by accessing its Internet server at _http://www.usitc.gov_. The public record for this investigation may be viewed on the Commission's electronic docket (EDIS) at _http://edis.usitc.gov_. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on (202) 205-1810.

SUPPLEMENTARY INFORMATION: This investigation was instituted on January 14, 2008, based on a complaint filed by Tessera, Inc. of San Jose, California ("Tessera") on December 21, 2007, and supplemented on December 28, 2007. 73 *Fed. Reg.* 2276 (Jan. 14, 2008). The complaint alleged violations of section 337 of the Tariff Act of 1930 (19 U.S.C. § 1337) in the importation into the United States, the sale for importation, and the sale within the United States after importation of certain semiconductor chips with minimized chip package size or products containing the same by reason of infringement of various claims of United States Patent Nos. 5,663,106 ("the '106 patent"); 5,679,977 ("the '977 patent"); 6,133,627 ("the '627 patent"); and 6,458,681 ("the '681 patent"). The complaint named eighteen respondents. Several respondents were terminated from the investigation based on settlement agreements and consent orders. Two respondents defaulted. The following respondents remain in the investigation: Acer Inc. of

Taipei, Taiwan; Acer America Corp. of San Jose, CA; Centon Electronics, Inc. of Aliso Viejo, CA; Elpida Memory, Inc. of Tokyo, Japan and Elpida Memory (USA), Inc. of Sunnyvale, CA (collectively, "Elpida"); Kingston Technology Co., Inc. of Fountain Valley, CA; Nanya Technology Corporation of Taoyuan, Taiwan; Nanya Technology Corp. USA of San Jose, CA; Powerchip Semiconductor Corporation of Hsinchu, Taiwan; ProMOS Technologies, Inc. of Hsinchu, Taiwan; Ramaxel Technology Ltd. of Hong Kong, China; and SMART Modular Technologies, Inc. of Fremont, CA. The '681 patent was terminated from the investigation prior to the hearing.

On August 28, 2009, the Administrative Law Judge ("ALJ") issued his final Initial Determination ("ID"), finding no violation of section 337 by Respondents with respect to any of the asserted claims of the asserted patents. Specifically, the ALJ found that the accused products do not infringe the asserted claims of the '106 patent. The ALJ also found that none of the cited references anticipates the asserted claims and that none of the cited references renders the asserted claims obvious. The ALJ further found that the asserted claims of the '106 patent satisfy the requirement of 35 U.S.C. § 112, first, second and fourth paragraphs. Likewise, the ALJ found that the accused products do not infringe the asserted claims of the '977 and '627 patents and that none of the cited references anticipates the asserted claims of the patents. The ALJ further found that the asserted claims of the '977 and '627 patents satisfy the definiteness requirement of 35 U.S.C. § 112, second paragraph, and that Respondents waived their argument with respect to obviousness. The ALJ also found that all chips Respondents purchased from Tessera licensees were authorized to be sold by Tessera and, thus, Tessera's rights in those chips became subject to exhaustion, but that Respondents, except Elpida, did not purchase all their chips from Tessera licensees.

On September 17, 2009, Tessera and the Commission investigative attorney filed petitions for review of the ID. That same day, Respondents filed contingent petitions for review of the ID. On October 1, 2009, the parties filed responses to the various petitions and contingent petitions for review.

On October 30, 2009, the Commission determined to review the final ID in part and requested briefing on several issues it determined to review, and on remedy, the public interest and bonding. 74 *Fed. Reg.* 57192 (Nov. 4, 2009). The Commission determined to review (1) the finding that the claim term "top layer" recited in claim 1 of the '106 patent means "an outer layer of the chip assembly upon which the terminals are fixed," the requirement that "the 'top layer' is a single layer," and the effect of the findings on the infringement analysis, invalidity analysis and domestic industry analysis; (2) the finding that the claim term "thereon" recited in claim 1 of the '106 patent requires "disposing the terminals on the top surface of the top layer," and its effect on the infringement analysis, invalidity analysis and domestic industry analysis; (3) the finding that the Direct Loading testing methodology employed by Tessera's expert to prove infringement is unreliable; and (4) the finding that the 1989 Motorola OMPAC 68-pin chip package fails to anticipate claims 17 and 18 of the '977 patent. *Id.*

On November 13, 2009, the parties filed written submissions on the issues under review, remedy, the public interest, and bonding. On November 20, 2009, the parties filed response submissions on the issues on review, remedy, the public interest and bonding.

Having examined the record of this investigation, including the ALJ's final ID, the Commission has determined that there is no violation of section 337. Specifically, the Commission has determined to (1) modify the ALJ's construction of the claim terms "top layer" and "thereon" recited in claim 1 of the '106 patent; (2) reverse the ALJ's finding that the accused μBGA products do not meet all of the limitations of the asserted claims of the '106 patent but affirm his finding that there is no infringement due to patent exhaustion; (3) affirm the ALJ's finding that the accused wBGA products do not infringe the asserted claims of the '106 patent; (4) affirm the ALJ's validity and domestic industry analyses pertaining to the asserted claims of the '106 patent; (5) affirm the ALJ's finding that the Direct Loading testing methodology employed by Tessera's expert fails to prove infringement; and (6) affirm the ALJ's finding that the 1989 Motorola OMPAC 68-pin chip package fails to anticipate claims 17 and 18 of the '977 patent under the on-sale bar provision of 35 U.S.C. § 102(b), but modify a portion of the ID.

The authority for the Commission's determination is contained in section 337 of the Tariff Act of 1930, as amended (19 U.S.C. § 1337), and in sections 210.42-46 of the Commission's Rules of Practice and Procedure (19 C.F.R. §§ 210.42-46).

By order of the Commission.

Marilyn R. Abbott
Secretary to the Commission

Issued: December 29, 2009

CERTAIN SEMICONDUCTOR CHIPS WITH MINIMIZED CHIP PACKAGE SIZE AND PRODUCTS CONTAINING SAME (III) **337-TA-630**

PUBLIC CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the attached **NOTICE OF COMMISSION'S FINAL DETERMINATION OF NO VIOLATION OF SECTION 337; TERMINATION OF THE INVESTIGATION** has been served by hand upon the Commission Investigative Attorney, Kecia J. Reynolds, Esq., and the following parties as indicated, on December 29, 2009.

Marilyn R. Abbott, Secretary
U.S. International Trade Commission
500 E Street, SW
Washington, DC 20436

On Behalf Of Complainant Tessera Incorporated:

Tom M. Schaumberg, Esq.
ADDUCI, MASTRIANI, SCHAUMBERG, LLP
1200 Seventeenth St., NW
Washington, DC 20036

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: ________

On Behalf Of Respondents Acer, Incorporated, Acer America Corporation, Nanya Technology Corporation, Nanya Technology Corporation USA, And Powerchip Semiconductor Corporation:

G. Hopkins Guy, Esq.
ORRICK HERRINGTON & SUTCLIFFE LLP
1000 Marsh Road
Menlo Park, CA 94025-1015

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: ________

On Behalf Of Respondents Kingston Technology Co., Incorporated:

Alan L. Unikel, Esq.
SEYFARTH SHAW LLP
131 South Dearborn Street, Suite 2400
Chicago, IL 60603

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: _________

On Behalf Of Respondents Elpida Memory Inc., And Elpida Memory (USA) Incorporated:

Larry L. Shatzer, Esq.
FOLEY & LARDNER LLP
Washington Harbour
3000 K Street, NW, Suite 600
Washington, DC 20007-5143

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: _________

On Behalf Of Respondent Smart Modular Technologies, Incorporated:

Jonathan M. James, Esq.
PERKINS COIE
2901 N. Central Avenue, Suite 2000
Phoenix, AZ 85012-2788

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: _________

On Behalf Of Respondent Centon Electronics, Incorporated:

Joseph P. DiVincenzo, Esq.
REMER DIVINCENZO & GRIFFITH
2121 E. Pacific Coast Highway, Suite 280
Corona Del Mar, CA 92625

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: _________

On Behalf Of Respondent Ramaxel Technology Ltd.:

Brian R. Nester, Esq.
FISH & RICHARDSON PC
1425 K Street, NW, 11th Floor
Washington, DC 20005

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: _________

On Behalf Of Respondent Promos Technologies Inc.:

Charles F. Gormly, Esq.
5101 Wisconsin Avenue NW, Suite 210
Washington, DC 20016

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: _________

PUBLIC VERSION

United States International Trade Commission
Washington, DC 20436

In the Matter of

CERTAIN SEMICONDUCTOR CHIPS WITH MINIMIZED CHIP PACKAGE SIZE AND PRODUCTS CONTAINING SAME (III)

Investigation No. 337-TA-630

COMMISSION OPINION

This investigation is before the Commission for a final disposition. The Commission has determined to affirm the presiding administrative law judge's ("ALJ") determination that Respondents did not violate section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, in connection with claims 1-4, 9, 10 and 33-35 of United States Patent No. 5,663,106 ("the '106 patent"), claims 17 and 18 of United States Patent No. 5,679,977 ("the '977 patent") and claims 1-4, 9-12, 15 and 16 of United States Patent No. 6,133,627 ("the '627 patent"). Specifically, the Commission has determined to (1) modify the ALJ's construction of the claim terms "top layer" and "thereon" recited in claim 1 of the '106 patent; (2) reverse the ALJ's finding that the accused μBGA products do not meet all of the limitations of the asserted claims of the '106 patent but affirm his finding that there is no infringement due to patent exhaustion for these products; (3) affirm the ALJ's finding that the accused wBGA products do not infringe the asserted claims of the '106 patent; (4) affirm the ALJ's validity and domestic industry analyses pertaining to the asserted claims of the '106 patent; (5) affirm the ALJ's finding that the Direct Loading testing methodology employed by Complainant's expert fails to prove infringement; and (6) affirm the ALJ's finding that the 1989 Motorola OMPAC 68-pin chip package fails to anticipate claims 17

and 18 of the '977 patent under the on-sale bar provision of 35 U.S.C. § 102(b), but modify a portion of the ALJ's final initial determination ("ID"). This opinion sets forth the Commission's reasoning underlying its determinations. The Commission adopts the ALJ's ID to the extent it is not inconsistent with this opinion.

I. BACKGROUND

A. Procedural History

The Commission instituted this investigation on January 14, 2008, based on a complaint filed by Tessera, Inc. of San Jose, California ("Tessera"). 73 *Fed. Reg.* 2276 (Jan. 14, 2008). The complaint alleged violations of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain semiconductor chips with minimized chip package size and products containing the same by reason of infringement of claims 1-4, 9, 10 and 33-35 of the '106 patent; claims 17 and 18 of the '977 patent; claims 1-4, 6, 9-12, 15 and 16 of the '627 patent; and claim 4 of United States Patent No. 6,458,681 ("the '681 patent"). Tessera named eighteen respondents.

On May 29, 2008, the ALJ[1] granted Tessera's motion to terminate the '681 patent from the investigation. *See* Order No. 16. On June 20, 2008, the Commission determined not to review the order. *See* Notice of Commission Determination Not to Review an Initial Determination Granting Complainant's Motion for Partial Termination of the Investigation with Respect to

[1] The investigation was originally assigned to Judge Bullock. On July 11, 2008, the investigation was reassigned to Judge Essex. *See* Notice of Commission Decision to Reassign Certain Section 337 Investigations.

United States Patent No. 6,458,681.

After the termination of several respondents based on settlement agreements, consent orders and defaults,[2] the following groups of respondents remained in the investigation:

1. Acer Inc. of Taipei, Taiwan; and Acer America Corp. of San Jose, CA (collectively, "Acer");
2. Centon Electronics, Inc. of Aliso Viejo, CA ("Centon");
3. Elpida Memory, Inc. of Tokyo, Japan; and Elpida Memory (USA), Inc. of Sunnyvale, CA (collectively, "Elpida");
4. Kingston Technology Co., Inc. of Fountain Valley, CA ("Kingston");
5. Nanya Technology Corporation of Taoyuan, Taiwan; and Nanya Technology Corp. USA of San Jose, CA (collectively, "Nanya");
6. Powerchip Semiconductor Corporation of Hsinchu, Taiwan ("Powerchip");
7. ProMOS Technologies, Inc. of Hsinchu, Taiwan ("ProMOS");
8. Ramaxel Technology Ltd of Hong Kong, China ("Ramaxel"); and
9. SMART Modular Technologies, Inc. of Fremont, CA ("SMART").

The ALJ held an evidentiary hearing from September 19, 2008, to October 3, 2008, and thereafter received post-hearing briefing from the parties. During the hearing, the ALJ granted Tessera's motion to withdraw claim 6 of the '627 patent from the investigation. Hearing Tr. at

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[2] The investigation was terminated as to respondents International Sourcing Group, Inc. (Order No. 17), Peripheral Devices and Product Systems d/b/a Patriot Memory (Order No. 25), and A-Data Technology Co., Ltd., and A-Data Technology (USA) Co. (Order No. 35) based on consent orders and/or settlement agreements. *See* Notice of Commission Determination Not to Review an Initial Determination Granting Joint Motion to Terminate Investigation as to One Respondent Based on Consent Order and Settlement Agreement (July 14, 2008); Notice Of Commission Determination Not To Review an Initial Determination Granting a Joint Motion to Terminate the Investigation as to Respondent Patriot Memory Based on a Consent Order and Settlement Agreement; Issuance Of Consent Order (Oct. 2, 2008); Notice of Commission Determination Not to Review an Initial Determination Granting the Motion of Respondent A-Data Technology Co., Ltd., and A-Data Technology (USA) Co. to Terminate the Investigation as to Them Based on a Consent Order; Issuance of Consent Order (Oct. 23, 2008). TwinMOS Technologies, Inc. and TwinMOS Technologies, USA, Inc. defaulted. *See* Order No 46; Notice of Commission Determination Not to Review an Initial Determination Finding Two Respondents in Default (Sept. 15, 2009).

95:23-25.

On January 30, 2009, the Commission issued its decision to review in part the final initial determination finding no violation of section 337 in a related investigation, Investigation No. 337-TA-605 ("the 605 Investigation"). *See* Notice of Commission Decision to Review in Part a Final Initial Determination Finding No Violation of Section 337. The '977 and '627 patents and the patents that were asserted in the 605 Investigation, U.S. Patent Nos. 5,852,326 and 6,433,419, belong to the same family of patents and name identical inventors. In addition, Tessera, the complainant in this investigation, was also the complainant in the 605 Investigation and relied on the same testing methodology employed by the same expert, Dr. Qu, to prove infringement in both investigations. Because of the Commission's decision to review in part the final initial determination in the 605 Investigation, the ALJ extended the target date in this investigation due to the relationship between the patents at issue in both investigations as well as the fact that the Commission was reviewing the methodology used by Tessera in the 605 Investigation, which is the same methodology used in this investigation to prove infringement. *See* Order No. 40. The Commission determined not to review Order No. 40. *See* Notice of Commission Decision Not to Review an Initial Determination Extending the Target Date for Completion of This Investigation.

On April 2, 2009, the ALJ extended the target date in this investigation to November 17, 2009, based on the Commission's decision to request additional briefing on remedy and to extend the target date in the 605 Investigation. *See* Order No. 41. On April 23, 2009, the Commission determined not to review Order No. 41. *See* Notice of Commission Decision Not to Review an

Initial Determination Extending the Target Date for Completion of This Investigation.

On May 20, 2009, the Commission issued its opinion in the 605 Investigation. *See Certain Semiconductor Chips With Minimized Chip Package Size and Products Containing Same,* Inv. No. 337-TA-605, Commission Opinion (May 20, 2009). On June 3, 2009, the Commission issued a public version of its opinion. *See Certain Semiconductor Chips With Minimized Chip Package Size and Products Containing Same,* Inv. No. 337-TA-605, Commission Opinion (Public Version) (May 20, 2009) ("605 Comm'n Op").

On June 12, 2009, the ALJ issued Order No. 43, seeking supplemental briefing on "how the Commission's Opinion in the 605 Investigation and its findings on Dr. Qu's infringement analysis will affect the ALJ's analysis in this investigation, if at all." *See* Order No. 43 at 2. In light of the supplemental briefing, the ALJ extended the target date in this investigation to December 29, 2009, with the final initial determination on violation being due no later than the close of business on August 28, 2009. *See* Order No. 43. On July 13, 2009, the Commission determined not to review Order No. 43. *See* Notice of Commission Determination Not to Review an Initial Determination Extending the Target Date for Completion of the Investigation by Six Weeks.

On August 28, 2009, the ALJ issued his final ID, finding no violation of section 337 by Respondents with respect to any of the asserted claims of the asserted patents. Specifically, the ALJ found that the accused products do not infringe the asserted claims of the '106 patent. ID at 53-54. The ALJ also found that none of the cited references anticipated the asserted claims and

that none of the cited references rendered the asserted claims obvious. ID at 109-116, 132-134. The ALJ further found that the asserted claims of the '106 patent satisfied the requirements of 35 U.S.C. § 112, first, second and fourth paragraphs. ID at 135-136. Likewise, the ALJ found that the accused products do not infringe the asserted claims of the '977 and '627 patents and that none of the cited references anticipated the asserted claims. ID at 79-80, 97, 118-126. The ALJ further found that the asserted claims of the '977 and '627 patents satisfied the definiteness requirement of 35 U.S.C. § 112, second paragraph, and that Respondents waived their argument with respect to obviousness. ID at 134, 136-139. The ALJ also found that all chips Respondents purchased from Tessera licensees were authorized to be sold by Tessera and, thus, Tessera's rights in those chips became subject to exhaustion, but that Respondents, except Elpida, did not purchase all their chips from Tessera licensees. ID at 143-153. The ALJ concluded that an industry existed within the United States with respect to Tessera's products that practiced the '106, '977 and '627 patents, as required by 19 U.S.C. § 1337(a)(2) and (3). ID at 154.

On September 17, 2009, Tessera filed a petition requesting review of the ALJ's construction of claim terms "top layer" and "thereon" recited in independent claim 1 of the '106 patent, the ALJ's finding that the testing methodology employed by its expert to prove infringement is unreliable, and the ALJ's finding that all chips Respondents purchased from Tessera licensees were authorized to be sold by Tessera and thus Tessera's rights in those chips became subject to exhaustion. *See* Complainant Tessera's Petition for Review of Initial Determination on Violation of Section 337 and Recommended Determination on Remedy and

Bond ("Tessera Pet."). That same day, the Commission investigative attorney ("IA") also filed a petition seeking review of the ALJ's construction and application of the claim terms "top layer" and "thereon" recited in claim 1 of the '106 patent as well as the ALJ's finding that the testing methodology employed by Tessera's expert to prove infringement is unreliable. *See* Office of Unfair Import Investigations' Petition for Review of the Initial Determination ("IA Pet."). Also on September 17, 2009, Respondents filed various contingent petitions for review of the ALJ's findings should the Commission decide to review the subject ID. The contingent petitions sought review of the ALJ's construction of claim terms "providing a protective barrier," "terminals" and "above" recited in asserted claim 1 of the '106 patent and the ALJ's findings regarding validity of the asserted claims and the adequacy of Respondents' representative products tested by Tessera for infringement. On October 1, 2009, Tessera, Respondents and the IA filed replies to the petitions for review.

On October 30, 2009, the Commission determined to review the final ID in part and requested briefing on several pertinent issues, and on remedy, the public interest and bonding. 74 *Fed. Reg.* 57192 (Nov. 4, 2009). The Commission determined to review (1) the finding that the claim term "top layer" recited in claim 1 of the '106 patent means "an outer layer of the chip assembly upon which the terminals are fixed," the requirement that "the 'top layer' is a single layer," and the effect of the findings on the infringement analysis, invalidity analysis and domestic industry analysis; (2) the finding that the claim term "thereon" recited in claim 1 of the '106 patent requires "disposing the terminals on the top surface of the top layer," and its effect on the

infringement analysis, invalidity analysis and domestic industry analysis; (3) the finding that the Direct Loading testing methodology employed by Tessera's expert to prove infringement is unreliable; and (4) the finding that the 1989 Motorola OMPAC 68-pin chip package fails to anticipate claims 17 and 18 of the '977 patent. *Id.* The Commission determined not to review the remaining issues decided in the ID. In its notice of review, the Commission asked the parties the following questions:

1. Would the accused products infringe the asserted claims of the '106 patent if construction of the claim term "top layer" does not encompass only a single layer? Please cite record evidence and/or relevant legal precedent to support your position.

2. Did the patentees of the '106 patent expressly disclaim the embodiment described in Figure 7 of United States Patent No. 5,148, 265 ("the '265 patent")? How would that affect the infringement analysis of the asserted claims of the '106 patent? *See* '106 Patent Prosecution History (JX-167) June 24, 1996, Office Action and December 24, 1996, Amendment; '265 patent (JX-2) at column 14, lines 19-34; FIG. 7. Please cite record evidence and relevant legal authority to support your position.

3. Does Dr. Qu state anywhere in the record that he relied on his direct loading testing methodology to independently prove infringement of the asserted claims of the '977 and '627 patents by the accused packages? Please cite only record evidence.

4. Was Dr. Qu's demonstrated stress relief in the solder balls of the accused packages due to terminal-to-chip displacement caused by the applied external load? Please cite only record evidence.

On November 13, 2009, the parties filed written submissions on the issues under review, remedy, the public interest and bonding. *See* Complainant Tessera, Inc.'s Response to Commission Questions on Review of ID ("Tessera Br."); OUII's Response to Notice of

Commission Determination to Review in Part a Final ID Finding No Violation of Section 337 and to Commission Questions ("IA Br."); Response to Commission Review of ID by Respondents Acer, Nanya, and Powerchip ("Resp Br."). On November 20, 2009, the parties filed reply briefs.

B. Patents and Technology at Issue

This investigation involves both semiconductor chip packages and a process for encapsulating certain semiconductor chip packages. ID at 8. The technology at issue in the '977 and '627 patents is generally directed to semiconductor chip packages and specifically to semiconductor chips having ball grid array ("BGA") packages that use solder balls to connect the semiconductor chip to a printed circuit board ("PCB") through an array of tiny solder balls that are arranged in a grid-like pattern under the package. *Id.* The technology at issue in the '106 patent is generally directed to a method of encapsulating small format BGA semiconductor chip packages, including DRAM chip packages. *Id.*

The BGA packages at issue in this investigation are either in the "face-up" or "face-down" orientation. *Id.* The orientation of a chip package is determined based on the orientation of the "face" of the semiconductor chip, which is the surface of the chip that contains the circuitry and contacts for electrical connection. *Id.* In a "face-up" BGA, the face points away from the PCB, whereas in a "face-down" BGA, the face points in the direction of the PCB. *Id.*

To prevent damage to the wire bonds or leads, the chip and other elements of the package during use, the chip is coated with a protective layer of encapsulant, in a process known as encapsulation. Tessera Pet. at 7-8. During the encapsulation process, the terminals of the package

are typically exposed and, because of the small size of the packages, encapsulation commonly contaminates the terminals. *Id.* Such contamination inhibits the ability to connect the package to the other system components and undermines the usability of the package. *Id.* The '106 patent discloses an allegedly novel process of protecting terminals of a face-down BGA package during the encapsulation process. *Id.* The process protects the terminals from contamination by using a protective barrier that comes in contact with the layer of the package that carries the exposed terminals. *Id.*

The '977 and '627 patents address certain problems attributable to stress caused by mismatches in coefficients of thermal expansion ("CTE") between the various materials, *e.g.*, the semiconductor chip, the package substrate, and/or the PCB, used in a semiconductor assembly. *Id.* at 44-47. Semiconductor devices generate heat during operation and subsequently cool when operation ceases. *Id.* Because the different materials have different CTEs, they expand and contract at different rates in response to temperature changes, leading to differential thermal expansion ("DTE") between the materials. *Id.* Moreover, joining together multiple materials with different CTEs causes the CTE of the combination to be different from any single material. *Id.* The repeated cycles of heating and cooling can place stress and strain on the electrical interconnections in a semiconductor assembly, particularly the solder balls, leading ultimately to breakage and electrical failure in the package. *Id.*

The asserted patents disclose an allegedly novel way to avoid the problem of stress and strain associated with DTE. *Id.* By using structures that transfer at least some of the strain from

the solder balls, or solder joints, into the semiconductor package itself, the asserted patents move strain from the outside of the package to the inside of the package, thereby improving reliability of the external connections. *Id.* As an example, the patents teach that this can be accomplished by introducing a compliant layer between the chip and the backing element to allow the package terminals to move relative to the chip when the package is heated and cooled. *Id.* By permitting this movement to occur, the patents claim that the inventive structures appreciably relieve the stresses that would otherwise be present in the solder balls as a result of DTE between the chip and the PCB. *Id.* In other words, the asserted patents teach transferring the strain from second-level electrical interconnections outside of the package *(e.g.,* solder balls) into the package using particular structures that allow relative movement between the chip and the terminals. *Id.*

The '106 patent, entitled "Method of Encapsulating Die and Chip Carrier," issued on September 2, 1997, to Konstantine Karavakis, Thomas H. Distefano, John W. Smith Jr. and Craig Mitchell. Tessera owns the '106 patent and has asserted claims 1-4, 9, 10 and 33-35 in this investigation. ID at 10-11. The '106 patent incorporates by reference two United States patents: United States Patent No. 5,148, 265 ("the '265 patent") and United States Patent No. 5,477,611 ("the '611 patent").[3]

The '977 patent, entitled "Semiconductor Chip Assemblies, Method of Making Same and

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[3] Patents incorporated by reference into another patent become part of that patent and the incorporated patents' disclosures become "effectively part of [that patent] as if [they] were explicitly contained therein." *Cook Biotech Inc. v. Acell, Inc.*, 460 F.3d 1365, 1367 (Fed. Cir. 2006).

Components for Same," issued on October 21, 1997, to Igor Y. Khandros and Thomas H. Distefano. Tessera owns the patent and has asserted claims 17 and 18 in this investigation. ID at 11-12.

The '627 patent, entitled "Semiconductor Chip Package with Center Contacts," issued on October 17, 2000, to Igor Y. Khandros and Thomas H. Distefano. Tessera owns the patent and has asserted claims 1-4, 9-12 and 15-16 in this investigation. ID at 12-14.

C. Products at Issue

The accused products in this investigation are primarily DRAM packages in the face-down orientation having a "center bonded" structure, where the chip is connected to the package substrate through wire bonds routed through a channel formed across the center of the package substrate. Tessera Pet. at 4. A few of the accused products have a face-up orientation or stacked configuration, with multiple chips being stacked on top of each other within a single package. *Id.* A majority of the accused packages use a laminate package substrate (wBGA packages), although a small handful use polyimide tape instead (µBGA packages). *Id.*

Specifically, products accused of infringing the '106 patent have the following characteristics: "(1) BGA packages, (2) that contain one or more chips where the chip nearest the package substrate is in a face-down orientation and (3) the chip is electrically bonded to the package substrate through a window in that substrate." *Id.* Products accused of infringing the '977 and '627 patents include packages that have the following characteristics: "(1) BGA packages (2) with solder ball pitch of 1.2 mm or less, (3) with at least one solder ball under the

die, (4) with a die attach modulus of elasticity of 3.5 GPa or less and (5) with more than 36 solder balls." *Id.*

Each Respondent manufactures or sells DRAM chip packages, memory modules, and/or consumer electronic products containing either DRAM chip packages or memory modules. ID at 14. Complainant Tessera does not manufacture products meeting the description of the accused products at issue. *Id.* Instead, Tessera's business is in developing and licensing technologies. *Id.*

II. STANDARD OF REVIEW

Under the Administrative Procedure Act, upon review of the initial determination of the ALJ, "the agency has all of the powers which it would have in making the initial decision except as it may limit the issues on notice or by rule." 5 U.S.C. § 557(b); *Certain Acid-Washed Garments and Accessories*, Inv. No. 337-TA-324, Commission Opinion at 4-5 (Aug. 28, 1992) (the Commission examines for itself the record on the issues under review); 19 C.F.R. § 210.45(c). In other words, once the Commission decides to review the decision of the ALJ, the Commission may conduct a review of the findings of fact and conclusions of law presented by the record under a *de novo* standard.

III. CLAIM CONSTRUCTION

A. Legal Standard

Claim construction "begin[s] with and remain[s] centered on the language of the claims themselves." *Storage Tech. Corp. v. Cisco Sys., Inc.*, 329 F.3d 823, 830 (Fed. Cir. 2003). That is, the words of the claims "define the scope of the patented invention." *Vitronics Corp. v.*

Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996). Claims should be given their ordinary and customary meaning as understood by a person of ordinary skill in the art, viewing the claim terms in the context of the entire patent. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (*en banc*). In construing claims, a court looks first to the intrinsic evidence, which consists of the language of the claims, the patent's specification and the prosecution history, as such evidence "is the most significant source of the legally operative meaning of disputed claim language." *Vitronics,* 90 F.3d at 1582. The claims themselves, however, "provide substantial guidance as to the meaning of particular claim terms." *Phillips,* 415 F.3d at 1314. In addition, it is essential to consider a claim as a whole when construing each term, because the context in which a term is used in a claim "can be highly instructive." *Id.*

When the meaning of a claim term remains uncertain, the specification is usually the first and best place to look, aside from the claim itself, in order to find that meaning. *Phillips,* 415 F.3d at 1315. The specification of a patent "acts as a dictionary" both "when it expressly defines terms used in the claims" and "when it defines terms by implication." *Vitronics,* 90 F.3d at 1582; *Phillips,* 415 F.3d at 1323. "The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." *Phillips,* 415 F.3d at 1316. "[I]t is axiomatic that a claim construction that excludes a preferred embodiment . . . is rarely, if ever correct and would require highly persuasive evidentiary support." *Anchor Wall Sys. v. Rockwood Retaining Walls Inc.*, 340 F.3d 1298, 1308 (Fed. Cir. 2003) (quoting *Vitronics,* 90 F.3d at 1583). A court, however, may not

read particular examples or embodiments discussed in the specification into the claims as limitations. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (*en banc*). "Absent a clear disclaimer of particular subject matter, the fact that the inventor anticipated that the invention may be used in a particular manner does not limit the scope to that narrow context." *Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1301 (Fed. Cir. 2003).

The prosecution history, which includes the cited prior art "provides evidence of how the PTO [United States Patent and Trademark Office] and the inventor understood the patent." *Phillips,* 415 F.3d at 1317. The prosecution history may inform the meaning of the claim language by demonstrating how an inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it otherwise would be. *Vitronics,* 90 F.3d at 1582-83. "The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution." *Chimie v. PPG Indus., Inc.,* 402 F.3d 1371, 1384 (Fed. Cir. 2005). For example, "[a]n amendment or argument made in the course of prosecution may . . . serve as a disclaimer of a particular interpretation of a claim term." *Arlington Indus., Inc. v. Bridgeport Fittings, Inc.*, 345 F.3d 1318, 1328-29 (Fed. Cir. 2003). For prosecution history disclaimer to attach, however, "the alleged disavowing actions or statements made during prosecution [must] be both clear and unmistakable." *Omega Eng'g, Inc. v. Raytek Corp.*, 34 F.3d 1314, 1326 (Fed. Cir. 2003). Moreover, "[t]here is no 'clear and unmistakable' disclaimer if a prosecution argument is subject to more than one reasonable interpretation, one of which is consistent with a proffered meaning

of the disputed term." *SanDisk Corp. v. Memorex Prods.*, 415 F.3d 1278, 1287 (Fed. Cir. 2005).

Differences between claims may be helpful in understanding the meaning of claim terms. *Phillips,* 415 F.3d at 1314. A claim construction that gives meaning to all the terms of a claim is preferred over one that does not do so. *Merck &* Co. *v. Teva Pharms. USA, Inc.,* 395 F.3d 1364, 1372 (Fed. Cir. 2005). In addition, the presence of a specific limitation in a dependent claim raises a presumption that the limitation is not present in the independent claim. *Phillips,* 415 F.3d at 1315. This presumption of claim differentiation is especially strong when the only difference between the independent and dependent claim is the limitation in dispute. *SunRace Roots Enter. Co. v. SRAM Corp.,* 336 F.3d 1298, 1303 (Fed. Cir. 2003).

B. Construction of the Claim Term "Top Layer" Recited in Asserted Independent Claim 1 of the '106 Patent

The Commission determined to review the finding that the claim term "top layer" recited in claim 1 of the '106 patent means "an outer layer of the chip assembly upon which the terminals are fixed," the requirement that "the 'top layer' is a single layer," and the effect of these findings on the infringement analysis, invalidity analysis and domestic industry analysis. Claim 1 of the '106 patent, with the key claim term emphasized for clarity, is reproduced below:

> 1. A method of encapsulating a semiconductor chip assembly having a **top layer** with an array of exposed terminals thereon, the terminals being electrically connected to the chip, said method comprising the steps of:
>
> > placing an encapsulant barrier adjacent the semiconductor chip assembly, said encapsulant barrier at least partially defining an encapsulant area;
> >
> > providing a protective barrier in contact with said **top layer** for

> protecting the terminals on the **top layer** from an encapsulant material; and
>
> introducing an encapsulation material into at least a portion of the encapsulation area so that the encapsulation material flows to fill the encapsulation area and then cures to a substantially solid condition, the protective barrier preventing the encapsulation material from contacting the terminals on the **top layer**.

The ALJ construed the claim term "top layer" as "an outer layer of the chip assembly upon which the terminals are fixed," adding that "the 'top layer' is a single layer." ID at 24. We find that the ALJ erred in his construction of the claim term. Specifically, by adding the word "outer" to his claim construction, the ALJ impermissibly broadened the claim, and by requiring a single layer, the ALJ impermissibly narrowed the claim. We therefore modify the ALJ's claim construction by reversing his substitution of "outer" for "top" and reversing his requirement that "the 'top layer' is a single layer."

The claim at issue recites "[a] method of encapsulating a semiconductor chip assembly having a top layer with an array of exposed terminals thereon." In other words, the plain language of the claim specifically requires that the "array of terminals" be located on a **<u>top</u>** layer. By substituting the word "outer" for "top," the ALJ improperly broadened the claim term because the word "outer" includes more scope than "top." For example, "outer" can refer to "top," "bottom" or "sides." In addition, the '106 patent incorporates by reference, the '265 patent, which defines a frame of reference for "top." The '265 patent states:

> The front or contact-bearing face 22 of the chip is regarded as **<u>defining the top of the chip</u>**. Thus, in specifying direction pointing out of front face 22, and away from the chip, *i.e.*, the

> direction pointing out of the plane of the drawing towards the viewer in FIG. 1. The downward direction is the opposite direction. As used in the present disclosure with respect to a semiconductor chip assembly, such terms should be understood as based on this convention and should not be understood as implying any particular direction with respect to the ordinary gravitational frame of reference.

'265 patent, col. 9, ll. 22-33 (emphasis added). In other words, the patent requires that "[t]he front or contact-bearing face" of the chip is the top of the chip and specifies a direction for "top." We share Tessera's view that "top" as recited in the patent modifies "layer" by providing specific directional reference, and the ALJ's construction, substituting the word "outer" for "top" renders the claim term "top" meaningless because "outer" does not provide any directional reference. Moreover, the ALJ's construction does not include language that would account for the directional reference that the claim term "top" conveys.

Tessera also asserted that the "top layer" need not be limited to a single layer but that it could encompass a composite layer as well. The ALJ rejected this assertion, finding that "top layer" meant a single layer. ID at 22. In reaching his decision, the ALJ noted that Figure 1 of the '106 patent describes a semiconductor chip and chip carrier, wherein "[t]he chip carrier 14 is made up of a top layer 16 (preferably a polyimide layer or the like) and an elastomeric pad 20 disposed between the top layer 16 and the semiconductor chip 12" and that "other embodiments in the '106 patent similarly describe the top layer as separate and distinct from the elastomeric pad, which in combination form the chip carrier." ID at 23 (citing '106 patent, col. 5, ll. 8-13;

col. 7, ll. 22-26; col. 9, ll. 1-4; Figures 1, 9, and 13). The ALJ further noted that the '265 patent specification describes an interposer, a component of the chip carrier, as "includ[ing] a flexible top layer 38 (FIG.3) formed by a thin sheet of material having a relatively high elastic modulus and a compliant bottom layer formed from a material having a relatively low elastic modulus." *Id.* (citing '265 patent, col. 9, ll. 50-54). The ALJ added that "the '611 patent describes a single 'dielectric layer' that carries the terminals, *i.e.*, the dielectric layer is the 'top layer' in the '611 patent." *Id.* (citing '611 patent, col. 4, ll. 23-25). Based on those disclosures, the ALJ concluded that "the '106 Patent specification explicitly distinguishes the different layers, *e.g.* 'top layer' and 'elastomeric' layer of the chip carrier," adding that "in both the '611 Patent and the '265 Patent, the term 'layer' refers to a single layer." *Id.*

We disagree with the ALJ's reasoning. Importantly, neither the specification of the '106 patent, the '265 patent, nor the '611 patent include any language indicating that the patentees expressly limited the claim term to a single layer, and the patentees did not explicitly disavow the use of a composite or multi-tiered layer during prosecution of the patent application.[4] Absent

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[4] Respondents argue that Tessera limited the scope of the claim to a single layer when during prosecution of the patent application it stated that "[t]he embodiment of Khandros Fig. 3 does not utilize the step of providing 'a protective barrier in contact with said top layer'" and that Tessera could have amended the claim to include the limitation "in contact with the [multi-layered] interposer layer," but chose not to. Resp Br. at 27-28. Respondents add that "[b]y specifically limiting the amendment to require contact with the single-layer 'top layer,' Tessera disclaimed any construction of 'top layer' as a composite layer." *Id.* We find this argument unpersuasive. Merely amending to state "said top layer" does not expressly disavow a multi-tiered top layer. Indeed, there is some evidence in the specification of the '265 patent that a layer may encompass more than one material. *See* '265 patent, col. 14, ll. 32-34.

clear indication that the patentees intended to limit the scope of the claim term to a single layer, the claim term should not be limited to a single layer. Even if there is no disclosure in the specification showing the top layer as a composite or multi-tiered layer, because nothing in the intrinsic evidence limits the claim term to a single layer, the ALJ incorrectly limited the claim term. *See Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) ("Even when the specification describes only a single embodiment, the claims of the patent will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope."). Thus, we construe the term "top layer" to mean "a layer disposed on the active side of the chip and which carries the terminals."

We note that our changes to the ALJ's claim construction do not affect his validity and domestic industry analyses.

C. Construction of the Claim Term "Thereon" Recited in Asserted Independent Claim 1 of the '106 Patent

The Commission determined to review the finding that the claim term "thereon" recited in claim 1 of the '106 patent requires "disposing the terminals on the top surface of the top layer," and its effect on the infringement analysis, invalidity analysis and domestic industry analysis.

The ALJ stated that he adopted the ordinary meaning of the claim term "thereon," concluding that construction of the term was unnecessary. ID at 26. In applying the claim term to the accused products, however, the ALJ applied a narrow meaning of the claim term by

requiring the terminals to be "'on or upon'—on the top of—the 'top layer.'" ID at 50. We find that the scope of the claim is broad enough to encompass locating the terminals on other surfaces of the "top layer" other than the top surface, such as on the bottom or side surfaces.

After careful review of the prosecution history of the '106 patent, we disagree with Respondents that it clearly disavows locating terminals on the bottom surface of the top layer under all conditions. Instead, we believe that if the applicants disavowed any subject matter, they disavowed locating terminals on the bottom of the top layer when the terminals are unexposed during encapsulation. This condition, however, does not arise in this investigation because the asserted claims of the '106 patent require exposed terminals. '106 patent, claim 1 ("A method of encapsulating a semiconductor chip assembly having a top layer with an array of **exposed** terminals thereon" (emphasis added)).

Respondents point to remarks made during prosecution of the '106 patent to support their argument that the patent applicants disclaimed locating the terminals on the bottom surface of the claimed "top layer." Response of Elpida Respondents to Tessera's and the IA's Petitions for Review ("Elpida Rep.") at 28-29; Resp Br. at 12. The '106 patent incorporates the '265 patent by reference and thus the '265 patent's disclosure is part of the '106 patent. However, the '265 patent is prior art to the '106 patent, and during prosecution of the '106 patent application, the Patent Office rejected the then-pending claims in light of the '265 patent. The Patent Office based its rejection on the view that the "interposer" described in the '265 patent corresponds to

the "protective barrier" recited in claim 1 of the '106 patent application. *See* '106 Patent Prosecution History (JX-6) June 24, 1996, Office Action. In order to overcome the Patent Office's rejection, the applicants of the '265 patent application amended the then-pending claims to stress that the "interposer" described in the '265 patent and the "protective barrier" of the '106 patent application do not correspond to each other.[5] The applicants added the following remarks:

> In the interview, the alternative embodiment of Khandros (Khandros Fig. 7) and column 14, line 19 – column 15, line 4 was also discussed. As pointed out in the interview, however, this embodiment of Khandros 265 does not involve encapsulation of a semiconductor chip layer which has "a top layer with an array of exposed terminals thereon." Rather, the terminals 148 are disposed on the undersurface of the top layer 138. At the time encapsulation 158 is applied, there are not exposed terminals to be protected. Rather, after application of encapsulant 158, radiant energy source 159 is used to punch holes 160 in top layer 138, thereby exposing the terminals. Clearly, this embodiment of Khandros '265 has no need for . . . "a protective barrier in contact with said top layer."

'106 Patent Prosecution History (JX-6) December 24, 1996 Amendment. According to Respondents, those remarks support their argument that the '106 patent disclaims locating the terminals on the bottom surface of the claimed "top layer." Elpida Rep. at 28-29; Resp Br. at 12. We disagree. Instead, the applicants explained that because the terminals are disposed on the undersurface of the top layer in the '265 patent, they are not exposed during encapsulation and

[5] Specifically, the amendment required that the "protective barrier" be provided "in contact with [the] top layer." '106 Patent Prosecution History (JX-6) December 24, 1996, Amendment.

that it is after application of the encapsulant that radiant energy is used to punch holes in the top layer to expose the terminals. The applicants thus argued that the '265 patent does not involve encapsulation of a semiconductor chip layer which has "a top layer with an array of exposed terminals thereon," as recited in claim 1 of the '106 patent application. If the applicants disclaimed any subject matter, they disclaimed only locating terminals on the bottom surface of the top layer when the terminals are not exposed during encapsulation.

The doctrine of claim differentiation provides further support for our conclusion. Claim 20, which depends from claim 1, includes the recitation, "wherein said top layer includes a top surface on which the array of terminals is disposed and said barrier includes a dam extending upwardly from said top surface." That is, dependent claim 20 further limits the invention described in independent claim 1 by requiring, *inter alia*, that the array of terminals be located on the top surface of the top layer, indicating that independent claim 1 is not so limited.

Respondents argue that Tessera presents the argument that the terminals are located on the bottom surface of the top layer for the first time in its petition for review and as such the argument is waived. Elpida Rep. at 28-29. Likewise, Tessera argues that Respondents' "disclaimer" argument, which is in response to its argument that the terminals are located on the bottom surface of the top layer, is untimely. Tessera Br. at 24. We, however, believe that Tessera only had the opportunity to present its arguments for the first time in its petition for review. The ALJ decided not to construe the claim term "thereon" and stated that he would

apply its plain and ordinary meaning. Tessera and the IA could have reasonably assumed that their argument was inherent in the plain and ordinary meaning of "thereon." In other words, Tessera and the IA had no reason to make their arguments until they realized what the ALJ meant by "plain and ordinary meaning" of the claim term "thereon." In addition, we believe that the argument was subsumed in Tessera's presentation explaining how the accused products infringe. *See* Tessera's Post-Hearing Brief at 52-53. Similarly, Respondents could not respond until Tessera made its argument, so we consider Respondents' argument.

We note that our changes to the ALJ's claim construction do not affect his validity and domestic industry analyses.

III. INFRINGEMENT

A. Legal Standard

After construing the claims of the patent, a factual determination must be made as to whether the properly construed claims read on the accused devices. *Markman*, 52 F.3d at 976. Literal infringement of a claim occurs when the properly construed claim reads on the accused device exactly, *i.e.,* when every limitation recited in the claim appears in the accused device. *Amhil Enters., Ltd. v. Wawa, Inc.,* 81 F.3d 1554, 1562 (Fed. Cir. 1996). In a section 337 investigation, the complainant bears the burden of proving infringement of the asserted patent claims by a "preponderance of the evidence." *Enercon GmbH v. Int'l Trade Comm'n,* 151 F.3d 1376, 1384 (Fed. Cir. 1998).

B. Infringement Analysis of the '106 Patent

The ALJ identified the elastomeric layer in Respondents' accused μBGA packages as the "top layer" and the laminate substrate core in Respondents' accused wBGA packages as the "top layer" because the record evidence showed that those were the layers that the terminals appeared to be "on or upon." ID at 50-51. The ALJ then found that the accused packages met the claimed "a top layer with an array of exposed terminals thereon," namely the "solder ball pads on the substrate core layer in wBGA products and the solder ball pads on the eastomeric layer of the package substrate in the μBGA products." *Id.* The ALJ, however, concluded that the accused packages do not infringe because "the 'protective barrier' never comes into contact with either the core substrate layer or the elastomeric layer." *Id.* at 52. Tessera and the IA dispute the ALJ's identification of "top layer" in the accused packages, and contend that the application of a proper construction of the claim terms "top layer" and "thereon" shows that the polyimide layer with an array of terminals thereon constitutes the "top layer" in the μBGA packages, and the multi-part laminate substrate layer, having the solder mask layer as the outer most layer represents the "top layer" in the wBGA packages.

To support their position, Tessera and the IA primarily rely on the embodiment described in Figure 7 of the '265 patent. *See* Tessera Pet. at 12, 23-24; IA Pet. at 7-8. Tessera emphasizes that the accused "μBGA packages have the exact structure of the interposer/chip carrier described and depicted in the '106 and '265 patents" and that although "like the accused

packages, the terminal is sandwiched between the top layer and the elastomeric layer; it comes in contact with, and can be said to be 'on' both surfaces," the '265 patent identifies the polyimide layer as the top layer. Tessera Pet. at 36. In other words, according to Tessera, although the terminals "can be said to be on both surfaces," the polyimide layer represents the claimed "top layer" because the '265 patent identifies it as such.

Nothing precludes identifying the polyimide layer as the claimed "top layer" in the µBGA packages. Indeed the '106 patent states that "[t]he chip carrier 14 is made up of a top layer 16 (preferably a polyimide layer or the like) and an elastomeric pad 20 disposed between the top layer 16 and the semiconductor chip 12." '106 patent, col. 5, ll. 10-13. That is, the '106 patent itself identifies the polyimide layer as the "top layer" and distinguishes between the "top layer" and the "elastomeric layer," which the ALJ determined was the "top layer." We therefore reverse the ALJ's finding that the polyimide layer cannot represent the claimed "top layer."

The ALJ found that the accused µBGA packages do not infringe because of his finding that the "protective barrier" (the second mold chase) does not come into contact with the top—elastomeric—layer. *See* ID at 51-53. As noted above, we disagree with the ALJ that the elastomeric layer exclusively represents the claimed "top layer." Rather, in our judgment, the polyimide layer may also represent the "top layer." The record evidence shows that the "protective barrier" comes into contact with the polyimide layer. *See* ID at 52 ("In µBGA products, the second mold chase is in contact with the polyimide layer."); RX 323C; RX-9C;

RX-310C; RX-311C. Thus, the μBGA packages meet each limitation of asserted claim 1 of the '106 patent. Nevertheless, the μBGA packages do not infringe because they are exclusively Elpida products (*See* Complainant Tessera Inc.'s Corrected Post-hearing Brief at 50-51) and Elpida established its patent exhaustion defense for all its products. ID at 153 (stating that "the ALJ finds that 100% of Elpida's suppliers were licensed entities").[6]

With respect to the wBGA products, Tessera's theory of infringement requires the claimed "top layer" to include the solder mask layer, either as a single layer or as part of a composite laminate substrate. *See* Tessera Pet. at 32-33. The intrinsic evidence of the '106 patent, however, makes clear that the solder mask layer and the claimed "top layer" are distinct components. For example, the figures of the patent identify the solder mask as component 30

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[6] At this late stage of the investigation, after the Commission has adopted the ALJ's determination with respect to Respondents' affirmative defense of patent exhaustion, Tessera invites the Commission in its brief on the issues of remedy, the public interest and bonding, to reconsider the ALJ's patent exhaustion determination. Complainant Tessera, Inc.'s Corrected Brief on the Issues of Remedy, the Public Interest, and Bonding at 65. Tessera asserts that *Jazz Photo Corporation v. United States International Trade Commission*, 264 F.3d 1094, 1105 (Fed. Cir. 2001) and the Commission opinion on enforcement in *Certain Ink Cartridges and Components Thereof*, Inv. No. 337-TA-565 (Sept. 24, 2009) stand for the proposition that only a "patent exhausting first sale" taking place in the United States can trigger patent exhaustion. *Id.* at 63. The IA appears to support Tessera's assertion, though the IA does not request review. *See* OUII's Reply to Respondents' Responses to Commission Questions at 18-19. Tessera and the IA, however, failed to present this argument to the ALJ during the course of the investigation to give him an opportunity to consider the argument and make appropriate findings. Indeed, Tessera did not even raise this argument in its petition for review to the Commission, and the IA did not even petition the Commission to review the ALJ's patent exhaustion determination. Against this backdrop, we decline Tessera's invitation and find that Tessera has waived the argument. *Broadcom Corp. v. Int'l Trade Comm'n*, 542 F.3d 894, 901 (Fed. Cir. 2008) ("Broadcom has therefore waived that argument by failing to preserve it in the proceedings before the administrative law judge."); 19 C.F.R. § 210.43(b)(2).

and the top layer as component 16. In addition, the patent states that "[p]referably, the solder mask is vacuum laminated to the top layer of the semiconductor chip assembly. More preferably, the solder mask is vacuum laminated not only to the top layer of the semiconductor chip assembly but also to the top side of the encapsulant barrier." '106 patent, col. 2, ll. 35-40. Nowhere does the '106 patent describe or suggest that the top layer includes the solder mask layer. Rather, the patent continually depicts them as separate and distinct components. *See, e.g.*, 106 patent, FIG. 1.

Unasserted claim 22 of the '106 patent, which depends from asserted independent claim 1, provides further support. Claim 22 includes the recitation:

> The method in claim 1, wherein said top layer includes a top surface on which the array of terminals are disposed, said protective barrier includes a sheet like mask [*i.e.*, solder mask layer], and said providing step includes attaching said mask to said top surface of said top layer and to said encapsulant barrier such that said mask extends over said encapsulation area.

In other words, consistent with the specification, claim 22 teaches attaching the solder mask layer to the top layer. The solder mask layer, therefore, cannot be the top layer. Given that the top layer cannot include the solder mask layer, the ALJ correctly concluded that for the wBGA packages, the laminate-based substrate core layer represents the claimed "top layer," and that because the "protective barrier" does not come into contact with that layer, the wBGA packages do not infringe the asserted claims of the '106 patent. ID at 51.

C. Infringement Analysis of the '977 and '627 Patents

We note that determinations reached by the Commission in prior investigations are not binding on subsequent investigations and each investigation must be decided on its own record evidence. *See Certain Flash Memory Circuits and Products Containing Same*, Inv. No. 337-TA-526, Final Initial and Recommended Determinations (Public Version) at 4-5 (Jan. 17, 2006). There is no doctrine of *stare decisis* in an administrative practice. Notwithstanding, no dispute exists that the testing methodology at issue in this investigation is the same as the testing methodology the Commission reviewed in the 605 Investigation. ID at 4; Order No. 40. Accordingly, we believe that the Commission's opinion regarding that testing methodology, while not binding in this investigation, remains instructive.

As described *supra* at Part I.B., the '977 and '627 patents are drawn to a semiconductor chip assembly that allegedly improves solder joint reliability by reducing the stress and strain on the solder joints caused by mismatched CTEs. The claimed inventions concentrate on the incorporation of a compliant layer into the semiconductor assembly to allow for terminal displacement to appreciably relieve stress caused by external loads. The stress relief on the solder joints improves the reliability of the semiconductor assembly when it is subjected to repeated heating and cooling cycles during operation. The patents do not claim achieving the improvement by matching the effective CTE of the semiconductor package to the CTE of the circuit board. Rather, the patents claim improvement by using movable terminals.

The parties agree that the central dispute is whether the accused products meet the recited "movable terminals" limitations. *See* ID at 54. The ALJ construed the term "movable terminals" to require that "in the operation of the assembly, the terminals are capable of being displaced relative to the central contacts of the chip by external loads applied to the terminals, to the extent that the displacement appreciably relieves mechanical stresses, such as those caused by differential thermal expansion which would be present in the electrical connections absent such displacement." *Id.* at 40. The limitation at issue in this investigation, "movable terminals" is the same limitation that was at issue in the 605 Investigation and in both investigations, the ALJ gave the limitation essentially the same construction. The main difference between this investigation and the 605 Investigation is that in the 605 Investigation, the asserted claims as well as the accused products were limited to "face up" packages. The Commission must determine whether the ALJ erred in finding that the methodology employed by Tessera's expert, Dr. Qu, to prove infringement failed to prove infringement.

In the 605 Investigation, the Commission noted that the ALJ criticized Dr. Qu's results because Dr. Qu admitted that chip packages are, in reality, non-linear systems and that his "linearity assumption" is merely an approximation of the packages' behavior. 605 Comm'n Op at 39. The Commission found the ALJ's criticism to be misplaced because Respondents' expert, Dr. Sitaraman, acknowledged the appropriateness of using the linearity assumption to determine displacement due to only external loads in his own modeling of the prior art and an accused package. *Id.* The Commission further noted that Dr. Qu's method of determining displacement

due to only external loads "is inherently logical" and that "[a]ny off-board displacement observed in the accused packages during thermal cycling must be due to internal forces only, as there are no external forces present when the package is off-board." *Id.* The Commission concluded that "[t]herefore, any deviation from the off-board displacement when the package is on-board must be due to the counteracting forces applied by the PCB, which is the very definition of 'external load'" and that "it is completely logical, as confirmed by both Drs. Qu and Sitaraman, to consider this deviation in displacement as an approximation of the external load." *Id.*

We note that Dr. Sitaraman's testimony is not of record in this investigation. Dr. Qu specifically testified that the linearity assumption would only be an accurate reflection of the accused packages if the accused packages were first proven to be linear and that the linearity assumption can provide a good approximation only if the accused packages were slightly non-linear. Qu, Tr. 807:1-14; 603:17-20. Dr. Qu, however, admitted that the accused packages in this investigation were non-linear:

> Q. Dr. Qu, these packages that are accused in this investigation, they are nonlinear, are they not?
>
> A. Yes, I agree they are nonlinear.

Qu, Tr. 539:7-10. Dr. Qu added that:

> [f]or solder, it is a little more complex because the behavior is nonlinear. In other words, when you double the amount of the force, you don't get double the amount of displacement. You get a nonlinear relationship. And not only that, that stress-strain relationship also depends on temperature. So it is not purely linear elastic deformation.

Qu, Tr. at 813:17-21. Dr. Qu did not determine the degree of non-linearity of the accused packages because in his own words it is "rather difficult to estimate the degree of non-linearity of the package assemblies." Qu, Tr. 604:5-15; CX-6486C (Qu. W.S.) Q.453. Due to the difficulty in determining the linearity of the accused packages, Dr. Qu testified that he did not rely on his direct loading methodology to prove infringement:

> Q. Can you tell us what types of methodologies or what different methodologies did you use to analyze the accused products?
>
> A. There are basically two types of methodologies . . . Then in one chapter I presented alternative method. That alternative method used the so-called linearity assumption. Okay? Now, that alternative method, as I discuss in my report is not an exact method because you have used the assumption that a system is linear. If you know the system linearity (sic, nonlinearity) is very weak, then that might be a good assumption. Therefore, the solution might be a good one. But if the nonlinearity is very high, that may not be. So I do not rely my opinion on that alternative methodology.

Qu, Tr. 806:17-807:14. In the 605 Opinion, the Commission found evidence in the expert report submitted by Dr. Qu that he believed that his direct loading testing independently showed infringement. 605 Comm'n Op at 38-39. Such evidence is not present in this investigation.[7] In addition, the expert for Respondents, Dr. Clech, testified that "[s]older is highly non-linear. Solder creeps and its response to loads is time and temperature dependent. Because of the non-

[7] The ALJ excluded all expert reports from being admitted into evidence in this investigation. *See* Prehearing Conf. Tr. 96:4-6.

linearity of the mechanical behavior of solder, applying a force is not equivalent to applying a displacement." RX-946C (Clech Rebuttal W.S.) Q. 253. We find that the record lacks sufficient evidence to show that the direct loading methodology as employed in this investigation proves infringement. The ALJ, therefore, did not err in his finding.

[

] The ALJ found this explanation troubling, stating that "[i]t is difficult to rely on science that is so inexact as to suggest a deviation should be somehow canceled out." ID at 74. In addition, Dr. Clech testified that the "physical and thermal-mechanical properties of solders are highly sensitive to the solder alloy composition." RX-946C (Clech, RWS) at Q. 185. Based on the evidence, the

ALJ concluded that [ ] was not scientifically sound, noting that "Dr. Qu himself testified multiple places that the correct materials properties are important to the accuracy of the model and changing them can have unpredictable results." *Id.* (citing Qu, Tr. 648:7-649:14; 673:7-18; 673:25-674:15; 675:8-21; 683:13-17.). We find nothing wrong with the ALJ's findings. Both experts for Tessera and Respondents testified to the unreliability of the linearity assumption when dealing with materials that are non-linear—as the record evidence indicates the solder material may be. Both experts also testified to the "dramatic effect" that can result in using the wrong material composition in the tested models—as was done here.

Moreover, Dr. Qu admitted that CAE improperly modeled the package substrate and PCB as isotropic, where the x, y and z axes have the same modulus, instead of orthotropic, where the z axis has a different modulus from the x and y axes, as he instructed CAE to do.[8] Dr. Qu explained the importance of correctly modeling the package substrate and PCB as orthotropic, testifying that the package substrate and PCB are reinforced with fiberglass, and as a result, they have different moduli on the x, y and z axes. Qu, Tr. at 573:8-574:13; 577:20-578-4, 833:19-22. Dr. Qu, however, was under the impression that CAE had modeled the substrate and PCB as orthotropic and only became aware of the discrepancy during cross examination at the hearing.

---

[8] CAE refers to Computer Aided Engineering Associates, a firm Dr. Qu engaged to model accused packages using Finite Element Analysis ("FEA").

CAE's President, Dr. Veikos, disputes Dr. Qu's assertion and testified that Dr. Qu instructed CAE to model the package substrate and the PCB isotropically. *See* Veikos, Tr. at 2500:14-2501:19.

Qu, Tr. at 576:16-577:20; 836:14-839:11. The ALJ found that "Dr. Qu never investigated, quantified, or even qualitatively analyzed the error because he did not know about the mistake until cross examination" and that "given the precision of these finite element models and the potentially compounding effect of mistakes, it is unclear whether the mistake would make a material difference." ID at 68. The ALJ's misgivings are not misplaced. *See Daubert v. Merrill Dow Pharm., Inc.*, 509 U.S. 579, 594 (1993) (stating that "in the case of a particular scientific technique, the court ordinarily should consider the known or potential rate of error") (citations omitted). The Commission agrees that because Dr. Qu was unaware of the mistake until the hearing, the impact of the mistake on Dr. Qu's analysis is unclear.

Finally, the Commission noted in its 605 opinion that:

> By simulating the external load applied to the packages and applying only this simulated external load to compare the plastic work of the solder joints between a package with a compliant layer and a package without a compliant layer, Dr. Qu successfully demonstrated that the observed increase in the solder reliability in the accused packages as compared to the baseline packages was due to the external load. The only **missing link precluding a finding of infringement** is a showing that the demonstrated stress relief in the solder balls of the accused packages was due to terminal-to-chip displacement caused by the applied external load.
>
> In their attempt to discredit Dr. Qu's testing method, Respondents provide this missing link. The ALJ and Respondents relied on Dr. Sitaraman's exhibit to show that there was little difference in the on-board and off-board terminal-to-chip displacement. RX-3483. As the data that Dr. Sitaraman extracted from Dr. Qu's second testing method shows, however, there is terminal-to-chip displacement in the accused packages when an external load is applied. *Id.* As is clear from the data, there is a difference in the positions of the terminals relative to the chip in the accused

> packages after thermal cycling when the chip is on-board as opposed to when the chip is off-board. This difference in positions is due solely to the external load the PCB is applying to the terminals.

605 Comm's Op at 48-49 (emphasis added). That is, the Commission noted that Dr. Qu's testing omitted a "missing link" necessary for a finding of infringement—a showing that the demonstrated stress relief in the solder balls of the accused packages was due to terminal-to-chip displacement caused by the applied external load. *Id.* The Commission, however, found the missing link in the exhibits presented by Respondents' expert, Dr. Sitaraman. *Id.* As noted, Dr. Sitaraman did not participate in this investigation and the record evidence does not contain evidence consistent with the exhibit that he presented in the 605 Investigation that the Commission found provided the "missing link."

The ALJ correctly concluded that the record evidence shows that Dr. Qu's moiré analysis[9] fails to provide the "missing link" and cannot compensate for the identified mistakes in Dr. Qu's direct loading methodology as respondents argued. ID at 90. The ALJ noted that Dr. Qu's moiré analysis confirmed his FEA to an extent that computer modeling predicted the actual displacements of packages to a reasonable degree of accuracy. *Id.* The ALJ pointed to Dr. Qu's statement that:

---

[9] Tessera explains that "[m]oiré is a technique for determining the deformation of a structure using laser pattern analysis. Lasers are projected onto the surface of a structure at rest as a control, then the structure is subjected to conditions that cause deformation and the lasers are re-projected onto the structure surface. Based on the difference in the patterns, the amount and direction of deformation can be compared to the amount and direction of deformation predicted by FEA." Tessera Pet. at 65.

> [m]ost importantly though, moiré results, regardless of how accurate they are or how many packages are tested, cannot by themselves prove infringement. They only show displacement. They do not allow measurement of whether there has been appreciable relief of stress within a particular package, as required by the claims of the asserted '977 and '627 patents.

CX-06486C (Qu DWS) at Q. 405. In other words, as the ALJ correctly noted, "while Dr. Qu's moiré result does not contradict the displacement results of the FEA, it does little to confirm the baseline comparison methodology and does not confirm any claimed movement." ID at 90.

Although Dr. Qu employed the same direct loading methodology in both this investigation and the 605 Investigation, the record evidence of the two investigations compel reaching different results. In particular, due to the uncertainty of the linearity assumption, Dr. Qu testified in this investigation that he did not rely on his direct loading methodology to prove infringement. In addition, [

] Dr. Qu modeled the solder material without copper, which experts for both Tessera and Respondents agree could result in unpredictable results. Moreover, CAE, the lab Dr. Qu employed, modeled the package substrate and PCB as isotropic instead of orthotropic, and Dr. Qu did not become aware of the discrepancy until the hearing. Finally, the "missing link" precluding a finding of infringement that the Commission found present in the 605 Investigation is absent in this investigation. Thus, we affirm the ALJ's finding of no infringement with respect to the asserted claims of the '977 and

’627 patents.

D. Whether the OMPAC Reference Anticipates the Asserted Claims of the ’977 and ’627 Patents

“Claimed subject matter is ‘anticipated’ when it is not new; that is, when it was previously known.” *Sanofi-Synthelabo v. Apotex, Inc.*, 550 F.3d 1075, 1082 (Fed. Cir. 2008). 35 U.S.C. § 102(b) provides that a person shall be entitled to a patent unless “the invention was . . . in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States.”

We find that the ALJ erred by relying on the “1990 date of invention” of the asserted claims of the ’977 patent. *See* ID at 117. The on-sale bar provision of 35 U.S.C. § 102(b) provides that sales made “more than one year prior to the date of the application” qualify as prior art. In other words, the “date of invention” has no bearing on this analysis. It is instead the earliest effective filing date of the patent that is important. Notwithstanding, the ALJ did not err in his finding that Respondents failed to show by clear and convincing evidence that the 1989 Motorola OMPAC 68-pin chip package (“OMPAC”) anticipates under the section 102(b) on-sale bar. The record evidence supports the ALJ’s finding that the OMPAC package was an experimental prototype and the “sale” from Citizen Watch to Motorola was subject to a confidentiality agreement. *Id.* at 118.

The ALJ stated that the evidence shows that Motorola contacted Citizen Watch in Japan

about producing "engineering samples" or "prototypes" of a package with characteristics that were specified by Motorola, and that Citizen Watch was subject to a confidentiality agreement with Motorola which precluded it from selling the engineering samples to any other company, or otherwise disclosing any information regarding the OMPAC to any entity but Motorola. *Id.* (citing CX-7349C (Ivey, Direct) Q. 255; CX-07355C (Urbish, Direct) Q. 38; Freyman, Tr. 1669:16-25, 1670: 1-11, 1676:13-15, 1678:8-13). The ALJ thus concluded that the sale to Motorola was for experimental purposes and did not constitute a commercial sale that would trigger the on-sale bar provision of section 102(b). ID at 118 (citing *Manville Sales Corp. v. Paramount Sys., Inc.*, 917 F.2d 544, 550 (Fed. Cir. 1990) (stating that "a sale that is primarily for experimental purposes, as opposed to commercial exploitation, does not raise an on sale bar")).

We agree with the ALJ's finding. We, however, modify the ALJ's decision to clarify that the "invention date" of the patent has no bearing on the section 102(b) on-sale bar analysis. Rather, the operative date is the earliest effective filing date.

VIII. CONCLUSION

For the reasons set forth above, we (1) modify the ALJ's construction of the claim terms "top layer" and "thereon" recited in claim 1 of the '106 patent; (2) reverse the ALJ's finding that the accused μBGA products do not meet all of the limitations of the asserted claims of the '106 patent but affirm his finding that there is no infringement due to patent exhaustion for the Elpida products; (3) affirm the ALJ's finding that the accused wBGA products do not infringe the

asserted claims of the '106 patent; (4) affirm the ALJ's validity and domestic industry analyses pertaining to the asserted claims of the '106 patent; (5) affirm the ALJ's finding that the Direct Loading testing methodology employed by Complainant's expert fails to prove infringement; and (6) affirm the ALJ's finding that the 1989 Motorola OMPAC 68-pin chip package fails to anticipate claims 17 and 18 of the '977 patent under the on-sale bar provision of 35 U.S.C. § 102(b), but modify a portion of the ID. Nevertheless, we affirm his determination that Respondents did not violate section 337.

By order of the Commission.

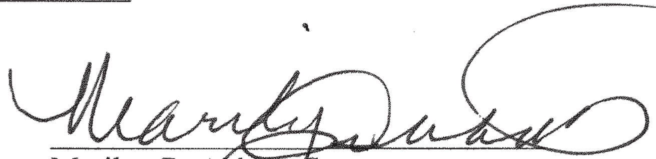
Marilyn R. Abbott
Secretary to the Commission

Issued: February 24, 2010

CERTAIN SEMICONDUCTOR CHIPS WITH MINIMIZED CHIP PACKAGE SIZE AND PRODUCTS CONTAINING SAME (III) **337-TA-630**

PUBLIC CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the attached **COMMISSION OPINION** has been served by hand upon the Commission Investigative Attorney, Kecia J. Reynolds, Esq., and the following parties as indicated, on February 24, 2010.



Marilyn R. Abbott, Secretary
U.S. International Trade Commission
500 E Street, SW
Washington, DC 20436

On Behalf of Complainant Tessera Incorporated:

Tom M. Schaumberg, Esq.
ADDUCI, MASTRIANI, SCHAUMBERG, LLP
1200 Seventeenth St., NW
Washington, DC 20036

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: ________

On Behalf of Respondents Acer, Incorporated, Acer America Corporation, Nanya Technology Corporation, Nanya Technology Corporation USA, and Powerchip Semiconductor Corporation:

G. Hopkins Guy, Esq.
ORRICK HERRINGTON & SUTCLIFFE LLP
1000 Marsh Road
Menlo Park, CA 94025-1015

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: ________

On Behalf of Respondents Kingston Technology Co., Incorporated and ProMOS Technologies Inc.:

Alan L. Unikel, Esq.
SEYFARTH SHAW LLP
131 South Dearborn Street, Suite 2400
Chicago, IL 60603

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: ________

On Behalf of Respondents Elpida Memory Inc., And Elpida Memory (USA) Incorporated:

Larry L. Shatzer, Esq.
FOLEY & LARDNER LLP
Washington Harbour
3000 K Street, NW, Suite 600
Washington, DC 20007-5143

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: ________

On Behalf of Respondent Smart Modular Technologies, Incorporated:

Jonathan M. James, Esq.
PERKINS COIE
2901 N. Central Avenue, Suite 2000
Phoenix, AZ 85012-2788

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: ________

On Behalf of Respondent Centon Electronics, Incorporated:

Joseph P. DiVincenzo, Esq.
REMER DIVINCENZO & GRIFFITH
2121 E. Pacific Coast Highway, Suite 280
Corona Del Mar, CA 92625

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: ________

On Behalf of Respondent Ramaxel Technology Ltd.:

Brian R. Nester, Esq.
SIDLEY AUSTIN LLP
1501 K Street, NW
Washington, DC 20005

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: ________

PUBLIC:

Heather Hall
LEXIS-NEXIS
9443 Springboro Pike
Dayton, OH 45342

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: ________

Kenneth Clair
THOMAS WEST
1100 Thirteen Street NW –Suite 200
Washington, DC 20005

( ) Via Hand Delivery
(✓) Via Overnight Mail
( ) Via First Class Mail
( ) Other: ________

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of CERTAIN SEMICONDUCTOR CHIPS WITH MINIMIZED CHIP PACKAGE SIZE AND PRODUCTS CONTAINING SAME (III)	Investigation No. 337-TA-630

INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND RECOMMENDED DETERMINATION ON REMEDY AND BOND

Administrative Law Judge Theodore R. Essex

(August 28, 2009)

Appearances:
For the Complainant Tessera, Inc.:

Wayne M. Barsky, Esq., H. Mark Lyon, Esq., Denis R. Salmon, Esq., Frederick S. Chung, Esq., Y. Ernest Hsin, Esq., Michael B. Smith, Esq., Jason C. Lo, Esq., and Sarah E. Piepmeier, Esq. of Gibson, Dunn & Crutcher, LLP of Los Angeles, CA.

Benjamin W. Hattenbach, Esq., Elliot N. Brown, Esq., and Kenneth Weatherwax, Esq. of Irell & Manella, LLP of Los Angeles, CA.

J. Anthony Downs, Esq., Scott L. Robertson, Esq., Jennifer A. Albert, Esq., and David M. Young, Esq. of Goodwin Proctor, LLP of Washington, DC

F. David Foster, Esq., and Barbara A. Murphy, Esq., of Miller & Chevalier Chartered of Washington, DC

For the Respondents Acer, Nanya and Powerchip:

G. Hopkins Guy, III, Esq., Mark Wine, Esq., Denise M. Mingrone, Esq., Sanjeet K, Dutta, Esq., and Brian Vanderzanden, Esq. of Orrick, Herrington & Sutcliffe, LLP of Denver, CO.

Cynthia Al.ison, Lock, Esq., of Orrick Herrington & Sutcliffe, LLP of Irvine, CA.

PUBLIC VERSION

For the Respondent A-DATA Technology:

Maureen F. Browne, Esq. of Heller Ehrman, LLP of Washington, DC.

For the Respondent Elpida Memory:

Larry L. Shatzer, Esq., Kenneth E. Krosin, Esq., George C. Beck, Esq., Shaun R. Snader, Esq., and Veronica S Ascarrunz, Esq. of Foley & Lardner, LLP of Washington, DC.

Gina A. Bibby, Esq., of Foley Lardner, LLP of Palo Alto, CA.

Michael R. Houston, Esq., of Foley Lardner, LLP of Chicago, IL.

For the Respondent Kingston Technology Co., Inc.:

Alan L. Unikel, Esq., Matthew A. Werber, Esq., of Seyfarth Shaw, LLP of Chicago, IL.

For the Respondent Promos Technologies, Inc.:

Alan L. Unikel, Esq., Matthew A. Werber, Esq., of Seyfarth Shaw, LLP of Chicago, IL.

For the Respondent Ramaxel Technology, Ltd.:

Timothy W. Riffe, Esq., Daniel X. Yan, Esq., Fish & Richardson, PC of Washington, DC.

For the Respondent Smart Modular Technologies, Inc.:

Michael A Oblon, Esq., of Perkins Coie, LLP of Washington, DC.

For the Commission Investigative Staff:
Lynn I. Levine, Esq., Director; Spence T. Chubb, Esq., Supervising Attorney; Kecia J. Reynolds, Esq., Investigative Attorney of the Office of Unfair Import Investigations, U.S. International Trade Commission, of Washington, D.C.

PUBLIC VERSION

Pursuant to the Notice of Investigation, 73 Fed. Reg. 2276 (2007), this is the Initial Determination of the investigation in the matter of *Certain Semiconductor Chips with Minimized Chip Package Size and Products Containing Same (III)*, United States International Trade Commission Investigation No. 337-TA-630. *See* 19 C.F.R. § 210.42(a).

It is held that no violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, has occurred in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain semiconductor chips with minimize chip package size and products containing same by reason of infringement of one or more of claims 17 and 18 of United States Patent No. 5,679,977; claims 1-4, 9-12, and 15-16 of United States Patent No. 6,133,627; and claims 1-4, 9, 10 and 33-35 of United States Patent No. 5,663,106.

The following abbreviations may be used in this Initial Determination:

CDX	Complainants' demonstrative exhibit
CFF	Complainants' proposed findings of fact
CIB	Complainants' initial post-hearing brief
CORFF	Complainants' objections to Respondents' proposed findings of fact
COSFF	Complainants' objections to Staff's proposed findings of fact
CPX	Complainants' physical exhibit
CRB	Complainants' reply post-hearing brief
CX	Complainants' exhibit
Dep.	Deposition
JSUF	Joint Statement of Undisputed Facts
JX	Joint Exhibit
RDX	Respondents' demonstrative exhibit
RFF	Respondents' proposed findings of fact
RIB	Respondents' initial post-hearing brief
ROCFF	Respondents' objections to Complainants' proposed findings of fact
ROSFF	Respondents' objections to Staff's proposed findings of fact
RPX	Respondents' physical exhibit
RRB	Respondents' reply post-hearing brief
RRX	Respondents' rebuttal exhibit
RX	Respondents' exhibit
SFF	Staff's proposed findings of fact
SIB	Staff's initial post-hearing brief
SOCFF	Staff's objections to Complainants' proposed findings of fact
SORFF	Staff's objections to Respondents' proposed findings of fact
SRB	Staff's reply post-hearing brief
Tr.	Transcript

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I. BACKGROUND

A. Institution and Procedural History of This Investigation

By publication of a notice in the *Federal Register* on January 14, 2008, pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, the Commission instituted Investigation No. 337-TA-630 with respect to U.S. Patent No. 5,663,106 ("the 106 patent"); U.S. Patent No. 5,679,977 ("the '977 patent"); U.S. Patent No. 6,133,627 ("the 627 patent"); and U.S. Patent No. 6,458,681 ("the '681 patent") to determine:

> [W]hether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain semiconductor chips with minimized chip package size or products containing same by reason of infringement of one or more of claims 1-4, 9, 10, and 33-35 of U.S. Patent No. 5,663,106; claims 17 and 18 of U.S. Patent No. 5,679,977; claims 1-4, 6, 9-12, 15, and 16 of U.S. Patent No. 6,133,627; and claim 4 of U.S. Patent No. 6,458,681 and whether an industry in the United States exists as required by subsection (a)(2) of section 337.

73 Fed. Reg. 2276 (2008).

Tessera, Inc. ("Tessera") of San Jose, California is the complainant. *Id.* The respondents named in the Notice of Investigation were: A-Data Technology Co., Ltd.; A-Data Technology (USA) Co., Ltd.; Acer Inc.; Acer America Corp.; Centon Electronics, Inc.; Elpida Memory, Inc.; International Products Sourcing, Group; Kingston Technology Corporation; Nanya Technology Corporation; Nanya Technology Corp. USA; Peripheral Devices & Products, d/b/a Patriot Memory; Powerchip Semiconductor Corp.; ProMos Technologies, Inc.; Ramaxel Technology, Ltd; SMART Modular Technologies, Inc.; TwinMOS Technologies, Inc.; and TwinMOS Technologies, USA, Inc (collectively "Respondents"). *Id.* The Commission Investigative Staff ("Staff") of the Commission's Office of Unfair Import Investigations is also a party in this

investigation. *Id.* The investigation was originally assigned to Administrative Law Judge Bullock. *Id.*

On May 29, 2008, Judge Bullock terminated the investigation as to the '681 patent. (Order No. 16.) On June 20, 2008, the Commission determined not to review the order. (*See* Notice of Commission Determination Not to Review an Initial Determination Granting Complainant's Motion for Partial Termination of the Investigation with Respect to U.S. Patent No. 6,458,681.)

On June 16, 2008, Judge Bullock terminated the investigation as to respondent International Sourcing Group, Inc. ("ISPG") based on consent order and settlement agreement. (Order No. 17.) On July 14, 2008, the Commission determined not to review the order. (*See* Notice of Commission Determination Not to Review an Initial Determination Granting Joint Motion to Terminate Investigation as to One Respondent Based on Consent Order and Settlement Agreement.)

On July 11, 2008, this investigation was reassigned to this ALJ. (*See* Notice of a Commission Decision to Reassign Certain Section 337 Investigations.)

On September 4, 2008, the ALJ terminated the investigation as to respondent Peripheral Devices and Product Systems d/b/a Patriot Memory based on consent order and settlement agreement. (Order No. 25.) On October 2, 2008, the Commission determined not to review the order. (*See* Notice Of Commission Determination Not To Review an Initial Determination Granting a Joint Motion to Terminate the Investigation as to Respondent Patriot Memory Based on a Consent Order and Settlement Agreement; Issuance Of Consent Order.)

On September 16, 2008, the ALJ granted Tessera's motion for summary determination that it had satisfied the domestic industry requirement. (Order No. 31.) On October 8, 2008, the

Commission determined not to review the order. (*See* Notice of Commission Determination Not to Review an Initial Determination Granting Tessera's Motion for Summary Determination That It Has Satisfied the Domestic Industry Requirement.)

On September 19, 2008, the ALJ granted Tessera's motion to withdraw claim 6 of the '627 patent. (Hearing Tr. at 95:23-25.)

The evidentiary hearing on the question of violation of section 337 commenced on September 19, 2008, and concluded on October 3, 2008. Tessera; A-Data Technology Co., Ltd.; A-Data Technology (USA) Co., Ltd.; Acer Inc.; Acer America Corp.; Centon Electronics, Inc.; Elpida Memory, Inc.; International Products Sourcing, Group; Kingston Technology Corporation; Nanya Technology Corporation; Nanya Technology Corp. USA; Peripheral Devices & Products, d/b/a Patriot Memory; Powerchip Semiconductor Corp.; ProMos Technologies, Inc.; Ramaxel Technology, Ltd; SMART Modular Technologies, Inc.; and Staff were represented at the hearing. (Hearing Tr. 1:1-6:8.)

On September 22, 2008, the ALJ issued an Initial Determination terminating respondent A-Data from this investigation based on consent order. (Order No. 35.) On October 23, 2008, the Commission determined not to review the order. (*See* Notice of Commission Determination Not to Review an Initial Determination Granting the Motion of Respondent A-Data Technology Co., Ltd., and A-Data Technology (USA) Co. to Terminate the Investigation as to Them Based on a Consent Order; Issuance of Consent Order.)

On January 2, 2009, the ALJ extended the target date in this investigation to July 6, 2009 due to his case load and obligations in other investigations. (Order No. 39.) On January 21, 2009, the Commission determined not to review the initial determination extending the target date. (*See* Notice of Commission Decision Not to Review an Initial Determination Extending the

Target Date for Completion of This Investigation (January 21, 2009).) Shortly thereafter, on January 30, 2009, the Commission issued its decision to review in part the final initial determination finding no violation of Section 337 in Investigation No. 337-TA-605 ("the 605 Investigation"). (*See* Notice of Commission Decision to Review in Part a Final Initial Determination Finding No Violation of Section 337 (January 30, 2009).) Based on the Commission's decision to review in part the final initial determination in the 605 Investigation, the ALJ extended the target date in this Investigation based on the relatedness of the patents at issue in both investigations as well as based on the fact that the Commission was reviewing the methodology used by Tessera in the 605 Investigation, which is the same method used in this Investigation to prove infringement. (*See* Order No. 40. (February 12, 2009).) The Commission determined not to review the initial determination extending the target date. (*See* Notice of Commission Decision Not to Review an Initial Determination Extending the Target Date for Completion of This Investigation (March 9, 2009).)

On April 2, 2009, the ALJ extended the target date in this investigation to November 17, 2009, based on the Commission's decision to request additional briefing on remedy and to extend the target date in the 605 Investigation. (*See* Order No. 41 (April 2, 2009).) On April 23, 2009, the Commission determined not to review the initial determination extending the target date. (*See* Notice of Commission Decision Not to Review an Initial Determination Extending the Target Date for Completion of This Investigation (April 23, 2009).)

On May 20, 2009, the Commission issued its opinion in the 605 Investigation. *See Certain Semiconductor Chips With Minimized Chip Package Size and Products Containing Same,* Inv. No. 337-TA-605, Commission Opinion (May 20, 2009). On June 3, 2009, the Commission issued a public version of its opinion. *See Certain Semiconductor Chips With*

Minimized Chip Package Size and Products Containing Same, Inv. No. 337-TA-605, Commission Opinion (Public Version) (May 20, 2009) ("605 Comm'n Op.").

On June 12, 2009, the ALJ issued Order No. 43 where he sought supplemental briefing on "how the Commission's Opinion in the '605 Investigation and its findings on Dr. Qu's infringement analysis will affect the ALJ's analysis in this investigation, if at all." (Order No. 43 at 2.) In light of the supplemental briefing, the ALJ extended the target date in this investigation to December 29, 2009 with the final initial determination on violation will be due no later than the close of business on August 28, 2009. (*See* Order No. 43 (June 12, 2009).) On July 13, 2009, the Commission determined not to review the order. (*See* Notice of Commission Determination Not to Review an Initial Determination Extending the Target Date for Completion of the Investigation by Six Weeks.)

B. The Parties

1. Tessera, Inc.

Tessera, Inc. is a Delaware corporation having a principal place of business in San Jose, California with facilities in North Carolina and Yokoham, Japan. (CX-06488C at Q. 29.) Tessera's primary business is licensing its technology, although it has a small manufacturing business. (*Id.* at Q. 21.) Tessera's primary source of income is through licensing of its intellectual property in the semiconductor chip packaging industry. (*Id.* at Q. 22.)

2. Acer Respondents

Acer Inc. is a Taiwanese corporation located in Taipei, Taiwan. Acer America Corp. is located in San Jose, California. (RX-19C at Q. 11.) Acer and Acer America are generally in the business of selling personal computer systems and servers. (*Id.* at Qs. 9, 11.) Acer is not in the

business of packaging or selling DRAMs, but rather purchases DRAMs from DRAM suppliers. (*Id.* at Q.15.)

3. Elpida Respondents

Elpida Memory, Inc. is a Japanese corporation located in Tokyo, Japan. Elpida Memory, Inc. is in the business of, *inter alia*, manufacturing DRAM chips and selling packaged DRAM chips and DRAM modules. (*See* RX-16C at Qs.13-14.) Elpida uses subcontractors to package DRAM chips that it manufacturers (Nakashima Tr. at 2418:20-23), and Elpida Memory (USA), Inc., is a subsidiary of Elpida Memory, Inc. and is located in Sunnyvale, California. (*See* RX-16C at p.4, Q. 22; Respondents' Pre-Hearing Statement at 14.) Elpida USA distributes Elpida's products in the United States. (*Id.*)

4. Kingston Technology

Kingston Technology Co., Inc. is a privately-held designer and manufacturer of memory modules and flash storage products with its headquarters in Fountain Valley, California. No corporate representative testified on behalf of Kingston during the hearing.

5. Nanya Respondents

Nanya Technology Corporation is a Taiwanese corporation located in Taoyuan, Taiwan. Respondent Nanya Technology Corp. USA is a United States-based subsidiary of Nanya. (RX-17C at Q. 8.) Nanya is in the business of, *inter alia,* selling various DRAM products, including DRAM devices and DRAM modules. (*Id.* at Q. 12.) Nanya does not package its own BGA DRAM chips. (*Id.* at Q.13.) Rather, Nanya uses subcontractors to assemble and package Nanya's BGA DRAM chips. (*Id.*)

6. Powerchip Semiconductor

Powerchip Semiconductor Corporation is a Taiwanese corporation located in Hsinchu, Taiwan. (RX-18C at Q. 8.) Powerchip is in the business of manufacturing and selling DRAM products. *Id.* Powerchip uses subcontractors to package its BGA DRAM chips. (*Id.*)

7. ProMOS Technologies, Inc.

ProMOS Technologies, Inc. is a semiconductor company based in Hsinchu, Taiwan. (RX-1930C at Q. 9.) ProMos sells packaged DRAM chips and memory modules to electronics manufacturers and computer companies, respectively. (*Id.*) ProMos also provides semiconductor wafer foundry services for customers. (*Id.*) ProMos relies on subcontractors its DRAM chips and assembly memory modules. (*Id.* at Q. 18.)

8. Ramaxel Technology Ltd.

Ramaxel Technology Ltd. Is a Chinese company incorporated and headquartered in Hong Kong, China. It is a developer and manufacturer of memory modules and supplies these modules to computer and server manufacturers. Ramaxel purchases packaged DRAM chips from external sources, such as Elpida, and incorporates those packaged DRAM chips into its modules. No corporate witness testified on behalf of Ramaxel during the hearing.

9. SMART Modular Technologies, Inc.

SMART Modular Technologies, Inc., is a Cayman Island corporation with its principal place of business in Fremont, California. SMART designs and manufactures DRAM memory modules for use in products such as servers, personal computers, and other electronic devices. (RX-20C at Q. 8.) SMART also buyers and resells packaged DRAM chips and DRAM memory modules. (*Id.*)

10. TwinMOS Respondents

TwimMOS did not file a response to the Complaint and never made an appearance in this investigation. Tessera moved for an order to show cause why TwinMOS should not be found in default and such an order was issued. (*See* Order No. 12 (Mar.12, 2008).) TwinMOS failed to respond to that order. TwinMOS did not appear at the hearing, and no one testified on behalf of TwinMOS during the hearing. On this same day, the ALJ issued an Initial Determination finding TwinMOS in default. (*See* Order No. 46 (Aug. 28, 2009).)

C. Overview of the Technology

This investigation involves both semiconductor chip packages and a process for encapsulating certain semiconductor chip packages. (CX-06489C at Q. 22.) The technology at issue in the '977 and '627 Patents is generally directed to specific semiconductor chip assemblies. *See* JX-00001 (the '977 Patent) and JX-00002 (the '627 Patent). The '106 Patent is generally directed to a method of encapsulating small format BGA semiconductor chip packages, including DRAM chip packages. (*See* JX-00003 (the '106 Patent).)

DRAM chips are memory storage units and are used in electronic devices, such as computers, PDAs (Smartphones), and digital cameras. (CX-06489C at Q. 22.) DRAM chips are packaged so as to protect the chip from damage and to connect the chip both electronically and mechanically to an external device, such as printed circuit board (PCB). (*Id.* at Q. 29.) DRAM chip packages may be used singularly or in a bundle (known as a memory module, where several DRAM chip packages are attached to a single PCB) in an electronic device. (CX-06488C at Q 16.) There are several specific types of DRAM at issue in this investigation, e.g., DDR, DDR2, and DDR3. (CX-6486C at Qs. 30-31.) DDR ("Double-Data-Rate Synchronous Dynamic

Random Access Memory") is a type of very fast computer memory, and DDR2 and DDR3 are the subsequent versions or next generations of DDR. (*Id.*)

DRAM chip packages may be manufactured as ball grid array "BGA" packages. (CX-6486C at Q. 66.) The BGA packages at issue in this investigation are either in the "face-up" or "face-down" orientation. (*Id.* at Q. 99.) The orientation of a chip package is determined based on the orientation of the "face" of the semiconductor chip, which is the surface of the chip that contains the circuitry and contacts for electrical connection. (*Id.* at Q. 37.) In a "face-up" BGA, the face points away from the PCB, whereas in a "face-down" BGA, the face points in the direction of the PCB. (*Id.*)

The heat generated by the semiconductor caused a problem that affects the chip packaging because heat causes different materials to expand at different rates and different amounts. (*Id.* at Q. 52.) Because a semiconductor chip has a much lower coefficient thermal of expansion ("CTE") than the PCB to which the chip package is attached, the package substrate beneath the chip tends to be constrained by the chip during heating and, like the chip itself, expands much less that the PCB. (*Id.* at Q. 53.) Specifically, when an integrated circuit package heats up and cools down, through repeated cycles, the PCB and the chip will expand and contract differently. (*Id.*) This can result in the bottom of the solder balls that connect the chip package to the PCB being pulled outward relative to the top of the solder ball where it connects to the chip package terminal so that the shape of the solder ball becomes distorted or deformed. (*Id.* at Qs. 56-58.) When the PCB and package are cooled, the bottom of the solder balls can be pulled back relative to the solder pad at the top of the solder ball and terminal. (*Id.*) These repeated cycles of heating and cooling cause strain on the solder balls, and can lead to solder fatigue and ultimately to package failure. (*Id.*)

To improve the reliability of the DRAM chips, an encapsulation process, as described in the '106 patent, is used where the chip package is encapsulated with an encapsulation material before it is attached to the PCB. (*See* CX-06482C at Q. 27.)

D. The Patents At Issue

This investigation pertains to three patents: U.S. Patent No. 5,663,106 ("the '106 Patent"), U.S. Patent No. 5,679,977 ("the '977 Patent") and U.S. Patent No. 6,133,627 ("the '627 Patent").

1. The '106 Patent

The asserted claims of the '106 Patent, entitled "Method of Encapsulating Die and Chip Carrier," are claims 1-4, 9, 10 and 33-35.

The asserted claims read as follows:

> 1. A method of encapsulating a semiconductor chip assembly having a top layer with an array of exposed terminals thereon, the terminals being electrically connected to the chip, said method comprising the steps of:
>
> placing an encapsulant barrier adjacent the semiconductor chip assembly, said encapsulant barrier at least partially defining an encapsulation area;
>
> providing a protective barrier in contact with said top layer for protecting the terminals on the top layer from an encapsulation material; and
>
> introducing an encapsulation material into at least a portion of the encapsulation area so that the encapsulation material flows to fill the encapsulation area and then cures to a substantially solid condition, the protective barrier preventing the encapsulation material from contacting the terminals on the top layer.
>
> 2. The method in claim 1, wherein said encapsulation material is a curable material which is in liquid form when introduced into said encapsulation area.
>
> 3. The method in claim 2, further comprising the step of curing said curable material after said curable material has been introduced into said encapsulation area.
>
> 4. The method in claim 3, wherein the curing step includes heating said curable material.

9. The method in claim 1, wherein said placing step includes placing said encapsulant barrier a spaced distance from the periphery of said semiconductor chip.

10. The method in claim 1, wherein said encapsulant barrier in said placing step is at least a portion of a mold, and further comprising the step of removing the mold after the encapsulation material is at least partially cured.

33. The method in claim 1, wherein said top layer is a spaced distance above said semiconductor chip, and further comprising the step of supporting said top layer above said semiconductor at least during said providing step.

34. The method in claim 33, wherein said step of supporting said top layer includes providing a compliant layer between said top layer and said chip.

35. The method in claim 1, wherein said protective barrier is a cap which engages by said top layer and covers said terminals.

(JX-00003.) The '106 Patent names Messrs. Konstantine Karavakis, Thomas H. Distefano, John W. Smith Jr. and Craig Mitchell as the inventors. (*See Id.*)

2. The '977 Patent

The asserted claims of the '977 Patent, entitled "Semiconductor Chip Assemblies, Methods of Making Same and Components for Same," in this investigation are claims 17 and 18.

Claims 17 and 18 read as follows:

17. A semiconductor chip assembly comprising:

(a) a semiconductor chip having a plurality of surfaces and having contacts on at least one said surface;

(b) a plurality of terminals, at least some of said terminals overlying one said surface of said chip;

(c) a layer of a compliant material disposed between said terminals and said chip and supporting at least some of said terminals above said one said surface of said chip; and

(d) flexible leads interconnecting said terminals with said contacts on said chip so that said terminals are movable with respect to said contacts.

18. A semiconductor chip assembly comprising:

(a) a semiconductor chip having a front surface and having contacts on said front surface;

(b) a plurality of terminals, at least some of said terminals overlying said front surface of said chip;

(c) a layer of a compliant material disposed between said terminals and said chip and supporting at least some of said terminals above said front surface; and

(d) flexible leads interconnecting said terminals with said contacts on said chip so that said terminals are movable with respect to said contacts.

(JX-00001.) The '977 Patent names Mssrs. Igor Y. Khandros and Thomas H. Distefano as the inventors. (*Id.*)

3. The '627 Patent

The asserted claims of the '627 Patent, entitled "Semiconductor Chip Package with Center Contacts," in this investigation are claims 1-4, 9-12, and 15-16.

The asserted claims read as follows:

1. A semiconductor chip assembly comprising:

(a) a semiconductor chip having a front surface defining the top of the chip, said front surface including a central region and a peripheral region surrounding said central region, whereby said central region is disposed inwardly of said peripheral region, said chip having central contacts disposed in said central region of said front surface;

(b) a dielectric element overlying said chip front surface, said dielectric element having a first surface facing toward said chip and a second surface facing away from said chip, said dielectric element having a hole encompassing said central contacts and an edge bounding said hole;

(c) a plurality of terminals disposed on said dielectric element for interconnection to a substrate and overlying said chip front surface; and

(d) a plurality of central contact leads extending between at least some of said central contacts and at least some of said terminals, each said central contact lead having a terminal end connected to one of said terminals and a contact end extending to one of said central contacts, said terminals being movable with

respect to said central contacts so as to compensate for thermal expansion of said chip.

2. A chip assembly as claimed in claim 1, wherein the terminal end of each said central contact lead is integrally formed with one of said terminals.

3. A chip assembly as claimed in claim 2, wherein said central contact leads are flexible.

4. A chip assembly as claimed in claim 1, wherein said dielectric element includes a compliant layer of a low modulus material, said compliant layer being disposed beneath said terminals.

9. A chip assembly as claimed in claim 1, wherein some of said terminals are disposed adjacent the edge bounding said hole.

10. A chip assembly as claimed in claim 1, wherein said plurality of terminals are disposed at said second surface of said dielectric element.

11. A chip assembly as claimed in claim 1 wherein the contact leads include wire bonds.

12. A semiconductor chip assembly comprising:

(a) a semiconductor chip having a front surface defining the top of the chip, said front surface including a central region and a peripheral region surrounding said central region, whereby said central region is disposed inwardly of said peripheral region, said chip having central contacts disposed in said central region of said front surface;

(b) a dielectric element overlying said chip front surface, said dielectric element having a first surface facing toward said chip and a second surface facing away from said chip;

(c) a plurality of terminals disposed on said dielectric element for interconnection to a substrate and overlying said chip front surface, said terminals being electrically connected to said central contacts and being movable with respect to said central contacts so as to compensate for thermal expansion of said chip.

15. A chip assembly as claimed in claim 12, wherein said plurality of terminals are disposed at said second surface of said dielectric element.

16. A chip assembly as claimed in claim 12 wherein said dielectric element includes as compliant layer disposed between said terminals and said front surface of said chip.

(JX-00002.) The '627 Patent names Mssrs. Igor Y. Khandros and Thomas H. Distefano as the inventors. (*Id.*)

E. The Products At Issue

The products at issue in this investigation are center-channel single DRAM chip packages in the face-down and face-up orientations, and multi-DRAM chip stacked configuration packages. (*See* CX-06486C at Q. 494.) The large majority of the accused products are single DRAM chip packages in the face down orientation. (*Id.*) DRAM memory modules, which are made up of several DRAM chips packages, and consumer products, such as computers, PDAs or Smartphones, and digital cameras that contain either a DRAM chip package or a memory module, are also at issue in this investigation. (CX-06489C at Q. 22.)

Each of the Respondents manufactures or sells DRAM chip package, memory modules, and/or consumer electronic products containing either DRAM chip packages or memory modules. (*See* CX-06488C at Q. 15.) Tessera does not manufacturer products meeting the description of the accused products at issue. (*Id.* at Q. 17.) Instead, as a noted previously, Tessera's business is in developing and licensing technologies. (*Id.*)

II. IMPORTATION OR SALE

The importation or sale requirement of section 337 has not been contested. (*See generally* RIB and RRB; *see also* RRCPFF IV. A.-J.) The evidence shows that each of the Respondents imported, sold for importation, and/or sold within the United States after importation at least one of the accused DRAM chip packages, memory modules containing the chip packages, and/or consumer products containing either the chip packages or the memory modules. (*See* CX-06489C at Qs. 24-34, 37.)

III. CLAIM CONSTRUCTION

A. Applicable Law

Pursuant to the Commission's Notices of Investigation, this investigation is a patent-based investigation. *See* 73 Fed. Reg. 2276 (2008). Accordingly, all of the unfair acts alleged by Tessera to have occurred are instances of alleged infringement of the '106 Patent, the '977 Patent and/or the '627 Patent. A finding of infringement or non-infringement requires a two-step analytical approach. First, the asserted patent claims must be construed as a matter of law to determine their proper scope.[1] Claim interpretation is a question of law. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (*en banc*), *aff'd*, 517 U.S. 370 (1996); *Cybor Corp. v. FAS Techs., Inc.*, 138 F.3d 1448, 1455 (Fed. Cir. 1998). Second, a factual determination must be made as to whether the properly construed claims read on the accused devices. 52 F.3d at 976.

In construing claims, the ALJ should first look to intrinsic evidence, which consists of the language of the claims, the patent's specification, and the prosecution history, as such evidence "is the most significant source of the legally operative meaning of disputed claim language." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996); *see also Bell Atl. Network Servs., Inc. v. Covad Comm'n. Group, Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001). The words of the claims "define the scope of the patented invention." *Id.* And, the claims themselves "provide substantial guidance as to the meaning of particular claim terms." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005), *cert. denied*, 546 U.S. 1170 (2006). It is essential to consider a claim as a whole when construing each term, because the context in which a term is used in a claim "can be highly instructive." *Id.* Claim terms are presumed to be used

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[1] Only claim terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Vanderlande Indus. Nederland BV v. Int'l Trade Comm.*, 366 F.3d 1311, 1323 (Fed. Cir. 2004); *Vivid Tech., Inc. v. American Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

consistently throughout the patent, such that the usage of the term in one claim can often illuminate the meaning of the same term in other claims. *Research Plastics, Inc. v. Federal Pkg. Corp.*, 421 F.3d 1290, 1295 (Fed. Cir. 2005). In addition:

> . . . in clarifying the meaning of claim terms, courts are free to use words that do not appear in the claim so long as the resulting claim interpretation . . . accord[s] with the words chosen by the patentee to stake out the boundary of the claimed property.

Pause Tech., Inc. v. TIVO, Inc., 419 F.3d 1326, 1333 (Fed. Cir. 2005).

Some claim terms do not have particular meaning in a field of art, in which case claim construction involves little more than applying the widely accepted meaning of commonly understood words. *Phillips*, 415 F.3d at 1314. Under such circumstances, a general purpose dictionary may be of use.[2] The presumption of ordinary meaning, however, will be "rebutted if the inventor has disavowed or disclaimed scope of coverage, by using words or expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope." *ACTV, Inc. v. Walt Disney Co.*, 346 F.3d 1082, 1091 (Fed. Cir. 2003).

Sometimes a claim term will have a specialized meaning in a field of art, in which case it is necessary to determine what a person of ordinary skill in that field of art would understand the disputed claim language to mean, viewing the claim terms in the context of the entire patent. *Phillips*, 415 F.3d at 1312-14; *Vitronics*, 90 F.3d at 1582. Under such circumstances, the ALJ must conduct an analysis of the words of the claims themselves, the patent specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, as well as the meaning of technical terms and the state of the art. *Id.*

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[2] Use of a dictionary, however, may extend patent protection beyond that to which a patent should properly be afforded. There is also no guarantee that a term is used the same way in a treatise as it would be by a patentee. *Id.* at 1322.

A patentee may deviate from the conventional meaning of claim term by making his or her intended meaning clear (1) in the specification and/or (2) during the patent's prosecution history. *Lear Siegler, Inc. v. Aeroquip Corp.*, 733 F.2d 881, 889 (Fed. Cir. 1984). If a claim term is defined contrary to the meaning given to it by those of ordinary skill in the art, the specification must communicate a deliberate and clear preference for the alternate definition. *Kumar v. Ovonic Battery Co.*, 351 F.3d 1364, 1368 (Fed. Cir. 2003). In other words, the intrinsic evidence must "clearly set forth" or "clearly redefine" a claim term so as to put one reasonably skilled in the art on notice that the patentee intended to so redefine the claim term. *Bell Atl.*, 262 F.3d at 1268.

When the meaning of a claim term is uncertain, the specification is usually the first and best place to look, aside from the claim itself, in order to find that meaning. *Phillips*, 415 F.3d at 1315. The specification of a patent "acts as a dictionary" both "when it expressly defines terms used in the claims" and "when it defines terms by implication." *Vitronics*, 90 F.3d at 1582. For example, the specification "may define claim terms by implication such that the meaning may be found in or ascertained by a reading of the patent documents." *Phillips*, 415 F.3d at 1323. "The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." *Id.* at 1316. However, as a general rule, particular examples or embodiments discussed in the specification are not to be read into the claims as limitations. *Markman*, 52 F.3d at 979.

The prosecution history "provides evidence of how the inventor and the PTO understood the patent." *Phillips*, 415 F.3d at 1317. For example, the prosecution history may inform the meaning of the claim language by demonstrating how an inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope

narrower than it otherwise would be. *Vitronics*, 90 F.3d at 1582-83; *see also Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) (stating, "The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution."); *Microsoft Corp. v. Multi-tech Sys., Inc.*, 357 F.3d 1340, 1350 (Fed. Cir. 2004) (stating, "We have held that a statement made by the patentee during prosecution history of a patent in the same family as the patent-in-suit can operate as a disclaimer."). The prosecution history includes the prior art cited, *Phillips*, 415 F.3d at 1317, as well as any reexamination of the patent. *Intermatic Inc. v. Lamson & Sessions Co.*, 273 F.3d 1355, 1367 (Fed. Cir. 2001).

Differences between claims may be helpful in understanding the meaning of claim terms. *Phillips*, 415 F.3d at 1314. A claim construction that gives meaning to all the terms of a claim is preferred over one that does not do so. *Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005), *cert. denied*, 546 U.S. 972 (2005); *Alza Corp. v. Mylan Labs. Inc.*, 391 F.3d 1365, 1370 (Fed. Cir. 2004). In addition, the presence of a specific limitation in a dependent claim raises a presumption that the limitation is not present in the independent claim. *Phillips*, 415 F.3d at 1315. This presumption of claim differentiation is especially strong when the only difference between the independent and dependent claim is the limitation in dispute. *SunRace Roots Enter. Co., v. SRAM Corp.*, 336 F.3d 1298, 1303 (Fed. Cir. 2003). "[C]laim differentiation takes on relevance in the context of a claim construction that would render additional, or different, language in another independent claim superfluous." *AllVoice Computing PLC v. Nuance Comm'ns, Inc.*, 504 F.3d 1236, 1247 (Fed. Cir. 2007).

The preamble of a claim may also be significant in interpreting that claim. The preamble is generally not construed to be a limitation on a claim. *Bell Comm'ns Research, Inc. v. Vitalink Comm'ns Corp.*, 55 F.3d 615, 620 (Fed. Cir. 1995). However, the Federal Circuit has stated that:

> [A] claim preamble has the import that the claim as a whole suggests for it. In other words, when the claim drafter chooses to use both the preamble and the body to define the subject matter of the claimed invention, the invention so defined, and not some other, is the one the patent protects.

Eaton Corp. v. Rockwell Int'l Corp., 323 F.3d 1332, 1339 (Fed. Cir. 2003). If said preamble, when read in the context of an entire claim, recites limitations of the claim, or if the claim preamble is "necessary to give life, meaning, and vitality" to the claim, then the claim preamble should be construed as if in the balance of the claim. *Kropa v. Robie*, 187 F.2d 150, 152 (CCPA 1951); *see also Rowe v. Dror*, 112 F.3d 473, 478 (Fed. Cir. 1997); *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251, 1257 (Fed. Cir. 1989). In addition:

> [W]hen discussing the "claim" in such a circumstance, there is no meaningful distinction to be drawn between the claim preamble and the rest of the claim, for only together do they comprise the "claim." If, however, the body of the claim fully and intrinsically sets forth the complete invention, including all of its limitations, and the preamble offers no distinct definition of any of the claimed invention's limitations, but rather merely states the purpose or intended use of the invention, then the preamble may have no significance to claim construction because it cannot be said to constitute or explain a claim limitation.

Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1305 (Fed. Cir. 1999).

In *Pitney Bowes*, the claim preamble stated that the patent claimed a method of, or apparatus for, "producing on a photoreceptor an image of generated shapes made up of spots." *Id.* at 1306. The Federal Circuit found that this was not merely a statement describing the invention's intended field of use, but rather that said statement was intimately meshed with the ensuing language in the claim. *Id.* For example, both of the patent's independent claims concluded with the clause, "whereby the appearance of smoothed edges are given to the

generated shapes." *Id.* Because this was the first appearance in the claim body of the term "generated shapes," the Court found that it could only be understood in the context of the preamble statement "producing on a photoreceptor an image of generated shapes made up of spots." *Id.* The Court concluded that it was essential that the preamble and the remainder of the claim be construed as one unified and internally consistent recitation of the claimed invention. *Id.*

Finally, when the intrinsic evidence does not establish the meaning of a claim, the ALJ may consider extrinsic evidence, *i.e.*, all evidence external to the patent and the prosecution history, including inventor testimony, expert testimony and learned treatises. *Phillips*, 415 F.3d at 1317. Extrinsic evidence may be helpful in explaining scientific principles, the meaning of technical terms, and terms of art. *Vitronics*, 90 F.3d at 1583; *Markman*, 52 F.3d at 980. However, the Federal Circuit has generally viewed extrinsic evidence as less reliable than the patent itself and its prosecution history in determining how to define claim terms. *Phillips*, 415 F.3d at 1318. With respect to expert witnesses, any testimony that is clearly at odds with the claim construction mandated by the claims themselves, the patent specification, and the prosecution history should be discounted. *Id.* at 1318.

If the meaning of a claim term remains ambiguous after a review of the intrinsic and extrinsic evidence, then the patent claims should be construed so as to maintain their validity. *Id.* at 1327. However, if the only reasonable interpretation renders a claim invalid, then the claim should be found invalid. *See Rhine v. Casio, Inc.*, 183 F.3d 1342, 1345 (Fed. Cir. 1999).

B. The Level of Ordinary Skill in the Art

1. The '106 Patent

Tessera asserts that a person of ordinary skill in the art in the 1993-94 time frame would have a Bachelor of Science degree in engineering and a few years of experience in electronics packaging, or an equivalent combination of education and/or experience. (*See* CIB at 21.) Neither Respondents nor Staff disagree with Tessera's position. (*See* ROCFF VI.417 and SOCFF VI.417.) Therefore, the ALJ finds one of ordinary skill in the art during the 1993-94 time frame would have Bachelor of Science degree in engineering and a few years of experience in electronics packaging, or an equivalent combination of education and/or experience.

2. The '977 and '627 Patents

Tessera asserts that a person of ordinary skill in the art to which the '627 and '927 patents pertain is someone with a Bachelor's degree in engineering and a few years of experience in electronic packaging, or an equivalent combination of education and/or experience. (*See* CX-6486C (Qu DWS) at Qs. 71-72.) Respondents offer two different standards. Respondents' expert Dr. Ulrich asserts that a person of ordinary skill in the art is someone with at least a bachelor's degree in either some area of engineering or a natural science such as physics and chemistry and with about three years experience in the field of semiconductor packaging, manufacture, research or development. (*See* RX-1C (Ulrich DWS) at Q. 84.) According to Dr. Ulrich, graduate work is not a substitute for the three years experience. (*Id.* at Q. 85.) Contrary to Dr. Ulrich, Respondents' expert Dr. Clech testified that a person of ordinary skill in the art could have a Master's degree without the three years experience. (*See* RX-3C (Clech DWS) at Q. 23.) The Staff argues that the evidence supports Tessera's definition of one of ordinary skill in the art. (SIB at 15.)

Tessera's and Respondents' definitions of one of ordinary skill in the art are very similar, especially when considering Dr. Clech's testimony as described above. Accordingly, the ALJ finds based on the record evidence that one of ordinary skill in the art at the time of the invention is someone with at least a Bachelor's degree in engineering or a natural science, such as physics and chemistry, and with a few years of experience in electronic packaging or manufacture, or an equivalent combination of education and/or experience.

C. The Disputed Claim Terms and Their Proper Construction

1. The '106 Patent

a) Claim 1

(1) "Top Layer"

Tessera argues that "top layer" should be construed to mean "a layer disposed upward of the active surface of the chip and which carries the terminals." (SIB at 73.[3]) The "top layer" under Tessera's construction encompasses an orientational element, namely that the top layer is in an upward direction from the face of the chip. (CRB at 23.) Tessera further asserts that the "top layer" need not be limited to a single layer, but can encompass a composite layer as well. (CRB at 22-23.)

[3] Tessera and Staff note that Tessera had inadvertently omitted its analysis of the parties' construction from its post hearing brief, but that it had filed several proposed findings of fact regarding the term, and therefore the omission should not be construed as a waiver of its arguments. CRB at 22, note 17; *see also* CPFF V.435-470. To the extent Tessera included their proposed construction for "top layer" within their findings of fact, the ALJ finds such action impermissible because the findings of fact are to be confined to facts, not argument. Additionally, including arguments in the findings of fact would improperly circumvent the page limits imposed on the parties in this investigation. Moreover, Ground Rule 11.1 states that "[t]he post-trial brief shall discuss the issues and evidence tried within the framework of the general issues determined by the Commission's Notice of Investigation, the general outline of the briefs as set forth in Appendix B, and those issues that are included in the pre-trial brief and any permitted amendments thereto. All other issues shall be deemed waived." Tessera's failure to provide any argument regarding "top layer" is a violation of Ground Rule 11.1. Accordingly, the ALJ finds that Tessera has waived any such arguments.

Respondents' construction is "the outer layer of the chip assembly upon which the terminals are fixed." (*See* RIB at 50.) Respondents further assert that the "top layer" refers to a single layer. (*Id.*)

Staff argues that the term should be given its plain and ordinary meaning, but if that the ALJ determines to construe the claim term; it should mean "a layer on the active side of the chip that carries the terminals." (SIB at 73.)

The ALJ finds that "top layer" means a single layer. Claims should be given their ordinary and customary meaning as understood by a person of ordinary skill in the art, viewing the claim terms in the context of the entire patent. *Phillips v. AWH Corp.,* 415 F.3d 1303, 1312-13 (Fed. Cir. 2005), *cert. denied*, 546 U.S. 1170 (2006). Here, one of ordinary skill in the art at the time of invention would understand the term to refer to a single layer. (RX-9C(a) at Qs.361, 364; RX-280 at 112; RX-281 at 1281.) In addition, the specification of the '106 Patent supports such a construction. The specification, in describing Figure 1, describes a semiconductor chip and chip carrier, wherein "[t]he chip carrier 14 is made up of a top layer 16 (preferably a polyimide layer or the like) and an elastomeric pad 20 disposed between the top layer 16 and the semiconductor chip 12." (JX-00003 (the '106 Patent) at 5:8-13; Figure 1.) Other embodiments in the '106 Patent similarly describe the top layer as separate and distinct from the elastomeric pad, which in combination form the chip carrier. (*See id.* at 7:22-26; 9:1-4; Figures 9 and 13.) Thus, the '106 Patent specification explicitly distinguishes the different layers, *e.g.* "top layer" and "elastomeric" layer of the chip carrier.

In addition, the '611 Patent and the '265 patent, which are incorporated by reference into the '106 Patent, further support such a construction. Specifically, the '265 patent specification describes an interposer, which is a component of the chip carrier, as "includ[ing] a flexible top

layer 38 (FIG.3) formed by a thin sheet of material having a relatively high elastic modulus and a compliant bottom layer formed from a material having a relatively low elastic modulus." ('265 patent 9:50-54.) Similarly, the '611 patent describes a single "dielectric layer" that carries the terminals, *i.e.*, the dielectric layer is the "top layer" in the '611 patent. ('611 patent at 4:23-25.) Thus, in both the '611 Patent and the '265 Patent, the term "layer" refers to a single layer.

The ALJ finds that the term "top layer" means "an outer layer of the chip assembly upon which the terminals are fixed." This construction is supported by the specification of the '106 patent. The figures of the '106 Patent show that the "top layer 16" is an outer layer of the chip assembly. For example, in Figure 1, the "top layer 16" is an outer layer of "chip carrier 14"

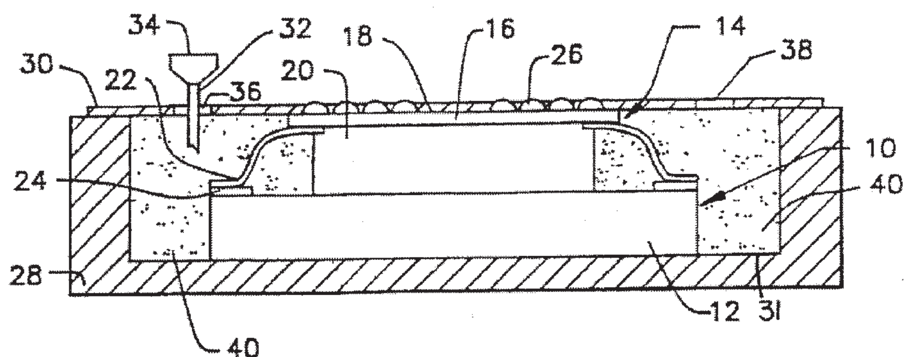

FIG. 1

(*See also* Figures 2-3, 5, 7- 9, 10B-10C and 11-13.) As set forth above, the specification of the '265 Patent also supports the ALJ's construction in describing the "top layer" of the interposer as further away from the chip than the "bottom layer."

Therefore, the ALJ finds that "top layer" means "an outer layer of the chip assembly upon which the terminals are fixed" and that the "top layer" is a single layer.

(2) "Terminals"

Tessera argues that "terminals" should be construed to mean "an endpoint for connection of the package to the outside." (CIB at 22.) Respondents argue that "terminals" should be construed to mean" an "endpoint for electrical connection of the chip package to the outside." (RIB at 49.) Staff argues that the term should be construed to mean an "electrically conductive element that connects the package to the outside – the connection may be mechanical and/or electrical." (SIB at 74.) All of the parties concede, however, that their proposed constructions are generally the same, namely that a terminal is an endpoint for connection of the package to the outside. (RRB at 24.)

The ALJ finds that the term "terminals" means "an endpoint for electrical and mechanical connection of the chip package to the outside." The specification of the '106 Patent describes "[t]he leads 22 are electrically connected to terminals 26 which protrude as bumps from the top surface 18 of the chip carrier 14" and that "[i]t is the terminals 26 which connect the semiconductor chip assembly 10 to a printed circuit board or other substrate (not shown)…." (JX-00003 (the '106 patent) at 5:16-17; 26-28.) The specification of the '265 Patent also supports such a construction as it describes "[t]hese masses may then be caused to flow and bond with the central terminals 48 and the contact pads 68 thereby forming mechanical and electrical connections between the central terminals and the contact pads." (the '265 Patent at 12:13-17.) Respondents' proposed construction, while correct in that the terminals do provide an electrical connection, fails to take into account the mechanical connection provided by the terminal. In fact, Respondents concede that the terminals provide a mechanical and electrical connection. (RIB at 49.) Thus, the intrinsic evidence supports the ALJ's claim construction that "terminals" are "an endpoint for electrical and mechanical connection of the chip package to the outside."

(3) "Thereon"

Respondents argue that "thereon" should be given its plain and ordinary meaning of "on or upon." (RIB at 52.) Tessera has not proposed any construction, but argues that Respondents' proposed construction ignores the entire context of the claim and that the embodiments of the '106 Patent and the '265 Patent and the claim language of the '106 Patent show that the terminals need not be disposed on the surface of the top layer. (CRB at 25-26.) Staff argues that, while Respondents' construction is not flawed, the term need not be construed and should be given its plain and ordinary meaning. (SIB at 76.)

The ALJ finds that the term "thereon" need not be construed as it is not unclear nor is it ambiguous. The term "thereon" should be given its plain and ordinary meaning. *Autogiro Co. of America v. United States,* 181 Ct. Cl. 55, 60-61 (Ct. Cl. 1967) ("Courts occasionally have confined themselves to the language of the claims. When claims have been found clear and unambiguous, courts have not gone beyond them to determine their content.") (citing *Keystone Bridge Co. v. Phoenix Iron Co.*, 95 U.S. 274, 278 (1877); *Borg-Warner Corp. v. Mall Tool Co.*, 217 F. 2d 850 (7th Cir. 1954); *Zonolite Co. and Insulating Concrete Corp. v. United States*, 138 Ct. Cl. 114, 149 F. Supp. 953 (1957).)

(4) "Encapsulant barrier"

Tessera argues that "encapsulant barrier" need not be construed as it is readily apparent that it is "a structure that is 'adjacent the semiconductor chip assembly' and as 'at least partially defining an encapsulation area.'" (CIB at 24.) Respondents argue that it means "a structure at least partially defining or shaping the encapsulation space." (RIB at 56.) Staff asserts that the term meaning is clear and unambiguous and that its plain and ordinary meaning is clear from the claim language. (SIB at 74.)

The ALJ finds that the term "encapsulant barrier" need not be construed and that its meaning is clear from the claim language. Respondents argue that the specification of the '106 Patent supports their argument that the term should be construed to include "shaping" as it accounts for the fact that the encapsulant barrier defines a three dimensional volume into which the encapsulant is introduced. (RIB at 56.) However, the ALJ finds that nothing in the specification of the '106 Patent that describes "defining a volume" or even "shaping," which would support adding the additional limitation as set forth by Respondents. Thus, the ALJ finds no basis for construing the claim to include such limitations. Thus, the ALJ finds that the plain and ordinary meaning of "encapsulant barrier" is clear and unambiguous based on the claim language.

(5) "Providing a protective barrier in contact with said top layer for protecting the terminals on the top layer from an encapsulation material"

In construing this step of claim 1, the parties have provided several different proposed constructions. Respondents have set forth two proposed constructions – one for the claim term "protective barrier" and a second for the "providing" step. Tessera has set forth its own construction for "protective barrier," but has not provided any proposed construction for the "providing" step except to set forth extensive arguments in opposition to Respondents' proposed construction. Staff argues that neither "protective barrier" nor the "providing" step should be construed as the terms and step are unambiguous and the plain and ordinary meaning is readily apparent to one of ordinary skill in the art.

Tessera argues that "protective barrier" should be construed as "a structure that is distinct from the top layer and protects the exposed terminals on the semiconductor chip assembly from encapsulation material." (CIB at 25.) Respondents argue that "protective barrier" means "a

structure that prevents encapsulation material from contacting the exposed terminals." (RIB at 56.) Respondents also argue that the "providing" step of claim 1 should be construed to mean "including a physical structure, in contact with the top layer, for the express purpose of preventing encapsulation material from contacting the terminals." (RIB at 53.) Tessera provides no proposed construction for this step, but argues that Respondents' proposed construction improperly reads an intent requirement onto the claim language. (CIB at 25.) Staff argues that "protective barrier" is unambiguous and its plain and ordinary meaning is readily apparent and further argues that the "providing" step does not require construction because once the other disputed claim terms in this step are construed, the meaning of the phrase will become unambiguous. (SIB at 75, 77.)

The ALJ finds that "protective barrier" means "a structure that is distinct from the top layer and protects the exposed terminals on the semiconductor chip assembly from encapsulation material." This construction is supported by the claims of the '106 Patent. Claim 1 describes the protective barrier as "in contact with said top layer" and "for protecting the terminals on the top layer from encapsulation material." (JX-00003 (the '106 Patent), Claim 1.) Claim 35 described a protective barrier as "a cap which engages said top layer and covers said terminals." (*Id.*, Claim 35.) Claim 38 similarly describes a cap as in Claim 35 that "is flexible and is forced against said top layer to prevent encapsulation material from contacting said terminals."

In addition, throughout the specification of the '106 Patent, the protective barrier is repeatedly described as a physical barrier for protecting the exposed terminals on the top layer:

> "A method of packaging a semiconductor chip assembly includes the encapsulation of the same after establishing an encapsulation area and providing a physical barrier for protecting the terminals of a chip carrier." ('106 Patent, Abstract)

> "The present invention relates generally to a method of encapsulating a semiconductor chip assembly, and more specifically to a method of encapsulating a semiconductor chip assembly within a ring or a can, while protecting the terminals on the chip carrier." (106 Patent; 1:6-10)
>
> "In accordance with one embodiment of the present invention, a semiconductor chip assembly or other component having a top layer with an array of exposed terminals is encapsulated by placing it in an encapsulent barrier next to the semiconductor chip assembly such that it at least partially defines an encapsulation area, and providing a protective barrier for protecting the exposed terminals on the top layer during encapsulation." ('106 Patent 1:50-52)
>
> "In other embodiments of the present invention, the protective barrier can be a dam, a cap, a cover, or any other means which protects the exposed terminals on the top layer of the semiconductor chips assembly. This could also include a flexible covering member which, upon the application of pressure, will deform into engagement with the top layer around the exposed terminals to protect the same." (106 Patent 2:58-64.)

(See also id. at 3:38-49; 3:67-4:3; 6:5-10; 6:56-7:2; 7:3-14; 7:15-21; 7:39-61.) Respondents' proposed construction is similar as it describes the protective barrier as "a structure that prevents encapsulation material from contacting the exposed terminals" and additionally construes this step of the claim to disclose "a physical structure, in contact with the top layer…" The point of contention focuses on whether the "protective barrier" is "for the express purpose of preventing encapsulation material from contacting the terminals" as Respondents contend in describing the "providing" step.

Respondents argue that this step "embodies what was invented by the '106 patent, and additional structure added to a dispensing method, the sole purpose of which was to protect terminals." (RIB at 53.) Respondents cite evidence in the prosecution history to support the proposed construction, namely that Tessera argued that the protective barrier was specifically for protecting the terminals or that it was meant to accomplish that task. (*Id.* at 54.) Respondents further argue that the term "for" in the claim language means that the additional and separate step of having a protective barrier "for the express purpose of protecting the terminals" is required

and that the fact that none of the other steps in claim 1 include the word "for" supports such an interpretation. (*Id.* at 53.)

Tessera argues that Respondents are incorrect and that the prosecution history fails to support such a contention. (CIB at 25.) Tessera argues that the inventors merely stated that the alleged protective barriers in the prior art did not function to protect the terminals and distinguished the prior art as not functionally equivalent to the protective barrier disclosed in the '106 Patent. (CRB at 26-27.)

The ALJ finds that nothing in the prosecution history or the specification or language of the claims of the '106 Patent supports Respondents' proposed construction of limiting the "providing" step of the claim 1 to disclosing protective barriers for the sole purpose of protecting the terminals. The specification of the '106 Patent discloses other purposes for the "protective barrier" other then just protection of the terminals. In describing using a solder mask made of dielectric material as a protective barrier, the specification of the '106 Patent states that "[s]ince its dielectric properties will be advantageous when the terminal 26 are employed during testing or final assembly. A photosensitive polymer film may be employed to permit formation of holes 37 by photographic processor. The preferred material for the solder mask 30 is Dupont VACREL 8100, which exhibits the desirable photosensitive and dielectric properties." (JX-00003 (the '106 Patent) at 5:65-6:4.) Thus, the specification points to other functions for the "protective barrier" other than the "for the sole purpose of protecting the terminals."

The prosecution history also fails to supports Respondents' proposed construction that the protective barrier is for the "sole purpose" of protecting the terminals from encapsulation material. In response to the examiner's argument that the prior art interposer corresponds to the protective barrier claimed in the '106 Patent, the inventors argued (1) that the interposer was not

functionally equivalent to the protective barrier and (2) to the extent they can be likened, the prior art did not teach that the interposer was for protecting the terminals from encapsulation material. (JX-00006(b).00153-.00154.) Thus, while the inventors did distinguish the '106 patent from the prior art on the basis that the prior art failed to teach that the interposer was for protecting the terminals, there is nothing in the prosecution history that specifically limits the protective barrier to the "sole purpose" of protecting the terminals. In other words, the prosecution history supports a construction of "protective barrier" as a physical structure that protects the terminals from encapsulation material, but that structure in not limited in function or purpose to *only* protecting the terminals as Respondents contend.

(6) "Compliant layer"

Tessera and Staff argue that "compliant layer" means "a layer that yields to an applied force." (CIB at 26; SIB at 75-76.) Respondents argue that the claim term is indefinite. (RIB at 54.)[4] Respondents argue that the term is indefinite because it is not defined anywhere in the specification and only mentioned once in the '106 Patent in claim 34. (*Id.*) Respondents further argue that the '265 specification provides no guidance because it "fails to identify the specific modulus of elasticity that would be necessary to properly understand the meaning of the term." (*Id.*)

Tessera argues that its construction is supported by the '265 Patent, which is incorporated by reference in the '106 Patent. Specifically, Tessera argues that the '265 Patent repeatedly describes examples wherein the "complaint [sic] layer is described as facilitating terminal movement relative to the chip." (CIB at 26.)

[4] Respondents further argue that Tessera's arguments should be excluded under Ground Rule 11.1 because it was not raised in their pre-hearing statement. (RRB at 26.) The ALJ finds, however, that pages 66-67 of Tessera's pre-hearing brief discuss Tessera's proposed construction for "compliant layer" and its arguments in support of that construction.

The ALJ finds that "compliant layer" means "a layer having a low modulus of elasticity that permits slight movement." The specification of the '265 Patent describes "a compliant layer of a material having a relatively low elastic modulus" (the '265 Patent at 6:9-11; 9:52-54 ("a compliant layer 40 formed from a material having a relatively low elastic modulus"); 9:57-58 ("The compliant, low-modulus material of bottom layer 40 may be an elastomer"); 9:64-66 ("Bottom, compliant layer 40 includes holes or voids 41 interspersed with masses 43 of the low-modulus material"); 10:15-17 ("Each central terminal 48 is aligned with one of the masses 43 of low modulus material in compliant layer 40"); *see also* 12:57-59 (describing the compliant layer as "flexible"); 14:34-37 (describing the compliant layer as "soft"). The '265 specification further describes a "compliant layer" that "permits slight [] movement." (the '265 Patent, Abstract) ("The interposer may be provided with a compliant layer disposed between the terminals and the chip to permit slight vertical movement of the terminals towards the chip during testing operations."; "A compliant layer disposed between the terminals and the chip permits slight vertical movement of the terminals towards the chip during testing operations, in which the terminals on the interposer are engaged with an assembly of test probes."; 6:11-15 ("[The compliant layer] permits slight downward movement of the central terminals towards the front face of the chip."); 11:21-24 ("Moreover, because the bottom layer 40 of the interposer is compliant, each central terminal 48 is displaceable towards and away from the front surface of the chip 20."); 11:37-41 ("Compliant layer 40 need only provide for sufficient downward movement of terminals 48 to accommodate tolerances in the components and test equipment by accommodating differences in vertical position between adjacent terminals and/or test probes.").)

The description of the "compliant layer" in the '265 specification, which is explicitly incorporated by reference in the '106 patent, contradicts Respondents contention that the claim

term is indefinite. Tessera and Staff's proposed construction is too broad as any material may yield to an applied force, even the stiffest materials. (RX-09 (Elenius WS) at Q. 260.) Their proposed construction also fails to take into account the repeated description of the "compliant layer" as having a low modulus of elasticity in the '265 specification. Therefore, the ALJ finds that "compliant layer" means "a layer having a low modulus of elasticity that permits slight movement."

(7) "Above"

Tessera and Staff argue that "above" means "a point upward of the reference point." (CIB at 27; SIB at 76.) Respondents argue that the term should be given "its plain and ordinary meaning of 'being at a higher place'." (RIB at 55.)

The ALJ finds that the term "above" means "a point upward of the reference point." The specification and the claims of the'106 patent support such a construction. In Figure 9, the patent describes the process of forming an elastomeric layer between the top layer and the chip carrier while simultaneously forming an encapsulation barrier as disclosed in the '611 patent, whose specification is incorporated by reference. (JX-00003 (the '106 patent) at 7:22-32.) The '611 patent specification specifically states that "[t]he term 'above' a reference point shall refer to a point upward of the reference point" and "directions referred to as 'upward' or 'rising from' shall refer to the direction orthogonal and away from the chip top surface 20." (CX-01033 (the '611 Patent) at 3:55-4:12.) Thus, unlike the '265 specification, where the term "top layer" was never addressed in the directional definitions disclosed therein, the specification of the '611 patent specifically defines the directional terms "above" and "upward." Thus, when the "top layer" is described as "above" the chip, it is "upward" of the top surface of the chip. In describing Figure 9, the '106 patent discloses for the first time a procedure wherein

> [i]t is preferable, particularly when the solder mask 30 is to be vacuum laminated to the top surface of the chip carrier 14, that the chip carrier 14 be *supported above* the chip 12 by outer structures in addition to leads 22 so that the integrity of the leads 22 and the connection of such leads to the chip 12 and the chip carrier 14 are not affected during lamination of the solder mask.

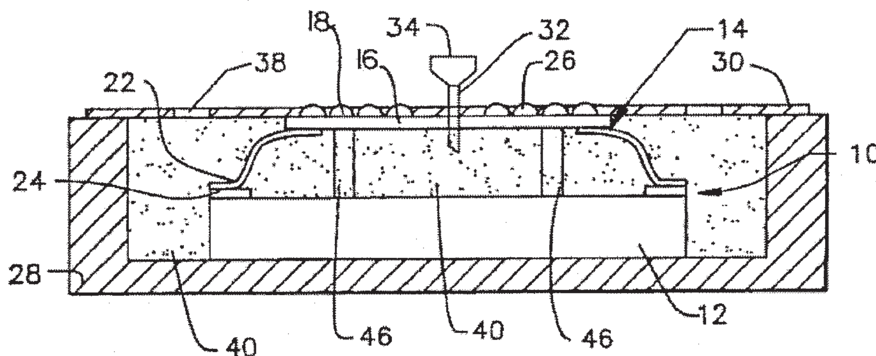

FIG. 9

('106 patent 7:42-47) (Emphasis added). Here, the "top layer 16" is upward of the reference point, namely the top surface of "chip 12." Similarly, claim 33 discloses a claimed invention where the "top layer" is specifically placed "upward" of the semiconductor chip:

> [t]he method as in claim 1, wherein said top layer *is a spaced distance above* said semiconductor chip, and further comprising the step of supporting said top layer includes providing a compliant layer between said top layer and said chip.

('106 patent, claim 33.).

Respondents argue that construing "above" to mean "a point upward of a reference point" would render the limitation "supporting" in claim 33 meaningless because it "necessitates a gravitational frame of reference." (RRB at 26.) However, the claim specifically discloses "supporting said top layer above said semiconductor," which, as construed by the ALJ describes the top layer as supported upward of the reference point, namely the top surface of the semiconductor chip. In other words, the term "supporting" does not require a gravitational frame

of reference, but rather, in the context of the claim, requires a point of reference from the chip top surface.

Therefore, the ALJ finds that "above" means "a point upward of a reference point."

2. The '977 and the '627 Patents

. The parties dispute the following claim terms in the '977 and 627 Patents: "movable," "dielectric element," "compliant layer," "flexible," and "terminals." However, only those claim terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Vanderlande Indus. Nederland BV v. Int'l Trade Comm.*, 366 F.3d 1311, 1323 (Fed. Cir. 2004); *Vivid Tech., Inc. v. American Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

(1) "movable" ('977 Patent - claims 17 and 18, '627 Patent – claims 1 and 12)

Tessera and the Staff argue that the limitation "movable" is properly construed to mean "in the operation of the assembly, the terminals are capable of being displaced relative to the chip by external loads applied to the terminals, to the extent that the displacement appreciably relieves mechanical stresses, such as those caused by differential thermal expansion which would be present in the electrical connections absent such displacement." (CIB at 11; SIB at 18-19.) Respondents argue that the term "movable" is indefinite under 35 U.S.C. § 112 ¶ 2. (RIB at 82-83.) However, respondents argue that should the term be found to be capable of construction that properly construed "movable" means "in the operation of the assembly, the terminals are capable of being displaced relative to the chip contacts by external forces applied to the terminals, to the extent that the displacement appreciably relieves mechanical stresses, such as those caused by differential thermal expansion which would be present in the electrical connection absent such displacement." (*Id.*) Respondents also argue that any construction should include a

statement that if the package includes a rigid substrate, the claimed movement is not present in the package. Respondents further argue that movement that relieves mechanical stresses due to CTE matching or inexact CTE matching is not the claimed movement. (*Id.*)

Turning first to the claims, it is observed that asserted independent claims 17 and 18 and non-asserted claim 19 of the '977 patent each require that the "terminals are movable with respect to said contacts." (JX-1 (the '977 patent) at 36:6-7, 36:18-19, 36:30-31.) Claims 1 and 12 of the '627 patent are more specific requiring the terminals to be "movable with respect to said central contacts so as to compensate for thermal expansion of said chip." (JX-2 (the '627 patent) at 34:32-34, 35:12-15.) According to a plain reading of the claims of the '977 and '627 patents, the required terminal movement must be in relation to the contacts of the chip. Additionally, the express language of the claims of the '627 patent requires that the movement of the terminals compensate for the thermal expansion of the chip. Although each party's proposed construction requires that the movement be due to external loads, it is worth noting that there is nothing in the claims to suggest that the movement of the terminals should be so limited.

The specifications also elucidate the proper claim construction. In particular, the specifications confirm that some "displacement of the terminals toward the chip" and "movement of said terminals toward said chip" is expected and accounted for in the invention. (*See, e.g.*, JX-1 at 3:45-46, 3:50-51, 4:20-23.) The specifications also confirm that the terminals may "move with respect to the chip in directions parallel to the chip surfaces," noting that such parallel movement provides compensation for the differential thermal expansion of the chip and substrate. (*See, e.g.*, JX-1 at 3:62-65.)

Additionally, the specifications state with reference to the embodiment depicted in part by Figure 3 that:

> The contact end 56 of each lead 50 is movable relative to the associated terminal 48. As best seen in Fig. 3, the contact end 56a of lead 50a can be displaced from its normal, undeformed position (shown in solid lines) in the directions parallel to the faces 44 and 46 of interposer 42 and parallel to the front face 38 of chip 28. For example, the contact end 56a may be displaced to the position indicated in broken lines at 56a'. This displacement is permitted by the flexibility of the lead 50 and by buckling and wrinkling of interposer 42. Encapsulant 60 is compliant, and does not substantially resist flexing of leads 50 and buckling and wrinkling of interposer 42. The displacement illustrated in FIG. 3, from the normal undisplaced position 56a to the displaced position 56a' places lead 50 in compression. That is, the terminal end 56a moves generally toward the associated terminal 48 in moving from position 56a to position 56a'. Movement in this direction is particularly well accommodated by buckling of the lead 50. The contact end of each lead can also move in other directions, such as in the opposite direction from position 56a away from the associated terminal 48, and in directions perpendicular to those directions, into and out of the plane of the drawing as seen in FIG. 3.

(JX-1 at 11:6-28.) The specifications' description of the "buckling and wrinkling" of the interposer upon which the terminals are located does not connote uniform movement, such as strictly horizontal or strictly vertical. Indeed, while the illustration of Figure 3 depicts movement parallel to the faces 44 and 46 of interposer 42 and parallel to the front face 38 of chip 28, the portion of the specifications quoted above states that the terminal end 56a moves *generally* toward the associated terminal 48 in moving from position 56a to position 56a'. In addition, the specifications teach that the movement depicted in Figure 3 is not the only movement that may occur or that the invention is designed to accommodate. The specifications explicitly state that "[t]he contact end of each lead can also move in other directions, such as in the opposite direction from position 56a away from the associated terminal 48, and in the directions perpendicular to these directions, into and out of the plane of the drawing as seen in FIG. 3." (JX-1 at 11:23-27.)

The specifications also discuss the requirement that the terminal movement compensate for the differential thermal expansion of the chip and substrate. Specifically, the specification states that:

> The interconnections-between the chip and the substrate (between peripheral contacts 830 and contact pads) are accommodated within the area of the chip itself, i.e., within the area on the substrate occupied by chip 820. Thus, no space on the surface of the substrate is wasted by a conventional "fan-out" pattern of interconnections. Moreover, the assembly is *substantially resistant to thermal cycling.* Each of the composite leads connecting one of the chip peripheral contacts and one of the central terminals 848 on the interposer is flexible. Thus, the partial leads 50 (FIG. 13) on the interposer surface itself preferably are flexible, and the fine bonding wires 856 are also flexible. The interposer itself, and particularly the top layer 838 and bottom compliant layer 840 may be flexible. Accordingly, there can be *substantial movement of terminals* 848 on the interposer relative to contacts 830 on the chip in directions parallel to the chip front surface. Such movement can be accommodated without applying substantial forces to the junctions between the leads and- the chip contacts. During use of the assembly, differential thermal expansion of chip 820 and substrate may cause appreciable displacement of the contact pads on the substrate relative to peripheral contacts 830 on the chip: Inasmuch as the central terminals 848 of the interposer are bonded to the contact pads of" the substrate by relatively, stiff noncompliant conductive masses, *the central terminals will tend to move with the contact pads.* However, such movement is readily accommodated and does not result in substantial stresses at the bonds between the central terminals and contact pads.

(JX-1 at 20:21-49 (emphasis added).) The patent specifications teach that differential thermal expansion of the chip and substrate may cause appreciable displacement of the contact pads on the substrate relative to the contacts on the chip. According to the specification, the assembly is "substantially resistant" to thermal cycling. Also, the specification teaches that there can be "substantial movement" of the terminals on the interposer relative to contacts on the chip in directions parallel to the chip front surface, and the central terminals will "tend to move" with the contact pads. In the specifications there is no indication that the terminals move to the same extent as the contact pads, in tandem with the contacts, or in a "fixed position" with respect to

the contacts. Furthermore, the specifications teach that "substantial stresses" at the bonds between the central terminals and contact pads will be avoided.

The prosecution history is examined next. As described in more detail below, during the prosecution of related U.S. Patent No. 6,433,419 (the '419 patent) Tessera disclaimed the use of CTE matching as a method for relieving the stress on the solder joints. The '419, '977 and '627 patents all claim priority to the same parent application and share substantially the same specification. Even though the '419 patent issued later than the '977 patent and the '627 patent, its prosecution history is still relevant to the proper construction of common claim limitations.

In the original prosecution of the '419 patent, the patent examiner rejected the pending claims as anticipated by U.S. Patent No. 5,216,278 to Lin, stating among other things that:

> Although Lin teaches at least some of the terminals of the backing element being disposed in the central region of said backing element and being movable "resilient" "compliant" with respect to the chip, Lin does not appear to explicitly teach that the intended use of the movable terminals is to compensate for differential thermal expansion of the chip and substrate. Nevertheless, the statement of intended use does not result in a structural difference between the claimed product and the product of Lin. Further, because the product of Lin is inherently capable of being used for the intended use: the statement of intended use does not patentably distinguish the claimed product from the device of Lin. Similarly, the manner in which a product operates is not germane to the issue of patentability of the product; *Ex parte Wikdahl* 10 USPQ 2d 1546, 1548 (BPAI 1989); *Ex parte McCullough* 7 USPQ 2d 1889, 1891 (BPAI 1988); *In re Finsterwalder* 168 USPQ 530 (CCPA 1971); *In re Casey* 152 USPQ 235,238 (CCPA 1967). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In *re Danley*, 120 USPQ 528, 531 (CCPA 1959). *See also, Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) In order to further clarify the teaching of compliant layer 20, it is noted that, as cited *supra*, Lin teaches that the layer is solder, and further teaches that solder is compliant.

(JX-4 at pp. 183, 194-95.) Tessera distinguished the prior art Lin reference stating:

> As construed in the Official Action, the teaching of Lin is that the solder balls 26 must deform in order to accommodate differential movement of the terminal solder pads 34 with respect to the substrate. A teaching of deformable solder balls

> used to connect terminals to a substrate does not suggest the combination of claim 2, which includes terminals movable relative to the chip to compensate for differential thermal expansion and thus reduce the need for deformation in the solder balls or other bond between the terminals and the contact pads of the substrate. Indeed, Lin's teaching that one should rely upon deformable solder balls and CTE matching of the 'carrier substrate 12' and the printed circuit board as a full and adequate solution to the problem of solder joint fatigue leads away from any suggestion that one should provide terminals movable relative to the chip to deal with this problem.

(CX-O1916C, August 20, 2001 Response to Office Action at 4-5.) Thus, in order to overcome the Examiner's rejection, Tessera distinguished solder ball deformation and CTE matching from the "claimed movement." This conclusion is consistent with the position of Tessera's expert Dr. Qu in this investigation. (*See* Qu, Tr. 598:5-599:8.)

Thus, while there is nothing in the plain language of the claims of the '977 and '627 patents that suggests that the claimed terminal movement should be limited to movement due to external forces, Tessera disavowed solder deformation and CTE matching as the claimed movement in its statements in the prosecution history. By disavowing solder deformation and CTE matching, Tessera ostensibly limited itself to terminal movement due to external loads.

Based on the examination of the intrinsic record as detailed above, including the claims, specification and prosecution history, the ALJ finds that the limitation "terminals are movable with respect to said contacts" in the '977 patent is properly construed as requiring that "in the operation of the assembly, the terminals are capable of being displaced relative to the contacts of the chip by external loads applied to the terminals, to the extent that the displacement appreciably relieves mechanical stresses, such as those caused by differential thermal expansion which would be present in the electrical connections absent such displacement." Similarly, the ALJ finds that the limitation "[terminals] being movable with respect to said central contacts so as to compensate for thermal expansion of said chip" in the '627 patent is properly construed as

requiring that "in the operation of the assembly, the terminals are capable of being displaced relative to the central contacts of the chip by external loads applied to the terminals, to the extent that the displacement appreciably relieves mechanical stresses, such as those caused by differential thermal expansion which would be present in the electrical connections absent such displacement."

(2) "Compliant layer" / "layer of compliant material" ('977 Patent - claims 17 and 18, '627 Patent – claims 4 and 16)

Tessera argues that the limitation "compliant layer" is properly construed to mean "a layer that yields to an applied force." (CIB at 17.) Respondents argue that the term "movable" is indefinite under 35 U.S.C. § 112 ¶ 2. (RIB at 88.) However, respondents argue that should the term be found to be capable of construction that properly construed the limitation means "a material that is appreciably compressible in a direction perpendicular to its surface." (*Id.*) The Staff argues that properly construed "compliant layer" means "a layer of material that is capable of allowing movement of the terminals." (SIB at 18, 59.)

Turning first to the claims, it is noted that claims 17 and 18 of the '977 patent require "a layer of compliant material disposed between said terminals and said chip and supporting at least some of said terminals." (JX-1 at 36:1-3, 36:14-16.) Dependent claim 21 of the '977 patent, which depends from claim 18, additionally requires that the "compliant material is an elastomeric material." (*Id.* at 36:36-37.) Claim 4 of the '627 patent requires that "said dielectric element includes a compliant layer of a low modulus material" and claim 16 of the '627 patent requires that "said dielectric element includes a compliant layer." (JX-2 at 34:40-42, 36:12.) Dependent claim 6 of the '627 patent, which depends from claim 4, additionally requires that "said complaint layer is formed from an elastomeric material," while dependent claim 7, which

also depends from claim 4, requires that "said compliant layer is formed from a compressible foam." (*Id.* at 34:50-53.)

In light of the particular limitation added by dependant claim 21 of the '977 patent, under the doctrine of claim differentiation there is a presumption that the layer of compliant material of claim 18 is not an elastomeric material. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed.Cir.2005) (en banc) (Under the doctrine of claim differentiation, "the presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim.".) Similarly, in light of the particular limitations added by dependant claims 6 and 7 of the '627 patent, there is a presumption that the compliant layer of claim 4 is not an elastomeric material or compressible foam.

Contrary to Respondents' proposed claim construction, there is nothing in the plain language of the claims to suggest that a compliant material is only compliant in a direction perpendicular to its surface. In fact, as discussed in detail, *infra*, the asserted patents make plain that the "movement" facilitated by the compliant layer can occur in a direction either perpendicular or parallel to the chip.

Having examined the language of the claims, the specification is consulted. The specification uses the term "compliant" idiosyncratically, thus connoting the breadth of the term. *See Johnson Worldwide Assocs. v. Zebco Corp.*, 175 F.3d 985, 991 (Fed. Cir. 1999) ("[v]aried use of [this] disputed term in the written description demonstrates the breadth of the term[,] rather than providing a limited definition."). Specifically, the specification describes the "compliant layer" as being: (1) compressible (*see* JX-1 at 3:47-51 ("said complaint layer will be compressed upon movement of said terminals toward said chip")); (2) resilient (*see id.* at 7:57-61 ("[T]he assembly may include resilient means for permitting movement of the terminals towards

the bottom surface but resisting such movement. For example, the assembly may incorporate a layer of a compliant material disposed between the chip rear surface and the terminals.")); (3) having a relatively low elastic modulus (*see id.* at 17:36-39 ("compliant bottom layer 840 formed from a material having a relatively low elastic modulus")); (4) flexible (*see id.* at 20:32-34 ("The interposer itself, and particularly the top layer 838 and bottom compliant layer 840 may be flexible.")); (5) soft (*see id.* at 22:4-6 ("Because the compliant layer is soft, the top layer will remain flexible even when bound to the chip through the compliant layer.")); and (6) elastic (*see id.* at 27:24-26 ("[A] resilient, compliant layer 964 (FIG. 25) formed from a relatively low elastic modulus material is provided in the lower or downwardly facing space 960 of box element 950. Preferably, this low-modulus material has elastic properties (including modulus of elasticity) comparable to those of soft rubber.")).

With regard to the Respondents' argument that a compliant material only permits movement in the direction perpendicular to its surface, the specification explicitly contradicts Respondents argument by making plain that the compliant layer permits both perpendicular and parallel movement. For example, the specification states that "a compliant layer is disposed between said terminals and said chip so that said compliant layer will be compressed upon movement of said terminals toward said chip." (JX-1 at 3:48-51.) Additionally, the specification states that "[b]ecause the compliant layer is soft, the top layer will remain flexible even when bound to the chip through the compliant layer, and the terminals will still be movable with respect to the contacts in directional [sic] parallel to the face of the chip." (JX-1 at 22:4-7.)

Respondents also assert that the prosecution history supports its proposed construction, arguing that Tessera distinguished its pending claims over the prior art on the grounds that the

prior art did not teach a material that was compressible in a direction perpendicular to its surface. (RIB at 89.) Specifically, respondents rely on the following passage:

> Moreover, at the interview counsel pointed out that claim 24, and hence claims 25, 30 and 35 specifically incorporate applicant's arrangement of "compliant" interposer which allows "each central terminal to be displaced downwardly towards said front surface of said chip."
>
> . . . But flexibility does not necessarily imply compliance. That is, there is no reason to believe that Niki's thin film could be compressed to any appreciable degree by application of a force directed into the film and towards the chip surface. Thus, if there were a terminal on the surface of this film facing away from the chip (which there is not), there is no reason to believe such terminal could be displaced towards the chip.
>
> At the interview, counsel demonstrated this difference by showing that a piece of ordinary note pad paper, placed atop the Examiner's desk was indeed flexible but not compliant. The piece of paper could not be appreciably compressed by applying a finger atop it and pressing down onto the desk through the paper. There is no reason to believe that the film specified by Niki is compliant, or that such film would permit any displacement of a terminal towards the chip front surface.

(JX-00070 at 10-11; RX-4C (Corrected Moresco RWS and Errata) at Qs. 168, 169.) While Tessera distinguished its invention over Niki, Tessera did not clearly and unmistakably disavow any claim scope. *Sorensen v. Int'l Trade Comm'n*, 427 F.3d 1375, 1378-79 (Fed.Cir.2005); *see also Omega Eng'g, Inc., v. Raytek Corp.*, 334 F.3d 1314, 1325-26 (Fed.Cir.2003) ("[F]or prosecution disclaimer to attach, our precedent requires that the alleged disavowing actions or statements made during prosecution be both clear and unmistakable."). Accordingly, the ALJ finds respondents' argument regarding the prosecution history unpersuasive.

With regard to Tessera's proposed construction of "compliant layer" as "a layer that yields to an applied force," the record evidence shows that any material will yield to an applied force. (*See* RX-4C (Corrected Moresco RWS) at Q. 161.) Because any material will yield to an applied force, the ALJ finds Tessera's proposed construction too broad, ostensibly depriving the

limitation of any particularized meaning. *See Innova/Pure Water, Inc. v. Safari Water Filtration Sys.*, 381 F.3d 1111, 1119 (Fed. Cir. 2004) ("While not an absolute rule, all claim terms are presumed to have meaning in a claim.").

Accordingly, based on the language of the claims and the specifications of the asserted patents, the ALJ finds that one of ordinary skill in the art at the time of the invention would construe the limitations "compliant layer" and "layer of compliant material" as a layer of material that is flexible, compressible, and/or elastic.

IV. INFRINGEMENT DETERMINATION

A. Applicable Law

In a section 337 investigation, the complainant bears the burden of proving infringement of the asserted patent claims by a preponderance of the evidence. *Certain Flooring Products*, Inv. No. 337-TA-443, Commission Notice of Final Determination of No Violation of Section 337, 2002 WL 448690 at 59, (March 22, 2002); *Enercon GmbH v. Int'l Trade Comm'n,* 151 F.3d 1376 (Fed. Cir. 1998). Each patent claim element or limitation is considered material and essential to an infringement determination. *See London v. Carson Pirie Scott & Co.*, 946 F.2d 1534, 1538 (Fed. Cir. 1991). Literal infringement of a claim occurs when every limitation recited in the claim appears in the accused device, *i.e.,* when the properly construed claim reads on the accused device exactly. *Amhil Enters., Ltd. v. Wawa, Inc.*, 81 F.3d 1554, 1562 (Fed. Cir. 1996); *Southwall Tech. v. Cardinal IG Co.*, 54 F.3d 1570, 1575 (Fed Cir. 1995).

If the accused product does not literally infringe the patent claim, infringement might be found under the doctrine of equivalents. The Supreme Court has described the essential inquiry of the doctrine of equivalents analysis in terms of whether the accused product or process

contains elements identical or equivalent to each claimed element of the patented invention. *Warner-Jenkinson Co., Inc. v. Hilton Davis Chemical Co.*, 520 U.S. 17, 40 (1997).

Under the doctrine of equivalents, infringement may be found if the accused product or process performs substantially the same function in substantially the same way to obtain substantially the same result. *Valmont Indus., Inc. v. Reinke Mfg. Co.,* 983 F.2d 1039, 1043 (Fed. Cir. 1993). The doctrine of equivalents does not allow claim limitations to be ignored. Evidence must be presented on a limitation-by-limitation basis, and not for the invention as a whole. *Warner-Jenkinson,* 520 U.S. at 29; *Hughes Aircraft Co. v. U.S.*, 86 F.3d 1566 (Fed. Cir. 1996). Thus, if an element is missing or not satisfied, infringement cannot be found under the doctrine of equivalents as a matter of law. *See, e.g.*, *Wright Medical*, 122 F.3d 1440, 1444 (Fed. Cir. 1997); *Dolly, Inc. v. Spalding & Evenflo Cos., Inc.*, 16 F.3d 394, 398 (Fed. Cir. 1994); *London v. Carson Pirie Scott & Co.*, 946 F.2d 1534, 1538-39 (Fed. Cir. 1991); *Becton Dickinson and Co. v. C.R. Bard, Inc.*, 922 F.2d 792, 798 (Fed. Cir. 1990).

The concept of equivalency cannot embrace a structure that is specifically excluded from the scope of the claims. *Athletic Alternatives v. Prince Mfg., Inc.*, 73 F.3d 1573, 1581 (Fed. Cir. 1996). In applying the doctrine of equivalents, the Commission must be informed by the fundamental principle that a patent's claims define the limits of its protection. *See Charles Greiner & Co. v. Mari-Med. Mfg., Inc.*, 92 F.2d 1031, 1036 (Fed. Cir. 1992). As the Supreme Court has affirmed:

> Each element contained in a patent claim is deemed material to defining the scope of the patented invention, and thus the doctrine of equivalents must be applied to individual elements of the claim, not to the invention as a whole. It is important to ensure that the application of the doctrine, even as to an individual element, is not allowed such broad play as to effectively eliminate that element in its entirety.

Warner-Jenkinson, 520 U.S. at 29.

Prosecution history estoppel may bar the patentee from asserting equivalents if the scope of the claims has been narrowed by amendment during prosecution. A narrowing amendment may occur when either a preexisting claim limitation is narrowed by amendment, or a new claim limitation is added by amendment. These decisions make no distinction between the narrowing of a preexisting limitation and the addition of a new limitation. Either amendment will give rise to a presumptive estoppel if made for a reason related to patentability. *Honeywell Int'l Inc. v. Hamilton Sundstrand Corp.*, 370 F.3d 1131, 1139-41 (Fed. Cir. 2004), *cert. denied*, 545 U.S. 1127 (2005)(citing *Warner-Jenkinson*, 520 U.S. at 22, 33-34; and *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.,* 535 U.S. 722, 733-34, 741 (2002)). The presumption of estoppel may be rebutted if the patentee can demonstrate that: (1) the alleged equivalent would have been unforeseeable at the time the narrowing amendment was made; (2) the rationale underlying the narrowing amendment bore no more than a tangential relation to the equivalent at issue; or (3) there was some other reason suggesting that the patentee could not reasonably have been expected to have described the alleged equivalent. *Honeywell*, 370 F.3d at 1140 (citing, *inter alia*, *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.,* 344 F.3d 1359 (Fed. Cir. 2003)(*en banc*)).

B. The '106 Patent

1. Claim 1

Tessera has accused Respondents of literal infringement and infringement under the doctrine of equivalents of independent claim 1 and dependent claims 2-4, 9-10 and 33-35 of the '106 Patent by the importation, the sale for importation or the sale after importation of certain semiconductor chips with minimized chip packages size and products containing same in the United States.

The parties dispute as to whether Respondents' accused product infringe claim 1 centers on whether Respondents' products satisfy the limitations of (1) "a top layer with an array of exposed terminals thereon"; (2) "a protective barrier in contact with said top layer"; and (3) the "providing step." The parties do not dispute whether Respondents' accused products satisfy other claim limitations. (*See generally* CRB at 28-33; RRB at 26-31.)

a) "A top layer with an array of exposed terminals thereon"

Tessera argues that Respondents' accused products meet this limitation both literally and under the doctrine of equivalents. Tessera argues that the "top layer" is "the solder mask layer" for laminate substrate packages and "the polyimide layer" for polyimide substrate packages. (CIB at 55.) For both the laminate substrate packages and the polyimide substrate packages, the "terminals" are the solder ball pads on the bottom surface of the solder mask or polyimide layer. (*Id.*) As such, Tessera contends that Respondents' accused products literally satisfy this claim limitation because the solder mask or the polyimide layer is the outer layer with an array of exposed solder ball pads thereon. (*Id.* at 55-56.) Staff agrees with Tessera on these points. (SIB at 79.)

Respondents argue that its products do not literally infringe or infringe under the doctrine of equivalents. Respondents argue that the "top layer" is the copper metallization layer upon which the terminals are fixed and that the "terminals" are the solder balls. (RIB at 57.) Respondents assert that since the solder balls are not yet attached to the accused products during encapsulation, then these products fail to meet this limitation of claim 1 since the accused packages do not have "terminals." (*Id.* at 59-60.) Even if the solder ball pads are the "terminals," Respondents argue that its products do not literally infringe because the solder ball pads are disposed on the top layer, but instead are found within the top layer.

As set forth above, the ALJ has found that "top layer" means "an outer layer of the chip assembly upon which the terminals are fixed" and that the "top layer" is a single layer. The ALJ further defined "terminals" to mean "an endpoint for electrical and mechanical connection of the chip package to the outside." The evidence shows that the "endpoint for electrical and mechanical connection of the chip package to the outside" is the solder ball pads. (CX-06482C (Goosey DWS) at Qs. 113, 114, 170, 176, 177, 228, 230, 231, 272, 278, 283, 284, 328; CX-01085, 01087-01139, 01141-01146; RX-9C (Elenius DWS) at Q&A 299, 302, 325, 327, 341 and 344; Elenius, Tr. 2599:11-14); RX-6C (Sinnadurai RWS) at Qs. 25-27; Sinnadurai, Tr. 2288:1-4; Nanya bonding diagrams; Powerchip substrate drawings and bonding diagrams.) Respondents argue that the "terminals" are the solder balls rather the solder ball pads because the '106 Patent describes the terminals as "bumps." (RIB at 57.) Such a construction goes against the intrinsic evidence, which specifically demonstrates that the solder ball pads are the terminals:

> The assembly is placed on the substrate so that the central terminals 48 face toward the electrical contact pad 68 on the substrate, and so that each central terminal 48 is aligned with one contact pad 68. Masses of an electrically conductive bonding material 70 such as a solder or an electrically conducted adhesive may be disposed between the central terminals and the contact pads 68 thereby forming mechanical and electrical connections between the central terminals and the contact pads.

(CX-01033 (the '265 patent) at 12:3-17; CX-06482C at Q. 283.) Thus, the patent clearly distinguishes the terminals from the solder balls, which are the means of mechanically and electrically connecting the terminals to the outside. (*Id.* at 12:3-13, 12:25-32, Fig. 5; CX-01032 (the '265 patent) at 12:3-13; Fig. 5; Elenius, Tr. 2578:23-2579:2, 2582:18-22; Sinnadurai, Tr. 2256:13-2257:16, 2258:5-10.) The "endpoint for electrical and mechanical connection of the chip package to the outside" is the solder ball pads, not the solder balls themselves. Rather, the

solder balls are the second level interconnect structures that are external to the package. (RX-9C (Elenius DWS) at Qs. 94, 96, 98; Sinnadurai, Tr. at 2252:16-20.)

The evidence further shows that the solder ball pads are formed from the copper metallization layer located on the substrate core or, in the case of polyimide packages, on the elastomeric layer of the package substrate. (RX-6C (Corrected Sinnadurai RWS) at Qs. 58, 130, 202; Goosey, Tr. at 950:4-14; RX-9C (Elenius RWS.)/RX-9C(a) (Elenius RWS Errata) at Qs. 198, 299, 309, 325, 332, 341, 346; RX-324C at 15; RDX-78C; RDX-79C; RX-323C at 1-3; RX-310C; RX-311C; RX-322C at 17-18, 27; RX-324C at 13-14; RX-302C; RX-301C; RX-323C at 9-10; RX-277.) Thus, the single layer upon which the terminals are "on or upon" is the substrate core layer or the elastomeric layer of the package substrate. (RX-6C (Corrected Sinnadurai RWS) at Qs. 58, 130, 202; RX-9C (Elenius RWS)/RX 9C(a) (Elenius Rebuttal W.S. Errata) at Q. 299, 300, 341, 325; RX-324C at 1-5; RDX-78C; RDX-79C; RX-322C at 1-7; RX-310C; RX-311C; RX-324C at 6-7; RX-323C at 1-3.) Tessera argues that the solder ball pads are actually "on" the bottom layer of the solder mask layer or the polyimide layer. (CIB at 55; CRB at 30.) In other words, Tessera has essentially combined the copper metallization layer and the solder mask layer or the polyimide layer into a composite "single layer" with the copper metallization layer forming the "bottom surface" of the composite single layer such that the terminals are "on" this composite single layer. However, the evidence clearly shows that the solder ball pads are formed from the copper metallization layer that is "on or upon" the core substrate for wBGA products or the elastomeric layer for µBGA products. (RX-6C (Corrected Sinnadurai Rebuttal W.S.) at Q. 58, 130, 202; Goosey, Tr. 950:4-14; RX-9C (Elenius Rebuttal W.S.)/RX-9C(a) (Elenius Rebuttal W.S. Errata) at Qs. 299, 309, 325, 332, 341, 346; RX-324C at 1-6; RDX-78C; RDX-79C; RX-324C at 13-14; RX-302C; RX-301C; RX-323C at 1-6, 9-10; RX-310C; RX-

311C; RX-322C at 2-7, 17-18.) Thus, Respondents' products literally meet the limitation of having "a top layer with an array of exposed terminals thereon," namely the solder ball pads on the substrate core layer in wBGA products and the solder ball pads on the elastomeric layer of the package substrate in the µBGA products.

Therefore, the ALJ finds that the evidence shows that Respondents' accused products literally meet the claim limitation of having "a top layer with an array of exposed terminals thereon." The evidence shows that the accused wBGA products have exposed solder ball pads that are on or upon the substrate core layer and that µBGA products have solder ball pads that are on or upon the elastomeric layer of the package substrate.

b) "A protective barrier in contact with the top layer"

Both Respondents and Tessera agree that the "protective barrier" is the second mold chase. (CIB at 52-53; RIB at 57-58.) The ALJ has construed "protective barrier" to mean "a structure that is distinct from the top layer and protects the exposed terminals on the semiconductor chip assembly from encapsulation material." The evidence shows that the second mold chase protects the solder ball pads from the encapsulant. (CX-06482C (Goosey DWS) at Q. 125,180, 234, 236, 286, 337; RX-9C (Elenius WS) at Qs. 303, 308, 329, 331, 345; RX-6C (Sinnadurai RWS) at Qs. 66-67, 85, 138-139, 157, 208-209, 227; Sinnadurai, Tr. 2289:9-13, 2290:25-2291:7; CX-01226C at 50; CX-01318C at 44-45.) The second mold chase is also a structure that is distinct from the top layer, *i.e.* the substrate core layer in wBGA products and the elastomeric layer of the package substrate in µBGA products. (*Id.*) Therefore, the ALJ finds that the second mold chase in Respondents' encapsulation process is the "protective barrier."

As set forth *supra*, the "top layer" in Respondents' accused products is the core substrate layer in wBGA products and the elastomeric layer of the package substrate in µBGA products.

See supra IV.B.1.a. The evidence shows that the "protective barrier" never comes into contact with the either the core substrate layer or the elastomeric layer. In wBGA products, the second mold chase is separated from the core substrate layer by the solder mask and the copper metallization layer. (RX 6C (Corrected Sinnadurai RWS) at Q. 72, 144, 214-216; CX-06482C (Goosey DWS) at Q. 125,180, 234; CX 01464C.) In μBGA products, the second mold chase is in contact with the polyimide layer and not the elastomeric layer. (RX-323C at 8; RX-9C (Elenius RWS)/RX 9C(a) (Elenius RWS Errata) Qs. 331, 395, 400; RX-310C; RX-311C.) Therefore, the ALJ finds that the accused products fail to satisfy this limitation of "a protective barrier in contact with the top layer."

Tessera argues that a proper application of "top layer" would mean that the "top layer" is the solder mask layer in wBGA products and the polyimide layer in the μBGA products. (CRB at 31.) However, as explained above, the evidence contradicts Tessera's attempt to create a composite single layer from the solder mask layer and copper metallization layer.

c) The "providing step"

Respondents argue that its accused products do not infringe because the BGAs are not encapsulated by a process where "a separate structure is 'provided' for the expressed purpose of protecting the solder ball pads." (RIB at 58.) The ALJ determined, however, that the "providing" step does not require the "protective barrier" to be limited to only providing protection of the terminals from the encapsulant material. *See supra* III.C.1.a (5)

d) Doctrine of equivalents

Tessera further asserts that Respondents' accused products infringe under the doctrine of equivalents. Assuming that Respondents are correct that the "array of exposed terminals

thereon" are the solder pads "within" the package substrate, Tessera argues the solder ball pads are exposed and function as the end point for the electrical connection of the package to the outside in same way as terminals that might be located on a different part of the top layer and still function to connect the chip package to another structure. (CIB at 56.) However, such a construction would vitiate the purpose of including "thereon" in the claim language, which requires the exposed to terminals to be "on or upon" the top layer. (RX 6C (Corrected Sinnadurai RWS) Q. 62, 132, 134, 204; RDX-805C.) Infringement under the doctrine of equivalents cannot stand if the "theory of equivalence would vitiate a claim limitation." *PC Connector Solutions LLC v. SmarDisk Corp.*, 406 F.3d 1359, 1365 (Fed. Cir. 2005) (citing *Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1160 (Fed. Cir. 1998)) ("As a matter of law, there can be no infringement under the doctrine of equivalents "if a theory of equivalence would vitiate a claim limitation.") Therefore, the ALJ finds that Respondents' products do not infringe under the doctrine of equivalents.

e) Conclusion

Therefore, the ALJ finds that the evidence shows that the accused BGA products have "a top layer with an array of exposed terminals thereon," namely the solder ball pads on the substrate core layer in wBGA products and the solder ball pads on the elastomeric layer of the package substrate in the μBGA products. However, the ALJ further finds that the accused BGA products fail to meet the limitation of "a protective barrier in contact with the top layer" because the evidence shows that the second mold chase is in contact with the solder mask layer in wBGA products (not the substrate core layer) and with the polyimide layer in μBGA products (not the elastomeric material of the package substrate). Respondents products fail to meet all of the claim

limitations of claim 1 and, therefore, fail to literally infringe claim 1. The ALJ further finds that Respondents' products do not infringe under the doctrine of equivalents.

2. Claims 2-4, 9-10 and 33-35

Claims 2-4, 9-10 and 33-35 depend on independent claim 1 of the '106 Patent. Inasmuch as each claim limitation must be present in an accused device in order for infringement to be found (either literally or under the doctrine of equivalents), a device cannot infringe a dependent claim if it does not practice every limitation of the independent claim from which it depends. See *Warner-Jenkinson Co.*, 520 U.S. at 40; *Monsanto Co. v. Syngenta Seeds, Inc.*, 503 F.3d 1352, 1359 (Fed. Cir. 2007). Furthermore, the Federal Circuit explained that:

> One may infringe an independent claim and not infringe a claim dependent on that claim. The reverse is not true. One who does not infringe an independent claim cannot infringe a claim dependent on (and thus containing all the limitations of) that claim.

Wahpeton Canvas Co., Inc. v. Frontier, Inc., 870 F.2d 1546, 1552 (Fed.Cir.1989).

As noted above, Respondents' accused products have been found not to literally infringe independent Claim 1 of the '106 Patent. (*Supra* B.1.a.) Therefore, since the ALJ determined that Respondents' accused products do not infringe independent claim 1, then the accused products cannot infringe dependent claims 2-4, 9-10 and 33-35.

C. The '977 and '627 Patents

Tessera has accused Respondents of literal infringement of claims 17 and 18 of the '977 patent, and claims 1, 2, 4, 9, 10, 11, 12, and 15 of the '627 patent by the importation, the sale for importation, or the sale after importation of certain semiconductor chips with minimized chip packages size. (*See* CIB at 28-29.) The primary dispute as to these claims is whether Respondents' accused products satisfy the "movable" terminals limitation. (*See generally* CIB at

31-41; RIB at 90-105.) Secondarily, it is disputed whether the accused packages have the "compliant layer."[5] The parties do not dispute whether Respondents' accused products satisfy other claim limitations. (*See generally* CRB at 28-33; RRB at 26-31.)

1. "Movable" Terminals

All of the asserted claims in the '977 and '627 patents require the "movable" terminals limitation. (*See* CIB at 29-31; RIB at 82; SIB at 19, 60.) Under the adopted construction, "movable" terminals in the asserted patents are terminals that are capable of being displaced relative to the chip by external loads applied to the terminals, to the extent that the displacement appreciably relieves mechanical stresses, such as those caused by differential thermal expansion, that would be present in the electrical connections absent such displacement.[6] (*See* Section III.C.2.(1), *supra.*)

To prove the claimed movable terminals, Tessera has proffered computer-based structural analysis of the accused packages by its expert Dr. Jianmin Qu. With the assistance of Computer Aided Engineering Associates ("CAE"), Dr. Qu used a modeling technique called finite element analysis ("FEA") to model "representative" accused packages. (*See* CIB at 36-41; CX-06486C (Qu DWS) at 38-45.) After conducting the FEA modeling on the representative accused products, Dr. Qu's expert opinion is that all of the accused packages practice "movable" terminals. (*See* CX-06486C (Qu DWS) at 99.) Staff agrees with Tessera that the accused packages practice the claimed movable terminals and finds Respondents' criticisms unpersuasive.

Respondents dispute the reliability of the FEA-based evidence. Specifically, Respondents argue that: (1) the fifty-two "representative" accused packages do not establish

[5] Respondents offer a claim construction of "compliant layer" but do not argue specifically in the initial or reply post-hearing briefs that the accused packages lack compliant layers. *See* RIB at 88-105, RRB at 44-48.
[6] The parties agree that a terminal is "an end point for the electrical connection of the package to the outside." (RX-4C (Corrected Moresco RWS) at Q. 327; CRRPFF at 959.)

infringement across all of the accused products; (2) the reliability of the underlying FEA models (completed by CAE under Dr. Qu's "supervision"); and (3) whether the FEA results, even if reliable, support Dr. Qu's conclusions. (*See* RIB at 90-106.)

The burden is Tessera's to show by a preponderance of the evidence that all of the accused packages practice the "movable" terminals limitation under the adopted construction.

a) Representative Products

FEA is a highly time-consuming modeling technique, it taking several days for computers to run a single model. As a result, Dr. Qu and CAE did not build FEA models of all of the (over 250) accused packages. Instead, Dr. Qu and CAE modeled 53 representative packages and conducted his analysis and formed opinions based on the subset. (*See* CX-06486C (Qu DWS) at Q. 220; CX-01022C (table listing the representative" packages).) Elpida alone identified over 220 accused packages. (*Id.* at 227.) The representative packages include fifteen (15) Nanya packages, three (3) Powerchip packages, three (3) "dual die" SMART packages, twelve (12) ProMOS packages, and ten (10) Elpida packages. (*Id.* at Qs. 222-226.)

Tessera argues that Dr. Qu carefully considered the accused products and chose his "representative" packages based on specific criteria. (CIB at 33 (citing CX-06486C (Qu DWS) at Qs. 229, 231).) According to Dr. Qu, he considered the following factors in choosing the representative products: (1) single versus multi-chip configurations; (2) the modulus of the die attach; (3) the thickness of the die attach; and (4) size of the die. (*Id.* at 33-34.) He represents that packages were selected "at the extremes" of these criteria in order to determine with confidence that other packages that fall within the net of those modeled would also be more likely than not to exhibit overall lifetime improvement results similar to those shown by the Modeled Elpida Packages. (*Id.*)

Respondents argue that the representative packages do not establish infringement of all accused packages. (RIB at 106.) Respondents point to Dr. Qu's testimony indicating that small changes in material properties and geometric dimension can have unpredictable effects on the claimed movement. (*Id.* (citing, *e.g.*, Qu, Tr. 648:7-649:14; 673:7-18; 673:25-674:15; 675:8-21; and 683:13-17).) Respondents argue that as a matter of law, a patentee cannot simply assume that all of the accused packages are like those tested and thereby shift to the alleged infringer the burden to show that is not the case. (citing *L&W, Inc. v. Shertech, Inc.*, 471 F.3d 1311, 1318 (Fed. Cir. 2006)).

Staff is of the view that the untested packages are likely to fall within the ranges tested as Dr. Qu and Tessera suggest. (*See* SIB at 23; SRB at 13.)

Tessera must show by a preponderance of the evidence that the tested packages are indeed "representative" of untested packages. *See Lucent Technologies, Inc. v. Gateway, Inc.*, 543 F.3d 710, 723 (Fed. Cir. 2008) ("A patentee may rely on either direct or circumstantial evidence to prove infringement."); *see also Certain Semiconductor Chip Packages With Minimized Chip Package Size And Products Containing The Same (II)*, Inv. No. 337-TA-605, Initial Determination at 55-57 (December 1, 2008) (reversed by the Commission on other grounds). While it is true that Respondents may not "simply assume" that the representative packages encompass the untested packages, "there is nothing improper about an expert testifying in detail about a particular device and then stating that the same analysis applies to other allegedly infringing devices that operate similarly, without discussing each type of device in detail." *See TiVo, Inc. v. Echostar Comm. Corp.*, 516 F.3d 1290, 1308 (Fed. Cir. 2008); *see also Union Carbide Chemical & Plastic Technology Corp. v. Shell Oil Co.*, 425 F.3d 1366, 1376-

1377 (Fed. Cir. 2005); *San Huan New Materials High Tech, Inc. v. Int'l Trade Comm'n*, 161 F.3d 1347, 1359-60 (Fed. Cir. 1998).

The ALJ finds that Dr. Qu did not "simply assume" that untested packages are covered by the representative packages. Rather, the evidence is that Dr. Qu made reasonable inferences about the untested packages based on the range of package characteristics that he selected in the tested packages. (*See* CX-06486C (Qu, DWS) at Q. 231.) As Tessera and Staff point out, Dr. Qu testified that he selected packages on or near "the extremes" of certain characteristics, such as high modulus (1000 MPa and above), low modulus (less than 500 Mpa), thick die attach (100 um and above), thin die attach (20 um or below), large die size, and smaller die packages (as determined by the diagonal of the package face). (*Id.*) He also selected single chip packages and multi-chip packages where appropriate. (*Id.*)

Moreover, Respondents provide little by way of evidence to rebut Dr. Qu's selection process and the reasonableness of his assertion that the "range" of packages tested by Dr. Qu encompass the untested packages. Rather, Respondents' seem to imply that Dr. Qu needed to test *all* of the accused products. (*See* RIB at 105-06.) The ALJ disagrees. Tessera's burden is to show by a preponderance of the evidence that the accused products infringe. To the extent that Dr. Qu's approach was reasonable, and Respondents fail to locate any specific flaws in the methodology or assumptions, the ALJ is persuaded that the representative products are demonstrative of all of the accused products.

By selecting representative products that span the range of values for those parameters that most directly affect the claimed movement, Dr. Qu has offered specific and substantial evidence as to why those accused products not selected by Dr. Qu can reasonably be expected to behave like the representative accused products.

b) The Validity of the Underlying FEA

Turning now to the modeling itself, the ALJ finds that a description by way of background is appropriate. FEA is a structural modeling technique that takes advantage of the mathematical power of computers. The first step in FEA modeling is to construct a virtual replica of the structure being exmined (the "solid model"). Real structural and geometric information should be used to build the solid model. (CX-06486C (Qu, DWS) at Q. 182-3; RRCPFF at 498.) Once built, the solid model is parceled into smaller elements, individually called "finite elements," that collectively constitute the "mesh" or "mesh model" of the replica. Critically, behavior-governing "constitutive equations" are then applied the finite elements within the mesh. (CX-06486C (Qu DWS) at Q. 196-197; RRCPFF at 500.) The equations incorporate real-world information about the inherent physical properties of the materials that comprise the particular element, such as the modulus of elasticity and coefficient of thermal expansion ("CTE"). (CX-06486C (Qu DWS) at Q. 198; RRCPFF at 501.) Once these constitutive equations are applied, the computer can be asked to calculate what happens to the model when the structure is subjected to heat or force vectors or other simulated parameters.

FEA is scientific evidence. The relevance and reliability of scientific evidence is discussed at length in *Daubert v. Merrill Dow Pharmaceuticals, Inc* . *See* 509 U.S. 579, 590-91, 113 S. Ct. 2786, 2795-96 (1993) (interpreting Rule 702 of the Federal Rules of Evidence); *see also Kumho Tire Co. v. Carmichael*, 526 U.S. 137, 119 S. Ct. 1167 (1999) (expanding on *Daubert*).[7] Although framed in the context of admissibility rather than weight, *Daubert* set-forth a non-exclusive check-list for trial courts to use in assessing the reliability of scientific expert

[7] The ALJ recognizes that the Federal Rules of Evidence, and consequently *Daubert* and *Kumho*, are not binding authority, and that the issues discussed therein pertain to admissibility of evidence rather than weight. However, as the *Daubert* Court states, "[t]he inquiry envisioned by Rule 702 is, we emphasize, a flexible one. Its overarching subject is the scientific validity -- and thus the evidentiary relevance and reliability -- of the principles that underlie a proposed submission." 509 U.S. at 594-95. Because the focus of *Daubert* is ultimately the validity of scientific evidence, the ALJ finds *Daubert* and its progeny instructive in assessing the weight.

testimony, including: "(1) whether the expert's technique or theory can be tested; (2) whether the technique or theory has been subject to peer review; (3) the known or potential rate of error in the technique; (4) the existence and maintenance of standards and controls; and (5) whether the technique or theory has been generally accepted." *See* Fed. R. Evid. 702 Advisory Committee's note.

FEA is a commonly accepted structural modeling technique, used in a wide variety of engineering applications. (*See* CPFF IV.49 (without objection at RRCPFF at 496).) Moreover, FEA results can tested or re-tested. (*See* RX-00003C (Clech DWS) at Qs. 236-38.) (Respondents' expert, Dr. Clech, testifying that he applied Dr. Qu's methodology even though he disagreed with it.) The issue with FEA in this investigation is not the general acceptability of FEA or the reproducibility of its results; the issue is whether the underlying constitutive equations and inputs used by CAE and Dr. Qu prove infringement. (*See* CIB at 39-41; CX-06486C (Qu DWS) at Qs. 181, 195-214.) For several reasons, Respondents argue that Tessera's FEA evidence is unreliable. (*See* RIB at 91.)

(1) The Relationship between Dr. Qu and CAE

As an initial point, Respondents argue that Dr. Qu did not perform the FEA modeling himself. Instead, CAE performed the FEA under Dr. Qu's "supervision." (RIB at 90-91; CX-06486C (Qu DWS) at Q. 215; Qu, Tr. at 410: 7-9.) Respondents argue that this led to unreliable results where Dr. Qu was not aware of the choices CAE made in carrying out the modeling.

The evidence is that CAE exercised substantial independent decision-making with respect to modeling the accused packages. CAE's President, Dr. Veikos, testified that his staff spoke with Dr. Qu three times to his knowledge. (Veikos, Tr. at 2475:6.) Dr. Qu stated that he spoke with CAE Staff about 12 times but could not say if it was more or less than 20 times. (Qu, Tr. at

414:7-8.) Moreover, Dr. Qu did not review CAE's native result files. (Qu, Tr. at 411:8-417:2.) Dr. Qu instead relied upon non-native files provide to him by CAE containing processed data, such as graphs and charts. (*Id.*) Dr. Qu testified that he "believes" CAE followed his instructions, but he did not check CAE's work:

> Q. Dr. Qu, what results did you get from CAE? What was the form of the results that you got from CAE?
> A. The results I got from CAE are either in tabular form or in graphics chart form, since these are the results in my expert report.
> Q. And were they in a computer file form?
> A. When you say computer file form, you mean the table is in the computer electronic form, not handwriting?
> Q. Yes, electronic form.
> A. Yes, they are, they are -- they were -- well, they are electronic forms.
> Q. They are in Excel spreadsheets, weren't they?
> A. Actually, the tables that I presented are not Excel form. They are just Microsoft Word table forms. These are the tables like, the one on page 109 of my witness statement, there is a table, and that's the table that I received from them, one of the tables I received from them.
> Q. So CAE provided you with a table that appears on pages 109 to 110 of your witness statement?
> A. Correct.
> Q. Okay. And that was in Microsoft Word form?
> A. If I remember correctly, it was in Microsoft form.
> Q. And you didn't produce that file to the Respondents, did you?
> A. But that file is this table.
> Q. You didn't produce an electronic form, did you?
> A. Was the expert report in the electronic form? I think so.
> Q. You didn't produce it in Microsoft Word form, did you?
> A. Well, I'm not so sure whether the report was in Microsoft Word form or any other electronic form, maybe in PDF form. I am not so sure.
> Q. You didn't produce the native file that CAE provided to you, did you?
> A. You mean that particular document they send me?
> Q. Yes.
> A. No, because all I did was I take that table from the document and cut and paste in my report.
> Q. If you never had the .RST files, you didn't verify the results from CAE personally, did you?

> A. I told them what to look for, and to extract the data for me and put it in this table. That's what -- I believe what they did.

(Qu. Tr. at 418:20-421:2.)

Dr. Qu's relationship with CAE is relevant because Respondents argue that CAE failed to build the FEA models in this investigation according to Dr. Qu's instructions. (RIB at 92.) Specifically, Respondents find error in CAE's models in six areas: (1) the materials properties of the package substrate and PCB materials; (2) the element geometries in certain regions; (3) the solder ball composition; (4) the plastic work measurements; (5) the mesh model convergence analysis; and (6) the stress free temperature. (*Id.* at 91-97.) Tessera argues that Respondents' criticisms are "nitpicking" – and that, "given the complexity of the models themselves and the deficiencies in the input data provided by Respondents, [perfection], although laudable, is not and cannot be practically possible – and has never been required previously." (CIB at 29-30.) Staff is of the view that Respondents criticisms are not persuasive. (SRB at 5-10.)

(2) Isotropic versus Orthotropic

Respondents' first criticism is that CAE modeled the package substrate and FR4 printed circuit board ("PCB") using the wrong constitutive equations. Specifically, Respondents argue that CAE modeled those materials as "isotropic"—having uniform properties across all three axes—when Dr. Qu testified that those materials should have been modeled with orthotropically or with different properties along the different axes. (RIB at 92.) Tessera argues that the materials properties used, *even if incorrect*, came from the manufacturer's website, Hitachi Chemical, and Respondents did not provide different moduli in responses to the interrogatories so CAE was justified in relying on the website. (CIB at 46-47.) Tessera also notes that the error would appear in all of the modeled packages (both the control or "baseline" packages and the

accused packages), therefore "tend[ ] to neutralize any effect of the mistake." (*Id.* at 47, n.22.) Staff agrees that the mistake is "cancelled out" by the fact that it was made in all if the modeled packages and the control packages. (SRB at 6.)

Indeed, Dr. Qu testified that the package substrate and FR4 printed circuit boards of the accused packages are not isotropic as CAE modeled them. (Qu, Tr. at 573:8-574:13.) The reason, he explained, is that the package substrate and PCB are reinforced with fiberglass, and as a result, they have different moduli on the x, y, and z axes. (*Id.*) More troubling perhaps than the mistake itself, however, is that Dr. Qu claims that he instructed CAE to model those materials as orthotropic as opposed to isotropic at some point in this investigation or in a prior case. (*See* Qu, Tr. at 577:20-578-4, 833:19-22.) In fact, until he was shown otherwise during cross-examination, Dr. Qu believed that CAE *had* modeled, for example, BT resin and FR4 as orthotropic. (*See* Qu, Tr. at 576:16-577:20; 836:14-839:11.) CAE's President, Dr. Veikos, very clearly testified that such was not the case, that those materials were modeled with the same moduli on all axes, i.e., isotropically.

> Q. Very quickly, Dr. Veikos, you agree that with respect to material number 3, it was modeled as an isotropic material at least with respect to its modulus of elasticity; is that correct?
> A. For whichever particular package we are discussing, that's correct.
> Q. With respect to the other material, material number 5, that was also modeled as an isotropic and not an orthotropic material; is that correct?
> A. That is correct.
> Q. Now, if you can turn to RX-4367C. And you identify that as one of the files that were deleted from the hard drives that were produced to the Respondents; is that correct?
> A. This is an ANSYS, it looks like an ANSYS output file.
> Q. And it was deleted; is that correct? A. It was not provided as part of the .db and .rst files, so if you -- how did you get this file?
> Q. We recovered it off of the hard drives.
> A. Okay. In that case it was one of the deleted files.
> Q. Yes.

> A. Yes.
> Q. Okay. If you will turn to page 26. I'm sorry, let's go to page 15 first. I jumped ahead of myself, sorry. If you can zoom in on parameter MAT name 1, 3. Do you see that on page 15 of RX-4367?
> A. Yes. Also, I would like to point out that I don't know if you are making a connection between –
> Q. Let me ask the questions.
> A. Well, I am just trying to understand.
> Q. I know. Let me follow through this way, okay? Thank you.
> A. Okay.
> Q. In this situation, this information in this deleted file indicates that material name 3 is actually the FR4 substrate; is that correct? A. Material 3 is the FR4 substrate.
> Q. If you can go to the next one shown right beneath that, the number 5, go down one more. All right. There the material number 5 is actually referred to as HL832hs. Is that correct? A. That's correct.
> Q. All right. And that's actually BT substrate; is that correct?
> A. That would be the substrate material.

(Veikos, Tr. at 2496:13-2498:18.) Indeed, Dr. Veikos' understanding was that Dr. Qu instructed CAE to model the package substrate and FR4 in that manner:

> Q. My question is very specific. Did Dr. Qu tell you to use an isotropic modulus of elasticity or Poisson's ratio for the BT substrate that you modeled in this example?
> A. Did he -- he specifically tell us to do that?
> Q. Yes.
> A. Did he specifically? I don't know if he specifically said that. We were following the instructions that he had given to us earlier to use the data if it were provided to us and if it were not, to find the data when we could.
> Q. Well, I asked you this question yesterday. Do you remember what you testified to then?
> A. I believe yesterday I said use the material data from the Respondents.
> Q. Let's see page 118, line 25 through page 119, line 4. I asked you the question: "Question: Did Dr. Qu tells you to use an isotropic modulus of elasticity or Kwason's ratio for BT substrate?" Your answer at that time is: "It is my understanding that he did for this case." Is that your testimony yesterday?
> A. That was my testimony yesterday.

> Q. Was it also your testimony yesterday that Dr. Qu instructed CAE that the FR4 was also to be modeled as an isotropic modulus of elasticity?
> A. That is my testimony from yesterday, that's correct but, again, the -- (objection).

(Veikos, Tr. at 2500:14-2501:19.) Dr. Qu had a very different recollection:

> Q. Okay. So continuing where we were, did CAE model the printed circuit board when they were constructing the models for this investigation as an isotropic material or an orthotropic material?
> A. Are you talking about the PCB or talking about the package substrate or both.
> Q. The FR4 printed circuit board.
> A. My understanding is model is orthotropic, that is, in the sense that we just talked about, in other words, X-Y direction are actually the same.
> Q. So in the CAE models, in this direction for the printed circuit board, the in plane X-Y is isotropic, but the Z direction, vertical, is orthotropic for the printed circuit board?
> A. That's the best I can remember now.
> Q. And, similarly, for the BT epoxy substrate, did CAE model that as an isotropic material or an orthotropic material?
> A. My understanding is orthotropic.
> Q. Now, when we say orthotropic, is it in plane X-Y isotropic and vertically orthotropic, or is it orthotropic in all three directions?
> A. I do not believe it is orthotropic in all three directions.
> Q. So X-Y in plane is isotropic?
> A. I think that's the case.
> Q. Okay. Now, Dr. Qu -- actually, let me back up a second. Did you discuss all this with CAE?
> A. I am pretty sure I had discussed with them, but these fundamental issues were more or less discussed earlier in prior cases because in prior cases, there were BTE, there were FR4 and so forth. So I don't recall whether I had any specific discussion with them on this particular case.
>
> ...
>
> Q. Do you remember you told us you instructed CAE to model the printed circuit board as orthotropic?
> A. Correct.
> Q. May we please go to ANSYS PSC 2. Do you understand this is an input file for an ANSYS model?
> A. Yes.
> Q. And if you look at the very top, you will see this is a file for a PSC_SPIL, the package we have been discussing?
> A. Yes.

> Q. And if we could look at the materials for the material statement for material 3, if we look down at the bottom, we will see for the CTE, there is CTE X, Y, and Z. Do you see that?
> A. Yes.
> Q. Those materials are isotropic in the X and Y plane and orthotropic in the Z plane, correct, in the Z direction?
> A. I am a little confused looking at this, because I am not so sure what the alpha X, alpha Y, ALPX, ALPY, ALPZs are. It sounds like alpha 1, alpha X, alpha Y, alpha Z. You know, the reason I am confused, alpha typically is used as the CTE. They will use alpha to represent the CTE. So I am not so sure whether these alphas are the three CTEs used in the PCB or the three CTEs used -- actually, they are the same value, okay?
> Q. They are the same value.
> A. Right. Okay. Indeed, yeah, okay, it is indeed the same value. Okay.
> Q. So as I described, in this model, the CTE for the printed circuit board is isotropic in the X/Y plane and orthotropic in the Z direction, correct?
> A. Okay, the CTE is different in the vertical direction of the PCB, that is correct, from looking at this document, material 3, material 3.
> Q. But CAE didn't follow your instructions for the modulus, did it? Can you go to the top of the list, please, highlight the material 3, EX.
> A. So here you are assuming EX is the Young's modulus.
> Q. Yes, EX is the Young's modulus, is it not?
> A. And MUXY is Poisson's ratio?
> Q. It only gives one value for EX, doesn't it?
> A. Well, it only gives one value of EX, which I am guessing at this point is the Young's modulus, but I am not so sure.
> Q. And in ANSYS, when you only give one value for EX, it automatically defaults EY and EZ to the same value, doesn't it?
> A. If I recall correctly, the ANSYS, when you assign material property, you actually select whether it is isotropic or orthotropic. Then if you select orthotropic, it asks you to input all three E's. I am not so sure. I am not so sure. Just looking at this document, I can't really say one way or the other.

(Qu, Tr. at 576:16-578:4, 833:19-42, 836:14-839:11.)

The ALJ finds this conflicting testimony problematic for obvious reasons. It appears that Dr. Qu's "supervision" of CAE's work did not catch something as fundamental as the constitutive equations of two most critical materials in the modeled packages.

While it can be argued, as Dr. Veikos does, that Respondents did not provide better modulus information in response to interrogatories so CAE used "the best information it had," the ALJ finds this argument unpersuasive. Firstly, Dr. Qu's testimony indicates that the "best information" CAE had at the time of the modeling was what *Dr. Qu* knew: namely that materials reinforced with fiberglass are not isotropic. CAE either never asked and Dr. Qu never offered this information Even though Dr. Qu was "supervising." Moreover, even if the Hitachi website was the best information CAE had, the website makes very clear that the listed modulus number (for FR4) was a "lengthwise" flexural modulus and *not* an isotropic modulus. (*See* CX-06834C.) Thus, it was not reasonable for CAE to model critical materials incorrectly based on that disclosure. On its face the Hitachi website suggested FR4 was not isotropic or at least provided no information to that effect.

With respect to the argument that the mistake is "cancelled out" because it was applied in both the baseline packages and the accused packages, the ALJ is not persuaded. This argument is problematic from the outset because the baseline packages are not necessarily thermal cycled in all of Dr. Qu's infringement analyses. Even if the cancellation argument works with respect to Dr. Qu's so-called "baseline comparison" methodology, it would not work in a situation where there is no baseline comparison such as in Dr. Qu's "direct loading" methodology. The direct loading methodology, discussed *infra*, does not involve thermal cycling baseline packages and thus mismodeling the CTE as isotropic when it is in fact orthotropic cannot be cancelled out. Furthermore, the cancellation argument is not persuasive because it is merely attorney argument. The ALJ finds no evidence on the record to support the contention that the effect of the mistake would be equivalent, discrete, linear or even similar across different packages (as the baseline and actual packages are). That may or may not be the case based on this record. What the record

does reflect is that the mistake is not necessarily minor; the moduli of the package substrates are 4 to 5 times greater in the "x" and "y" dimensions than in the "z" dimension, and the moduli of the PCB are 6 times greater in the "x" and "y" dimensions than in the "z" dimension. (Moresco Tr. at 2734:12-2735:l.)

Most importantly, Dr. Qu never investigated, quantified, or even qualitatively analyzed the error because he did not know about the mistake until cross examination. Understanding the errata of a particular methodology is key to assessing its reliability. *See Daubert*, 509 U.S. 579, 594 ("in the case of a particular scientific technique, the court ordinarily should consider the known or potential rate of error") (citations omitted). Given the precision of these finite element models and the potentially compounding effect of mistakes, it is unclear whether the mistake would make a material difference.

(3) Aspect Ratios

Respondents' next criticism is of some of CAE's geometry, the so-called "aspect ratios" of the finite elements. (RIB at 92.) Respondents argue that a forensically-recovered ANSYS file from CAE drives showed that ANSYS generated warnings during CAE's FEA runs to the tune of "7,394 of the 110,361 selected elements violate shape warning limits" – having high aspect ratios. (*Id.*; *see also* RX-2904C.) Tessera and Staff do not dispute the existence of the warnings, but argue that Dr. Qu credibly explained that ANSYS warnings do not necessarily render FEA results unreliable. (*See* CIB at 43; SIB at 6-7.) According to Dr. Qu, such warnings are "commonplace" and an experienced user can check the warnings and decide if there is a problem. (*Id.*) Tessera and Staff also argue that Dr. Qu credibly explained that higher aspect ratios do not undermine reliability when the model is converged. (*See* CRB at 4-5; SIB at 7.)

The evidence is that ANSYS will only generate a warning when that element's aspect ratio is above 20. (Qu, Tr. 427:2-3.) Dr. Qu testified that "You want that [aspect ratio] to be as close to 1 as possible...If the aspect ratio is too long in one direction, too narrow in the other, the solution becomes unstable." (Qu, Tr. 444:18-23.) However, Dr. Qu also testified that aspect ratio warnings are commonplace in meshes with 100,000 elements. (Qu, Tr. 428:20-25.) Dr. Qu even indicated that there is a "tradeoff" between high mesh density and low aspect ratios. (Qu, Tr. at 756:9-757:24.)

While the ALJ does not necessarily follow Dr. Qu's explanation of a tradeoff between mesh density and the fidelity of aspect ratios,[8] or find factual evidence to support such an opinion, the ALJ does find Dr. Qu's tie-in to convergence studies persuasive. Respondents apparently do not dispute that poor aspect ratios are not important if a model is "converged." (*See* RPFF-3845 ("*If* a finite element model has not converged, the size and shape of the elements affects the accuracy of the model.") (emphasis added).) Dr. Clech criticizes Dr. Qu's poor aspect ratios, but does not address whether poor aspect ratios remain problematic in a converged model. (*See* RX-00946C (Clech RWS) at Qs. 170-173; RPFF 3836-3889.) Accordingly, the ALJ finds that the warnings discovered in the recovered ANSYS file are not necessarily evidence of unreliable finite element modeling due to poor aspect ratios and the evidence shows that poor aspect ratios can be cured by mesh convergence studies.

(4) Mesh Convergence

[8] Dr. Qu explains that "it is sort of a tradeoff" because some of the layers in the package are thin. (Qu, Tr. at 756:15-757:1.) Of course, if the elements are *smaller*, than the thin layers is not a problem. It seems like Dr. Qu is actually talking about the modeling architecture, not the mesh density. For example, if a model were comprised of 500,000 elements, rather than the 100,000 or so elements in CAE's models, the "thinness" of a particular layer would *not* be more problematic for the model with greater mesh density.

Respondents argue that CAE performed "only 2 convergence studies for the 300 different finite element models of Dr. Qu's analysis." (RIB at 96-97.) Respondents note that each model is different in geometry and material properties, and that Dr. Qu testified that small difference in those factors can lead to unpredictable results. (*Id.* at 97 (citing Qu, Tr. at 717: 18-20; *see also* 648:7-649:14; 673:7-18; 673:25-674:15; 675:8-21; and 683:13-17).) Respondents point out that convergence studies were not done on multi-chip packages, and were not done for packages with polyimide substrates. (*See* RPFF 3901-3907.) Respondents contend that is improper for Dr. Qu to apply the results from two convergence studies to all of the accused packages. (RIB at 97.)

Tessera and Staff argue that the two "representative" mesh convergence studies performed by CAE sufficiently established that reliability of the mesh density used to model the accused packages. (CIB at 39-40; SRB at 7.) According to Tessera and Staff, the studies demonstrate that as the number of elements increase, the results will no longer change, meaning that the mesh Dr. Qu used converged and was appropriate for this context. (CIB at 39.) Tessera and Staff further argue that all of the accused packages have similar structures and shapes to the packages studied for convergence, and were modeled on a similar mesh. (*Id.*)

The parties agree that mesh convergence is an important step for building accurate FEA models. (Qu, Tr. 507:6-12; RPFF 3894.) A mesh convergence study is done by starting with a relatively coarse mesh, and gradually reducing it until the results do not vary anymore when further reducing the finite element size. (*See* CX-06486C (Qu, DWS) at Q. 333.) According to Dr. Qu, if you do not perform the mesh convergence study correctly, FEA solutions may not be accurate. (*See* Qu, Tr. 508: 1-6; RPFF 3895.)

The accused packages were modeled on meshes containing on the order of 100,000 elements. (*See* CX-06486C (Qu DWS) at Q. 188; CPFF VI.510 (no objection).) The evidence

shows that two mesh convergence studies were performed under Dr. Qu's oversight. (*See* CX-06486C (Qu DWS) at Q. 333; RPFF 3890.) According to the results of those studies, very little change occurred in the modeled structures with regard to cumulative plastic work as between approximately 70,000-element meshes and over 200,000-element meshes. (*See* CX-00382C and CX-00382C.) Dr. Qu testified that once one convergence study is performed, it is unnecessary to do another convergence study on the same kind of a structure with the same bonding conditions, and same temperature loading and so forth. (*See* Qu, Tr. 508:21-509:12.) Respondents put forth little evidence to rebut Dr. Qu's testimony in this respect. (*See* RFF 3890-3911.)

The ALJ is persuaded that the accused packages are of similar enough geometry and materials that the two convergence studies proffered establish the reliability of the mesh density. CX-00382C and CX-00383C indicate that the 100,000-element meshes used by CAE and relied upon by Dr. Qu are almost 50% denser than is required to see an appreciable decrease in percentage change in accumulated plastic work. Respondents have not persuaded the ALJ that multi-chip packages or packages with polyimide substrates are substantially different in geometry or materials that Dr. Qu's testimony is mistaken or unreliable. Accordingly, the ALJ finds that it is reasonable to infer that all of the modeled packages would converge at 100,000 elements due to their similarities with the tested packages. Moreover, because the parties agree that poor aspect ratios are cured by convergence, the ALJ finds that the ANSYS warnings Respondents recovered do not affect the reliability of the FEA relied upon by Dr. Qu.

(5) Solder Ball Properties

Respondents also challenge the way that CAE modeled the solder balls of the accused packages. (RIB at 94.)

ball

. (*Id.*) Dr. Clech modeled the two solder compositions and testified that the difference led to a 10% difference in reliability. (RX-946C (Clech RWS) at Q. 192.)

Tessera also argues that Dr. Qu used an analysis more sophisticated than Dr. Clech's, wherein Dr. Qu accounted for both solder "creep" and "inelastic" deformation and nine separate material constants (Anand's constants) in order to simulate the behavior of the solder. (*Id.*) Tessera argues that Dr. Clech's 10% difference number is not accurate because the solder creep model Respondents relied upon does not take inelastic deformation into account. (*Id.*) Finally, Tessera argues that any alleged error in the absolute number would be at least partially canceled out between the baseline and accused models, and 10% would not significantly affect reliability anyway. (*Id.*)

Staff's main argument is that any differences between what CAE should have modeled and did model for solder composition is "cancelled out" between the baseline and accused models. (SRB at 6.)

Dr. Qu testified that modeling the solder balls without copper could have substantial effects on the results:

(Qu, Tr. at 546:16-548:3; 551:1-552:2) (emphasis added).

It is difficult to rely on science that is so inexact as to suggest a deviation should be "somehow canceled out." The ALJ finds little support for this contention. Indeed, the evidence is to the contrary. Solder behavior is unpredictable and highly nonlinear:

> "For solder, it is a little more complex because the behavior is nonlinear. In other words, when you double the amount of the force, you don't get double the amount of displacement. You get a nonlinear relationship. And not only that, that stress-strain relationship also depends on temperature. So it is not purely linear elastic deformation."

(*See* Qu, Tr. at 813:17-21.) Dr. Clech testified that the "physical and thermal-mechanical properties of solders are highly sensitive to the solder alloy composition." (RX-946C (Clech, RWS) at Q. 185.) Moreover, it is important to understand that the solder balls are a *part* of the package: the effective CTE of the entire package depends on the individual CTEs of individual components. (Qu, Tr. all 831:4-21.) This would presumably include the solder ball. If using a different solder ball composition could affect both the plastic work measurement and the effective CTE of the package, and the baseline packages already contain substituted silicon and BT core material for die attach and solder mask (see discussion of the baseline packages, *infra*), the number of variables that are supposed to be "somehow cancelled out" looms ominously. The solder balls are critical because the plastic work was calculated based on their displacement. (Veikos, Tr. 2481:9-14.)

[redacted]

[redacted]. There is little record evidence that this election was sound scientifically. Dr. Qu himself testified in multiple places that the correct materials properties are important to the accuracy of the model and changing them can have unpredictable results. (*See*

Qu, Tr. 648:7-649:14; 673:7-18; 673:25-674:15; 675:8-21; 683:13-17.) At one point, he stated that modeled packages should be "identical" to one another if they are going to be compared. (*See* Qu, Tr. at 560:25-561:5 ("The criterion to make the base line has to be that the package -- the baseline package is *identical* to the actual package that you are trying to investigate in every aspect, except that the base line should have none, or less, at least, claimed movement.") (emphasis added).) If composition can have "dramatic" effects on the behavior of a solder ball, including displacement, then the changes in the solder ball composition can distort the plastic work. In order for Dr. Qu's opinion to be given weight over that of Dr. Clech, using the Anand's constants in combination with the *wrong* solder composition would need to be more accurate than using the correct solder composition without Anand's constants. The ALJ finds no evidence to that effect and in fact there is evidence to the contrary.

(*See* CX-06486C (Qu DWS) at Qs. 215-16.) Plasticity is "the deformation when the solder ball is stressed beyond its elastic limits, meaning that when the load is removed, the solder ball will not recover its original shape." (CX-06486C (Qu DWS) at Q. 212.) Thus, the importance of plasticity depends on the number of times the solder ball is stressed beyond its elastic limits. The record demonstrates, however, that CAE measured the plastic work between the first and second cycles. (Veikos, Tr. 2487:18-22.) If the plastic work calculations are done based on measurements after only one cycle, it is not readily apparent that "plasticity" will play a large role in ensuring the accuracy of the models. Once again, that may or may not be the case.

The solder balls are critical to the reliability of Dr. Qu's tests. Dr. Qu agrees that he did not have the correct solder, that small changes in the materials in solder can cause large differences in behavior, and that different compositions will have different overall CTEs and moduli. The record divulges little about Anand's constants. The proper values for each material are crucial, and the suggestion that any error will be canceled out because it is in both models is mistaken. As Dr. Qu does not account for any of these factors in his evidence, it is not reliable..

(6) Incorrect Thermal Cycle

Confounding the solder ball composition issue, Respondents contend that CAE measured plastic work during the wrong thermal cycle (between cycles one and two) and from the wrong point of measurement (then neck of the solder ball). (RIB at 94-95.) Tessera and Staff argue that that these mistakes do not render the evidence unreliable, and that to some extent the mistakes are "cancelled out" because they were made in both the baseline and accused packages. (CRB at 10; *Id.* at n.10; SRB at 8.) Staff asserts that Dr. Qu never testified that measuring plastic work after the first cycle was improper. (SRB at 8.) Staff also argues that CAE took plastic work measurements from the location that Dr. Qu indicated. (*Id.*)

Once again, Tessera does not adequately overcome the evidence put forth by Respondents. Despite Tessera's and Staff's creative interpretations of CX-6486C at Q. 257-58 (*see also* CX-00384C), Dr. Qu did in fact testify in this investigation that the plastic work is still changing between the first two thermal cycles. Dr. Qu's own work cycle convergence study, CX-00384C, shows that the plastic work is changing fairly significantly during that period. (*See* CX-00384C ("Cycle Convergence Study…').) Dr. Veikos testified that CAE calculated plastic work between cycle one and cycle two. (Veikos, Tr. at 2487:18-22.) It is purely attorney argument to suggest that this evidence does not affect the reliability of Dr. Qu's analysis. The ALJ's

interpretation of Dr. Qu's witness statement is that he intended the plastic work to be taken at two cycles *because* "the plastic work stabilizes." (CX-6486C at Q. 257.)

Regarding the recurring "canceling out" argument, the incorrectness of the argument could not be clearer than with respect to this issue. The whole point of Dr. Qu's Cycle Convergence Study was to determine the best time period to take measurements for the plastic work, considering all of the factors including the time required to run models and the reliability of measurements. Dr. Qu's study shows that the plastic work measurement will be more accurate after the second cycle because it is changing very rapidly prior to the second cycle. It is true that any inaccuracies would affect both the baseline and accused package measurements as Tessera and Staff point out, but it is not true that the effects of the inaccuracies would cancel out. In point of fact, the inaccuracies will affect *both* packages and thus actually *compound* the inaccuracy, rather than assuage it.

With regard to the location of the plastic work measurement on the "neck" of the solder ball, the ALJ agrees with Staff that Respondents point to no evidence that explains what Dr. Veikos meant by "the neck" of the solder ball. (*See* CX-06486C, pp. 72-73, Q. 314, and Veikos, Trans. at 2145:8-14.)

(7) Stress-free Temperature

In Respondents' final criticism of CAE's work it is argued that CAE used the wrong stress free temperature in the FEA it conducted for Dr. Qu. (RIB at 97-98.) Specifically, Respondents contend that the stress free temperature directly impacts plastic work calculations, and with CAE's finite element models, artificially inflates plastic work values. (*Id.*) As a result, Dr. Qu's percentage life improvement values are unreliable. (*Id.*)

Tessera argues that Respondents do not demonstrate that the stress free temperature CAE used rendered unreliable results. (CRB at 10.) Tessera argues that Respondents "overlook" the fact that Dr. Qu's range is "the same as or less than the typical temperature range used by most manufacturers (including the Respondents) when performing accelerated life testing of their products." (*Id.*) Accelerated thermal cycle testing is commonly used by most manufacturers because doing effective reliability testing at normal temperature ranges would simply require much too long a testing cycle. (*Id.*)

Staff argues that Dr. Qu explained that the reference temperatures were selected because they mimic the manufacturing and assembly process of the packages. (SRB at 9.) Staff's view is that Dr. Qu explained in detail that each of the Respondents' packages is overmolded and during the overmolding process, particularly during the curing phase, the liquid molding material cools to a solid phase and it induces residual stresses on the package, and more residual stresses are generated once the package is at room temperature because of the CTE mismatch between the mold compound and other materials in the package. (*Id.*) Thus, to simulate the package stress-free temperature, i.e. the temperature where there is no residual stress on the package, the reference temperature was set to 175 degrees C for off-board packages. (*Id.*)

Dr. Qu used different stress-free temperatures for moiré analysis and finite element modeling: 125 degrees C for moiré, and 175 degrees C in the FEA. (CX-06486 (Qu DWS) at Q. 252, 262.) In an actual computer, the junction temperature of solder balls can probably get to about 70 degree C or 80 degree C, but probably not 180 degrees C. (*See* Qu, Tr. at 628:12-18; RPFF 3825.) Dr. Clech testified that having the exceedingly high stress-free temperatures "exaggerates the amount of thermally induced strain." (CX-946C (Clech RWS) at Q. 271.) Dr. Clech refutes Dr. Qu's justification for the higher temperature on the basis that even if used in

certain industry applications, "there is no need; however, to utilize the extreme temperature ranges of accelerated thermal cycling in a simulation of operating conditions, and Dr. Qu failed to explain why such temperatures should be used." (*Id.* at Q. 272.)

The ALJ finds that Respondents have not directly refuted Dr. Qu's explanation of the stress free temperatures. The ALJ is persuaded that cycling the accused products at the temperatures used corresponds to those used in reliability testing in the industry, and Respondents have not provided reasons as to why that it inappropriate here. Similarly, Respondents have not shown that "operating" temperatures are controlling under the claim construction.

c) Conclusion

To summarize, Tessera's underlying FEA evidence is suspect in several respects. CAE modeled the package substrate and the PCB as "isotropic" when Dr. Qu clearly intended that those materials be modeled as orthotropic. The solder balls—critical in the calculation of the plastic work—were modeled with the wrong material composition without adequate justification. Moreover, CAE calculated plastic work between cycles one and two, contrary to Dr. Qu's intentions and testimony that the packages are not stable at that point. There are also less persuasive concerns regarding the thousands of ANSYS warnings, the mesh convergence studies, and the stress free temperatures. The overall impression is that Dr. Qu and CAE were not on the same page regarding many aspects of the FEA. The ALJ finds it difficult to find infringement on evidence that had admitted errors without quantitative or at least qualitative explanations of those errors. It is also difficult to find the maintenance of "adequate standards and controls," as the *Daubert* case termed it, given that Dr. Qu was unaware of important aspects of CAE's work such as the directional moduli used in the package substrate and PCB, the number of ANSYS

warnings generated, the time point at which plastic work was calculated, and so forth. It is not clear that some of the specific methods Dr. Qu relied upon in this specific application of FEA would stand up to peer review.

Ultimately, it is not Respondent's burden to prove that Tessera's proffered evidence is false; rather, it is Tessera's burden to show that the FEA evidence it has supplied is reliable. For reasons stated above, the ALJ finds that Tessera's FEA evidence is not reliable.

2. Baseline Comparison and Direct Loading Methodologies

The baseline comparison test is Dr. Qu's primarily methodology of proving infringement. (*See* CIB at 35-36; 42; CX-06486C (Qu DWS) at Q. 264.) The test consists of modeling, in ANSYS, control packages specially designed to lack the claimed movement and comparing them to the accused packages to demonstrate that the claimed movement exists. (*See* CX-06486 (Qu DWS) at Q. 265.) The control "baseline" packages were created by replacing the behavior-governing values of the compliant die attach and solder mask materials with the values of more rigid silicon and package substrate core material, respectively. (CX-06486 (Qu DWS) at Q. 267-68.) Dr. Qu stated that the base line packages were designed to be "in all respects the same as the package being modeled, with the only changes being to eliminate or minimize the claimed movement." He stated he then had CAE model those packages in FEA, and compared them to the accused packages. (Qu, Tr. at 740:25-741:2.) Based on the FEA results, Dr. Qu's opinion is that the baseline packages do not have the claimed movement and the accused packages do have that claimed movement. (*See* CX-06486C (Qu DWS) at Q. 99.)

Respondents argue that the baseline packages are not a valid control package. Respondents specifically argue that the baseline comparison test does not isolate movement due to "external loads" as required under the adopted construction. (RIB at 100.) Respondents also argue that the baseline packages do not have the same geometric and materials properties of the accused packages and therefore are not "the same in all respects." (*Id.* at 102.) Respondents point to differences in the thickness and effective CTE of the baseline packages compared to the accused package, and conclude that "it is impossible to know whether Dr. Qu's purported reliability improvement results from the change in the effective CTE of the baseline package or from the claimed "movable" terminals." (RIB at 101-102.)

Tessera obviously disputes Respondents' criticisms of the baseline comparison methodology, as does Staff. (*See* CRB at 2-11; SRB at 11-12.) Tessera argues that "[p]reliminarily, but very importantly, Respondents' experts performed no FEA analysis of any of Respondents' on-board products to attempt to show that the Accused Packages do not infringe the asserted claims, even though they clearly could have done so." (*See* CRB at 2.) Tessera also argues that "Respondents…present no evidence that such alleged 'errors' actually affect the overall conclusion that Respondents' products infringe." (*Id.* at 9.) Staff argues that Dr. Qu replaced the die attach and solder mask with stiffer materials because he believed that these are two features of the accused products that permit the claimed movement. (SRB 11-12.) In Staff's view, Dr. Qu was able to determine that at least a portion of the displacement in the accused packages is caused by external loads and that the portion of the displacement caused by the external load appreciably relieves stress in the solder balls and thus improves package reliability. (SIB at 23-24.) Staff also contends that Dr. Qu confirmed his results from the FEA models "by

conducting other tests, such as Moire analysis," a physical test where the actual chip package attached to the PCB is tested. (*Id.* at 24.)

The ALJ notes at the outset that the burden is Tessera's to show that any errors that are admitted are not material, that is, they do not affect the results. While Tessera need not necessarily quantify the portion of movement due to claimed movement in every case, it is insufficient to merely state that Respondents criticism are not demonstrably dispositive of the FEA results. There must be a preponderance of evidence to that affect. To the extent that errors are not quantified, Tessera must provide evidence that at least suggests the error are not material.

(1) The "similarity" of the baseline packages

The first issue is whether the baseline packages are "similar in all respects" as Dr. Qu testified is necessary for baseline comparison methodology to work. (*See* Qu, Tr. 740:25-741:2; CX-06486 (Qu DWS) at Q. 265.) Respondents argue that the baselines are not the same in every respect. (RIB at 102.) Tessera and Staff argue that Respondents have not shown that the differences are important. (*See* CRB at 13 ("Other Arguments"); SRB 4-13.)

The evidence is that the baseline packages are not the same in every respect minus the claimed movement. The replacement of the compliant layers in the accused packages, comprising die attach and/or solder mask, with silicon and BT core material in the baseline packages affects not only the stiffness of the packages—which perhaps is the closest factor that might permit in the claimed movement— it also affects the effective CTE of the packages. This potential change in the effective CTE is important. If the effective CTE of an accused package is different than its corresponding baseline package, any analysis of the differences in observed terminal-to-chip displacement between the two packages would take on added complexity. Not only would one need to determine how much the difference in the observed displacement was

due only to external loads, but one would also need to account for how much of the observed displacement is due to internal loads caused by the differences of CTEs of the two packages. While terminal-to-chip displacement due to external loads is the claimed invention, terminal-to-chip displacement from internal loads was disclaimed by Tessera, and is, therefore, not part of the claimed invention. The question, therefore, is just how significant to the analysis is the difference in the effective CTEs of the accused and baseline packages.

The ALJ finds that any change in the effective CTE of a package is highly problematic because it is difficult to overstate the importance of distinguishing the claimed movement from terminal movement due to "CTE matching." CTE matching is prior art. (*See* the '977 Patent at Column 1, ll. 59-68; Column 2, l. 1; Column 3, ll. 52-65; Column 5, ll. 58-67; Column 7, 51-59; and likewise in the '627 Patent.) As Dr. Distefano testified, the inventors understood that CTE matching was one solution to the DTE problem in chip packages:

> A. … The problem was how to attach a chip with a low expansion, about three parts per million per degree C, to these circuit boards with expansions of about 17. And that was a problem, to attach the chip to a circuit board where the circuit board expands and moves relative to the chip, and to do that attachment reliably.
> Q. Why did that present a reliability issue?
> A. What happens is that the electrical and mechanical attachment of the chip to the circuit board is stressed as the circuit board expands more than the chip. And that expansion over cycles will cause failure of the connection, usually a solder connection.
> Q. Why not just use lower expansion materials then?
> A. Well, at the time all of the – most of the multi-chip modules in the world were low expansion. Around the world companies had spent billions of dollars to develop low expansion substrates, most of them ceramic that was a standard approach.
>
> Q. What was your solution?
> A. What we did was to decouple the expansion of the circuit board from the expansion of the chip, to allow the circuit board to expand and move without inducing stress on either the circuit board, chip or the connection between the two.

> Q. You used the word decoupling. Can you explain to the Court what you mean by that in this context?
> A. Decoupling as we used it was allowing the circuit board to move, and the connection between the circuit board and the chip to move or decouple from the chip itself. So the terminal on the chip package could move to follow the expansion of the substrate without being coupled rigidly to the chip.
>
> Q. You said it was unorthodox. In what way was it unorthodox?
> A. ***The orthodox approach was to match the expansion of chip to substrate***, look at various solder compositions that would allow the solder ball to flex somewhat. That was the industry approach. Ours was to allow the chip package to actually deform. For us, for me, at least, personally, it was unsatisfying because now the package was not precisely defined but it is something that was rubbery or deformable.

(Distefano, Tr. at 154:4-155:9; 156:7-23; 158:15-159:2.) (emphasis added)

Based on the plain language of the patent, and the testimony of Dr. Qu and Dr. Distefano, is clear that the die attach layer facilitates CTE matching, and that the CTE matching appreciably relieves the stress on the connections. By changing the effective CTE of the package, the possibility of CTE matching as the source of solder stress relief in the package is not accounted for. Without measuring, estimating, or otherwise quantifying the effective CTE of the baseline packages due to the thicker silicon and solder mask substitutions, the ALJ agrees with Respondents that it is "impossible to tell" whether the relief measured by Dr. Qu is due to the claimed movement or due to CTE matching or a combination of the two. While it is true that the presence of *some* CTE matching does not exclude the possibility of the claimed movement, that ALJ finds that its presence must be accounted for and quantified in some fashion to know that there is *some* claimed movement, and, if there is some claimed movement, that it, and not CTE matching, is providing appreciable relief of stress on the solder balls.

Dr. Qu stated that the baseline packages would need to be "identical" to the accused packages except without the compliant layer. (Qu, Tr. at 560:25-561:5.) Yet, by substituting silicon into the baseline packages Dr. Qu changed more than just the flexibility of the compliant layer; he also changed the effective CTE of the package. Dr. Qu never quantified the significance of this change in CTE, and thus the ALJ finds it erroneous to compare the simulated deformation of the baseline packages to the simulated deformation of the accused packages. While Tessera is correct when they argue that they do not have the burden to prove all change in the motion is due to the claimed movement, they must prove that there is at least some "claimed" movement and that the claimed movement is enough to provide significant relief to the stress. They have failed to do so.

(2) CTE matching

Tessera argues that "the use of 'CTE-matched" BT-resin package substrates, where the CTE of the package substrate is matched to the CTE of the PCB, simply does not mean that the claimed movement *cannot* be found, despite Respondents' arguments to the contrary. (*See* CPFF VI.474-76 (emphasis added).) While this statement may be correct, it is arguing the wrong issue. Even if CTE matching does not preclude the possibility that the package could have claimed movement, it does prove that there is movement within the package that is not the claimed movement and that movement alone can relieve stress on the solder ball. We must focus once more on the fact that Tessera must provide the evidence of infringement; it is not Respondents burden to show that a portion of the stress relief is *not* due to the claimed movement; rather, it is Tessera's burden so show that the claimed movement *is* at least partially responsible for the significant stress relief. In other words, Tessera must demonstrate or isolate the claimed

movement to a degree that it is clear the claimed movement is providing the appreciable stress relief, not the CTE matching. While we need not quantify the claimed movement to a mathematical certainty, the burden on the Tessera requires quantification to the degree that they prove there is claimed movement, not just CTE movement, and that claimed movement alone, not combined with CTE, provides significant relief on the solder joint. In the absence of such proof, Tessera's case fails. As Tessera says, "Tessera's invention can work in conjunction with "CTE matching" (*See* CPFF 476-77), yet they must prove its workings provide significant stress relief.

Tessera's argument is, essentially, that "it is impossible to conclude that CTE-matching has so effectively occurred that there are no stresses in the solder ball to be relieved using the patented Tessera technology." (CIB at 42-43.) Note that this reasoning stands the burden of proving infringement entirely on its head. Respondents do not have to prove that the CTE matching "has so effectively occurred that there are no stresses in the solder ball to be relieved using the patented Tessera technology." Rather, Tessera must prove that the claimed movement is, in fact, there and that it is providing the claimed significant relief. Until we know the relief provided by the CTE matching, and the presence of even greater stress relief due to "claimed movement" alone, Tessera has not met its burden, and no amount of confusing the issue can make it so.

Tessera also argues that it is Respondents' burden to show that Dr. Qu and CAE did not use reasonable numbers within the ranges of materials properties. The materials did have a range of moduli, and thicknesses, and these values certainly impact the performance of materials in actual function. Dr. Qu did not perform the tests for his analysis himself, and did not review the data that was used to run the tests, but only received an excel spread sheet of the results of

interest to him. As Tessera bears the burden to prove infringement, and their proof does not even inform us of what material properties were used to achieve the results, the proof must fail. In effect, the expert, Dr. Qu, is not even saying "trust me, I put in good numbers," but asking the Commission to trust that *CAE*, not modeling *experts*, put in valid figures, even though Dr. Qu did not see inputs and they were not offered in evidence. He further asks us to trust that they did so in a manner that would provide valid results. When this caliber of evidence is offered to prove infringement, it cannot succeed.

While it may be true that the compliant layer is the heart of the invention, and thus it "makes sense" to remove the compliant layer to make a control or baseline package, the ALJ nonetheless finds that the results of Dr. Qu's comparison tests do not account for the possible improved reliability in the accused packages due to CTE matching. The baseline packages are not the same in every material respect to the accused packages except the claimed movement, and thus the baseline packages are not reliable controls upon which Dr. Qu could base his opinion. Indeed, we know that neither the baseline packages nor the packages used for comparison have the same material qualities as Respondents' actual packages.

(3) Terminal to chip displacement measurements

Assuming *arguendo* that the baseline packages are reliable control packages for comparison, Respondents argue that Dr. Qu never measured the *relative* displacement between the terminals and the chip contacts even though that is what the claimed movement requires. (RIB at 98-99.) Respondents note that Dr. Qu instructed CAE to measure the relative displacement between the terminal and a point on top of the chip rather than the bottom of the chip which would be more accurate. Respondents argue that Dr. Qu instructed CAE to measure displacements exactly where there would be the greatest movement. (*Id.*)

Tessera argues that Dr. Qu's measurement of relative displacement is acceptable because "what is important is relative – not absolute – displacement." (CIB at 47-48.) Specifically, Tessera argues that so long as one point is consistently chosen, "it does not matter what point on the chip is used to determine whether the terminals move with respect to the chip." (*Id.*)

Staff agrees that there is nothing wrong with choosing a particular point on the top of the chip to measure relative displacement. (SIB at 11.) Staff's view is that although the absolute value for the relative displacement may be affected by the choice of a particular point, that number does not affect the ultimate conclusion of infringement. (*Id.*)

Most of the accused packages in this investigation are in the "face-down" disposition, although a few if Elpida's packages are in the "face-up" position. (CX-06486C (Qu DWS) at 494, 515; Qu, Tr. at 524:3-525:3.) Dr. Qu testified that measuring the displacement at the top of the chip is a way of determining the displacement of the *chip contacts* because "it doesn't really matter where you measure the chip…the chip, it really doesn't deform a whole lot…it is only a little bit different." (Qu, Tr. at 526:11-20.)

Dr. Qu's explanation of his "indirect" measurement is reasonable, but it does not answer the question of why the measurement was not taken from the terminal itself. Dr. Qu's logic also leaves room for variables, seen and unseen, that might affect the reliability of measurements taken indirectly where those measurements could have been taken directly. Taking the measurements from the top of the chip rather than the chip contacts introduces unnecessary uncertainty. However, Respondents have not produced any evidence indicating that the degree of uncertainty introduced by the peripheral measurement would change the result. Respondents concede that the ".rst" ANSYS files produced to Respondents have relative displacements between every point within a finite element model. (*See* RFF 3548-3570.) If Respondents felt

that Dr. Qu's measurements were in error, Respondents were free to demonstrate the difference between measuring the relative displacement change between the top terminal and chip, versus the top of the terminal and the top of the chip. In the end, it is unclear whether the top of the chip is a reasonable proxy for the purposes of calculating the displacement of the top terminal, but Dr. Qu's explanation is the best evidence available.

b) Moire Validation

Tessera and Staff argue that Dr. Qu "validated" the displacements of the baseline packages calculated by ANSYS using a real-world physical technique called moiré. (*See* CIB at 41; SRB at 1.) Moire is a technique for determining the deformation of a structure using laser pattern analysis. (*See* CX-06486C (Qu DWS) at Qs. 384-94.) Lasers are projected onto the surface of a structure at rest as a control, then the structure is subjected to conditions that cause deformation and the lasers are re-projected onto the structure surface. Based on the difference in the patterns, the amount and direction of deformation can be compared to the amount and direction of deformation predicted by FEA. After conducting Moire on the accused packages, Dr. Qu concluded that the FEA and Moire results were in substantial agreement, "confirming" the FEA technique. (*Id.* at Q. 415.)

Respondents argue that using Dr. Qu's own moiré images, the evidence shows that there is strong coupling between the chip and substrate package at the measured temperature in the accused packages. (RIB at 103; RX-946C (Clech RWS) QQ. 97-100.) Chip/package substrate coupling is evidence, according to Respondents, that the accused packages do not have the claimed movement. (*Id.*)

Staff agrees with Tessera that Dr. Qu's moiré analyses are reliable and confirm the FEA. (SIB at 9-10.)

The ALJ agrees that Dr. Qu's moiré confirms Dr. Qu's FEA to an extent that ANSYS predicted the actual displacements of packages to a reasonable degree of accuracy. However, as Dr. Qu stated:

> Most importantly though, moiré results, regardless of how accurate they are or how many packages are tested, cannot by themselves prove infringement. They only show displacement. They ***do not allow measurement of whether there has been appreciable relief of stress within a particular package, as required by the claims of the asserted '977 and '627 patents.***

(CX-06486C (Qu DWS) at Q. 405.) (emphasis added). Thus, while Dr. Qu's moiré result does not contradict the displacement results of the FEA, it does little to confirm the baseline comparison methodology and does not confirm any claimed movement.

c) Direct Loading Methodology

In addition to the baseline comparison test, Dr. Qu performed an FEA-based, on-board/off-board comparison that Tessera calls the "direct loading methodology." (*See* CIB at 41.) The direct loading method is a second test conducted by Dr. Qu that does not involve thermal cycling the "baseline" packages – which invokes the CTE matching problems described above.

The direct loading methodology is an FEA-based test that compares the movement of the chip package attached to the PCB ("on-board") with the chip package not attached to the PCB ("off-board"). (*See* CX-06486C (Qu DWS) at Qs. 448-461.) The way the method works is that each of the packages are modeled in FEA and thermal cycled. The displacements of the off-board and on-board packages are determined from measurements taken from the bottom of the solder balls. The loads of the on-board and off-board FEA results are calculated based on the displacements. The load of the package off-board is subtracted from the load of the package on-board. (*Id.*) The difference between the two loads is presumptively the "external load." Once

the external load is known, it is directly applied to the actual and baseline packages, plastic work computed, and reliability determined. (*See id.* at 454.)

The concept behind the direct loading method is that the on-board package is subject to both internal and external loads, but the off-board package is subject to only internal loads. Thus, the difference between the two loads is the external load. (*See id.* at 450.) The purpose of the direct loading methodology is to isolate the amount of external load placed on the accused packages, which is complicated to do in the baseline comparison test because the substitution of silicon and BT core material changes the effective CTE of the packages. In the direct loading methodology, the effective CTE of the baseline package is irrelevant because the baseline package is never thermal cycled.

(1) The "Linearity" Assumption

There are several critical assumptions that must be valid for the direct loading methodology to be reliable. The first critical assumption is the linearity assumption. "The linearity assumption is the assumption that all materials in the system behave in a linear way." (CX-06486C (Qu DWS) at Q. 450.) Dr. Qu testified that the linearity assumption is not necessarily reliable as applied to these packages:

> Q. Can you tell us what types of methodologies or what different methodologies did you use to analyze the accused products?
> A. There are basically two types of methodologies . . . Then in one chapter I presented alternative method. That alternative method used the so-called linearity assumption. Okay? Now, that alternative method, as I discuss in my report is not an exact method because you have used the assumption that a system is linear. If you know the system linearity is very weak, then that might be a good assumption. Therefore, the solution might be a good one. But if the nonlinearity is very high, that may not be. ***So I do not rely my opinion on that alternative methodology.***

(Qu, Tr. 806:17-807:14) (emphasis added). In addition, in his rebuttal witness statement, Dr. Qu testified that the second testing method is not necessary:

> This approach serves only a confirmatory purpose, in that it just further confirmed the opinion I had already formed after conducting the first onboard analysis. The use of the second method is not necessary....

(CX-7348C (Qu RWS) at Q. 68.)

The record is clear that Dr. Qu did not rely on the second testing method because, among other things, he had not established the prerequisite that any of the accused packages were only "slightly nonlinear." Dr. Qu testified:

> Q. Now, you have not determined if the components of the accused packages are slightly nonlinear or very nonlinear, as you understand slightly nonlinear and as you understand very nonlinear, have you?
> A. That is correct.
> Q. You have not determined if the accused packages are slightly nonlinear or very nonlinear as you interpret slightly nonlinear or very nonlinear, have you.
> A. That is correct.

(Qu, Tr. at 604:5-15.)

Tessera acknowledges the difficulties posed by this assumption:

> In addition to his primary methodology of comparing on-board actual and baseline packages, Dr. Qu also perform[ed] a completely separate, alternate moveability analysis, which relies on the "linearity assumption." The linearity assumption presumes that all materials in a system behave in a linear way, thereby making it possible to calculate the amount of displacement of the terminals in the package due to external forces as a result of thermal cycling. The biggest difference between Dr. Qu's primary approach and the alternate approach is that the first approach is an exact method. ***The alternative approach, in contrast, provides an approximation, which may be good if the degree of non-linearity in the assumption is relatively low.*** ...[B]ut it is not necessary to his conclusions. Instead, it simply provides further confirmation

> for the infringement conclusions reached using the primary methodology.

(CIB at 41-42 (internal citations omitted) (emphasis added); *see also* CSRB at 7; SIB at 18.)

(2) Internal and external relief

The linearity assumption is not the only assumption in the direct loading method. Tessera also assumes that because there is no stress on the solder ball off-board, the only relief of stress that will be observed in the accused packages is necessarily due to displacement of the terminal from the external effects of the PCB tugging on the solder ball. (CRB at 9-10.)

Tessera's suggestion that the only relief of stress that will be observed in the accused packages is necessarily due to displacement of the terminal from the external effects of the PCB "tugging" on the solder ball, is patently false. While it is true that the PCB can expand more than the substrate and package, stress relief can also come from increasing the CTE of the package, as the patents state.

Dr. Qu testified that internal forces can stress the joints, external forces can stress the joints, or if the movements are similar, the combined forces do not lead to an increase in the stress on the solder balls:

> Q. Dr. Qu, do you remember last Friday during your tutorial, Judge Essex asked you a few questions? Do you remember that?
> A. Yes, I do.
> Q. One question that Judge Essex asked was: "If the internal force is such that the terminal moves at the same rate as the bottom of your solder ball, you have zero stress on the solder, will you not?" Do you remember that question?
> A. Yes, I do.
> Q. And you responded, "yes, agreed." Do you remember that?
> A. Yes, I do.
> Q. And then Judge Essex asked you, "so the internal force has a lot to do with the stress of the solder ball if it is matched to the PCB. Is that not correct?" Do you remember that?

A. I don't remember the exact wording, but something to that extent.
Q. And you responded, "if it is theoretically matched perfectly, it moves exactly by the same amount, there will be no stress in the solder. In that case, there is no external force. Right?" Do you remember that?
A. Again, I don't remember the exact wording, but roughly the idea is correct.

. . . .

Q. Now, Dr. Qu, on Friday, Judge Essex asked you another question. Judge Essex stated: "Let me ask you another hypothetical. Let's assume these various things heat up at different times. The chip will probably get hot first, then the substrate and eventually the PCB board it seems to me, if the substrate is expanding and the PCB is not yet heated up, so it is not expanding, you would have stress on the solder ball, would you not? Do you remember?" And you responded, "yes, correct." Do you remember that?
A. Yes.
Q. Judge Essex then followed up with: "But the only force that I can see is that that's being applied by the expansion of the substrate, correct?" And do you remember that?
A. Yes, not word by word, but that's, I think, what roughly, what it is.
Q. Okay. Now, let's walk through a hypothetical here. Now, suppose a plastic ball grid array package is mounted on a printed circuit board in an electronic device which is a computer, okay?
A. Okay.
Q. And the power is turned on, correct?
A. Okay.
Q. And so an electrical current starts flowing through the chip, right?
A. Okay.
Q. As the current flows through the chip it falls through a voltage drop, so it is generating power, correct?
A. Can you repeat again?
Q. As the electrical current flows through the chip, it goes through a voltage drop so it starts generating power, correct?
A. I didn't hear the word, because of what?
Q. Let me rephrase it. As the electrical current flows through the chip, it generates power, correct? I will strike and ask it again. As electrical current flows through the chip, the chip starts to heat, correct?
A. Correct.

> Q. And the chip starts to heat, and the silicon starts to expand, correct?
> A. Correct, not as much, but it does.
> Q. And as the silicon of the chip heats, that starts to heat the package substrate, correct?
> A. Correct.
> Q. And as the package substrate starts to heat, it starts to expand, correct?
> A. That is also correct.
> Q. And the solder balls are under stress, correct?
> A. Just to confirm that this is a package on the PCB, right?
> Q. Yes.
> A. Yeah, when the package expands more than the PCB does, because PCB at this point is not warm enough yet, yes, the solder joint will be subject to stress because the PCB is holding the bottom solder back, not letting it move outward.

(Qu. Tr. at 563:9-564:12; 600:16-306:7.) Since any of the movements in the package and PCB can result in more stress on the connection, or less stress on it, it is not correct to assume that solder is stressed only by "external" forces. Anytime the relationship between the terminal on the substrate and the terminal on the PCB changes, relative to each other, the amount of stress on the solder will change as well.

Dr. Qu ran tests on the movement of the actual packages as they thermal cycled off-board. The amount of movement he quantified in the off-board modeling in the FEA analysis of the off-board packages was due entirely to the CTE of the accused packages; that is the internal movement. Tessera argues that this movement is not relevant because it relieves no stress, as if there were solder balls attached to the package, and they were not attached to a board, the movement would cause no stress, and relieve none. While true, this does not address the correct question, which is, when the package is thermal cycled in the model as if it were on the board, could the CTE of the substrate account for all the observed movement of the solder balls? Dr. Qu's analysis of the actual packages when they were theoretically attached to a PCB board resulted in less total movement than he observed in the off-board movement of the same

packages in most cases, and where the on-board model had more movement than the off-board test, the differences were negligible.

Because the "claimed" movement is not isolated or quantified, his results are flawed, and cannot demonstrate that the Tessera invention is providing any improved reliability, and therefore cannot demonstrate that reliability is appreciably improved.

All or substantially all of the movement of the terminals can be accounted for by the CTE of the substrate. The "tugging" theory merely assumes that there is claimed movement without accounting for CTE matching. As Dr. Qu only measures the movement of the bottom terminal, and uses a mistaken value for the material properties of the solder, we do not know, through any evidence offered in the case, what actually or virtually happens to the terminal on the substrate (at the top of the solder ball). If the solder deforms before the substrate would move, there could be no stress relief at all. The point is: if we do not know the movement of the top terminal, we know nothing about potential stress relief.

(3) Bottom of the solder ball

Another problem with the alternative methodology is that the displacement of the on and off-board packages was measured from the bottom of the solder ball. Dr. Qu explains that doing so is acceptable because the solder ball moves at the bottom in the same manner as the terminal at the top, because there is no PCB holding the bottom of the solder ball or pulling it. While this is true for the off-board situation, we know from the lab notebooks, the claims, the patent and the inventor's testimony that when the package is mounted on a PCB (i.e. in the on-board situation), the top and bottom of the solder move differently. The terminal on the substrate (the top of the solder ball) does not move with the terminal on the PCB. If the solder has deformed, which does

happen according to the patent, the top terminal may not have moved at all. By only measuring at the bottom of the solder ball, and subtracting what the top did off-board from the bottom of the solder ball's movement on-board, and calling that the claimed movement, we are assuming that movement exists, not proving it, and in so doing we are assuming that infringement exists, not proving it. The bottom of the solder ball moves differently when it is on a PCB board than when it is off. But what happened at the top is not known. Further complicating this problem is the fact that the linearity assumption is weakest in the one material in the package that is most critical for the assumption, the solder itself.

So, when you take a measurement from the bottom of the solder ball, and assume that it is an approximation of the top of the solder ball, you are mistaken. Without measuring the movement of the top terminal, under Dr. Qu's on-board modeling, you do not know if the top terminal, the terminal on the substrate has a) moved at all, but stayed in place and the solder deformed, b) if it moved exactly as it did off-board, again, its movement not being mirrored by the terminal at the bottom of the solder ball, because the solder deforms, or c) something else happened. Without evidence proving a strong correlation demonstrating the displacement of the bottom of the solder ball and the top of the solder ball, to assume they are the same assumes the entire "movable" terminals element.

The burden is Tessera's to prove infringement, and it is not met using the direct loading evidence.

V. VALIDITY

A. Background

One cannot be held liable for practicing an invalid patent claim. *See Pandrol USA, LP v. AirBoss Railway Prods., Inc.*, 320 F.3d 1354, 1365 (Fed. Cir. 2003). However, the claims of a

patent are presumed to be valid. 35 U.S.C. § 282; *DMI Inc. v. Deere & Co.*, 802 F.2d 421 (Fed. Cir. 1986). Although a complainant has the burden of proving a violation of section 337, it can rely on this presumption of validity. A respondent that has raised patent invalidity as an affirmative defense must overcome the presumption by "clear and convincing" evidence of invalidity. *Checkpoint Systems, Inc. v. United States Int'l Trade Comm'n*, 54 F.3d 756, 761 (Fed. Cir. 1995).

B. Priority Date Of The '997 Patent and '627 Patents

1. Conception

"Conception is the 'formation in the mind of the inventor, of a definite and permanent idea of the complete and operative invention, as it is hereafter to be applied in practice.'" *Shum v. Intel Corp.*, 499 F.3d 1272, 1277 (Fed. Cir. 2007) (citation omitted). "Conception is complete when the idea is so clearly defined in the inventor's mind that only ordinary skill would be necessary to reduce the invention to practice, without extensive research or experimentation." *Stern v. Trustees of Columbia University in City of New York*, 434 F.3d 1375, 1378 (Fed. Cir. 2006) (internal quotations omitted). An idea is sufficiently definite for conception "when the inventor has a specific, settled idea, a particular solution to the problem at hand, not just a general goal or research plan he hopes to pursue." *Invitrogen Corp. v. Clontech Labs., Inc.*, 429 F.3d 1052, 1072-73 (Fed. Cir. 2005). If an inventor's oral testimony is relied upon for conception, the testimony must be corroborated by "evidence which shows that the inventor disclosed to others his completed thought expressed in such clear terms as to enable those skilled in the art to make the invention." *Coleman v. Dines*, 754 F.2d 353, 359 (Fed. Cir. 1985) (internal quotations omitted).

a) The '977 Patent

The '977 patent is a continuation in part of Patent Application No. 08/586,758 ("the '758 application") which was filed on March 21, 1991 and issued as U.S. Patent No. 5,148,266 ("the '266 patent"). (*See* JX-00001.) Tessera argues that the asserted claims of the '977 patent are entitled to a conception date of no later than June 10, 1990. (CIB at 63.) Tessera argues that both Dr. Distefano and Dr. Bottoms testified that conception of a face-up chip assembly having all of the claimed elements occurred sometime in early June, 1990. (*Id.* at 64.) Tessera argues that Dr. Khandros' June 1, 1990 and June 10, 1990 notebook entries, among other entries, corroborate Distefano's and Bottom's testimony regarding conception of a face-up chip assembly having all the claimed elements. Tessera argues that Dr. Distefano and Dr. Khandros validated the notebook entries by having the notebook entries written by one person and witnessed by another person. (*Id.*) It is Tessera's burden to prove the priority date of its inventions. *Coleman*, 754 F.2d. at 359.

Respondents do not discuss the priority date of the '977 patent. (*See* RIB at 107-114; RRB at 40-43.)

The Staff does not dispute Tessera's asserted June 1, 1990 conception date. (SIB at 38.)

The record evidence shows that in the early days of Tessera (formally IST), particularly during 1990, Khandros and Distefano memorialized their technical data in engineering notebooks. (Distefano, Tr. at 160:13-21.) The purpose of the engineering notebooks was to record their inventive efforts. (Distefano, Tr. at 160:22-161:3; Bottoms, Tr. at 242:21-243:9.) To validate the engineering notebook entries, Distefano and Khadros had a discipline of having the notebook entries written by one person and witnessed by another person. (Distefano, Tr. at 160:13-21; Bottoms, Tr. at 242:21-243:9.) Consistent with his role, Dr. Khandros acted as the

scribe for the notebook entries. (Distefano, Tr. 160:22-161:7.) Exhibit CX-6822C is a copy of the notebook that documents the work of Distefano and Khandros during the first few years at Tessera. (Distefano, Tr. at 161:14-162:15, 163:1-4; Bottoms, Tr. 243:24-248:8.)

Inventor Distefano testified that he and inventor Khandros conceived of an idea to decouple the expansion of the circuit board from the expansion of the chip, to allow the circuit board to expand and move without inducing stress on the circuit board, chip or the connection between the two. (Distefano, Tr. at 156:8-13.) Dr. Distefano testified that decoupling the circuit board from the chip allowed the circuit board to move, and the connection between the circuit board and the chip to move. (Distefano, Tr. at 156:17-23.) According to Distefano, instead of taking up the strain in the solder balls, their solution transferred the strain in the solder ball inside the package, so the package itself deformed. (Distefano, Tr. at 160:4-12.) Distefano testified that this greatly increased reliability because with the decoupling, the stress on the solder connection is greatly reduced and the stress on the chip is reduced, so that failures due to solder cracking or chip cracking were reduced. (Distefano, Tr. at 156:24-157:7.)

Distefano's testimony is corroborated by Dr. Bottoms, who is not an inventor on either of the patents in suit. Dr. Bottoms was actively involved in the startup of Tessera (formally IST). (Bottoms, Tr. at 235:16-23.) Dr. Bottoms began regularly meeting with Distefano and Khandros "Face-to-face about once a month. On the phone, much more often." (Bottoms, Tr. at 236:3-237:8, 240:3-8.) Dr. Bottoms testified that he was aware of the semiconductor chip packaging issues on which Distefano and Khandros were working. (Bottoms, Tr. at 237:4-17.) According to the evidence, Bottoms would review the lab notebook every time he visited IST to catch up on what had occurred at IST since his last visit. (Bottoms, Tr. at 243:10-23.) Bottoms testified that in the May-June 1990 time frame, Di Stefano and Khandros were working on a solution to the

thermal mismatch problem between the semiconductor chip and the substrate on which it was mounted. (Bottoms, Tr. at 237:18-20, 238:24-239:8, 240:21-241:2.) Specifically, Bottoms testified that Distefano and Khandros's solution required the insertion of a flexible interposer element between the circuit board that has a high thermal expansion coefficient, and the silicon, that has a low thermal expansion coefficient, so that they could move with respect to one another without any damage. (Bottoms, Tr. at 240:9-20.) Bottoms also testified that during the May-June 1990 time frame he had discussions with Distefano and Khandros regarding a face-up embodiment that addressed the thermal mismatch problem that Distefano and Khandros were working on. (Bottoms, Tr. at 241:3-16.) In fact, Bottoms testified that around June 1990 he was shown a model of what IST was intending to build and that model had the semiconductor chip in a face-up orientation. (Bottoms, Tr. at 241:17- 242:3.)

Distefano's and Bottom's testimony is further corroborated by the entries in IST's engineering notebook.

The disclosure of the face-up configuration in this entry corroborates the testimony of Distefano and Bottoms that the inventors were considering face-up configurations in June of 1990.

Based on the evidence detailed above, including the testimony of Dr. Distefano and Dr. Bottoms, and the entries in the IST notebook, the ALJ finds that as of June 1990 inventors

Distefano and Khandros had conceived of the inventions embodied in the asserted claims of the '977 patent such that only ordinary skill would be necessary to reduce the invention to practice. *Stern v. Trustees of Columbia University in City of New York*, 434 F.3d 1375, 1378 (Fed. Cir. 2006) ("[c]onception is complete when the idea is so clearly defined in the inventor's mind that only ordinary skill would be necessary to reduce the invention to practice, without extensive research or experimentation." (internal quotations omitted)). Accordingly, the ALJ finds that the inventions claimed in the asserted claims of the '977 patent is entitled to a date of conception of no later than June 1990.

b) '627 Patent

The '627 patent claims priority to Patent Application No. 673,020 ("the '020 application") which was filed on March 21, 1991 and issued as U.S. Patent No. 5,148,265. (*See* JX-2.) Tessera argues that the asserted claims of the '627 patent are entitled to a conception date of no later than November 21, 1990. (CIB at 63.) It is Tessera's burden to prove the priority date of its inventions. *Coleman*, 754 F.2d. at 359.

Respondents do not discuss the priority date of the '627 patent. (*See* RIB at 107-114; RRB at 40-43.)

The Staff also does not discuss the priority date of the '627 patent. (*See* SIB at 70-72.)

Distefano testified that the inventions claimed in the asserted claims of the '627 patent were conceived no later than November 21, 1990. (Distefano, Tr. 156:7-172:4.) Distefano's testimony is corroborated by a written communication sent by Dr. Khandros on November 21, 1990, to IST's patent attorney, Marcus Millet. (*See* Distefano, Tr. 168:6-169:24; CX-1908C at 1.) According to the record evidence, the fax included a few extra drawings and extensions of the concept of a compliant package. (*Id.*) The evidence shows that the drawings were intended to

be, and in fact actually were, included in the patent application that Millet was drafting for IST. (Distefano, Tr. 169:4-18.) Dr. Distefano testified that the drawings attached to the November 21, 1990 fax show "various configurations of that chip package that decouples the stress or decouples the motion of the terminal in the package from the chip." (Distefano, Tr. 169:14-24.) In particular, the Figure on page 3 of the fax depicts a face-down, center-bonded chip package with a package substrate having a central hole, or window, through which the central bond wires connecting the terminals and chip's central contacts pass. (CX-1908C at 3; Distefano, Tr. 169:25-171:21.) According to Distefano, the terminals in the face-down, center-bonded chip package depicted on page 3 of the fax are able to decouple from the chip's contacts in response to external thermal stresses via a compliant layer. (Distefano, Tr. 169:25-172:4.)

Based on the evidence detailed above, including the testimony of Dr. Distefano and Dr. Bottoms, the entries in the IST notebook, and the fax communication sent from Khandros to Millet, the ALJ finds that as of November 1990 inventors Distefano and Khandros had conceived of the inventions embodied in the asserted claims of the '627 patent such that only ordinary skill would be necessary to reduce the invention to practice.

2. Reduction to Practice

The evidence shows that continuing from June 1990, inventors Distefano and Khandros acted with due diligence in reducing their conceived inventions to practice, culminating with the filing of the '265 patent application on March 21, 1991. In particular, the evidence shows that from June 1990, to the March 1991 filing date of the '265 patent, the inventors were either busy obtaining the equipment and materials necessary to build working prototypes that would implement their inventions or actually building the prototypes themselves. (*See* Distefano, Tr. at 174:18-25, 175:10-14, 176:2-18, 177:9-178:3, 178:15-179:3; Bottoms, Tr. at 242:2-20; CX-

191OC (invoices documenting material and equipment purchases by IST in the 1990-1991 time frame); CX-1911C (photographs of vintage chip packages made by IST during their early years).) The ALJ finds based on the above cited evidence of record that the inventors of the asserted '977 and '627 patents acted with due diligence in reducing their intentions to practice.

Having determined above that inventors Distefano and Khandros conceived of the inventions embodied in the asserted claims of the '977 patent in June 1990 and thereafter diligently reduced their invention to practice, the ALJ finds based on the record evidence discussed above that the '977 patent is entitled to a priority date of no later than June 10, 1990. Likewise, having found that that inventors Distefano and Khandros conceived of the inventions embodied in the asserted claims of the '627 patent in June 1990 and thereafter diligently reduced their invention to practice, the ALJ finds based on the record evidence discussed above that the '627 patent is entitled to a priority date of no later than November 21, 1990.

C. Anticipation

A patent may be found invalid as anticipated under 35 U.S.C. § 102(a) if "the invention was known or used by others in this country, or patented or described in a printed publication in this country, or patented or described in a printed publication in a foreign country, before the invention thereof by the applicant for patent." 35 U.S.C. § 102(a). A patent may be found invalid as anticipated under 35 U.S.C. § 102(b) if "the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States." 35 U.S.C. § 102(b). Under 35 U.S.C. § 102(e), a patent is invalid as anticipated if "the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent." 35 U.S.C. § 102(e). Anticipation is a

question of fact. *Texas Instruments, Inc. v. U.S. Int'l Trade Comm'n*, 988 F.2d 1165, 1177 (Fed. Cir. 1993) ("*Texas Instruments II*"). Anticipation is a two-step inquiry: first, the claims of the asserted patent must be properly construed, and then the construed claims must be compared to the alleged prior art reference. *See, e.g., Medichem, S.A. v. Rolabo, S.L.*, 353 F.3d 928, 933 (Fed. Cir. 2003). It is axiomatic that claims are construed the same way for both invalidity and infringement. *W.L. Gore v. Garlock, Inc.,* 842 F.2d 1275, 1279 (Fed. Cir. 2008.)

"Claimed subject matter is 'anticipated' when it is not new; that is, when it was previously known. Invalidation on this ground requires that *every element and limitation* of the claim was *previously described in a single prior art reference*, either *expressly or inherently*, so as to place a person of ordinary skill in possession of the invention." *Sanofi-Synthelabo v. Apotex, Inc.*, 550 F.3d 1075, 1082 (Fed. Cir. 2008) (emphasis added) (citing *Schering Corp. v. Geneva Pharms., Inc.*, 339 F.3d 1373, 1379 (Fed. Cir. 2003) and *Continental Can Co. USA v. Monsanto Co.*, 948 F.2d 1264, 1267-69 (Fed. Cir. 1991)).

To anticipate, a single prior art reference must be enabling and it must describe the claimed invention, *i.e.*, a person of ordinary skill in the field of the invention must be able to practice the subject matter of the patent based on the prior art reference without undue experimentation. *Sanofi*, 550 F.3d at 1082. The presence in said reference of *both* a specific description and enablement of the subject matter at issue are required. *Id.* at 1083.

To anticipate, a prior art reference also must disclose all elements of the claim within the four corners of said reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) ("*NMI*"); *see also Abbott Labs. v. Sandoz, Inc.*, 544 F.3d 1341, 1345 (Fed. Cir. 2007) (stating, "Anticipation is established by documentary evidence, and requires that every claim element and limitation is set forth in a single prior art reference, in the same form and order as in

the claim."). Further, "[b]ecause the hallmark of anticipation is prior invention, the prior art reference--in order to anticipate under 35 U.S.C. § 102--must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements 'arranged as in the claim.'" *Id.* (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). The Federal Circuit explained this requirement as follows:

> The meaning of the expression 'arranged as in the claim' is readily understood in relation to claims drawn to things such as ingredients mixed in some claimed order. In such instances, a reference that discloses all of the claimed ingredients, but not in the order claimed, would not anticipate, because the reference would be missing any disclosure of the limitations of the claimed invention 'arranged as in the claim.' But the 'arranged as in the claim' requirement is not limited to such a narrow set of 'order of limitations' claims. Rather, *our precedent informs that the 'arranged as in the claim' requirement applies to all claims and refers to the need for an anticipatory reference to show all of the limitations of the claims arranged or combined in the same way as recited in the claims, not merely in a particular order.* The test is thus more accurately understood to mean 'arranged or combined in the same way as in the claim.'

Id. at 1370 (emphasis added). Therefore, it is not enough for anticipation that a prior art reference simply contains all of the separate elements of the claimed invention. *Id.* at 1370-71 (stating that "*it is not enough [for anticipation] that the prior art reference discloses part of the claimed invention, which an ordinary artisan might supplement to make the whole*, or that it includes multiple, distinct teachings that the artisan might somehow combine to achieve the claimed invention." (emphasis added)). Those elements must be arranged or combined in said reference in the same way as they are in the patent claim.

If a prior art reference does not expressly set forth a particular claim element, it still may anticipate the claim if the missing element is inherently disclosed by said reference. *Trintec Indus., Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 1295 (Fed. Cir. 2002); *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Inherent anticipation occurs when "the missing descriptive

material is 'necessarily present,' not merely probably or possibly present, in the prior art." *(Id.)*; *see also Rhino Assocs. v. Berg Mfg. & Sales Corp.*, 482 F. Supp.2d 537, 551 (M.D. Pa. 2007). In other words, inherency may not be established by probabilities or possibilities. *See Continental Can*, 948 F.2d at 1268. Thus, "[t]he mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Id.*

The critical question for inherent anticipation here is whether, as a matter of fact, practicing an alleged prior art reference necessarily features or results in each and every limitation of the asserted claim at issue. *See, e.g., Toro Co. v. Deere & Co.*, 355 F.3d 1313, 1320 (Fed. Cir. 2004).

If there are "slight differences" between separate elements disclosed in a prior art reference and the claimed invention, those differences "invoke the question of obviousness, not anticipation." *NMI*, 545 F.3d at 1071; *see also Trintec*, 295 F.3d at 1296 (finding no anticipation and stating that "the difference between a printer and a photocopier may be minimal and obvious to those of skill in this art. Nevertheless, obviousness is not inherent anticipation."). Statements such as "one of ordinary skill may, in reliance on the prior art, complete the work required for the invention," and that "it is sufficient for an anticipation if the general aspects are the same and the differences in minor matters is only such as would suggest itself to one of ordinary skill in the art," *actually relate to obviousness*, not anticipation. *Connell*, 722 F.2d at 1548; *see infra*.

1. The '106 Patent

a) Juskey '759

Respondents argue that U.S. Patent No. 5,218,759 ("Juskey '759") is prior art under 35 U.S.C. § 102(b) and that it discloses every limitation of the asserted claims of the '106 Patent. (RIB at 68.) The parties disagree that Juskey '759 discloses certain limitations of the asserted

claims, namely (1) exposed terminals; (2) a protective barrier in contact with the top layer; (3) a top layer and (4) a compliant layer. (RIB at 68-70; CIB at 88-91; SIB at 87-88.)

Respondents argue that the "array of exposed terminals" in the Juskey '759 is the "array of pads" mounted on the semiconductor substrate and the "top layer" is the carrier substrate of the semiconductor; the temporary support substrate in combination with the adhesive acts as the "protective barrier"; and that any material used to mount the chip to the substrate would be a "compliant layer" since any material will satisfy Tessera's construction of "compliant layer," which is any material that "yield[s] to an applied force." (RIB at 68-70.) Tessera argues that Juskey '759 does not teach an "array of exposed terminals" before encapsulation as taught by the '106 Patent, but instead Juskey '759 teaches "exposed terminals" after encapsulation. (CIB at 88-89.) Tessera further argues that Juskey '759 fails to teach a "top layer" as it is "disposed ***downward*** of the active surface of the die"; that the "protective barrier" is not in contact with the top layer because of the layer of adhesive; and that Juskey '759 fails to teach a "compliant layer" because it is not clear what method or material would be used to attach the die. (CIB at 89-91) (emphasis in original).

The ALJ finds that Respondents have failed to show by clear and convincing evidence that Juskey '759 discloses each and every limitation of the asserted claims of the '106 Patent. While the array of pads taught in Juskey '759 may be exposed prior to encapsulation, the evidence is insufficient to establish clearly and convincingly that the array of pads is, in fact, an "array of exposed terminals" as disclosed by the '106 Patent. (RX-912 (Juskey '759 Patent); CX-07350C (Goosey RWS) at Q. 74-75.) Respondents argue that because Jusky '759 discusses preventing substrate contamination, one of ordinary skill in the art would understand this to mean that the terminals are necessarily exposed prior to encapsulation. (RRB at 33.)

While the presence of such a disclosure establishes the probability or possibility that "array of pads" are exposed, it does not follow that such a disclosure inherently discloses "exposed terminals" to satisfy this limitation of the asserted claims. *See Cont'l Can Co. v. Monsanto Co.*, 948 F.2d 1264, and 1268-69 (Fed. Cir. 1991); *Finnigan*, 180 F.2d at 1365 ("Inherency may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient."). Such a disclosure fails to rise to clear and convincing evidence that the Jursky '759 discloses or teaches "exposed terminals." This is especially true because Jusky '759 actually teaches means of covering the terminals with adhesive rather then keeping them exposed during encapsulation. (RX-912 (Juskey '759 Patent) at 2:45-49, 3:1-12, 3:36-38; CX-07350C (Goosey RWS) at Q. 64-65, 82, 85-86; Goosey, Tr. 3335:9-3336:3.)

In addition, Respondents have argued that the "protective barrier" is the temporary support substrate in combination with the adhesive. However, such a combination contradicts the evidence because the Juskey '759 makes clear that the temporary support substrate and the adhesive used to attach the temporary support substrate are two separate and distinct things. (RX-912 (Juskey '759 Patent) at 2:33-35, 2:45-49; CX-07350C (Goosey RWS) at Q. 64-65, 99-100.) Thus, the temporary support substrate, the "protective barrier," is not "in contact" with the top layer because the adhesive used to attach the temporary support barrier prevents contact between the two. At a minimum, Juskey '759 fails to disclose "an array of exposed terminals" and "a protective barrier in contact with the top layer."[9]

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[9] As for whether Juskey '759 discloses a "top layer" or a "compliant layer," Respondents' and Tessera's arguments focus on whether Juskey '759 has a "top layer" that satisfies Tessera's proposed claim construction of being "a layer upward of the active surface of the chip." (RIB at 70; CIB at 89-90.) However, under the ALJ's claim construction, the term "top layer" does not require an orientational frame of reference. (*See supra* at Section III.C.1.a.(1).)

Therefore, the ALJ finds that the Respondents have failed to show by clear and convincing evidence that the Juskey '759 discloses each and every limitation of the asserted claims.

b) Worp '366

Respondents argue that U.S. Patent No. 5,136,366 (Worp '366) is prior art under art under 35 U.S.C. § 102(b) and that it discloses every limitation of the asserted claims of the '106 Patent. (RIB at 71.) The parties disagree that Worp '366 discloses (1) a protective barrier in contact with the top layer; (2) a top layer; and (3) a compliant layer. (RIB at 71-73; CIB at 91-93; SIB at 88-89.)

Respondents argue that Worp '366 discloses a "protective barrier in contact with said top layer" because it teaches using a lower mold that "presses up against the bottom surface of the substrate [that carries the pads] to shape and constrain where mold compound can flow, protecting the terminals from contamination." (RIB at 71.) In other words, Respondents assert that the lower mold is the "protective barrier" that comes "into contact" with the bottom surface of the substrate that carries the terminals, which is the "top layer."

Tessera argues that the lower mold does not come into contact with the substrate because of the presence of the conductors. (CIB at 92.) Tessera asserts that during encapsulation, the conductors would create a small gap between the lower mold and the substrate which would allow encapsulant to wick across the substrate and contact the conductors. (CIB at 92.)

The ALJ finds that Respondents have failed to show by clear and convincing evidence that the Worp '366 discloses each and every limitation of the '106 Patent. While the Worp '366 does disclose transfer molding and the use of mold tools in its specification (RX-5C (Corrected Sinnadurai DWS and Errata) Q. 308; RX-916 (Worp '366) at 1:17-65; 3:20-4:66; Goosey, Tr.

3297:1-4.), Worp '366 fails to disclose or teach the shape of the lower mold, how it is configured, how they work or how they come together such that one could determine whether and/or how the lower mold is fitted to the substrate and whether it actually comes into contact with the "top layer." (RX-916 (Worp '366 Patent); CX-07350C (Goosey RWS) at Q. 59, 60, 61, 127; Sinnadurai, Tr. 2375:6-2376:24; Goosey, Tr. 3301:15-19, 3336:4-12, CX-01716 ('688 Patent) at Figs. 3b, 4.) Respondents fail to cite any disclosure in the Worp '366 that would support their contention, except for the extensive analysis performed by Dr. Sinnudurai. While the evidence shows that there is a strong possibility that the lower mold cavity may come into contact with the substrate,[10] such a possibility and likelihood does not rise to the heavy burden of proving such an occurrence by clear and convincing evidence.

Therefore, the ALJ finds that the Worp '366 fails to disclose a "protective barrier in contact with said top layer" and fails to anticipate the '106 Patent.

c) Ohi '452

Respondents argue that Japanese Publication No. 1992-84452 ("Ohi '452") is prior art under art under 35 U.S.C. § 102(b) and that it discloses every limitation of the asserted claims of the '106 Patent. (RIB at 74.) The parties disagree that Ohi '452 discloses (1) a top layer; (2) exposed terminals; and (3) a protective barrier. (RIB at 73-78; CIB at 95-98; SIB at 90-91.)

Respondents argue that Ohi '452 discloses a pin grid array (PGA) package and a pad array carrier (PAC) package that has a "top layer," which is the resin substrate upon which the terminals are located; has "exposed terminals," which are the contact pins protruding from the

[10] As for Tessera's argument that the lower mold would be created such that it would allow encapsulation material to contaminate the terminals, the ALJ finds such an argument unpersuasive. (*See* CIB at 91-93.) As Tessera's own expert, Dr. Goosey, stated, engineers engaged in transfer molding would design the mold and take into consideration the need to prevent encapsulation material from contacting the exposed terminals. (CX-06482C (Goosey DWS) at Q. 127, 184, 237, 288; 237.)

resin substrate; and has a "protective barrier" that protects the terminals on the top layer, which is the frame pattern in the PGA embodiment and the solder mask in the PAC embodiment. (RIB at 74-78.)

Tessera argues that Ohi '452 fails to disclose a "protective barrier" because the frame pattern is part of the package substrate and not distinct from the top layer and that, even if it were considered distinct, fails to protect the terminals by itself. (CIB at 96-97.) Tessera further argues that the pins are not the "exposed terminals" because the pin is not part of the package and provide the second level interconnect, but rather the terminals are either the plated through holes in which the pins are inserted or the metal pads on the top side of the package to which the individual die contacts are connected and to which the pins abut. (CIB at 96.)

The ALJ finds that Respondents have failed to show by clear and convincing evidence that the Ohi '452 discloses each and every limitation of the '106 Patent. Specifically, the ALJ finds that Ohi '452 fails to disclose "exposed terminals" as required by the '106 Patent. As set forth above, the ALJ has construed "terminals" to mean "an endpoint for electrical and mechanical connection of the chip package to the outside." The pins are not the "endpoint" but rather the means of mechanically and electrically connecting the endpoint to the outside, *i.e.*, the second level interconnect. Indeed, this is supported by the intrinsic evidence wherein the '265 Patent states that "the pins would serve as a means for connecting terminals 48 to the contact pads of the substrate." ('265 patent 12:31-32.) As such, the "terminals" are either the (1) plated through holds in which the pins are inserted or (2) the metal pads on the top side of the package substrate to which individual die contacts are connected and against with the pins abut. (RX-915 at Figs 9-12, 13-15; CX-07350C (Goosey RWS) at Q&A 177-178, 181.) If the terminals are the plated through holes, then they are not "exposed." (RX-915 at Figs 9-12, 13-15; CX-07350C

(Goosey RWS) at Q&A 178, 181.) If the terminals are the metal pads, then they would be directly encased in encapsulation material. (RX-915 at Figs 9-12, 13-15; CX-07350C (Goosey RWS) at Q&A 178, 181.) Thus, Ohi '452 fails to satisfy the "exposed terminals" limitation of the '106 Patent.

Therefore, the ALJ finds that the Respondents have failed to show by clear and convincing evidence that the Ohi'452 discloses each and every limitation of the asserted claims.

d) Chia '349

Respondents argue that U.S. Patent No. 4,868,349 ("Chia '349") is prior art under art under 35 U.S.C. § 102(b) and that it discloses every limitation of the asserted claims of the '106 Patent, except for claim 34. (RIB at 79.) The parties disagree that Chia '349 discloses (1) exposed terminals and (2) a top layer that is a spaced distance above said semiconductor chip. (RIB at 79-80; CIB at 95-98; SIB at 89-90.)

Respondents argue that discloses a method of transfer molding pin grid array package with "exposed terminals," which are the package pins since they extend from the surface of the substrate and serve as the endpoints to connect the pin grid array package to the printed circuit board. (RIB at 78.) Respondent further argue that Chia '329 discloses a "top layer" that is "a spaced distance above said semiconductor chip," because the chip is located in the well formed in the substrate and bonded to the well, then it is a defined distance from the substrate ("top layer"). (RIB at 78-79.)

Tessera argues that Chia '349 is directed to resolving heat transfer problems in a pin grid array package and is not directed at the problem solved by the '106 Patent. Specifically, Tessera argues that Chia '349 is cumulative of prior art already considered by the patent examiner and did not prevent the examiner from allowing the '106 Patent to issue. Tessera further argues that

Chia '349 fails to disclose "exposed terminals" because the terminals, the plated holes, are not exposed since the pins are inserted into the plated holes prior to encapsulation. (RIB at 94.) Chia '349 further fails to disclose a "spaced distance above said semiconductor chip" because the package substrate is to the side of the semiconductor chip and not "orthogonal and away from the chip top surface."

The ALJ finds that Respondents have failed to show by clear and convincing evidence that Chia '349 discloses each and every limitation of the '106 Patent. Specifically, the ALJ finds that Chia '349 fails to disclose "exposed terminals" as required by the '106 Patent. As set forth above, the ALJ has construed "terminals" to mean "an endpoint for electrical and mechanical connection of the chip package to the outside." The pins are not the "endpoint" but rather the means of mechanically and electrically connecting the endpoint to the outside, *i.e.*, the second level interconnect. Indeed, this is supported by the intrinsic evidence wherein the '265 Patent states that "the pins would serve as a means for connecting terminals 48 to the contact pads of the substrate." ('265 patent 12:31-32.) As such, the "terminals" are the plated through holds in which the pins are inserted and are not "exposed." (RX-917 at Fig 2; CX-07350C (Goosey RWS at Q. 150-154; Sinnadurai, Tr. 2308:8-13, 2309:2-2310:6, 2312:2-9.) Thus, Chia '349 fails to satisfy the "exposed terminals" limitation of the '106 Patent.

The ALJ further finds that Chia '349 fails to disclose a "top layer" that is "a spaced distance above said semiconductor chip." As the ALJ set forth above, the "top layer" is the "outer layer of the chip assembly upon which the terminals are fixed." Here, the "top layer" is the package substrate, which is the outer layer of the chip assembly upon which the terminals are fixed. (RX-917 2:57-61, Figs. 1, 2 and 5; CX-07350C (Goosey RWS) at Q. 158.) As shown in

Chia '349, the package substrate (11) is next to the chip (20) and not "a spaced distance" above it. (RX-917 at Fig. 2; 2:57-3:13).

Therefore, the ALJ finds that the Respondents have failed to show by clear and convincing evidence that Chia '349 discloses each and every limitation of the asserted claims.

2. The '627 and '977 Patents

a) The 1989 68HC11 OMPAC

Respondents argue that the 1989 68HC11 OMPAC chip package ("OMPAC") anticipates claims 17 and 18 of the '977 patent under 35 U.S.C. §102(b). Respondents assert that OMPAC anticipates because it was on sale more than one year before the priority date of the asserted patents. (RIB at 107.) Specifically, Respondents argue that in July 1989 Citizen Watch offered to make and sell OMPAC packages. Respondents argue that the OMPAC packages were then assembled and delivered to Motorola in the United States in September 1989. (*Id.* at 107.) Respondents assert that both the commercial offer for sale in July 1989 and the actual sale in September 1989 were at least one year before the March 21, 1991 priority date asserted by Tessera. (*Id.*) Respondents also assert that the fabrication of the OMPAC packages in September 1989 constitutes a reduction to practice. (*Id.*)

Tessera and the Staff contest Respondents' argument that the '977 patent is anticipated by OMPAC. Tessera and the Staff contend that there was no commercial offer for sale between two separate entities and that, at that time, the OMPAC packages were not ready for patenting. Tessera and the Staff also argue that Respondents have not established that the OMPAC packages practice the asserted claims of the '977 patent.

35 U.S.C. §102(b) prohibits an invention from being patented if it was on sale in the United States more than one year prior to the filing date of the application. 35 U.S.C. § 102(b).

To qualify as prior art under §102 (b), the alleged on-sale product: (1) must have been the subject of a commercial offer for sale more than one year before the critical date of the asserted patents; and (2) must have been ready for patenting. *Pfaff v. Wells Elecs.*, 525 U.S. 55, 66-67 (1998). The ALJ has found herein that the asserted claims of the '977 patent are entitled to a June 10, 1990 date of invention. *See*, *supra*, at V.B.2. Therefore, the alleged July 1989 offer by Citizen Watch to make and sell OMPAC packages for Motorola was not more than one year prior to the June 1990 date accorded the '977 patent. Accordingly, the alleged July 1989 offer for sale of OMPAC packages from Citizen Watch to Motorola does not qualify as prior art under 35 U.S.C. §102(b) and thus cannot invalidate the asserted claims of the '977 patent.

Even if the '977 patent has a date of invention that is later than June 1990, the evidence still does not clearly and convincingly show that the OMPAC packages were ever "on-sale" within the meaning of 102(b). Specifically, the evidence shows that Motorola contacted Citizen Watch in Japan about producing "engineering samples" or "prototypes" of a package with characteristics that were specified by Motorola. (CX-7349C (Ivey, Direct) Q. 255; Freyman, Tr. 1669:16-25, 1676:13-15, 1678:8-13.) Additionally, Freyman testified that Citizen Watch was subject to a confidentiality agreement with Motorola. (CX-07355C (Urbish, Direct) Q. 38; Freyman, Tr. 1670:l-11.) Pursuant to that agreement, Citizen Watch could not have sold the engineering samples to any other company, or otherwise have disclosed any information regarding the 1989 OMPAC 68-pin package to any entity but Motorola. (*Id.*)

As detailed above, the subcontract agreement between Motorola and Citizen Watch was subject to a confidentiality agreement that prevented Citizen from disclosing or selling the OMPAC to any entity other than Motorola. Confidentiality obligations are a factor in determining whether the on sale bar should apply. *See Netscape Communs. Corp. v. Konrad*,

295 F.3d 1315, 1320-1321 (Fed. Cir. 2002). Additionally, the evidence shows that the 200 prototypes were for Motorola's experimental use. *See* Freyman, Tr. 1676:13-15; *see also Atlanta Attachment Co. v. Leggett & Platt, Inc.*, 516 F.3d 1361, 1365 (Fed. Cir. 2008) ("While [a]ny attempt to use [an invention] for profit ... would deprive the inventor of his right to a patent, an inventor's use by way of experiment does not bar patentability. Therefore, we must consider whether the suspect activities were experiments as opposed to an attempt to profit from the invention, that is, whether the primary purpose of the offers and sales was to conduct experimentation") (internal quotations and citations omitted); *Manville Sales Corp. v. Paramount Sys., Inc.*, 917 F.2d 544, 550 (Fed.Cir.1990) ("a sale that is primarily for experimental purposes, as opposed to commercial exploitation, does not raise an on sale bar"); *U.S. Envt'l Prods., Inc. v. Westall*, 911 F.2d 713, 716 (Fed.Cir.1990) ("[a] section 102(b) bar is avoided if the primary purpose of the sale was experimental"). Accordingly, the ALJ finds Citizen Watch's production and sale of 200 OMPAC prototypes for Motorola's consumption in 1989 was not a "commercial sale" that would trigger the on-sale bar of 35 U.S.C. § 102 (b). Moreover, the ALJ finds that Respondents have failed to prove clearly and convincingly that the OMPAC meets all the limitations of the '977 patent. Accordingly, the ALJ finds that the OMPAC does not anticipate the '977 patent under 35 U.S.C. § 102(b).

b) The Hsia Patent

Respondents argue that U.S. Patent No. 4,932,883 ("Hsia") anticipates the '977 patent under 35 U.S.C. § 102(b). (RIB at 110-111.) Respondents assert that Hsia discloses a semiconductor assembly that includes a semiconductor chip having contacts on its front surface. (*Id.* at 111.) Additionally, respondents argue that the contacts on the chip are connected to the terminals in Hsia by thin flexible, conductive leads. (*Id.*) Also, respondents argue that the

terminals overly both surfaces of the semiconductor chip. (*Id.*) Further, respondents assert that the terminals are supported above the chip by an elastomeric material, which "functions to deform and provide a requisite reactionary force for contacting the" contacts on the chip surface. *Id.* Thus, according to respondents, because Hsia discloses structures that necessarily give rise to the movable limitation, the claim element is met. (*Id.*)

Tessera argues that the Hsia '883 reference does not include a compliant layer "between said terminals and said chip," as required by both asserted claims of the '977 Patent. (CRB at 13-14.) Tessera also argues that Respondents fail to offer even one proposed finding that Hsia discloses terminals under Respondents' claim construction of "an end point for the electrical connection of the package to the outside." (*Id.* at 14.)

The Staff argues that Tessera's expert, Prof. Ivey, described Hsia '883 as directed to a flip-chip on board configuration, and not to a conventional semiconductor chip package, where an elastomeric connector is used to attach flip-chips to a ceramic substrate. (SIB at 41.) The Staff adopts Prof. Ivey's opinion that the flip-chip configuration of Hsia does not have terminals as the term has been properly construed; thus there are no terminals that will displace relative to the chip. (*Id.*)

The Hsia '883 patent was issued on June 12, 1990 on an application filed July 20, 1989. (RX-237 at 1.) The '883 Patent names Liang-Choo Hsia, Thomas P. McAndrew, and Fred E. Steubner as the inventors. (*Id.*) The structure disclosed by the Hsia '883 Patent is a flip-chip on-board package, not a conventional package as contemplated by the asserted claims of the '977 and '627 patents. (CX-7349C (Ivey, Direct) Q. 743.) The only mention of CTE mismatch in the Hsia '883 Patent appears as part of the general background discussion of problems that have affected the semiconductor industry. (RX-237 at 1:24-47.) Additionally, the structure disclosed

in the Hsia '883 Patent contains no solder joint for which stress could be relieved. (*See* RX-237 at 12:40-42.) Both asserted claims of the '977 patent require a plurality of terminals, at least some of which overlie either a front surface or another surface of the chip. (*See* JX-1 at 35:63-36:19.) Additionally, the claims require that the terminals be movable with respect to the contacts of the chip. (*Id.* at 36:17-19, 36:30-31.) Under the construction of "terminals" used by Tessera and respondents, a terminal must be a point to connect "the package to the outside." (CX-7349C (Ivey, Direct) Q. 746; RX-1CA (Ulrich, Direct) Q. 111.) The structures disclosed in the Hsia '883 patent do not include "packages," but are instead attached directly to a ceramic substrate. (*See* RX-237 at 5:35-37, 6:35-39, 8:49-53, 12:40-42; CX-7349C (Ivey, Direct) QQ. 745-46.) If a device does not have a package, then it cannot possibly have a "terminal" as that term is used by Tessera and the Respondents, because without a package there can be no possible distinction between what is "inside" and "outside" of the non-existent package. (CX-7349C (Ivey, Direct) Q. 746.)

The asserted claims of the '977 patent also require that there be a layer of complaint material disposed between the terminals and the chip. (JX-1 at 36:14:15, 36:26-27.) Respondents identify elastomeric connector 10 in the Hsia '883 patent as the asserted "compliant material." (RX-1CA (Ulrich, Direct) Q. 197.) Even assuming that the elastomeric connector 10 is a compliant material as construed herein, the evidence shows that the Hsia '883 Patent does not disclose '"a layer of compliant material disposed between said terminals and said chip and supporting at least some of said terminals." (CX-7349C (Ivey, Direct) Q. 766-67.)

Accordingly, for the reasons discussed above, the ALJ finds that respondents have failed to prove by clear and convincing evidence that the asserted claims of the '977 patent are anticipated by the Hsia '883 patent.

c) Fukuda

Respondents argue that Japanese patent publication S61-137335 ("Fukuda") is anticipatory prior art to the '627 patent under 35 U.S.C. § 102(b). (RIB at 111-112.) According to Respondents, Fukuda discloses a "semiconductor device" having a flexible dielectric film 12 overlying a semiconductor chip 16. Respondents argue that the semiconductor chip 16 has inner electrodes 19 disposed towards the center of the front of the semiconductor chip 16. (*Id.* at 112.) Respondents also argue that the flexible dielectric film 12 has a bonding hole 13 that encompasses inner electrodes 19. (*Id.*) Additionally, respondents assert that Fukuda discloses that the semiconductor assembly includes cantilevered wiring leads 11, with the first portion of the leads disposed on the flexible dielectric film 12 for interconnection to a printed wiring board or substrate and overlying the front of the semiconductor chip 16 and a second portion of the leads that connects the inner electrodes 19 to the first portion of the leads. (*Id.*) Respondents contend that Fukuda further discloses that the flexible dielectric film 12 is made of "a polyimide, glass epoxy or the like." (*Id.*) Respondents argue that Fukuda teaches that the first portion of leads 11 are movable with respect to inner electrodes 19 of the semiconductor chip 16 so as to compensate for thermal expansion of the semiconductor chip 16. (*Id.*)

Tessera argues that the Fukuda reference does not anticipate the asserted claims of the '627 patent. According to Tessera, the Fukuda reference relates "solely to chip-on-board structures, and not the semiconductor packages at issue in the '627 Patent." (CIB at 17.) Tessera also argues that Respondents' mere recitation of the claim elements does not describe how the elements would interact in a manner so as to give rise to the claimed movement, and Respondents do not suggest how a person of ordinary skill would derive such a conclusion from unrelated teachings of the Fukuda Reference. (*Id.* at 18.)

The Staff also argues that Fukuda does not anticipate. Specifically, the Staff argues that Prof. Ivey explained in his witness statement that Fukuda does not disclose a chip package as claimed, but rather discloses a chip-on-board semiconductor structure. (SRB at 14.) The Staff argues that because it is a chip-on-board structure, there are no terminals as that word is properly construed. (*Id.*)

Japanese Patent Publication S55-42353 to Fukuda (the "Fukuda reference") appears to have a disclosure date of September 13, 1978. (RX-255 at 1.) The Fukuda reference discloses a structure in which a semiconductor chip is mounted face-down on a PCB by virtue of two layers of leads connection to each other: inner and outer electrodes 17 and 19, which connect to cantilevered wiring leads 11 and interconnect leads 14 running along the PCB. (See *Id.* at 2, Fig. 2; CX-7349C (Ivey, Direct) Q. 722.) According to the evidence, the Figures in the Fukuda reference depict a chip that is connected to a PCB extending past the chip to an unknown point. In the structure disclosed in the Fukuda reference, the evidence suggests that the long wiring leads 11 could connect to points outside the structure pictured in the Figures along the pictured composite substrate of rigid dielectric board 15 and flexible dielectric film 12. Thus, according to the credible testimony of Ivey, these Figures do not depict independent structures, but rather enlargements of points along a larger PCB. (RX-255 at Figs. 1-2; CX-7349C (Ivey, Direct) Q. 723.) Additionally, the Fukuda reference does not address the issue of differential thermal expansion or suggest a method of alleviating stresses caused by differential thermal expansion. (CX-7349C (Ivey, Direct) Q. 725; RX-255.) In fact, the Fukuda reference does not contain any teaching of the claimed movement or even of displacement of its elements. (CX-7349C (Ivey, Direct) Q. 730; RX-255.) Further, the evidence suggests that the rigid board 15 would prevent the wiring leads 11 from having any movement or displacement. (*Id.*)

Accordingly, for at least the reasons discussed above, the ALJ finds that respondents have failed to prove by clear and convincing evidence that the asserted claims of the '627 patent are anticipated by the Fukuda reference.

d) Sakamaki

Respondents argue that Japanese patent publication S61-137335 ("Sakamaki reference") is prior art to the '627 patent under 35 U.S.C. § 102(b). (RIB at 112.) According to Respondents, Sakamaki discloses "a semiconductor device that mounts a semiconductor element on a substrate." (*Id.*) In particular, respondents argue that Sakamaki teaches a semiconductor assembly having a flexible substrate 1 attached to the front of a semiconductor chip 4. (*Id.*) Respondents argue that the semiconductor chip 4 has wire bonding pads 6 disposed toward the center of the front of the semiconductor chip 4. (*Id.* at 113.) Respondents also argue that the flexible substrate 1 has a plurality of apertures 7 that encompass wire bonding pads 6. (*Id.*) Additionally, respondents argue that a plurality of wire bonding pads 3 are disposed on the flexible substrate 1. (*Id.*) Respondents also assert that Sakamaki discloses that the "film-like" flexible substrate 1 is made of a polyimide resin. (*Id.*) Respondents also argue that the semiconductor chip 4 is attached to the flexible substrate 1 using a suitable adhesive. (*Id.*) Respondents argue that the front of the semiconductor chip 4 also includes a passivation film 5. *Id.* Further, respondents argue that Sakamaki teaches that wire bonding pads 3 of the flexible substrate 1 are movable with respect to wire bonding pads 6 of the semiconductor chip 4 so as to compensate for thermal expansion of the semiconductor chip 4. (*Id.*)

Tessera argues that Sakamaki does not anticipate the asserted claims of the '627 patent. In particular, Tessera argues that because there is no package in the Sakamaki reference, there is no reference point from which terms such as "inside" or "outside" can have meaning. (CIB at 77;

CRB at 17.) According to Tessera, Sakamaki does not disclose "terminals," much less terminals with the claimed movement. (CIB at 77.) Tessera also argues that the Sakamaki reference never even mentions "thermal expansion of the semiconductor chip" much less any method of relieving stress from such expansion. (*Id.*) Further, Tessera argues that Sakamaki fails to disclose a compliant layer as that term is properly construed.

Staff also argues that Sakamaki does not anticipate. The Staff argues that Sakamaki does not disclose a semiconductor assembly as claimed because the semiconductor structure in Sakamaki is a chip-on-board semiconductor structure. (SRB at 15.) Further, the Staff argues that Sakamaki does not disclose terminals as properly construed. (*Id.*)

Japanese Laid-Open Patent Application JP 6-137335 to Sakamaki has a disclosure date of June 25, 1986, based on an application filed December 10, 1984. (RX-254 at 1.) The evidence suggests that the Sakamaki reference discloses a chip-on-board semiconductor structure, not a chip package as disclosed in the '627 patent. (RX-254 at 3, Fig. 1, Fig. 2; CX-7349C (Ivey, Direct) Q. 703.) In Figure 6 of the Sakamaki reference, conductor patterns 2, located in the top right comer of the Figure, do not connect to the depicted chip. (RX-254, Fig. 6.) A person of ordinary skill in the art would understand that because the leads go off to an unknown point, Figure 6 depicts an incomplete portion of a larger structure, not an independent package. (CX-7349C (Ivey, Direct) Q. 704; RX-254 at Fig. 6.) Under the construction of "terminals" used by Tessera and respondents, a terminal must be a point to connect "the package to the outside." Since the evidence suggests the Sakamaki reference does not disclose a package, it cannot disclose "terminals," or end-points of connection of a package to the outside. (CX-7349C (Ivey, Direct) Q. 707.) Thus, the evidence suggests that the Sakamaki reference does not disclose "a plurality of terminals disposed on said dielectric element for interconnection to a substrate and

overlying said chip front surface," as claimed in the '627 patent. (RX-254; JX-2 at 34:24-26; CX-7349C (Ivey, Direct) Q. 706, 708.) Moreover, the evidence suggests that the Sakamaki reference does not disclose any terminals that could be movable with respect to the central contacts on the chip so as to compensate for the thermal expansion of the chip. (CX-7349C (Ivey, Direct) Q. 709.)

Accordingly, for at least the reasons discussed above, the ALJ finds that respondents have failed to prove by clear and convincing evidence that the asserted claims of the '627 patent are anticipated by the Sakamaki reference.

e) Other Prior Art

Respondents also argue that each of the following prior art references anticipate or render obvious one or more of the asserted claims of the '977 and '627 patents. (RIB at 113-14.)

- Japanese Patent Publication 63-079335 ("Saito '335") anticipates claims 17 and 18 of the '977 patent under 35 U.S.C. § 102(b);
- Dohya Akihiro, et al., "Packaging Technology for the NEC SX-3/SX-X Supercomputer," Proceedings of the 40th Electronic Components & Technology Conference, pp. 525-533 ("Akihiro"), anticipates claims 17 and 18 of the '977 patent under 35 U.S.C. § 102(b) or 102(a);
- Japanese Patent Publication 1-155633 ("Yamada") anticipates claims 17 and 18 of the '977 patent under 35 U.S.C. § 102(b);
- U.S. Patent No. 4,989,069 ("Hawkins") invalidates claims 17 and 18 of the '977 patent under 35 U.S.C. § 102(a) or 102(e);
- U.S. Patent No. 4,954,878 ("Fox") anticipates claims 17 and 18 of the '977 patent and claims 1-4, 6, 9-12, 15, and 16 of the '627 patent under 35 U.S.C. § 102(a) or 102(b);

- Hinrichsmeyer, et al., "Solder-Filled Elastomeric Spacer," IBM Technical Disclosure Bulletin, vol. 27, No. 8, p. 4855 ("Hinrichsmeyer"), anticipates claims 17 and 18 under 35 U.S.C. § 102(b);

- U.S. Patent No. 5,014,161 ("Lee") anticipates claims 17 and 18 of the '977 patent under 35 U.S.C. § 102 (a) or 102(e);

- U.S. Patent No. 5,216,278 ("Lin") anticipates claims 17 and 18 under 35 U.S.C. § 102(e);

- U.S. Patent No. 4,700,276 ("Freyman") anticipates claims 17 and 18 of the '977 patent under 35 U.S.C. § 102(b); and

- Lea, "A Scientific Guide to Surface Mount Technology," published by Electrochemical Publications Limited ("Lea"), anticipates claims 17 and 18 of the '977 patent and claims 12, 15, and 16 of the '627 patent under 35 U.S.C. § 102(b).

Respondents provide no argument in their initial post-hearing brief as to why the above ten references either anticipate or render obvious the asserted claims of the '977 and '627 patents. Respondents only cite to their findings of fact. To the extent respondents included their anticipation and obviousness arguments within their findings of fact the ALJ finds such action impermissible because the findings of fact are to be confined to facts, not argument. Additionally, including arguments in the findings of fact would improperly circumvent the page limits imposed on the parties in this investigation. Moreover, Ground Rule 11.1 states that "[t]he post-trial brief shall discuss the issues and evidence tried within the framework of the general issues determined by the Commission's Notice of Investigation, the general outline of the briefs as set forth in **Appendix B**, and those issues that are included in the pre-trial brief and any permitted amendments thereto. All other issues shall be deemed waived." Respondents failure to

provide any argument regarding the above ten references is a violation of Ground Rule 11.1. Accordingly, the ALJ finds that respondents have waived any such arguments.

D. Obviousness

Included within the presumption of validity is a presumption of non-obviousness. *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 714 (Fed. Cir. 1984). Obviousness is grounded in 35 U.S.C. § 103, which provide, *inter alia*, that:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negative by the manner in which the invention was made.

35 U.S.C. § 103(a). Under 35 U.S.C. § 103(a), a patent is valid unless "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." 35 U.S.C. § 103(a). The ultimate question of obviousness is a question of law, but "it is well understood that there are factual issues underlying the ultimate obviousness decision." *Richardson-Vicks Inc.*, 122 F.3d at 1479; *Wang Lab., Inc. v. Toshiba Corp.*, 993 F.2d 858, 863 (Fed. Cir. 1993).

Once claims have been properly construed, "[t]he second step in an obviousness inquiry is to determine whether the claimed invention would have been obvious as a legal matter, based on underlying factual inquiries including: (1) the scope and content of the prior art, (2) the level of ordinary skill in the art, (3) the differences between the claimed invention and the prior art; and (4) secondary considerations of non-obviousness" (also known as "objective evidence"). *Smiths Indus. Med. Sys., Inc. v. Vital Signs, Inc.*, 183 F.3d 1347, 1354 (Fed. Cir. 1999), citing *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). The ultimate determination of whether an

invention would have been obvious is a legal conclusion based on underlying findings of fact. *In re Dembiczak*, 175 F.3d 994, 998 (Fed. Cir. 1999).

Obviousness may be based on any of the alleged prior art references or a combination of the same, and what a person of ordinary skill in the art would understand based on his knowledge and said references. If all of the elements of an invention are found, then:

> a proper analysis under § 103 requires, inter alia, consideration of two factors: (1) whether the prior art would have suggested to those of ordinary skill in the art that they should make the claimed composition or device, or carry out the claimed process; and (2) whether the prior art would also have revealed that in so making or carrying out, those of ordinary skill would have a reasonable expectation of success. *Both the suggestion and the reasonable expectation of success must be founded in the prior art, not in the applicant's disclosure.*

Velander v. Garner, 348 F.3d 1359, 1363 (Fed. Cir. 2003) (emphasis added) (internal citations omitted).

The critical inquiry in determining the differences between the claimed invention and the prior art is whether there is a reason to combine the prior art references. *See C.R. Bard v. M3 Sys.*, 157 F.3d 1340, 1352 (Fed. Cir. 1998). For example:

> *[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art*. Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, *it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered* and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.

KSR Int'l Co. v. Teleflex, Inc., 550 U.S. 398, 418-19 (2007) (emphasis added). The Federal Circuit case law previously required that, in order to prove obviousness, the patent challenger must demonstrate, by clear and convincing evidence, that there is a "teaching,

suggestion, or motivation to combine. The Supreme Court has rejected this "rigid approach" employed by the Federal Circuit in *KSR Int'l Co. v. Teleflex Inc.*, 500 U.S. 398 (2007), 127 S.Ct. 1727, 1739. The Supreme Court stated:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. Sakraida and Anderson's-Black Rock are illustrative–a court must ask whether the improvement is more than the predictable use of prior art elements according to their established function.
>
> Following these principles may be more difficult in other cases than it is here because the claimed subject matter may involve more than the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement. Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. To facilitate review, this analysis should be made explicitly. See *In re Kahn*, 441 F.3d 977, 988 (CA Fed. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusions of obviousness"). As our precedents make clear, however, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

[. . .]

> The obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents. The diversity of inventive pursuits and of modern technology counsels against limiting the analysis in this way. In many fields it may be that there is little discussion of obvious techniques or combinations, and it often may be the case that market demand, rather than scientific literature, will drive design trends. Granting patent protection to advance that would occur in the ordinary course without real

> innovation retards progress and may, in the case of patents combining previously known elements, deprive prior inventions of their value or utility.

KSR, 550 U.S. at 417-419; 127 S.Ct. at 1740-41. The Federal Circuit has harmonized the KSR opinion with many prior circuit court opinions by holding that when a patent challenger contends that a patent is invalid for obviousness based on a combination of prior art references, "the burden falls on the patent challenger to show by clear and convincing evidence that a person of ordinary skill in the art would have had reason to attempt to make the composition or device, or carry out the claimed process, and would have had a reasonable expectation of success in doing so. *PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007)(citing *Medichem S.A. v. Rolabo S.L.*, 437 F.3d 1175, 1164 (Fed. Cir. 2006)); *Noelle v. Lederman*, 355 F.3d 1343, 1351-52 (Fed. Cir. 2004); *Brown & Williamson Tobacco Corp. v. Philip Morris, Inc.*, 229 F.3d 1120, 1121 (Fed .Cir. 2000) and *KSR*, 127 S.Ct. at 1740 ("a combination of elements 'must do more than yield a predictable result'; combining elements that work together 'in an unexpected and fruitful manner' would not have been obvious"). Further, a suggestion to combine need not be express and may come from the prior art, as filtered through the knowledge of one skilled in the art. *See Certain Lens-Fitted Film Pkgs.*, Inv. No. 337-TA-406, Order No. 141 at 6 (May 24, 2005).

"Secondary considerations," also referred to as "objective evidence of non-obviousness," must be considered in evaluating the obviousness of a claimed invention, but the existence of such evidence does not control the obviousness determination. *Graham*, 383 U.S. at 17-18. A court must consider all of the evidence under the *Graham* factors before reaching a decision on obviousness. *Richardson-Vicks Inc.*, 122 F.3d at 1483-84. Objective evidence of non-obviousness may include evidence of the commercial success of the invention, long felt but unsolved needs, failure of others, copying by others, teaching away, and professional acclaim.

See Perkin-Elmer Corp. v. Computervision Corp., 732 F.2d 888, 894 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 857 (1984); *Avia Group Int'l, Inc. v. L.A. Gear California*, 853 F.2d 1557, 1564 (Fed. Cir. 1988); *In re Hedges*, 783 F.2d 1038, 1041 (Fed. Cir. 1986); *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565 (Fed. Cir. 1986), *cert. denied*, 479 U.S. 1034 (1987). The burden of showing secondary considerations is on the patentee and, in order to accord objective evidence substantial weight, a patentee must establish a nexus between the evidence and the merits of the claimed invention; a *prima facie* case is generally set forth "when the patentee shows both that there is commercial success, and that the thing (product or method) that is commercially successful is the invention disclosed and claimed in the patent." *In re GPAC Inc.*, 57 F.3d 1573, 1580 (Fed. Cir. 1995); *Demaco Corp. v. F. Von Langsdorff Licensing Ltd.*, 851 F.2d 1387, 1392 (Fed. Cir. 1988), cert. denied, 488 U.S. 956 (1988); *Certain Crystalline Cefadroxil Monohydrate*, Inv. No. 337-TA-293, Comm'n Op. (March 15, 1990). Once a patentee establishes nexus, the burden shifts back to the challenger to show that, *e.g.*, commercial success was caused by "extraneous factors other than the patented invention, such as advertising, superior workmanship, etc." *(Id.)* at 1393.

Generally, a prior art reference that teaches away from the claimed invention does not create *prima facie* case of obviousness. *In re Gurley*, 27 551, 553 (Fed. Cir. 1994); *see also Andersen Corp. v. Pella Corp.*, No. 2007-1536, 2008 U.S. App. LEXIS 24087, *13-18 (Fed. Cir. Nov. 19, 2008); *Certain Rubber Antidegradants*, Inv. No. 337-TA-533 (Remand), Final ID (Dec. 3, 2008) (stating, "*KSR* reaffirms that obviousness is negated when the prior art teaches away from the invention.")). However, the nature of the teaching is highly relevant. *Id.* "A reference may be said to *teach away when* a person of ordinary skill, upon reading the reference, would be *discouraged from following the path set out in the reference, or would be led in a direction*

divergent from the path that was taken by the applicant." *Id.* (emphasis added). For example, "a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant." *Id.*

1. The '106 Patent

a) Analysis of the asserted claims

Respondents argue that the combination of U.S. Patent Nos. 5,148,265 ("Khandros '265"), which issued on September 15, 1992, and 4,059,708 ("Heiss '708"), which issued on November 22, 1977, renders claims 1-4, 9-10 and 33-35 obvious. (RIB at 80.) Respondents argue that Khandros '265 anticipates all of the asserted claims except that it failed to disclose the use of a structure placed "in contact" with the dielectric interposer for the purpose of protecting the terminal structures and that Heiss '708 teaches the use of protective structures that are in contact with the substrate in order to prevent flow of the encapsulation material to areas that are used for electrical connections like the terminals. (RIB at 79-80.) The motivation to combine these two references stems from the "fundamental goal" of semiconductor packaging to protect the terminals from encapsulant and, given the limited number of alternative solutions, one of ordinary skill in the art would have "looked to techniques used for similar devices" to achieve that goal. (RIB at 80.)

Tessera argues that there is no motivation to combine the two references because (1) Heiss '708 teaches away from the combination because it teaches that rubber masks can damage circuit components and that the dams provide limited resolution when used with flow coating encapsulation; (2) the liquid mask of Heiss '708, which is made of "water and/or alcohol soluble polymer," would be disrupted by the pressurized liquid encapsulant taught by Khandros '265; and (3) the examiner already made the same obviousness argument, which was ultimately

rebutted by the inventors and the '106 Patent issued. (CIB at 99-100.) Tessera argues that secondary considerations weigh against a finding obviousness. Specifically, Tessera cites the commercial success of Respondents' products, the long felt need of fixing terminal contamination problems; copying of the claimed invention by Respondents and non-respondent Micron; and the licensing of the '106 Patent, including settled respondents International Products Sourcing Group and Patriot Memory. (CIB at 100-101.) Staff agrees. (SIB at 95-96.)

Staff argues that Respondents have failed to provide a complete obviousness analysis, including *Graham* factors. (SIB at 95.) Staff further argues that the evidence teaches away from the prior art combination of Heiss '708 and Khandros '265 and that the patent examiner considered similar arguments during prosecution, which the inventors were able to overcome. (SIB at 95.)

Respondents do not address Tessera's assertions of secondary considerations either in its initial post hearing brief or in its reply brief. (*See* RIB at 67-81; RRB at 32-40.)

The ALJ finds that, by simply making cursory assertions and conclusory arguments comprised of two paragraphs, Respondents have blatantly failed to meet the clear and convincing standard necessary to invalidate the '106 Patent based on obviousness. *See PharmaStem*, 491 F.3d at 1360 (stating that a patent challenger must "show by clear and convincing evidence that a person of ordinary skill in the art would have had reason to attempt to make the composition or device, or carry out the claimed process, and would have had a reasonable expectation of success in doing so."); *see also Tech. Licensing*, 545 F.3d at 1327 (stating, "When an alleged infringer attacks the validity of an issued patent, [the] well-established law places the burden of persuasion on the attacker to *prove invalidity by clear and convincing evidence*." (emphasis added)). A person is not entitled to a patent if the differences between the claimed invention and the prior art

"are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. §103. The underlying factual inquiries relating to non-obviousness include: 1) the scope and content of the prior art, 2) the level of ordinary skill in the art, 3) the differences between the claimed invention and the prior art, and 4) secondary considerations of non-obviousness, such as long-felt need, commercial success, and the failure of others. *See Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). Respondents merely cursorily address the first three of these factors and fails to address the last factor relating to secondary considerations. Respondents' cursory argument are insufficient to meet the clear and convincing evidence standard necessary to invalidate the '106 Patent as obvious.

2. The '977 and '627 Patents

As set forth *supra*, the ALJ has found that Respondents have waived their obviousness arguments. *See supra* at V.C.2.e.

E. Definiteness

Claims must ". . . particularly point [ ] out and distinctly claim [ ] the subject matter which the applicant regards as his invention." 35 U.S.C. § 112, ¶ 2; *Miles Laboratories, Inc. v. Shandon Inc.*, 997 F.2d 870, 874-75 (Fed. Cir. 1994). The purpose of this definiteness requirement is to ensure that the claims delineate the scope of the invention using language that adequately notifies the public of the patentee's right to exclude. *Young v. Lumenis, Inc.*, 492 F.3d 1336, 1346 (Fed. Cir. 2007). If a claim read in light of the specification reasonably apprises one of ordinary skill in the art of its meaning, that claim satisfies § 112, ¶2. *Id.* In contrast, if a claim limitation is "insolubly ambiguous" or "not amenable to construction," then the claim

containing that limitation is invalid for indefiniteness. *See, e.g., Datamize, LLC v. Plumtree Software, Inc.*, 417 F.3d 1342, 1347-1356 (Fed. Cir. 2005) (affirming summary judgment of invalidity due to indefiniteness); *Honeywell Int'l, Inc. v. United States Int'l Trade Comm.*, 341 F.3d 1332, 1338-1339 (Fed. Cir. 2003).

1. The '106 Patent

Respondents argue that claim 34 of the '106 Patent is invalid because the claim term "compliant layer" renders the claim indefinite under 35 U.S.C. § 112, ¶ ¶ 1 & 2. (*See* RIB at 81.) However, as set forth *supra*, the ALJ determined that the claim term "compliant layer" means "a layer having a low modulus of elasticity that permits slight movement" citing portions of the specification that support that construction. Furthermore, the evidence shows that one of ordinary skill in the art would understand "compliant layer." (*See* CX-07350C (Goosey RWS) at Q. 398.) Therefore, the ALJ finds that Respondents have failed to show that claim 34 is invalid under 35 U.S.C. § 112, ¶ ¶ 1 & 2 .

Respondents further argue that claim 3 of the '106 Patent is invalid under 35 U.S.C. § 112, ¶ 4 because claim 3 fails to add any limitation not already present in claims 1 and 2 from which claim 3 depends. (RIB at 81.) Specifically, Respondents conclusorily state that claim 3, which depends from claim 2, claims "the step of curing said curable material after said curable material has been introduced into said encapsulation area," and that this is already claimed in independent claim 1, which claimed "introducing and encapsulation material into at least a portion of the encapsulation area so that the encapsulation material flows to fill the encapsulation area and then cures to a substantially solid condition." (RIB at 81.)

Tessera argues that Respondents have waived this argument as they failed to raise or disclose this argument during discovery and, further, that Respondents failed to present any

evidence on this during the hearing. (CRB at 41,) Furthermore, Tessera argues that the invention claimed in claim 1 is different from that claimed in claim 3. (CRB at 41.)

Staff similarly argues that Respondents failed to offer any evidence at the hearing on this matter and, further, that the "patent speaks for itself" in demonstrating that claim 3 further limits claims 1 and 2. (SIB at 85-86.)

The ALJ finds that simply making cursory assertions and conclusory arguments, without citing to any evidence of further analysis, is insufficient for Respondents to meet the clear and convincing standard necessary to invalidate claim 3 of the '106 Patent.

2. The '977 and '627 Patents

a) "movable"

Respondents contend that the limitation "movable," which is found in each of the asserted claims of the '977 and '627 patents, is indefinite under 35 U.S.C. § 112, ¶ 2. (RIB at 116.) Specifically, Respondents argue that the asserted patents fail to disclose: (1) any methodology or test to determine what movement falls within the claims; (2) any reference point from which to determine the claimed terminal movement; and (3) the amount or range of terminal movement required by the claims. (*Id.*) Tessera argues that its proposed construction of the limitation "movable" is definite. (CRB at 18.) The Staff also argues that the limitation is not indefinite. (SRB at 15.)

The limitation "movable" has been construed herein to mean that "in the operation of the assembly, the terminals are capable of being displaced relative to the chip by external loads applied to the terminals, to the extent that the displacement appreciably relieves mechanical stresses, such as those caused by differential thermal expansion which would be present in the electrical connections absent such displacement." (*See supra*, at III.C.2.a.) The above claim

construction makes plain that the claimed movement is movement caused by an outside force (*i.e.*, external load) that appreciably relieves mechanical stresses that would be present absent such movement. So, for example, terminal movement not due to an outside force or terminal movement that does not appreciably relieve mechanical stresses that would be present absent such movement, is not the "claimed movement." Thus, the ALJ finds Respondents' argument that the asserted patents do not distinguish between the claimed and unclaimed movement unpersuasive.

With regard to Respondents' argument that the specification fails to identify any objective way to determine what amount of claimed movement constitutes infringement, the ALJ again is unpersuaded. The claim construction adopted herein and recited above requires terminal movement due to external loads that *appreciably relieves* mechanical stresses, such as those caused by differential thermal expansion which would be present in the electrical connections absent such displacement. "A patentee need not define his invention with mathematical precision in order to comply with the definiteness requirement." *Oakley, Inc. v. Sunglass Hut Int'l*, 316 F.3d 1331, 1341 (Fed. Cir. 2003). Terms such as significant and substantial are "ubiquitous in patent claims" and routinely are upheld by the courts. *See Andrew Corp. v. GahrietElectronics, Inc.*, 847 F.2d 819, 821 (Fed. Cir. 1988) (the term "closely approximate" is definite); *see also Charvat v. Commissioner of Patents*, 503 F.3d 138, 148 (Fed. Cir. 1978) (courts frequently validate terms such as "substantial") (citing *Ethel Process Co. v. Minnesota. & Ontario Paper Co.*,261 U.S. 45, 65-66 (1923). Therefore, there is nothing inherently wrong with the requirement that the terminal movement *appreciably relieves* mechanical stresses.

The question is whether one of ordinary skill in the art can discern what is meant by "appreciably relieves mechanical stresses . . ." On this point, the evidence shows that one skilled

in the art would readily be able to understand the scope of the asserted claims of the '977 and '627 patents when read in light of the specifications. (*See* CX-7349C (Ivey Direct) QQ. 873, 896, 899; CX-06486C (Qu Direct) Q. 154.) In fact, the evidence shows that Respondents' own expert Dr. Ulrich was able to discern the metes and boundaries of the asserted claims. (CX-7349C (Ivey Direct) Q. 905.)

Accordingly, for the reasons discussed above, the ALJ finds that Respondents have failed to prove by clear and convincing evidence that the limitations "terminals are movable with respect to said contacts" and "[terminals] being movable with respect to the central contacts to compensate for differential thermal expansion" are indefinite under 35 U.S.C. § 112 ¶ 2.

b) "compliant layer"

Respondents argue that the limitations "compliant layer" and "layer of compliant material" which is found in each of the asserted claims of the '977 and '627 patents, is indefinite under 35 U.S.C. § 112, ¶ 2. (RIB at 116-17.) Specifically, Respondents argue that the asserted patents fail to delineate a range of materials that are compliant. *Id.* Tessera argues that its proposed construction of the limitations are definite. (CRB at 19.) The Staff also argues that the limitations are not indefinite. (SRB at 15.)

The evidence of record indicates that one of ordinary skill in the art at the time of the invention would understand what is called for by the limitations "compliant layer" and "layer of compliant material." Specifically, Dr. Ivey testified that:

> **Q. 920 What is your opinion regarding whether a person of ordinary skill would know how much compliancy is needed?**
> That person would know. As we discussed earliler, that person would have tools such as a Coffin-Manson-type equation to use. Additionally, let me refer you to the testimony of Respondents' own expert on this issue, Dr. Ulrich, because I thnk it sums things up nicely.

> Now, clearly, if this were being done with no other consideration other than lessening the stress, a light-year thick layer would be better than a mil thick layer. But that would be impractical. And although that's a ridiculous example, the same logic holds.
> Principally in the use of complaiant layers, such as die attach materials, you can make it thicker and thicker and thicker, and you can make the Young's modulus smaller and smaller and smaller, and as you do so, you will get less stress throughtout the package, something we've known long before this patent come out. And that's a good thing. But you create other effects, as well, that are not good things.
> One principal problem that you cause is that it becomes very difficult to wire bond to a chip that has thick compliant layer underneath. Another is that having more material underneath tends to outgas a bit more. And another problem is it costs more money. If you're doing several hundred million of these a month, even increase of a penny can - - can hurt stock prices.
> So my understanding of the word "maximize" in this context is that it maximizes the mechanical strees releief attainable when employed in a practical manner inside of the package to which it's being used.

(Ulrich 8/17/08 Depo Tr. 62:24-64:1).

Q. 921 Do you agree with Dr. Ulrich's testimony on this issue?
I think Dr. Ulrich and I both agree that a person of ordinary skill tasked with creating a "compliant layer" or "compliant material" would not be a loss simply because the '627 and '977 Patents do not explicity disclose the thickness or some other property of that layer. Instead, a person of ordinary skill would know how to balance different factors such as thickness, modulus of elasticity, material and cost in the given situation. After all, striking this kind of balance is what engineers do all the time.

(CX-7349C (Ivey Direct) QQ. 920-21.)

Accordingly, the ALJ finds that Respondents have failed to prove by clear and convincing evidence that the limitations "compliant layer" and "layer of compliant material" are indefinite under 35 U.S.C. § 112 ¶ 2.

VI. RESPONDENTS' AFFIRMATIVE DEFENSES

Respondents have asserted the affirmative defenses of license and patent exhaustion. (RIB at 5-34; RRB at 2-19.) Elpida additionally asserts the defense of equitable estoppel. (RIB

at 34-36; RRB at 19-20.) The burden falls on the accused infringers to establish their defenses. *Jazz Photo Corp. v. International Trade Com'n,* 264 F.3d 1094, 1102 (Fed. Cir. 2001).

A. LICENSE DEFENSE

Selling or importing a patented product is not infringement if the authority to do so has been granted. *See* 35 U.S.C. §271(a) ("whoever ***without authority*** makes, uses, offers to sell or sells any patented invention, within the United States or imports into the United States any patented invention ... infringes the patent) (emphasis supplied). The Supreme Court long ago recognized that a license is a complete defense to a claim of infringement. *See De Forest Radio Tel. & Tel. Co. v. United States*, 273 U.S. 236, 241 (1927). A license is also a complete defense in a Section 337 Investigation. *See Certain Cardiac Pacemakers and Components Thereof,* ITC Inv. No. 337-TA-162, 1984 WL 273841, at *10 (May 23, 1984) ("Telectronics' motion for termination of the Investigation relative to Telectronics for infringement of the '242 patent is hereby granted because a valid license is an absolute defense to patent infringement.") The burden of proof lies on the accused infringer to prove the license. *Bandag, Inc. v. Al Bolser's Tire Stores, Inc.*, 750 F.2d 903, 924 (Fed. Cir. 1984).

Respondents argue that the "license" defense applies in this investigation because "all or substantially all" of the accused DRAM was purchased from licensed entities. In addition, Tessera's complaint states that "properly licensed" products are not subject to this investigation. (RRB at 4-5.) (citing Complaint at ¶ 9.) Respondents argue that whether Tessera's licensed-entities failed to pay royalties should not affect Respondents' lawful ability to assemble, use, or sell DRAM that was sold to Respondents under the color of a Tessera Compliant Chip ("TCC") license. (RIB at 10-22.)

Tessera argues that Respondents have not met their burden because: (1) at least a portion of Respondents' accused products came from unlicensed entities; and

(CIB at 105-113; CRB at 45-54.) Tessera argues that Respondents knew that Tessera's licensed-entities were capable of selling unlicensed product and therefore Respondents "assumed the risk" of purchasing unlicensed DRAM. Tessera contends that Respondents could have avoided the risk by purchasing their own licenses. (CIB at 102-103.)

Staff argues that Respondents' license defense is actually a patent exhaustion or implied license defense because none of the Respondents are themselves licensees. (SIB at 52-55.)

Tessera admits that "properly licensed" products are not subject to this investigation. (Complaint at ¶ 9.) The Tessera License Agreements are governed by California law. (Jager, Tr. 3092:12-15; CX 05536C at XV.A; JX-00026C at XVI.A., Griffin, Tr. 1103:14-17; JX-00032C at XIV.A.; JX-00045C at XIV.A; Marcucci, Tr. 1225:9-1226:15; RX 4363C; JX 00011C at XIV.A; RX 2633C at XIV.A; JX-00020C at XVI.A; JX-00036C at XIII.A; RX 2635C at XIII.A; Griffin, Tr. 1121:20-23; JX-00044C at XIV.A; RX 2641C at XIV.A.; JX-00057C at 12; RX 2642C at 12; JX-00024C at XVI.A; RX 2634C at XVI.A; Griffin, Tr. 1128:2-21; JX-00069C at XVI.A; RX 2645C at XVI.A.; JX-00064C at XVI.A; RX 2635C at XVI.A; Griffin, Tr. 1140:6-8; JX-00065C at XIV.A; RX 4363C.). *See also Certain Semiconductor Chips with Minimized Chip Package Size and Products Containing Same*, Inv. No. 337-TA-432, Order No. 5 (August 9, 2000) (stating California law governs interpretation of "Limited TCC License Agreement" between Tessera and Texas Instruments).

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[11]

In California, contracts are generally binding and enforceable only on the parties who executed the contract. *See Murphy v. Allstate Ins. Co.*, 17 Cal. 3d 937, 944 (1976) ("[a] third party should not be permitted to enforce covenants made not for his benefit, but rather for others... He is not a contracting party; his right to performance is predicated on the contracting parties' intent to benefit him.")[12],[13] The exception is "a contract, made *expressly* for the benefit of a third person, may be enforced by him." Cal. Civ. Code § 1559 (emphasis added).

Respondents are not Tessera licensees. (*See* RRCPFF X.2-11.) Respondents do not argue that they are third party beneficiaries under California law. Moreover, none of the Respondent's names appear in the asserted licenses, and none were made for Respondents' "express" benefit. (*See generally* RIB at 5-33; *See* CX-03605C; CX-03607C; CX-03609C, CX-03710C, CX-03713C, CX-03758C, CX-03759C, CX-03780C, CX-03782C, CX-03783C, CX-03824C-CX-03827C, CX-03836C, CX-03844C, CX-03855C-CX-03858C, CX-03860C, CX-03861C, CX-03889C-CX-03896C, CX-04042C, CX-04141C, CX-04193C, CX-04194C, CX-04200C, CX-05519C, CX-05521C-CX-05524C, CX-05527C, CX-05529C-CX-05536C,

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[12] Under 35 U.S.C. § 271(a), whoever "without authority" makes, uses, offers to sell, or sells any patented invention infringes the patent. Authority is a question of contract. *See Spindelfabrik Suessen-Schurr v. Schubert & Salzer Maschinenfabrik AG*, 829 F.2d 1075, 1081 (Fed. Cir. 1987) *cert. denied*, 484 U.S. 1063 (1988) (holding that patent licenses are "no more than a covenant by the patentee not to sue."). A contractual obligation not to sue may be express or implied. *See De Forest Radio Tel. Co. v. United States*, 273 U.S. 236, 241, 47 S. Ct. 366, 367 (1927) ("Any language used by the owner of the patent, or any conduct on his part exhibited to another from which that other may properly infer that the owner consents to his use of the patent in making or using it, or selling it, upon which the other acts, constitutes a license and a defense..."); *see also Wang Laboratories, Inc. v. Mitsubishi Electronics America, Inc.*, 103 F.3d 1571, 1576 (Fed. Cir. 1997) ("An implied license is a form of implied-in-fact contract.")

[13] Commercial contracts are generally interpreted under state law, but where federal statutes apply a patent license will be interpreted under the federal scheme. *See Rhone-Poulenc Agro, S.A. v. DeKalb Genetics Corp.*, 284 F.3d 1323, 1328 (Fed. Cir. 2002) ("interpretation of patent license contracts is generally governed by state law...However [i]t would be anomalous for federal law to govern [a] defense in part and for state law to govern in part."). The bona fide purchaser defense is one such area of the law where uniform federal law is favored over state law. *Id.* ("There is quite plainly a need for a uniform body of federal law on the bona fide purchaser defense.") (citing 35 U.S.C. §261). But "[s]tate law is not displaced merely because the contract relates to intellectual property." *Aronson v. Quick Point Pencil Co.*, 440 U.S. 257, 262 (1979); *see also Lear, Inc. v. Adkins*, 395 U.S. 653, 661-63 (1969) ("[C]onstruction of the 1955 licensing agreement is solely a matter of state law."); *Gjerlov v. Schuyler Labs., Inc.*, 131 F.3d 1016, 1020 (Fed. Cir.1997); *Studiengesellshcaft Kohle, M.B.H. v. Hercules, Inc.*, 105 F.3d 629, 632 (Fed. Cir.1997); *Sun Studs, Inc. v. Applied Theory Assocs., Inc.*, 772 F.2d 1557, 1561 (Fed. Cir.1985.)

CX-05538C, CX-05544C-CX-05547C, CX-05549C-CX-05560C, CX-06063C, CX-06135C; JX-00008C-JX-00045C, JX-00050C-JX-00069C, JX-00541C-JX-00543C; RX-567C, RX-568C, RX-571C, RX-572C, RX-584C, RX-2633C-RX-2635C, RX-2641C-RX-2643C, RX-2645C, RX-2646C.) Thus, Respondents do not have a "license" defense *per se*. The ALJ finds that Respondents have failed to meet their burden in proving their affirmative defense of "license."

B. PATENT EXHAUSTION

Respondents' license defense is better framed as a patent exhaustion defense. Patent exhaustion doctrine provides that the first authorized unconditional sale of a patented item terminates patent rights to that item. *Quanta Comp., Inc. v. LG Elecs., Inc.*, 128 S. Ct. 2109, 2115 (2008). The patented article becomes the purchaser's personal property, with the purchaser acquiring "the right to use it, repair it. modify it, discard it, or resell it, subject only to overriding conditions of the sale." *Jazz Photo Corp. v. ITC,* 264 F.3d 1094, 1102 (Fed. Cir. 2001) (*citing Mitchell v. Hawley*, 83 U.S. 544, 548 (1872)).

Respondents argue that Tessera "authorized" licensees to sell DRAM embodying the '106, '977 and '627 patents and Respondents purchased it, exhausting Tessera's rights. Tessera argues that: (1) at least a portion of Respondents' packages came from *un*licensed entities—who would have no authority to sell the packages, and (2) some "licensed entities" have sold "unlicensed products" by operation of the Exclusion Provisions. [redacted] Under

[14] "[redacted]

Tessera's construction of the Exclusions Provisions in its TCC license agreements, a product does not become fully licensed until the licensee pays royalties.

Staff argues that regardless of the Exclusion Provisions, Respondents have each purchased packages from unlicensed sources. (SRB at 53.) Staff further notes that some of Respondents' licensed suppliers were indeed "not in good standing." (*Id.*). Staff concludes that Respondents have not proven their exhaustion defense.

Respondent Elpida contends that 100% of its accused packages were purchased from licensed entities. (RRB at 13.) The rest of the Respondents contend that "all or a substantial portion" of the accused products are purchased from Tessera licensees. Respondents generally concede that while a portion of their *worldwide* DRAM is purchased from unlicensed sources, the fact is that Respondents purchase more than enough DRAM from licensed suppliers to "saturate" their U.S. market. (RIB at 6-7.) Respondents also assert that even if the DRAM they purchased was only "potentially" licensed at the time of sale, Tessera still granted authority for the sale which is sufficient under *Quanta.* (RRB at 17.)

The ALJ finds that Respondents are correct that Tessera conflates the concepts of "authority to sell" and "licensed product." Tessera's contention that the issue of license is a "threshold question" of exhaustion is incorrect as a matter of law. Under the Supreme Court's holding in *Quanta*, the threshold question is "authority to sell"—not license:

> Because Intel was *authorized to sell* its products to Quanta, the doctrine of patent exhaustion prevents LGE from further asserting its patent rights... Intel's authorized sale to Quanta thus took its products outside the scope of patent monopoly, and as a result, LGE can no longer assert its patent rights against Quanta"

128 S. Ct. 2121-22 (emphasis added). The ALJ acknowledges that most of the time the "authority to sell" is derived from a license agreement. Indeed, in *Quanta*, the Court looked to

Intel's license agreement with LGE to determine if Intel had authorization to sell LGE technology. The Court found that Intel did possess such authority. *Id.* at 2121 ("[n]othing in the License Agreement restricts Intel's right to sell its microprocessors and chipsets to purchasers who intend to combine them with non-Intel parts.").

[REDACTED]

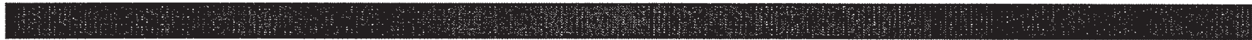
The facts of *Quanta* are stridently similar to those in the instant investigation. Respondents are third party purchasers, like Quanta. Respondents assert that their suppliers and packagers had "authority to sell" based on an ongoing license relationship with the patent holder, Tessera. [REDACTED] In *Quanta*, the condition subsequent was third party use of the technology in combination with non-Intel parts. 128 S. Ct. at 2121. [REDACTED]

However, even if a post-sale condition could be binding on a third party purchaser of patented technology, it is not clear that the Exclusion Provisions should be construed as post-sale conditions because Tessera and Respondents interpret the provision differently. The text of a representative Exclusion Provision[15] states:

[REDACTED]

[15] As mentioned in note 7, the "Exclusion from License" provisions may vary slightly from one agreement to the next. However, since the parties treat them the same, the ALJ will do the same.

(RX-2633 at II.D; *see also* (RX-10C (Murtha Direct W.S.) QQ. 169, 171, 172.; CX-07352C (Griffin Rebuttal W.S.) QQ. 13-15; JX-00036C at II.D ; JX-00032C; RX-2897C ; Jager, Tr. 3085:6-3086:18; RX-2633 at II.D.)



In the event that the ALJ finds the Exclusion Provisions ambiguous, Tessera argues that parole evidence supports its construction and not Respondents' proposed construction. Tessera proffered evidence that a Tessera licensee not named in this investigation [redacted] understood the conditional nature of the Exclusion Provision. (CRB at 107).

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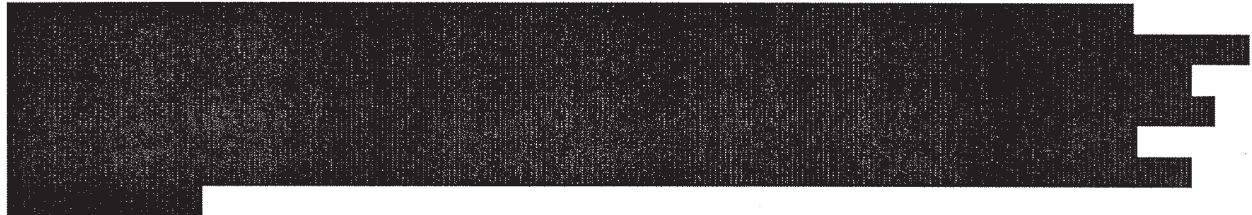
[16] [redacted]



"Construction of [a] licensing agreement is solely a matter of state law." *Lear Inc. v. Adkins,* 395 U.S. 653, 661-63 (1969). "State law is not displaced merely because the contract relates to intellectual property." *Aronson v. Quick Point Pencil Co.*, 440 U.S. 257, 262 (1979). As an initial matter, the TCC licenses are be interpreted under California law by operation of their forum selection clauses as noted *supra.* Under California contract statutes, particular clauses of a contract are subordinate to its "general intent." Cal. Civ. § 1650. "Words in a contract which are wholly inconsistent with its nature, or with the main intention of the parties, are to be rejected." Cal. Civ. § 1653. A condition involving forfeiture must be strictly interpreted against the party for whose benefit it is created. Cal. Civ. § 1442.

The ALJ finds that the TCC Exclusion Provisions are ambiguous:

Because the provision is capable of carrying either interpretation on its face, the ALJ resorts to the tools of interpretation set forth in California contract statutes.

First, Tessera's interpretation involves a condition and Respondents' interpretation does not. Under California contract statutes, the ALJ must favor Respondents' interpretation because conditions are strictly construed. By burying the condition that the drafter risked a construction of this most critical condition in a manner adverse to that intent. If the exclusion clause were given its literal meaning,

Moreover, Tessera's construction contradicts other provisions in the TCC contracts. [redacted]

[redacted] The difference between a breach of contract and the nonoccurrence of a condition is significant: a breach is a "violation of a contractual obligation by failing to perform one's own promise..." whereas the nonoccurrence of a condition determines whether an obligation even *exists*. Black's Law Dictionary (8th ed. 2004) ("condition") ("breach of contract"). Finally, Tessera created the ambiguity as the drafter and the contract is therefore most strongly interpreted against Tessera. *See* Cal. Civ. Code § 1654 (2008) ("In cases of uncertainty not removed by the preceding rules, the language of a contract should be interpreted most strongly against the party who caused the uncertainty to exist."). The ALJ is compelled to reject Tessera's construction of the Exclusion Provisions as a condition.

Tessera argues that this approach leaves them without any remedy. (CIB at 108.) This is simply not true, and Tessera itself has provided the ALJ with the evidence that it is untrue. Under its license agreements, [redacted]

[redacted] Despite these on-contract remedies, Tessera continues to argue that it needs the ability to seek remedy against innocent third parties purchasers because it cannot know how much it is owed.

In contradiction of its own arguments and witness statements regarding the need for third party remedies, Tessera filed the results of its arbitration case with Amkor, *Tessera v. Amkor.* (*See Tessera v. Amkor Technology, Inc.*, Case No. 14 268/EBS/VRO (ICC International Court of

Arbitration); EDIS Document ID 313173.) In arbitration, Tessera was able to do precisely what it now says it cannot: vigorously dispute license claims regarding third parties and determine royalty amounts due with relative precision, including interest. This result seems more than mere coincidence and show that Tessera's licenses are perfectly and properly enforceable against Tessera's licensees on-contract.

While the Uniform Commercial Code ("the U.C.C.") is not strictly binding on license agreements, it is certainly influential. *See* Raymond T. Nimmer, *Modern Licensing Law §2:9* (2008) ("One significant influence [of licensing law] has been U.C.C. Article 2, or at least some of the general doctrines it incorporates.") The Code states that the purpose of the law is to "simplify, clarify and modernize" commercial transactions and it should be construed liberally to achieve those ends.[17] *See Id.*, § 1103(a). When a third party purchaser in good faith buys an item from a dealer whose business is to sell similar items, the purchaser takes the item free and clear of third party interests. *See* Cal. Com. Code §§ 1201(9), 2403(1)(b).

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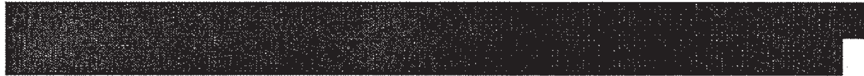
[17] Cal. Comm. Code § 1103. (a) This code shall be liberally construed and applied to promote its underlying purposes and policies, which are:

(1) to simplify, clarify, and modernize the law governing commercial transactions;

(2) to permit the continued expansion of commercial practices through custom, usage, and agreement of the parties; and

(3) to make uniform the law among the various jurisdictions.



(CRB at 55.)

By contrast, Tessera's interpretation creates chaos. Under Tessera's construction, secondary purchasers are not certain that the products they buy are free from third party claims. If a company decides to purchase products from a dealer, they can (1) ask the company prove they have a license, and/or (2) ask Tessera to confirm the company is a licensee in good standing. But those measures get the third party purchaser nowhere because, according to Tessera, the licensee in good standing, amazingly, might not be selling "licensed products." This is because the licensee's authority is conditioned on a future event, namely the quarterly payment of royalties. Thus, until the royalty is paid, no entity, including Tessera, can be sure the packages are "licensed." Indeed, unless the third party purchaser is able to account for each chip or package the Tessera licensee has sold, it cannot be safe from a future action.

The argument is further complicated because most, if not all, of the TCC license agreements are confidential, so the very third party that Tessera claims is obligated to enforce the contract cannot gain access to the contract. Under Tessera's construction, the only possible way that the third party could safeguard their business from unmet future conditions is to purchase a license themselves and risk paying double royalties — one royalty price is embedded in the purchase price marketed by the licensee and the other price is paid from the third party purchaser directly to Tessera. While Tessera has disavowed any desire to collect double royalties, they have presented no evidence that preventative or corrective steps are or will be affirmatively taken to avoid overpayment. The sole example of Tessera taking corrective action regarding overpayment occurred when a *customer* determined that Tessera was collecting an undeserved

windfall and confronted the company. (Griffin 9/24/08 Tr. 1014:3-20.) Tessera's willingness to refund its customers in that situation is hardly assurance that future overpayment will be avoided.

In support of this conclusion, the ALJ notes that Tessera's notions of "flexible licensing" were before the Supreme Court in *Quanta* and not adopted. *See* 2007 WL 4340883 (Tessera's Amicus Br. in Supp. of LGE.). In Tessera's amicus brief filed in support of LGE, Tessera argued that "today's global economy depends on flexible licensing strategies that in many cases require separate licenses for components, systems, and methods at different levels of manufacturing, distribution, and retail chain in order to capture all of the value of the patented inventions." *Id.* at *2. The *Quanta* Court squarely rejected this argument by relying on *Univis Lens, Co. v. United* States, 316 U.S. at 244, 254 (1942). *Univis* invalidated a licensing scheme that involved royalty payments from multiple licensees within the same supply chain. *Id.* at 254.

A second amicus brief from *Quanta* is instructive: Qualcomm, Inc. submitted a brief arguing that retro-actively terminating an already-granted license should be permissible if the licensee breaks a condition subsequent. 2007 WL 43400879 at *8-9. In the case of Qualcomm, the condition subsequent was that licensees promised not to sell Licensed Products to non-"Authorized Purchasers." *Id.* The Supreme Court's decision in *Quanta* rejected LGE's argument and thus rejected Qualcomm's similar argument. The Court considered and rejected licensing schemes permitting the after-sale control of patented items based on retro-active revocation of an otherwise valid license grant.

For the reasons stated above, Tessera's assertion that licensed entities sold Respondents unlicensed product is rejected. The ALJ finds that all chips Respondents purchased from licensed entities were authorized to be sold by Tessera and Tessera's rights in those chips became subject to exhaustion.

Nevertheless, DRAM purchased from unlicensed entities is not exhausted where Tessera did not otherwise authorize the entities to sell. Respondents' packages from unlicensed suppliers needed to be "sorted" away from U.S. market to avoid or otherwise be subject to an exclusion order. Respondents that purchased DRAM from *unlicensed entities* have failed to demonstrate that unauthorized chips were diverted, and thus no exhaustion defense has been proven by those Respondents. All Respondents, except Elpida, concede that at least a small portion of their worldwide DRAM purchases are made from unlicensed suppliers.[18]

Respondents "market saturation" evidence—namely demonstrating that they purchased enough licensed DRAM to *potentially* cover 100% of their U.S. market—does not demonstrate that they *actually* supplied the U.S. market with product purchased from licensed entities. Elpida is the only respondent that asserts that *all* of its DRAM was purchased through licensed suppliers.

For the reasons stated above, the ALJ finds that Respondents have met their burden of proving the affirmative defense of patent exhaustion as it relates to those packaged DRAM purchased from Tessera's licensees. As such, Tessera's patent rights are exhausted at the time Tessera's licensees sell their packaged DRAM components to Respondents, and Tessera cannot enforce patent law remedies against Respondents as it relates to those DRAMs purchased from Tessera's licensees thereafter. Elpida is the only respondent, however, that has proven that 100% of its imported packaged DRAM came from Tessera licensees. The remaining respondents have failed to that 100% of its accused packaged DRAM were purchased from Tessera licensees. In that regard, Respondents' defense of patent exhaustion fails.

C. ELPIDA'S ESTOPPEL DEFENSE

Respondent Elpida asserts the defense of equitable estoppel. Specifically, Elpida contends Tessera represented that no license was needed if Elpida used licensed packagers, but then sued Elpida when a royalty payment issue arose. (RIB at 19.) Elpida argues that it had no knowledge of underpayments at the time of suit.

Elpida's defense of estoppel turns on the conduct of the parties alone and not on contract interpretation. When analyzing whether a party should be estopped from asserting a claim of infringement based on equitable estoppel, the following three elements should be considered: (1) whether the claimant communicates something in a misleading way, either by words, conduct, or silence; (2) whether the other relies upon that communication; and (3) whether the other would

be materially harmed if the actor is later permitted to assert any claim inconsistent with the communication. *Auckerman Co. v. R.L. Chaides Constr. Co.*, 960 F.2d 1020, 1041 (Fed. Cir. 1992).

The ALJ finds that because Tessera has no right against Elpida and because Eplida's patent exhaustion defense has been found, Elpida's estoppel defense need not be reached.

VII. DOMESTIC INDUSTRY

On September 16, 2008, the ALJ issued an Initial Determination finding that Tessera has satisfied the domestic industry requirement pursuant to Section 337(a)(3)(C). *See* Order No. 31 (September 28, 2009). On October 8, 2008, the Commission determined not to review the order. *See Notice of Commission Decision Not to Review an Initial Determination Granting Tessera's Motion for Summary Determination That It Has Satisfied the Domestic Industry Requirement* (October 8, 2008).

VIII. CONCLUSIONS OF LAW

1. The Commission has personal jurisdiction over the parties, and subject-matter jurisdiction over the accused products.
2. The importation or sale requirement of section 337 is satisfied.
3. The accused products do not literally infringe the asserted claims of the '106 Patent, the '977 Patent and the '627 Patent
4. The accused products not infringe the asserted claims of the '106 Patent under the doctrine of equivalents.
5. The asserted claims of the '106 Patent, the '977 Patent and the '627 Patent are not invalid under 35 U.S.C. § 102 for anticipation.
6. The asserted claims of the '106 Patent, the '977 Patent and the '627 Patent are not invalid under 35 U.S.C. § 103 for obviousness.
7. The asserted claims of the '106 Patent, the '977 Patent and the '627 Patent satisfy the definiteness requirement of 35 U.S.C. § 112 ¶ 2.
8. A domestic industry for all of the asserted patents exists, as required by section 337.
9. Respondents have failed to prove the affirmative defense of licensing.
10. Respondents, with the exception of Elpida, have failed to prove the affirmative defense of patent exhaustion for all of their accused products.
11. Respondent Elpida has proven that its accused products were purchased from Tessera licensed entities are subject to patent exhaustion and do not infringe.
12. It has not been established that a violation of section 337 for the '977 Patent, the '627 Patent and the '106 Patent has occurred.

IX. INITIAL DETERMINATION AND ORDER

Based on the foregoing, it is the INITIAL DETERMINATION ("ID") of this ALJ that no violation of section 337 of the Tariff Act of 1930, as amended, has occurred in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain semiconductor chips with minimized chip package size and products containing same by reason of infringement of one or more of claims 17 and 18 of United States Patent No.5,679,977; claims 1-4, 9-12, and 15-16 of United States Patent No. 6,133,627; and claims 1-4, 9, 10 and 33-35 of United States Patent No. 5,663,106. The ALJ further determines that a domestic industry exists that practices United States Patent Nos. 5,679,977, 6,133,627 and 5,663,106.

Further, this Initial Determination, together with the record of the hearing in this investigation consisting of:

(1) the transcript of the hearing, with appropriate corrections as may hereafter be ordered, and

(2) the exhibits received into evidence in this investigation, as listed in the attached exhibit lists in Appendix A,

are CERTIFIED to the Commission. In accordance with 19 C.F.R. § 210.39(c), all material found to be confidential by the undersigned under 19 C.F.R. § 210.5 is to be given *in camera* treatment.

The Secretary shall serve a public version of this ID upon all parties of record and the confidential version upon counsel who are signatories to the Protective Order (Order No. 1.) issued in this investigation, and upon the Commission investigative attorney.

X. RECOMMENDED DETERMINATION ON REMEDY AND BOND

I. Remedy and Bonding

The Commission's Rules provide that subsequent to an initial determination on the question of violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, the administrative law judge shall issue a recommended determination containing findings of fact and recommendations concerning: (1) the appropriate remedy in the event that the Commission finds a violation of section 337, and (2) the amount of bond to be posted by respondents during Presidential review of Commission action under section 337(j). *See* 19 C.F.R. § 210.42(a)(1)(ii).

A. General Exclusion Order

Under Section 337(d), the Commission may issue either a limited or a general exclusion order. A limited exclusion order instructs the U.S. Customs and Border Protection ("CBP") to exclude from entry all articles that are covered by the patent at issue and that originate from a named respondent in the investigation. A general exclusion order instructs the CBP to exclude from entry all articles that are covered by the patent at issue, without regard to source.

A general exclusion order may issue in cases where (a) a general exclusion from entry of articles is necessary to prevent circumvention of an exclusion order limited to products of named respondents; or (b) there is a widespread pattern of violation of Section 337 and it is difficult to identify the source of infringing products. 19 U.S.C. § 1337(d)(2). The statute essentially codifies Commission practice under *Certain Airless Paint Spray Pumps and Components Thereof*, Inv. No. 337-TA-90, Commission Opinion at 18-19, USITC Pub. 119 (Nov. 1981) ("*Spray Pumps*"). *See Certain Neodymium-Iron-Boron Magnets, Magnet Alloys, and Articles Containing the Same,* Inv. No. 337-TA-372 ("*Magnets*"), Commission Opinion on Remedy, the

Public Interest and Bonding at 5 (USITC Pub. 2964 (1996)) (statutory standards "do not differ significantly" from the standards set forth in *Spray Pumps*).

In *Magnets*, the Commission confirmed that there are two requirements for a general exclusion order: a "widespread pattern of unauthorized use;" and "certain business conditions from which one might reasonably infer that foreign manufacturers other than the respondents to the investigation may attempt to enter the U.S. market with infringing articles." The Commission went on to state the following factors as relevant to determining whether there is a "widespread pattern of unauthorized use":

> (1) a Commission determination of unauthorized importation of the infringing article into the United States by numerous foreign manufacturers; or
>
> (2) the pendency of foreign infringement suits based on foreign patents corresponding to the U.S. patent; [or]
>
> (3) other evidence which demonstrates a history of unauthorized foreign use of the patented invention.

Magnets, Commission Opinion on Remedy, the Public Interest, and Bonding at 6 (citing *Spray Pumps*).

In addition, the Commission listed the following factors as relevant to showing whether "certain business conditions" – the second *Spray Pumps* factor – exist:

> (1) the existence of an established demand for the article in the U.S. market and conditions of the world market;
>
> (2) the availability to foreign manufacturers of U.S. marketing and distribution networks;
>
> (3) the cost for foreign entrepreneurs to build a facility that can produce the patented articles;
>
> (4) the number of foreign manufacturers whose facilities could be converted to manufacture the patented article; and

> (5) the foreign manufacturers' cost to convert a facility to produce the patented articles.

Id.

1. Widespread Pattern of Unauthorized Use

Tessera argues that there is a widespread pattern of unauthorized sale and importation of the "Accused Packaged Chips."[19] (CIB at 118.) Tessera argues that a vast majority of the DRAM chips imported into the U.S. use the accused technology and that hundreds of millions of unlicensed Accused Packaged Chips, totaling nearly $1 billion, were used or incorporated into electronic devices that were imported into the United States. (*Id.*)

Respondents argue that there is no widespread pattern of unauthorized use since over 90% of the U.S. and worldwide DRAM market is already licensed. (RRB at 57.) Rather, Respondents argue that there is a widespread pattern of authorized use and that the percentages of unlicensed products will likely decrease as the use of newer DRAM expands. (RRB at 62-63.)

Staff argues that there is a widespread pattern of unauthorized use as there is evidence of high demand for DRAMs and that a substantial number of unlicensed chip packages are imported into the U.S. (SIB at 98-99.)

2. Business Conditions

Tessera argues that the business conditions in the DRAM industry indicate that non-respondents will likely attempt to enter the U.S. market. (CIB at 121.) Specifically, Tessera argues that there is (1) significant demand for the Accused Packages with one billion DRAMs imported as standalone chips and the remaining 84% of DRAM chips arriving in downstream

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[19] Tessera uses "Accused Packaged Chips" to describe Respondents' specific accused products that were analyzed by Dr. Qu and Dr. Goosey and other small forma BGA chip packages that would be impacted by an exclusion order. (CIB at 118, note 34.)

products; (2) established U.S. distribution channels not controlled by Respondents that new infringers could easily access; (3) existing facilities could easily be taken over by new entities and non-respondent manufacturers can easily expand their operations; and (4) non-respondents downstream manufacturers can simply buy Accused Chip Packages from unlicensed DRAM manufacturers and incorporate those chips into downstream products prior to importation. (CIB at 121-123.)

Respondents argue that new unlicensed market entrants are unlikely in the field of semiconductor manufacturing because all DRAM manufacturers with a measurable share of the worldwide DRAM market are either already licensed or named as Respondents in this investigation. (RRB at 63.) Furthermore, Respondents argue that given the highly depressed state of the DRAM market and the high cost of starting a new manufacturing facility (billions of dollars), the likelihood of new entrant is remote. (RRB at 63-64.)

Staff argues that certain business conditions exist, namely that the accused chip packages are found in many electronic products, which are imported by electronic manufacturers and memory module makers in high volumes and there is evidence that semiconductor chip packages of manufacturers located abroad are incorporated into memory modules or other consumer electronics that are imported into the U.S.. (SIB at 99.)

3. Risk of Circumvention

Tessera argues that a general exclusion order is necessary to prevent circumvention of a limited exclusion order ("LEO") since a majority of the unlicensed Accused Packaged Chips is incorporated into downstream products that are imported by non-Respondents, which would not be subject to an LEO. (CIB at 118-119.) Tessera further argues that the low market price of DRAMs provide an incentive to unlicensed DRAM manufacturers to undercut their licensed

competitors and that should only an LEO issue, Respondents would have incentive to sell their DRAM business to non-respondents or create spin-off companies in order to avoid the LEO. (CIB at 119.) Tessera further argues that it is difficult to identify the source of the DRAM chip because they do not have uniform markings and do not sell the products under their brand names, which will make evasion of the LEO even more likely. (CIB at 119-120.)

Respondents argue that the risk of circumvention argued by Tessera is of its own making since Tessera made a strategic decision to not name known downstream manufacturers and that Tessera should not now be able to rely upon that decision as justification for the issuance of a GEO. (RRB at 56.) More specifically, Respondents argue that Tessera has failed to prove circumvention or evasion of a LEO is likely for the downstream products that Tessera is seeking to exclude especially since Tessera's own evidence shows that a majority of DRAM chips enter the U.S. as chips or modules and not in downstream products. (RRB at 58-59.) Rather, Tessera simply makes conclusory statements with little evidence to support its proposition. (RRB at 58-59.) Respondents argue that Tessera has failed to show that DRAM manufacturers who avoid paying a royalty to Tessera are a result of market incentives and that such an argument is not particularly relevant as to whether a GEO should issue. (RRB at 59.) Respondents further argue that Tessera's concern with "spin-off" corporations or the sale of manufacturing businesses is eliminated by Tessera's proposed language for the exclusion order, which includes language with successor liability. (RRB at 59-60.) Respondents further argue that it is not difficult to identify the manufacturer of the chips since the identity of the manufacturer is readily apparent on chips and modules and, for computers and servers, the manufacturer of the module are readily apparent upon removal of the computer casing. (RRB at 60-61.)

4. Conclusion

The ALJ finds that Tessera has failed to show that a general exclusion order is warranted should the Commission find a violation of Section 337. Tessera has failed to show that there is a widespread pattern of unauthorized use or that the source of the products is difficult to identify. Tessera has conceded that it knew and or learned of the identity of the downstream manufacturers but chose not to name them: "Tessera could not have named all of the downstream product manufacturers that incorporate Respondents' Accused Products. SMART sold products to more than [redacted] customers in 2007 alone, and Nanya, Elpida, and Kingston each have [redacted] of customers. The identities of Respondents' customers and the volumes of Respondents sales to them were determined only through discovery in this Investigation." (CRB at 68-69) (internal citations omitted). Furthermore, the evidence shows that while there is a widespread pattern of use of Tessera's patented technology, most of that use is authorized. (CX-06484C (Marcucci DWS) Q. 66; Marcucci, Tr. 1204:2 7; RX-12C (Corrected Malackowski DWS) Q. 90; Griffin, Tr. 1145:2-1146:8, CX-06488C (Griffin DWS)at Q. 114, Griffin, Tr. 1115:3-17; Griffin, Tr. 1106:24-1107:25, 1115:3-17.) Tessera argues that the percentages cited by Respondents are misleading and irrelevant and instead cite the actual number of imported unlicensed DRAMs. However, these numbers absent any context, *e.g.* the total number of imported DRAMs, is equally misleading and irrelevant and the ALJ finds it unpersuasive. Furthermore, the business conditions in the DRAM industry, on balance, weigh against a general exclusion order. Specifically, the latter three factors[20] weigh against the issuance of a general exclusion order. The evidence shows that the DRAM industry is a "capital intensive industry"

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[20] "(3) the cost for foreign entrepreneurs to build a facility that can produce the patented articles; (4) the number of foreign manufacturers whose facilities could be converted to manufacture the patented article; and (5) the foreign manufacturers' cost to convert a facility to produce the patented articles." *Magnets* at 6 (citing *Spray Pumps*).

that is unlikely to gain new entrants, especially given the current economic downturn in the DRAM market. (Kerr, Tr. 1349:5-19, 1424:10-18; RX-14C (Mulhern RWS) Q&A 81; CX-06489C (Kerr DWS) at Q&A 139.)

The Commission rejected similar arguments by Tessera in the 605 Investigation finding that Tessera "had not made a sufficient showing with respect to the difficulty of identifying the source of the infringing products." (Comm'n Op. at 68.) The Commission further noted that, as in this Investigation, Tessera was able to learn of the identities of the source of the allegedly infringing downstream products through discovery in the 605 Investigation, but chose not to amend the Complaint to add them and "[w]ithout more, Tessera has not established by this argument that it is difficult to identify the source of the infringing products." (*Id.* at 69.)

As for Tessera's arguments relating to the risk of circumvention of a limited exclusion order, the ALJ finds those arguments to be unpersuasive. The Commission considered similar arguments in the 605 Investigation and ultimately rejected those arguments. In the 605 Investigation, the Commission noted that the incorporation of the accused chips into downstream products outside of the United States was a pre-existing practice which could not serve as a basis for circumvention. (Comm'n Op. at 66-67.) In this investigation, the incorporation of Respondents' Accused Chip Packages was a pre-existing practice as well and, similarly, cannot serve as a basis for circumvention. The Commission also rejected Tessera's hypothetical arguments that Respondents could circumvent the limited exclusion order by "transferring" the incorporation of assemblies to their overseas customers and that Respondents could create joint ventures or spin-offs to avoid the order (Comm'n Op. at 67-68.) Those same arguments are rejected here. Thus, the ALJ finds that Tessera has failed to meet the heightened burden of showing that it is entitled to a general exclusion order. To the extent the ALJ finds that Tessera

is not entitled to a general exclusion order, the ALJ finds that it is not necessary to address Tessera's request for a "tailored" general exclusion order.

The ALJ recommends, however, that should Commission issue a general exclusion order, a certification provision should be included in the exclusion order. Neither Respondents nor Tessera disputes that such a certification provision. (CRB at 73; RRB at 64; SRB at 31.)

B. Limited Exclusion Order

Under Section 337(d), the Commission may issue either a limited or a general exclusion order. A limited exclusion order directed to respondents' infringing products is among the remedies that the Commission may impose, as is a general exclusion order that would apply to all infringing products, regardless of their manufacturer. *See* 19 U.S.C. § 1337(d).

Tessera requests that, should the Commission deny its request for general exclusion order, a limited exclusion order be issued that prohibits the importation of Respondents' Accused Packages, memory modules that incorporate the Accused packages, and computers, including desktops, notebooks, and servers that incorporate such memory modules. (CIB at 117.)

Respondents agree that should a limited exclusion order issue in this investigation, a self-administered certification program would be appropriate. (RRB at 64.)

The ALJ agrees that the evidence shows that, if a violation is found and the Commission decides not to issue a general exclusion order, a limited exclusion order would be proper. The limited exclusion order should apply to respondents Acer Inc.; Acer America Corp.; Centon Electronics, Inc.; Kingston Technology Corporation; Nanya Technology Corporation; Nanya Technology Corp. USA; Powerchip Semiconductor Corp.; ProMos Technologies, Inc.; Ramaxel Technology, Ltd; SMART Modular Technologies, Inc.; TwinMOS Technologies, Inc.; and TwinMOS Technologies, USA, Inc. and all of their affiliated companies, parents, subsidiaries, or

other related business entities, or their successors or assigns.[21] The ALJ further recommends that the limited exclusion order should apply to the Accused Chip Packages that come from unlicensed sources.[22] The ALJ further recommends that the Commission should include a certification provision in the exclusion order in order.

C. Downstream Products

The Commission may add "downstream products" to an exclusion order. Thus, products may be excluded from importation because they contain one or more accused devices. The Commission has held that in determining whether or not to exclude downstream products it will consider the so-called *EPROM* factors, set forth in *Erasable Programmable Read-Only Memories, Components Thereof Products Containing Such Memories, and Process for Making Such Memories*, Inv. No. 337-TA-276, USITC Pub. 2196, Comm'n Op. at 125-26 (May 1989) (*Aff'd sub nom., Hyundai Electronics Co. v. United States Int'l Trade Comm'n*, 899 F.2d 1204 (Fed. Cir. 1990).) The *EPROM* factors are:

(1) the value of the infringing articles compared to the value of the downstream products in which they are incorporated;

(2) the identity of the manufacturer of the downstream products, i.e., whether it can be determined that the downstream products are manufactured by the respondent or by a third party;

(3) the incremental value to complainant of the exclusion of downstream products;

(4) the incremental detriment to respondents of exclusion of such products;

(5) the burdens imposed on third parties resulting from exclusion of downstream products;

(6) the availability of alternative downstream products that do not contain the infringing articles;

[21] As noted *supra* in Section VI. B, the ALJ found that respondent Elpida's suppliers were licensed entities and that Elpida's products were licensed and, as such, not in violation of Section 337.

[22] For those Accused Chip Packages that are from licensed sources, the ALJ found that those products were not in violation of Section 337.

> (7) the likelihood that the downstream products actually contain the infringing articles and are thereby subject to exclusion;
>
> (8) the opportunity for evasion of an exclusion order that does not include downstream products; and
>
> (9) the enforceability of an order by Customs . . . .

Comm'n Op. at .125-26. These factors were not meant to be exclusive of other considerations, as "the Commission may identify and take into account any other factors which it believes bear on the question of whether to extend remedial exclusion to downstream products, and if so to what specific products." *Id.* The Commission may exclude downstream products even though not all of the factors weigh in favor of doing so. *See Id.* at 127 (excluding certain downstream products even though the value of the EPROMs relative to the downstream products was small).

While the Commission may exclude downstream products of named respondents in a limited exclusion order weighing the *EPROM* factors, the Commission may not exclude products of unnamed respondents unless the heightened requirements of a general exclusion order in §§ 337(d)(2)(A) or (B) are satisfied. *Kyocera Wireless Corp. v. ITC* ,. 545 F.3d 1340, 1358 (Fed. Cir. 2008) ("*Kyocera*"). In *Kyocera*, the Federal Circuit found that the Commission did not have the authority in a limited exclusion order to exclude the downstream products of unnamed respondents. *Id.* at 1355-58. Specifically, the Federal Circuit stated that the Commission's authority to exclude products in a limited exclusion order is limited to those products of the named respondents in the complaint. (*Id.* at 1356.) The Federal Circuit further explained that "[i]f a complainant wishes to obtain an exclusion order operative against articles of non-respondents, it must seek a GEO by satisfying the heightened burdens of §§ 1337(d)(2)(A) and (B)." (*Id.* at 1356.) Thus, a complainant may no longer exclude downstream products of non respondents in a limited exclusion order by simply satisfying the *EPROM* factors. Rather, in

order to exclude the downstream products of unnamed respondents, the complainant must meet the heightened requirements of a general exclusion order in order to exclude those products.

Tessera argues that the *EPROM* factors support the exclusion of downstream memory modules and computers. (CIB at 123.) Tessera argues that since a vast majority of the Accused Packaged Chips is imported into the U.S. after they are incorporated into downstream products, a downstream order is essential in order to gain effective relief. (CIB at 123-124.) Tessera argues that each of the *EPROM* factors weight in its favor: (1) it is undisputed that the Accused Packaged Chips are vital to downstream products into which they are incorporated as they could not function without the chip packages and they constitute a significant percentage of the monetary value of the downstream products; (2) it was impractical for Tessera to have named every actual infringer and that Tessera named manufacturers of the Accused Packaged Chips and the downstream projects, which was sufficient to protect the interests of others similarly situated; (3) the incremental value of the downstream exclusion order to Tessera and its licensees is significant since Tessera relies on revenues derived from royalties and license fees from those licensees that utilize Tessera's technology and, absent downstream relief, non-licensed manufacturers can undercut Tessera's licensees and downstream manufacturers can purchase and incorporate the lower cost unlicensed chip packages into their products prior to importation thereby avoiding having to pay Tessera; (4) the downstream order should have no adverse consequences to Respondents' business interests since Respondents can easily take a license from Tessera or purchase its chips from Tessera's licensees, of which there are numerous non-infringing sources, and need only provide CBP with a certification; (5) a downstream exclusion order will have a minimal impact on third parties as they can simply certify that their products are licensed, switch to licensed suppliers, ensure their suppliers are licensed, take a license

themselves, or use non-infringing technology; (6) non-infringing alternatives are available to third parties, including flip-chip technology; (7) it is undisputed that downstream products contain the infringing articles since the computer market has moved to DDR2 technology; (8) any remedy that did not include a general downstream order would not provide Tessera with any meaningful relief since a majority of the infringing chips are imported after incorporation into downstream products; and (9) CBP could easily enforce the downstream orders through a self-certification program covering the accused products and downstream products. (CIB at 123-133.) Tessera further argues that the Commission may also issue a "tailored" GEO "that excludes only downstream products incorporating the products of the named Respondents, rather than of all third parties." (CIB at 131, note 37.)

Respondents opposes Tessera's request for a "tailored" GEO as well as its attempts to exclude downstream products. (RRB at 54-55.) Respondents argue that Tessera seeks to exclude entire categories of downstream products for which no evidence was admitted. (RRB at 55.) Respondents further argue that in light of *Kyocera*, Tessera must meet the heightened burden of a general exclusion order in order to exclude the downstream products of non-respondents and that Tessera has failed to do so. (RRB at 64-65.) Nevertheless, Respondents argue that the *EPROM* factors do not warrant downstream relief against third parties since (1) the value of the alleged infringing element in the downstream product neither weigh in favor or against excluding downstream products because there are other available types of DRAM, the value of the DRAM varies depending on the downstream products and the cost to perform the one step in chip manufacturing covered by Tessera's patents is [redacted] (2) a majority of the downstream producers are not respondents and they are easily identifiable and finite in number; (3) more than 90% of DRAM supplies originates from licensed sources with a vast majority of

Respondents' imported products being licensed and Tessera's licensees' lost sales cannot be solely based on the availability of unlicensed products on the market; (4) the exclusion of downstream products will result in additional expenses for Respondents and loss of sales; (5) burden of complying with a certification program exists; (6) there is an absence of evidence on whether any unlicensed DRAM is found in downstream products and compliance programs instituted by Respondents Nanya, Acer and Powerchip make it unlikely that any unlicensed DRAM in downstream products will enter the U.S.; (7) the likelihood of evasion is low since nearly 90% of the DRAM supply is already licensed and the remaining supply would be covered by a limited exclusion order; and (8) there are significant difficulties in enforcing the order since it is still unclear what constitutes a product "produced under an active and applicable Tessera license" and the sheer volume of products subject to the order would be a burden for Customs. (RRB at 64-69.) Respondents do concede, however, that licensed products are available on the market.

Staff generally agrees with Tessera in its entirety as it relates to the individual analysis of the *EPROM* factors. (SIB at 100-104.) Staff notes however that while the accused chip packages are critical to the function of the electronic products, the percentage value for the chip package varies depending on the downstream product. (SIB at 100-101.) Staff further notes that while an analysis of the *EPROM* factors warrants an exclusion order that includes downstream products, an exclusion of all downstream products containing infringing packages would be overly broad and unduly burdensome. Staff argues that the exclusion order should encompass memory modules and desktop and laptop computers regardless of the source incorporating the packages and that *all* of the named Respondents downstream products should be excluded. (SIB at 104-105.)

As set forth *supra*, the ALJ found that Tessera had failed to meet its heightened burden of showing that a general exclusion order is warranted. (*See* I.A.4.) Consequently, in light of the *Kyocera*, Tessera has also failed to meet its burden of excluding the downstream products of non-respondents.

Nevertheless, in addition to failing to satisfy the *Spray Pump* factors for the issuance of a general exclusion order, Tessera has further failed to show that downstream products should be excluded in light of the *EPROM* factors.[23] For example, in addressing the fourth and fifth factors ("(4) the incremental detriment to respondents of exclusion of such products and (5) the burdens imposed on third parties resulting from exclusion of downstream products"), Tessera argues that those can easily be addressed by Respondents and third parties taking a license from Tessera. Tessera's arguments miss the point. Indeed, regardless of whether Respondents or the unnamed third parties choose to take a license from Tessera, the burden and detrimental impact of an exclusion order that includes downstream products can still be very real. Indeed, the evidence shows that should an exclusion order issue that included downstream products, Respondents will likely lose customers and sales and incur significant internal costs. (RX-14C (Mulhern DWS) at Q&A 134-135; JX 00667C; JX-006611C; JX-00691C; JX-0072C at 14-15, 48-49, 54-55.) Similarly, the burden on third parties will be significant – particularly the certification provision in light of Tessera's position regarding licensing. (*See supra* at VI.) This difficulty with the certification provision will similarly create issues for the CBP in the enforcement of the orders since it is still unclear what constitutes a product "produced under an active and applicable

[23] The *EPROMs* factors are used to determine whether a complainant is entitled to a limited exclusion order that includes downstream products. *Certain EPROM, EEPROM, Flash Memory, and Flash Microcontroller Semiconductor Devices and Products Containing Same*, Inv. No. 337-TA-395, USITC Pub. No. 3392, Comm'n Op. at 82 (October 16, 2000). In light of the Federal Circuit's recent decision in *Kyocera*, it is not clear whether the same *EPROMs* analysis should be performed when the complainant seeks a general exclusion order that seeks to exclude downstream products of third parties. Nevertheless, out of an abundance of caution, the ALJ has provided his analysis of the *EPROMs* factors.

Tessera license" since Tessera may withhold licensed status to products from a licensed source until some indefinite future date upon which Tessera has determined that royalties were paid. The first factor also does not weigh in Tessera's favor since there are other types of DRAM available on the market and the actual value of the DRAM varies depending on the downstream products, *e.g.* the value of DRAM in memory modules can be as high as 72.4% while only 7.5% for laptops. (CX-06489C at Q&A 109; CX-6890C).

While Tessera may benefit from a general exclusion order, it is not clear that incremental value of the exclusion of downstream products is as substantial as set forth by Tessera, especially in light of the fact that more than 90% of DRAM supplies originates from licensed sources with a vast majority of Respondents' imported products being licensed. Indeed, Tessera merely makes conclusory statements regarding the value of excluding downstream products, without citing to any specific value or benefit. (*See* CIB at 126-127.) Such statements are insufficient to justify the extreme measure of issuing a general exclusion order. While factors six and eight weigh slightly in Tessera's favor, the remaining factors do not tip the scales in Tessera's favor. Specifically, a majority of the downstream producers are not respondents and they are easily identifiable and finite in number and there is an absence of evidence on whether any unlicensed DRAM is found in downstream products, especially in light of compliance programs instituted by Respondents Nanya, Acer and Powerchip that make it unlikely that any unlicensed DRAM in downstream products will enter the U.S..

Therefore, the ALJ finds that Tessera has failed to meet its burden of showing that downstream products should be included in a general exclusion order should the Commission find a violation of Section 337 and determine to issue a general exclusion order.

D. Cease and Desist Order

Section 337 provides that in addition to, or in lieu of, the issuance of an exclusion order, the Commission may issue a cease and desist order as a remedy for violation of section 337. *See* 19 U.S.C. § 1337(f)(1). The Commission generally issues a cease and desist order directed to a domestic respondent when there is a "commercially significant" amount of infringing, imported product in the United States that could be sold so as to undercut the remedy provided by an exclusion order. *See Certain Crystalline Cefadroxil Monohydrate*, Inv. No. 337-TA-293, USITC Pub. 2391, Comm'n Op. on Remedy, the Public Interest and Bonding at 37-42 (June 1991); *Certain Condensers, Parts Thereof and Products Containing Same, Including Air Conditioners for Automobiles*, Inv. No. 337-TA-334, Comm'n Op. at 26-28 (Aug. 27, 1997).

Tessera requests a cease and desist order against respondents Acer, Centon, Kingston, Nanya, Elpida and SMART because each of these respondents maintain a significant inventory of infringing goods. (CIB at 133.) Staff agrees. (SIB at 105.)

Respondents argue that a cease and desist order is not necessitated because a "vast majority" of Accused Packaged Chips entering the U.S. are licensed and the turnover rate of DRAMs is so fast that there is no time to build a significant inquiry. (RRB at 70-71.) Respondents further argue that Tessera has failed to present any evidence that the Respondents actually do maintain a significant inventory of infringing DRAMs. (RRB at 71.)

The ALJ recommends that should the Commission find a violation a cease and desist order against respondents Acer, Centon, Kingston, Nanya, Elpida and SMART should be issued. The evidence shows that these respondents maintain a significant inventory of infringing goods. (CPFF XII 144-1482.) The fact that respondents may experience a high turnover rate does not render the Commission's cease and desist order preventing the respondents from selling the inventory meaningless. Rather, it would appear that since respondents do experience such a high

turnover rate, a cease and desist order is all the more appropriate and necessary to provide effective relief to Tessera.

E. Bond During Presidential Review Period

The Administrative Law Judge and the Commission must determine the amount of bond to be required of a respondent, pursuant to section 337(j)(3), during the 60-day Presidential review period following the issuance of permanent relief, in the event that the Commission determines to issue a remedy. The purpose of the bond is to protect the complainant from any injury. 19 C.F.R. § 210.42(a)(1)(ii), § 210.50(a)(3).

When reliable price information is available, the Commission has often set the bond by eliminating the differential between the domestic product and the imported, infringing product. *See Certain Microsphere Adhesives, Processes for Making Same, and Products Containing Same, Including Self-Stick Repositionable Notes*, Inv. No. 337-TA-366, Comm'n Op. a 24 (1995). In other cases, the Commission has turned to alternative approaches, especially when the level of a reasonable royalty rate could be ascertained. *See, e.g., Certain Integrated Circuit Telecommunication Chips and Products Containing Same, Including Dialing Apparatus*, Inv. No. 337-TA-337, Comm'n Op. at 41 (1995). A 100 percent bond has been required when no effective alternative existed. *See, e.g., Certain Flash Memory Circuits and Products Containing Same*, Inv. No. 337-TA-382, USITC Pub. No. 3046, Comm'n Op. at 26-27 (July 1997)(a 100% bond imposed when price comparison was not practical because the parties sold products at different levels of commerce, and the proposed royalty rate appeared to be *de minimis* and without adequate support in the record).

Tessera argues that a bond should be set in the amount of 100% of the entered value of any infringing import, which Tessera estimates to be $3.23 per infringing packaged 512 Mb

DRAM chip or the equivalent. The total amount of infringing megabits should be divided by 512 and then multiplied by $3.23. (CIB at 133-134.)

Respondents argue that the bond should be set at a reasonable royalty rate of 1%, which is supported by documentary evidence and expert testimony including Tessera's own expert. (RRB at 69-70.) Staff agrees arguing that Tessera has a record of royalties in its license agreement, which should be the measure for the bond. (SIB at 105-106.)

Should the Commission find a violation of Section 337, the ALJ recommends that a bond be set at a reasonable royalty rate as determined by Tessera's license agreements. The evidence shows that Tessera has a record of royalties as determined by its numerous license agreements and, as such, a bond of 100% is not necessary.

II. Conclusion

In accordance with the discussion of the issues contained herein, it is the RECOMMENDED DETERMINATION ("RD") of the Court that in the event the Commission finds a violation of section 337, a general exclusion order that includes downstream products is not warranted. To the extent the Commission determines to issue a general exclusion order, the ALJ recommends that the exclusion order include a certification provision. Should the Commission decide not to issue a general exclusion order, the Commission should issue limited exclusion order directed only to respondents Acer Inc.; Acer America Corp.; Centon Electronics, Inc.; Kingston Technology Corporation; Nanya Technology Corporation; Nanya Technology Corp. USA; Powerchip Semiconductor Corp.; ProMos Technologies, Inc.; Ramaxel Technology, Ltd; SMART Modular Technologies, Inc.; TwinMOS Technologies, Inc.; and TwinMOS Technologies, USA, Inc. and all of their affiliated companies, parents, subsidiaries, or other related business entities, or their successors or assigns. Should the Commission find a violation,

the Commission should also issue a cease and desist order directed toward the domestic respondents Acer, Centon, Kingston, Nanya, Elpida and SMART. Furthermore, if the Commission imposes a remedy following a finding of violation, Respondents should be required to post a bond set at a reasonable royalty rate as determined by Tessera's license agreements during the Presidential review period.

Within seven days of the date of this document, each party shall submit to the office of the Administrative Law Judge a statement as to whether or not it seeks to have any portion of this document deleted from the public version. The parties' submissions must be made by hard copy by the aforementioned date.

Any party seeking to have any portion of this document deleted from the public version thereof must submit to this office a copy of this document with red brackets indicating any portion asserted to contain confidential business information by the aforementioned date. The parties' submission concerning the public version of this document need not be filed with the Commission Secretary.

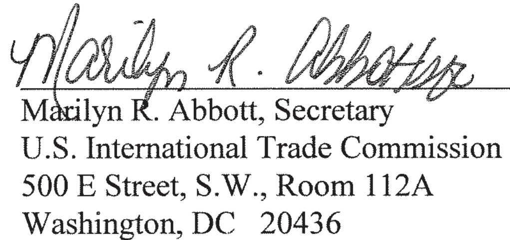
SO ORDERED.

Theodore R. Essex
Administrative Law Judge

IN THE MATTER OF CERTAIN SEMICONDUCTOR CHIPS WITH MINIMIZED CHIP PACKAGE SIZE AND PRODUCTS CONTAINING SAME (III) **337-TA-630**

PUBLIC CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the attached **INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND RECOMMENDED DETERMINATION ON REMEDY AND BONDING** has been served by hand upon, the Commission Investigative Attorney, **Kecia J. Reynolds, Esq.,** and the following parties as indicated on September 25, 2009.



Marilyn R. Abbott, Secretary
U.S. International Trade Commission
500 E Street, S.W., Room 112A
Washington, DC 20436

COMPLAINANT TESSERA, INC.

Tom M. Schaumberg, Esq.
ADDUCI, MASTRIANI, SCHAUMBERG, LLP
1200 Seventeenth St.. NW
Washington, DC 20036

( ) Via Hand Delivery
(X) Via Overnight Mail
( ) Via First Class Mail
( ) Other: __________

RESPONDENTS ACER, INC., ACER AMERICA CORPORATION, NANYA TECHNOLOGY CORPORATION, NANYA TECHNOLOGY CORPORATION U.S.A., AND POWERCHIP SEMICONDUCTOR CORPORATION

G. Hopkins Guy., Esq.
ORRICK, HERRINGTON & SUTCLIFFE, LLP
1000 Marsh Road
Menlo Park, CA 94025

( ) Via Hand Delivery
(X) Via Overnight Mail
( ) Via First Class Mail
( ) Other:___________

IN THE MATTER OF CERTAIN SEMICONDUCTOR CHIPS WITH MINIMIZED CHIP PACKAGE SIZE AND PRODUCTS CONTAINING SAME (III) **337-TA-630**

CERTIFICATE OF SERVICE- PAGE 2

RESPONDENTS ELPIDA MEMORY, INC. & ELPIDA MEMORY (USA) INC.

Larry L. Shatzer, Esq.	( ) Via Hand Delivery
FOLEY & LARDNER, LLP	(X) Via Overnight Mail
3000 K Street, N.W., Suite 500	( ) Via First Class Mail
Washington, DC 20007	( ) Other:__________

RESPONDENTS ProMOS TECHNOLOGIES, INC.:

ProMos Technologies, Inc.	( ) Via Hand Delivery
No.19, Li-Hsin Road	(X) Via Overnight Mail
Hsinchu Science Park	( ) Via First Class Mail
Hsinchu, Taiwan 30078	( ) Other:__________

RESPONDENT KINGSTON TECHNOLOGY CO., LTD.

Alan I. Unikel, Esq..	( ) Via Hand Delivery
SEYFARTH SHAW LLP	(X) Via Overnight Mail
131 South Dearborn Street, Ste. 2400	( ) Via First Class Mail
Chicago, IL 60603	( ) Other:__________

RESPONDENTS RAMAXEL TECHNOLOGY LTD.

Brian R. Nester, Esq.	( ) Via Hand Delivery
FISH & RICHARDSON P.C.	(X) Via Overnight Mail
1425 K Street, N.W., 11th Floor	( ) Via First Class Mail
Washington, DC 20005	( ) Other:__________

RESPONDENT CENTON ELECTRONICS, INC.

Joseph P. DiVincenzo, Esq.	( ) Via Hand Delivery
REMER, DIVINCENZO & GRIFFITH	(X) Via Overnight Mail
2121 E. Pacific Coast Highway, Suite 280	( ) Via First Class Mail
Corona Del Mar, CA 92625	( ) Other:__________

IN THE MATTER OF CERTAIN SEMICONDUCTOR CHIPS WITH MINIMIZED CHIP PACKAGE SIZE AND PRODUCTS CONTAINING SAME (III) **337-TA-630**

CERTIFICATE OF SERVICE- PAGE 3

RESPONDENT SMART MODULAR TECHNOLOGIES, INC.

Jonathan M. James, Esq. **PERKINS COIE BROWN & BAIN PA** 2901 N. Central Avenue, Suite 2000 Phoenix, AR 85012-2788	( ) Via Hand Delivery (X) Via Overnight Mail ( ) Via First Class Mail ( ) Other:___________

IN THE MATTER OF CERTAIN SEMICONDUCTOR CHIPS WITH MINIMIZED CHIP PACKAGE SIZE AND PRODUCTS CONTAINING SAME (III) **337-TA-630**

CERTIFICATE OF SERVICE- PAGE 4

PUBLIC MAILING LIST

Heather Hall
LEXIS - NEXIS
9443 Springboro Pike
Miamisburg, OH 45342

( ) Via Hand Delivery
(X) Via Overnight Mail
( ) Via First Class Mail
( ) Other:__________

Kenneth Clair
THOMSON WEST
1100 – 13th Street NW
Suite 200
Washington, DC 20005

( ) Via Hand Delivery
(X) Via Overnight Mail
( ) Via First Class Mail
( ) Other:__________

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C. 20436

In the Matter of **CERTAIN SEMICONDUCTOR CHIPS WITH MINIMIZED CHIP PACKAGE SIZE AND PRODUCTS CONTAINING SAME (III)**	**Investigation No. 337-TA-630**

NOTICE OF COMMISSION DETERMINATION TO REVIEW IN PART A FINAL INITIAL DETERMINATION FINDING NO VIOLATION OF SECTION 337; SCHEDULE FOR FILING WRITTEN SUBMISSIONS ON THE ISSUES UNDER REVIEW AND ON REMEDY, THE PUBLIC INTEREST AND BONDING

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has determined to review in part the final initial determination ("ID") issued by the presiding administrative law judge ("ALJ") on August 28, 2009, finding no violation of section 337 of the Tariff Act of 1930, 19 U.S.C. § 1337, in this investigation.

FOR FURTHER INFORMATION CONTACT: Panyin A. Hughes, Esq., Office of the General Counsel, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 205-3042. Copies of non-confidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 205-2000. General information concerning the Commission may also be obtained by accessing its Internet server (*http://www.usitc.gov*). The public record for this investigation may be viewed on the Commission's electronic docket (EDIS) at *http://edis.usitc.gov*. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on (202) 205-1810.

SUPPLEMENTARY INFORMATION: This investigation was instituted on January 14, 2008, based on a complaint filed by Tessera, Inc. of San Jose, California ("Tessera") on December 21, 2007, and supplemented on December 28, 2007. 73 *Fed. Reg.* 2276 (Jan. 14, 2008). The complaint alleges violations of section 337 of the Tariff Act of 1930 (19 U.S.C. § 1337) in the importation into the United States, the sale for importation, and the sale within the United States after importation of certain semiconductor chips with minimized chip package size or products containing same by reason of infringement of various claims of United States Patent Nos. 5,663,106 ("the '106 patent"); 5,679,977 ("the '977 patent"); 6,133,627 ("the '627 patent"); and 6,458,681 ("the '681 patent"). The complaint names eighteen respondents. Several

respondents were terminated from the investigation based on settlement agreements and consent orders. Two respondents defaulted. The following respondents remain in the investigation: Acer Inc. of Taipei, Taiwan; Acer America Corp. of San Jose, CA; Centon Electronics, Inc. of Aliso Viejo, CA; Elpida Memory, Inc. of Tokyo, Japan and Elpida Memory (USA), Inc. of Sunnyvale, CA (collectively, "Elpida"); Kingston Technology Co., Inc. of Fountain Valley, CA; Nanya Technology Corporation of Taoyuan, Taiwan; Nanya Technology Corp. USA; Powerchip Semiconductor Corporation of Hsinchu, Taiwan; ProMOS Technologies, Inc. of Hsinchu, Taiwan; Ramaxel Technology Ltd. of Hong Kong, China; and SMART Modular Technologies, Inc. of Fremont, CA. The '681 patent was terminated from the investigation prior to the hearing.

On August 28, 2009, the ALJ issued his final ID, finding no violation of Section 337 by Respondents with respect to any of the asserted claims of the asserted patents. Specifically, the ALJ found that the accused products do not infringe the asserted claims of the '106 patent. The ALJ also found that none of the cited references anticipate the asserted claims and that none of the cited references render the asserted claims obvious. The ALJ further found that the asserted claims of the '106 patent satisfy the requirement of 35 U.S.C. § 112, first, second and fourth paragraphs. Likewise, the ALJ found that the accused products do not infringe the asserted claims of the '977 and '627 patents and that none of the cited references anticipate the asserted claims of the patents. The ALJ further found that the asserted claims of the '977 and '627 patents satisfy the definiteness requirement of 35 U.S.C. § 112, second paragraph, and that Respondents waived their argument with respect to obviousness. The ALJ also found that all chips Respondents purchased from Tessera licensees were authorized to be sold by Tessera and, thus, Tessera's rights in those chips became subject to exhaustion, but that Respondents, except Elpida, did not purchase all their chips from Tessera licensees.

On September 17, 2009, Tessera and the Commission investigative attorney filed petitions for review of the ID. That same day, Respondents filed contingent petitions for review of the ID. On October 1, 2009, the parties filed responses to the various petitions and contingent petitions for review.

Having examined the record of this investigation, including the ALJ's final ID, the petitions for review, and the responses thereto, the Commission has determined to review the final ID in part. Specifically, the Commission has determined to review (1) the finding that the claim term "top layer" recited in claim 1 of the '106 patent means "an outer layer of the chip assembly upon which the terminals are fixed," the requirement that "the 'top layer' is a single layer," and the effect of the findings on the infringement analysis, invalidity analysis and domestic industry analysis; (2) the finding that the claim term "thereon" recited in claim 1 of the '106 patent requires "disposing the terminals on the top surface of the top layer," and its effect on the infringement analysis, invalidity analysis and domestic industry analysis; (3) the finding that the Direct Loading testing methodology employed by Tessera's expert to prove infringement is unreliable; and (4) the finding that the 1989 Motorola OMPAC 68-pin chip package fails to anticipate claims 17 and 18 of the '977 patent. The Commission has determined not to review the remaining issues raised by the petitions for review.

The parties are requested to brief their positions on the issues under review with reference to the applicable law and the evidentiary record. In connection with its review, the Commission is particularly interested in responses to the following questions:

1. Would the accused products infringe the asserted claims of the '106 patent if construction of the claim term "top layer" does not encompass only a single layer? Please cite record evidence and/or relevant legal precedent to support your position.

2. Did the patentees of the '106 patent expressly disclaim the embodiment described in Figure 7 of United States Patent No. 5,148, 265 ("the '265 patent")? How would that affect the infringement analysis of the asserted claims of the '106 patent? *See* '106 Patent Prosecution History (JX-167) June 24, 1996, Office Action and December 24, 1996, Amendment; '265 patent (JX-2) at column 14, lines 19-34; FIG. 7. Please cite record evidence and relevant legal authority to support your position.

3. Does Dr. Qu state anywhere in the record that he relied on his direct loading testing methodology to independently prove infringement of the asserted claims of the '977 and '627 patents by the accused packages? Please cite only record evidence.

4. Was Dr. Qu's demonstrated stress relief in the solder balls of the accused packages due to terminal-to-chip displacement caused by the applied external load? Please cite only record evidence.

In connection with the final disposition of this investigation, the Commission may (1) issue an order that could result in the exclusion of the subject articles from entry into the United States, and/or (2) issue one or more cease and desist orders that could result in the respondent(s) being required to cease and desist from engaging in unfair acts in the importation and sale of such articles. Accordingly, the Commission is interested in receiving written submissions that address the form of remedy, if any, that should be ordered. If a party seeks exclusion of an article from entry into the United States for purposes other than entry for consumption, the party should so indicate and provide information establishing that activities involving other types of entry either are adversely affecting it or likely to do so. For background, *see In the Matter of Certain Devices for Connecting Computers via Telephone Lines*, Inv. No. 337-TA-360, USITC Pub. No. 2843 (December 1994) (Commission Opinion).

If the Commission contemplates some form of remedy, it must consider the effects of that remedy upon the public interest. The factors the Commission will consider include the effect that an exclusion order and/or cease and desist orders would have on (1) the public health and welfare, (2) competitive conditions in the U.S. economy, (3) U.S. production of articles that are like or directly competitive with those that are subject to investigation, and (4) U.S. consumers.

The Commission is therefore interested in receiving written submissions that address the aforementioned public interest factors in the context of this investigation.

If the Commission orders some form of remedy, the U.S. Trade Representative, as delegated by the President, has 60 days to approve or disapprove the Commission's action. *See* Presidential Memorandum of July 21, 2005, 70 *Fed. Reg.* 43251 (July 26, 2005). During this period, the subject articles would be entitled to enter the United States under bond, in an amount determined by the Commission. The Commission is therefore interested in receiving submissions concerning the amount of the bond that should be imposed if a remedy is ordered.

WRITTEN SUBMISSIONS: The parties to the investigation are requested to file written submissions on the issues identified in this notice. Parties to the investigation, interested government agencies, and any other interested parties are encouraged to file written submissions on the issues of remedy, the public interest, and bonding. Such submissions should address the recommended determination by the ALJ on remedy and bonding. Complainants and the IA are also requested to submit proposed remedial orders for the Commission's consideration. Complainants are also requested to state the dates that the patents expire and the HTSUS numbers under which the accused products are imported. The written submissions and proposed remedial orders must be filed no later than close of business on Friday, November 13, 2009. Reply submissions must be filed no later than the close of business on Friday, November 20, 2009. No further submissions on these issues will be permitted unless otherwise ordered by the Commission.

Persons filing written submissions must file the original document and 12 true copies thereof on or before the deadlines stated above with the Office of the Secretary. Any person desiring to submit a document to the Commission in confidence must request confidential treatment unless the information has already been granted such treatment during the proceedings. All such requests should be directed to the Secretary of the Commission and must include a full statement of the reasons why the Commission should grant such treatment. *See* 19 C.F.R. § 210.6. Documents for which confidential treatment by the Commission is sought will be treated accordingly. All nonconfidential written submissions will be available for public inspection at the Office of the Secretary.

The authority for the Commission's determination is contained in section 337 of the Tariff Act of 1930, as amended (19 U.S.C. § 1337), and in sections 210.42-46 and 210.50 of the Commission's Rules of Practice and Procedure (19 C.F.R. §§ 210.42-46 and 210.50).

By order of the Commission.

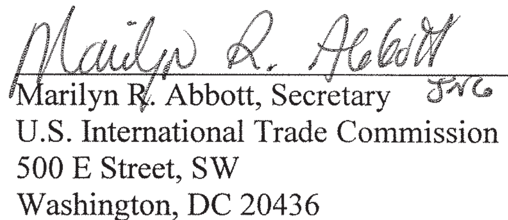
Marilyn R. Abbott
Secretary to the Commission

Issued: **October 30, 2009**

CERTAIN SEMICONDUCTOR CHIPS WITH MINIMIZED CHIP PACKAGE SIZE AND PRODUCTS CONTAINING SAME (III) **337-TA-630**

PUBLIC CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the attached **NOTICE OF COMMISSION DETERMINATION TO REVIEW IN PART A FINAL INITIAL DETERMINATION FINDING NO VIOLATION OF SECTION 337; SCHEDULE FOR FILING WRITTEN SUBMISSIONS ON THE ISSUES UNDER REVIEW AND ON REMEDY, THE PUBLIC INTEREST AND BONDING** has been served by hand upon the Commission Investigative Attorney, Kecia J. Reynolds, Esq., and the following parties as indicated, on October 30, 2009.



Marilyn R. Abbott, Secretary
U.S. International Trade Commission
500 E Street, SW
Washington, DC 20436

On Behalf Of Complainant Tessera Incorporated:

Tom M. Schaumberg, Esq.
ADDUCI, MASTRIANI, SCHAUMBERG, LLP
1200 Seventeenth St., NW
Washington, DC 20036

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: ________

On Behalf Of Respondents Acer, Incorporated, Acer America Corporation, Nanya Technology Corporation, Nanya Technology Corporation USA, And Powerchip Semiconductor Corporation:

G. Hopkins Guy, Esq.
ORRICK HERRINGTON & SUTCLIFFE LLP
1000 Marsh Road
Menlo Park, CA 94025-1015

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: ________

On Behalf Of Respondents Kingston Technology Co., Incorporated:

Alan L. Unikel, Esq.
SEYFARTH SHAW LLP
131 South Dearborn Street, Suite 2400
Chicago, IL 60603

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: _________

On Behalf Of Respondents Elpida Memory Inc., And Elpida Memory (USA) Incorporated:

Larry L. Shatzer, Esq.
FOLEY & LARDNER LLP
Washington Harbour
3000 K Street, NW
Suite 550
Washington, DC 20007-5143

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: _________

On Behalf Of Respondent Smart Modular Technologies, Incorporated:

Jonathan M. James, Esq.
PERKINS COIE
2901 N. Central Avenue, Suite 2000
Phoenix, AZ 85012-2788

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: _________

On Behalf Of Respondent Centon Electronics, Incorporated:

Joseph P. DiVincenzo, Esq.
REMER DIVINCENZO & GRIFFITH
2121 E. Pacific Coast Highway, Suite 280
Corona Del Mar, CA 92625

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: _________

On Behalf Of Respondent Ramaxel Technology Ltd.:

Brian R. Nester, Esq.
FISH & RICHARDSON PC
1425 K Street, NW, 11th Floor
Washington, DC 20005

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: _________

On Behalf Of Respondent Promos Technologies Inc.:

Charles F. Gormly, Esq.
5101 Wisconsin Avenue NW, Suite 210
Washington, DC 20016

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: _________

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C. 20436

In the Matter of

CERTAIN SEMICONDUCTOR CHIPS WITH MINIMIZED CHIP PACKAGE SIZE AND PRODUCTS CONTAINING SAME (III)

Investigation No. 337-TA-630

NOTICE OF COMMISSION DETERMINATION NOT TO REVIEW AN INITIAL DETERMINATION FINDING TWO RESPONDENTS IN DEFAULT

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has determined not to review the presiding administrative law judge's ("ALJ") initial determination ("ID") (Order No. 46) in this investigation finding respondents TwinMOS Technologies Inc. and TwinMOS Technologies USA Inc. in default.

FOR FURTHER INFORMATION CONTACT: Panyin A. Hughes, Office of the General Counsel, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 205-3042. Copies of non-confidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 205-2000. General information concerning the Commission may also be obtained by accessing its Internet server (*http://www.usitc.gov*). The public record for this investigation may be viewed on the Commission's electronic docket (EDIS) at *http://edis.usitc.gov*. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on (202) 205-1810.

SUPPLEMENTARY INFORMATION: This investigation was instituted on January 14, 2008, based on a complaint filed by Tessera, Inc. of San Jose, California ("Tessera") on December 21, 2007, and supplemented on December 28, 2007. 73 *Fed. Reg.* 2276 (January 14, 2008). The complaint alleges violations of section 337 of the Tariff Act of 1930 (19 U.S.C. § 1337) in the importation into the United States, the sale for importation, and the sale within the United States after importation of certain semiconductor chips with minimized chip package size or products containing same by reason of infringement of various claims of United States Patent Nos. 5,663,106; 5,679,977; 6,133,627; and 6,458,681. The complaint names eighteen respondents.

On February 19, 2008, Tessera filed a motion for an order to show cause and default against two respondents: TwinMOS Technologies Inc. and TwinMOS Technologies USA Inc. (collectively "TwinMOS"). On March 12, 2008, the ALJ issued Order No. 12 ordering those respondents to show cause why they should not be found in default for failing to respond to the complaint and notice of investigation.

On August 28, 2009, the ALJ issued the subject ID finding TwinMOS in default. No petitions for review of this ID were filed. The Commission has determined not to review the ID.

The authority for the Commission's determination is contained in section 337 of the Tariff Act of 1930, as amended (19 U.S.C. § 1337), and in section 210.42 of the Commission's Rules of Practice and Procedure (19 C.F.R. § 210.42).

By order of the Commission.

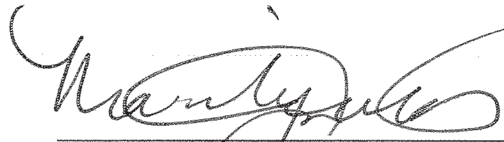
Marilyn R. Abbott
Secretary to the Commission

Issued: September 15, 2009

CERTAIN SEMICONDUCTOR CHIPS WITH MINIMIZED CHIP PACKAGE SIZE AND PRODUCTS CONTAINING SAME (III) **337-TA-630**

PUBLIC CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the attached **NOTICE OF COMMISSION DETERMINATION NOT TO REVIEW AN INITIAL DETERMINATION FINDING TWO RESPONDENTS IN DEFAULT** has been served by hand upon the Commission Investigative Attorney, Kecia J. Reynolds, Esq., and the following parties as indicated, on September 15, 2009.



Marilyn R. Abbott, Secretary
U.S. International Trade Commission
500 E Street, SW
Washington, DC 20436

ON BEHALF OF COMPLAINANT TESSERA INCORPORATED:

Mark N. Reiter, Esq.
GIBSON DUNN CRUTCHER LLP
2100 McKinney Avenue, Suite 1100
Dallas, TX 75201

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: ________

ON BEHALF OF RESPONDENTS ACER, INCORPORATED, ACER AMERICA CORPORATION, NANYA TECHNOLOGY CORPORATION, NANYA TECHNOLOGY CORPORATION USA, AND POWERCHIP SEMICONDUCTOR CORPORATION:

G. Hopkins Guy, III, Esq.
ORRICK HERRINGTON & SUTCLIFFE LLP
1000 Marsh Road
Menlo Park, CA 94025-1015

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: ________

ON BEHALF OF RESPONDENTS KINGSTON TECHNOLOGY CO., INCORPORATED AND ProMOS TECHNOLOGIES, INCORPORATED:

Alan L. Unikel, Esq.
SEYFARTH SHAW LLP
131 South Dearborn Street, Suite 2400
Chicago, IL 60603

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: ________

ON BEHALF OF RESPONDENTS ELPIDA MEMORY INC., AND ELPIDA MEMORY (USA) INCORPORATED:

Larry L. Shatzer, Esq.
FOLEY & LARDNER LLP
Washington Harbour
3000 K Street, NW
Suite 550
Washington, DC 20007-5143

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: ________

ON BEHALF OF RESPONDENT SMART MODULAR TECHNOLOGIES, INCORPORATED:

Jonathan M. James, Esq.
PERKINS COIE
2901 N. Central Avenue, Suite 2000
Phoenix, AZ 85012-2788

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: ________

ON BEHALF OF RESPONDENT CENTON ELECTRONICS, INCORPORATED:

Joseph P. DiVincenzo, Esq.
REMER DIVINCENZO & GRIFFITH
2121 E. Pacific Coast Highway, Suite 280
Corona Del Mar, CA 92625

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: ________

ON BEHALF OF RESPONDENT RAMAXEL TECHNOLOGY LTD.:

Brian R. Nester, Esq.
FISH & RICHARDSON PC
1425 K Street, NW, 11th Floor
Washington, DC 20005

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: ________

ON BEHALF OF RESPONDENTS PERIPERAL DEVICES AND PRODUCTS SYSTEMS, INC. D/B/A PATRIOT MEMORY:

John V. Picone, III, Esq.

( ) Via Hand Delivery

HOPKINS & CARLEY
A Law Corporation
70 South First Street
San Jose, CA 95113

( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: _________

<u>RESPONDENTS:</u>

TwinMOS Technologies, Inc.
No. 3, Tzu Chiang Road
Hsin-Chu Industrial District, Hu Kou Xiang
Hsin-Chu,
Taiwan 303

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: _________

TwinMOS Technologies USA, Inc.
1649 S. Main Street, Suite 105
Milpitas, CA 95035

( ) Via Hand Delivery
( ) Via Overnight Mail
(✓) Via First Class Mail
( ) Other: _________