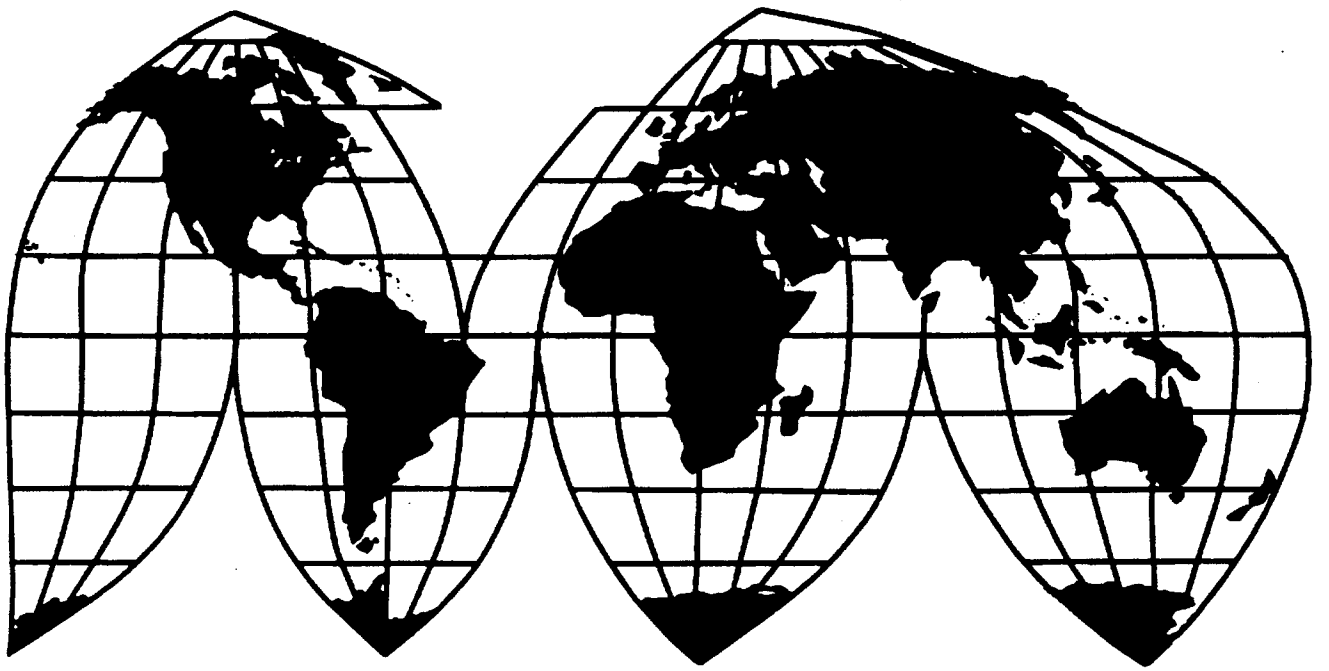
In the Matter of
Certain Integrated Circuits, Processes for Making Same, and Products Containing Same

Investigation No. 337-TA-450

Publication 3624 **August 2003**

U.S. International Trade Commission



Washington, DC 20436

U.S. International Trade Commission

COMMISSIONERS

Deanna Tanner Okun, Chairman
Jennifer A. Hillman, Vice Chairman
Marcia E. Miller
Stephen Koplan

Address all communications to
Secretary to the Commission
United States International Trade Commission
Washington, DC 20436

U.S. International Trade Commission

Washington, DC 20436
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In the Matter of
Certain Integrated Circuits, Processes for Making Same, and Products Containing Same

Investigation No. 337-TA-450

Publication 3624

August 2003

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	Inv. No. 337-TA-450
CERTAIN INTEGRATED CIRCUITS, PROCESSES FOR MAKING SAME, AND PRODUCTS CONTAINING SAME	

NOTICE OF RESCISSION OF LIMITED EXCLUSION ORDER AND VACATUR OF ADMINISTRATIVE LAW JUDGE ORDER NO. 5

AGENCY: U.S. International Trade Commission.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has rescinded the limited exclusion order issued on October 8, 2002, at the conclusion of the above-captioned investigation, and vacated Administrative Law Judge ("ALJ") Order No. 5.

FOR FURTHER INFORMATION CONTACT: David I. Wilson, Esq., Office of the General Counsel, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone 202-708-2310. Copies of the Commission Order and all other nonconfidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone 202-205-2000. General information concerning the Commission may also be obtained by accessing its Internet server at http://www.usitc.gov. The public record for this investigation may be viewed on the Commission's electronic docket (EDIS-ON-LINE) at http://edis.usitc.gov. Hearing-impaired persons are advised that information on the matter can be obtained by contacting the Commission's TDD terminal on 202-205-1810.

SUPPLEMENTARY INFORMATION: On March 6, 2001, the Commission voted to instituted this investigation, which concerned allegations of unfair acts in violation of section 337 of the Tariff Act of 1930, 19 U.S.C. § 1337, in the importation and sale of certain integrated circuits, processes for making same, and products containing same. 66 *Fed. Reg.* 13,567 (Mar. 6, 2001). On October 8, 2002, the Commission found a violation of section 337 in the unlawful importation and sale by respondents Silicon Integrated Systems Corp. of Taiwan and Silicon Integrated Systems Corp. of the United States (collectively "respondents") of certain integrated circuits, and certain products containing same, made by a process covered by claim 13 of U.S. Patent No. 6,117,345, owned by complainants United Microelectronics Corp., UMC Group (USA), and United Foundry Service, Inc. (collectively "complainants").

On March 13, 2003, complainants and respondents filed a joint petition to rescind the limited exclusion order under Commission rule 210.76(a)(1), 19 C.F.R. §210.76(a)(1), on the basis of a settlement agreement they had reached. Complainants and respondents asserted that their settlement agreement constituted "changed conditions of fact or law" sufficient to justify rescission of the order

under Commission rule 210.76(a)(1). Complainants and respondents also sought in their joint petition to have the Commission vacate Administrative Law Judge ("ALJ") Order No. 5, which restricted the patent prosecution activities of William H. Wright of Hogan & Hartson, counsel for complainants, and other patent practioners at Hogan & Hartson, who had subscribed to the administrative protective order. ALJ Order No. 5 had been entered at the request of respondents.

This action is taken under the authority of section 337 of the Tariff Act of 1930, 19 U.S.C. § 1337, and section 210.76(a)(1) of the Commission's Rules of Practice and Procedure, 19 C.F.R. § 210.76(a)(1).

By order of the Commission.

Marilyn R. Abbott
Secretary to the Commission

Issued: April 23, 2003

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of CERTAIN INTEGRATED CIRCUITS, PROCESSES FOR MAKING SAME, AND PRODUCTS CONTAINING SAME	Inv. No. 337-TA-450

ORDER

On October 8, 2002, the Commission found a violation of section 337 of the Tariff Act of 1930 (19 U.S.C. §1337), as amended, in the unlawful importation and sale by respondents Silicon Integrated Systems Corp. of Taiwan and Silicon Integrated Systems Corp. of the United States (collectively "respondents") of certain integrated circuits, and certain products containing same, made by a process covered by claim 13 of U. S. Patent No. 6,117,345, owned by complainants United Microelectronics Corp., UMC Group (USA), and United Foundry Service, Inc. (collectively "complainants").

On March 13, 2003, complainants and respondents filed a joint petition to rescind the limited exclusion order under Commission rule 210.76(a)(1), 19 C.F.R. § 210.76(a)(1), on the basis of their settlement agreement. Complainants and respondents asserted that the settlement agreement constituted "changed conditions of fact or law" sufficient to justify rescission of the limited exclusion order under Commission rule 210.76(a)(1).

Complainants and respondents also sought in their joint petition to have the Commission vacate Administrative Law Judge ("ALJ") Order No. 5, which restricts the patent prosecution activities of William H. Wright of Hogan & Hartson, counsel for complainants, and other patent practioners at Hogan & Hartson, who had subscribed to the administrative protective order. ALJ Order No. 5 had been imposed at the request of respondents.

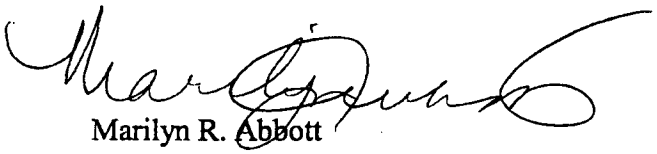
Having reviewed the parties' submissions, the Commission finds that the petition and settlement agreement of complainants and respondents satisfies the requirements for rescinding the limited exclusion order under Commission rule 210.76(a)(1). The Commission also finds that the restrictions ordered by ALJ Order No. 5 are no longer necessary in view of the current business relationship between complainants and respondents and because the restrictions were imposed at respondents' request. Accordingly, it is HEREBY ORDERED THAT:

1. The limited exclusion order issued on October 8, 2002 in this investigation is rescinded;

2. ALJ Order No. 5 is vacated; and

3. The Secretary shall serve copies of this Commission Order upon each party of record to this investigation and publish notice thereof in the Federal Register.

By Order of the Commission.



Marilyn R. Abbott
Secretary to the Commission

Issued: April 23, 2003

CERTAIN INTEGRATED CIRCUITS, PROCESSES FOR MAKING SAME, AND PRODUCTS CONTAINING SAME **337-TA-450**

CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the **Notice Of Rescission of Limited Exclusion Order and Vacatur of Administrative Law Judge Order. No. 5,** was served upon the following parties via first class mail and air mail where necessary, on **April 23, 2003.**

Marilyn R. Abbott, Secretary
U.S. International Trade Commission
500 E Street, SW - Room 112
Washington, DC 20436

ON BEHALF OF COMPLAINANT UNITED MICROELECTRONICS CORPORATION, UMC GROUP AND UNITED FOUNDRY SERVICE, INCORPORATED:

Steven J. Routh, Esq.
Hogan and Hartson
555 13th Street, NW
Washington, DC 20004

William H. Wright, Esq.
Biltmore Tower
Hogan and Hartson
500 S. Grand Avenue
Suite 1900
Los Angeles, CA 90071

ON BEHALF OF SILICON INTEGRATED SYSTEMS CORPORATION:

Tom M. Schaumberg, Esq.
Adduci, Mastriani and Schaumberg, LLP
1200 Seventeenth Street, NW
Fifth Floor
Washington, DC 20036

Kirk R. Ruthenberg, Esq.
Sonnenschein Nath and Rosenthal
1301 K Street, NW
Suite 600, East Tower
Washington, DC 20005

Edward H. Rice, Esq.
Sonnenschein Nath and Rosenthal
8000 Sears Tower
Chicago, IL 60606

Michael A. Molano, Esq.
Sonnenschein Nath and Rosenthal
685 Market Street, 6th Floor
San Francisco, CA 94105

ON BEHALF OF THE COMMISSION:

Shival P. Virmani, Esq.
Commission Investigative Attorney
Office of Unfair Import Investigation
500 E Street, SW - Room 401-J
Washington, DC 20436

James B. Coughlan, Esq.
Commission Investigative Attorney
Office of Unfair Import Investigations
500 E Street, SW - Room 401-L
Washington, DC 20436

Timothy Monaghan, Esq.
Advisory Attorney
Office of General Counsel
500 E Street, SW - Room 707-U
Washington, DC 20436

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C. 20436

In the Matter of	
CERTAIN INTEGRATED CIRCUITS, PROCESSES FOR MAKING SAME, AND PRODUCTS CONTAINING SAME	Inv. No. 337-TA-450

CONFIDENTIAL INFORMATION DELETED

ORDER

The Commission instituted this investigation by notice published in the *Federal Register* on March 6, 2001. The complainants are United Microelectronics Corporation, Hsinchu City, Taiwan; UMC Group (USA), Sunnyvale, CA; and United Foundry Service, Inc., Hopewell Junction, NY. The Commission named two respondents, Silicon Integrated Systems Corp., Hsinchu City, Taiwan, and Silicon Integrated Systems Corporation, Sunnyvale, CA (collectively, "SiS"). The complaint, as supplemented, alleged violations of section 337 in the importation, the sale for importation, and the sale within the United States after importation of certain integrated circuits and products containing same by reason of infringement of certain claims of U.S. Patent No. 5,559,352 and claims 1, 3-16, and 19-21 of U.S. Patent No. 6,117,345 ("the '345 patent").

Following an evidentiary hearing, the presiding administrative law judge (ALJ) issued his final ID on May 6, 2002, concluding that there was no violation of section 337 of the Tariff Act of 1930 (19 U.S.C. § 1337). The ALJ found, *inter alia*, that each of the '345 patent claims listed in the notice of investigation, including claim 13, is invalid as anticipated by and made obvious by certain prior art. On June 21, 2002, the Commission determined to review the ID in part. On October 7, 2002, the Commission determined that there is a violation of section 337 as to claim 13 of the '345 patent, but no violation of the statute as to the remaining claims in issue of the '345 patent and no violation as to the claims in issue of the '352 patent. On the same day, the Commission issued its opinion supporting its final determination and also issued a limited exclusion order.

PUBLIC VERSION

CONFIDENTIAL INFORMATION DELETED

On October 25, 2002, respondents filed a petition for reconsideration[1] pursuant to Commission rule 210.47, requesting that the Commission reconsider its October 7, 2002, final determination. Respondents' petition characterizes the Commission's final determination as rejecting their argument that U.S. Patent No. 5,580,701 ("the '701 patent) "provided alternative evidence for supporting the ALJ's determination that one skilled in the art would know to use [[ ]] to form the cap layer of claim 13." Petition at 1 (citing Commission opinion at 32, 54-55), 5. Respondents assert that the Commission's final determination raises the new question of whether the Commission can refuse to consider "record evidence that provides alternative support for an ALJ's determination." Petition at 3. Complainants and the Commission investigative attorney ("IA") opposed the petition.

In the "Background" section of their petition, respondents state that they argued in their opposition to the petitions for review of the ALJ's ID filed by complainants and the IA that the '701 patent provided additional evidentiary support for their argument that a person of ordinary skill in the art would know to use [[ ]] to form the cap layer of claim 13. Petition at 2 (citing Respondents' Opposition to Complainants' and OUII's Petitions for Review at 25-26). Respondents further state that in their initial and response briefs to the Commission on review, they cited the '701 patent as additional record evidence supporting their arguments that claim 13 is obvious. Petition at 3 (citing respondents' brief at 28-34 and respondents' reply brief at 55-56).

Complainants' response put respondents on notice that the Commission might reject arguments that had not been presented to the ALJ. Complainants' brief at 93 n.44 (arguing that '701 patent argument raised in Respondents' Opposition to Complainants' and OUII's Petitions for Review was "misplaced" because, *inter alia*, "this argument was not raised before or considered by the ALJ"). Respondents therefore could have presented their current arguments concerning what they have identified in their petition for reconsideration as a "new question" in their earlier reply brief,[2] before the Commission ever made its final determination. Consequently, respondents' petition for reconsideration is not directed toward "new questions" upon which respondents "had no opportunity to submit arguments" as required by Commission rule 210.47, and the petition must therefore be denied.

Therefore, having examined the record in this investigation, including respondents' petition pursuant to rule 210.47 for reconsideration of the Commission's October 7, 2002, final

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[1] Respondents' Motion for Reconsideration (filed October 25, 2002).

[2] Respondents in fact made some of those arguments, and the Commission rejected them. Commission opinion at 32.

determination, and the responses thereto, it is hereby ORDERED THAT:

1. Respondents' petition for reconsideration is denied.
2. The Secretary shall serve copies of this Order on all parties of record.

By order of the Commission.

Marilyn R. Abbott
Secretary to the Commission

Issued: January 7, 2003

PUBLIC VERSION

CERTAIN INTEGRATED CIRCUITS, PROCESSES FOR MAKING SAME, AND PRODUCTS CONTAINING SAME **337-TA-450**

CONFIDENTIAL CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the attached **CONFIDENTIAL ORDER**, was served upon the following parties via first class mail and air mail where necessary, on **January 7, 2003.**

Marilyn R. Abbott, Secretary
U.S. International Trade Commission
500 E Street, SW - Room 112
Washington, DC 20436

ON BEHALF OF COMPLAINANT UNITED MICROELECTRONICS CORPORATION, UMC GROUP AND UNITED FOUNDRY SERVICE, INCORPORATED:

Steven J. Routh, Esq.
Mark S. McConnell, Esq.
David A. Kikel, Esq.
Sten A. Jensen, Esq.
Hogan and Hartson
555 13th Street, NW
Washington, DC 20004

William H. Wright, Esq.
Biltmore Tower
Hogan and Hartson
500 S. Grand Avenue
Suite 1900
Los Angeles, CA 90071

ON BEHALF OF SILICON INTEGRATED SYSTEMS CORPORATION:

Tom M. Schaumberg, Esq.
Adduci, Mastriani and Schaumberg, LLP
1200 Seventeenth Street, NW
Fifth Floor
Washington, DC 20036

Kirk R. Ruthenberg, Esq.
Sonnenschein Nath and Rosenthal
1301 K Street, NW
Suite 600, East Tower
Washington, DC 20005

Edward H. Rice, Esq.
Sonnenschein Nath and Rosenthal

8000 Sears Tower
233 South Wacker Drive
Chicago, IL 60606
Michael A. Molano, Esq.
Sonnenschein Nath and Rosenthal
685 Market Street - 6th Floor
San Francisco, CA 04105

ON BEHALF OF THE COMMISSION:

Shival P. Virmani, Esq.
Commission Investigative Attorney
Office of Unfair Import Investigation
500 E Street, SW - Room 401-J
Washington, DC 20436

James B. Coughlan, Esq.
Commission Investigative Attorney
Office of Unfair Import Investigations
500 E Street, SW - Room 401-L
Washington, DC 20436

Clara Kuehn, Esq.
Advisory Attorney
Office of General Counsel
500 E Street, SW - Room 707-T
Washington, DC 20436

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C. 20436

In the Matter of	)	
CERTAIN INTEGRATED CIRCUITS, PROCESSES FOR MAKING SAME, AND PRODUCTS CONTAINING SAME	)	Inv. No. 337-TA-450

NOTICE OF FINAL DETERMINATION AND ISSUANCE OF LIMITED EXCLUSION ORDER

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has found a violation of section 337 of the Tariff Act of 1930 (19 U.S.C. § 1337) as to one claim of one patent and has issued a limited exclusion order in the above-captioned investigation.

FOR FURTHER INFORMATION CONTACT: Clara Kuehn, Esq., Office of the General Counsel, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 205-3012. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on 202-205-1810. General information concerning the Commission may also be obtained by accessing its Internet server (*http://www.usitc.gov*).Copies of the Commission order, the Commission opinion in support thereof, and all nonconfidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone 202-205-2000.

SUPPLEMENTARY INFORMATION: The Commission instituted this investigation by notice published in the *Federal Register* on March 6, 2001. 66 *Fed. Reg.* 13567 (2001). The complainants were United Microelectronics Corporation, Hsinchu City, Taiwan; UMC Group (USA), Sunnyvale, CA; and United Foundry Service, Inc., Hopewell Junction, NY. *Id.* The Commission named two respondents, Silicon Integrated Systems Corp., Hsinchu City, Taiwan, and Silicon Integrated Systems Corporation, Sunnyvale, CA (collectively, "SiS"). *Id.* The complaint, as supplemented, alleged violations of section 337 in the importation, the sale for importation, and the sale within the United States after importation of certain integrated circuits and products containing same by reason of infringement of claims 1, 2, and 8 of U.S. Letters Patent 5,559,352 ("the '352 patent") and claims 1, 3-16, and 19-21 of U.S. Letters Patent 6,117,345 ("the '345 patent"). *Id.*

On November 2, 2001, the presiding administrative law judge ("ALJ") issued an initial determination ("ID") (ALJ Order No. 15) granting complainants' motion for summary determination on the issue of importation and denying respondents' motion for summary determination of lack of importation. That ID was not reviewed by the Commission. A tutorial session was held on November 5, 2001, and an evidentiary hearing was held from November 7, 2001, through November 16, 2001, and from December 10, 2001, through December 12, 2001.

The ALJ issued his final ID on May 6, 2002, concluding that there was no violation of section 337. With respect to the '352 patent, the ALJ found that: complainants have not established that the domestic industry requirement is met; none of respondents' accused devices infringe any asserted claim of the '352 patent literally or under the doctrine of equivalents; and claims 1 and 2 of the '352 patent are invalid as anticipated under 35 U.S.C. § 102 and claim 8 of the '352 patent is invalid for obviousness under 35 U.S.C. § 103. With respect to the '345 patent, the ALJ found each of the claims listed in the notice of investigation, *i.e.*, claims 1, 3-16, 19-20, and 21, invalid as anticipated by and made obvious by certain prior art. The ALJ stated that, in their post-hearing filings, complainants asserted only claims 1, 3-5, 9, 11-13, and 20-21 of the '345 patent against respondents. He found that, if valid, each of the asserted claims of the '345 patent, *i.e.*, claims 1, 3-5, 9, 11-13, and 20-21, is literally infringed by SiS's existing (or old) SiON manufacturing process, but that respondents' new N_2O process does not infringe any asserted claim of the '345 patent. The ALJ further found that a domestic industry exists with respect to the '345 patent. On May 13, 2002, the ALJ issued his recommended determination on remedy and bonding.On May 20, 2002, complainants and the Commission investigative attorney ("IA") petitioned for review of the subject ID, and respondents filed a contingent petition for review of the ALJ's final ID.

On June 21, 2002, the Commission determined to review the ID in part. Specifically, the Commission determined to review and clarify that the ALJ found claim 13 of the '345 patent made obvious, but not anticipated, by the Tobben patent. The Commission also determined to review: (1) the ALJ's findings and conclusions of law regarding the '352 patent with respect to infringement of the asserted claims and domestic industry under the doctrine of equivalents; (2) the ALJ's finding that respondents' old E5 model ESD transistor does not infringe any asserted claim of the '352 patent, either literally or equivalently; (3) the ALJ's claim construction of the limitations "an ESD protection device" (claims 1, 2, and 8 of the '352 patent), "a gate" (claims 1 and 2), "gates" (claim 8), and "source/drain regions . . . with each source/drain region comprising" (claims 1, 2, and 8), and the ALJ's invalidity, domestic industry, and infringement findings and conclusions of law with respect to those limitations; (4) the ALJ's finding that claim 8 of the '352 patent is invalid as made obvious by a combination of prior art references; (5) whether the economic prong of the domestic industry requirement is met with respect to the '352 patent; (6) the ALJ's findings that the "second antireflective coating" (claim 1 and asserted dependent claims 3-8 of the '345 patent) and "cap layer" (claims 9-16, 19-20, and 21 of the '345 patent) are disclosed in the Tobben patent, and consequently (a) the ALJ's findings with respect to etching the second antireflective coating or cap layer (claims 4 and 12), (b) the ALJ's ultimate finding that the Tobben patent anticipates claims 1, 3-16, 19-20, and 21 of the '345 patent, and (c) the ALJ's conclusion that claim 13 is made obvious by the Tobben patent and other prior art;

(7) the ALJ's conclusion that claim 13 of the '345 patent is invalid as obvious in light of the Tobben patent; and (8) the ALJ's conclusion that claims 1, 3-16, 19-20, and 21 of the '345 patent are invalid as made obvious by the Abernathey patent in combination with the Pan, Yagi, and/or Yota publications. The Commission determined not to review the remainder of the ID, including the ID's conclusions and findings of fact with respect to whether the Tobben patent is prior art to the '345 patent, infringement of the asserted claims of the '345 patent, domestic industry concerning the '345 patent, and failure to disclose the best mode of practicing the invention of the '345 patent. The Commission requested briefs on the issues under review, and posed briefing questions for the parties to answer. The Commission also requested written submissions on the issues of remedy, the public interest, and bonding. 67 *Fed. Reg.* 43338. Initial briefs were filed on July 9, 2002, and reply briefs were filed on July 16, 2002, and July 17, 2002.

Having examined the record in this investigation, including the briefs and the responses thereto, the Commission determined that there is a violation of section 337 as to claim 13 of the '345 patent, but no violation of the statute as to the remaining claims in issue of the '345 patent (*viz.*, claims 1, 3-5, 9, 11-12, 20, and 21) and no violation as to the claims in issue of the '352 patent (*viz.*, claims 1, 2, and 8). With respect to the '352 patent, the Commission determined to modify the ALJ's construction of certain limitations in the asserted claims of the '352 patent, and to affirm the ALJ's findings and conclusions that (a) the asserted claims are not infringed, and (b) complainants failed to establish the technical prong of the domestic industry requirement under the revised claim construction.

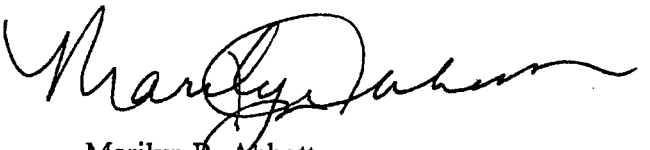
The Commission also determined to affirm the ALJ's finding that claims 1 and 2 of the '352 patent are invalid as anticipated, to reverse the ALJ's finding that claim 8 of the '352 patent is invalid as made obvious, and to take no position as to whether complainants established the economic prong of the domestic industry requirement with respect to the '352 patent. With respect to the '345 patent, the Commission determined to vacate the ALJ's findings and conclusions as to invalidity with respect to claims 6-8, 10, 14-16, and 19; to reverse the ALJ's finding that claims 1, 3-5, 9, 11-12, 20, and 21 are invalid as anticipated; to affirm the ALJ's conclusion that claims 1, 3-5, 9, 11-12, 20, and 21 of the '345 patent are invalid as obvious; and to clarify that claim 13 is not anticipated and reverse the ALJ's conclusion that claim 13 is invalid as obvious.

The Commission also made determinations on the issues of remedy, the public interest, and bonding. The Commission determined that the appropriate form of relief is a limited exclusion order prohibiting the unlicensed entry of integrated circuits, including chipsets and graphics chips, that are made by a process covered by claim 13 of U.S. Letters Patent 6,117,345 and manufactured by or on behalf of respondents, and motherboards containing such integrated circuits.

The Commission also determined that the public interest factors enumerated in 19 U.S.C. § 1337(d) do not preclude the issuance of the limited exclusion order, and that the bond during the Presidential review period should be set at 100 percent of the entered value of integrated circuits subject to the Commission's order and 39 percent of the entered value of motherboards containing such integrated circuits.

The authority for the Commission's determinations is contained in section 337 of the Tariff Act of 1930, as amended (19 U.S.C. § 1337), and in sections 210.45 - 210.51 of the Commission's Rules of Practice and Procedure (19 C.F.R. §§ 210.45 - 210.51).

By order of the Commission.



Marilyn R. Abbott
Secretary to the Commission

Issued: October 7, 2002

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	
CERTAIN INTEGRATED CIRCUITS, PROCESSES FOR MAKING SAME, AND PRODUCTS CONTAINING SAME	Inv. No. 337-TA-450

LIMITED EXCLUSION ORDER

The Commission has determined that there is a violation of section 337 of the Tariff Act of 1930 (19 U.S.C. § 1337) in the unlawful importation and sale by respondents Silicon Integrated Systems Corp. of Taiwan and Silicon Integrated Systems Corporation of the United States (together, "respondents") of integrated circuits, and certain products containing same, made by a process covered by claim 13 of U.S. Letters Patent 6,117,345.

Having reviewed the record in this investigation, including the recommended determination of the presiding administrative law judge and the written submissions of the parties, the Commission has made its determination on the issues of remedy, the public interest, and bonding. The Commission has determined that the appropriate form of relief is a limited exclusion order prohibiting the unlicensed entry of integrated circuits, including chipsets and graphics chips, that are made by a process covered by claim 13 of U.S. Letters Patent 6,117,345 and manufactured by or on behalf of respondents, and motherboards that contain such infringing integrated circuits.

The Commission has also determined that the public interest factors enumerated in 19 U.S.C. § 1337(d) do not preclude issuance of the limited exclusion order, and that the bond during the Presidential review period shall be in the amount of 100 percent of the entered value of integrated circuits, including chipsets and graphics chips, subject to the Commission's order, and 39 percent of the entered value of motherboards containing such integrated circuits.

Accordingly, the Commission hereby **ORDERS THAT:**

1. Integrated circuits, including chipsets and graphics chips, that are made by a process covered by claim 13 of U.S. Letters Patent 6,117,345 and are manufactured abroad and/or imported by or on behalf of respondents or any of their affiliated companies, parents, subsidiaries, or other related business entities, or their successors or assigns, and motherboards containing same, are excluded from entry for consumption into the United States, entry for consumption from a foreign trade zone, or withdrawal from a warehouse for consumption, for the remaining term of the patent, except under license of the patent owner or as provided by law.

2. Integrated circuits, including chipsets and graphics chips, that are excluded by paragraph 1 of this Order are entitled to entry for consumption into the United States, entry for consumption from a foreign trade zone, or withdrawal from a warehouse for consumption, under bond in the amount of 100 percent of entered value pursuant to subsection (j) of section 337 of the Tariff Act of 1930, as amended 19 U.S.C. § 1337(j), from the day after this Order is received by the President until such time as the President notifies the Commission that he approves or disapproves this action but, in any event, not later than sixty (60) days after the date of receipt of this action.

3. Motherboards that are excluded by paragraph 1 of this Order are entitled to entry for consumption into the United States, entry for consumption from a foreign trade zone, or withdrawal from a warehouse for consumption, under bond in the amount of 39 percent of entered value pursuant to subsection (j) of section 337 of the Tariff Act of 1930, as amended 19 U.S.C. § 1337(j), from the day after this Order is received by the President until such time as the President notifies the Commission that he approves or disapproves this action but, in any event, not later than sixty (60) days after the date of receipt of this action.

4. Pursuant to procedures to be specified by U.S. Customs Service, as the Customs Service deems necessary, persons seeking to import integrated circuits, including chipsets and graphics chips, or motherboards containing same, that are potentially subject to this Order shall certify that they are familiar with the terms of this Order, that they have made appropriate inquiry, and thereupon state that, to the best of their knowledge and belief, the products being imported are not excluded from entry under paragraph 1 of this Order. At its discretion, the Customs Service may require persons who have provided the certification described in this paragraph to furnish such records or analyses as are necessary to substantiate the certification.

5. In accordance with 19 U.S.C. § 1337(l), the provisions of this Order shall not apply to integrated circuits and motherboards containing same that are imported by and for the use of the United States, or imported for, and to be used for, the United States with the authorization or consent of the Government.

6. The Commission may modify this Order in accordance with the procedures described in section 210.76 of the Commission's Rules of Practice and Procedure, 19 C.F.R. § 210.76.

7. The Secretary shall serve copies of this Order upon each party of record in this investigation and upon the Department of Health and Human Services, the Department of Justice, the Federal Trade Commission, and the U.S. Customs Service.

8. Notice of this Order shall be published in the *Federal Register*.

By Order of the Commission.

Marilyn R. Abbott
Secretary to the Commission

Issued: October 7, 2002

CERTAIN INTEGRATED CIRCUITS, PROCESSES FOR MAKING SAME, AND PRODUCTS CONTAINING SAME **337-TA-450**

CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the **Notice Of Final Determination and Issuance of Limited Exclusion Order,** was served upon the following parties via first class mail and air mail where necessary, on **October 8, 2002.**

Marilyn R. Abbott, Secretary
U.S. International Trade Commission
500 E Street, SW - Room 112
Washington, DC 20436

ON BEHALF OF COMPLAINANT UNITED MICROELECTRONICS CORPORATION, UMC GROUP AND UNITED FOUNDRY SERVICE, INCORPORATED:

Steven J. Routh, Esq.
Hogan and Hartson
555 13th Street, NW
Washington, DC 20004

William H. Wright, Esq.
Biltmore Tower
Hogan and Hartson
500 S. Grand Avenue
Suite 1900
Los Angeles, CA 90071

ON BEHALF OF SILICON INTEGRATED SYSTEMS CORPORATION:

Tom M. Schaumberg, Esq.
Adduci, Mastriani and Schaumberg, LLP
1200 Seventeenth Street, NW
Fifth Floor
Washington, DC 20036

Kirk R. Ruthenberg, Esq.
Sonnenschein Nath and Rosenthal
1301 K Street, NW
Suite 600, East Tower
Washington, DC 20005

Edward H. Rice, Esq.
Sonnenschein Nath and Rosenthal
8000 Sears Tower
Chicago, IL 60606

Michael A. Molano, Esq.
Sonnenschein Nath and Rosenthal
685 Market Street, 6th Floor
San Francisco, CA 94105

ON BEHALF OF THE COMMISSION:

Shival P. Virmani, Esq.
Commission Investigative Attorney
Office of Unfair Import Investigation
500 E Street, SW - Room 401-J
Washington, DC 20436

James B. Coughlan, Esq.
Commission Investigative Attorney
Office of Unfair Import Investigations
500 E Street, SW - Room 401-L
Washington, DC 20436

Timothy Monaghan, Esq.
Advisory Attorney
Office of General Counsel
500 E Street, SW - Room 707-U
Washington, DC 20436

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington D.C. 20436

In the Matter of	
CERTAIN INTEGRATED CIRCUITS, PROCESSES FOR MAKING SAME, AND PRODUCTS CONTAINING SAME	**Investigation No. 337-TA-450**

CONFIDENTIAL INFORMATION DELETED

COMMISSION OPINION

This section 337 investigation is before the Commission for final disposition of the issues under review and, if necessary, for determinations on remedy, the public interest, and bonding. We find a violation of section 337 of the Tariff Act of 1930 as to claim 13 of U.S. Letters Patent 6,117,345 ("the '345 patent"), but no violation of the statute as to the remaining claims in issue of the '345 patent (*viz.*, claims 1, 3-5, 9, 11-12, 20, and 21) and no violation as to the claims in issue of U.S. Letters Patent 5,559,352 ("the '352 patent") (*viz.*, claims 1, 2, and 8).

We have determined that the appropriate form of relief is a limited exclusion order prohibiting the unlicensed entry of integrated circuits, including chipsets and graphics chips, that are made by a process covered by claim 13 of the '345 patent and manufactured by or on behalf of respondents Silicon Integrated Systems Corp. of Taiwan and Silicon Integrated Systems Corporation of the United States, and motherboards containing such integrated circuits. We determined that the statutory public interest factors do not preclude the issuance of such a limited exclusion order, and that the bond during the Presidential review period should be set in the

amount of 100 percent of the entered value of integrated circuits subject to the Commission's order and 39 percent of the entered value of motherboards containing such integrated circuits.

PROCEDURAL HISTORY

The Commission instituted this investigation based on a complaint filed on January 26, 2001, by United Microelectronics Corporation, Hsinchu City, Taiwan; UMC Group (USA), Sunnyvale, CA; and United Foundry Service, Inc., Hopewell Junction, NY. The complaint, as supplemented, alleged violations of section 337 by Silicon Integrated Systems Corp., Hsinchu City, Taiwan, and Silicon Integrated Systems Corporation, Sunnyvale, CA (collectively, "SiS" or "respondents") in the importation, the sale for importation, and the sale within the United States after importation of certain integrated circuits and products containing same by reason of infringement of claims 1, 2, and 8 of the '352 patent and claims 1, 3-16, and 19-21 of the '345 patent. The Commission's notice of investigation was published in the *Federal Register* on March 6, 2001. 66 *Fed. Reg.* 13567 (2001).

On November 2, 2001, the presiding administrative law judge ("ALJ") issued an initial determination ("ID") (ALJ Order No. 15) granting complainants' motion for summary determination on the issue of importation and denying respondents' motion for summary determination of lack of importation. That ID was not reviewed by the Commission. A tutorial session was held on November 5, 2001, and an evidentiary hearing was held from November 7, 2001, through November 16, 2001, and from December 10, 2001, through December 12, 2001.

The ALJ issued his final ID on May 6, 2002, concluding that there was no violation of section 337. On May 13, 2002, the ALJ issued his recommended determination on remedy and

bonding in the event that the Commission were to find a violation of section 337.

On May 17, 2002, complainants and the Commission investigative attorney ("IA") petitioned for review[1] of portions of the ALJ's final ID, and respondents filed a contingent petition[2] for review. On May 24, 2002, complainants, respondents, and the IA filed their responses to the petitions for review.[3]

On June 21, 2002, the Commission determined to review the ID in part. In its review notice, the Commission invited the parties to file written submissions on the issues under review, invited interested persons to file written submissions on the issues of remedy, the public interest and bonding, and requested briefing from the parties on 11 questions. Initial briefs[4] were filed on July 9, 2002, and responses[5] were filed on July 16, 2002, and July 17, 2002.[6]

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[1] Complainants' Petition for Review of the May 6, 2002 Initial Determination and Order ("complainants' petition"); Office of Unfair Import Investigations' Petition for Review of Portions of the Initial Determination ("IA's petition").

[2] Contingent Petition of Respondents Silicon Integrated Systems Corp. and Silicon Integrated Systems Corporation for Review of the Initial Determination ("respondents' petition).

[3] Complainants' Response to Respondents' Contingent Petition for Review of the May 6, 2002 Initial Determination and Order ("complainants' response"); Respondents' Response to Petitions for Review of the May 6, 2002 Initial Determination and Order ("respondents' response"); The Office of Unfair Import Investigations' Response to Complainants' and Respondents' Petitions for Review of the Final Initial Determination (IA's response").

[4] Complainants' Brief on Questions Posed and Issues Identified for Review in June 21 Notice of Commission Decision to Review Portions of Initial Determination ("complainants' brief"); Respondents' Brief on Commission's June 21, 2002 Decision to Review the May 6, 2002 Initial Determination ("respondents' brief"); Submission of Respondents Silicon Integrated Systems Corporation (Taiwan) and Silicon Integrated Systems Corporation (U.S.) on Remedy, Bonding and the Public Interest ("respondents' remedy brief"); Office of Unfair Import Investigations' Brief on the Issues under Review and on Remedy, the Public Interest, and Bonding ("IA's brief").

[5] Complainants' Reply Brief on Questions Posed and Issues Identified for Review in June 21 Notice of Commission Decision to Review Portions of Initial Determination ("complainants' reply"); Respondents' Reply Brief on Commission's June 21, 2002 Decision to Review the May 6, 2002 Initial Determination ("respondents' reply"); The Office of Unfair Import Investigations' Response to Complainants' and Respondents' Briefs on the Issues under Review and on Remedy, the Public Interest, and Bonding ("IA's reply").

[6] The private parties filed reply briefs on July 16, 2002. The Chairman exercised his discretion in accepting the IA's late-filed reply brief on July 17, 2002.

Having examined the record in this investigation, including the briefs and the responses thereto, we determined that there is a violation of section 337 as to claim 13 of the '345 patent, but no violation of the statute as to the remaining claims in issue of the '345 patent (*viz.*, claims 1, 3-5, 9, 11-12, 20, and 21) and no violation as to the claims in issue of the '352 patent (*viz.*, claims 1, 2, and 8).

ISSUES UNDER REVIEW

I. Standards on Review

This investigation is before us on review of the ALJ's final ID on violation, which issued on May 6, 2002. Commission rule 210.45 (c), 19 C.F.R. § 210.45 (c) states:

> On review, the Commission may affirm, reverse, modify, set aside or remand for further proceedings, in whole or in part, the initial determination of the administrative law judge. The Commission also may make any findings or conclusions that in its judgment are proper based on the record in the proceeding.

Once the Commission determines to review an ID, it reviews the determination under a *de novo* standard. *Certain Acid-Washed Denim Garments and Accessories*, Inv. No. 337-TA-324, Commission Opinion at 4-5 (August 28, 1992) (the Commission examines for itself the record on the issues under review); *accord, Certain Flash Memory Circuits and Products Containing Same*, Inv. No. 337-TA-382, Commission Opinion at 14 (January 9, 1997). Commission practice is consistent with the Administrative Procedure Act, 5 U.S.C. § 1 et seq. (APA). The APA provides that once an initial agency decision is taken up for review, "the agency has all the powers which it would have in making the initial decision except as it may limit the issues on notice or by rule." 5 U.S.C. §557(b). This statutory provision and Commission rule 210.45(c) reflect the fact that the Commission is not an appellate court, but the body responsible for making

the final agency decision. On appeal, only the Commission's final decision is at issue. *Fischer & Porter Co. v. United States Int'l Trade Comm'n,* 831 F.2d 1574, 1576-77 (Fed. Cir. 1987).

As stated in the Commission's review notice, the Commission determined to review in part the ALJ's final ID. The Commission thereby adopted as its own the unreviewed portions of the ID. With respect to the portions of the ID that are under review, the ALJ's findings, conclusions, and supporting analysis that are not inconsistent with this opinion are adopted by the Commission. The ALJ's findings, conclusions, and supporting analysis that are inconsistent with this opinion are not adopted.

II. The '345 Patent

The notice of investigation identifies the claims in issue of the '345 patent as 1, 3-16, and 19-20, and 21. 66 *Fed. Reg.* 13567. With respect to the '345 patent, the ALJ found each of the claims listed in the notice of investigation (*i.e.*, claims 1, 3-16, 19-20, and 21) invalid as anticipated and/or made obvious by the prior art. In their post-hearing filings, complainants asserted a subset of the '345 patent claims in issue against respondents, *i.e.*, claims 1, 3-5, 9, 11-13, 20, and 21. ID at 67. The ALJ found that, if valid, each of the asserted claims (*i.e.*, claims 1, 3-5, 9, 11-13, and 20-21) is literally infringed by SiS's existing (or old) SiON manufacturing process, but that respondents' new N_2O process does not infringe any asserted claim of the '345 patent. The ALJ further found that a domestic industry exists with respect to the '345 patent.

The Commission determined to review certain of the ALJ's findings and conclusions as to invalidity with respect to the '345 patent, but determined not to review the remainder of the ID

with respect to this patent, and thereby adopted the unreviewed portions of the ID as its own.[7] On review, the Commission determined to reverse the ALJ's ultimate finding of no violation of section 337 with respect to the '345 patent, and to find a violation as to claim 13. With respect to the issues under review concerning this patent, the Commission determined (1) to vacate the ALJ's findings and conclusions as to invalidity with respect to claims 6-8, 10, 14-16, and 19; (2) to modify the ID to clarify that claim 13 is not anticipated by the Tobben patent[8]; (3) to affirm the ALJ's conclusion that claims 1, 3-5, 9, 11-12, 20, and 21 are invalid as obvious, but reverse his finding that those claims are anticipated; and (4) to reverse the ALJ's conclusion that claim 13 is invalid as obvious.

As to the first issue, the ALJ found claims 6-8, 10, 14-16, and 19 invalid as anticipated and/or made obvious by the prior art. Complainants did not assert those claims against respondents in their post-hearing briefing before the ALJ, and the ALJ made no infringement findings with respect to those claims. No party petitioned for review of the ALJ's infringement findings with respect to the '345 patent. Because the infringement of claims 6-8, 10, 14-16, and 19 of the '345 patent is not at issue in this investigation, the question before the Commission on review, *viz.*, whether those claims are invalid as anticipated or made obvious by the prior art, is moot. The Commission therefore determined to vacate the ALJ's findings and conclusions as to the invalidity of claims 6-8, 10, 14-16, and 19 of the '345 patent. As to the second issue, as

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[7] The unreviewed portions of the ID concerning the '345 patent include the ID's conclusions and findings of fact with respect to whether the Tobben patent is prior art to the '345 patent, infringement of the asserted claims of the '345 patent, domestic industry concerning the '345 patent, and failure to disclose the best mode of practicing the invention of the '345 patent.

[8] U.S. Letters Patent 5,854,126 to Tobben et al. ("the Tobben patent") is entitled "Method for Forming Metallization in Semiconductor Devices with a Self-Planarizing Material." RX-70.

pointed out by complainants and acknowledged by the ALJ (ID at 134 n.16), respondents did not contend that the Tobben patent anticipated claim 13.

With respect to the remaining issues under review, the Commission determined to reverse the ALJ's finding that the Tobben patent anticipates independent claim 1 (and asserted dependent claims 3-5), independent claim 9 (and asserted dependent claims 11, 12, and 20), and independent claim 21 of the '345 patent, and to reverse the ALJ's conclusion that claim 13 is made obvious by the Tobben patent. The Commission determined to affirm the ALJ's conclusion that the Abernathey patent in view of Dean combined with Pan, Yagi, or Yota renders obvious independent claim 1 (and asserted dependent claims 3-5), independent claim 9 (and asserted dependent claims 11, 12, and 20), and independent claim 21 of the '345 patent, but to reverse the ALJ's conclusion that claim 13 is made obvious by the Abernathey patent in combination with other prior art.[9] The Tobben patent is discussed in Part II.A, *infra*, and the Abernathey patent is discussed in Part II.B.

A. The Tobben Patent

The ALJ found claims 1, 3-5, 9, 11-12, 20, and 21 of the '345 patent anticipated by the Tobben patent. ID at 134, FF 471-544. He also found claim 13 made obvious by the Tobben patent in view of the knowledge of a person of ordinary skill in the art. ID at 134 n.61, 276-77. With respect to the ALJ's invalidity findings regarding the Tobben patent, the Commission

[9] U.S. Letters Patent 5,219,788 to Abernathey et al. ("the Abernathey patent") is entitled "Bilayer Metallization Cap for Photolithography." RX-156. The other publications are Pan et al., "Integrated Interconnect Module Development" (RX-82); Yagi, "Multilevel interconnection technology in system LSI" (RX-85); Yota et al., "Integration of ICP High-Density Plasma CVD with CMP and its Effects on Planarity for Sub-0.5 m CMOS Technology" (RX-86); and Dean et al. "Investigations of deep ultraviolet photoresists on TiN substrates" (RX-177).

determined to review: (1) the ALJ's finding that the Tobben patent discloses the "second antireflective coating" (claim 1 and asserted dependent claims 3-5 of the '345 patent), (2) the ALJ's finding that Tobben discloses the "cap layer" (claims 9, 11-13, 20, and 21 of the '345 patent), and (3) the ALJ's conclusion that claim 13 of the '345 patent is invalid as obvious in light of the Tobben patent.[10]

As discussed below, the Commission determined to reverse the ALJ's finding that the Tobben patent inherently discloses the "second antireflective coating" (claims 1, 3-4, and 5), and consequently, also to reverse the ALJ's findings that Tobben discloses etching the second antireflective coating (claim 4), and that Tobben anticipates claims 1, 3-4, and 5. The Commission determined to reverse the ALJ's finding that the Tobben patent discloses the "cap layer" of claims 9 and 21. The Commission consequently also determined to reverse the ALJ's findings that Tobben discloses etching the cap layer (claim 12) and that Tobben anticipates claims 9, 11-12, 20, and 21; and determined to reverse his conclusion that Tobben renders claim 13 obvious. Finally, the Commission determined to reverse the ALJ's conclusion that Tobben renders claim 13 obvious on the alternate, independent ground that respondents have failed to demonstrate the requisite motivation to modify the teachings of the Tobben reference to use a silicon nitride or an oxynitride material in place of silicon dioxide for the cap layer.

[10] In their briefing to the Commission, complainants stated that the Commission is also reviewing the ALJ's anticipation findings regarding the Tobben prior art with respect to the gap fill limitations. The Commission did not determine to review the ID as to those findings.

1. Whether the Tobben Patent Discloses "A Second Antireflective Coating" (claim 1).

The ALJ found that the second antireflective coating of claim 1 was disclosed in the Tobben patent's planarization layer because the range of thicknesses for the planarization layer disclosed in Tobben (300 Å to 2000 Å) included values for which the layer would act as an antireflective coating through destructive interference and the planarization layer would act as an antireflective coating for some portions of the wafer. ID at 128-130. Having examined the record in this investigation, including the briefs and the responses thereto, the Commission determined to reverse the ALJ's factual finding that the Tobben patent's planarization layer inherently discloses the "second antireflective coating" of claim 1 (and dependent claims 3-5) of the '345 patent.

If a prior art reference is silent about a claimed characteristic, the reference may still anticipate if the characteristic is "inherently" present in the reference. The Federal Circuit has held that inherent characteristic must be "necessarily present in the thing described in the reference." *Continental Can Co. USA v. Monsanto Co.*, 948 F.2d 1264 (Fed. Cir. 1991). The court has repeatedly stated that inherency "may not be established by probabilities or possibilities." *Mehl/Biophile Int'l Corp. v. Milgraum*, 192 F.3d 1362, 1365 (Fed. Cir. 1999) (quoting *In re Oelrich*, 666 F.2d 578, 581 (CCPA 1981) (quoting *Hansgirg v. Kemmer*, 102 F.2d 212, 214 (CCPA 1939))).

In their petition for review and again in their brief to the Commission, complainants characterized the ID as adopting a "theory that the Tobben patent inherently discloses a second [antireflective coating] because, by using a planarization layer that varies in thickness from 300

to 2000 Å, there might be a particular 'spot' on the wafer where the planarization layer has antireflective properties." Complainants' brief at 78; complainants' petition at 47-49. They asserted that "the ALJ improperly *assumed* that the planarization layer disclosed in Tobben would necessarily include at least one 'spot' where the layer had antireflective properties. The thickness of Tobben's planarization layer varies according to the contours of the uneven metal layer beneath it. Accordingly, one cannot control the thickness of that layer at any location on the wafer, and it is possible that the planarization layer could contain a range of thicknesses that are entirely within one or more bands where constructive interference occurs, creating an increase in reflectivity." Complainants' brief at 78-79; complainants' petition at 47-48. Complainants contended that "if Tobben's planarization layer turned out to include both areas that were reflective and areas that were antireflective, the Tobben patent could not serve as an anticipatory reference because an antireflective coating would not be 'necessarily present' at any particular point on the wafer." Complainants' brief at 79; complainants' petition at 48.

Although the ALJ found that the Tobben planarization layer disclosed the second antireflective layer because the layer "in fact would" act as an antireflective coating for "some regions" of the wafer (ID at 130), as discussed below, the record does not support a finding that the planarization layer disclosed in Tobben must contain at least one spot where the layer acts as an antireflective coating. Moreover, in their reply brief to the Commission, respondents concede that "[c]omplainants are correct that one could construct a Tobben embodiment like the [embodiment identified by complainants in their brief to the Commission at 79] in which the planarizing thickness varies in such a way that it is never antireflective." Respondents' reply at

39. Because the disclosed planarization layer could be entirely reflective, a finding that the disclosed layer must always have at least a "spot" where it is antireflective is incorrect.

The factual finding at issue is the ALJ's statement that "[r]espondents' expert [Peltzer] testified that *in fact there would be regions* in which the planarization layer in Tobben (such as the silicon dioxide layer which is described in detail) would act as an antireflective coating, for example, above a titanium nitride layer." ID at 130 (citing Trans. (Fair) at 1395; (Peltzer) at 815) (emphasis added). The testimony of respondents' expert (Peltzer) cited by the ALJ in support of the factual finding reads as follows:

> Q Mr. Peltzer, let me interrupt you at that point. Does the thickness for the SiO2 layer of 300 angstroms to 2000 angstroms correspond in any way to the thickness disclosed for the cap layer in the '345 patent?
> A It is of such thickness range to be a quarter-wave plate over *portions*.
>
> * * *
>
> BY MR. HOVANEC:
>
> Q So in your opinion, the SiO2 layer in Tobben is a second antireflective coating on the first antireflective coating?
> A Yes. This range from 300 to 2000 angstroms clearly encompasses ranges where we get an interferometric coating, get cancellation of the reflected light from the surface of this coating, with the reflected light from the bottom surface. So this is an antireflective coating, over most of the range it's an antireflective coating. There's a small range where the reflection might be worse.

Trans. at 814:3 - 815:3 (emphasis added). (The ALJ cited Peltzer's testimony on page 815 of the transcript. The remainder of the testimony on page 815 is noted below.[11]) The word "portions"

[11] The remainder of the testimony on page 815 of the transcript is as follows:

> Q The next element is forming a mask layer. Is that in Tobben?
> A Yes. "Next, a photoresist layer is spun on the planar surface," and the following cite, the "mask is

in Peltzer's response to the first question in the above-quoted testimony refers to portions of the range of thicknesses (*i.e.*, the vertical dimension of the layer) rather than to a spot or area (*i.e.*, the horizontal dimension of the layer). We reach this understanding by looking to the specific question that Peltzer is answering. The question asked for a comparison between (1) the 300 Å to 2000 Å thickness range for the SiO_2 layer disclosed in Tobben, and (2) the thickness of the cap layer in the '345 patent. Peltzer answered the question by stating that the thickness for the SiO2 layer disclosed in Tobben "is of such thickness range [300 Å to 2000 Å] *to be a quarter-wave plate* over portions." The '345 patent specification states that "the cap layer may be used as a quarter wave plate." '345 patent, col. 7 ll. 58-64; ID at 77 and n. 36. According to the '345 patent, "the quarter wave plate creates destructive interference to prevent light from reflecting up to the photoresist layer." '345 patent, col. 7 lines 58-65. The '345 patent specification goes on to

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used to pattern exposed portions of the underlying planarization layer."

Q The next element of claim 1 is etching the first antireflective coating. Is that discussed in Tobben?
A Yes, then we have the mask is used to pattern exposed portions of the underlying planarization layer. And referring to figure 4, the photoresist mask is used to etch the exposed portions of the planarization layer, yes.

Q Now, continuing with the remainder of claim 1 -- I'm sorry, just one moment. I think I picked up the wrong one. Continuing with the next part of claim 1, is depositing a dielectric material within the gaps disclosed in Tobben?
A Yes, it says here a layer of silicon dioxide may be deposited over the surface, of the grooved surface using high-density plasma deposition techniques, HDP techniques.

Q Now, would you continue with claim 3?
A The method of claim 1 wherein the mask layer is a patterned photoresist layer, in column 3, lines 21 through 22 of Tobben. "Next, a photoresist layer is spun on the planar surface of the planarization layer." Continuing, "the photoresist layer is then developed to remove the exposed or polymerized portions creating grooves or slots." That's patterning. And again, I'm saying I am interpreting the patterning as this creating grooves or slots portion.

Trans. (Peltzer) 815:3 - 816:7.

discuss the thickness of the cap layer in connection with the quarter wave plate function: "Those of ordinary skill in the art will appreciate that the particular thickness of [the cap] layer 28 to be provided when layer 28 has its preferred function as a quarter wave plate is different for different materials. The preferred thickness for layer 28 can be determined by setting the thickness to be one quarter of the wavelength of the exposure light taking into account the dielectric constant of the material in layer 28 at the wavelength of the exposure light." '345 patent, col. 7, l. 67 - col. 8, l. 8. Furthermore, the next question and answer clarifies that "cancellation of the reflected light from the surface" occurs only over a part of the range of thicknesses of 300 Å to 2000 Å. Consequently, the ALJ's finding that there "in fact would be regions" (*i.e.*, horizontal areas, rather than thicknesses) in which the planarization layer would act as an antireflective coating is incorrect because it lacks support in the record.[12]

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[12] The testimony of complainants' expert (Fair), which is also cited by the ALJ in support of the factual finding at issue, supports our conclusion. Fair's testimony reads as follows:

> Q: And if we only looked at that region, the middle two wiring lines in figure 4 in Tobben, in that region you would expect to have a uniform planarization layer, a uniform thickness for the planarization layer 16, and therefore a second [antireflective coating], correct?
>
> A: There's no way of telling. I mean, because you don't know what the thickness is. It may cause constructive interference and therefore not be an [antireflective coating]. It may cause destructive interference and in that local area it may function as an [antireflective coating]. So you don't really know.
>
> Q: So you acknowledge that at least in some specific regions throughout a wafer made according to the Tobben disclosure there would be a second [antireflective coating] above the Ti nitride layer, correct?
>
> A: Well, it's possible that that could happen by fortuitous circumstance. But two things. There's no explicit disclosure that layer 16 is an [antireflective coating] and it's certainly not inherently an [antireflective coating]. It could be or it couldn't be.
>
> Q: Now, in Tobben it identifies that the thickness of the planarization layer is no more than 300 angstroms to 2,000 angstroms, but it certainly doesn't exclude the possibility that the thickness of the planarization layer is far more tightly controlled, correct?
>
> A: There's no teaching one way or another. It's a function of what the topography is.

The ALJ found that "[a]ccording to Dr. Peltzer, the thickness for the SiO2 layer of 300 A to 2000A clearly encompasses ranges where cancellation of reflected light from the surface of this coating [is] such as to be a quarter wave plate *making the SiO2 layer in Tobben a second antireflective coating*. Peltzer Tr. 814: 3-815:3." FF 475 (emphasis added). The ALJ further found that "Dr. Peltzer's opinion was supported by a mathematical calculation of reflectivity of the type upon which engineers ordinarily rely in the course of work concerning the subject matter of the '345 patent. Peltzer Tr. 856: 21-11; RPX-46." FF 476. However, because the 300 Å to 2000 Å range of thicknesses for the planarization layer disclosed in Tobben includes thicknesses where there will be constructive interference (*i.e.*, an *increase* in reflectivity), the antireflective property is not "necessarily present." Consequently, an antireflective coating is not inherent in that disclosure.

Respondents do not contend that the layer is antireflective for thicknesses at every value within the disclosed range of 300 Å to 2000 Å. *See, e.g.*, Respondents' reply brief at 38; Respondents' Rebuttal Brief for the Hearing Completed November 16, 2001, at 21 (filed December 27, 2001) (stating that silicon dioxide is not an antireflective coating using destructive interference for DUV [deep ultraviolet] light at 248 nm between 640 Å and 820 Å). The testimony of respondents' expert (Peltzer) at 814:3-815:3, on which the ALJ relies in FF 475, stated only that "over *most* of the range" of disclosed thicknesses of the Tobben planarization layer, *i.e.*, for most thicknesses in the disclosed range of 300 Å to 2000 Å, the Tobben planarization layer acts as an antireflective coating. Indeed, Peltzer there conceded that "[t]here's

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Trans. (Fair) at 1394:17-1395:20.

a small range where the reflection might be worse." Exhibit RPX-46, cited by the ALJ in FF 476, presents the results of Peltzer's reflectivity calculation. Exhibit RPX-46 is discussed by Peltzer in the hearing transcript at 848-57. Peltzer testified that for thicknesses between 640 Å and 820 Å the planarization layer *increased* reflectivity. Trans. (Peltzer) at 856:12-20; RPX-46 at 2-4. The 300 Å to 2000 Å range of thicknesses for the planarization layer disclosed in Tobben includes thicknesses where there will be constructive interference (an *increase* in reflectivity).

In support of their argument that, because the disclosed planarization layer functions as an antireflective coating over part of the disclosed thickness range of 300 Å to 2000 Å, the Tobben planarization layer inherently discloses the "second antireflective coating" for anticipation purposes, respondents cite *In re Schreiber*, 128 F.3d 1473, 44 USPQ2d 1429 (Fed. Cir. 1997). In that case, the Federal Circuit upheld a Patent Office rejection of an application claim for a conically shaped top for dispensing popped popcorn. *Schreiber*, 44 USPQ2d at 1429-33. The claimed top has an opening in the narrow end of the cone that allows only a few kernels of popcorn to pass through at a time. *Schreiber*, 44 USPQ2d at 1430. The Patent Office rejected the claim as anticipated by a prior art patent to Harz disclosing "a spout for nozzle-ready canisters." *Schreiber*, 44 USPQ2d at 1430. Respondents argued that "[j]ust as one embodiment of the prior art oil can lid necessarily was 'capable of' dispensing popcorn in *Schreiber*, the planarizing layer in various Tobben embodiments necessarily is 'capable of' performing as an [antireflective coating]." Respondents' brief at 17. They further argued that --

> [c]omplainants' argument that Tobben's planarizing layer does not "always" or "inevitably" act as an [antireflective coating] applies the wrong legal test. Under Complainants' test, a prior art reference anticipates a claim only if the claim reads on every embodiment disclosed in that reference. But that is not the

> law. If it were, then the oil can lid in the Harz reference would not have anticipated the *Schreiber* popcorn dispenser because some sizes could not be used for popcorn. Large lids would not dispense a few popcorn kernels at a time and small lids would not let any popcorn out. Yet the Harz reference anticipated the Schreiber popcorn lid because *one* potential oil can lid embodiment was inherently "capable of" performing the popcorn lid function.

Respondents' brief at 18.

Respondents reliance on *Schreiber* is misplaced. In finding the claim anticipated, the Patent Office relied on an illustration in the prior art, which the office scaled "up to the size necessary to fit a standard oil can without changing the proportions of the figure in any way." *Schreiber*, 44 USPQ2d at 1432-33. The illustration in the prior art Harz patent "was obviously not intended to be a full-sized representation" and the Harz patent specifically stated that its spout is useful for purposes such as dispensing oil from an oil can. *Schreiber*, 44 USPQ2d at 1430, 1432-33. In selecting a portion of the 300 Å to 2000 Å thickness range for the planarization layer disclosed in Tobben to support their inherency argument, respondents are not "scaling" the planarization layer, nor are they relying on an identified use for the disclosed structure.

Relying on *Atlas Powder Co. v. Ireco, Inc.*, 190 F.3d 1342 (Fed. Cir. 1999), respondents argued that even though the planarization layer disclosed in Tobben encompasses thickness values such that the disclosed layer lacks the claimed antireflective functionality, Tobben anticipates. Respondents' argued as follows:

> When the claimed structure encompasses a range of values and the prior art discloses a range of values, the prior art anticipates if there is *any* overlap between the claimed range and the prior art range. *Atlas Powder Co.*, 190 F.3d at 1346. In *Atlas Powder Co.*, the Federal Circuit held invalid a patent (Clay) that claimed explosive compositions in view of two prior art references (Egly and Butterworth)

that disclosed the same component materials in ratios that overlapped with the claimed ratios, as reflected in the following table from that case:

	Clay	Egly	Butterworth
Composition Contents			
Water-in-oil Emulsion	10-40%	20-67%	30-50%
Solid Ammonium Nitrate	60-90%	33-80%	50-70%
Emulsion Contents			
Ammonium Nitrate	70-90%	50-70%	65-85%
Water	About 3-15%	About 15-about 35%	[7]-27%
Fuel Oil	About 2-15%	About 5-about [20]%	2-27%
Emulsifier	0.1-5%	About 1-5%	0.5-15%

Although the prior art range included values outside the Clay range and the Clay range included values outside the prior art range, the Federal Circuit held that *any* overlap in the ranges would render the Clay patent anticipated, reasoning that:

> Anticipation of a patent claim requires a finding that the claim at issue "reads on" a prior art reference . . . . In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art. . . . Specifically, when a patent claims a chemical composition in terms of ranges of elements, any single prior art reference that falls within each of the ranges anticipates the claim.

Id. at 1346. Accordingly, the Federal Circuit held that the Egly patent anticipated the Clay patent even though the overlap between certain ingredient ratios was minimal (*e.g.*, Clay claimed water at about 3-15% and Egly claimed water at about 15% to about 35%).

> Here, as in *Atlas Powder Co.*, the prior art reference anticipates the disputed claim even though that reference also encompasses values outside the disputed claim. If Complainants' "inherency" argument were correct, the Federal Circuit would have reached the opposite result in *Atlas Powder Co.* because the disputed claim read on some Egly embodiment but not others. Here, Tobben anticipates the "second antireflective coating" limitation because in *some* Tobben invention embodiments, the planarization layer is inherently antireflective.

Respondents' brief at 19-20.

Respondents' argument is not persuasive. As pointed out by complainants, the general rule on which respondents rely, *viz.*, that a claim for a chemical composition in terms of ranges of elements is anticipated by a single prior art composition that includes elements within each of the ranges, is "a straightforward application of the law of anticipation, without regard to the doctrine of inherency." Complainants' brief at 63-64; *see also Titanium Metals Corp. v. Banner*, 778 F.2d 775, 782 (Fed. Cir. 1985) ("It is also an elementary principle of patent law that when, as by a recitation of ranges or otherwise, a claim covers several compositions, the claim is 'anticipated' if *one* of them is in the prior art") (citing *In re Petering*, 301 F.2d 676, 682 (CCPA 1962); *In re Gosteli*, 872 F.2d 1008, 1010 (Fed. Cir. 1989) (single prior art species within chemical composition patent's claimed genus anticipates). In this case, however, the Tobben prior art -- not the claim at issue -- discloses a range of values. *See, e.g., Ultradent Prods. Inc. v. Life-Like Cosmetics Inc.*, 127 F.3d 1065, 1071-72 (Fed. Cir. 1997) (claim to functionally defined chemical composition not anticipated by prior art reference disclosing a broad range of compositions) and cases cited therein.

Moreover the inherency analysis in *Atlas Powder* is inapposite to the present case. As discussed above, the planarization layer disclosed in the prior art Tobben patent lacks the claimed

antireflective functionality over part of the layer's disclosed thickness range of 300 Å to 2000 Å. Although respondents contended that "a Tobben planarization layer that, for example, is 300 Å at its thinnest and 500 Å at its thickest, *necessarily* will act as an [antireflective coating] – – every time" (respondents' brief at 18; *see also* respondents' brief at 10, 12-13), they provided no basis in the Tobben prior art providing that selection of this portion of the disclosed range of thicknesses is necessarily present. As discussed below, there is no indication that the claimed functional limitation found to be inherent in *Atlas Powder* ("sufficient aeration") is lacking in any part of the range of elements that the disclosed compositions in the prior art have in common with the claimed composition.

The inherency issue in *Atlas Powder* was whether the claimed "sufficient aeration . . . to enhance sensitivity" was present in the prior art explosive compositions. 190 F.3d at 1347. The "[s]ensitivity of a blasting composition refers to the ease of igniting its explosion." 190 F.3d at 1344. The *Atlas Powder* trial record "established that whether sufficient air is present in the explosive composition to facilitate detonation is a function of the ratio of the emulsion to the solid constituent." 190 F.3d at 1348. The claimed explosive composition (Clay) range was 10-40% emulsion and 60-90% solid. 190 F.3d at 1344. The comparable ranges for the prior art compositions were 20-67% emulsion (33-80% solid) (Egly) and 30-50% emulsion (50-70% solid) (Butterworth). The lower end (20%) of the Egly composition range (20-67% emulsion) and the lower end (30%) of the Butterworth composition range (30-50% emulsion) are within the claimed range of 10-40%. Thus, the emulsion ranges disclosed in Egly and in Butterworth overlap with the claimed range for all disclosed emulsion values up to 40%, while disclosed

values over 40% are outside the claimed range.

The Federal Circuit stated as follows:

> *The trial record contains exhaustive evidence regarding the inherency of both interstitial and porous air in the Egly and Butterworth compositions within the overlapping ranges.* The testimony from expert witnesses for both parties established that whether sufficient air is present in the explosive composition to facilitate detonation is a function of the ratio of the emulsion to the solid constituent. Dr. Clay testified that "if you mix porous prills, for example, with 30% typical water-in-oil emulsions, you're going to have air in there and it will detonate." Another of Atlas' experts testified that a mixture of 30% of either an Egly or a Butterworth emulsion, mixed with 70% standard fertilizer grade porous AN [ammonium nitrate] would have interstitial air, assuming nothing was done to disturb the size distribution of the AN prills. *The other experts agreed that the emulsions described in both Egly and Butterworth would inevitably and inherently have interstitial air remaining in the mixture up to a ratio of approximately 40% emulsion to 60% solid constituent.* The expert testimony supports the district court's conclusion that "sufficient aeration" is inherent in both Egly and Butterworth.
>
> *The district court also relied on evidence from several tests which showed that "sufficient aeration ... to enhance sensitivity" was inherently present within the overlapping ranges of the Clay patents and Egly and Butterworth.* In tests conducted with porous prilled AN combined with FO [fuel oil], stable detonations were obtained in every 8" diameter bore hole test where the percentage of emulsion ranged from 30% to 42.5%. Butterworth specifically discloses the use of porous prilled AN. Butterworth, p. 3, ll. 35-50. These tests, therefore, support the finding that "*[t]he emulsions described by Butterworth, combined with the ratios of ANFO [ammonium nitrate and fuel oil] disclosed by Butterworth, would inevitably and inherently have interstitial air remaining up to approximately 40% emulsion.*" The district court also found that the solid AN disclosed in Egly would have included porous prills. These tests, therefore, further support the court's finding that "*emulsions described in the Egly Patent, combined with either AN or ANFO, would inevitably and inherently have interstitial air remaining in the mixture up to approximately 40% emulsion to 60% solid constituent.*" This court discerns no clear error in the district court's conclusion that "sufficient aeration" was inherent in each anticipating prior art reference.

190 F.3d at 1348 (emphasis added). The Federal Circuit noted that Egly "teaches away" from air entrapment 190 F.3d at 1349. It stated that, although "showing that Egly did not recognize the function of the inherently present interstitial air," that teaching did not defeat inherency. 190

F.3d at 1349. The court further stated that – –

> even in Egly itself, the only way taught for removing interstitial air is the addition of more emulsion. *See [Egly patent]*, col. 1, ll. 50-55. Egly, however, teaches the use of a broad range - between 20% and 67% by weight - of water-in-oil emulsion. *See id.*, col. 3, ll. 21-24. *While Egly compositions containing amounts approaching 67% by weight of water-in-oil emulsions may have little or no entrapped air, the evidence established that at emulsion levels below 40%, Egly compositions "inevitably and inherently" trap sufficient amounts of air to enhance sensitivity.* This evidence included both substantial amounts of expert testimony and data showing extensive testing of Egly compositions.
>
> Finally, although the record showed that special mixing techniques - such as grinding and screening the AN particles - remove interstitial air from the blasting compositions, Egly did not teach or suggest any such techniques. Thus, *although Egly may have suggested removal of air, it nonetheless inherently contained interstitial aeration sufficient to enhance sensitivity when comprised of elements within the Clay patent ranges.*

190 F.3d at 1349 (emphasis added). In view of the above, we do not believe that *Atlas Powder* supports respondents' contention that the disclosed Tobben planarization layer of 300 Å to 2000 Å is an inherent disclosure of the claimed "second antireflective coating."

For the reasons discussed above, the Commission determined to reverse the ALJ's finding that the Tobben patent inherently discloses the "second antireflective coating" (claims 1, 3-4, and 5), and consequently, also to reverse the ALJ's findings that Tobben discloses etching the second antireflective coating (claim 4), and that Tobben anticipates claims 1, 3-4, and 5.

2. Whether the Tobben Patent Discloses the "Cap Layer" (claims 9 and 21)

The ALJ construed the term "cap layer" as a layer that consists of a material that is not conductive and which layer serves as an antireflective coating, a hard mask for metal line etching, and/or a protector for the top corners of metal wiring lines during the HDPCVD process. ID at 87-90, 119, 131. The Commission determined not to review this claim construction, and

thereby adopted it.

The ALJ found that the Tobben patent disclosed the "cap layer" of independent claim 9 (and dependent claims 11-13, and 20) and independent claim 21. ID at 130-33; FF 496-544. The Commission determined to review the ALJ's finding that the Tobben prior art disclosed the "cap layer" limitation. Having examined the record in this investigation, including the briefs and the responses thereto, the Commission determined to reverse the ALJ's factual finding that the Tobben patent discloses the "cap layer" of claims 9, 11-13, 20, and 21 of the '345 patent. For the reasons discussed below, the Commission determined that the planarization layer disclosed in Tobben does not inherently function as an antireflective coating, a hard mask for metal line etching, and/or a protector for the top corners of metal wiring lines during the HDPCVD process.

a. Whether Tobben discloses a cap layer that functions as an antireflective coating.

Respondents argued that "some embodiments of the invention disclosed in the Tobben patent may include a planarization layer with thickness values that fall squarely within the range for a quarter-wave plate [antireflective coating]" and "[t]hese planarization layers anticipate the '345 'cap layer.'" Respondents' brief at 22 (cross-referencing arguments concerning Tobben anticipation of "second antireflective coating"); respondents' reply at 43 ("Tobben's planarization layer is a 'cap layer' for the same reasons that it is an [antireflective coating]"). As discussed above, however, the Commission determined that Tobben's planarization layer does *not* inherently disclose the "second antireflective coating" of claim 1 because it is not antireflective throughout the range of thicknesses for the planarization layer.

Tobben also discloses a composite planarization layer (RX-70, col. 3, ll. 6-20)

embodiment with a bottom portion (16a) and an upper "cap layer" (16b). Tobben states that "[i]n one embodiment, the thickness of the cap layer is about 300-500 Å, preferably about 400-500 Å, even more preferably about 500 Å." RX-70, col. 3, ll. 18-20. Although respondents correctly recognized that the upper cap layer (16b) of Tobben's composite planarization layer does not disclose the "cap layer" of claim 21 (or the "second antireflective coating" of claim 1) of the '345 patent because Tobben's cap layer is deposited "on" the Tobben planarization layer, they contended that the upper cap layer (16b) of the composite planarization layer discloses the "cap layer" of claim 9.

Respondents' argument that the upper layer (16b) of Tobben's planarization layer discloses the "cap layer" of claim 9 of the '345 patent because layer 16b serves as an antireflective layer is unpersuasive. Although Tobben identifies restricted ranges, *e.g.*, 300 Å-500 Å of preferred thicknesses for the upper layer 16b of the composite planarization layer disclosed in the Tobben patent, those layers rest on a lower layer 16a. Respondents' argument that Tobben discloses materials other than silicon dioxide for this lower layer is unpersuasive because the passage in the Tobben specification on which they rely (RX-70, col. 2, ll. 57-63) concerns a different embodiment of the planarization layer. In discussing the composite planarization layer embodiment, Tobben states that the material for the layer 16a is "spun-on silicon dioxide glass." RX-70, col. 3, ll. 6-20. Although Tobben states that the upper layer (16b) "comprises a dielectric material," respondents have not identified evidence in the record establishing that a dielectric material other than silicon dioxide (expressly disclosed in RX-70, col. 3, ll. 12-15) would operate as an antireflective coating when applied on top of a silicon

dioxide planarization layer. Finally, because respondents have offered no explanation why two layers of the same material (*i.e.*, silicon dioxide) would not function optically as a single layer, they have not demonstrated that the upper layer 16b of Tobben's composite planarization layer discloses the cap layer of claim 9 of the '345 patent. Consequently, the Commission determined that the Tobben patent does not disclose a cap layer that functions as an antireflective layer.

b. Whether Tobben discloses a cap layer that functions as a hard mask.

The '345 patent specification states that when the cap layer is used as a hard mask for wiring line etching, the photoresist is removed before the cap layer acts as a mask:

> the cap layer 28 may also be used as a hard mask for wiring line etching. In embodiments where the cap layer is used as a hard mask for wiring line etching, the etching is accomplished in a two step process in which the photoresist layer 30 acts as a mask during the first etch step, and the cap layer 28 acts as a mask during the second etch step. The first etch step etches through the portions of the cap layer that [are] not covered by the photoresist. The second etch step etches through the protective layer 26, the wiring layer 24 and the surface layer 22. By carrying out the etching process in two steps with the photoresist being removed prior to the second etching step, the likelihood of contaminants, such as carbon compounds from the photoresist layer, being deposited deep within the gaps 36 between wiring lines 34 is decreased. Alternatively, the etching can be carried out in a process in which the photoresist is used as the mask for etching all of the layers. This alternative process is faster, but runs a greater risk of contamination that could adversely affect device performance.

'345 patent, col. 8, ll. 33-51. The ALJ construed the term "hard mask." to require removal of the photoresist before the hard mask is used for etching. *See* FF 225 ("A hard mask is a layer which is etched using the photoresist as a mask, followed by removal of the photoresist to leave the patterned hard mask layer which then serves as a mask for subsequent etching of underlying layers. Yang Tr. 1613:5-18; Lee Tr. 1661:14-18; Peltzer Tr. 1808:22 to 1809:22") (FF 225 is found in the section of the ID's findings of fact labeled V.A ("Infringement of the '345 Patent,"

"Claim Construction")). No party challenged the ALJ's construction of the term "hard mask" or FF 225 in its petition for review. The Commission determined not to review the ID's claim construction with respect to the '345 patent, and thereby adopted it.

Respondents contended in their response to the petitions for review that Tobben's planarization layer may function as a hard mask. They argued that Tobben explicitly states that a second "mask 28" is "formed within the planarization layer 16," exposing portions of the metal layer 14, which are then "etched away" to form the conductive wires. Respondents' response at 24 (citing RX-155 [the Tobben patent] at Col. 3, lines 51-58); *see also* FF 510 and 511. The portion of the Tobben patent cited by respondents reads as follows:

> [n]ext, *using remaining portion of the photoresist masking layer 18*, and the second mask 28 formed within the planarization layer 16, *i.e.*, with the second mask 28 exposing underlying nonplanar surface portions of the metal layer 14, the exposed portions of the metal layer 14 are etched away using RIE to form the plurality of electrically conductive wires 36 over the dielectric layer 13, as shown in [figure] 4.

RX-155, col. 3, lines 51-58 (emphasis added). Because the italicized portion of the above-quoted excerpt indicates that the photoresist has not been removed, the passage does not demonstrate that the "mask 28" formed within Tobben's planarization layer 16 is being used as a "hard mask," as that term is construed by the Commission. Consequently, the Commission determined that the Tobben patent does not disclose a cap layer that functions as a hard mask.

c. Whether Tobben discloses a cap layer that functions as a top corner protector.

The ALJ did not identify specific support in the record for his finding that the Tobben patent discloses a "cap layer" that functions as a top corner protector. ID at 131 ("Respondents logically argue that because the planarization [layer] may be left on the TiN layer during the HDP

CVD gap filling, it would necessarily function to protect the TiN layer and the metal wiring lines during this step"). In their briefing to the Commission, respondents contended that Tobben's planarization layer (and the cap layer in Tobben's composite planarization layer embodiment) "inherently acts as a sacrificial barrier between the wiring lines and the etching component of the HDPCVD process in embodiments where only the photoresist is removed before HDPCVD processing." Respondents' brief at 22; *see also* respondents' reply at 53-54. However, respondents' argument is not persuasive, and the ALJ's finding cannot stand without support in the record.

As pointed out by complainants in their petition for review and in their briefing to the Commission, a layer that is etched all the way through in the HDPCVD process does not function as a top corner protector.[13] In response to complainants' petition for review, respondents asserted that – –

> there is no question that Tobben's 300 to 2000 angstrom thick silicon dioxide layer will play no less a top corner protective function than the 'cap layer' disclosed in the '345 patent. Indeed, the '345 [patent] specifically discloses an embodiment of the invention in which "silicon dioxide is used for cap layer 28." RX-40 at col.7, line 52. Complainants identify absolutely no distinction between Tobben's silicon dioxide "cap layer" and the silicon dioxide "cap layer" in this '345 patent embodiment.

Respondents' response at 24; *see also* respondents' brief at 22 ("the Tobben 'cap layer' necessarily will be 'sacrificially etched during the HDPCVD processing' as described in the '345 patent") (quoting '345 patent, col. 6, ll. 34-36). We agree with complainants that this response of

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[13] In his infringement analysis, the ALJ found that a layer in respondents' process that does not prevent the HDPCVD process from eroding the underlying TiN layer did not function as a protective layer within the meaning of the '345 patent's "cap layer." ID at 119. No party challenged the ALJ's infringement analysis in the petitions for review. The Commission determined not to review the ID in this regard, and thereby adopted it.

respondents is inadequate support for respondents' argument that Tobben's silicon dioxide layer *inherently* functions as a top corner protector because the '345 patent expressly acknowledges that its cap layer does not *always* function as a top corner protector. '345 patent, col. 8, ll. 52-54 ("the cap layer 28 *may* also act as a wiring line top corner protector during subsequent HDPCVD processing") (emphasis added). Consequently, the Commission determined that the Tobben patent does not disclose a cap layer that functions as a top corner protector.

d. Conclusion.

Respondents bear the burden of proof on the issue of whether Tobben discloses the cap layer, and for the reasons discussed above, the Commission determined that they have failed to carry it. Consequently, the Commission determined to reverse the ALJ's factual finding that the Tobben patent discloses the "cap layer" of claims 9, 11-13, 20, and 21 of the '345 patent.

3. Whether Claim 13 Is Made Obvious by the Tobben Patent.

Claim 13 depends from claim 9, which the ALJ found anticipated by the Tobben prior art.[14] The Commission determined to review the ALJ's conclusion that claim 13 is made obvious by the Tobben patent in view of the knowledge of a person of ordinary skill in the art. The Commission requested briefing on the following question: "Assuming that claim 9 of the '345 patent is anticipated by the Tobben patent, is claim 13 obvious?" Having examined the record in this investigation, including the briefs and responses thereto, the Commission determined to reverse the ALJ's conclusion of obviousness on the independent, alternative ground that

[14] As discussed above, the Commission determined that claim 9 is not anticipated by the Tobben patent, and consequently determined to reverse the ALJ's conclusion that dependent claim 13 is made obvious by the Tobben patent.

respondents have not identified a suggestion or motivation to modify the Tobben reference to use a silicon nitride or an oxynitride for the cap layer.

An analysis of obviousness requires determinations regarding the scope and content of the prior art; the differences between the prior art and the claimed invention; the level of ordinary skill in the art; and any so-called "secondary" or "objective" indicia that the invention is nonobvious, such as commercial success, copying, or a long-felt but unmet need. *Graham v. John Deere Co.*, 383 U.S. 1, 17. In addition, there must be some *suggestion* to combine the references, for it is impermissible to use hindsight to piece the invention together using the patented invention as a template. *See, e.g., Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1385 (Fed. Cir. 2001); *Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1348 (Fed. Cir. 2000); *Heidelberger Druckmaschinen AG v. Hantscho Commercial Prods., Inc.*, 21 F.3d 1068, 1072, 30 U.S.P.Q.2d 1377, 1379-80 (Fed. Cir. 1994). Even when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference. *In re Kotzab*, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). The motivation to select the combination of components used by the inventor is an "essential evidentiary component of an obviousness holding." *C.R. Bard, Inc. v. M3 Sys., Inc.*, 157 F.3d 1340, 1352 (Fed. Cir. 1998) (reversing jury verdict based on obviousness where no prior art provided teaching or showing of motivation to modify prior art). Although the ultimate question of obviousness is a question of law based on underlying factual issues, *see, e.g., Richardson-Vicks Inc. v. Upjohn Co.*, 122 F.3d 1476, 1479 (Fed. Cir. 1997), whether a motivation to combine references has been demonstrated is a question of fact. *Winner Int'l*, 202 F.3d at 1348.

Respondents acknowledged that "[i]t is undisputed that Tobben does not specifically disclose the use of a silicon nitride material or an oxynitride material to form the cap layer. Tobben only teaches the use of silicon dioxide for that purpose." Respondents' response at 25. Respondents asserted that the motivation to combine a silicon nitride or an oxynitride material with the Tobben reference is found in the Tobben patent's teaching that the cap layer is made from a dielectric material. Respondents' brief at 31 (citing RX-70, col. 3, ll. 10-11). Respondents maintained that one of ordinary skill in the art would know that silicon nitride and oxynitride are dielectric materials. The Tobben specification reads in relevant part as follows:

> Alternatively, the planarization layer 16 comprises, for example, a composite layer as shown in FIG. 2B. As shown, the composite planarization layer 16 includes a spun-on silicon dioxide glass as a bottom portion 16a and a cap or upper layer 16b formed thereon. The cap layer comprises a dielectric material. The cap layer promotes adhesion between the photoresist and the planarizing layer. In one embodiment, the cap layer 16b comprises silicon dioxide formed by, for example, plasma enhanced chemically vapor deposited (PE CVD).

RX-70, col. 3, ll. 6-15. Respondents argued that "[a] finite number of microchip fabrication materials are 'dielectric' materials, [and] silicon nitrides, oxynitrides, and silicon dioxide all fall within this category. It would be obvious to a person skilled in the art to substitute one material for another material in the same category." Respondents' brief at 31 (citing *In re Raynes*, 7 F.3d 1037 (Fed. Cir. 1993); *Smith v. Hayashi*, 209 USPQ 754, 759 (Bd. of Pat. Inter. 1980)). Complainants and the IA argued that Tobben does not motivate one of skill in the art to substitute any dielectric material for silicon dioxide, but only those dielectric materials that would also possess the other properties of silicon dioxide that Tobben associates with the functioning of the cap layer (*e.g.*, promot[ing] adhesion between the photoresist and the

planarizing layer).

In re Raynes is on point. That case involved a patent application for the invention of an interactive automobile service station having a programmable video display (a cathode ray tube (CRT)) at the fuel pumps. The Patent Office rejected the Raynes claim in question as made obvious by a prior art patent (Savary) that disclosed all of the limitations except the programmable video display at the fuel pumps. Although the Savary patent disclosed fuel pumps having a display panel at the pumps (a light emitting diode (LED) or liquid crystal display (LCD)) for displaying the price and quantity of the fuel, Savary's panel was not a video display. The Savary patent stated that the display system can be any conventional system but, in the present embodiment, it comprises using a seven segment display. *Raynes*, 7 F.3d at 1039. The Patent Office found that a CRT video display is a conventional display system, and held that it would have been obvious to replace Savary's display system with a video-capable CRT. *Raynes*, 7 F.3d at 1039. On appeal, the Raynes applicant argued that the Savary patent "contemplated no more than the display of fuel quantity and price information using a system conventional for that purpose," and further argued that the Savary display system required different circuitry than a video system. *Raynes*, 7 F.3d at 1039-40. The Federal Circuit affirmed the Patent Office rejection.

In *Raynes*, the Federal Circuit stated that "[t]he question presented by the Raynes application is *not whether the CRT, the LED, and the LCD are known display systems*, but whether Raynes' combination including video display at the fuel pump would have been obvious to a person of ordinary skill." *Raynes*, 7 F.3d at 1039 (emphasis added). In affirming the Patent

Office's conclusion that "the combination of video display with the display of other information at the fuel pump would have been obvious to a person of ordinary skill," the Federal Circuit took judicial notice of the fact that "the use of video to display programming and other information is . . . ubiquitous." *Raynes*, 7 F.3d at 1040. *Raynes* suggests that the issue before the Commission on review is not whether silicon nitride, oxynitride, and silicon dioxide are dielectric materials, but whether the use of silicon nitride or oxynitride for the cap layer as claimed in claim 13 of the '345 patent would have been obvious to a person of ordinary skill in the art. *Raynes* provides no support for respondents' assumption that the restrictive purpose (*viz.*, "promot[ing] adhesion between the photoresist and the planarizing layer," RX-70, col. 3, ll. 11-12) for the cap layer disclosed in Tobben is irrelevant. The Commission agrees with complainants and the IA that Tobben does not motivate one of skill in the art to substitute any dielectric material for silicon dioxide, but only to substitute those dielectric materials that would also possess the other properties of silicon dioxide that Tobben associates with respect to the functioning of the disclosed cap layer.[15]

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[15] We do not understand respondents' reliance on *Smith v. Hayashi*. That case concerned an interference between the Hayashi patent and the Smith application. The Federal Circuit phrased the issue as "whether the use of vitreous selenium itself is patentably distinct from the generic concept claimed by Smith et al. [a layer of amorphous (vitreous) selenium, a selenium alloy, or a powdered or sintered photoconductive layer such as cadmium sulfoselenide or phthalocyanine] *in the environment of the invention defined by the involved patent claim* (and count)." 209 USPQ at 759 (emphasis in original). The court noted that the "key to the issue" was "the equivalence set up by the Smith et al. disclosure with respect to the *environment of their claim*." 209 USPQ at 759 (emphasis in original). "The Smith et al. disclosure makes it clear that various prior art photoconductors used in electrophotography, including selenium, its alloys and [phthalocyanine] may be used in their [photoconductive] layer 'b'." 209 USPQ at 759. The court concluded that "the disclosure of Smith et al. shows that both [phthalocyanine] and selenium are known *photoconductors in the art of electrophotography*. This, in our view, presents strong evidence of obviousness in substituting one for the other *in an electrophotographic environment as a photoconductor*." 209 USPQ at 759 (emphasis added). *Smith* provides no support for respondents' assumption that the restrictive purpose for the cap layer disclosed in Tobben is irrelevant.

Relying on *In re Dillon*, 919 F.2d at 691-92, respondents further maintained that claim 13 is obvious in view of Tobben combined with complainants' '701 patent, which latter patent "teaches that the claim 13 materials -- silicon nitride and oxynitride materials -- are analogous compositions to silicon dioxide (Tobben's preferred 'cap layer' embodiment) for use as antireflective materials." Respondents' brief at 31. Respondents did not contest complainants' point that these arguments were not raised before the ALJ, but asserted that the Commission should consider respondents' '701 patent argument because the '701 patent was in the record, the Commission has the authority to make findings and conclusions on the record (Commission rule 210.45(c)), and "appellees always have the right to assert alternative grounds for affirming the judgment that are supported by the record" (*MEHL/Biophile*, 192 F.3d at 1366). Respondents' reply at 56. The Commission declines to consider these arguments because they were not raised before the ALJ. *Hazani v. United States Int'l Trade Comm'n*, 126 F.3d 1473, 1476-77 (Fed. Cir. 1997). Respondents' reliance on *MEHL/Biophile* is misplaced because the argument that the Federal Circuit considered in *MEHL/Biophile*, while not reached by the district court, had been presented to the district court.[16] 192 F.3d at 1363, 1366.

For the reasons discussed above, the Commission determined to reverse the ALJ's legal conclusion that claim 13 is obvious in view of Tobben based on the absence in the prior art of the requisite motivation to modify the Tobben reference.

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[16] In any event, respondents' *Dillon* argument concerning the '701 patent is not persuasive in light of our conclusion discussed *supra* that neither Tobben's planarization layer nor Tobben's upper cap layer of the composite planarization layer are disclosures of the antireflective functionality aspect of the '345 patent cap layer or of the "second antireflective coating."

B. The Abernathey Patent

The ALJ found claims 1, 3-5, 9, 11-13, 20, and 21 of the '345 patent are invalid as made obvious by the Abernathey patent in combination with either the Pan (RX-82), Yagi (RX-85), or Yota (RX-86) publications. ID at 138-40. He found that every element of those claims is disclosed in the prior art Abernathey patent, except the step of HDPCVD deposition "within the gaps" "to fill the gaps" (claims 1, 9, and 21), which step is disclosed in each of the Pan, Yagi, and Yota publications. ID at 134 n.62, 138.

The Commission determined to review the ALJ's conclusion that those claims are invalid as made obvious by the Abernathey patent in combination with the Pan, Yagi, and/or Yota publications. In the petitions for review and briefing to the Commission on this issue, the parties disputed the following six issues: (1) whether Abernathey discloses the "second antireflective coating" (claim 1), (2) whether Abernathey discloses the "cap layer" (claims 9 and 21), (3) whether respondents established that the Yota, Pan, and Yagi references are prior art to the '345 patent, (4) whether respondents established a motivation to combine the Yota, Pan, and Yagi references with Abernathey for the gap filling step of HDPCVD deposition, (5) whether Abernathey combined with Yota, Pan, or Yagi discloses etching the second antireflective coating (claim 4) or etching the cap layer (claim 12), and (6) whether Abernathey combined with other prior art renders obvious a cap layer comprised of silicon nitride or oxynitride (claim 13). The Commission's resolution of each of the specific issues disputed by the parties is discussed more fully below.

In sum, the Commission determined to affirm the ALJ's conclusion that the Abernathey

patent in combination with other prior art renders claims 1, 3-5, 9, 11-12, 20, and 21 obvious, but to reverse his conclusion that the combination renders claim 13 obvious. The Commission determined that the "second antireflective coating" (claims 1, 3-4, and 5) is not disclosed expressly or inherently in the Abernathey patent. The Commission determined, however, that one of ordinary skill in the art would have found it obvious to modify the Abernathey patent's barrier layer of silicon dioxide to act as a second antireflective coating on top of an antireflective coating of titanium nitride by selecting a thickness for the silicon dioxide layer in which the layer acts as an antireflective coating. The Commission further determined that, because the Abernathey patent's silicon dioxide barrier layer when so modified functions as an antireflective layer, the silicon dioxide barrier layer also meets the "cap layer" limitation of claims 9 and 21 for obviousness purposes. The Commission determined to affirm the ALJ's conclusion that the Yota, Pan, and Yagi references are prior art, to adopt the ALJ's findings with respect to motivation to combine the Abernathey, Pan, Yagi, and Yota prior art for the gap filling step of HDPCVD deposition, and to adopt the ALJ's findings and conclusions with respect to the etching limitations (claims 4 and 12).

1. Whether Abernathev Discloses the "Second Antireflective Coating" (claim 1)

Complainants argued that respondents have not met their burden of showing by clear and convincing evidence that Abernathey discloses the second antireflective coating elements of claim 1. Respondents argued that the "second antireflective coating" is expressly disclosed in Abernathy and inherently disclosed in Abernathey's silicon dioxide barrier layer. The Commission determined that the "second antireflective coating" (claims 1, 3-4, and 5) is not

disclosed expressly or inherently in the Abernathey patent. The Commission determined, however, that one of ordinary skill in the art would have found it obvious to modify the Abernathey patent's barrier layer of silicon dioxide to act as a second antireflective coating on top of an antireflective coating of titanium nitride by selecting a thickness for the silicon dioxide layer in which the layer acts as an antireflective coating.

Respondents' arguments that the Abernathey prior art discloses the "second antireflective coating" of the '345 patent because Abernathey states that its barrier layer is intended to reduce reflectivity or because Abernathey's silicon barrier layer functions as an antireflective coating are unpersuasive. In support of their first argument, respondents relied on language in the Abernathey patent at col. 2, lines 40-44, *viz.*, "[y]et another object of this invention is to provide a satisfactory barrier that avoids undesirable interactions while at the same time providing a technique that achieves photolithographic low reflectivity." However, this statement should not be understood as identifying the achievement of photolithographic low reflectivity as a function of the barrier layer, in view of other statements in the specification teaching an antireflective coating (preferably titanium nitride) and a barrier layer of silicon or SiO_2 that prevents interactions between the photoresist and the titanium nitride layer. *See, e.g.*, Abernathey patent, col. 2, ll. 51-66; col. 3, ll. 7-10; col. 3, ll. 67-68; col. 4, ll. 36-38.

As to whether the disclosed silicon barrier is antireflective, respondents' expert (Peltzer) stated during cross-examination that the silicon layer described in Abernathey does not serve as an antireflective coating. Trans. (Peltzer) at 945:15-946:13. The statements in complainants' prior art '701 patent (RX-46 at col. 2, ll. 39-41; col. 3, lines 18-20) on which respondents rely in

support of their argument, *viz.*, that amorphous silicon is a well-known antireflecting material, are less persuasive on this factual issue than statements of respondents' expert that are based on that expert's models of the silicon layer on top of titanium nitride disclosed in Abernathey. *Cf.* Trans. (Peltzer) at 943:9 - 946:7, RPX-46.

Respondents' argument that Abernathey's SiO_2 (spun on glass) barrier layer inherently discloses the "second antireflective coating" is not persuasive. Respondents have represented to the Commission that the "thin" silicon dioxide barrier layer in Abernathey is spun-on at thicknesses between 1000 Å and 1500 Å. Respondents' reply at 77 ("The parties agree that Abernathey discloses a 'thin' SiO_2 layer that is 1000 Å-1500 Å thick."), 78 ("Respondents do not contest the testimony from Complainants' expert that SiO_2 is spun-on at thicknesses between 1000 Å and 1500 Å" (citing respondents' brief at 35-36, 130-31)). As discussed in our anticipation analysis of the Tobben prior art, for a layer that is disclosed in terms of a range of thicknesses "inherently" to disclose a claimed function, the layer must exhibit the claimed functionality throughout the disclosed range. Respondents have not identified evidence in the record that would establish that a SiO_2 (spun on glass) layer will necessarily be antireflective for all thicknesses between 1000 Å and 1500 Å.[17] Consequently, respondents have not met their burden of proof on this issue. *Superior Fireplace Co. v. Majestic Prods. Co.*, 270 F.3d 1358, 1367 (Fed. Cir. 2001) (challenges to claim validity must be proved by clear and convincing

[17] In their post hearing reply brief (Nov. hearing), respondents stated that "[c]ontrary to [c]omplainants' and the [s]taff's erroneous allegations, between 300 angstroms and 2000 angstroms there are only two 180 angstrom thick ranges when silicon dioxide is not an antireflective coating using destructive interference for DUV light at 248 nm. RPX-46 (between about 640 angstroms and 820 angstroms *and between about 1370 angstroms and 1550 angstroms*)." Respondents' post hearing reply brief (Nov. hearing) at 21 (filed December 27, 2001) (emphasis added).

evidence); *Am. Hoist & Derrick Co. v. Sowa & Sons, Inc.*, 725 F.2d 1350, 1360 (Fed. Cir. 1984) (burden of proving invalidity is on patent challenger and "that burden is constant and never changes and is to convince the court of invalidity by clear evidence").

In support of their argument that Abernathey's SiO_2 (spun on glass) layer functions as an antireflective coating, respondents rely on (1) FF 564, (2) the testimony of their expert (Peltzer) at 857:6-23, (3) the Dean reference (RX-177 at 519, ID at 137), and (4) complainants' prior art '701 patent. With respect to FF 564, respondents asserted that "the ALJ properly found that within [the] thickness range [of 1000 Å to 1500 Å], SiO_2 is antireflective—*i.e.*, this range encompasses an odd integer multiple of the quarter-wave plate thickness." Respondents' brief at 35. The ALJ's finding of fact, FF 564, reads as follows: "Calculations of reflectivity of the type that an engineer would rely on concerning work related to the subject matter of the '345 patent demonstrate that the titanium nitride layer and the SiO2 on top in the Abernathey patent is the same as the first and second antireflective coatings formed on the metal wiring line in claim 1 of the '345 patent." FF 564. This finding makes no mention of the range of thicknesses of the SiO_2 layer. Consequently, and contrary to respondents' contention, it is not a finding that the layer will necessarily be antireflective for all thicknesses between 1000 Å and 1500 Å.

Respondents relied on the following testimony of their expert (Peltzer):

> Q Mr. Peltzer, are these mathematical calculations of reflectivity, is this something that an engineer would rely upon in the course of his work with respect to the subject matter of the '345 patent and antireflective coatings?
>
> A Yes, it's common.
>
> Q And does this evidence -- I'm sorry, your Honor.

> Does the calculation in RPX-46 support your opinion that the Abernathey patent with the silicon oxide and the Tobben patent with the silicon oxide discloses a second antireflective coating on top of the titanium nitride layer?
> A Yes.
>
> Q In your opinion, is there any doubt that the silicon oxide layer in the Abernathey patent and the silicon oxide layer in the Tobben patent are second antireflective coatings above the titanium nitride layer?
> A No.

Trans. (Peltzer) at 857:12-23. Respondents asserted that the above-quoted testimony "based on standard antireflectivity calculations . . . establishes that Abernathey's 1000-1500 Å SiO_2 barrier layer would function as a second [antireflective coating]." Respondents' reply at 58-59. RPX-46, the exhibit referred to in the above-quoted testimony, concerns calculations of the amount of reflection from the surface of an aluminum layer overcoated by materials such as titanium, titanium nitride, silicon, and SiO_2. Trans. (Peltzer) at 848:18-849:17. The calculations that Peltzer identified as corresponding to the Abernathey patent's SiO_2 layer over titanium nitride involve SiO_2 thicknesses up to 250 Å, rather than thicknesses between 1000 Å and 1500 Å.[18] Trans. (Peltzer) at 849:21-857:5; 954:2-13. At the hearing, Peltzer testified on cross-examination that Abernathey's reference to a "thin" SiO2 layer disclosed a layer with a thickness on the order of 250 Å. Trans. (Peltzer) at 958:21-959:21. Consequently, Peltzer's testimony cannot be understood as establishing that the SiO_2 barrier layer of Abernathey, at thicknesses throughout the range of 1000 Å to1500 Å, would function as a second antireflective coating.

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[18] Peltzer testified that other calculations in RPX-46 involving a SiO_2 layer of 10 Å to 1200 Å concerned the Tobben prior art. Trans. (Peltzer) 854:19-855:18.

Respondents also point to the Dean reference, specifically the passage reproduced in the ID at 137 n.63, in support of their argument that Abernathey's SiO_2 (spun on glass) barrier layer inherently discloses the "second antireflective coating." But the cited passage in the Dean reference refers only to a 100 nm (1000 Å) silicon dioxide film on TiN, and respondents offered no explanation as to how Dean's mention of this specific thickness can be extended to other thicknesses in the range of 1000 Å to1500 Å. Similarly, respondents argued based on complainants' '701 patent that a silicon dioxide film at a thickness value of 1275 Å would be antireflective when exposed to DUV light. Again, respondents offered no explanation as to how this argument applies to other thicknesses in the range of 1000 Å to1500 Å. Indeed, in response to complainants' argument that the 1275 Å value is inconsistent with the testimony of respondents' expert identifying the quarter wave plate thicknesses of 300, 900, 1500, and 2100 Å, respondents conceded that Peltzer's calculations result in "a slightly different set of values than those taught by the '701 patent." Respondents' reply at 59. Respondents have failed to prove that Abernathey's SiO_2 (spun on glass) barrier layer inherently discloses the "second antireflective coating."

Although respondents' arguments that the Abernathey patent's barrier layer expressly or inherently disclose the "second antireflective coating" are unpersuasive, the following passage in the ID may also be understood as relating to obviousness:

> At the time of the alleged invention of the '345 patent, one skilled in the art would have known that a TiN layer could be replaced by a better antireflective coating, or that a second antireflective coating could be used in addition to TiN. *See, e.g.*, Fair Tr. 1108-1109; RX-46. Furthermore, that a layer of silicon dioxide can serve as an antireflective layer, and that such information would be available to engineers using ordinary calculations of reflectivity, has already been addressed in connection with

> Tobben. Moreover, references such as RX-282 (*Silicon Processing for the VLSI Era, Vol. 1: Process Technology* by Wolf) [the "Wolf" publication] at 371-73, which discusses the sputter deposition of silicon dioxide to provide dielectric layers, and RX-177 (*SPIE* Vol. 2438: "Investigations of deep ultraviolet photoresists on TiN substrates" by Dean,et al.)(the "Dean" publication) at 519.[19] which discusses the use of silicon dioxide on TiN, demonstrates that the titanium nitride layer and the silicon dioxide on top, which is disclosed in Abernathey, satisfies the requirement of claim 1 of a first and second antireflective coating formed on the wiring line.

ID at 137. In their petition for review, complainants stated that "[i]t is not clear why the ALJ concluded that one of ordinary skill would modify the Abernathey patent's silicon or spin-on glass barrier layer to be an [antireflective coating]." Complainants' petition at 69. They argued that "[w]ith Abernathey's solution to the 'footing' problem in hand, one of ordinary skill would understand that TiN is an adequate antireflective coating for deep ultraviolet photolithography and would have no motivation to alter Abernathey's silicon or spin-on glass barrier layer in any respect."[20] Complainants' brief at 96.

The motivation to modify a reference may come from the nature of the problem to be solved. *Pro-Mold & Tool Co. v. Great Lakes Plastics Inc.*, 37 USPQ2d 1626, 1630 (Fed. Cir. 1996). In their petition for review, complainants described certain problems that led to the

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[19] [This footnote is number 63 in the ID at 137.] The Dean publication states in part:

> Ultimately, the deposition of a 100 nm silicon dioxide film on the TiN effectively blocked proton access to the TiN film and eliminated footing. This observation provides one possible solution to DUV resist footing on TiN--deposit a thin inorganic layer that could act as an antireflective layer and that is easily removed (during the plasma etch stop?). Most organic spin-on antireflective layers also provide the necessary barrier layer, but those films are problematic due to defects, added cost, and etch complications

RX-177 at 519.

[20] The ALJ's findings explain the footing problem as follows: "When photoresist is applied to the top of a titanium nitride layer and exposed, there is a footing problem that can lead to loss of control of critical dimensions with the required precision or accuracy. The footing problem is that the base of the photoresist pattern gets wider due to interaction with the titanium nitride layer." FF 290 (citing Trans. (Peltzer) at 1731:20-1732:3).

solutions of the '345 patent as follows: "The inventions in the '345 patent came about because the technologies used to manufacture integrated circuits with relatively larger feature sizes (1.0 micron down to 0.35 microns) were found to be inadequate as the leading companies in the industry began manufacturing integrated circuits with feature sizes of 0.25 microns and smaller in the 1996-97 time period." Complainants' petition at 31. Complainants noted that "[m]ore specifically, the '345 patent provided a 'process integration solution' to . . . problems encountered in moving to the manufacture of circuits with minimum feature sizes of 0.25 microns and smaller [including] movement from I-line light sources to deep ultraviolet ("DUV") light sources for photolithography, which in turn required improved antireflective functionality." Complainants petition at 31 n.9. Respondents have identified record evidence that rebuts complainants' argument that one of ordinary skill would have no motivation to modify Abernathey's barrier layer. As pointed out by respondents, a co-inventor of the '345 patent, Dr. Lur, testified that TiN is not sufficiently antireflective under the light source at issue (DUV light), and that DUV light was necessary to 0.25 micron feature size process technologies. Trans. (Lur) at 47:5-10; 47:16-48:3; *see also* Trans. (Lur) at 39:6-40:11. Thus, one skilled in the art using the Abernathey invention under DUV light would have been dissatisfied with the reflectivity of the TiN layer.

As the ALJ found, at the time of the alleged invention of the '345 patent, one skilled in the art would have known that a TiN layer could be replaced by a better antireflective coating, or that a second antireflective coating could be used in addition to TiN. ID at 137 (citing Trans. (Fair) at 1108-1109). Although as discussed, *supra*, the Commission determined to reverse the ALJ's ultimate findings that the Tobben prior art anticipates, we do not question that a layer of

silicon dioxide *can* serve as an antireflective layer at *some* thicknesses, and that that information would be available to engineers using ordinary calculations of reflectivity. Moreover, the passage from the Dean publication[21] quoted in the ID at 137 n.63 concerning the use of a 1000 Å silicon dioxide film on TiN to eliminate the footing problem (*i.e.*, the same problem and solution attributed to the Abernathey patent by complainants in their petition for review at 65) states that such a silicon dioxide film could act as an antireflective layer.[22] Therefore, one skilled in the art using the Abernathey invention under DUV light would have found it obvious to modify the silicon dioxide barrier layer to act as a second antireflective coating by selecting a thickness for the silicon dioxide layer in which the layer acts as an antireflective coating.

2. Whether Abernathey Discloses the "Cap Layer" (claims 9 & 21)

Complainants contended that claims 9 and 21 are not made obvious because the Abernathey patent's silicon dioxide layer does not serve as a "cap layer." The ALJ construed the term "cap layer" as a layer that consists of a material that is not conductive and which layer serves as an antireflective coating, a hard mask for metal line etching, and/or a protector for the top corners of metal wiring lines during the HDPCVD process. ID at 87-90, 119, 131. The Commission determined not to review this claim construction, and thereby adopted it. Complainants asserted that the ALJ did not find that Abernathey's silicon dioxide layer serves as a top corner protector. They argued that Abernathey's silicon dioxide layer does not act as an

[21] Complainants' argument that no weight should be given to the Dean reference is unpersuasive. Complainants cite no legal authority supporting their argument in their petition for review. *See* Commission rule 210.37(b).

[22] Therefore, the IA's argument that Abernathey "teaches away" from an antireflective silicon dioxide barrier layer is unpersuasive given the parties' agreement that the range of thicknesses for the silicon dioxide barrier layer includes 1000 Å.

antireflective coating, cross-referencing their argument concerning the second antireflective coating (claim 1). With respect to the hard mask function, complainants asserted that the testimony of respondents' expert relied upon by the ALJ in FF 565 is insufficient to prove obviousness because it is conclusory and supports only the possibility that the silicon dioxide layer would serve as a hard mask.

As discussed in the previous section, the Commission determined that one of ordinary skill in the art would have found it obvious to modify the Abernathey patent's barrier layer of silicon dioxide to act as a second antireflective coating on top of an antireflective coating of titanium nitride by selecting a thickness for the silicon dioxide layer in which the layer acts as an antireflective coating. When so modified to function as an antireflective coating, the Abernathey patent's silicon dioxide barrier layer also meets the "cap layer" limitation of claims 9 and 21 for obviousness purposes. Consequently, the Commission determined to affirm the ALJ's conclusions that claims 9 and 21 are invalid as made obvious by the Abernathey patent in view of Dean combined with the Yota, Pan, or Yagi prior art, with the clarification that the silicon dioxide barrier layer (when modified as discussed *supra* to act as a second antireflective coating) on top of a first antireflective coating of titanium nitride meets the "cap layer" limitations of claims 9 and 21.[23]

The ID provided no specific citations to the record in support of its finding that "the silicon dioxide layer in Abernathey (especially in view of Dean) forms a cap layer which protects

[23] The "cap layer" of claim 21 is "disposed on the top surface of the protective layer" (claim 21), and "the titanium nitride layer between the SiO2 layer and the metal wiring line in Abernathey (and/or Dean) is the same as the protective layer in claim 21 of the '345 patent" (ID at 138).

and serves as a hard mask during etching if there is HDP CVD deposition as required by claim 9" (ID at 137-38). The ALJ's finding of fact, FF 565, states that "[t]he SiO2 layer on top in the Abernathey patent would serve as a cap layer to protect and *possibly* serve as a hard mask during etching if HDPCVD were deposited as in claim 9 of the '345 patent." FF 565 (emphasis added). FF 565 is insufficient to support a finding that the SiO2 layer inherently functions as a hard mask because the finding speaks only of possibilities. *Mehl/Biophile*, 192 F.3d at 1365. The testimony of respondents' expert (Peltzer) cited by the ALJ in support of FF 565 also speaks only of possibilities. Moreover, respondents have not identified any other support in the record for the ID's finding on this point. Consequently, the Commission determined to reverse the ALJ's finding that "[t]he silicon dioxide layer in Abernathey (especially in view of Dean) forms a cap layer which protects and serves as a hard mask during etching if there is HDP CVD deposition as required by claim 9" (ID at 137-38) as unsupported by the record.[24]

3. Whether Yota, Pan, and Yagi Are Prior Art to the '345 Patent.

Complainants argued that respondents failed to prove the publication dates for the Pan, Yagi, and Yota references. They asserted that, because respondents failed to prove that these references are prior art, the references cannot be used to establish that the '345 patent is invalid on obviousness grounds. Complainants first raised the issue of respondents' failure to prove the publication dates of the three references in a footnote in their post-hearing reply brief for the hearing completed November 16, 2001). Complainants' post-hearing reply at 18. n.11 (filed Jan.

[24] The ALJ's finding appears in the same sentence with a second finding, *viz.*, that "the titanium nitride layer between the SiO2 layer and the metal wiring line in Abernathey (and/or Dean) is the same as the protective layer in claim 21 of the '345 patent" (ID at 138). No party has challenged this second finding, which is adopted by the Commission.

8, 2002). The Commission determined that complainants waived this issue by failing to properly raise it before the ALJ.[25] The ALJ's instructions to the parties with respect to their posthearing submissions following the November hearing included the following: "The reply briefs are limited to responses to arguments presented in opposing parties' briefs. They should not be used as an opportunity to present new arguments."[26] Trans. (Judge Harris) at 1271:13-16.

Complainants and the IA argued that respondents failed to prove publication dates for the undated Yagi reference (RX-85) and offered no evidence to establish a publication date. With respect to the Yota (RX-86) and Pan (RX-82) references, complainants contended that "respondents offered no evidence of a publication date for the bound volume of the conference proceedings in which the references were included, nor did they present any evidence concerning the conference proceedings at which the papers were allegedly presented." Complainants' brief at 102. Complainants and the IA stated that respondents have failed to prove the public accessibility necessary to prove that the Yota and Pan references are "printed publications" for prior art purposes under 35 U.S.C. § 102.

Respondents' expert (Peltzer) testified as to the publication dates for the references at issue. RPX-32, entitled "'345 Prior Art Chronology," presents a timeline for the period June 15, 1993, to April 2, 1997. The references at issue are located on the timeline with the labels: "April 1996 Yagi Reference Published," "August 1996 Yota, et al. Reference Published," and

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[25] As pointed out by the IA, the ID did not address complainants' publication dates argument.

[26] This is not a new rule. *Above-Ground Swimming Pools*, Inv. No. 337-TA-25, Recommended Determination, 1977 WL 52319 (Feb. 10, 1977) (ALJ "will not, and he has not in this recommended determination considered any new issues raised for the first time in reply briefs which were not direct responses to discussions of the same issue or issues in the brief to which the reply was addressed").

"**June 18-20, 1996** Pan, et al. Reference Published." RPX-32 (emphasis in original).

Respondents' expert (Peltzer) testified as follows:

> MR. HOVANEC: Finally, your Honor, I'm going to put RPX-32 [the chronology] on the board, just to place in time perspective the various prior art references with respect to the '345 patent.
>
> BY MR. HOVANEC:
>
> Q Mr. Peltzer, would you explain this exhibit, please? I can move it closer, if you like.
>
> A Oh, that would be nice.
>
> Q Or you can come over, either way.
>
> A We have June 1993, with the Abernathey patent being issued, the Abernathey patent, remember, discloses ways to make well-defined metal lines. Then we have the Jain patent in '94. We have *Pan* in 1996, in which Pan is describing HDP as a preferred method or as a method for depositing this oxide. Then we have *Yota*, which is in August of '96. *Yagi* in 1996. And then we have the '345 provisional application filed in 1997 and then we have Tobben filed on March 31, 1997, so it's April 2, 1997 compared to March 31, 1997.
>
> Basically, here you can see that in the 1996 time frame, there were quite a number of HDPCVD references, and these would have been applied to Abernathey. Abernathey is separated from the Pan by several years. During that period of time, Abernathey would have caused people to look for the HDP and attempt to use the HDP at these better defined metal lines.

Trans. (Peltzer) 857:24-858:24 (emphasis added). As pointed out by respondents, complainants did not object to RPX-32, cross-examine respondents' expert (Peltzer) on RPX-32, or challenge the dates for Pan, Yota, or Yagi. *See, e.g., Symbol Techs., Inc. v. Opticon, Inc.*, 935 F.2d 1569, 1575 (Fed. Cir. 1991) (opposing party bears responsibility for challenging the factual underpinnings of expert's testimony on cross-examination).

Complainants contended that issues surrounding the alleged publication of the Yota, Pan, and Yagi references are factual inquiries, and not a proper subject for expert testimony. They asserted that relevant facts concerning the conference papers' accessibility include attendance at the conference, attendees' interest in the relevant art, and whether copies of the paper were freely available to the attendees, and that "[e]xpert opinion is of no benefit to the fact finder in resolving these purely factual findings, and Mr. Peltzer's conclusory testimony, which provided no factual information on these subjects, should be given no weight." Complainants' reply at 81-82 (citing Fed. R. Evid. 702).

In *Symbol Technologies*, the Federal Circuit upheld a district court's finding of infringement based on the *unrebutted* summary testimony of an expert, including the claim charts and drawings the expert used to demonstrate infringement. 935 F.2d 1569. Complainants' attempt to distinguish *Symbol Technologies* (on the ground that while expert testimony is useful on the issue of infringement, it is of "no benefit" on the question of public accessibility or publication) is not persuasive. An expert would be knowledgeable about the technical literature within his area of expertise, and such knowledge would be helpful to the finder of fact on the issue of whether a reference is prior art.[27] Expert testimony would "assist the trier of fact to

[27] For example, an expert could well have special knowledge about the attendance and publication practices followed at particular conferences. We would also expect an expert to be familiar with the technical journals in his area of expertise and to recognize citations to technical publications (*e.g.*, citations in the list of references in RX-82, RX-85, RX-86). For example, RX-86 (Yota), includes as the twelfth entry under the heading "References," "J.T. Pan, D. Ma, T. Sahin, R. Tolles, S. Broydo, H. Miyamoto, K. Kishimoto, M. Suzuki, T. Homma, M. Kikuchi, 'Integrated Interconnect Module Development,' *1996 Proceedings of Thirteenth International VLSI Multilevel Interconnection Conference (VMIC)*, edited by T.E. Wade, pp. 46-51, VMIC, Santa Clara, 1996," and the legend "SPIE Vol. 2875 / 265" appears at the bottom right corner of RX-86 (Yota).

understand the evidence or to determine a fact in issue." *See* Fed. R. Evid. 702; *In re Japanese Elec. Prods. Antitrust Litig.*, 723 F.2d 238, 279 (3d Cir. 1983), *rev'd on other grounds sub nom Matsushita Elec. Indus. Corp. v. Zenith Radio Corp.*, 475 U.S. 574 (1986) (admissibility requirement that "expert testimony be 'beyond the jury's sphere of knowledge' adopts a formulation which was rejected by the drafters of Rule 702"); *see generally* 4 *Weinstein's Federal Evidence* § 702.03[2][b] (2nd ed. 2002) (although "expert testimony concerning matters that are within the knowledge and experience of ordinary lay people is generally not admissible," there is "a large gray area" of "matters respecting which expert testimony may assist the finder of fact, but that arguably fall within the realm of common knowledge and common sense").

For the above reasons, the Commission determined to adopt the ALJ's conclusion that the Yota (RX-86), Pan (RX-82), and Yagi (RX-85) references are prior art.

4. Whether respondents established a motivation to combine the Yota, Pan, and Yagi references with Abernathey for the gap filling step (claims 1, 9 and 21).

Complainants argued that respondents presented no clear and convincing evidence of a suggestion to combine Yota, Pan, and/or Yagi with Abernathey to fill the gaps using the HDPCVD techniques.

A motivation to combine references may flow from the nature of the problem. *In re Rouffet*, 149 F.3d 1350 (Fed. Cir. 1998). The ALJ found that – –

> Abernathey discloses every element of the asserted claims of the '345 patent, except the step of HDP CVD deposition. Abernathey discloses no gap filling step because it is not the object of Abernathey to carry the process of manufacturing an integrated circuit to that point. However, the record is clear that anyone skilled in the art in 1996 knew that to make a useful product one would have to proceed from the teachings of Abernathey, and fill the gaps between the metal wiring lines with a

> dielectric material. *See, e.g.*, Peltzer Tr. 833; Fair Tr. 1418, 1424-1425. By 1996, the Novellus company, among others, was selling machines and telling customer and potential customers to use HDP CVD for void free (or substantially void-free) gap filling in metal wiring line patterns. *See* Fair Tr. 1422-1425. There is no doubt that those skilled in the art (especially the hypothetical person skilled in the art with a comprehensive knowledge of prior art, and especially a person with the advanced education and experience proposed by Complainants and accepted in this opinion) knew that gap filling was necessary, and that HDP CVD, along with HDP CVD equipment, was available to perform that task
>
> Accordingly, the Abernathey patent combined with Pan (RX-82), Yagi (RX-85), or Yota (RX-86), each of which discloses the use of HDP CVD for gap filling, renders claim 1 on the '345 patent obvious.

ID at 138. In suggesting that the ALJ relied on evidence of a trend in the industry to compensate for the lack of any specific technological principle, complainants mischaracterize the ALJ's reasoning, which was that those skilled in the art knew that gap filling was necessary to make a useful product, and further that HDPCVD was available to perform the task. The Commission determined to adopt the ALJ's findings with respect to motivation to combine the Abernathey, Pan, Yagi, and/or Yota prior art for the gap filling step.

5. Whether Abernathey Discloses the "Etching" Limitations (claims 4, 12)

The Commission determined to adopt the ALJ's findings and conclusions with respect to whether Abernathey combined with Pan, Yagi, or Yota discloses etching the second antireflective coating (claim 4) or etching the cap layer (claim 12).

Complainants argued that neither Abernathey, Pan, Yota, nor Yagi teach the etching of a second antireflective coating or a cap layer of claims 4 and 12. They further asserted that the evidence is undisputed that etching is not inherent in the HDPCVD process. Complainants cross-referenced their related argument concerning the Tobben prior art in which they argued that the ALJ relied on conclusory testimony by respondents' expert (Peltzer) without supporting

evidence and that such evidence was insufficient to show invalidity. Complainants' brief at 116 (citing *Biacore AB v. Thermo Bioanalysis Corp.*, 79 F. Supp.2d 422, 461 (D. Del. 1999).

With respect to claims 4 and 12 of the '345 patent, respondents' expert (Peltzer) testified as follows:

> Q Now, again, turn to claim 4. Now, in this case you show nothing in Abernathey that discloses claim 4 of the '345 patent; correct?
> A That's correct.
>
> Q And you are relying on other teachings from other publications to try to read a disclosure of claim 4; is that correct?
> A That's correct.
> Q Can you identify for me in any of the other teachings that you rely on, *where they teach or disclose etching a portion of the second antireflective coating during the HDPCVD process*?
> A Well, *the group of other publications that we supply all teach the use of HDPCVD, of the HDPCVD operation, sputter etching is a component. And the sputter etching would etch a portion of the second antireflective coating in Abernathey, when it is used.*
> Q *In any of those other publications that you cite, do they etch a second antireflective coating?*
> A *I don't recall that they do.*
> Q Okay. And then turn to claim 12. Would your answer there be the same, that in none of the other publications that you're referring to, do they report etching or partially etching the cap layer during the HDPCVD process?
> A Well, explain first *if you consider the Ti/titanium nitride as antireflective and the titanium nitride being the upper second antireflective reflective coating, then we have the claim 4 position that this is taught in some of the references disclosed.*
> Would you repeat your next question, please?
> Q *Do any of the teachings or any of the*

publications that you cite teach partial etching of the cap layer during the deposition of the HDPCVD process?

A *That's in claim --*

Q *12.*

A *12. And again, in the case where titanium/titanium nitride is the upper layer, the titanium nitride would be equivalent to the cap layer.*

Q Do you consider titanium nitride to be the cap layer for purposes of claim 12?

A Well, let's see, I think the question was are there teachings in some of the supplied references which teach the use of HDPCVD. In the teachings of HDPCVD, I think it was Yagi shows a titanium nitride --

JUDGE HARRIS: You've got to lift your voice and be closer to the microphone.

THE WITNESS: Yes, I will be happy to. *In the case in Yagi in which Yagi discloses a titanium nitride layer on the top of the metal line, the titanium/titanium nitride layer can be considered a dual antireflective layer, that is, a first antireflective layer of titanium and a second antireflective layer of titanium nitride.*

In the case where the titanium nitride is serving as the second antireflective layer, it is in the same position as the cap layer identified in the '345.

BY MR. KIKEL:

Q But my question here in the context of claim 12 is, do you consider in Yagi or any of the other publications you cite that you have etching of what is referred to in claim 12 as the cap layer?

A Well, *Yagi also discloses the use of HDPCVD, which contains a sputtering component. If the titanium nitride layer is exposed and serving the purpose like the cap layer, then it would be etched by the HDPCVD process.*

* * *

Q So using your construction of the term cap layer, Yagi does not teach etching of the cap layer, as that term is used in claim 12; correct?

A Yagi only teaches the etching of a layer that is in the same position as the cap layer, that's correct.

Trans. (Peltzer) at 935:11-937:25; 939:13-17 (emphasis added).

In the above-quoted testimony, Peltzer stated unequivocably that HDPCVD contains a sputtering component, and that a layer that is exposed is etched by the HDPCVD process. The ALJ could choose to rely on the testimony of this expert, rather than on the testimony of complainants' expert. The testimony of respondents' expert (Peltzer) supports the ALJ's conclusions that "[c]laim 4 is obvious in view of the combination because the second antireflective coating, if left on the first antireflective coating, is etched during the HDP CVD process" and that "[c]laim 12 is obvious in view of the combination because the cap layer, if left on the first antireflective coating, is etched during the HDP CVD process." ID at 139; Trans. (Peltzer) at 935:11-937:25; 939:13-17.

The expert testimony found insufficient to support a finding of anticipation by inherency in *Biacore, AB v. Thermo Bioanalysis Corp.*, 79 F.Supp.2d 422, 442, 461 (D. Del. 1999), was, unlike the testimony of Peltzer, qualified rather than unequivocal. The district court in *Biacore* characterized the expert testimony as "conclusory allegations -- that it would have been apparent to one of ordinary skill in the art not only that the matrix coatings taught in the prior art references possess charged groups but also the conditions necessary to take advantage of electrostatic concentration prior to covalent binding -- are insufficient to establish anticipation.[28] These assertions lack the kind of support in the record needed for proof of

[28] The district court cross-referenced the following finding of fact concerning the expert testimony at issue: "[the expert] opined generally that it would have been apparent to one of skill in the art possessing knowledge of organic chemistry that incorporated in the matrix coatings disclosed in the aforementioned references are charged groups that would act, *under the proper conditions*, to attract and concentrate ligands. Moreover, [the expert] opined that *one of ordinary skill in the art would have known from, for example, ion exchange chromatography literature, of the conditions, i.e., the pH, necessary to take advantage of the charged groups to concentrate the desired biomolecules prior to covalent binding.*" *Biacore*, 79 F.Supp.2d at 442 (citations omitted) (emphasis added).

invalidity by clear and convincing evidence. Moreover, they do not establish that the asserted references 'necessarily function' in accordance with the claimed limitations." *Biacore*, 79 F.Supp.2d at 461.

For the reasons discussed above, the Commission determined to adopt the ALJ's findings and conclusions with respect to whether Abernathey combined with Pan, Yagi, or Yota discloses etching the second antireflective coating (claim 4) or etching the cap layer (claim 12).

6. Whether Claim 13 is Made Obvious by Abernathey

Claim 13 of the '345 patent concerns the material comprising the cap layer, *viz.*, "[t]he method according to Claim 9, wherein the cap layer comprises a material from the group consisting of a silicon nitride material and an oxynitride material." The Commission determined to reverse the ALJ's legal conclusion that "[c]laim 13 would be obvious in view of the combination because one skilled in the art would understand that silicon nitride and oxynitride would be ready substitutes for the silicon dioxide of Abernathey"[29] (ID at 139). The ID cited no support for this conclusion and, in their briefing to the Commission supporting the ID, respondents did not identify any evidence of record that would support the ID's conclusion.

Complainants argued that claim 13 is not made obvious by the Abernathey patent because Abernathey teaches away from replacing silicon dioxide with a nitride-containing material. They asserted that the goal of the Abernathey patent was to avoid the footing problem caused by contact between the photoresist and the nitride in the titanium layer. They contended that silicon

[29] The "combination" of prior art referred to is "the Abernathey patent combined with Pan (RX-82), Yagi (RX-85), or Yota (RX-86)." ID at 138.

nitride or oxynitride "would simply exacerbate the 'footing' problem that Abernathey is trying to cure," and that those compounds cannot be "spun on." Complainants' brief at 142-43 (citing Trans. (Fair) at 1045-46). Complainants identified evidence in support of their contention that Abernathey teaches away, and respondents do not contest this point in their briefing to the Commission.

Rather than addressing complainants' contention that Abernathey teaches away from replacing silicon dioxide with a nitride-containing material, respondents argue that claim 13 is obvious in view of Abernathey in combination with the HDPCVD process *and the '701 patent.* Because respondents did not present this argument to the ALJ, the Commission declines to consider it.[30] *Hazani v. United States Int'l Trade Comm'n*, 126 F.3d 1473, 1476-77 (Fed. Cir. 1997). Relying on a claim chart for the '701 patent attached as Exhibit C to their brief, respondents further argued that claim 13 is obvious in view of the '701 patent combined with the HDPCVD gap-filling process.[31] As pointed out by complainants, respondents' claim chart for the '701 patent was not presented to the ALJ. Respondents' exhibit lists (included in the *Addendum to the Initial Determination* (filed May 20, 2002)) do not identify any hearing exhibit that

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[30] Respondents did not raise this argument in their post-hearing briefing. *See* Respondents' post-hearing brief (Nov. hearing) at 24-26; respondents' post-hearing reply brief (Nov. hearing) at 20-21; Respondents' supplemental brief (Dec. hearing) at 11-16. Respondents also did not raise the argument that claim 13 is obvious in view of Abernathey in combination with the '701 patent in their prehearing statements. Respondents' prehearing statement (Dec. hearing) at 5; Respondents' prehearing statement (Nov. hearing) at 41-55. Pursuant to the ALJ's ground rule 4.d contentions not set forth in detail in the prehearing statement "shall be deemed abandoned or withdrawn."

[31] As stated above, claim 13 of the '345 patent concerns the material comprising the cap layer, *viz.*, "[t]he method according to Claim 9, wherein the cap layer comprises a material from the group consisting of a silicon nitride material and an oxynitride material." Respondents' chart for claim 13 quotes the text of claim 13 and then states that "[t]he anti-reflecting material used in the inventive process are well-known films such as SiO_2, Si_3N_4 ('silicon nitride'), SiO_xN_y, and amorphous silicon (RX-046 ['701 patent] at Col. 2, lines 39-41)." Respondents' brief, Exhibit C.

corresponds to the claim chart for the '701 patent attached as Exhibit C to their brief. Because respondents did not present this argument to the ALJ,[32] the Commission declines to consider it. *Hazani*, 126 F.3d at 1476-77.

For the reasons discussed above, the Commission determined to reverse the ALJ's conclusion that claim 13 is invalid as obvious in view of Abernathey combined with Yota, Pan, or Yagi.

III. The '352 Patent

The ALJ found no violation of section 337 with respect to the '352 patent. He found that complainants have not established that the domestic industry requirement is met; none of respondents' accused devices infringe any asserted claim of the '352 patent literally or under the doctrine of equivalents; claims 1 and 2 of the '352 patent are invalid as anticipated under 35 U.S.C. § 102 and claim 8 is invalid as obvious under 35 U.S.C. § 103.

The Commission determined to review: (1) the ALJ's construction of the claim terms "an ESD protection device" (claims 1, 2, and 8), "a gate" (claims 1 and 2), "gates" (claim 8), and "source/drain regions . . . with each source/drain region comprising" (claims 1, 2, and 8), and the ALJ's invalidity, domestic industry, and infringement findings and conclusions of law with respect to those terms; (2) the ALJ's findings and conclusions of law regarding the '352 patent with respect to infringement of the asserted claims and domestic industry under the doctrine of equivalents; (3) the ALJ's finding that respondents' old E5 model ESD transistor does not

[32] We note that section B.4 of respondents' post-hearing brief (Nov. hearing) (pages 26-27) contains an obviousness discussion entitled "Additional References" that refers to the '701 patent and unspecified "admitted prior art." This section, however, does not raise the argument at issue concerning claim 13.

infringe any asserted claim of the '352 patent, either literally or equivalently; (4) the ALJ's finding that claim 8 of the '352 patent is invalid as made obvious by a combination of prior art references; and (5) whether the economic prong of the domestic industry requirement is met with respect to the '352 patent. The Commission determined not to review the remainder of the ID with respect to the '352 patent. On review, the Commission determined to affirm the ALJ's ultimate finding of no violation of section 337 with respect to the '352 patent.

With respect to the claim construction issues under review, the Commission determined to adopt the ALJ's conclusion that the "ESD protection device(s)" (claims 1, 2, and 8) "is designed to protect a circuit from damage due to electrostatic discharge (ESD)" (ID at 12), and determined to clarify, as discussed below, that the term does *not* require a protection device that is separate and apart from the circuit it protects. The Commission determined to adopt the ALJ's construction of the term "a gate" (claim 1 and 2) as "a single, particular gate for a specific transistor, with each single, particular gate having a spacer on the left and the right-hand sides of the gate" (ID at 15 and n.6) and his construction of the plural term "gates" (claim 8) as two or more transistor gates (ID at 16-17), and determined to modify the ALJ's rationale as discussed below. The Commission determined to modify the ALJ's construction of the "source/drain regions . . . with each source/drain region comprising" limitation (claims 1, 2, and 8) to reflect that – – consistent with the general rule for claims containing the patent law term of art "comprising" following the preamble – – the structural limitations set out in claims 1, 2, and 8 are not exclusive. The Commission determined to construe the "source/drain regions" limitation such that the three claimed implants are not required for every source and every drain for every

FET transistor in a claimed ESD protection device. but that a claimed ESD protection device must include at least one "gate" (*viz.*, a single, particular gate for a specific transistor) with at least two "source/drain regions" each of which contains the claimed three implants.

Under the revised claim construction, the Commission determined to find that none of respondents' accused devices infringe any asserted claim of the '352 patent, either literally or equivalently, determined to find that complainants have not established the technical prong of the domestic industry requirement, and determined to take no position as to whether complainants have satisfied the economic prong of the domestic industry requirement. Consequently, the Commission determined to affirm the ALJ's ultimate findings of no infringement and no domestic industry.

The Commission determined to affirm the ALJ's conclusion that claims 1 and 2 of the '352 patent are anticipated by the Umemoto prior art,[33] and to clarify that whether Umemoto discloses a "dedicated" ESD protection device that is "separate and apart" from the circuit it protects is irrelevant because "separate and apart" is not a claim limitation. The Commission determined to reverse the ALJ's conclusion that claim 8 is made obvious by the Umemoto prior art in combination with either the Soeda or Kamioka prior art,[34] and determined that it has not been shown by clear and convincing evidence that claim 8 is invalid as made obvious by the Umemoto prior art alone or in combination with Soeda or Kamioka. To the extent the

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[33] The Umemoto publication (Japanese Kôkai No. 64-23573) (RX-17, RX-18) is entitled "Semiconductor Integrated Circuit."

[34] The Soeda publication (Japanese Kôkai No. 3-196677) (RX-23, RX-24) is entitled "Semiconductor Device." The Kamioka publication (Japanese Kôkai No. 1-134961) (RX-195) is entitled "Input Protecting Circuit for Semiconductor Integrated Circuit."

Commission determined to review the ALJ's invalidity findings and conclusions with respect to the Kishi publication (RX-19, RX-20), the Commission determined to adopt those findings and conclusions. To the extent the Commission determined to review the ALJ's invalidity findings and conclusions with respect to the Yasui publication (RX-21, RX-22), the Commission determined to find that, in view of the fact that complainants' proposed claim construction has not been adopted, no party contended that the Yasui publication anticipates claims 1 or 2 of the '352 patent or renders claim 8 obvious in combination with other prior art.

Part III.A of this opinion, *infra*, discusses the claim construction issues under review. The issues of infringement and domestic industry are discussed in Part III.B. Invalidity is discussed in Part III.C, *infra*.

A. Claim Construction

This section presents the Commission's analysis of the claim construction issues under review, *viz.*, the terms "an ESD protection device" (claims 1, 2, and 8), "a gate" (claims 1 and 2), "gates" (claim 8), and "source/drain regions . . . with each source/drain region comprising" (claims 1, 2, and 8).

1. "ESD Protection Device(s)" (claims 1, 2, and 8)

Having examined the record in this investigation, including the briefs and responses thereto, the Commission determined to adopt the ALJ's conclusion that the "ESD protection device(s)" (claims 1, 2, and 8) is designed to protect a circuit from damage due to electrostatic discharge (ESD) (ID at 12). The Commission determined to adopt the ALJ's general approach of construing the first and second ESD protection devices of claim 8 consistently with the ESD

protection device of claim 1. In his ID, the ALJ stated that "[i]t is agreed by all parties that the claim terms were used in a generally consistent manner among the claims of the '352 patent, albeit claim 1 is directed toward '[a]n ESD protection device,' [and] claim 8 is expanded to cover 'an ESD protection circuit, having first and second ESD protection devices'." ID at 24-25. The parties' briefing to the Commission on review focuses on the language of claim 1 and the term "[a]n ESD protection device" used in that claim. No party presented any substantive argument distinguishing between the ESD protection device of claim 1 and the first and second ESD protection devices of claim 8. For the reasons discussed below, the Commission determined to clarify that the term "[a]n ESD protection device" (claim 1) does *not* require a protection device that is separate and apart from the circuit it protects.

Complainants' argument that "an ESD protection device" must be "separate and apart" is incorrect because the phrase "connected to an integrated circuit which includes FET devices" in the preamble of claim 1 does not limit the scope of the claim. In *Catalina Mktg. Int'l. Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 62 USPQ2d 1781, 1785 (Fed. Cir. 2002), the Federal Circuit stated that, although "[n]o litmus test defines when a preamble limits claim scope," "guideposts . . . have emerged from various cases discussing the preamble's effect on claim scope." Complainants' arguments rely on two such guideposts: (1) "dependence on a particular disputed preamble phrase for antecedent basis may limit claim scope because it indicates a reliance on both the preamble and the claim body to define the claimed invention," and (2) "when reciting additional structure or steps underscored as important by the specification, the preamble may operate as a claim limitation." *Catalina*, 289 F.3d at 808-09, 62 USPQ2d at 1785.

Complainants contended that the references to "said ESD protection device" in the body of the claims at issue have their antecedent basis in the italicized portion of the preamble language: "*[a]n EDS protection device* with reduced junction breakdown voltage, *connected to an integrated circuit which includes FET devices*." Complainants' argument regarding the phrase "connected to an integrated circuit which includes FET devices," which does not appear in the body of claim 1, relies on *Bell Communications Research, Inc. v. Vitalink Communications Corp.*, 55 F.3d 615 (Fed. Cir. 1995), the case cited in *Catalina* with respect to the antecedent basis "guidepost." Complainants asserted that – –

> In *Bell Communications*, the preamble to claim 6 recited a "method for transmitting a packet over a system comprising a plurality of networks . . . said packet including a source address and destination address," 55 F.3d at 621. The court noted that claim 6 thereafter made references to "said packet," thereby relying on the preamble for an antecedent basis. *Id.* According to the Federal Circuit, the references to "'*said* packet' expressly incorporated by reference the preamble phrase 'said packet including a source address and a destination address'" into the body of the claim and caused that preamble recitation to limit the claim. *Id.* (emphasis in original).
>
> This holding from *Bell Communications* is controlling precedent for the construction of the claims of the '352 patent in this investigation. The preamble to claim 1 defines an ESD protection device as "connected to an integrated circuit which includes FET devices". . . . As in *Bell Communications*, the repeated use of the term "said" ESD protection device in the claim elements necessarily relies on the reference to "ESD protection device" in the preamble for its antecedent basis. Accordingly, as in *Bell Communications*, the preamble's definition of ESD protection device is "incorporated by reference" and consequently constitutes a limitation each time the claim recites "said protection device."

Complainants' reply at 19-20.

Complainants' interpretation of *Bell Communications* is overly broad in light of the specific claim language at issue in that case. Unlike the phrase "connected to an integrated circuit which includes FET devices" at issue in this case, the body of the claim language at issue

in *Bell Communications* expressly referred to the "source address" and "destination address" that appeared in the preamble phrase "said packet including a source address and a destination address."[35] Moreover, the Federal Circuit cautioned that "[w]e have long eschewed the use of an absolute rule according or denying all preambles limiting effect, *having recognized that one cannot determine a preamble's effect except by reference to the specific claim of which it is a component*. [The claim at issue in *Bell Communications*], as drafted and in light of the specification, is plainly limited such that it literally reads only on methods that transmit packets having both source and destination addresses." *Bell Communications*, 34 USPQ2d at 1821 (emphasis added). The court then noted that "[t]he claim cannot literally read on a method for transmitting packets that, for example, lack source addresses." *Bell Communications*, 34 USPQ2d at 1821, n.2.

Furthermore, complainants' interpretation of *Bell Communications* would lead to a different outcome in *Catalina*. In *Catalina*, the Federal Circuit concluded that a preamble phrase, which is italicized in the claim language quoted below, was *not* limiting: "A [system] for controlling the selection and dispensing of product coupons at a plurality of remote terminals *located at predesignated sites such as consumer stores* wherein each terminal comprises: activation means for activating such terminal for consumer transactions." *Catalina*, 62 USPQ2d at 1783, 1786 (italics in original, underscoring added). Under complainants' interpretation of

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[35] The claim at issue in *Bell Communications* contains the following limitation: "for each gateway receiving *said packet*, (i) determining for *each said packet said source address, said destination address* and said packet identifier, (ii) if said receiving gateway does not process packets having said identifier, inhibiting forwarding of said packet; otherwise, inserting *said source address* in the corresponding one of said lists associated with said identifier, and (iii) inhibiting forwarding of said packet if *said destination address* is in said corresponding list." *Bell Communications*, 34 USPQ2d at 1818 (emphasis added).

Bell, the phrase "such terminal" in the claim body would incorporate by reference the phrase "located at predesignated sites such as consumer stores" and make that preamble phrase a limitation of the claim. But *Catalina* reached the opposite result, even though *Catalina* cited *Bell Communications* on the issue of the construction of claim preambles that provide antecedent basis for terms appearing in the claim body.

Complainants also argued that the preamble indicates a separate and apart structural relationship, which constitutes additional structure that is underscored as important by the specification. According to complainants, because the preamble term "connected" "implies a separation to be spanned," the ESD protection device cannot be "one and the same" with the circuit to be protected. Complainants' reply at 25. Complainants argued that "[t]he '352 [patent] specification indicates that one of the particular problems the inventors of the patent were seeking to address was the need for an ESD protection device separate and distinct from the integrated circuit it was protecting and located between the integrated circuit and the external contacts." Complainants' reply at 22 (arguing that the particular problem is identified in statements in the "Background of the Invention" section of the '352 patent specification and was recognized in the ALJ's findings of fact 10-16).

The particular problem identified by complainants is not set out in the statements in the "Background of the Invention" section of the '352 patent or in the ALJ's findings of fact that they cited to the Commission. For example, the statement that "[i]n order to prevent such damage [from large electrostatic charges], workers in the field have added input protection devices which are typically located between the external contacts and the FET devices," '352 patent, col. 1, ll.

26-28, does not mean that ESD protection devices *must* be located between an integrated circuit and its external contacts. This statement, therefore, does not suggest that the inventors were solving the problem of a "need" for "separate" ESD protection devices. Instead, the specification supports construing the phrase "an ESD protection device . . . connected to an integrated circuit which includes FET devices" as reciting a use for the ESD protection device. '352 patent, col. 1, ll. 17-18 ("[t]he invention relates . . . to input protection devices to protect attached integrated circuits from damage due to electrostatic discharge").

Moreover, to the extent that the purpose of the invention reflects the problem to be solved, *see, e.g., Applied Materials Inc. v. Advanced Semiconductor Materials*, 40 USPQ2d 1481, 1488 (Fed. Cir. 1996), the '352 patent specification supports the argument of the IA and respondents that the body of claim 1 sets forth a structurally complete invention, rather than complainants' argument that the problem to be solved was the need for an ESD protection device separate and apart from the protected integrated circuit. The '352 patent identifies the object of the invention as "provid[ing] a structure of an ESD protection device with a reduced junction breakdown voltage which improves the ESD characteristics of the protection device," and states that this object is achieved by specific structures, "field oxide regions in and on said silicon substrate," "gates with adjacent spacers," "source/drain regions," "first lightly implanted region," "heavier implanted region," and "second lightly implanted region," that are also recited in the body of claim 1. '352 patent, col. 2, ll. 12-28. Further, in the discussion of preferred embodiments, the patent specification explains how the "second lightly implanted region" reduces the junction breakdown voltage. FF 33-34, 51. "[A] preamble is not limiting 'where a

patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention'." *Catalina*, 62 USPQ.2d at 1784-85 (quoting *Rowe v. Dror*, 112 F.3d 473, 478, 42 USPQ.2d 1550, 1553 (Fed. Cir. 1997)).

In response to the IA and respondents' argument that the body of claim 1 describes a "structurally complete invention," complainants reassert their antecedent basis and additional structure arguments, which we discussed *supra*. Complainants further argued that an ESD protection device is separate and apart from the integrated circuit to be protected in order to ensure that the ESD protection device can safely discharge current. Complainants' reply at 23 n.6. However, this argument fails because complainants have provided no support for their contention that "[t]he ESD protection device would operate differently if it were not separate and apart [from the integrated circuit to be protected], because the internal circuits would be directly exposed to the damaging ESD currents." Complainants' reply at 23 n.6. Although complainants asserted in their initial brief (at 18-19), relying on ALJ findings of fact 14 and 16, that "[i]f the ESD protection device is simply placed among the integrated circuit's FET devices, rather than being placed between the integrated circuit's external contacts and the internal FET devices, then the ESD protection device will not be capable of providing an external path for safely discharging the electrostatic energy before it reaches the integrated circuit's FET devices," the cited findings of fact (and the passages in the '352 patent specification cited by the findings of fact) do not support complainants' assertion because they do not discuss a distinction between an ESD protection device placed "among" a circuit's FET devices and an ESD protection device placed "between" a circuit's external contacts and a circuit's internal FET devices as advocated by

complainants.

For the reasons discussed above, the Commission determined that the phrase "connected to an integrated circuit which includes FET devices" does not have a limiting effect on the claim scope, and that the "ESD protection device" does not require a protection device that is "separate and apart" from the circuit it protects.

2. "A Gate" (claims 1 and 2), "Gates" (claim 8), and "Source/Drain Regions . . . with Each Source/Drain Region Comprising" (claims 1, 2, and 8)

The Commission determined to modify the ALJ's construction of the "source/drain regions . . . with each source/drain region comprising" (claims 1 and 8) limitation, as discussed below. The Commission determined to adopt the ALJ's construction of the term "a gate" (claim 1) and "gates" (claim 8), but to modify the ALJ's rationale for that construction.

The ALJ construed the "source/drain regions . . . with each source/drain region comprising" limitation to require the claimed implants in every source and every drain of every FET making up the claimed ESD protection device. In so construing the limitation, the ALJ relied on the addition of the phrase "each source/drain region" to the limitation "source/drain regions for said ESD protection device between said gate and said field oxide regions, with each source/drain region" in a Preliminary Amendment.[36] This construction of the amended claim is inconsistent with the use of the standard term of art "comprising" following the preamble. The Commission determined to review the ALJ's construction of the "source/drain regions" limitation and requested that the parties address the term "comprising" in their review briefing.

[36] The preliminary amendment at issue is set forth in FF 61.

The IA argued that the addition of the phrase "with each source/drain region" was made "to ensure that, *consistent* with the symmetrical fabrication process discussed in the '352 patent specification. every source and every drain of each transistor that makes up the protection device has the required three implants."[37] IA's brief at 12, 13-18 (emphasis added). The disclosure of a symmetrical fabrication process does not compel the conclusion that *all* transistors making up the device must have symmetrical implants, because we do not understand the relevance of the manufacturing process disclosed in the specification to *unclaimed* aspects of the ESD protection device. As pointed out by complainants, such a construction "would allow an infringer to escape infringement by adding to an otherwise-infringing ESD protection device an extraneous FET transistor that lacked one or more of the implants and then arguing that, overall, its ESD device did not infringe because not every source/drain region for every transistor in the device contained the requisite implants." Complainants' brief at 22.

In the ID, the ALJ rejected complainants' proposed construction, which would not require *any* transistor to have symmetrical implants, *i.e.*, under complainants' construction all of the transistors could have implants on only one side of the gate (either source or drain, but not both source and drain). The ALJ stated that – –

> if Complainants' proposed claim construction were correct, one would expect the '352 patent to contain a teaching or embodiment in which the insulating layer (item 30) is formed over (1) some -- but not all -- of the source regions of the device being protected, or (2) some -- but not all -- of the drain regions of the device being protected. CX-2 ('352 Patent), col. 3, lines 12-20, Fig. 5. That such a teaching is not present within the '352 patent is reflected in the hearing testimony of Complainants'

[37] The IA's argument is that the processing steps disclosed in the patent are performed on each side of the gate and therefore produce source and drain regions with symmetrical implants.

expert witness:

> Q Can you show me where in the patent it -- one would understand that one of ordinary skill could block the opening 32 [with photoresist] on just one side of the gate but not the other?
>
> A I don't think there's any specific teaching in the patent for that to happen.
>
> * * *
>
> Q But you can't find any embodiment whatsoever in the '352 patent that says one of these openings can be blocked; isn't that correct?
>
> A I believe that would be correct. There's no specific teaching.

Fair Tr. 356-357.

ID at 22-23. Here, the ALJ is rejecting a construction where the fabrication process disclosed in the patent would not be used to produce *any* of the transistors in the claimed ESD protection device, *i.e.*, the fabrication process disclosed in the patent would not be used at all. The IA argued to the Commission that if an ESD device includes a transistor that cannot be made with the symmetrical fabrication process disclosed in the '352 patent, then the ESD device is outside the claims -- even if the ESD device includes some transistors that have symmetrical implants (and therefore the disclosed fabrication process could be used for some of the transistors in the device).

The word "comprising" generally means that the claims do not exclude additional structures in the claimed apparatus in addition to those explicitly recited in the claims. The general rule applies "absent some special circumstance or estoppel [that] excludes the additional

factor." *Vivid Techs., Inc. v. Am. Sci. & Eng'g Inc.*, 200 F.3d 795, 811 (Fed. Cir. 1999). The prosecution history may override the general usage of the term "comprising." *Phillips Petroleum Co. v. Huntsman Polymers Corp.*, 157 F.3d 866, 874-75 (Fed. Cir. 1998) (construing claim for "block copolymer *comprising* a first polymer block . . . adjacent . . . to a second polymer block" to require "significant portion" of constituent molecules to be polymer blocks based on patent applicant's statement to the Patent Office that "[t]he [patent] specification clearly teaches that these polymer blocks are each a significant portion of the entire macromolecule and the claims could not be reasonably interpreted to read on polymers in which the macromolecules contained an insignificant number of serially lined monomer units"). Because no reason for overriding the general rule has been shown in this case, the Commission determined to modify the ALJ's construction of the "source/drain regions . . . with each source/drain region comprising" limitation to reflect the general rule that, because claim 1 uses the standard term of art "comprising" following the preamble, the structural limitations set out in the claim are not exclusive.

The ALJ construed the term "a gate" as "a single, particular gate for a specific transistor, with each single, particular gate having a spacer on the left and the right-hand sides of the gate." ID at 27. Before the ALJ, complainants argued that, because one of ordinary skill in the art recognizes that an ESD protection device is often composed of multiple transistors connected together in parallel that act as one transistor, the term "gate" means a collection of transistor gate electrodes electrically coupled together that controls the current of the set of multiple transistors. ID at 13-14. The ALJ rejected complainants' alternative construction based on the prosecution

history of the '352 patent, reasoning as follows:

> As the Commission Investigative Staff points out, ESD protection devices may contain several FETs, and claim 1 uses the term "a gate" following the term of art, "comprising," and thus may mean one or more gates. In order to resolve any ambiguity, it is proper to examine the entire specification and prosecution history. *Id.* at 5 (citing *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2001)).
>
> The file history of the '352 patent shows that the applicants, through their attorney, amended original divisional application claim 7 to replace "*gates* with adjacent spacers for said ESD protection device," with the language "*a gate* with adjacent spacers for said ESD protection device" *See* CX-4 (Preliminary Amendment, Application Paper No. 2) (emphasis added). In the Remark to the Amendment, the applicants stated: "Please enter the above Preliminary Amendment to the Divisional Patent Application that is enclosed. The amended claims are believed to clarify the invention and put the application in condition for allowance." CX-4 (Preliminary Amendment, Application Paper No. 2).
>
> By this amendment, the applicants did not disclaim an ESD protection device with multiple FETs, in which there would be multiple gates associated with these FETs. Nevertheless, the applicants have clearly disclaimed a claim construction that equates "a gate" with what may be multiple gates of an ESD protection device's FETs.
>
> Indeed, as enabled by the '352 patent specification, the language "a gate" and "gates with adjacent spacers" both refer to a single, particular gate for a specific transistor, with each single, particular gate having a spacer on the left and the right-hand sides of the gate. *See* CX-2 ('352 Patent), col. 2, lines 10-11, 20-27, 54-56, Figs. 3, 7; Peltzer Tr. 710, 719-720. A gate interconnect does not mean a collection of gate electrodes, as argued by Complainants.[38]
>
> Consequently, "a gate" must be associated with a specific FET. Furthermore, due to the applicants' amendment, there is no range of equivalents for "a gate" beyond the literal meaning, inasmuch as the term "a gate" represents claim language that was amended and narrowed (to require that "each source/drain region" includes, *inter alia*, a second lightly implanted region) for reasons of patentability. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., Ltd.*, 234 F.3d 558, 574 (Fed. Cir. 2000), *cert. granted*, -- U.S. -- 121 S.Ct. 2519, 150 L.Ed.2d 692 (2001).

ID at 14-15 (italics in original, underscoring added) (footnote omitted).

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[38] [The ALJ noted that "[a]s Mr. Peltzer, Respondents' expert witness testified, a gate interconnect attaches plural gates together and is, therefore, not part of the gate." ID at 15 n.6 (citing Trans. (Peltzer) at. 780).]

In their briefs to the Commission, complainants asserted that, in stating that "applicants' Amendment during prosecution of the '352 patent merely allowed claim 1 to cover two types of protection devices, those with a single FET and those with multiple FETs" (ID at 19), the ALJ conceded that the amendment broadened the claim in some respects. They contended that the ALJ should have concluded that the claim was generally broadened and no disclaimer was being made.[39]

The ALJ concluded that the "gate" limitation was narrowed by amendment because he construed the amendment's addition of the phrase "each source/drain region" to require the claimed implants in every source and every drain region of each FET making up the '352 patent's ESD protection device. As discussed above, the Commission determined not to adopt this aspect of the ALJ's claim construction because it is inconsistent with the use of the standard term of art "comprising" following the preamble. Because the unamended gate limitation ("gates") reads on devices with multiple gates, while the amended claim limitation ("a gate") reads on devices with multiple gates and devices with single gates, the Commission concluded that the amendment from "gates" to "a gate" broadens the gate limitation. However, the '352 patent applicant's amendment of "gates" to "a gate" explicitly recognizes a difference between the terms "gates" and "a gate," and this amendment is inconsistent with a claim construction that equates "a gate"

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[39] Relying on *Ekchian v. Home Depot, Inc.*, 104 F.3d 1299, 1304 (Fed. Cir. 1997), complainants also argued that, because the '352 patent applicants did not characterize the prior art in making the amendment, the ALJ should not have found that they disclaimed a claim interpretation. Complainants' brief at 108-09. The Commission disagrees with complainants' interpretation of *Ekchian*. After concluding that arguments in an Information Disclosure Statement (IDS) may be used to interpret the claims and/or be the basis for prosecution history estoppel, the Federal Circuit examined the arguments the applicant made in the IDS. The court's conclusion in *Ekchian* turned not on whether the applicant "characterized the prior art," but rather on precisely what the applicant said to differentiate his invention from the prior art.

with multiple gates. Furthermore, complainants' proposed claim construction is based on extrinsic evidence (the testimony of complainants' expert and engineers in the field) that contradicts intrinsic evidence (the amendment appearing in the prosecution history of the '352 patent). *Bell & Howell Document Mgmt. Prods. Co. v. Altek Sys.*, 132 F.3d 701 (Fed. Cir. 1997); *see also* respondents' brief at 49-50 (discussing implicit definition of "gate" in '352 patent specification, '352 patent, col. 2, lines 54-62, Figs. 1 and 2). Because of the inconsistency between complainants' proposed construction (equating "a gate" with multiple gates) and the applicant's amendment ("gates" to "a gate"), the Commission determined to reject complainants' claim construction. The Commission, therefore, determined to affirm the ALJ's construction of the term "a gate" as "a single, particular gate for a specific transistor, with each single, particular gate having a spacer on the left and the right-hand sides of the gate." ID at 15 (citing CX-2 ('352 Patent), col. 2, lines 10-11, 20-27, 54-56, Figs. 3, 7; Peltzer Tr. 710, 719-720).

Complainants argued that, even if the term "a gate" refers to a single, particular gate for a specific FET, certain FET configurations result in "one gate" with "two source regions and two drain regions." Complainants' reply at 29-30 (citing Trans. (Fair) at 185-89). The ALJ, however, rejected this argument relying instead on the testimony of respondents' expert (Peltzer) (ID at 15 and n.6), and the Commission determined to adopt the ALJ's conclusion.

In their briefing to the Commission, complainants did not rebut respondents' argument that if "a gate" is construed as an individual FET gate, then the plain language of claim 1 compels construing the claim to require at least one FET with the required implants on both the source and the drain. Consequently, the Commission determined to adopt respondents' position

that: (1) claim 1 requires "source/drain regions" with "each source/drain region" containing "a first lightly implanted region . . . *under one of said spacers*," (2) the antecedent for "said spacers" is "a gate with adjacent spacers," *viz.*, a single, particular gate for a specific FET transistor with a spacer on the left and right hand sides of the gate, (3) the claimed ESD protection device requires at least one FET with two implanted regions, one under the spacer on one side of the gate (source) and another under the spacer on the other side of the gate (drain), and (4) given that the antecedent for "said spacers" is "a gate with adjacent spacers," the "a first lightly implanted region . . . under one of said spacers" limitation prohibits identifying the claimed "source/drain regions" with source/drain regions from different FETs.

With respect to the term "gates" and "source/drain regions . . . with each source/drain region" in claim 8, claim 8 was not amended, but was added in the Preliminary Amendment that changed the wording of claim 1. ID at 24. The ALJ stated that "[i]t is agreed by all parties that the claim terms were used in a generally consistent manner among the claims of the '352 patent, albeit claim 1 is directed toward '[a]n ESD protection device,' [and] claim 8 is expanded to cover '[a]n ESD protection circuit, having first and second ESD protection devices'." ID at 24-25. The parties' briefing to the Commission generally focuses on the language of claim 1, rather than on claim 8. The Commission determined to construe the plural term "gates" (claim 8) consistently with the "a gate" limitation in claim 1, as referring to two or more transistor gates. The Commission determined to adopt the ALJ's reasoning and his conclusion that "this limitation must be construed as two or more gates in which each of the gates has a field oxide region on each side." ID at 16-17 (explaining that such a construction is consistent with the symmetric

fabrication taught in the '352 patent specification). With respect to the "source/drain regions" limitation of claim 8, the Commission determined to construe the limitation consistently with the limitation in claim 1. *CVI/Beta Ventures, Inc. v. Tura LP*, 112 F.3d 1146, 1159 (Fed. Cir. 1997) (construing term 'elasticity' consistently throughout the claims).

B. Infringement and Domestic Industry

The Commission determined to review the ALJ's finding that respondents' old E5 model ESD transistor does not infringe any asserted claim of the '352 patent, either literally or equivalently. The Commission determined to review the ALJ's domestic industry and infringement findings and conclusions of law with respect to the limitations "an ESD protection device" (claims 1, 2, and 8 of the '352 patent), "a gate" (claims 1 and 2), "gates" (claim 8), and "source/drain regions . . . with each source/drain region comprising" (claims 1, 2, and 8). The Commission also determined to review the ALJ's findings and conclusions of law regarding the '352 patent with respect to infringement of the asserted claims and domestic industry under the doctrine of equivalents. The Commission's analysis of these issues is discussed below.

1. Infringement by Respondents' Old E5 Model Transistors

The dispute regarding infringement of the '352 patent by the old E5 model transistor involves the interpretation of the following two statements in the "Stipulation to Further Revise Prehearing Schedule" (filed Oct. 16, 2001): (1) "[s]olely for purposes of this investigation and not for use in any district court action or in any other matter, respondents stipulate that they will not contest infringement of the '352 patent by SiS's old ("source and drain") E5 model ESD transistor," and (2) "[s]olely for purposes of this investigation and not for use in any district court

action or in any other action, respondents further do not contest that products that contain the old ("source and drain") E5 model ESD transistor infringe the '352 patent under the claim construction of the '352 patent proffered by either respondents or complainants." Stipulation ¶¶ 21, 23. Respondents argued that they did not stipulate to the fact of infringement, but only agreed not to contest infringement. According to respondents, complainants had the burden of presenting a *prima facie* case on the issue of whether the old E5 model ESD transistor infringes the '352 patent. Complainants have not argued in their briefing to the Commission that the stipulation relieves them of the burden of presenting a *prima facie* case. The IA argued that while "[r]espondents may not have admitted to actual infringement . . . procedurally the stipulation operates the same as an admission of infringement, in the same sense that a criminal plea of *'nolo contendere'* is not an admission of guilt but has the same effect as a guilty plea." IA's reply at 17-18.

For the reasons discussed below, the Commission interpreted the words "respondents stipulate that they will not contest infringement" and "respondents further do not contest that products that contain the old ("source and drain") E5 model ESD transistor infringe" as requiring complainants to present a *prima facie* case of infringement, but as preventing respondents from challenging that *prima facie* case. As discussed below, the Commission determined that complainants failed to make their *prima facie* case that respondents' old E5 model ESD transistor infringes. Thus, the Commission determined that respondents' old E5 model ESD transistor does not infringe any asserted claim of the '352 patent, either literally or equivalently.

The statements at issue in the stipulation are found in paragraphs 21 and 23. Those

paragraphs read in full as follows:

> ¶ 21. **Solely for purposes of this investigation and not for use in any district court action or in any other matter, respondents stipulate that they will not contest infringement of the '352 patent by SiS's old ("source and drain") E5 model ESD transistor.** Respondents reserve the right to contest validity of the '352 patent, importation, and domestic industry as to the '352 patent both with respect to the old E5 model ESD transistor as well as with respect to the ("drain only") E6 model ESD transistor, the ("drain only") E7 model ESD transistor, the new ("drain only") E5 model ESD transistor, as well as with respect to any other SiS ESD transistor or device accused by complainants of infringing the '352 patent.
>
> ¶ 23. Solely for purposes of this investigation and not for use in any district court action or in any other matter, respondents do not contest that SiS has manufactured certain products that contain an ESD transistor (referred to herein as the "old" ("source and drain") E5 model ESD transistor) which contained at least one gate with a PESD implant in both the source region and in the drain region of the gate. **Solely for purposes of this investigation and not for use in any district court action or in any other action, respondents further do not contest that products that contain the old ("source and drain") E5 model ESD transistor infringe the '352 patent under the claim construction of the '352 patent proffered by either respondents or complainants.** SiS employees have testified that, since beginning sometime in 2001, SiS' old ("source and drain") E5 model ESD transistor has been modified so that there are no longer any PESD implants in the source regions (*i.e.*, the new "drain only" E5 model ESD transistors). To the extent that SiS products contain the new ("drain only") E5 model ESD transistor that has been so modified, they will be covered by the following paragraph of this Stipulation.

Stipulation to Further Revise the Prehearing Schedule ¶¶ 21, 23 (Oct. 16, 2001) (emphasis added). Another paragraph in the same Stipulation concerns infringement of the '345 patent by SiS's SiON process and tracks the above-quoted language of paragraph 21:

> ¶ 20. Solely for purposes of this investigation and not for use in any district court action or in any other matter, respondents stipulate that they will not contest infringement of the '345 patent by SiS's SiON process. Respondents reserve the right to contest validity of the '345 patent, importation, and domestic industry as to the '345 patent both with respect to SiS's SiON process and with respect to SiS's N2OPT process as well as with respect to any other process accused by complainants of infringing the '345 patent.

Stipulation to Further Revise the Prehearing Schedule ¶ 20 (Oct. 16, 2001). In the ID, the ALJ construed paragraph 20, which concerns respondents' stipulation not to contest infringement of the '345 patent by SiS's SiON process, as leaving complainants with the burden of presenting a *prima facie* case:

> At the hearing, Complainants' expert rendered an opinion as to each element of each asserted claim of the '345 patent to the effect that the SiS SiON process infringes. The expert's opinion was based on his review of SiS operational manufacturing procedures as recorded in SiS documents entered into evidence. *See* Fair Tr. 144, 154-175; CX-12C; CX-13C. In view of Respondents' stipulation not to contest Complainants' infringement allegation with regard to their SiON process and the '345 patent, Complainants' *prima facie* evidence is adequate to prevail on the question of whether or not SiS's SiON process practices the asserted claims of the '345 patent. Accordingly, if it were found that the asserted '345 patent claims were valid (and enforceable), it would be found that Respondents' SiON process infringed those claims.

ID at 99 (footnote omitted). The ALJ noted that "[d]ue to their stipulation, Respondents were not entitled to rebut Complainants' *prima facie* case." ID at 99 n.47. Thus, the ALJ's interpretation of similar language in paragraph 20 of the stipulation is consistent with respondents' interpretation of paragraphs 21 and 23.

The "Stipulation to Further Revise Prehearing Schedule" (filed October 16, 2001) appears to be between the private parties. The Stipulation is signed by the attorneys for the private parties, and begins "[s]ubject to the approval of [the ALJ], Complainants United Microelectronics Corporation, UMC Group (USA), and United Foundry Service, Inc. (collectively 'complainants') and Respondents Silicon Integrated Systems Corp. and Silicon Integrated Systems Corporation (collectively 'respondents') stipulate and consent, in writing, to the following further revisions to the prehearing schedule set in Order No. 4." Stipulation at 1.

The last sentence states that "[t]he Commission Investigative Staff will file a paper regarding this stipulation." A letter from the IA addressed to the ALJ was filed on October 17, 2001. In his letter the IA states that "[a]s [the ALJ] requested at the October 10 hearing (Tr. 48:21-22), the Commission Investigative Staff participated in drafting the proposed stipulation."[40] Letter to ALJ of October 17, 2001 at 1 (filed Oct. 17, 2001). In the letter, the IA identifies certain provisions with which he "does not wholly agree," and concludes by stating that "[o]ther than the above-identified matters, the Staff does not oppose the private parties' October 16 stipulation." *Id.* at 2.

As stated above, complainants have not argued in their briefing to the Commission that the stipulation relieves them of the burden of presenting a *prima facie* case, and respondents' position that the stipulation leaves complainants with the burden of presenting a *prima facie* case of infringement is consistent with statements made by complainants in their prehearing statement. *See* Complainants' prehearing statement at 14 ("Complainants will introduce testimony at the hearing from Dr. Richard Fair establishing *inter alia* that all ESD protection devices containing the 'old' E5 transistor (with ESD implants in both the source and drain regions) infringe the '352 patent. Respondents have stipulated that 'they will not contest infringement of the '352 patent by SiS' old ('source and drain') E5 model ESD transistor.' *See* October 16 Stipulation ¶ 21").

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[40] The cited portion of the hearing transcript contains the following statement by the ALJ, "So you're going to check and confirm about the state of the design-around process . . . this evening and inform counsel and my office by letter, I suppose, about what you've done and then make sure that counsel for OUII is included in your stipulation. You're going to submit a stipulation having to do with infringement of the old E-5 plus all of the discovery, which is going to be done when and how and the location by Monday evening." Oct. 10 hearing, Trans. at 48:16-25.

For the reasons discussed above, the Commission interpreted the stipulation as requiring complainants to present a *prima facie* case of infringement. The next question is whether complainants have done so. In their petition for review, complainants relied on the testimony of their expert (Fair) (at 199-203, 373-376) as establishing that respondents' old E5 ("source and drain") transistor infringes claims 1, 2. and 8 of the '352 patent. Summary testimony of an expert is sufficient to establish a *prima facie* case of infringement. *Symbol Tech,. Inc. v. Opticon, Inc.*, 935 F.2d 1569 (Fed. Cir. 1991). The Commission's briefing questions included the following: "Does respondents' old E5 model ESD transistor infringe any asserted claim of the '352 patent? In your response, please address *Symbol Technologies, Inc. v. Opticon, Inc.*, 935 F.2d 1569 (Fed. Cir. 1991)."

In their briefing to the Commission, complainants and the IA relied on the same testimony of complainants' expert (Trans. (Fair) at 199-203, 373-76), asserting that it establishes a *prima facie* case of infringement. The expert testimony cited by complainants and the IA as establishing complainants' *prima facie* case on the issue of whether respondents' old E5 model ESD transistor infringes is insufficient. In the cited testimony, complainants failed to present any expert opinions on the old E5 model ESD transistor.

We find that, as argued by respondents, the transcript at pages 199 to 203 does not refer to respondents' old E5 model ESD transistor. As to the transcript at pages 373-376, we find that complainants' expert did not read the '352 claim elements onto the old E5 model ESD transistor. By failing to make their *prima facie* case, complainants have lost the benefit of respondents' stipulation.

Finally, complainants' argument that respondents should be estopped from disputing the sufficiency of their *prima facie* case is unpersuasive. In their reply, complainants argued that --

> [h]aving first stipulated not to contest infringement by their old E5 transistor, and then blocked Complainants' efforts to develop further evidence on this point, Respondents should be estopped from now arguing that more detailed testimony was required on the very issue they contended at the November 2001 hearing had been more fully developed than necessary in light of their stipulation. Indeed if the Commission countenanced Respondents' tactics, parties in Section 337 investigations would be loath to enter into evidentiary stipulations for fear of falling victim to such sandbagging.

Complainants' reply at 42-43. In support of this argument complainants cited hearing testimony at 866-868 and 989. The cited portions of the hearing transcript (at 866-68 and 989) do not support complainants' contention that they were "blocked" from developing further evidence as to infringement by the old E5 transistor.[41]

The transcript at 866-68 is a portion of the cross-examination of respondents' expert (Peltzer), regarding questions addressing two topics, respondents' old silicon oxynitride (SiON) process (infringement of the '345 patent, the subject of Stipulation ¶ 20) and respondents' old E5 ("source and drain") transistor (infringement of the '352 patent, the subject of Stipulation ¶¶ 21 and 23). Complainants' suggestion that respondents' objection to the question by complainants'

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[41] The passage at 989 is as follows:

> MR HOVANEC [counsel for respondents]: Your Honor, what's the relevance of going into the old E5? We estimated [sic] we're not contesting infringement of the old E5.
> JUDGE HARRIS: I think it goes to claim construction, does it not?
> MR. KIKEL: Yes, your Honor. I mean, if I don't put something in, he will say there's[[ ]]I'm seeking his interpretation of[[ ]]
> JUDGE HARRIS: All right.

Trans. at 989:17-990:1.

counsel (Mr. Kikel) regarding the old E5 design and the '352 patent blocked their efforts to develop testimony on infringement is unpersuasive because the witness answered the question and stated that he had "not reviewed that process" and "have just not formed any opinion there." Trans. at 868:12-25. The portion of the transcript at issue also demonstrates that complainants' counsel recognized that they had the burden of presenting a *prima facie* case on infringement notwithstanding the stipulations. It is reproduced below:

> BY MR: KIKEL [complainants' counsel]:
>
> Q Now, Doctor, you've gone through a number of different pieces of art, and you've read various claims from the '345 and the '352 patent on that art and confirmed that every element of those claims was present in pieces of art here and there. Let me ask you a threshold question. Are you familiar with the SiS manufacturing process which uses silicon oxynitride as a cap layer, the current process they're using to manufacture all of their products?
>
> A I was not asked to review that process. I'm aware that at one time there was such a process.
>
> MR. HOVANEC [respondents' counsel]:
>
> Your Honor, I object. We made the stipulation that we're not contesting infringement. Mr. Kikel went through this with Dr. Fair. There was nothing in my direct about the SiS process using silicon oxynitride. I don't understand why we're wasting time going into the silicon oxynitride process.
>
> MR. KIKEL [complainants' counsel]:
> Your Honor, they don't stipulate. They just indicate that they will not contest. Just in case there's going to be any question about well, maybe we didn't prove it up fully, I think this witness in 15 seconds can answer the question as to whether, given the analysis he has done of this claim and the processes involved, whether it reads on the claims of the '345 and the 352 -- whether the claims of the '345 and '352 patent read on the processes that are not being contested.
>
> JUDGE HARRIS: Well, if you know, you can answer the question.

THE WITNESS: I've not been asked to review the SiS silicon oxynitride process or the SiS process with an oxide cap layer on the surface, and I'm using this term loosely. I have not formed any opinion in this area. I would have to look -- at the minimum, I would have to look at the process flow and some of the thicknesses involved.

BY MR. KIKEL [complainants' counsel]:

Q What thicknesses would you need to know in order to be able to determine whether or not claims, let's say, of the claims 1, 9 and 21 of the '345 process read on?

JUDGE HARRIS: Well, I mean, I was prepared to let you ask that first question, but if it's a matter that they have stipulated not to contest and you've already proved it up, I don't see any sense in needing to prove it up further with this witness.

MR. KIKEL: Fine, your Honor. Then if I may just ask one question on the '352 patent.

JUDGE HARRIS: Yes, go ahead.

BY MR. KIKEL:

Q: On the '352 patent, the old E5 design that had the implants and the source and the drain, does claim 1 of the '352 patent read on that -- on products manufactured with that old design, with the implants and the source and the drain?

MR. HOVANEC [respondents' counsel]:

Same objection, your Honor. I think this is irrelevant and a waste of time.

THE WITNESS: Well, again, I have not reviewed that process as to where the implants were in the older process, where they were physically located and what step in the process they entered. I have just not formed any opinion there.

JUDGE HARRIS: Let's get on to cross-examination of the invalidity questions.

Trans. 866:15-868:25.

Because complainants failed to make their *prima facie* case, the Commission determined that respondents' old E5 model ESD transistor does not infringe any asserted claim of the '352 patent, either literally or equivalently.

2. Literal Infringement

The Commission determined that complainants have not established that respondents' "drain-only" ESD protection devices, *viz.*, the new E5 model ESD transistor, the E6 model ESD transistor, and the E7 model ESD transistor literally infringe claims 1, 2, or 8 of the '352 patent under the Commission's revised claim construction.

In their briefing to the Commission, respondents asserted that the parties do not dispute that the three claimed implants are found only in the "drain regions" of individual transistors within the ESD protection device of respondents' new E5 model ESD transistor, E6 model ESD transistor, and E7 model ESD transistor. Respondents contended that those devices do not literally infringe claims 1 or 2 under a claim construction requiring at least one individual FET with the three claimed implants in both the source and drain regions, and do not literally infringe claim 8 under a similar claim construction that would require at least two individual FETs in which both source and drain contain the three claimed implants. Respondents further argued that because complainants failed to challenge the ALJ's interpretation of "voltage source" (ID at 26-27) and failed to challenge FF 82,[42] complainants abandoned these issues under Commission rule

[42] FF 82 reads as follows: "The sources of the NG, NGX, NGY and NGZ transistors, located below the drains in the RPX-225 circuit diagram, are connected to 0VSS (zero volts), which is ground. RX-225C; Pelzer Tr. 772:3-5, 7."

210.43(b)(2). Respondents asserted that the ALJ's construction of "voltage source" and FF 82 establish that respondents' devices do not meet the "third electrical connection, to a voltage source, of said source of said first ESD protection device" (claim 8).

In their briefing to the Commission, complainants did not argue that respondents[[ ]]literally infringe if the claim term "a gate" refers to a single, particular gate for a specific FET transistor (*i.e.*, under the Commission's revised claim construction). Instead, complainants argued that, if the term "a gate" is construed to include the collection of all gate electrodes of FET transistors connected in parallel in a single ESD protection device, then claims 1 and 2 are literally infringed; but the Commission did not adopt this claim construction. As to respondents' [[ ]] argument, complainants stated that they "agree that the ALJ's claim construction of the term [[ ]]precludes a finding of literal infringement of claim 8."[43] Complainants' reply at 35.

Having examined the record in this investigation, including the briefs and the responses thereto, the Commission determined that none of respondents' [[ ]] contain [[ ]] *See* ID at 29; FF 64-85. Consequently, none of those accused devices literally infringe claims 1, 2, or 8 of the '352 patent under the Commission's claim construction.

[43] Complainants argument that this limitation is infringed under the doctrine of equivalents is addressed in the next section, III.B.2.

3. Infringement Under the Doctrine of Equivalents

The ALJ concluded that, under *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 234 F.3d 558, 574, 56 USPQ2d 1865, 1870 (Fed. Cir. 2000) (*en banc*), *judgment vacated and remanded*, ___ U.S. ___, 122 S.Ct. 1831 (May 28, 2002), the doctrine of equivalents is not applicable in this case because the patent applicant had narrowed the claim language during patent prosecution for reasons of patentability.[44] ID at 15-16, 31-35. Specifically, the ALJ found no range of equivalents for the "a gate" limitation of claim 1, and further that claim 8 is not infringed under the doctrine of equivalents because the accused devices [[

]] ID at 35.

The Commission determined to review the ALJ's findings and conclusions of law regarding the '352 patent with respect to infringement of the asserted claims and domestic industry under the doctrine of equivalents. The Commission requested that in their briefing the parties address the recent Supreme Court decision *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S.Ct. 1831 (May 28, 2002). Having examined the record in this investigation, including the briefs and the responses thereto, the Commission determined that none of respondents' [[

]] infringe claims 1, 2, or 8 of the '352 patent under the doctrine of equivalents.

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[44] After the ALJ issued his final ID on May 6, 2002, the Supreme Court vacated the Federal Circuit's judgment and replaced the Federal Circuit's "absolute bar" to the doctrine of equivalents with a more flexible approach.

Respondents argued in their reply brief[45] that the Commission need not reach the issue of infringement under the doctrine of equivalents given respondents' stipulation that the issue of whether respondents' devices infringe the '352 patent "can be resolved based solely on claim construction of the patent." Notwithstanding the stipulation, however, the ALJ considered complainants' argument that respondents' devices infringe the asserted claims under the doctrine of equivalents and rejected that argument on the merits. ID at 31-35. Respondents' petition for review did not raise the ALJ's consideration of complainants' doctrine of equivalents argument with respect to whether respondents' devices infringe the asserted claims of the '352 patent (notwithstanding the stipulation), and respondents have therefore abandoned this issue. Commission rule 210.43(b)(2).

As discussed above, the Commission determined to construe the term "a gate" (claim 1) as referring to a single, particular FET transistor gate, and *not* to a collection of FET transistor gates connected in parallel, and determined to construe the term "gates" (claim 8) consistently with the term "a gate" in claim 1. The Commission determined to construe the limitation "source/drain regions . . . with each source/drain region comprising: a first lightly implanted region . . . under one of said spacers; a heavier implanted region . . .; a second lightly implanted region" (claims 1, 2, and 8) as requiring that all three claimed implants (*viz.*, a first lightly implanted region, a second lightly implanted region, and a heavier implanted region) be present in each of the source region and the drain region of a single, particular FET transistor.

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[45] Respondents do not appear to have raised this issue in their first brief to the Commission. *See* Respondents' brief at 62-69.

Complainants contended that, under the doctrine of equivalents, a [[

]] and therefore respondents' [[ ]] infringe claims 1, 2, and 8.[46]

Respondents and the IA argued that complainants' reliance on the doctrine of equivalents is barred by prosecution history estoppel under *Festo*, because the '352 patent applicant amended and narrowed the claims at issue during prosecution of the application that matured into the '352 patent. Complainants' took the position that the amendments at issue broadened, rather than narrowed, the claims.

In *Festo*, the Supreme Court stated that "[e]stoppel arises when an amendment is made to secure the patent and the amendment narrows the patent's scope." 535 U.S. ___ (2002), slip op. at 11. Respondents identified the narrowing amendment as the addition of the phrase "each source/drain region comprising" in a Preliminary Amendment. Complainants argued that respondents overlook the deletion from the original claim in the patent application of another limitation referring to "source/drain regions," and that such deletion was broadening. The text of the Preliminary Amendment is quoted in FF 61 (the changes to the claim language discussed by the parties are shown in bold):

> FF 61. Claim 7 as amended in the '373 Application appears as follows, with material added to the claim being underlined, and material deleted from the claim being enclosed by square brackets.
>
> 7. (AMENDED) An ESD protection device with reduced junction breakdown voltage, connected to an integrated circuit which includes

[46] As discussed below, complainants further argue that the "third electrical connection" to a "voltage source" is met in claim 8 under the doctrine of equivalents.

FET devices, comprising:

a silicon substrate having a first conductivity type;

field oxide regions in and on [a] said silicon substrate for isolation of said ESD protection device;

a gate[s] with adjacent spacers for [for] said ESD protection device, between said field oxide regions;

[source/drain regions for said ESD protection device between said gate and said field oxide regions, with a heavy ion implant; and]

source/drain regions for said ESD protection device between said gate and said field oxide regions, with each source/drain region comprising:

a first lightly implanted region having a second conductivity type opposite to said first conductivity type, under one of said spacers[,];

a heavier implanted region of the same conductivity type as said [light ion implant between] first lightly implanted region, located between said first lightly implanted region and one of said field oxide regions[,]; [and]

a second lightly implanted region of [opposite] same conductivity type as said silicon substrate, centered under said heavier implanted region.

FF 61 (citing RX-2, Preliminary Amendment dated December 8, 1994) (underscoring and square brackets in original, bold added).

Even if we were to accept respondents' argument that the addition of the phrase "each

source/drain region comprising" to the original claim limitation ("source/drain regions for said ESD protection device between said gate and said field oxide regions, with each source/drain region comprising:") *narrows* the scope of the original claim in some respects by requiring that the "source/drain regions" claimed by the limitation *each* contain the specified three implants (*viz.*, first lightly implanted region, heavier implanted region, and second lightly implanted region), we reject respondents' contention that complainants' doctrine of equivalents argument is thereby barred. This is because the doctrine of equivalents applies on an element-by-element basis. *Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 29-34 (1997). In our view, the issue presented is whether prosecution history estoppel bars recourse to the doctrine of equivalents for a particular claim element.[47] *Id.*

Complainants argue that, under the doctrine of equivalents, a collection of transistor gates connected together in parallel is the equivalent of a single FET transistor gate (*i.e.*, the "a gate" limitation). In appears to us that the narrowing amendment identified by respondents as giving rise to prosecution history estoppel under *Festo* (*viz.*, the addition of the phrase "each source/drain region comprising" to the original claim limitation "source/drain regions for said ESD protection device between said gate and said field oxide regions, with each source/drain region comprising:") should not be understood as narrowing the scope of the limitation that is the target of complainants' doctrine of equivalents argument (*viz.*, "*a gate* with adjacent spacers").[48]

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[47] This approach is consistent with *Festo*. 535 U.S. ___ (2002) slip. op. at 12 ("Our conclusion that prosecution history estoppel arises when a claim is narrowed to comply with § 112 gives rise to the second question presented: Does the estoppel bar the inventor from asserting infringement against any equivalent to the narrowed element or might some equivalents still infringe?")

[48] As discussed above in the claim construction section of this opinion, the Commission determined to construe the term "gates" (claim 8) consistently with term "a gate" in claim 1. *CVI/Beta Ventures, Inc. v. Tura LP*, 112 F.3d

Respondents' argument appears to be that the amended "source/drain regions" limitation requires at least one FET transistor with the three claimed implants in each of the source and the drain regions of that transistor. As discussed *supra*, the Commission construed the claim (as amended) to require at least one FET with the three claimed implants in each of the source and drain regions. The requirement of at least one double-implant FET flows from the Commission's construction of the "a gate" limitation as referring to the gate of a single, particular FET transistor, rather than from the limitation "source/drain regions . . . each source/drain region comprising: a first lightly implanted region . . . under one of said spacers; a heavier implanted region . . . ; a second lightly implanted region."

Respondents identified the narrowing amendment as "each source/drain region comprising," which amendment narrowed the scope of the "source/drain regions" limitation to require all three implants in each of at least two "source/drain regions." The amending phrase, "each source/drain region comprising," is followed by the elements setting forth the implants, *i.e.*, "*a first lightly implanted region* having a second conductivity type opposite to said first conductivity type, *under one of said spacers*; a heavier implanted region . . .; a second lightly implanted region." Although the limitation specifies that a first lightly implanted region is located under one of said spacers and the antecedent for said spacers is "a gate with adjacent

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1146, 1159 (Fed. Cir. 1997) (construing term 'elasticity' consistently throughout the claims). The source/drain regions . . . with each source/drain region comprising" limitations of claims 1 and 8 are also construed consistently. "[I]n the context of literal infringement, it is well-settled that identical claim terms used in different claims must be interpreted consistently. Similarly, under the doctrine of equivalents, we see no reason to assign different ranges of equivalents for the identical term used in different claims in the same patent, absent an unmistakable indication to the contrary." *Am. Permahedge, Inc. v. Barcana, Inc.*, 105 F.3d 1441, 1446 (Fed. Cir. 1997) (citation omitted). Consequently, our conclusions with respect to the doctrine of equivalents as to "a gate" apply equally to the "gates" of claim 8.

spacers," the added phrase "each source/drain region comprising" does not narrow the "*a gate* with adjacent spacers" limitation. Consequently, respondents' argument that complainants' doctrine of equivalents argument is barred by prosecution history estoppel is not persuasive.[49]

Respondents do not appear to have addressed the merits of complainants' doctrine of equivalents argument, which is that a collection of FET gates connected in parallel is the functional equivalent of a large single FET gate. Complainants argued that the ALJ's suggestion (ID at 32 and n.14) that the testimony of complainants' expert (Fair) on this issue is insufficient to demonstrate equivalence in view of the testimony of respondents' expert (Peltzer) is incorrect. The ALJ noted that "[w]hile Mr. Peltzer testified that connecting two transistors in parallel would be the functional equivalent of increasing the size of the single transistor in the ESD protection device, from the standpoint of increasing the current-carrying capacity of an ESD protection device, he did not testify that in all other respects two transistors in parallel are the equivalent of a single transistor. *In fact, his testimony indicates that in the two different structures, there could be other relevant areas, aside from current-carrying capacity, that would not be equivalent.*" ID at 32 n.14 (we have added the italicized emphasis, which is not present in

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[49] Respondents also argued that complainants' argument that a collection of FET gates connected in parallel is equivalent to a single FET gate fails because the doctrine of equivalents cannot be used to read a limitation completely out of the claim. We reject respondents' argument. As discussed above in the claim construction section of this opinion, the source/drain regions limitation requires at least two source/drain regions each of which contains the three implants and also requires that the implants be located under the spacers of "said gate with adjacent spacers." If the antecedent gate is an FET transistor, then all of the source/drain regions of the FET have the requisite three implants -- but this is because an FET transistor has only one source and one drain. This is not a requirement of the source/drain regions limitation, but rather flows from the construction of the term "gate with adjacent spacers" to mean a single, particular FET gate. Applying the doctrine of equivalents to the "a gate" limitation, therefore, does not read a limitation requiring three implants on each of the source and drain regions out of the claim because the source/drain regions limitation only requires that at least two source/drain regions under the spacers of "said gate" each have the claimed implants.

the ID). We understand complainants' argument to be that, even if Peltzer's testimony is credited, it is insufficient to rebut Fair's testimony on the factual issue of equivalence. Respondents and the IA apparently did not address this point.

It is true that Peltzer's testimony does not rebut Fair's testimony regarding the functional equivalence of a large single transistor and transistors connected in parallel *with respect to current-carrying capacity*. The ALJ acknowledged this, but further stated that "in the two different structures, there could be other relevant areas, aside from current-carrying capacity, that would not be equivalent." ID at 32 n.14. Complainants appear to be objecting to the ALJ's implicit finding that *any* function other than "current-carrying capacity" is relevant to the issue of equivalence between a large single transistor and transistors connected in parallel in the context of the '352 patent claims.

The testimony of complainants' expert cited to us by complainants (*viz.*, Trans. (Fair) at 194-96, 347-48 cited in complainants' brief at 28-33) does not address the issue of whether functions other than "current-carrying capacity" are relevant to the function served by a single FET (*i.e.*, the "a gate with adjacent spacers") in the invention of the '352 patent. The testimony of complainants' expert appears to us to be comparing the current flow in the two transistor configurations. For example, he testifies that "[t]he equivalence comes about that I get the same current by combining the outputs of these drains, I get the same current as I would with this device." Trans. (Fair) at 196:8-10. Moreover, respondents' expert (Peltzer) elsewhere testified that the function of an FET transistor gate in an ESD protection device includes turning the current beneath the gate on and off. Trans. (Peltzer) at 718:24-719:15 ("Normally the gate gates,

or turns on and off a carrier flow beneath the gate from the source to the drain"), 780-81. It seems to us that "turning on and off" is an additional function to current-carrying capacity.

In the portion of respondents' expert (Peltzer) testimony cited by the ALJ. Peltzer identifies differences in the way the two configurations of transistors operate and states that "the actual function of one of these ESD circuits is really quite complicated, after a charge is received." ID at 32 n.14. Although complainants argue that respondents' expert (Peltzer) "did not contend that [the] 'minor differences' [between the two configurations identified by Peltzer] would cause a substantial difference in the way Respondents' products function or the results achieved," the burden of proof is on complainants to demonstrate insubstantial differences, not on respondents to show substantial differences. The ALJ's finding that "in the two different structures, there could be other relevant areas, aside from current-carrying capacity, that would not be equivalent" is supported by the record and establishes that complainants have not met their burden of proving infringement of claims 1, 2, or 8 under the doctrine of equivalents.

We also reject complainants' other argument for infringement under the doctrine of equivalents, *viz.*, [[ ]] are functionally equivalent to devices with source and drain implants. This doctrine of equivalents argument fails because, as discussed *supra* in the claim construction section of this opinion, the [[

]] Complainants' doctrine of equivalents argument attempts to satisfy the "at least two" source/drain regions limitation with [[ ]] and this in

effect reads a limitation out of the claim, which is impermissible.[50] *Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 29 (1997).

Finally, complainants argued that the ALJ made no finding as to whether his construction of "voltage source" to mean "a source of energy or, more specifically, an operating voltage," but *not* to mean "ground" or "connected to ground" (ID at 26-27), precluded a finding of infringement under the doctrine of equivalents. Relying on the testimony of their expert (Fair), complainants argued that "[r]espondents' *ESD protection devices* function in the same way as *the ESD protection circuit* disclosed in claim 8 when the source regions of [r]espondents' ESD protection devices are connected to ground rather than to an operating voltage." Complainants' brief at 35-36 (citing Trans. (Fair) at 253). In the cited testimony, complainants' expert (Fair) testified with reference to figure 8 of the '352 patent that *an ESD protection device* would function the same way whether the third electrical connection is connected to ground or whether it is connected to a voltage source. As argued by respondents, complainants' doctrine of

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[50] Complainants' argument (applying the doctrine of equivalents to the source/drain regions limitation) is also barred by prosecution history estoppel. The "source/drain regions for said ESD protection device between said gate and said field oxide regions, with each source/drain region comprising" limitation was narrowed by amendment in adding the phrase "each source/drain region comprising." The added phrase changed the scope of the unamended source/drain regions limitation to require that the three claimed implants be present in *each* of the claimed plural "source/drain regions" of the limitation. Consequently, prosecution history estoppel applies to complainants' doctrine of equivalents argument concerning the source/drain regions limitation. *Festo*, 535 U.S. ___, slip op. at 11-12. As discussed *supra* in the claim construction section of this opinion, given the Commission's construction of the term "a gate" as referring to a single, particular gate for a specific FET, the claimed "source/drain regions" cannot be identified with source/drain regions from different FETs. Because the added phrase "each source/drain region comprising" changed the scope of the source/drain regions limitation to require that the three claimed implants be present in *each* of at least two "source/drain regions," claim coverage of ESD devices with only drain-only implant FETs (*i.e.*, devices with not even one FET with both source and drain implants) was surrendered by the amendment. *Festo*, 535 U.S. ___, slip op. at 15 ("patentee's decision to narrow his claims through amendment may be presumed to be a general disclaimer of the territory between the original claim and the amended claim"). Because complainants have not offered any substantive arguments or evidence to rebut the presumption, their doctrine of equivalents argument is barred.

equivalents argument and evidence appear to be directed toward the "function" of an ESD protection device (*i.e.*, the claimed invention as a whole) rather than toward the function of the particular claim element (voltage source) that is not literally present in the accused devices. Consequently, complainants have failed to prove that respondents' accused devices infringe claim 8 under the doctrine of equivalents. *Warner-Jenkinson*, 520 U.S. at 29 ("the doctrine of equivalents must be applied to individual elements of the claim, not to the invention as a whole").

For the reasons discussed above, the Commission determined that none of respondents' [[

]] infringe claims 1, 2, or 8 of the '352 patent under the doctrine of equivalents.

4. Domestic Industry

The Commission determined to review the ALJ's domestic industry findings and conclusions of law with respect to the limitations "an ESD protection device" (claims 1, 2, and 8 of the '352 patent), "a gate" (claims 1 and 2), "gates" (claim 8), and "source/drain regions . . . with each source/drain region comprising" (claims 1, 2, and 8). The Commission determined to review the ALJ's findings and conclusions of law regarding the '352 patent with respect to the technical prong of the domestic industry requirement under the doctrine of equivalents. The Commission also determined to review the issue of whether complainants established the economic prong of the domestic industry requirement with respect to the '352 patent. The Commission requested briefing on those issues. Having examined the record in this

investigation, including the briefs and the responses thereto, the Commission determined that complainants have not established the technical prong of the domestic industry requirement, and further determined to take no position as to whether complainants have satisfied the economic prong of the domestic industry requirement. *Beloit Corp. v. Valmet Oy*, 742 F.2d 1421 (Fed. Cir. 1984).

Because complainants' products are [[ ]] (ID at 149), the products [[ ]] as required by the asserted claims under the Commission's claim construction. Complainants argued that, even if the claims of the '352 patent are limited to "a gate" for a particular FET, the UMC ESD protection devices like those illustrated in CX-29C meet the limitations of claim 1 either literally or, at a minimum, under the doctrine of equivalents. They argued that these devices [[ ]] Complainants' reply at 40 (cross-referencing reply at 29-31). According to complainants, in these configurations [[ ]] Complainants' reply at 30 and n.9. The Commission rejected complainants' argument because, as discussed in the claim construction section of this opinion, it adopted the ALJ's construction of "a gate" (claim 1), which excludes gate interconnects (ID at 15 n.6; Trans. (Peltzer) at 780-81).

Complainants argued that their devices practice the patent under the doctrine of

equivalents, and in support, cross-referenced their doctrine of equivalence arguments concerning respondents' [[ ]] devices. Respondents argued that the Commission should not consider whether complainants practice the '352 patent under the doctrine of equivalents given complainants' stipulation that the issue of whether they practice the '352 patent "can be resolved based solely on the claim construction of the patent." Respondents' brief at 813-85. Citing the ID at 149, respondents state that "[t]he ALJ -- having rejected the Complainants' claim construction -- properly concluded that the Complainants cannot meet the technical prong of the domestic industry requirement." Respondents' brief at 84.

Notwithstanding the stipulation, however, the ALJ considered complainants' argument that complainants' devices practice the '352 patent under the doctrine of equivalents and rejected the argument on the merits. ID at 35 n.15. Respondents' petition for review did not raise the ALJ's consideration of complainants' doctrine of equivalents argument with respect to whether their devices practice the '352 patent (notwithstanding the stipulation), and respondents have therefore abandoned the issue. Commission Rule 210.43(b)(2). The Commission determined, however, that complainants have not established that their devices practice the '352 patent under the doctrine of equivalents for purposes of the technical prong of the domestic industry requirement. In their briefing to the Commission, the parties supported their arguments regarding complainants' practice of the '352 patent by cross-referencing the arguments that they made concerning the application of the doctrine of equivalents to respondents' [[ ]] As discussed above, the Commission determined that respondents' [[ ]] do not infringe claims 1, 2, or 8 under the doctrine of equivalents, and the same analysis supports

the Commission's determination that complainants' devices do not practice the '352 patent.

For the reasons discussed above, the Commission determined that complainants have not established the technical prong of the domestic industry requirement.

C. Invalidity

The Commission determined to review the ALJ's claim construction of the limitations "an ESD protection device" (claims 1, 2, and 8 of the '352 patent), "a gate" (claims 1 and 2), "gates" (claim 8), and "source/drain regions . . . with each source/drain region comprising" (claims 1, 2, and 8), and the ALJ's invalidity findings and conclusions of law with respect to these limitations. The Commission also determined to review the ALJ's finding that claim 8 of the '352 patent is invalid as made obvious by a combination of prior art references.

With respect to the Umemoto publication (RX-17, RX-18), complainants argued that Umemoto does not anticipate claims 1 and 2, and does not render claim 8 obvious, because Umemoto does not disclose a dedicated ESD protection device that is separate and apart from the integrated circuit being protected. As discussed in the claim construction section of this opinion, the Commission determined to clarify that the term "[a]n ESD protection device" (claim 1) does *not* require a protection device that is separate and apart from the circuit it protects and determined to adopt the ALJ's general approach of construing the first and second ESD protection devices of claim 8 consistently with the ESD protection device of claim 1. Consequently, the Commission determined that whether Umemoto discloses an ESD protection device that is "separate and apart" from the circuit it protects is irrelevant because "separate and apart" is not a claim limitation. The Commission determined to affirm the ALJ's conclusion that

claims 1 and 2 of the '352 patent are anticipated by the Umemoto prior art.

Complainants and the IA argued that claim 8 of the '352 patent is not made obvious by the Umemoto publication in view of the Soeda (RX-23, RX-24) or Kamioka (RX-195) publications because respondents failed to identify clear and convincing evidence of a motivation or suggestion to combine the references. Respondents argued that Umemoto alone renders claim 8 obvious. Complainants argued that the combination of Umemoto and Soeda does not render claim 8 obvious because Soeda lacks the element of claim 8 dealing with the first electrical connection. The Commission's analysis of the parties' arguments on these issues is discussed in detail below in sections III.C.1 and III.C.2.[51] In sum, although the Commission determined that complainants' argument that the combination of Umemoto and Soeda does not render claim 8 invalid as obvious because Soeda does not disclose the claimed "first electrical connection" is not persuasive (as discussed *infra* in section III.C.2), the Commission determined to reverse the ALJ's conclusion that claim 8 is invalid as obvious in view of Umemoto and either Soeda or Kamioka. As discussed *infra* in section III.C.1, none of respondents' arguments for a finding of a motivation to combine these references are persuasive, and a finding of motivation to combine is essential to obviousness. *C.R. Bard, Inc. v. M3 Sys., Inc.*, 157 F.3d 1340, 1352 (Fed. Cir. 1998). The Commission also determined (as discussed *infra* in section III.C.1) that respondents waived their argument that Umemoto alone renders claim 8 invalid as obvious, and in any event, their argument is not persuasive. Consequently, the Commission determined to reverse the ALJ's

[51] Complainants also argued that Umemoto does not anticipate claims 1 and 2, and does not render claim 8 obvious, because this prior art does not disclose "centering of a second lightly implanted region." Complainants' brief at 40-49; complainants' reply at 44-48. The Commission determined not to review the ALJ's anticipation findings with respect to this issue, and therefore adopted the ID's findings.

conclusion that claim 8 is made obvious by the Umemoto prior art in combination with either the Soeda or Kamioka prior art, and determined that it has not been shown by clear and convincing evidence that claim 8 is invalid as made obvious by the Umemoto prior art alone or in combination with Soeda or Kamioka.

As to the Kishi publication, in his briefing to the Commission the IA argued that Kishi anticipates claims 1 and 2. The ALJ found that "the record contains little overall information about the Kishi publication and the device disclosed therein, including a clear explanation of how the disclosed device would operate. Although the Kishi publication may have anticipated claims 1 and 2 of the '352 patent, that fact has not been established by clear and convincing evidence." ID at 53. To the extent that the Commission determined to review the ALJ's invalidity findings and conclusions with respect to the Kishi publication, the Commission determined to adopt those findings.

Respondents argued that under complainants' proposed claim construction, claims 1 and 2 of the '352 patent are anticipated by the Yasui publication and claim 8 is made obvious by Yasui in combination with the Soeda and Kamioka publications. To the extent that the Commission determined to review the ALJ's invalidity findings and conclusions with respect to the Yasui publication, the Commission determined that, in view of the fact it did not adopt complainants' proposed claim construction, no party contended that the Yasui publication anticipates claims 1 or 2 of the '352 patent or, in combination with other prior art, renders claim 8 obvious.

1. Whether the Umemoto Prior Art, Alone or in Combination with Soeda or Kamioka, Renders Claim 8 Obvious

The ALJ concluded that independent claim 8 of the '352 patent is invalid as made obvious

by the combination of Umemoto with either Soeda or Kamioka. The ALJ identified the "primary issue" as "whether it has been established that one of ordinary skill would have been motivated to combine the Umemoto publication with the other references." ID at 60. In finding a motivation to combine, the ALJ concluded that the "plain language" of Umemoto "motivates one to expand the application of the invention beyond the scope of the particular embodiment depicted therein." ID at 62 (citing RX-18 at 4). In reaching that conclusion, the ALJ relied on the statement in Umemoto that "[w]ith this invention, the electrostatic breakdown withstand voltage of a LDD structure MOS type semiconductor integrated circuit can be increased, without causing a deterioration in the properties of the integrated circuit, which has major practical implications." ID at 62. The ALJ interpreted this statement as telling one of ordinary skill that he could "increase the effect of the invention," and stated that the publication "invites one to go to the art and to find the necessary information needed to effect such an increase." ID at 62. The above-quoted statement in Umemoto, however, describes the effect of the invention as to "increase" "the electrostatic breakdown withstand voltage." *See, e.g.*, Umemoto at 3 ("The purpose of this invention is to solve these past defects and to provide a semiconductor integrated circuit that *increases the electrostatic breakdown withstand voltage of the LDD structure MOS type semiconductor integrated circuits*, without inviting deterioration of the properties of the integrated circuit"). Thus, the statement in Umemoto is *not* an invitation "to go to the art and to find the necessary information needed to effect . . . an increase." Because the ALJ's analysis is incorrect in this regard, respondents' reliance on the ALJ's analysis of Umemoto to support a finding of motivation to combine is misplaced. *See* Respondents' brief at 79-80.

In their briefing to the Commission, respondents generally rephrase the argument they made before the ALJ (summarized in the ID at 60-62), *viz.*, that starting from Kamioka or Soeda, it would have been obvious to one of skill in the art to substitute the ESD protection device of Umemoto for the individual protection devices disclosed as connected together in Kamioka or Soeda.[52] Respondents assert, relying on *In re Raynes*, 7 F.3d 1037 (Fed. Cir. 1993), and *Smith v. Hayashi*, 209 USPQ 754, 759 (Bd. of Pat. Inter. 1980), that "[a] combination claim is obvious over a prior art reference that discloses a similar combination in which one of the claimed components is replaced with a substitute component that is known to be structurally and functionally equivalent." Respondents' brief at 78.

Respondents' argument is not persuasive because they have not identified clear and convincing evidence that one of skill in the art would know that the ESD protection devices of Kamioka, Soeda, and Umemoto are structurally and functionally equivalent. The statement in the ID that "[o]ne skilled in the art would have understood at the time of the alleged invention of the '352 patent that any ESD protection devices could have been substituted for the generic ESD protection devices of Kamioka" (ID at 61), upon which respondents rely in their brief, is a restatement by the ALJ of respondents' arguments rather than a finding of fact made by the ALJ. We reach this conclusion because the statement in the ID is not supported by any citations to the record, and appears in a long single-paragraph summary of respondents' arguments as to motivation to combine. Moreover, the paragraph immediately following the summary of

[52] Respondents have apparently not argued that the testimony of their expert (Peltzer) at 778 is sufficient to establish a motivation to combine the references. The IA is correct that Peltzer's testimony, standing alone, is insufficient in this regard. *Upjohn Co. v. MOVA Pharm. Corp.*, 225 F.3d 1306, 1310-11 (Fed. Cir. 2000).

respondents' arguments begins with the statement, "[t]he arguments made by Respondents concerning the motivation to combine the Umemoto publication with the Soeda or the Kamioka publication are persuasive;" ID at 62. This statement would be redundant given an earlier adoption of respondents' argument by the ALJ.

In their reply brief, respondents assert that "since one skilled in the art would know that one ESD transistor type (*i.e.*, one type of NMOS transistor) can be substituted for another in the Kamioka or Soeda dual-transistor ESD devices, one would know he could substitute an Umemoto-type ESD transistor for the transistors disclosed in Kamioka or Soeda." Respondents' reply at 34. In support of their argument, respondents state that "the ESD transistor disclosed in Umemoto is an N-channel MOS (NMOS) transistor, which is what is called for in the '352 patent and by both Kamioka and Soeda." Respondents' reply at 34.[53] Respondents state that "Soeda specifies that 'N-type MOSFETS 5, 6' be used." Respondents' reply at 34 (citing Soeda, at 2, lines 13-15 ("A polysilicon resistor 1, diffusion layer resistor 2, stray capacitances 3, 4, i.e., diffusion layers, and N-type MOSFETSs 5, 6 are shown in Figure 3"). Respondents state that "Kamioka specifies that 'two N-channel MOS transistors' be used." Respondents' reply at 34 (citing Kamioka at 1). This argument was apparently never presented to the ALJ. *See* respondents post-hearing brief (Nov. hearing) at 4-5 (filed Dec. 5, 2001); respondents post-hearing reply brief (Nov. hearing) at 19-20 (filed Dec. 27, 2001). By raising this argument for

[53] Respondents cite the following specific language in Umemoto and the '352 patent: Umemoto, at 3, lines 30-31 ("Figure 1 is a sectional drawing of a N channel MOS transistor of this invention") and '352 patent, col. 4, ll. 42-46 ("The invention can be more fully understood by referring to the circuit diagram of FIG. 8. An ESD protection device 40, made by the inventive method, is shown connected to input, or output, (I/O) pad 70, and consists of two NMOS devices.").

the first time in their reply brief, complainants and the IA have been denied the opportunity to respond.

Respondents' new argument is not persuasive on the merits. Although they have identified statements in Kamioka and Soeda indicating that N-MOS transistors are used (*see also* FF140, 148, 152) in the disclosed input protection circuits, and indicating that Umemoto discloses an N-channel MOS transistor (*see also* FF 135), respondents have not identified any evidence (let alone clear and convincing evidence) as to why these particular statements would be understood by one of skill in the art as establishing that (1) one type of NMOS transistor can be substituted for another kind of NMOS transistor in the Kamioka or Soeda input protection circuits, or that (2) the N-channel MOS transistor of Umemoto could be substituted for the N MOS transistors used in Kamioka and Soeda. Moreover, respondents have not demonstrated by clear and convincing evidence that the teachings they have identified would suggest to one of skill in the art substituting the ESD protection device of Umemoto for the devices connected together in Kamioka or Soeda. *Compare Sandt Tech., Ltd. v. Resco Metal and Plastics Corp.*, 264 F.3d 1344, 1355 (Fed. Cir. 2001) (obvious substitution of claimed threaded studs for welds disclosed in prior art found where "weld was inconvenient . . . [u]sing studs was . . . cleaner, faster, and more convenient") *with Gillette Co. v. S.C. Johnson & Son, Inc.*, 919 F.2d 720, 724 (Fed. Cir. 1990) (although individual components of claimed composition were well known at the time of the invention, claimed composition is not made obvious by "prior art [that] made no suggestion, *clear or otherwise*, of substituting the claimed water-soluble polymers for [prior art] oil-soluble jellifying agent").

In their reply brief, respondents raise another new argument. They contend that, because Kamioka and Soeda do not disclose how to build the individual ESD transistors, one of skill in the art would look to Umemoto or other references to complete the device. This argument was apparently never presented to the ALJ. *See* respondents post-hearing brief (Nov. hearing) at 4-5 (filed Dec. 5, 2001); respondents post-hearing reply brief (Nov. hearing) at 19-20 (filed Dec. 27, 2001). By raising this argument for the first time in their reply brief, complainants and the IA have been denied the opportunity to respond. The argument is incorrect with respect to Soeda because complainants' expert (Fair) testified at 1061-62 that Soeda addresses at least some aspects of building ESD transistors. Further, respondents' argument fails with respect to Kamioka because respondents have not established by clear and convincing evidence that one of skill in the art would look to Umemoto to build the individual ESD transistors of Kamioka.

As discussed above, the Commission determined that the ALJ's analysis finding a motivation to combine Umemoto with Kamioka or Soeda is incorrect, and rejected the arguments raised by respondents in support of finding a motivation to combine the references. Because the required motivation to combine the references is lacking,[54] the Commission determined to reverse the ALJ's conclusion that independent claim 8 of the '352 patent is invalid as made obvious by the combination of Umemoto with either Soeda or Kamioka.

In their brief to the Commission, respondents also raised the argument that claim 8 is rendered obvious by Umemoto itself. In support of this argument, respondents pointed to the

[54] The motivation to select the combination of components used by the inventor is an "essential evidentiary component of an obviousness holding." *C.R. Bard, Inc. v. M3 Sys., Inc.*, 157 F.3d 1340, 1352 (Fed. Cir. 1998) (reversing jury verdict based on obviousness where no prior art provided teaching or showing of motivation to modify prior art).

ALJ's finding that "one of ordinary skill in the art would have an advanced degree such as a master's degree (or equivalent education or experience), in a field relevant to ESD technology, such as electrical engineering or physics, and further, such a person would have substantial experience in integrated circuit and device design" (ID at 12). Respondents then asserted that Umemoto itself would provide the motivation to put two of the Umemoto devices together "simply to build a larger ESD device to protect a larger circuit or a more delicate circuit device." Respondents' brief at 77. Respondents' argument that Umemoto alone renders claim 8 obvious is not persuasive because (1) by not raising this invalidity theory in their pre-hearing statement before the ALJ, respondents have waived it (Respondents' pre-hearing statement at 38-40; ALJ ground rule 4.d (Order No. 2 at 7)), (2) respondents have cited no evidence supporting their argument concerning what one of skill in the art would have understood from Umemoto, and (3) respondents have failed to address the disclosure of the last three limitations of claim 8 (*viz.*, "a first electrical connection," "a second electrical connection," and "a third electrical connection") under their new, only Umemoto, obviousness theory.[55]

2. Whether Soeda Discloses the "First Electrical Connection" (claim 8)

In their briefing to the Commission, complainants argued that Umemoto combined with Soeda does not render claim 8 obvious, separate and apart from the motivation to combine issue, because Soeda lacks the element of claim 8 dealing with the first electrical connection. For the reasons discussed below, the Commission determined to affirm the ALJ's implicit finding that

[55] The Umemoto claim charts in Appendix E to respondents' brief only address claims 1 and 2 of the '352 patent; the claim charts for claim 8 are Umemoto/Kamioka and Umemoto/Soeda.

Soeda discloses the element of claim 8 dealing with the first electrical connection. ID at 57-58. 63; FF 148-152.

The ALJ found that "[t]he necessary disclosures which make claim 8 of the '352 patent obvious in conjunction with the Umemoto publication are found in . . . the Soeda publication." ID at 63. Complainants argued that "respondents' expert was forced to concede at the hearing" that Soeda lacks the element of claim 8 dealing with the first electrical connection." Complainants' reply at 51 n.12 (citing Trans. (Peltzer) at 1007). The claim limitation at issue concerns a connection between the input/output pad and the *drain* regions of the first and second ESD protection devices. The limitation reads "a first electrical connection between said input/output pad, said drain regions of said first and second ESD protection devices, and said integrated circuit." '352 patent, col. 6, ll. 28-30.

The cited testimony by respondents' expert (Peltzer) reads as follows:

> Q Would you turn to Exhibit 166, your table for the Soeda publication, RX 166? And in particular, I want to focus on the first electrical connection which is referred to in the bottom box on the first page. Now, on the left you cite the provisions of claim 8 of the '352, which require that the first electrical connection between said input/output pad and said drains, it requires that connection between the input/output pad and the drains; correct?
>
> A Yes.
>
> Q And you read that provision as being satisfied by Soeda; correct?
>
> A Yes.
>
> Q Would you turn to the next page on your chart. In particular, the second box. *Do you recite Soeda for the proposition that the drain of MOSFET 5 is connected to*

power potential V?

A Yes, and now here, we have a third electrical connection to a voltage source of said first ESD protection device, and the connection which is made is the drain -- as described in Soeda. is the drain of MOSFET 5, whereas on the previous page. we have '352 talking about the drains being connected to the pad.

Now, as we've discussed, especially in the use of the term "source/drain region," unless there's some distinguishing characteristic, these devices are symmetrical. So Soeda has installed the device and termed it backwards from the connections identified in the '352. That's permissible. This is a symmetrical device. That's why we went to the Kamioka, because it was clearer.

This is the same teaching. I mean, this is the circuit and the connections are still the same. They just call the terminals of the upper device different names.

Trans. (Peltzer) 1007:1-1008:8 (emphasis added). The next question and answer reads:

Q And notwithstanding those changes in which source or drain are being connected, you find that it read [sic] on claim 8 of the '352 patent; correct?

A Yes, because I'm aware that that device is a symmetrical device and this is a problem of nomenclature.

Trans. (Peltzer) 1008:9-1008:13.

The ALJ's findings of fact, specifically FF 148-152, are fully consistent with this testimony. Relying on complainants' expert (Fair), the ALJ found that "[s]tructurally, a source and a drain may be identical." FF 151. He further found that "[i]n NMOS symmetric devices, source regions and drain regions can be flipped. The source and drain of the first MOSFET 5 can be flipped such that the drain is connected to pad 8 and the source is connected to the potential V." FF 152 (citations omitted). The ALJ's implicit finding that Soeda discloses the element of claim 8 dealing with the first electrical connection is supported by the ALJ's findings of fact and

the testimony of respondents' expert (Peltzer). FF 148-152. Trans. (Peltzer) 1008:9-1008:13.

REMEDY, THE PUBLIC INTEREST, AND BONDING

On May 13, 2002, the ALJ issued his recommended determination ("RD") on remedy and bonding. The ALJ recommended that, in the event the Commission were to find a violation of section 337, it should issue a limited exclusion order[56] under section 337(d) directed to respondents' infringing products (including chipsets and graphics chips). RD at 6, 9. The ALJ recommended that any limited exclusion order cover products made for respondents by third party manufacturers/fabricators in addition to products made by respondent Silicon Integrated Systems Corp. of Hsinchu City, Taiwan. RD at 7-8. He also recommended that any limited exclusion order cover some downstream products, specifically motherboards containing respondents' infringing circuits, but not computers or point-of-sale terminals. RD at 8 (stating that the IA had "proposed a reasonable balancing of the *EPROMs* factors"). The ALJ stated that "there is precedent for a certification provision to allow third parties to certify that their motherboards do not contain excluded SiS parts."[57] RD at 9 (citing *Certain Electrical Connectors and Products Containing Same*, Inv. No. 337-TA-374, Order, ¶ 4 (May 3, 1996). The ALJ did not recommend issuance of cease and desist orders, and none were requested by complainants. RD at 6 n.5. Finally, the ALJ recommended that, in the event a violation of section 337 is found, the Commission impose a bond during the 60-day Presidential review

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[56] Complainants have not requested issuance of a general exclusion order.

[57] A certification provision facilitates the administration of an exclusion order by the U.S. Customs Service by permitting importers to certify that the imported motherboards do not contain respondents' infringing circuits. Certification is required at the discretion of Customs.

period in the amount of 100 percent of entered value. RD at 9-10.

The Commission determined to adopt the ALJ's recommended determination as to remedy and bonding with the modification that, although the amount of the bond for integrated circuits subject to the Commission's order is 100 percent of entered value, the amount of the bond for motherboards containing such integrated circuits should be 39 percent of entered value.

Remedy

The U.S. Court of Appeals for the Federal Circuit has recognized that "the Commission has broad discretion in selecting the form, scope, and extent" of the remedy. *Viscofan, S.A. v. United States Int'l Trade Comm'n*, 787 F.2d 544, 548 (Fed. Cir. 1986); *see also Hyundai Elecs. Indus. Co. v. United States Int'l Trade Comm'n*, 899 F.2d 1204 (Fed. Cir. 1990). Complainants argued that any limited exclusion order should extend to other downstream products containing the accused products in addition to motherboards, including laptop computers, personal computers, and point-of-sale terminals. Respondents argued that any limited exclusion order should not extend to any downstream products containing the accused products, not even to motherboards. The IA supported the RD.

With respect to whether a limited exclusion order should cover downstream products, in *Certain Erasable Programmable Read Only Memories, Components Thereof, Products Containing Such Memories, and Processes for Making Such Memories*, Inv. No. 337-TA-276, USITC Pub. No. 2196 (Mar. 16, 1989) (*EPROMs*), the Commission identified ten factors (the *EPROMs* factors) bearing on the issue, and the Commission's approach was approved by the Federal Circuit in *Hyundai*. 899 F.2d at 1209.

In their briefing to the Commission, complainants and the IA generally repeated the arguments they made before the ALJ concerning the *EPROMs* factors. Respondents also repeated the arguments that they raised before the ALJ. Respondents further argued that, because

[[

]] Respondents also contended that [[

]]

The IA responded that respondents' first argument "can be made by almost any respondent that makes infringing components." IA's reply at 36. Complainants characterized respondents' arguments as "overstated speculation" and asserted that there is "absolutely no evidence in the record" of [[

]] Complainants' reply at 113. The IA submitted that "nothing in the evidentiary record shows that these [[

]] " and that "the fact that providing effective relief to Complainants may result in some inconvenience to

Respondents' customers is not an adequate basis for declining such relief." IA's reply at 36. In their reply brief, respondents argued that --

> [c]urrently, [[
>
>]]

Respondents' reply at 90.

The RD's conclusion that motherboards, but not computers or point-of-sale terminals, should be included in the limited exclusion order was based on the ALJ's acceptance of the "reasonable balancing of the *EPROM* factors" proposed by the IA, and respondents' new arguments provide no persuasive reason not to follow the ALJ's recommendation in this regard. By providing citations to the record in support of their argument only in their reply brief, respondents denied the IA and complainants the opportunity to respond. The Commission determined that the cited testimony does not demonstrate that [[

]] In any event, we agree with the IA that inconvenience to respondents' customers is not an adequate basis for denying effective relief to complainants. In their briefing to the Commission, respondents also argued that "[c]omplainants' and [the IA's] inclusion of the words 'or withdrawal from a warehouse for consumption' in their respective proposed limited exclusion orders [is] inappropriate because, as all parties agree, a cease and desist is not warranted in this investigation." Respondents' reply at 90 n.10. However, the "withdrawal from a warehouse for consumption" language in the proposed limited exclusion

order is standard and has been included in previous limited exclusion orders. *E.g., Certain 4-Androstenediol*, 337-TA-440, Limited Exclusion Order (Aug. 2, 2001) (no request for cease and desist order); *Certain Oscillating Sprinklers, Sprinkler Components, and Nozzles*, 337-TA-448, Limited Exclusion Order (Mar. 1, 2002) (no request for cease and desist order).

In this investigation, the Commission found a violation of section 337 only as to claim 13 of the '345 patent. Claim 13 is a method claim. The ALJ found that respondents' old SiON process infringes claim 13, but that respondents' new N_2O plasma treatment process does not infringe. ID at 99, 120, 276. Respondents argue that complainants' and the IA's proposed limited exclusion order language "imposes a burden on the importer and the Customs Service in that it requires them to know which [[

]] infringes any claims of the '345 patent." Respondents' reply at 91. They urge that the certification provision should "require the importer to declare [[

]]." Respondents' reply at 91. The limited exclusion order in this investigation reads in relevant part as follows:

> Pursuant to procedures to be specified by U.S. Customs Service, as the Customs Service deems necessary, persons seeking to import integrated circuits, including chipsets and graphics chips, or motherboards containing same, that are potentially subject to this Order shall certify that they are familiar with the terms of this Order, that they have made appropriate inquiry, and thereupon state that, to the best of their knowledge and belief, the products being imported are not excluded from entry under paragraph 1 of this Order.

Limited exclusion order ¶ 4. The certification language is standard and has been included in many previous limited exclusion orders. *E.g., Certain Integrated Repeaters, Switches,*

Transceivers and Products Containing Same, 337-TA-435, Limited Exclusion Order (Oct. 24, 2001). We see no reason to deviate from that language here. Moreover, method claims (like claim 13) are the classic example of situations where a certification provision is appropriate. This is so because, as far as we are aware, there is no way to know from inspecting an imported chip how it was made.

Before the ALJ, respondents argued that an exclusion order should cover only infringing integrated circuits manufactured by respondents, and not [[

]]

Respondents' post-hearing brief at 46 n.9. The ALJ rejected this argument, reasoning as follows:

> With respect to the question of whether an exclusion order should cover only devices made at [Silicon Integrated System Corp. of Hsinchu City, Taiwan], there appears to be no basis for making such a recommendation. As pointed out by the [IA], Commission exclusion orders ordinarily focus on whether or not a product infringes or is made by a process that infringes a suit patent, and may, for example, cover products manufactured abroad and/or imported by or on behalf of a respondent or any of its affiliated companies, parents, subsidiaries, or other related business entities, or their successors or assigns. Such exclusion orders cannot be circumvented merely by having an infringing product made, or by having an infringing process carried out, by another overseas fab. Consequently, it is not recommended that the Commission limit any exclusion order that may issue in this investigation so as to permit third-party fabrication.

ID at 7-8.

In their briefing to the Commission, respondents argued that, by extending the limited exclusion order to cover third party manufacturers and fabricators, the order effectively becomes a general exclusion order. They maintained that, in *EPROM, EEPROM, Flash Memory, and*

Flash Microcontroller Semiconductor Devices, and Products Containing Same, Inv. No. 337-TA-395, the Commission refused to modify a limited exclusion order to cover third party foundries. They quoted the following from a Commission notice in that investigation:

> Atmel has not established that any semiconductor devices manufactured for intervenor Silicon Storage Technology, Inc. by foreign foundries other than Sanyo Electric Co., Ltd. and/or Winbond Electronics Corporation of Taiwan infringe the claims at issue of the '903 patent. If Atmel believes that it can support such allegations and that the Commission's limited exclusion order should be modified, it may petition the Commission to modify the exclusion order pursuant to rule 210.76 (19 C.F.R. § 210.76).

EPROM, EEPROM, Flash Memory, and Flash Microcontroller Semiconductor Devices, and Products Containing Same, Inv. No. 337-TA-395, Notice (Dec. 19, 200). In response, complainants argued that the above-quoted notice relied upon by respondents "contains little explanation [and] appears to be narrowly intended to respond to specific, unstated 'concerns' expressed by the complainant's counsel, apparently relating to the enforcement of an exclusion order by the Customs Service," and asserted that the Commission has issued limited exclusion orders containing the "by or on behalf of" language. Complainants' reply at 113-14.

The ALJ considered respondents' request to limit the exclusion order to infringing products manufactured by respondents, and correctly rejected it because "exclusion orders cannot be circumvented merely by having an infringing product made, or by having an infringing process carried out, by another overseas [fabricator]." RD at 8. The ALJ followed the Commission's standard practice of extending exclusion orders to cover infringing products made

on behalf of a respondent.[58]

Public Interest

By rule, the ALJ's RD on remedy and bonding did not address the issue of the public interest. Commission rule 210.50(b)(1).

Respondents asserted that the inclusion of downstream products or chips manufactured by third parties in any limited exclusion order would adversely affect competitive conditions in the U.S. economy, the production of like or directly competitive articles in the United States, and U.S. consumers. They suggest that limiting the exclusion order to infringing chipsets manufactured by respondents would avoid adverse effects on the public interest by avoiding disruption to legitimate trade and limiting disruption of the personal computer and motherboard industry caused by increased importation difficulties.

The IA argued that no public interest concerns are raised by the RD because "there is no evidence that the U.S. demand for [r]espondents' accused products cannot be met by other entities. Moreover, there is no evidence that the products at issue are the types of products that would implicate any public interest concerns that would militate against entry of a limited

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[58] The language appears in the following limited exclusion orders: *Certain Variable Speed Wind Turbines and Components Thereof*, Inv. No. 337-TA-376, Order (Aug. 30, 1996); *Certain Oscillating Sprinklers, Sprinkler Components, and Nozzles*, Inv. No. 337-TA-448, Limited Exclusion Order (Mar. 1, 2002); *Certain 4-Androstenediol*, Inv. No. 337-TA-440, Limited Exclusion Order (Aug. 2, 2001); *Certain Integrated Repeaters, Switches, Transceivers and Products Containing Same*, Inv. No. 337-TA-435, Limited Exclusion Order (Oct. 24, 2001); *Certain Condensers, Parts Thereof and Products Containing Same, Including Air Conditioners for Automobiles*, Inv. No. 337-TA-334 (Remand), Order (Aug. 20, 1997); *Certain Flash Memory Circuits and Products Containing Same*, Inv. No. 337-TA-382, Limited Exclusion Order (June 2, 1997); *Certain Neodymium-Iron-Boron Magnets, Magnet Alloys, and Articles Containing Same*, Inv. No. 337-TA-372 (Enforcement Proceeding), Limited Exclusion Order (Sept. 26, 1997). Although the "by or on behalf of" language does not appear in the October 15, 1997, limited exclusion order issued in *Certain Toothbrushes and the Packaging Thereof* cited by complainants, that order excludes infringing products manufactured abroad by "contractors" of the respondents subject to the order.

exclusion order against [r]espondents. and [the IA] is not aware of any other public interest concerns or any arguments by [r]espondents or any non-parties to that effect." IA's brief at 77; *see also* complainants' brief at 150-51.

Under section 337(d). the Commission must consider the effect of any remedy on the public interest before issuing an exclusion order. We are aware of no public interest concerns presented in the instant investigation that should prevent the issuance of a limited exclusion order. We agree with the IA that there is no evidence that the U.S. demand for respondents' accused products cannot be met by other entities.

Bonding

Pursuant to section 337(j)(3), the bond during the Presidential review period is to be set "in an amount determined by the Commission to be sufficient to protect the complainant from any injury." 19 U.S.C. § 1337(j)(3). The limited exclusion order covers integrated circuits, including chipsets and graphic chips. that are made by a process covered by claim 13 of the '345 patent and motherboards containing such integrated circuits. In the RD, the ALJ found[[

]] RD at 8-9. Consequently, the Commission has determined that if the amount of the bond for integrated circuits subject to the Commission's order is 100 percent of entered value as recommended by the RD, the bond for motherboards containing such integrated circuits should be set at 39 percent of entered value, given the statutory purpose of the bond to protect complainants from "any injury."

Respondents argued that the bond during the Presidential review period should not

exceed 10 percent of the entered value of the integrated circuits in question. They argued that the Commission has set Presidential review period bonds based on the price differential between the domestic and infringing product or based on a reasonable royalty rate. They asserted that, [[

]] Respondents further asserted that "[t]here is no evidence [[

]] Respondents' remedy brief at 12. They contended that a 100 percent bond would be unjust because "the evidentiary failure rests with [c]omplainants." Respondents' remedy brief at 12. Relying on *Certain Neodymium-Iron-Boron Magnets, Magnet Alloys, and Articles Containing Same*, Inv. No. 337-TA-372, USITC Pub. No. 2964, Commission Opinion on Remedy, Public Interest, and Bonding at 15 (May 1996), the IA argued that, absent comparative price information, reasonable royalty rate, or other reasonable formulations to compensate for the harm to complainants, a bond of 100 percent of the entered value is appropriate. Complainants asserted that, [[

]]there has been no evidentiary failure on their part. The IA argued that comparative price information is not useful to calculate the bond because respondents make chipsets and graphics chips, while complainant United Microelectronics Corporation "acts as a foundry for various third party customers" and "does not appear to manufacture such products." IA's brief at 78-79.

The Commission has determined to adopt the ALJ's recommendation to set the bond for

integrated circuits subject to the Commission's order at 100 percent of entered value. The ALJ stated that "no proposal was made concerning a reasonable royalty rate, a bond based on a reasonable price comparison, or any other reasonable formula. Furthermore, Respondents do not rely on any substantial evidence in opposing a bond of 100%." RD at 10. No party appears to have challenged these findings. Although a 100 percent bond is justified by previous Commission decisions,[59] the Commission appears not to have been faced before with the current situation, *i.e.*, where complainants may be in control of information that would provide a reasonable basis for setting a lower bond. Consequently, the Commission has not been presented with the particular "injustice" urged by respondents. However, respondents have not shown that the pricing information in question is missing through any fault of complainants, and they have not contended that complainants withheld any relevant information. The Commission has therefore determined to set the bond for integrated circuits subject to the Commission's order at 100 percent of entered value, and to set the bond for motherboards containing such integrated circuits at 39 percent of entered value.

[59] *E.g.*, *Certain Flash Memory Circuits and Products Containing Same*, Inv. No. 337-TA-382, USITC Pub. No. 3046, Comm'n Op. at 26-27 (July 1997); *Certain Neodymium-Iron-Boron Magnets, Magnet Alloys, and Articles Containing Same*, Inv. No. 337-TA-372, USITC Pub. No. 2964, Commission Opinion on Remedy, Public Interest, and Bonding at 15 (May 1996).

CERTAIN INTEGRATED CIRCUITS, PROCESSES FOR MAKING SAME, AND PRODUCTS CONTAINING SAME **337-TA-450**

CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the **PUBLIC VERSIONS OF COMMISSION OPINON AND ORDER** was served upon the following parties via first class mail and air mail where necessary, on July 24, 2003.

Marilyn R. Abbott, Secretary
U.S. International Trade Commission
500 E Street, SW - Room 112
Washington, DC 20436

ON BEHALF OF COMPLAINANT UNITED MICROELECTRONICS CORPORATION, UMC GROUP AND UNITED FOUNDRY SERVICE, INCORPORATED:

Steven J. Routh, Esq.
Hogan and Hartson
555 13th Street, NW
Washington, DC 20004

William H. Wright, Esq.
Biltmore Tower
Hogan and Hartson
500 S. Grand Avenue
Suite 1900
Los Angeles, CA 90071

ON BEHALF OF SILICON INTEGRATED SYSTEMS CORPORATION:

Tom M. Schaumberg, Esq.
Adduci, Mastriani and Schaumberg, LLP
1200 Seventeenth Street, NW
Fifth Floor
Washington, DC 20036

Kirk R. Ruthenberg, Esq.
Sonnenschein Nath and Rosenthal
1301 K Street, NW
Suite 600, East Tower
Washington, DC 20005

Edward H. Rice, Esq.
Sonnenschein Nath and Rosenthal
8000 Sears Tower
Chicago, IL 60606

Michael A. Molano, Esq.
Sonnenschein Nath and Rosenthal
685 Market Street, 6th Floor
San Francisco, CA 94105

ON BEHALF OF THE COMMISSION:

Shival P. Virmani, Esq.
Commission Investigative Attorney
Office of Unfair Import Investigation
500 E Street, SW - Room 401-J
Washington, DC 20436

James B. Coughlan, Esq.
Commission Investigative Attorney
Office of Unfair Import Investigations
500 E Street, SW - Room 401-L
Washington, DC 20436

Timothy Monaghan, Esq.
Advisory Attorney
Office of General Counsel
500 E Street, SW - Room 707-U
Washington, DC 20436

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C. 20436

In the Matter of	)	
CERTAIN INTEGRATED CIRCUITS, PROCESSES FOR MAKING SAME, AND PRODUCTS CONTAINING SAME	)	Inv. No. 337-TA-450

NOTICE OF COMMISSION DECISION TO REVIEW PORTIONS OF AN INITIAL DETERMINATION FINDING NO VIOLATION OF SECTION 337 OF THE TARIFF ACT OF 1930

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has determined to review certain portions of a final initial determination (ID) of the presiding administrative law judge (ALJ) finding no violation of section 337 of the Tariff Act of 1930, as amended, in the above-captioned investigation.

FOR FURTHER INFORMATION CONTACT: Clara Kuehn, Esq., Office of the General Counsel, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 205-3012. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on 202-205-1810. General information concerning the Commission may also be obtained by accessing its Internet server (*http://www.usitc.gov*).

Copies of the public version of the ALJ's ID and all other nonconfidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone 202-205-2000.

SUPPLEMENTARY INFORMATION: The Commission instituted this investigation by notice published in the *Federal Register* on March 6, 2001. 66 *Fed. Reg.* 13567 (2001). The complainants are United Microelectronics Corporation, Hsinchu City, Taiwan; UMC Group (USA), Sunnyvale, CA; and United Foundry Service, Inc., Hopewell Junction, NY. *Id.* The Commission named two respondents, Silicon Integrated Systems Corp., Hsinchu City, Taiwan, and Silicon Integrated Systems Corporation, Sunnyvale, CA (collectively, "SiS"). *Id.* The

complaint, as supplemented, alleged violations of section 337 in the importation, the sale for importation, and the sale within the United States after importation of certain integrated circuits and products containing same by reason of infringement of claims 1, 2, and 8 of U.S. Letters Patent 5,559,352 ("the '352 patent") and claims 1, 3-16, and 19-21 of U.S. Letters Patent 6,117,345 ("the '345 patent"). *Id.*

On November 2, 2001, the presiding ALJ issued an ID (ALJ Order No. 15) granting complainants' motion for summary determination on the issue of importation and denying respondents' motion for summary determination of lack of importation. That ID was not reviewed by the Commission. A tutorial session was held on November 5, 2001, and an evidentiary hearing was held from November 7, 2001, through November 16, 2001, and from December 10, 2001, through December 12, 2001.

The ALJ issued his final ID on May 6, 2002, concluding that there was no violation of section 337. With respect to the '352 patent, the ALJ found that: complainants have not established that the domestic industry requirement is met; none of respondents' accused devices practice any asserted claim of the '352 patent literally or under the doctrine of equivalents; and claims 1 and 2 of the '352 patent are invalid as anticipated under 35 U.S.C. § 102 and claim 8 of the '352 patent is invalid for obviousness under 35 U.S.C. § 103. The ALJ found each of the '345 patent claims listed in the notice of investigation, *i.e.*, claims 1, 3-16, 19-20, and 21, invalid as anticipated by and made obvious by certain prior art. The ALJ stated that, in their post-hearing filings, complainants asserted only claims 1, 3-5, 9, 11-13, and 20-21 of the '345 patent against respondents. He found that, if valid, each of the asserted claims of the '345 patent, *i.e.*, claims 1, 3-5, 9, 11-13, and 20-21, is literally infringed by SiS's existing (or old) SiON manufacturing process, but that respondents' new N_2O process does not infringe any asserted claim of the '345 patent. The ALJ further found that a domestic industry exists with respect to the '345 patent. On May 13, 2002, the ALJ issued his recommended determination on remedy and bonding.

On May 17, 2002, complainants and the Commission investigative attorney ("IA") petitioned for review of the subject ID, and respondents filed a contingent petition for review. On May 24, 2002, complainants, the IA, and respondents filed responses.

Having examined the record in this investigation, including the ID, the petitions for review, and the responses thereto, the Commission has determined to review and clarify that the ALJ found claim 13 of the '345 patent made obvious, but not anticipated, by the Tobben patent. The Commission has also determined to review:

(1) the ALJ's findings and conclusions of law regarding the '352 patent with respect to infringement of the asserted claims and domestic industry under the doctrine of equivalents;

(2) the ALJ's finding that respondents' old E5 model ESD transistor does not infringe any asserted claim of the '352 patent, either literally or equivalently;

(3) the ALJ's claim construction of the limitations "an ESD protection device" (claims 1, 2, and 8 of the '352 patent), "a gate" (claims 1 and 2), "gates" (claim 8), and "source/drain

regions . . . with each source/drain region comprising" (claims 1, 2, and 8), and the ALJ's invalidity, domestic industry, and infringement findings and conclusions of law with respect to those limitations;

(4) the ALJ's finding that claim 8 of the '352 patent is invalid as made obvious by a combination of prior art references;

(5) whether the economic prong of the domestic industry requirement is met with respect to the '352 patent;

(6) the ALJ's findings that the "second antireflective coating" (claim 1 and asserted dependent claims 3-8 of the '345 patent) and "cap layer" (claims 9-16, 19-20, and 21 of the '345 patent) are disclosed in the Tobben patent, and consequently (a) the ALJ's findings with respect to etching the second antireflective coating or cap layer (claims 4 and 12), (b) the ALJ's ultimate finding that the Tobben patent anticipates claims 1, 3-16, 19-20, and 21 of the '345 patent, and (c) the ALJ's conclusion that claim 13 is made obvious by the Tobben patent and other prior art;

(7) the ALJ's conclusion that claim 13 of the '345 patent is invalid as obvious in light of the Tobben patent; and

(8) the ALJ's conclusion that claims 1, 3-16, 19-20, and 21 of the '345 patent are invalid as made obvious by the Abernathey patent in combination with the Pan, Yagi, and/or Yota publications.

The Commission has determined not to review the remainder of the ID, including the ID's conclusions and findings of fact with respect to whether the Tobben patent is prior art to the '345 patent, infringement of the asserted claims of the '345 patent, domestic industry concerning the '345 patent, and failure to disclose the best mode of practicing the invention of the '345 patent.

On review, the Commission requests briefing based on the evidentiary record on all issues under review and is particularly interested in receiving answers to the following questions, with all answers cited to the evidentiary record:

1. Have complainants established the economic prong of the domestic industry requirement with respect to the '352 patent?

2. Should the term "an ESD protection device" in claims 1, 2, and 8 of the '352 patent be construed to require a protection device that is separate and apart from the circuit it protects?

3. Assuming that the term "a gate" refers to a single, particular gate for a specific FET (but without excluding multiple-FET ESD protection devices) (ID at 14-15), should the limitation "source/drain regions . . . with each source/drain region comprising" be construed as excluding from the claimed ESD protection device source/drain regions that lack one or more of the three implants (*i.e.*, the "first lightly implanted region," "heavier implanted region," and "second lightly implanted region")? In responding to this question please address the "open" transition in claim 1 of the '352 patent ("An ESD protection device . . . *comprising*").

4. In light of your answers to questions 2 and 3, are claims 1, 2, or 8 of the '352 patent infringed (literally or under the doctrine of equivalents)? Have complainants established the

technical prong of the domestic industry requirement with respect to the '352 patent? In your response, please address *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S.Ct. 1831 (2002).

5. Does respondents' old E5 model ESD transistor infringe any asserted claim of the '352 patent? In your response, please address *Symbol Technologies, Inc. v. Opticon, Inc.*, 935 F.2d 1569 (Fed. Cir. 1991).

6. In light of your answers to questions 2 and 3, are claims 1, 2, or 8 of the '352 patent invalid?

7. In light of the ALJ's construction of the term "antireflective coating" to require, *inter alia*, "an antireflective effect . . . whether through absorption or interference . . . significant to the purposes of the invention" (ID at 79), does the Tobben patent's planarization layer disclose the "second antireflective coating" of claim 1 (and dependent claims 3-8) of the '345 patent?

8. In light of the ALJ's construction of the term "cap layer" of independent claims 9 and 21 of the '345 patent (ID at 119-20), does the Tobben patent disclose a cap layer that acts as either (a) an "antireflective coating" or (b) a protector for the top corners of metal wiring lines during the HDPCVD process? With respect to (a), above, please address column 3, lines 6-20 of the Tobben patent.

9. Assuming that claim 9 of the '345 patent is anticipated by the Tobben patent, is claim 13 obvious?

10. For purposes of obviousness under 35 U.S.C. § 103, does the Abernathey patent teach one of ordinary skill in the relevant art a barrier layer that serves as an "antireflective coating"? In your response please address how one of ordinary skill in the art would understand the thickness of the silicon dioxide barrier layer disclosed in the Abernathey patent.

11. Was the issue of the publication dates of the Yota, Pan, and Yagi references (*see* complainants' petition for review at 77) raised before the ALJ?

In connection with the final disposition of this investigation, the Commission may issue (1) an order that could result in the exclusion of the subject articles from entry into the United States, and/or (2) cease and desist orders that could result in respondents being required to cease and desist from engaging in unfair acts in the importation and sale of such articles. Accordingly, the Commission is interested in receiving written submissions that address the form of remedy, if any, that should be ordered. If a party seeks exclusion of an article from entry into the United States for purposes other than entry for consumption, the party should so indicate and provide inform-ation establishing that activities involving other types of entry that either are adversely affecting it or are likely to do so. For background information, see the Commission Opinion, *In the Matter of Certain Devices for Connecting Computers via Telephone Lines*, Inv. No. 337-TA-360.

If the Commission contemplates some form of remedy, it must consider the effects of that remedy upon the public interest. The factors the Commission will consider include the effect that an exclusion order and/or cease and desist orders would have on (1) the public health and welfare, (2) competitive conditions in the U.S. economy, (3) U.S. production of articles that are like or directly competitive with those that are subject to investigation, and (4) U.S. consumers.

The Commission is therefore interested in receiving written submissions that address the aforementioned public interest factors in the context of this investigation.

If the Commission orders some form of remedy, the President has 60 days to approve or disapprove the Commission's action. During this period, the subject articles would be entitled to enter the United States under a bond, in an amount to be determined by the Commission and prescribed by the Secretary of the Treasury. The Commission is therefore interested in receiving submissions concerning the amount of the bond that should be imposed.

On May 6, 2002, the ALJ issued Order No. 24 granting in part complainants' September 13, 2001, motion for sanctions. Pursuant to rule 210.25(d) of the Commission's Rules of Practice and Procedure, 19 C.F.R. § 210.25(d), the Commission has specified below the schedule for the filing of any petitions appealing Order No. 24 and the responses thereto.

WRITTEN SUBMISSIONS: The parties to the investigation are requested to file written submissions on the issues under review. The submission should be concise and thoroughly referenced to the record in this investigation, including references to exhibits and testimony. Additionally, the parties to the investigation, interested government agencies, and any other interested persons are encouraged to file written submissions on the issues of remedy, the public interest, and bonding. Such submissions should address the ALJ's May 13, 2002, recommended determination on remedy and bonding. Complainant and the Commission investigative attorney are also requested to submit proposed remedial orders for the Commission's consideration. The written submissions and proposed remedial orders must be filed no later than the close of business on July 5, 2002. Reply submissions must be filed no later than the close of business on July 12, 2002. No further submissions will be permitted unless otherwise ordered by the Commission.

Any petitions appealing Order No. 24 must be filed no later than close of business on July 26, 2002. Reply submissions must be filed no later than the close of business on August 2, 2002.

Persons filing written submissions must file with the Office of the Secretary the original and 14 true copies thereof on or before the deadlines stated above. Any person desiring to submit a document (or portion thereof) to the Commission in confidence must request confidential treatment unless the information has already been granted such treatment during the proceedings. All such requests should be directed to the Secretary of the Commission and must include a full statement of the reasons why the Commission should grant such treatment. *See* 19 C.F.R § 201.6. Documents for which confidential treatment is granted by the Commission will be treated accordingly. All nonconfidential written submissions will be available for public inspection at the Office of the Secretary.

This action is taken under the authority of section 337 of the Tariff Act of 1930, as amended (19 U.S.C. § 1337), and in sections 210.25 and 210.42 - .45 of the Commission's Rules of Practice and Procedure (19 C.F.R. §§ 210.25, 210.42 - .45).

By order of the Commission.

Marilyn R. Abbott
Secretary

Issued: June 21, 2002

CERTAIN INTEGRATED CIRCUITS, PROCESSES FOR MAKING SAME, AND PRODUCTS CONTAINING SAME **337-TA-450**

CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the **NOTICE OF COMMISSION DECISION TO REVIEW PORTIONS OF AN INITIAL DETERMINATION FINDING NO VIOLATION OF SECTION 337 OF THE TARIFF ACT OF 1930,** was served upon the following parties via first class mail and air mail where necessary, on June 21, 2002.

Marilyn R. Abbott, Secretary
U.S. International Trade Commission
500 E Street, SW - Room 112
Washington, DC 20436

ON BEHALF OF COMPLAINANT UNITED MICROELECTRONICS CORPORATION, UMC GROUP AND UNITED FOUNDRY SERVICE, INCORPORATED:

Steven J. Routh, Esq.
Hogan and Hartson
555 13th Street, NW
Washington, DC 20004

William H. Wright, Esq.
Biltmore Tower
Hogan and Hartson
500 S. Grand Avenue
Suite 1900
Los Angeles, CA 90071

ON BEHALF OF SILICON INTEGRATED SYSTEMS CORPORATION:

Tom M. Schaumberg, Esq.
Adduci, Mastriani and Schaumberg, LLP
1200 Seventeenth Street, NW
Fifth Floor
Washington, DC 20036

Kirk R. Ruthenberg, Esq.
Sonnenschein Nath and Rosenthal
1301 K Street, NW
Suite 600, East Tower
Washington, DC 20005

Edward H. Rice, Esq.
Sonnenschein Nath and Rosenthal
8000 Sears Tower
Chicago, IL 60606

Michael A. Molano, Esq.

Sonnenschein Nath and Rosenthal
685 Market Street, 6th Floor
San Francisco, CA 94105

ON BEHALF OF THE COMMISSION:

Shival P. Virmani, Esq.
Commission Investigative Attorney
Office of Unfair Import Investigation
500 E Street, SW - Room 401-J
Washington, DC 20436

James B. Coughlan, Esq.
Commission Investigative Attorney
Office of Unfair Import Investigations
500 E Street, SW - Room 401-L
Washington, DC 20436

Timothy Monaghan, Esq.
Advisory Attorney
Office of General Counsel
500 E Street, SW - Room 707-U
Washington, DC 20436

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of

CERTAIN INTEGRATED CIRCUITS, PROCESSES FOR MAKING SAME, AND PRODUCTS CONTAINING SAME

Investigation No. 337-TA-450

INITIAL DETERMINATION
Administrative Law Judge Sidney Harris

Pursuant to the Notice of Investigation, 66 Fed. Reg. 13567 (2001), this is the Administrative Law Judge's Initial Determination in the Matter of Certain Integrated Circuits, Processes for Making Same, and Products Containing Same, United States International Trade Commission Investigation No. 337-TA-450. 19 C.F.R. § 210.42(a).

The Administrative Law Judge hereby determines that no violation of section 337 of the Tariff Act of 1930, as amended, has been found in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain integrated circuits or products containing same by reason of infringement of claims 1, 2 or 8 of U.S. Letters Patent 5,559,352, or claims 1, 3-16 or 19-21 of U.S. Letters Patent 6,117,345.

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I. BACKGROUND

A. Institution and Procedural History of This Investigation

On March 6, 2001, by publication of a Notice of Investigation in the *Federal Register*, this investigation was instituted, pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, to determine:

> [W]hether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain integrated circuits or products containing same by reason of infringement of claims 1, 2, or 8 of U.S. Letters Patent 5,559,352 or claims 1, 3-16, or 19-21 of U.S. Letters Patent 6,117,345, and whether an industry in the United States exists as required by subsection (a)(2) of section 337.

66 Fed. Reg. 13567 (2001).

The complainants are: United Microelectronics Corporation, No. 3, Li-Hsin Road 2, Science-Based Industrial Park, Hsinchu City, Taiwan ("UMC"); UMC Group (USA), 488 De Guigne Drive, Sunnyvale, CA 94086; and United Foundry Service, Inc., 1989 Route 52, Hopewell Junction, NY 12533 (collectively, "Complainants"). *Id.*

The Commission named as the respondents: Silicon Integrated Systems Corp., No. 16, Creation Road, Science-Based Industrial Park, Hsinchu City, Taiwan ("SiS-TW"); and Silicon Integrated Systems Corporation, 240 North Wolfe Road, Sunnyvale, CA 94086 ("SiS-US") (collectively, "SiS" or "Respondents."). *Id.*

Shival P. Virmani, Esq. of the Office of Unfair Import Investigations ("OUII") was designated as the Commission Investigative Attorney. *Id.*

On April 17, 2001, the Administrative Law Judge issued Order No. 3, setting a target date

of approximately 14 months for this investigation.

On November 7, 2001, a prehearing conference was held in this investigation. On that date, the hearing on the question of violation of section 337 commenced. The hearing was recessed on November 16, 2001, to be reconvened on December 10, 2001, for the primary purpose of receiving additional evidence pertaining to Respondents' new products. On December 10, 2001, the hearing reconvened. All testimony concluded and the hearing was adjourned on December 12, 2001.

On January 7, 2001, Order No. 16 extended the target date to 15 months.

On February 22, 2002, the Administrative Law Judge issued Order No. 17, an initial determination extending the target date for completion of this investigation to September 6, 2002. On March 13, 2002, the Commission issued its Notice of a Commission Determination Not to Review an Initial Determination Extending the Target Date for Completion of the Investigation.

All parties have submitted main and reply briefs, as well as proposed findings, with respect to the November portion of the hearing, and also separate briefs and findings with respect to the December portion of the hearing.[1] The issues are now ripe for determination.

The following abbreviations may be used in this Initial Determination:

ALJ - Administrative Law Judge

ALJX - Administrative Law Judge Exhibit

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[1] On December 21, 2001, Complainants filed their Motion for Leave to File Errata Pages for Post-Hearing Brief for Hearing Completed November 16. Motion Docket No. 450-25. Attached to the Motion are replacement pages for pages ii and 21 of Complainants' main post-hearing brief. The replacement pages correct non-substantive typographical errors. Motion No. 450-25 is GRANTED.

CX - Complainants' Exhibit

CPX - Complainants' Physical Exhibit

Dep. - Deposition

EDIS - Electronic Document Imaging System

FF - Finding(s) of Fact

JX - Joint Exhibit

PCL - Proposed Conclusion of Law (CPCL, RPCL or SPCL)

PFF - Proposed FF (CPFF, RPFF or SPFF)

PRF - Proposed Reply or Rebuttal Finding (CPRF, RPRF or SPRF)

RPX - Respondents' Physical Exhibit

RX - Respondents' Exhibit

SX - Commission Investigative Staff (OUII) Exhibit

Tr. - Transcript.

B. The Products at Issue

The products at issue are integrated circuits that are made in Taiwan by SiS-TW. SiS-TW chipsets containing integrated circuits have been sent by SiS-TW to SiS-US. Issues have been raised in this investigation as to whether accused SiS integrated circuits contain an electrostatic discharge ("ESD") protection device covered by the asserted claims of the '352 patent, whether accused SiS integrated circuits are made by a method covered by the asserted claims of the '345 patent, and whether these patents are valid. All parties recognize that certain SiS products have been modified over time, and that there may be old, current or newly designed

generations or versions of various SiS products that have the same or similar product designations or codes. There are disputes as to whether certain SiS devices now infringe or ever infringed the asserted patent claims. There are disputes concerning the substance and materiality of modifications to SiS devices, and whether certain avoid infringement.

II. IMPORTATION OR SALE

On November 2, 2001, the Administrative Law Judge issued Order No. 15, which consisted of an initial determination granting Complainants' motion for summary determination on the importation issue, and an order denying Respondents' motion for summary determination of lack of importation. On December 3 and 5, 2001, the Commission issued notices to the effect that it would not review the initial determination contained in Order No. 15, thus making that determination the determination of the Commission. *See* 66 Fed. Reg. 64061; 66 Fed. Reg 63409. Consequently, the importation or sale requirement of section 337 has been established for purposes of this Initial Determination.

III. INFRINGEMENT OF THE '352 PATENT

A finding as to infringement or non-infringement requires a two-step analytical approach. First, the claims of the patent must be construed as a matter of law to determine their proper scope. Second, a factual determination must be made as to whether the properly construed claims read on the accused device. *See Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976, 979 (Fed. Cir.1995)(*en banc*), *aff'd*, 517 U.S. 370 (1996).

A. Claim Construction

1. The General Law Pertaining to the Interpretation of Patent Claims

To construe a claim, one first looks to the claim language. *Pitney Bowes, Inc. v.*

Hewlett-Packard Co., 182 F.3d 1298, 1305 (Fed. Cir.1999)("The starting point for any claim construction must be the claims themselves."); *Comark Communications, Inc. v. Harris Corp.*, 156 F.3d 1182, 1186 (Fed. Cir.1998) ("The appropriate starting point ... is always the language of the asserted claim itself."). Then, one looks to the other intrinsic evidence, beginning with the specification and concluding with the prosecution history, if in evidence. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996); *Markman*, 52 F.3d at 979 ("Claims must be read in view of the specification, of which they are a part.").

If the claim language is clear on its face, then a court's consideration of other intrinsic evidence is restricted to determining if a deviation from the clear language of the claims is specified. *Interactive Gift Express, Inc. v. Compuserve Inc.*, 231 F.3d 859, 865 (Fed. Cir. 2000). A deviation may be necessary if, for example, "a patentee [has chosen] to be his own lexicographer and use[s] terms in a manner other than their ordinary meaning." *Id.* (quoting *Vitronics*, 90 F.3d at 1582). Any such special definition given to a word must be clearly defined in the specification. *Markman*, 52 F.3d at 980. A deviation may also be necessary if a patentee has "relinquished [a] potential claim construction in an amendment to the claim or in an argument to overcome or distinguish a reference." *Interactive Gift Express*, 231 F.3d at 865 (quoting *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 979 (Fed. Cir. 1999).

If the claim language is not clear on its face, then a court's consideration of the remaining intrinsic evidence is directed to resolving, if possible, the lack of clarity. *Interactive Gift Express*, 231 F.3d at 865.

In looking to the specification to construe claim terms, care must be taken to avoid reading "limitations appearing in the specification . . . into [the] claims." *Intervet Am., Inc. v.*

Kee-Vet Lab., Inc., 887 F.2d 1050, 1053 (Fed. Cir.1989). Examples or embodiments appearing in the written description may not be read into a claim. One looks "to the specification to ascertain the meaning of the claim term as it is used by the inventor in the context of the entirety of his invention," and not merely to limit a claim term. *Comark*, 156 F.3d at 1186-87.

If the meaning of the claim limitation is apparent from the totality of the intrinsic evidence, then the claim has been construed. If, however, a claim limitation remains unclear, one may look to extrinsic evidence to help resolve the lack of clarity.[2] Relying on extrinsic evidence to construe a claim is "proper only when the claim language remains genuinely ambiguous after consideration of the intrinsic evidence." *Bell & Howell Document Mgmt. Prods. Co. v. Altek Sys.*, 132 F.3d 701, 706 (Fed. Cir.1997); *Vitronics*, 90 F.3d at 1583-85 ("Such instances will rarely, if ever, occur."). Extrinsic evidence may always be consulted, however, to assist in understanding the underlying technology. *See Pitney Bowes*, 182 F.3d at 1309 ("[C]onsultation of extrinsic evidence is particularly appropriate to ensure that [a judge's] understanding of the technical aspects of the patent is not entirely at variance with the understanding of one skilled in the art."); *Vitronics*, 90 F.3d at 1585 ("Had the district court relied on the expert testimony and other extrinsic evidence solely to help it understand the underlying technology, we could not say the district court was in error."). Extrinsic evidence may never be used "for the purpose of varying or contradicting the terms in the claims." *Markman*, 52 F.3d at 981.

As stated in the in the *Markman*, opinion, "the focus in construing disputed terms in

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[2] Dictionaries are a form of extrinsic evidence with a special place in claim construction, and may sometimes be considered along with the intrinsic evidence. *See Vitronics*, 90 F.3d at 1584 n.6 (stating that, although technically the court is free to consult dictionaries at any time to help determine the meaning of claim terms, it may do so "so long as the dictionary definition does not contradict any definition found in or ascertained by a reading of the patent documents").

claim language is not the subjective intent of the parties to the patent contract when they used a particular term. Rather the focus is on the objective test of what one of ordinary skill in the art at the time of the invention would have understood the term to mean." 52 F.3d at 968. *Accord Hoechst Celanese Corp. v. BP Chems. Ltd.*, 78 F.3d 1575, 1578 (Fed. Cir.1996)(The court assigns a claim term the meaning that it would be given by persons experienced in the field of the invention.).

2. Interpretation of the Claims at Issue

As explained in the specification of the '352 patent (entitled "ESD Protection Improvement"), the claimed "invention relates to the manufacture of highly dense integrated circuits, and more particularly to input protection devices to protect attached integrated circuits from damage due to electrostatic discharge." CX-2/RX-1 ('352 Patent), col. 1, lines 16-19. As further explained by the specification:

> During handling and operation of integrated circuit devices using Field Effect Transistor (FET)[3] technology, large electrostatic charges can be transferred from external contacts of the integrated circuit into

---

[3] A field effect transistor, or "FET," is a transistor with a source, a gate and a drain. Mr. Peltzer succinctly defined an FET during the hearing, as follows:

> Q What is a field effect transistor?
>
> A Well, a field effect transistor is a typical MOS, that is a metal oxide silicon transistor, or FET, field effect transistor, and contains three essential elements: A source, a gate and a drain.
>
> We have an addition to the structure as the technology has advanced, that in the source region and the drain regions, typically nowadays we have what's called a lightly doped drain, which I explained in the tutorial is a small region of higher resistivity which slows down electrons to keep them from sticking in the oxide under the gate. But the principal components are a source and a gate and a drain.

Peltzer Tr. 707.

> the interior of the circuit, causing damage and/or destruction to FET devices within. In order to prevent such damage, workers in the field have added input protection devices which are typically located between the external contacts and the FET devices. These protection devices are designed to provide a path to safely discharge the electrostatic charge and prevent damage to the internal FET devices.

Id. col. 1, lines 21-31.

The '352 patent specification provides some description of the related art, and states that the principal object of the claimed invention, which is described in the patent as an improvement to ESD protection technology, is "to provide a method for forming an ESD protection device with a reduced junction breakdown voltage which improves the ESD characteristics of the protection device." *Id.* at col. 1, line 1, and lines 51-54.

Based on the allegations contained in the complaint, the notice of investigation covers allegations that Respondents infringe claims 1, 2 or 8 of the '352 patent. In their post-hearing filings, Complainants asserted each of those claims against Respondents. *See* Complainants' Proposed Conclusions of Law for Hearing Completed November 16, 2001 at 14. The asserted claims of the '352 patent are as follows:

> **1.** An ESD protection device with reduced junction breakdown voltage, connected to an integrated circuit which includes FET devices, comprising:
>
> a silicon substrate having a first conductivity type;
>
> field oxide regions in and on said silicon substrate for isolation of said ESD protection device;
>
> a gate with adjacent spacers for said ESD protection device, between said field oxide regions;
>
> source/drain regions for said ESD protection device between said gate and said field oxide regions, with each source/drain region

comprising:

a first lightly implanted region having a second conductivity type opposite to said first conductivity type, under one of said spacers;

a heavier implanted region of the same conductivity type as said first lightly implanted region, located between said first lightly implanted region and one of said field oxide regions;

a second lightly implanted region of same conductivity type as said silicon substrate, centered under said heavier implanted region.

2. The ESD protection device of claim **1** wherein said first conductivity type is P-type, and said second conductivity type is N-type.

8. An ESD protection circuit, having first and second ESD protection devices, connected to an integrated circuit which includes FET devices, and connected to an input/output pad, comprising:

a silicon substrate having a first conductivity type;

field oxide regions in and on said silicon substrate for isolation of said ESD protection devices;

gates with adjacent spacers for each of said ESD protection devices, between said field oxide regions;

source/drain regions for said ESD protection devices between said gates and said field oxide regions, with each source/drain region comprising:

a first lightly implanted region having a second conductivity type opposite to said first conductivity type, under one of said spacers;

a heavier implanted region of the same conductivity type as said first lightly implanted region, located

between said first lightly implanted region and one of said field oxide regions;

a second lightly implanted region of same conductivity type as said silicon substrate, centered under said heavier implanted region;

a first electrical connection between said input/output pad, said drain regions of said first and second ESD protection devices, and said integrated circuit;

a second electrical connection to ground of said gates of said first and second ESD protection devices, and said source region of said second ESD protection device; and

a third electrical connection, to a voltage source, of said source of said first ESD protection device.

CX-2/RX-1 ('352 Patent).

In order to interpret these claims, as discussed in the legal discussion in this section, one must construe the patent claims as one of ordinary skill in the art at the time of the invention. Thus, the first step in construing the claims of the '352 patent will be to determine the level of ordinary skill in the art. There is no dispute that the relevant art pertains to ESD protection devices, and that the hypothetical person of ordinary skill might have an educational background in a technical discipline such as electrical engineering, physics – or as proposed by Respondents, even chemical engineering or metallurgy.

A dispute has arisen, however, as to the level of education one of ordinary skill would have, and the level of experience that one would have obtained. Based upon the testimony of their expert, Mr. Peltzer, Respondents argue that a person of ordinary skill in the art relating to the '352 patent is one who has a bachelor of science degree or a master of science degree in electrical engineering, physics, chemical engineering or metallurgy. *See* RPFF 12 (citing Peltzer

Tr. 707). Complainants specifically state their disagreement with Respondents' argument, and based upon the testimony of their expert, Dr. Fair, Complainants argue that one of ordinary skill in the art of ESD protection devices would have an advanced degree such as a master's degree in electrical engineering or physics, along with substantial experience in integrated circuit design and device design. It is argued that this level of skill is required because of the very complex nature of the subject matter involved in the '352 patent.[4] *See* CRF 12 (citing Fair Tr. 139).

Complainants' proposal, which requires a person to have more education and to have substantial experience, is closer to the mark than Respondents' proposal. An examination of the transcript portion relied upon by Respondents shows that Mr. Peltzer testified that one of ordinary skill would have a bachelor's of science or a master's of science in a technical field, and also "approximately two years of experience in the field." Peltzer Tr. 707. Furthermore, the overall testimony received in this investigation relating to the '352 patent demonstrated that the patent is directed to persons with advanced education, who are experienced in relevant technical fields, and who are responsible for making important design or manufacturing choices in the production of integrated circuits. Consequently, it has been demonstrated that one of ordinary skill in the art would have an advanced degree such as a master's degree (or equivalent education

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[4] Dr. Fair testified on the question of ordinary skill, as follows:

> Q Turning to the '352 patent now, Doctor, what would one of ordinary skill in the art in the practice of the '352 patent have in the way of professional education and training?
>
> A It would be my experience that an advanced degree such as a master's degree in electrical engineering or physics would be required. This is a very complex subject. With also substantial experience in integrated circuit design and device design.

Fair Tr. 139.

or experience), in a field relevant to ESD technology, such as electrical engineering or physics, and further, such a person would have substantial experience in integrated circuit and device design.

With respect to the specific terms of the '352 patent claims that must be construed as one skilled in the art, the parties have made various proposals and arguments. There is no dispute that these claims pertain to a device, as described in the specification, which is designed to protect a circuit from damage due to electrostatic discharge, i.e., ESD. However, disputes have arisen as to the precise meaning of numerous terms used in the asserted claims. To present their divergent claim constructions in the briefs, the parties have divided the language used in the asserted claims differently. Certain terms and concepts are clearly central to the issues presented in the parties' briefs and in this investigation generally, although there is substantial overlap among the terms and phrases isolated by the parties.

Complainants cite proposed findings of fact and conclusions of law with respect to 16 specific terms or phrases found in the '352 patent claims. They argue that "[m]ost of the differences in the parties' claim constructions arise out of Respondents' effort to construe the claims of the '352 patent as if an ESD protection device were limited to the structure of a single MOS transistor, whereas Complainants construe the term in the '352 patent as being applicable to an ESD protection device which consists of one or more transistors." Within that framework, Complainants' main post-hearing brief focuses specifically on the terms "gate," "gate with adjacent spacers" and "source/drain regions." *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 13-16.

Respondents, in their main post-hearing brief, cite to proposed findings with respect to 17

terms or phrases, including "gate with adjacent spacers" (as the first item). They also brief the meanings of the terms "source/drain regions" and "voltage source." *See* Respondents' Post-Hearing Brief (Following the November Hearing) at 8-12.

The Commission Investigative Staff briefs the terms: (1) "a gate . . ." (as used in claim 1) and "gates with adjacent spacers" (as used in claim 8); (2) "source/drain regions and "each source/drain region comprising" (as used in claims 1 and 8); (3) "first and second ESD protection devices" (as used in claim 8); and (4) "voltage source" (which is found in claim 8). *See* OUII Post-Hearing Brief (Following the November Hearing) at 5-10.

Although the terms source, drain and gate -- and even voltage -- are common terms in transistor technology, much of the conflicts in the parties' proposed claim constructions center around these terms, as well as basic questions about how the claimed invention may be configured. The categories used by the Commission Investigative Staff in its main post-hearing brief provide a sufficient framework for addressing these questions, and is used in the claim construction discussion that follows.[5]

"a gate . . ." (as used in claim 1) and "gates with adjacent spacers" (as used in claim 8)

Complainants' proposed claim construction does not equate the "gate" of a claimed ESD protection device with the "gate" of a transistor. Complainants argue that neither independent claim 1 nor independent claim 8 recites the presence of a single MOS transistor, nor is there any reason to read such a limitation into the claims based on a preferred embodiment. Rather, it is argued, those of ordinary skill in the art appreciate that an ESD protection device often is

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[5] Any specific questions of claim meaning that remain may be addressed with respect to specific infringement or noninfringement arguments made by the parties (as indeed some of the parties' briefing on infringement questions touches upon examples of claim interpretation).

configured as a collection of multiple transistors connected in parallel, which act as one transistor. Thus, Complainants argue that the term "gate" means a collection of gate electrodes that are electrically coupled together to control the current of the transistors which make up the ESD protection device. It is argued that similarly "gate with adjacent spacers" means that the adjacent spacers are all of the spacers along the edges of the gate electrodes that collectively make up the "gate" of an ESD protection device. *See, e.g.*, Complainants' Post-Hearing Brief (Following the November Hearing) at 14-15.

In contrast to Complainants' proposal, Respondents argue that "a gate with adjacent spacers" means a single, particular gate which forms in part a gate electrode for a field effect transistor in the claimed ESD protection device. *See, e.g.*, Respondents' Post-Hearing Brief (Following the November Hearing) at 8.

The Commission Investigative Staff also argues that "a gate" refers to the gate of a single, particular and specific FET. However, the Staff does not argue that claim 1, which contains an element directed toward "a gate with adjacent spacers for said ESD protection device" covers only devices with one FET and thus one gate. *See* OUII Post-Hearing Brief (Following the November Hearing) at 5-6.

As the Commission Investigative Staff points out, ESD protection devices may contain several FETs, and claim 1 uses the term "a gate" following the term of art, "comprising," and thus may mean one or more gates. In order to resolve any ambiguity, it is proper to examine the entire specification and prosecution history. *Id.* at 5 (citing *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2001)).

The file history of the '352 patent shows that the applicants, through their attorney,

amended original divisional application claim 7 to replace "*gates* with adjacent spacers for said ESD protection device," with the language "*a gate* with adjacent spacers for said ESD protection device" *See* CX-4 (Preliminary Amendment, Application Paper No. 2)(emphasis added). In the Remark to the Amendment, the applicants stated: "Please enter the above Preliminary Amendment to the Divisional Patent Application that is enclosed. The amended claims are believed to clarify the invention and put the application in condition for allowance." CX-4 (Preliminary Amendment, Application Paper No. 2).

By this amendment, the applicants did not disclaim an ESD protection device with multiple FETs, in which there would be multiple gates associated with these FETs. Nevertheless, the applicants have clearly disclaimed a claim construction that equates "a gate" with what may be multiple gates of an ESD protection device's FETs.

Indeed, as enabled by the '352 patent specification, the language "a gate" and "gates with adjacent spacers" both refer to a single, particular gate for a specific transistor, with each single, particular gate having a spacer on the left and the right-hand sides of the gate. *See* CX-2 ('352 Patent), col. 2, lines 10-11, 20-27, 54-56, Figs. 3, 7; Peltzer Tr. 710, 719-720. A gate interconnect does not mean a collection of gate electrodes, as argued by Complainants.[6]

Consequently, "a gate" must be associated with a specific FET. Furthermore, due to the applicants' amendment, there is no range of equivalents for "a gate" beyond the literal meaning, inasmuch as the term "a gate" represents claim language that was amended and narrowed (to require that "each source/drain region" includes, *inter alia*, a second lightly implanted region) for

[6] As Mr. Peltzer, Respondents' expert witness testified, a gate interconnect attaches plural gates together and is, therefore, not part of the gate. *See* Peltzer Tr. 780.

reasons of patentability. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co., Ltd.*, 234 F.3d 558, 574 (Fed. Cir. 2000), *cert. granted*, -- U.S. -- 121 S.Ct. 2519, 150 L.Ed.2d 692 (2001).[7]

With regard to the word "gates" in claim 8, this limitation must be construed as two or more gates in which each of the gates has a field oxide region on each side. Such a construction

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[7] A review of the '352 patent prosecution history shows that as a Preliminary Amendment, the action taken by the applicants in amending application claim 7 (claim 1, as issued) might be characterized as voluntary or largely unexplained (even though the Remarks, discussed, *infra*, explain that in general the amendment was for the purposes of clarification and patentability). Nevertheless, the amendment serves to inform those who seek the metes and bounds of the claimed invention that the applicants superseded, or gave up, the "gates" language in the claim in favor of the term "gate."

In the *Festo* case, the Court of Appeals for the Federal Circuit outlined a series of question to be resolved *en banc*. The answers to those questions clearly indicate that any amendment for the purposes of patentability, including the Preliminary Amendment in question in this investigation, would foreclosure application of the doctrine of equivalents with respect to claim language that was the subject of the amendment. The Federal Circuit held in part:

> We begin with a brief synopsis of our answers to the en banc questions and a summary of how those answers affect the disposition of this appeal. In response to En Banc Question 1, we hold that "a substantial reason related to patentability" is not limited to overcoming prior art, but includes other reasons related to the statutory requirements for a patent. Therefore, *an amendment that narrows the scope of a claim for any reason related to the statutory requirements for a patent will give rise to prosecution history estoppel with respect to the amended claim element.* In response to En Banc Question 2, *we hold that "voluntary" claim amendments are treated the same as other claim amendments; therefore, any voluntary amendment that narrows the scope of a claim for a reason related to the statutory requirements for a patent will give rise to prosecution history estoppel with respect to the amended claim element.* In response to En Banc Question 3, we hold that when a claim amendment creates prosecution history estoppel, no range of equivalents is available for the amended claim element. In response to En Banc Question 4, *we hold that "unexplained" amendments are not entitled to any range of equivalents*. We do not reach En Banc Question 5, for reasons which will become clear in our discussion of the specific case before us.

234 F.3d at 564-64 (footnote omitted concerning the use of the term "element" in the *en banc* questions to mean limitation expressed in claim language)(emphasis added).

is consistent with the teachings of the '352 specification, which shows that the devices at issue are symmetrically fabricated. *See* CX-2, col. 2, lines 43-46, Fig. 1. In the embodiment depicted in Figure 1, oxide regions (item 16) are formed on each side of the gate. *Id.*, col. 2, lines 46-49, Fig. 1.

"source/drain regions" and "each source/drain region comprising" (as used in claims 1 and 8)

Complainants argue that "source/drain regions" is a broad term, as demonstrated by its use in the specification of the '352 patent, and by the term's use in U.S. Patent No. 5,142,345 to Kazuaki Miyata, cited in the background of the '352 patent.

With respect to their use of the Miyata patent in their proposed claim construction, Complainants cite *Arthur A. Collins, Inc. v. Northern Telecom Ltd.*, 216 F.3d 1042 (Fed. Cir. 2000), in which the Federal Circuit stated: "When prior art that sheds light on the meaning of a term is cited by the patentee, it can have particular value as a guide to the proper construction of the term, because it may indicate not only the meaning of the term to persons skilled in the art, but also that the patentee intended to adopt that meaning."). It is argued that the Miyata patent is cited in the '352 patent specification, and thus shows that Miyata's allegedly broad use of the term "source/drain region" was adopted by the '352 patentee. In particular, Complainants argue that the Miyata patent uses the term "source/drain region" to refer to the source region, or the drain region, or to the combination of both the source and the drain region, of a transistor. Complainants' Post-Hearing Brief (Following the November Hearing) at 15-16.

Complainants argue further that inasmuch as an ESD protection device can contain more than one transistor, the "source/drain regions" of an ESD protection device refers to the source

regions or the drain regions, or the combination of both source and drain regions collectively, of all of the transistors that comprise the ESD protection device. It is argued that use of the plural "source/drain regions" requires only that, among all of the transistors that comprise the ESD protection device, the implants specified in the 5th, 6th and 7th elements of claim 1 be found in two or more source regions or drain regions, or the combination of source and drain regions collectively, in these transistors. *See Id.* at 16.

Respondents argue that inasmuch as the phrase "source/drain regions" in claim 1 must be construed consistently with the phrase in claim 8 and because in claim 8 the phrase "source/drain regions" must include a "source region" and a "drain region" for each ESD, claim 1 requires that the particular gate have both a "source region" *and* a "drain region" and further that each of the regions has the "second lightly implanted region of same conductivity type as said silicon substrate" (e.g., the PESD implant). Respondents' Post-Hearing Brief (Following the November Hearing) at 11-12. Respondents argue that the description of the prior art in the '352 patent is at best ambiguous on the source/drain question. With particular reference to the Miyata patent, it is argued that the Miyata patent is extrinsic evidence and should be ignored unless the term "source/drain" were somehow found to be indefinite. *Id.* at 12.

The Commission Investigative Staff argues that the intrinsic evidence requires "source/drain regions" be construed to cover both sides of an individual FET's gate. It is argued that as such, "source/drain regions" refers to the source region on one side of the gate and also to the drain region on the other side of that gate, with the term "source/drain regions" (a plural term) thus referring to the source and drain regions associated with a single FET's gate. OUII Post-Hearing Brief (Following the November Hearing) at 7-8.

There are ambiguities in the plain claim language. However, the Commission Investigative Staff's proposed construction is supported by the prosecution history. In a Preliminary Amendment, original divisional application claim 7 (issued as claim 1) was amended, in pertinent part, as shown:

> source/drain regions for said ESD protection device between said gate and said field oxide regions, with each source/drain region comprising:

CX-4 (Preliminary Amendment, Application Paper No. 2)(added claim language underlined in original).

By amendment, the term "each" was added to claim 1 to require that every source and *every* drain region of each FET that makes up the '352 protection device have a (1) "first lightly implanted region," (2) "a heavier implanted region," and (3) "a second lightly implanted region." CX-2, col. 5, lines 19-29 (claim 1). Indeed, the claim provides "source /drain regions" in the plural. The three implants at col. 5, lines 19-29, are for each and every source/drain region of each and every transistor that is included in the '352 protection device.

Claim 1 should not be construed to be limited to an ESD protection circuit with a single FET. Rather, claim 1 describes the characteristics of each and every FET of a single protection device in which each and every one of these FETs' source and drain regions has the three implants disclosed in the claims. The applicants' Amendment during prosecution of the '352 patent merely allowed claim 1 to cover two types of protection devices, those with a single FET and those with multiple FETs. However, each of these FETs' source and drain regions have identical implants associated with the source and drain, and the language of the Amendment does convey a different meaning. Therefore, this Preliminary Amendment (regardless of whether it is

best described as a broadening or a narrowing of the claim language) does not support Complainants' argument that "source/drain regions" refers to different regions of different FETs (*e.g.*, the source region of one FET and the drain region of another). There is nothing in the '352 specification to support such a construction.

Indeed, according to Complainants, the "source/drain regions" limitation "collectively" refers to the source/drain regions of a protection device that consist of multiple transistors. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 15-16. By using the term "collectively" in its interpretation of "source/drain regions," Complainants attempt to read this limitation to cover the source from one transistor of the ESD protection device and drain from another transistor of the ESD protection device. Alternatively, Complainants would have this limitation cover a pair of sources or a pair of drains, wherein each one of these source or drain pairs may be from different transistors.

Neither the intrinsic nor the extrinsic evidence supports Complainants' proposed claim construction. As explained by the Commission Investigative Staff in its proposed findings of fact for the November hearing (*see* SPFF 26-48), several processing steps are taken to manufacture an ESD protection device covered by the '352 patent and the FETs protected by that device. CX-2, col. 1, line 50 to col. 2, line 29; item 10 in Fig. 6; item 12 in Fig. 6 .[8] According to the patent, these processing steps are performed on each side of the gate and, therefore, produce source and drain regions with symmetrical implants.

First, the ESD protection device (item 10) and the internal FET device (*i.e.*, the circuit

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[8] Figures 1-7 illustrate a total of two FETs, items 10 and 12. CX-2 ('353 Patent), col. 2, lines 40-43. Item 10 is the ESD protection device and item 12 is the circuit or device being protected. *Id.*

being protected (item 12)) "are formed at the same time on a single P-substrate (item 14)." CX-2 ('352 Patent), col. 2, lines 43-46, Fig. 1.[9] Next, after the gate (20) is formed (CX-2, col. 2, lines 46-56, Fig. 1), N– material is implanted on each side of the gate (i.e., the first ion implant). This implant forms the source and drain regions for both the protection device (item 10) and the internal FET device (item 12). CX-2, col. 2, lines 57-62, Fig. 2. Then, an insulating layer of SiO_2 (silicon dioxide), which is initially deposited over the entire substrate surface. (CX-2, col. 2, lines 63-67), is later etched away to form two sets of spacers (items 24): one set for the ESD protection device and another set for the FET device being protected. CX-2, col. 2, line 63 to col. 3, line 2, Fig. 3. Afterward, a heavy ion implant is performed with respect to both the ESD protection device and the device being protected (i.e., there is a heavy ion implant on each side of the gate for the ESD protection device and each side of the gate for the device being protected). CX-2, col. 3, lines 3-7, Fig. 4. Subsequently, the SiO_2 insulating layer (item 30), which was previously formed over the entire structure (CX-2, col. 2, lines 63-67; col. 3, lines 12-15, Fig. 5), is etched on both sides of the gate for only the ESD protection device. CX-2, col. 3, lines 15-20. As a result, contact openings (item 32) are formed above each source and each drain region (items 28) of the protection device (item 10), but not above the source and drain regions of the device being protected (item 12). CX-2, col. 3, lines 18-21, Fig. 5. Next, a photoresist (item 34) masks only the openings (item 32) of the FET device (item 12) being protected (CX-2, col. 3, lines 23-25, Fig. 6), but not the openings above the ESD protection device, and a light ion implant of opposite conductivity (P-) is performed (items 36). CX-2, col. 3, lines 22-27, Fig. 6.

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[9] "P-substrate" refers to conductivity-type of the substrate. *See, e.g.*, CX-2 ('352 Patent), claims 1 and 2.

Nothing in the '352 patent provides that any of the ESD protection device's contact openings are masked. All of the ESD devices' sources and drains receive a "light implant." There is no intrinsic (or extrinsic) evidence that indicates that only certain of the protection device's openings receive an implant, whereas others do not -- the photoresist (item 34 in Fig. 6) is not applied in such a manner. The symmetrical fabrication process makes it clear that the source and drain region of each the ESD protection device's transistors have "a second lightly implanted region."

According to Complainants, however, the '352 patent only requires that some of the ESD protection device's transistors' have sources with a second lightly implanted region, whereas the drains do not have such an implant; or, alternatively, some of the transistors have drains with a second lightly implanted region, whereas the sources do not have such an implant. In other words, Complainants assert that so long as the ESD protection device contains at least two "lightly implanted regions," regardless of whether or not they are associated with the same gate, the "source/drain regions" limitations of claims 1 and 8 are met. Complainants' Post-Hearing Brief (Following the November Hearing) at 16 ("[t]he use of [this limitation] only requires that, among all of the transistors that comprise the ESD protection device, the implants specified in the 5th, 6th and 7th elements of claim 1 be found in two or more source regions or drain regions, or the combination of source and drain regions collectively, in these transistors.").

Complainants' proposed claim construction cannot be accepted. With regard to the intrinsic evidence, if Complainants' proposed claim construction were correct, one would expect the '352 patent to contain a teaching or embodiment in which the insulating layer (item 30) is formed over (1) some -- but not all -- of the source regions of the device being protected, or (2)

some -- but not all -- of the drain regions of the device being protected. CX-2 ('352 Patent), col. 3, lines 12-20, Fig. 5. That such a teaching is not present within the '352 patent is reflected in the hearing testimony of Complainants' expert witness:

> Q Can you show me where in the patent it -- one would understand that one of ordinary skill could block the opening 32 [with photoresist] on just one side of the gate but not the other?
>
> A I don't think there's any specific teaching in the patent for that to happen.
>
> * * *
>
> Q But you can't find any embodiment whatsoever in the '352 patent that says one of these openings can be blocked; isn't that correct?
>
> A I believe that would be correct. There's no specific teaching.

Fair Tr. 356-357.

In summary, the intrinsic and extrinsic evidence require a claim construction in which the term "source/drain regions" refers to: (1) each and every source of each and every transistor for the ESD protection device, and (2) each and every drain of each and every transistor for the ESD protection device. As such, the '352 patent claims must be construed to require that all of the sources and all of the drains of the ESD protection devices' transistors have "a lightly implanted region."

"first and second ESD protection devices" (as used in claim 8)

Claim 8 pertains to "[a]n ESD protection circuit, having first and second ESD protection devices, connected to an integrated circuit which includes FET devices . . . " comprising, among other things, "source/drain regions for said ESD protection devices between said gates and said field oxide regions . . . ."

Complainants argue that the argument they made regarding claim 1 applies with greater force to claim 8 because in claim 8 source/drain region is referred to in the plural. *See, e.g.*, CPCL 37-40; CPFF 416-417.

Respondents proposed construction of claim 8 is also consistent with its construction of claim 1. In general, it is argued that the phrase "source/drain regions" in claim 8 must include a "source region" and a "drain region" for each ESD. Furthermore, Respondents argue that if claim 8 were construed to require multiple gates for each ESD device, the Patent Examiner would have rejected the application as not illustrating the claimed invention and would have rejected claim 8 as not supported by the specification (pursuant to M.P.E.P. § 706.03(c)) because such an arrangement is not illustrated in the '352 patent nor is there any support in the specification for such an arrangement. *See* Respondents' Post-Hearing Brief (Following the November Hearing) at 10-11.

The Commission Investigative Staff also argues that claim 8 must be construed in a manner that is consistent with the construction of claim 1. Thus, the Staff argues that inasmuch as the terms "each" and "source/drain regions" are present in both claim 1 and claim 8 the phrase in claim 8's preamble, "first and second ESD protection devices," should be construed to mean that the devices have four implants (i.e., two sources and two drains). *See* OUII Post-Hearing Brief (Following the November Hearing) at 9-10.

Claim 8 was not amended. Rather, it was added in the Preliminary Amendment which changed the wording of claim 1. Accordingly, there are differences as well as obvious symmetries between claim 1 and claim 8. It is agreed by all parties that the claim terms were used in a generally consistent manner among the claims of the '352 patent, albeit claim 1 is

directed toward "[a]n ESD protection device," claim 8 is expanded to cover "an ESD protection circuit, having first and second ESD protection devices." The only consistent and logical reading of the terms of claim 8, as acknowledged by the parties, in view of the proper construction of claim 1, discussed above, is that "first and second ESD protection devices," should be construed to mean that these devices have four implants (i.e., two sources and two drains), and that each ESD protection device has one source and one drain.

"voltage source"

Complainants argue that the term "voltage source" (which is found in claim 8 of the '352 patent) is not defined in the '352 patent or its file history, nor is it a commonly used term. Complainants rely on the *Electronic Engineers' Handbook,* which defines voltage source as "a low impedance point within the circuit which can serve as an internal voltage supply." (CX-746C, tab 2 at p. 8-47), and on *Network Analysis*, which states that "if in some manner the terminal voltage is made equal to zero, the source behaves as a short circuit" (*Id.* at tab 3, p. 27), to argue that a voltage source may achieve ground potential. Complainants further argue that a voltage source may source or sink current while maintaining its terminal voltage, and thus, that the voltage source can be grounded and still constitute a "voltage source" as that term is used in claim 8. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 14; CPCL 41(citing CPFF 419-422).

By contrast, Respondents argue that the term "voltage source" used in claim 8 means the supply voltage to the integrated circuit (conventionally referred to as "V_{cc}"). It is argued that although Complainants attempt somehow find a way to construe "voltage source" to mean connected to "ground" in order to read claim 8 on the accused devices, the term "voltage source"

means a source of energy, which cannot be ground. *See* Respondents' Post-Hearing Brief (Following the November Hearing) at 11-12.

The Commission Investigative Staff, argues that "voltage source" should be construed as the operating voltage of the circuits shown in Figures 8 and 9 of the '352 patent. *See* OUII Post-Hearing Brief at 10 (citing Peltzer Tr. 765-767).

Complainants' proposed claim construction must be rejected in favor of that proposed by Respondents and the Commission Investigative Staff. The Staff's reference to the example provided by the specification of the '352 patent is illustrative of the term's meaning. Furthermore, the extrinsic evidence provided by Respondents' expert was persuasive in that equating a voltage source with ground would be unreasonable and disfavored by an engineer of ordinary skill.[10] *See* Peltzer Tr. 767-778.[11] Accordingly, the term "voltage source" is construed

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[10] On the subject of voltage source, Mr. Peltzer testified in part, as follows:

BY MR. HOVANEC:

Q Now, Mr. Peltzer, you heard Dr. Fair testify that an equivalent circuit to that shown in figure 8 is a circuit having VCC connected to ground. Do you have any opinion about that statement by Dr. Fair?

Well, that's very strained. If VCC is connected to ground, VCC, if it were for example a battery, the VCC would short to ground and you would drain the battery, or certainly have a lot of current between the VCC and ground, the voltage supply and ground.

Q In a desktop computer, if VCC were connected to ground, what would happen?

A Parts of it would melt, the battery would drain. It would be very awkward.

Q Would any reasonable engineer ever connect VCC to ground?

(continued...)

to refer to a source of energy or, more specifically, an operating voltage. "Voltage source" cannot be construed to mean "ground" or "connected to ground."

B. Infringement Determination

Literal infringement of a claim occurs when every limitation recited in the claim appears in the accused device, i.e., when "the properly construed claim reads on the accused device exactly." *Amhil Enters., Ltd. v. Wawa, Inc.*, 81 F.3d 1554, 1562 (Fed. Cir.1996); *Southwall Tech. v. Cardinal IG Co.*, 54 F.3d 1570, 1575 (Fed Cir. 1995).

If a product does not literally infringe an asserted patent claim, it may still be found to infringe under the doctrine of equivalents, which prevents an accused infringer from avoiding liability for infringement by changing only minor or insubstantial details of a claimed invention while retaining the invention's essential identity. *See Festo*, 234 F.3d at 558, 564 (citing *Graver Tank & Mfg. Co. v. Linde Air Prods. Co.*, 339 U.S. 605, 608 (1950)). The determination of equivalence should be applied as an objective inquiry on an element-by-element basis. The so-called "triple identity" test -- which focuses on the function served by a particular claim element, the way that element serves that function, and the result thus obtained by that element -- is a suitable method for determining equivalence with respect to some devices, e.g., certain mechanical devices. It often, however, provides a poor framework for analyzing other products

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[10] (...continued)
A Not intentionally. You might for a party, fireworks.

Peltzer Tr. 767-768. *See also* Peltzer 768-769 (discussing V_{cc} and the power supply illustrated in Figure 9 of the '352 patent specification).

[11] In addition, the sources relied upon by Dr. Fair for his proposal were dated well before the filing date of the patent, including a textbook admittedly published before the invention of integrated circuits. *See* Fair Tr. 249.

or processes. The particular linguistic framework used is less important than whether the test is probative of the essential inquiry, which is whether or not the accused product or process contains elements identical or equivalent to each claimed element of the patented invention. *Warner-Jenkinson Co., Inc. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 39-40 (1997).

The doctrine of equivalents attempts to strike a balance between ensuring that the patentee enjoys the full benefit of his patent and ensuring that the claims give "fair notice" of the patent's scope. Prosecution history estoppel is one tool that prevents the doctrine of equivalents from vitiating the notice function of claims. Thus, actions by the patentee, including claim amendments and arguments made before the Patent Office, may give rise to prosecution history estoppel. Prosecution history estoppel precludes a patentee from obtaining under the doctrine of equivalents coverage of subject matter that has been relinquished during the prosecution of its patent application. The logic of prosecution history estoppel is that the patentee, during prosecution, has created a record that fairly notifies the public that the patentee has surrendered the right to claim particular matter as within the reach of the patent. *Festo*, 234 F.3d at 564-65.

If the patent holder demonstrates that an amendment required during prosecution had a purpose unrelated to patentability, a court must consider that purpose in order to decide whether an estoppel is precluded. Where the patent holder is unable to establish such a purpose, a court should presume that the purpose behind the required amendment is such that prosecution history estoppel would apply. *Warner-Jenkinson*, 520 U.S. at 40-41.

A party alleging infringement has the burden of proving infringement by a preponderance of the evidence. *Envirotech Corp. v. Al George. Inc.*, 730 F.2d 753, 758 (Fed. Cir. 1984); *Hughes Aircraft Co. v. United States*, 717 F.2d 1351, 1361 (Fed. Cir. 1983). The question of

infringement of properly interpreted claims is one of fact. *Mannesmann Demag Corp. v. Engineered Metal Prods. Co.*, 793 F.2d 1279, 1282 (Fed. Cir. 1986).

In this investigation, Complainants assert that the accused devices infringe claims 1, 2 and 8 of the '352 patent, either literally or under the doctrine of equivalents. The accused devices contain SiS's old E5 model ESD transistor, SiS's new E5 transistor, SiS's E6 model ESD transistor, or SiS's E7 model ESD transistor. *See* CPCL 54-57; Stipulation to Further Revise the Prehearing Schedule (Oct. 16, 2001)(EDIS Document Identification No. 200110160020), ¶¶ 21, 23; Letter of Shival P. Virmani, Esq. (October 17, 2001)(EDIS Document Identification No. 200110170034).

For the purposes of this investigation, Respondents stipulated that they would not contest infringement of the '352 patent by the SiS's old E5 model ESD transistor. Complainants and Respondents also stipulated that if Respondents' E6 model ESD transistor is found not to infringe claim 1 of the '352 patent, then neither does claim 1 read on the new E5 model ESD transistor; and further that if Respondents' E6 model ESD transistor is found to infringe claim 1 of the '352 patent, then claim 1 also reads on the new E5 model ESD transistor. *See Id.*

Complainants argue that all sets of ESD circuit diagrams produced by Respondents [12] and that if their proposed construction of a gate is accepted (in which the

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(continued...)

term "gate" encompasses a collection of gate electrodes electrically connected in parallel), then each of the gate electrodes in the accused devices has a source/drain region containing all of the implants in the 5th through 7th elements of claim 1, with the ESD protection device having at least three source/drain regions, thereby satisfying the plural source/drain element of claim 1. It is further argued that Dr. Fair's testimony established that all of the other elements of claims 1, 2 and 8 are literally present in the accused circuits. Complainants take the position that adoption of their proposed construction of the term "gate" supports a finding of literal infringement of claims 1, 2 and 8 of the '352 patent.[13] *See* Complainants' Post-Hearing Brief at 18 (citing CPFF 517-518).

Respondents argue that independent claims 1 and 8 of the '352 patent set forth, in part, "a first lightly implanted region having a second conductivity type opposite to said first conductivity type, under one of said spacers," and they further recite, in part, "a second lightly implanted region of same conductivity type as said silicon substrate, centered under said heavier implanted region." It is argued that according to the proper claim construction, the "second lightly implanted region" must be present for both the source and drain regions of the same gate of the

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[12] (...continued)

[13] Based on similar arguments, Complainants also argue that their own ESD protection devices, which consist of [ ] practice the '352 patent. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 18 n.8 (citing CPFF 525). For the reasons stated, *infra*, the claims of the '352 patent do not read literally on such devices.

ESD device, and that such is not the case with any of SiS's new E5, E6 or E7 model ESD transistors. Thus, Respondents argue, the accused devices in dispute do not literally infringe any asserted claims of the '352 patent. *See* Respondents' Post-Hearing Brief (Following the November Hearing) at 12-13 (citing RPFF 264-284; RX-1 ('352 Patent), claims1 and 8).

The Commission Investigative Staff argues that there cannot be literal infringement of the asserted '352 patent claims because unless one accepts Complainants' proposed interpretation of the term "gate," there is nothing in the '352 patent that teaches or suggests that the "source/drain regions" limitation of claims 1 and 8 refers to the source region of one transistor and the drain regions associated with another transistor. *See* OUII Post-Hearing Reply Brief (Following the November Hearing) at 7-8.

As acknowledged by all parties, a determination of literal infringement as to any of the disputed accused devices depends upon the proper construction of the asserted claims, particularly the term "gate" in independent claim 1 (which necessarily also affects the construction of other terms, including "a first lightly implanted region," a "second lightly implanted region, and the term "gates" in claim 8). As discussed above, Complainants' proposed interpretation of the term "gate" has not been adopted. It is therefore found that the term "gate," as used in claim 1, would not be understood by one of ordinary skill to refer to an ESD protection device comprising multiple transistors with a single gate. Rather, the patent's disclosures are all limited to circuits fabricated symmetrically so that each and every source and each and every drain of each and every transistor has a "lightly implanted region."

Consequently, none of the contested accused devices literally infringes any asserted claim of the '352 patent. Nevertheless, Complainants also contend that application of the doctrine of

equivalents shows infringement by Respondents.

Complainants first argue that prosecution history estoppel does not apply in this case because claim 1 was not narrowed during the prosecution. It is argued that the Preliminary Amendment concerning application claim 7 (issued claim 1) did not follow a prior art or other rejection, nor was there ever a prior art rejection of the claims presented in the parent to the application that matured into the '352 patent. Complainants argue that inasmuch as the original form of application claim 7 recited at least four "source/drain regions," and issued claims 1 and 8 of the '352 patent recite two or more source/drain regions, application claim 7 did not read on the embodiment illustrated in Fig. 7 of the '352 patent, although it is undisputed that issued claim 1 of the '352 patent reads on that figure. Thus, Complainants argue, original claim 7 was amended in a manner that broadened the claim, rather than narrowed it.

Second, Complainants argue that [

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14 While Mr. Peltzer testified that connecting two transistors in parallel would be the functional equivalent of increasing the size of the single transistor in the ESD protection device, from the standpoint of increasing the current-carrying capacity of an ESD protection device, he did not testify that in all other respects two transistors in parallel are the equivalent of a single transistor. In fact, his testimony indicates that in the two different structures, there could be other relevant areas, aside from current-carrying capacity, that would not be equivalent. Mr. Peltzer testified in part:

Q And do you select only one gate to read claim 1 on an infringing device when there's more than one gate contained within an ESD protection

(continued...)

[14] (...continued)
device?

A Well, I understand the term "a gate" not to be limiting, but there must be a particular gate which has the properties identified in claim 1.

Q Now, you testified yesterday that when you use the word "equivalent," you don't speak in terms of its legal meaning but for you it means the same or identical; correct?

A Yes, the common terminology as opposed to the legal interpretation.

Q If you want to increase the current-carrying capacity of an ESD protection device, you could connect a second transistor in parallel or you could physically increase the size of a single transistor; correct?

A Yes.

Q And connecting two transistors in parallel would be the functional equivalent of increasing the size of the single transistor in the ESD protection device; correct?

A Connecting two transistors in parallel would have the same gross effect. It would differ slightly in minor effects.

Q It would be the functional equivalent of increasing the size of the single transistor in the ESD protection device; correct?

A Yes, *in the sense that you could sink more current.*

Q It would be the functional equivalent, would it not, Mr. Peltzer?

A Well, I think I responded, or I hope I responded. In the major effect of sinking more current, that's correct. But there will be minor differences such as if there's increased resistance in the interconnect, the devices when they turn on, they turn on and form parasitic devices. The parasitic devices turn on.

So the actual function of one of these ESD circuits is really quite complicated, after a charge is received. To connect two transistors in parallel and expect it to operate exactly like a single transistor, that

(continued...)

Respondents argue that according to proper claim construction, the "second lightly implanted region" must be present for both the source and drain regions of the same gate of the ESD device, which is not the case with SiS's new E5, E6, or E7 model ESD transistors. It is argued that there is no literal infringement of claims 1 or 8 of the '352 patent, nor can there be infringement under the doctrine of equivalents. Respondents argue that contrary to Complainants' assertions, the Preliminary Amendment in fact narrowed the scope of application claim 7 because the phrase "gates with adjacent spacers"in the original application claim was replaced with the phrase "a gate with adjacent spacers," to require that "each source/drain region" includes, *inter alia*, a second lightly implanted region. It is further argued that in the Remarks to the Amendment, the attorney (who was also the attorney of record for the parent application) stated that "[t]he amended Claims are believed to clarify the invention and put the application in condition for allowance," clearly showing that the amendment was made for the purpose of patentability, and thus foreclosing application of the doctrine of equivalents. Respondents' Post-Hearing Brief (Following the November Hearing) at 13-14.

In addition, Respondents argue that their devices are of the type disclosed by certain prior art references, and that a patentee cannot assert an equivalent that would encompass the prior art. *Id.* at 15 (citing *Wilson Sporting Goods Co. v. Geoffrey & Assocs.*, 904 F.2d 677, 684 (Fed. Cir.

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[14] (...continued)

> may not occur, because of the activation of these secondary devices.
>
> These devices are quite complicated in their operation after the ESD event has occurred.

Peltzer Tr. 980-981 (emphasis added).

1990)). Thus, it is argued, there can be no infringement under the doctrine of equivalents.

The Commission Investigative Staff similarly argues that the amendment to application claim 7 (issued claim 1) narrowed the scope of the claim, and was made for purposes of patentability, thus precluding infringement under the doctrine of equivalents. OUII Post-Hearing Brief (Following the November Hearing) at 11-12.

As discussed above with respect to claim construction, the Preliminary Amendment to application claim 7 (issued claim 1) was made for patentability reasons and narrowed the limitation, thereby creating an estoppel. During prosecution of the '352 patent application, Complainants' patent attorney filed Remarks with the PTO in which he pointed out that "the amended claims are believed to clarify the invention and put the application in condition for allowance." Thus, the amendment sought, at the least, to avoid a rejection (possible under section 112 due to lack of clarity), and in any event "put the application in condition for allowance," i.e., for reasons of patentability. *See Festo*, 234 F.3d 558, 566 ("a 'substantial reason related to patentability' is not limited to overcoming or avoiding prior art, but instead includes any reason which relates to the statutory requirements for a patent").

Inasmuch as "a gate" was amended for patentability reasons, there is no range of equivalents for that claim 1 limitation. Furthermore, neither is claim 8 infringed under the doctrine of equivalents [

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15 Complainants also argue that if their devices are not found to practice the '352 patent literally, then the devices should be found to practice the patent under the doctrine of equivalents. However, Complainants state that the proposed application of the doctrine of equivalents is similar to that used with respect to Respondents' devices. *See* Complainants' Post-Hearing Brief (continued...)

IV. VALIDITY OF THE '352 PATENT

A patent is presumed to be valid. 35 U.S.C. § 282; *DMI Inc. v. Deere & Co.*, 802 F.2d 421 (Fed. Cir. 1986). Although a complainant has the burden of proving a violation of Section 337, it can rely upon the presumption of validity, which a respondent must overcome by clear and convincing evidence. *Checkpoint Systems, Inc. v. United States Int'l Trade Comm'n,* 54 F.3d 756, 761 (Fed. Cir. 1995).

Respondents allege that the asserted claims of the '352 patent are invalid due to anticipation and/or obviousness. *See* Respondents' Post-Hearing Brief (Following the November Hearing) at 1-9. Certain arguments made by Respondents would apply if Complainants' proposed claim construction were to be adopted. *See* Respondents' Post-Hearing Brief (Following the November Hearing) at 6.

The Commission Investigative Staff alleges that claims 1 and 2 of the '352 patent are invalid due to anticipation under 35 U.S.C. § 102. The Commission Investigative Staff does not support Respondents' obviousness allegations under 35 U.S.C. § 103. OUII Post-Hearing Brief (Following the November Hearing) at 12-18.

Complainants oppose the invalidity allegations of the other parties. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 39-43; Complainants' Post-Hearing

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[15] (...continued)
(Following the November Hearing) at 20. For the reasons stated, *supra*, the doctrine of equivalents cannot be used to read the claims of the '352 patent onto structures such as those found in Respondents' and Complainants' devices. Consequently, inasmuch as Complainants' devices have not been shown to practice any claim of the '352 patent either literally or under the doctrine of equivalents, the technical element of the domestic industry requirement is not satisfied. The statutory requirements of section 337 concerning a domestic industry, as well as a discussion of the economic element of the domestic industry requirement, are discussed, *infra*, in section VII.

Reply (Following the November Hearing) at 30-32. Furthermore, Complainants argue that Respondents are prevented from effectively challenging the validity of the '352 patent due to assignor estoppel. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 35-39; Complainants' Post-Hearing Reply (Following the November Hearing) at 29.

A. Assignor Estoppel

The doctrine of assignor estoppel bars an assignor of a patent and parties in privity from challenging an assigned patent's validity. *See Lannom Mfg. Co. v. United States Int'l Trade Comm'n*, 799 F.2d 1572, 1579 (Fed. Cir. 1986). The doctrine has been developed to avoid "the unfairness and injustice that would be suffered by the assignee [of a patent] if the assignor were allowed to raise defenses of patent invalidity" in a subsequent infringement action brought by the assignee. *Diamond Scientific Co. v. Ambico, Inc.*, 848 F. 2d 1220, 1225 (Fed. Cir. 1988).

Courts and the Commission have consistently recognized the inequality of permitting an assignor to defend a patent infringement claim by attempting to prove "that what he assigned was worthless." *See Id.* at 1226; *Intel Corp. v. United States Int'l Trade Comm'n*, 946 F. 2d 821, 837 (Fed. Cir. 1991). Although application of the doctrine of assignor estoppel could result in the issuance of a section 337 remedy against products practicing an invalid patent, the Commission and the Federal Circuit have concluded, based on the language of 19 U.S.C. § 1337(c) and case law, that the doctrine of assignor estoppel must be considered if it is duly raised, and, if applicable, estoppel must be applied in section 337 investigations inasmuch as all legal and equitable defenses may be presented in all section 337 cases. *See Intel*, 946 F. 2d at 837 (quoting *Lannom*, 799 F.2d at 1579).

Neither of the two patentees/assignors of the '352 patent is named as a respondent in this

investigation. However, at least one of the assignors, Mr. Hsue, is an employee of respondent SiS-TW. Thus, in an effort to prevent Respondents from attacking the validity of the '352 patent, Complainants argue that Respondents are in privity with Mr. Hsue. The question of privity was addressed in detail by the Federal Circuit in *Shamrock Tech. Inc. v. Medical Sterilization Inc.*, 903 F. 2d 789 (Fed. Cir. 1990). The Federal Circuit considered whether an assignor's new employer was sufficiently in "privity" with the assignor so as to be subject to assignor estoppel. In this regard, the *Shamrock* court stated:

> Privity, like the doctrine of assignor estoppel itself, is determined upon a balance of the equities. If an inventor assigns his invention to his employer company A and leaves to join company B, whether company B is in privity and thus bound by the doctrine will depend on the equities dictated by the relationship between the inventor and company B in light of the act of infringement. The closer the relationship, the more the equities will favor applying the doctrine to the company.

Shamrock, 903 F. 2d at 793.

Before finding that the assignor was more than a "mere employee" and was directly involved in causing the employer's infringing operations, the *Shamrock* court made the following findings: (a) the employee/assignor joined the new employer/alleged infringer as Vice-President in charge of operation; (b) the employee/assignor received 50,000 shares; (c) the new employer built the facilities to carry out the accused infringement after the employee/assignor was hired; (d) the assignor and employer jointly made the decision to begin the accused activity; and (e) the employee/assignor was personally in charge of all the employer's operations.

The factors considered in the *Shamrock* case are useful to determine the central question of whether "the ultimate infringer availed itself of the inventor's 'knowledge and assistance' to

conduct infringement."[16] *See Intel*, 946 F.2d at 839 ("What is significant is whether the ultimate infringer availed itself of the inventor's 'knowledge and assistance' to conduct infringement."); *see also Mentor Graphics Corp. v. Quickturn Design Systems, Inc.*, 150 F.3d 1374, 1379 (Fed. Cir. 1998)(privity found where assignor company bought accused infringer company so that it could undertake the actions in dispute); *Shamrock*, 903 F.2d at 794 ([A]s above indicated, [assignor] Luniewski was far more than a mere employee of MSI and the undisputed facts establish MSI's direct involvement of Luniewski in MSI's infringing operations. MSI clearly availed itself of Luniewski's "knowledge and assistance" to conduct infringement.").

Complainants assert that under the *Shamrock* standard, assignor estoppel should be applied against Respondents in this investigation. [

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[16] Much of the formulation relating to assignor estoppel may be traced back at least to *Mellor v. Carroll*, 141 F. 992, 993-94 (C.C.D. Mass. 1905)("If the estopped assignor enters into business with others, *who derive from him their knowledge of the patented process or machine availing themselves of this knowledge and assistance*, enter with him upon a manufacture infringing the patent which he has assigned, they are bound by his estoppel." (emphasis added)).

[

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Respondents contend that the *Shamrock* standard is not satisfied for several reasons which in their totality counsel against the application of assignor estoppel. [

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[

] Thus, the Staff concludes that no purposeful relationship between the assignor and accused infringer is apparent. OUII Post-Hearing Brief (Following the November Hearing) at 15.

[

] On December 1, 1999, [ ], Mr. Hsue joined SiS-TW as deputy director of the fab. Hsue Tr. 1132.

Mr. Hsue's initial responsibilities at SiS involved the integration of the process used at the fab. Currently, Mr. Hsue is the director of the process technology department, and his major responsibility is process technology development. Hsue Tr. 1132, 1135-1136, 1186-1187. [

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Complainants argue that SiS, as a former customer of UMC, did not need assistance from Mr. Hsue, or anyone else, to copy the design and layout for an infringing ESD protection device.[17] Rather, Complainants argue, SiS needed Mr. Hsue's assistance to implement and refine that design as part of the manufacturing process, and that is how Mr. Hsue facilitated the alleged infringing activities as an SiS employee. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 37-38; Complainants' Post-Hearing Reply Brief (Following the November Hearing) at 29 (citing CPFF 754-75; CPRF 103-04, 112-24.); CPFF 759-75.

However, Mr. Hsue testified that when he was hired by SiS, there was no understanding that he would be working to develop or improve ESD protection device designs or layouts. Mr. Hsue also testified that the people working on the ESD protection device designs and layouts did not work for him, and that he was never consulted on SiS's ESD protection device designs or layouts before or during his employment with SiS. Mr. Hsue also testified that he did not and does not supervise the development and refinement of SiS's ESD protection device designs or layouts. Mr. Hsue testified that he has never learned, nor is he responsible for, the details

[17] Implementation and refinement of the ESD protection device design are at the core of Complainants' assignor estoppel argument. For example, Complainants argue that it is of no moment SiS may have adopted a design rule incorporating elements of the accused device design even before Mr. Hsue began working at SiS-TW. *See* Complainants' Post-Hearing Reply Brief (Following the November Hearing) at 29.

pertaining to SiS's ESD protection device designs and layouts. *See, e.g.*, Hsue Tr. 1136, 1142-1143.

While the record shows that Mr. Hsue was working at SiS and thus able to assist in making the sorts of refinements to the ESD designs that Complainants say he did, the record does not contain persuasive evidence that he actually did so. Furthermore, Mr. Hsue testified that he did not make refinements to SiS's ESD designs. *See, e.g.*, Hsue Tr. 1136, 1142-1143, 1197-1202. Indeed, as detailed in other parts of this opinion, the record shows that SiS does not use the ESD protection device covered by the '352 patent. It would, therefore, be illogical to apply assignor estoppel on the grounds that Mr. Hsue provided expertise to SiS on how to implement his '352 patent ESD protection device design, when in fact SiS does not use the '352 patent's ESD protection device.

Consequently, the record does not support a conclusion that SiS availed itself of Mr. Hsue's knowledge and assistance to conduct infringement. Respondents are not estopped from raising their affirmative defenses of invalidity of the '352 patent.

B. Anticipation

Anticipation is a question of fact which must be proven by clear and convincing evidence. *Glaxo Inc. v. Novopharm Ltd.*, 52 F.3d 1043, 1047 (Fed. Cir.), *cert. denied*, 516 U.S. 988 (1995); *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 1576 (Fed. Cir. 1991). A claim is anticipated, and therefore invalid, if a single prior art reference discloses each and every limitation of the claim. *Bard v. M3 Systems*, 157 F.3d 1340, 1349 (Fed. Cir. 2000); *Glaxo*, 52 F.3d at 1047. The disclosure need not be express, but may anticipate by inherency where such inherency would be appreciated by one of ordinary skill in the art. *Glaxo*, 52 F.3d at 1047;

Standard Havens Prod., Inc. v. Gencor Indus., Inc., 953 F.2d 1360, 1369 (Fed. Cir. 1991); *Continental Can Co. USA Inc. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991).

Respondents argue that Japanese Kôkai No. 64-23573 ("the Umemoto publication"),[18] entitled "Semiconductor Integrated Circuit," published on January 26, 1989, anticipates claims 1 and 2 of the '352 patent. *See* Respondents' Post-Hearing Brief (Following the November Hearing) at 1-3. Respondents also argue that if Complainants' proposed claim construction were adopted, claims 1 and 2 of the '352 patent would be anticipated by Japanese Kôkai No. 5-102475 ("the Yasui publication"). *See Id.* at 6.

The Commission Investigative Staff argues that both the Umemoto publication and Japanese Kôkai No. 63-141778 ("the Kishi publication") anticipate claims 1 and 2 of the '352 patent, and that the Yasui publication fails to teach every element of the asserted claims and is, therefore, not an anticipatory reference. *See* OUII Post-Hearing Brief (Following the November Hearing) at 16.

Complainant argues that none of the references relied upon by the other parties (i.e., the Umemoto publication, the Yasui publication or the Kishi publication) invalidates any allegedly anticipated claim of the '352 patent. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 39-41; Complainants' Post-Hearing Reply Brief (Following the November Hearing) at 29-32.

[18] The Umemoto publication (Japanese Kôkai No. 64-23573), entitled "Semiconductor Integrated Circuit," was published on January 26, 1989, more than one year prior to the earliest effective filing date of the '352 patent. The Umemoto publication was published by the Japan Patent and Trademark Office in the *Laid Open [KÔKAI] Patent Gazette*. *See* RX-17 at 389; RX-18 at 1; Peltzer Tr. 734, 779.

1. The Umemoto Publication

Respondents argue that claims 1 and 2 of the '352 patent are anticipated by the Umemoto publication because it discloses the precise structure disclosed in the preferred embodiment of the '352 patent. *See* Respondents' Post-Hearing Brief (Following the November Hearing) at 1-3.

The Commission Investigative Staff argues that the Umemoto publication anticipates claims 1 and 2 of the '352 patent. *See* OUII Post-Hearing Brief (Following the November Hearing) at 16 (citing SPFF).

Complainants argue that the Umemoto publication does not disclose each and every element of claims 1 and 2 of the '352 patent. It is argued that in particular, Respondents failed to prove by clear and convincing evidence that the Umemoto publication discloses a dedicated ESD protection device, implanted regions, or that the PESD implant in the Umemoto publication is centered under a heavier implanted region. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 39-40; Complainants' Post-Hearing Reply Brief at 30.

The preamble of claim 1 of the '352 patent recites "[a]n ESD protection device with reduced junction breakdown voltage, connected to an integrated circuit which includes FET devices. . . ." The Umemoto publication states in language similar to the '352 patent that the "invention pertains to electrostatic breakdown strength of MOS type semiconductor integrated circuits."[19] RX-18 at 1; *see* Peltzer Tr. 743-744. In particular, the Umemoto publication states:

> By disposing a region of the same conductivity type as the substrate semiconductor and with a higher impurity concentration than that of the substrate semiconductor just under the contact part between a drain diffusion layer and a power source wiring layer in this

[19] As discussed, *supra*, an FET (field effect transistor) is typically a MOS (metal oxide silicon) transistor, which contains a source, a gate and a drain. *See* Peltzer Tr. 707.

> invention, the junction breakdown voltage between the drain diffusion layer and the high concentration region is lowered, whereby a momentary high voltage impressed on the drain through the power source wiring layer will cause junction breakdown voltage to occur before the gate oxide film is damaged.

RX-18 at 2.

The first element of claim 1 of the '352 patent is "a silicon substrate having a first conductivity type." Similarly, with respect to Figure 1 of the Umemoto publication, the publication states: "In this figure, 1 is a P type silicon substrate." RX-18 at 3; *see* Peltzer Tr. 744-746.

The second element of claim 1 of the '352 is "field oxide regions in and on said silicon substrate for isolation of said ESD protection device." The Umemoto publication also discloses such isolation by oxide regions. *See* RX-18 at 4 ("9 is an element isolation oxide film . . ."); *see* Peltzer Tr. 744-745.

The third element of claim 1 of the '352 patent is "a gate with adjacent spacers for said ESD protection device, between said field oxide regions." Similarly, the Umemoto publication discloses that "3 is a gate electrode . . ." and "8 is a sidewall oxide film. . ." RX-18 at 4, figure 1; *see* Peltzer Tr. 745.

The fourth and final element of claim 1 of the '352 patent begins with the recitation of "source/drain regions for said ESD protection device between said gate and said field oxide regions, with each source/drain region comprising . . . ." The Umemoto publication is also directed toward a device with similar "source and drain diffusion layers 26, 27 . . . ." RX-18 at 2, figures 1 and 2. The fourth element of claim 1 proceeds to require "a first lightly implanted region having a second conductivity type opposite to said first conductivity type, under one of

said spacers. . . ." The Umemoto publication likewise discloses that "5 is a low-concentration (up to $10^{18}/cm^3$) drain region unique to LDD structures."[20] RX-18 at 4; Peltzer Tr. 745. The fourth element of claim 1 of the '352 patent also requires "a heavier implanted region of the same conductivity type as said first lightly implanted region, located between said first lightly implanted region and one of said field oxide regions . . . ." The Umemoto publication requires that "4 is a drain (n+) region . . . " RX-18 at 4, figure 1; Peltzer Tr. 745. Finally, the fourth element of claim 1 of the '352 patent requires "a second lightly implanted region of same conductivity type as said silicon substrate, centered under said heavier implanted region." Similarly, the invention of the Umemoto publication has a "high concentration (up to $10^{17}/cm^3$) impurity region, i.e., P type diffusion region 7 is added to the . . . LDD structure MOS transistor structure, just under the contact part between the power source." RX-18 at 4; Peltzer Tr. 745.

Claim 2 of the '352 patent reads: "The ESD protection device of claim 1 wherein said first conductivity type is P-type, and said second conductivity type is N-type." The device disclosed in the Umemoto publication also covers such first and second conductivities, stating: "Figure 1 is a sectional drawing of a N channel MOS transistor of this invention. In this figure, 1 is a P type silicon substrate . . . ." RX-18 at 3; *see* Peltzer Tr. 746.

Thus, the Umemoto publication discloses all the elements of claims 1 and 2 of the '352 patent.

Complainants argue that claims 1 and 2 are not anticipated because the prior art Umemoto reference (RX-17 and 18) fails to disclose "second lightly implanted regions" that are

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[20] The acronym "LDD" is used in the Umemoto publication to mean "lightly doped drain structures." *See* RX-18 (English translation) at 4. Similarly, the '352 patent refers to "LDD (lightly doped drain) regions." CX-2/RX-1 ('352 Patent), col. 1, lines 42-43.

"centered" and made from "ion implantation." *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 39-40. Although the term "centered"is found in the '352 claim language, the specification contains no elaboration on the significance or necessity for centering in the patent. Indeed, during the hearing, Respondents' expert could not find in the specification an explication of the centering of the second lightly implanted region, yet indicated that a teaching or disclosure of such "centered" regions was in his view the essential difference between claims 1 and 2 of the '352 patent and the Umemoto publication.[21] *See* Fair Tr. 1076-

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[21] Dr. Fair testified in pertinent part, as follows:

> Q Professor Fair, are you saying that everything in claim 1 is in the prior art, except for the word "centered for the second lightly implanted region of same conductivity type as said silicon substrate"? If we just said "under said heavier implanted region" and not "centered under said heavier implanted region," everything would be shown in the prior art?
>
> A That would be my opinion, subject to under -- if there's clarification as to what this structure really represents.
>
> Q So I believe both Complainant and Respondents have failed the Court, because neither side has provided a claim construction for the term "centered." What is your definition, your claim construction for the word "centered" in claim 1 of the '352 patent?
>
> MR. KIKEL: Your Honor, I'll note for the record that we did provide a claim construction for "centered."
>
> JUDGE HARRIS: Then it will be easy for him to answer.
>
> THE WITNESS: UMC's construction of centered under said ESD implanted region is found on page 9 of CPX-7. And in this regard, "centered" means placed in the center of the heavier implanted region, which is above the second lightly implanted region. And the second lightly implanted region is geometrically in the central portion of the cross-sectional view of the heavier implanted region.
>
> BY MR. HOVANEC:

(continued...)

[21] (...continued)

Q And what is the importance of being geometrically in the central portion of the cross-sectional view of the heavier implanted region?

A Well, since you have a huge surge of energy coming into the drain electrode, which is -- so if this were a drain electrode connected to a pad, you would have a huge amount of energy coming in here. What you would like to do is to make sure that the breakdown is initiated across a region such that the energy can be divided. When it goes to the left or to the right, you like it to be uniformly distributed so that one of these transistors does not receive more than some equal share of energy.

Q Is that explained anywhere in the text of the '352 patent?

A I don't believe so, but this would be something that one of ordinary skill reading the patent would have this knowledge with them.

Q Now, in this claim construction that you referred to, the next -- well, first you're discussing the preferred embodiment when you define the term "centered." Is that correct? On page 9 of CPX-7.

A I'm not referring to any particular preferred embodiment. I'm talking about -- I don't believe. Let me just verify that, please. I'm having difficulty finding the portion of the specification that uses the term "centered."

MR. HOVANEC: Your Honor, I'm sorry, I'm not aware of any discussion of the word "centered." Otherwise I would help the witness to speed this along.

THE WITNESS: I did not find any reference to centered in the spec.

BY MR. HOVANEC:

Q Now, going back to the UMC construction at page 9 of CPX-7, the last sentence says "however, the term 'centered' is not limited by this preferred embodiment combined region." Does that mean that the word "centered" doesn't mean geometrically in the central portion of the cross-sectional view of the heavier implanted region?

A Could you ask that again? I'm sorry.

(continued...)

1079.

The Umemoto publication likewise does not contain explicit textual statements that the second lightly implanted regions are "centered." The Umemoto publication does, however, provide that this region is "just under" the source drain region. RX-18 at 4. Furthermore, the Umemoto publication figures clarify that in addition to being "just under" the source and drain, the "second lightly implanted region" is also "centered" under the source and drain. RX-17 at 2 (abstract), 5 (document page 391).

Complainants argue that one of ordinary skill in the art would not understand the Umemoto figures to teach a "centered" implant under the source and drain. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 40. However, where, as here, the drawing provides a clear teaching, in this case of a centered implant, that drawing can and should

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[21] (...continued)

Q I'm directing your attention to page 9 of CPX-7, and under the "UMC construction," the last sentence says "however, the term 'centered' is not limited by this preferred embodiment combined region."

Does that mean that the term "centered" does not mean a region that is geometrically in the central portion of the cross-sectional view of the heavier implanted region?

A No, not at all. Because if you look at figure 7, it says that the regions 36 are created through the contact windows 32, and the term "centered" is not limited by the preferred embodiment in which the implants are performed through the contact windows.

Q Well, I'm confused, Dr. Fair. Do the second lightly implanted regions of same conductivity type as said silicon substrate have to be geometrically in the central portion of the cross-sectional view of the heavier implanted region or not?

A Yes, they do.

Fair Tr. 1076-1079.

be used for anticipation purposes. Indeed, 35 U.S.C. § 102(b) provides no arbitrary distinction between the words or drawings of a prior art reference. *See Ecolochem, Inc. v. Southern California Edison Co.*, 227 F.3d 1361, 1370 (Fed. Cir. 2000) (proper for district court to use figure from a public presentation in order to render anticipated certain claims of asserted patent); *In re Aslanian,* 590 F.2d 911, 914 (C.C.P.A. 1979)("This court has stated that a drawing in a utility patent can be cited against the claims of a utility patent application even though the feature shown in the drawing was unintended or unexplained in the specification of the reference patent").

Complainants further argue that the Umemoto publication fails to disclose ion implantation. Complainants' Post-Hearing Brief (Following the November Hearing) at 39-40. However, the record shows that persons of ordinary skill in the art at the time the '352 patent application was filed understood that dopants in the source/drain regions could be provided by either diffusion or ion implantation. Peltzer Tr. 746-747. Furthermore, persons of ordinary skill also recognized that there is little or no difference between implantation and diffusion.[22] Peltzer

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[22] Mr. Peltzer cited examples from the art to support his conclusions, and also testified in part, as follows:

BY MR. HOVANEC:

> Q We can do that now. Is there any difference between a diffusion layer and an implantation layer?
>
> A Well, I learned from the early days starting in '67 that implants were equivalent to what was known as "predep." You introduce dopants into the wafer by a chemical process known as "predeposition," and then you redistribute those by diffusion. In other words, you heat the wafer and the dopant atoms move away from the high concentration regions to the low concentration regions, which I think of as the dopant atoms go downhill. There's a law for this.

(continued...)

Tr. 746-749, 755; RX-222 at 4; RX-28, col. 12, lines 25-40.[23]

Consequently, for the reasons discussed above, it is found that the record demonstrates by clear and convincing evidence that claims 1 and 2 of the '352 patent are anticipated by the Umemoto publication.

2. The Kishi Publication

Respondents did not address the Kishi publication (RX-19, RX-20) in detail in their main post-hearing brief, and appear not to mention it in their reply brief. Where the Kishi publication

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[22] (...continued)

> The implant is also a technique for introducing dopant into the wafer, just like predeposition, and it is customary to follow the implant by a heating step. The heating step has two purposes. One is to anneal damage caused by implanting into the wafer, implanting ions into the wafer, which break up the silicon a bit. And secondly, the heating step diffuses the implant, and depending on the length of the heating step, you can diffuse great distances or short distances.
>
> So the term "diffusion" refers to the structure after the heating step from implant or predeposition. So I find the term "implant" to be equivalent to the term "diffusion" in this case.

Peltzer Tr. 746-747.

Complainants' expert, Dr. Fair, testified about differences between implantation and diffusion processes, and that a preference developed for implantation technology. Nevertheless, his testimony failed to point out, from the standpoint of a manufactured product (rather than a process), any significant differences between the Umemoto publication and the '352 patent. *See* Fair Tr. 1051-1053. Dr. Fair's testimony also does not contradict that of Mr. Peltzer to the extent that one of ordinary skill in the art would find in the Umemoto publication a disclosure of the claimed invention of claims 1 and 2 of the '352 patent.

[23] In addition to arguing that the Umemoto publication is not anticipatory because it fails to disclose "second lightly implanted regions" that are centered and made from ion implantation, Complainants also argue that the publication is directed to a single transistor, whereas the '352 patent discloses an ESD protection device. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 39. However, Complainants' proposed claim construction has not been adopted. Claims 1 and 2 of the '352 patent cover ESD protection devices that include single or multiple transistors.

is mentioned, it is in connection with other publications. *See* Respondents' Post-Hearing Brief at 8, 15; Respondents' Post-Hearing Reply Brief (Following the November Hearing).[24] Respondents do, however, propose a series of findings of fact concerning alleged anticipation by the Kishi publication of claims 1 and 2 of the '352 patent. *See* CPFF 173-199.

The Commission Investigative Staff does not address in detail the Kishi publication in its post-hearing brief. The Commission Investigative Staff does, however, state that the Kishi publication anticipates claims 1 and 2 of the '352 patent, and refers to the Commission Investigative Staff's proposed findings of fact. *See* OUII Post-Hearing Brief (Following the November Hearing) at 16-17; *see also* SPFF 64-65 (concerning alleged anticipation of claim 1 and 2 of the '352 patent by the Kishi publication). The Commission Investigative Staff mentions the Kishi publication only briefly in its reply. *See* OUII Post-Hearing Reply Brief (Following the November Hearing) at 10 n.8.

Complainants argue that the Kishi publication does not anticipate claims 1 and 2 of the '352 patent in that Respondents have failed to prove by clear and convincing evidence that the Kishi publication discloses: a dedicated ESD protection device; an ESD protection device with reduced junction breakdown voltage; or a centered PESD implant. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 40. In their reply, Complainants address obviousness arguments made by Respondents with respect to the Kishi publication. It also appears that Complainants interpret Respondents' main post-hearing brief as having conceded that the Kishi publication does not anticipate any claims of the '352 patent. Complainants' Post-Hearing Reply Brief (Following the November Hearing) at 32.

[24] Respondents have styled their reply brief as a "rebuttal brief."

No party has briefed the Kishi publication in sufficient detail to explain why the publication should be found to anticipate claim 1 or claim 2 of the '352 patent. Respondents' proposed findings concerning the Kishi publication which purport to demonstrate that Kishi anticipates claim 1 and 2 of the '352 patent are based on the publication itself and expert testimony received at the hearing from Respondents' expert, Mr. Peltzer (*see, e.g.* Peltzer Tr. 778-787). The testimony shows that Mr. Peltzer gave careful consideration to the Kishi publication, and in one instance asked for re-translation of a portion of the Kishi publication to be sure that he understood the structure of the disclosed device. The testimony also refers to a table in which Mr. Peltzer has equated each limitation of claims 1 and 2 of the '352 patent with a portion of the Kishi publication's disclosure. The Kishi publication may anticipate claims 1 and 2 of the '352 patent. However, despite Mr. Peltzer's work with the Kishi publication, the record contains little overall information about the Kishi publication and the device disclosed therein, including a clear explanation of how the disclosed device would operate. Although the Kishi publication may have anticipated claims 1 and 2 of the '352 patent, that fact has not been established by clear and convincing evidence.

3. The Yasui Publication

Respondents argue that the Yasui publication (RX-21, RX-22) should be found to anticipate claims 1 and 2 of the '352 patent if Complainants' proposed claim construction is adopted for the '352 patent. *See* Respondents' Post-Hearing Brief (Following the November Hearing) at 6.

The Commission Investigative Staff argues that the Yasui publication fails to teach every element of the asserted claims of the '352 patent. *See* OUII Post-Hearing Brief (Following the

November Hearing) at 16. Complainants argue that the Yasui publication does not anticipate claim 1 or claim 2 of the '352 patent. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 40-41; Complainants' Post-Hearing Reply Brief (Following the November Hearing) at 31.

In view of the fact that Complainants' proposed claim construction has not been adopted in this Initial Determination, no party seeks a determination that the Yasui publication is anticipatory. Furthermore, as Mr. Peltzer testified at the hearing, the device disclosed in the Yasui patent, like the SiS products, does not have a p^+ implant on the source side. Thus, the device disclosed in the Yasui publication is not covered by any asserted claim of the '352 patent when properly construed. *See* Peltzer Tr. 757.

The Administrative Law Judge does not find that the record establishes anticipation by the Yasui publication.

C. Obviousness

1. Background

Respondents argue that claims 1, 2 and 8 of the '352 patent are invalid for obviousness, based on various combinations of prior art. *See* Respondents' Post-Hearing Brief (Following the November Hearing) at 3-7; Respondents' Post-Hearing Reply Brief (Following the November Hearing) at 19-20. The Commission Investigative Staff does not argue that any claim of the '352 patent has been shown to be obvious, and affirmatively argues that there is a lack of evidence with respect to the combination of certain prior art. OUII Post-Hearing Brief (Following the November Hearing) at 16-18. Complainants argue that the record does not support a finding that any asserted claim of the '352 patent is obvious. *See* Complainants' Post-Hearing Brief

(Following the November Hearing) at 40-43; Complainants' Post-Hearing Reply Brief (Following the November Hearing) at 31-32.

Pursuant to 35 U.S.C. § 103, a patent may be found invalid if "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." 35 U.S.C. § 103. The ultimate question of obviousness is a question of law, but "it is well understood that there are factual issues underlying the ultimate obviousness decision." *Richardson-Vicks Inc. v. The Upjohn Co.*, 122 F.3d 1476, 1479 (Fed. Cir. 1997).

After construing the claims, the next step in an obviousness inquiry is to determine whether the claimed invention would have been obvious as a legal matter. "In order to determine obviousness as a legal matter, four factual inquiries must be made concerning: 1) the scope and content of the prior art; 2) the level of ordinary skill in the art; 3) the differences between the claimed invention and the prior art; and 4) secondary considerations of nonobviousness, which in case law is often said to include commercial success, long-felt but unresolved need, failure of others, copying, and unexpected results."[25] *Ruiz v. A.B. Chance Co.*, 234 F.3d 654, 662-63 (Fed.

[25] Respondents argue in their main post-hearing brief that Complainants have made no showing as to any secondary considerations that would support the patentability of claim 8 of the '352 patent. Respondents argue that Complainants apparently have never used the particular circuitry of claim 8 in any commercial product and do not use the "key element of the lightly doped P- regions 36" under the source region and the drain region of an ESD protection device as recited in claim 1. Indeed, they argue, grounded gate devices have been known for many years and were in the prior art with respect to the '352 patent. *See* Respondents' Post-Hearing Brief (Following the November Hearing) at 5-6 (citing Fair Tr. 361).

Complainants did not, in fact, address secondary considerations (objective indicia) in their main or reply briefs. Nor does it appear that Complainants proposed a set of findings for this

(continued...)

Cir. 2000)(citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966) and *Miles Labs., Inc. v. Shandon, Inc.*, 997 F.2d 870, 877 (Fed. Cir.1993)).

The prior art (and the combinations thereof) that are relied upon by Respondents as to specific patent claims are the following (in the order presented by Respondents): alleged obviousness of claim 8 over Japanese Kôkai No. 3-196677 (RX-23, RX-24)("the Soeda publication") or Japanese Kôkai No. 01-134961 (RX-195)("the Kamioka publication) in view of Umemoto publication; alleged obviousness of claims 1 and 2 over the Yasui publication and alleged invalidity of claim 8 over Soeda or Kamioka in view of the Yasui publication; and alleged invalidity of claim 8 over the Yasui publication in view of the Soeda publication.[26, 27] *See* Respondents' Post-Hearing Brief (Following the November Hearing) at i, 3-7. These contentions are discussed below in the order in which they are addressed in Respondents' main post-hearing brief (in which the arguments are cumulative).

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[25] (...continued)
factor. In addition, the Administrative Law Judge is aware of no evidence in the record that is relevant to secondary considerations and would outweigh the technical evidence indicating obviousness of claim 1, 2 or 8 of the '352 patent.

[26] It does not appear that any party contests that these references relied on by Respondents are prior art. The Administrative Law Judge has also included findings in the Findings of Fact portion of the Initial Determination concerning the prior art status of the references at issue.

[27] In their main post-hearing brief, Respondents also discuss their request that the PTO reexamine the '352 patent based on certain prior art also relied on in this investigation, as well as an additional patent to Bergonzoni (U.S. Patent No. 4,968,639). While the Administrative Law Judge notes these arguments, their presentation does not constitute an additional and separate basis for alleged invalidity. *See* Respondents' Post-Hearing Brief (Following the November Hearing) at 7-8.

2. Alleged Obviousness of Claim 8 over the Soeda Publication or the Kamioka Publication in View of the Umemoto Publication

As discussed in the section on claim construction, in independent claim 1, the term "a gate" must be associated with a specific FET, while in independent claim 8, the term "gates" must be construed as two or more gates in which each of the gates has a field oxide region on each side. As found above, the Umemoto publication invalidates independent claim1 (and dependent 2) of the '352 patent. Respondents argue that the Soeda publication and the Kamioka publication make claim 8 obvious in view of the Umemoto publication. Thus, Respondents must demonstrate that the Soeda publication and the Kamioka publication bridge the gap for a claim that reads on a single gate (as in claim 1), and one that reads on plural gates (as in claim 8).

With respect to the Soeda publication, Respondents argue that it is directed to a semiconductor device characterized by gate oxide films of MOSFETs[28] that include input/output circuits connected to the pad on a semiconductor substrate being formed so that they are thicker than the gate oxide films of other MOSFETs on the substrate. Furthermore, it is argued that the Soeda publication teaches the electrical connection of NMOS ESD protection devices in which: the gates are connected to ground and the source of the second ESD device (6') is also connected to ground; and the drain of the second ESD device (6') and the source of the first ESD device (5') are connected to the pad with the drain of the first ESD device connected to V_{cc}. Structurally, a source and a drain are identical. Thus, Respondents argue, inasmuch as the ESD devices in the

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[28] Although Respondents' main post-hearing brief refers to a "MOFSET" or to "MOFSETS," Respondents undoubtedly intend to refer to a MOSFET or to MOSFETs. This is confirmed by Respondents' proposed findings of fact, which refer to MOSFETs, and an examination of the Soeda publication, which also refers to MOSFETs.

Soeda publication, like the Umemoto publication and the '352 patent, are all completely symmetrical and the gates of both ESD transistors are connected to ground, it is a matter of semantics whether in Soeda the "drain" of the first ESD device is connected to V_{cc} with the "source" connected to the pad or vice versa. Respondents' Post-Hearing Brief (Following the November Hearing) at 3-4 (citing Fair Tr. 357; RPFF 244-254); Respondents' Post-Hearing Brief (Following the November Hearing) at 19-20.

With respect to the Kamioka publication, Respondents argue that it discloses: an input protection circuit for a semiconductor integrated circuit which has an electrical connection between an input pad and drain regions of two input protection circuit transistors; an electrical connection which is made to ground for the gates of the input protection circuit transistors, as well as for the source region of one of the transistors; and that an electrical connection is also made between V_{cc} and the source of the other input protection circuit transistor. Respondents further argue that, as in the case of the Soeda publication, the gates of the two ESD devices disclosed in the Kamioka publication are connected to ground with the source of the first ESD device connected to V_{cc}; the source of the second ESD device in the Kamioka publication is connected to ground; and finally, the drains of Kamioka's first and second ESD devices are connected to the pad. Respondents' Post-Hearing Brief (Following the November Hearing) at 3-4; Respondents' Post-Hearing Brief (Following the November Hearing) at 19-20.

The Commission Investigative Staff argues that in its pre-hearing statement, the Staff took the position that claim 8 of the '352 patent is obvious when the Umemoto publication is combined with the Soeda publication, upon the expectation that Respondents would put forward evidence as to the motivation of a person of ordinary skill in the art to combine these two prior

art references. The Staff argues that at the hearing Respondents failed to adduce evidence of any motivation whatsoever, and that instead, Mr. Peltzer simply testified that the Umemoto publication in view of the Soeda publication would fully disclose the elements of claim 8 of the '352 patent. The Staff argues that by contrast, Dr. Fair testified as to why a person skilled in the art would not be motivated to combine them as follows:

> Umemoto focuses on improving the breakdown withstand voltage of a transistor in an integrated circuit rather than an ESD protection device. And Soeda is concerned only with electrically connecting ESD protection devices. So Soeda teaches input/output circuits with two protection devices. So there's no motivation or suggestion to combine these two references.
>
> * * *
>
> Umemoto doesn't talk at all about wiring his transistors into any kind of an input/output circuit.

OUII Post-Hearing Brief (Following the November Hearing) at 16-18 (citing Peltzer Tr. 778; Fair Tr. 1061). Thus, the Staff argues, the weight of the testimony requires the conclusion that Respondents have not proven their obviousness-related contentions by clear and convincing evidence. OUII Post-Hearing Brief (Following the November Hearing) at 18 (citing *In re Zurko*, 258 F.3d 1379, 1384-85 (Fed. Cir. 2001)(Even under the standard applied before the Patent Office's Board of Patent Appeals (which is less than clear and convincing evidence) the Board cannot rely on general conclusions about what is "basic knowledge" or "common sense." Rather, an obviousness finding must be based on concrete findings in the evidentiary record)).

Much of Complainants' argument concerning a combination of the Umemoto publication with either the Soeda publication or the Kamioka publication is based on their argument that the Umemoto publication lacks elements common to claim 8 and claim 1. Those arguments have

been rejected in connection with the anticipation discussion above. Nevertheless, other arguments made by Complainants are relevant to the obviousness question. Complainants argue that the Soeda publication focuses on thickening gate oxides and does not focus on any other aspects of the structures of the devices in the author/patentee's input/output circuit. Complainants further argue that the Kamioka publication teaches how to connect electrically the configuration of two transistors in an ESD protection circuit, and that it has not been shown how one of skill in the art, having been provided with the Umemoto publication covering an FET device, would be motivated to look to the Kamioka publication, or the Soeda publication, to find out how to connect electrically the device of the Umemoto publication. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 42-43; Complainants' Post-Hearing Reply Brief (Following the November Hearing) at 31.

Upon examination of the parties' arguments, and having already determined the scope of the Umemoto publication's disclosure vis-a-vis claim 1, the primary issue to be decided in determining whether the Soeda publication and the Kamioka publication render claim 8 obvious in view of the Umemoto publication is whether it has been established that one of ordinary skill would have been motivated to combine the Umemoto publication with the other references.

Respondents specifically addressed the question of motivation in their main post-hearing brief. They argue that inasmuch as the Soeda and Kamioka patents/publications disclose a wiring arrangement for first and second ESD protection devices, it would have been obvious to one skilled in the art at the time of the alleged invention of the '352 patent that the ESD protection devices of Umemoto could be substituted for the ESD devices described in the Soeda and Kamioka publications. The motivation to combine the teachings of the Soeda or Kamioka

publications with the teachings of the Umemoto patent, Respondents argue, is provided in the patents themselves: The Soeda publication describes a circuit that has first and second input protection devices, and it would have been obvious to one skilled in the art that any ESD protection device (e.g., the protection device of the Umemoto publication) could be substituted for the protection devices of the Soeda publication. Similarly, in the Kamioka publication, two ESD protection devices are connected in a particular circuitry without regard to the structure of the ESD protection devices. One skilled in the art would have understood at the time of the alleged invention of the '352 patent that any ESD protection devices could have been substituted for the generic ESD protection devices of Kamioka. Respondents argue moreover that in the Umemoto publication, it is expressly stated that the conventional LDD structure is "widely used in highly integrated MOS type semiconductor integrated circuits" and that "the electrostatic breakdown withstand voltage of a LDD structure MOS type semiconductor integrated circuit can be increased," thus motivating one to expand the application of the Umemoto disclosure. Respondents' Post-Hearing Brief (Following the November Hearing) at 4-5 (citing RPFF 232-254; RX-18, Umemoto translation, pp. 2, 4). Inasmuch as the Umemoto publication expressly discloses that its ESD protection device can be used to increase the breakdown withstand voltage of the "widely used" MOS type semiconductor integrated circuits and because Umemoto does not disclose any particular circuitry, it is implicit from Umemoto's text that it would have been obvious to one skilled in the art that the Umemoto ESD protection device can be used widely in any ESD protection circuitry such as is shown in either Soeda or in Kamioka. *Id* at 4 (citing *Pro-Mold and Tool Co., Inc. v. Great Lakes Plastics, Inc.*, 75 F.3d 1568, 1573 (Fed. Cir. 1996)("the reason to combine arose from the very nature of the subject matter involved") and *Para-*

Ordnance Mfg., Inc. v. SGS Imps. Int'l, Inc., 73 F.3d 1085, 1090 (Fed. Cir. 1995), *cert. denied*, 519 U.S. 822 (1996)(suggestion or motivation to make the claimed invention "leaps at the person of ordinary skill in the art")).

The arguments made by Respondents concerning the motivation to combine the Umemoto publication with the Soeda or the Kamioka publication are persuasive. Notwithstanding the testimony of Complainants' expert, the Umemoto publication (which forms the basis of a Japanese patent) by its plain language motivates one to expand the application of the invention beyond the scope of the particular embodiment depicted therein. The portion of the Umemoto publication quoted by Respondents is, as follows:

> (Effect)
> With this invention, the electrostatic breakdown withstand voltage of a LDD structure MOS type semiconductor integrated circuit can be increased, without causing a deterioration in the properties of the integrated circuit, which has major practical implications.

RX-18 at 4.

Thus, a person of ordinary skill in the art is expressly told that one could increase the effect of the invention disclosed in the Umemoto publication without deterioration and with major practical implications (or practical effect). While the Umemoto publication does not contain an additional disclosure or claimed invention, the Umemoto publication invites one to go to the art and to find the necessary information needed to effect such an increase. Indeed, the hypothetical person of ordinary skill in the art is charged with knowledge of all the contents of the relevant prior art. The scope of the relevant prior art includes that which is reasonably pertinent to the particular problem with which the inventor was involved. *In re Carlson*, 983 F.2d 1032, 1037 (Fed. Cir. 1992). Therefore, the prior art relevant to an obviousness

determination necessarily encompasses not only the field of the inventor's endeavor but also any analogous arts. *In re GPAC*, 57 F.3d 1573, 1577-78 (Fed. Cir. 1995)(citing *Heidelberger Druckmaschinen v. Hantscho Commercial*, 21 F.3d 1068, 1071 (Fed. Cir.1994)("References that are not within the field of the inventor's endeavor may also be relied on in patentability determinations, and thus are described as 'analogous art', when a person of ordinary skill would reasonably have consulted those references and applied their teachings in seeking a solution to the problem that the inventor was attempting to solve.")).

In this case, knowledge of the Soeda and the Kamioka publications must be imputed to the hypothetical person of ordinary skill, who has been found in this case to be a highly skilled individual.[29] The necessary disclosures which make claim 8 of the '352 patent obvious in conjunction with the Umemoto publication are found in both the Soeda publication and the Kamioka publication. *See* Peltzer Tr. 776-779.

Therefore, it has been demonstrated by clear and convincing evidence that claim 8 of the '352 patent is invalid for obviousness due to the Umemoto publication in view of the Soeda publication, and due to the Umemoto publication in view of the Kamioka publication.

3. Alleged Obviousness of Claims 1 and 2 over the Yasui Publication; Alleged Invalidity of Claim 8 over the Soeda Publication or the Kamioka Publication in View of the Yasui Publication

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[29] *See Ruiz v. A.B. Chance Co.*, 234 F.3d 654, 662-63 (Fed. Cir. 2000)(citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966)(the level of ordinary skill in the art must be determined in deciding a question of obviousness). As detailed, *supra*, in the section on claim construction, the Administrative Law Judge rejected Respondents' proposal for the definition of one of ordinary skill in the art relating to the '352 patent in favor of a definition based primarily on the proposal made by Complainants, which requires advanced education, such as a master's degree in a relevant field, and substantial experience.

Respondents argue that if Complainants' proposed claim construction were adopted for the '352 patent, claims 1 and 2 of the '352 patent would be anticipated by the Yasui publication. Complainants's proposed claim construction has not been adopted, thus Respondents' argument in this regard is moot. Respondents' Post-Hearing Brief (Following the November Hearing) at 6.

Respondents also argue in their main post-hearing brief that if their proposed claim construction is adopted and the "key element 36"[30] of the '352 patent must be under both the source region and the drain region of the ESD protection device, claims 1 and 2 would be obvious in view of the teachings of the Yasui publication, and that claim 8 is invalid over the teachings of the Soeda patent/publication or the Kamioka patent/publication in view of the patent/publication. *Id.* (citing RPFF 200-231). In particular, it is argued that Yasui discloses an LDD structure in which the common drain between two gates includes a p-type region centered under the heavily doped n+ region, and that in this way, the Yasui ESD is like the Complainants' ESD devices and like the SiS new E5, the SiS E6 and the SiS E7 model ESD transistors. *Id.* at 6 (citing RPFF 216-231).

The Commission Investigative Staff argues that the Yasui publication does not teach every element of claim 1 of the '352 patent, and does not join in Respondents' arguments

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[30] Respondents refer to the use of the term "key element" in the '352 patent specification, which states:

> A cross-sectional representation of the FIG. **8** circuit, and connections, is shown in FIG. **9**, wherein similar elements from earlier figures are given the same numbers. The key element of the lightly doped P- regions **36** are shown, and provide the lower junction breakdown voltage and subsequent improved ESD characteristics of the invention.

CX-2/RX-1 ('352 Patent), col. 4, lines 62-67.

concerning the Yasui publication in combination with the Soeda or Kamioka publication to invalidate claim 8 of the '352 patent for obviousness. *See* OUII Post-Hearing Brief (Following the November Hearing) at 17-18.

Complainants argue that claims 1 and 2 of the of the '352 patent are not made obvious by the Yasui publication and claim 8 is not obvious by combining the Yasui publication with the Soeda publication or the Kamioka publication. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 40-43. In particular, Complainants argue that Respondents' expert conceded that claim 1 of the '352 patent does not read on the Yasui publication, and that connecting the structure in the Yasui publication to the electrical connections in the Soeda or Kamioka publication would cause the transistor to be constantly turned on so that it would not function as an ESD protection transistor.[31] Complainants argue, moreover, that Respondents have failed to identify any evidence of a motivation or suggestion to combine these references. Complainants' Post-Hearing Reply Brief (Following the November Hearing) at 31-32 (citing CPFF 835, 867, 869-870, 879-881).

The record concerning the Yasui publication's disclosures is not as clear as that relating to the Umemoto publication, especially with respect to the motivation to combine the reference with other prior art such as the Soeda publication or the Kamioka publication. Consequently, it is not found by clear and convincing evidence that claim 1 or claim 2 of the '352 patent is obvious in view of the Yasui publication, or that claim 8 is obvious in view of the Yasui

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[31] The proposed findings of fact cited by Complainants to support this supposed admission by Respondents' expert are CPFF 867 and 879. Complainants' Post-Hearing Reply Brief (Following the November Hearing) at 32. However, those proposed findings of fact cite to the hearing testimony of Complainants' expert, and furthermore do not directly support the substance of Complainants' statement.

publication in combination with either the Soeda publication or the Kamioka publication.

4. Alleged Invalidity of Claim 8 over the Yasui Publication in View of the Soeda Publication

To argue that claim 8 of the '352 patent is invalid over the Soeda publication in view of the Yasui publication, and separately under a second heading to argue that claim 8 is invalid over the Yasui publication in view of the Soeda publication, as Respondents have done in their main post-hearing brief (*see* Respondents' Post-Hearing Reply Brief (Following the November Hearing) at 6-7), is essentially to argue the same contention twice.

Respondents argue that claim 8 of the '352 patent requires both gates to be grounded while the Yasui publication Figure 1 (A) shows only one of the gates to be grounded. The Soeda publication teaches that both gates of the two nMOS devices can be grounded in an ESD structure, satisfying the condition that both transistors be biased off in normal operation. Thus, Respondents argue, that it would have been obvious to one skilled in the art at the time of the alleged invention to use grounded gates on the two NMOS devices considering the Yasui publication in view of the Soeda publication. Respondents' Post-Hearing Reply Brief (Following the November Hearing) at 7 (citing RPFF 244-254).

Nevertheless, the deficiencies addressed above concerning the Yasui publication remain. It is not clear that one of ordinary skill in the art would draw the same conclusions about the combination of the disclosure from the Yasui and Soeda publications that Respondents have drawn in their brief. Consequently, the Administrative Law Judge declines to find that a combination of the Yasui publication and the Soeda publication makes claim 8 of the '352 patent invalid for obviousness.

5. Conclusions on the Issue of Obviousness

The record establishes by clear and convincing evidence that claim 8 of the '352 patent is invalid as obvious in view of the Umemoto publication and either the Soeda publication or the Kamioka publication. It has not been established by clear and convincing evidence that claim 1, 2 or 8 of the '352 patent is obvious in view of any other single item, or combination of prior art.

V. INFRINGEMENT OF THE '345 PATENT

As discussed in Section III (relating to the '352 patent), a finding as to infringement or non-infringement requires a two-step analytical approach. First, the claims of the patent must be construed to determine their scope. Second, a determination must be made as to whether the properly construed claims read on the accused device. *See Markman*, 52 F.3d at 976.

A. Claim Construction

Based on the statements contained in the complaint, the notice of investigation would cover allegations that Respondents infringe any or all of claims 1, 3-16, or 19-21 of the '345 patent. However, in their post-hearing filings, Complainants asserted a smaller subset of '345 patent claims against Respondents, i.e., claims 1, 3-5, 9, 11-13, and 20-21. *See* Complainants' Proposed Conclusions of Law for Hearing Completed November 16, 2001 at 13-14; Complainants' Proposed Conclusions of Law for Hearing Completed December 12, 2001 at 2-3. The asserted claims of the '345 patent are as follows:

> **1.** A method for forming conducting structures separated by gaps on a substrate, comprising:
>
> providing a substrate and a wiring line layer above the substrate;
>
> forming a first antireflective coating on the wiring line layer;

forming a second antireflective coating on the first antireflective coating, wherein the first antireflective coating and the second antireflective coating are formed from different materials;

forming a mask layer above the second antireflective coating, wherein the mask layer covers selected portions of the second antireflective coating and exposes other portions of the second antireflective coating;

etching the first antireflective coating, the second antireflective coating, and the wiring line layer, at the location where the second antireflective coating is exposed by the mask layer, to form wiring lines separated by gaps; and

depositing a dielectric material within the gaps to fill the gaps, using high density plasma chemical vapor deposition.

3. The method of claim **1**, wherein the mask layer is a patterned photoresist layer.

4. The method of claim **1**, wherein a portion of the second antireflective coating is etched during the high density plasma chemical vapor deposition.

5. The method of claim **1**, further comprising the formation of a surface layer between the substrate and the wiring line layer, the surface layer being a barrier between the substrate and wiring line layer.

9. A method for forming conducting structures separated by gaps on a substrate, comprising:

providing a substrate and a wiring line layer above the substrate;

forming a cap layer above the wiring line layer;

forming a mask layer above the cap layer, wherein the mark [sic] layer covers selected portions of the cap layer and exposes other portions of the cap layer;

etching the cap layer, and the wiring line layer, at the locations where the cap layer is exposed by the mask layer, to form wiring lines

separated by gaps, the wiring lines having a remaining portion of the cap layer thereon; and

depositing a dielectric material within the gaps at a sputtering rate sufficient to fill the gaps, using high density plasma chemical vapor deposition.

11. The method of claim **9**, wherein the cap layer is an antireflective coating.

12. The method of claim **9**, wherein the remaining portion of the cap layer is partially etched during the deposition of a dielectric material using high density plasma chemical vapor deposition.

13. The method of claim **9**, wherein the cap layer comprises a material selected from the group consisting of a silicon nitride material and an oxynitride material.

20. The method of claim **9**, wherein the mask layer is a patterned photoresist layer.

21. A method for forming conducting structures separated by gaps filled with dielectric material, comprising the steps of:

providing a substrate containing silicon, the substrate having a surface;

forming a surface layer comprising at least one material selected from the group consisting of titanium nitride, titanium suicide [sic] and a titanium-tungsten alloy, the surface layer disposed on the substrate surface;

forming a metal wiring layer on the surface layer, the metal wiring layer having an upper surface;

forming a protective layer comprising at least one material selected from the group consisting of titanium nitride, titanium silicide and a titanium-tungsten alloy, the protective layer disposed on the upper surface of the metal wiring layer, the protective layer having a top surface;

forming a cap layer comprising at least one material selected from the group consisting of an oxide, a nitride, and an oxynitride, the cap

layer disposed on the top surface of the protective layer;

forming a patterned photoresist layer above the cap layer, said patterned photoresist layer covering selected portions of the cap layer and exposing other portions of the cap layer;

etching the exposed portions of the cap layer, the protective layer and the metal layer to form wiring lines separated by gaps; and

forming a layer of high density plasma chemical vapor deposition dielectric material within the gaps to fill the gaps.

CX-1/RX-40 ('345 Patent).

These claims must be construed as one of ordinary skill in the art would do so. Respondents' expert, Mr. Peltzer, testified that a person of ordinary skill in the art relating to the '345 patent would have a B.S. or an M.S. degree in electrical engineering, physics, chemical engineering or metallurgy. Peltzer Tr. 791. Complainants' expert, Dr. Fair, testified that around 1997,[32] one of ordinary skill in the art would have had at least a master of science degree in electrical engineering or chemical engineering or chemistry or physics, with substantial experience in semiconductor device processes. Fair Tr. 138. Dr. Fair's opinion requires the application of a higher standard than that described by Mr. Peltzer. Dr. Fair explained that his requirement of a more advanced degree and substantial experience is based on his personal experience in the semiconductor industry, including the hiring and training of persons to work in the field. Fair Tr. 138-139. Based on the testimony of the expert witnesses, and the technically complicated record relating to the '345 patent, it appears that more would be required of one or ordinary skill than merely a bachelor's or master's of science degree. Thus, it is found that one

[32] The '345 patent entitled "High Density Plasma Chemical Vapor Deposition Process" issued on September 12, 2000, based on an application filed in 1997.

of ordinary skill in the art, for the purposes of the '345 patent, is a person with at least a master's degree in electrical engineering, physics, chemistry, chemical engineering or metallurgy, with substantial experience in semiconductor device processes.

There is no dispute that in general the '345 patent covers a method for depositing dielectric material into gaps between wiring lines in the formation of a semiconductor device, including the formation of a cap layer and the formation of gaps into which high density plasma chemical vapor deposition (HDP CVD) dielectric material is deposited. *See, e.g.*, RX-40 ('345 Patent), Abstract; Fair Tr. 142-143; Peltzer Tr. 791-801. However, questions concerning the meaning of numerous terms found in the asserted claims are raised in the parties' briefs.[33] Several of those terms are common to the arguments of all parties, and are of sufficient significance to be discussed individually below.

(i) wiring line layer

Complainants argue that "wiring line layer" means a layer that may be formed from a variety of materials, such as aluminum, aluminum alloyed with silicon or copper, copper, alloys including copper and multilayer structures including comparatively inexpensive metals and more expensive metals such as the refractory metals. It is argued that titanium is a refractory metal, and a titanium layer is part of the wiring line layer when present. Complainants reject any proposal that the wiring line layer be made of polysilicon. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 12 (citing CPCL 12 and CPFF 310-15); CPCL 12 (citing CPFF 310-15).

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[33] The parties' briefs relating to the '345 patent consist of those filed in connection with both the November and December, 2001 proceedings.

Respondents argue that "wiring line layer" means a polysilicon or aluminum-based metal layer that can be etched to form conducting structures for interconnecting regions within devices and for interconnecting one or more devices within the integrated circuits. It is argued that the "wiring line layer" is the conductive material, e.g., aluminum/copper alloy, and does not include layers of materials such as titanium (Ti) or titanium nitride (TiN) that have other functions. Respondents' Post-Hearing Brief (Following the November Hearing) at 18 (citing '345 Patent, Col. 1, lines 16-29; RPFF 399-402; RPCL 44).

The Commission Investigative Staff argues that the '345 specification (at col. 7, lines 3-7) provides that the "wiring line layer" may be formed from a variety of materials, such as (1) aluminum, (2) aluminum alloyed with silicon or copper, (3) alloys including copper, or (4) multilayer structures that include inexpensive and more expensive materials such as refractory metals. The Staff argues that any construction limiting the "wiring line layer" to polysilicon is not supported by the intrinsic evidence, and that Respondents' contention that the wiring line layer necessarily excludes titanium or titanium nitride is not supported by the intrinsic or extrinsic evidence. The Staff argues that Respondents' argument is contrary to the testimony of their expert witness, and that the '345 specification clearly teaches that the "wiring line layer" may be formed from expensive materials such as refractory metals, an example of which is titanium. OUII Post-Hearing Brief (Following the November Hearing) at 23-24 (citing CX-1, col. 7, lines 3-7; Fair Tr. 146; Peltzer Tr. 870, 872, 878-880).

The specification of the '345 patent, including its discussion of a particular preferred embodiment, explicitly teaches that the wiring line "may be formed from a variety of metals, such as aluminum, aluminum alloyed with silicon or copper, copper, alloys including copper and

multilayer structures including comparatively inexpensive metals and more expensive metals such as refractory metals." CX-1/RX-40 ('345 Patent) at col 7, lines 4-8. The expert testimony, including that of Respondents' expert witness, demonstrates that titanium is such a refractory metal.[34] *See, e.g.*, Peltzer Tr. 887-880. Thus, without deciding whether titanium is suitable for

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[34] Mr. Peltzer testified:

> Q Now, in your proffered construction, you said titanium wiring line layer does not include -- wiring line layer does not include titanium. That's an affirmative statement. Can you show me, anywhere in the specification or the claims, support for your affirmative statement that wiring line layer does not include titanium?
>
> A Well, the embodiment which is taught here shows on this column 7 that the refractory metal can be included as part of the wiring line layer. But again, as I go back to this first part here and I look at the heading of this entire section, it's the description of the preferred embodiments, and *I will certainly agree with you that the titanium being part of the wiring line is an embodiment.*
>
> Q Mr. Peltzer, you misunderstand. You are offering an affirmative statement to the Court. The wiring line layer does not include titanium. My question is, where do you find support for your affirmative statement in either the claims or specification that the wiring line layer does not include titanium?
>
> A Let's see, I am trying to understand the difficulty here. The situation, as I see it, is the situation in which the wiring line layer has titanium in it, is an embodiment. And then on the other hand, you understand from knowledge of titanium that when you look at the surface of a wafer coated with titanium, it reflects less than the aluminum layer. And that I could then use the titanium layer as an antireflective coating.
>
> In such an instance, then, the titanium layer that moves out of the description of the preferred embodiment here into a description in which we have the wiring line, which is the aluminum or aluminum/copper, and now a titanium layer because [sic in Tr., "became"] the first antireflective coating.
>
> Q Let's go back to page 1 of the CPX-5, the wiring line layer construction. So Mr. Peltzer, would you agree that in the preferred embodiment, the wiring line layer can and does include titanium?

(continued...)

[34] (...continued)

A Well, it includes a refractory metal, as described here in this column 7.

Q And titanium is a refractory metal?

A Yes, I agree.

Q So that certainly, to rule out titanium as part of the wiring line is not support by the patent; right? There's a flat-out ban on titanium being considered part of the wiring line layer is contrary to the specification; correct?

A Would you repeat that? I followed you a little bit but I lost you.

Q I'm looking again at your affirmative statement which says in effect, under all circumstances, the wiring line layer does not include titanium. Would you agree that that's not a correct statement, as set forth in the specification and claims of this patent?

MR. HOVANEC: Your Honor, could I ask that there be only one question? I'm not sure which question is put to this witness.

JUDGE HARRIS: Well, I think the witness understands now. But I think to be fair here, I think what he said is that it's just another embodiment. I don't think he said that by saying that it is the preferred embodiment, you're not ruling out under all circumstances that it would be part of the wiring line layer.

MR. KIKEL: I certainly understand, your Honor, although I haven't had any identification of any other embodiment in the specification. The point that I was trying to address with the question, though, is that to the extent that SiS is offering a construction which says it cannot include titanium in the wiring line layer, that's certainly contradicted by the preferred embodiment.

JUDGE HARRIS: Why don't you ask the next question.

BY MR. KIKEL:

Q Let me just ask one cleanup and we'll move on to the next construction, because I don't want to spend too long here. Under the preferred embodiment, titanium would be included as part of the wiring line layer since it is a refractory metal; correct?

A In column 7, it specifically states that a refractory metal can be used, yes. This

(continued...)

any particular embodiment of the claimed invention, there is no basis upon which to limit the wiring line layer to a polysilicon or aluminum-based metal in all instances, or to exclude completely titanum or layers containing titanium.

(ii) antireflective coating

Complainants argue that "antireflective coating"[35] means a layer that provides antireflective functionality by one of two primary means: destructive interference or absorption. It is argued that if the coating's antireflective functionality is primarily based on destructive interference (i.e., forming a quarter wave plate), then its thickness must be set at an appropriate multiple of one quarter of the wavelength of the exposure light, taking into account the dielectric constant of the material, and minor variations from the quarter wave plate thickness are permitted. However, it is argued, that if the coating's antireflective functionality is primarily based on absorption, then its thickness and absorption must be sufficient to cause a measurable reduction in the amount of light passing through the antireflective coating and reflecting from the layer on which the antireflective coating resides. *See* CPCL 13 (citing CPFF 316-25).

Respondents argue that "antireflective coating" means a layer which significantly reduces or completely eliminates the reflectivity of light as compared to the layer on which the antireflective coating resides. Respondents' Post-Hearing Brief (Following the November

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[34] (...continued)
is a location in which titanium as a refractory metal can be put in a wiring line in that preferred embodiment.

Peltzer 877-880 (emphasis added).

[35] The term "antireflective coating" is referred to frequently in the parties' briefs, and occasionally in this Initial Determination as "ARC."

Hearing) at 17 (citing CX-1/RX-40 ('345 Patent), col. 7, lines 10-17, col. 7, line 58 - col. 8 line 32; RPFF 388-396; RPCL 42). Contrary to perceptions of the other parties, Respondents do not propose that "antireflective coating" be limited to absorption. However, consistent with their general arguments concerning "antireflective coating," Respondents argue that the claim language, "works by absorption" means an antireflective layer that works by absorbing light transmitted during the exposure of the photoresist to light, and that "works by interference" means an antireflective layer that acts as a quarter wave plate to create destructive interference to prevent light from reflecting up to the photoresist layer. Respondents' Post-Hearing Brief (Following the November Hearing) at 18 (citing CX-1/RX-40 ('345 Patent), col. 7, lines 33-51, lines 58-67; RPFF 403-407; RPCL 45-46).

The Commission Investigative Staff argues that the '345 specification provides that antireflectiveness can be carried in at two least different ways: either by (1) destructive interference, or (2) absorption. The Staff argues that Respondents' proposed claim construction covers only one of these anti-reflective means, namely absorption, and should be rejected. It is argued that while Respondents contend that the antireflective coating should be construed as a coating that "significantly reduces or completely eliminates the reflectivity of light as compared to the layer on which the antireflective coating resides," the claims do not contain these limitations; that the '345 patent does not teach that the antireflective coating "significantly reduces" or "completely eliminates" light; and that instead, the claims merely provide that, in at least one embodiment, the antireflective coating is to be absorptive. In addition, the Staff argues, the '345 patent does not teach that the coating's antireflectiveness is a function of the reflectivity of the layer beneath it. OUII Post-Hearing Brief (Following the November Hearing) at 24-25

(citing CX-1/RX-40 ('345 Patent), col. 7, line 11 - col. 8, line 32; Fair Tr. 150-153 (extent or magnitude of absorption not specified in claims)).

There is no dispute that an antireflective coating may work by absorption or interference, and there is support for that contention in the '345 patent. For example, claim 2 of the '345 patent explicitly covers, "[t]he method of claim **1**, wherein the first antireflective coating works by absorption, and the second antireflective coating works by interference. *See* CX-1/RX-40 ('345 Patent), col. 10, lines 28-31. Furthermore, there appears to be agreement that to work by interference means an antireflective layer that acts as a quarter wave plate to create destructive interference to prevent light from reflecting up to the photoresist layer. In any event, there is ample support in the specification for such a construction, based upon the knowledge of one of ordinary skill in the art.[36] *See* CX-1/RX-40 ('345 Patent), col. 7, line 58 - col. 8, line 14.

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[36] The '345 patent specification states in pertinent part:

> The cap layer **28** may serve a number of functions. During the exposure of the photoresist layer to light to shape the mask prior to etching, the cap layer may be used as a quarter wave plate in order to prevent light from passing through the cap layer and reflecting back up to the photoresist layer and causing the photoresist layer to become exposed in regions that are supposed to remain unexposed. Rather than absorbing light like the protective layer **26**, the quarter wave plate creates destructive interference to prevent light from reflecting up to the photoresist layer. Those of ordinary skill in the art will appreciate that the particular thickness of layer **28** to be provided when layer **28** has its preferred function as a quarter wave plate is different for different materials. The preferred thickness for layer **28** can be determined by setting the thickness to be one quarter of the wavelength of the exposure light taking into account the dielectric constant of the material in layer **28** at the wavelength of the exposure light. More generally, the thickness may be set so that twice the thickness of the layer **28** is an odd number of half wavelengths of the exposure light, taking into account the dielectric constant of the material. It should further be appreciated that minor variations from the optimal thickness of layer **28** as a quarter wave plate will typically be effective in reducing reflectivity, although less effectively.

(continued...)

There is a variance among the proposed constructions concerning the term and the concept of "absorption" and, in general, what it means to call a coating "antireflective."[37] As stated above, Complainants argue that if the coating's antireflective functionality is primarily based on absorption, then its thickness and absorption must be sufficient to cause a *measurable* reduction in the amount of light passing through the antireflective coating and reflecting from the layer on which the antireflective coating resides. Respondents argue that *any* antireflective coating must *significantly reduce* or *completely eliminate* the reflectivity of light as compared to the layer on which the antireflective coating resides. At the outset, common sense would suggest that Complainants' and Respondents' definitions of what "antireflective" means are not far apart. However, Complainants' proposal (which would require only a *measurable* reduction in the amount of light passing through the coating and reflecting from underneath) may leave open the possibility that coatings which for all practical purposes serve no antireflective purpose or function whatsoever might be called "antireflective coatings" merely because someone could *measure* some small decrease in light. Furthermore, Complainants' proposal for when a coating that works by interference may properly be called "antireflective" remains unclear.

The problem that is addressed by the use of antireflective coatings is stated plainly in the '345 specification:

> Reduced design rules for forming integrated circuit devices have

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[36] (...continued)
CX-1/RX-40 ('345 Patent), col. 7, line 58 - col. 8, line 14.

[37] The differences between Complainants' and Respondents' positions on this point appear to be minimized in Respondents' reply brief. *See* Respondents' Post-Hearing Reply Brief (Following the December Hearing) at 9-10. However, the variances are important and are addressed herein.

> necessitated the use of photolithography steppers that use short wavelength exposure sources. Such short wavelength exposure sources allow for finer resolution lithography, but have the drawback of much higher levels of reflection from different components of the integrated circuit device. For example, *during exposure of the photoresist mask, it is possible that light may pass entirely through the photoresist and reflect from the surface of the first metal layer back into the lower portions of the photoresist layer.* To the extent that the reflected light is scattered by the surface of the first metal layer, it is possible that unwanted portions of the photoresist layer might be exposed. These unwanted reflections could undesirably narrow the first level metal wiring lines formed in this process.

CX-1/RX-40 ('345 Patent), col. 1, line 58 - col. 2, line 5 (emphasis added).

Thus, Respondents' proposed construction that "antireflective coating" means a layer that *significantly* reduces or *completely* eliminates the reflectivity of light as compared to the layer on which the antireflective coating resides is a helpful definition, whether the antireflective result is effected by absorption or interference. The words *significantly or completely* do not appear in the claim language, and other words might be substituted to explain the nature of an antireflective coating. There is no need or basis for attempting to add those particular words to the claim language. The patent specification discusses embodiments of the invention in terms of reducing reflectivity, without the use of qualifiers such as "measurable" or "significantly." *See* CX-1/RX-40 ('345 Patent) at col 8, lines 24-32. Nevertheless, it is reasonable to expect that the antireflective effect of a coating, whether through absorption or interference, must be significant to the purposes of the invention in order for that coating to satisfy the claim limitation and to be described as "antireflective."

Closely related to the arguments concerning the meaning of "antireflective coating" are arguments made by Respondents in their post-hearing brief following the December, 2001

hearing, in which they argue that a competitor looking at the '345 patent would understand that the term "different materials" used with respect to "the first and the second antireflective coating" in independent claim 1 means that there should be, at the least, a difference between metal and non-metal components. Respondents rely on the fact that no special definition of "different materials" is provided in the '345 patent, and the fact that the specification teaches that the first antireflective layer -- the layer **26** -- is disclosed as titanium nitride, titanium-silicide, or a titanium-tungsten alloy, while the second antireflective layer -- the layer **28** -- is disclosed as silicon nitride or oxynitride. Respondents' Post-Hearing Brief (Following the December Hearing) at 10-11 (citing CX-1/RX-40 ('345 Patent), col. 6, lines 60-65 and col 7 lines 10-11, 31-33; Peltzer Tr. 1178-1181).

In their reply following the December, 2001 hearing, Complainants argue that Respondents rely on a simplistic approach taken by their expert at the hearing, i.e., [

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Complainants argue that one of ordinary skill in the art would understand the term "different materials" in the '345 patent to be focused on the different chemical compounds formed from atoms and the differences in the properties of compounds. Complainants present specific data relevant to products accused in this investigation and to the details of an infringement analysis.[38] *See* Complainants' Post-Hearing Reply Brief (Following the December Hearing) at 15 (citing

[38] Complainants argue that certain accused products have a second antireflective coating on" a first antireflective coating. However, those arguments are couched in terms of the infringement analysis, rather than claim construction. Complainants' Post-Hearing Reply Brief (Following the December Hearing) at 18-19.

CPFF 1196, 1203).

The Commission Investigative Staff, with respect to the term "different materials," argues that Respondents merely assume that because one teaching of the '345 patent states that the "first antireflective coating" (item 26) *may* be titanium nitride, titanium silicide, or titanium-tungsten alloy (*see* CX-1/RX-40, col. 6, lines 60-65) and the "second antireflective coating" (item 28) *may* be silicon oxide, silicon nitride, or oxynitride, competitors would understand "different materials" to be a difference between metal and non-metal components. The Staff argues that Respondents attempt to create limitations that are not present in the specification, and to import them into the claims. The Staff argues that the '345 patent specification does not contain any teaching that provides that "different" materials requires a difference between metal and non-metal components. OUII Post-Hearing Reply Brief (Following the December Hearing) at 5-6 (The Staff also presents argument relevant to infringement determinations).

Although Respondents clearly rely on the teachings of the '345 patent specification to propose a construction for the term "different materials," no party argues that the '345 patent specification provides a specific definition of the term "different materials" or the word "different"(i.e., to quote a term of art, with respect to which the patentees have sought to be their own lexicographers). The dispute among the parties concerning the term "different materials" centers primarily around the word "different" (e.g., need the materials involved be metal and non-metal, or need they simply exhibit different characteristics, and if so, how different?).

A standard dictionary definition of the word "different" shows that the word conveys two main ideas that are relevant to this discussion: "**1:** partly or totally unlike in nature, form, or quality . . . : having at least one property not possessed by another . . . **2 :** not the same : distinct

or separate (from another or from others is a group) . . . ." WEBSTER'S THIRD NEW INTERNATIONAL DICTIONARY OF THE ENGLISH LANGUAGE UNABRIDGED 630 (1976)("Webster's Unabridged"). Indeed, one may refer to something as "different" whenever there is a single property not possessed by another. Thus, two things that are not exactly alike may be said to be "different." Yet, the word "different" may also be used to covey the idea that two things are appreciably "distinct" or "separate."

In the case of the "different materials" required for the antireflective coatings of the '345 patent, it appears that to some extent all parties would favor the latter meaning (i.e., conveying the distinctiveness or separateness), or if the former meaning is preferred, that the definition of "different" in this instance should stress how "unlike" the antireflective coatings are in nature or quality. For example, Respondents rely on a preferred embodiment of the specification to argue that the '345 teaches that the antireflective coating must be as "different" as metal versus non-metal. Complainants reject that metal versus non-metal limitation, yet in bridging the gap between proposed claim construction and infringement analysis, their briefing relies on scientific evidence to argue that there are "substantial differences in chemical composition, density, resistivity and optical properties" in the alleged first and second antireflective coatings used in the accused processes. *See, e.g.*, Complainants' Post-Hearing Brief (Following the December Hearing) at 5-9. No party argues that the antireflective coatings may be said to be of "different materials" due to slight or insignificant divergences in form, nature or function. The applicants would not have specified "different materials" in their claim language to include materials that are substantially alike. A construction which requires "different materials" to exhibit significant, if not substantial (in Complainants' words), differences in chemical composition and relevant

properties (such as resistivity) is supported by the specification, which teaches that the purpose of using different materials for layers 26 and 28 in a preferred embodiment is to augment the effect of using just one layer. *See* CX-1/RX-40 ('345 Patent), col. 7, line 58 - col. 8, line 32 (containing the discussion relied on by Respondents). Thus, there is utility to using two layers comprised of "different materials," and a clear reason for the applicants to place such a limitation in the claim language.

Respondents also argue that for the purposes of an infringement analysis, the word "on" (as used in the phrase "forming a second antireflective coating on the first antireflective layer") means adjacent to and above, and does not mean "in." It is argued that the word "on" is not given any special meaning in the '345 patent, and thus must be given its ordinary meaning. *Id.* at 11-13.

Complainants argue that the '345 patent does not provide a special definition of the word "on" or the word "in." Furthermore, it is argued that Dr. Fair, Complainants' expert, testified that the word "on", as used in the third element of claim 1 of the '345 patent, means "above" or "in contact with." Complainants criticize Respondents for raising this issue in their briefing. However, especially as seen below in the summary of the Commission Investigative Staff's arguments concerning the word "on," the use of this simple word in the claim language is in need of clarification. Complainants' Post-Hearing Reply Brief (Following the December Hearing) at 7-8 (citing CPFF 1167).

The Commission Investigative Staff argues that there is nothing in the '345 patent specification or prosecution history that provides that the term "on" or "above," as used in the 'the '345 patent excludes "in." The Staff argues that as long as the second antireflective coating

is "on" or "above" the first layer, independent claims 1, 9 and 21 are infringed, whether or not the second antireflective coating is also "in." OUII Post-Hearing Reply Brief (Following the December Hearing) at 3-5.

Although the Staff does not rely primarily on a dictionary definition of the term "on," it nevertheless quotes such a definition for additional support of its proposed claim construction. In particular, the Staff argues that "on" has the following meanings: "(1) '*in* or into a position of contact with an upper surface' and (2) '*in* or into a position of being attached to or covering a surface.'" OUII Post-Hearing Reply Brief (Following the December Hearing) at 5 (quoting WEBSTER'S NEW COLLEGIATE DICTIONARY at 824 (9th ed. 1985)("Webster's Collegiate")(emphasis in original Staff reply brief).

The Staff emphasizes the dictionary definition's use of the word "in" when defining the word "on." The Staff, however, misinterprets the quoted definition. The quoted definition defines "on" as having the characteristic of being "*in*" a particular "*position*" -- i.e., a "position of contact" with an upper surface, or "in" a "position" of being attached to or covering a surface. The term "in" as used in this dictionary definition does not state or suggest that something is located "on" something else by virtue of being *in contact* with an upper surface and at the same time *in the upper surface* or *in* the structure that has an upper surface. The state of being *in a position of contact* with an upper surface and being *in an upper surface* are two very different concepts and indeed physical locations. Similarly, this definition does not state or suggest that something is located "*on*" something else by virtue of covering a surface, and yet also exists in the covered surface or in the structure that has a surface. A proposed interpretation that would combine or confuse "on" with "in" cannot be adopted with respect to the '345 patent.

Indeed, the claim language and the discussion of the preferred embodiments of the '345 patent supports use of the common understanding of the term "on." The plain language of claim 1 requires "forming a first antireflective coating on the wiring line layer" and in a separate element, "forming a second antireflective coating on the first antireflective coating, wherein the first antireflective coating and the second antireflective coating are formed from different materials." Thus, a first antireflective coating and a second antireflective coating "are formed from different materials" – i.e., they have different origins; they are formed from different materials, not the same material – and one coating is placed "on" the other. Likewise, the specification teaches that the antireflective coatings are "*formed from* different materials" (as opposed to in or within one or the other), and further that a protective layer has surfaces, including a "top surface."

The processes and the physical properties described in the '345 patent specification support the placement of one antireflective coating "on" another in the usual sense that one object is said to be "on" another. *See, e.g.*, CX-1/RX-40 ('345 Patent), col. 3, line 22 - col. 4, line 8. Common dictionary definitions, including the dictionary definition quoted by the Commission Investigative Staff, when read carefully, are appropriate to construe the word "on."[39]

(iii) mask layer

Complainants argue that "mask layer" means a patterned layer for etching, and claim 1 of the '345 patent does not limit the mask layer to a patterned photoresist layer. *See* CPCL 14

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[39] The definition of "on" in Webster's Collegiate, as quoted by the Commission Investigative Staff, is nearly identical to the primary definitions for the word "on," when used as an adverb, contained in Webster's Unabridged (a dictionary quoted elsewhere in this opinion). *See* Webster's Unabridged at 1575.

(citing CPFF 326-28).

Respondents argue that "mask layer" means a patterned layer of photoresist for etching underlying exposed regions. Respondents' Post-Hearing Brief (Following the November Hearing) at 17 (citing '345 Patent, Col. 7, lines 37-45; RPFF 397-398; RPCL 43).

The Commission Investigative Staff argues that in view of the fact that claim 3 provides that the "mask layer is a patterned photoresist layer," "mask layer" should not be limited to a patterned layer of photoresist for etching underlying exposed regions. Such a limitation, it is argued, would render claim 3 superfluous. The Staff notes that the '345 patent specification provides that "*[a]lternatively*, the photoresist layer itself may be used as the mask for etching layers 28, 26, 24, and 22." CX-1/RX-40 ('345 Patent), col. 7, lines 42-45 (emphasis added). The Commission Investigative Staff relies in part on the Federal Circuit's opinion in *Xerox Corp. v. 3Com Corp.* 267 F.3d 1361, 1366-67 (Fed. Cir. 2001)("There is presumed to be a difference in meaning and scope when different words or phrases are used in separate claims. To the extent that the absence of such difference in meaning and scope would make a claim superfluous, the doctrine of claim differentiation states the presumption that the difference between claims is significant.")(quoting *Tandon Corp. v. United States Int'l Trade Comm'n*, 831 F.2d 1017, 1023 (Fed. Cir.1987)). OUII Post-Hearing Brief (Following the November Hearing) at 25-26.

The parties agree that a "mask layer"means, at least, a patterned layer for etching. That statement of what constitutes a mask layer is a simple yet adequate definition for the purposes of this investigation.

In the "Description of the Related Art," the '345 patent specification states that: "*Generally*, the etch mask is formed by providing a layer of photoresist on the surface of the first

metal layer, exposing the layer of photoresist through an exposure mask and developing the photoresist to form the etch mask." CX-1/RX-40 ('345 Patent), col. 1, lines 51-55 (emphasis added). Respondents would augment the simple definition of "mask layer" to require that the patterned layer in the '345 patent claims must be a layer of photoresist. Respondents' proposal is based on language in the '345 patent specification that discusses a preferred embodiment (*see* col. 7, lines 37-41; RPFF 397). There is no need or justification for reading that feature of a preferred embodiment into the independent claims of the patent as a limitation. It is further noted that claim 3 provides for "[t]he method of claim **1**, wherein the mask layer is a patterned photoresist layer." Thus, especially with respect to claim 1, it would be expected that the claim language "mask layer" should be broad enough to cover a mask layer made of photoresist, although one would not expect such a limitation to be read from dependent claim 3 into independent claim 1.[40]

(iv) cap layer

Complainants argue that "cap layer" means a layer that may serve a number of functions, including acting as an antireflective coating, a hard mask for metal line etching, and/or a

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[40] Similarly, Respondents argue that "acts as a mask" and "used as a hard mask" means that after etching the second antireflective coating, the photoresist mask layer is removed and the patterned second reflective coating is then used as a mask to etch exposed portions of underlying material. Respondents' Post-Hearing Brief (Following the November Hearing) at 17 at 18 (citing CX-1/RX-40 ('345 Patent), col. 7, lines 37-42, col. 8, lines 33-51). The portions of the specification cited by Respondents also relate to preferred embodiments, including an embodiment in which the cap layer **28** is used as a hard mask for wiring line etching. As in the case of the general term "mask layer," there is no indication that these aspects of preferred embodiments should be read into the claims. In addition, independent claim 9 calls for "forming a cap layer above the wiring line, and there is dependent claim 20, which specifically adds the limitation to "claim **9**, wherein the mask layer is a patterned photoresist layer." It would be redundant and unusual to read the limitation of claim 20 into claim 9.

protector for the top corners of metal wiring lines during the HDP CVD process. *See* CPCL 15 (citing CPFF 329-31).

Respondents argue that "cap layer" means a dielectric, insulating layer that may serve as an antireflective coating, a hard mask for metal line etching, and/or a protector for the top corners of metal wiring lines during the HDP CVD process. Respondents' Post-Hearing Brief (Following the November Hearing) at 17 (citing CX-1/RX-40 ('345 Patent), col. 4, lines 57-60; RPFF 369-387; RPCL 41).

The Commission Investigative Staff argues (based on col. 4, lines 57-60) that "cap layer" should be construed as a layer that serves several functions, including acting as (1) an antireflective coating, and/or (2) a hard mask for metal line etching, and/or (3) a protector for the top corners of the metal wiring lines during HDP CVD. The Staff argues that Respondents' proposal that the "cap layer" means a dielectric, insulating layer should be rejected. The Staff argues that while the '345 patent teaches the use of a dielectric material, that teaching is directed to the composition of the material used to fill the gaps between the wiring lines and should not, therefore, be inserted as a limitation for "cap layer." OUII Post-Hearing Brief (Following the November Hearing) at 26-27 (citing Peltzer Tr. 884-885 (Respondents' expert agrees that the claim language does not require that cap layer be a dielectric)).

Given the broad functions outlined by the '345 specification for the cap layer, even with respect to the preferred embodiments, the functions that a cap layer might fulfill are not at issue.[41]

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[41] The '345 specification provides: "The cap layer may serve a number of functions, acting as an antireflective coating, a hard mask for metal line etching, and a protector for the top corners of metal wiring lines during the HDPCVD process." CX-1/RX-40 ('345 Patent), col. 4, lines 57-60 (general discussion of the preferred embodiments). *See also* CX-1/RX-40 ('345 Patent), col. 7, (continued...)

Nevertheless, a question is raised as to whether in all instances the claims of the '345 patent require that the cap layer be a "dielectric, in

sulating layer."

The specification teaches the use of such a layer as a preferred embodiment, in which cap layer **28** "is preferably formed from silicon oxide, silicon nitride or oxynitride." *See, e.g.*, CX-1/RX-40 ('345 Patent), col. 7, lines 31-32; Peltzer Tr. 884-885. While neither the claims nor the specification contains language indicating that the precise limitation proposed by Respondents ("dielectric, insulating" layers) must be used for cap layers in all possible embodiments covered by the claims of the '345 patent, the specification nevertheless teaches: "In another aspect of certain embodiments, the cap layer, which may not be a conductive material, may be removed prior to an electrical connection being made to the wiring lines." *Id.* at col. 9, lines 61-64. It appears that the information to be conveyed about "certain embodiments" is that the cap layer "may be removed prior to an electrical connection being made to the wiring lines." However, the statement that a cap layer "may not be a conductive material" is best understood as a statement about cap layers, in general, under the claims of the '345 patent.[42] Indeed, it is logical to define a cap layer as non-conductive, rather than conductive, because during the HDP

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[41] (...continued)
lines 58-64 ("The cap layer **28** may serve a number of functions. During the exposure of the photoresist layer to light to shape the mask prior to etching, the cap layer may be used as a quarter wave plate in order to prevent light from passing through the cap layer and reflecting back up to the photoresist layer and causing the photoresist layer to become exposed in regions that are supposed to remain unexposed.").

[42] It is clear from the '345 patent specification that the cap layer **28** in a preferred embodiment is preferably a silicon, which is not a conductive material, and that the cap layers in "certain embodiments" -- a rather open-ended phrase -- which are discussed in column 9 are also non-conductive.

CVD gap-filling process, portions of the cap layer may be redeposited within the gap, and a manufacturer

would avoid increased capacitance between wiring lines. *See, e.g.*, CX-1/RX-40 ('345 Patent), col. 9, lines 49-55. Consequently, while it is not required to impose the precise limitation that a cap layer be formed from a "dielectric, insulating" material, the term "cap layer" as used in the claims of the '345 patent is understood to consist of a material that is not conductive.[43]

(v) at a sputtering rate sufficient to fill the gaps

Complainants argue that "at a sputtering rate sufficient to fill the gaps" means using a sputtering rate sufficient to remove and redistribute dielectric material from the wiring line sidewalls so as to enable substantially void-free filling of gaps, enhance planarization, and prevent buildup at the corners of the wiring line and thus resulting in better gap-filling. Complainants argue that nothing in the claims or specification imposes a limitation that only a single dielectric can be deposited, nor is there any limitation as to "an appropriate E/D ratio."

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[43] As a non-conductive material, some may refer to such as layer simply as a "dielectric." *See, e.g.*, THE AMERICAN HERITAGE DICTIONARY OF THE ENGLISH LANGUAGE 519 (3d ed. 1992)("**dielectric** . . . *n.* A nonconductor of electricity, especially a substance with electrical conductivity less than a millionth (10^{-6}) of a siemens."); *but see* WEBSTER'S NEW WORLD ENCYCLOPEDIA 332 (1992)(**dielectric** a substance (an insulator such as a ceramic, rubber, or glass) capable of supporting electric stress."). *See also* International SEMATECH Official Dictionary, Rev 5.0, *http://www.sematech.org/public/publications/dict/* ("**dielectric** *n* 1 : a nonconductive material; an insulator. Examples are silicon dioxide and silicon nitride. [SEMATECH] 2 : a material applied to the surface of a ceramic or preformed plastic package to provide functions such as electrical insulation, passivation of underlying metallization, and limitations to solder flow. [SEMI G33-90]"); Lucent Technologies Glossary (online), *http://www.lucent.com/search/glossary/glossary.html* ("**Insulator** A material, such as glass, wood or rubber, that is a poor conductor of electricity, or a device made from such a material. It's used to separate conductors from one another.").

See CPCL 15 (citing CPFF 332-36).

Respondents argue that "at a sputtering rate sufficient to fill the gaps" means depositing a single dielectric material between patterned wiring lines to fill the gaps completely without voids, using only high density plasma chemical vapor deposition at an appropriate E/D ratio. Respondents' Post-Hearing Brief (Following the November Hearing) at 17 (citing CX-1/RX-40 ('345 Patent), col. 2, lines 44-47 and 52-54; Fig. 4; PFF 425; RPCL 52).

The Commission Investigative Staff argues that Complainants' proposed claim construction for "sputtering rate sufficient to fill the gaps" is supported by the intrinsic evidence, whereas Respondents' proposed construction is not. It is argued that the '345 specification, provides the following teaching:

> [S]puttering removes and redistributes dielectric material from wiring line sidewalls and enables substantially void-free filling of gaps and enhances planarization . . . [T]he sputter component acts to prevent material buildup at the corners of the wiring lines and results in better gap filling.

CX-1/RX-40 ('345 Patent), col. 6, lines 17-22.

The Staff argues that neither the claims and specification nor prosecution history teach that only a "single" dielectric can be used, and relying on Peltzer Tr. 887, that the intrinsic evidence does not provide that there is any limitation as to the appropriate etch-to-deposition ratio. Rather, citing col. 6, line 19; col. 11, line 2 (claim 9), the Staff argues that the only requirement for the sputtering rate is that it be "sufficient" to fill the gaps. The Staff argues that Respondents' construction of "sputtering rate sufficient to fill the gaps" is based on portions of the specification that describe the "Background of the Invention" and not the disclosed embodiments. OUII Post-Hearing Brief (Following the November Hearing) at 27-29 (citing Fair

Tr. 163-64).

A review of the '345 patent specification and testimony at issue shows that the claim language "at a sputtering rate sufficient to fill the gaps," which is found in independent claim 9, does not necessarily require the added limitation of a "single" dielectric material. Nor does that phrase necessarily require the addition of an "appropriate E/D ratio." Although it may be desirable or necessary to have an etch to deposition ratio that is *appropriate*, this does not appear to be a matter of basic claim construction.

With respect to the question of whether the phrase "at a sputtering rate sufficient to fill the gaps" covers only processes that "completely" fill gaps or also processes that "substantially" fill gaps, it is noted that the claim language itself uses no such qualifier. It simply refers to a sputtering rate sufficient *to fill* the gaps.

The portion of the specification relied on by Respondents addresses the "background of the invention" and the "related art." It states that dielectric material deposited into the gaps between wiring lines "should be able to *completely* fill the gap between conductors," yet also that "it is important to accurately form wiring lines and gaps, and to deposit a high quality, *substantially* void-free dielectric into gaps." *See* CX-1/RX-40 ('345 Patent), col. 2, lines 44-54 (emphasis added). These portions do not bear directly on a limitation to the claimed invention, and demonstrate that the precision sought to be added by Respondents as a claim limitation is apparently not present in the prior art (as least as the prior art is discussed in the '345 specification). In addition, the portion of the specification relied on by the Commission Investigative Staff, demonstrates that at least with respect to a preferred embodiment, sputtering "enables *substantially void-free filling* of gaps." *See* CX-1/RX-40 ('345 Patent), col. 6, lines 14-

23 (emphasis added).

Consequently, the limitation that Respondent seek to have added to claim 9, with respect to complete filling of gaps, is not adopted. Specific questions as to whether Respondents' accused processes are covered by the claims of the '345 patent are discussed in the section below on the infringement issue.

(vi) oxide, (vii) nitride, (viii) oxynitride

Some or all of the terms "oxide," "nitride" and "oxynitride" are found in ceratin claims of the '345 patent with reference to cap layer. *See* CX-1/RX-40 ('345 Patent), claims 13 and 21. The parties advance similar arguments with respect to each of these terms.

Complainants argue that "oxide" means the oxide of a material and can be represented by the chemical symbol MO_x where M can be any element and the subscript x is a number greater than zero, and the fact that silicon oxide is a preferred embodiment does not limit oxide to silicon oxide. *See* CPCL 17 (citing CPFF 338-39). Respondents argue that "oxide" means silicon oxide or SiO or SiO_2. Respondents' Post-Hearing Brief (Following the November Hearing) at 18 (citing CX-1/RX-40 ('345 Patent), col. 7, lines 30-32; RPFF 408-421; RPCL 47). The Commission Investigative Staff argues that "oxide" should not be limited to silicon oxide or silicon dioxide. The Staff argues that while Respondents rely on the statement "[c]ap layer . . . is *preferably* formed from silicon oxide," such a construction relies on importing limitations from the '345 patent's preferred embodiments, a practice that runs afoul of controlling Federal Circuit authority. The Staff is of the view that "oxide" should be construed as "the oxide of a material." OUII Post-Hearing Brief (Following the November Hearing) at 29 (citing *Pall Corp. v. PTI Techs., Inc.*, 259 F.3d 1383, 1391 (Fed. Cir. 2001); Peltzer Tr. 888-889 (agrees that Respondents

construe "oxide" based on preferred embodiment)).

Complainants argue that "nitride" means the nitride of a material and can be represented by the chemical symbol MN_y where M can be any element and the subscript y is a number greater than zero, and the fact that silicon nitride is a preferred embodiment does not limit nitride to silicon nitride. *See* CPCL 18 (citing CPFF 340-41). Respondents argue that "nitride" means silicon nitride. Respondents' Post-Hearing Brief (Following the November Hearing) at 18 (citing (CX-1/RX-40 ('345 Patent), col. 7, lines 30-32; RPFF 408-421; RPCL 48). The Commission Investigative Staff argues that it is well-settled that claims generally are not to be limited to the preferred embodiments, yet Respondents incorrectly construe "nitride" as being limited to silicon nitride. The Staff argues that "nitride" should be construed to mean the nitride of any material, wherein silicon oxide, silicon nitride, and oxynitride are examples. OUII Post-Hearing Brief (Following the November Hearing) at 30 (citing CX-1/RX-40 ('345 Patent), col. 7, lines 30-32 ("[c]ap layer 28 . . . is *preferably* formed from silicon oxide, silicon nitride or oxynitride . . .")(emphasis added); Peltzer Tr. 890).

Complainants argue that "oxynitride" means the oxynitride of a material and can be represented by the chemical symbol MO_xN_y where M can be any element and the subscripts x and y are greater than zero. Complainants argue that nothing in the claims or specification limits oxynitride to silicon oxynitride. *See* CPCL 19 (citing CPFF 342-43). Respondents argue that "oxynitride" means silicon oxynitride. Respondents' Post-Hearing Brief (Following the November Hearing) at 18 (citing CX-1/RX-40 ('345 Patent), col. 7, lines 30-32; RPFF 408-421; RPCL 49). The Commission Investigative Staff argues that "oxynitride," like "oxide" and "nitride," should be construed in accordance with its well-accepted meaning to one of ordinary

skill in the art, and that thus, consistent with the intrinsic evidence, "oxynitride" should be construed as the oxynitride of a material. OUII Post-Hearing Brief (Following the November Hearing) at 30-31.

The record demonstrates that there is an insufficient basis to read characteristics of the particular oxide, nitride and oxynitride from the preferred embodiments of the '345 specification into the patent claims. Consequently, Respondents' proposed limitations for oxide, nitride and oxynitride are not adopted.

B. Infringement Determination

Complainants argue that SiS's [ ] manufacturing process and its [ ] process infringe numerous claims of the '345 patent.[44] The issues relating to these two, distinct processes are discussed separately below.

1. Respondents' [ ] Manufacturing Process Which Uses an SiON Cap Layer

Complainants argue in their main post-hearing brief that their expert Dr. Fair went through SiS's [ ] manufacturing process step-by-step to show that the process contains all the elements of the asserted claims of the '345 patent, and thus Respondents' [ ] process, which uses [ ], infringes all

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[44] Complainants' briefs do not raise the doctrine of equivalents in connection with infringement of the '345 patent. Respondents argue that no evidence of infringement under the doctrine of equivalents was adduced at the hearing; that Respondents have not been apprised of arguments under the doctrine of equivalents; and that all independent claims of the '345 patent were amended during patent prosecution in overcome rejections by the PTO. *See* Respondents' Post-Hearing Brief (Following the December Hearing) at 15-16. Moreover, the Administrative Law Judge is aware of no argument or evidence in this investigation that is relevant to the doctrine of equivalents and would result in a different ultimate conclusion of infringement or noninfringement than would be reached under the law of literal infringement.

asserted claims of the '345 patent. Furthermore, Complainants argue that in accordance with the parties' October 16, 2001 stipulation, Respondents did not contest the evidence of infringement, and therefore Respondents' [ ] process should be found to infringe the '345 patent. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 16-17 citing CPFF 460-99). In particular, Complainants allege that Respondents infringe claims 1, 3-9, 11-13 and 20-21 of the '345 patent. *See* CPFF 462; Complainants' Proposed Conclusions of Law for Hearing Completed November 16, 2001 at 13-14 (CPCL 44-53).

The Commission Investigative Staff supports a finding of infringement by Respondents' [ ] process. *See* OUII Post-Hearing Brief (Following the November Hearing).

Respondents argue in their main post-hearing brief that although they stipulated that they would not contest infringement of the '345 patent by [ ] process," Complainants retained the burden of establishing infringement of each asserted '345 patent claim. Respondents argue that at most Complainants have established infringement of only claim 9 (which recites a "cap layer" on a metal wiring line layer,) because in the [ ] process, [ ]. Respondents' Post-Hearing Brief (Following the November Hearing) at 33.

With respect to independent claim 1 and its dependent claims, Respondents argue that Complainants did not establish that the [ ] process had first and second antireflective coating. In particular, Respondents argue that Dr Fair testified that only by measuring reflectivity can one determine whether a layer is antireflective, and he questioned whether a layer could serve as an antireflective coating if none of the incident light passes through the second antireflective coating to the first antireflective coating. Respondents argue that Complainants submitted no

evidence that any incident light during DUV photolithography passes through [

]. *Id.*

With respect to claim 21, Respondents argue that while the surface layer [

].

In their reply brief, Complainants argue that notwithstanding the stipulation that Respondents would not contest infringement of the '345 patent by their [ ] process (October 16 Stipulation ¶ 20), Respondents have attempted to do just that by arguing that Complainants have not met the burden of establishing infringement of the asserted claims of the '345 patent. Complainants further argue that in addition to the fact that Respondents should be precluded by their stipulation from contesting infringement, the substance of Respondents' infringement arguments is wrong because Dr. Fair's step-by-step testimony concerning the [ ] process established that the process contains all elements of claims 1, 3, 4, 5, 9, 11, 12, 13, 20 and 21 of the '345 patent, including a first and second antireflective coating as required by claim 1, and a surface layer "comprising at least one material selected from the group consisting of titanium nitride, titanium silicide and a titanium tungsten alloy" as required by claim 21. Complainants' Post-Hearing Reply Brief (Following the November Hearing) at 7 (citing CPFF 464-69, 492-99).

In addition, Complainants argue that Respondents are wrong in their assertion that the record contains no evidence regarding [ ]. Complainants argue that Respondents submitted exhibits containing such evidence. Moreover, Complainants argue, Dr. Fair testified that [

].

Finally, Complainants argue that Respondents are also wrong in asserting that [ ] process does not infringe claim 21 because [

].

The pertinent part of the stipulation entered into by Complainants and Respondents with

[45] The report was prepared by n&k Technology, Inc. of Santa Clara, California. The company is hereinafter referred to as "n&k."

respect to infringement by SiS's SiON process is as follows:

> Solely for purposes of this investigation and not for use in any district court action or in any other matter, respondents stipulate that they will not contest infringement of the '345 patent by SiS's SiON process. Respondents reserve the right to contest validity of the '345 patent, importation, and domestic industry as to the '345 patent both with respect to SiS's SiON process and with respect to SiS's N2OPT process as well as with respect to any other process accused by complainants of infringing the '345 patent.

Stipulation to Further Revise the Prehearing Schedule (Oct. 16, 2001), ¶ 20.[46]

At the hearing, Complainants' expert rendered an opinion as to each element of each asserted claim of the '345 patent to the effect that the [ ] process infringes. The expert's opinion was based on his review of SiS operational manufacturing procedures as recorded in SiS documents entered into evidence. *See* Fair Tr. 144, 154-175; CX-12C; CX-13C. In view of Respondents' stipulation not to contest Complainants' infringement allegation with regard to [ ] process and the '345 patent, Complainants' *prima facie* evidence is adequate to prevail on the question of whether or not [ ] process practices the asserted claims of the '345 patent.[47] Accordingly, if it were found that the asserted '345 patent claims were valid (and enforceable), it would be found that Respondents' [ ] process infringed those claims.

2. Respondents' [ ] Process

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[46] On February 7, 2002, Respondents filed their "Motion for Leave to Withdraw Stipulation and Request for a Determination on Whether Respondents' 'SiON' Process Infringes '345 Patent." Motion Docket No. 450-28. *See* Order No. 18 (concerning Motion No. 450-28); Order No. 19 (concerning Motion No. 450-28). On April 23, 2002, Respondents filed their "Notice of Withdrawal of Respondents' Motion to Withdraw Stipulation and Request for a Determination on Whether Respondents' 'SiON' Process Infringes '345 Patent."

[47] It is generally accepted at law that an unrebutted *prima facie* case is, by definition, a "preponderance of the evidence." *See Kewley v. HHS*, 153 F.3d 1357, 1365 (Fed. Cir. 1998); *Hale v. Dept. of Transportation*, 772 F.2d 882, 885-86 (Fed. Cir. 1985). Due to their stipulation, Respondents were not entitled to rebut Complainants' *prima facie* case.

a. Background

[

] Complainants argue that SiS's [

] process infringes claims 1, 3, 4, 5, 9, 11, 12, 20 and 21 of the '345 patent. *See, e.g.*, Complainants' Post-Hearing Brief (Following the December Hearing); Complainants' Post-Hearing Reply Brief (Following the December Hearing). The Commission Investigative Staff also argue that the asserted claims are infringed by the [ ] process. *See, e.g.*, OUII Post-Hearing Brief (Following the December Hearing); OUII Post-Hearing Reply Brief (Following the December Hearing). Respondents deny the allegations of Complainants and the Staff with respect to the [ ] process, and argue that Complainants have failed to carry their burden of establishing infringement of the asserted claims. Respondents' Post-Hearing Brief (Following the December Hearing); Respondents' Post-Hearing Reply Brief (Following the December Hearing).

[

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[

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[

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b. Alleged Infringement of Claims 1, 3, 4 and 5 of the '345 Patent – "Forming a Second Antireflective Coating"

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[48] [

]

[49] [

]

i. Summary of the Parties' Arguments and Evidence

Following the December, 2001 hearing, which was concerned almost entirely with the [ ] process, the parties filed new main and reply briefs, and new main and reply findings. [

] The parties' arguments are briefly summarized below.

Complainants argue that, as testified to during the hearing by their expert, Dr. Fair, the term "coating" and "layer" would have the same meaning to those of ordinary skill in the art, and further, that "forming," as used in claim 1, is not limited to forming a film on top of the first antireflective coating by means of a deposition process. Rather, it is argued, the terms "forming" or "formed" may refer to altering a materials' composition, thus [

]

Complainants argue while the third element of claim 1 of the '345 patent requires that the first and second antireflective coatings be made from "different materials," [

]

Complainants also offer a series of arguments to support its position that [

]

With respect to particular claims of the '345 patent, Complainants argue that [

]

The Commission Investigative Staff supports a finding that the asserted claims of the '345 patent are infringed by SiS's [ ] process. *See* OUII Post-Hearing Brief (Following the December Hearing) at 1-12.

Respondents argue, with respect to independent claim 1 of the '345 patent, that Complainants have failed to demonstrate that the [ ] process includes each and every element of the process described in claim 1 of the '345 patent. A primary basis

for Respondents' position is their argument that [

]

Respondents take the position that according to the '345 patent, the relative dielectric constants of the photoresist, the first antireflective layer, and the purported second antireflective layer must be considered to determine whether there is a second antireflective layer, yet [

] Respondents argue that those conclusions could be made without knowing values for the index of refraction for layers or structures in the wafer, without knowing or assuming thickness of layers in the wafer, and without knowing or assuming the material composition of layers in the wafer, whereas Complainants' expert, Dr. Fair, assumed material compositions, assumed layer thicknesses, calculated n and k values, assumed the existence of a planar interface between layers, and assumed no effect from roughness of the surface. That plethora of assumptions exposes Dr. Fair's conclusions to significant uncertainty and lack of precision. Moreover, Respondents argue that Dr. Fair embraced the absurd position that [

]

Respondents further argue that their [ ] process does not form layers of different materials. In particular, [

]

Finally, Respondents argue that the SiS [ ] process does not form a coating "on" the TiN layer; rather, [

]

In addition, Respondents argue that absent a second antireflective coating, other steps (or elements) of claim 1 cannot be satisfied. For example, [

] Thus, Respondents argue, the fourth step of claim 1 is not satisfied. [

] Thus, it is argued the fifth step of claim 1 is not satisfied. *See Id.* at 24.

Respondents argue that the [ ] process does not literally infringe claim 1 because it does not perform either the second, third, or fourth steps of that claim. *See Id.*

With respect to the claims 3, 4 and 5 of the '345 patent, Respondents argue that each depends from claim 1 and requires that all elements of claim 1 be present; yet claim 1 is not infringed by the [ ], and thus the dependent claims cannot be infringed. *Id.* at 24-25 (citing *Wahpeton Canvas Co., Inc. v. Frontier, Inc.*, 870 F.2d 1546 (Fed. Cir. 1989). In addition, Respondents argue that the [

]

ii. Analysis

"Antireflective Coating"

It is clear from the parties' briefs that the primary question on which their infringement arguments depend is the meaning of the term "antireflective coating." As explained in detail in the section on claim construction, the antireflective effect of a coating must be significant to the purposes of the invention in order for that coating to satisfy the claim limitation and to be described as "antireflective." A coating that is simply less than a perfectly reflective mirror (*see* OUII Post-Hearing Brief (Following the December Hearing) at 9) or that has the opposite effect and actually increases reflectivity is plainly not an "antireflective coating," whether one applies simple logic or the intrinsic evidence relating to the '345 patent.

The "intrinsic evidence," i.e., the patent claims, the patent specification, and the prosecution history, constitute the "most significant source of the legally operative meaning of disputed claim language." *Vitronics*, 90 F.3d at 1582. If the intrinsic evidence cannot resolve a genuine ambiguity as to claim meaning, then one may consider "extrinsic evidence" such as expert testimony, treatises, and technical references. *Digital Biometrics, Inc. v. Identix, Inc.*, 149 F.3d 1335, 1344 (Fed. Cir. 1998). The intrinsic evidence thus forms the public record on which competitors are entitled to rely in determining claim scope and designing around the claimed invention. *Vitronics* at 1583. Respondents have made a case that they have done precisely that -- that they have relied upon the public record and designed around the '345 patent. As the Federal Circuit has admonished, "[a]llowing the public record to be altered or changed by extrinsic

evidence introduced at trial, such as expert testimony, would make this right meaningless." *Vitronics*, at 1583.

As argued in Respondents' briefing, the evidence shows that [

]

Complainants arranged for Acton Research Corp. to conduct wafer reflectivity tests on wafers [

]

Although it is not Respondents' burden to prove lack of infringement, nevertheless the preponderance of the evidence relating to direct wafer reflectivity tests demonstrates that [

]

Complainants, who bear the burden of proving that the [

]

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[50] [

(continued...)

[

]53

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50 (...continued)

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51 [

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52 [

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53 [

(continued...)

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[

]

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[53] (...continued)

]

[ ]

"Different materials"

Claim 1 requires that a first and second antireflective coating be made from "different materials." Complainants argue that one of ordinary skill in the art would consider [

] For example, using SIMS analysis,[54] an independent testing laboratory determined that [

]

[

[54] SIMS is an acronym for secondary ion mass spectroscopy. Peltzer Tr. 1760.

]

"On" the first antireflective layer

Claim 1 reads on a process that includes the step of forming a second antireflective coating "on" a first antireflective coating. [

] As discussed in detail in the section on claim construction, the term "on," is given its ordinary meaning.

As Respondents argue: [

]

c. Alleged Infringement of Claims 9, 11, 12, 20 and 21 –

"Forming a Cap Layer"

i. Summary of the Parties' Arguments

In addition to arguing that the [ ] process infringes certain claims pertaining specifically to a first and second ARC, Complainants assert that the [ ] process infringes claims 9, 11, 12, 20 and 21 of the '345 patent, which involve the formation of a cap layer.

Complainants acknowledge that Respondents argue that the cap layer must be a dielectric. While Complainants oppose such a construction, they argue that [

]

The Commission Investigative Staff argues that claims 9, 11, 12, 20 and 21 are infringed because a "cap layer" is formed as a result of [ ]

[

]

Respondents argue that a cap layer must function as a hard mask, an antireflective coating or a metal-line top corner protective layer, and that [ ] process does not use a cap layer. For example, it is argued that, [

]

Furthermore, Respondents argue that the third step of claim 9 requires that a mask layer cover selected portions of the cap layer and expose other portions of the cap layer, yet [

]

[ ] Similarly, it is argued that the fourth step of claim 9 requires etching of the cap layer at the exposed locations to form wiring lines, yet [

]

Respondents argue that as to claim 11, [

] It is argued that claims 11, 12 and 20 cannot be infringed because they depend from claim 9, and all elements of claim 9 are not present. *See Id.* at 28-29.

With respect to claim 21, Respondents argue that [

] As to the sixth step of claim 21, which requires formation of a patterned photoresist above the cap layer, [

] Similarly, it is argued, with respect to the seventh step of claim 21, which requires that exposed portions of the cap layer be etched, [ ]

[

]

ii. Analysis

It is undisputed that the term "cap layer" means a layer that serves one of three functions – *i.e.*, "acting as an antireflective coating, a hard mask for metal line etching, and/or a protector for the top corners of metal wiring lines during the HDPCVD process. *See, e.g.*, Complainants' Post-Hearing Brief (Following the December Hearing) at 20; Respondents' Post-Hearing Brief (Following the December Hearing) at 20. Furthermore, the '345 specification expressly states that the cap layer "may not be a conductive material," and the claims of the patent have been so construed.

[

]

[

]

d. Conclusion Regarding Alleged Infringement of the '345 Patent by Respondents' [ ] Process

For the reasons stated above, as supplemented by the Administrative Law Judge's findings of fact, the [ ] process does not infringe any asserted claim of the '345 patent.

VI. VALIDITY OF THE '345 PATENT

A. Anticipation Under 35 U.S.C. § 102(a) in View of the Tobben Patent

1. The Question of Whether Tobben Is Prior Art

Respondents argue that inasmuch as United States Patent No. 5,854,126 to Tobben et al. ("Tobben")(RX-70) is based on an application filed on March 31, 1997, and the '345 patent is based on an application filed on April 2, 1997, Tobben is prior art to the '345 patent to determine invalidity questions under 35 U.S.C. § 102. Respondents argue that Complainants' attempt at the hearing to establish that the '345 patent disclosure was brought to the United States in early 1997

[55] [

]

is based on speculation and conjecture. It is further argued that even if the '345 patent were entitled to an earlier date, Tobben would in any event be prior art because Tobben was conceived during an April 1996 joint development project in the United States involving Siemens, IBM and Toshiba. *See* Respondents' Post-Hearing Brief (Following the November Hearing) at 22-24.

Complainants argue that Tobben is not prior art with respect to the '345 patent because the '345 patent is entitled to an invention date of January 16, 1997, and Tobben is not entitled to an invention date earlier than March 31, 1997. Complainants argue that although Dr. Wright, a patent attorney, did not specifically recall bringing the '345 patent disclosure to the United States, there is no way that he could have received the invention disclosure form for the '345 patent other than on a trip he made to Taiwan in January 1997, and that Dr. Wright's testimony and the documentary evidence is more than sufficient to establish a January 1997 date of invention for the '345 patent. Complainants also reject arguments that a firm other than that associated with Dr. Wright drafted the provisional application filed on April 2, 1997, which led to the '345 patent. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 22; Complainants' Post-Hearing Reply Brief (Following the November Hearing) at 8-10.

The Commission Investigative Staff argues that Respondents have not shown that Tobben is prior art. *See* OUII Post-Hearing Brief (Following the November Hearing) at 33-34; OUII Post-Hearing Reply Brief (Following the November Hearing) at 13-14.

With respect to the question of whether Tobben is entitled to an invention date earlier than its filing date, it is found that Respondents have failed to set forth clear and convincing evidence to that effect. Respondents rely on the testimony of Dr. Schutz, who was a 30(b)(6)-type witness for Infineon, a U.S. subsidiary of Siemens, the Tobben assignee.

Respondents' key argument is that Mr. Tobben must have submitted his invention before August of 1996 because Dr. Schutz began to supervise Mr. Tobben in August of 1996, and Dr. Schutz knows that Mr. Tobben did not submit the invention disclosure from that time forward. Respondents' argument is founded on a mixture of deduction and conjecture, which although founded on certain established facts, does not rise to the level of clear and convincing evidence needed to fix an earlier invention date for invalidating or potentially invalidating prior art. Consequently, the date used for the Tobben patent for the purposes of this Initial Determination is March 31, 1997, Tobben's application filing date.

Similarly, Complainants rely on deduction and conjecture in an attempt to establish an early date for the claimed invention of the '345 patent. Dr. Wright's belief that he must have brought a disclosure that led to the '345 patent to the United States upon his return from a particular trip to Taiwan is too speculative to establish a January, 1997 date for the '345 patent, even under the lesser standard of a preponderance of the evidence. Consequently, the date used for the '345 patent for the purposes of this Initial Determination is April 2, 1997, the '345 patent's provisional application filing date.

Therefore, Tobben is considered prior art to the '345 patent in connection with all the invalidity arguments made by Respondents under sections of 35 U.S.C. § 102.

2. The Question of Whether Tobben Discloses All Elements of the Asserted Claims of the '345 Patent

a. Description of Tobben's Disclosure and Brief Summary of the Parties' Arguments

The '126 patent to Tobben et al. is entitled "Method for Forming Metallization in

Semiconductor Devices with a Self-Planarizing Material." RX-70. The Tobben specification explains that in modern integrated circuit metalization processing, electrically conductive wires are formed over an integrated circuit substrate using photolithographic-chemical etching processes. A photoresist layer is deposited over the surface of a metal layer into which the conductive wires are to be formed. A mask having the desired pattern for the conductive wires is placed over the photoresist layer, and light is then projected onto the mask, with such light passing through openings in the mask and onto exposed portions of the photoresist layer. The photoresist layer is then developed with the light-exposed regions of it removed. The patterned photoresist layer is then used as an etching mask to etch away portions of the metal layer exposed by the developed photoresist mask. Thus, the patterned photoresist layer is transferred to the metal layer to pattern the metal layer into the electrically conductive wires. Tobben explains, however, that in forming conductive wires with widths in the order of one-quarter micron, it is necessary that the photoresist layer have an extremely high degree of planarity. However, problems may occur because when the metal layer is formed, it has a non-planar surface because the underlying surface is non-planar. Thus, if the photoresist layer is deposited onto the metalization layer, the photoresist layer (which is generally a non-conformal layer) will have a non-uniform thickness. The Tobben patent states that one technique used to obtain a uniform thickness for the photoresist layer is planarizing the underlying surface upon which the metal layer is deposited using chemical mechanical polishing (CMP) techniques. Such CMP techniques, however, are relatively expensive. So, the Tobben patent discloses another, apparently less costly, technique. *See* RX-70 ('126 Tobben Patent), col. 1, lines 6-38.

The Tobben specification teaches that, in accordance with the claimed invention, a

method is provided for forming a plurality of electrically conductive wires on a substrate by depositing a self-planarizing material over the relatively non-planar metal layer. The self-planarizing material forms a planarization layer over the surface of the metal layer, yet the planarization layer has a surface which is relatively planar compared to the relatively non-planar metal layer. A photoresist layer is deposited over the surface of the planarization layer. The photoresist layer has a planar surface and is patterned with a plurality of grooves to form a mask. The grooves expose underlying portions of the planarization layer. The photoresist mask is used as a mask to etch grooves in the exposed portions of the planarization layer. The etched planarization layer forms a second mask. The second mask exposes underling portions of the relatively non-planar metal layer. The second mask is used to etch grooves in the relatively non-planar metal layer and thereby form the plurality of electrically conductive wires in the metal layer. The wires are separated from each other by the grooves formed in the relatively non-planar metal layer. *Id.* at col. 1, lines 41-62.

The specification further teaches that in accordance with other features of the invention: (1) the step of forming the planarization layer comprises the step of spinning on the self-planarizing material; (2) the spinning step comprises the step of spinning on an organic polymer, e.g., an organic polymer having silicon, or a flowable oxide, or a hydrogensilsequioxane,[56] or divinyl-siloxane-benzocyclobutene; and finally (3) in accordance with another feature of the invention, the step of etching the metal layer comprises the step of

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[56] In certain passages, the Tobben specification (including the claims) refers to "hydrogensilsequioxane," while in others, the reference is to "hydrogensilseguioxane." It is believed that in all such instances, the reference should be to "hydrogensilsequioxane," and that the apparent typographical error is of little or no consequence, especially to one skilled in the art.

using reactive ion etching. *Id.* at col. 1, line 63 to col. 2, line 7.

Respondents argue, with particular reference to the embodiment detailed in the specification, that Tobben discloses the forming of semiconductor integrated circuit patterns covered with an antireflective coating of titanium nitride and a planarization layer of dielectric material of appropriate thickness to serve as an antireflective coating over at least a portion of the surface of the integrated circuit. Respondents further argue that Tobben discloses a wiring line structure on a substrate, where the wiring line structure is composed of a lower layer of titanium/titanium nitride, an intermediate layer of aluminum, and an upper antireflective layer of titanium/titanium nitride. It is also argued that Tobben discloses a dielectric cap layer of, for example, silicon dioxide which is deposited on the upper antireflective layer, and that high density plasma processing is disclosed as a method for filling the gaps between wiring lines with dielectric material. Respondents' Post-Hearing Brief (Following the November Hearing) at 19-21.

Thus, with respect to the asserted claims of the '345 patent, Respondents argue that Tobben anticipates the process of the '345 patents, and in particular, the use of a second antireflective layer (claim 1) and a cap layer (claims 9 and 21) along with the use of HDP CVD to fill the gaps between metal wiring lines. Respondents further argue that the mask layer in Tobben is a patterned photoresist layer (claim 3); that the second antireflective coating may be left on the first antireflective coating, and etched during the HDP CVD process (claim 4); that in Tobben, a barrier layer is between the substrate and the wiring line layer (claim 5); that Tobben discloses the use of the second antireflective layer as a hard mask (claim 7); that the second antireflective coating on the wiring lines has the cross section of a rectangle after etching

(claim 8); that the second antireflective layer in Tobben comprises a "cap layer" because a layer which is above the TiN layer and which serves as an antireflective coating is a "cap layer" (as required by Complainants' construction of independent claim 9); that Tobben discloses the use of the second antireflective layer as a hard mask (claim 10); that the cap layer in Tobben is an antireflective coating (claim 11); that the cap layer (the second antireflective coating), if left on the first antireflective coating, is etched during the HDP CVD process (claim 12); the cap layer (the second antireflective coating) has the cross section of a rectangle after etching (claim 14); claims 15 and 16 are either anticipated by Tobben as an inherent shape for the cross section after etching or as an obvious cross-sectional shape for the cap layer (the second antireflective coating) after etching; that claim 19 is anticipated by Tobben because the cap layer (the second antireflective coating), if left on the first antireflective coating, is etched during the HDP CVD process and would necessarily be redeposited into the gaps during HDP CVD; that claim 20 is anticipated by Tobben because the mask layer is a patterned photoresist layer; and finally that claim 21 is anticipated by Tobben because each and every element of claim 21 is expressly disclosed in the Tobben patent (*see, e.g.*, RPFF 510-528). *See* Respondents' Post-Hearing Brief (Following the November Hearing) at 19-21.

Complainants deny that Tobben anticipates (or makes obvious) any asserted claim of the '345 patent. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 23-27; Complainants' Post-Hearing Reply Brief (Following the November Hearing) at 12-16. Complainants' arguments concerning Tobben fall into four main categories, summarized briefly as follows:

(1) Tobben does not disclose the second antireflective coating required by claim 1. It is

argued that Tobben's planarization layer cannot constitute an ARC coating within the meaning of the '345 patent because at the range of thickness taught by Tobben, this layer would experience constructive interference which would increase reflectivity and cause damage to the wafer. It is argued that persons of ordinary skill in the art never have understood Tobben's SiO2 planarization layer (a layer of transparent glass) to have any antireflective functionality. Complainants further argue that Respondents attempt to take a "new tack" in their supplemental briefing is also to no avail. It is argued that Respondents claim Tobben discloses a second ARC because the drawings in the '345 patent show only three wiring lines over a portion of the substrate and the Tobben planarization layer might operate as an ARC in such a discrete region of the wafer. However, Complainants argue that such a contention is based on a mischaracterization of Dr. Fair's testimony, ignores how one of ordinary skill would read the '345 and Tobben patents, and ignores a substantial body of case law on "inherent disclosure."

(2) Tobben does not disclose a "cap layer" that operates as a hard mask or a top corner protector during HDP CVD, as required by claim 9 because, as Dr. Fair testified, the photoresist is not removed in Tobben before the metal lines are etched. It is argued that Respondents have misread certain portions of the Tobben specification, and that in the embodiment of the Tobben patent relied on by Mr. Peltzer, the planarization layer is removed before HDP CVD, and further there is no teaching in Tobben that the planarization layer protects the wiring line, nor is such protection inherent, inasmuch as corner clipping will not necessarily occur during HDP CVD.

(3) Although claims 4 and 12 of the '345 patent require that the second ARC and the cap layer be etched during the HDP CVD process, Tobben's brief mention of HDP CVD does not teach that these layers are etched, nor is such etching inherent because, as taught in the '345

patent, such etching is dependent on the E/D ratio.

(4) Mention of HDP CVD in Tobben does not satisfy the "gap fill" requirements of claims 1, 9 and 21 because nowhere does Tobben teach removing and redistributing dielectric material from the wiring line sidewalls so as to provide substantially void-free filling of gaps between wiring lines, and that indeed Mr. Peltzer admitted that such gap-filling with HDP CVD is the result of proper process design that would not occur without teaching.

The Commission Investigative Staff also argues that Tobben fails to anticipate any asserted claim of the '345 patent. *See* OUII Post-Hearing Brief (Following the November Hearing) at 33-35.

b. Analysis

second antireflective coating (ARC)

As seen from the brief summary of the parties' arguments, one of the primary disputes among the parties is whether Tobben discloses a second antireflective coating as required by independent claim 1 of the '345 patent. With respect to a *first* antireflective coating, Tobben, in its detailed description of an embodiment, discloses that "metal layer **14** is a composite layer made up of a lower relatively thin layer of titanium/titanium nitride, and intermediate, relatively thick layer of sputtered aluminum; and an upper, thin antireflective coating (ARC) layer of titanium/titanium nitride." RX-70, col. 2, lines 36-40. Respondents rely on this passage, and it appears that there is no dispute that either in this passage or elsewhere, Tobben discloses a first ARC. *See* RPFF 437; CPRF 437.

With respect to a *second* ARC, Respondents cite the teachings of Tobben concerning the planarization layer, specifically including the passages which teach that "a planarization layer **16**

is formed over the surface **15** of the metal layer **14**," "[t]ypically, the thickness of the planarization layer is no more than 300 Å to 2000 Å," and "[a]lternatively . . . the composite planarization layer **16** includes a spun-on silicon dioxide glass as a bottom portion ***16a*** and a cap or upper layer ***16b*** formed thereon."[57] RX-70, col. 2, lines 47-48, col. 3, lines 3-10.

Persuasive testimony of Mr. Peltzer establishes that silicon dioxide, SiO2, in thicknesses of 300Å to 2000 Å, encompasses ranges where cancellation of reflected light from the surface of this coating is such that the silicon dioxide layer acts as a second antireflective coating (through interference as contemplated by the '345 patent, rather than absorption, also contemplated by the '345 patent).[58] *See* Peltzer Tr. 814-815, 847-848, 856 (using mathematical calculations to determine reflectivity).

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[57] *See also* RX-70, col. 3, lines 15-20 ("The silicon oxide is deposited by PE CVD at a temperature of about 400° C. or less and has a thickness sufficient to promote adhesion between the photoresist and the planarizing material. In one embodiment, the thickness of the cap layer is about 300-500 Å, preferably about 400-500 Å, even more preferably about 500 Å.").

[58] Mr. Peltzer testified in part:

> Q Mr. Peltzer, let me interrupt you at that point. Does the thickness for the SiO2 layer of 300 angstroms to 2000 angstroms correspond in any way to the thickness disclosed for the cap layer in the '345 patent?
>
> A It is of such thickness range to be a quarter-wave plate over portions.
>
> * * *
>
> Q So in your opinion, the SiO2 layer in Tobben is a second antireflective coating on the first antireflective coating?
>
> A Yes. This range from 300 to 2000 angstroms clearly encompasses ranges where we get an interferometric coating, get cancellation of the reflected light from the surface of this coating, with the reflected light from the bottom surface. So this is an antireflective coating, over most of the range it's an antireflective coating. There's a small range where the reflection might be worse.

Peltzer Tr. 814-815.

Complainants argue, and Respondents concede, that there would or could be regions on a wafer in which the planarization layer disclosed by Tobben (particularly silicon dioxide in the thicknesses taught in the specification) would not act as an antireflective coating. Yet, it is conceded by Complainants' expert that there could be other regions on a wafer in which the planarization layer in Tobben would act as an antireflective coating. Furthermore, Respondents' expert testified that in fact there would be regions in which the planarization layer in Tobben (such as the silicon dioxide layer which is described in detail) would act as an antireflective coating, for example, above a titanium nitride layer. *See* Fair Tr. 1395; Peltzer Tr. 815. There is no limitation in the '345 patent, including claim 1, that the method taught therein encompasses an entire wafer.[59] Thus, it is found the Tobben planarization layer is a second antireflective coating as required by the '345 patent.

cap layer

A central dispute concerning the question of whether the Tobben planarization layer protects the wiring line during HDP CVD is whether the cap Tobben planarization layer (e.g., planarization layer **16**) is removed before the HDP CVD gap filling step is performed. While the Tobben specification, at col. 4, lines 5-7, teaches that in at least one embodiment the

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[59] The parties' debate as to whether the three wiring lines depicted in the '345 patent could represent the entire invention or represent merely a portion of a continuum across an entire wafer although relevant to this question is not dispositive because even if the depiction is merely representative of a substrate covering a larger region of the wafer or the entire wafer, there is no indication under the claims of the patent that infringement would occur only if the claimed invention were practiced throughout an entire wafer.

Inasmuch as the claims of the '345 patent would be infringed by a region of a wafer, perhaps as small as that depicted in Figure 1 of the '345 patent, the claims are invalidated by prior art that encompasses a region of a wafer. *See Lewmar Marine, Inc. v. Barient, Inc.*, 827 F.2d 744, 747 (Fed. Cir. 1987) (explaining that, in assessing the validity and infringement of a patent claim, it is axiomatic that what literally infringes if later, anticipates if earlier).

planarization layer **14** is removed before the gap filling step, the specification further teaches that "if a second metalization layer is to be used, only the photoresist layer **18** is removed."[60]

A question is also raised as to whether or not the Tobben planarization layer would function as a "cap layer" within the meaning of claim 9 of the '345 patent. For example, Complainants argue that the Tobben planarization layer does not operate as a hard mask, and there is no teaching in Tobben that the planarization layer protects the wiring line, nor is such protection inherent because corner clipping will not *necessarily* occur during HDP CVD. However, Respondents logically argue that because the planarization may be left on the TiN layer during the HDP CVD gap filling, it would necessarily function to protect the TiN layer and the metal wiring lines during this step.

Furthermore, as discussed in the section on claim construction, it is undisputed that a "cap layer" may function as an antireflective coating, a hard mask for metal line etching, and/or a protector for the top corners of metal wiring lines during the HDP CVD process. As further discussed immediately above, the Tobben specification teaches the use of a composite planarization layer **16** which includes a spun-on silicon dioxide glass bottom portion **16*a*** and a silicon dioxide "cap or upper layer" **16*b*** formed, for example, by PE CVD. According to the specification at col. 3, lines 10-11, "[t]he cap layer comprises a dielectric material," and as further discussed above in connection with Mr. Peltzer's testimony, the planarization layer, and

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[60] Respondents argue that even by 1996, integrated circuits with multiple metalization layers were common. The record does, in fact, demonstrate that fact. *See* RX-76; RX-91C; JX-48C (Yota Dep.) Tr. 85-86. Although not necessarily required for anticipation, this fact shows that the passage in Tobben allowing for the planarization layer to remain after the photoresist is removed would have been useful to those skilled in the art even at the time that the Tobben patent issued.

the cap layer portion in particular with a thickness of preferably about 500 Å serves as an antireflective coating.

In addition, the Tobben specification teaches that after the planarization and cap layer are formed:

> Next, a photoresist layer **18** (**FIG. 3**) is spun on the planar surface **19** of the planarization layer 16 (i.e., either the single planarization layer **16** shown in **FIG. 2A** or the composite planarization layer **16** shown in **FIG. 2B**). A mask (not shown) is used to expose portions of the photoresist with an exposure source from, for example, a conventional stepper lithography system. The portions of the photoresist exposed by the exposure source are polymerized. The photoresist layer is then developed to remove the exposed or polymerized portions, creating grooves or slots **20**. The unremoved portions of the photoresist layer serves as a mask for patterning the underlying layers. As shown, the mask is used to pattern exposed portions **25** of the underlying planarization layer **16**. The exposed portions **25**, for example, correspond to regions electrically separating the electrically conductive wires to be patterned into the conductive metal layer **14**. Alternatively, a negative photoresist layer **18** is used. The use of a negative photoresist results in the unexposed portions being developed away.

RX-70 ('126 Tobben Patent), col. 3, lines 22-39.

Consequently, the planarization layer in Tobben is used in accordance with the element of claim 9, which requires that a mask layer be formed above the cap layer, wherein the mask layer covers selected portions of the cap layer and exposes other portions of the cap layer.

Tobben also teaches etching the cap layer, and the wiring line layer, at locations where the cap layer is exposed by the mask layer, to form wiring lines separated by gaps, the wiring lines having a remaining portion of the cap layer thereon, as required by claim 9. In particular, Tobben teaches that "the exposed portions of the metal layer . . . are etched away to form the plurality of electrically conductive wires over the dielectric layer," that the metal layer is a

composite made up of "an upper, thin antireflective coating (ARC) of titanium/titanium nitride," and that grooves are etched into the conductive metal layer to form the plurality of electrically conductive wires separated by the grooves. *See* RX-70, col. 2, lines 36-40, col 3, lines 56-66.

Thus, the planarization layer taught by Tobben, which includes the Tobben "cap layer," discloses the "cap layer" referred to in the '345 patent, particularly in independent claim 9.

etching of the second ARC or cap layer, the "gap fill" requirements of claims 1, 9 and 21

As discussed above in the section on claim construction, particular E/D ratios are not disclosed by the claims of the '345 patent. However, claims 4 and 12 do require that the second antireflective coating or remaining portions of the cap layer are etched during HDP CVD. Indeed, there is a gap filling requirement, for example in claim 21, which requires the formation of HDP CVD deposition material within the gaps to fill the gaps.

As discussed above, Tobben expressly teaches at col. 3, lines 10-11, that the "cap layer comprises a dielectric material." In particular, silicon dioxide is used in the detailed or preferred embodiment of the Tobben specification. Furthermore, that etching of the second ARC or cap layer occurs during HDP CVD, that gap filling thus occurs, is taught in the Tobben specification (after the portion quoted above concerning the etching of the cap layer and the wiring lines) when it states that in one embodiment the planarization layer is removed using, for example, wet chemistry, and that alternatively, a layer of silicon dioxide may be deposited over the surface of the grooved structure using SA (subatmospheric) CVD or instead "HDP techniques." *See* RX-70 ('126 Tobben Patent), col. 4, lines 5-18; Peltzer Tr. 830.

3. Conclusion As to Whether Tobben Anticipates the Asserted Claims of the '345 Patent

For the reasons stated above, and as further illustrated in the findings of fact contained in this Initial Determination, there is clear and convincing evidence that each element of the asserted patent claims (whether disputed or not) is disclosed in Tobben, or in the case of claim 13 is obvious in view of Tobben and other prior art.[61]

B. Obviousness

Respondents argue that pursuant to 35 U.S.C. § 103, the asserted claims of the '345 patent are invalid as obvious over U.S. Patent No. 5,219,788 to Abernathey et al., entitled "Bilayer Metallization Cap for Photolithography" (RX-156)("Abernathey") in combination with any of several other publications.[62] *See, e.g.*, Respondents' Post Hearing Brief (Following the

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[61] Claim 13 covers the method of claim 9 "wherein the cap layer comprises a material selected from the group consisting of a silicon nitride material and an oxynitride material." Respondents argue that claim 13, while not anticipated by Tobben, would be obvious in view of Tobben because one skilled in the art would understand that silicon nitride and oxynitride would be ready substitutes for the silicon dioxide of Tobben. Respondents' Post-Hearing Brief (Following the November Hearing) at 21 (citing RPFF 492-494). Complainants argue that Respondents have not pointed to any evidence to that effect. The Tobben specification indeed discloses a cap layer of silicon dioxide, and further, at col. 3, lines 10-11, teaches that "the cap layer comprises a dielectric material." Thus, claim 13 would be obvious in view of Tobben as well as anticipated, as inherent in Tobben based on the teachings of the Tobben specification and the high level of skill in the art.

[62] The other publications discussed primarily in Respondents' briefing are: Pan et al., "Integrated Interconnect Module Development" (presented at the June 18-20, 1996 VMIC Conference) ("Pan")(RX-82); Yagi, "Multilevel interconnection technology in system LSI" (April 1996)("Yagi")(RX-85); and Yota et al., "Integration of ICP High-Density Plasma CVD with CMP and its Effects on Planarity for Sub-0.5 m CMOS Technology" (August 1996) ("Yota")(RX-86).

These publications contain detailed information concerning HDP CVD and gap filling, including etch-to deposition ratios. For example, Pan states: "HDP CVD oxide with properly selected deposition-to-sputter ratio can achieve consistent void-free gap-fill." RX-82 at 49; *see* Peltzer Tr. 836-837 (how one skilled in the art would combine Abernathey with Pan). Yota's

(continued...)

November Hearing at 24-26; Respondents' Post Hearing Reply Brief (Following the November Hearing at 20-21; Respondents' Supplement Brief (Following the December Hearing) at 24-26.

The Abernathey patent Abstract briefly explains the patent as follows:

> A process of patterning a conductive layer on a substrate avoiding webbing yet permitting high density patterning places two layers between the resist and the metal. The first layer is an antireflective coating such as titanium nitride applied to the metal. The second layer is a barrier comprising silicon such as sputtered silicon or SiO_2. The barrier layer may also be a thin coating of spin-on glass. The barrier layer prevents interaction between the TiN and acid groups which are generated during exposure of the resist. With this structure in place the resist is applied, exposed and developed.

RX-156 ('788 Abernathey Patent), Abstract.

Respondents argue, relying in part of the preferred embodiments detailed in the specification, that Abernathey discloses a bilayer cap for patterning a metalization layer using a deep UV photoresist; that the substrate of the Abernathey patent is coated with titanium, then coated with an aluminum/copper/silicon layer, then coated with titanium nitride, and then coated with a silicon layer; and that after applying a photoresist layer which is patterned, the underlying layers are etched to define wiring lines separated by gaps. It is argued that while the Abernathey patent does not expressly discuss a gap filling process to fill the gaps between the conductive metal wiring lines with dielectric insulation, Abernathey also does not pertain to completed

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[62] (...continued)
Abstract states: "The planarity and gap-fill requirements for interlevel dielectrics become increasingly stringent as design rules shrink below 0.5μm. * * * Results show that the etch-to-deposition ratio and the thickness of the HDP CVD oxide will influence the final topography (both profiles and step height) before CMP." RX-86 at 265. Yota proceeds to provide explicit information about the ratios used. *See, e.g.*, RX-86 at 266 ("The ratio was varied by changing the O_2/SiH_4 flow rate and the high frequency RF power applied. The E/D ratio splits are 0.25, 0.30. and 0.35, while the HDP thickness splits are 5300 Å, 6600 Å, and 7600 Å.").

devices and thus has no reason to disclose that then well-known process. Respondents argue that at least certain additional references, i.e., Pan, Yagi and Yota, disclose HDP CVD gap filling and can be combined with the Abernathey patent to show that the asserted claims of the '345 patent were invalid as obvious to one of ordinary skill in the art at the time of the alleged invention. According to Respondents, one of ordinary skill in the art would be motivated to combine the wiring line stack of Abernathey with the art discussing the HDP CVD process because the HDP CVD process was well-known in the art, including gap filling on the scale addressed by the '345 patent. *See, e.g.*, Respondents' Post-Hearing Brief (Following the November Hearing) at 25-26 (citing RPFF 716-722, 730, 732-733; Lur Tr. 106; CX-653C, including evidence from Complainants' files showing that Novellus advocated HDP CVD for .35 μm gap filling).

Complainants deny that Abernathey in combination with other art renders any asserted claims of the '345 obvious. *See, e.g.*, Complainants' Post Hearing Brief (Following the November Hearing at 16-18; Complainants' Post Hearing Reply Brief (Following the November Hearing at 20-21. It is argued that Respondents' arguments are fundamentally flawed because the SiO2 barrier layer in Abernathey (a "thin" 1000-1500 Å in thickness) could not possibly serve as a second ARC within the meaning of the claims of the '345 patent, and that SiO2 would not be understood to have antireflective properties. It is also denied that there would have been any suggestion or motivation in Abernathey to combine it with any reference that teaches gap filling with HDP CVD. In addition, it is argued that none of the combinations of art relied on by Respondents disclose that the second ARC or cap layer would be etched during HDP CVD (as required by '345 patent claims 4 and 12), or that the cap layers could be formed from the subset of materials as required in claims 13 and 21.

The Commission Investigative Staff also argues that Respondents failed to present clear and convincing evidence of obviousness. *See* OUII Post-Hearing Brief (Following the November Hearing) at 35-37.

At the time of the alleged invention of the '345 patent, one skilled in the art would have known that a TiN layer could be replaced by a better antireflective coating, or that a second antireflective coating could be used in addition to TiN. *See, e.g.*, Fair Tr. 1108-1109; RX-46. Furthermore, that a layer of silicon dioxide can serve as an antireflective layer, and that such information would be available to engineers using ordinary calculations of reflectivity, has already been addressed in connection with Tobben. Moreover, references such as RX-282 (*Silicon Processing for the VLSI Era, Vol. 1: Process Technology* by Wolf) at 371-73, which discusses the sputter deposition of silicon dioxide to provide dielectric layers, and RX-177 (*SPIE* Vol. 2438: "Investigations of deep ultraviolet photoresists on TiN substrates" by Dean et al.)(the "Dean" publication) at 519,[63] which discusses the use of silicon dioxide on TiN, demonstrates that the titanium nitride layer and the silicon dioxide on top, which is disclosed in Abernathey, satisfies the requirement of claim 1 of a first and second antireflective coating formed on the wiring line. The silicon dioxide layer in Abernathey (especially in view of Dean) forms a cap

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[63] The Dean publication states in part:

> Ultimately, the deposition of a 100 nm silicon dioxide film on the TiN effectively blocked proton access to the TiN film and eliminated footing. This observation provides one possible solution to DUV resist footing on TiN--deposit a thin inorganic layer that could act as an antireflective layer and that is easily removed (during the plasma etch stop?). Most organic spin-on antireflective layers also provide the necessary barrier layer, but those films are problematic due to defects, added cost, and etch complications

RX-177 at 519.

layer which protects and serves as a hard mask during etching if there is HDP CVD deposition as required by claim 9, and the titanium nitride layer between the SiO2 layer and the metal wiring line in Abernathey (and/or Dean) is the same as the protective layer in claim 21 of the '345 patent.

Abernathey discloses every element of the asserted claims of the '345 patent, except the step of HDP CVD deposition. Abernathey discloses no gap filling step because it is not the object of Abernathey to carry the process of manufacturing an integrated circuit to that point. However, the record is clear that anyone skilled in the art in 1996 knew that to make a useful product one would have to proceed from the teachings of Abernathey, and fill the gaps between the metal wiring lines with a dielectric material. *See, e.g.*, Peltzer Tr. 833; Fair Tr. 1418, 1424-1425. By 1996, the Novellus company, among others, was selling machines and telling customer and potential customers to use HDP CVD for void free (or substantially void-free) gap filling in metal wiring line patterns. *See* Fair Tr. 1422-1425. There is no doubt that those skilled in the art (especially the hypothetical person skilled in the art with a comprehensive knowledge of prior art, and especially a person with the advanced education and experience proposed by Complainants and accepted in this opinion) knew that gap filling was necessary, and that HDP CVD, along with HDP CVD equipment, was available to perform that task

Accordingly, the Abernathey patent combined with Pan (RX-82), Yagi (RX-85), or Yota (RX-86), each of which discloses the use of HDP CVD for gap filling, renders claim 1 on the '345 patent obvious.[64] Similarly, claim 3 is obvious in view of the combination because the

[64] Complainants did not address secondary considerations (objective indicia) in their main or reply briefs. Nor does it appear that Complainants proposed a set of findings for this factor. In (continued...)

mask layer in Abernathey is a patterned photoresist layer. Claim 4 is obvious in view of the combination because the second antireflective coating, if left on the first antireflective coating, is etched during the HDP CVD process. Claim 5 is obvious in view of the combination because of the disclosure of a barrier layer between the substrate and the wiring line layer. Claim 6 is obvious in view of the combination because the second antireflective coating may be removed after the HDP CVD process. Claim 7 is obvious in view of the combination because of the disclosure to use the second antireflective layer as a hard mask. Claim 8 is obvious in view of the combination because the second antireflective coating on the wiring lines has the cross section of a rectangle after etching. Claim 9, an independent claim, is obvious in view of the combination because the second antireflective layer comprises a "cap layer" which is above the TiN layer and which serves as an antireflective coating. (*See* "cap layer" definition under Complainants' construction of Claim 9). Claim 10 is obvious in view of the combination because of the disclosure to use the second antireflective layer as a hard mask. Claim 11 is obvious in view of the combination because the cap layer in Abernathey is an antireflective coating. Claim 12 is obvious in view of the combination because the cap layer (the second antireflective coating), if left on the first antireflective coating, is etched during the HDP CVD process. Claim 13 would be obvious in view of the combination because one skilled in the art would understand that silicon nitride and oxynitride would be ready substitutes for the silicon dioxide of Abernathey. Claim 14 is obvious in view of the combination because the cap layer

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[64] (...continued)
addition, the Administrative Law Judge is aware of no evidence in the record that is relevant to secondary considerations that would outweigh the technical evidence indicating obviousness of the asserted claims of the '345 patent.

(the second antireflective coating) has the cross section of a rectangle after etching. Claims 15 and 16 are obvious in view of the combination as inherent shapes for the cross section after etching or as an obvious cross-sectional shape for the cap layer (the second antireflective coating) after etching. Claim 19 is obvious in view of the combination because the cap layer (the second antireflective coating), if left on the first antireflective coating, is etched during the HDP CVD process and would necessarily be redeposited into the gaps during HDP CVD. Claim 20 is obvious in view of the combination because the mask layer is a patterned photoresist layer. Finally, asserted claim 21 is obvious in view of the combination of Abernathey with HDP CVD prior art because each and every element of claim 21, except for the use of HDP CVD, is expressly disclosed in Abernathey. *See* FF, Section VI; RX-62; RX-82; RX-85; RX-86; RX-169.

C. Anticipation Under 35 U.S.C. § 102(g)

In addition to their arguments pertaining to the invalidity of the asserted claims of the '345 patent over prior art, Respondents also argue that the asserted claims are invalid as anticipated pursuant to 35 U.S.C. § 102(g) in view of "documents and prior activities of several companies, including IBM, Applied Materials, and Conexant Systems, Inc. (formerly 'Rockwell Semiconductor Systems, Inc.')." It is argued that although priority of invention most frequently arises in the context of a contest between two or more entities seeking a patent, prior invention is also a ground for anticipation under 35 U.S.C. § 102, and a source for prior art in determining obviousness under 35 U.S.C. § 103. Respondents' Post-Hearing Brief (Following the November Hearing) at 27-30 (citing, *inter alia*, *Checkpoint Sys., Inc. v. United States Int'l Trade Comm'n*, 54 F.3d 756, 762 (Fed. Cir. 1995); *Texas Instruments, Inc. v. United States Int'l Trade Comm'n*, 988 F.2d 1165, 1177 (Fed. Cir. 1993)).

Complainants argue on several grounds that Respondents cannot show that any claim of the '345 patent is invalid under section 102(g). Complainants' Post-Hearing Reply Brief (Following the November Hearing) at 21-26.

The Commission Investigative Staff argues that Respondents have not shown by clear and convincing evidence that any claims of the '345 patent were anticipated under section 102(g). OUII Post-Hearing Reply Brief (Following the November Hearing) at 14.

The question of whether the asserted claims of the '345 patent are invalid pursuant to section 102(g) was the subject of scant briefing, and little or no testimony at the hearing. Respondents rely on deposition testimony and documentary evidence (along with a substantial number of proposed findings of fact) to make their arguments. Having considered the arguments and the evidence set forth by the parties, it has been determined that the record does not show by clear and convincing evidence each of the elements necessary to prove a case pursuant to section 102(g), including, for example, a clear exposition as to how each element of the asserted claims is found in the prior activities of IBM, Applied Materials, and Rockwell/Conexant Systems. Nevertheless, the evidence relied on by Respondents, which includes activities involving Dr. Pan of Applied Materials and Dr. Yota of Rockwell/Conexant (both of whom authored documents cited above in the obviousness discussion), illustrates the high level of sophistication in the art, even before the filing of the '345 patent application, pertaining to the use of HDP CVD, including the use of HDP CVD in connection with silicon dioxide and gap filling. *See* RPFF 554-685.

D. Disclosure of the Best Mode

The first paragraph of section 112 of the Patent Act provides:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, *and shall set forth the best mode contemplated by the inventor of carrying out his invention.*

55 U.S.C. § 112, ¶ 1 (emphasis added).

The Court of Appeals for the Federal Circuit has held that "[t]he purpose of the best mode requirement is to ensure that the public, in exchange for the rights given the inventor under the patent laws, obtains from the inventor a full disclosure of the preferred embodiment of the invention." *Dana Corp. v. IPC Ltd. Partnership*, 860 F.2d 415, 418 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989). The Federal Circuit has explained the best mode requirement, as follows:

> In short, a proper best mode analysis has two components. The first is whether, at the time the inventor filed his patent application, he knew of a mode of practicing his claimed invention that he considered to be better than any other. This part of the inquiry is wholly subjective, and resolves whether the inventor must disclose any facts in addition to those sufficient for enablement. If the inventor in fact contemplated such a preferred mode, the second part of the analysis compares what he knew with what he disclosed -- is the disclosure adequate to enable one skilled in the art to practice the best mode or, in other words, has the inventor "concealed" his preferred mode from the "public?" Assessing the *adequacy* of the disclosure, as opposed to its *necessity*, is largely an objective inquiry that depends upon the scope of the claimed invention and the level of skill in the art.

Chemcast Corp. v. Arco Indus. Corp., 913 F.2d 923, 927-28 (Fed. Cir. 1990) (emphasis in original).

The first prong of the above test involves a subjective inquiry, focusing on the inventor's state of mind at the time of filing. *U.S. Gypsum Co. v. Nat'l Gypsum Co.*, 74 F.3d 1209, 1212 (Fed. Cir. 1986); *Chemcast*, 913 F.2d at 928. The second prong involves an objective inquiry, focusing on the scope of the claimed invention and the level of skill in the art. *U.S. Gypsum,* 74 F.3d at 1212; *Chemcast*, 913 F.2d at 928. With respect to the second prong of the best mode requirement, the extent of information that an inventor must disclose depends on the scope of the claimed invention. *Engel Indus. v. Lockformer Co.*, 946 F.2d 1528, 1531 (Fed. Cir.1991); *see also Chemcast,* 913 F.2d at 927, 16 U.S.P.Q.2d at 1037 (an "objective limitation on the extent of the disclosure required to comply with the best mode requirement is, of course, the scope of the claimed invention"); *Randomex, Inc. v. Scopus Corp.*, 849 F.2d 585, 588, 7 U.S.P.Q.2d 1050, 1053 (Fed. Cir.1988) ("It is concealment of the best mode of practicing the claimed invention that section 112 ¶ 1 is designed to prohibit"). Accordingly, an inventor need not disclose a mode for obtaining unclaimed subject matter unless the subject matter is novel and essential for carrying out the best mode of the invention. *Applied Med. Resources Corp. v. United States Surgical Corp.*, 147 F.3d 1374, 1377, 47 U.S.P.Q.2d 1289, 1291 (Fed. Cir.1998).

Nevertheless, when a best mode relates directly to a claimed invention, it must be disclosed. *See Northern Telecom Ltd. v. Samsung Electronics*, 215 F.3d 1281 at 1289 (Fed. Cir. 2000)(discussing *Dana Corp. v. IPC*, 860 F.2d 415 (Fed. Cir. 1989), and *Northern Telecom v. Datapoint Corp.*, 908 F.2d 931 (Fed. Cir. 1990)). In *Dana*, the Federal Circuit held that the failure to disclose an unclaimed fluoride treatment, which was necessary for satisfactory performance of the claimed seal, was a violation of the best mode requirement. *Dana*, 860 F.2d at 419. Similarly, in *Datapoint*, the Court found that the failure to disclose special audiotapes for

capturing data, which the inventors preferred to conventional audio cassettes, was a violation of the best mode requirement, where the claim included the use of magnetic tapes. 908 F.2d at 940-41.

In this case, Respondents claim at the time of filing the '345 patent application, the inventors knew a best mode of practicing the claimed invention and deliberately withheld it in order to preserve trade secrecy. In particular, Respondents argue the '345 patent specification does not provide any information as to the parameters of the HDP CVD process, despite the fact that the applicants knew the complex algorithms for determining a proper etch-to-deposition ratio in varying situations, and knew the actual ratios for many specific situations. *See* Respondents' Post-Hearing Brief (Following the November Hearing) at 30-32; Respondents' Post-Hearing Reply Brief (Following the November Hearing) at 21-23.

Complainants deny that the applicants deliberately withheld knowledge of the HDP CVD process. Complainants further argue that the applicants were not required to disclose an "optimum" E/D ratio (or the ratio described in the patent) because the subject matter of the '345 patent reaches many uses for which the applicants' actual [ ] E/D ratio would be inappropriate inasmuch as appropriate E/D ratio will depend on a number of factors -- including the feature size, aspect ratio, metal profile, cap layer composition (if any), type of machine and materials used, and other manufacturer choices. Thus, Complainants argue, experimentation will always be required to determine the values of the parameters for finding an appropriate E/D ratio to match the particular needs of the manufacturer. It is argued that the applicants' lack of disclosure of mere production details does not violate the best mode requirement. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 31-35; Complainants' Post-Hearing Reply

Brief (Following the November Hearing) at 19-21.

The Commission Investigative Staff argues that the process value in the patent depends upon several parameters that are only known to the end-user practicing the patent, and thus the applicants' failure to include a specific value in the specification is not a violation of the best mode requirement. The Staff believes the patent is not limited to a specific feature size, but that the E/D ratio varies with feature size, equipment and the materials used. *See* OUII Post-Hearing Brief (Following the November Hearing) at 37-39.

The use of the HDP CVD process to fill gaps between metal wiring lines had been discussed in a number of published sources prior to the conception of the '345 invention in 1996. *See* Lur Tr. 105-106. Indeed, the '345 patent does not, and could not, claim as an invention the HDP CVD process to fill gaps between metal wiring lines. A number of factors must be taken into consideration to arrive at any proper E/D ratio (including silane flow rate, oxygen flow rate, argon flow rate, helium flow rate, ratio of oxygen to silane, low frequency RF power, high frequency RF power, pedestal height, pressure and temperature). As one of the named inventors testified, "what is important is the series of processes that were used to determine the E/D ratio, not the E/D ratio itself." Liu Tr. 545-555.

The hearing testimony shows that at least one reason why the applicants did not disclose information about how they arrived at the correct E/D ratio was that they did not want to disclose competitive information. *See* Lur Tr. 121-122, 551. However, it appears that the concern was concentrated on UMC's particular manufacturing parameters apart from the claimed invention, and not a fear that competitors would actually be able to determine E/D ratios for themselves and use the claimed invention. Nor does it appear that there is a best way of implementing the

claimed invention with respect to E/D ratios. For example, persons skilled in the art could implement the claimed invention by using a variety of equipment to manufacture devices of various sizes.

Respondents' expert testified that the disclosure of UMC's E/D ratio for its 0.25 micron products would have been useful "signposts" or "buoys" for determining E/D ratios for other products.[65] Peltzer Tr. 845. However, it does not appear that the '345 patent fails to disclosure information that would not be readily available to those skilled in the art, or that disclosure of the production details pertaining to UMC's E/D ratio would have greatly assisted others in determining their own appropriate E/D ratios. In summary, there is not clear and convincing evidence that Complainants failed to describe anything that could genuinely be described as a best mode.[66]

VII. DOMESTIC INDUSTRY

In a patent-based investigation, section 337 requires that an industry in the United States relating to the patent or to articles protected by the patent exist or be in the process of being established. 19 U.S.C. §1337(a)(2). The statute further provides that:

> [A]n industry in the United States shall be considered to exist if there

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[65] Such "signposts" or information were available to those skilled in the art, including information from HDP CVD equipment manufacturers (whose particular equipment would require the use of different ratios). *See* Peltzer Tr. 972-975; Lur Tr. 512-517, 530-531; CX-41C; CX-653C; CX-654C.

[66] It is noted, however, that if Complainants' arguments about the supposed insufficiency of the prior art were adopted, a different conclusion on the issue of "best mode" might be compelled. For example, Complainants argue that HDP CVD was an "immature technology." CPRF 704. *See also* CPRF 456 ("[W]hether the second antireflective coating was etched would depend on the etch-to-deposition ratio used in the HDPCVD process."); CPRF 490 ("[W]hether or not a cap layer is etched will depend on the etch-to-deposition ratio used in the HDPCVD process.").

> is in the United States, with respect to the articles protected by the patent ... concerned –
>
> (A) significant investment in plant and equipment;
>
> (B) significant employment of labor or capital; or
>
> (C) substantial investment in its exploitation, including engineering, research and development, or licensing.

19 U.S.C. §1337(a)(3).

In most cases, the domestic industry requirement consists of two prongs: the technical prong and the economic prong. *Certain Variable Speed Wind Turbines and Components Thereof*, Inv. No. 337-TA-376, USITC Pub. 3003, Comm'n Opinion at 14-17 (1996). "The technical prong involves whether the complainant practices the asserted patents; the economic prong involves investment activities, set out in section 337(a)(3), in a domestic industry with respect to articles protected by the asserted patents." *Id.* However, it is not always necessary to show that the products of the complainant or its licensees are covered by the patent. For example, when a domestic industry exists under subsection 337(a)(3)(C) due to a substantial investment made in the licensing of a patent, it is not necessary to prove that a patent holder or licensee is involved in actual domestic production. *See Certain Semiconductor Chips with Minimized Chip Package Size and Products Containing Same*, Inv. No. 337-TA-432, Order No. 13 (Jan. 24, 2001)(unreviewed Initial Determination); *Semiconductor Chips*, Notice of a Commission Determination Not to Review (Feb. 26, 2001)(EDIS Document Identification No. 200102260025).[67]

[67] Whether a licensing program could constitute a domestic industry was an open question until section 337 was amended to provide specifically for such an industry. *See, e.g., Certain* (continued...)

In this investigation, there is no evidence that products which exploit the '352 or '345 patent are manufactured in the United States. It is uncontested that all of UMC's products at issue are made overseas. Nor do Complainants rely on domestic manufacture by any licensee. Nevertheless, with respect to both patents, Complainants argue (and with respect to the '345 patent, the Commission argues) that a domestic industry exists due to Complainants' investments and activities in the United States that relate to or exploit the patent. It is alleged that Complainants provide design-related assistance and information about UMC products and design rules so that companies in the United States can purchase and use Complainants' products which allegedly practice the '352 and/or '345 patents. *See, e.g.*, Complainants' Post-Hearing Brief (Following the November Hearing) at 1-11.

As a threshold technical matter, Respondents have stipulated that all of Complainants' products at issue practice the '345 patent. *See, e.g.*, Stipulation to Further Revise the Prehearing Schedule (Oct. 16, 2001), ¶ 26; RPFF 1005. However, Respondents deny that any of Complainants' products practice the '352 patent. *See* Respondents' Post-Hearing Brief (Following the November Hearing) at 34-37. The Commission Investigative Staff similarly argues that Complainants practice the '345 patent, yet argues that they do not practice the '352 patent. *See* OUII Post-Hearing Brief (Following the November Hearing) at 40.

The parties agree that the dispute concerning the technical prong for the '352 patent can

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[67] (...continued)
Soft Sculpture Dolls Popularly Known as "Cabbage Patch Kids," Related Literature and Packing Therefor, Inv. No. 337-TA-231, Comm'n Decision to Review Portions of an Initial Determination Finding a Violation of Section 337 of the Tariff Act of 1930 (Sept. 4, 1986)(51 Fed. Reg. 31731 (1986)(referring to *Certain Products with Gremlin Character Depictions*, Inv. No. 337-TA-01)).

be resolved as a matter of claim construction. *See, e.g.*, Stipulation to Further Revise the Prehearing Schedule (Oct. 16, 2001), ¶ 25; Complainants' Post-Hearing Brief (Following the November Hearing) at 1. Indeed, there is no material dispute concerning the structure and function of the UMC devices in question. The dispute centers on the fact that UMC's ESD devices [

], and the parties disagree as to how the term "source/drain regions" (and related terms such as "source/drain region" and "gate") should be construed.

As detailed above in discussing the '352 patent claims, it is shown that the intrinsic and extrinsic evidence requires a claim construction in which the term "source/drain regions" refers to: (1) each and every source of each and every transistor for the ESD protection device, and (2) each and every drain of each and every transistor for the ESD protection device. As such, the '352 patent claims must be construed to require that all of the sources and all of the drains of the ESD protection devices' transistors have "a lightly implanted region." Furthermore, contrary to Complainants' proposed claim construction, it has been determined that "a gate" covered by the '352 patent must be associated with a specific FET. In general, Complainants' proposed claim construction has not been adopted, and there has been a determination of noninfringement of the asserted claims of the '352 patent. Similarly, it is not found that the UMC products practice any claim of the '352 patent. Therefore, given the nature of Complainants' domestic industry arguments (which rely on UMC's alleged practice of the asserted patents), Complainants cannot establish that the domestic industry requirement of section 337 is satisfied with respect to the '352 patent.

A question remains as to whether the requisite domestic industry exists with respect to the

'345 patent, which UMC practices. Over the past few years, Complainants have employed [ ] people in the United States and invested [ ] dollars domestically in plant and equipment, employee salaries, and engineering.[68] There appears to be no dispute concerning the question of whether or not such activities and investments are "substantial" or "significant," as required by the section 337 statute. Regardless of how one would allocate Complainants' activities and expenditures, they would be adequate from a simple financial or personnel perspective to satisfy the domestic industry requirement. The dispute arises with respect to whether or not Complainants' domestic activities and investments are carried out "with respect to articles protected by the patent" or relate to the "exploitation" of the patent, as required by the statute, i.e., whether there is a "nexus" between the '345 patent and the activities and investments relied on by Complainants.

As argued by Respondents, the domestic industry requirement was retained to preclude holders of U.S. intellectual property rights who have no other contact with the United States from using section 337. Furthermore, the mere marketing and sale of products in the United States is insufficient to constitute a domestic industry. *See* Respondents' Post-Hearing Brief (November Hearing) at 42-43 (citing, *inter alia*, S. Rep. No. 71, 100th Cong. 1st Sess., at 129 (1987); H.R. Rep. No. 40, 100th Cong., 1st Sess., pt. 1, at 157 (1987)). However, as Complainants argue, Section 337(a)(3)(C) may include "application engineering, design work or other such activities."

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[68] Some of the research and development evidence relied on by Complainants pertains exclusively to the '352 patent. *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 5. Inasmuch as there is no proof that Complainants practice the '352 patent, and Complainants' interpretation of the '352 patent claims differs materially from the proper construction determined in this opinion, that evidence has not been considered. Such evidence is irrelevant to the question of whether or not a domestic industry exists with respect to the '345 patent.

Complainants' Post-Hearing Reply Brief (Following the November Hearing) at 4 (citing H.R. Rep. 40, 100th Cong., 1st sess., at 157 (1987), and S. Rep. No. 71, 100th Cong., 1st Sess., at 130 (1987)).

It has long been recognized that a variety of domestic activities and investments may satisfy the domestic industry requirement of section 337, even when the actual production of articles protected by the patent may take place overseas. For example, in *Certain Diltiazem Hydrochloride and Diltiazem Preparations*, Inv. No. 337-TA-349, USITC Pub. No. 2902, Comm'n Opinion at 134, 144-45 (June 1995), the patent at issue covered a method for producing bulk diltiazem HCl. As evidence of a domestic industry, the Commission cited the complainants' substantial investments in the United States relating to the development of diltiazem HCl in dosage form, as well as to investments connected to testing that was necessary to satisfy the requirements of the U.S. Food and Drug Administration. *See also Schaper Mfg. Co. v. United States Int'l Trade Comm'n*, 717 F.2d 1368, 1373 (Fed. Cir. 1983) (in proper cases, "industry" may encompass more than the manufacturing of the patented item); *Certain Salinomycin Biomass and Preparations Containing Same*, Inv. No. 337-TA-370, Commission Opinion at 120-28 (October 10, 2000)(domestic industry found where the complainant performed additional processing in the United States of salinomycin produced abroad).

Furthermore, the Commission Investigative Staff and Complainants rely in part on *Certain Microcomputer Memory Controllers, Components Thereof And Products Containing Same*, Inv. No. 337-TA-331, Order No. 6, (unreviewed) Initial Determination (Jan. 8, 1992); *Microcomputer Memory Controllers*, 57 Fed. Reg. 5170 (Feb. 12, 1992), a summary determination that has some parallels with this case. The patent at issue related to certain

personal computer components, referred to as "chipsets." The Administrative Law Judge granted the complainant's motion for summary determination as to the "economic prong" of the domestic industry requirement even though the chipsets were manufactured overseas. The Administrative Law Judge noted that the complainant had made substantial pre-manufacturing investments in research and development relating to the chipsets, including collaboration between the complainant's engineers and prospective customers in the initial design of the chipsets needed by the customers, and the efforts of complainant's engineers to debug those new designs. It was determined that there was no reason to compare the relative amount of work done in the United States to that done in a foreign country in manufacturing the products, or to compare "value added" by labor in a foreign country to the original cost of exploitation of the patents in the United States. As adopted by the Commission, the Administrative Law Judge's conclusion was that "the customer participation in R & D and the engineering support that complainant gives to customers can be included in a broad definition of research and development under subsection (C) [of section 337(a)(3)]." *Microcomputer Memory Controllers*, Order No. 6 (unreviewed Initial Determination) at 1-4.

In this investigation, the evidence shows that Complainants have made substantial investments in the United States to assist customers in the design of integrated circuits that are allegedly covered by the patents at issue. Specifically, an initial step in the process of producing an integrated circuit is to develop an integrated circuit design that conforms to certain essential manufacturing parameters that are referred to as "design rules." *See* Wan Tr. 651-662; Peltzer Tr. 865-886. The evidence shows that Complainants work with their U.S. customers to test the customers' integrated circuit designs to ensure that they are in compliance with the UMC design

rules. If a customer's design does not comply with the design rules, then Complainants will work with that customer to modify the design to bring it into compliance. Lam Tr. 596-597; Wan Tr. 665-666. In an effort to address this compliance problem, Complainants have also hired third-party vendors in the United States to create and maintain libraries of compliant designs for various integrated circuit components. Wan Tr. 667-670. Therefore, customers have the option of building their integrated circuit designs by adapting pre-approved component designs that are stored in the libraries.

To support these activities in the United States, Complainants have leased [ ] square feet of office space in California at a cost of about [ ] over the last [ ] years, and [ ] of that office space is devoted to providing engineering support to assist customers and third-party vendors in the design of integrated circuits that comply with the design rules. Chen Tr. 453. The evidence also shows that Complainants spent [ ] to prepare that office space for use as a design support facility and spent approximately [ ] to improve further the office space and purchase office equipment and computer hardware and software, much of which is dedicated to providing engineering support to assist UMC customers and third-party vendors to design UMC articles. *See* Chen Tr. 458; CX-237. Undisputed evidence shows that Complainants employ [ ]customer and field engineers who are paid a total of approximately [ ] in salaries and benefits to assist customers in the design of compliant integrated circuits and engage in marketing and sales activities. *See* Chen Tr. at 458; CX-687. In addition, Complainants paid approximately [ ] million to domestic third-party "library vendors" to produce the design libraries that can be referenced by customers in order to create compliant integrated circuit designs that will be produced through the practice of the

method covered by the '345 patent method. *See* Chen Tr. 463; CX-692.

The crux of Respondents' argument is that Complainants' domestic activities cannot provide the basis for a domestic industry because Complainants have not established a nexus between their domestic activities and the patents at issue, and that Complainants' circuit design support is merely sales and marketing activity that cannot form the basis of a domestic industry. *See, e.g.*, Respondents' Post-Hearing Brief (Following the November Hearing) at 43; Respondents' Post-Hearing Reply Brief (Following the November Hearing) at 1-6. However, in this investigation, the record demonstrates that Complainants' activities go beyond mere sales and marketing. Complainants have made substantial investments in engineering and development in the United States, including circuit design support and the debugging of circuit designs that will then be used to produce integrated circuits that are covered by the '345 patent at issue.

In addition, on the question of "nexus" or exploitation of the asserted patents, the hearing testimony showed that certain features of the UMC design rules directly relate to the process of the '345 patent. For example, in order to permit use of the '345 patent's manufacturing processes and technologies, including the filling of gaps between wiring lines using UMC's particular HDP CVD recipes and the cap layer, the wiring lines in a customer's design must adhere to UMC design rules that limit the maximum aspect ratios for those wiring lines. Liu Tr. 518, 523-526. The aspect ratio for wiring lines is the ratio of the height of the wiring lines to the space between the wiring lines. Liu Tr. 517-518. In general, the greater the aspect ratio, the more difficult it is to fill gaps between wiring lines, and where aspect ratios are increased, adjustments must be made in the HDP CVD recipes used by a manufacturer so as to increase the

E/D ratio, and corresponding changes may be needed in the cap layer used to protect the wiring lines from corner clipping during the HDP CVD process. Liu Tr. 518-519, 526. In order to ensure the proper minimum spacing between wiring lines, UMC's [ ] for each generation of technologies include minimum wiring line spacing rules for each metal level within a customer's integrated circuit design. Liu Tr. 524-525; Yang Tr. 565-566; Lam Tr. 602; CX-162C at 18, 20, 22, 24, 26; CX-163C at 16, 18, 20, 22, 24, 26; CX-161C at 10, 12, 14, 16, 18. Furthermore, for each generation of technology, UMC has an [ ] that specifies the height of wiring lines for each metal level within an integrated circuit. Liu Tr. 525- 526; CX-167C at UMC 100334. Thus, the UMC [ ] and [ ] provide design rules that establish the aspect ratios to be used in customer designs, and the steps taken by Complainants to ensure compliance with those rules ensure that production of customer designs at UMC's foundries can be accomplished effectively using the manufacturing processes and technologies of the '345 patent. *See* Liu Tr. 526.

In accordance with the Commission's prior determinations, *e.g.*, in the *Diltiazem*, *Microcomputer Memory Controllers*, and *Salinomycin* investigations, there is in this case a sufficient nexus between Complainants' domestic activities and investments and the patents at issue so as to satisfy the economic prong of the domestic industry requirement under section 337(a)(3)(C).[69]

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[69] Complainants argue that the evidence demonstrates that their activities and investments satisfy the domestic industry requirement with respect to all three subparts of section 337(a)(3). *See* Complainants' Post-Hearing Brief (Following the November Hearing) at 9-10. However, it is necessary only to satisfy one of those subparts. The evidence of record relevant to the domestic industry issue clearly shows that there exists a domestic industry under section 337(a)(3)(C), and it is not necessary to make further determinations as to section

(continued...)

Accordingly, the evidence demonstrates that Complainants have satisfied the "technical prong" and the "economic prong" of the domestic industry requirement as to the '345 patent by virtue of their activities and investments which assist customers to design integrated circuits that will be made according to the '345 patented method, and thus a domestic industry exists in satisfaction of the requirements of section 337(a)(2).

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[69] (...continued)
337(a)(3)(A)-(B).

FINDINGS OF FACT

I. BACKGROUND

1. United Microelectronics Corporation ("UMC") is a Taiwanese corporation based in Hsinchu City, Taiwan. UMC is the owner of the patents at issue and is a manufacturer of integrated circuits. Complaint, ¶ 2.1, p. 3, ¶ 2.2, p. 3; Lee Tr. 479.

2. UMC Group (USA) ("UMC-US") is a California corporation based in Sunnyvale, California, and is a wholly owned subsidiary of UMC. Complaint, ¶ 2.3, p. 3; Chen Tr. 451-452. UMC-US markets and sells UMC's manufacturing services to U.S.-based integrated circuit design customers. *Id.*; Wan Tr. 651.

3. United Foundry Services, Inc. ("UFS") is a California corporation based in Hopewell Junction, New York. Complaint, ¶ 2.5, p. 4.

4. UFS is also a wholly owned subsidiary of UMC and is in the business of research and development of manufacturing processes for integrated circuits. Complaint, ¶ 2.6, p. 4 Tang Tr. 444; Chen Tr. 453-460.

5. Silicon Integrated Systems Corp. ("SiS-TW") is a Taiwanese corporation with its principal place of business in Hsinchu City, Taiwan. Complaint, ¶ 3.1, pp. 4-5.

6. Silicon Integrated Systems Corporation ("SiS-US") is a California corporation with its principal place of business in Sunnyvale, California, and is a wholly owned subsidiary of SiS-TW. Complaint, ¶ 3.2, p. 5; RPFF 4. Complainants allege that SiS-US offers for sale and sells after importation the accused integrated circuits. Complaint, ¶ 3.2, p. 5.

7. U.S. Patent No. 5,559,352 ("the "352 patent") issued on September 24, 1996 and is entitled "ESD Protection Improvement." CX-2/RX-1 ('352 Patent).

8. U.S. Patent No. 6,117,345 ("the '345 patent") issued on September 12, 2000 and is entitled "High Density Plasma Chemical Vapor Deposition Process." CX-1/RX-40 ('345 Patent).

II. IMPORTATION AND SALE

9. The importation or sale requirement of section 337 has been established for the purposes of this Initial Determination. Order No. 15 (Initial Determination); Commission Notice Not to Review (Dec. 5, 2001); Commission Notice Not to Review (Dec. 3, 2001). *See also* CPFF 972-1028, 1029-1029, 1041-1110 (uncontested proposed findings of fact relating to the issue of importation and/or sale).

III. INFRINGEMENT OF THE '352 PATENT

A. Claim Construction

10. The '352 patent relates to the production and manufacture of input protection devices that are used in integrated circuits, wherein these devices are used to protect other devices in the integrated circuits from electrostatic discharge ("ESD"). CX-2, col. 1, lines 15-21.

11. There is a relationship between the ESD protection device or circuit and the device or circuit being protected, as shown in several figures of the '352 patent.

12. Figures 1 and 7 of the patent show an ESD protection device or circuit (item 10) that is protecting an internal circuit (item 12). CX-2, col. 2, lines 43-44.

13. In Figure 8, an ESD protection device (item 40) protects an internal CMOS device (item 42). *Id.*, col. 4, lines 43-46 and 54-56.

14. ESD devices are required because during the handling and operation of integrated circuits using FET technology significant electrostatic charges may be transferred from the

integrated circuit's external contacts into the interior of the circuit, thus causing damage to and even destruction of the circuit's FET devices. *Id.*, col. 1, lines 20-26.

15. To reduce or eliminate such electrostatic charge-related damage, input protection devices are placed between the integrated circuit's external contacts and the FET devices. *Id.*, col. 1, lines 20-31.

16. These ESD protection devices are designed to provide a path that safely discharges the electrostatic charge, thus preventing damage to the internal FET devices of the integrated circuit being protected. *Id.*, col. 1, lines 29-31.

17. In a preferred embodiment disclosed in the patent, several processing steps are undertaken to manufacture the FETs that act as both the ESD protection device and the device being protected. CX-2, col. 1, line 50 to col. 2, line 29. Figures 1-7 illustrate a total of two FETs (items 10 and 12), one of which (10) serves as the ESD protection device.

18. In the '352 patent, the ESD protection device (item 10) and the internal FET device, *i.e.*, the circuit being protected (item 12), are formed at the same time on a single P-substrate (item 14). *Id.*, col. 2, lines 43-46; Fig. 1. "P-substrate" refers to conductivity-type of the substrate. *See e.g.*, claims 1 and 2.

19. Then, oxide regions (item 16), which isolate the protection device and the circuit being protected, are formed. *Id.*, col. 2, lines 46-49; Fig. 1.

20. Next, gate layers (items 18) are deposited for each of the circuits (items 10 and 12). *Id.*, col. 2, lines 51-53; Fig. 1.

21. Fourth, a gate electrode, consisting of gate oxide and a gate (item 20), is formed for each

circuit by patterning the gate layer with conventional lithography and etching. *Id.*, col. 2, lines 53-56; Fig. 1.

22. The gate electrode consists of the gate and a gate oxide located below the gate, hence the gate "forms in part" the gate electrode. RX-1, col. 2, lines 54-56).

23. Next, a first ion implant of N^- material (item 22) is performed. *Id.*, col. 2, lines 57-62; Fig. 2.

24. This implant forms the source and drain regions of the protection device and the internal FET device. *Id.*

25. An insulating layer, *e.g.*, SiO_2 (silicon dioxide) is deposited over the entire surface by chemical vapor deposition ("CVD"). *Id.*, col. 2, lines 63-67.

26. Thereafter, a portion of the insulation layer is etched away to form spacers (items 24) on each side of the gates of the device and the FET. *Id.*, col. 2, line 63 to col. 3, line 2; Fig. 3.

27. A heavy ion implant, which is followed by a drive-in step, is performed. *Id.*, col. 3, lines 3-7; Fig. 4.

28. As a result of the ion implant and drive-in step, the previously formed source/drain regions (*id.*, col. 2, lines 57-62; items 22 in Figs. 2 and 3) have a lightly doped N^- region under the spacers (items 26 in Fig. 4), while the rest of the source/drain regions are N^+ (items 28 in Fig. 4). *Id.*, col. 3, lines 7-10.

29. An insulting layer (item 30) is formed over the entire structure. *Id.*, col. 3, lines 12-15; Fig. 5.

30. This insulating layer is then patterned using lithography and etching to form contact

openings (items 32) above the source/drain regions (items 28). *Id.*, col. 3, lines 18-21; Fig. 5.

31. A photoresist (item 34) is formed over only the FET device (item 12) (*i.e.*, the circuit being protected). *Id.*, col. 3, lines 23-25; Fig. 6.

32. This photoresist "masks" the FET device (item 12). *Id.*

33. Next, the invention's "critical step" is performed: a light ion implant of opposite conductivity (P^-) (items 36) is performed through the contact openings (items 32) into the protection device's active regions (items 28). *Id.*, col. 3, lines 22-27; Fig. 6.

34. The purpose of the ion implant is to reduce the device's junction breakdown voltage from approximately 10-14 volts to around 5-8 volts. *Id.*, col. 3, lines 31-35.

35. Breakdown voltage is inversely proportional to a substrate's impurity concentration. *Id.*, col. 3, lines 37-39.

36. Adding the P^- regions (items 36) increases the impurity concentration at the location between the ESD device's active regions (items 28) and the substrate (item 14), which is P^- even prior to the implant. *Id.*, col. 2, lines 43-46; col. 3, lines 41-45.

37. A reduction in breakdown voltage improves the protection device's ESD characteristics, since breakdown voltage of a "p-n junction" (*i.e.*, the area between the ESD device's active regions (items 28) and the substrate (item 14)) is inversely proportional to the substrate impurity concentration. *Id.*, col. 3, lines 40-45. ESD characteristics and breakdown voltage are related in that a reduction in breakdown voltage allows more electrical current to be discharged through the protection device (item 10) for a given amount of power. *Id.*, col. 3, lines 40-50.

38. Finally, the photoresist (item 34) is removed from the device (item 12) being protected. *Id.*, col. 3, lines 58-61; Fig. 7.

39. Figures 8 and 9 show, *inter alia*, an (1) ESD protection circuit (item 40) with two FETs (items 72 and 74) made in accordance with the above-described steps, and (2) an I/O ("input/output") pad (item 70).

40. Electrostatic discharges will enter through the I/O pad but be prevented from damaging the circuit being protected, which consists of FETs 76 and 78. CX-2, col. 4, lines 46-48.

41. A grounded "voltage source" would be unreasonable and disfavored by an engineer of ordinary skill. Peltzer Tr. at 767-78.

42. Dr. Fair admits that his definition of "voltage source" is based upon a textbook that predates the invention date of integrated circuits. Fair Tr. at 249.

43. The named inventors of the '345 patent are Chen-Chiu Hsue and Joe Ko. RX-1; Hsue Tr. 1144:24 to 1145:8, 1158:14-17.

44. Mr. Hsue has a Bachelor's Degree in electro physics and a Master's Degree in electronic engineering. Hsue Tr. 1130:6-10.

45. Joe Ko's formal Chinese name is Tsung-Hsi Ko. JX-12C Hsue 8/14 Dep. Tr. 32:3-6.

46. Mr. Ko has a Bachelor's Degree in electrical engineering, and no further degrees. JX-20C Ko Dep. Tr. 4:20-24, 5:2-4.

47. The '352 patent issued from Application No. 08/354,373 ("the '373 application"), filed December 12, 1994. RX-1, RX-2, Filing Under 37 C.F.R. 1.60 dated December 8, 1994.

48. The '373 application is a divisional of Application No. 08/139,858, filed October 22, 1993. RX-1, RX-2, Filing Under 37 C.F.R. 1.60 dated December 8, 1994.

49. A field effect transistor (FET) is a typical metal oxide silicon (MOS) transistor, and contains three essential elements, a source, a gate and a drain. A lightly doped drain (LDD) is an additional region within each source region and drain region. The LDD is a small region of higher resistivity than the source region or drain region which slows down electrons to keep them from sticking in the gate oxide under the gate. Peltzer Tr. 708:7-19.

50. Formation of the second lightly implanted region is the critical step of the invention described in the '352 patent (paragraph bridging pages 7 and 8). JX-12C Hsue 8/16 Dep. Tr. 248:6-15.

51. The "second lightly implanted region" recited in the claims of the '352 patent is of the same conductivity type as the substrate and has the effect of reducing the junction breakdown voltage of the device. Peltzer Tr. 716:12-17; RPX-10, region 36 marked in blue; RX-1, col. 3, lines 25-35 and Fig. 7.

52. Figure 9 of the '352 patent is the disclosed embodiment of the ESD protection circuit claimed in claim 8. RX-1.

53. Of the asserted claims, claims 1 and 8 of the '352 patent are independent and claim 2 is dependent. RX-1.

54. The '352 Patent is a division of Application Ser. No. 139,858 ("the '858 Application"), filed Oct. 22, 1993, U.S. Pat. No. 5,374,565 ("the '565 patent"). The '858 Application, as filed, contained both product claims and process claims; specifically, two product claims (claims 7 and 8) and six process claims (claims 1-6). The product claims of the '858 Application read as follows:

7. An ESD protection device with reduced junction breakdown voltage, connected to an integrated circuit which includes FET devices, comprising:

field oxide regions in and on a silicon substrate for isolation of said ESD protection device;

gates with adjacent spacers for [for] said ESD protection device, between said field oxide regions;

source/drain regions for said ESD protection device between said gate and said field oxide regions, with a heavy ion implant; and

source/drain regions for said ESD protection device between said gate and said field oxide regions, with a first lightly implanted region under said spacers, a heavier implanted region of same conductivity as said light ion implant between said first lightly implanted region and said field oxide regions, and a second lightly implanted region of opposite conductivity centered under said heavier implanted region.

8. The ESD protection device of claim 7 wherein said reduced junction breakdown voltage of said device is between about 5 and 8 volts.

RX-11, specification pages 17-18.

55. In the first Office Action issued in the '858 application, the Examiner pointed out that the claimed product invention was distinct from the claimed method invention, and issued a restriction requirement. The Applicants were required to elect which of the two inventions would be examined in the '858 application. RX-11, Official Action issued April 19, 1994 .

56. The Applicants elected the process claims, and the product claims were cancelled in the '858 Application. RX-11, Response to Restriction Requirement dated May 10, 1994.

57. After the Applicants' election, one of their attorneys had a telephone interview with the

Examiner, following which the Examiner allowed the six process claims and canceled both product claims from the application. U.S. Patent No. 5,374,565 ("the '565 Patent") was issued from the '858 Application, that patent containing the six process claims. RX-11, Examiner Interview Summary Record dated August 2, 1994.

58. The papers filed with the '373 application included a copy of the '858 application together with a Preliminary Amendment. The Preliminary Amendment amended claim 7 (the original independent product claim), canceled claim 8, and added seven new claims, i.e., claims 9-15. New claims 9-14 were dependent claims, depending directly or indirectly from amended claim 7, while new claim 15 was an independent claim. RX-2, Preliminary Amendment dated December 8, 1994.

59. During the pendency of the '565 Patent, and before the '373 application was filed, the patent Examiner had cited U.S. Patent No. 4,968,639, issued November 6, 1990, to Bergonzoni (RX-13), and identified it as well as other patents to the patent attorney. RX-11, Notice of Reference Cited, form PTO-892, dated August 2, 1994; RX-13.

60. The attorney who filed the '373 Application and the preliminary amendment was the attorney of record in the '565 Patent. RX-11, Declaration and Power of Attorney for Patent Application, executed September 29, 1993; RX-2, Filing Under 37 CFR 1.60, dated December 8, 1994.

61. Claim 7 as amended in the '373 Application appears as follows, with material added to the claim being underlined, and material deleted from the claim being enclosed by square brackets.

> 7. (AMENDED) An ESD protection device with reduced junction breakdown voltage, connected to an integrated circuit

which includes FET devices, comprising:

a silicon substrate having a first conductivity type;

field oxide regions in and on [a] said silicon substrate for isolation of said ESD protection device;

a gate[s] with adjacent spacers for [for] said ESD protection device, between said field oxide regions;

[source/drain regions for said ESD protection device between said gate and said field oxide regions, with a heavy ion implant; and]

source/drain regions for said ESD protection device between said gate and said field oxide regions, with each source/drain region comprising:

a first lightly implanted region having a second conductivity type opposite to said first conductivity type, under one of said spacers[,];

a heavier implanted region of the same conductivity type as said [light ion implant between] first lightly implanted region, located between said first lightly implanted region and one of said field oxide regions[,]; [and]

a second lightly implanted region of [opposite] same conductivity type as said silicon substrate, centered under said heavier implanted region.

RX-2, Preliminary Amendment dated December 8, 1994.

62. The patent attorney filed remarks together with the claim changes in the Preliminary Amendment, and in those remarks he pointed out that:

> The amended Claims are believed to clarify the invention and put the application in condition for allowance.

RX-2, Preliminary Amendment dated December 8, 1994.

63. New claim 15, presented in the Preliminary Amendment, was directed to "An ESD protection circuit" which utilizes two ESD protection devices of the type claimed in claim 7. Specifically, claim 15 read as follows:

> 15. An ESD protection circuit, having first and second ESD protection devices, connected to an integrated circuit which includes FET devices, and connected to an input/output pad, comprising:
>
> a silicon substrate having a first conductivity type;
>
> field oxide regions in and on [a] said silicon substrate for isolation of said ESD protection devices;
>
> gates with adjacent spacers for each of said ESD protection devices, between said field oxide regions;
>
> source/drain regions for said ESD protection devices between said gates and said field oxide regions, with each source/drain region comprising:
>
> > a first lightly implanted region having a second conductivity type opposite to said first conductivity type, under one of said spacers;
> >
> > a heavier implanted region of the same conductivity type as said first lightly implanted region, located between said first lightly implanted region and one of said field oxide regions;
> >
> > a second lightly implanted region of same conductivity type as said silicon substrate, centered under said heavier implanted region;
>
> a first electrical connection between said input/output pad, said drain regions of said first and second ESD protection devices, and said integrated circuit;
>
> a second electrical connection to ground of said gates of said first and second ESD protection devices, and said source region of said second ESD protection device; and

a third electrical connection, to a voltage source, of said source of said first ESD protection device.

RX-2, Preliminary Amendment dated December 8, 1994.

B. Infringement Determination

64. Subject to importation, domestic industry and Respondents' affirmative defenses, the parties have agreed and stipulated that the issue of infringement with respect to the '352 patent in this investigation can be resolved based solely on claim construction of the patent. Stipulation to Further Revise Prehearing Schedule dated October 16, 2001, Stipulation 22.

65. [

].

66. [

]

67. The parties have stipulated that: (1) if Respondents' E6 model ESD transistor is found not to infringe claim 1 of the '352 patent, then claim 1 of the '352 patent does not read on the new [ ] E5 model ESD transistor; (2) if respondents' E6 model ESD transistor is found to infringe claim 1 of the '352 patent, then claim 1 of the '352 patent also reads on the new [ ] E5 model transistor. Stipulation to Further Revise Prehearing Schedule dated October 16, 2001, Stipulation 24.

68. Respondents' E1, E3, or E4 model ESD transistors (1.8V devices) do not infringe claims 1, 2 or 8 of the '352 patent. Fair Expert Report, par. 130; RX-134C, pp. 4-7.

69. [

]

70. [

]

71. The layout shown in RPX-25 is a top view of Respondents' [ ] transistor.

72. [

]

73. [

]

74. [

]

[ ]

75. The layout shown in RPX-24 and RPX-26 is a top view of Respondents' E6 model ESD field effect transistor. The layout is representative of the E6 transistors manufactured by Respondents. RPX-24; RPX-26; Peltzer Tr. 734:8-18.

76. [

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80. [

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81. [

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82. [

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83. [

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84. Respondents' ESD protection circuit of RPX-225C is not connected in the same manner as the ESD protection circuit claimed in claim 8 of the '352 patent. RX-225C; Peltzer Tr. 772:10-24.

85. [

]

[ ]

IV. VALIDITY OF THE '352 PATENT

A. Assignor Estoppel

86. Co-inventor Peter Hsue listed on the '352 patent currently works for SiS-TW in Hsinchu, Taiwan. Hsue Tr. 1129:24-1130:3.

87. [ ]

88. [

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89. [

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90. [

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91. [

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93. [ ]

[

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94. [

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95. [ ]

96. At the time Mr. Hsue joined SiS, none of the people working for him directly worked on ESD designs or layouts. Hsue Tr. 1136:2-4.

97. Mr. Hsue's responsibilities at SiS include process technology development. He is the director of that department. Hsue Tr. 1136:5-11.

98. [

]

99. [

]

100. [

]

101. [

]

102. A "spice" model is provided to the design department for wiring simulation, so that when the process development has been completed, the device department needs to provide the

electrical parameters to the design department. Thus, once the data is collected on the electrical characteristics; the data will be input to a spice model, which is an empirical equation. Hsue Tr. 1154:17-1155:18.

103. A spice model task force is responsible for the device spice, however, Mr. Hsue is not a member of this task force at SiS. Hsue Tr. 1155:22-1156:9.

104. [

]

105. [

]

106. Mr. Hsue did not participate in any way in selecting the ESD designs that were used by SiS for any product produced in the SiS fab. Hsue Tr. 1142:5-8.

107. When Mr. Hsue was hired by SiS there wasn't any kind of understanding that he would be working to develop or improve ESD designs or layouts for SiS. Hsue Tr. 1142:9-12.

108. Mr. Hsue was not consulted on the SiS designs or layouts before or after he started working for SiS. Hsue Tr. 1142:13-18.

109. Mr. Hsue is not an officer of SiS, nor has he ever been one. Hsue Tr. 1143:3-6.

110. Mr. Hsue has never made financial decisions for SiS. Hsue Tr. 1143:22-24.

111. [

]

B. Anticipation

112. With respect to the '352 patent, a person of ordinary skill in the art would have an

advanced degree such as a master's degree (or equivalent education or experience) in a field relevant to ESD technology, such as electrical engineering or physics, and further, such a person would have substantial experience in integrated circuit and device design. Fair Tr. 139; Peltzer Tr. 707.

113. Japanese Kôkai No. 64-23573 ("the Umemoto publication"), entitled "Semiconductor Integrated Circuit," was published on January 26, 1989, more than one year prior to the earliest effective filing date of the '352 patent. RX-17, p. 389; RX-18, p. 1; Peltzer Tr. 734:15-16, 779:5-10.

114. The Umemoto publication discloses that the "invention pertains to technology to improve the electrostatic breakdown strength of MOS type semiconductor integrated circuits." RX-18, p. 1, penultimate paragraph; RX-163.

115. An ESD protection device is to protect the circuit against ESD events. Peltzer Tr. 744:4-5, 750:11-13. This improvement in electrostatic breakdown strength is accomplished by lowering in a MOS transistor the junction breakdown voltage between a drain diffusion layer and a high-concentration region formed under a contact region between the drain diffusion region and a power source wiring layer. RX-18, p. 3, lines 7-20; Peltzer Tr. 750:24 to 751:19; RX-163.

116. The transistor illustrated in Figure 1 of the Umemoto publication is an FET, which is a MOS-type device. RX-17, Figure 1; RX-163; Peltzer Tr. 750:14.

117. With reference to Figure 1, the Umemoto publication discloses that "1 is a P type silicon substrate . . . ." RX-17, Figure 1; RX-18, p. 3, line 31; Peltzer Tr. 744:20-21, 751:20; RX-163.

118. With reference to Figure 1, the Umemoto publication discloses that "9 is an element isolation oxide film . . . ." RX-17, Figure 1; RX-18, p. 3, line 31; RX-163 Peltzer Tr. 751:20-22. As illustrated in Figure 1, the element isolation oxide film 9 is in and on the silicon substrate 1. RX-17, Figure 1.

119. With reference to Figure 1, the Umemoto publication discloses that "3 is a gate electrode . . ." RX-18, p. 4, line 1 and Figure 1; Peltzer Tr. 744:5-6, 22-23, 750:22) and "8 is a sidewall oxide film . . ." RX-17, Figure 1; RX-18, p. 4, lines 12-13; RX-163; Peltzer Tr. 744:5-7, 22-24.

120. As illustrated in Figure 1, the sidewall oxide film 8 forms a spacer adjacent each sidewall of the gate electrode 3. RX-17, Figure 1; RX-163; Peltzer Tr. 744:23-24, 750:22-23.

121. The gate electrode 8 and spacers 8 are located between the element isolation oxide film regions 9. RX-17, Figure 1; RX-163; Peltzer Tr. 744:22-24.

122. With reference to Figure 2, the Umemoto publication describes a known MOS transistor with a conventional LDD structure as having "low-concentration source and drain n-layers 21, 22 beside the gate electrode 25 . . . contacting the source and drain diffusion layers 26, 27 . . . ." RX-17, Figure 2; RX-18, p. 2, lines 8-15; RX-163.

123. The device illustrated in Figure 1 of the Umemoto publication uses an LDD structure having source and drain regions corresponding to those shown in Figure 2. RX-17, Figures 1 and 2; RX-18, p. 4, lines 2-4; RX-163; Peltzer Tr. 745:1-3.

124. The source and drain regions are located between the gate 3 and the element isolation oxide film regions 9. RX-17, Figure 1; RX-163; Peltzer Tr. 745:4-9, 752:3-10.

125. With reference to Figure 1, the Umemoto publication discloses low-concentration (up to

$10^{18}/cm^3$) regions 5 of n– conductivity type unique to LDD structures. RX-17, Figure 1; RX-18, p. 4, lines 3-4 and p. 5, line 2; Peltzer Tr. 745:10-14; 752:14-29.

126. These low-concentration regions 5 are each located under a sidewall oxide film 24. RX-17, Figure 1; Peltzer Tr. 744:8-9, 745:10-15. The n– conductivity type region 5 is implanted. Peltzer Tr. 750:19-20.

127. With reference to Figure 1, the Umemoto publication discloses that "4 is a drain (n+) region with an impurity concentration of approximately $1x10^{20}/cm^3$." RX-17, Figure 1; RX-18, p. 4, lines 2-3; RX-163; Peltzer Tr. 745:14-15, 752:21.

128. Figure 1 shows that the n+ region 4 is between regions 5 and an element isolation oxide film region 9. RX-17, Figure 1; RX-163.

129. With reference to Figure 1, the Umemoto publication discloses "a high-concentration (up to $10^{17}/cm^3$) impurity region, i.e., P type diffusion region 7" added just under the contact part between the power source wiring layer 6 and the drain region 4. RX-17, Figure 1; RX-18, p. 4, lines 4-8; RX-163; Peltzer Tr. 744:10-13, 753:3-5. Figure 1 shows this p-type region 7 as being under both the n+ source and drain regions 4. RX-17, Figure 1; Peltzer Tr. 744:10-13, 745:18-20, 753:6-11.

130. Figure 1 of the Umemoto publication shows each p-type diffusion region 7 as being centered under a drain (n^+) region 4. RX-17, Figure 1; Peltzer Tr. 745:18-20.

131. Lightly doped drain (LDD) structures are prepared by ion implantation. Peltzer Tr. 750:18-23; 750:19-20; RX-28, col. 12, lines 25-40; RX-22, pars. 0009, 0018, 0020.

132. According to the testimony of Mr. Peltzer, it is customary to follow ion implantation by a heating step. The heating step has two purposes: one is to anneal the damage caused by

implanting into the wafer; a second is to diffuse the implanted ions. Peltzer Hr. Tr. 746:5 - 747:3; RX-222 (A.S. Grove, Physics and Technology of Semiconductor Devices).

133. As used in the Umemoto publication, the terms "implant" and "diffusion" are the same. Peltzer Tr. 746:5 to 747:3, 747:4 to 749:20; 755:12-23; RX-222, p. 4; RX-28, col. 12, lines 25-40; attachment to CX-7C.

134. Professor Fair testified that he is not aware of any commercial use of diffusion rather than ion implantation for making LDD structures. Fair Tr. 1097:20-23.

135. With reference to Figure 1, the Umemoto publication discloses an N channel MOS transistor having a p-type silicon substrate 1, an (n+)-type drain region 4, and a low-concentration (n-)-type drain region. RX-17, Figure 1; RX-18, p. 3, line 30 to p. 4, line 4, and p. 5, line 2; RX-163; Peltzer Tr. 753:25 to 754:8.

136. Professor Fair acknowledged that use of ion implantation would be an option that would be available to one of ordinary skill in the art in forming the first lightly implanted region, the heavier implanted region, and the second lightly implanted region. Fair Tr. 1099:7-13.

C. Obviousness

137. Japanese Kôkai No. 1-134961 ("the Kamioka publication"), entitled "Input Protecting Circuit for Semiconductor Integrated Circuit," was published on May 26, 1989, more than one year prior to the earliest effective filing date of the '352 patent. RX-195, English abstract; Peltzer Tr. 779:5-10.

138. The Kamioka publication discloses an input protection device for a semiconductor integrated circuit. RX-195, Figures 1 and 2, translation, p. 1, lines 25-27.

139. The ESD protection circuit disclosed by the Kamioka publication is connected in the same manner as the ESD protection circuit claimed in claim 8. Peltzer Tr. 776:24 to 777:2.

140. With reference to Figures 1 and 2, the Kamioka publication discloses that the drain electrodes of two N-channel MOS transistors are connected by an aluminum lead 6 to an input pad 20 and an input gate electrode. RX-195, Figures 1 and 2, translation, p. 2, lines 17-20; Peltzer Tr. 776:17-21.

141. With reference to Figures 1 and 2, the Kamioka publication discloses that gate electrodes 3 and 4 are both connected to a ground wiring 8 through a polycrystalline silicon layer 9. RX-195, Figures 1 and 2, English trans., p. 2, lines 20-21; Peltzer Hr. Tr. 776:10-16.

142. The source electrode of the second transistor (bottom transistor in Figure 2) is connected to a ground electrode pad through an aluminum lead 8. RX-195, Figures 1 and 2, English trans., p. 2, lines 21-23; Peltzer Tr. 776:22-23.

143. With reference to Figures 1 and 2, the Kamioka publication discloses that the source electrode of the first transistor (top transistor in Figure 2) is connected to a power source (VCC pad) through aluminum lead 7. RX-195, Figures 1 and 2, English trans., p. 2, lines 21-23; Peltzer Tr. 776:22-24.

144. The Kamioka publication discloses as an effect of the invention, that "[r]elease of electric charges is easier in such a design, which increases breakdown strength in input protection." RX-195, Eng. trans., p. 3, lines 10-11.

145. Japanese Kôkai No. 5-102475 ("the Yasui publication"), entitled "Semiconductor Device and its Method of Manufacture," was published on April 23, 1993. RX-21, p. 1; RX-22,

p. 1.

146. Japanese Kôkai No. 3-196677 ("the Soeda publication"), entitled "Semiconductor Device," was published August 28, 1991, more than one year prior to the earliest effective filing date of the '352 patent. RX-23, English abstract; RX-24, p. 1; Peltzer Hearing Tr. 7795-10.

147. The Soeda publication pertains to a semiconductor device that is provided with a means of countering the electrostatic breakdown of MOSFETs. RX-24, p. 2, lines 1-2.

148. With reference to Figure 3, the Soeda publication discloses input protective circuits 9 connected to a pad 8. The input protective circuits as shown include two FET devices. The source of the first (upper) MOSFET 5 and the drain of the second (lower) MOSFET 6 are each connected to the pad 8. RX-23, Figure 3; RX-24, p. 2, lines 17-22; Peltzer Tr. 777:14-15, 19-22.

149. With reference to Figure 3, the Soeda publication discloses that the gates of first MOSFET 5 and second MOSFET 6, and the source of second MOSFET 6 are connected to ground potential G. RX-23, Figure 3; RX-24, p. 2, lines 19-21; Peltzer Tr. 777:10-15.

150. With reference to Figure 3, the Soeda publication discloses that the drain of first MOSFET 5 is connected to the potential V. RX-23, Figure 3; RX-24, p. 2, lines 19-20.

151. Structurally, a source and a drain may be identical. Fair. Tr. 357:19.

152. In NMOS symmetric devices, source regions and drain regions can be flipped. Peltzer Tr. 777:19-22. The source and drain of the first MOSFET 5 can be flipped such that the drain is connected to pad 8 and the source is connected to the potential V.

V. INFRINGEMENT OF THE '345 PATENT

A. Claim Construction

153. The named inventors of the '345 patent are Chih-Chien Liu, Ta-Shan Tseng, Wen-Bin Shih, Juan-Yuan Wu, Water Lur and Shih-Wei Sun. Lur Tr. 36:4-38:23; RX-40.

154. Chih-Chien Liu was responsible for HDPVCD technology development at the time of the '345 patent application. Lur Tr. 37:14-16.

155. Co-inventor Ta-Shan Tseng was an etching engineer in UMC's 8" fab and is responsible for etching in the production line. Lur Tr. 37:23-38:3.

156. Co-inventor Water Lur was involved in new module technology development. Lur Tr. 38:12-14.

157. In June 1995, co-inventor Lur began participating in UMC's Advanced Technology Development group. Lur Tr. 11:7-18.

158. Co-inventor Lur remained in the Advanced Technology Development group until October 1999. Lur Tr. 11:20-23.

159. Co-inventor Lur transferred from the Advanced Technology Development group to UMC's intellectual property rights legal group in October 1999. Lur Tr. 15:18-23.

160. Co-inventor Lur has been working in the intellectual property rights legal group since October 1999. Lur Tr. 15:24-16:1.

161. Co-inventor Wen-Bin Shieh was involved in the photolithography on UMC's production line. Lur Tr. 38:4-6.

162. Co-inventor Shih-Wei Sun was the Advanced Technology Development manager who advised on integration issues. Lur Tr. 38:16-20.

163. Co-inventor Shih-Wei Sun is also the director of UMC's Fab 8AB and former director of UMC's Fab 2. JX-35 Sun Dep. Tr. 6:21-7:15.

164. The '345 patent application that matured into the '345 patent was filed on October 28, 1997. RX-40.

165. The '345 patent claims priority from provisional application 60/041,790 filed April 2,1997. RX-40.

166. According to co-inventor Liu, Jiang Chyun is a company that UMC uses to write its patent application. JX-24C 7/6 Liu Dep. Tr. 135:6-22.

167. The '345 patent relates to a method for forming interconnect wiring patterns on the surface of integrated circuits and for filling the gaps between conductive regions in the wiring pattern, with a dielectric material, using HDP chemical vapor deposition. Peltzer Tr. 791:17-21.

168. RPX-33 is the '345 preferred embodiment. Peltzer Tr. 804:8-10.

169. The preferred embodiment includes a substrate. Peltzer Tr. 804:10-12.

170. Above the substrate in the preferred embodiment is titanium nitride, which serves as a barrier between the wiring line and the substrate. RPX-33; Peltzer Tr. 804:12-13; 17-18.

171. Above the wiring lines in the preferred embodiment is titanium nitride, which is a protective layer. RPX-33; Peltzer Tr. 804:13-17. The titanium nitride is the first antireflective coating identified in Claim 1. Peltzer Tr. 805:11-14.

172. In the final step, a dielectric material is deposited within the gaps to fill the gaps by high density plasma chemical vapor deposition ("HDPCVD)". Peltzer Tr. 806:22-807:3.

173. The structure is surrounded by oxide, which is deposited from HDPCVD. Peltzer Tr.

804:21-23.

174. Claim 1 does not say anything about protecting the metal wiring lines from corner clipping or from any erosion during the HDPCVD process. Peltzer Tr. 807:4-7.

175. Claim 3 depends from claim 1 and further defines that "the mask layer is a pattered photoresist layer." RX-40, claim 3, col. 10, lines 32-33.

176. Claim 4 also depends from claim 1 and further defines that "a portion of the second antireflective coating is etched during the high density plasma chemical vapor deposition." RX-40, claim 4, col. 10, lines 34-36.

177. Claim 5 also depends from claim 1 and is directed to the method of claim 1 "further comprising the formation of a surface layer between the substrate and the wiring line layer, the surface layer being a barrier between the substrate and wiring line layer." RX-40, claim 5, col. 10, lines 37-39.

178. Claim 6 also depends from claim 1 and is directed to the method of claim 1 "further comprising the step of removing the second antireflective coating after the deposition of a dielectric material within the gaps." RX-40, claim 6, col. 10, lines 41-43.

179. Claim 7 also depends from claim 1 and further defines that "part of the second antireflective coating is removed and remaining portions of the second antireflective coating act as a mask during the etching of the first antireflective coating and the wiring line layer." RX-40, claim 7, col. 10, lines 44-48.

180. Claim 8 also depends from claim 1 and further defines that "after etching each wiring line has a portion of the second antireflective coating on each wiring line having a cross-sectional shape selected from the group consisting of a rectangle, a triangle, a trapezoid,

and a rectangle having its upper corners etched away." RX-40, claim 8, col. 10, lines 48-54.

181. Claim 9 does not require that the cap layer protect the corners of the metal wiring line during HDPCVD. Peltzer Tr. 808:21-24.

182. Claim 10 also depends from claim 9 and further defines "the cap layer is used as a hard mask during etching of the wiring line layer." RX-40, claim 10, col. 11, lines 3-5.

183. Claim 11 also depends from claim 9 and further defines "the cap layers is an antireflective coating." RX-40, claim 11, col. 11, lines 6-7.

184. Claim 12 also depends from claim 9 and further defines "the remaining portion of the cap layer is partially etched during the deposition of the dielectric material using high density plasma chemical vapor deposition." RX-40, claim 12, col. 11, lines 8-10.

185. Claim 13 also depends from claim 9 and further defines "the cap layer comprises a material selected from the group consisting of a silicon nitride material and an oxynitride material." RX-40, claim 13, col. 11, lines 11-12.

186. Claim 14 also depends from claim 9 and further defines "the remaining portion of the cap layer on a least one wiring line has a rectangular shape in cross section." RX-40, claim 14, col. 11, lines 14-17.

187. Claim 15 also depends from claim 9 and further defines "the remaining portion of the cap layer on at least one wiring line has a trapezoidal shape in cross section." RX-40, claim 15, col. 11, lines 18-20.

188. Claim 16 depends from claims 9 and 15 and further defines "the trapezoidal shape [to] include[] top and bottom surfaces parallel to one another and side surfaces that extend

inwardly from the bottom surface to the top surface." RX-40, claim 16, col. 11, lines 20-24.

189. Claim 19 depends from claim 9 and further defines "the remaining portion of the cap layer [to be] partially etched and redeposited into the gaps during the high density plasma chemical vapor deposition process." RX-40, claim 19, col. 11, lines 32-35.

190. Claim 20 depends from claim 9 and further defines "the mask layer [to be] a patterned photoresist layer." RX-40, claim 20, col. 12, lines 1-2.

191. Claim 21 is similar to claims 1 and 9, except that a protective layer comprising at least one material selected from the group consisting of titanium nitride, titanium silicide and a titanium-tungsten alloy is disposed on the upper surface of the metal wiring layer and a cap layer comprising at least one material selected from the group consisting of an oxide, a nitride, and an oxynitride, is disposed on the top surface of the protective layer. Peltzer Tr. 809:18-24; RPX-34.

192. The specification of the '345 patent discloses that a "cap layer may serve a number of functions, acting as an antireflective coating, a hard mask for metal line etching, and a protector for the top corners of metal wiring lines during the HDP CVD process." RX-40, col. 4, lines 57-60.

193. According to co-inventor Liu, the "cap layer" in the '345 patent has three functions, including serving as an antireflective layer, cap layer and protector of metal line corners. Liu Tr. 539: 1-6.

194. According to co-inventor Liu, the cap layer provides the same benefits for the litho process when using PECVD for gap-filling as when using HDP-CVD for gap-filling. JX-

24C 8/22 Liu Dep. Tr. 87:20-25.

195. According to Mr. Peltzer, a cap layer is an insulating layer that has the property of reducing the amount of reflected light, has the property of being a hard mask, and is a protector for the top corners, against a feature that is described as corner clipping. Peltzer Tr. 800:25-801:5.

196. Two antireflective coatings are identified in the '345 patent as features "26" and "28." RX-40, RPX-28, RPX-29, Fair Tr. 792:9-10.

197. The specification of the '345 patent discloses that "an anti-reflective coating over the wiring line layer and below the layer of photoresist [works] by absorbing light transmitted during the exposure of the photoresist to light." RX-40, col. 7, lines 10-17.

198. The specification of the '345 patent also discloses that "that the cap layer may be used as a quarter wave plate in order to prevent light from passing through the cap layer and reflecting back up to the photoresist layer to become exposed in regions that are supposed to remain unexposed." RX-40, col. 7, lines 58-63.

199. The cap layer must have at least one of the following characteristics: 1) an antireflective function, 2) a hard mask function, and/or 3) a corner clipping protection function. RX-40, col. 4, lines 57-60; col. 7, line 58-col. 9, line 5.

200. The specification of the '345 patent discloses that "a layer of photoresist is provided over the cap layer and the photoresist is shaped to form an etching mask[.]" RX-40, col. 7, lines 37-40.

201. The "wiring line layer" can be etched into "wiring lines." Peltzer Tr. 803:3-6.

202. The wiring line is identified in the '345 patent as "24." RX-40; RPX-29; Fair Tr.792:7-8.

203. The specification of the '345 patent discloses that an antireflective coating may be "absorptive at the wavelength used to expose the photoresist layer during formation of the etch mask." RX-40, col. 7, lines 11-22 and 63-66.

204. There are generally two types of antireflective coatings. In one type, light is absorbed as it enters the coating. Peltzer Hr. Tr. 799:8-14.

205. The specification of the '345 patent discloses that "a quarter wave plate creates destructive interference to prevent light from reflecting up to the photoresist layer." RX-40, col. 7, lines 64-66.

206. The specification of the '345 patent discloses "[a] cap layer, which is preferably formed from silicon oxide, silicon nitride or oxynitride" that is deposited over the protective layer. RX-40, col. 7, lines 30-32. Further, "if the silicon oxide is used for cap layer[], then it is preferred that a silicon rich oxide (SRO, SiO2-x), i.e., a silicon oxide have a greater concentration of silicon than is stoichiometric for silicon dioxides[.]" RX-40, col. 7, lines 33-36.

207. Silicon oxide, silicon nitride and silicon oxynitride are all dielectrics. Peltzer Tr. 802:10-12; RPX-44.

208. The specification of the '345 patent discloses a "protective layer [serving] several functions, including protecting the wiring line layer, limiting electromigration, providing more reproduceable contacts and acting a an antireflective coating over the wiring line layer[.]" RX-40, col. 7, lines 8-17.

209. The '345 patent relates to a method for forming interconnect wiring patterns on the surface of integrated circuits and for filling the gaps between conductive regions in the

wiring pattern, with a dielectric material, using HDP chemical vapor deposition. Peltzer Tr. 791:17-21.

210. At the time of the invention disclosure on which the '345 patent is based, it was known to fill the spaces or gaps between the wiring lines using high density plasma chemical vapor deposition (HDP CVD). Liu Tr. 536:5-9; Liu Tr. 105:15-22.

211. The '345 patent repeatedly discloses that the application of an antireflective layer reduces the reflection of light up into the photoresist as compared to the reflection that would exist up from the titanium nitride layer alone. Peltzer Tr. 1738:21-1741:14.

212. An antireflective coating cannot increase the amount of reflected light that would reflect from the wiring line surface in the absence of that coating. Peltzer Tr. 1701:12-14; 1703:15-1704:3.

213. The purpose of an antireflective coating is to reduce the amount of reflected light in order to make it easier to define the photoresist patterns in the photoresist. Peltzer Tr. 1701:14-18.

214. Increasing the amount of reflected light coming up from the layer below the photoresist would make it harder to define the photoresist patterns in the photoresist. Peltzer Tr. 1701:14-18; 1704:6-9.

215. The reference Ogawa, Exhibit RX-180, pertains to the optimization of the performance of antireflective coatings. Peltzer Tr. 1755:8-1756:4.

216. Ogawa, Exhibit RX-180, discloses a method for optimizing optical conditions, namely, minimizing the reflection of light back into the photoresist for any given material and coating thicknesses below the photoresist. Peltzer Tr. 1756:9-23; 1757:6; 1758:2.

217. According to Ogawa, Exhibit RX-180, if the layer at issue would increase the amount of reflected light going back into the photoresist as compared to the amount of reflected light in the absence of the layer, then in order to optimize the performance of that layer, its thickness should be zero and thus the layer should be removed. Peltzer Tr. 1758:3-14.

218. An antireflective coating reduces the amount of reflected light from the surface below the photoresist as compared to the amount of reflected light in the absence of that coating. Peltzer Tr. 1706:10-1707:11.

219. The '345 patent, in describing different materials for use as antireflective coatings, identifies a group of materials containing titanium for one layer and a separate group of materials containing silicon, but not titanium, for the other layer. Peltzer Tr. 1778:19-6.

220. Nowhere in the specification of the '345 patent is any special definition given to the word "on." RX-40.

221. The following excerpts from the '345 patent confirm that the applicants distinguished between "in" and "on":

> . . . device structures ***in or on*** the substrate . . . [Col. 1, lines 26-27][Emphasis added];
>
> . . . devices such as FETs, diodes or transistors are formed ***in and on*** the substrate . . . [Col. 1, lines 37-38][Emphasis added];
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> . . . deposited ***in*** the gaps between wiring lines or on the wiring lines . . . [Col. 2, lines 27-28][Emphasis added];
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> . . . voids ***in*** the intermetal dielectric . . . [Col. 5, line 25][Emphasis added]; and
>
> . . . material ***in*** the layer 28 . . . [Col. 8, line7][Emphasis added].

222. The '345 patent states:

> Cap layer 28, which is preferably formed from silicon oxide, silicon nitride or oxynitride, is ***deposited over*** the protective layer 26.

Col. 8, lines 31-33 (emphasis added).

223. The specification of the '345 patent discloses that a "cap layer may serve a number of functions, acting as an antireflective coating, a hard mask for metal line etching, and a protector for the top corners of metal wiring lines during the HDP CVD process." RX-40, col. 4, lines 57-60.

224. According to Mr. Peltzer, a cap layer is an insulating layer that has the property of reducing the amount of reflected light, has the property of being a hard mask, and is a protector for the top corners, against a feature that is described as corner clipping. Peltzer Tr. 800:25-801:5.

225. A hard mask is a layer which is etched using the photoresist as a mask, followed by removal of the photoresist to leave the patterned hard mask layer which then serves as a mask for subsequent etching of underlying layers. Yang Tr. 1613:5-18; Lee Tr. 1661:14-18; Peltzer Tr. 1808:22 to 1809:22.

226. The '345 patent discloses that the cap layer "may not be a conductive material." RX-40, col. 9, lines 60-64.

227. According to co-inventor Liu, the "cap layer" must be a dielectric material. JX-24C 7/5 Liu Dep. Tr. 77:14-21.

228. According to co-inventor Wu, the protective layer must be a dielectric material, such as silicon oxynitride, SiO2, SiN, or silicon rich oxide. JX-44C 7/11 Wu Dep. Tr. 21: 19-21;

19:13-25.

229. According to co-inventor Lur, the secondary ARC layer will be a dielectric material, such as silicon dioxide, and if the etched-away materials are silicon dioxide and other dielectric materials, then the gap to be filled will not have the problem of metals in between the wiring lines encountered when the inventors developed this technology in the very beginning. JX-27C 7/17 Lur Dep. Tr. 116:14-25.

230. According to co-inventor Shieh, the cap layer cannot be a conductive material. JX-33C 7/9 Shieh Dep. Tr. 65:6-8.

231. According to co-inventor Liu, titanium nitride is not a dielectric material and titanium nitride cannot be used for the cap layer. JX-24C 7/5 Liu Dep. Tr. 78:9-12.

232. According to co-inventor Liu, back when he first had the idea of using a cap layer on top of the metal line as a sacrificial layer, he had silicon dioxide, silicon nitride, silicon oxynitride and silicon-rich dioxide materials in mind to use for the cap layer. JX-24C 7/5 Liu Dep. Tr. 83:1-8.

233. According to co-inventor Shieh, silicon oxide and silicon nitride are both acceptable as the cap layer, but not as good as silicon oxynitride. JX-33C 7/9 Shieh Dep. Tr. 60:6-25.

234. According to co-inventor Liu, "titanium oxide" does not fit his definition of "cap layer." JX-24C 8/22 Liu Dep. Tr. 33:6-18.

235. According to co-inventor Liu, the cap layer as a top ARC is an ARC layer on top of the titanium nitride layer. JX-24C 8/22 Liu Dep. Tr. 88:1-4.

B. Infringement Determination

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247. Exhibit RX-230C, Bates Nos. SiS 032449-032460, is SiS's operation instruction (OI) process recipes. Lee Tr. 1638:12-16; RX-230C, SiS 032449-032460.

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250. The date of the operation instruction (OI) in Exhibit RX-230C is July 18, 2001. Lee Tr. 1639:3-8; RX-230C, SiS 032449.

251. In Exhibit RX-230C, SiS 032450 five recipes are set forth at the top of the page in a table. Lee Tr. 1639:14-16; RX-230C, SiS 032450.

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273. The TEM photomicrograph shown in Exhibit RX-139C, SiS 265318, was prepared for Dr. Lee. Lee Tr. 1653:21-23; RX-139C, SiS 265318.

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275. Dr. Lee and K. H. Wang, who works for Dr. Lee, made the measurement shown in RX-139C, SiS 165318. Lee Tr. 1654:3-7; RX-139C, SiS 265318.

276. The thicknesses shown in Exhibit RX-139C are estimated. Dr. Lee testified that the TEM photomicrographs show the same materials with different concentrations as different shades of color. The measurement made from such PEM photomicrographs is an estimate of the thickness. Lee Tr. 1654:12 to 1655:5; RX-139C.

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282. Dr. Shyh-Dar Lee joined SiS at the end of September, 2000. Lee Tr. 1635:2-4.

283. When Dr. Lee joined SiS, his position was Technical Manager. Lee Tr. 1635:5-8.

284. Dr. Lee's current position at SiS is Advanced Module Technology Development Manager. Lee Tr. 1635:9-11.

285. Dr. Lee became the Advanced Module Technology Development Manager in February, 2001. Lee Tr. 1635:12-14.

286. Dr. Lee's responsibilities as Advanced Module Technology Development Manager include: (1) development of advanced technology; (2) yield improvement; and (3) development of cost reduction process. Lee Tr. 1635:15-24.

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435. Claim 3 of the '345 patent depends from claim 1 and further recites that "the mask layer is a patterned photoresist layer." RX-40, col. 10, lines 32-33.

436. Claim 3 of the '345 patent includes all of the elements of claim 1. RX-40, col. 10, lines 32-33.

437. Claim 4 of the '345 patent includes all of the elements of claim 1, [

]. Peltzer Tr. 1735:11 to 1736:15; 1792:19 to 1793:19; RX-40, col. 10, lines 33-36.

438. Claim 5 of the '345 patent depends from claim 1 and further recites "the formation of a surface layer between the substrate and the wiring line layer, the surface layer being a barrier between the substrate and wiring line layer." RX-40, col. 10, lines 37-39.

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452. The wiring lines of the '345 patent may include the cap layer, a protective coating layer, a metal layer and a glue layer. RX-40, col. 4, lines 45-60.

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VI. VALIDITY OF THE '345 PATENT

460. With respect to the '345 patent, a person of ordinary skill in the art would have at least a master's degree in electrical engineering, physics, chemistry, chemical engineering or metallurgy, with substantial experience in semiconductor device processes. Fair Tr. 138-139.

Invalidity Based on Prior Art

461. Dr. Wright is acting as UMC trial counsel in this Investigation.

462. Dr. Wright worked for Law+ from 1995 to 1997. Wright Tr. 265:24-266:2.

463. During his tenure at Law+, Wright was involved in the preparation and prosecution of patent applications on behalf of UMC. Wright Tr. 266:6-10.

464. While at Law+, Wright traveled to Taiwan every two to three months and prepared about 100 patent applications. Wright Tr. 266:20-267:2.

465. On certain trips to Taiwan, Wright did not bring any invention disclosure forms back to the U.S. Wright Tr. 279:23-280:1.

466. Upon return trips form Taiwan, Wright did not open up any new client matters or other indicia in the Law+ accounting record to reflect when the invention disclosures were brought back. Wright Tr. 281:19-23.

467. Wright does not have any copies of the '345 invention disclosure statement indicating that it was received in the Law+ offices. Wright Tr. 282:7-11.

468. All the work done in connection with the invention disclosure statement which was used to prepare the '345 patent was made in Taiwan. Wright Tr. 275:25-276:3.

469. Wright does not have a precise recollection of the time or date when he received the

invention disclosure statement (i.e., CX-637C) which the '345 patent is based on. Wright Tr. 282:7-11.

470. The Tobben patent is not a cited reference of the '345 patent. RX-155.

471. The method disclosed in the Tobben patent "includes forming a . . . metal layer over a surface of the substrate." RX-155, col, 1, lines 43-44. The formation of the metal layer over the substrate disclosed in the Tobben patent is the same disclosure as the "substrate and . . . wiring line layer above the substrate" disclosed in claim 1 of the '345 patent. Peltzer Tr. 812:23-813:4; RX-40, col. 10, lines 8-10.

472. The Tobben patent further discloses a "metal layer [that] is a composite layer made up of a lower relatively thin layer of titanium/titanium nitride, and intermediate, relatively thick layer of sputtered aluminum; and an upper, thin antireflective coating (ARC) layer of titanium/titanium nitride." RX-155, col 2, lines 36-40; Peltzer Tr. 811:10-12; RPX-34.

473. The composite layer disclosed in the Tobben patent is the same disclosure as the "first antireflective coating on the wiring line layer" disclosed in claim 1 of the '345 patent. Peltzer 813:5-12; RX-40, col. 10, lines 11-12.

474. The Tobben patent further discloses a "planarization layer . . . formed over the surface of the [thin antireflective coating (ARC) layer of titanium/titanium nitride]." RX-155, col. 2, lines 36-40, 47-48. "The . . . planarization layer . . . includes a spun-on silicon dioxide glass as a bottom portion . . . and a cap or upper layer . . . formed thereon." RX-155, col. 3, lines 8-10; Peltzer 811:21-22; RPX-34.

475. The Tobben patent continues in column 3 to state that "[t]ypically, the thickness of the planarization layer is of no more than 300A to 2000A." RX-155, col. 3, lines 8-10.

According to Dr. Peltzer, the thickness for the SiO2 layer of 300 A to 2000A clearly encompasses ranges where cancellation of reflected light from the surface of this coating such as to be a quarter wave plate making the Sio2 layer in Tobben a second antireflective coating. Peltzer Tr. 814: 3-815:3.

476. Dr. Peltzer's opinion was supported by a mathematical calculation of reflectivity of the type upon which engineers ordinarily rely in the course of work concerning the subject matter of the '345 patent. Peltzer Tr. 856: 21-11; RPX-46.

477. The Tobben patent further discloses a "photoresist layer [that] is spun on the planar surface . . . of the planarization layer[.]" RX-155, col. 3, lines 21-22. "The mask [photoresist layer] is used to pattern exposed portions of the underlying planarization layer[.]" RX-155, col. 3, lines 32-34.

478. The Tobben patent further discloses use of the photoresist mask "to etch the exposed portions of the planarization layer within the grooves of the photoresist layer." RX-155, col. 3, lines 40-42. Further, "the exposed portions of the metal layer . . . are etched away using REI to form the plurality of electrically conducive wires . . .over the dielectric layer." RX-155, col. 3, lines 56-58; *see also* RX-155, col. 3, lines 62-66.

479. The use of the photoresist mask to etch the exposed portions of the planarization layer within the grooves of the photoresist layer and metal layer is the same disclosure as the "etching of the first antireflective coating, the second antireflective coating, and the wiring line layer, at the location where the second antireflective coating is exposed by the mask layer, to form wiring lines separated by gaps" disclosed in claim 1 of the '345 patent. Peltzer Hrg Tr. 815:6-15; RX-168; RX-40, col. 10, lines 21-24.

480. The Tobben patent also discloses HDP CVD processing as a method for filling the spaces between wiring lines with dielectric material. RX-155.

481. The Tobben patent discloses the deposition of silicon dioxide "over the surface of the grooved structure ... [and into the grooves] . . . using . . . high density plasma deposition (HDP[)] techniques." RX-155, col. 4, lines 11-18.

482. The use of HDPCVD disclosed in the Tobben patent is the same disclosure as the "depositing [of] a dielectric material within the gaps to fill the gaps, using high density plasma chemical vapor deposition" disclosed in claim 1 of the '345 patent. Peltzer Tr. 815:16-23; RX-168; RX-40, col. 10, lines 25-28.

483. Claim 1 of the '345 patent is therefore fully disclosed by the Tobben patent.

484. The Tobben patent discloses "a photoresist layer [that] is spun on the planar surface of the planarization layer." RX-155, col. 4, lines 21-22. "The photoresist layer is then developed to remove the exposed or polymerized portions, creating grooves or slots." RX-155, col. 3, lines 28-30.

485. The use of a photoresist layer on the planar surface of the planarization layer that is developed to remove exposed portions, creating grooves or slots is the same disclosure as the "mask layer [being] a patterned photoresist" is disclosed in claim 3 the '345 patent. Peltzer Tr. 815:24-816:7; RX-168; RX-40, col. 10, lines 32-33.

486. Everything disclosed in claim 3 of the '345 patent was disclosed in the Tobben patent. Peltzer Tr. 815:24-815:25; RX-168.

487. The Tobben patent discloses the stripping away of the photoresist layer. RX-155, col. 4, lines 5-7. "Then, the planarization layer . . . is removed using, for example, a wet

chemistry." RX-155, col. 4, lines 5-7. Also, "a layer of silicon dioxide may be deposited over the surface of the grooved structure using . . . high density plasma deposition (HDP techniques." RX-155, col. 4, lines 15-18.

488. Because HDP deposition involves sputter etching during deposition that would remove, or partially remove, the planarization level, the disclosures of the Tobben patent is the same as the disclosure of "[t]he method of claim 1, wherein a portion of the second antireflective coating is etched during the high density plasma chemical vapor deposition" disclosed in claim 4 of the '345 patent. Peltzer Tr. 816:23-817:2; RX-168; RX-40, col. 10, lines 3-35.

489. The Tobben patent discloses a "metal layer ... [that] is a composite layer made up of a lower relatively thin layer of titanium/titanium nitride . . . ." RX-155, col. 2, lines 36-40. The composite layer disclosed in the Tobben patent is the same as the disclosure of "[t]he method of claim 1, further comprising the formation of a surface layer between the substrate and the wiring line layer, the surface layer being a barrier between the substrate and the wiring line layer" disclosed in claim 5 of the '345 patent. RX-40, col. 10, lines 37-40.

490. The Tobben patent discloses "a layer of silicon dioxide . . . deposited over the surface of the grooved structure using . . . high density plasma deposition (HDP techniques." RX-155, col. 4, lines 15-18. Tobben also discloses "planarizing the underlying surface upon which the metal layer is deposited using chemical mechanical polishing (CMP) techniques." RX-155, col. 1, lines 33-37. "Next, the second metalization layer is deposited over the patterned planarization layer." RX-155, col. 4, lines 18-20.

491. The Tobben disclosure is the same as "the step of removing the second antireflective coating after the deposition of a dielectric material within the gaps" disclosed in claim 6 of the '345 patent because CMP would remove at least portions of the planarization layer when HDP processing is used and portions of the planarization layer remain after dielectric deposition." RX-40, col. 10, lines 40-43.

492. The Tobben patent discloses "using remaining portion of the photoresist masking layer. . . , and the second mask . . . formed within the planarization layer . . . i.e., with the second mask . . . exposing underlying non-planar surface portions of the metal layer . . ., the exposed portions of the metal layer . . . are etched away." RX-155, col. 3, lines 51-56. Peltzer Tr. 818:8-22; RX-168.

493. The disclosure in the Tobben patent is the same as the disclosure of claim 7 of "[t]he method of claim 1, wherein part of the second antireflective coating is removed and remaining portions of the second antireflective coating act as a mask during the etching of the first antireflective coating and the wiring line layer." RX-40, col. 10, lines 43-48.

494. The Tobben patent discloses the patterned planarization layer remaining with a "rectangular cross section on the left and right." RX-155, figures 4 and 5.

495. The disclosure in the Tobben patent is the same as the disclosure of "the method of claim 1, wherein after etching each wiring line has a portion of the second antireflection coating thereon, the portion of second antireflection coating on each wiring line have a cross-sectional shape selected from the group consisting of a rectangle, a triangle, and a rectangle having its upper corners etched away" disclosed in claim 8 of the '345 patent. Peltzer Tr. 818:23-819:12; RX-168; RX-40, col. 110, lines 48-54.

496. Claim 9 does not mention use of an antireflective coating. RX-40.

497. The Tobben patent discloses "a method . . . for forming a plurality of electrically conductive wires on a substrate." RX-155, col. 1, lines 41-43.

498. The disclosure in the Tobben patent is the same disclosure as "[a] method for forming conducting structures separated by gaps on a substrate" disclosed in claim 9 of the '345 patent because "both are talking about conductive structures." Peltzer Tr. 819:22-820:1; RX-168; RX-40, col. 10, lines 53-56.

499. The Tobben patent discloses a "method including forming a . . . metal layer over a surface of the substrate." RX-155, col. 1, lines 43-44.

500. The disclosure in the Tobben patent is the same disclosure as "providing a substrate and a wiring line layer above the substrate" disclosed in claim 9 of the '345 patent. Peltzer Tr. 820:2-6; RX-168; RX-40, col. 10, lines 57-58.

501. The Tobben patent discloses a "cap layer compris[ing] of dielectric material." RX-155, col. 3, lines 8-10.

502. The Tobben patent expressly recites a cap layer comprising a dielectric material which is the same disclosure as "forming a cap layer above the wiring line layer" disclosed in claim 9 of the '345 patent. Peltzer Tr. 820: 7-15; RX-168; RX-40, col. 10, line 58.

503. The Tobben patent discloses that "the photoresist layer is then developed to remove the exposed or polymerized portions, creating grooves or slots []. The unremoved portions of the photoresist layers serves as a mask for patterning the underlying layers." RX-155, col. 3, lines 28-34.

504. The disclosure in the Tobben patent is the same disclosure as "forming a mask layer

above the cap layer, wherein the mark[sic] layer covers selected portions of the cap layer and exposes other portions of the cap layer." Peltzer Tr. 820:17-23; RX-168; RX-40, col. 10, lines 60-63)

505. The Tobben patent further discloses "[a] mask . . . used to pattern exposed portions of the underlying planarization layer [.]" RX-155, col. 3, lines 32-34. The "photoresist mask [] is used to etch the exposed portions of the planarization layer within the grooves of the photoresist layer." RX-155, col. 3, lines 40-42.

506. The Tobben patent further discloses that "[t]he exposed portions of the metal layer . . . are etched away . . . to form the plurality of electrically conductive wires over the dielectric layer." RX-155, col. 3, lines 56-58. "Here, the metal layer [] is a composite layer made up of . . . an upper, thin antireflective coating (ARC) layer of titanium/titanium nitride." RX-155, col. 2, lines 36-40. "Grooves [] are etched into the . . . conductive metal layer . . . to form the plurality of electrically conductive wires[,] . . . separated by the grooves" RX-155, col. 3, lines 62-66.

507. The disclosure in the Tobben patent is the same disclosure as the "etching the cap layer, and the wiring line layer, at the locations where the cap layer is exposed by the mask layer, to form wiring lines separated by gaps, the wiring lines having a remaining portion of the cap layer thereon[.]" disclosed in claim 9 of the '345 patent. Peltzer Tr. 820:20-24; RX-168; RX-40, col. 10, lines 63-68.

508. The Tobben patent discloses the use of "a layer of silicon dioxide . . . deposited over the surface of the grooved structure using . . . high density plasma deposition (HDP techniques." RX-155, col. 4, lines 15-18. Specifically, "a planarized dielectric surface is

deposited over the structure and into the grooves." RX-155, col. 4, lines 11-13.

509. The Tobben disclosure is the same as the disclosure of "depositing a dielectric material within the gaps at a sputtering rate sufficient to fill the gaps, using high density plasma chemical vapor deposition" disclosed in claim 9 of the '345 patent. Peltzer Tr. 821:21-822:4; RX-168; RX-40, col. 11, lines 1-3 .

510. The Tobben patent discloses the use of a cap layer comprised of a dielectric material. RX-155, col. 3, lines 8-10. Further, "using the remaining portion of the photoresist masking layer and second mask formed within the planarization layer, . . . the exposed portions of the metal layer are etched away . . . to form the plurality of electrically conducive wires . . . over the dielectric layer." RX-155, col. 3, lines 52-58.

511. The disclosure of the Tobben patent is the same as the disclosure of "[t]he method of claim 9, wherein the cap layer is used as a hard mask during etching of the wiring line layer" disclosed in claim 10 of the '345 patent. Peltzer Tr. 822:9-823:1; RX-168; RX-40, col. 11, lines 4-5.

512. The Tobben patent discloses that "the thickness of the planarization layer is of no more than 300 A to 2000A," which encompasses the thickness of antireflective coatings based on interference effects. RX-155, col. 3, lines 3-5; Peltzer Tr. 823:6-8.

513. The disclosure of Tobben is the same as the disclosure of "[t]he method of claim 9, wherein the cap layer is an antireflective coating" disclosed in claim 11 of the '345 patent. Peltzer Tr. 823:2-11; RX-168; RX-40, col. 11, lines 6-7.

514. The Tobben patent discloses the stripping away of the photoresist and removal of the planarization layer. RX-155, col. 4, lines 5-7. The Tobben patent further discloses the

deposition of silicon dioxide over the grooved structure using HDP techniques, which involves sputter etching during deposition that would remove, or partially remove, the planarization layer. RX-155, col. 4, lines 15-18.

515. The disclosure of the Tobben patent is the same as "[t]he method of claim 9, wherein the remaining portion of the cap layer is partially etched during the deposition of a dielectric material using high density plasma chemical vapor deposition." Peltzer Tr. 823:12-824:2; RX-168; RX-40, col. 11, lines 8-11.

516. The Tobben patent discloses the use of dielectic material for the cap layer. RX-155, col. 3, lines 10-11.

517. Because silicon nitride and oxynitride are dielectric materials, the Tobben disclosures are the same as the disclosure of "[t]he method of claim 9, wherein the cap layer comprises a material selected from the group consisting of silicon nitride material and oxynitride material. Peltzer 824:3-8; RX-168; RX-40, col. 11, line 12-14.

518. The Tobben patent discloses at figure 4 and 5 that the planarization layer has a rectangular cross section on the left and right of the figures. RX-155, figures 4 and 5.

519. The disclosures in figures 4 and 5 are the same as the disclosure of the "method of claim 9, wherein the remaining portion of the cap layer on at least one wiring line has a rectangular shape in cross section" disclosed in claim 14 of the '345 patent. Peltzer Tr. 824:9-14; RX-168; RX-40, col. 11, lines 15-17.

520. The Tobben patent discloses in figures 4 and 5 trapezoidal cross sections. RX-155, figures 4 and 5. Exact rectangular shapes are virtually unattainable.

521. The disclosure of figures 4 and 5 are the same as the disclosure of the "the method of

claim 9, wherein the remaining portion of the cap layer on at least one wiring line has a trapezoidal shape in cross section" disclosed in claim 15 of the '345 patent. Peltzer Tr. 824:15-21; RX-168; RX-40, col.11, lines 18-20.

522. The Tobben patent discloses in figures 4 and 5 trapezoidal cross sections. RX-155, figures 4 and 5. Exact rectangular shapes are virtually unattainable; they are generally tilted in with the top narrower than the bottom Peltzer Tr. 825:5-6.

523. The disclosure of figures 4 and 5 are the same as the disclosure of the "method of claim 15, wherein the trapezoidal shape includes top and bottom surfaces parallel to one another and side surfaces that extend inwardly from the bottom surface to the top surface." Peltzer Tr. 824:22-825:6; RX-40, col. 11, lines 21-24.

524. The Tobben patent discloses the stripping away of the photoresist layer and the removal of the planarization layer. RX-155, col. 4, lines 5-7. The Tobben patent further discloses that "a layer of silicon dioxide may be deposited over the surface of the grooved structure using . . . high density plasma deposition (HDP[)] techniques." RX-155, col. 4, lines 15-16.

525. The disclosures of the Tobben patent are the same as the disclosure of the "method of claim 9, wherein the remaining portion of the cap layer is partially etched and redeposited into gaps during the high density plasma chemical vapor deposition process." Peltzer Tr. 825:7-22; RX-168; RX-40, col. 11, lines 32-36.

526. The Tobben patent discloses the placement of the photoresist layer on the surface of the planarization layer, the development of the photoresist layer to remove the exposed or polymerized portions, creating grooves or slots. RX-155, col. 3, lines 21-21 and 28-30.

527. The disclosure in the Tobben patent is the same as the disclosure of the "method of claim 9, wherein the mask layer is a patterned photoresist layer" disclosed in claim 20 of the '345 patent. Peltzer Tr. 825:23-826:3; RX-168; RX-40, col. 12, lines 1-3.

528. The Tobben patent discloses a method for "forming a plurality of electrically conductive wires on substrate." RX-155, col. 1, lines 41-43. Further, "a layer of silicon dioxide [a dielectric material] may be deposited over the surface of the grooved structure using . . . high density plasma deposition (HDP techniques." RX-155, col. 3, lines 28-30.

529. The disclosures in Tobben are the same as a "method for forming conducting structures separated by gaps filled with dielectric material" disclosed in claim 21 of the '345 patent. Peltzer Tr. 826:8-18; RX-168; RX-40, col.12, lines 3-5.

530. The Tobben patent discloses "a semiconductor substrate [ ] comprising, for example, silicon is provided. It is noted that the upper surface [ ] of the substrate [ ] is relatively non-planar." RX-155, col. 2, lines 23-26.

531. The disclosure in the Tobben patent is the same disclosure as "providing a substrate containing silicon, the substrate having a surface" disclosed in claim 21 of the '345 patent. Peltzer Tr. 826:19-23; RX-168; RX-40, col. 12, lines 5-7.

532. The Tobben patent discloses a "metal layer [that is] a composite layer made up of a lower, relatively thin layer of titanium/titanium nitride, and intermediate, relative thick layer of sputtered aluminum; and an upper, thin antireflective coating (ARC) layer of titanium/titanium nitride." RX-155, col. 2, lines 36-40.

533. The disclosure in the Tobben patent is the same as the disclosure of "forming a surface layer comprising at least one material selected from the group consisting of titanium

nitride, titanium silicide and a titanium tungsten alloy, the surface layer disposed on the substrate surface" disclosed in claim 21 of the '345 patent. Peltzer Tr. 826:24-827:17; RX-168; RX-40, col.12, lines 7-10.

534. The disclosure in the Tobben patent is also the same as the disclosure of "forming a metal wiring line layer on the surface layer, the metal wiring line layer having an upper surface" also disclosed in claim 21 of the '345 patent. Peltzer Tr. 827:18-828:5; RX-185; RX-40, col. 12, lines 12-13.

535. The Tobben patent discloses a metal layer that is a composite metal layer "made up of a lower, relatively thin layer of titanium/titanium nitride, and intermediate, relative thick layer of sputtered aluminum; and an upper, thin antireflective coating (ARC) layer of titanium/titanium nitride." RX-155, col. 2, lines 36-40.

536. The disclosure in Tobben is the same as the disclosure of "forming a protective layer comprising at least one material selected from the group consisting of titanium nitride, titanium silicide and titanium-tugsten alloy, the protective layer disposed on the upper surface of the metal wiring line layer, the protective layer having a top surface" disclosed in claim 21 of the '345 patent. Peltzer Tr.; 827:18-828:5; RX-168 RX-40, col. 12, lines 13-19.

537. The Tobben patent discloses a "composite planarization layer [that] includes a spun-on silicon dioxide glass as a bottom portion [of the composite planarization layer] and a cap or upper layer [of the composite planarization layer] formed thereon, [with] . . . the cap layer compris[ing] a dielectric layer." RX-155, col. 3, lines 8-10. Further, "in one embodiment, the cap layer [] comprises silicon dioxide formed by, for example, plasma

enhanced chemically vapor deposited (PE CVD)." RX-155, col. 3, lines 12-13.

538. The disclosure in the Tobben patent is the same as the disclosure of "forming a cap layer comprising at least one material selected from the group consisting of an oxide, a nitride, and an oxynitride, the cap layer disposed on the top surface of the protective layer" disclosed in claim 21 of the '345 patent. Peltzer Tr. 828:6-16; RX-168; RX-40, col. 12, lines 19-23.

539. The Tobben patent further discloses that "[t]he photoresist layer is then developed to remove the exposed or polymerized portions, creating grooves or slots[]. The unremoved portions of the photoresist layer serve as a mask for patterning the underlying layers. As shown, the mask is used to pattern exposed portions [] of the underlying planarization layer." RX-155, col. 3, lines 28-34.

540. The disclosure of the Tobben patent is the same as the disclosure of "forming a patterned photoresist layer above the cap layer, said patterned photoresist layer covering selected portions of the cap layer and exposing other portions of the cap layer" disclosed in claim 21 of the '345 patent. Peltzer Tr. 828:17-829:2; RX-168; RX-40, col. 12, lines 23-27.

541. The Tobben patent discloses that "the mask is used to pattern exposed portions of the underlying planarization level." RX-155, col. 3, lines 32-34. The mask is "used to etch the exposed portions of the planarization layer within the grooves of the photoresist layer." RX-155, col. 3, lines 40-42. "[T]he exposed portion of the metal layer [] are etched away . . . to form the plurality of electrically conducive wires [] over the dielectric layer." RX-155, col. 3, lines 56-58.

542. Here, the metal layer [] is a composite layer made up of . . . an upper, thin antireflective

coating (ARC) layer of titanium/titanium nitride." RX-155, col. 2, lines 36-40.

"[G]rooves [] are etched into the . . . conductive metal layer [] to form the plurality of electrically conductive wires[,]" which are separated by grooves." RX-155, col. 3, lines 62-66.

543. The disclosure of Tobben is the same as the disclosure of "etching the exposed portions of the cap layer, the protective layer and the metal layer to form wiring lines separated by gaps" disclosed in claim 21 of the '345 patent. Peltzer Tr. 829:3-25; RX-168; RX-40, col. 12, lines 25-30.

544. The disclosure in the Tobben patent is the same as the disclosure of "forming a layer of high density plasma chemical vapor deposition dielectric material within the gaps to fill the gaps" disclosed in claim 21 of the '345 patent. Peltzer Tr. 830:1-14; RX-168; RX-40, col. 12, lines 31-35.

545. Dr. Ronald Schutz was designated as the 30(b)(6) witness for Infineon Technologies North America Corporation for the categories in the subpoena. JX-31C, Schutz Dep. Tr. 6:10-18.

546. Dr. Schutz worked for Infineon since August 1996. JX-31C, Schutz Dep. Tr. 7:7-11.

547. Dr. Schutz met Dirk Tobben in August 1996 and Dirk Tobben worked for Dr. Schutz. JX-31C, Schutz Dep. Tr. 9:21-10:line 4.

548. When Dr. Schutz started work for Siemans Infineon in August of 1996, Mr. Tobben was living and working in the United States. JX-31C, Schutz Dep. Tr. 24:19-24.

549. The other inventors of the Tobben patent, Bruno Spuler, Marin Gutsche, Peter Weigand were all living and working in the United States in August of 1996. JX-31C, Schutz Dep.

Tr. 24:25-25:12.

550. Dirk Tobben, Bruno Spuler, Marin Gutsche, and Peter Weigand were all working for Siemans or for some organization under Siemans in August of 1996. JX-31C, Schutz Dep. Tr. 25:13-26:14.

551. Mr. Tobben was working on dielectric deposition processes in August of 1996. JX-31C, Schutz Dep. Tr. 26:15-24.

552. Mr. Tobben was working on HDP-CVD for Dr. Schutz as one of the dielectric deposition processes in August of 1996. JX-31C, Schutz Dep. Tr. 27:4-10.

553. Mr. Tobben was working on projects where the planarization layer was made from spun-on silicon oxide glass in August of 1996. JX-31C, Schutz Dep. Tr. 39:11-16.

554. Mr. Tobben would occasionally use a two-layer cap layer in his spin-on glass work in August of 1996. JX-31C, Schutz Dep. Tr. 46:15-22.

555. U.S. Patent No. 5,219,788 ("the '788 patent" or "Abernathey patent") is entitled "Bilayer Metallization Cap for Photolithography." RX-156.

556. The Abernathey patent was filed February 25, 1991, which is well before the April 2, 1997 priority date claimed by the '345 patent from provisional application 60/041,790. RX-156.

557. The Abernathey patent shows an aluminum/copper layer under which is titanium and the substrate. On top of the aluminum/copper layer is the titanium nitride and SiO2. Peltzer Tr. 832:20-833:3; RPX-35.

558. The Abernathey patent describes forming conductive lines. RX-169. It discloses a bilayer cap for patterning the Metallization layer, using deep UV photoresist. RX-169.

559. According to co-inventor Liu, the conventional wiring line stack comprised of titanium nitride at the bottom, aluminum on top of the titanium nitride, and titanium and titanium nitride on top of the aluminum existed prior to the invention of the '345 patent. Liu Hr. Tr. 535:6-536:4.

560. Co-inventor of the '345 patent Lur is also a named inventor on U.S. Patent 5,580,701 patent. RX-46.

561. The '701 patent issued on December 3, 1996. RX-46.

562. The '701 patent discloses the use of two antireflective coatings. Peltzer Tr. 796:1-7; RX-46.

563. Specifically, the '701 patent discloses that the two antireflective coatings may be used on the surface of a poly line, as well as on other materials, including metal. Peltzer Tr. 797:9-14; RX-46.

564. Calculations of reflectivity of the type that an engineer would rely on concerning work related to the subject matter of the '345 patent demonstrate that the titanium nitride layer and the SiO2 on top in the Abernathey patent is the same as the first and second antireflective coatings formed on the metal wiring line in claim 1 of the '345 patent. Peltzer Tr. 833:13-17; 857:12-23; RPX-35; RPX-46.

565. The SiO2 layer on top in the Abernathey patent would serve as a cap layer to protect and possibly serve as a hard mask during etching if HDPCVD were deposited as in claim 9 of the '345 patent. Peltzer Tr. 833:18-834:1; RPX-35.

566. The titanium nitride layer between the silicon oxide layer and metal wiring line in Abernathey is the same as the protective layer in claim 21 of the '345 patent. Peltzer Tr.

834:2-6; RPX-35.

567. Abernathey does not disclose any process to fill the gaps. Peltzer Tr. 835:1-6.

568. The Abernathey patent does not disclose filling the gaps between metal lines with dielectric, but that is the next step in the manufacturing of integrated circuits and it would have been obvious to one with ordinary skill in the art to use HDP CVD to fill gaps between the metal wiring line layers of the '788 patent. Peltzer Tr. 833:4-12; RPX-35.

569. Filling the gaps between the metal wiring lines with high-density plasma chemical vapor deposition (HDPCVD) dielectrics appears in many references. Peltzer 837:7-9.

570. One skilled in the art would understand that one could use a variety of processes, including HDP-CVD which was popular and a well-published "in play" technology. Peltzer Tr. 835:12-18.

571. According to co-inventor Liu, HDPCVD was a known before the invention of the '345 patent. Liu Hr. Tr. 536:5-9.

572. According to co-inventor Lur, the inventors identified in the '345 patent did not invent the idea of using HDPCVD to fill gaps in wiring lines. Lur Tr. 105:15-22.

573. According to co-inventor Lur, Novellus advocated using HDPCVD for .35 um gap filling. Lur Hrg Tr. 106:13-107:3; CX 653.

574. According to co-inventor Liu, at least as of December 1995, HDPCVD was known to people for intermetal dielectric processing in integrated circuit fabrication. Liu Tr. 536:14-537:5.

575. J.T. Pan, D. Ma, T. Sahin, R. Tolles and S. Broydo (of Applied Materials) and H Miyamoto, K, Kishimoto, M. Suzuki, To. Homma and M. Kikuchi (of NEC Corporation)

presented an article at the June 18-20, 1996 VMIC Conference entitled "Integrated Interconnect Module Development (the "Pan publication.") RX-82; RPX-38.

576. The Pan publication discloses a substrate with titanium/titanium nitride underlaying an aluminum/copper/silicon Metallization layer with a titanium nitride layer on top. Peltzer Tr. 835:19-836:3; RX-82; RPX-38.

577. The Pan publication also discloses HDP CVD as a method of filling gaps in wiring line layers. RX-82; RPX-38, Peltzer Tr. 836:7-9.

578. One skilled in the art would combine the wire line stack from Abernathey with the teachings of the Pan publication to have the embodiment of the '345 patent. Peltzer Tr. 836:10-21; RPX-38.

579. One skilled in the art would combine the disclosures of the Pan publication and Abernathey patent because Abernathey does not disclose any particular process for gap fill, yet it is obviously required, and Figure 4(b) in the Pan publication shows excellent gap fill achieved with HDP CVD. RX-82; Peltzer Tr. 837:4-9.

580. One skilled in the art would be motivated to combine the Pan publication and the Abernathey patent based on the well-known difficulties of putting down the dielectric oxide and because HDP-CVD was well-known in publications as being superior to PECVD. Peltzer Tr. 837:4-9.

581. Further, one skilled in the art would be motivated to combine the Pan publication and the Abernathey patent because, if one were forming the metal wiring lines according to Abernathey, one would look to HDPCVD as being an improved method of forming the dielectric. Peltzer Tr. 837:10-12.

582. Moreover, if one used the dual antireflective coating approach of Abernathey, the resolution with which one could form the wiring lines is improved by removing the reflections, so one should be able to make smaller gaps between the wiring lines. Peltzer Tr. 837:10-18.

583. The dual layer antireflective coating in Abernathey with added resolution and therefore smaller gaps would lead someone with ordinary skill in the art to use HDPCVD instead of PECVD to fill smaller gaps, particularly because it was known that HDPCVD could fill gaps with small spaces. Peltzer Tr. 837:10-25.

584. Since the smaller gaps are harder to fill and PECVD would have trouble filling these gaps, one skilled in the art would be motivated to look for a technology that could fill the closer spacing and smaller gaps available by employing Abernathey because there would be a large monetary incentive to create smaller and faster integrated circuits. Peltzer Tr. 837:18-25.

585. In April 1996, Haruyoshi Yagi published an article entitled "Multilevel Interconnection Technology in System LSI" (the "Yagi publication"). RX-85.

586. The Yagi publication discloses a substrate with a titanium/titanium nitride layer underneath, an aluminum/copper wiring line with titanium on top of the wiring line and titanium nitride on top of the titanium. Peltzer Tr. 838:20-23; RX-85; RPX-37. On top and on the side is HDPCVD. Peltzer Tr. 838:23-25; RX-85; RPX-37.

587. Because the titanium layer is much rougher with a lower reflectivity than aluminum, it is an antireflective coating. Peltzer Tr. 840:7-13.

588. One skilled in the art would combine the disclosures of the Abernathey patent and the

Yagi publication because Abernathey does not disclose any particular process for gap-fill, yet it is obviously required, and Yagi specifically discloses that HDPCVD has been shown to result in void-free gap fill and in a significant reduction in complexity of the gap fill process. RX-85, p. 265.

589. The Yota publication disclosed titanium nitride under the aluminum/copper wiring layer with titanium nitride on top. Peltzer Tr. 842:23-24; RX-86; RPX-36. On the top and on the side is HDPCVD. Peltzer Tr. 842:24-25: RX-86; RPX-36.

590. One skilled in the art could be lead to combine the disclosures of the Abernathey patent and the Yota publication because the Abernathey patent does not disclose a particular process for gap-fill and the Yota publication disclosed HDPCVD. Peltzer Tr. 843:9-17; RX-86; RPX-36.

591. Yota et al, "Integration of ICP High-Density Plasma CVD with CMP and its Effects on Planarity for Sub-o.5um CMOS technology" ("the Yota publication") disclosed in August 1996 that "HDP CVD is a technology that utilizes simultaneous sputter etching and chemical vapor deposition of silicon dioxide using SiH4/)2Ar gases." RX-86; RPX-36.

592. The Yagi publication, Pan publication, and Yota reference, as well as the numerous other references, demonstrate that the use of HDP CVD that would have been combined with the Abernathey patent wiring line was obvious to one of ordinary skill in the art at the time of the '345 invention. Peltzer Tr. 858:8-24; RPX-32.

593. "RIE" stands for reactive ion etching. RX-70, col. 3, lines 43-44; Fair Tr. 1404:24-25.

594. According to Dr. Fair, the photoresist is developed and then the photoresist is used to etch the planarization layer. Fair Tr. 1405:14-17.

595. According to Dr. Fair, the mask layer in claim 9 above the cap layer can be photoresist. Fair Tr. 1407:14-15.

596. According to Dr. Fair, claim 9 is not limited to a photoresist mask and claim 9 is broad enough that it can cover other types of masking layers. Fair Tr. 1405:20-22.

597. According to Dr. Fair, in late 1996, at the time of the Tobben patent, HDP-CVD was already known by one skilled in the art as a technique for filling gaps in metal wiring lines. Fair Tr. 1409:14-18.

598. According to Dr. Fair, a wafer has no commercial utility after the metal wiring lines have been patterned without all of the subsequent steps in the wafer fabrication process , like gap-filling. Fair Tr. 1424:15-19, 1425:14-19.

599. The process of filling the gaps between wiring lines with a dielectric to prevent capacitance problems and to improve IC performance when electrical charges are moving through the wiring lines is referred to as the inter-metal dielectric ("IMD") process. Lur Tr. 27:11 – 27:21.

Best Mode

600. As one part of its invention, the '345 patent teaches the use of HDPCVD as an IMD process in manufacturing ICs with wiring lines that have relatively high aspect ratios, in place of PECVD or other more conventional IMD processes. CX-1 Col. 2:31-54.

601. The HDPCVD process can be performed using high density plasma that is attracted to a "biased" wafer in such a way that it deposits a dielectric material onto and into the gaps between wiring lines while at the same time "sputtering" or etching some of that dielectric material off of the top corners or sidewalls of the wiring lines, so that the gaps

are filled, substantially void-free, with dielectric material. Lur Tr. 48:7 – 50:18.

602. The "etch-to-deposition" ratio – referred to sometimes simply as the E/D ratio -- is a "reference index" that is used by some manufacturers of HDPCVD machines to describe the extent to which an HDPCVD process deposits dielectric material, on the one hand, versus the extent to which it simultaneously etches that material from the tops and sidewalls of wiring lines, on the other. Lur Tr. 115:8 – 115:12; Liu Tr. 511:5 – 511:17.

603. The '345 patent does not claim use of HDPCVD as an IMD process itself; nor could it, as use of HDPCVD as an IMD process was discussed in a number of published sources prior to the conception of the '345 invention by UMC engineers in 1996. Lur Tr. 105:15 - 106:8; *see, e.g.*, CX-3 at UMC 044456 (Pye article submitted with application for '345 patent, which discusses potential use of HDPCVD to fill gaps between wiring lines with high ratios of wiring line height to spacing between wiring lines.

604. The '345 specification discloses the fact that fully operational HDPCVD systems adequate for use in the invention of the '345 patent already exist and can be obtained from commercial vendors:

> High density plasma chemical vapor deposition (HDPCVD) systems have been developed which are capable of providing high quality dielectric layers at deposition temperatures significantly reduced from conventional CVD of dielectric layers. HDPCVD systems are commercially available (for example, from Novellus Systems, Inc.), which deposit a dielectric layer having superior density, moisture, resistance and planarization properties as compared to conventional CVD dielectric layers.

CX-1 Col. 4:61 – Col. 5:6.

605. The inventors of the '345 had significant experience with Novellus Systems as well as with other commercial vendors of HDPCVD systems, in connection with their work at

UMC and their invention of the methods claimed in the '345 patent, and they knew from that experience that those vendors routinely provided detailed information regarding the proper operation of HDPCVD machines to persons interested in using such systems. Liu Tr. 512:11 – 515:9, 530:21 – 531:13; CX-41C; CX-653.

606. The '345 specification discusses the "bias sputter component" in HDPCVD systems, whereby a bias can be introduced to the substrate to alter the deposition conditions, by "altering the energy of the CVD precursor gases and the extent to which etching and sputtering processes occur during deposition." CX-1 Col. 5:6-12.

607. The '345 specification provides much additional information on specific considerations relating to the bias sputter component of HDPCVD in filling gaps between metal lines, including discussion of the "dc self-bias effect," the use of "independently variable rf bias," the types of ions that may be used for purposes of the bias sputter component of HDPCVD, and the "angle of incidence of etching ions" and how that may effect the etch rate in HDPCVD. CX-1 Col. 5:23 – Col. 6:4.

608. The '345 specification discloses the need for attention to the relationship between the deposition component of HDPCVD and the sputter or etch component of the process. *See, e.g.*, CX-1 Col. 6:14-28.

609. Notwithstanding that the specification for the '345 patent contains substantial disclosure regarding the sputter-etch and deposition components of HDPCVD, the claims of the patent do not attempt to cover use of HDPCVD for filling gaps between wiring lines, either generally or with respect to any particular "optimum" or other level of gap filling that would require use of a particular E/D ratio. Fair Tr. 164:12 – 165:3.

610. In depositing a film using HDPCVD for purposes of filling gaps between wiring lines as part of the process of manufacturing ICs, a manufacturer can adjust certain parameters of the process, including the bias applied to the wafer, the temperature and pressure used in the process, the rates at which various materials are introduced into the process, and the position of the wafer within the HDPCVD machine during the process. Lur Tr. 76:18 –78:17, 79:6 – 79:16; CX-41C Listing parameters identified by Novellus for use in connection with its HDPCVD machine for manufacturing ICs with 0.25 micron minimum feature size.

611. The particular combination of parameters used by a manufacturer with respect to the use of HDPCVD to fill gaps between wiring lines in a particular manufacturing process is sometimes referred to as the "recipe" for that HDPCVD process. Lur Tr. 77:16 – 77:20.

612. The E/D ratio is a "reference index" that can be calculated for a particular HDPCVD recipe to express the extent to which that particular mix of parameters will produce sputter-etching as part of the HDPCVD process as compared with the extent to which that recipe will produce deposition of the material being deposited as part of the process. Lur Tr. 76:18 – 78:17, 115:2 – 115:12, 116:16 – 117:23.

613. During the 1996 to 1997 period, when UMC engineers were developing and refining the invention of the '345 patent, those same engineers and others at UMC worked with a number of manufacturers of HDPCVD machines, including Novellus, which ultimately sold UMC its first HDPCVD machines. Lur Tr. 55:20 – 57:12.

614. As part of its sale of HDPCVD equipment to UMC, Novellus provided UMC with information and training relating to E/D ratio and the equipment parameters that could

effect E/D ratio. Liu Tr. 512:11 – 515:9; CX-41C; CX-653.

615. The information that Novellus provided to UMC regarding E/D ratio and the related parameters for Novellus HDPCVD machines was the type of information that Novellus and other manufacturers of HDPCVD machines routinely make available to customers and potential customers who purchase or are interested in purchasing HDPCVD equipment for use in manufacturing ICs. Liu Tr. 530:21 – 531:14; Peltzer 1011:3 – 1011:8.

616. Any manufacturer that is provided with the type of basic information regarding parameters for the HDPCVD process that Novellus provided to UMC would be able to determine, with reasonable investigation, a recipe – and thereby an E/D ratio – to provide a satisfactory IMD process for its particular manufacturing context. Lur Tr. 124:25 – 126:11; Liu Tr. 515:11 – 515:23, 530:21 – 531:14, 548:5 – 548:11, 550:19 – 551:10; Peltzer Tr. 975:18 – 975:22 (the need for experimentation by each manufacturer to arrive at satisfactory HDPCVD parameters for its processes is inevitable. That is how UMC determined to use a [ ] E/D ratio (rather than the [ ] E/D ratio initially suggested by Novellus) for its particular wiring line configuration when it first began using HDPCVD to fill gaps between wiring lines in connection with the production of 0.25 minimum feature size ICs in UMC foundries, and it further is how UMC has determined an appropriate E/D ratio for subsequent generations of IC technologies. Lur Tr. 82:15 – 83:6, Lur Tr. 116:16 – 117:23, 124:25 – 125:17; 515:11 – 515:23, 520:13 – 521:4, 545:6 – 545:12, 559:23 – 560:10; CX-41C; CX-654C at UMC 105046

617. Before the installation of the first HDPCVD machine at UMC, Novellus provided UMC

with a recipe of proposed HDPCVD parameters and a recommended E/D ratio of [ ] for use in manufacturing ICs with minimum feature sizes of 0.25 microns using Novellus' SPEED HDPCVD machine. Lur Tr. 116:16 – 117:23, 124:25 – 125:17; Liu Tr. 515:11 – 515:23, 520:13 – 521:4, 545:6 – 545:12, 559:23 – 560:10; CX-41C; CX-654C at UMC 105046.

618. In a patent application that was cited in the prosecution history and considered by the examiner for the '345 patent, another manufacturer of HDPCVD equipment, Lam Research, similarly recommended certain HDPCVD parameters and a 0.32 E/D ratio for use in connection with its machines in manufacturing 0.25 micron ICs. Peltzer Tr. 969:21 – 972:14.

619. Another cited reference in the prosecution history of the '345 patent – a December 1995 journal article from Solid State Technology by Pye et al. – similarly recommended that a 0.35 E/D ratio was "representative of 0.25-micron gap fill with a 4:1 aspect ratio and vertical side wall structures." CX-3 at UMC 044459.

620. Although the '345 patent specifically provides for use of HDPCVD as part of the IMD process, HDPCVD is not limited to use in connection with filling gaps between wiring lines in ICs of a particular minimum feature size, with wiring lines of a particular aspect ratio or metal profile, or with any particular machine or other manufacturing equipment or material. CX-1; Liu Tr. 534:14 – 534:20.

621. In the training materials that Novellus provided to UMC, Novellus indicated that an appropriate E/D ratio could vary from as low as 0.05 to as high as 0.50. CX-653 at UMC 105043.

622. An appropriate recipe of parameters for use in HDPCVD for filling gaps between wiring line – and thus the appropriate E/D ratio – would be different, for example, depending on the minimum feature size of the IC being manufactured. Lur Tr. 83:1 – 83:14; Lur Tr. 124:5 – 124:17; Peltzer Tr. 974:9 – 974:19.

623. The appropriate parameters for use in HDPCVD for filling gaps between wiring lines – and thus the appropriate E/D ratio – would be different depending on the aspect ratio for wiring lines in the IC being manufactured, which will change as the minimum feature size of the IC changes. Lur Tr. 120:11 – 121:14, 124:25 – 125:17; Liu Tr. 517:19 – 519:15.

624. Different IC manufacturers may elect to have different aspect ratios for wiring lines in ICs, even of a single minimum feature size; e.g., the aspect ratio used by UMC in manufacturing ICs with minimum 0.18 micron feature size will not necessarily be the same as the aspect ratio used by other IC manufacturers for 0.18 micron ICs. Liu Tr. 559:14 – 559:22.

625. The appropriate parameters for use in HDPCVD for filling gaps between wiring lines – and thus the appropriate E/D ratio – would be different depending on the metal pattern or metal profile; (i.e., the precise shape and pitch) of the wiring lines in the IC being manufactured. Lur Tr. 120:11 – 121:14; Liu Tr. 516:17 – 517:13.

626. Different IC manufacturers may elect to use different metal profiles in manufacturing ICs and thus will need to use different HDPCVD recipes and different E/D ratios if they use HDPCVD to fill gaps between wiring lines. Liu Tr. 517:14 – 517:18, 559:14 – 559:22.

627. The prosecution history for that patent includes a published article that comments on the relationship between aspect ratios, metal profiles, and E/D ratios. Liu Tr. 519:16 –

520:12; CX-3 at UMC 044459.

628. The recipe or parameters used in connection with HDPCVD also can vary depending on a manufacturer's selection of materials to be used in connection with the HDPCVD process and how those materials are introduced into the process. Lur Tr. 80:14 – 80:25, 127:1 – 127:10; Liu Tr. 520:13 – 522:9, 559:14 – 559:22.

629. The recipe or parameters to be used when HDPCVD is used as an IMD process will vary depending on which particular HDPCVD machine is used. Peltzer Tr. 975:8 – 975:17.

630. Different manufacturers may use different parameters to control and describe the HDPCVD process within their machines. Lur Tr. 81:1 – 82:14; Liu Tr. 522:10 – 523:18; CX-40C.

631. The appropriate E/D ratio may vary depending on the depth and material of the cap layer that a manufacturer elects to use to protect against corner clipping of the wiring lines. Liu Tr. 551:15 – 552:5, 559:14 – 559:22.

632. In establishing the E/D ratio to be used in connection with an HDPCVD gap-filling step, a manufacturer must balance its desire for substantially complete filling of gaps between wiring lines with its desire for reasonable "throughput," which reflects the amount of time and resources it takes to complete the process step. Lur Tr. 78:7 – 78:17, 126:12 – 126:25.

VII. DOMESTIC INDUSTRY

633. As Dr. Water Lur, the Research Director for Complainant UMC, explained, the development of technologies relating to the manufacture of ICs is often described with reference to the minimum feature size contained within an IC. Lur Tr. 6:19 – 6:20.

634. Currently, most of the ICs being manufactured by UMC for commercial sale have minimum feature sizes of 0.25, 0.18, and 0.15 microns. Lur Tr. 9:9 – 9:21.

635. A principal role played by UMC-US with respect to UMC customers in the United States is "to make sure our customer understands what our new technology road map is and [to] explain to them the benefits of that technology" and to ensure that customer designs take advantage of it. Wan Tr. 683:10 – 684:1.

636. In recent years, UMC has begun to require its customers to incorporate ESD protection devices that use the '352 patented structure (including a PESD implant) in some circumstances and to recommend the use of that structure in other circumstances to ensure an appropriate level of ESD protection in ICs with advanced minimum feature sizes, because heightened protection from ESD events is particularly important for ICs with minimum feature sizes of 0.25 and smaller. Tang Tr. 412:2 – 412:15, 426:9 – 427:23.

637. Currently, approximately [ ] of UMC's United States-based customers use ESD protection devices that practice the '352 patent, with its distinctive PESD implant. Yang Tr. 563:25 – 564:2.

638. In order for a foundry, such as UMC, effectively to manufacture a new generation of ICs with a new, smaller feature size, the designs for the ICs prepared by its customers must take account of and be consistent with the manufacturing processes and tools used in UMC's foundries. As Complainants' Vice President for Field Engineering explained:

> When the customer design is brought into an UMC technology, for example the .18 micron process, it is designed specifically for that process. Typically, it will not work in any other semiconductor manufacturer's factory. Therefore, it's very

> important for us to work with that customer to ensure that all of the rules that we have provided [the customer] for designing into that process are followed so that the parts can be manufacturable, which is very important in our business and in our customer's business, because that impact the yield of the product. So in a way, I guess this could be thought of as manufacturing and design are integrated into one step here.

Wan Tr. 651:14 – 652:2.

639. Among Complainants' investments and activities in the United States relating to the articles of commerce at issue in this investigation (i.e. ICs manufactured by UMC with minimum feature sizes of 0.25 microns or smaller) are the following:

> UMC-US's establishment and maintenance of a [ ] facility in Sunnyvale, California, at a cost in excess of [ ] over the past [ ] years for rent, leasehold improvements, equipment, and software, much of which is used for Design Rule checks and related engineering and technical activities. Chen Tr. 453:9 – 455:11; Wan Tr. 663:3 – 665:5; CX-237 at UMC 029510 & UMC 029512;
>
> UMC-US's employment at its Sunnyvale facility of between [ ] employees – to whom UMC-US pays compensation in excess of [ ] per year – including [ ] field engineers and customer engineers who spend all or much of their work time providing engineering and technical support to UMC customers and Library Vendors in the United States to ensure compliance with UMC Design Rules. Chen Tr. 458:5 – 459:10; CX-250; CX-687 at UMC 105080; CX-691 at UMC 105090; and
>
> UMC and UMC-US's investment of over [ ] as well as support from UMC-US field and customer engineers for engineering work by Library Vendors and other I/P Providers to develop IC "building blocks" that comply with UMC Design Rules Chen Tr. 463:3 – 463:23; Lee Tr. 487:16 – 488:10, 491:25 – 492:4; Lam Tr. 623:18 – 624:10; CX-175C; CX-177C; CX-180C; CX-191C at 8, ¶ 6.5; CX-193C at 7, ¶ 6.5; CX-198C at 7, ¶ 6.5.

640. Design rules are established by each IC manufacturer as a way of ensuring that IC designs prepared for production at its foundry take account of and are consistent with the technologies used by the manufacturer at the foundry. Fair Tr. 131:8 – 131:22.

641. As Complainants' expert on ICs testified: "Design rules capture the ability of a [manufacturing] process to have a design made in that particular process. Basically, the design rules are the measures and rules that an integrated circuit designer would use to design a circuit for manufacture in a particular process. . . . [I]n developing those design rules, it takes a huge amount of activity, because you have to know how far apart features are spaced, what the pitch of various lines might be, what the minimum dimensions are, all of which give a designer some confidence that if he designs – he or she designs – in that process, that the circuits are going to work and you're not going to have failures or reliability problems." Fair Tr. 131:8 – 131:22.

642. Respondents' IC expert similarly testified that a manufacturer's "design rules are a critical part of the design and manufacturing process" and that it is essential that steps be taken to "check" compliance with each rule – to ensure that IC designs correspond precisely to the particular manufacturing processes and technologies to be used in their manufacture – in order to allow for the effective production of ICs from those designs. Peltzer Tr. 741:13 – 742:3, 865:2 – 866:15.

643. Respondent's IC expert further testified that a manufacturer's design rules are "very serious" parts of the IC production process and that each of the millions of internal components and wiring lines within an IC design must be checked to ensure that they follow those rules closely and carefully. Peltzer Tr. 741:17 – 742:3, 865:13 – 865:17.

644. A customer's compliance with a manufacturer's design rules is "closely related" to the performance that the customer's ICs will have after they are manufactured, and thus design rule compliance is of critical importance to customers as well as to manufacturers. Yang Tr. 594:4 – 594:15.

645. UMC provides each of its customers with a Design Rule Manual that contains UMC's [

] (collectively "Design Rules") for the minimum feature size or sizes in which the customer intends to design ICs. Yang Tr. 564:3 – 567:22.

646. In developing IC designs for manufacture at UMC foundries, UMC customers are required to comply with all UMC Design Rules that apply to their designs, so that those designs can be manufactured using UMC's manufacturing processes and technologies. Yang Tr. 567:23 – 569:1, 588:14 – 589:4; Lam Tr. 598:22 – 599:5 ("and if you do not comply with the rules, you may run [the] risk of either the chip will not [work] totally or you will have a yield problem, meaning . . . you will not get as good finished product as you can have".

647. To assist customers in ensuring that the millions of components and wiring lines in their IC designs comply with all applicable UMC Design Rules, UMC has developed a Design Rule Check ("DRC") process that may be used at various stages of a customer's development of IC designs and that is mandatory before the final "tape out" stage, immediately before the customer's design database is sent to the mask maker so that masks can be made to use in the manufacturing of ICs by UMC for the customer. Yang

Tr. 569:8 – 572:2; Lam Tr. 598:12 – 598:21.

648. UMC-US field engineers and customer engineers serve as "the front line" in dealing with UMC customers in the United States with respect to DRCs and other engineering or technical issues; if unusually complex customer issues arise the Design Support Division of UMC or other technical or process experts in Taiwan become involved. Tang Tr. 415:3 – 415:19, 446:11 – 447:5; Chen Tr. 471:18 – 472:8; Yang 570:8 – 570:19; Wan Tr. 682:9 – 682:15 (UMC-US field engineers are the "design experts" and UMC-US customer engineers are "process experts" for purposes of providing support to UMC customers in the United States.

649. The [ ] employees of UMC-US are organized into four divisions: (1) [

]. CX-250; CX-251.

650. In the last two of those divisions, UMC-US employs [ ] field engineers and approximately [ ] customer engineers. Chen Tr. 457:13 – 457:19; Wan Tr. 653:8 – 654:17; CX-250; CX-251.

651. UMC-US field engineers spend approximately [ ] of their work time on engineering and technical issues relating to DRCs and other "postsale" technical support for existing UMC customers and/or for Library Vendors already under contract to UMC. All of that work is done in the United States. Lam Tr. 597:19 – 597:25, 602:5 – 602:10; Wan Tr. 653:19 – 655:14, 656:16 – 657:4.

652. The remaining [ ] of the work time of UMC-US field engineers is devoted to "presale activities," which involve meeting with UMC customers and potential customers

to "assess what their technical requirements are so we can match that to the technology offerings that we have." Wan Tr. 655:15 – 655:21, 656:16 – 657:4.

653. UMC-US's director of worldwide field engineering summarized the role of UMC-US field engineers as follows: "Our main goal is basically to solve customer problems, on design issues," including "running" DRCs for customers, "presale and postsale" support on "technical problems," and work with Library Vendors and I/P Providers to "find solutions for customers." Lam Tr. 596:23 – 597:25.

654. As discussed further below, UMC-US engineers have assisted customers with design issues specifically related to the layout of ESD and PESD layers, the spacing between metal lines, and the number of metal lines to use in a particular design. CX-548C at UMC 63046 (ESD and PESD layers) and at UMC 63048 (noting concern as to whether design [

]); CX-586C (advice to customer regarding number of metal lines to use in a design.

655. The types of engineering and technical assistance that UMC-US field engineers provide to UMC customers in the United States is "essential" to the successful operation of UMC's foundry business. As the Vice President for Field Engineering testified: "[l]ook across any semiconductor company, they typically have a group called [the] field engineering group or field application engineering group, whose job it is to work with the customers to design the customer's product into that company's [processes] and/or technologies." Wan Tr. 655:22 – 656:8.

656. UMC-US customer engineers have "dual roles." They act in part as "account managers"

with responsibility for "securing the business from the customer," and they "also have the role of technical support from the process side," providing "the process knowledge that our customers need to integrate their chip into our [UMC's] process and technology." Wan Tr. 654:17 – 655:4.

657. UMC-US's [ ] customer engineers spend approximately [ ] of their work time on "account manager" functions and the other [ ] of their work time assisting UMC customers in the United States with technical or "process knowledge" issues. Wan Tr. 655:5 – 655:10.

658. UMC-US's customer engineers not only have engineering backgrounds in terms of their formal education and work experience (as do UMC-US field engineers), but they also have specific experience and knowledge working in a "semiconductor manufacturing environment," so that they are familiar with the types of manufacturing processes and technologies that are used in producing ICs. Wan Tr. 657:5 – 19.

659. UMC-US also provides training and materials to its customer engineers regarding the manufacturing processes and technologies used in UMC's foundries, including visits to UMC's foundries, so that they will have current and detailed information to provide to UMC customers and to use in assisting those customers with technical issues. Wan Tr. 657:20 – 658:22; CX-498C.

660. UMC-US's customer engineers receive a users guide that includes process flow information and an SEM that shows the formation of metal lines M1 through M6 after the process disclosed in the '345 patent has been performed and that further indicates that UMC uses HDP for filling the gaps between metal lines. CX-498C at UMC 57215,

57220, 57225.

661. Each UMC customer in the United States is assigned at least one UMC-US customer engineer who is responsible for providing technical support to the customer, including information and assistance relating to UMC's manufacturing processes and Design Rules. Wan Tr. 658:23 –659:18.

662. UMC-US customer engineers provide technical support even after a customer's IC design has cleared the DRC process and is in production or test production in one of UMC's foundries: "Many times when a design is already in production at UMC, there might be some manufacturing issues. So our CEs have to be very knowledgeable in the manufacturing side and work with the customers on potentially debugging a part" to determine whether the issue is "design related," "manufacturing related," "test related," or related to some other factor. Wan Tr. 659:23 – 660:20.

663. The type of process-related engineering and technical support provided by UMC-US customer engineers is a "commonly expected service" in the semiconductor foundry business that is essential to the successful operation of such a business. Wan Tr. 660:21 – 661:1.

664. The process of performing a DRC and generating a DRC report often occurs multiple times during the process of a customer's development of an IC design. Wan Tr. 665:6 – 665:22.

665. In addition to DRCs conducted at interim stages of the design process, before an IC design developed by a UMC customer in the United States is sent to UMC in Taiwan for "tapeout" and creation of a set of masks for use in manufacturing, it is subjected to a "job

deck view" DRC at UMC-US, which is "one final check" in the United States. Wan Tr. 661:23 – 662:10.

666. The performance of such a "job deck view" DRC in advance of the initiation of IC manufacturing at UMC's foundries is a "critical standard industry practice," because the cost of creating production masks can be very expensive -- [ ] -- and thus waiting until after manufacturing begins to discover a Design Rule violation could result in a loss of [ ] of dollars. Wan Tr. 662:11 – 663:2; Lam Tr. 620:21 – 620:24.

667. Both interim and "job deck view" DRCs are carried out at UMC-US by use of a "DRC deck," which is a software package that can be used to check every component of a customer's design database for compliance with every applicable UMC Design Rule. Yang Tr. 569:20 – 570:7.

668. UMC maintains a license for [ ] types of DRC decks that are manufactured by independent software vendors; those DRC decks are referred to by the trade names [ ]. Yang Tr. 569:20 – 570:7; Lam Tr. 599:6 – 599:16.

669. In addition to the licensed portion of the DRC deck, to perform a DRC, one must have a set of "command files" that include the UMC Design Rules. Yang Tr. 582:22 – 583:11; Lam Tr. 599:17 – 600:3.

670. Field engineers at UMC-US have written command files that correspond to the UMC Design Rules for each of the technologies in which UMC manufactures ICs for use in DRCs of UMC customer designs. Lam Tr. 600:11 – 601:16.

671. UMC-US field engineers also have done "design rule coding" to improve the DRC deck

software and command files used as part of the DRC process. Lam Tr. 606:18 – 608:13.

672. If a customer itself has a license for the [ ] DRC deck software, then it may download the command files for UMC Design Rules from a secure portion of the UMC website and perform a DRC itself for its partial or completed IC designs. Yang Tr. 569:23 – 572:2.

673. If a UMC customer in the United States does not have a license for DRC deck software, or if the customer simply wants or needs assistance in performing a DRC, then UMC-US field or customer engineers will assist in carrying out the DRC. Yang Tr. 569:23 – 572:2; Lam Tr. 602:1 – 602:10.

674. UMC-US maintains [ ] DRC deck software packages and has [ ] workstations at its Sunnyvale, California facility at which UMC-US field and customer engineers perform DRCs for UMC customers and work with UMC customers to resolve any issues that come up as part of the DRC process. Yang Tr. 572:3 – 573:11, 583:12 – 583:19; Wan Tr. 661:10 – 664:6.

675. After a DRC has been performed on a customer's IC design database, the DRC deck provides a DRC report of any violations of UMC Design Rules identified in the design database. Lam Tr. 604:1 – 606:17; CX-591.

676. UMC field engineers or customer engineers will then work with the UMC customer to determine whether the violations contained in a DRC are "true" or "false" violations – i.e., whether the reported violations in fact reflect a lack of consistency between the customer's IC design and UMC Design Rules – and, if a true violation exists, how best to correct that violation, a process that requires considerable technical expertise and

experience. Lam Tr. 604:1 – 606:17, 608:14 – 611:19, 614:7 – 616:8; Wan Tr. 665:23 – 665:25 ; CX-605.

677. To permit use of the '345 patent's manufacturing processes and technologies – including filling of gaps between wiring lines using UMC's particular HDPCVD recipes and cap layer – the wiring lines provided for in a customer's design must adhere to UMC Design Rules that limit the maximum aspect ratios for those wiring lines. Liu Tr. 518:4 – 518:16, 523:19 – 526:21.

678. The aspect ratio for wiring lines is the ratio of the height of the wiring lines to the space between the wiring lines. Liu Tr. 517:19 – 518:3.

679. In general, the greater the aspect ratio, the more difficult it is to fill gaps between wiring lines, and where aspect ratios are increased, adjustments must be made in the HDPCVD recipes used by a manufacturer so as to increase the E/D ratio, and corresponding changes may be needed in the cap layer used to protect the wiring lines from corner clipping during the HDPCVD process. Liu Tr. 518:4 – 519:15, 526:12 – 526:21.

680. In order to ensure the proper minimum spacing between wiring lines, UMC's [ ] for each generation of technologies include minimum wiring line spacing rules for each metal level within a customer's IC design. Liu Tr. 524:22 – 525:17; Yang Tr. 565:21 – 566:13; Lam Tr. 602:11 – 602:23; CX-162C at 18, 20, 22, 24 and 26; CX-163C at 16, 18, 20, 22, 24 and 26; CX-161C at 10, 12, 14, 16 and 18.

681. For each generation of technology, UMC has an [ ] that specifies the height of wiring lines for each metal level within an IC. Liu Tr. 525:18 – 526:11; CX-167C at UMC 100334.

682. The UMC [ ] provide Design Rules that establish the aspect ratios to be used in customer designs, and the steps taken by Complainants to ensure compliance with those rules ensure that production of customer designs at UMC's foundries can be accomplished effectively using the manufacturing processes and technologies of the '345 patent. Liu Tr. 526:3 – 526:21.

683. The minimum spacing requirements of the UMC Design Rules have been incorporated into the DRC command files written by UMC-US engineers and used in the DRC process, thus ensuring that customer designs comply with those requirements. Lam Tr. 602:24 – 603:25; CX-557 at UMC 63662 – 63667 (UMC command file for checking minimum width of metal lines 1-6 and minimum spacing between metal lines 1-6).

684. If a DRC identifies a violation in a UMC customer's IC design with respect to the minimum spacing between metal lines, then a UMC-US customer engineer or field engineer will work with the customer to resolve the violation, so that the customer's IC design can be put into production in UMC's foundry and make use of the manufacturing processes of the '345 patent. Yang Tr. 572:9 – 573:22; Lam Tr. 604:1 – 606:17, 608:14 – 611:19; CX-591 at UMC 73915 (UMC-US engineers identify violations [ ]); CX-605 (UMC-US engineers identify [ ]).

685. UMC-US engineers also developed a special "two-pass" DRC method that reduced the level of reported "false" errors that arose because of differences between the general topological rules and the rules for memory, including differences in the spacing between

metal lines. Lam Tr. 606:18 – 608:13.

686. This new method of performing DRCs enabled UMC-US to eliminate [ ] "false" errors and thereby to improve the quality of DRC reports. Lam Tr. 608:4 – 608:9.

687. An example of UMC-US identifying a "false error" through its inventive new DRC approach is shown on CX-605C. Lam Tr. 610:16 – 611:19; CX-605C at UMC 76497 (finding false violation [ ].

688. Strict compliance with Design Rules relating to the aspect ratios for wiring lines is particularly important in light of the significant role played by wiring line structures in the overall performance of ICs, especially with respect to ICs that use advanced technologies with minimum feature sizes of 0.25, 0.18 and 0.15 microns. Wan Tr. 666:10 – 667:4.

689. In addition, the UMC [ ] and [ ] for each size technology specify the spacing required for the source/drain regions of ESD protection devices to permit the effective use of the PESD implant and other structures of the '352 patent. Yang Tr. 566:14 – 568:1, 590:6 – 591:14; CX-39C; CX-162C through CX-166C; Fair Tr. 384:16 – 385:7.

690. UMC's [ ] include provisions that specify the structures that must be included in ESD protection devices to be manufactured by UMC, among which are provisions that specifically address the spacing between structures that must be used in order to allow for a PESD implant as part of ESD protection devices that practice the '352 patent. CX-163C; CX-164C to CX-166C; Tang Tr. 409:11 – 410:1.

691. UMC's [ ] specify that

customers who wish to use cascode-type ESD protection devices [

]. Tang Tr. 412:2 – 412:15, 426:9 – 427:23; CX-162C at 29; CX-163C at 29.

692. Of UMC's [ ] United States-based customers, [ ] customers currently make use of ESD protection devices that use the PESD implant and the other structural features of the '352 patent. Yang Tr. 563:24 – 564:2, 569:2 – 569:7.

693. UMC-US has a special DRC command file to allow its engineers to perform DRCs for ESD protection devices in IC designs with minimum feature sizes of 0.18 microns, which includes commands that pertain to the PESD implant of the '352 patent. Lam Tr. 611:20 – 613:13, 647:13 – 648:4; CX-603C; CX-604C; CX-609C.

694. The fact that UMC's design rule documents do not mention the '345 patent or the '352 patent and do not specifically refer to the inventions, processes or technologies embodied in those patents is neither surprising nor relevant. Fair Tr. 294:5 – 294:20.

695. Design rules are intended to convey information needed by IC designers to ensure that their designs can be effectively manufactured using the manufacturing processes and technologies employed in the foundry where IC production will take place; to do so, design rules need not actually discuss the manufacturing processes and technologies, they need only communicate what design parameters and features must be maintained so that the designs can be "enabled" by manufacturing processes and technologies. Fair Tr. 294:5 – 294:20; Wan Tr. 684:2 – 684:16.

696. Since July or August of 1999, UMC-US has maintained a [ ] square foot facility in Sunnyvale, California, approximately [ ] percent of which is used for the work of the [ ] field engineers and [ ] customer engineers employed by UMC-US to provide engineering and technical assistance to UMC customers in the United States. Chen Tr. 452:9 – 452:17, 453:6 – 453:8; Wan Tr. 661:2 – 661:9.

697. In the years [ ], UMC-US has invested approximately [ ] in lease payments for its Sunnyvale facility. Chen Tr. 455:4 – 455:11; CX-237 at UMC 029512.

698. Within UMC-US's Sunnyvale facility, there is an "incubator room" and other smaller work rooms that are equipped and maintained so that UMC customers can work with UMC-US field and customer engineers to perform DRCs and other design-related engineering and technical work. Chen Tr. 452:18 – 453:5; Wan Tr. 661:22, 662:18 – 663:2.

699. UMC-US invested approximately [ ] for leasehold improvements and equipment to permit use of its Sunnyvale facility to perform DRCs and provide other assistance to UMC customers, including workstations that are used for DRCs and related work. Chen Tr. 453:9 – 453; Wan Tr. 663:3 – 663:8; CX-237 at UMC 029510.

700. UMC-US also has invested approximately [ ] in DRC deck software and other software used in its Sunnyvale facility to perform DRCs and other design-related work with or for UMC customers, so that their IC designs will take account of and be consistent with UMC manufacturing processes and technologies. Wan Tr. 663:9 – 665:5.

701. In [ ], UMC-US paid [ ] in employee salaries and bonuses to its [ ]

employees, and it paid another [ ] dollars in employee salaries and bonuses during the first six months of [ ]. Chen Tr. 458:5 – 459:10; CX-687 at UMC 105080; CX-691 at UMC 105090.

702. Focusing solely on UMC-US field engineers and customer engineers, UMC pays approximately [ ] in salaries and approximately [ ] in benefits per year to those employees. Chen Tr. 458:5 – 459:13.

703. The DRCs and related work performed by UMC-US field and customer engineers adds value to the ICs that UMC manufactures for its customers by ensuring that the IC designs – and thus the ICs manufactured by UMC – take account of and are consistent with UMC manufacturing processes and technologies, including the processes and technologies of the '345 patent and '352 patent. Chen Tr. 466:19 – 466:22.

704. In addition to the investment and activities of UMC-US designed to support customer compliance with UMC Design Rules, UMC's senior ESD engineer, Mr. Tang, met with one of UMC's largest customers in the United States and provided that customer with engineering and technical advice that led that customer to incorporate into all of its IC designs ESD protection devices that practice the '352 patent. Tang Tr. 413:10 – 415:2.

705. Another way in which UMC has sought to support customer compliance with UMC Design Rules – and thereby to ensure that customer IC designs will take account of and be consistent with UMC manufacturing processes and technologies, including those of the '345 and '352 patents – is through the development of "free libraries" and "non-free libraries" developed and made available by Library Vendors and other I/P Providers. Lee Tr. 479:24 – 480:6; Wan Tr. 667:15 – 668:25.

706. Library Vendors develop designs for functional "building blocks" or standard cells that can be incorporated as components in IC designs. Tang Tr. 405:17 – 405:23; Lee Tr. 481:23 – 482:11; Wan Tr. 669:24 – 670:9 ("[f]or example, a typical [IC] today will have a million gates, what they call a million gates, which is a million of these standard cells connected together in various ways to perform the function that [designers] want").

707. UMC has entered into contracts with two California-based Library Vendors, Virtual Silicon Technologies ("VST") and Artisan Components, Inc. ("Artisan"), to develop libraries of standard cells that are specifically "ported" to UMC's manufacturing processes and technologies and that are then made available to UMC customers free-of-charge. Tang Tr. 405:24 – 407:9; Lee Tr. 481:2 – 481:7; Lam Tr. 616:14 – 617:18.

708. Under its contracts with VST and Artisan, UMC has [ ] those Library Vendors approximately [ ] in [ ] for the development of standard-cell libraries that can be used by UMC customers without charge. Chen Tr. 463:3 – 463:23; Lee Tr. 482:16 – 483:10, 484:7 – 492:16; CX-168C; CX-179C; CX-180C; CX-181C; CX-182C; CX-169C; CX-170C; CX-173C; CX-177C; CX-175C; CX-193C; CX191C; CX-196C; CX-198C; CX-189C; and CX-194C.

709. UMC has [ ] VST to develop [ ] for UMC customers for 0.25, 0.18, and 0.15, and 0.13 technologies, and it has [ ] Artisan to develop [ ] for UMC customers for 0.25 and 0.18 technologies. Tang Tr. 409:5 – 409:10; Lee Tr. 482:16 – 492:16; Tr. 575:1 – 575:12; *see, e.g.*, CX-191C at 17 ([

]); CX-193C at 16 ([

]); CX-198C at 18 ([

]); CX-168C at 22 ([

]); CX-179C at 4

([

]); CX-229.

710. There are over [ ] engineers working at VST on UMC [ ]. Yang Tr. 578:25 – 579:5, 593:1 – 593:11.

711. In order to ensure that VST and Artisan design their libraries specifically for use with UMC's processes for each size technology, the contracts require that UMC provide these vendors with all of UMC's design rules. CX-179C at 3; CX-168C at 21; CX-193C at 20; CX-191C at 22; CX-198C at 22.

712. UMC has entered into a number of additional agreements with VST and Artisan for these vendors to develop new cells for their respective libraries or to recharacterize existing cells based on a change in UMC's process technology. [

]

713. VST currently is designing a 0.10 [ ] for UMC customers, and Ed Wan of UMC-US currently is negotiating with Artisan for development of a [ ] for UMC customers. Yang Tr. 575:4 – 575:15.

714. Engineers at UMC-US and UMC-Taiwan have worked together to develop the specifications for the standard cells to be developed by VST and Artisan, which include requirements that the cells developed by those Library Vendors for UMC be consistent with UMC Design Rules. Yang Tr. 574:1 – 574:11; Lam Tr. 616:20 – 617:18.

715. Most UMC customers make use of the Library Vendors' "building block components" or standard cells in preparing their IC designs for manufacture by UMC. Lee Tr. 481:23 – 482:11.

716. From [ ], there were over [ ] customer downloads of VST design kits from VST's website and over [ ] customer downloads of tape-out kits. CX-313C.

717. There are also many customers in the United States that utilize the library Artisan developed to be used with UMC's process technology. CX-578C.

718. UMC customers are permitted to use the VST and Artisan [ ] only in connection with IC designs that will be manufactured by UMC; indeed, because those libraries are "foundry-specific" and designed for the manufacturing processes and technologies used in UMC's foundries, they would not be appropriate for use in IC designs prepared for manufacture in other foundries. Lee Tr. 482:12 – 482:15; Yang Tr. 581:15 – 581:22.

719. The standard cells developed by VST and Artisan for free libraries for UMC customers

must comply with all applicable UMC Design Rules; this ensures that, if UMC customers incorporate one or more standard cells into their IC designs, then those portions of the customer's IC designs necessarily will take account of and be consistent with UMC's Design Rules. Tang Tr. 408:10 – 409:4, 410:2 – 410:25; Lee Tr. 481:8 – 481:16, 486:9 – 486:24; Yang Tr. 574:12 – 574:25, 578:16 – 578:22.

720. In fact, UMC's [ ] to VST and Artisan under contracts with UMC are [ ] upon the standard cells developed pursuant to those contracts passing a DRC; [ ] a UMC-US field engineer reviews the Library Vendor's work and approves the engineering work done by the Library Vendor. Yang Tr. 581:23 – 582: 21 .

721. Library Vendors subject the "building blocks" or standard cells that they develop for UMC free libraries to the same type of DRC process that UMC customers use to check their IC designs. Tang Tr. 411:1 – 412:1; Yang Tr. 577:9 – 577:16; Lam Tr. 598:12 – 598:21.

722. As part of the development process by which VST and Artisan have developed free libraries for UMC customers, UMC-US field engineers and customer engineers provide engineering and technical support in the United States to answer questions from the Library Vendors, assist with DRCs, and provide advice in resolving reported Design Rule violations with respect to standard cells in the libraries. TAng Tr. 406:11 – 408:1; Yang Tr. 577:17 – 578:24.

723. For example, [ ], a field engineer at UMC-US, performed a DRC on [ ]. Thereafter, on [

]

CX-343C.

724. Thus, UMC-US engineers "check the work [of Library Vendors] to make sure the libraries are clean so when the customers use them, they don't have to worry about having library elements that are violating DRC rules." Wan Tr. 668:5 – 668:25.

725. During the development of a [ ] by VST or Artisan, UMC-Taiwan and UMC-US engineers have worked with Library Vendor engineers, including by participating in weekly telephone or video conferences, to ensure that the standard cells being developed for the libraries are consistent with UMC Design Rules and are otherwise responsive to the needs of UMC customers. Yang Tr. 574:12 – 576:23; Lam Tr. 604:1 – 606:17, 617:19 – 619:20; CX-325C; CX-591C.

726. UMC-US engineers have arranged for video conferences so that UMC, UMC-US and VST could discuss technical issues, including issues related to PESD implants. CX-622C.

727. In addition to Design Rules, UMC also provides library vendors – as well as customers and IP vendors – with the UMC [ ], which is "created for improving the integration environment with uniform gdsii layer sequences. It is believed that a standard interface should be delivered to align databases from different sites (customers/UMC/library and IP vendors)." CX-31C at UMC 100125.

728. The [ ] is "mandatory for a library/IP vendor to adopt it in your products provided to UMC customers in order to reduce the trouble they might

encounter during the database merging." CX-31C at UMC 100125.

729. The [ ] defines layers for Logic and Mixed Mode processes for 0.18, 0.15 and 0.13 micron technology, and [ ] in the Official Layer Mapping Table provides for a PESD implant. CX-31C at 100125 and 100128.

730. UMC-US engineers also have worked with Library Vendors in the United States, as well as with UMC engineers in Taiwan, to evaluate test chips for standard cells to be included in free libraries, to subject the designs for those cells to DRCs, and to refine or "fine tune" the designs of those standard cells. Lee Tr. 485:2 – 485:23; Lam Tr. 619:21 – 622:9; CX-508.

731. For example, if a DRC performed on a standard cell developed by VST or Artisan indicates that one or more violations exist with respect to the standard cell, then "UMC USA field engineers or customer engineers will do a further check to see if this error is genuine or is a false alarm" and then will work with the Library Vendor (as well as the UMC Design Support Division and other technical experts in Taiwan, if necessary) to determine what steps should be taken to correct the violation or to obtain a "waiver" from UMC process engineers for the apparent violation. Tang Tr. 411:11 – 412:1; Lam Tr. 604:1 – 606:17, 614:7 – 616:8; CX-508C; CX-563C; CX-591C; CX-606C.

732. All of the standard cells in the VST and Artisan "free libraries" include wiring lines that must comply with the applicable UMC [

], including the rules relating to the height of wiring lines and the spacing between wiring lines, which establish the aspect ratio for those wiring lines. Yang Tr. 581:5 – 581:10.

733. Input/output or I/O cells are one of the three principal types of "building block" cells developed by VST and Artisan for the [ ] made available to UMC customers. Lee Tr. 480:9 – 480:23, 483:20 – 484:3; CX-229.

734. Because of their complexity, I/O cells are the most [ ] of the standard cells developed by VST and Artisan, in terms of [ ] by UMC. Lee Tr. 490:23 – 491:7; CX-168C at 22 ([

]).

735. I/O cells must be designed to include ESD protection devices adequate to protect the internal components of the IC. Tang Tr. 406:4 – 406:10.

736. The I/O cells developed by VST and Artisan in the United States for inclusion in the UMC [ ] incorporate ESD protection devices with the PESD implant and other structural features of the '352 patent, consistent with Complainants' claim construction for that patent. Tang Tr. 412:17 – 413:9; Yang Tr. 579:6 – 581:4; CX-229C; CX-26C through CX-29C ([

]); CX-618C and CX-619C ([

]); CX-342C ([

]); CX-345C at UMC 91982 ([

]).

737. Nimcho Lam, the Director of Worldwide Field Engineering at UMC-US, communicates with library vendors and UMC employees regarding ESD issues, including the use of PESD implants disclosed in the '352 patent. CX-415C; CX-416C; CX-422C; CX-465C; CX-466C; CX-468C; CX-469C; CX-470C; CX-476C; CX-481C; CX-485C; CX-490C; CX-617C; CX-618C; CX-619C.

738. Mr. Lam was involved, for example, in identifying and trying to resolve the ESD problems [ ]. CX-438C; CX-450C; CX-452C; CX-454C.

739. UMC-US field engineers also have performed DRCs on I/O cells developed by VST and Artisan and have worked with those Library Vendors [

]. Lam Tr. 611:20 – 614:22; CX-549C; CX-603; CX-604; CX-606C.

740. In addition to using specialized ESD DRCs, UMC also has used [

]. CX-609C at UMC 89810; Lam Tr. 647:13 – 648:4.

741. [

]

742. [

]

743. To date, UMC has paid approximately [

]. Chen Tr. 463:3 – 463:23.

744. UMC pays [

]. Lee

Tr. 487:16 – 488:10, 491:25 – 492:4; Lam Tr. 623:18 – 624:7; CX-191C at 8, ¶ 6.5; CX-

193C at 7, ¶ 6.5; CX-198C at 7, ¶ 6.5.

745. The customer support that VST has provided to UMC customers in the United States has included technical advice relating to ESD protection devices and the use of PESD implants in such devices. Lam Tr. 624:11 – 625:15; CX-588C ([

]); CX-347C ([

]); CX-348C ([

]); CX-311C ([

]).

746. [ ], the ESD engineer at VST in the United States, frequently communicates with UMC regarding ESD issues, including issues relating to the use of the PESD implants disclosed in the '352 patent. Lam Tr. 625:5 – 625:15; CX-328C; CX-329C; CX-330C; CX-332C; CX-333C; CX-334C, CX-338C; CX-344C; CX-346C.

747. VST has also provided UMC customers with an updated [

]. CX-316C.

748. UMC also pays [

]. Lee Tr. 487:16 – 488:10, 491:25 – 492:4; Lam Tr. 624:19 – 624:10; CX-180C; CX-177C; CX-175C.

749. [ ], the ESD engineer at Artisan in the United States, frequently communicates

with UMC regarding ESD issues, including issues related to the use of the PESD implants disclosed in the '352 patent. Lam Tr. 625:5 – 625:13; CX-425C; CX-427C; CX-464C; CX-466C; CX-468C; CX-469C; CX-476C; CX-627C; CX-632C.

750. The investment made by Complainants in the United States of both money and time (on the part of UMC-US field and customer engineers) in engineering work by VST and Artisan has been augmented by related investment and activities with respect to I/P Providers. Wan Tr. 670:10 – 674:16.

751. Whereas Library Vendors develop libraries of standard "building blocks" or cells commonly used in IC designs, I/P Providers develop more complex or specialized cells for sale to one or more IC designers. Lam Tr. 625:16 – 626:2; Wan Tr. 670:10 – 671:5.

752. UMC has identified I/P Providers in the United States and has provided support to them to ensure that the cells they develop for UMC customers are ported to UMC manufacturing processes and technologies. CX-229.

753. That support has come in part in the form of engineering and technical advice and assistance from UMC-US field and customer engineers, to ensure that I/P Providers who are designated to develop cells for sale to UMC customers have access to and understand the UMC Design Rules. Lam Tr. 626:10 –627:1; Wan Tr. 670:10 – 672:6 ("we work closely with [designated I/P Providers] to make sure that [their] IPs are also DRC clean and meet all the latest UMC rules, so that when they sell it to an end customer, . . . we know that the IP is DRC clean and meets all our rules").

754. UMC-US also has worked with I/P Providers to develop test chips for cells that are ported to UMC technologies and to manufacture those test chips as part of the UMC

"silicon shuttle" program. [

] Lam Tr. 627:2 – 627:15; Wan Tr. 672:7 – 673:12.

755. UMC-US engineers also will run DRCs for the designated I/P Providers to ensure that the cells they develop for UMC customers are consistent with UMC Design Rules, using UMC-US's facilities, equipment, and software. Lam Tr. 627:16 – 627:25; Wan Tr. 670:10 – 671:11; CX-563C ([ ]); CX-494C ([ ]).

756. Complainants support designated I/P Providers to provide UMC customers in the United States access to various cells needed for cost-effective IC design that are consistent with UMC's Design Rules and that can be manufactured in UMC's foundries using UMC's manufacturing processes and technologies. Lam Tr. 626:3 – 626:9; Wan Tr. 673:13 – 674:16.

CONCLUSIONS OF LAW

1. The Commission has personal jurisdiction over the parties and subject matter jurisdiction over this investigation. *See* Op. at 1; FF 6, Section II.

2. The importation or sale requirement of section 337 has been established for purposes of this Initial Determination. *See* Op. Section II, at 4; FF, Sections I and II.

3. None of the accused devices practices any asserted claim of the '352 patent literally or under the doctrine of equivalents. *See* Op. at 31, 35.

4. It has not been demonstrated that Respondents are prohibited from challenging the validity of the '352 patent due to assignor estoppel. *See* Op. at 42.

5. It is found by clear and convincing evidence that claims 1 and 2 of the '352 patent are invalid pursuant to 35 U.S.C. § 102 due to anticipation by the Umemoto publication. *See* Op. at 51.

6. It is found by clear and convincing evidence that claim 8 of the '352 patent is invalid pursuant to 35 U.S.C. § 103 for obviousness due to the Umemoto publication in view of the Soeda publication, and due to the Umemoto publication in view of the Kamioka publication. *See* Op. at 63, 67.

7. If it were found that the asserted '345 patent claims were valid, it would be found that Respondents' old process infringes those claims. *See* Op. at 99.

8. Respondents' new process does not practice any asserted claim of the '345 patent. *See* Op. at 120.

9. It is found by clear and convincing evidence that each element of the asserted patent

claims is disclosed in Tobben, or in the case of claim 13 is obvious in view of Tobben and the knowledge of a person of ordinary skill in the art. Thus, the asserted claims of the '345 patent are anticipated, or made obvious, by the Tobben patent. *See* Op. at 134.

10. It is found by clear and convincing evidence that the Abernathey patent in combination with other art renders obvious each asserted claim of the '345 patent. *See* Op. at 138-140.

11. It has not been shown by clear and convincing evidence that any claim of the '345 patent is invalid pursuant to 35 U.S.C. § 102(g). *See* Op. at 140-41.

12. It has not been shown by clear and convincing evidence that any claim of the '345 is invalid pursuant to 35 U.S.C. § 112 due to a failure to disclose the best mode. *See* Op. at 146.

13. It has been demonstrated that with respect to the '345 patent, a domestic industry exists in satisfaction of the requirements of section 337(a)(2). *See* Op. at 155-56.

INITIAL DETERMINATION AND ORDER

Based on the foregoing opinion, findings of fact, conclusions of law, the evidence, and the record as a whole, and having considered all pleadings and arguments, including the proposed findings of fact and conclusions of law, it is the Administrative Law Judge's INITIAL DETERMINATION ("ID") that no violation of section 337 of the Tariff Act of 1930, as amended, exists in the importation into the United States, sale for importation, or the sale within the United States after importation of certain integrated circuits or products containing same by reason of infringement of claims 1, 2 or 8 of U.S. Letters Patent 5,559,352, or claims 1, 3-16 or 19-21 of U.S. Letters Patent 6,117,345.

The Administrative Law Judge hereby CERTIFIES to the Commission this ID, together with the record of the hearing in this investigation consisting of the following:

1. The transcript of the hearing, with appropriate corrections as may hereafter be ordered by the Administrative Law Judge; and further,

2. The exhibits accepted into evidence in this investigation as listed in the attached exhibit lists.

In accordance with 19 C.F.R. § 210.39(c), all material found to be confidential by the Administrative Law Judge under 19 C.F.R. § 210.5 is to be given *in camera* treatment.

The Secretary shall serve a public version of this ID upon all parties of record and the confidential version upon counsel who are signatories to the Protective Order (Order No. 1) issued by the Administrative Law Judge in this investigation, and upon the Commission

investigative attorney.

To expedite service of the public version, counsel are hereby ORDERED to serve on the Administrative Law Judge by no later than May 14, 2002, a copy of this ID with those sections considered by the party to be confidential bracketed in red, accompanied by a list indicating each page on which such a bracket is found.

Pursuant to 19 C.F.R. § 210.42(h), this ID shall become the determination of the Commission unless a party files a petition for review pursuant to § 210.43(a) or the Commission, pursuant to § 210.44, orders on its own motion a review of the ID or certain issues herein.

Sidney Harris
Administrative Law Judge

Issued: May 6, 2002

CERTAIN INTEGRATED CIRCUITS, PROCESSES FOR MAKING SAME, AND PRODUCTS CONTAINING SAME

INV. NO. 337-TA-450

CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the attached Recommended Determination was served upon Shival P. Virmani, Esq. and upon the following parties via first class mail, and air mail where necessary, on November 12, 2002.

Marilyn R. Abbott, Secretary
U.S. International Trade Commission
500 E Street, S.W.
Washington, D.C. 20436

FOR COMPLAINANT UNITED MICROELECTRONICS CORPORATION, UMC GROUP (USA), AND UNITED FOUNDRY SERVICE, INC.:

Steven J. Routh, Esq.
David A. Kikel, Esq.
Sten A. Jensen, Esq.
Hogan & Hartson
555 13th Street, N.W.
Washington, DC 20004

William H. Wright, Esq.
Joanne L. Leasure, Esq.
Hogan & Hartson
Biltmore Tower
500 S. Grant Avenue
Suite 1900
Los Angeles, CA 90071

CERTAIN INTEGRATED CIRCUITS, PROCESSES FOR MAKING SAME, AND PRODUCTS CONTAINING SAME

INV. NO. 337-TA-450

FOR RESPONDENTS SILICON INTEGRATED SYSTEMS CORP., AND SILICON INTEGRATED SYSTEMS CORPORATION:

Tom M. Schaumberg, Esq.
Adduci, Mastriani & Schaumberg, LLP
1200 Seventeenth Street, N.W. - 5th Flr.
Washington, D.C. 20036

Kirk R. Ruthenberg, Esq.
Edward H. Rice, Esq.
Sonnenschein Nath & Rosenthal
Suite 600, East Tower
1301 K Street, N.W.
Washington, D.C. 20005

FOR NON-PARTY BURNS, DOANE, SWECKER, & MATHIS, LLP:

F. David Foster, Esq.
Sturgis M. Sobin, Esq.
Charles Abernathy, Esq.
Miller & Chevalier Chartered
655 Fifteenth Street, N.W. - Ste. 900
Washington, D.C. 20005

David D. Hudgins, Esq.
Hudgins Law Firm
515 King Street - Ste. 400
Alexandria, VA 22314

Robert DeVos, Esq.
Burns, Doane, Swecker & Mathis, LLP
1737 King Street - Ste. 500
Alexandria, VA 22314

PUBLIC MAILING LIST

Donna Wirt
LEXIS - NEXIS
1150 18th Street, NW
Suite 600
Washington, D.C. 20036

Ronnita Green
West Group
901 Fifteenth Street, NW
Suite 230
Washington, D.C. 20005