Hardware Schematic Description

Background:

Two pieces of hardware have been developed for the NOAA, an IF Digitizer and an RF Digitizer. The IF digitizer is a complete subset of the RF digitizer. We maintain one schematic for both designs. The IF digitizer has been extensively tested and it meets GOES-R specifications. The RF digitizer has not been demonstrated to meet GOES-R specifications. It is recommended that users refer primarily to the IF design.

Device Description:

The IF DIGITIZER was designed as part of a weather receiving station for the NOAA. The weather station receives weather images down-linked via a satellite link and displays them for a user. The description of the system is shown in figure 1. The weather images come down at an RF frequency of 1.69 GHz. An antenna is used to receive this signal, then the signal is fed into a downconverter that downconverts the RF frequency to an IF frequency of 140 MHz. From there, our board was designed to simply bring the 140 MHz signal down to baseband, and convert it from analog to digital. The IF DIGITIZER outputs the digital data to a computer for further processing via a USB cable. No demodulation is done on the IF DIGITIZER board.

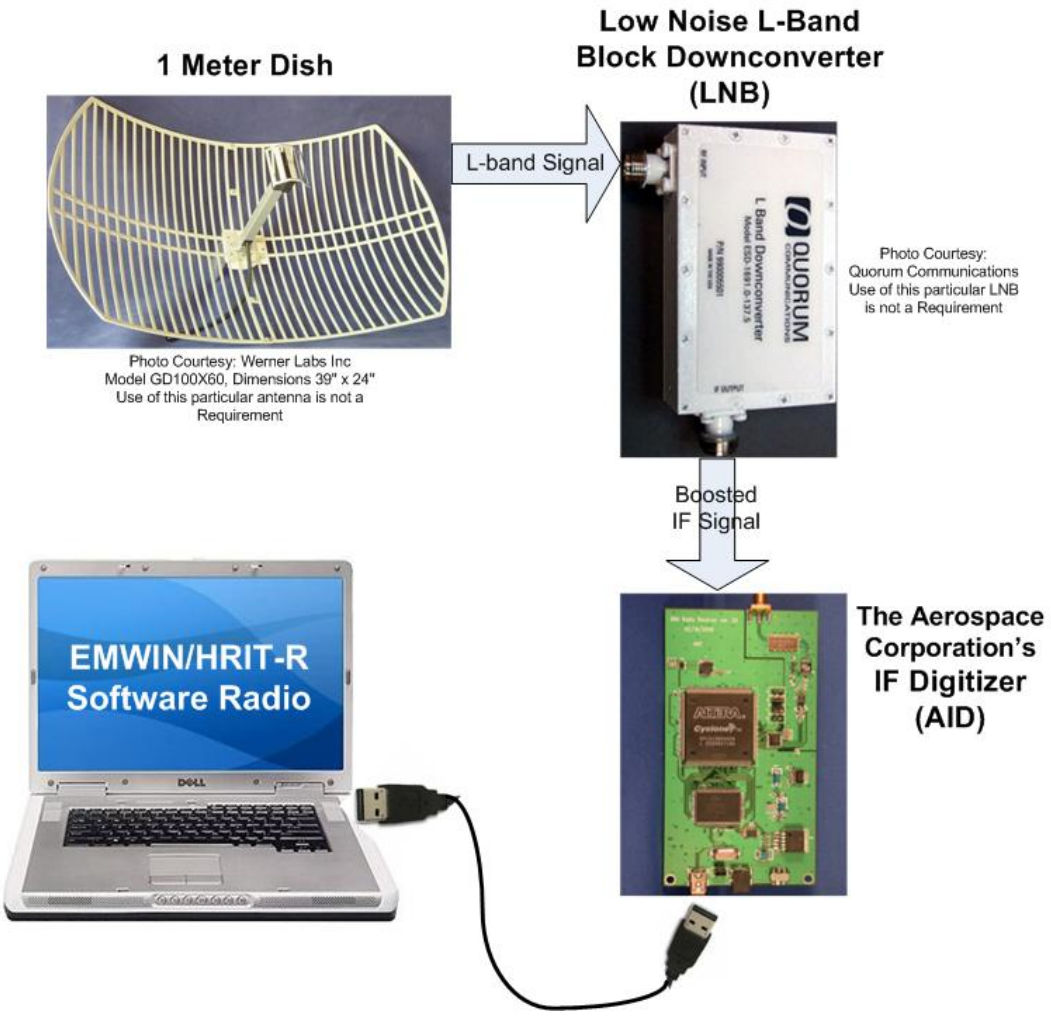

Figure 1: HRIT System Diagram

Below is a block diagram of the IF DIGITIZER board. The analog input comes into the SMA connector. The signal is filtered, and then sent into an Automatic Gain Controller (AGC) to maintain constant levels. Then the analog signal is sampled via an A/D converter. The digital samples are then fed into an FPGA chip. The FPGA chip downconverts the signal from IF (Intermediate Frequency of 140 MHz) to baseband (0 Hz) using the digital multiplier. After that, the FPGA decimates the signal by M (throws away samples and low pass filters it), and sends the samples out to a USB port for further processing. All of the chips are commercially available.

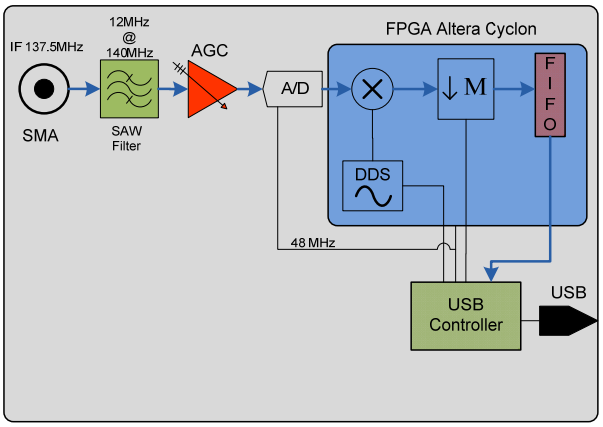

Figure 2: IF Digitizer Block Diagram

In addition to the IF DIGITIZER board, we also delivered a board that converts a signal directly from RF (1.69 MHZ) to baseband, and converts from analog to digital. This allows users to bypass the second component shown in figure 1. This board was called the RF Digitizer. It is shown below.

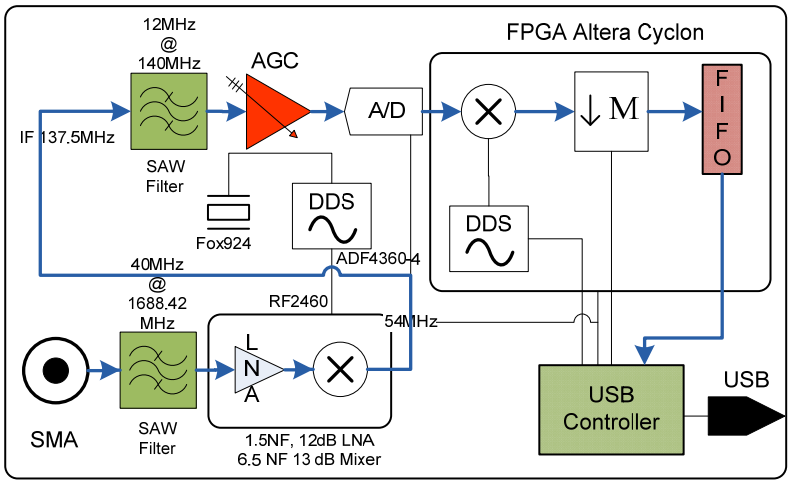

Figure 3: RF Digitizer Block Diagram

This board is very similar to the IF DIGITIZER. The only difference is that it has a few extra components that move it from RF to IF, before going from IF to baseband. The first step is the SMA analog input, shown on the bottom left hand corner. After that it is filtered and amplified by a Low Noise Amplifier (LNA). After that, it goes through a mixer (multiplier and filter) which downconverts it from RF to IF. The mixer is driven by a Digital Frequency Synthesis unit (DDS), which produces an oscillator at a user specified frequency. This allows the user to downconvert from an RF frequency of 1.69 GHz, to a multitude of frequencies in the 100 MHz range. After going from RF to IF, the remainder of the board is equivalent to the IF DIGITIZER.

Schematic Description

One schematic has been attached for both the RF Digitizer and the IF DIGITIZER. The schematic is seven pages long. It is partitioned to make it more readable. Most of the chips used on the board have signal pins, power pins, and clock pins. As such, one page of the schematic is dedicated to signal lines, one for power, one for clocking, etc. At the bottom right hand corner of each page there is a title. The page titles are as follows

1. GNU Signal Buses
2. Front Power (RF Digitizer only)
3. GNU Power
4. GNU Clocking
5. Front LNA and Mixer (RF Digitizer only)
6. Front DFS and LO (RF Digitizer only)
7. GNU display

Because the IF DIGITIZER is a subset of the RF Digitizer, one schematic can be used to describe both devices. Sheet 2, 5, 6 are unique to the RF Digitizer. If these sheets are removed, the schematic becomes the IF DIGITIZER schematic.

Below is a table that relates the major devices referred to in figures 2 and 3, to the part numbers as shown throughout the schematic.

Table 1: Part Names and Their Respective Schematic Part Numbers

Part Number	Device Name
MA05267	Saw Filter
ADB367	AGC
LTC2226	A/D Converter
EP1C12-PQ240	FGPA
CY7C68013-TQ100	USB controller
RF3866	LNA
RF2460	Mixer
ADF4360-1	DDS
24C01	24 MHz Clock
FOX924B	Local Oscillator

Page 1 of the schematic represents the signal path as shown by the blue lines in figures 2 and 3. The signal goes through the SAW filter (MAO5267), and then the AGC (ADB367), and then the A/D converter (LTC2226). At the bottom of page 1, the FPGA is shown twice. On the left, the signal lines between the FPGA and USB controller are shown. On the right, the signal lines between the FPGA and the A/D converter are shown.
Page 2 just shows the power circuits. On the left, is the power connection to the LNA (RF3866 as shown on page 5), and on the right, is the power connection to the Mixer (RF2460 as shown on page 5).
Page 3 shows the GNU power (which refers to the power that is sent to all the components of the IF DIGITIZER board). Power goes to the FGPA, the USB controller, AGC, and the A/D.

Page 4 shows how the clock is routed to the FPGA and the USB controller. An external clock can be fed into the system via an SMA, which gets routed through a buffer circuit (CD5V304). This circuit is shown towards the bottom and horizontally near the middle. The clock is initially fed to the USB controller by a 24 MHZ crystal (24C01). This is shown on the far left, second from the top.
Page 5 covers the signal path for the Mixer and LNA as shown by the blue lines at the bottom of figure 3. The first two chips shown are the two LNAs (RF3866). The last chip is the mixer chip (RF2460). The signal, clock, and power connections for the Mixer and DDS are shown in page 6. Finally page 7 shows a simple network to control LED indicator lights on the board.