Microfluidic Test Station

Front-end sample preparation is an often-neglected aspect in the implementation of chemical- and biological-warfare-detection instrumentation. Over the past ten years LLNL has created many microfluidic-based modules to aid in the separation, concentration, purification and/or fractionation of "trace" analytes from a complex noisy-background matrix. These modules have their own application space, yet all improve the overall system performance by starting the assay with a more concentrated and purified sample. For all the microfluidic technologies involved in the suite of front-end sample preparation projects, there is one common aspect: the need for an experimental data acquisition system.

This project aims to integrate existing experimental capabilities into one common platform to aid in the construction and the testing capabilities of microfluidic-based modules when applied to chemical- and biological-detection instrumentation.

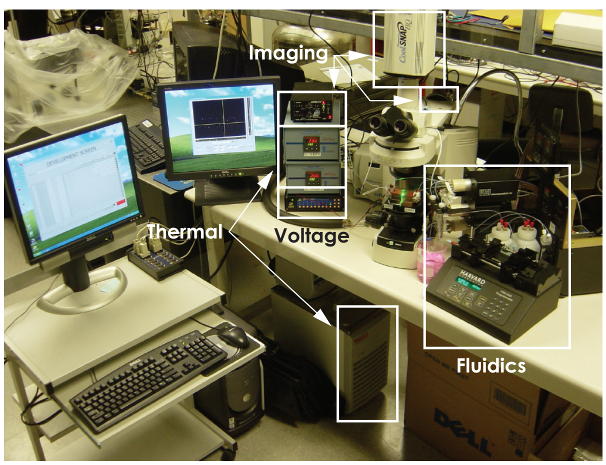

Figure 1. Adaptable, automated microfluidic test station.

Project Goals

The goal of this project is to deliver an automated microfluidic-based test station to control and sense temperatures, voltages, pressures, and fluid-flow rates while performing quantitative fluorescent image acquisition. This platform needs to manage all the necessary output data

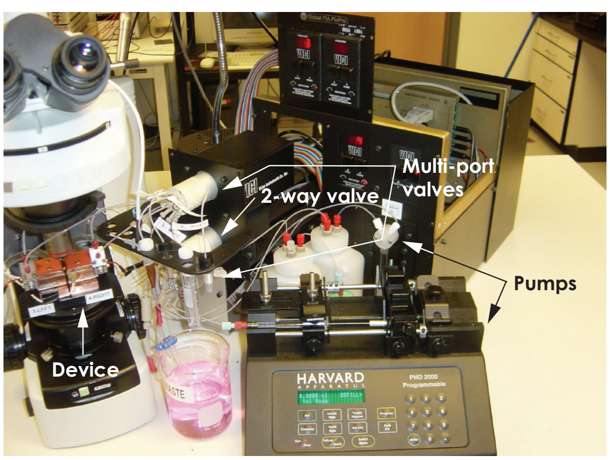

Figure 2. Fluidic control scheme.

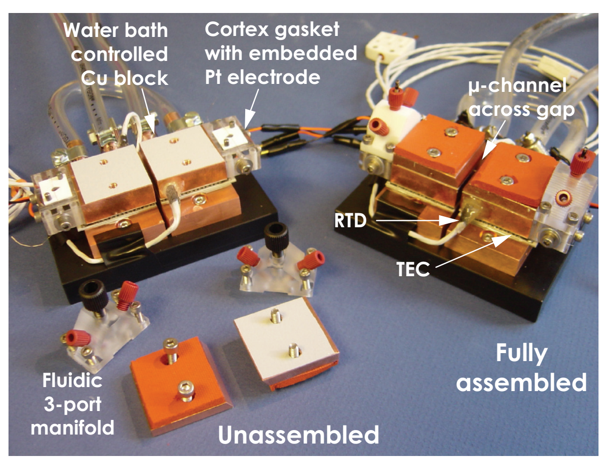

Figure 3. General package for loading microcapillaries.

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with minimal user interaction for possible future integration into a deployable system. In addition, this project includes a standardized package for both high-aspect-ratio microcapillaries and microfluidic chips. The package must allow for ease of integration with future microfluidic projects and must have the ability to control temperatures, voltages, and fluid-flow rates in each of the microchannel geometries. Thus, a complete microfluidic workstation, minus the actual microfluidic module, is the delivered product.

Relevance to LLNL Mission

This microfluidic test station (software and hardware) will reduce the typical prototype implementation cycle by reducing and improving the experimental testing/validation phase for front-end sample preparation devices. A significant benefit will be the cross-pollination of available testing procedures from the many LLNL projects (standardized through the software).

FY2005 Accomplishments and Results

Two complete systems have been requested and are being built for LLNL programs. Our accomplishments are as follows.

Software. We have produced easy-to-use and adaptable software for large experimental studies, with an automatic data management system.

Hardware. We have achieved integration of and simultaneous synchronized control over multiple pieces of equipment (Figs. 1 and 2) common to the microfluidics community:

1. "n" TEC regulating units;
2. a chilled-water-bath recirculation system;
3. an eight-channel high-voltage power supply;
4. "n" liquid-flow monitors;
5. "n" multi-port valves;
6. "n" two-way switching valves;
7. eight negative/positive pressure lines for pneumatic valves;
8. six different pumps (spanning low- and high-flow rates);
9. an electronic shutter for a light source; and
10. a scientific CCD camera.

Packaging I. We have created a general package for loading microcapillaries with a six-port fluidic manifold containing internally integrated electrodes, two independent temperature control regions, and optical access to fluid (Fig. 3).

Packaging II. We have created a package for loading a standardized microfluidic chip with eight fluid ports, eight electrodes, two heating elements, eight temperature sensors, self-sealing fluidic interconnects, and an overall low-profile (< 5 mm) for optical access (Fig. 4).

Chip Layout. We have prepared guidelines for microfluidic chips with heaters, temperature sensors, and internal electrodes for fabrication from identified external foundries in glass or plastic (Fig. 5).

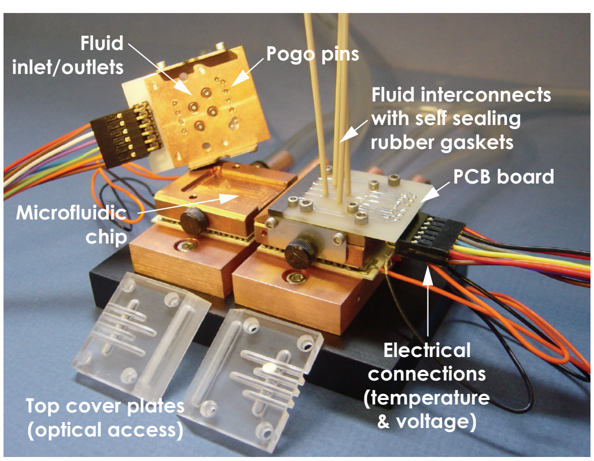

Figure 4. Standard package for a multi-port microfluidic chip.

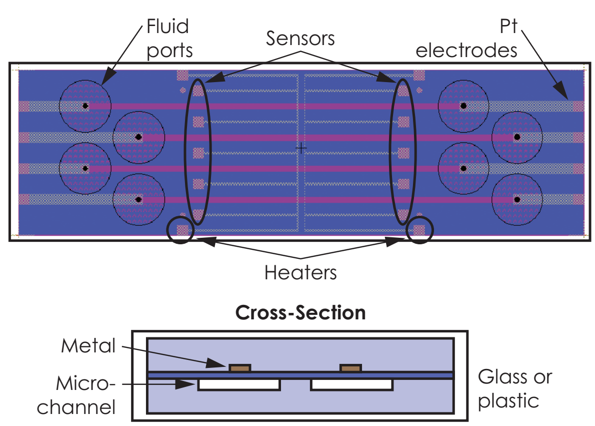

Figure 5. Drawing of a typical mask layout for a microfluidic chip.