Silicon-Deposition Process Implementation

The deposition of silicon layers is one of the key steps in the fabrication of microelectronics, microsensor devices, and micro-electromechanical systems (MEMS). As the technology of microfabrication (and now nanofabrication) advances, silicon continues to be a key material, and more advanced systems for depositing silicon are needed to keep pace. In addition to the needs for ever-increasing layer quality and uniformity, modern equipment must be able to deposit such layers on wafers of ever larger size.

This project involved the installation and testing of a new high performance system for silicon layer deposition, as well as the engineering of the layer deposition process itself in order to tune the system to produce the high-quality films required by current research. The system is a Thermco low-pressure chemical vapor deposition (LPCVD) system. LPCVD is the process used by large-scale, high-reliability production semiconductor fabrication facilities. Based on the thermally-induced decomposition of a reactive silicon-bearing source gas such as silane (SiH4), this process yields very high quality films that are deposited conformally over the substrate wafers with minimal variation in thickness or microstructure.

The process development effort has resulted in process recipes for both undoped (electrically insulating) and phosphorus-doped (electrically conductive) layers. The process characterization involved the measurement and adjustment of such parameters as deposition rate,

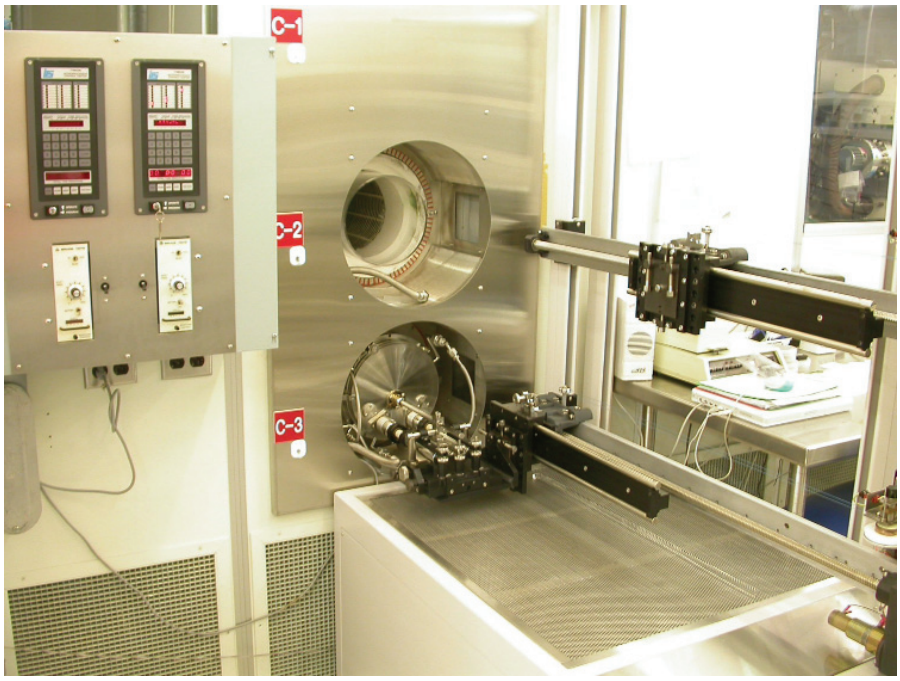

Figure 1. The new Thermco LPCVD silicon-deposition system installed in LLNL's Micro-fabrication Laboratory. The silicon system is located in the lower unit. The upper unit allows for a comparably upgraded silicon-nitride-deposition capability in the future.

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uniformity, film conductivity, and residual stress. Now ready for use, the system allows the deposition of high-quality silicon layers on all types of substrates up to 6 in. in diameter.

Project Goals

The goal of this project was to complete the installation and testing of the new LPCVD silicon-deposition system (Figs. 1 and 2). This includes the implementation and characterization of new process recipes that can be used to deposit the different types of films required for different types of microfabricated devices.

Relevance to LLNL Mission

The availability of a new, state-of-the-art silicon-deposition capability is a boost to the core microfabrication capabilities at LLNL, which serve both internal and external customers.

FY2005 Accomplishments and Results

The installation of the system was completed, including connections to electrical and mechanical utilities in the facility; the modification of gas-handling manifolds and other interface hardware; and the plumbing of specialty gas lines to provide the SiH_4 and phosphine (PH_3) source gases used for silicon deposition. Process recipes were written and tested, and characterization of the resulting films was used to fine-tune the recipes.

Characterization included film thickness and deposition rate, residual film stress, and electrical conductivity. The control of residual stresses in the deposited films is very important for MEMS and other mechanical devices, and the measurement of residual stress also provides information about the microscale structure of the deposited silicon layers. Electrical conductivity is important in the case of doped films, in which atoms from a secondary source (such as PH_3) are incorporated to allow electrons to flow through the silicon. Doped films are required for the fabrication of a great many types of silicon sensors and actuators, as well as microscale heaters and some types of microelectronic devices.

As a result of this project, the Microfabrication Laboratory and its customers now enjoy the capability to deposit both undoped (resistive) and phosphorous-doped (conductive) silicon films for a wide range of applications.

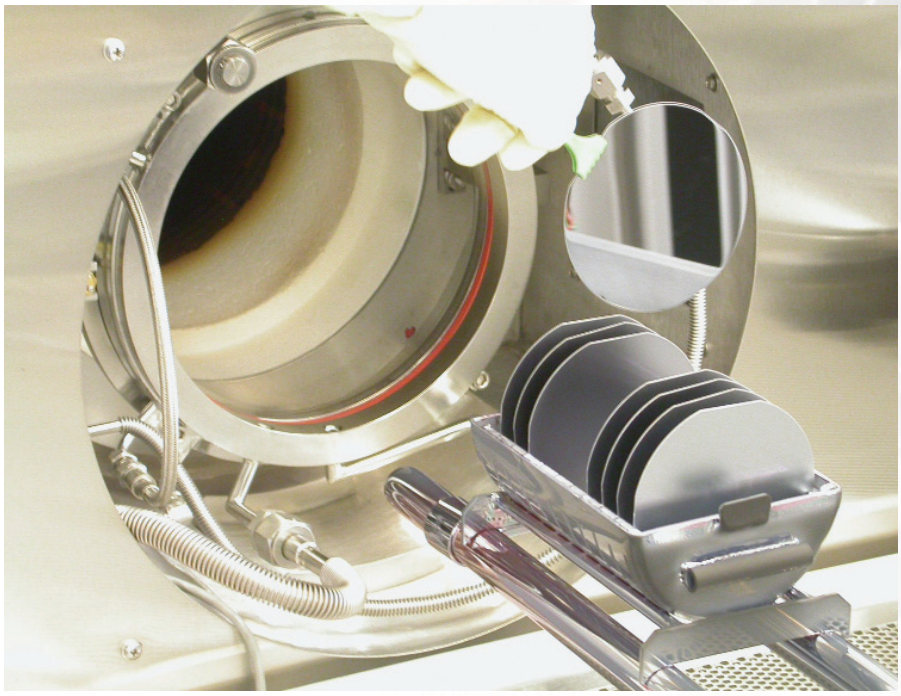

Figure 2. Close-up of the LPCVD silicon-deposition system. This modern system allows us to deposit high-quality doped and undoped silicon films on 4- or 6-in. wafers.