PUBLIC

UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

In the Matter of **RAMBUS INC.,** **a corporation.**	**Docket No. 9302**

RAMBUS INC.'S RESPONSES TO COMPLAINT COUNSEL'S PROPOSED FINDINGS OF FACT

VOLUME III

XI. Had Rambus Timely Disclosed its Intellectual Property Claims, JEDEC Would Have Acted to Avoid Granting Economic Power to Rambus.

2100. Had Rambus disclosed to JEDEC before the SDRAM and DDR SDRAM standards were finalized and the industry became locked in to use of the standards that it had pending patent applications that might relate to programmable CAS latency and burst length, on-chip DLL, and a dual edged clock, JEDEC and JEDEC members would have acted to avoid granting economic power to Rambus. CCFF 2101-2464.

Rambus's Response to Finding No. 2100:

The proposed finding is not supported by the weight of the evidence. Three independent lines of evidence show that JEDEC would have adopted Rambus's technologies had Rambus made the additional disclosures Complaint Counsel allege should have been made. First, the evidence shows that the additional disclosures would not have changed JEDEC's revealed preference for Rambus's technologies; JEDEC elected to adopt those technologies into a new standard even after Rambus's patents issues and it began to seek royalties. (*See* RPF 1532; Section IX.A). Second, there were no cost-performance equivalent noninfringing alternatives; thus, rational JEDEC members would have selected Rambus's technologies accounting for Rambus's royalties. (*See* Rapp, Tr. 9907-09; RPF Section IX.B). Third, an analysis of JEDEC's and Rambus's economic incentives and past behavior shows that JEDEC would have incorporated the Rambus technologies even if Rambus had made the additional disclosures. (*See* RPF Section IX.C). This behavior would be consistent with the recorded behavior of JC 42.3, which routinely standardizes technologies that have patent issues. (*See* RPF 1220-38).

A. Had Rambus Disclosed On a Timely Basis, JEDEC Likely Would Have Adopted Alternative Technologies.

2101. Had Rambus disclosed the scope of its patent applications while JEDEC was still working on the standards, some JEDEC members testified that they would have adopted alternative technologies. (Sussman, Tr. 1416-17 ("If I understood that there was IP on the

programmable [CAS latency and burst length], I would have voted – changed my direction and voted to take the fixed one."); Prince, Tr. 9022-23 (if she had known before 1996 that Rambus might have patents on programmable CAS latency and burst length, it would have affected her decision-making on those two technologies); Lee, Tr. 6635-36 (if Rambus had disclosed to JEDEC before 1996 that it had a pending patent application that it believed contained claims that would cover use of programmable CAS latency and burst length, he would have opposed the use of those technologies in SDRAM and supported the SDRAM lite device that proposed a fixed latency and length); Lee, Tr. 6717 (if Rambus had disclosed to JEDEC before 1996 that it had a pending patent application that it believed contained claims that would cover the use of dual edged clocking, he would have opposed the vote to standardize dual edged clocking in DDR SDRAM); Lee, Tr. 6686 (if Rambus had disclosed to JEDEC before 1996 that it had a pending patent application that it believed contained claims that would cover use of on-chip PLL or DLL, he would have recommended that Micron avoid using that technology); *see also* Kellogg, Tr. 5136, 5146, 5170, 5187 (IBM would consider patent issues seriously and would certainly consider alternatives); CX2107 at 137 (Oh, Dep.) (Hyundai would not have developed DDR SDRAM if it had known that it would have royalties associated with it); (Meyer, Tr. 440-41 (had Rambus disclosed before 1996, Infineon engineers would have come up with specific proposals for him to present to JEDEC as alternatives to technologies that Rambus would be obtaining patents on.)).

Rambus's Response to Finding No. 2101:

The proposed finding is incomplete. Weighing against the after-the-fact testimony of interested witnesses is what JEDEC members did in the real world. First, JEDEC members voted for and adopted Rambus's technologies into SDRAM and DDR despite rampant and widespread concerns that Rambus could and would obtain patents covering those standards. (*See* RPF Section VI). Though JEDEC members were well aware that Rambus could and would seek to obtain patents on technologies incorporated into the SDRAM and DDR standards, they were also convinced that Rambus's patents would not issue or would be invalid because of prior art. (See RPF Section VI; RPF Section IX.A.2.d). For example, Hans Wiggers, the HP JEDEC representative testified:

> Q. . . . If you had heard Richard Crisp say in a JEDEC meeting that he believed that Rambus had invented the use of both edges of the clock to transmit

data in a memory device, what would your reaction have been?

A. I would have said that that was not something that he could have patented because it was a known technology, so I could not see that as a proprietary technique.

(Wiggers, Tr. 10588).

Thus, the evidence shows that JEDEC members did and would have ignored information about Rambus's patents as they related to the SDRAM and DDR standards. (*See also* Lee, Tr. 6981 (testifying that he and others ignored assertion that Rambus would have patents on dual-edge clocking because he "didn't believe it was true")).

Second, JEDEC adopted each of the same four Rambus technologies into the DDR2 standard after examining the alternatives and with full knowledge of Rambus's issued patents and its demands for royalties. (RPF 746-63). The most glaring example of this is Rambus's programmable burst length technology. The preliminary DDR2 specification, which was published in July 2001 (at least one and a half years after Rambus's patents issued and it began to demand royalties), specified a single fixed burst length, thereby avoiding Rambus's patents. (RX 1854 at 20; Macri, Tr. 4733-34). Yet at the September 2001 JC 42.3 meeting, with full knowledge of Rambus's issued patents and its demands for royalties, the committee voted unanimously to amend the preliminary standard to add Rambus's programmable burst length technology. (CX 174 at 7-8). The fact that the preliminary standard avoided the use of programmable burst length demonstrates that JEDEC was not "locked in" to using the Rambus technologies for any economic or technological reason. JEDEC adopted the Rambus technology with full knowledge of Rambus's patents because it was superior to the alternatives. (CX 174 at

37 (citing potential performance "Improvement of 4-10% On High-Bandwidth Applications" as reason to incorporate Rambus's technology)).

Third, JC 42.3 has repeatedly and routinely standardized technologies despite patent issues. The JEDEC minutes shows that from May 1990 through the end of 1995, patented or potentially patented technologies were proposed on at least a dozen occasions and in each and every instance JC 42.3 standardized the technology. (*See* RPF 1224-38). This conclusion is doubly sure if Rambus had given a RAND letter, which it had every incentive to do. (See RPF 1184-1203). The long-time chair of JC 42.3 could not recall a single instance in which JEDEC avoided a patented technology it thought was best after receiving a RAND letter. (Kelley, Tr. 2707-09). And the fact that JEDEC repeatedly selected Rambus's technologies demonstrates beyond dispute that JEDEC believed that they were the best technologies. (*See* RPF 724-31; Kelley, Tr. 2707-09 (Rambus's programmable CAS latency and programmable burst length technologies considered the best alternatives).

1. There Were Multiple Alternatives To Avoid the Technologies In Question.

2102. There are almost always multiple ideas about what features JEDEC should and should not include in a particular device. (Rhoden, Tr. 414-15). "[I]f you give ten engineers a problem, you'll probably get 12 or 14 solutions, and the same is true inside the [JC 42.3] committee. People were proposing a number of other approaches to the same type of thing." (*Id.* 434-35).

Rambus's Response to Finding No. 2102:

The proposed finding is irrelevant. The evidence shows that multiple alternatives to the four features at issue were considered by JEDEC and that these alternatives were rejected; this is not surprising given that the alternatives either would not have worked at all or would have had a

significant impact on performance or cost. (RRFF 2130-2414).

2103. DRAM manufacturers could have developed commercially viable solutions that would have avoided Rambus patents.(CX2109 at 77-78 (Davidow, Dep.) ("I think you could have sat a group of people down in a room and said you can't use this stuff, come up with different solutions and people could have come up with different solutions."); *Id.* at 77 ("[C]ould they have done alternatives, [ ] could [they] have competed within the market effectively by making different cost performance trade-offs, my guess is the answer would be [ ] yes.")).

Rambus's Response to Finding No. 2103:

The proposed finding is not supported by the weight of the evidence. Complaint Counsel rely solely on offhand comments by Mr. Davidow for this finding. Detailed analysis of actual alternatives that have been proposed by JEDEC members and Complaint Counsel's technical expert shows that DRAM manufacturers could not have developed commercially viable solutions that would have avoided Rambus patents. (RRFF 2130-2414).

2104. Before 1996, there were alternatives to programmable CAS latency, programmable burst length, dual edge clocking, and on-chip DLL. (Jacob, Tr. 5365; Wagner, Tr. 3859-60; Kelley, Tr. 2548-49; CX2109 at 67-68 (Davidow, Dep.) (based on internal discussion at Rambus, Mr. Davidow concluded that there were "many ways to improve performance" without infringing Rambus patents); CX2109 at 68-69 (Davidow, Dep.) (Davidow assumes that JEDEC could have pushed work-arounds to dual edged clocking "pretty far"); CX2109 at 70-71 ("[t]here are lots of other solutions" besides programmable cas latency and burst length)).

Rambus's Response to Finding No. 2104:

The proposed finding is not supported by the weight of the evidence. (RRFF 2130-2414).

2105. Before 1996, JEDEC considered alternatives to programmable CAS latency, programmable burst length, dual edged clocking, and on-chip DLL. (CCFF 2131, 2235, 2323-24, 2367).

Rambus's Response to Finding No. 2105:

The proposed finding is incomplete. The alternatives considered by JEDEC to these four features were all rejected.

2106. It would have been relatively easy to implement alternatives to programmable CAS latency, programmable burst length, dual edged clocking, and on-chip DLL in the 1991-1996 time frame. (Polzin, Tr. 3987-89 (Rambus patents on dual edge clocking, programmable CAS latency, and programmable burst length and on-chip DLL were "pretty simple things to work around if we had known about them a long time ago."); Peisl, Tr. 4452 (it would have been "relatively easy" to implement alternatives in the early 1990's)).

Rambus's Response to Finding No. 2106:

The proposed finding is misleading and partially incorrect. It is true that it would have been relatively easy to implement alternatives to programmable CAS latency and programmable burst length in the 1991-96 time frame, and it remained true that alternatives to these features would have been relatively easy to implement after that time (for example in DDR SDRAM or DDR2 SDRAM). (Soderman, Tr. 9417-19; Geilhufe, Tr. 9615). Nevertheless, DRAM manufacturers have not implemented alternatives to these features despite full knowledge of Rambus's patent claims.

The proposed finding regarding the implementation of alternatives to dual edged clocking and on-chip DLL in the 1991-96 time frame makes no sense because dual edged clocking and on-chip DLL were not themselves implemented until after that time. These two features are part of the DDR SDRAM standard which was not approved until 1999. (RPF 400). Formal consideration of the DDR SDRAM standard at JEDEC did not begin until December 1996. (RPF 401-413). In any case, it would have been very difficult to implement alternatives to dual edge clocking at any time, while on-chip DLL or PLL is required for high speed operation. (Soderman, Tr. 9419-21).

2107. JEDEC members viewed the alternatives as viable, and many members preferred one or more of the alternatives to the technologies that were actually selected. (Kellogg, Tr. 5117, 5131-32 (testifying that manufacturers would have likely preferred a fixed burst length and that burst length alternatives were viable); Bechtelsheim, Tr. 5811 (testifying that he would have

preferred the use of pins to set CAS latency); Sussman, Tr. 1380 ("I had a lot of arguing to do to get the degree of programmable features [programmable CAS latency and burst length] into the [JEDEC standard];" Lee, Tr. 6666, 6683 (testifying that a read clock, or an echo clock, was a viable alternative and that Micron preferred to avoid the use of an on-chip DLL); Kellogg, Tr. 5168-69 (testifying that he preferred vernier circuits to on-chip DLL); Polzin, Tr. 3991-92 ("Pin strapping" was a viable design alternative to the current JEDEC standard of setting CAS latency and "[c]ertainly no more costly.")).

Rambus's Response to Finding No. 2107:

The proposed finding is misleading. Of course, for every technology presented at JEDEC, there are some who view them as viable or they would not be presented. For all of the alternatives to Rambus technology, however, that JEDEC considered, a majority of JEDEC members preferred the Rambus technology. Moreover, they had good reason to do so, because there were no viable alternatives. (RRFF 2130-2414).

2. There is No Reliable Evidence to Contradict The Commercial Viability of Alternative Technologies.

2108. Dr. Soderman and Mr. Geilhufe lacked the expertise and experience to conclude what technologies JEDEC members would have considered to be acceptable alternatives to the technologies at issue. (CCFF 2109-2115).

Rambus's Response to Finding No. 2108:

The proposed finding is incorrect. Dr. Soderman and Mr. Geilhufe each has over 30 years experience in the semiconductor industry and each has DRAM circuit design experience. (RPF 787-88). By contrast, Professor Jacob, Complaint Counsel's technical expert, was still earning his first engineering degree in the mid-1990s when SDRAM was being standardized, has never worked in the semiconductor industry, and has no DRAM circuit design experience. (RPF 786; Jacob, Tr. 5354-57, 5588, 11148).

2109. During the relevant time period, neither Dr. Soderman nor Mr. Geilhufe was involved in or supervising the design of DRAMs. (Soderman, Tr. 9342-43; Geilhufe, Tr. 9627-28

("Of course not. I was an executive in the industry. I was no longer designing.")).

Rambus's Response to Finding No. 2109:

The proposed finding is incomplete. In contrast to Complaint Counsel's expert, Professor Jacob, both Dr. Soderman and Mr. Geilhufe were working in the semiconductor industry druing the relevant time period, and, again in contrast to Professor Jacob, both have DRAM circuit design experience. (RRFF 2108).

2110. Much of Dr. Soderman's recent experience has involved the sales of software. Soderman, Tr. 9337-38.) Dr. Soderman's primary experience from 1981 to 1997, at ASIC Design & Marketing, Xilinx, Intel, and LSI Logic, involved programmable logic and gate arrays, not DRAMs. (*Id*. 9338-42.)

Rambus's Response to Finding No. 2110:

The proposed finding is misleading. Dr. Soderman testified that much of his work experience in the semiconductor industry in the 1980s and 1990s involved systems that included DRAMs and he had to be familiar with the DRAMs in order to interface to them. (Soderman, Tr. 9514).

2111. Dr. Soderman hasn't designed a DRAM since the late 1970's. (Soderman, Tr. 9342-43.) The DRAM he designed was used in typewriters. (*Id*. 9343.)

Rambus's Response to Finding No. 2111:

The proposed finding is misleading. The DRAM core has not changed since Dr. Soderman's work with DRAMs in the late 1970s and the interface logic, that has changed, is very similar to the sorts of circuits that Dr. Soderman has been working on in other contexts. (Soderman, Tr. 9513-14). Moreover, much of Dr. Soderman's work in the 1980s and 1990s involved systems that included DRAMs. (RRFF 2110).

2112. The last time Mr. Geilhufe formally contributed to a DRAM design was sometime

in the mid to late 1980s. (Geilhufe, Tr. 9625-26). Mr. Geilhufe's last hands-on DRAM design experience was in 1978. (*Id.* 9626).

Rambus's Response to Finding No. 2112:

The proposed finding is incomplete. Mr. Geilhufe received the initial DRAM patent which was filed in 1968 and has received four other DRAM patents since then. (Geilhufe, Tr. 9553). In the 1980s, as general manager and director of components contracting for Intel, Mr. Geilhufe established, negotiated and managed international manufacturing operations for Intel, primarily relating to EPROMs and DRAMs, with many of the major DRAM manufacturers. (Geilhufe, Tr. 9549-50). In the 1990s, Mr. Geilhufe's work at Information Storage Devices involved becoming familar with DRAM fabrication procedures. (Geilhufe, Tr. 9551).

2113. Neither Dr. Soderman nor Mr. Geilhufe ever designed an SDRAM or DDR SDRAM. (Soderman, Tr. 9342-43; Geilhufe, Tr. 9628). Neither Dr. Soderman nor Mr. Geilhufe ever designed a JEDEC-compliant DRAM. (Soderman, Tr. 9424 ("that particular part was a unique IBM part"); Geilhufe, Tr. 9628).

Rambus's Response to Finding No. 2113:

The proposed finding is incomplete. Professor Jacob has never done the circuit design for an SDRAM, DDR SDRAM or any other kind of DRAM. By contrast to Professor Jacob, both Dr. Soderman and Mr. Geilhufe have DRAM circuit design experience. (RRFF 2108). Moreover, Professor Jacob has never worked in the semiconductor industry. (RRFF 2108). By contrast, Dr. Soderman and Mr. Geilhufe have each worked in the semiconductor industry for over 30 years and much of their work has involved DRAMs. (RRFF 2111-12).

2114. Mr. Geilhufe worked at Winbond from 1999 to 2000. (Geilhufe, Tr. 9628). Winbond did not design any DRAMs. (*Id.* 9628-29). Mr. Geilhufe's manufacturing experience at Winbond was limited to being aware of the volumes and types of DRAMs that were being manufactured and the profitability of the DRAM business. (*Id.* 9629).

Rambus's Response to Finding No. 2114:

Rambus has no specific response.

2115. Neither Dr. Soderman nor Mr. Geilhufe attended JEDEC meetings during the relevant time period. (Soderman, Tr. 9429, 9447-48, 9473 ("[Mr. Macri] was at the [JEDEC] meeting. I was not . . . I have no firsthand knowledge how the JEDEC committee decided to standardize on the [burst length] values.")). Mr. Geilhufe attended only one JEDEC meeting approximately twenty years ago. (Geilhufe, Tr. 9624). The only person he remembers supervising whose job responsibility included attending standard-setting organization meetings, was an employee of Intel who briefly reported to him sometime in 1975. (Geilhufe, Tr. 9625).

Rambus's Response to Finding No. 2115:

The proposed finding is irrelevant. Attendance at JEDEC meetings is irrelevant to the opinions that Dr. Soderman and Mr. Geilhufe offered. There is no evidence that Professor Jacob, Complaint Counsel's technical expert, ever attended a JEDEC meeting.

2116. Dr. Soderman and Mr. Geilhufe failed to consult highly relevant materials relating to JEDEC's consideration of alternative technologies. (CCFF 2117-2221).

Rambus's Response to Finding No. 2116:

Contrary to the proposed finding, Dr. Soderman and Mr. Geilhufe consulted whatever materials were relevant to their opinions.

2117. Dr. Soderman failed to consider a number of critical presentations at JEDEC. (Soderman, Tr. 9493, 9493-94, 9503-04). Dr. Soderman couldn't recall whether he had considered a number of other important presentations at JEDEC. (Soderman, Tr. 9485-86, 9487 ("I've seen a lot of presentations about incorporating Vernier's on these. They are all kind of blending together, all very similar."); 9491, 9502-03).

Rambus's Response to Finding No. 2117:

The proposed finding is irrelevant. Dr. Soderman analyzed and opined on the alternative technologies proposed by Professor Jacob from a technical standpoint; a consideration of JEDEC presentations was not necessary.

2118. Mr. Geilhufe never reviewed any JEDEC meeting minutes or any JEDEC policy manuals. (Geilhufe, Tr. 9622).

Rambus's Response to Finding No. 2118:

The proposed finding is irrelevant. Mr. Geilhufe was not offering an opinion on any topic that would have required a review of JEDEC meeting minutes or policy manuals.

2119. Dr. Soderman failed to review the deposition or trial testimony of virtually all the relevant fact witnesses, including Drs. Oh and Peisl and Messrs. Lee, Shirley, Sussman, Kellogg, Heye, Macri, Goodman, Rhoden, Gross, Becker, and Krashinsky. (Soderman, Tr. 9427-28, 9433, 9435, 9440, 9494, 9499, 9503, 9505-06, 9508). Mr. Geilhufe did not recall reviewing the testimony of any fact witness other than the deposition testimony of Dr. Peisl, who disagreed with his conclusions. (Geilhufe, Tr. 9619, 9729-31).

Rambus's Response to Finding No. 2119:

The proposed finding is irrelevant. Dr. Soderman analyzed and opined on the alternative technologies proposed by Professor Jacob from a technical standpoint. Mr. Geilhufe performed a cost analysis of the type that he has been performing in the industry for decades. (Geilhufe, Tr. 9553-54). Neither of these tasks required reviewing the deposition or trial testimony of the fact witnesses in this case.

2120. Dr. Soderman failed to interview anybody who had attended JEDEC meetings during the relevant time period and who had observed the JEDEC work in progress. (Soderman, Tr. 9447-48, 9472, 9488, 9491, 9503, 9506-07). As a result, he had no understanding of why various alternatives were proposed at JEDEC, how JEDEC members reacted to it, what was said in the discussions of the alternatives, or which companies supported the alternatives. (*Id*. 9447-48).

Rambus's Response to Finding No. 2120:

The proposed finding is irrelevant. Dr. Soderman analyzed and opined on the alternative technologies proposed by Professor Jacob from a technical standpoint. Interviews with JEDEC members or an analysis of JEDEC members' motiviations and reactions was not necessary.

2121. Mr. Geilhufe did not do anything to ensure that the analysis that he did was the type of analysis that was done at JEDEC. (Geilhufe, Tr. 9622). Nor did he speak to any JEDEC member or any JEDEC employee to determine how the questions he was asked to answer are answered at JEDEC. (*Id.* 9623). Mr. Geilhufe did not even know whether the questions he was asked to answer were ever asked at JEDEC. (*Id.* 9622).

Rambus's Response to Finding No. 2121:

The proposed finding is irrelevant. Mr. Geilhufe performed a cost analysis of the type that is done in industry and that he has been performing in the industry for decades. (Geilhufe, Tr. 9553-54). Interviews with JEDEC members were not necessary.

The proposed finding is also misleading because costs were not discussed at JEDEC. The EIA Legal Guides that governed JEDEC meetings expressly forbade such discussions, apparently as a result of anitrust concerns. (CX0204 at 3 ("Discussion at EIA meetings of industry costs is normally not permitted."); *see* Krashinsky, Tr. 2833 ("Q. Mr. Krashinsky, to your knowledge, were there ever discussions at JEDEC meetings of the relative costs of using one feature or another feature in connection with DRAM? A. The cost issue is not raised at JEDEC.")). However, given the undisputed importance of costs to JEDEC members (*see, e.g.*, CCFF 125), cost analyses of the type performed by Mr. Geilhufe must have been done by JEDEC members outside the JEDEC context in connection with any serious consideration of alternative technologies.

Furthermore, regardless of what questions were asked at JEDEC, as Dr. Rapp explained, whether an altenrnative is a close economic substitute does not depend on what was discussed at JEDEC: "the commercial viability and substitution qualities of those alternatives are independent of what got said in JEDEC." (Rapp, Tr. 10111).

2122. The methodology that Mr. Geilhufe used to reach his conclusions about the costs of alternative technologies was unreliable. (CCFF 2123-24).

Rambus's Response to Finding No. 2122:

Contrary to the proposed findings, Mr. Geilhufe's methodology was reliable.

2123. Mr. Geilhufe recognized that his estimates were "rough estimates." (Geilhufe, Tr. 9696). He agreed that the margin of error for each of the cost elements described in his presentation is as high as 25 percent. (*Id.* 9665).

Rambus's Response to Finding No. 2123:

The proposed finding is misleading and incomplete. Mr. Geilhufe recognized that, given the lack of detail in Professor Jacob's proposals, it would be impossible to do very precise cost estimates. (Geilhufe, Tr. 9673). However, Mr. Geilhufe was generally conservative and endeavored to err on the low end for his cost increase estimates. (Geilhufe, Tr. 9746). Moreover, Mr. Geilhufe followed the same methodology as he used to make decisions in industry. (Geilhufe, Tr. 9553-54).

2124. Mr. Geilhufe did not compare his projections in this case with any actual data. (Geilhufe, Tr. 9665-66). Mr. Geilhufe reviewed no evidence in this case relating to the costs of DRAM manufacturers for the product design, good die yield, final test and good unit yield cost elements from the relevant period other than the Peisl deposition and, in the case of good unit yield, "confidential" evidence that is not in the record. (Geilhufe, Tr. 9680, 9698, 9706).

Rambus's Response to Finding No. 2124:

The proposed finding is incomplete and misleading. Professor Jacob's proposed alternatives have not been implemented so "actual data" regarding the cost of the alternatives is nonexistent.

2125. Dr. Soderman's conclusions regarding the coverage of certain of Rambus's patents is inherently unreliable. (CCFF 2126-29).

Rambus's Response to Finding No. 2125:

The proposed finding is incorrect. Dr. Soderman testified to his understanding of the coverage of certain Rambus patents as a person of skill in the art. This is precisely how patent claims are to be analyzed. (Fliesler, Tr. 8778).

2126. Dr. Soderman failed to consider technical dictionaries, treatises, or learned texts to determine the common usage of the terms in the claims. (Soderman, Tr. 9478). Dr. Soderman failed to consider the expert reports filed by Rambus's patent experts in the private patent litigation to determine whether his interpretation of terms was consistent with those of Rambus's patent experts. (*Id*. 9478-79).

Rambus's Response to Finding No. 2126:

The proposed finding is irrelevant. Dr. Soderman testified to his understanding of the claim terms as a person of skill in the art – he did not need to consult any extrinsic sources in order to do so.

2127. Dr. Soderman failed to present a claims chart or any other analysis demonstrating that each of the elements of the claim is satisfied. (Soderman, Tr. 9371-73, 9373-74 (In analyzing whether claim 1 of the '120 patent covers use of transmitting burst length information as part of the read command, Dr. Soderman's entire analysis of the various terms used in and elements of that claim consists of: "Claim 1 covers this. It just says, 'receiving block size information'.")).

Rambus's Response to Finding No. 2127:

The proposed finding is irrelevant. Dr. Soderman testified to his understanding of the key claim terms.

2128. Among the terms in claim 1 that Dr. Soderman failed to analyze was the term "operation code." On cross-examination, Dr. Soderman admitted that he had previously interpreted that term as part of a request packet. (Dr. Soderman, Tr. 9456 ("Operation code . . . something that happens, okay. In this case you were requesting the information that has the protocol packet transmit to the DRAM."); *id*. 9457 ("Operation code . . . just means some sort of operation to me, and the information here was well defined as transmitting information to this packet to the DRAM.")). Unlike RDRAMs, JEDEC-compliant SDRAMs and DDR SDRAMs do not use packets. (CCFF 1268, 1272, 1306, 1357).

Rambus's Response to Finding No. 2128:

The proposed finding is incorrect. The cited testimony from Dr. Soderman simply refers to the description of the preferred embodiment in the specification of the '120 patent where "operation code" is used in the context of a request packet. (Soderman, Tr. 9456-57). Dr. Soderman did not testify that claim 1 of the '120 patent was restricted to a packetized system. To the contrary, claim 1 itself defines "operation code" as simply a code that "instructs the memory device to perform a read operation." (RPF 938).

In any event, the proposed finding is irrelevant. If Complaint Counsel were correct and claim 1 of the '120 patent were restricted to packetized systems, then claim 1 would, for that reason, cover neither SDRAMs nor the proposed alternatives at issue. But Rambus has asserted the '120 patent against SDRAMs. (Parties' First Set of Stipulations, Exh. A). Complaint Counsel has introduced the proposed alternatives in order to argue that, if Rambus had disclosed its pending patent applications, then JEDEC had alternatives that it could have chosen to avoid potential Rambus claims. (CCFF 2100). If an alternative does not differ from SDRAM in any material way so far as infringement is concerned (i.e. either both SDRAM and the alternative infringe Rambus's patents or neither do), then there is no reason to think that the alternative would have avoided Rambus's patent claims either.

Moreover, other Rambus patents that do not refer to an "operation code," such as U.S. Patent No. 6,034,918, would cover this alternative. (*See* CCFF 1667-68; CX1525 at 29-30).

2129. Dr. Soderman testified previously that other individuals, including patent attorneys or legal opinion, could answer better than he could whether the claims would be infringed only if, in the alternative in question, values representing both the number of clock cycles and block size were received. (Soderman, Tr. 9457-58; *see also id*. 9479 (his conclusion could be subject to a more legal interpretation that he was not prepared to do).

Rambus's Response to Finding No. 2129:

The proposed finding is incorrect. Dr. Soderman testified to his understanding of the coverage of certain Rambus patents as a person of skill in the art. This is precisely how patent claims are to be analyzed. (Fliesler, Tr. 8778).

3. Alternatives to Programmable CAS Latency.

2130. In the 1991-1996 time frame, there were at least six alternatives to the use of programmable CAS latency in JEDEC SDRAM and DDR SDRAM. (Jacob, Tr. 5370-71). JEDEC could have used fixed CAS latency parts. (Jacob, Tr. 5370). Second, it could have had OEMs blow fuses to determine the CAS latency of a part. (Jacob, Tr. 5378-79). Third, it could have chosen to scale CAS latency to clock frequency. (*Id.* 5370). Fourth, it could have chosen to use either an existing or dedicated pin(s) to set CAS latency. (Jacob, Tr. 5385-86). Fifth, JEDEC could have chosen to encode the CAS latency in either the read or write command. (Jacob, Tr. 5389-90). Sixth, it could have stayed with an asychronous style DRAM. (Jacob, Tr. 5370-71).

Rambus's Response to Finding No. 2130:

The proposed finding is not supported by the weight of the evidence. None of the proposed alternatives to programmable latency were viable alternatives to Rambus's technology. (RRFF 2133-2233).

2131. Three of these alternatives – fixed CAS latency, use of fuses to set CAS latency, and use of pins to set CAS latency – were proposed for incorporation in the JEDEC SDRAM standard in the 1991-1992 time period. (JX0010 at 71, 74; CX0034 at 149; Rhoden, Tr. 425-434; Kellogg, Tr. 5136; Williams, Tr. 798; Kelley, Tr. 2548-49).

Rambus's Response to Finding No. 2131:

The proposed finding is incomplete. These three alternatives were all rejected in favor of programmable CAS latency.

2132. In the 1991-1992 time period, the manufacturing costs associated with three of these alternatives – fixed CAS latency, use of fuses, or use of a dedicated pin(s) – compared to programmable CAS latency using a mode register were relatively similar. (*See generally* CCFF 2133-2177, 2184-2218; Kellogg, Tr. 5143 ("Q. Was there also some difference in cost among

the three options? A. This is a fine-grained question in that if "cost" is my ability to react, yes. If "cost" is strictly manufacturing, the difference between these is so -- it's slightly different. It's very difficult to assess, and I don't recall that we actually assigned a cost differential between these. I do believe it's somewhat fine-grained. In other words, it's not a large number.")).

Rambus's Response to Finding No. 2132:

The proposed finding is not supported by the weight of the evidence. (RRFF 2133-77, 2184-2218).

(A) Fixed CAS Latency.

2133. Fixed CAS latency means that a manufacturer would sell DRAM parts that could operate with only one CAS latency. (Jacob, Tr. 5371). A manufacturer could fix the CAS latency of a part at either the design phase, processing phase, or packaging phase. (Jacob, Tr. 5371).

Rambus's Response to Finding No. 2133:

Rambus has no specific response.

2134. At the design phase, a manufacturer could design a part to only perform with one CAS latency. (Jacob, Tr. 5373).

Rambus's Response to Finding No. 2134:

Rambus has no specific response.

2135. A manufacturer could use a metal mask option to fix CAS latency during the processing phase. (Jacob, Tr. 5373-74). To use a metal mask option to fix CAS latency, a manufacturer could hardwire the chip to operate with either a CAS latency of 2 or 3. (*Id.*). During the processing phase, the metal mask would create a connection with either the CAS latency of 2 circuitry or the CAS latency of 3 circuitry. (*Id.*). That connection would determine that CAS latency of the part. (*Id.*).

Rambus's Response to Finding No. 2135:

Rambus has no specific response.

2136. A manufacturer could use a bond wire option to fix CAS latency during the packaging phase. (Jacob, Tr. 5375). To fix CAS latency during the packaging phase, the manufacturer could design a chip containing both CAS latency 2 circuitry and CAS latency 3

circuitry. (*Id.*). A multiplexor, or a mux, could be attached to both the CAS latency of 2 circuitry and the CAS latency of 3 circuitry. (*Id.*). The CAS latency of the part would depend on whether, during the packaging phase, a bond wire connected the mux to a power pin or a ground pin. (*Id.*).

Rambus's Response to Finding No. 2136:

Rambus has no specific response.

2137. In comparison to the use of a mode register to program CAS latency, there are technical and cost advantages to fixed CAS latency. (Jacob, Tr. 5376). It is potentially a cheaper design because it eliminates the mode register. (*Id.*). The die size of a part refers to the geographic area that a chip occupies on a semiconductor wafer. (Jacob, Tr. 5377). The cost of a part depends substantially on its die size. (*Id.*). Before 1996, fixed CAS latency was potentially cheaper than using a mode register to program CAS latency because it would require a smaller die size. (Jacob, Tr. 5377). It is potentially cheaper to test fixed CAS latency parts because it is no longer necessary to test each part for operation with multiple CAS latencies. (*Id.*).

Rambus's Response to Finding No. 2137:

The proposed finding is not supported by the evidence. While Professor Jacob testified that a fixed latency device could lead to cost savings in certain areas, Complaint Counsel introduced no evidence as to the amount of these purported cost savings, and unrebutted evidence introduced by Rambus shows that any cost savings would be substantially outweighed by other cost increases.

Professor Jacob testified that the design was potentially cheaper because of the elimination of the mode register. First, Professor Jacob is simply mistaken: removing programmable CAS latency would not lead to elimination of the mode register because, as Professor Jacob conceded, it is used for purposes other than setting CAS latency. (Jacob, Tr. 5594; RPF 834). Second, Professor Jacob failed to take into account the fact that multiple fixed latency parts would have to be designed, leading to higher design costs over all. (RPF 827).

Professor Jacob also testified that there would be cost savings because elimination of the

mode register would lead to a smaller die size. As noted above, the mode register could not be eliminated since it is used for purposes other than programming CAS latency. While the three bits of the mode register used for storing a CAS latency value could be removed, the savings from eliminating those three bits would result in the removal of 40 or so transistors from a chip containing some 10 million transistors. (Geilhufe, Tr. 9737). The resulting cost savings would be negligible. (*Id.*)

It is true that there would be some cost savings due to simplified testing; Mr. Geilhufe expressly took this into account when he calculated a net cost increase of 6 cents per unit for the fixed CAS latency alternative. (RPF 835-37).

2138. In 1991-1992, JEDEC considered using fixed CAS latency. Samsung presented an SDRAM proposal that included a fixed CAS latency of 2. (JX0010 at 71; Rhoden, Tr. 425-27; Kellogg, Tr. 5099-5101).

Rambus's Response to Finding No. 2138:

The proposed finding is incomplete. The Samsung presentation was a first showing (JX0010 at 5), and there is no evidence that it ever progressed beyond the first showing stage.

2139. In 1995-1996, JEDEC considered an SDRAM lite part. (JX0027 at 64-68). The use of a single fixed CAS latency was among the features proposed for SDRAM lite. (Lee, Tr. 6626). The use of fixed CAS latency was proposed to reduce cost. (JX0027 at 65 (NEC's SDRAM lite presentation stated that it would "Save money (for everyone)."); Lee, Tr. 6633 ("It was simpler for us. It was -- it would be faster for design. We felt it would be cheaper to produce and cheaper to test. Our feedback from the test group and design was they much preferred the "lite" device over a full-feature device.")).

Rambus's Response to Finding No. 2139:

The proposed finding is misleading and incomplete. The SDRAM lite proposal was for a *single* fixed CAS latency part. (Lee, Tr. 6626). The cost increases identified by Mr. Geilhufe

result from having multiple fixed CAS latency parts (RPF 823, 827-29, 838); thus, there is no dispute that a single fixed latency part could be cheaper than a programmable latency part. However, a single fixed latency part is not acceptable from a user standpoint, as evidenced by the number of different CAS latencies in use and projected to be used in the future. (RPF 813-821). Indeed, the SDRAM lite proposal is itself evidence that a single fixed CAS latency part was unacceptable because the proposal was rejected. (Sussman, Tr. 1416-17).

2140. Dr. Soderman's testimony that fixed CAS latency would interfere with a manufacturer's ability to speed grade parts and thus would impact a manufacturer's yield is contradicted by the weight of the evidence. (Soderman, Tr. 9347-48; CCFF 2141-2148). Likewise, Mr. Geilhufe's testimony that fixed CAS latency would result in reduced yield due to speed distribution is contracted by the weight of the evidence. (Geilhufe, Tr. 9577; CCFF 2141-2148).

Rambus's Response to Finding No. 2140:

The proposed finding is incorrect. Dr. Soderman's and Mr Geilhufe's testimony is supported by the weight of the evidence as set forth below. (RRFF 2141-48).

2141. Manufacturers supported fixed CAS latency. (CCFF 2142-2144, 2146).

Rambus's Response to Finding No. 2141:

The proposed finding is incomplete and misleading. The evidence shows only that, at one point in 1995, a handful of JEDEC members supported fixed CAS latency in the SDRAM lite proposal. (CCFF 2142-44, 2146). The SDRAM lite proposal was rejected. (Sussman, Tr. 1416-17). The subsequent DDR SDRAM and DDR2 SDRAM standards both include programmable CAS latency, and the DDR2 SDRAM standard substantially expands the number of latency options. (RPF 816, 819).

2142. In September 1995, NEC made a proposal for an SDRAM lite part in which it proposed a part with a fixed CAS latency of 3. (JX0027 at 65; Lee, Tr. 6626, 6629). NEC's

presentation on SDRAM lite stated that it would "save money (for everyone)." (JX0027 at 65). It also proposed to mark parts based on frequency rather than cycle time. (*Id.*).

Rambus's Response to Finding No. 2142:

The proposed finding is misleading and incomplete. As discussed above, a single fixed CAS latency part could be cheaper than a more flexible programmable CAS latency part, but the former would be unacceptable from a user standpoint. (RRFF 2139.) The SDRAM Lite proposal for a single fixed latency part was rejected. (Sussman, Tr. 1416-17).

2143. In the 1995-1996 time frame, there was substantial support for one fixed CAS latency of 3. (JX0029 at 13-14; Lee, Tr. 6627-31 (discussing SDRAM lite survey ballot results). There was unanimous support that no values other than CAS latencies of 2 and 3 were needed. (*Id.*).

Rambus's Response to Finding No. 2143:

The proposed finding is misleading. More JEDEC members voted against a single fixed latency than for it. (JX0029 at 13). The proposed finding that "[t]here was unanimous support that no values other than CAS latencies of 2 and 3 were needed," is not supported by the evidence. The survey ballot cited only asked about those two CAS latency values, making it unclear whether any JEDEC members would have wanted other latency values, or the potential for other latency values, included. (*Id.*) The evidence shows that, in fact, other CAS latency values other than 2 and 3 are in use, with more planned for the future. (RPF 813-21).

2144. Mr. Lee testified that Micron supported SDRAM lite and, in January 1996, fixed CAS latency was acceptable from a technical and cost perspective. (Lee, Tr. 6633). Design and test groups at Micron, at the time, preferred SDRAM lite. (*Id.* ("Our feedback from the test group and design was they much preferred the "lite" device over a full-feature device."). Fixed CAS latency "would be faster to design and it would be cheaper to produce and test." (*Id.* 6626). As Mr. Lee explained, Micron preferred fixed CAS latency at the time because it would have enabled Micron to avoid designing in different modes of operation and considering combinations of CAS latency and burst length. (*Id.*).

Rambus's Response to Finding No. 2144:

The proposed finding is irrelevant. Clearly a single fixed CAS latency part was technically feasible and would not suffer from manufacturing cost disadvantages since it would be simpler than a programmable CAS latency part; it would, however, be unacceptable from a user standpoint. (RRFF 2139). If the additional performance and flexibility offered by a programmable CAS latency part were not important, there would be no reason to include it in SDRAMs, DDR SDRAMs, and DDR2 SDRAMs.

2145. Mr. Kellogg testified that there would be a measurable performance advantage to fixed CAS latency "if 'fixed' implied no circuitry in the access path." (Kellogg, Tr. 5138 ("I would just point out that fixed CAS latency would result in measurably improved performance if "fixed" implied no circuitry in the access path.").

Rambus's Response to Finding No. 2145:

The proposed finding is incomplete. Mr. Kellogg also testified that fixed CAS latency parts did not offer the flexibility that was required. (Kellogg, Tr. 5139 ("[W]e weren't convinced that we knew the right latency and we did expect that the DRAM frequency would go up over time -- that we knew the correct latency if we were to select one and we expected that the DRAM frequency could increase over time, which meant we might wish to change the CAS latency.")).

2146. Micron was in favor of using a fixed CAS latency for Burst EDO. At the January 1995 JC 42.3 meeting, Micron made a presentation on a Burst EDO that would use a fixed CAS latency. (Williams, Tr. 823, 825; JX0023 at 68).

Rambus's Response to Finding No. 2146:

The proposed finding is irrelevant and misleading. As an initial matter, it makes no sense to refer to "fixed CAS latency for Burst EDO." "CAS latency" in SDRAMs refers to the number of clock cycles that transpire between a read request and the output of data. (Rhoden, Tr. 382).

Since Burst EDO is asynchronous (CCFF 568), its read operations are not driven by a clock (CCFF 500). In any case, Burst EDO failed in the marketplace in competition with SDRAM with programmable CAS latency. (Williams, Tr. 829; CX2108, Oh Depo., at 236).

2147. Mr. Lee, an experienced engineer for Micron, testified that using a fixed CAS latency would not impact a manufacturer's ability to speed grade parts. (Lee, Tr. 11012). At the wafer probe stage, a manufacturer would test the part to determine what the highest operating frequency was for the part to operate with a particular fixed CAS latency. (*Id.* ("Q. Now, with respect to the SDRAM-Lite proposal, did you have any concern that if JEDEC adopted that proposal, Micron would not be able to speed grade parts? A . No. Q. Can you please explain why not? A. Sure. We would speed grade our parts, we would be able to test that at probe would be the typical way we would do it, at that time, so we would have the same ability to do that whether it was a fixed latency or multiple latencies."); *see also* Becker, Tr. 1140-42 (discussing CX2466, which is an Infineon parts catalogue, and testifying that manufacturers speed grade their products by operating frequency)).

Rambus's Response to Finding No. 2147:

Mr. Lee's testimony regarding speed grading is not supported by the weight of evidence. The testimony that speed testing at the wafer probe stage is not as reliable as speed testing after packaging has not been contradicted by Mr. Lee or any other witness. (RPF 823). Thus, if CAS latency were not programmable, it would have to be fixed prior to the time that the speed could be reliably tested. (*Id.*) This means that some parts would not be capable of operating at the CAS latency to which they have been set, while other parts would have been capable of higher performance than the CAS latency to which they were set. (RPF 823-24).

2148. Mr. Lee testified further that Micron believed that the yield for SDRAM lite "would be the same or better than the full-feature [SDRAM] part." (Lee, Tr. 11013).

Rambus's Response to Finding No. 2148:

The proposed finding is irrelevant. As discussed above, the SDRAM Lite proposal was for a single fixed CAS latency part. (RRFF 2139). There is no dispute that there would be no

yield problems in the case of a single fixed CAS latency part with the CAS latency set a high (i.e. low performance) value. (Geilhufe, Tr. 9701). Such a part would not, however, be acceptable from a user standpoint. (RRFF 2139).

2149. Both Dr. Soderman and Mr. Geilhufe testified that fixed CAS latency would require multiple parts. (Soderman, Tr. 9346-47; Geilhufe, Tr. 9578). Mr. Geilhufe's cost model assumed that fix CAS latency would require three parts. (Geilhufe, Tr. 9578). Their testimony is contradicted by the weight of the evidence. CCFF 2150-2153.

Rambus's Response to Finding No. 2149:

The proposed finding is incorrect. The weight of the evidence supports the fact that, if fixed CAS latency were chosen as an alternative to programmable CAS latency, multiple CAS latency parts would be required. First, even the findings cited by Complaint Counsel indicate that at least two CAS latency values would be required. (CCFF 2150-53). Moreover, more than two values have been in use in the past, more than two values are in use today, and many more latency options will be available in the future. (RPF 813-21).

2150. Although other values have existed, the typical CAS latencies for SDRAM are 2 and 3. (Rhoden, Tr. 394).

Rambus's Response to Finding No. 2150:

The proposed finding is incomplete and misleading. Not only have other CAS latency values been used, but values of CAS latency other than two or three are in use today. (RRFF 2151). Moreover, as Mr. Rhoden himself projected, other values will be used in the future. (RPF 818-19). Indeed, the "Future SDRAM Features" survey ballot that was disributed in October 1995 noted that "[i]n order to allow clock frequencies in excess of ~150 MHz, higher CAS latencies may be required. There are currently 4 reserved states in the mode register's CAS latency field that could logically accommodate CAS latencies of 5, 6, 7 and 8." (CX0260 at 9).

Fourteen of the respondents believed that "it is important to standardize CAS latencies beyond a CAS latency of 4, while only two disagreed. (JX0028 at 42).

2151. For SDRAM, customers primarily use CAS latencies of 2 and 3. (Lee, Tr. 11004-05). No one has used CAS latency of 1 for SDRAM. (*Id.* 11005). Further, no one has used CAS latency of 4 for main memory. (*Id.*).

Rambus's Response to Finding No. 2151:

The proposed finding is incorrect. Complaint Counsel's bases the proposition that "[n]o one has used CAS latency of 1 for SDRAM" on the testimony of Mr. Lee of Micron who testified based on "my knowledge." (Lee, Tr. 11005). Mr. Lee's "knowledge," even as to Micron parts was proven incorrect on cross-examination when Mr. Lee, faced with a Micron data sheet, admitted that Micron makes an SDRAM which uses CAS latency one (in addition to CAS latencies two and three). (Lee, Tr. 11064).

The proposed finding that "no one has used CAS latency of 4 for main memory" is, once again, based solely on Mr. Lee's "knowledge." (Lee, Tr. 11005). Mr. Lee admitted on cross-examination that one of Micron's first SDRAM data sheets included CAS latencies of 1, 2, 3 and 4. (Lee, Tr. 11063). DDR2 parts will also use CAS latency of 4, in addition to other values. (RPF 819).

2152. In the 1995-1996 time frame, JEDEC considered adopting an SDRAM lite part. (Lee, Tr. 11007). "The goal of the SDRAM-Lite was to try to end up with one CAS latency and one burst length." (*Id.*). Settling on one CAS latency and burst length would have resulted in a simpler part that was cheaper to produce. (*Id.* 11008). There was a unanimous position that no value other than CAS latencies of 2 and 3 were needed. (JX0029 at 13-14).

Rambus's Response to Finding No. 2152:

The proposed finding is misleading and incomplete. (*See* RRFF 2139, 2143).

2153. When JEDEC published Release 9 of Standard 21-C, it had removed CAS latency

of 1 from the SDRAM standard because no one was using that CAS latency. (Lee, Tr. 11006-07 ("CAS latency one was being not used, none of the customers were using it as such, so they removed it from the standard."); *Cf.* JX0056 at 114 (Release 4 showing a required CAS latency of 1) with CX0234 at 150 (Release 9 showing that CAS latency of 1 is no longer either a required or optional feature)).

Rambus's Response to Finding No. 2153:

The proposed finding is incomplete and misleading. Complaint Counsel cite Mr. Lee of Micron for the proposition that CAS latency of 1 is not being used, but, in fact, Mr. Lee admitted under cross-examination that Micron currently makes an SDRAM that uses a CAS latency of 1. (RRFF 2151).

2154. Mr. Geilhufe testified that fixed CAS latency would involve extra photo tool costs of approximately $50,000 for each part. (Geilhufe, Tr. 9576). This testimony is contradicted by the weight of the evidence. (*Id.*).

Rambus's Response to Finding No. 2154:

The proposed finding is incorrect. Mr. Geilhufe's testimony is supported by the weight of the evidence. (RRFF 2155-56).

2155. SDRAM lite, which was a proposal for a fixed CAS latency part, would not have involved extra photo tool costs. (Lee, Tr. 11016 ("Okay, my understanding is it did not involve extra tool costs. We were only going to provide the one latency, so there was no other mask required.")).

Rambus's Response to Finding No. 2155:

The proposed finding is irrelevant. As discussed above, the SDRAM Lite proposal was for a single fixed CAS latency part. (RRFF 2139). Such a part would not, however, be acceptable from a user standpoint. (RRFF 2139). The extra photo tool costs are due to the requirement of multiple parts if the fixed latency alternative were selected. (RPF 827).

2156. Even if SDRAM lite would had included two different CAS latencies, it still would not necessarily have involved extra photo tool costs. (Lee, Tr. 11017 ("[If] [w]e had two

choices[,] [w]e could have implemented this with a fuse, which would therefore require no extra tooling, or if we created a second metal mask, then there would be an extra tool charge.")).

Rambus's Response to Finding No. 2156:

The proposed finding is misleading. Complaint Counsel cite Mr. Lee's testimony, but Mr. Lee testified only that if fuses were used to set CAS latency, there would have been no extra photo tool costs. While this may be true, setting CAS latency with fuses is a distinct alternative with its own net costs. (RPF 849-55).

(B) Blowing Fuses to Set CAS Latency.

2157. Manufacturers could have included in their designs CAS latency circuitry with a value of 2 and CAS latency circuitry with a value of 3. (Jacob, Tr. 5378-80; *see* DX0071). Each hardwire would have a fuse attached to it. (*Id.*). The CAS latency of the part would have depended on which fuse was blown. (*Id.*). The latency of the part would correspond to the latency value that was not blown. (*Id.*).

Rambus's Response to Finding No. 2157:

Rambus has no specific response.

2158. Fuses are used to disable connections between DRAM circuits. (Jacob, Tr. 5379-80). The concept of fuses is that they can select among DRAM circuits by disabling the connection to the undesired circuit while leaving intact the desired circuit. (*Id.*). Antifuses can be used to perform the same function as fuses. (Lee, Tr. 11170-71 (Micron uses fuses for redundancy repair); *see* {
}).

Rambus's Response to Finding No. 2158:

The proposed finding is incomplete. While antifuses can be used to perform the same function as fuses, they are less reliable than laser-blown fuses. (Soderman, Tr. 9356-57; Geilhufe, Tr. 9732-33).

2159. Manufacturers have reliably used fuses since at least the early 1990s for redundancy repair. (Jacob, Tr. 5381; Kellogg, Tr. 5130; Lee, Tr. 11167-70; {
}). In 1991, fuses were commonly used to select between particular functions of a

DRAM. (Rhoden, Tr. 428-29 ("So, fuses were pretty common at this time, still are very common, and [Samsung] w[as] proposing using a fuse similar to the ones that were in common use at the time and still today to actually select this option.")).

Rambus's Response to Finding No. 2159:

The proposed finding is incomplete. While DRAM manufacturers did use fuses in the 1990s, they generally used laser-blown fuses. (Geilhufe, Tr. 9581-82). Not all manufacturers had antifuse, or electrically-blown fuse technology available. (Geilhufe, Tr. 9582, 9740-41).

2160. It is possible to blow fuses either electrically or with laser technology. (Jacob, Tr. 5380-81; see DX0071-DX0073; Lee, Tr. 11170). Lasers can only blow fuses before packaging. (*Id.*). Electrically blown fuses, however, are typically used to blow fuses after packaging parts. (*Id.*).

Rambus's Response to Finding No. 2160:

The proposed finding is incomplete. Not all manufacturers had electrically-blown fuse technology available in the 1990s; for those manufacturers, it would not have been possible to blow fuses electrically. (Geilhufe, Tr. 9582, 9740-41).

2161. Manufacturers could design parts that were capable of operating with more than one CAS latency. (Jacob, Tr. 5378-79). Manufacturers or OEMs could then use fuses to determine the CAS latency of a part. (Jacob, Tr. 5378-79; { }).

Rambus's Response to Finding No. 2161:

The proposed finding is incorrect. OEMs could not use fuses to determine CAS latency. (Soderman, Tr. 9354-55). First, OEM's could only blow fuses capable of being blown after packaging, and not all DRAM manufacturers had such fuse technology available. (Geilhufe, Tr. 9582, 9740-41). Second, even if DRAMs with electrically blown fuses that could be blown after packaging were sent to OEMs, the OEMs do not have the equipment to perform the required testing of the DRAMs after blowing the fuses. (Soderman, Tr. 9355-56). Complaint Counsel

rely solely on the testimony of Professor Jacob for the proposition that OEMs could blow the fuses ({

}). Professor Jacob conceded, however, that OEMs could not test whether the fuse had been blown correctly (Jacob, Tr. 5597); Professor Jacob also admitted that he knows of no instance where fuses have been blown by OEMs. (Jacob, Tr. 5597-98).

2162. Manufacturers could have used either electrically blown or laser blown fuses to determine the CAS latency of a part on behalf of OEMs. (Rhoden, Tr. 425-28 (discussing a proposal from a DRAM manufacturer, Samsung, to the JC 42.3 Subcommittee to use fuses to determine one of the DRAM's operating modes); Sussman, Tr. 1379 ("Some companies were saying that we should [not] have [programmable CAS latency or burst length] at all. Their customers only are a very narrow base, not needed. There were some that were proposing that we do it by fuse option.")).

Rambus's Response to Finding No. 2162:

The proposed finding is incorrect. Manufacturers could not have used electrically blown fuses to determine CAS latency because some manufacturers did not have this technology available. (Geilhufe, Tr. 9582, 9740-41).

2163. JEDEC could have adopted use of electrically blown fuses to set CAS latency, which would have permitted either manufacturers or OEMs to set the latency. (Jacob, Tr. 5597; { }). Manufacturers could have tested the functionality of parts for different CAS latencies before they shipped the parts to OEMs who would have blown electrical fuses to determine latency. (Jacob, Tr. 5597).

Rambus's Response to Finding No. 2163:

The proposed finding is incorrect. JEDEC could not have adopted use of electrically blown fuses to set CAS latency because some manufacturers did not have this technology available. (Geilhufe, Tr. 9582, 9740-41). Even if electrically blown fuses were used, OEMs could not blow the fuses. (RRFF 2161).

2164. Using fuses to determine latency, before 1996, would have been simpler and cheaper and could have lowered test costs. (Jacob, Tr. 5382 ("After blowing the fuse, you would only need to test one CAS latency value instead of having to test all possible CAS latency values, so it would be a cheaper alternative potentially.")).

Rambus's Response to Finding No. 2164:

The proposed finding is incorrect. Complaint Counsel rely entirely on the testimony of Professor Jacob, who did not even attempt to quantify the cost increases and decreases associated with this (or any other) alternative. (Jacob, Tr. 5643-44). Mr. Geilhufe, who did do such an analysis, determined that the alternative of setting CAS latency using fuses would have led to a net cost increase of seven cents per unit. (RPF 853-54).

2165. Using fuses to determine CAS latency would have preserved a manufacturer's ability today to use latency as a way to distinguish between faster and slower DRAMs and fetch higher prices for parts that can operate at faster latencies. (Kellogg, Tr. 5141-42; {
}).

Rambus's Response to Finding No. 2165:

The proposed finding is misleading and incomplete. Once a fuse is blown, the DRAM becomes a fixed latency part. (Jacob, Tr. 5378-79). Thus, using fuses in an attempt to allow manufacturers to use latency between faster and slower DRAMs would have the same negative impact on yield as making multiple fixed latency parts by some other method. (RPF 846).

2166. At the December 1991 JC 42.3 meeting, Samsung gave a presentation that proposed a fuse option to select between two different types of DRAM operating modes. (JX0010 at 71 ("Fuse option for serial and interleaved wrap mode."); Rhoden, Tr. 427-428 (In testifying about Samsung's presentation, Rhoden stated, "[Serial and interleaved wrap mode] were two different modes of operation of the device, and they were proposing for selecting between those two different burst options. [Samsung] w[as] proposing using a fuse to do that.")).

Rambus's Response to Finding No. 2166:

The proposed finding is misleading and incomplete. The Samsung presentation did not

propose using fuses to set CAS latency, and there is no evidence that the Samsung presentation progressed beyond the first showing stage. (JX0010 at 5, 71).

2167. At the May 1992 JC 42.3 meeting, Cray gave a presentation that proposed the use of fuses to choose between two different CAS latencies, 2 and 3, for an SDRAM part. (CX0034 at 149 (proposing feature sets, which included CAS latency, for two SDRAM configurations and stating, "[d]efault [s]et fuse programmable by supplier")).

Rambus's Response to Finding No. 2167:

The proposed finding is misleading and incomplete. The referenced presentation by Cray did not involve simply a choice between two CAS latency values; rather, Cray was proposing to use a fuse to select between a set of features for a single bank configuration and a set of features for a dual bank configuration, where the feature set included, *inter alia*, the CAS latency value. (CX0034 at 149). This would not have yielded the flexibility of programmable CAS latency because the CAS latency could not be adjusted independently of numerous other features. Moreover, the Cray presentation was not even identified as a first showing in the minutes (CX0034 at 3-12), and there is no evidence that it ever progressed to even a first showing.

2168. Both Dr. Soderman and Mr. Geilhufe testified that blowing fuses to test CAS latency would result in fixed CAS latency parts, which would create the same inventory costs that were associated with multiple fixed CAS latency parts. (Soderman, Tr. 9354; Geilhufe, Tr. 9585-86).

Rambus's Response to Finding No. 2168:

Rambus agrees with this proposed finding, except that it should read "blowing fuses to *set* CAS latency."

2169. If the fuses were blown before packaging, Dr. Soderman and Mr. Geilhufe would be correct that thereafter, the parts would resemble fixed CAS latency parts. The issues identified by Dr. Soderman and Mr. Geilhufe could have been overcome, however, by use of slightly more sophisticated memory controllers that could detect when incomptible DIMMs are placed in the same system. (Jacob, Tr. 5382-83). Or, more sophisticated labeling of DIMMs.

(*Id.*). Dr. Soderman and Mr. Geilhufe disregard the advantages of fixed CAS latency parts, including faster access time and lower cost. (Soderman, Tr. 9346-53; Geilhufe, Tr. 9575-79; Jacob, Tr. 5375; Kellogg, Tr. 5138 ("I would just point out that fixed CAS latency would result in measurably improved performance if "fixed" implied no circuitry in the access path.")).

Rambus's Response to Finding No. 2169:

The proposed finding is incorrect and not supported by the evidence. Professor Jacob did not testify that using more sophisticated memory controllers would address the inventory costs associated with multiple fixed latency parts raised by Dr. Soderman and Mr. Geilhufe. (Jacob, Tr. 5382-83). Indeed, more sophisticated memory controllers have nothing to do with the costs in the manufacturing and distribution chains of having multiple parts instead of one.

The proposed finding is also incorrect that Dr. Soderman and Mr. Geilhufe disregarded advantages of fixed CAS latency parts. To the contrary, Mr. Geilhufe acknowledged that such parts would have lower testing costs and he incorporated these lower testing costs into his cost analysis. (RPF 835).

2170. If OEMs were to blow the fuses to set the CAS latency at the desired value, the issue identified by Dr. Soderman and Mr. Geilhufe as being associated with fixed CAS latency parts would not arise. (Bruce, Tr. 5379 (As Dr. Jacob explains, "[T]he DRAM manufacturer could ship a part that was capable of performing as a CAS latency 2 part or a CAS latency 3 part, ship that part to the OEM and the OEM would blow a fuse and it would at that point become a fixed latency part, but it would have either 2 or 3.")).

Rambus's Response to Finding No. 2170:

The proposed finding is irrelevant since OEMs could not blow the fuses. (RRFF 2161). Moreover, even if OEMs could blow fuses, the problems identified by Dr. Soderman and Mr. Geilhufe as being associated with fixed CAS latency parts would not be solved. Not all memory is purchased by OEMs – for example, consumers often purchase memory to upgrade their own computer systems. (Heye, Tr. 3746 ("The expectation of the user who buys that [PC]

is that at some time in the future they want to upgrade their memory, they can go buy some PC-100 memory and plug it in.")).

2171. Dr. Soderman and Mr. Geilhufe testified that electrically blown fuses are unreliable. (Soderman, Tr. 9356-57; Geilhufe, Tr. 9581-82). As evidence to support his point, Dr. Soderman testified that only two of the fifty Micron data sheets he reviewed included the use of electrically blown fuses. (Soderman, Tr. 9357). Mr. Geilhufe further testified that antifuse technology is generally not available in the DRAM process. (Geilhufe, Tr. 9583). The testimony of Dr. Soderman and Mr. Geilhufe on fuses is contradicted by the weight of the evidence. CCFF 2172-2177.

Rambus's Response to Finding No. 2171:

The proposing finding is incorrect. Dr. Soderman's and Mr. Geilhufe's testimony regarding fuses is supported by the weight of the evidence. { } (Lee, Tr. 11170 (*in camera*)). { } (*Id.*) This supports Mr. Geilhufe's testimony that laser blown fuses were the dominant fuse technology used by DRAM manufacturers in the 1995 time frame.

2172. All of Micron's SDRAM parts use electrically blown fuses. (Lee, Tr. 11022-23). Micron's data sheets do not indicate the use of electrically blown fuses because Micron's use of fuses is transparent, or invisible, to the customer and customers do not use fuses during system operation. (*Id.*).

Rambus's Response to Finding No. 2172:

The proposed finding is irrelevant because it relates to Micron's current SDRAM products. { } (Lee, Tr. 11170 (*in camera*)). Mr. Geilhufe's testimony that certain major manufacturers, such as Samsung, did not have electrically blown fuse technology available and that it would have been

very expensive for such manufacturers to develop the technology is unrebutted. (RPF 845, 855). A technology that was unavailable to certain major DRAM manufacturers could not realistically be incorporated into the standard.

2173. Inside DRAM chips, there are redundant storage elements which enable the repair of defective elements. In 1991 and 1992, manufacturers used fuses to replace bad bits of memory with good bits. (Rhoden, Tr. 428-29). Manufacturers still use fuses today to perform the same function. (*Id.*). Today, manufacturers use both electrical and laser fuses to disable defective memory storage elements. (Jacob, Tr. 5381).

Rambus's Response to Finding No. 2173:

The proposed finding is incomplete. The dominant fuse technology among DRAM manufacturers in the 1995 time frame was laser-blown fuses. (RPF 845).

2174. {

}

Rambus's Response to Finding No. 2174:

Rambus has no specific response.

2175. {
} (Lee, Tr. 11170, *in camera*). {
} (Lee, Tr. 11170-71, *in camera*). { } (*Id.*).

Rambus's Response to Finding No. 2175:

The proposed finding is irrelevant. (*See* RRFF 2172). In 1992, IBM used electrical fuses for redundancy repair. (Kellogg, Tr. 5130).

2176. In 1992, IBM used electrical fuses for redundancy repair. (Kellogg, Tr. 5130).

Rambus's Response to Finding No. 2176:

The proposed finding is irrelevant. (*See* RRFF 2172).

2177. Before 1996, it was potentially simpler and cheaper to use fuses to determine latency. (Jacob, Tr. 5382).

Rambus's Response to Finding No. 2177:

The proposed finding is incorrect. Complaint Counsel rely entirely on the testimony of Professor Jacob, who did not even attempt to quantify the cost increases and decreases associated with this (or any other) alternative. (Jacob, Tr. 5643-44). Mr. Geilhufe, who did do such an analysis, determined that the alternative of setting CAS latency using fuses would have led to a net cost increase of seven cents per unit. (RPF 853-54).

(C) Scale CAS Latency with Clock Frequency.

2178. The concept of scaling CAS latency with clock frequency could be implemented in one of two ways. (Jacob, Tr. 5383). The DRAM could sense the speed of the bus and internally calculate its own CAS latency. (*Id.* 5383-84). Or, the memory controller could tell the DRAM the speed of the bus. (*Id.* 5384-85).

Rambus's Response to Finding No. 2178:

Rambus has no specific response.

2179. If CAS latency were scaled with clock frequency, parts would operate with their optimum latency. (Jacob, Tr. 5384-85).

Rambus's Response to Finding No. 2179:

Rambus has no specific response.

2180. Dr. Soderman's testimony that this alternative would require complex additional circuitry carries little weight. (Soderman, Tr. 9358; CCFF 2181).

Rambus's Response to Finding No. 2180:

The proposed finding is incorrect. Dr. Soderman's testimony is supported by the weight of the evidence. (*See* RRFF 2181).

2181. Dr. Jacob testified that implementing this alternative would only require "a simple

circuit that would look at the bus frequency, the existing bus frequency, and do an edge detect to see if the bus frequency is faster than or slower than the internal reference." (Jacob, Tr. 5384).

Rambus's Response to Finding No. 2181:

Professor Jacob's testimony is entitled to little weight. Professor Jacob concedes that he did no design or simulation in connection with this alternative. (Jacob, Tr. 5591). Professor Jacob provided no indication of how the "internal reference" frequency was to be generated. (Jacob, Tr. 5384). Moreover, the circuit would only be able to distinguish between two particular bus frequencies (since it can only determine whether the frequency is faster or slower than some particular reference). This is clearly insufficient to deal with the various bus frequencies that actually exist. Professor Jacob gives the example of distinguishing between 100 MHz and 150 MHz, but then his "simple circuit" could not identify the intermediate bus frequency of 133 MHz. (*See* Heye, Tr. 3677 (noting that one version of SDRAM operates at 133 MHz)). Dr. Soderman's testimony that complex circuitry would be required to detect more than two bus frequencies is uncontradicted. (Soderman, Tr. 9358).

2182. It is true that this alternative would require either a slightly more sophisticated memory controller or labeling system in order to prevent the situation in which there were DIMMs operating with two incompatible latencies. (Jacob, Tr. 5385).

Rambus's Response to Finding No. 2182:

The proposed finding is incomplete and misleading. The alternative would require complex circuitry to detect more than two bus frequencies. (RRFF 2181).

2183. Dr. Soderman's testimony that this alternative would have been covered by Rambus patents is not supported by any evidence. (Soderman, Tr. 9359). Dr. Soderman did not identify which Rambus patent would be infringed. (*Id.*). Further, he did not engage in any patent analysis whatsoever beyond testifying that the alternative would require "some sort of a register." (*Id.*)

Rambus's Response to Finding No. 2183:

The proposed finding is incorrect. Dr. Soderman testified that this alternative would require the use of a register to store a CAS latency value. (Soderman, Tr. 9359). Complaint Counsel allege that Rambus has asserted patents against DRAM manufacturers that cover SDRAMs with a register to store a CAS latency value. (CCFF 1661). In introducing Dr. Jacob's testimony about alternatives, Complaint Counsel seek to show that JEDEC could have chosen alternatives that would have avoided Rambus's claimed intellectual property (CCFF 2100), that is, that JEDEC would not have chosen to use a register to store a CAS latency value. Dr. Soderman's testimony thus establishes that the purported alternative of scaling CAS latency with clock frequency is no alternative at all because it would infringe the same Rambus patents as are infringed by current SDRAMs.

Moreover, Dr. Soderman's opinion is supported by the analysis of Mark Kellogg of IBM. When Micron proposed just this alternative to avoid Rambus's patents Mr. Kellogg concluded that the problem with the proposal "was that nothing changed except the name assigned to the command register bits (originally defined as CAS Latency, now to be defined as frequency range or something similar). As such, I felt they were walking a fine line and that this change would not hold up in court as being anything other than an attempt to circumvent possible patent infringement via a term redefinition." (RX1626 at 2; RPF 866-67.)

(D) Using Dedicated Pin(s) to Set Latency.

2184. Rather than storing the CAS latency value at which a DRAM will operate in a mode register after system initialization, JEDEC could have dedicated a pin to set the CAS latency value during operation. (Jacob, Tr. 5386).

Rambus's Response to Finding No. 2184:

The proposed finding is incorrect. JEDEC could not have used a single dedicated pin because that would have only allowed a choice between two CAS latency values. (Lee, Tr. 11103). More than two values of CAS latency have been in use in the past, more than two are currently in use, and even more are expected to be used in the future. (RPF 813-21).

2185. JEDEC could have used one dedicated pin to store two different CAS latency values. (Jacob, Tr. 5386-87; Lee, Tr. 11025-26). Binary signals, or signals that can carry either a high or a low voltage level, are used to transmit information to DRAMs. (Rhoden, Tr. 359-60). A manufacturer could design a part that would operate as a CAS latency of 2 part when a high voltage level is present on a dedicated pin and a CAS latency of 3 part when a low voltage is asserted on that pin. (Jacob, Tr. 5386-87).

Rambus's Response to Finding No. 2185:

The proposed finding is incomplete. A single pin selecting between two CAS latency values would have been insufficient. (*See* RRFF 2184).

2186. In the 1991-1992 time frame, JEDEC considered the use of pins to set CAS latency. (Rhoden, Tr. 434).

Rambus's Response to Finding No. 2186:

The proposed finding is not supported by the evidence. Complaint Counsel cite to the following testimony of Mr. Rhoden:

Q. And [we've discussed] use of pins to set CAS latency and burst length.

Is that right?

A. That is correct.

However, the prior discussion reflects no proposals involving the use of pins to set CAS latency (and a single Mitsubishi proposal to set burst length with pins). (Rhoden, Tr. 431-34).

2187. Mr. Bechtelsheim testified that he would have preferred the use of pins to set CAS

latency because it was simpler and less effort on the system side. (Bechtelsheim, Tr. 5811 ("Personally, I actually preferred the pins because it was simpler, less effort on the system side, but the JEDEC group chose the mode register.")).

Rambus's Response to Finding No. 2187:

Rambus has no specific response.

2188. Use of a dedicated pin provided the same advantage of flexibility as programmable CAS latency without the need for circuitry on the DRAM. (Kellogg, Tr. 5127-38 (The use of dedicated pins was "one means by which we could produce parts through the production facility, put them into stock and have those parts capable of doing more than one mode of operation."); *Id.* 5129 ("The predominant advantage is that we could produce a part that could provide multiple functional modes to service a variety of applications.")).

Rambus's Response to Finding No. 2188:

The proposed finding is incorrect. A single dedicated pin would not have "provided the same advantage of flexibility as programmable CAS latency." A single dedicated pin could only select between two different CAS latency values while the SDRAM standard allows for up to 8 different values. (RPF 815).

2189. The disadvantage of using dedicated pins to set CAS latency was the test cost, which was also a disadvantage of programmable CAS latency. (Kellogg, Tr. 5127 ("The predominant disadvantage would be that we would have to test each mode, which would have some impact to our test cost, test time."); Kellogg, Tr. 5127). Kellogg articulated the same disadvantage for the use of a programmable mode register. (Kellogg, Tr. 5129 ("The predominant disadvantage -- and I'm summarizing here -- was that we would have to test each of the mode register options to ensure they all functioned properly.")).

Rambus's Response to Finding No. 2189:

The proposed finding is incomplete. There are various other disadvantages to using dedicated pins to set CAS latency. First, using pins instead of a mode register to set CAS latency would be less reliable because noise glitches could perturb the signal indicating the latency value from the controller to the DRAM. (RPF 871). In addition, the alternative would require

additional pins on the DRAM and controller, as well as, potentially, a more expensive connector, leading to substantial additional costs. (RPF 881-83).

2190. {

} (Macri, Tr. 4770, *in camera*){

}.

Rambus's Response to Finding No. 2190:

The proposed finding is not supported by the weight of the evidence. {

) (Macri, Tr. 4770 (*in camera*)). However, there is no evidence in the record regarding what sort of analysis, if any, Mr. Macri performed in arriving at a cost estimate. Mr. Geilhufe's conclusion, based on a cost analysis of the type that he performed repeatedly in industry, is more reliable than Mr. Macri's testimony.

2191. Both Dr. Soderman and Mr. Geilhufe assume that JEDEC would have had to add pins to DRAM packages in order to implement the dedicated pin alternative. (Soderman, Tr. 9362; Geilhufe, Tr. 9580). This assumption is not necessarily valid. (CCFF 2192-2201).

Rambus's Response to Finding No. 2191:

The assumption that pins would have had to be added to DRAM packages in order to implement the dedicated pin alternative is a valid assumption for the purpose of analyzing the cost of this alternative.

First, as Complaint Counsel concede, a number of SDRAM configurations did not have "no connect" pins available. (CCFF 2196.)

Second, the fact that a pin may be labeled "no connect" does not necessarily mean that it is available to be used for programming CAS latency. The pin might be used for testing purposes

(RPF 873), or it might be reserved for future uses or uses in other configurations (RPF 874-75).

Third, even if there were "no connect" pins available in a given package for programming CAS latency, that does not mean that the use of those pins is costless. By using the no connect pins, they would not be available for other purposes in the future meaning that future generations of the device would be forced into a larger, more expensive package that much sooner. As Gordon Kelley of IBM testified, using up a pin is not something that was done "easily, because once you use that pin up for a function, you don't have it available to you in the future for generation advance. As the memory densities increase, we need pins for more addressing of more address locations and those pins are very valuable for that feature, so this would have limited the number of generations of DRAM design that we could have used if we were to use up this pin." (Kelly, Tr. 2552-53).

2192. JEDEC would not necessarily had to have added new pins to DRAMs in order to implement the dedicated pin alternative to programmable CAS latency. (Jacob, Tr. 5387).

Rambus's Response to Finding No. 2192:

The proposed finding is misleading. (*See* RRFF 2191).

2193. No-connect pins are pins that do not connect to any circuit and therefore have no existing function for the part. (Jacob, Tr. 5387; Lee, Tr. 11030). JEDEC could have used a no-connect pin to set CAS latency. (*Id.*).

Rambus's Response to Finding No. 2193:

The proposed finding is incorrect. The pin might be used for testing purposes (RPF 873), or it might be reserved for future uses or uses in other configurations (RPF 874-75). Indeed, Mr. Lee, whom Complaint Counsel cite, testified that if a manufacturer used the same mask for x4, x8 and x16 configurations, and if a pin designated "no connect" in the x4 and x8 configurations

was used as a data pin in the x16 configuration, that pin could not be used for other purposes in the x4 and x8 configurations; in other words, the pin would need to remain a "no connect" pin in the x4 and x8 configurations. (Lee, Tr. 11084-87).

2194. JEDEC almost always provides for no-connect pins in its SDRAM and DDR SDRAM pinouts. (Lee, Tr. 11037; CX0234 at 80-142).

Rambus's Response to Finding No. 2194:

The proposed finding is irrelevant because no-connect pins cannot necessarily be used for other purposes and, even if they could be used, this would lead to less flexibility and increased cost in the future. (*See* RRFF 2191).

2195. At the time JEDEC was considering whether to adopt programmable CAS latency, there were pins available that could have been used to set CAS latency. (Sussman, Tr. 1377-78). Howard Sussman, for example, proposed a package for SDRAM that had a no-connect pin that could have been used to program CAS latency. (*Id.*). There were a number of presentations made at JEDEC that proposed using no-connect pins for other functions. (*Id.* 1378).

Rambus's Response to Finding No. 2195:

The proposed finding is incorrect. Mr. Sussman's testimony referred to a single no-connect pin, and the presentation referred to showing only a single no-connect pin. (Sussman, Tr. 1377-78; JX0010 at 54). That pin could be used, at most, to select between two different latency values. (*See* RRFF 2188).

2196. In Release 9 of JEDEC Standard No. 21-C, forty-four out of forty-seven pinouts for SDRAM and DDR SDRAMs have no-connect pins that are available to use for a function like determining CAS latency. (CX0234 at 80-142). Because the vref pin is hardly ever used, it could be available as a no-connect. (Lee, Tr. 11035). Counting the vref pin, forty-four out of forty-seven pinouts for SDRSAMs and DDR SDRAMs have two or more no-connect pins available. (Lee, Tr. 11037; CX0234 at 80-81 83, 85, 86, 87, 88-89, 90, 99, 100, 102, 104, 105, 106, 107-09, 110,121-22, 124-125, 127-28, 130, 131, 132-33, 134-35, 142).

Rambus's Response to Finding No. 2196:

The proposed finding is not supported by the evidence. Mr. Lee testified only that the VREF pin was not used for the particular SDRAM part whose pinout he was being shown. (Lee, Tr. 11035). There is no evidence to support the proposition that the vref pin was not used in other SDRAMs or in DDR SDRAMs.

2197. Even if there were no available no-connect pins, JEDEC would not necessarily have to add new pins in order to implement the dedicated pin alternative. (Lee, Tr. 11031-32). Before the standard was adopted, there was some flexibility with respect to assigning functions to pins, and a pin could have been reassigned to set CAS latency. (Kellogg, Tr. 5123-26).

Rambus's Response to Finding No. 2197:

The proposed finding is incorrect. Mr. Lee testified that JEDEC could have chosen to assert a "super voltage" on an existing pin; this procedure would not have been a viable alternative as set forth below. (RRFF 2198). Mr. Kellogg testified that JEDEC could have chosen to "multiplex" one or more pins – that is, to use pins to transmit different sorts of information at different times; this procedure likewise would not have been a viable alternative as set forth below. (RRFF 2199).

2198. To avoid adding a new pin, JEDEC could have asserted a super voltage on an existing pin to set the CAS latency if there were no available no-connect pins. (Lee, Tr. 11032). Manufacturers know how to use super voltages today because they use them in test mode. (*Id.*).

Rambus's Response to Finding No. 2198:

The proposed finding is not supported by the weight of the evidence. By a "super voltage" on a pin, Mr. Lee means a third voltage level other than the two already being used. Mr. Lee offered no evidence that this could be feasibly done or that the use of "super voltages" in test mode is analogous to their use in normal operation. Rambus, on the other hand, offered

substantial evidence that implementing more than two voltage levels on a pin was not feasible. (RPF 878). Indeed, Rambus tried to implement this technology in an early part and it was not successful. (RPF 879). It is telling that, despite the desire to keep pin counts low, no SDRAM or DDR SDRAM parts support more than two voltage levels per pin in normal operation. (Jacob, Tr. 11125-26).

2199. Another way to avoid adding a pin to determine CAS latency would be to multiplex existing pins or use a single pin for two functions. (Polzin, Tr. 4026 ("Q. And if there were no available pins on the DRAM, you'd have to add pins to the package; right? A. Or multiplex existing pins.")).

Rambus's Response to Finding No. 2199:

The proposed finding is irrelevant. While it might be possible to multiplexing exist pins to determine CAS latency, this alternative would not avoid Rambus's patents. Indeed, significantly, Professor Jacob, Complaint Counsel's technical expert on alternatives, did not testify that multiplexing existing pins was a viable alternative. Professor Jacob testified only to the possibility of using *dedicated* pins (Jacob, Tr. 5386 ("The idea is that rather than placing the value in a mode register, you send that same value over a dedicated pin, and so that pin would contain only – or it would transmit only that information during the lifetime of the DRAM.")). Multiplexing, on the other hand, means that the pins are not dedicated, but are used to transmit different types of information at different times. If the pins were multiplexed, however, since the CAS latency value would not always be available at the pins, it would have to be stored on the DRAM in a register. (Polzin, Tr. 4028-29). Thus, multiplexing pins is not an alternative at all – it would still require storing the CAS latency value in a register and would infringe Rambus's claims covering programmable CAS latency to the same extent as current SDRAMs.

2200. JEDEC could have multiplexed column address pins to determine CAS latency. (Kellogg, Tr. 5125-26 (In discussing options to determine burst length and other functions, Kellogg testified: "My first preference in that time period would be to use column address pins or pins that were not used during the column address portion of the read or write operation.")).

Rambus's Response to Finding No. 2200:

The proposed finding is irrelevant. Multiplexing pins would still require a register on the DRAM to store a CAS latency value and, therefore, would not avoid Rambus's patents. (*See* RRFF 2199).

2201. JEDEC's SDRAM and DDR SDRAM standard multiplexes a column address pin, A10. (CX0234 at 147, 151; Kellogg, Tr. 5125). Address pin, A10, can either be used to identify a column address or tell the DRAM to perform an autoprecharge function. (*Id.*).

Rambus's Response to Finding No. 2201:

The proposed finding is irrelevant. Multiplexing pins is possible in some circumstances, but to use multiplexed pins to set CAS latency would still require a register on the DRAM to store the CAS latency value and, therefore, would not avoid Rambus's patents. (*See* RRFF 2199).

2202. { } (Macri, Tr. 4765-77, *in camera*).

Rambus's Response to Finding No. 2202:

Rambus has no specific response, except to point out that Mr. Geilhufe's estimate of the cost of the pins that would be required to set CAS latency is uncontradicted.

2203. JEDEC could have used a DC pin that was dedicated only to determining the CAS latency of a part. (Kellogg, Tr. 5126; Jacob, Tr. 5387-88).

Rambus's Response to Finding No. 2203:

The proposed finding is incorrect. A single dedicated pin could have been used to

distinguish between only two CAS latency values. (RRFF 2188). Mr. Geilhufe's estimate of the cost of the pins that would be required to set CAS latency is uncontradicted.

2204. There are cost advantages associated with the use of DC pins to implement ths alternative. (Jacob, Tr. 5387-88). DC signals are constant signals and would therefore not require complicated receivers. (*Id.*).

Rambus's Response to Finding No. 2204:

Rambus has no specific response, except to point out that Mr. Geilhufe's estimate of the cost of the pins that would be required to set CAS latency is uncontradicted.

2205. DC pins are less expensive than data pins. (Jacob, Tr. 5387-88). Unlike data pins, whose voltage level change rapidly, DC pins carry a constant voltage level. (*Id.*; Kellogg, Tr. 5120). This allows for flexibility in the placement of DC pins in a package. (Jacob, Tr. 5387-88; Kellogg, Tr. 5124-25). DC pins can be placed in the less desirable location in the package so that more desirable locations can be reserved for data pins. (Kellogg, Tr. 5124-45 (In describing his understanding at the time of how a proposal, in 1992, for a dedicated burst length pin could be implemented, Mr. Kellogg testified, "We would select a pin in a region of the package that was not characterized or would not require special consideration from high speed set of attributes. In other words, this is a DC pin, so we'll place it somewhere out of the way.")).

Rambus's Response to Finding No. 2205:

Rambus has no specific response, except to point out that Mr. Geilhufe's estimate of the cost of the pins that would be required to set CAS latency is uncontradicted.

2206. Dr. Soderman assumed that the dedicated pin alternative would require storage like a mode register. (Soderman, Tr. 9360-62)(discussing a serially shifted register that could store a latency value). Dr. Soderman's testimony is not reliable. CCFF 2207-2210.

Rambus's Response to Finding No. 2206:

The proposed finding is incorrect and misrepresents Dr. Soderman's testimony. Dr. Soderman testified that if there were an attempt to use a single dedicated pin to select among more than two latency values by "serially shifting" the latency value – that is, by transmitting bits over more than one cycle – a register would be required to store the value. (Soderman, Tr.

9360-61). Dr. Soderman went on to testify that if multiple dedicated pins were used, a register would not be necessary, although there could be noise problems without one. (Soderman, Tr. 9361 ("Q. Okay. Now, if you weren't going to serially shift the latency value, can you avoid the use of a register? A. If you had multiple pins on the DRAM you could fix those values through some sort of special wires coming back on the DRAM package through the DIMMs, D-I-M-M-s, back through the controller. The DIMMs, that's the module that holds the individual DRAMs. And if you added all of those additional interconnections you could avoid having to store it, maybe. The problem you have is this is a very critical parameter, and any wires that you would run from the DIMMs to the memory controller or other processor that would be connected to it has noise . . . .")).

2207. Assuming that the burst length and burst type of a part were not programmed in a mode register, there is one implementation of the dedicated pin alternative that would entirely eliminate the need for storage. (Kellogg, Tr. 5126). If the DC pin were dedicated exclusively to identifying the CAS latency latency that a part would operate with, then the DC pin could hold the CAS latency value during system operation without a register. (*Id.*). The DC pin itself would essentially function as 'storage.' (*Id.*).

Rambus's Response to Finding No. 2207:

The proposed finding is incomplete. A single dedicated pin could only select between two CAS latency values. (Lee, Tr. 11103). More than two values of CAS latency have been in use in the past, more than two are currently in use, and even more are expected to be used in the future. (RPF 813-21).

2208. Even if JEDEC had chosen not to use a DC pin, it still would not need a register to implement the dedicated pin alternative. (Kellogg, Tr. 5126-27). It could have used a latch, which is not a register, to store the CAS latency value. (*Id.*).

Rambus's Response to Finding No. 2208:

The proposed finding is not supported by the weight of the evidence. In fact, a register is simply a generic class of storage (Soderman, Tr. 9450-51), and one type of register is a latch. (*Id.*; Horowitz, Tr. 8508-09 ("Register is just a storage -- a circuit that will remember something. And it's like a memory cell except -- so if you looked at them you could tell, but you use it a slightly different way, and it could either be a flip-flop or a latch, you know.) Complaint Counsel's technical expert, Professor Jacob concedes that "a register might be built out of latches." (Jacob, Tr. 5393). He testified that: "A latch is a specific implementation. A register implies how a piece of storage is being used." (*Id.*) In this case, if latches were used to store latency information, they would be used for precisely the same purpose as the mode register in an SDRAM.

2209. A latch is a storage element that can store a bit of information, either a positive or negative charge. (Kellogg, Tr. 5127). A register, on the other hand, stores a number of bits. (*Id.*). As Mr. Kellogg, from IBM, testified: "My view of a latch versus a register in th[e] [1992] time frame was that a latch typically stored a bit of information, either a plus or minus, whereas a register typically stored a numerous set of bits for an extended period of time." (*Id.*).

Rambus's Response to Finding No. 2209:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 2208). Moreover, even if the distinction Mr. Kellogg is trying to draw – namely, that a latch stores a signle bit, while a register stores numerous bits – were a valid one, a latch could only be used to select between two latency values and a register would be required to store information allowing a more than two latency options. More than two values of CAS latency have been in use in the past, more than two are currently in use, and even more are expected to be used in the future. (RPF 813-21).

2210. Dr. Soderman did not consider Mark Kellogg's testimony that the dedicated pin concept would not require a register at all, but instead would only require a latch. (Soderman, Tr. 9450-51 ("I have not read [Kellogg's testimony], but a latch is just a type of register, so you're calling it -- you're changing the name, but it's the same thing.")).

Rambus's Response to Finding No. 2210:

Rambus has no specific response.

2211. Because the dedicated pin alternative would eliminate the mode register and the interface necessary to program it, it would be simpler and therefore cheaper than programming CAS latency with a mode register. (Jacob, Tr. 5388).

Rambus's Response to Finding No. 2211:

The proposed finding is incorrect. First, Professor Jacob is simply mistaken: using dedicated pins to set CAS latency would not lead to elimination of the mode register because, as Professor Jacob conceded, the mode register is used for purposes other than setting CAS latency. (Jacob, Tr. 5594; RPF 834). Second, Complaint Counsel rely entirely on the testimony of Professor Jacob, who did not even attempt to quantify the cost increases and decreases associated with this (or any other) alternative. (Jacob, Tr. 5643-44). Mr. Geilhufe, who did do such an analysis, determined that the alternative of using dedicated pins to set CAS latency would have led to a net cost increase of four cents per unit. (RPF 880-81), not even taking into account the cost of additional pins on the controller and, potentially, a new, more expensive connector (RPF 882-83).

2212. Dr. Soderman testified that the dedicated pin alternative would require three pins and possibly four if it were necessary to add three additional pins in order to implement the alternative. (Soderman, Tr. 9362). His testimony is not reliable. (CCFF 2213-2218).

Rambus's Response to Finding No. 2212:

Rambus agrees that Dr. Soderman testified that three pins would have to be added to

implement the dedicated pins alternative, and, since pins must be added in pairs, four pins would actually be required. (Soderman, Tr. 9362-63). Contrary to the proposed finding, as set forth below, his testimony is reliable. (RRFF 2213-18).

2213. Dr. Soderman's testimony is based on the assumption that it would be necessary to preserve all of the optional values for CAS latency that currently exist in the mode register. (Soderman, Tr. 9362, 9462-63). Dr. Soderman admits that if the industry had decided that they only wanted two CAS latency values, then it could have done that with only one pin. (Soderman, Tr. 9463).

Rambus's Response to Finding No. 2213:

The proposed finding is misleading. The industry required the flexibility of allowing for more than two CAS latency values. (*See* RRFF 2215-18).

2214. JEDEC could have decided that they only needed two options for CAS latency. (CCFF 2215-2218).

Rambus's Response to Finding No. 2214:

The proposed finding is incorrect. (*See* RRFF 2215-18).

2215. Although other values have existed, the industry has typically only used CAS latency 2 or 3 for SDRAM. (Rhoden, Tr. 394).

Rambus's Response to Finding No. 2215:

The proposed finding is incomplete and misleading. The original SDRAM standard provided for four CAS latency values, three required and one optional. (JX 56 at 114; Lee, Tr. 11003-04). There were early SDRAMs that incorporated all four of those latency values. (Lee, Tr. 11063-64). Currently, SDRAMs are being produced with three latency values. (Lee, Tr. 11064-67). Although not all of the eight possible values of CAS latency are used in SDRAMs, the other possibilities were reserved to preserve flexibility for future additions. (Lee, Tr. 11072-73).

Complaint Counsel rely on Mr. Rhoden's testimony for this proposed finding, but Mr. Rhoden himself projected in 1996 that CAS latency values of 4, 5 and 6 would be required in the future. (JX0031 at 64). The DDR2 SDRAM standard greatly increases the number of latency options that can be programmed. (RPF 819).

2216. In September 1995, the JC 42.3 Subcommittee began to consider a number of proposals to reduce the number of required CAS latency options for SDRAM. (JX0029 at 8, 64-68). The Subcommittee overwhelmingly voted in favor of eliminating any required CAS latency values other than 2 and 3. (*Cf.* JX0056 at 114 (showing the original SDRAM mode register as requiring cas latencies 1, 2, and 3) with JX0027 at 8 (showing that the Committee reached a strong consensus in favor of making cas latency of 1, which would leave only cas latency of 2 and 3 as required)).

Rambus's Response to Finding No. 2216:

The proposed finding is misleading and incomplete. First, the Subcommittee did not vote to remove CAS latency of 1 from the standard, but rather to make it optional rather than required. (JX0027 at 8). Second, the Subcommittee did not vote to remove the flexibility provided by the mode register allowed for adding other CAS latency values in the future. (Lee, Tr. 11072-73). This is not surprising given that, in March 1996, Desi Rhoden was predicting that CAS latencies of 4, 5 and 6 would be necessary in the future. (JX0031 at 64).

2217. In January 1996, the JC 42.3 Subcommittee reviewed votes on a survey ballot for SDRAM lite. (JX0029 at 13). A majority of the Subcommittee wanted SDRAM lite to use a CAS latency of 3, but there was no consensus on whether to also needed to include the capability to use a CAS latency of 2. (*Id.*; Lee, Tr. 6630-31).

Rambus's Response to Finding No. 2217:

The proposed finding is incomplete and misleading. More JEDEC members voted for including CAS latency 2 than voted against it. (JX0029 at 13). The SDRAM lite proposal was rejected. (Sussman, Tr. 1416-17).

2218. When JEDEC published Release 9 of Standard 21-C, it had two required CAS latency values for SDRAM and DDR SDRAM. (Lee, Tr. 11006).

Rambus's Response to Finding No. 2218:

The proposed finding is incomplete and misleading. Release 9 of Standard 21-C, published in 1999, included two required CAS latency values for SDRAM and an optional value, as well as two required CAS latency values for DDR SDRAM and three optional values. (CX0234 at 150). The remaining possible values for CAS latency in the mode register were reserved to provide flexibility for future addtions. (Lee, Tr. 11072-73).

(E) Identifying CAS Latency in the Command.

2219. Identifying CAS latency in the command involves including CAS latency information in the command signal that is sent to initiate any operation. (Jacob, Tr. 5389-90).

Rambus's Response to Finding No. 2219:

Rambus has no specific response.

2220. Identifying CAS latency in the command would require defining a presently unused command set to identify the CAS latency for DRAM operation. (Jacob, Tr. 5389-90).

Rambus's Response to Finding No. 2220:

The proposed finding misrepresents the proposed alternative in its reference to an "unused command set." SDRAMs currently have a "command set" – that is, a correspondence between combinations of the five control signals and the commands that are to be performed by the DRAM in response to receiving those combinations. (Jacob, Tr. 5389-90). Professor Jacob testified that certain combinations of command signals are not currently used to specify commands and that these unused combinations could be used to issue commands that encode the CAS latency values rather than storing the CAS latency in the mode register. (Jacob, Tr. 5391).

2221. The truth table for SDRAM and DDR SDRAM contains command sets that are available to create new read commands that identify one or more CAS latencies. (Jacob, Tr. 5390). The five command lines can carry a combination of thirty-two signals; only about twelve combinations of which are currently used. (Jacob, Tr. 5390-91).

Rambus's Response to Finding No. 2221:

The proposed finding is unsupported. *See* RRFF 2220.

2222. In the JEDEC standard for SDRAM and DDR SDRAM, there is a "truth table" which defines all of the combinations of command signals that are currently used for "standard SDRAM operational functions." (CX0234 at 145; Lee, Tr. 11031-32). There are many combinations of command signals that currently do not define any function in the truth table. (Jacob, Tr. 5391). Instead of adding a new pin, JEDEC could have used one of the currently undefined combinations of command signals in the truth table to define a particular CAS latency. (Lee, Tr. 11032).

Rambus's Response to Finding No. 2222:

The proposed finding is irrelevant because, even if JEDEC could have redefined the command set to encode CAS latency values in commands, it would not have provided an alternative to Rambus's intellectual property. A command to a DRAM is valid for only a brief time period; in order for a CAS latency value in the command to be retained and used by the DRAM, it would have to be stored in a register. (Soderman, Tr. 9365).

2223. Identifying CAS latency in the command might require more complex decoding circuitry for command sets. (Jacob, Tr. 5392). However, the increased complexity of the decode circuitry would not have significant cost implications. (*Id.*). The cost implications of more complex decode circuitry may be balanced out by the removal of the initialization circuitry that was necessary to program CAS latency with a mode register. (*Id.*).

Rambus's Response to Finding No. 2223:

The proposed finding is incomplete. In addition to requiring more complex decoding the alternative would reduce the flexibility of the current command set. (Jacob, Tr. 5599 ("This would have the negative side effect of limiting the simultaneous issuing of independent

commands that is possible with the current command set, for example, setting DQ mask during the same cycle as issuing a column write.") (quoting expert report)). In order to preserve the flexibility of the command set as currently defined, an extra pin would be required. (Jacob, Tr. 5392).

2224. Dr. Soderman testified that identifying CAS latency in the command would require something that looks like a register. (Soderman, Tr. 9365). This testimony is not reliable. (CCFF 2225).

Rambus's Response to Finding No. 2224:

Dr. Soderman did testify that identifying CAS latency in the command would require a register. As set forth below, this testimony is reliable. (RRFF 2225).

2225. A latch could be used to store the CAS latency value after the command which identified the CAS latency for a system's operation was sent over the command bus. (Jacob, Tr. 5393). A latch is not a register. (Jacob, Tr. 5393; Kellogg, Tr. 5126-27 discussed, *supra*, at CCFF 2207-2209).

Rambus's Response to Finding No. 2225:

The proposed finding is not supported by the weight of the evidence. A register is a generic class of storage which can consist of latches or other forms of storage elements. (Soderman, Tr. 9450-51; Horowitz, Tr. 8508-09; Jacob, Tr. 5393; Rambus's Response to Finding No. 2208). Even if the distinction tthat Mr. Kellogg draws in his testimony were valid – namely, that a latch stores a single bit, while a register stores numerous bits – a latch could only be used to select between two latency values and a register would be required for more latency options.

2226. Mr. Geilhufe testified that identifying CAS latency in the read command might require an additional pin and possibly two if the package needs to be balanced. (Geilhufe, Tr. 9580). His testimony is contradicted by the weight of the evidence.

Rambus's Response to Finding No. 2226:

Mr. Geilhufe did testify that identifying CAS latency in the command could require an additional pin, and, since pins are added in pairs, two pins could be required. (Geilhufe, Tr. 9580). As set forth below, this testimony is reliable. (RRFF 2227).

2227. Identifying CAS latency in the command only requires defining a new command set and sending over wires to existing pins. (Jacob, Tr. 5389-90). It therefore does not require the addition of a new pin. (*Id.*).

Rambus's Response to Finding No. 2227:

The proposed finding is incorrect. As Professor Jacob testified, in order to preserve the flexibility provided by the current command set, an additional pin would be required. (RRFF 2223).

(F) Stay Asynchronous.

2228. The primary difference between asynchronous and synchronous memory is whether or not the system clock directly controls the DRAM or not. (Jacob, Tr. 5394-95). In synchronous memory, the system clock directly controls both the memory controller and the DRAM. (*Id.*). In asynchronous memory, the system clock directly controls the memory controller. The memory controller in turn controls the DRAM by means of the RAS and CAS signals that the memory controllers sends to it over the bus. (*Id.*).

Rambus's Response to Finding No. 2228:

Rambus has no specific response.

2229. In the early 1990s, JEDEC considered an asynchronous design as an alternative to the SDRAM proposals. (CX0711 at 1 (During a September 22, 1993, JEDEC meeting, Crisp noted that HP, Micron, and Mitsubishi stated that "EDO is the right thing to do [and] that it offers better performance than DRAM at a much lower cost than SDRAM.").

Rambus's Response to Finding No. 2229:

The proposed finding is misleading in its suggestion that the choice between considering asynchronous designs and pursuing SDRAM were mutually exclusive. To the contrary, the

evidence shows that JEDEC continued to pursue asynchronous designs during and after the time that SDRAM was standardized. For example, at the February 1992 JC-42.3 meeting, during the SDRAM standardization process, numerous presentations were made regarding SDRAM and also regarding various asynchronous memories. (JX0012 at 5-14). At this meeting, Toshiba, Fujitsu and NEC made presentations regarding both SDRAM and certain asynchronous memory technology they were proposing to develop. (JX0012 at 8-9, 10-11; RRFF 519).

After the SDRAM standard was adopted in 1993, JEDEC continued to consider aysnchronous memory technologies. For example, a new generation of EDO DRAMs, called "Burst EDO" was developed and standardized at JEDEC in mid-1995. (Williams, Tr. 873, 879-80; RX 585 at 1). However, Burst EDO failed in the marketplace in competition with SDRAM. (Williams, Tr. 829). As Dr. Oh of Hyundai testified regarding Burst EDO: "[T]his is enhanced version of EDO, and we wanted to convince our customers the advantages of this part, but was not accepted by our customers." (CX2108, Oh Dep. at 236).

2230. Burst EDO is an asynchronous memory. (CX2632 at 1). In the 1994-1996 time frame, Micron promoted Burst EDO within JEDEC as an alternative to SDRAM for the PC market. (Williams, 821-22).

Rambus's Response to Finding No. 2230:

The proposed finding is incomplete and not supported by the evidence. The cited testimony indicates that Micron promoted Burst EDO as an alternative to SDRAM for the PC market to its customers, but does not mention such promtion "within JEDEC." It is true that Burst EDO was standardized by JEDEC in 1995. (*See* RRFF 2229). However, Burst EDO failed in competition with SDRAM in the marketplace. (*Id.*)

2231. For 66 mhz busses, BEDO could have been faster than SDRAM by two clock

cycles for each burst of data. (CX2632 at 5 (figure 2 illustrates the speed advantages of BEDO compared to SDRAM).

Rambus's Response to Finding No. 2231:

The proposed finding is incomplete, misleading and based on unreliable evidence. Complaint Counsel cite, as the only support for this proposition, a Micron marketing document touting Burst EDO entitled "The Burst EDO DRAM Advantage." (CX2632 at 1). Even this document admits that Burst EDO would not be suitable for the high speed operation required in the future, noting that Burst EDO "will probably reach its limit somewhere around 100 MHz." (CX2632 at 5).

2232. In 66 mhz PC main memory applications, BEDO had one less lead-off cycle than SDRAM in all accesses. (CX2632 at 6). This could equate to as much as a 10 to 12 percent performance advantage in favor of BEDO as compared to SDRAM. (*Id.*).

Rambus's Response to Finding No. 2232:

The proposed finding is incomplete, misleading and based on unreliable evidence. (*See* RRFF 2231).

2233. Asynchronous memory could have been improved incrementally just as synchronous memory has been. (*See, e.g.,* Williams, Tr. 829-30 (testifying that improvements could have been made to increase the performance of BEDO devices)).

Rambus's Response to Finding No. 2233:

The proposed finding is not supported by the evidence. Even the testimony of Mr. Williams, one of the proponents of Burst EDO at Micron, on which Complaint Counsel rely states only:

> [W]e thought that right around 120 -- 100 megahertz, somewhere in that area, it would need to have more work done on it to increase the performance beyond

that, whether that was changing the I/O signaling levels or whatever, there would be more work that needed to be done, and actually I indicated that on page 5 of that same document. So, we knew that more work needed to be done on it. Where ultimately it could have gone would just be based upon the work that we did.

(Williams, Tr. 829-30.)

There is no evidence of what analysis, if any, Mr. Williams did to arrive at this conclusion or what he would have done to improve Burst EDO performance other than "changing the I/O signaling levels or whatever."

In fact, it was generally understood in the 1990s that asynchronous memories were not capable of reaching the speeds that would be required for future DRAMs. (RPF 897-901).

4. Alternatives to Programmable Burst Length.

2234. In the 1991-1996 time frame, there were at least six alternatives to the use of programmable burst length in JEDEC SDRAM and DDR SDRAM. (Jacob, Tr. 5397-98; see DX0078). First, JEDEC could have used a fixed burst length. (*Id.* 5397). Second, it could have used fuses to program the burst length. (*Id.* 5398). Third, it could have used a dedicated pin(s) to determine the burst length. (*Id.*). Fourth, it could have identified the burst length in the read command. (*Id.*). Fifth, JEDEC could have used a burst terminate mechanism to determine burst length. (*Id.*). Sixth, JEDEC could have toggled the CAS pulse in order to determine burst length. (*Id.*).

Rambus's Response to Finding No. 2234:

The proposed finding is incorrect. None of the proposed alternatives were viable alternatives to programmable burst length. (RPF 903-63; RRFF 2237-2321).

2235. Five of these alternatives – fixed burst length, use of fuses to set burst length, use of pins to set burst length, burst terminate, and identifying burst length in the command – were proposed for incorporation in the JEDEC SDRAM standard in the 1991-1992 time period. (JX0010 at 71, 74-75; CX0034 at 149; JX0027 at 64-69; Kellogg, Tr. 5102, 5110-11; Rhoden,

Tr. 426-434; Sussman, Tr. 1388-89, 1416-17; Lee, Tr. 6625-26).

Rambus's Response to Finding No. 2235:

The proposed finding is incomplete. Four of these five alternatives were considered and rejected in favor of programmable burst length. An optional burst terminate command was included in the JEDEC SDRAM standard (CX0234 at 161), but, contrary to Complaint Counsel's assertion that this was a viable alternative to programmable burst length, programmable burst length was also included (CX0234 at 150).

2236. In the 1991-1992 time period, the costs associated with these alternatives – fixed burst length, use of fuses to set burst length, use of pins to set burst length, and burst terminate – compared to programmable burst length using a mode register were relatively similar. (Kellogg, Tr. 5132 ("Q. And again, in the 1992 time period, when you were doing this analysis, did you consider any of the four options listed on DX-57 to be unsatisfactory from a cost point of view? A. The cost associated with each of those was relatively similar in the large scheme of things, so I would say from a cost standpoint, that was a large factor in our decision.")).

Rambus's Response to Finding No. 2236:

The proposed finding is not supported by the weight of the evidence with respect to the first three of these alternatives. (RRFF 2237-95). Using the burst terminate command would not have added cost, but it was unacceptable from a performance standpoint. (RRFF 2306-18).

(A) Fixed Burst Length.

2237. As with fixed CAS latency, a manufacturer could fix the burst length of a part during the design, manufacturing, or packaging phase. (Jacob, Tr. 5398-99).

Rambus's Response to Finding No. 2237:

Rambus has no specific response.

2238. During the design phase, a manufacture could hardwire a single burst length value that would drive the burst length circuitry inside of a chip. (Jacob, Tr. 5399; see DX0080).

Rambus's Response to Finding No. 2238:

Rambus has no specific response.

2239. In 1991-1992, fixing a single burst length in the design phase would have had technical and cost advantages. (Kellogg, Tr. 5117-18). It would have simplified the design and thereby reduced the design cycle time necessary to implement it. (*Id.*). It would have improved the performance of SDRAM by eliminating the propagation delay that occurs when the circuitry necessary to implement programmable burst length is driven. (*Id.*). It would reduce test costs because it would not have been necessary to test a part for its ability to work with different burst length options. (*Id.*).

Rambus's Response to Finding No. 2239:

The proposed finding is irrelevant. Clearly a single fixed burst length part was technically feasible and would not suffer from manufacturing cost disadvantages since it would be simpler than a programmable burst length part; it would, however, be unacceptable from a user standpoint – different burst lengths are required for different applications. (RPF 907). Indeed, Mr. Kellogg of IBM, on whose testimony Complaint Counsel rely for this proposed finding, testified that he recommended to his company in 1992 that they support the programmable burst length feature because "[i]t offered us the greatest flexibility. We had a lot of applications." (Kellogg, Tr. 5132). If the additional performance and flexibility offered by a programmable burst length part were not important, there would be no reason to include it in SDRAMs, DDR SDRAMs, and DDR2 SDRAMs.

2240. Assuming that CAS latency and burst type were fixed as well, a fixed burst length could potentially eliminate the mode register. (Jacob, Tr. 5401-02). It could thereby also eliminate the circuitry that is necessary to initialize the mode register. (*Id.*). Because it potentially eliminates circuitry, fixed burst length would result in a smaller and therefore potentially cheaper part than programmable burst length. (*Id.*). Depending on the phase at which burst length was fixed, it could also have reduced test costs. (*Id.*).

Rambus's Response to Finding No. 2240:

The proposed finding is incorrect. As an initial matter, Professor Jacob testified that fixing burst length alone could eliminate the mode register (Jacob, Tr. 5402); Complaint Counsel, apparently recognizing that this was in error because the mode register is used for other purposes, seek a finding that if CAS latency, burst length, and burst type were all fixed that the mode register could be eliminated. However, even if CAS latency, burst length and burst type were all fixed (and Complaint Counsel have not introduced any evidence whatsoever to suggest that it would be feasible to fix burst type), the mode register is used for yet additional purposes and could not be eliminated. (RPF 834). In some SDRAMs, the mode register is also used for programming operating mode and write burst mode; yet additional features to be programmed in the mode register are added in DDR SDRAMs and DDR2 SDRAMs. (RPF 834; RX 2100-13 at 3).

The proposed finding is also incomplete. While the fixed burst length alternative could have reduced test costs, the cost savings would have been outweighed by the cost increases in other areas. (RPF 915-20).

2241. If JEDEC had wanted to preserve the flexibility of a part without using a mode register to program burst length, a manufacturer could have hardwired two different burst length values in a chip, each of which could drive the burst length circuitry inside of the chip. (Jacob, Tr. 5399-5400; see DX0081; *see also* Kellogg, Tr. 5118-19). During the manufacturing phase, a metal mask option would have selected one of the hardwired values to drive the burst length circuitry. (*Id.*).

Rambus's Response to Finding No. 2241:

The proposed finding is incomplete and misleading. Two burst lengths would not have been sufficient. Micron, for example, sells SDRAMs that offer five different burst lengths.

(RX 2100-13 at 1; Lee, Tr. 11078-80). Even if only four different fixed burst length parts were made, the net cost increase would have amounted to four cents per unit. (RPF 915-20).

2242. A manufacturer could hardwire a multiplexor inside of a chip with two different burst length values that connected to the burst length circuitry. (Jacob, Tr. 5400-01; see DX0082). In one implementation, one of the burst length values inside of the multiplexor would connect to power and the other would connect to ground. (*Id.*). During the packaging phase, a bonding option would connect the multiplexor to either power or ground and thereby determine what burst length value would drive the burst length circuitry. (*Id.*).

Rambus's Response to Finding No. 2242:

The proposed finding is incomplete and misleading. (*See* RRFF 2241).

2243. In 1991-1992, JEDEC considered using fixed burst length. Samsung presented an SDRAM proposal that included a fixed burst length of 8. (JX0010 at 71; Rhoden, Tr. 426-27).

Rambus's Response to Finding No. 2243:

The proposed finding is incomplete. The Samsung presentation was a first showing (JX0010 at 5), and there is no evidence that it ever progressed beyond the first showing stage.

2244. In 1995-1996, JEDEC considered an SDRAM lite part. (JX0027 at 64-68). The use of a single fixed burst length was among the features proposed for SDRAM lite. (Lee, Tr. 6626).

Rambus's Response to Finding No. 2244:

The proposed finding is incorrect and misleading. The SDRAM lite proposal cited did not propose a single fixed burst length, but, rather, proposed two burst lengths. (RRFF 572). Even this proposal was ultimately rejected. (Sussman, Tr. 1416-17).

2245. In 1995-1996, Micron was in favor of SDRAM lite because it was simpler and faster to design that full-featured SDRAM. (Lee, Tr. 6633).

Rambus's Response to Finding No. 2245:

The proposed finding is misleading and incomplete. (*See* RRFF 2244).

2246. In 1995-1996, the use of fixed burst length was acceptable from both a technical and cost perspective. (Lee, Tr. 6633-34; *see also* Kellogg, Tr. 5131-32).

Rambus's Response to Finding No. 2246:

The proposed finding is irrelevant. As discussed above, while a single fixed burst length part would have been technically feasible and would not have suffered from cost disadvantages, it was unacceptable from a user standpoint. (*See* RRFF 2239).

2247. Both Dr. Soderman and Geilhufe assumed that fixed burst length would require multiple parts. (Soderman, Tr. 9369; Geilhufe, Tr. 9595). Mr. Geilhufe testified that fixed burst length would require four parts. (Geilhufe, Tr. 9595). Their testimony is contradicted by the weight of the evidence. (CCFF 2248-2250).

Rambus's Response to Finding No. 2247:

Rambus agrees that Dr. Soderman and Mr. Geilhufe testified that fixed burst length would require multiple parts and that Mr. Geilhufe assumed that four parts would be required for his cost analysis. Contrary to the proposed finding, this assumption is supported by the weight of the evidence. (*See* RRFF 2248-50).

2248. Release 4 of JEDEC Standard 21-C requires only two burst lengths, a burst length of 4 and 8. (JX0056 at 114; Lee, Tr. 11013-14).

Rambus's Response to Finding No. 2248:

The proposed finding is incomplete. Release 4 of JEDEC standard 21-C also includes three optional burst lengths of 1, 2 and "full page"; three other values are "reserved." (JX0056 at 114). Moreover, Release 9 of JEDEC Standard 21-C added a required burst length value – it had three required burst length values and two optional values. (CX0234 at 150). SDRAMs are being sold that include all five options for burst length. (RX 2100-13 at 1; Lee, Tr. 11078-80).

2249. Release 4 of JEDEC Standard 21-C contains two optional burst lengths, a burst length of 1 and 2. (JX0056 at 114; Lee, Tr. 11014). Neither has been used in main memory.

(Lee, Tr. 11014).

Rambus's Response to Finding No. 2249:

The proposed finding is incorrect. Release 4 also includes a third optional burst length of "full page." (RRFF 2248).

The proposed finding that burst lengths of 1 and 2 have not been used in main memory is irrelevant and based on unreliable testimony. Mr. Lee testified that he was "not aware" of burst lengths of 1 or 2 being used in main memory (Lee, Tr. 11014), but Mr. Lee is an unreliable witness. Mr. Lee also testified that he had no knowledge of CAS latency 1 being used in SDRAM, until he was confronted with a Micron SDRAM data sheet using CAS latencies of 1, 2 and 3. (RRFF 2151). However, even if Mr. Lee were correct and these burst lengths were not used in main memory, they are used in graphics applications (Lee, Tr. 11076) and, therefore, would still have to be supported.

2250. In the 1995-1996 time frame, JEDEC considered adopting an SDRAM lite part. (Lee, Tr. 11017). "The goal of the SDRAM-Lite was to try to end up with one CAS latency and one burst length." (*Id.* 11007). For SDRAM lite, JEDEC considered the most popular burst length at the time which was a burst length of 4. (Lee, Tr. 11015).

Rambus's Response to Finding No. 2250:

The proposed finding is misleading and not supported by the weight of the evidence. The SDRAM lite proposal included two burst lengths – 1 and 4. (RRFF 572). Even this proposal was ultimately rejected. (Sussman, Tr. 1416-17). While the most popular burst length was 4, in response to an SDRAM lite survey ballot, substantially more members voted to retain burst lengths of 1 and 2 also than voted to reject them. (JX0029 at 13).

2251. Mr. Geilhufe testified that adopting fixed CAS latency and fixed burst length would require 12 parts for SDRAM and 15 parts for DDR SDRAM per density. (Geilhufe, Tr.

9601). Mr. Geilhufe's testimony assumes that JEDEC would have needed to standardize three different CAS latencies and four different burst lengths for SDRAM. (*Id.*). It also assumes that JEDEC would have needed to standardize three different CAS latencies and five different burst lengths for DDR SDRAM. (*Id.*). This testimony is contradicted by the weight of the evidence. (Refer to CCFF 2149-2153, 2247-2250, challenging the Mr. Geilhufe's testimony that fixed CAS latency requires three parts and fixed burst length requires four); *see also* CCFF 2252-2255).

Rambus's Response to Finding No. 2251:

The proposed finding is misleading. Mr. Geilhufe's cost estimates for the fixed latency alternative were based on three different parts. (RPF 838). Mr. Geilhufe's cost estimates for the fixed burst length alternative were based on four different parts. (RPF 918). Both of these assumptions are supported by the weight of the evidence. (RRFF 2149-53, 2247-50). Mr. Geilhufe also noted that if JEDEC had chosen to fix both CAS latency and burst length, retaining the various options offered by SDRAM and DDR SDRAM would have led to 12 and 15 parts, respectively, and much greater inventory costs. (RPF 921).

2252. In 1995-1996, JEDEC considered adopting an SDRAM lite part with a single fixed latency and length. (JX0029 at 13; Lee, Tr. 11018-19). If JEDEC had reach agreement on a single fixed latency and length for SDRAM lite, that would have resulted in one part per density. (*Id.*).

Rambus's Response to Finding No. 2252:

The proposed finding is misleading and not supported by the weight of the evidence. Neither a single fixed latency nor a single fixed burst length would have been acceptable from a user standpoint. (*See* RRFF 2139, 2239). Moreover, the SDRAM lite proposal actually included two, not one, burst lengths. (RRFF 572). The SDRAM lite proposal was rejected. (RRFF 2139, 2239).

2253. At most, JEDEC would have needed to standardize two different CAS latencies for SDRAM and DDR SDRAM. For SDRAM, customers primarily use CAS latencies of 2 and 3. (Lee, Tr. 11004-05). The use of CAS latency of 1 for SDRAM was never widespread. (*Id.*).

In Release 9 of JEDEC Standard 21-C, there are only two require CAS latencies. (*Id.* 11006; CX0234 at 150).

Rambus's Response to Finding No. 2253:

The proposed finding is not supported by the weight of the evidence. Not only have CAS latency values other than 2 and 3 been used in the past, but other values are in use today, and more values will be used in the future. (RRFF 2151). Mr. Lee's testimony, on which Complaint Counsel rely for this proposed finding, is not reliable. Mr. Lee testified that he had no knowledge of CAS latency 1 being used in SDRAM, until he was confronted with a Micron SDRAM data sheet using CAS latencies of 1, 2 and 3. (RRFF 2151).

2254. At most, JEDEC would have needed to standardize two different burst lengths for SDRAM and DDR SDRAM. Intel-compatible PCs use a burst length of 4. (Polzin, Tr. 3994). DRAM customers like AMD, however, use a burst length of 8. (*Id.*). Use of burst lengths of 1 and 2, however, have not been widespread. (Lee, Tr. 11014).

Rambus's Response to Finding No. 2254:

The proposed finding is not supported by the weight of the evidence. SDRAMs are being sold that include five options for burst length. (RX 2100-13 at 1; Lee, Tr. 11078-80). Complaint Counsel rely on Mr. Lee's testimony that the use of burst lengths of 1 and 2 have not been widespread, but Mr. Lee is not a reliable witness. (*See* RRFF 2253). Moreover, Mr. Lee admitted that burst lengths of 1 and 2 are used in graphics applications. (Lee, Tr. 11076).

2255. If JEDEC had reached agreement on two different CAS latencies and burst lengths, that would have resulted in only four parts per density. (Refer to Geilhufe, Tr. 9601 (explaining his methodology on the number of parts fixed CAS latency and burst length would require)).

Rambus's Response to Finding No. 2255:

The proposed finding is irrelevant. More than two different CAS latency values and burst

length values would have been required. (RRFF 2253-54.)

2256. Mr. Geilhufe testified that fixed burst latency would involve extra photo tool costs of $50,000 for each part. (Geilhufe, Tr. 9594). This testimony is contradicted by the weight of the evidence. (*Id.*).

Rambus's Response to Finding No. 2256:

Mr Geilhufe did testify that fixed burst length would involve extra photo tool costs of $50,000 per part. Contrary to the proposed finding, Mr. Geilhufe's testimony is supported by the weight of the evidence. (RRFF 2257-58).

2257. SDRAM Lite, which was a proposal for a fixed burst length part, would not have involved extra photo tool costs. (Lee, Tr. 11016 ("Okay, my understanding is it did not involve extra tool costs. We were only going to provide the one latency, so there was no other mask required.")).

Rambus's Response to Finding No. 2257:

The proposed finding is irrelevant. The extra photo tool costs stemmed from the requirement for multiple parts. (RPF 916). Moreover, the SDRAM lite proposal was not for a fixed burst length part. (RRFF 572).

2258. Even if SDRAM lite would had included two different burst lengths, it still would not necessarily have involved extra photo tool costs. (Lee, Tr. 11017 ("[If] [w]e had two choices[,] [w]e could have implemented this with a fuse, which would therefore require no extra tooling, or if we created a second metal mask, then there would be an extra tool charge.")).

Rambus's Response to Finding No. 2258:

The proposed finding is misleading. Complaint Counsel cite Mr. Lee's testimony, but Mr. Lee testified only that if fuses were used to set burst length, there would have been no extra photo tool costs. While this may be true, setting burst length with fuses is a distinct alternative with its own net costs. (RPF 927-32).

2259. Mr. Geilhufe testified that fixed burst length parts would require $100,000 extra in

design costs per part. (Geilhufe, Tr. 9594 ("You will find that fixed burst length is identical to fixed CAS latency. It has exactly the same characteristics. So, the $100,000 is a design effort for each part type."). Mr. Geilhufe's testimony is contradicted by the weight of the evidence. (CCFF 2260).

Rambus's Response to Finding No. 2259:

Mr Geilhufe did testify that fixed burst length would involve extra design costs of $100,000 per part. Contrary to the proposed finding, Mr. Geilhufe's testimony is supported by the weight of the evidence. (RRFF 2260).

2260. The design costs of SDRAM lite with a fixed burst length would have been less than the design costs for an SDRAM part with programmable burst length. (Lee, Tr. 11018 ("Q. Mr. Lee, what was your understanding in the 1995 to 1996 time frame as to the cost of designing an SDRAM-Lite with fixed burst length as opposed to the cost of designing an otherwise identical SDRAM with programmable burst length? A. Our design effort would have been less for the fixed length part, and therefore, our design costs would have been less.")).

Rambus's Response to Finding No. 2260:

The proposed finding is irrelevant. The extra design costs referred to by Mr. Geilhufe stemmed from the requirement for multiple parts. (RPF 916). Moreover, the SDRAM lite proposal was not for a single fixed burst length part. (RRFF 572).

(B) Blowing Fuses to Set Burst Length.

2261. A manufacturer could hardwire a part with two burst length values. (Jacob, Tr. 5403). Either electrical or laser blown fuses could be used to select the burst length value for a part. (*Id.* 5403-04; DX0084-85).

Rambus's Response to Finding No. 2261:

The proposed finding is incorrect. Not all manufacturers could use electrically-blown fuses to select burst length because not all had this technology available. (Geilhufe, Tr. 9582, 9740-41). The dominant fuse technology among DRAM manufacturers in the mid-1990s was laser-blown fuses. (RPF 845).

2262. For example, a manufacturer could use either electrical or laser blown fuses to connect two different hardwired values for burst length to the burst length circuitry. (Jacob, Tr. 5403; DX0083). The manufacturer would blow one of the fuses to disable the connection. (*Id.*). Thereafter, the burst length circuitry would operate according to the hardwired burst length that was still connected to it. (*Id.*).

Rambus's Response to Finding No. 2262:

The proposed finding is incorrect. (*See* RRFF 2261).

2263. Using fuses to set the burst length is potentially cheaper to design, produce, and test than programmable burst length. (Jacob, Tr. 5404-05).

Rambus's Response to Finding No. 2263:

The proposed finding is incorrect. Complaint Counsel rely entirely on the testimony of Professor Jacob, who did not even attempt to quantify the cost increases and decreases associated with this (or any other) alternative. (Jacob, Tr. 5643-44). Mr. Geilhufe, who did do such an analysis, determined that the alternative of setting burst length using fuses would have led to a net cost increase of five cents per unit. (RPF 930-31).

2264. Using fuses to determine burst length would have preserved the degree of flexibility that a manufacturer has today to make one part that serves multiple applications. (Kellogg, Tr. 5131).

Rambus's Response to Finding No. 2264:

The proposed finding is incomplete. Preserving flexibility using fuses would have come at the increased cost identified by Mr. Geilhufe of five cents per unit. (RPF 930-31).

2265. In December 1991, JEDEC considered the use of fuses to determine a mode of operation that JEDEC ultimately decided to determine in the mode register. (JX0010 at 71; JX0056 at 114). Samsung proposed to use fuses to determine the burst type of a part. (JX0010 at 71).

Rambus's Response to Finding No. 2265:

The proposed finding is incomplete. The Samsung presentation was a first showing

(JX0010 at 5), and there is no evidence that it ever progressed beyond the first showing stage.

2266. In May 1992, JEDEC considered the use of fuses to choose between two different burst lengths, full page and 8, for an SDRAM part. (CX0034 at 149).

Rambus's Response to Finding No. 2266:

The proposed finding is misleading and incomplete. The referenced presentation by Cray did not involve simply a choice between two burst lengths, but, rather, two entire feature sets which included burst length. (CX0034 at 149). This would have yielded less flexibility that programmable burst length because the burst length could not be adjusted independently of the other features. Moreover, the Cray presentation was not even identified as a first showing in the minutes (CX0034 at 3-12), and there is no evidence that it ever progressed to even a first showing.

2267. Dr. Soderman testified that one of the disdavantages of using fuses to set burst length is that manufacturers would have to distribute a part with a specific burst length. (Soderman, Tr. 9370). The weight of the evidence indicates that this would not have been a significant issue for DRAM manufacturers. CCFF 2268.

Rambus's Response to Finding No. 2267:

The proposed finding is misleading and ambiguous because it is not clear whether it is referring to a single fixed burst length part or multiple fixed burst length parts. While it would not have been a significant issue for DRAM manufacturers to distribute a single fixed burst length part, a single fixed burst length part would have been unacceptable from a user standpoint. (RRFF 2239). Manufacturers could also have distributed multiple fixed burst length parts, but it would have resulted in the increased costs identified by Mr. Geilhufe. (RPF 927-32).

2268. In 1995-1996, JEDEC considered an SDRAM lite part with a fixed burst length. (JX0029 at 13; Lee, Tr. 6630, 6632). There was substantial support for a fixed burst length of 4. (*Id.*).

Rambus's Response to Finding No. 2268:

The proposed finding is misleading and incomplete. (*See* RRFF 2250).

2269. Dr. Soderman testified that he would raise the same technical points about the feasibility and reliability of fuses to discredit the use of fuses to set burst length as he raised to discredit the use of fuses to set CAS latency. (Soderman, Tr. 9370-71). The weight of the evidence indicates that manufacturers have used fuses reliably since the early 1990s and continue to use fuses today. (CCFF 2159, 2172-2177).

Rambus's Response to Finding No. 2269:

Dr. Soderman's testimony is supported by the weight of the evidence. (RRFF 2159, 2172-77).

(C) Using a Dedicated Pin to Set Burst Length.

2270. JEDEC could have dedicated a pin to holding the burst length value during system operation. (Jacob, Tr. 5405).

Rambus's Response to Finding No. 2270:

The proposed finding is incorrect. JEDEC could not have used a single dedicated pin because that would have allowed a choice between only two burst length values. Release 9 of JEDEC standard 21-C specified three required burst length values for SDRAMs as well as two optional values. (CX0234 at 150). SDRAMs are being produced that provide all five values. (RX 2100-13 at 1; Lee, Tr. 11078-80).

2271. The findings for using a dedicated pin to set CAS latency are applicable by extension to the use of a dedicated pin to set burst length. (Jacob, Tr. 5405-06 ("Q. Now, when you were discussing use of a pin, a dedicated pin, to determine CAS latency, I believe you described certain attributes, such as DC power, et cetera. Would those attributes also apply to the pin that you'd have in mind to determine burst length? A. Absolutely. The same -- the same conditions apply."); Geilhufe, Tr. 9599 ("Q. If we could go then to the next alternative, Burst Length Via Pins, is – is your understanding of how this alternative works similar to your understanding of how you would set CAS latency via pins? A. That is correct.")).

Rambus's Response to Finding No. 2271:

Rambus agrees that the same considerations generally apply to the alternatives of setting CAS latency using dedicated pins and setting burst length using dedicated pins.

2272. JEDEC could have used one dedicated pin to set one of two different burst length values. (CCFF 2213, 2291; Lee, Tr. 11025-26). JEDEC could have used a DC pin, which is less expensive than a data pin, to set the burst length. CCFF 2282-2283.

Rambus's Response to Finding No. 2272:

The proposed finding is incomplete and misleading. A single dedicated pin, allowing a choice of only two burst length values, would not have been sufficient. (RRFF 2239). Moreover, Mr. Geilhufe's testimony regarding the cost of the pins that would have been required for this alternative is uncontradicted.

2273. Using a pin to set the burst length is potentially smaller, cheaper to produce, and easier to test than programming the burst length in a mode register. (Jacob, Tr. 5405).

Rambus's Response to Finding No. 2273:

The proposed finding is incorrect. Complaint Counsel rely entirely on the testimony of Professor Jacob, who did not even attempt to quantify the cost increases and decreases associated with this (or any other) alternative. (Jacob, Tr. 5643-44). Mr. Geilhufe, who did do such an analysis, determined that the alternative of using dedicated pins to set burst length would have led to a net cost increase of two cents per unit, assuming that CAS latency was also being set with dedicated pins, and four cents per unit otherwise. (RPF 940-41).

2274. In December 1991, JEDEC considered the use of two dedicated pins to set burst length and burst type. (JX0010 at 74). Mitsubishi proposed an SDRAM that would use two pins, BT and WP, to program the burst length. (*Id.*; Kellogg, Tr. 5102). In its proposal, Mitsubishi provided for two burst length options, a burst length of 4 and 8. (JX0010 at 74).

Rambus's Response to Finding No. 2274:

The proposed finding is incomplete. The Mitsubishi presentation was designated as a "first time presentation." (JX0010 at 5). There is no evidence that it ever progressed beyond this stage.

2275. Before 1996, the use of a pin was viable from both a technical and cost perspective. (Kellogg, Tr. 5131-32).

Rambus's Response to Finding No. 2275:

The proposed finding is misleading and incomplete. Using a single pin, which could only select between two burst lengths, would not have sufficed. (RRFF 2239). Multiple pins could have been used, but the increased costs identified by Mr. Geilhufe would have been incurred. (RPF 940-41). Moreover, the alternative would not have avoided Rambus's intellectual property. (*See* RRFF 2300-03).

The evidence shows, moreover, that JEDEC members considered the alternative of using dedicated pins to be inferior to programmable burst length using a mode register. Mr. Kelley of IBM testified regarding the advantages of using pins to set burst length:

> I can't think of a lot of advantages compared to the programmable feature, which did not require a pin. I can think of the disadvantage that having a pin or using up a pin to do burst length selection was not a thing that we did easily, because once you use that pin up for a function, you don't have it available to you in the future for generation advance. As the memory densities increase, we need pins for more addressing of more address locations and those pins are very valuable for that feature, so this would have limited the number of generations of DRAM design

that we could have used if we were to use up this pin.

(Kelley, Tr. 2552-53).

Likewise, Mr. Kellogg, on whose testimony Complaint Counsel rely for this proposed finding, testified that IBM supported programmable burst length via a mode register over using dedicated pins because "[i]t offered us the greatest flexibility. We had a lot of applications." (Kellogg, Tr. 5132).

2276. Both Dr. Soderman and Mr. Geilhufe testified that the dedicated pin alternative would have required the addition of new pins to the DRAM package. (Soderman, Tr. 9371; Geilhufe, Tr. 9599-9600).

Rambus's Response to Finding No. 2276:

Dr. Soderman and Mr.Geilhufe did testify that the dedicated pin alternative would have required the addition of new pins to the DRAM package. Their testimony is supported by the weight of the evidence. (RRFF 2277-80).

2277. The dedicated pin alternative does not necessarily require the addition of new pins. CCFF 2192-2201.

Rambus's Response to Finding No. 2277:

The proposed finding is incorrect. (RRFF 2192-2201, 2278-80).

2278. JEDEC could have used a no-connect pin to implement this alternative. CCFF 2193-2196.

Rambus's Response to Finding No. 2278:

The proposed finding is incorrect and misleading to the extent that it suggests that the use of a no-connect pin is costless. First, Complaint Counsel concede that a number of SDRAM configurations did not have no-connect pins available. (RRFF 2191, 2196). Second, pins that are labeled "no connect" are not always available for other purposes. (RRFF 2191; RPF 873-75).

Third, even if there were a sufficient number of no-connect pins that were available to be used, this would simply mean that as pins became required in the future (e.g. for addressing more address locations in a larger memory), a larger package with more pins would become necessary sooner and the cost of the pins used up for setting burst length would be incurred at that point. (RRFF 2191; Kelley, Tr. 2552-53).

2279. If a no-connect pin was not available, JEDEC could have multiplexed a column address pin to implement this alternative. CCFF 2197, 2199-2201.

Rambus's Response to Finding No. 2279:

The proposed finding is misleading in indicating that this would be an "alternative." Professor Jacob testified to the use of dedicated pins as an alternative. Multiplexing a column address pin would not be "dedicated" because the same pin would be used for two different purposes, transmitting burst length information and column address information, at different times. In this case, since the burst length information would not always be available at the pins, it would have to be stored in a register. (RRFF 2199; Polzin, Tr. 4028-29). This is precisely what happens in SDRAMs currently: burst length information, received over pins that are used for other purposes at other times, is stored in a register called a mode register.

2280. If a no-connect pin was not available, JEDEC could have asserted a super-voltage level on a pin to define the burst length in order to implement this alternative. CCFF 2198.

Rambus's Response to Finding No. 2280:

The propose finding is not supported by the weight of the evidence. Asserting a super-voltage on a pin is not feasible. (RRFF 2198).

2281. This alternative would not necessarily require storage. CCFF 2206-2210.

Rambus's Response to Finding No. 2281:

The proposed finding is irrelevant. Rambus's patents covering synchronous memory devices with variable burst length do not depend on the burst length being placed in storage. (RRFF 2292).

2282. JEDEC could have dedicated a DC pin exclusively to holding the burst length value during a system's operation, which would have eliminated the need for storage entirely. CCFF 2207.

Rambus's Response to Finding No. 2282:

The proposed finding is irrelevant. (*See* RRFF 2281).

2283. Cost advantages are associated with the use of DC pins to set burst length. CCFF 2205. DC pins are less expensive that data pins. (*Id.*). They can also be placed in the less desirable locations of a chip package. (*Id.*).

Rambus's Response to Finding No. 2283:

Rambus has no specific response, except to point out that the Mr. Geilhufe's testimony regarding the cost of the pins that would be necessary to implement this alternative is uncontradicted.

2284. Even if JEDEC chose not to dedicate a DC pin exclusively to setting burst length, this alternative would still not require a register. CCFF 2208-2209.

Rambus's Response to Finding No. 2284:

The proposed finding is irrelevant. Rambus's patents covering synchronous memory devices with variable burst length do not depend on the burst length being placed in a register. (RRFF 2292).

2285. JEDEC could have multiplexed an existing pin, sharing it to set burst length and perform some other function. CCFF 2199-2201, 2208-2209. After the burst length was asserted on that pin, a latch could store the burst length value during system operation. (*Id.*). Although a latch is a type of storage, it is not a register. (*Id.*).

Rambus's Response to Finding No. 2285:

The proposed finding is irrelevant. (RRFF 2284). It is also incorrect. (RRFF 2208-09).

2286. Assuming that CAS latency and burst type are set by some other method than a mode register, this alternative would eliminate the mode register. (Jacob, Tr. 5406). It also eliminates the circuitry required to initialize the mode register. (*Id.*). This would make the part potentially smaller and therefore cheaper. (*Id.*).

Rambus's Response to Finding No. 2286:

The proposed finding is incorrect. The mode register in certain SDRAMs, and all DDR SDRAMs and DDR2 SDRAMs, is used for various purposes other than setting CAS latency, burst length, and burst type. (RRFF 2240).

2287. If there was both an insufficient number of no-connect pins and JEDEC could not multiplex exiting pins to implement the dedicated pin alternative, then adding pin(s) to implement this alternative might add cost. (Jacob, Tr. 5406-07). However, the cost of adding the kind of pin that would have been necessary to implement this alternative would not have been as significant as adding a data pin. (*Id.* ("Q. How significant would the cost increases have been had it been necessary to add an additional pin? A. Not -- as I said before, not as significant as adding a data pin because this would be a signal that would not be changing over -- it would not be changing dynamically, so it would be a DC value, it would be a simpler receiver, the pin could be in an undesirable location on the package, the pad could be in an undesirable location on the DRAM die, and much simpler to add this.")).

Rambus's Response to Finding No. 2287:

The proposed finding is incorrect and misleading. First, even if no connect pins were available, this would not be a costless solution because it would force the device into a larger, more expensive package sooner. (RRFF 2278). Second, multiplexing existing pins, far from "implement[ing] the dedicated pin alternative," by definition does not use dedicated pins; it is no different from what is done in SDRAMs now. (RRFF 2279). Third, whether the cost of adding dedicated pins for burst length would be greater or less than the cost of data pins is irrelevant because Mr. Geilhufe's testimony regarding the cost of the dedicated pins that would be

necessary to implement this alternative is uncontradicted.

2288. Mr. Geilhufe testified that adding fours pins would have been necessary in order to set the burst length via pins. (Geilhufe, Tr. 9599-9600). However, assuming that four pins had already been added to set the CAS latency, Mr. Geilhufe testified that setting burst length would then only require the addition of two more pins. (*Id.*). This testimony is contradicted by the weight of the evidence. (CCFF 2289-2291).

Rambus's Response to Finding No. 2288:

Contrary to the proposed finding, Mr. Geilhufe's testimony is supported by the weight of the evidence. (RRFF 2289-91).

2289. In 1995-1996, JEDEC considered adopting a part that operated with a single burst length of 4. (JX0029 at 13).

Rambus's Response to Finding No. 2289:

The proposed finding is incomplete. A single fixed burst length part was unacceptable from a user standpoint. (RRFF 2239). Moreover, the proposal cited in the proposed finding, SDRAM lite, was not a proposal for a fixed burst length part. (RRFF 572, 2250).

2290. JEDEC could have decided that it only needed two options for burst length. (*See* following proposed findings). Intel-compatible PCs use a burst length of 4. (Polzin, Tr. 3994). DRAM customers like AMD, however, use a burst length of 8. (*Id.*). Use of burst lengths of 1 and 2, however, have not been widespread. (Lee, Tr. 11014).

Rambus's Response to Finding No. 2290:

The proposed finding is not supported by the weight of the evidence. (RRFF 2254).

2291. JEDEC would only have needed one pin to support two different burst length options. (Lee, Tr. 11025-26).

Rambus's Response to Finding No. 2291:

The proposed finding is irrelevant. Two different burst length options would not have been acceptable. (RRFF 2254).

2292. Dr. Soderman testified that claim 1 of Rambus patent 6,324,120 (the '120 patent) covers the concept of using pins to determine burst length. (Soderman, Tr. 9371; *see* RX 2099-52 at 31). Dr. Soderman's testimony is contradicted by the weight of the evidence. (CCFF 2293-2295).

Rambus's Response to Finding No. 2292:

Dr. Soderman did testify that claim 1 of the '120 patent covers the concept of using pins to determine burst length. Dr. Soderman's testimony is supported by the weight of the evidence. (RPF 938-39). Unlike Rambus's '263 patent relating to storing a latency value in a register, claim 1 of the '120 patent contains a limitation that the synchronous memory device "receive block size information," but does not require that the information be stored. (RPF 938 (text of claim 1)). Thus, claim 1 covers receiving burst length information at dedicated pins, regardless of whether the information is stored in a register thereafter. (RPF 938-39).

Ultimately, however, this proposed finding is not relevant and the Court need not engage in an infringement analysis of the '120 patent. Complaint Counsel apparently argues that the '120 patent would not cover the dedicated pins alternative because it is limited to packetized systems. (CCFF 2295). But, if this were the case, then the '120 patent would not cover SDRAMs as they currently exist either. (CCFF 1306). In other words, current SDRAMs and the "dedicated pins" alternative do not differ in a material way so far as infringement of the '120 patent is concerned. It is stipulated between the parties that the '120 patent has been asserted by Rambus in litigation against DRAM manufacturers. (Parties First Set of Stipulations, Exh. A). Complaint Counsel has introduced evidence of alternatives to suggest that JEDEC members could have chosen paths that would have avoided Rambus's patent claims. Since SDRAMs and the "dedicated pins" alternative do not differ in a material way so far as infringement of the '120

patent is concerned, the use of dedicated pins would not have avoided Rambus's patent claims and, consequently, it is not an alternative at all.

2293. Dr. Soderman's testimony regarding the '120 patent is unreliable because Dr. Soderman did not present a proper claims analysis demonstrating that every element of the claim would be satisfied. (Soderman, Tr. 9456-57).

Rambus's Response to Finding No. 2293:

The proposed finding is incorrect. Dr. Soderman testified to his opinion, as a person of skill in the art, that claim 1 of the '120 patent covers the alternative of using dedicated pins to set burst length. Complaint Counsel have failed to introduce any contrary evidence and have suggested only that one limitation, the "operation code" of claim 1 is not satisfied. As set forth below, Complaint Counsel are incorrect. (RRFF 2295).

In any event, the proposed finding is irrelevant. (RRFF 2292).

2294. Dr. Soderman did not consult technical dictionaries, treatises or textbooks, or the expert reports in the private litigation to determine the ordinary meaning in the industry of the terms used in the patent. (Soderman, Tr. 9456-57).

Rambus's Response to Finding No. 2294:

The proposed finding is irrelevant. Dr. Soderman testified to his understanding of the claim terms as a person of skill in the art – he did not need to consult any extrinsic sources in order to do so. The proposed finding is also irrelevant for the reasons stated above. (RRFF 2292).

2295. Dr. Soderman's own interpretation of the term "operation code" to a portion of a packet signal limits the scope of claim 1 to Rambus's packetized system. (Soderman, Tr. 9456-57).

Rambus's Response to Finding No. 2295:

The proposed finding is incorrect. The cited testimony from Dr. Soderman simply refers

to the description of the preferred embodiment in the specification of the '120 patent where "operation code" is used in the context of a request packet. (Soderman, Tr. 9456-57). Dr. Soderman did not testify that claim 1 of the '120 patent was restricted to a packetized system. To the contrary, claim 1 itself defines "operation code" as simply a code that "instructs the memory device to perform a read operation." (RPF 938).

Moreover, other Rambus patents that do not refer to an "operation code," such as U.S. Patent No. 6,034,918, would cover this alternative. (*See* CCFF 1667-68; CX1525 at 29-30).

In any event, the proposed finding is irrelevant. (RRFF 2292).

(D) Identifying Burst Length in the Command.

2296. Identifying burst length in the command involves including burst length information in the command signal to initiate any operation. (Jacob, Tr. 5407). This would be similar to the method of identifying the CAS latency in the read command. (*Id.*).

Rambus's Response to Finding No. 2296:

Rambus has no specific response.

2297. JEDEC could have used one or more of the available command sets in the truth table to encode the burst length in the read command. (Jacob, Tr. 5408). The effect of implementing this alternative would be to have two or more different read commands, each encoding a different burst length within the command set. (*Id.*).

Rambus's Response to Finding No. 2297:

The proposed finding misrepresents the proposed alternative in its reference to "available command sets in the truth table." SDRAMs currently have a "command set" – that is, a correspondence between combinations of the five control signals and the commands that are to be performed by the DRAM in response to receiving those combinations. (Jacob, Tr. 5390). This correspondence is set forth in a so-called "truth table." (*See, e.g.*, JX0056 at 111-12).

Professor Jacob testified that certain combinations of command signals are not currently used to specify commands and that these unused combinations could be used to issue commands that encode the burst length values rather than storing the burst length in the mode register. (Jacob, Tr. 5407-08).

The proposed finding is also misleading in referring to encoding burst length in the command as an "alternative." This would not be an alternative to the use of Rambus technology, because it would still be covered by certain Rambus patents. (RRFF 2300).

2298. Assuming that CAS latency and burst type are set by some other means besides a mode register, identifying burst length in the command could potentially eliminate the mode register. (Jacob, Tr. 5408). It would also eliminate the circuitry necessary to initialize the mode register. (*Id.*). This could potentially make this alternative cheaper than programming burst length with a mode register. (*Id.*).

Rambus's Response to Finding No. 2298:

The proposed finding is incorrect. The mode register in certain SDRAMs, and all DDR SDRAMs and DDR2 SDRAMs, is used for various purposes other than setting CAS latency, burst length, and burst type. (RRFF 2240).

2299. This alternative would require that the circuitry within the chip that decodes command sets recognizes new read commands which identify the burst length. (Jacob, Tr. 5408). This could require more complex decode circuitry than currently exists to implement programmable burst length with a mode register. (*Id.*). However, the increased complexity in the decode circuitry would not be significant. (*Id.* 5407-08).

Rambus's Response to Finding No. 2299:

The proposed finding is also misleading in referring to encoding burst length in the command as an "alternative." This would not be an alternative to the use of Rambus technology, because it would still be covered by certain Rambus patents. (RRFF 2300).

2300. Dr. Soderman testified that claim 1 of Rambus patent 6,324,120 covers the

concept of identifying burst length in the read command. (Soderman, Tr. 9374; *see* RX 2099-52 at 31). Dr. Soderman's testimony is contradicted by the weight of the evidence. (CCFF 2301-2303).

Rambus's Response to Finding No. 2300:

Contrary to the proposed finding, Dr. Soderman's testimony is supported by the weight of the evidence. Claim 1 of the '120 patent covers synchronous memory devices that receive burst length information, whether it be encoded in a command or by some other method. (RRFF 2292). Moreover, the proposed finding is irrelevant for the same reasons stated above. (*Id*.)

2301. Dr. Soderman's testimony regarding the '120 patent is unreliable because Dr. Soderman did not present a proper claims analysis demonstrating that every element of the claim would be satisfied. (Soderman, Tr. 9456-57).

Rambus's Response to Finding No. 2301:

The proposed finding is incorrect and irrelevant. (*See* RRFF 2293).

2302. Dr. Soderman did not consult technical dictionaries, treatises or textbooks, or the expert reports in the private litigation to determine the ordinary meaning in the industry of the terms used in the patent. (Soderman, Tr. 9456-57).

Rambus's Response to Finding No. 2302:

The proposed finding is irrelevant. (*See* RRFF 2294).

2303. Dr. Soderman's own interpretation of the term "operation code" to a portion of a packet signal limits the scope of claim 1 to Rambus's packetized system. (Soderman, Tr. 9456-57).

Rambus's Response to Finding No. 2303:

The proposed finding is incorrect and irrelevant. (*See* RRFF 2295).

2304. Mr. Geilhufe testified that identifying burst length in the read command might require an additional pin and possibly two if the package needs to be balanced. (Geilhufe, Tr. 9580, 9596). His testimony is contradicted by the weight of the evidence.

Rambus's Response to Finding No. 2304:

Contrary to the proposed finding, Mr. Geilhufe's testimony is supported by the weight of the evidence. (*See* RRFF 2305).

2305. Identifying burst length in the command only requires defining a new command set and sending over wires to existing pins. (Jacob, Tr. 5407). It therefore does not require the addition of a new pin. (*Id.*).

Rambus's Response to Finding No. 2305:

The proposed finding is incorrect. Professor Jacob conceded that redefining the command set would require an additional pin to preserve the ability to issue simultaneous commands as in the current command set. (RRFF 2223).

(E) Burst Terminate.

2306. JEDEC could support two burst lengths, such as 4 and 8, with the burst terminate command. (Jacob, Tr. 5409-10).

Rambus's Response to Finding No. 2306:

The proposed finding is misleading and incomplete. First, two burst lengths would not have been acceptable. (RRFF 2254). Second, using the burst terminate command would have substantially degraded performance. (RRFF 2311). Professor Jacob's own study showed that his proposal of using a burst terminate command as an alternative to programmable burst length could lead to a 10-15% decrease in the efficiency of the system. (Jacob, Tr. 5604-06; RPF 953). Moreover, JEDEC participants agreed that the burst terminate command was "an internal device timing nightmare" (CX0415 at 10) and that using a burst terminate command would interfere with pipelining and, therefore, degrade the efficiency of the system (Polzin, Tr. 4038-40).

Indeed, the SDRAM standard includes an optional burst terminate command, while the

DDR SDRAM standard includes a limited form of a burst terminate command. (CX0234 at 161, 174; RPF 950). Despite the availability of these commands, both SDRAMs and DDR SDRAMs program burst length in a mode register. (CX0234 at 150).

2307. To implement the burst terminate alternative, a manufacturer could design a part to operate with a long burst length (e.g., burst length of 8). (Jacob, Tr. 5409-10). To effect a short burst length, the memory controller could send a read command before the longer burst length was completed. (*Id.*). So, for example, to effect a burst length of 4 in parts that are designed to operate with a burst length of 8, the memory controller would send a read command after the DRAM sent four bits of data onto the bus. (*Id.*). The read command would thereby terminate the burst length of 8. (*Id.*).

Rambus's Response to Finding No. 2307:

Rambus has no specific response.

2308. JEDEC's SDRAM and DDR SDRAM standards include a burst terminate command. (CX0234 at 161; JX0056 at 121 (reference to "interrupted bursts")).

Rambus's Response to Finding No. 2308:

The proposed finding is incomplete and misleading. The SDRAM standard an optional burst terminate command, while the DDR SDRAM standard included a mandatory, but limited, burst terminate command. (CX0234 at 161, 174).

2309. Implementation of the burst terminate command alternative would not require the addition of a pin. (Jacob, Tr. 5410-11).

Rambus's Response to Finding No. 2309:

Rambus has no specific response.

2310. This burst terminate command alternative could have potentially made the part a simpler to design, test, and manufacture. (Jacob, Tr. 5411-12).

Rambus's Response to Finding No. 2310:

The proposed finding is irrelevant. Since a burst terminate command was available in

SDRAMs and DDR SDRAMs, it is clear that designing, testing, and manufacturing a device with such a feature was technically feasible. (RRFF 2308). The fact that this command was available, but that burst length was nevertheless programmed in the mode register demonstrates that JEDEC members understood that the degradation of performance from using a burst terminate command as an alternative to programming burst length was unacceptable.

2311. Dr. Soderman testified that a cuing mechanism issue is associated with the burst terminate command. (Soderman, Tr. 9374-75). He testified that the burst terminate causes a wasted cycle when a write interrupts a read, which would degrade performance and cause problems with pipelining. (*Id.* 9374-76).

Rambus's Response to Finding No. 2311:

The proposed finding misrepresents Dr. Soderman's testimony. Dr. Soderman did testify that the burst terminate command causes a wasted cycle when a write interrupts a read which would degrade performance and cause problems with pipelining. (Soderman, Tr. 9374-76). He made no mention of queuing mechanisms, however. Professor Jacob testified on rebuttal that queuing mechanisms in controllers (which reorder the commands in a queue so that there will be fewer instances of writes interrupting reads) could alleviate this problem. (Jacob Tr. 11114 (misspelling "queuing" as "cuing")). Professor Jacob conceded, however, that such a queuing mechanism would not eliminate all of the inefficiency of using a burst terminate command to set burst length. (Jacob, Tr. 11126). Indeed, Professor Jacob's own study showed his proposal of using a burst terminate command as an alternative to programmable burst length could lead to a 10-15% decrease in the efficiency of the system. (Jacob, Tr. 5604-06; RPF 953). JEDEC participants agreed that the burst terminate command was "an internal device timing nightmare" (CX0415 at 10) and that using a burst terminate command would interfere with pipelining and,

therefore, degrade the efficiency of the system (Polzin, Tr. 4038-40).

2312. SDRAMs and DDR SDRAMs are already designed to handle wasted cycles. (Jacob, Tr. 11109-10). A wasted cycle is not a significant problem. (*Id.*). In DDR SDRAM, a wasted cycle already occurs every time a read follows a write or a write follows a read. (*Id.* 11110 ("[F]or example, if you look at current DDR protocols, whenever the bus is being handed off from one driver to another, from one bank to another or from the memory controller to a bank, so currently whenever you have a read followed by a write or a write followed by a read and some reads followed by other reads, you already have wasted cycles. That's the definition of the DDR protocol. So, [burst terminate] would introduce nothing more than that.")).

Rambus's Response to Finding No. 2312:

The proposed finding is misleading and incomplete. (*See* RRFF 2311).

2313. Mr. Geilhufe testified that it might not be possible to use the burst terminate command to effect a burst length of 1. (Geilhufe, Tr. 9598). This testimony is contradicted by the weight of the evidence. (CCFF 2314). Even if Mr. Geilhufe's testimony were true, it is not clear that it detracts from the viability of the burst terminate command as a technical and commercial alternative. (CCFF 2315).

Rambus's Response to Finding No. 2313:

Contrary to the proposed findings, Mr. Geilhufe's testimony is supported by the weight of the evidence. (*See* RRFF 2314). Moreover, the inability to provide for a burst length of 1 does detract from the viability of the burst terminate command as an alternative. (*See* RRFF 2315).

2314. Release 9 of JEDEC Standard 21-C, which includes the SDRAM and DDR SDRAM standards, provides for a burst terminate command that could effect a burst length of 1. (CX0234 at 161). JEDEC's SDRAM standards includes burst length of 1 as an optional burst length. (*Id.* at 150). It states that, "If the Burst stop command [also called Burst Terminate] is included in an SDRAM [ ], the following functionality is required: 1. BST applies to all burst lengths, including the optional full page burst length when included." (*Id.* at 161).

Rambus's Response to Finding No. 2314:

The proposed finding is incorrect and unsupported by the evidence. The statement in JEDEC standard 21-C that "BST applies to all burst lengths, including the optional full page burst length when included," plainly does *not* mean that the burst terminate command can be

used to effect a burst of any length; rather, it means that regardless of the burst length programmed into the mode register, the burst terminate command can be used. The latter is the only reasonable reading; otherwise, the statement that BST applies to . . . the optional full page burst length," the longest burst length available, would be nonsensical.

Mr. Geilhufe's testimony that burst terminate could not be used to achieve a burst length of 1 is uncontradicted. (RPF 951).

2315. Burst length of 1 is used infrequently, if at all, in the DRAM market. (Lee, Tr. 11014).

Rambus's Response to Finding No. 2315:

The proposed finding is not supported by the evidence. Mr. Lee, on whose testimony Complaint Counsel rely for this finding, did *not* testify that burst length of 1 is used infrequently in the DRAM market. Rather, Mr. Lee testified only that he was "not aware of it being used in main memory." (Lee, Tr. 11014). Mr. Lee admitted that burst lengths of 1 were used in graphics applications. (Lee, Tr. 11076). Furthermore, even Mr. Lee's testimony regarding the use of burst length 1 in main memory is suspect, since Mr. Lee was incorrect about the use of CAS latency 1. (*See* RRFF 2253).

2316. Dr. Soderman testified that DDR II limits the use of burst terminate to terminating a burst length of eight to get a burst length of 4 because of timing difficulties. (Soderman, Tr. 9376-77). Whether or not Dr. Soderman's testimony is true does not detract from the viability of burst terminate as an alternative to programmable burst length. (CCFF 2317-2318).

Rambus's Response to Finding No. 2316:

The proposed finding misrepresents Dr. Soderman's testimony. Dr. Soderman testified that timing difficulties led DDR2 SDRAM to limit the use of burst terminate not only in the way specified in the proposed finding, but also so that read commands could not interrupt write

commands and vice versa. (Soderman, Tr. 9377; RPF 957). These limitations plainly would detract from the viability of burst terminate as an alternative to programmable burst length, since, unlike programmable burst length, burst terminate would simply not be available in certain situations to stop the burst at the desired length.

2317. Burst lengths of 1 and 2 are used infrequently, if at all, in the DRAM market. (Lee, Tr. 11014).

Rambus's Response to Finding No. 2317:

The proposed finding is not supported by the evidence. Mr. Lee, on whose testimony Complaint Counsel rely for this finding, did *not* testify that burst lengths of 1 and 2 are used infrequently in the DRAM market. Rather, Mr. Lee testified only that he was "not aware" of these burst lengths being used in main memory. (Lee, Tr. 11014). Mr. Lee admitted that burst lengths of 1 and 2 were used in graphics applications. (Lee, Tr. 11076). Furthermore, even Mr. Lee's testimony regarding the use of burst lengths of 1 and 2 in main memory is suspect, since Mr. Lee was incorrect about the use of CAS latency 1. (*See* RRFF 2253).

2318. JEDEC's decision to include a modified version of the burst terminate command in the DDR II standards confirms that the burst terminate command was a viable means of selecting between burst lengths of 4 and 8. { } (Macri, Tr. 4774, *in camera*). { } (*Id., in camera*). { } (*Id.* 4775, *in camera*) { } (*Id.* 4774, in camera) { }

Rambus's Response to Finding No. 2318:

The proposed finding is incorrect and not supported by the evidence cited. The modification of the burst terminate command in DDR2 SDRAMs restricts the command so that it cannot be used to terminate bursts in certain situations (i.e. when a read interrupts a write, and vice versa). (RRFF 2316). This means that, without programmable burst length, the lengths of certain bursts would simply continue to the maximum burst regardless of the desired burst length.

(F) Toggle CAS Pulse to Control Data Output.

2319. JEDEC could have toggled the CAS pulse to output data. (Jacob, Tr. 5411-12).

Rambus's Response to Finding No. 2319:

The proposed finding is not supported by the weight of the evidence. The alternative of toggling the CAS pulse to output data would not operate as Professor Jacob described it because the DRAM would not be able to determine whether a signal on the CAS line were intended to be a "toggle" that was part of a burst of data or a new command. (Soderman, Tr. 9378-79). Solving this problem would require expensive, sophisticated additional circuitry, not specified by Professor Jacob. (Soderman, Tr. 9379; RPF 962).

2320. Assuming that CAS latency and burst type were set by others means besides a mode register, toggling CAS to output data would have eliminated the mode register. (Jacob, Tr. 5412). It also would have eliminated the circuitry necessary to initialize the mode register. (*Id.*). This would have made the part "simpler, smaller, easier to test." (*Id.*).

Rambus's Response to Finding No. 2320:

The proposed finding is incorrect. The mode register in certain SDRAMs, and all DDR SDRAMs and DDR2 SDRAMs, is used for various purposes other than setting CAS latency,

burst length, and burst type. (RRFF 2240).

2321. There are no significant disadvantages to using the CAS pulse to control data output as compared to using a programmable mode register to control the burst length. (Jacob, Tr. 5412).

Rambus's Response to Finding No. 2321:

The proposed finding is incorrect. In addition, to the cost of the additional circuitry mentioned above (RRFF 2319), this alternative would not allow efficient interleaving between banks. (Soderman, Tr. 9379-80; RPF 963). Solving this problem would require three additional CAS lines as well as associated pins and circuitry. (*Id.*)

5. Alternatives to Dual Edge Clocking.

2322. In the 1991-1996 time frame, there were at least seven alternatives to dual edged clocking. (Jacob, Tr. 5416-17). JEDEC could have doubled the clock frequency instead of using both edges of the clock to double the data rate. (*Id.* 5416). Second, it could have interleaved on-chip banks. (*Id.*). Third, it could have interleaved banks at the module level. (*Id.*). Fourth, it could have increased the data width of the DRAM chip to double the data rate. (*Id.*). Fifth, it could have increased the data width at the module level. (*Id.*). Sixth, it could have used simultaneous bidirectional I/O. (*Id.*). Seventh, it could have used toggle mode DRAM. (*Id.*).

Rambus's Response to Finding No. 2322:

The proposed finding is incorrect. None of the proposed alternatives were viable alternatives to dual edge clocking. (RPF 990-1077; RRFF 2325-65).

2323. In 1990-1991, JEDEC considered using toggle mode DRAM. (CX0314 at 1; CX0315 at 1-3; CX0318 at 1; CX2431 at 1).

Rambus's Response to Finding No. 2323:

The proposed finding is misleading. The evidence cited indicates that, in 1990-91, IBM and Siemens made certain presentations regarding toggle mode DRAM and JEDEC considered standardizing the technology.

2324. In 1996-2000 time frame, JEDEC considered doubling the clock frequency of SDRAM in order to achieve double the data rate. (JX0031 at 64;CX0371 at 3; Lee, Tr. 6710-11; Kellogg, Tr. 5176-77). JEDEC also considered interleaving on-module banks. (CX0150 at 109-117; Kellogg, Tr. 5176-77).

Rambus's Response to Finding No. 2324:

The proposed finding is incomplete and misleading. With respect to JEDEC's consideration of doubling the clock frequency rather than using both clock edges, Mr. Lee wrote: "A single frequency clock is not practical. There is no real support yet for the higher freque ncy clock idea yet." (Lee, Tr. 11039, 11087-89).

The "interleaving on-module banks" proposal cited by Complaint Counsel was a first showing by Kentron. (CX0150 at 109-117). Kentron's subsequent motion to ballot its technology at JEDEC failed due to lack of a second. (CX0160 at 1). Kentron's technology was expensive and rejected by customers. (RPF 1012-17).

Mr. Kellogg testified that, in comparing dual edge clocking to these proposals at the time, IBM believed that dual edge clocking was "the simplest means of speeding up data transfer" which would "result in the least EMI concerns, for example, electromagnetic interference." (Kellogg, Tr. 5179).

(A) Single Edge Clock with Double Clock Frequency.

2325. Doubling the clock frequency would require keeping the single-edged clocking scheme used in SDRAM but with a faster clock that would output data on the positive edges fast enough to achieve the desired data rate. (Jacob, Tr. 5433 ("[Double the clock frequency] means using a single-edged clocking scheme and simply doubling that clock, at least for read commands, and doubling the data bandwidth as well.")).

Rambus's Response to Finding No. 2325:

Rambus has no specific response.

2326. Use of a single edge clock operating at double the frequency of a dual edge clock could be accomplished in various ways. A faster single edge clock could be run throughout the entire system (a faster system clock) or the system clock could run at the same speed throughout the system and then be doubled by means of a clock splitter on the DRAM. (CX0371 at 3).

Rambus's Response to Finding No. 2326:

Rambus has no specific response.

2327. Use of dual edge clocking involves certain technical difficulties. Dual edged clocking requires something close to a 50% duty cycle. (Jacob, Tr. 5422; Williams, Tr. 836-837; Sussman, Tr. 1371; Lee, Tr. 6802; { }). It also requires relatively symmetric slew rates. (*Id.*). A 50% duty cycle means that the positive edge, or high voltage state of the clock signal, takes up half a clock cycle and the negative edge, or the low voltage signal state, takes the remaining half of the cycle. (Jacob, Tr. 5422; *see* DX0090; Kellogg, Tr. 5181; Williams, Tr. 836; { }). Symmetric slew rates means that it takes as much time to go from a low to a high signal state as it does to go from a high to a low signal state. (Jacob, Tr. 5422). { } (Macri, Tr. 4780, *in camera*). It is much easier to design and test a clock circuit that produces an asymmetric clocking scheme than a symmetric clocking scheme. (Jacob, Tr. 5424-45; *see* DX0090). { } (Macri, Tr. 4780, *in camera*).

Rambus's Response to Finding No. 2327:

The proposed finding is misleading, because using a double frequency single edged clocking scheme would involve greater technical difficulties. (*See* RRFF 2328).

2328. Use of a single edge clock with double the clock frequency would not require either a 50% duty cycle or symmetric slew rates. (Jacob, Tr. 5433; Kellogg, Tr. 5181-82; Williams, Tr. 836-837); { }, *in camera*). It is therefore an easier clocking scheme to design and test. (*Id.* 5424-25).

Rambus's Response to Finding No. 2328:

The proposed finding that it would be easier to design and test a single edged clocking scheme is not supported by the weight of the evidence. In fact, doubling the frequency of a single edge clock would lead to difficult problems of implementation due to power consumption,

clock distribution problems, and electromagnetic interference. (RPF 1045-47).

Indeed, Mr. Kellogg of IBM, on whose testimony Complaint Counsel rely, testified that dual edge clocking was "the simplest means of speeding up data transfer" compared to other possibilities (including doubling the frequency of a single edge clock, and would "result in the least EMI concerns, for example, electromagnetic interference." (Kellogg, Tr. 5179).

Moreover, a double frequency single edge clock was considered for DDR2 SDRAM in 2000 and consensus was reached that a "single data rate clock is preferred provided that we can make it work." (CX0426 at 4; RPF 1051). Apparently, it could not be made to work, because DDR2 SDRAM uses both clock edges. (RPF 1052).

2329. High speed clock chips would have been available to implement this alternative. Companies had made standard SDRAMs that could run at 250 mhz. (Wagner, Tr. 3871). By September 2000, 400 mhz clock chips were already available. (CX2769 at 13). Today, NVidia uses a specialized DDR2 SGRAM that operates with a 500 mhz clock chip. (Wagner 3837-38, 3845-46).

Rambus's Response to Finding No. 2329:

The proposed finding is irrelevant. The availability of high speed clock chips would not address the power, distribution and EMI problems of a high speed clock.

2330. What is and is not considered a very high speed signal changes over time. (Kellogg, Tr. 5182). In the 1996-97 time frame, signals that traveled at speeds of greater than or equal to 533 mhz were considered "very high speed signals." (Kellogg, Tr. 5182-83). Today, signals that are greater than or equal to 2.5 ghz are considered to be very high. (*Id.*).

Rambus's Response to Finding No. 2330:

The proposed finding is irrelevant. Mr. Kellogg, on whose testimony Complaint Counsel rely for this proposed finding, himself testified that dual edge clocking was the best alternative. (Kellogg, Tr. 5179).

2331. {

} (Macri, Tr. 4780, *in camera*).

Rambus's Response to Finding No. 2331:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 2328).

2332. In March 1996, JEDEC considered running a single-edged clock faster in order to double the data rate. (JX0031 at 64; Rhoden, Tr. 542-43). VLSI proposed using higher speed clocks to achieve data rates of up to 300 mhz. (*Id.*).

Rambus's Response to Finding No. 2332:

The proposed finding is unsupported by the evidence. The referenced presentation is not a proposal at all, much less a proposal for using higher speed clocks, but simply a prediction of what features might be used at future clock or bus speeds. (JX0031 at 64).

2333. In July 1997, JEDEC considered two different implementations of a single edge clock. (CX0371 at 3; Lee, Tr. 6710-11). TI made a presentation for two different versions of a single edged data rate clock. (*Id.*). In one version, TI proposed using a high speed clock throughout the entire system. (CX0371 at 3 (refer to the top drawing); Lee, Tr. 6712). It also proposed to use an on-chip clock frequency doubler to double the clock speed of the external clock signal. (CX0371 at 3 (refer to bottom drawing); Lee, Tr. 6712-13).

Rambus's Response to Finding No. 2333:

The proposed finding is incomplete. There is no evidence that this TI presentation ever progressed beyond this initial presentation. Mr. Lee's reaction to the TI presentation at the time was: "A single frequency clock is not practical. There is no real support yet for the higher frequency clock idea yet." (Lee, Tr. 11087-89).

2334. In 1996-97, using a single edge clock at double the frequency was a viable alternative. (Kelley, Tr. 5184-95; Lee, Tr. 6713 (The TI proposal to use an on-chip clock frequency doubler was technically feasible; TI's proposal to run a high speed clock throughout the entire system was technically feasible as well but would have required "changes to the bus topology to make it work at the data rates [TI] wanted to make it work at.")).

Rambus's Response to Finding No. 2334:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 2328).

2335. In 1996-97, using a single edge clock at double the frequency was acceptable from a cost perspective. (Lee, Tr. 6713-14 (Micron did not view TI's proposals for doubling the clock frequency as adding additional cost over existing proposals to use both edges of the clock; Both of TI's proposals represented acceptable alternatives to dual edged clock from a cost perspective.); *see also* Kellogg, Tr. 5185 (using a single edge clock might or might not incur some cost depending on how it was implemented)).

Rambus's Response to Finding No. 2335:

The proposed finding is not supported by the weight of the evidence. Complaint Counsel rely on Mr. Lee's testimony that the TI proposal for a double frequency single-edge clock was acceptable from a costs persepective ; however, at the time of the TI proposal, Mr. Lee wrote that it was "not practical." (Lee, Tr. 11087-89). Moreover, there is no evidence that Mr. Lee, or anyone at Micron, did any actual cost analysis. Mr. Geilhufe, who did perform a cost analysis, determined that the alternative of doubling the clock frequency would have led to a cost increase of 28 cents per unit.

2336. Dr. Soderman testified that doubling the clock frequency would create clock distribution problems. (Soderman, Tr. 9393). Dr. Soderman testified, further, that operating internal core circuitry twice as fast is difficult. (*Id.* 9394). This testimony is contradicted by the weight of the evidence. (CCFF 2337).

Rambus's Response to Finding No. 2336:

Contrary to the proposed finding, Dr. Soderman's testimony is supported by the weight of the evidence.

2337. Doubling the clock frequency does not require the internal core circuitry to operate twice as fast. (Jacob, Tr. 11114-15). Dr. Soderman misunderstands the alternative proposed by Professor Jacob. (*Id.*). In a high speed single-edged data rate scheme, nothing inside the DRAM runs any faster than it did before if only the data is designed to run with the higher speed clock. (*Id.*). In the clocking scheme that Dr. Jacob proposed, command and data run off a slower speed

system clock while data runs off a clock that runs at double the speed of the system clock. (*Id.* 11115 ("So, nothing runs any faster than it did before if you're going to compare it to DDR, for example.")).

Rambus's Response to Finding No. 2337:

The proposed finding is incomplete and mislead. Whether the alternative is implemented by running the internal circuitry at double speeed or not, the clock distribution and EMI problems would remain, since these are independent of the internal circuitry. (Soderman, Tr. 9393-95).

2338. When he reviewed TI's presentation on two different implementations for a high speed single-edged clock, Mr. Lee did not understand there to be any clock distribution problems associated with the proposal. (Lee, Tr. 11039-40).

Rambus's Response to Finding No. 2338:

The proposed finding is not supported by the weight of the evidence. Mr. Lee's current testimony is contradicted by his contemporaneous e-mail regarding the TI presentation which stated: "A single frequency clock is not practical. There is no real support yet for the higher frequency clock idea yet." (Lee, Tr. 11087-89).

2339. Dr. Soderman testified that doubling the clock frequency would increase electromagnetic radiation in a way that could run afoul with Federal Communication Commission ("FCC") guidelines. (Soderman, Tr. 9395). His testimony is contradicted by the weight of the evidence. (CCFF 2340-2341).

Rambus's Response to Finding No. 2339:

Contrary to the proposed finding, Dr. Soderman's testimony is supported by the weight of the evidence. (RRFF 2340-41).

2340. Soderman has no experience with FCC guidelines. He is not an expert in the FCC's regulation of electromagnetic interference. (Soderman, Tr. 9500). He does not have any individual experience in trying to comply with FCC guidelines. (*Id.*).

Rambus's Response to Finding No. 2340:

The proposed finding is misleading. Dr. Soderman testified that, while he was not an expert in FCC guidelines, he has reviewed materials by experts and that he personally has designed high speed clocks with electromagnetic interference problems. (Soderman, Tr. 9501).

2341. There are clocks that run very fast today, from 400 mhz up to over 2.5 ghz, that do not appear to run afoul of FCC guidelines. (CX2769 at 13; Kellogg, Tr. 5182).

Rambus's Response to Finding No. 2341:

The proposed finding is irrelevant because the issue is not what clock technology may be available today, but, rather, what was available at the time of DDR SDRAM standardization. Mr. Kellogg, whose testimony Complaint Counsel cite for this finding, testified that at that time there was a great deal of concern about electromagnetic interference problems from high speed clocks:

> Q. And again focusing on the time period you were considering these when they were being proposed at JEDEC, what, if any, did you understand to be the disadvantages of speeding up a single-edged clock?
>
> A. The predominant disadvantage was -- I think I mentioned EMI before. It's electromagnetic interference, radiation, the fact that fast pulses tend to radiate. And we've constantly been concerned, and at that time was no different, about our ability to distribute very high-speed signals throughout a system.

(Kellogg, Tr. 5182).

Moreover, the proposed finding is not supported by the evidence. Complaint Counsel cite a presentation by Terry Lee of Micron stating that "single data rate may be possible," and

noting that "400 MHz chips are already available." (CX2769 at 13). The presentation does not refer to FCC guidelines or indicate whether any testing whatsoever has been done to determine that operating those chips in a DRAM environment would comply with FCC guidelines. Moreover, the presentation is dated September 2000. Two months later, in November 2000, JEDEC members, including Mr. Lee, reached a consensus that a "single data rate clock is preferred provided that we can make it work." (CX0426 at 4; RPF 1051). Apparently, it could not be made to work, because DDR2 SDRAM uses both clock edges. (RPF 1052).

2342. Mr. Geilhufe testified that doubling the clock frequency would require an on-DIMM PLL/DLL. (Geilhufe, Tr. 9609). He estimated the cost of an on-DIMM PLL/DLL at $3.80 per unit. (*Id.* 9610). His testimony is contradicted by the weight of the evidence. (CCFF 2343).

Rambus's Response to Finding No. 2342:

Contrary to the proposed finding, Mr. Geilhufe's testimony is supported by the weight of the evidence. (RRFF 2343).

2343. Micron uses on-DIMM PLLs for its registered DIMMs to redistribute the clock to all of the DRAMs on the module. (Lee, Tr. 11040-42). {
} (Lee, Tr. 11179, *in camera*); *see also* Goodman, Tr. 6048-49 (a standard PLL generally costs around $1)).

Rambus's Response to Finding No. 2343:

The proposed finding is irrelevant. Mr. Geilhufe made clear that the cost of a PLL is a function of its frequency and can range from prices less than the amount he quoted up to as high as seven or eight dollars. (Geilhufe, Tr. 9609-10). Complaint Counsel have introduced no evidence that the price quotes that they obtained are for PLLs operating at the appropriate frequency.

(B) Interleaving On-chip Banks.

2344. There are two different ways to double the data rate by interleaving on-chip banks. (Jacob, Tr. 5418-20; *see* DX0089). This alternative assumes that each SDRAM has two internal banks. (*Id.*). One implementation of this alternative would be to send two read commands that are delayed from each other by half a clock cycle; one read command would be directed to bank 1 while the other read command would be directed to bank 2. (*Id.*). Another way to implement this alternative would be to send a clock and a delayed clock where the first clock would control bank 1 and the delayed clock would control bank 2. (*Id.*). Either implementation would result in two bits of data being sent across the bus per clock cycle. (*Id.*).

Rambus's Response to Finding No. 2344:

The proposed finding misrepresents Professor Jacob's description. In both implementations a first clock signal would go to one bank, and a second clock signal corresponding to the first clock signal delayed by half a cycle would go to the second bank. The difference between the two implementations is that in one case the delay would be caused by a delay element on the DRAM, while in the other case the delay would be inserted by the controller. (Jacob, Tr. 5419-20).

The proposed finding is also misleading in describing this as an "alternative," because it is covered by Rambus's patents. (RPF 995-98).

2345. An advantage to interleaving on-chip banks is that it does not require symmetric duty cyles or slew rates. (Jacob, Tr. 5424-25). It is possible to implement this alternative with asymmetric duty cycles and slew rates. (*Id.*).

Rambus's Response to Finding No. 2345:

The proposed finding is not supported by the weight of the evidence. In Professor Jacob's proposal the second clock is delayed by half a cycle from the first, as it must be for efficiency. (RRFF 2344; RPF 995). This means that the rising edge of the second clock occurs halfway through a cycle of the first clock – i.e. the rising edge of the second clock is where the

falling edge of the first clock would be if the first clock had a symmetric duty cycle. This alternative requires a multiplexer to drive data onto the bus first from one bank, on the rising edge of the first clock signal, and then from the other, on the rising edge of the second clock signal. (RPF 995). Since the only timing references available are the first and second clock signals, one of those timing references must be supplied to the multiplexer to control its switching between the banks, or a third clock must be added to control the multiplexer. (*Id.*) The clock that controls the multiplexer must have one edge, say the rising edge, correspond to the rising edge of the first clock and its other edge, in this case the falling edge, correspond to the rising edge of the second clock so that it can ensure that the multiplexer switches at the appropriate times – that is, the clock that drives the multiplexer must have a symmetric duty cycle. (*Id.*) In other words, this "alternative" would still require dual edge clocking since data will be output onto the bus on both the rising and falling edges of the clock driving the multiplexer.

This proposed finding is also irrelevant. Even if Professor Jacob's proposal did not require dual edge clocking, it would still not be an alternative because Rambus's patents are broad enough to cover this situation where two clock signals are used. (RPF 996-98).

2346. There would not have been any significant disadvantages to interleaving on-chip banks to double the data rate. (Jacob, Tr. 5425).

Rambus's Response to Finding No. 2346:

The proposed finding is not supported by the weight of the evidence. First, interleaving on-chip banks would have required both banks to remain active leading to significant increased power dissipation. (RPF 1000). Second, interleaving on chip banks would have resulted in

increased costs of six cents per unit. (RPF 1001-06).

2347. Interleaving on-chip banks would not necessarily require a multiplexor. (Jacob, Tr. 11136-37).

Rambus's Response to Finding No. 2347:

The proposed finding is not supported by the weight of the evidence. Dr. Soderman testified that a multiplexer would be required to switch between the banks. (Soderman, Tr. 9384). Professor Jacob asserted on rebuttal that a multiplexer was not required because he could design an output driver that would "inherent[ly]" sense when it should turn on and off without any kind of timing signal controlling its operation. (Jacob, Tr. 11136-37). This testimony by Professor Jacob was not reliable since Professor Jacob admitted that he had never designed such an output driver and could not name any examples of such an output driver. (Jacob, Tr. 11137, 11139).

This testimony is also irrelevant. Even if a multiplexer were not required (so that a dual-edge clock would not be required to drive the multiplexer), Rambus's patents are still broad enough to cover Professor Jacob's proposal that two clock signals be used. (RPF 996-98).

2348. Dr. Soderman testified that efficient implementation of this alternative would still use dual edged clock. (Soderman, Tr. 9386-87). Dr. Soderman testified that this alternative would require three clocks, clock, delayed clock, and a clock to guarantee the duty cycleë (*Id.*). Based on his conclusion that this alternative would require mulitple clocks, Dr. Soderman further testified that this would result in "significant overhead" and "increased power assumption." (*Id.*). This testimony is contradicted by the weight of the evidence. (CCFF 2349).

Rambus's Response to Finding No. 2348:

The proposed finding misrepresents parts of Dr. Soderman's testimony. Dr. Soderman's conclusion that interleaving on-chip banks would result in increased power dissipation was primarily based not on multiple clocks, but on the necessity of keeping two banks active

simultaneously. (RRFF 2346). Dr. Soderman's testimony that dual edge clocking and multiple clocks would be required is supported by the evidence. (RRFF 2345).

2349. Dr. Soderman's testimony assumes that it would be necessary to guarantee a 50% duty cycle to efficiently implement interleaving on-chip banks. (Jacob, Tr. 11117, 11119-20; *see* DX0358). This assumption is contradicted by the weight of the evidence. (CCFF 2327-2328, 2345). If it were necessary to use symmetric clocks to drive banks 1 and 2, then it would look like data is synchronous with the positive and negative edges of each clock. (Jacob, Tr. 11118-19). The clocks driving banks 1 and 2, however, can be asymmetric. (CCFF 2345). The use of asymmetric clocks to implement interleaving on-chip banks means that this alternative would only require the use of the positive edge of each clock and could differ significantly from dual edge clocking. (*Cf.* Jacob, Tr. 11118-20 with Jacob, Tr. 11120-21; *see also* DX0358).

Rambus's Response to Finding No. 2349:

Dr. Soderman's testimony that a 50% (*i.e.* symmetric) duty cycle would be required to efficiently implement interleaving on-chip banks is supported by the evidence. (RRFF 2345).

2350. JEDEC would have chosen asymmetric clocks in order to interleave on-chip banks. (Jacob, Tr. 11124 ("Because it's cheaper, it's easier to build, it's just a simpler design.").

Rambus's Response to Finding No. 2350:

The proposed finding is not supported by the weight of the evidence. A clock with a symmetric duty cycle would be required to efficiently implement this alternative. (RRFF 2345).

(C) Interleaving Banks on the Module.

2351. There are multiple DRAM chips on a module. (Jacob, Tr. 5426-27). Groups of DRAM chips can be organized into ranks of memory. (*Id.*). The positive edge of two clocks, clock and delayed clock, would drive the data from each rank of memory on a module in order to double the data rate. (*Id.*).

Rambus's Response to Finding No. 2351:

The proposed finding is incomplete. In order to accomplish the interleaving, expensive high speed switches would also be required. (RPF 1010).

2352. Interleaving banks on the module in order to double the data rate would have

simplified the design of DRAM chips. (Jacob, Tr. 5427).

Rambus's Response to Finding No. 2352:

The proposed finding is misleading. Professor Jacob testified that this alternative would have shifted some complexity from the DRAM chips to the module. (Jacob, Tr. 5427-28).

2353. In 1996-97, JEDEC considered interleaving SDRAM chips on the module in order to double the data rate. (Kellogg, Tr. 5177-78, 5783-86; *see also* CX0150 at 109-117 (Kentron made a proposal to JEDEC to interleave SDRAM chips on the module: "Operate each bank with its individual CLK . . . Provide/Sample data for every rising edge of both CLKs.")).

Rambus's Response to Finding No. 2353:

The proposed finding is incomplete. Kentron's subsequent motion to ballot its technology at JEDEC failed due to lack of a second. (CX0160 at 1). Kentron's technology was expensive and rejected by customers. (RPF 1012-17).

2354. This alternative would not have required asymmetric duty cycles or slew rates. (Jacob, Tr. 5428). JEDEC would have chosen asymmetric clocks to implement this alternative. (Jacob, Tr. 11124 ("Because it's cheaper, it's easier to build, it's just a simpler design.")).

Rambus's Response to Finding No. 2354:

The proposed finding is misleading in suggesting that JEDEC would have done anything with this technology. The technology was presented to JEDEC and soundly rejected. (RRFF 2354).

2355. Interleaving banks on the module would slightly increase the complexity of the module. (Jacob, Tr. 5428; Kellogg, Tr. 5185-86 ("That's relatively low cost, but that would still remain.")).

Rambus's Response to Finding No. 2355:

The proposed finding is incomplete and misleading in suggesting that a slight increase in the complexity of the module is the only disadvantage of this alternative. In fact, this alternative

would have required expensive high speed switches and related circuitry that would have added a cost of 25 cents per unit. (RPF 1010, 1012, 1020-21). Moreover, it would have led to a less flexible memory increment and would not be available for those DRAM applications that do not use modules. (RPF 1018-19). Finally, potential buyers who evaluated this technology were not convinced that it would work at all due to "signal integrity" issues. (RPF 1014-15).

(D) Increasing DRAM Width.

2356. JEDEC could have doubled the data rate by doubling the width of the data bus. (Jacob, Tr. 5429). With this alternative, JEDEC would not have had to increase the clock rate in order to increase the data rate and could have still used a single-edged clocking scheme. (*Id.*).

Rambus's Response to Finding No. 2356:

The proposed finding is incomplete. While doubling the width of the data bus could have been done, it would have resulted in substantially increased costs of 31 cents per unit. (RPF 1029-34). Moreover, the increased number of data pins could cause noise that would degrade performance. (RPF 1027).

2357. JEDEC would have only had to double the number of data pins on the DRAM in order to implement this alternative and add any necessary power and ground poins. (Jacob, Tr. 5429). It would not have had to add any command or address pins. (*Id.* 5429-30).

Rambus's Response to Finding No. 2357:

Rambus has no specific response.

2358. Increasing the number of pins on the DRAM in order to double the data rate would have required a far simpler clock circuit than dual edged clocking. (Jacob, Tr. 5430 ("Q. Now, what, if any, would have been the advantages had JEDEC chosen to increase the number of pins per DRAM rather than using a dual-edged clock? A. Again, you could retain the use of the single-edged clocking scheme, which means that you could use a far simpler clock circuit design. It would mean that your signals are transitioning at a slower rate than, for instance, a DDR-type interface, so rather than having a 200-megabit-per-second data pin, now you stick with a 100-megabit-per-second data pin, so the power of the DRAM actually goes down comparatively.")). Slower clock circuits and pins indicates that this alternative might consume

less power than dual edged clocking. (*Id.*). Increasing the number of pins would not have resulted in a significant increase in noise relative to dual edged clocking. (*Id.* 5430-31).

Rambus's Response to Finding No. 2358 :

The proposed finding is incomplete and misleading in suggesting that doubling the width of the data bus was an attractive alternative. In fact, doubling the width of the data bus would have resulted in substantially increased costs of 31 cents per unit. (RPF 1029-34). Contrary to the proposed finding, the increased number of data pins could cause noise that would degrade performance. (RPF 1027).

(E) Increase Pins on the Module.

2359. JEDEC could have doubled the data rate by doubling the number of data pins on the memory module. (Jacob, Tr. 5431). With this alternative, JEDEC would not have had to increase the clock rate in order to increase the data rate and could have still used a single-edged clocking scheme. (*Id.*). Further, JEDEC would not have had to increase the number of pins on the DRAM. (*Id.*).

Rambus's Response to Finding No. 2359:

The proposed finding is incomplete. This alternative would have substantially increased costs; indeed, Complaint Counsel's own economic expert determined that this alternative was *not* commercially viable. (McAfee, Tr. 7378). Moreover, this alternative would not be available in the many applications that do not use modules. (RPF 1019).

2360. There are advantages to increasing the number of pins on the module in order to double the data rate rather than dual edged clocking. (Jacob, Tr. 5431-32). It would have been a "far cheaper design to build and test." (*Id.*) Compared to DDR SDRAM, noise and power levels would have been reduced. (*Id.*).

Rambus's Response to Finding No. 2360:

The proposed finding is incomplete. Complaint Counsel's own expert determined that any advantages are so far outweighed by disadvantages that increasing the number of pins on the

module would not be commercially viable. (McAfee, Tr. 7378).

(F) Simultaneous Bidirectional I/O.

2361. Simultaneous bi-directional I/O could have been an alternative to dual edged clocking. (Jacob, Tr. 5435-36). It is a technology that allows reads and writes to be occurr simultaneously. (*Id.*). This would allow for more efficient bus utilization, which could improve the performance of the bus. (*Id.*).

Rambus's Response to Finding No. 2361:

The proposed finding is not supported by the weight of the evidence. Simultaneous bidirectional I/O would have been very expensive and difficult, if not impossible, to implement. (RPF 1063-64). Indeed, Rambus has considered using this technology for high speed signaling, but has not been able to implement it successfully. (RPF 1066). Moreover, even if it could be implemented, Professor Jacob concedes that it would not achieve the performance of DDR SDRAM except in the ideal case when read and write operations are perfectly balanced. (RPF 1065).

2362. Simulteaneous bi-directional I/O technology would have increased the data rate "without having to increase the speed of the system, so this would not increase the power consumption of the system. It would not increase the power consumption of the clock or power dissipation of the clock." (Jacob, Tr. 5436-37).

Rambus's Response to Finding No. 2362:

The proposed finding is incomplete and misleading. While it may be true that simultaneous bi-directional I/O technology would not have the particular disadvantage of increased power dissipation, it was not a viable alternative for various other reasons. (*See* RRFF 2361).

(G) Toggle Mode DRAM.

2363. JEDEC could have used IBM's toggle mode to double the data rate. (Jacob, Tr.

5416-17).

Rambus's Response to Finding No. 2363:

The proposed finding is not supported by the weight of the evidence. IBM's toggle mode DRAM was asynchronous (RRFF 509), and could not acheive the performance of synchronous DRAM technology (RPF 898-900). Indeed, an IBM researcher described IBM's toggle mode DRAM as "very big, very hot, and very nonstandard" and went on to note that "in the commodity market, these attributes are disastrous." (RX 2099-7 at 16; Soderman, Tr. 9399-9400). Moreover, the IBM toggle mode would have been an expensive alternative, increasing costs by approximately 13 cents per unit. (RPF 1072-77).

2364. Rambus does not consider toggle mode to be the same or similar to dual edged clocking. (Soderman, Tr. 9398; Geilhufe, Tr. 9610). Although Professor Jacob testified that it was an example of dual edged clocking, he included toggle mode DRAM on his list of alternatives to dual edged clocking because of Rambus's characterization. (Jacob, Tr. 5418; *see* DX0088).

Rambus's Response to Finding No. 2364:

The proposed finding is incomplete. In fact, Professor Jacob's opinion that IBM's toggle mode technology was the same as Rambus's technology is at odds not only with Rambus's opinion, but also with that of the Patent and Trademark Office. One of the patents that Rambus has asserted in litigation, U.S. Patent No. 6,378,020, has claims involving an implementation of dual edge clocking. (CX1540 at 30-31 (claim 1 includes limitations involving a first portion of data being output in response to a rising edge of a clock signal and a second portion of data being output in response to a falling edge)). The PTO issued this patent to Rambus even though it considered patents and articles relating to IBM's toggle mode DRAM. (*Id.* at 2 (citing Aichelmann, Jr. et al., U.S. Patent No. 4,845,664), 3 (citing H.L. Kalter et al., "A 50-ns 16Mb

DRAM with a 10-ns Data Rate and On-Chip ECC")).

2365. In 1990-1991, JEDEC considered IBM's toggle mode DRAM multiple times. (CX0314 at 1; CX0315 at 1-3; CX0251 at 1; CX0318 at 1).

Rambus's Response to Finding No. 2365:

The proposed finding is incomplete. Despite a number of presentations about it at JEDEC, it is not surprising that IBM's toggle mode was ultimately not pursued given its limitations. (RRFF 2363).

6. Alternatives to On-Chip PLL/DLL.

2366. In the 1991-1996 time frame, there were at least seven alternatives to the use of on-chip DLL in JEDEC SDRAM and DDR SDRAM. (Jacob, Tr. 5444-45; see also DX0094). Jedec could have decided not to use any method to align the system clock with data. (CCFF 2369, 2372). Second, JEDEC could have used either a PLL or DLL in the memory controller. (*Id.* 5444). Third, it could have put either a PLL or DLL on the module. (*Id.*). Fourth, it could have used a vernier circuits instead of a either a pll or dll circuit. (*Id.*). Fifth, if JEDEC had decided to increase the number of pins in order to increase performance, it could have avoided the use of on-chip DLL circuits. (*Id.*). Sixth, JEDEC could have decided to rely entirely on the DQS strobe and avoided the use of on-chip DLL circuits. (*Id.* 5445). Seventh, JEDEC could have adopted read clocks, which were sometimes referred to as echo clocks, in order to avoid replicating DLL circuits on each DRAM chip. (Lee, Tr. 6664, 6666-67).

Rambus's Response to Finding No. 2366:

The proposed finding is incorrect. None of the proposed alternatives were viable alternatives to on-chip PLL/DLL. (RPF 1078-1120; RRFF 2368-2414).

2367. In the 1994-1997 time frame, JEDEC considered five of these alternatives to on-chip DLL for incorporation into the JEDEC DDR SDRAM standard. (Kellogg, Tr. 5154-55 (JEDEC considered vernier circuits, DQS strobe, read clocks, and doing nothing at all); JX0031 at 71 (PLL on the controller); JX0036 at 64 (vernier circuits); CX0368 at 4 (rely on DQS strobe); JX0029 at 17 (echo clocks)).

Rambus's Response to Finding No. 2367:

The proposed finding is incomplete. An on-chip DLL or PLL was required for high

speed operation and this was generally recognized in the mid-1990s. (RRFF 2369). Not suprisingly, the alternatives to on-chip DLL that JEDEC did consider were rejected.

(A) Use No Method of Aligning Data to the System Clock.

2368. In JEDEC DDR SDRAM, on-chip DLL circuits are used to align the data valid window of each DRAM chip with the system clock. (Jacob, Tr. 5438-42; *see* DX0093; JX0029 at 17; Kellogg, Tr. 5154-55).

Rambus's Response to Finding No. 2368:

The proposed finding is misleading. In DDR SDRAMs, on-chip DLL circuits are used to align the data signals and data strobe output by each DRAM chip with the system clock. (JX0057 at 5 ("DLL aligns DQ and DQS transitions with CK transitions")).

2369. In working towards a DDR SDRAM standard, JEDEC considered not doing anything at all with respect to aligning the data with the clock. (Kellogg, Tr. 5155). When it did consider how to align the data with the clock, however, it considered using PLL/DLL circuits as a solution. (JX0029 at 17).

Rambus's Response to Finding No. 2369:

The proposed finding is misleading and misrepresents the evidence. While Mr. Kellogg did testify that, since "there was no effort to align data with the clock at the DRAM" for SDRAMs, this was the "starting point for consideration" of whether such an effort needed to be made for DDR SDRAMs. (Kellogg, Tr. 5155). There was, however, general recognition in the mid-1990s among JEDEC members that, as bus speeds increased, an on-chip PLL or DLL would become necessary. (Soderman, Tr. 9408-10; Rhoden, Tr. 546 ("I don't think we ever had any question whether we would use the technology [on-chip PLL or DLL]. It was just a question of when."); RX1040 ("Without them [DLLs] we won't get much beyond 125 MHz"); {

}).

2370. PLLs, or phase locked loops, and DLLs, or delay locked loops, are very similar circuits. (Jacob, Tr. 5443). The primary difference between them is that a PLL contains an oscillator and a DLL does not. (*Id.*).

Rambus's Response to Finding No. 2370:

The proposed finding is incomplete and misleading. PLLs are similar to DLLs in that they can be used for similar purposes in some applications. (Jacob, Tr. 5617). They are, however, different types of circuits: A PLL uses a voltage controlled oscillator while a DLL uses variable delay lines. (Jacob, Tr. 5616-17).

2371. In January 1996, JEDEC was debating two different objectives for future SDRAM clocking. (JX0029 at 17). JEDEC had been considering the use of PLL/DLL circuits to accomplish the objective of aligning the read data to the system clock. (*Id.*). In 1996, however, Micron questioned the wisdom of replicating PLL/DLL circuits in every DRAM in the system. (JX0029 at 18). Micron recommended shifting the focus of future SDRAM clocking towards ensuring that read data capture occurred during the data valid windows. (*Id.* at 17, 20).

Rambus's Response to Finding No. 2371:

The proposed finding is misleading to the extent that it suggests that there was any actual proposal to include on-chip PLL/DLL in future SDRAMs in the January 1996 timeframe. Complaint Counsel rely on a January 1996 Micron presentation which states that "PLL/DLL circuits are being considered." There is no evidence that this is anything but a reference to a survey ballot, the results of which had been presented at a JEDEC meeting the previous month, which included a question regarding whether on-chip PLLs or DLLs should be included in future SDRAMs. (JX0028 at 35).

The proposed finding is also misleading in suggesting that Micron wanted to "shift[] the

focus of future SDRAM clocking towards ensuring that read data capture occurred during data valid windows" – the whole point of on-chip PLLs and DLLs is to ensure that data is captured during data valid windows. (RPF 1079-82).

2372. In 1996-1997, JEDEC did not need to perfectly align the data with the system clock for high speed DRAM operation. (Jacob, Tr. 5442-43; Lee, Tr. 6662-63; Kellogg, Tr. 5161).

Rambus's Response to Finding No. 2372:

The proposed finding is misleading. As the testimony cited by Complaint Counsel makes clear, it is generally the case, in 1996-97 and during all other time periods, that data need not be "perfectly align[ed]" with the system clock for high speed DRAM operation. (Jacob, Tr. 5442-43; Lee, Tr. 6662-63; Kellogg, Tr. 5161). The issue is whether the data is sufficiently closely aligned to the clock to allow for the data to be read correctly. (*Id.*) There was general recognition in the mid-1990s that, as bus speeds increased, an on-chip PLL or DLL would become necessary to ensure that data was sufficiently closely aligned to the clock to allow for the data to be read correctly. (RRFF 2369).

2373. What was necessary, in 1996-1997, was to design a system that guaranteed that the memory controller would capture data during the data valid window. (Jacob, Tr. 5442-43; Lee, Tr. 6662-63; Kellogg, Tr. 5154-55, 5161).

Rambus's Response to Finding No. 2373:

The proposed finding is misleading to the extent that it suggests that data could be reliably captured during the data valid window (i.e. read) for high bus speeds without an on-chip PLL or DLL. (*See* RRFF 2372).

2374. The problem of guaranteeing high speed data capture stems from the fact that it takes time to propagate signals through a memory system. (Jacob, Tr. 5438-39). There are three kinds of signal propagation delays: outbound, internal, and return. (*Id.*; *see* DX0093). At high

rates of speed, it becomes necessary to mitigate the effect of some of the timing uncertainties that result from these propagation delays. (*Id.*). On-chip PLL/DLLs cancel out some of the internal chip delays in a system that can cause the data valid window to vary. (*Id.* 5442-43).

Rambus's Response to Finding No. 2374:

Rambus has no specific response.

2375. There are five different types of skew that can cause the data valid window to vary: (1) clock skew to DRAMs; (2) on-chip skew (DRAMs); (3) chip-to-chip skew (DRAMs); (4) data path skew after DRAMs; (5) memory configuration skew (minimal populated vs. maximally populated). (JX0029 at 20; Lee, Tr. 6655-61 (explaining each of the five components of skew)).

Rambus's Response to Finding No. 2375:

Rambus has no specific response.

2376. On-chip PLL/DLL primarily improves the third component of skew, which is the skew between DRAM chips in a system. (Lee, Tr. 6663).

Rambus's Response to Finding No. 2376:

The proposed finding is not supported by the weight of the evidence. Professor Jacob, Complaint Counsel's own technical expert, testified that an on-chip DLL would also rectify "on-chip delay," that is, the second component of skew identified. (Jacob, Tr. 5442-43).

2377. Using an on-chip PLL/DLL is one way to facilitate valid data capture. (Kellogg, Tr. 5154-56).

Rambus's Response to Finding No. 2377:

The proposed finding is misleading to the extent that it suggests that there were other viable alternatives to ensure valid data capture at high speeds; there were not. (RPF 1078-1120).

2378. In January 1996, Micron proposed a new clocking scheme that would use echo clocks to control the variation in data valid windows. (JX0029 at 17, 20). It would not replicate PLL/DLL circuits in every DRAM in the system. (*Id.* 18). Micron would later propose the use of a data strobe, which is slightly different than the echo clock concept, for data capture in DDR SDRAM. (CX0368 at 4; Lee, Tr. 6666-67).

Rambus's Response to Finding No. 2378:

The proposed finding is misleading and incomplete. Micron's presentation regarding echo clocks was in a presentation on "future SDRAM clock issues." (JX0029 at 4). Unlike specific proposals that are designated as a "first showing" or a "second showing," Micron's presentation was designated simply as a "first presentation." (*Id.*) There is no evidence that Micron's presentation regarding echo clocks ever progressed beyond the first presentation stage.

It is unclear where, or to whom, Micron's proposal regarding the use of a data strobe was made – the proposal is dated April 3, 1997 which is not the date of a JC-42.3 subcommittee meeting.

2379. In 1996-1997, JEDEC members considered not using an on-chip DLL and instead relying on the data strobe to ensure valid data capture. A majority of JEDEC members agreed that on-chip DLL could be eliminated if a data strobe were used to capture data. (Lee, Tr. 6682-83). JEDEC could not, however, reach a consensus in favor eliminating on-chip DLL. (*Id.*). A compromise was struck to include both the data strobe and on-chip DLL in the DDR standard in order to allow for those few companies who wanted to use DDR parts in applications that would not rely on a data strobe. (*Id.*).

Rambus's Response to Finding No. 2379:

The proposed finding is not supported by the weight of the evidence. Complaint Counsel rely entirely on Mr. Lee's testimony that a majority of JEDEC members agreed that on-chip DLL could be eliminated if a data strobe were used to capture data. However, the evidence shows that there was general recognition that an on-chip PLL or DLL would be required at high bus speeds. (*See* RPF 1082-85.) {

}

(RX1086 at 1 (*in camera*)).

Hans Wiggers of Hewlett-Packard expressly addressed the viability of relying on the data strobe in a November 6, 1997 e-mail in which he explained "why I think they [DLLs] are essential." (RX1040). Mr. Wiggers noted that while "strobes do help," they are insufficient and concluded that without DLLs "we won't get much beyond 125 MHz." (*Id*.)

The Synclink consortium's SLDRAM design also included a data strobe. (RX0911 at 3 (noting that SLDRAM would have data strobe and dual edge clocking like DDR, but would add packet-based protocol)). Like complaint counsel here, the Synclink consortium "claim[ed] that the strobe mechanism avoids the need for PLLs/DLLs." (CX0711 at 72). However, despite the existence of the data strobe and their stated desire to avoid an on-chip PLL or DLL, the Synclink Consortium ultimately did add an on-chip DLL. (RPF 1109-10).

2380. In 1996-1997, numerous mechanisms were available besides on-chip PLL/DLL to facilitate valid data capture. (Jacob, Tr. 5443; Kellogg, Tr. 5154-55, 5162; *see* DX0059; CX2109 at 67-68 (based on internal discussions at Rambus, Davidow concluded that there were "many ways to improve performance" without using an on-chip DLL)).

Rambus's Response to Finding No. 2380:

The proposed finding is not supported by the weight of the evidence. The alternatives proposed by Professor Jacob, as well as the ones considered by JEDEC, were not viable. (RPF 1078-1120). Indeed, the very fact that certain alternatives were considered, and rejected, by JEDEC indicates that they were considered not to be viable or, at a minimum, to be inferior solutions. The cited testimony of Mr. Davidow, based on his vague recollections, of conversations at Rambus is not reliable. For example, Mr. Davidow recalled some discussion of moving the DLL off the chip (CX2109, Davidow FTC depo., at 65-66). But Mark Horowitz, to

whom Mr. Davidow deferred (*id*. at 66-67) and who was actually involved in such efforts at Rambus, testified that Rambus was unable to move the DLL off the chip and still meet the necessary timing requirements. (Horowitz, Tr. 8561-62).

(B) DLL in the Memory Controller.

2381. The memory controller could use a DLL circuit to "make sure that all of the DRAMs are in sync with each other rather than [having] each DRAM do[ ] [that] on its own." (Jacob, Tr. 5445).

Rambus's Response to Finding No. 2381:

The proposed finding is not supported by the weight of the evidence. A DLL on the controller would not be sufficient for high speed operation because it could not account for timing differences between the DRAMs. (RPF 1089). Rambus has actually tried to move the DLL off the DRAM and onto the controller, but found that it could not be done while meeting the necessary timing requirements. (RPF 1090).

2382. If the DLL circuit were in the memory controller, it could potentially eliminate outbound, internal chip, and return delays. (Jacob, Tr. 5446).

Rambus's Response to Finding No. 2382:

The proposed finding is incomplete. A DLL on the memory controller would not be able to account for timing differences between DRAMs and, therefore, is not sufficient for high speed operation. (RRFF 2381).

2383. This alternative would eliminate DLL circuitry in the DRAM. (Jacob, Tr. 5446-47). As a result, the DDR SDRAM would consume less power and have lower test costs. (*Id.*). It would also reduce the die size of the part, which would lower manufacturing costs. (*Id.*).

Rambus's Response to Finding No. 2383:

The proposed finding is incomplete. It was precisely in order to eliminate DLL circuitry

that Rambus tried to move the DLL off the DRAM and onto the controller; however, Rambus found it could not be done and still meet the necessary timing requirements. (Horowitz, Tr. 8561-62).

2384. In March 1996, JEDEC considered the use of a PLL in the memory controller instead of every DRAM chip in the system for future SDRAM. (JX0031 at 71; Rhoden, Tr. 513-514; Lee, Tr. 6691). Samsung proposed taking the PLL circuit off the DRAM chip and place it inside of the memory controller in order to generate a phase-shifted read clock that the memory controller would use to sample data off both of the read clock's edges. (Lee, Tr. 6691).

Rambus's Response to Finding No. 2384:

The proposed finding is incomplete. The Samsung presentation on "future SDRAM concepts" is not identified in the minutes as either a first showing or second showing, but simply as a "presentation." (JX0031 at 9). There is no evidence that the Samsung presentation ever progressed any further.

(C) DLL on the Module.

2385. DDR SDRAM could have used either a single or multiple DLLs on the module to ensure that each DRAM chip on the module was in sync with the system clock. (Jacob, Tr. 5448). The internal delay could thereby be accounted for. (*Id.*).

Rambus's Response to Finding No. 2385:

The proposed finding is incomplete. A single DLL on the module would have been insufficient for high speed operation, because it could not account for timing differences between individual DRAMs. (RFP 1094). Indeed, Professor Jacob concedes as much, while quibbling about the speed at which a single DLL would be insufficient. (Jacob, Tr. 5449 ("if you envision going to much higher rates of speed, you could require a separate DLL per DRAM on the module")). This would have led to significantly higher costs. (RPF 1095-1102; Landgraf, Tr. 1709 (having DLLs on individual DRAMs rather than on the module "reduces the overall

cost of the system and also improves the performance of the system")).

2386. This alternative would eliminate DLL circuitry in the DRAM, "thereby reducing its power consumption, reducing its cost, reducing the design time. (Jacob, Tr. 5450).

Rambus's Response to Finding No. 2386:

The proposed finding is incomplete and misleading. While the certain DRAM related costs would have been reduced, the costs associated with the DLL on the module would have led to a net increase in cost of 21 cents per unit. (RPF 1097-1102).

2387. Mr. Geilhufe testified that it would cost $3.80 to pay for the DLL circuit necessary to move the DLL onto the module. (Geilhufe, Tr. 9613). This testimony is contradicted by the weight of the evidence. CCFF 2388..

Rambus's Response to Finding No. 2387:

Contrary to the proposed finding, Mr.Geilhufe's testimony is supported by the weight of the evidence. (*See* RRFF 2388).

2388. Micron uses on-DIMM PLLs for its registered DIMMs to redistribute the clock to all of the DRAMs on the module. (Lee, Tr. 11040-42). { } (Lee, Tr. 11179, *in camera*); *see also* Goodman, Tr. 6048-49 (a standard PLL generally costs around $1.00)).

Rambus's Response to Finding No. 2388:

The proposed finding is irrelevant. Mr. Geilhufe made clear that the cost of a PLL is a function of its frequency and can range from prices less than the amount he quoted up to as high as seven or eight dollars. (Geilhufe, Tr. 9609-10). Complaint Counsel have introduced no evidence that the price quotes that they obtained are for PLLs operating at the appropriate frequency.

_____(D) Verniers.

2389. A vernier circuit is a circuit that can introduce a static amount of delay on a signal

in order to reduce timing uncertainties in a memory system. (Jacob, Tr. 5450). JEDEC could have used a vernier circuit in every DRAM in order to eliminate internal chip delays. (*Id.* 5451). If it were necessary to compensate for dynamic changes in skew, the memory controller could have periodically recalibrated each vernier circuit. (*Id.* 5452-43).

Rambus's Response to Finding No. 2389:

The proposed finding is not supported by the weight of the evidence. A vernier could not be used in place of a DLL because, since a vernier introduces a static delay, it cannot account for dynamic changes in skew. (RPF 1106-07). Professor Jacob's proposed solution to this problem – to have the memory controller periodically recalibrate the vernier – would impair the efficiency of the system. (RPF 1108). Indeed, the Synclink consortium tried to design a high speed DRAM that used verniers alone to account for skew, but ultimately found that they had to include an on-chip DLL. (RPF 1109-10; *see also* JX0026 at 97 (May 1995 SyncLink presentation stating "Avoid using PLL in DRAM components")).

2390. On-chip verniers could have potentially eliminated all three types of delays: outbound, internal, and return. (Jacob, Tr. 5451). Vernier circuits would have been easier to design than DLLs. (*Id.*).

Rambus's Response to Finding No. 2390:

The proposed finding is misleading to the extent that it suggests that on-chip verniers could have accounted for skew to a sufficient extent to permit high speed operation. On-chip verniers could not have replaced on-chip DLLs in this respect. (RRFF 2389).

2391. In January 1997, JEDEC considered the benefits of vernier circuits to control the problem of skew in high speed DRAMs. (Kellogg, Tr. 5154-55; CX0367 at 3 ("The inclusion of the vernier in the memory for read data timing manipulation is good for all but the simple one memory device system.")).

Rambus's Response to Finding No. 2391:

The proposed finding is incomplete. Complaint Counsel cites a presentation touting the

use of verniers in Synclink's SLDRAM. (CX0367 at 3). However, as Professor Jacob concedes, Synclink was ultimately forced to add an on-chip DLL to the SLDRAM. (RPF 1110; Jacob, Tr. 5620-21).

2392. In March 1997, JEDEC considered the use of on-chip vernier circuits. (JX0036 at 58, 64). Desi Rhoden, from VLSI, gave a presentation on DDR SDRAM clocking that included a slide showing SLDRAMs with vernier circuits. (*Id.*).

Rambus's Response to Finding No. 2392:

The proposed finding is incomplete. While Mr. Rhoden did give a presentation in March 1997 showing SLDRAMs with vernier circuits, ultimately, Synclink had to add an on-chip DLL to the SLDRAM. (RPF 1110).

2393. Dr. Soderman testified that vernier circuits were not a viable alternative to on-chip DLLs, in part, because they could not account for temperature and voltage variations on the DRAM. (Soderman, Tr. 9411). He further testified that recalibration of the vernier is not sufficiently precise and consumers bandwidth. (*Id.* 9412). This testimony is contradicted by the weight of the evidence. (CCFF 2394-2399).

Rambus's Response to Finding No. 2393:

Contrary to the proposed finding, Dr. Soderman's testimony is supported by the weight of the evidence. (*See* RRFF 2394-99).

2394. Mr. Lee testified that, in the 1996-1997 time frame, he considered verniers to be a viable technical and commercial alternative to on-chip DLLs. (Lee, Tr. 6676-77). Mr. Lee further testified that he understood verniers to have certain advantages compared to on-chip DLL. (*Id.* 6677). For example, verniers did not require the lock time that was necessary to initialize the DLL. (*Id.*). Also, Mr. Lee testified that at the time he did not believe it was necessary to replicate vernier circuits in every DRAM but instead one vernier circuit could be used in the memory controller. (*Id.*). Using a single vernier circuit in the memory controller would have reduced the cost and complexity of DRAM. (*Id.*).

Rambus's Response to Finding No. 2394:

Mr. Lee's testimony is not supported by the weight of the evidence. The evidence shows

that there was general recognition in the 1996-97 time frame that an on-chip PLL or DLL would be required at high bus speeds. (*See* RRFF 2369.) {

} (RX1086 at 1 (*in camera*)).

2395. Some IBM systems were using memory busses with vernier circuits instead of DLL circuits. (Kellogg, Tr. 5161-62). For example, the z900 memory card had a vernier circuit. (*Id.*). Mr. Kellogg believed that vernier circuits were the optimal solution to the data capture issue. (Kellogg, Tr. 5168).

Rambus's Response to Finding No. 2395:

The proposed finding that certain IBM systems with memory busses were using vernier circuits is irrelevant without some evidence of the speed of those busses. It is undisputed, and not material, that, at sufficiently low bus speeds, a DLL is not required.

The finding that Mr. Kellogg believed that vernier circuits were the optimal solution to the data capture issue is incomplete. Mr. Kellogg testified that he supported verniers, but *also* supported on-chip PLL/DLL because it "helped further." (Kellogg, Tr. 5168-69.) This suggests that, as the Synclink consortium ultimately decided, the best solution involved both a vernier *and* an on-chip DLL (RPF 1110); it does not support the conclusion, and Synclink apparently determined to the contrary, that a vernier alone was sufficient for high speed operation.

2396. In the 1995-1998 time frame, IBM assessed the data capture problem. (Kellogg, Tr. 5157). It looked at all the elements associated with data capture, and concluded that the vernier compensated for the largest portion of those elements. (*Id.*).

Rambus's Response to Finding No. 2396:

The proposed finding is incomplete. While IBM may have concluded that the vernier was sufficient up to certain bus speeds, there is no evidence that it believed that higher speed operation would not require an on-chip DLL or PLL. To the contrary, there was general recognition that, eventually, an on-chip DLL or PLL would be required. (RRFF 2369).

2397. IBM promoted the use of vernier circuits at JEDEC meetings. (Kellogg, Tr. 5154-55).

Rambus's Response to Finding No. 2397:

The proposed finding is incomplete. First, this indicates no more than that IBM believed that a vernier was sufficient up to certain bus speeds. (RRFF 2396). Second, JEDEC rejected the use of vernier circuits in DDR SDRAM.

2398. Dr. Soderman relied, in part, on the fact that SLDRAM initially considered using vernier circuits in the controller and every DRAM without use of on-chip DLL, but ultimately decided to add DLL circuits to conclude that on-chip DLLs are necessary. (Soderman, Tr. 9412-14). This testimony is contradicted by the weight of the evidence. (CCFF 2399). Instead, Dr. Soderman's testimony demonstrated a fundamental misunderstanding of the function of vernier circuits and DLLs in the proposed SyncLink architecture.

Rambus's Response to Finding No. 2398:

Contrary to the proposed finding, Dr. Soderman's testimony is supported by the weight of the evidence. (RRFF 2399).

2399. The SLDRAM Consortium relied on vernier circuits for data capture. (Lee, Tr. 11044). The Consortium did not add DLL circuits to assist in data capture. (*Id.* 11046). Instead, it added DLL circuits to achieve a purpose other than data capture. (*Id.*).

Rambus's Response to Finding No. 2399:

As an initial matter, the proposed finding is irrelevant. Complaint Counsel concede that Synclink, which had wanted to avoid an on-chip PLL or DLL, was ultimately forced to add one.

Moreover, Complaint Counsel rely entirely on Mr. Lee's testimony which is both unreliable and not supported by the weight of the evidence. Although Mr. Lee testified at trial that the DLL was not used for the same purpose as the vernier, he told Professor Jacob that "the vernier was set in each of the DRAMs, and that the DLL was used to make that timing a little bit more accurate." (Jacob, Tr. 5619). Moreover, Mr. Lee's testimony of the purpose of the DLL in SLDRAMs is at odds with the description of that purpose in an article about SLDRAM written by Peter Gillingham of Mosaid and Bill Vogley of Texas Instruments. (RX2099-11 at 5; Lee, Tr. 11092).

(E) Increase the Number of Pins.

2400. At higher rates of speed, it is necessary to use a mechanism to guarantee that whatever is capturing data captures it during the data valid window. (Jacob, Tr. 5438-39, 5442-43). If JEDEC had chosen to improve performance by increasing the number of data pins, it would not have had to speed up the memory bus at all. (Jacob, Tr. 5454). Because the bus speed would have relatively stayed the same, increasing the number of pins in order to improve performance would not have required on-chip DLLs. (*Id.*).

Rambus's Response to Finding No. 2400:

The proposed finding is incomplete. Increasing the number of pins would have been prohibitively expensive and would have caused noise problems. (*See* RRFF 2358-60).

2401. Increasing the number of pins would have been an alternative to dual edged clocking and on-chip PLL/DLL. (Jacob, Tr. 5454).

Rambus's Response to Finding No. 2401:

The proposed finding is incomplete. (*See* RRFF 2400).

2402. Increasing the number of pins would have required less power consumption that dual-edged clocking with on-chip DLL. (Jacob, Tr. 5454). Eliminating the DLL circuit from the DRAM would have simplified DDR SDRAM design and decreased the die size. (*Id.*).

Rambus's Response to Finding No. 2402:

The proposed finding is incomplete. (*See* RRFF 2400).

(F) Rely on DQS Strobe.

2403. JEDEC could have relied on the DQS strobe to guarantee valid data capture. (Jacob, Tr. 5456). JEDEC did not need to perfectly align the read data with the system clock. (Jacob, Tr. 5442-43; Lee, Tr. 6662-63; Kellogg, Tr. 5161). In 1997, a majority of JEDEC members agreed that relying on the data strobe (or DQS) would have been sufficient for valid data capture. (Lee, Tr. 6682-83). It was not necessary to also include an on-chip DLL for valid data capture. (*Id.* 6682-83).

Rambus's Response to Finding No. 2403:

The proposed finding is not supported by the weight of the evidence. JEDEC could not have relied on the DQS data strobe without a DLL. (*See* RRFF 2379).

2404. The technical advantage of using a DQS strobe to ensure valid data capture is that the DQS strobe experiences the same propagation delays as the data because it travels with the data on the same signal path to/from the memory controller. (Kellogg, Tr. 5158-59). By experiencing the same signal delays as the data, it will tell the memory controller to capture data during the data valid window. (*Id.*).

Rambus's Response to Finding No. 2404:

The proposed finding is incomplete. As Hans Wiggers of IBM pointed out in explaining why a DLL is "essential": "[S]trobes do help, but at some point I still need to resynchronize to a clock on teh [sic] memory controller." (RX1040). This requires a DLL. (*Id.*)

2405. In April 1997, Micron proposed an edge-aligned, bi-directional data strobe for DDR SDRAM. (CX0368 at 1). An edge-aligned strobe allowed implementation without DLL. (*Id.* at 4).

Rambus's Response to Finding No. 2405:

The proposed finding is incomplete. DDR SDRAMs have a "bidirectional data strobe (DQS)," yet still use a DLL to align the strobe with the clock. (JX0057 at 5).

2406. In July 1997, Silicon Graphics proposed a unidirectional data strobe for read operations. (CX0370 at 3). Its proposal identified the following as a problem with current DDR SDRAM clocking proposals: "DLLs introduce instability, cut into dram core cycle time." (*Id.* at 2).

Rambus's Response to Finding No. 2406:

The proposed finding is incomplete. The Silicon Graphics proposal was a first showing. (JX0039 at 11). There is no evidence that the proposal progressed beyond this stage.

2407. In 1997, SGI had experience implementing Craylink and XTALK. (CX0370 at 2). Both Craylink and XTALK were source synchronous interfaces that could operate at 800 MB/sec. (*Id.*).

Rambus's Response to Finding No. 2407:

The proposed finding is irrelevant. Complaint Counsel have introduced no evidence as to what "Craylink" and "XTALK" were and whether they were in any way comparable to DRAM systems.

2408. In November 1997, Micron advocated eliminating the DLL from several DDR SDRAM clocking ballots. (CX-2713 at 2; Lee, Tr. 6651, 6654).

Rambus's Response to Finding No. 2408:

The proposed finding is incomplete. The proposal cited is by Kevin Ryan of Micron. (CX2713 at 2). {

} (RX1086 at 1 (*in camera*)).

2409. Dr. Soderman testified that the fact that DDR SDRAM uses both the DQS strobe and DLL shows that it would not have been feasible to rely on the DQS strobe. (Soderman, Tr. 9416). This testimony is contradicted by the weight of the evidence. (CCFF 2410).

Rambus's Response to Finding No. 2409:

Contrary to the proposed finding, Dr. Soderman's testimony is supported by the weight of

the evidence. (RRFF 2410).

2410. JEDEC included the DQS strobe in the DDR SDRAM standard because a majority at JEDEC wanted to use a strobe synchronous with the data in order to ensure valid data capture. (Lee, Tr. 6682). It included on-chip DLL to satisfy a minority of a few companies in JEDEC that did not want to use a scheme that relied on a data strobe. (*Id.* 6682-83). For those few companies, it was necessary to include a mechanism that aligned data with the system clock. (*Id.*).

Rambus's Response to Finding No. 2410:

The proposed finding is not supported by the weight of the evidence. JEDEC could not have relied on a data strobe absent a DLL. (RRFF 2379).

(G) Read Clocks.

2411. In the 1995-1998 time period, JEDEC considered read clocks as an alternative to using DLL circuits in every DRAM. (Kellogg, Tr. 5159-60; Lee, Tr. 6663-65; JX0029 at 18-19).

Rambus's Response to Finding No. 2411:

The proposed finding is incomplete. A read clock is less accurate than a strobe. (Kellogg, Tr. 5161). Since JEDEC could not rely on a strobe absent a DLL (RRFF 2379), it certainly could not have relied on a read clock. Indeed, even Complaint Counsel's technical expert, Professor Jacob, did not testify that a read clock was a viable alternative to on-chip DLL. (Jacob, Tr. 5444-45).

2412. In January 1996, Micron proposed a new clocking scheme for future SDRAM that would use an echo clock to control the variation in data valid windows. (JX0029 at 18-19; Lee, Tr. 6655). The proposal recommended the scheme as a way to avoid the replication of PLL/DLL circuits in every DRAM in the system. (*Id.*). An echo clock is a read clock. (Lee, Tr. 6664-65, using the terms "echo clock" and "read clock" interchangeably).

Rambus's Response to Finding No. 2412:

The proposed finding is incomplete. JEDEC could not have relied on a read clock absent a DLL. (RRFF 2411). Micron's presentation was designated in the minutes as a "first

presentation" (JX0029 at 4), and there is no evidence that it progressed beyond that stage.

2413. One of the advantages, in the 1995-1998 time frame, of read clocks versus data strobes was that read clocks required a significantly fewer number of pins to implement than data strobes. (Kellogg, Tr. 5160).

Rambus's Response to Finding No. 2413:

The proposed finding is irrelevant since read clocks could not have been used absent a DLL. (RRFF 2411).

2414. Read clocks would not have required the lock time that DLL circuits require and they address more components of skew than on-chip DLLs. (Lee, Tr. 6665). Because read clocks would have eliminated DLL circuits, they would have decreased the cost and power consumption of present day DDR SDRAMs. (*Id.* 6665-66).

Rambus's Response to Finding No. 2414:

The proposed finding is not supported by the weight of the evidence. Read clocks would not have eliminated DLLs. (RRFF 2411).

7. JEDEC Rules Prohibited Use of Patented Technologies Without a RAND Letter.

2415. If Rambus had disclosed that it had pending patent applications containing claims, or could have amended its pending applications to add claims, that covered the technologies in question and refused or failed to submit a letter promising to license the technologies on reasonable and non-discriminatory (RAND) terms, JEDEC would not have adopted Rambus's technologies into its SDRAM and DDR SDRAM standards. (Kelley, Tr. 2575, 2564-65; Rhoden, Tr. 350; Landgraf, Tr. 1714 ("If we knew in advance that they were not going to comply with the JEDEC patent policy, we would have voted against it.")).

Rambus's Response to Finding No. 2415:

The proposed finding is misleading because it leaves out relevant information. The proposed finding assumes that JEDEC would have requested a RAND letter from Rambus. The record shows, however, that JEDEC may well have ignored Rambus's disclosures. JEDEC members were convinced that Rambus's patents could not cover SDRAM or DDR because of

prior art. (*See* RPF 764-84). For instance, when JEDEC members examined Rambus's PCT application, they believed that it was merely "a collection of prior art." (CX 2058, Meyer Dep. at 300). Similarly, Mitsubishi (relying in part on work done by Cray Corporation) investigated Rambus's patents and concluded, "We have not been concerned about infringing on Rambus patent since if dispute would occur we believe we have sufficient *prior art* to show." (RX 660 at 1). Second, JEDEC members believed that Rambus was trying to slow or stop competing standards. (Gustavson, Tr. 9297; Wiggers, Tr. 10589). These facts might well have caused JEDEC to not ask Rambus for a RAND letter to avoid a situation in which Rambus could refuse, thereby stopping the standard even though JEDEC believed the Rambus patents would not cover the standard. (*See* RPF 1159-82). Another EIA committee adopted a technology despite a member's assertion that its patent covered the technology and apparent unwillingness to give a RAND assurance. (*See* RPF 1166-71). The EIA refused to request a RAND letter from the member because the EIA believed that (1) the member was trying to provoke such a request so that the member could refuse, thereby preventing the adoption of the technology so that its technology would prevail; and (2) the technology was not in fact covered by the patents. (*See* RPF 1168-70). JEDEC might well have done the same had Rambus disclosed.

Further, the evidence shows at least seven occasions during the period from May 1990 to the end of 1995 where the 42.3 committee adopted standards despite patent concerns and without a RAND letter. (*See* RPF 1225-37).

2416. If Rambus had disclosed that it had pending patent applications containing claims, or could have amended its pending applications to add claims, that covered the technologies in question and refused or failed to submit a RAND letter, JEDEC rules would have prohibited it from adopting the technologies in question into the standard. (CCFF 347).

Rambus's Response to Finding No. 2416:

The proposed finding is misleading because it leaves out relevant information. The proposed finding assumes that JEDEC would have requested a RAND letter from Rambus, which the evidence shows might well not have happened. (*See* RRFF 2415). Further, the evidence shows at least seven occasions during the period from May 1990 to the end of 1995 where the 42.3 committee adopted standards despite patent concerns and without a RAND letter. (*See* RPF 1225-37).

2417. JEDEC would not have knowingly adopted technologies subject to Rambus's patent application without a RAND letter. (Rhoden, Tr.350; Kelley, Tr. 2564-65). The ideal RAND letter would have offered patented technologies on a royalty-free basis. (Kelley, Tr. 2566). The next ideal RAND letter would have offered patented technologies on reasonable and nondiscriminatory terms. (*Id.*). If Rambus failed to submit a RAND letter, JEDEC would not have adopted Rambus's technologies into its SDRAM and DDR SDRAM standards. (Kelley, Tr. 2575, 2564-65; Rhoden, Tr. 350).

Rambus's Response to Finding No. 2417:

The proposed finding is misleading because it leaves out relevant information. The proposed finding assumes that JEDEC would have requested a RAND letter from Rambus, which the evidence shows might well not have happened. (*See* RRFF 2415). Further, the evidence shows at least seven occasions during the period from May 1990 to the end of 1995 where the 42.3 committee adopted standards despite patent concerns and without a RAND letter. (*See* RPF 1225-37).

2418. Rambus would not have agreed to RAND terms. (CCFF 2419-2432).

Rambus's Response to Finding No. 2418:

The proposed finding is contradicted by the weight of the evidence. Rambus would have had much to gain and little to lose by agreeing to RAND terms. (*See* RPF 1184-1203). Had

Rambus made the additional disclosures Complaint Counsel contend should have been made, it would have already lost any benefits of keeping that information confidential. (Teece, Tr. 10334). Rambus earns all of its revenues from licensing; thus, it would have had major economic incentives to ensure that JEDEC adopted, and its members licensed, Rambus's technology. (Teece, Tr. 10341-51). In light of this, Complaint Counsel's own economic expert could not testify that Rambus would not give a RAND assurance. (McAfee, Tr. 7730, 7733). Moreover, the evidence shows that Rambus has in fact licensed its SDRAM and DDR technologies on RAND terms. (*See* RPF Section XI).

2419. Agreeing to RAND terms would have been inconsistent with Rambus's existing business practices. (Diepenbrock, Tr. 6225-26; CX3129 at 488-89 (Vincent, Dep.) ("My best recollection is that standards bodies often said they wanted licenses under a reasonable, nondiscriminatory basis. And my best recollection is that Rambus licenses, that was not the basis for them.")). According to Mr. Diepenbrock, who served as Rambus's in-house patent counsel from 1995-1999, it was not clear to him whether Rambus had ever entered into an agreement that would have been consistent with RAND terms. (Diepenbrock, Tr. 6099, 6228).

Rambus's Response to Finding No. 2419:

The proposed finding is not supported and is contradicted by more reliable evidence. First, the evidence shows that Rambus has in fact licensed its SDRAM and DDR technologies on RAND terms. (*See* RPF Section XI). Rambus also intends to continue to license its SDRAM and DDR technology on reasonable and nondiscriminatory terms. (CX 2112, Mooring Dep. at 197). That Rambus has complied with RAND terms in the real world is the best evidence that it would agree to do so in the but-for world.

Second, agreeing to RAND terms would have been consistent with Rambus's business model, which was based earning revenues from licensing its patented technologies. (*See* RPF 1193-95). By agreeing to a RAND commitment, Rambus would increase the likelihood that

JEDEC would adopt its technologies and that Rambus would gain royalty revenue. (Teece, Tr. 10341-45).

Third, the cited evidence does not support the proposition. The basis for Mr. Diepenbrock's testimony that he had not studied all of Rambus's contracts; thus, "there was no way for me to be certain that all of the terms met RAND." (Diepenbrock, Tr. 6227). Mr. Diepenbrock did not testify that "it was not clear to him whether Rambus had ever entered into an agreement that would have been consistent with RAND terms"; rather, he testified that it was not clear to him that "*every* contract that had ever been signed by Rambus up to that point would meet that standard." (Diepenbrock, Tr. 6228 (emphasis added)). In addition, Mr. Vincent, upon whose testimony Complaint Counsel rely, was Rambus's outside counsel, not a Rambus business person. (CX 3123, Vincent Dep. at 9).

2420. When requested to do so, Rambus refused to assure the IEEE that it would license on RAND terms. (CCFF 2421-2426).

Rambus's Response to Finding No. 2420:

The proposed finding is misleading, incomplete, and irrelevant. Rambus was requested by the IEEE to provide a RAND assurance for Ramlink. (CX 487 at 1; Wiggers, Tr. 10595-96). Rambus's response stated that it had "already licensed its technology and patents to a substantial number of licensees and will continue to license its technology in accordance with its existing business practices." (CX 855 at 2). According to Mr. Diepenbrock, Rambus's in-house counsel who responded to the IEEE request, he could not determine whether all of Rambus's *existing* licenses met the RAND requirement because he had not studied the licenses so "there was no way for me to be certain that all of the terms met RAND." (Diepenbrock, Tr. 6227). In other

words, apparently IEEE's policy required Rambus to confirm that all of its existing RDRAM licenses met the RAND requirement. The JEDEC RAND requirement, however, is specific to a particular standard. (*See* CX 711 at 188 (Crisp email stating that Desi Rhoden informed him that Rambus can chose to comply with the JEDEC policy on a "case by case basis" and concluding that the policy was not as "onerous" as people at Rambus had believed)). The evidence of how Rambus responded to the IEEE request, therefore, does not aid the determination of what Rambus would have done had JEDEC asked for a RAND letter.

2421. On December 13, 1995, Ms. Cheryl Rowden of the IEEE wrote Rambus's President, Mr. Tate, to inquire whether it might have patents that could apply to IEEE draft document P1596.4. (CX0487 at 1). She asked Mr. Tate to inform the IEEE by January 15, 1996, whether or not Rambus had applicable patents and, if so, to "advise whether or not your company will issue a letter of assurance, in accordance with IEEE Standards Patent Policy." (*Id.*). If Mr. Tate did not respond by January 15, 1996, Ms. Rowden informed him that IEEE would have to assume that Rambus had no applicable patents. (*Id.*).

Rambus's Response to Finding No. 2421:

The proposed finding is irrelevant. (*See* RRFF 2420).

2422. On Rambus's behalf, Lester Vincent prepared draft responses to the IEEE stating explicitly that Rambus would not agree to be bound by the IEEE's licensing terms. (CCFF 2423-2424).

Rambus's Response to Finding No. 2422:

The proposed finding is irrelevant. (*See* RRFF 2420).

2423. Mr. Vincent prepared a draft dated January 11, 1996 stating that Rambus believed it was "under no obligation to any standards body to license its intellectual property" or "to disclose its intellectual property in order to retain the right to enforce" it. (CX0853 at 1). The draft letter further stated that Rambus "reserves the sole right to decide whether or not to license its intellectual property, and if so, at what rate or rates." *Id.* The draft letter concluded, "Rambus will not . . . issue the letter of assurance that you have requested regarding a non-discriminatory license. Indeed, Rambus is offering no such license. Rambus reserves all rights to enforce its intellectual property on whatever terms Rambus decides." (*Id.* at 2).

Rambus's Response to Finding No. 2423:

The proposed finding is irrelevant. (*See* RRFF 2420).

2424. Mr. Vincent prepared a draft dated January 15, 1996 stating that Rambus wished to continue to license its technology on terms that are "consistent with Rambus's own business plan and that are not set by any standards body," and that Rambus therefore was "unable" to provide the IEEE with the letter of assurance that the IEEE sought. (CX0856 at 1).

Rambus's Response to Finding No. 2424:

The proposed finding is irrelevant. (*See* RRFF 2420).

2425. On January 15, 1996, Mr. Anthony Diepenbrock responded to Ms. Rowden of the IEEE. (CX0855). His letter did not promise to license on RAND terms. Rather, Mr. Diepenbrock's letter stated that Rambus would continue to license its technology "in accordance with its existing business practices." (CX0855 at 2).

Rambus's Response to Finding No. 2425:

The proposed finding is irrelevant. (*See* RRFF 2420).

2426. In a letter dated February 16, 1996, Cheryl Rowden of IEEE thanked Mr. Diepenbrock for making it clear to IEEE in an earlier letter that Rambus would license pertinent patents on reasonable and nondiscriminatory terms. (CX0490 at 1; Diepenbrock, Tr. 6223). Mr. Diepenbrock did not agree with Ms. Rowden's interpretation of his earlier letter to her. (Diepenbrock, Tr. 6223-24). Mr. Diepenbrock sent Ms. Rowden another letter in which he stated that, "Rambus has already licensed its technology and will continue to license its technology in accordance with its existing business practices." (CX0869 at 1; Diepenbrock, Tr. 6623-24).

Rambus's Response to Finding No. 2426:

The proposed finding is irrelevant. (*See* RRFF 2420).

2427. Rambus's standard license agreement was inconsistent with JEDEC's patent licensing policy because Rambus preserved the right to discriminate between those it would and would not license to. (CX3124 at 235 (Vincent, Dep.) ("Q What was it about the terms of Rambus's standard license agreement that was not consistent or may not be consistent where the JEDEC policy? A I don't really recall the terms of the Rambus license agreement. The one thing, though, would be that -- that would come to me now would be that Rambus would not be under an obligation to license somebody if they didn't want to.)).

Rambus's Response to Finding No. 2427:

The proposed finding is irrelevant. (*See* RRFF 2420).

2428. In draft versions of its withdrawal letter to JEDEC, Rambus made it clear that it could not comply with JEDEC's patent licensing policy. In developing a withdrawal letter to JEDEC, someone had suggested that Rambus inform JEDEC that it would not agree with the terms of JEDEC's patent licensing policy. (Crisp, Tr. 3384 ("Q. Now, someone had also suggested that Rambus tell JEDEC that Rambus would not agree to the terms of the JEDEC patent licensing policy. Isn't that right? A. Yes, sir, that's correct.")).

Rambus's Response to Finding No. 2428:

The proposed finding is irrelevant. The weight of the evidence shows that Rambus would have given a RAND letter had it been asked. (*See* RRFF 2418). What Rambus put in a draft letter, which was never sent to JEDEC, does not bear on what Rambus would have done in response to a RAND request from JEDEC after it made the additional disclosures that Complaint Counsel claim should have been made. Further, the evidence shows that Rambus's SDRAM and DDR licenses are in fact consistent with a RAND commitment. (*Id.*)

2429. In a draft withdrawal letter dated March 20, 1996, Mr. Crisp wrote: "As you are aware, Rambus Inc. is a technology developer with a primary source of revenue coming from licensing patents and collecting royalties from their use. Accordingly, Rambus Inc. cannot agree to the terms of the JEDEC patent policy as it limits our ability to solely control the dissemination and use of our intellectual property." (CX0873 at 1).

Rambus's Response to Finding No. 2429:

The proposed finding is irrelevant. The weight of the evidence shows that Rambus would have given a RAND letter had it been asked. (*See* RRFF 2418). What Rambus put in a draft letter, which was never sent to JEDEC, does not bear on what Rambus would have done in response to a RAND request from JEDEC after it made the additional disclosures that Complaint Counsel claim should have been made. Further, the evidence shows that Rambus's SDRAM and

DDR licenses are in fact consistent with a RAND commitment. (*Id.*)

2430. In another draft withdrawal letter dated March 20, 1996, Mr. Crisp wrote: "As you are aware, Rambus Inc. is a high speed memory technology developer driving revenue from licensing fees and royalties. Rambus Inc. cannot agree to the terms of the JEDEC patent policy as it limits our ability to conduct business according to our business model." (CX0874 at 1).

Rambus's Response to Finding No. 2430:

The proposed finding is irrelevant. The weight of the evidence shows that Rambus would have given a RAND letter had it been asked. (*See* RRFF 2418). What Rambus put in a draft letter, which was never sent to JEDEC, does not bear on what Rambus would have done in response to a RAND request from JEDEC after it made the additional disclosures that Complaint Counsel claim should have been made. Further, the evidence shows that Rambus's SDRAM and DDR licenses are in fact consistent with a RAND commitment. (*Id.*)

2431. In its withdrawal letter to JEDEC, Rambus made it clear that it would license its technology according to its own terms which would not necessarily be consistent with RAND terms. (CX0887 at 1 ("Recently at JEDEC meetings, the subject of Rambus patents had been raised. Rambus plans to continue to license its proprietary technology on terms that are consistent with the business plan of Rambus, and those terms may not be consistent with the terms set by standard setting bodies, including JEDEC."); CX3129 at 488-89 (Vincent, Dep.)).

Rambus's Response to Finding No. 2431:

The proposed finding is irrelevant. The weight of the evidence shows that Rambus would have given a RAND letter had it been asked. (*See* RRFF 2418). Further, the evidence shows that Rambus's SDRAM and DDR licenses are in fact consistent with a RAND commitment. (*Id.*)

2432. Rambus wanted to maintain the right to exclude companies from obtaining licenses to its technology. (CX3129 at 488-89 (Vincent, Dep.) (Rambus "did not necessarily have to license everybody, they could license who they wanted to.")). Further, Rambus wanted the freedom to license on whatever terms the market would bear. (*Id.* ("Q: And on terms that the market would bear? A: Right. On a mutual meeting of the minds in terms of a license.")).

Rambus's Response to Finding No. 2432:

The proposed finding is contradicted by more reliable evidence. The proposed finding relies only on the testimony of Rambus's outside counsel. In its actual licensing practices, however, Rambus has offered to license its SDRAM and DDR technologies to all DRAM manufacturers. (Farmwald, Tr. 8242). Further, Rambus would have had overriding economic incentives to agree to give a RAND letter and give up its right to exclude. (*See* RPF 1184-1203).

8. JEDEC Likely Would Have Avoided Rambus Patents Even If Rambus Had Promised To License On RAND Terms.

2433. Even if Rambus had promised RAND terms, JEDEC members likely would have adopted alternative technologies. At JEDEC, there have been instances of disclosure where the disclosing company had agreed to RAND terms but JEDEC nevertheless chose to investigate and ultimately work around technologies that would have been patented. (Kellogg, Tr. 5046-48, discussing Cypress disclosure and Kentron disclosures). IBM personally experienced instances of disclosure which were followed by a RAND letter after which JEDEC chose not to pursue IBM's technology. (*Id.* 5049).

Rambus's Response to Finding No. 2433:

The proposed finding is not supported and contradicted by more reliable evidence. First, the evidence shows that JEDEC preferred Rambus's technologies for SDRAM and DDR over all alternatives; it chose the Rambus technologies after evaluating alternatives. (*See* RPF 724-32). Second, the evidence shows that JEDEC's revealed preference for Rambus's technologies would not have changed had Rambus made additional disclosures; JEDEC adopted all four of the technologies in the DDR2 standard after examining alternatives and despite knowing that Rambus had issued patents over the four technologies and was demanding royalties. (*See* RPF 732-63). Third, the evidence shows that there were no acceptable, noninfringing alternatives and that rational DRAM manufacturers would have chosen the Rambus technologies

for SDRAM and DDR because they are less costly than the alternatives, even accounting for Rambus's royalties. (*See* RPF 785-1146). Fourth, JEDEC's behavior indicates that upon receiving a RAND assurance, it would have proceeded to adopt Rambus's technologies. (*See* RPF 1219-44). More specifically, from the May 1990 through the end of 1995, the 42.3 committee standardized at least a dozen technologies that it was aware were patented or potentially patented. (*See* RPF 1225-37). On five of these occasions, the 42.3 committee received a RAND assurance. (*See* RPF 1237). On at least seven occasions, the 42.3 committee proceeded to adopt a technology despite patent issues without first receiving a RAND letter. (*See id.*)

Fifth, the cited testimony does not support the proposition that JEDEC would have avoided Rambus's technologies had Rambus made additional disclosures and agreed to give a RAND letter. Mr. Kellogg testified that, on a few occasions, JEDEC chose to use alternatives to patented technologies for which JEDEC had received a RAND letter. (Kellogg, Tr. 5046-49). He did *not* testify that the reason that JEDEC chose to use alternatives was the presence of intellectual property; in fact, Mr. Kellogg did not give *any* reason for why JEDEC opted for alternatives in these instances. (*Id.*)

The only evidence on this issue shows that JEDEC avoided these technologies because of technical reasons, not intellectual property reasons. Mr. Kellogg testified that JEDEC opted for an alternative to Hyundai's proposed TRIMM technology for which Hyundai disclosed "patent activity." (Kellogg, Tr. 5048). The record shows that this decision was driven by technical concerns. (CX 2237 at 4 ("Hyundai's 160pin SO TRIMM failed due to issues with size and reliability of connector/socket")). Mr. Kellogg testified that JEDEC opted for an alternative to

Kentron's technology for doubling the data rate off of a module. (Kellogg, Tr. 5048). The record shows that a motion to ballot Kentron's Quad Band Memory technology, which doubles the data rate from a module, failed for a lack of a second at the September 2000 JEDEC meeting. (CX 0160 at 1). The minutes state, "The Committee wanted to see more information on how the spec would look before balloting it." (CX 0160 at 1). Additionally, there was testimony at trial that members of the industry did not believe that Kentron's technology would work. (Polzin, Tr. 4035-36). The record does not reflect when, if, or why JEDEC opted for alternatives to the other technologies about which Mr. Kellogg testified.

In the case of Rambus's technologies, however, JEDEC's evaluation shows that they were the best alternatives. (Kelley, Tr. 2707-09; RPF 724-32). Gordon Kelly, the long-time chair of 42.3, could not recall *any* instance in which the committee did not adopt a patented technology the committee thought was best after receiving a RAND letter. (Kelley, Tr. 2707-09).

2434. Even if Rambus had disclosed its patent claims before 1996 and provided JEDEC with a RAND letter, JEDEC would have had the option to adopt alternatives to the four technologies at issue in this case. (Meyer, Tr. 378-39; Kelley, Tr. 2564-65)

Rambus's Response to Finding No. 2434:

The proposed finding is misleading and incomplete. JEDEC did not have the "option" to adopt alternatives because there were no acceptable, noninfringing alternatives. (*See* RPF 785-1146). Further, the weight of the evidence shows that JEDEC would have adopted Rambus's technologies. (*See* RRFF 2433).

2435. In other instances where JEDEC members suspected a technology under discussion might be covered by Rambus patents, JEDEC did not continue to pursue those technologies for standardization. (CCFF 2436-2440).

Rambus's Response to Finding No. 2435:

The proposed finding is misleading and contradicted by more reliable evidence. First, the cited evidence recounts one instance (not instances) in which JEDEC purportedly avoided a technology proposed by NEC because of a concern regarding Rambus patents. (*See* CCFF 2436-40). Second, if JEDEC avoided the NEC proposal because of Rambus's intellectual property, it did so because committee members did not believe that Rambus would license on RAND terms. The minutes of the JEDEC meeting at which NEC made this proposal state, "Some Committee members did not feel that the Rambus patent license fee fit the JEDEC requirement of being reasonable. Rambus has also told JEDEC that they do not intend to comply with JEDEC patent policies." (JX 36 at 7). This incident, therefore, gives no insight into how JEDEC would have reacted had Rambus *agreed* to give a RAND letter. Third, the record is replete with instances in which JEDEC and its members proceeded to adopt Rambus's technologies for standards despite concerns about Rambus's patents. (*See* RPF Section VI).

2436. In March 1997, NEC proposed a clocking scheme that used a looped-back topology. (Lee, Tr. 6694). The clocking scheme proposed by NEC was different from the one that was ultimately included in the DDR SDRAM standard. (JX0036 at 7; Lee, Tr. 6694).

Rambus's Response to Finding No. 2436:

The proposed finding is misleading and incomplete. (*See* RRFF 2435).

2437. Some JEDEC members who were knowledgeable at the time about Rambus architectures expressed their concern that Rambus might have intellectual property that covered NEC's proposed clocking scheme. (JX0036 at 7; Rhoden, Tr. 527-28). Terry Lee stated that the bus topology NEC proposed for its clocking scheme looked similar to Rambus's '703 patent. (Lee, Tr.6694-95). Many people during the meeting strongly objected to further consideration of NEC's proposal for a DDR clocking scheme. (*Id.* 6695)("Many other people in the room also objected. There was a variety of comments from quite a few people from the committee who were -- strongly objected to the consideration of this proposal for the standard.").

Rambus's Response to Finding No. 2437:

The proposed finding is misleading and incomplete. (*See* RRFF 2435).

2438. JEDEC members refused to consider using NEC's proposal "specifically because of the disclosure that had take place by others knowledgeable in the industry." (Rhoden, Tr. 527-28; *see also* Lee, Tr. 6695-96).

Rambus's Response to Finding No. 2438:

The proposed finding is misleading and incomplete. (*See* RRFF 2435).

2439. In April 1997, Micron presented an alternative to NEC's proposal for a DDR clocking scheme that intentionally did not require the use of looped-back clocks. (CX0368 at 2; Lee, Tr. 6697-98). Micron's proposal noted that, "Loop back strobe could have intellectual property problems." (*Id.* 6699). The latter was a reference to the Rambus patent issues raised during NEC's clocking proposal. (*Id.* 6699). Micron wanted JEDEC to avoid the patent problems associated with NEC's clocking proposal. (*Id.*). Micron proposed using a bidirectional data strobe for reads and writes that did not use a looped-back technology. (CX0368 at 1-4; Lee, Tr. 6698-99).

Rambus's Response to Finding No. 2439:

The proposed finding is misleading and incomplete. (*See* RRFF 2435). Further, the cited evidence shows that Mr. Lee is not credible. The NEC "loop back clock" proposal was not limited to a narrow-bus architecture. (Rhoden, Tr. 579; Lee, Tr. 6961). Mr. Lee's testimony that he recognized NEC's proposal as being covered by Rambus's '703 patent therefore demonstrates that members of JEDEC did not believe that Rambus's patents were limited to a narrow-bus architecture. Mr. Lee, however, specifically testified that he believed that the '703 patent was limited to a "loop back clock in connection with this multiplexed command/address/data bus for this narrow bus system," i.e., that it was limited to "specifically to this bus architecture." (Lee, Tr. 6609-10). His announcement to JEDEC that the NEC proposal would be covered by Rambus's '703 patent, and Micron's presentation that avoided using a loop-back clock even for

wide-bus DDR architecture, completely contradicts his claim that he thought Rambus's technology was limited to a narrow-bus architecture. (Lee, Tr. 6694-96; CX 368 at 2). Accordingly, Mr. Lee did not give credible testimony.

2440. JEDEC ultimately adopted a bidirectional data strobe that did not use a looped back topology into its DDR SDRAM standard. (CX0234 at 164; Lee, Tr. 6681-82).

Rambus's Response to Finding No. 2440:

The proposed finding is misleading and incomplete. (*See* RRFF 2435).

B. If Rambus Had Disclosed On A Timely Basis And JEDEC Wanted To Use The Technologies In Its Standards, JEDEC Members Likely Would Have Sought To Negotiate Acceptable Royalty Rates Before Becoming Locked In To Use of the JEDEC Standards.

2441. Even if JEDEC had still decided to adopt the four technologies at issue in this case after disclosure had occurred from Rambus before 1996, JEDEC members likely would have negotiated a lower royalty rate than they are able to negotiate today. (CCFF 2442-2464).

Rambus's Response to Finding No. 2441:

The proposed finding is not supported by the evidence. The evidence shows that had Rambus made the additional disclosures that Complaint Counsel contend should have been made and JEDEC had adopted the Rambus technologies, negotiations between Rambus and JEDEC members would have occurred after Rambus's patents issued in 1999. (*See* RPF 1204-18). There is no evidence of "*ex ante*" negotiations occurring in any other situation. (*See* RPF 1206-07). Moreover, negotiations for rights to potential claims pending in a patent application are difficult, costly, and therefore unlikely to occur. (*See* RPF 1208-11). In fact, Complaint Counsel's economic witness could only testify that JEDEC members would have an "incentive" to engage in such "*ex ante*" negotiations; he did not testify that such negotiations would have in fact occurred. (McAfee, Tr. 7493-94).

Moreover, as explained in detail below, JEDEC members who negotiated with Rambus for RDRAM licenses prior to the issuance of Rambus's SDRAM and DDR patents did not seek rights to use Rambus's technologies in SDRAM and DDR despite concerns that Rambus may obtain patents on those devices. (*See* RRFF 2449-60). This is likely because JEDEC members were convinced that Rambus's patents could not cover those technologies because of prior art. (*See* RPF 764-84).

2442. DRAM manufacturers must be concerned about minimizing costs. (Appleton, Tr. 6277; CX2107 at 136 (Oh, Dep.)). The DRAM business is a commodity business which is characterized by a high degree of competition and low profit margins. (Appleton, Tr. 6280-81 (Micron, for example, has always had a policy to reduce costs because the selling price of DRAM can be so volatile.); CX2107 at 136 (Oh, Dep.)).

Rambus's Response to Finding No. 2442:

The proposed finding is contradicted by other evidence. The evidence shows that there is a high degree of communication and coordination between the DRAM manufacturers, which restrains competition in the DRAM business. (*See* RRFF 1802 1808, 1813, 1840).

2443. DRAM customers require DRAM manufacturers to meet their performance requirements for as little cost as possible. (Polzin, Tr. 3960 (AMD "needed to make sure that whatever memory [they] chose in [their] systems for [their] microprocessors was a commodity and met the requirements at the lowest possible cost."); Williams, Tr. 823-34 (During meetings with customers regarding Burst EDO, "Keeping the cost low of DRAM was the goal."); CX2777 at 1 ("...the age old rule for DRAMs still apply. Customers will take as much performance as we can give them for absolutely no added cost over the previous technology. They will not pay extra for increased DRAM performance."); CX1708 at 2 ("Compaq (Dave Wooten) like the others, stressed that price was the major concern for all of their systems. . . . Sun echoed the concerns about low cost. They really hammered on that point."); Gross, Tr. 2302-03 (HP and Compaq have sometimes adopted memory that did not offer any performance improvement but did reduce costs.)).

Rambus's Response to Finding No. 2443:

The proposed finding is incomplete and misleading. Not surprisingly, DRAM customers

want to pay the lowest price possible for DRAM that meets their performance needs. DRAM prices to customers (their "costs"), however, are not necessarily related to the manufacturing cost of DRAM. (Gross, Tr. 2338). Rather, the cost of DRAM to DRAM customers is driven by the volume of DRAM produced. (Gross, Tr. 2339).

2444. DRAM manufacturers and customers will forego a performance benefit in order to achieve lower cost. (CX2777 at 1 (In October 2000, Micron decided to vote against a proposed improvement to DDR II standardization efforts because it "add[ed] too much cost to be a standard feature and would jeapordize the success of DDRII if it were required."); Sussman, Tr. 1441-42 (Sussman did not recommend RDRAM for PC main memory because it was too expensive even though it offered more performance per pin than SDRAM.); Crisp, Tr. 3008-09 ("Q. You understood that a customer might be willing to leave some performance on the table in order to achieve low cost? A. Yes, sir, that's correct."); CX0711 at 34).

Rambus's Response to Finding No. 2444:

The proposed finding is misleading and incomplete. DRAM manufacturers and customers are concerned with arriving at the optimal solution in price/performance terms. (Kellogg, Tr. 5113 (attempting to "work within the industry to develop the optimal solution, price/performance")). During the 1990's, however, the industry was faced with a growing memory bottleneck, which drove the need for improved DRAM performance. (*See* RPF 27-40). DRAM manufacturers and customers have therefore often opted for a more costly technology in order to meet performance or flexibility goals. For example, using a single fixed burst length part would have been less costly for DRAM manufacturers. (Kellogg, Tr. 5117-18). The initial DDR2 standard specified a single burst length. (RX 1854 at 20; Macri, Tr. 4733-34; Krashinsky, Tr. 2834 (JEDEC based preliminary DDR2 specification on single (fixed) burst length)). At the September 2001 JC42.3 meeting, however, both Intel and AMD proposed that DDR2 have burst length of 8 in addition to 4. (CX 174 at 7-8). According to Intel, adding a burst length of 8

would result in a "[p]otential Improvement of 4-10% On High-Bandwidth Applications." (CX 174 at 37). The vote to ballot this proposal was unanimous. (CX 174 at 7-8). DRAM manufacturers and customers therefore insisted on using programmable burst length despite the added manufacturing cost and despite knowing that using this technology could require payment of royalties to Rambus. (Macri, Tr. 4679-83; Polzin, Tr. 4046-47).

2445. JEDEC members aim to keep the cost of implementing the standard for the next generation product as close as possible to the cost of implementing the standard for the previous generation. (Kelley, Tr. 2476, 2526-27 ("The first requirement of a DRAM is low cost. If you cannot make a DRAM low cost, then you won't be in the business. DRAM low cost was paramount before our eyes [at JEDEC]."); CX0034 at 4; CX0711 at 1; CX2294 at 15);

Rambus's Response to Finding No. 2445:

The proposed finding is incomplete. The evidence shows that users of DRAM wanted the price to them for the next generation DRAM to be approximately 5% to 10% of the previous generation. (Tabrizi, Tr. 9081; Kelley, Tr. 2526-27). Similarly, DRAM manufacturers aim to reduce costs to within 5% of the previous generation. (CX 34 at 4).

2446. The pressure to reduce costs also drives the DRAM industry to avoid paying royalties whenever possible. (CCFF 107; Appleton, Tr. 6299 (Over the past ten years, Micron has focused on reducing its royalty expenses in order to further its general policy of reducing costs).

Rambus's Response to Finding No. 2446:

The proposed finding is misleading and contradicted by other evidence. The evidence shows that the DRAM industry routinely agrees to pay royalties for licensed technology and that JEDEC routinely adopts patented technologies knowing that royalties will need to be paid. Hyundai agreed to pay Texas Instruments 8% to license technology used in DRAMs. *Texas Instruments, Inc. v. Hyundai Electronics Indus.*, 42 F. Supp. 2d 660, 663-64, 671, 676-77 & n.39

(E.D. Tex. 1999); *Texas Instruments, Inc. v. Hyundai Electronics Indus.*, 49 F. Supp. 2d 893, 897 (E.D. Tex. 1999). Samsung licensed technology from Texas Instruments and agreed to pay 9% on the sales of DRAMs in the United States and 3% on the sales of DRAMs in Japan. *Texas Instruments, Inc.*, 49 F. Supp. 2d at 902. Andreas Bechtelscheim testified that Sun expected memory module manufacturers to pay for the use of Sun's patented technology when they made products for Sun's SPARC workstations. (Bechtelscheim, Tr. 5899-901). Similarly, JEDEC has repeatedly standardized technologies that have patent implications. For instance, in May 1990, JC 42.3 sent a ballot to Council to standardize the 256K x4 MPDRAM technology knowing that Digital Equipment Corporation had a patent on the technology and demanded a royalty rate of 1%. (JX 1 at 6, 24). In July 1992, JC 42.3 passed ballots to standardize 2M x8/x9 Sync DRAM in TSOP II knowing that Motorola had an issued patent on the technology and would demand royalties. (JX 13 at 9-10, 136). Similarly, JEDEC members voted to rescind a hold on TI's Quad CAS technology knowing that TI would require the payment of royalties. (RX 562 at 13; JX 25 at 5). Similarly, DRAM industry members agreed to pay Rambus royalties for its RDRAM technologies. (*See* RRFF 2450). Further, JEDEC adopted each of the four technologies at issue in this case for the DDR2 standard despite knowing that Rambus had issued patents covering those technologies and that Rambus was demanding royalties for their use. (*See* RPF 724-63).

2447. JEDEC members aim to avoid royalties whenever possible. (CX0838 at 1 ("I think that Samsung is on a path to do anything they can to get out of paying us royalties. . . . "); (CX2107 at 137 (Oh, Dep.) (open architecture was important to Hyundai "[b]ecause it means that it is adopted by JEDEC, and thus it requires no royalty or no fees at all."); CX2294 at 15 ("Strong Points . . . Open architecture without royalties or fees"); CX0676 ("[Samsung] will think that 2% is high for a commodity (memories)"); CX2726 at 7 ("Why DDR Is Cost Effective No Royalties")).

Rambus's Response to Finding No. 2447:

The proposed finding is misleading and contradicted by other evidence. (*See* RRFF 2446).

2448. Representatives of companies who participate in JEDEC testified that they would not have developed SDRAM and DDR SDRAM had they know there were royalties associated with those device. (Bechtelsheim, Tr. 5813-14 (Had Mr. Bechtelsheim known that programmable CAS latency and burst length could potentially have royalties associated with them, he would have opposed their inclusion in JEDEC SDRAM standards.); CX2107 at 137 (Oh, Dep.) (Dr. Oh testified that Hyundai would not have developed DDR SDRAM if it had been known to have royalties associated with.)).

Rambus's Response to Finding No. 2448:

The proposed finding is contradicted by more reliable evidence. The proposed finding relies on after-the-fact testimony of witnesses who were not JEDEC representatives. Actual JEDEC representatives who were at the relevant meetings admitted that had Rambus made the additional disclosures that Complaint Counsel contend should have been made, they would have been willing to adopt Rambus's technology even though doing so would have entailed the payment of royalties. For example, HP's JEDEC representative testified that he would have still voted to incorporate Rambus's technologies into the DDR standard if Rambus would comply with the JEDEC patent policy, which would have meant that Rambus would receive reasonable royalties. (Landgraf, Tr. 1714). Similarly, IBM's representative, who was the chair of JC 42.3, testified that if Rambus had agreed to give a RAND assurance, he would have had to considered adopting the covered technologies. (Kelley, Tr. 2564-66). Moreover, the 42.3 committee repeatedly adopted patented technology for its standards during the 1991-95 time frame knowing that members would have to pay royalties for those technologies. (*See* RPF 1220-37; Kelley, Tr. 2707-09 (chair of 42.3 testifying that he could recall no instance in which JEDEC pursued an

alternative after receiving a RAND assurance). Further, JEDEC adopted each of the four technologies at issue in this case for the DDR2 standard despite knowing that Rambus had issued patents covering those technologies and that Rambus was demanding royalties for their use. (*See* RPF 724-63).

2449. When JEDEC members cannot avoid royalties, they seek to negotiate royalty rates down to acceptably low levels. (CCFF 2450-2454).

Rambus's Response to Finding No. 2449:

Rambus does not have a specific response to this proposed finding but, rather, responds below to the specific proposed findings cited in support. (*See* RRFF 2450-54).

2450. DRAM manufacturers thought that royalties of 1-2% for technologies used in main memory were unacceptable. (Lee, Tr. 7047-48 ("[Rambus's demand for royalties of] 2 percent, was larger than anything we'd ever heard of for an interface technology and certainly the largest thing we ever heard of for some sort of fee we'd have to pay to produce main memory."); Appleton, Tr. 6337-39 ("[W]e thought the [2%] royalty rate was quite high. We thought the NRE package, the nonreoccurring engineering charge, was high. To us it looked exorbitant. It was just pretty high cost."); RX-855 at 1 ("0.1% royalty okay, 1-2% ridiculous); CX0711 at 61 (On March 23, 1995, Richard Crisp wrote: "Farhad . . . says their #1 issue with the Rambus business proposal is the royalty rate. They do not want to be straddled [sic] with 3% royalties."); Lee, Tr. 6614 (Micron did not take a license with Rambus in 1995 because the cost "combined with the royalty for doing that product was unacceptable."); CX2078 at 139-42 (JEDEC members considered TI's offer of a 1% royalty rate on a packaging technology to be unreasonable and therefore rejected TI's technology as a standard.)).

Rambus's Response to Finding No. 2450:

This proposed finding is misleading and contradicted by more reliable evidence. The proposed finding relies on statements during negotiations and other communications. The evidence of the royalty rates that DRAM manufacturers actually paid is more reliable. Industry royalty rates, including those paid by DRAM manufacturers, typically exceed 1-2% and average approximately 4.5%. (*See* RPF 1378-1393). IBM's policies, which were shown to JEDEC, set

forth royalty rates for its technologies from 1-5% of selling price. (JX 9 at p.24; Kellogg, Tr. 5232, 5238-39; Kelley, Tr. 2618-20; *see also* RX 653 at IBM/2 128124 ("The normal royalty rate for a license to IBM patents ranges from 1% to 5% of the selling price for the apparatus that practices the patents"). JEDEC standardized a memory technology patented by Digital Equipment Corporation knowing that Digital would require payment of a royalty rate of 1% of sales. (JX 1 at 24). Kentron structured the pricing of its proprietary flex tabs for its FEMMA technology to receive the equivalent of a 5% royalty, which is effectively charging that royalty rate. (Goodman, Tr. 6020-22, 6078-80; Teece, Tr. 10432). Hyundai agreed to pay Texas Instruments 8% to license technology used in DRAMs. *Texas Instruments, Inc. v. Hyundai Electronics Indus.*, 42 F. Supp. 2d 660, 663-64, 671, 676-77 & n.39 (E.D. Tex. 1999); *Texas Instruments, Inc. v. Hyundai Electronics Indus.*, 49 F. Supp. 2d 893, 897 (E.D. Tex. 1999). Samsung licensed technology from Texas Instruments and agreed to pay 9% on the sales of DRAMs in the United States and 3% on the sales of DRAMs in Japan. *Texas Instruments, Inc.*, 49 F. Supp. 2d at 902. Industry surveys show average royalty rate in the semiconductor industry are about 4.5%. (Teece, Tr. 10444-45; RX 2105-05 at 3; RX 2105-03 at 3; Teece, Tr. 10448).

In addition, each of the DRAM manufacturers agreed to pay Rambus's RDRAM royalties, which ranged from 2% to 5%. In July 1991, long before Intel became interested in RDRAM, NEC signed an RDRAM license agreement that specified a 2% royalty rate for Rambus Microprocessors and Microcontrollers, 1% for Rambus Memory Devices, 3% for Rambus Peripherals, and 3% for Customer Specific Rambus Products. (RX 538 at 22). In November 1994, again well before Intel selected RDRAM for the next generation DRAM, Samsung agreed to an RDRAM license that specifies a 2% royalty rate, which declines at certain

volume marks. (RX 518 at 23). Hyundai agreed, in December 1995, to an RDRAM license agreement that specifies a 2.5% royalty rate for Rambus DRAMs (which declines to 2% then 1.5% in 2000 and 2002 respectively), 3% for Rambus processors, and 5% for Rambus ASICs and Peripherals. (CX 1600 at 12). Micron agreed to an RDRAM license in March 1997 that specifies a 2% royalty rate. (CX 1646 at 11). Also in 1997, Siemens entered into an RDRAM license that specified a royalty rate of 2.5% for Rambus DRAMs (which reduced to 2% if RDRAMs exceeded 25% of Siemens total DRAM sales) and 5% for Rambus Peripherals. (CX 1617 at 12). Mitsubishi entered into a February 1998 RDRAM license that specifies a 2.5% royalty rate on Rambus DRAMs, 3% for Rambus processors, and 5% for Rambus ASICs and Peripherals. (CX 1609 at 11). AMD {

} (Heye, Tr. 3919-20 (*in camera*); CX 1420 at 8 (*in camera*)).

The proposed finding also misrepresents the testimony of Joel Karp. Mr. Karp did not testify that "JEDEC members considered TI's offer of a 1% royalty rate on a packaging technology to be unreasonable and therefore rejected TI"s technology as a standard." (CCFF 2450 (citing CX 2078)). Rather, when asked whether JEDEC found it unreasonable that TI promoted a standard without disclosing issued patents that read on that standard then, after standardization, requesting a 1% royalty, Mr. Karp testified, "Actually, I can't answer that because – because I don't know that that was the only reason or that that was the reason why the standard was rejected. The standard was rejected by the JEDEC members, but I don't recall any – I don't recall a reason being put with that, but it was rejected." (CX 2078, Karp Dep. at 139-40).

2451. During negotiations with Rambus over licensing terms and royalty rates for

RDRAM, many companies sought better terms. (RX0829 at 1-2 (Micron considered ways to negotiate a lower royalty rate from Rambus in 1997.); CX0913 at 1 (On December 3, 1996, David Mooring wrote: "Steve, Jeff, and I met with more than a dozen IBM DRAM apps... They have all TI's IP concerns, but worse. . . They asked lots of suspicious questions on our IP, patent pooling, and biz model. . . . He assured me that they are seriously considering Rambus. But the IP thing is a real dilemma."); CX0974 at 1 (On December 1, 1997, Geoff Tate wrote: "On royalty reduction we tried several trial discussions with major dram partners and NONE were willing to trade royalty reductions for CHANGES IN BEHAVIOR: all said give me lower royalty and I'll be more motivated, but weren't willing to commit [ ] to specific commitments...")).

Rambus's Response to Finding No. 2451:

The proposed finding is incomplete. While DRAM manufacturers naturally sought better term in their negotiations with Rambus for RDRAM licenses, DRAM manufacturer agreed to pay royalties of ranging from 2% to 5% for Rambus technologies in various types of products. (*See* RRFF 2450).

2452. DRAM manufacturers might have considered a royalty rate of substantially less than 1% for a main memory device to have been acceptable. (RX-855 at 1 ("0.1% royalty okay, 1-2% ridiculous)). Intel sought to persuade Rambus to offer a 0.5% royalty rate to those DRAM partners that produced a sufficient volume of RDRAM. (CX0952 at 2 ("[Intel] want[s] us to have license deals that...have long term reduction of royalty based on volume going to less than ½% for rdrams (at this point I choked/gasped).")).

Rambus's Response to Finding No. 2452:

The proposed finding is misleading and contradicted by more reliable evidence. The evidence shows that DRAM manufacturers have in fact agreed to pay royalty rates well over 1% for main memory devices. In fact, DRAM manufacturers agreed to pay royalties ranged from 2% to 5% for the use of Rambus's technologies in RDRAM related products. (*See* RRFF 2450).

2453. DRAM manufacturers were particularly concerned with royalty rates once production reached high volume. (CX0768 at 1 (in order to secure a contract with Samsung, Rambus agreed to a 0% royalty rate five years after the date on which Samsung had shipped the 500,000th unit of RDRAM)).

Rambus's Response to Finding No. 2453:

The proposed finding is misleading and incomplete. First, it cites only one RDRAM license. Other RDRAM licensees did not have provisions that had royalty rates that decreased with volume. (*See, e.g.*, CX 1609 at 11 (Mitsubishi license did not provide for lower royalty rates at high volumes); CX 1646 at 11 (Micron license did not provide for lower royalty rates at high volumes); RX 538 at 22 (NEC license did not provide for lower royalty rates at high volumes)). Second, the provision in the Samsung license agreement was a concession that Rambus gave in return for a commitment from Samsung for a continuing best efforts obligation. (CX 768 at 1). The rate drop therefore reflects a concession given by Rambus in return for a concession from Samsung, not necessarily a particular concern on Samsung's part. Moreover, the cited license agreement only reduces the royalty to 0% after the licensee, Samsung, first shipped 10,000,000 units then, 5 years after the shipment of another 500,000 units, the rate drops. (RX 518 at 23). The rate therefore only drops at very high volume marks.

2454. Intel was concerned that if Rambus did not offer a lower royalty rate, many DRAM companies would spend millions to develop alternative technologies that would have enabled them to avoid paying royalties to Rambus. (CX0952 at 2).

Rambus's Response to Finding No. 2454:

The proposed finding is misleading and incomplete. The document cited states that one person at Intel, Mr. Gelsinger, suggested that Rambus should offer lower royalties based on volume and time to market so that DRAM companies would not seek alternatives. (CX 952 at 2). This sentiment was apparently not shared by Mr. Parker of Intel. (*Id.*) Moreover, when Intel entered into a license with Rambus for RDRAM, the contract effectively provided a cap of 2% for Rambus's RDRAM royalty – i.e., that any royalties over 2% paid to Rambus by other licenses

would go to Intel, not Rambus. (MacWilliams, Tr. 4824-25; RX 904 at 9). According to Intel's internal documents, this royalty rate was at a "supportable level." (RX 904 at 9). Further, Mr. Gelsinger's proposal was apparently in response to the DRAM manufacturer's concerted refusal to manufacture RDRAM parts in volume. (*See* RRFF 1802, 1808, 1813, 1840).

2455. Had Rambus disclosed, companies likely would have negotiated rates for SDRAMs and DDR SDRAMs aggressively at the time they negotiated RDRAM licenses. (CCFF 2456-2457).

Rambus's Response to Finding No. 2455:

The proposed finding is contradicted by the weight of the evidence. First, the evidence shows that ex ante negotiations would not have occurred. (*See* RRFF 2441). Second, the evidence shows that the DRAM manufacturers were in fact concerned that Rambus's patents would cover SDRAM, DDR, and SyncLink. (RPF 464-595). Yet, with one exception discussed below, the DRAM manufacturers did not negotiate with Rambus for licenses to these specific technologies prior to 1999-2000. For example, the evidence shows that in 1995, Mitsubishi was concerned that SDRAMs would infringe Rambus's patents. (*See* RPF 676-677, 693-702). But when Mitsubishi licensed Rambus's RDRAM technology in 1997, it did not include a provision in its license agreement that addressed SDRAM. (CX 1609). Similarly, although Micron was on record in as being concerned about Rambus's patents covering SyncLink and was informed that Rambus claimed dual-edge clocking (RX 663 at 2 ("Rambus says their patents may cover our SyncLink approach . . . . Micron is particularly concerned to avoid the Rambus patents"; RX 920 at 1), when it entered into an RDRAM license with Rambus in 1997 and later amended that agreement in 1999, it did not include any provision to license Rambus's intellectual property for these technologies. (CX 1646). This is likely because DRAM manufacturers were convinced

that Rambus's patents could not cover those technologies because of prior art. (*See* RPF 764-84). For example, Mitsubishi documents show that it found what it thought was prior art on Rambus's patents. (RX 660A at 3; RPF 776-77). Similarly, Micron documents show that it believed Rambus's patents would be invalidated by prior art. (RX 829 at 2).

2456. In 1994, Samsung had insisted upon rights to use Rambus technology in non-Rambus products as part of any RDRAM license. (CX0768 at 1 ("[W]e had to make some major concessions to win this one."; Rambus could not sue Samsung "for patent infringement on any non-Rambus memories UNLESS they are intentionally using Rambus Technology to compete with Rambus DRAMs.")).

Rambus's Response to Finding No. 2456:

The proposed finding is misleading and incorrect. The Samsung license agreement provides that Rambus would not sue Samsung for using Rambus intellectual property in non-RDRAM products provided that Samsung "does not intentionally use such non-assertion status granted to design, make and sell devices which compete with Rambus DRAMs and which utilize substantial portions of Rambus technology." (RX 518 at 19). The agreement did not give Samsung the "rights to use Rambus technology in non-Rambus products." (CCFF 2456). Rather, the license agreement provided that Rambus would not sue Samsung for the unintentional use of Rambus technologies in competing products. (RX 518 at 14). Moreover, this non-assertion clause was given in return for a commitment that Samsung exert its best effort to "make, cost-reduce and market Rambus DRAMs." (CX 768 at 1). If Samsung complied with its obligations, Rambus knew "it's unlikely we'll get any compensation if a few of our patent claims end up on SDRAMs," but if Samsung failed to do so, Rambus could "terminate the deal and go after them 100% for any infringement." (CX 768 at 1).

Samsung's failure to demand a clear provision allowing it to use Rambus technologies in

non-RDRAM products was likely due to its belief that Rambus's patents would be invalid. Prior to negotiating with Rambus, Samsung hired Dr. Betty Prince to give a presentation on Rambus's technology. (Prince, Tr. 9003-04). According to that presentation, "Many of the large systems houses believe that Rambus patents are challengeable by previous internal work and/or patents." (RX 2153 at 10). Thus, the presentation continued, "The early concern about the impact of the Rambus patents on the major systems houses seems to have diminished considerably." (*Id.*)

2457. In 1995, Hyundai insisted upon an "other use" (or "other DRAMs") clause in its RDRAM license in response to the possibility that Rambus might have patents relating to SyncLink. (CCFF 1548-50). Hyundai likely would have negotiated more aggressively for lower royalty rates if it had not viewed the "other DRAMs" provision to be "just an insurance program." (CX2107 at 99 (Oh, Dep.) ("At the time you entered into this license agreement, did you think that Hyundai would have to pay 2.5 percent royalties for Other DRAMs as specified in paragraph 5.3(a)(ii)? A: This is just an insurance program.")).

Rambus's Response to Finding No. 2457:

The proposed finding is misleading and incorrect. Hyundai's RDRAM license does provide that it would pay a royalty of 2.5% for the use of Rambus technologies in other DRAM. (CX 1600 at 3-4, 12). But the evidence does not support the proposition that Hyundai would have negotiated more aggressively. Dr. Oh testified that when Rambus asserted that SyncLink might infringe Rambus patents, Hyundai did not investigate the claim but rather sought the "other DRAM" provision in the RDRAM license agreement, thereby agreeing to pay 2.5% for the use of Rambus technologies in SyncLink parts. (CX 2108, Oh Dep. at 277-28). He further testified that Hyundai's practice is *not* to investigate the claims; Hyundai took Rambus's representation that SyncLink infringed a face value. (*Id.*) There is no reason to believe that Hyundai would have negotiated any differently had Rambus made the additional disclosures that Complaint Counsel contend should have been made.

Further, the evidence shows that in 1998, Hyundai and Rambus later negotiated a provision that would have provided a higher royalty rate for Rambus technologies incorporated in SDRAM, DDR, and SLDRAM. (RX 2275; CX 2108, Oh Dep. at 285-89). As an addendum to the 1995 RDRAM license agreement, Rambus proposed a provision that would have required that the parties negotiate a license for Rambus technologies in these types of parts that were "substantially higher than Rambus' royalty rates for Compatible DRAMs." (RX 2275 at 2; CX 2108, Oh Dep. at 285-89).

Finally, when Hyundai merged with LG to form Hynix, the emerging entity chose to continue under LG's license with Rambus, which did not have any clause that allowed Hynix to use Rambus's patented technologies in non-RDRAM uses. (CX 2105, Mooring Dep. at 265-66; Farmwald, Tr. 8242 (Hynix in litigation with Rambus)).

2458. In the mid-1990's, Micron, Infineon, and others would have had the opportunity during the course of negotiations for RDRAM licenses to negotiate aggressively with Rambus for rights to use Rambus technology in SDRAMs and DDR SDRAMs. (CCFF 2459-2464).

Rambus's Response to Finding No. 2458:

The proposed finding is misleading and incomplete. (*See* RRFF 2455).

2459. In the 1995-1997 time frame, Micron and Rambus had been involved in a series of license negotiations. (Appleton, Tr. 6335-37; Lee, Tr. 6612-15).

Rambus's Response to Finding No. 2459:

The proposed finding is incomplete. In January 1996, Micron was expressed great concern that SyncLink would infringe Rambus's patents. (RX 663 at 2). Its 1997 RDRAM license, however, does not have any provision allowing it to use Rambus technologies in SyncLink or any non-RDRAM part. (CX 1646). Micron was informed in 1997 that Rambus

claimed it had patents over dual-edge clocking. (RX 920 at 1). Yet when it negotiated an addendum to its RDRAM license in 1999, it made no provision to use Rambus technologies in DDR. (CX 1646 at 25-29). This is likely because Micron believed Rambus's patents would be invalidated by prior art. (RX 829 at 2).

2460. In 1997, Rambus and Siemens had been involved in contentious license negotiations. (CX0937 at 2 (On July 11, 1997, Mr. Mooring wrote, "In summary, Siemens' today is fiercely oppositional. After they sign the contract and we have started to support them, they should become at least neutral."). On July 23, 1997, Rambus and Siemens entered into an RDRAM license agreement. (CX1617 at 22).

Rambus's Response to Finding No. 2460:

The proposed finding is misleading and incomplete. The issue of contention in the Siemens/Rambus negotiations was Rambus's requirement that Siemens enter into a patent pool. (CX 939 at 1-2). Royalties were not the issue:

> We also explained to Siemens that with our RDRAM royalty cap of 2% (per the our contract with Intel) plus the patent pooling, the RDRAM will be the least royalty burdened DRAM. For example, Samsung is proud to have settled with TI for a billion dollars in royalty payments for DRAM patent infringement. On the other side, Samsung is going after Fujitsu and others for SDRAM interface patent infringement.

(CX 929 at 1-2).

Further, as early as 1992, Siemens engineers were concerned that SDRAM would infringe Rambus's patents. (*See* RPF 466-529). For instance, an April 1992 memorandum from Willi Meyer, Siemen's JEDEC representative, stated, "RAMBUS has announced a claim against

Samsung for USD 10 million due to the similarity of the SDRAM with the RAMBUS storage device architecture. For that reason, IBM is seriously considering to preemptively obtain a license as soon a possible (at an introductory price)." (RX 286A at 2). Mr. Meyer also prepared a chart that recognized that "2-bank" Sync DRAMs may fall under Rambus's patents, and he testified that he thought Rambus might obtain patents over synchronous DRAMs. (RX 289 at 1; CX 2088, Meyer Infineon Trial Tr. 4/26/01at 44). This is not surprising, earlier, in 1990, Siemens reviewed Rambus's technical descriptions and recognized that Rambus was using each of the four features at issue in this case. (*See* RPF 626-32). Mr. Meyer was also present at the September 1995 JEDEC meeting at which Richard Crisp gave a written response to concerns that Rambus's patents covered SyncLink that stated, "Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's considertation nor does it make any statement regarding potential infringement of Rambus intellectual property." (JX 27 at 1, 26). Despite these concerns and warning about Rambus patents affecting SDRAM, the four technologies in DDR, and SyncLink, the Siemen's RDRAM agreement did not include any provision for the use of Rambus technologies in any of these products. (CX 1617). This is likely because Siemens believed that Rambus's patents would be invalid due to prior art. (RPF 772-73).

2461. In the mid-1990s, Rambus likely would have considered seriously demands of negotiating partners for "other use" clauses in RDRAM licenses. (Farmwald, Tr. 8324 ("Well, a number of companies had been approaching us all along about nonconforming uses of Rambus, noncompatible uses of Rambus, so I believe we were starting to take it more seriously that that's something that we should consider pretty seriously. Intel was also pushing us pretty hard that they wanted a license to Rambus technology for nonconforming uses and we had to take them very seriously.")).

Rambus's Response to Finding No. 2461:

The proposed finding is misleading and incomplete. Dr. Farmwald's testimony refers to the "very late '90s," not the mid-1990s. (Farmwald, Tr. 8234). Through the 1990s, however, Rambus did consider granting licenses for noncompatible uses, but its "standard response" was that it would grant such a licenses only if the royalty rate was higher than its rate for RDRAM. (Farmwald, Tr. 8179). The reason was that Rambus gained benefits from its RDRAM licenses that it would not gain from noncompatible licenses. (Farmwald, Tr. 8179-80, 8241 ("If they're using compatible parts, it's a partnership. We're working with them. We get feedback. We get information. We get to work with customers.")).

2462. During the early and mid-1990's, Rambus was willing to make, and often made, concessions to potential RDRAM partners in order to conclude licensing agreements. (CX0543A at 23 (Draft Business Plan: "Of course the terms are negotiable. Rambus is willing to make concessions for additional commitments on the part of the IC licensee regarding press, or high visibility/high volume logic chips etc."); CX0711 at 61-62 (Crisp email proposing a DRAM royalty rate for Hyundai "declining to 1.25% after 50 million cum units ship"); CX0782 at 1 (Crisp email: "The issue that was raised by GM Han was that they felt our price was too high. . . I explained to them that they could make us a counter proposal telling us what they would like."); CX0765 at 1 (Tate email: "[W]e cannot get a samsung deal without something like the IP compromise we gave them. . . . I don't like the compromise but it's what we can get.")).

Rambus's Response to Finding No. 2462:

The proposed findings is incomplete. While Rambus was willing to make concessions to potential RDRAM customers, on certain issues Rambus held firm. (CX 939 at 1 (stating that Rambus would not back down on patent pooling requirement though it was the "largest" issue with Siemens)).

2463. Indeed, during the early-to-mid-1990's, when Rambus was facing financial pressures, Rambus even considered the possibility of licensing its technologies for use in SDRAMs for a flat cash payment. (CX0543A at 42 ("There are many potential deals we can do with current and future licensees to generate cash if we had a significant need . . .. As a final

example, we could approach manufacturers of Sync DRAMs with our patent portfolio and negotiate for a cash license payment."); *see also* CX0757 at 1 ("I wonder if we can play a game of getting NEC to belly up some dollars by negotiating an 'other use' license and get some bucks out of the deal in license fees and royalties.")).

Rambus's Response to Finding No. 2463:

The proposed finding is incomplete. Though Rambus's 1992 business plan states that, as a last resort, Rambus could consider licensing patent rights for Sync DRAMs, Rambus consistently sought royalties higher than its RDRAM rates for noncompatible uses. (*See* RRFF 2464).

2464. During the early and mid-1990's, Rambus likely would have had to accept a significantly lower royalty rate in exchange for JEDEC members knowingly incorporating technologies potentially subject to Rambus patent rights in the JEDEC SDRAM and DDR SDRAM standards. (CX1941 at 1 (Advising JEDEC of patent application . . . would license @ 1% royalty.")).

Rambus's Response to Finding No. 2464:

The proposed finding is contradicted by other more reliable evidence. First, the proposed finding assumes that parties would have negotiated with Rambus for SDRAM and DDR licenses before Rambus's patents issued in 1999. Despite concerns about Rambus's patents, however, none of the DRAM manufacturers sought licenses for rights to intentionally use Rambus's technologies in SDRAM or DDR. (*See* RRFF 2455).

Second, Mike Farmwald, one of Rambus's founders, testified at trial that, for a number of economic reasons, Rambus consistently sought royalty rates for noncompatible uses (such as SDRAM and DDR) that were higher than Rambus's rates for RDRAM. (Farmwald, Tr. 8179-80, 8241 ("If they're using compatible parts, it's a partnership. We're working with them. We get feedback. We get information. We get to work with customers.")). For instance, in negotiations

with Samsung in 1993, Rambus sought royalty rates for noncompatible uses that were higher than its RDRAM rates. (CX 2114, Karp Dep. at 301-02; RX 411 (notes of negotiations stating, "noncompatible royalties can never be less than compatible royalties"). The economic soundness of this approach was confirmed by Professor Teece. (Teece, Tr. 10534-35 (*in camera*)
({

}).

Third, the only evidence of what Rambus and a DRAM manufacturer agreed to as a royalty rate for the use of Rambus's technologies in a non-RDRAM product is Hyundai's license with Rambus, which specifies a 2.5% royalty rate for such use. (CX 1600 at 3-4, 12).

Fourth, there were no acceptable, noninfringing alternatives. (*See* RPF 785-1146). Rather, the evidence shows that, even putting aside performance issues, rational DRAM manufacturers would have accepted Rambus's SDRAM and DDR license rates because to do so was less costly than using any noninfringing alternatives. (*See* RPF 969-88, 1125-40).

2465. Paragraphs 2465 - 2499 are unused.

XII. Industry Participants Are Now "Locked In" to the JEDEC Standards.

2500. The DRAM industry, the industries that make components that work with DRAMs, and those that use DRAMs in their own products, are committed to both the SDRAM (CCFF 2501-505), and DDR SDRAM (CCFF 2506-526) standards. No individual DRAM manufacturer can switch from the current JEDEC standards for SDRAM or DDR SDRAM (CCFF 2527-562). The entire industry could eventually switch through JEDEC, but to do so would be costly and take years (CCFF 2563-584).

Rambus's Response to Finding No. 2500:

As explained below, the proposed finding is not supported by the weight of the evidence. (*See* RRFF 2501-84).

A. The Industry Is Already Committed to the JEDEC Standards, and the Presence of the Technologies in Those Standards Is the Cause of Rambus Market Power.

1. The Industry is Committed to the SDRAM Standard.

2501. DRAM manufacturers were developing SDRAM by the mid-1990s. For example, Hyundai began its first SDRAM design in late 1992, and by 1994 had two different design teams working on 16M and 64M SDRAM designs. (CX2107 (Oh, Dep.) at 23, 34-35). Micron began design work on SDRAM by { }. (Shirley, Tr. 4209-11, *in camera*). Infineon began selling SDRAM in the mid-1990s. (Peisl, Tr. 4384-85). By 1999, SDRAM was nearly 80% of the worldwide DRAM market. (CX2747 at 31; McAfee, Tr. 7226-27; see DX141).

Rambus's Response to Finding No. 2501:

The proposed finding is misleading because it treats "SDRAM" as a single product. There are three different and incompatible standards that comprise SDRAM: PC66, PC100, and PC133. (Gross, Tr. 2348-56). PC100, for example, was not backward compatible with PC66. (Gross, Tr. 2352-53). Further, these different sub-standards required different complementary products such as chipsets. (Polzin, Tr. 4000-01). DRAM manufacturers first moved from producing PC66 to PC100 SDRAM products, and they later moved from PC100 to PC133. (CX2451 at 7 (Industry roadmap showing PC66 production in 1997, PC100 production in 1998,

and PC133 production in 1999); CX 2427 at 55 (Siemens document showing transitions from PC66 to PC100 to PC133 by market segment); CX 415 at 23 (AMI2 main memory forecast showing transitions from PC66 to PC100 to PC133)). As Joe Macri of ATI described it, moving from PC100 to PC133 was a "change from one standard to the next." (Macri, Tr. 4632 ("Now, in the figure below, there are arrows going from boxes with the terms PC-100, PC-133 . . . those boxes represent . . . the JEDEC standards. Is that accurate? A. Yes. Q. And what do the arrows represent? A. They represent the change *from one standard to the next*." (emphasis added)).

These different sub-standards were developed through different means. Because the JEDEC SDRAM standard led to the production of incompatible parts, Intel developed the PC100 SDRAM specification in 1996. (MacWilliams, Tr. 4907-09). As stated in that standard, it "define[s] a new Synchronous DRAM specification ('PC SDRAM') which will remove extra functionality from the current JEDEC standard specification, so that it will be a 'fully compatible' device among all vendor designed parts." (RX 2103-14 at 9). The Intel PC SDRAM specification also set forth the standards for PC66. (MacWilliams, Tr. 4908; RX 2103-14 at 60-61). Later, a small group of DRAM manufacturers and OEMs developed the PC133 standard. (MacWilliams, Tr. 4912-13).

Further, each of these sub-standards is produced by DRAM manufacturers in several different configurations. For instance, Infineon's 2002 product information guide indicates that Infineon intended to produce 27 different types of SDRAM (different densities, different organizations, and different sub-standards). (CX 2466 at 6-7).

2502. Computer and system companies began committing themselves to SDRAM by

1996. For example, Compaq computer began using SDRAM in 1997. (Gross, Tr. 2275). Hewlett Packard began work on the memory subsystem for the "Superdome" Server in 1996. That server which uses up to 128 CPUs and took over 5 years to design. HP's Superdome server uses SDRAM. (Krashinsky, Tr. 2778-81).

Rambus's Response to Finding No. 2502:

The proposed finding is misleading in that it treats SDRAM as a single product. This leads to the fallacious implication that "SDRAM" products never change. Compaq started using products compliant with Intel's PC66 SDRAM standard in 1997. (Gross, Tr. 2348-49). In 1998, Compaq began to use products compliant with Intel's PC100 SDRAM standard. (Gross, Tr. 2350-51). In 1999, Compaq began to use products compliant with Intel's PC133 SDRAM standard. For its Superdome server, HP uses another type of SDRAM product that operates at 125 MHz. (Krashinsky, Tr. 2810).

Further, the proposed finding is misleading to the extent that its use of the word "committing" it implies that computer and system companies could not change to different or alternative standards. The evidence shows that such transitions occur with great frequency. Within seven years, for example, Compaq shifted from EDO DRAM to PC66 to PC100 to PC133 to DDR266 to DDR333. (RPF 1322-28). Similarly, between June 1999 and May 2003, systems using AMD's K7 switched from using PC100 to PC133 to DDR200 and 266 to DDR333 to DDR400. (RPF 1311-20).

2503. Changing the memory subsystem, even in 2000, in response to changes to the SDRAM standard would have been "disastrous" for HP. (Krashinsky, Tr. 2782-84).

Rambus's Response to Finding No. 2503:

The proposed finding is not supported. While it accurately quotes Mr. Krashinsky, on cross-examination Mr. Krashinsky admitted that he had never prepared a budget for a memory

subsystem and that he had never done any cost estimates for changes to a memory system. (Krashinsky, Tr. 2801-02). He therefore had no basis to support his assertion.

2504. Companies using SDRAM other than computer and system companies have also committed themselves to SDRAM. For example, approximately 80% of the DRAM used by Cisco for its network switches is currently JEDEC-compliant SDRAM. (Bechtelsheim, Tr. 5861-62).

Rambus's Response to Finding No. 2504:

The proposed finding is misleading in that is treats SDRAM as a single product. (*See* RRFF 2502). The proposed finding is also misleading to the extent "committed" implies an inability to change to a different or slightly different DRAM standard. (*See* RRFF 2502).

2505. If the DRAM manufacturers had chosen to redesign SDRAM in response to the Rambus lawsuits, the cost to Cisco alone to adapt to that change would be in the range of $1 billion. (Bechtelsheim, Tr. 5881-82). It would have taken Cisco at least a year to make the transition to the new DRAM standards once those standards had been established. (Bechtelsheim, Tr. 5884 ("[W]e can only start the work once we know what the specification is.")).

Rambus's Response to Finding No. 2505:

The proposed finding is misleading. Mr. Bechtelsheim testified that it would cost $1 billion if Cisco had to redesign and requalify all of the 1500 different PC board assemblies produced by Cisco that contain DRAM. (Bechtelsheim, Tr. 5881-82). On cross-examination, however, Mr. Bechtelsheim admitted that no one has ever suggested to him that Cisco would not be able to continue to sell products that use SDRAM. (Bechtelsheim, Tr. 5890). He further admitted that the only discussion he has ever had with other managers at Cisco regarding a change to SDRAM was a discussion of the "absolute worst case," yet no one has ever suggested that would actually occur. (Bechtelsheim, Tr. 5890-91). He admitted that no company, not even Micron, Infineon, or Hynix – the three DRAM manufacturers in litigation with Rambus – ever

suggested any concern that they would not be able to supply Cisco with SDRAM. (Bechtelsheim, Tr. 5892-93).

The evidence shows that DRAM industry participants would not have had to go through the "worst case" scenario posited by Mr. Bechtelscheim. The DRAM industry goes through natural transitions from one standard to the next all of the time. (*See* RPF 1308-32). Within seven years, for example, Compaq shifted from EDO DRAM to PC66 to PC100 to PC133 to DDR266 to DDR333. (RPF 1322-28). Similarly, between June 1999 and May 2003, systems using AMD's K7 switched from using PC100 to PC133 to DDR200 and 266 to DDR333 to DDR400. (RPF 1311-20). In fact, Mr. Bechtelscheim testified that Cisco is right now – over three years after Rambus's patents issued and it began to start demanding royalties – starting a transition to DDR. (Bechtelscheim, Tr. 5860). Alternative technologies could be incorporated during one of these transitions. (Soderman, Tr. 9418; Geilhufe, Tr. 9675). Such a transition would not require Cisco to redesign all 1500 of its PC board designs. In fact, Complaint Counsel's economic expert admitted that switching away from Rambus's technologies in SDRAM to alternatives (if acceptable, noninfringing alternatives were in fact available) would only require the same categories of switching costs as those incurred by the industry in switching from SDRAM to DDR or from PC100 to another grade of SDRAM. (McAfee, Tr. 7714-15, 11357).

2. The Industry Is Committed to the DDR SDRAM Standard.

2506. The industry is phasing out SDRAM in favor of DDR. (McAfee, Tr. 11227; Rapp, Tr. 10161; *see,* Gross, Tr. 2275; DX-0219).

Rambus's Response to Finding No. 2506:

The proposed finding is misleading because it treats "SDRAM" and "DDR" as single products. The evidence shows that SDRAM encompasses three different sub-standards and multiple types of products. (*See* RRFF 2502). The same is true for DDR. There are multiple sub-standards for DDR – DDR200, DDR266, DDR333, and DDR400. (RPF 1313-19). Each of these sub-standards of DDR utilizes different complementary products; each needs to be matched with different chip sets and different motherboards; some need different DIMMs. (RPF 1313-19; Polzin, Tr. 4006-07, 4049 ("Q. Did that improvement in performance from the 200 to 266 and the 266 to 333 and the 333 to 400, did that have any implication for your chipset or motherboard suppliers and partners? A. Yes. Our chipset partners needed to design faster circuitry in their chipsets and our motherboard partners needed to adhere to stricter design rules in their manufacture of their motherboards.")).

Each of these sub-standards is produced by DRAM manufacturers in several different configurations. For instance, Infineon intended to produce 34 different types of DDR in 2002 (different densities, different organizations, and different sub-standards). (CX 2466 at 5).

2507. Currently, only 20% of the DRAMs that HP buys are SDRAM. (Gross, Tr. 2274). Because SDRAM is phasing out as the dominant standard DRAM, HP procures SDRAM only for mature products. (Gross, Tr. 2275 ("Our newer models incorporate DDR")).

Rambus's Response to Finding No. 2507:

The proposed finding is misleading and incomplete. It treats "SDRAM" as a single product and "DDR" as single product, but each of these standards encompasses multiple sub-standards and multiple products. (*See* RRFF 2501, 2506).

2508. Today, 80% of the DRAMs purchased by HP are DDR SDRAM. (Gross, Tr.

2274-75). As one of the largest PC manufacturers in the world, HP procures between 12 and 15 percent of the world's output of DRAM. (Gross, Tr. 2272-75). HP will spend approximately $3 billion on DRAM in 2003. (Gross, Tr. 2277). Approximately 95 percent of the DRAM purchased by HP is for computers. (Gross, Tr. 2272). However HP also procures DRAM for other products such as printers, cameras and camera accessories. (Gross, Tr. 2273).

Rambus's Response to Finding No. 2508:

The proposed finding is misleading and incomplete. It treats "SDRAM" as a single product and "DDR" as single product, but each of these standards encompasses multiple sub-standards and multiple products. (*See* RRFF 2501, 2506). Compaq/HP, for example, shifted from using PC133 SDRAM to DDR266 in 2001. (Gross, Tr. 2354). It switched to using DDR333 in 2002. (Gross, Tr. 2356).

2509. DRAM manufacturers and other firms have been preparing to manufacture and use DDR SDRAM since at least 1997. By the end of 1998, 64-megabit DDR SDRAM was available from 8 DRAM suppliers, 128-megabit DDR SDRAM was available from one supplier, and 256-megabit DDR SDRAM was available from 2 DRAM suppliers. (CX0303 at 9).

Rambus's Response to Finding No. 2509:

The proposed finding is incomplete and not supported by the weight of the evidence. First, the proposed finding improperly treats DDR as a single product when the evidence shows that "DDR" consists of several sub-standards and multiple products. (*See* RRFF 2506). Further, the statistical evidence shows that DDR (in any form) was not purchased in the market until 2000 when all types of DDR accounted for 0.4% of DRAM revenue. (RPF 1274). In 2001, all types of DDR accounted for only 5.3% of DRAM revenue. Compaq/HP did not start using any DDR product until 2001. (Gross, Tr. 2354). AMD did not produce K7 systems that worked with DDR (specifically, DDR200 and 266) until September 2000. (Heye, Tr. 3805-10; Polzin, Tr. 3998-4005).

2510. IBM began design work on its first DDR SDRAM chip in late 1996 or early 1997. (G. Kelley, Tr. 2589). Although the standard was not yet completed, DRAM designers were designing the basic architectures of their DDR SDRAM chips and adding features as information regarding those features became available from JEDEC. (G. Kelley, Tr. 2591).

Rambus's Response to Finding No. 2510:

The proposed finding improperly treats DDR as a single product when the evidence shows that "DDR" consists of several sub-standards and multiple products. (*See* RRFF 2506). Further, the proposed finding inaccurately portrays the evidence; the "features" that IBM was able to add later in the design process were "control features," i.e., the types of features at issue in this case:

> We could begin the DRAM before JEDEC information became finalized because most of the DRAM is not the control features that are decided at JEDEC. Most of the DRAM is the memory array, and all of that is going to be the same regardless of what the JEDEC feature/function requirements are and we could add those control features as JEDEC began to make decisions late in the design process.

(Kelley, Tr. 2590; Guilhufe, Tr. 9559 (four features at issue are in the peripheral circuitry, not the memory array)). In other words, the type of design work that would encompass the Rambus technologies at issue in this case would have occurred late in the process. This also shows that the majority of the design work done for DDR products was not dependent on and did not involve the "JEDEC feature/function requirements" – the majority of the design work would be "the same regardless" of those features and functions, which could be added or changed late in

the process. (*See* Kelley, Tr. 2590; Geilhufe, Tr. 9559).

2511. Micron has been designing DDR SDRAM chips since { }. (Shirley, Tr. 4209-11, *in camera*). By March of 1998, Micron had already planned production of DDR SDRAM chips for the fourth quarter of 1998. (CX2718 at 26; Lee, Tr. 6721-22). By May of 1999, Micron was ramping production of its first generation 64-megabit DDR SDRAM. (CX2737 at 46). By the time that Rambus began suing the DRAM manufacturers, Micron had already made considerable investments in both SDRAM and DDR SDRAM. (Appleton, Tr. 6386).

Rambus's Response to Finding No. 2511:

The proposed finding is misleading in that it treats "SDRAM" and "DDR" as single products while the evidence shows that each consists of several sub-standards and multiple different products. (*See* RRFF 2501, 2506). Further, the proposed finding is incomplete because the evidence shows that no type of DDR was used in the market until 2000 and all types of DDR accounted for only 5.3% of DRAM revenue in 2001. (*See* RRFF 2509)

2512. Once Micron became committed to the standards it is virtually impossible to change to another standard. Micron would have to incur costs to change from the current standard to a new standard, and changing the standard would require that the DRAM manufacturer's customer base change from the current standard. (Appleton, Tr. 6386-87, 6399-6400 ("It's virtually impossible to make that kind of a change after you go through the development and the investment.")).

Rambus's Response to Finding No. 2512:

The proposed finding is not supported by the weight of the evidence. The proposed finding rests solely on the testimony of Steve Appleton, the CEO of Micron, who admitted on cross-examination that he has never given any direction to the engineers at Micron to try to design its products to avoid Rambus's patents. (Appleton, Tr. 6408). Nor has he assigned any Micron engineers to try to eliminate any of the four Rambus technologies. (Appleton, Tr. 6411). Nor is he aware of any Micron engineers who have been trying to do so. (Appleton, Tr. 6411). Yet Brian Shirley, Design Operations Manager for Micron, testified that Micron routinely

redesigns its DRAM products and routinely introduces new DRAM products. He testified Micron is {

} (Shirley, Tr. 4282 (*in camera*)). Between 1995 and 1997, Micron taped out {

} (Shirley, Tr. 4218 (*in camera*)). In 1998, {

} (Shirley, Tr. 4218-19, 4226 (*in camera*)). In 1999, {

}

(Shirley, Tr. 4220-23, 4225-26 (*in camera*)). In 2000 and thereafter (after Rambus's patents issued) this trend continued. In 2000, {

} (Shirley, Tr. 4223-25 (*in camera*)). In 2001, { } (Shirley, Tr. 4227 (*in camera*)). In 2002, {

} (Shirley, Tr. 4228-29 (*in camera*)). In other words, after 2000, Micron has continued to tape out {

} products. Within "SDRAM" and "DDR" products, of course, there are several sub-standards - PC66, PC100, PC133, DDR200, DDR266, DDR333, and DDR400. (*See* RRFF 2501, 2506). Micron could have incorporated alternatives to Rambus's technologies (if they exist) at the time these new products were designed. (Geilhufe, Tr. 9674-75). According to Steve Polzin at AMD, during a transition from one DRAM standard to another, alternatives could be incorporated "costlessly." (Polzin, Tr. 4042).

Further, internal Micron documents show that changing DRAM standards is not difficult.

In a December 1996 "response script" prepared by Micron, the company represented that switching from one DRAM standard to another "involves only changing priorities in design and product engineering and may mean some differences in our assembly and test equipment purchases." (RX 836 at 3). The script went on to state that different DRAM standards "all use the same fab equipment and core DRAM technology. In short, while the flavors might change, it's still a DRAM." (*Id.*)

2513. Infineon began design of its first DDR SDRAM product in early 1998. (Peisl, Tr. 4377-78). By March of 2000, Infineon was ramping up volume production of its first DDR product. (Peisl, Tr. 4454).

Rambus's Response to Finding No. 2513:

Rambus has no specific response.

2514. In 2000, Infineon was not capable of removing the technologies claimed by Rambus from DDR SDRAM. (Peisl, Tr. 4444 ("In 2000, ... it would have been very hard and very costly and I would say near impossible to go back and to implement any changes back in the 2000 time frame.")).

Rambus's Response to Finding No. 2514:

The proposed finding is not supported by the evidence. The proposed finding rests solely on the testimony of Martin Peisl, who, in 2000 was in technical marketing, not DRAM design or manufacturing, and who admitted that when he became aware of Rambus's issued patents and its requests for royalties did nothing because "[t]hat was not my job." (Peisl, Tr. 4365-66, 4459). Further, after receiving an email stating that Rambus was considering suits against the whole industry (RX 1613 at 1), Mr. Peisl made no investigation to determine whether Infineon's products actually infringe because it was "not my job." (Peisl, Tr. 4471-73). Nor was Mr. Peisl aware of any effort by Infineon to design around Rambus's patents. (Peisl, Tr. 4535).

Accordingly, Mr. Peisl had no basis to say how difficult it would have been for Infineon to remove the Rambus technologies from Infineon's "DDR" products; he never considered the issue nor is he aware of any effort at Infineon to deal with the question.

The proposed finding is also misleading in that it improperly treats DDR as a single product when the evidence shows that "DDR" consists of several sub-standards and multiple products. (*See* RRFF 2506). It is not clear which of the "DDR" sub-standards the finding is referring to. The evidence shows that Infineon produces multiple DDR products. In the last two quarters of 2002 *alone*, Infineon was introducing 17 new DDR products (i.e., new DDR200, DDR266, DDR333, and DDR400 devices in different densities and configurations). (CX 2466 at 5-6). In addition, in 2002, Infineon was phasing out as "End of Life" 2 DDR products (different configurations of DDR200). (*Id.*)

2515. Hyundai has been designing DDR SDRAM chips since 1997. (CX2107 at 122-123 (Oh, Dep.)). By April of 1999, a Hyundai 64-megabit DDR SDRAM chip had finished successful testing in customer systems. (CX2334 at 22; Tabrizi, Tr. 9211). That chip had engineering samples by November of 1998, and was in mass production by March of 1999. (CX2334 at 20). Design work on Hyundai's 256-megabit DDR SDRAM product began by August of 1999. (CX2108 at 202 (Oh, Dep.)).

Rambus's Response to Finding No. 2515:

The proposed finding is misleading and not supported by the weight of the evidence. Dr. Oh testified that design work on Hyundai's first DDR product (a 64Mb part) began in December 1997 and was in mass production by August 1998. (CX 2108, Oh Dep. at 237 ("Q. And was that first DDR part the 64-meg DDR part? A. Yes. Q. And just to make sure that I've got the timing right, did you say that design work on that part began in December of 1997? A. Yes. Q. And then mass manufacture of that part began in -- was it August or September of

1998? A. August 1998.")).

The proposed finding is also misleading because it improperly treats DDR as a single product when the evidence shows that "DDR" consists of several sub-standards and multiple products. (*See* RRFF 2506). It is not clear which of the "DDR" sub-standards the finding is referring to.

2516. Once customers started to use DDR SDRAMs, it was too late for Hyundai to change its DRAMs to avoid the Rambus patents. (CX2108 at 231-32 (Oh, Dep.) ("[I]t's impossible, almost impossible.")).

Rambus's Response to Finding No. 2516:

The proposed finding is not supported by the weight of the evidence. Dr. Oh, on whose testimony the proposed finding rests, left Hyundai in 1999. (CX 2107, Oh Dep. at 13). Further, he testified that Hyundai's transition from SDRAM to DDR was rapid and easy. (CX 2108 at 237 ("Q. And just to make sure that I've got the timing right, did you say that design work on that part began in December of 1997? A. Yes. Q. And then mass manufacture of that part began in -- was it August or September of 1998? A. August 1998. Q. August 1998. And I believe you testified that *this was a relatively fast time frame because it was pretty easy to go from SDRAM to DDR SDRAM; is that right*? A. Yes." (emphasis added))). Further, the evidence shows that DRAM manufacturers routinely switch to producing new types of DRAM and routinely switch to new DRAM standards. (*See* RPF Section X.A).

The proposed finding is also misleading because it improperly treats DDR as a single product when the evidence shows that "DDR" consists of several sub-standards and multiple products. (*See* RRFF 2506). It is not clear which of the "DDR" sub-standards the finding is referring to. Hyundai's internal business plans show that it intended to migrate from PC133 to

DDR266 to DDR333 to DDR400. (CX 2334 at 3).

2517. AMD had made the decision to design its chip-sets for DDR in early 1999. (CX2158 at 2). At that time, AMD could have implemented alternatives to the Rambus claimed technologies. (Polzin, Tr. 4042). However, by the time AMD was approached by Rambus in 2000, AMD was already in the middle of the product launch for its DDR-compatible chipset. (Polzin, Tr. 3989-990 ("[The Rambus patents] were pretty simple things to work around if we had known about them a long time ago, but we were in the middle of ramping up an infrastructure. This was just when we were trying to get ... the first DDR motherboards out the door.... The work arounds that were obvious required some big changes to the device, to the chipsets, to the motherboards, et cetera.... The bottom line is any change when you are trying to do a production ramp is extremely difficult....")).

Rambus's Response to Finding No. 2517:

The proposed finding is incomplete. AMD started to ship is K7 processors with a newly designed 266 MHz front side bus and a newly designed AMD 760 chipset in October 2000. (Polzin, Tr. 3998-4005). This chipset was compatible with DDR200 and DDR266 devices. (*Id.*) In October 2002, AMD launched a new version of its K7 processor with a 333MHz front side bus. (*Id.*) This required third party chipset vendors to design and produce a new chipset that would support DDR333 and third party motherboard manufacturers to design compatible boards. (Polzin, Tr. 3998-4005, 4049-50). Seven months later, AMD launched a new version of its K7 processor with a 400 MHz front side bus, and third party vendors designed, produced, and launched compatible chipsets and motherboards that would support DDR400. (*Id.*) Alternatives to Rambus's technologies could have been adopted during these changes. (Geilhufe, Tr. 9675). According to Steve Polzin at AMD, the Rambus technologies were "pretty simple things to work around," and alternatives could be incorporated "costlessly" during a transition to another iteration of DRAM. (Polzin, Tr. 3989, 4042).

2518. By September of 1999, most leading graphics controllers either were supporting or planned to support DDR SDRAM. (CX2747 at 58, 65).

Rambus's Response to Finding No. 2518:

The proposed finding is misleading because it improperly treats DDR as a single product when the evidence shows that "DDR" consists of several sub-standards and multiple products. (*See* RRFF 2506). This is even more true for graphics controllers because the specifications for graphics DRAM are often different from the standard types of DRAM used in other applications. (Wagner, Tr. 3865 ("Q. And often times what they provide you is something that is not JEDEC – is not within the JEDEC specifications? A. Correct."); Wagner, Tr. 3835-36 ("Q. Do you have an understanding of whether the DRAM used with nVidia's graphics processors are always JEDEC compliant? A. The graphics processors are not necessarily compliant in a true JEDEC sense. . . .")).

2519. By { } September 2000, ATI had graphics cards already shipping that included DDR SDRAM. (CX1383 at 49, *in camera* (Macri, Tr. 4756, *in camera*)). Changing its products { } was not a reasonable possibility. (*See, e.g.,* Macri, Tr. 4767, *in camera* ("[T]he cost to the company in terms of engineering resources would have affected our product plans well into the future, as well as disrupting the current products we were shipping. I mean, it would have been ... very chaotic to our business and the expense would have been huge.")).

Rambus's Response to Finding No. 2519:

The proposed finding is not supported by the weight of the evidence. The proposed finding rests entirely on the say-so of Joe Macri, who admitted on cross-examination that { } (Macri, Tr. 4786 (*in camera*)). In fact, he admitted that { }. (*Id.*) He also admitted that after { }. (Macri, Tr. 4783 (*in camera*)). Nor did he {

}. (Macri, Tr. 4783-84 (*in camera*)).

Moreover, the evidence shows that Mr. Macri led the Future DRAM Task Group, which adopted all four of the Rambus technologies for the DDR2 standard despite full knowledge of Rambus's issued patents and its requests for royalties. (*See* RPF 746-63). This shows that there were no acceptable alternatives for Rambus's technologies. The most glaring example of this is Rambus's programmable burst length technology. The preliminary DDR2 specification, which was published in July 2001 (at least one and a half years after Rambus's patents issued and it began to demand royalties), specified a single fixed burst length, thereby avoiding Rambus's patents. (RX 1854 at 20; Macri, Tr. 4733-34). Yet at the September 2001 JC 42.3 meeting, with full knowledge of Rambus's issued patents and its demands for royalties, the committee voted *unanimously* to amend the preliminary standard to *add* Rambus's programmable burst length technology. (CX 174 at 7-8). Further, the evidence shows that Mr. Macri himself was in favor of an alternative for Rambus's dual-edge clocking technology "if it works." The minutes of a November 2000 Future DRAM Task Group conference call show that Mr. Macri (on behalf of ATI) preferred "Single data rate" clocking. (CX 426 at 2). The overall consensus of the group was: "Single data rate clock is preferred provided that we can make it work." (CX 426 at 4). The Task Group, however, opted to incorporate Rambus's dual-edge clocking technology. (Polzin, Tr. 4047).

What is more, the evidence shows that members of the DRAM industry, especially graphics companies like ATI, are constantly switching to new DRAM standards. (*See* RPF 1308-32; Wagner, Tr. 3875-76 (graphics company launched 14 new products in 6 years)). The

specifications for graphics DRAM are often different from the standard types of DRAM used in other applications. (Wagner, Tr. 3865 ("Q. And often times what they provide you is something that is not JEDEC – is not within the JEDEC specifications? A. Correct."); Wagner, Tr. 3835-36 ("Q. Do you have an understanding of whether the DRAM used with nVidia's graphics processors are always JEDEC compliant? A. The graphics processors are not necessarily compliant in a true JEDEC sense. . . .")).

2520. Graphics cards using DDR-compatible graphics processors from graphics chip designer NVidia began to ship in the fall of 1999. NVidia began work on those chips approximately two years earlier in 1997. (Wagner, Tr. 3840-41). Currently, nearly all graphics cards used with NVidia's processors ship with DDR. (Wagner, Tr. 3844).

Rambus's Response to Finding No. 2520:

The proposed finding is misleading and not supported. The evidence shows that nVidia graphics cards were not compatible with "standard" DDR products. (Wagner, Tr. 3835-36 ("Q. Do you have an understanding of whether the DRAM used with nVidia's graphics processors are always JEDEC compliant? A. The graphics processors are not necessarily compliant in a true JEDEC sense. . . .")). Moreover, nVidia often sought to have DRAM manufacturers produce non-standard DRAM for its graphics processors. (Wagner, Tr. 3865 ("Q. And often times what they provide you is something that is not JEDEC – is not within the JEDEC specifications? A. Correct.")). For nVidia, performance and a second source were more important than using industry standards DRAM:

> Q. In the next paragraph under general – I'm sorry, in that same paragraph, under general targets, is the statement that "JEDEC is a nice-to-have, but more important is to have a second source which provides compatible

products." And I believe I misstated, it's in the next paragraph. Do you see that?

A. Yes.

Q. Does this passage accurately state your understanding of nVidia's interests in the importance of JEDEC for this particular DRAM chip?

A. For this particular DRAM chip, yes. We participate in JEDEC to try to drive our requirements in, but in the graphics space, for the highest performance devices, we know JEDEC is not going to be the one defining that requirement, they focus on the dims at a much lower speed, therefore if we can get it out of JEDEC, that would be great, but the reality is we have to do it ourself.

(Wagner, Tr. 3849; CX 2828 at 7).

2521. By the time Rambus began suing the DRAM manufacturers for the use of the technologies in the JEDEC standards, it was too late for NVidia to remove those technologies from its own products. (Wagner, Tr. 3862-63 ("We were trying to launch products into the market and if the standard was going to change, that meant we had to change our development plan and go change to something new that was yet undefined. For us it's a painful process to go through and not be able to release a product that's basically ready to be released and have to start over again.")).

Rambus's Response to Finding No. 2521:

The proposed finding is not supported. First, nVidia used non-standard DRAM. (*See* RRFF 2520). Second, on cross-examination, Mr. Wagner (on whose testimony the proposed finding rests) testified that he was not aware of the specifics of Rambus's patent claims until "some time around getting asked to participate in this trial." (Wagner, Tr. 3867-68). More important, Mr. Wagner testified that nVidia would leave it up to the memory vendors as to whether to change the standards:

Q. So, when Mr. Davis asked you if you ever went to JEDEC and

proposed that they changed the standard with respect to programmable CAS latency or programmable burst length or dual edge clock, when is the first time that you even knew those issues might be involved in the lawsuit?

A. At some point, I don't recall exactly what year, memory vendors came to us and said would you like to change this, we're finding some IP issues over it, and our feedback was, well, if the industry is going to change, we need to change with it and we basically left it up to them to go off and decide to change or not.

(Wagner, Tr. 3868-69).

2522. IBM began development of memory interface units designed to be used in their servers with DDR SDRAM in the third quarter of 1997. (Kellogg, Tr. 5015). IBM began selling the p-Series servers, using DDR SDRAM, in December of 2001. Development on those servers began approximately three years earlier. (Kellogg, Tr. 5014-15). IBM was making inquiries to DRAM manufacturers regarding their 256-megabit DDR SDRAM chips as early as April of 1998. (CX2306), and was stating a preference of using DDR SDRAM in servers to DRAM manufacturers as early as November of 1997. (CX2264 at 2; Tabrizi, Tr. 9159-63).

Rambus's Response to Finding No. 2522:

The proposed finding is misleading in that it improperly treats DDR as a single product when the evidence shows that "DDR" consists of several sub-standards and multiple products. (*See* RRFF 2506). It is not clear which of the "DDR" sub-standards the finding is referring to.

2523. By August of 1997, a number of firms, including VIA, ALi and AMD were considering the development of DDR-compatible chipsets. (CX2297 at 76; CX2747 at 65). By February of 1998, Hyundai expected chipset support for DDR for main memory in high-end workstations and servers from IBM, HP, DEC, Sun and SGI. Additionally, Hyundai expected chipset support for DDR for main memory in PCs from VIA, AMD, SIS, ALi, and Opti. Hyundai expected chipset support for DDR in graphics memory from S3, Trident, ATI, and Intel's Chips and Technology division. (CX2303 at 19).

Rambus's Response to Finding No. 2523:

The proposed finding is misleading in that it improperly treats DDR as a single product when the evidence shows that "DDR" consists of several sub-standards and multiple products. (*See* RRFF 2506). It is not clear which of the "DDR" sub-standards the finding is referring to.

2524. HP was expressing interest to DRAM manufacturers in DDR SDRAM for its servers and high end workstations as early as July of 1997. (CX2294 at 11). HP had prototypes of a "four way" server, code-named Everest available in the third quarter of 2000. That product used DDR SDRAM. (Krashinsky, Tr. 2793). Work on that project began at HP prior to 2000. (Krashinsky, Tr. 2817).

Rambus's Response to Finding No. 2524:

The proposed finding is misleading in that it improperly treats DDR as a single product when the evidence shows that "DDR" consists of several sub-standards and multiple products. (*See* RRFF 2506). It is not clear which of the "DDR" sub-standards the finding is referring to.

2525. In 2000, HP did not support changes to the DDR standard to avoid the Rambus patents due to the costs such changes in the DRAM standard would have imposed on HP. (Krashinsky, Tr. 2794-95 ("[T]here was already a standard ... that was adopted at JEDEC and we were counting on it, and therefore we didn't support any changes again because HP does not want to support changes that will cause a lot of expenses to HP.")).

Rambus's Response to Finding No. 2525:

The proposed finding is misleading in that it improperly treats DDR as a single product when the evidence shows that "DDR" consists of several sub-standards and multiple products. (*See* RRFF 2506). It is not clear which of the "DDR" sub-standards the finding is referring to. Compaq/HP did not start to use any DDR products until it shifted from using PC133 SDRAM to DDR266 in 2001. (Gross, Tr. 2354). It switched to using DDR333 in 2002. (Gross, Tr. 2356). As of May 2003, it had not used DDR400. (Gross, Tr. 2356). Alternatives to Rambus's technologies (if they existed) could have been incorporated during this transitions. (Geilhufe, Tr.

9675). According to Steve Polzin at AMD, the Rambus technologies were "pretty simple things to work around," and alternatives (if they existed) could be incorporated "costlessly" during a transition to another iteration of DRAM. (Polzin, Tr. 3989, 4042).

2526. Approximately 15% of the DRAM used by Cisco for its network switches is currently JEDEC-compliant DDR SDRAM. (Bechtelsheim, Tr. 5861).

Rambus's Response to Finding No. 2526:

The proposed finding is misleading in that it improperly treats DDR as a single product when the evidence shows that "DDR" consists of several sub-standards and multiple products. (*See* RRFF 2506). It is not clear which of the "DDR" sub-standards the finding is referring to. Further, the evidence shows that, as of June 2003, Cisco is only beginning to use any "DDR" products. (Bechtelscheim, Tr. 5860).

B. No Individual DRAM Manufacturer Can Switch from the Rambus Claimed Technologies in Response to a Change in the Price of Those Technologies.

2527. For any individual DRAM manufacturer, changing its DRAM designs and manufacturing the new DRAM design would have been a costly and time consuming process. (CCFF 2528-540). Even if a DRAM manufacturer did attempt to switch, it would not be able to sell the new DRAM to most large DRAM customers unless that DRAM were produced by other DRAM manufacturers as well. (CCFF 2541-549). Finally, even if a number of DRAM manufacturers switched, they would not be able to sell their new DRAMs unless other firms, which manufacture complimentary components, agreed to switch as well. (CCFF 2550-562).

Rambus's Response to Finding No. 2527:

As explained below, the proposed finding is not supported by the weight of the evidence. (*See* RRFF 2528-62).

1. Changing the Designs for SDRAM and DDR SDRAM Products Would Be Expensive and Disruptive.

2528. Any attempt to change SDRAM and DDR SDRAM products in 2000 to work around Rambus's patents would have required changes to the product designs, followed by

layout, tape out, simulation and verification, the creation of a new mask set, manufacture of initial silicon, validation and qualification, and ramp up to full production. (*See* CCFF 46-65).

Rambus's Response to Finding No. 2528:

The proposed finding is incomplete. DRAM manufacturers routinely change product designs, do layouts, tape outs, simulations and verification, create new mask sets, manufacture initial silicon, validate and qualify, and ramp up to full production. (*See* RPF Section X.A.3). In the last two quarters of 2002 *alone*, Infineon was introducing *forty seven* new DRAM products: 17 new DDR products (i.e., new DDR200, DDR266, DDR333, and DDR400 devices in different densities and configurations), 15 new SDRAM products (i.e., new PC100 and PC133 devices in different densities and configurations), 4 new Graphics RAM products, 5 new Mobile-RAM products, and 6 new RLDRAM products. (CX 2466 at 5-9). In addition, in 2002, Infineon was phasing out as "End of Life" *fourteen* different DRAM products: 2 DDR products (different configurations of DDR200) and 12 SDRAM products (different configurations of PC100, PC133 and PC166). (CX 2466 at 5-6).

Similarly, between 1995 and 1997, Micron taped out { } (Shirley, Tr. 4217-18 (*in camera*)). In 1998, { } (Shirley, Tr. 4218-19, 4226 (*in camera*)). In 1999, { } (Shirley, Tr. 4220-23, 4225-26 (*in camera*)). In 2000, { } (Shirley, Tr. 4223-25 (*in camera*)). In 2001, { } (Shirley, Tr. 4227 (*in camera*)). In 2002, { } (Shirley, Tr. 4228-29 (*in camera*)).

Changes to incorporate alternatives to Rambus's technologies could have been

incorporated during the design of one of these new products. (Geilhufe, Tr. 9675).

2529. Any attempt to change the design of SDRAM and DDR SDRAM products to work around Rambus's patents in 2000 would have involved major expense and delay. (CCFF 66-77, 2530-540).

Rambus's Response to Finding No. 2529:

As explained below, the proposed finding is not supported by the weight of the evidence. (*See* RRFF 2530-40).

2530. In addition to the costs of the redesign itself, the additional costs of a revision design can be broken down into three primary types of costs: out-of pocket-costs, inventory costs, and opportunity costs. (Shirley, Tr. 4170).

Rambus's Response to Finding No. 2530:

The proposed finding is irrelevant. There is no testimony nor any other evidence that a "revision design" was necessary to adopt alternative technologies. The sole evidence cited for the proposed finding is the testimony of Brian Shirley. Mr. Shirley testified about various types of design work, including "new design," "derivative design," "design shrink," "configuration change," "cut-down," "flip-out," and "revision design." (Shirley, Tr. 4155, 4158-59). He never identified which of these types of design work, if any, would be necessary to adopt alternatives to Rambus's technologies. In contrast, the evidence shows that any effort to adopt alternatives could "piggyback" on other design effort that DRAM manufacturers perform all the time. (Geilhufe, Tr. 9675). According to Steve Polzin at AMD, during a transition from one DRAM standard to another, alternatives could be incorporated "costlessly." (Polzin, Tr. 4042). Accordingly, there is no evidence that the costs identified in the proposed finding have any relevance to the issues in this case. In contrast, Rambus's manufacturing expert did provide estimates of the costs necessary to adopt the various alternatives suggested by Complaint

Counsel. (*See* RPF X.B).

2531. A revision design involves taking an existing design and changing certain circuitry in that design. A revision design usually occurs only when a DRAM manufacturer has found something fundamentally wrong with a DRAM design project that has already made it to silicon. (Shirley, Tr. 4168).

Rambus's Response to Finding No. 2531:

The proposed finding is irrelevant. (*See* RRFF 2530).

2532. Out of pocket costs of a revision design involves the actual expenditures that a DRAM manufacturer must make in order to accomplish a revision design, particularly the costs of additional mask sets. (Shirley, Tr. 4170). Revision designs require a new set of masks. (Shirley, Tr. 4264). For Micron, as of the fourth quarter of 2002, the cost of a mask set for a DRAM currently in production is in the range of { }, corresponding to a range of { } micron process technologies. (Shirley, Tr. 4231-35, *in camera;* see DX40-DX41, *in camera*).

Rambus's Response to Finding No. 2532:

The proposed finding is irrelevant. (*See* RRFF 2530).

2533. For Micron, as of the fourth quarter of 2002, the total cost of mask sets required to fabricate SDRAM and DDR SDRAM was approximately { }. (Shirley, Tr. 4234-35, *in camera*; see DX40-DX41, *in camera*). In mid-2000, Micron had { } mask sets, including { } SDRAM mask sets and { } DDR SDRAM mask sets. The total cost of those mask sets to Micron was approximately { }. (Shirley, Tr. 4239-40, *in camera*).

Rambus's Response to Finding No. 2533:

The proposed finding is irrelevant. (*See* RRFF 2530). Further, the evidence shows that Micron is, in the regular course of business, constantly { } (Shirley, Tr. 4282 (*in camera*)).

2534. The inventory costs of a revision design relates to the DRAMs already produced, or those in process of being produced when the problem that led to the revision design was discovered. As a result, inventory costs include DRAMs that cannot be sold because of the problem, and the magnitude of those costs depend on the quantity of such DRAM. (See Shirley, Tr. 4206-7, *in camera*).

Rambus's Response to Finding No. 2534:

The proposed finding is irrelevant. (*See* RRFF 2530). Further, there is nothing stopping a DRAM manufacturer from continuing to sell DRAM incorporating Rambus technologies until it can transition to noninfringing alternatives. There would therefore be no lost inventory.

2535. In the fourth quarter of 2002, Micron finished { } DRAM chips per day, of which approximately { } were SDRAM and { } were DDR SDRAM. (Shirley Tr. 4237-39, *in camera*; see DX42, *in camera*). In mid-2000, Micron finished { } SDRAM chips per day. (Shirley Tr. 4241, *in camera*). It takes between 45 days and 55 days for a DRAM to go through the entire fabrication process, so DRAM manufacturers have between 45 and 55 days worth of "work in progress" inventory at any given time. (Shirley Tr. 4153, 4170). Micron also maintains an average of { } of inventory on hand at any given time. (Shirley Tr. 4238, *in camera*).

Rambus's Response to Finding No. 2535:

The proposed finding is irrelevant. There is nothing stopping a DRAM manufacturer from continuing to sell DRAM incorporating Rambus technologies until it can transition to noninfringing alternatives. There would therefore be no lost inventory.

2536. The opportunity costs of a revision design are the delay caused to other projects when a DRAM design team is pulled from their current project to work on the revision design. (Shirley Tr. 4207, *in camera*).

Rambus's Response to Finding No. 2536:

The proposed finding is irrelevant. (*See* RRFF 2530).

2537. Changing their production in order to introduce DRAMs that wouldn't infringe Rambus's patents would have required DRAM manufacturers to dedicate a substantial amount of resources from projects intended to improve their products. (Appleton, Tr. 6399-400, 6402-03 ("All companies have limited resources, and we have to apply those resources to the most productive path that we can. Simply taking those resources and applying them to do a technology that doesn't provide any additional advantage to the current technology that's being produced is an enormous cost."); Appleton, Tr. 6402-403; Heye, Tr. 3811-13)). In one case at Micron, the opportunity costs alone of a revision design were in the neighborhood of { }. (Shirley Tr. 4208-9, *in camera*).

Rambus's Response to Finding No. 2537:

The proposed finding is not supported by the weight of the evidence and is contrary to Complaint Counsel's other proposed findings. First, the evidence shows that any effort to adopt alternatives could "piggyback" on other design effort that DRAM manufacturers perform all the time. (Geilhufe, Tr. 9675). Second, there is no evidence that any costs associated with a "revision design" are relevant. (*See* RRFF 2530). Third, the evidence shows that the costs for a DRAM manufacturer to switch to alternatives to Rambus's technologies (if such alternatives were acceptable) is on the order of $4 million, including opportunity costs. (*See* RPF 1334-46). Fourth, Complaint Counsel's own proposed findings purport to show that paying Rambus's royalties imposes substantial costs on DRAM manufacturers that could be avoided by designing around Rambus's patents. (*See* CCFF 3100). Accordingly, if acceptable, noninfringing alternatives actually existed, switching to those alternative technologies would *lower* DRAM manufacturers' costs, which is the purpose of much of the redesign work performed by these manufacturers every day.

2538. Trying to redesign SDRAM and DDR SDRAM products to work around Rambus's patents at the same time that other design changes would not have been feasible because of the time required for the design changes and the added complexity of trying to combine a redesign with a shrink or a density change. (CCFF 2539-540).

Rambus's Response to Finding No. 2538:

The proposed finding is not supported. (*See* RRFF 2539-40).

2539. A DRAM manufacturer normally does not attempt to do two different types of changes at the same time. (Reczek, Tr. 4304-305; CX2108 at 257 (Oh, Dep.) ("We normally don't [redesign some of the internal circuitry at the time of a shrink] unless . . . [the part] has a big problem, if it does not work, then we do, but normally we don't do that.")). For example, when a DRAM manufacturer does a shrink, it does a shrink on a product that already exists so that there are fewer changes to track. (Becker, Tr. 1157-58 ("[F]or instance, when we went from

.24 [micron] to .20 [micron], we did that with the same 64-meg SDRAM. So, we did all of our product learning at 0.24 [micron], we had to do all of our process and technology learning at 0.2 [micron], but we did it with a product we already knew."); CX2108 at 254 (Oh, Dep.) (when doing a shrink, "You don't change anything" on the inside of the DRAM, "It has nothing to do with the circuit. No circuit change at all."), CX2108 at 257 (Oh, Dep.) (Hyundai's practice was not to modify its design at the time it did a shrink)).

Rambus's Response to Finding No. 2539:

The proposed finding is irrelevant. First, that DRAM manufacturers do not "normally" attempt to do two different types of changes at the same time does not preclude the possibility that a manufacturer could change two to four features in the peripheral circuitry of an SDRAM or DDR product at the same time as other redesign work is being done. (Geilhufe, Tr. 9675). According to Steve Polzin at AMD, during a transition from one DRAM standard to another, alternatives could be incorporated "costlessly." (Polzin, Tr. 4042). Second, even if it were not possible to adopt Rambus's technologies while making other changes, designing around Rambus's patents would allow DRAM manufacturers to avoid paying royalties to Rambus. Complaint Counsel's own proposed findings purport to show that paying Rambus's royalties imposes substantial costs on DRAM manufacturers that could be avoided by designing around Rambus's patents. (*See* CCFF 3100). Accordingly, if acceptable, noninfringing alternatives actually existed, switching to those alternative technologies would *lower* DRAM manufacturers' costs, which is the purpose of much of the redesign work performed by these manufacturers every day. The proposed finding is also not supported. (*See* RRFF 75-76).

2540. Trying to combine a redesign with a shrink or a change in density adds complexity to the effort because multiple changes makes it difficult to determine what has gone wrong if the DRAM has a defect. (Reczek 4304-4305 ("So, in the case you take two steps at one time, so this might lead to very big problems, and for example, if something is not working, you don't know whether the technology is not working or the design is not working. So, its very difficult to figure out what's really going on, what's really going wrong there.")).

Rambus's Response to Finding No. 2540:

The proposed finding is unsupported and irrelevant. (*See* RRFF 2539, 75-76).

2. Changes to the SDRAM and DDR SDRAM Standards to Avoid the Rambus Patents Would Lead To Products That Were Not Compatible with the Current Standards or with Other Components.

2541. A DRAM has value only if it is compatible with the other components in the products that include the DRAM. (Peisl, Tr. 4410 ("Interoperability [means] that the DRAM works flawlessly together with all the components in the system. It's not only one chip that the DRAM is interfacing with but all the other components on the motherboard, ... other components on the modules, for instance, like registers. You have to make sure your part is fully compliant with all the specifications of the other chips.")).

Rambus's Response to Finding No. 2541:

Rambus has no specific response.

2542. When Rambus began suing DRAM manufacturers, systems manufactures were concerned that DRAM manufacturers might attempt to change the existing SDRAM and DDR SDRAM standards because new standards might not have been compatible with the systems sold by those system manufacturers. (Heye, Tr. 3733-34 ("So, the concerns around that would have been first, it would have taken time to establish the new standards; depending on what they were, you would have had to change the memory component, the north bridge, possibly both, you would possibly have to change the motherboard. You may possibly have to change the [DIMM], once you've made all those changes, you would have to implement them,...")).

Rambus's Response to Finding No. 2542:

The proposed finding is misleading and incomplete. It treats "SDRAM" as a single product and "DDR" as single product, but each of these standards encompasses multiple sub-standards and multiple products. (*See* RRFF 2501, 2506). This leads to the fallacious implication that "SDRAM" and "DDR" products never change. This is critical, because the evidence shows that chipsets and motherboards for AMD's systems *were* redesigned after 2000 (the proposed finding cites only the testimony of an AMD witness). AMD started to ship is K7 processors with a newly designed 266 MHz front side bus and a newly designed AMD 760

chipset in October 2000. (Polzin, Tr. 3998-4005). This chipset was compatible with DDR200 and DDR266 devices. (*Id.*) In October 2002, AMD launched a new version of its K7 processor with a 333MHz front side bus. (*Id.*) This required third party chipset vendors to design and produce a new chipset that would support DDR333 and third party motherboard manufacturers to design compatible boards. (Polzin, Tr. 3998-4005, 4049-50). Seven months later, AMD launched a new version of its K7 processor with a 400 MHz front side bus, and third party vendors designed, produced, and launched compatible chipsets and motherboards that would support DDR400. (*Id.*) Alternatives to Rambus's technologies could have been incorporated into these new designs with no disruption.

2543. Changing the SDRAM standard now to avoid the Rambus patents would lead to DRAM chips that are incompatible with some systems using the existing DRAM infrastructure. (Jacob, Tr. 5567-74 ("If one were to build a DRAM using one of the alternatives highlighted in red, you would produce a DRAM that's incompatible with present JEDEC-compliant systems. If one were to use one of the other alternatives that are not highlighted in red, you would produce a part that may or may not be compatible with existing JEDEC-compliant systems, and it would depend upon the system in question."); *see also* DX0106-0107).

Rambus's Response to Finding No. 2543:

The proposed finding is misleading and incomplete. It treats "SDRAM" as a single product, but this standard encompasses multiple sub-standards and multiple products. (*See* RRFF 2501). This leads to the fallacious implication that "SDRAM" products never change. The evidence shows that DRAM manufacturers are constantly introducing new "SDRAM" products and retiring older products. For instance, the evidence shows that in the second half of 2002 alone, Infineon was introducing 15 new SDRAM products (i.e., new PC100 and PC133 devices in different densities and configurations). (CX 2466 at 5-9). In addition, in 2002, Infineon was phasing out as "End of Life" 12 different SDRAM products (different

configurations of PC100, PC133 and PC166). (CX 2466 at 6). Alternatives to Rambus's technologies could have been incorporated into new products as the older products are phased out. (Geilhufe, Tr. 9675). According to Steve Polzin at AMD, during a transition from one DRAM standard to another, alternatives could be incorporated "costlessly." (Polzin, Tr. 4042).

2544. Changing the DDR SDRAM standard to avoid Rambus's patents on dual-edged clocking now would lead to DRAM chips that are incompatible with all systems using the existing DRAM infrastructure. (Jacob, Tr. 5574-75 ("[I]n this instance all of the alternatives would produce parts that would be incompatible with JEDEC-compliant systems of today."); *see,* DX0108). The least disruptive of the alternatives, doubling the clock frequency, would require changes to the system clock and the memory controller. (Jacob, Tr. 5575-76).

Rambus's Response to Finding No. 2544:

The proposed finding is also misleading because it improperly treats DDR as a single product when the evidence shows that "DDR" consists of several sub-standards and multiple products. (*See* RRFF 2506). This leads to the fallacious implication that "DDR" products never change. The evidence shows that DRAM manufacturers are constantly introducing new "DDR" products and retiring older products. In the last two quarters of 2002 *alone*, Infineon was introducing 17 new DDR products (i.e., new DDR200, DDR266, DDR333, and DDR400 devices in different densities and configurations). (CX 2466 at 5-9). In addition, in 2002, Infineon was phasing out as "End of Life" 2 of its DDR products (different configurations of DDR200). (CX 2466 at 5). Moreover, complementary products for DDR DRAM devices have changed numerous times. In fact, new DDR 400 chip sets and motherboards for AMD's K7 processor were introduced after the beginning of the trial in this matter. (Polzin, Tr. 4004-05). Alternatives to Rambus's dual-edge clocking technology could have been incorporated into new products as the older products are phased out. (Geilhufe, Tr. 9675). According to Steve Polzin

at AMD, during a transition from one DRAM standard to another, alternatives could be incorporated "costlessly." (Polzin, Tr. 4042).

2545. Changing the DDR SDRAM standard now to avoid the Rambus patents on on-chip PLL/DLL would lead to DRAM chips that are incompatible with some systems using the existing DRAM infrastructure. (Jacob, Tr. 5576-79 ("So those highlighted in red, alternatives 1, 2, 3 and 4, would produce parts that are incompatible with existing systems, and alternative 5 would produce a part that may or may not be incompatible with existing JEDEC-compliant systems, and it would depend on the system in question."); *see also* DX0109)

Rambus's Response to Finding No. 2545:

The proposed finding is also misleading because it improperly treats DDR as a single product when the evidence shows that "DDR" consists of several sub-standards and multiple products. (*See* RRFF 2506). This leads to the fallacious implication that"DDR" products never change. The evidence shows that DRAM manufacturers are constantly introducing new "DDR" products and retiring older products. In the last two quarters of 2002 *alone*, Infineon was introducing 17 new DDR products (i.e., new DDR200, DDR266, DDR333, and DDR400 devices in different densities and configurations). (CX 2466 at 5-9). In addition, in 2002, Infineon was phasing out as "End of Life" 2 of its DDR products (different configurations of DDR200). (CX 2466 at 5). Moreover, complementary products for DDR DRAM devices have changed numerous times. In fact, new DDR 400 chip sets and motherboards for AMD's K7 processor were introduced after the beginning of the trial in this matter. (Polzin, Tr. 4004-05). Alternatives to Rambus's on-chip PLL/DLL technology could have been incorporated into new products as the older products are phased out. (Geilhufe, Tr. 9675). According to Steve Polzin at AMD, during a transition from one DRAM standard to another, alternatives could be incorporated "costlessly." (Polzin, Tr. 4042). Further, the evidence shows that on-chip

PLL/DLL is not necessary to produce DRAM that will be compatible with "DDR" complementary products. (*See* RRFF 655).

2546. Changing the DDR SDRAM standard now to avoid all of Rambus's patents on the standard would lead to a DRAM that would not be compatible with any JEDEC-compliant systems. (Jacob, Tr. 5579-80 ("If one were to replace all of the technologies in dispute with one of the alternatives, you would produce a DRAM part that would fail to be compatible with any existing JEDEC-compliant system."); Heye 3742-43).

Rambus's Response to Finding No. 2546:

The proposed finding is also misleading because it improperly treats DDR as a single product when the evidence shows that "DDR" consists of several sub-standards and multiple products. (*See* RRFF 2506). This leads to the fallacious implication that "DDR" products never change. In the last two quarters of 2002 *alone*, Infineon was introducing 17 new DDR products (i.e., new DDR200, DDR266, DDR333, and DDR400 devices in different densities and configurations). (CX 2466 at 5-9). In addition, in 2002, Infineon was phasing out as "End of Life" 2 of its DDR products (different configurations of DDR200). (CX 2466 at 5). Moreover, complementary products for DDR DRAM devices have changed numerous times. In fact, new DDR 400 chip sets and motherboards for AMD's K7 processor were introduced after the beginning of the trial in this matter. (Polzin, Tr. 4004-05). Alternatives to Rambus's technologies could have been incorporated into new products as the older products are phased out. (Geilhufe, Tr. 9675). According to Steve Polzin at AMD, during a transition from one DRAM standard to another, alternatives could be incorporated "costlessly." (Polzin, Tr. 4042).

3. Because SDRAM and DDR SDRAM Are Commodity Products and Customers Require Multiple Sources, No Individual Manufacturer Can Switch from the Rambus Claimed Technologies.

2547. Individual DRAM manufacturers could not remove the Rambus-claimed

technologies from the standards without agreement from their customers. (Appleton, Tr. 6400 ("[t]he product that actually gets consumed in the marketplace is not determined by Micron, its determined by the customer base. The customer has developed product platforms based on these standards,... and until the customer decides that they're no longer going to buy this product, then Micron really cannot make a change in its product portfolio, and we have to continue just to provide the product that we have been providing for some time."); Peisl, Tr. 4451-52 ("The impact on the customers on changing of standards are huge.... So the customers' main concern was of course that standards are not being changed and they're not deducted any features going out of the standard"); CX2108 (Oh, Dep.) at 232. ("Of course, customers will not change it. I mean, they – it's – it cost a lot to change the design. You have to – changing means that changing all the usage of customer, I mean, the computers. You have to change the – their customer's mind. It means – it's impossible, almost impossible."); Peisl, Tr. 4449 ("It would be very painful – Infineon couldn't do anything in changing parameters or changing anything on the standards side because we ... are only a part of the industry...")).

Rambus's Response to Finding No. 2547:

The proposed finding is misleading and incomplete. The evidence shows that DRAM customers switch to new DRAM standards on a regular basis – about once every year or so. For example, Compaq went through six different types of DRAM in seven years. It started using EDO DRAM in its products in 1995. (Gross, Tr. 2348-56). In 1997, Compaq shifted to using PC66 SDRAM. (Gross, Tr. 2348-50). In 1998, Compaq shifted to using PC100 SDRAM. (Gross, Tr. 2351). In 1999, Compaq shifted to using PC133 SDRAM. (Gross, Tr. 2353). In 2001, Compaq/HP shifted to using DDR 266. (Gross, Tr. 2354). And in 2002, Compaq/HP shifted to using DDR 333. (Gross, Tr. 2356).

AMD went through similar transitions with systems using its K7 processor. In June 1999, AMD launched the first K7 processor, which used the AMD750 chipset compatible with PC100 SDRAM. (Polzin, Tr. 3998-4005). Soon thereafter, third party vendors such as VIA designed and launched chipsets for the K7 processor that were compatible with PC133 SDRAM. (Polzin, Tr. 3998-4005; Heye, Tr. 3769-70). In September 2000, AMD launched a new version

of the K7 processor, which used the AMD760 chipset and was compatible with DDR200 and DDR266. (Polzin, Tr. 3998-4005). In October 2002, AMD launched a new version of the K7 and third party chipsets were made for this version that compatible with DDR333. (Polzin, Tr. 3998-4005). Less than one year later, in May 2003, AMD launched the K7 processor for which newly designed third party chipsets use DDR400. (Polzin, Tr. 3998-4005).

Each of these transitions required the design and production of new complementary components such as chip sets and motherboard. (Polzin, Tr. 3998-4005, 4049-50). Thus, while DRAM manufacturers must coordinate with their customers during changes to a new type of DRAM, this is done in the regular course of business every year or so. Acceptable alternatives to Rambus's technologies (if they existed) could have been incorporated during these regular transitions. (Geilhufe, Tr. 9675). According to Steve Polzin at AMD, during a transition from one DRAM standard to another, alternatives could be incorporated "costlessly." (Polzin, Tr. 4042).

2548. An individual DRAM manufacturer cannot deviate from the JEDEC standards in order to work around Rambus's patents in part because DRAM customers require multiple sources of commodity DRAM. (CX1075 ("… everyone wants multiple-sourced DRAMs, so to make DELL happy, you need multiple suppliers of DRAMs, modules, connectors, and clock chips"); CX1354 at 5 ("DRAM Industry: commodity business, Customers want multiple sourced, compatible DRAMs."); Williams, Tr. 763 ("for Micron, they make memory products that are used in the industry. Their customers are mainly computer customers who require that they are able to buy products from multiple sources ..."); Gross, Tr. 2307-08).

Rambus's Response to Finding No. 2548:

The proposed finding is misleading. Though DRAM customers want multiple sources of DRAM, this does not prevent manufacturer from switching to alternatives to Rambus's technologies and producing DRAM that is not compliant with JEDEC standards. The evidence

shows that DRAM manufacturers can and do this sort of production. For instance, DRAM manufacturers produce various graphics DRAMs that are non-JEDEC standard compliant. (Wagner, Tr. 3865 ("Q. And often times what they provide you is something that is not JEDEC – is not within the JEDEC specifications? A. Correct."); Wagner, Tr. 3835-36 ("Q. Do you have an understanding of whether the DRAM used with nVidia's graphics processors are always JEDEC compliant? A. The graphics processors are not necessarily compliant in a true JEDEC sense. . . .")). Yet customers of graphics DRAM are able to obtain multiple sources for their non-standard DRAM. (Wagner, Tr. 3849; CX 2828 at 7). Similarly, Micron and Infineon were able to develop and produce RLDRAM without any JEDEC specification. (Bechtelsheim, Tr. 5965-66).

Further, the evidence shows that the DRAM industry can and does manage changes to DRAM standards on a regular basis. (*See* RRFF 2547).

2549. An individual DRAM manufacturer could not change its SDRAM and DDR SDRAM designs if that would cause the critical parameters of its designs to differ in any way from those of other DRAM manufacturers. (*See* Lee, Tr. 6859 ("[I]n our business, we have to have perfectly substitutable products from other suppliers, so there needs to be multiple sources of the same part."); Peisl, Tr. 4448-49 ("Infineon couldn't do anything on their own in changing parameters or changing anything on the standards side because we were – we wouldn't – we are only a part of the industry . . ."); Polzin, Tr. 3943-44, 3952-53; Appleton, Tr. 6280; Bechtelsheim, Tr. 5788; *see also* CCFF 25-28).

Rambus's Response to Finding No. 2549:

The proposed finding is misleading. It treats "SDRAM" as a single product and "DDR" as single product, but each of these standards encompasses multiple sub-standards and multiple products. (*See* RRFF 2501, 2506). This leads to the fallacious implication that "SDRAM" and "DDR" products never change. The evidence shows that the industry has switched from one type

of SDRAM to another and then from one type of DDR to another. (*See* RRFF 2547).

4. DRAM must Be Compatible with Other Components and Switching to Alternatives to the Rambus Claimed Technologies Would Require Changes in Other Components to Ensure Compatibility.

2550. Even if a group of manufacturers were able to design and build a new DRAM that avoided Rambus's patents**,** they would not be able to sell those DRAMs unless they were supported by other components. (CX1075 ("A phone or computer that is almost compatible is one that doesn't work. If people build parts 99% compatible, the systems companies won't buy them"); Polzin, Tr. 3954 ("It gets back to just because you have a DRAM doesn't mean you are able to build a computer. You need a lot of support components around it to make a fully functional computer and its critical that in the commodity market you have multiple suppliers of all these components that all agree on the same specification and build compatible parts.")).

Rambus's Response to Finding No. 2550:

The proposed finding is incomplete. The evidence shows that manufacturers of complementary components for DRAM (i.e., chip sets, motherboards, etc.) routinely and rapidly design and produce products compatible with new DRAM designs. For instance, when AMD redesigned its chipsets for its K7 microprocessor to work with DDR200 and DDR266 devices, it took only 15 to 18 months. (Heye, Tr. 3767-69). It took motherboard manufacturers only six months to produce new motherboards compatible with these chipsets. (Polzin, Tr. 4017-18). Similarly, from June 1999 to May 2003 (less than four years), AMD K7 systems have gone from using PC100 to PC133 to DDR200 and DDR266 to DDR333 to DDR400, and for each of these transitions new chipsets and motherboards were designed and produced. (RPF 1310-20; Polzin, Tr. 4049-50). According to Steve Polzin at AMD, during a transition from one DRAM standard to another, alternatives (if they exist) could be incorporated "costlessly." (Polzin, Tr. 4042).

2551. Efforts to transition to a new DRAM standard often encounter a "chicken and egg" problem. (Macri, Tr. 4625-29). Industry acceptance of a new DRAM standard requires the existence of additional compatible components, including particularly memory controllers. Those same considerations dictate that sales of a memory controller depend on the existence of

compatible DRAMs. In both cases, unless one is available, the firms making the other will be hesitant to produce their component. (CX2315 at 1 ("It is a chicken and an egg problem..... The vendors won't line up to produce the device unless there are users.... but the users won't consider the part unless the suppliers/infrastructure is in place."); Polzin, Tr. 4012; Macri, Tr. 4619-20).

Rambus's Response to Finding No. 2551:

The proposed finding is incomplete. Whatever "chicken and egg" problem exists, the DRAM industry routinely overcomes any difficulties in adopting new DRAM standards. Since 1995, industry members have coordinated transitions from EDO to PC66, from PC66 to PC100, from PC100 to PC133, from PC133 to DDR200, from DDR200 to DDR266, from DDR266 to DDR333, and from DDR333 to DDR400. (*See* RPF 1308-32). Each of these transitions has required the development of new DRAM and new complementary products. (Polzin, Tr. 4049-50). According to Steve Polzin at AMD, during a transition from one DRAM standard to another, alternatives (if they exist) could be incorporated "costlessly." (Polzin, Tr. 4042).

2552. Changing either the SDRAM standard or the DDR SDRAM standard in 2000 to avoid Rambus's patents would have required manufacturers of components such as controllers, motherboards and modules to redesign, test and reissue their products. (Peisl, Tr. 4457 ("It would not have affected only us as a DRAM supplier; it would have affected all the other suppliers as well. Motherboards would have to be redesigned, controllers would have to be reissued and BIOS would have to be rewritten. It's all a very costly issue.")).

Rambus's Response to Finding No. 2552:

The proposed finding is misleading and incomplete. Since 1995, industry members have coordinated transitions from EDO to PC66, from PC66 to PC100, from PC100 to PC133, from PC133 to DDR200, from DDR200 to DDR266, from DDR266 to DDR333, and from DDR333 to DDR400. (*See* RPF 1308-32). Each of these transitions has required the development of new DRAM and new complementary products. (Polzin, Tr. 4049-50). In fact, new DDR 400 chip sets and motherboards for AMD's K7 processor were introduced after the beginning of the trial

in this matter. (Polzin, Tr. 4004-05). According to Steve Polzin at AMD, during a transition from one DRAM standard to another, alternatives (if they exist) could be incorporated "costlessly." (Polzin, Tr. 4042).

2553. By 2000, the entire industry had implemented the JEDEC standards to such a degree that it would have been extremely difficult and costly for all industry members to change their respective designs to avoid Rambus's patents. (Peisl, Tr. 4444 ("In 2000, the advancements of the SDR and DDR specifications had already reached a degree that the complete industry, the DRAM industry, motherboard industry, the components industry, the module industry, and the controller industry, has reached – had reached a level of implementation of the JEDEC-related standards that it would have been very hard and very costly and I would say near impossible to go back and to implement any substantial changes back in the 2000 time frame."); *see also* CX1340 at 25 ("Setting a new standard is hard ... Compelling benefits over existing standard ... Critical mass of suppliers and users")).

Rambus's Response to Finding No. 2553:

The proposed finding is not supported by the evidence. The evidence shows that DRAM manufacturers routinely redesign DRAM products and that alternatives to Rambus's technologies could be implemented at these times. (Geilhufe, Tr. 9675). In the last two quarters of 2002 *alone*, Infineon was introducing *forty seven* new DRAM products: 17 new DDR products (i.e., new DDR200, DDR266, DDR333, and DDR400 devices in different densities and configurations), 15 new SDRAM products (i.e., new PC100 and PC133 devices in different densities and configurations), 4 new Graphics RAM products, 5 new Mobile-RAM products, and 6 new RLDRAM products. (CX 2466 at 5-9). In addition, in 2002, Infineon was phasing out as "End of Life" *fourteen* different DRAM products: 2 DDR products (different configurations of DDR200) and 12 SDRAM products (different configurations of PC100, PC133 and PC166). (CX 2466 at 5-6).

Similarly, between 1995 and 1997, Micron taped out { }

(Shirley, Tr. 4217-18 (*in camera*)). In 1998, { }
(Shirley, Tr. 4218-19, 4226 (*in camera*)). In 1999, {
} (Shirley, Tr. 4220-23, 4225-26 (*in camera*)). In 2000, {
} (Shirley, Tr. 4223-25 (*in camera*)). In 2001, {
} (Shirley, Tr. 4227 (*in camera*)). In 2002, {
} (Shirley, Tr. 4228-29 (*in camera*)).

The evidence further shows that the cost for a DRAM manufacturer to switch to alternatives to Rambus's technologies would be fairly minimal compared to the overall costs of production and compared to paying Rambus's royalties. (Rapp, Tr. 9878-87; RPF 1340-45). Switching costs do not prevent DRAM manufacturers from moving to alternatives. (*Id.*)

Nor do any coordination difficulties or costs associated with producing new complementary products prevent switching. The evidence shows that the DRAM industry routinely coordinates transitions to new types of DRAM. Since 1995, industry members have coordinated transitions from EDO to PC66, from PC66 to PC100, from PC100 to PC133, from PC133 to DDR200, from DDR200 to DDR266, from DDR266 to DDR333, and from DDR333 to DDR400. (*See* RPF 1308-32). Each of these transitions has required the development of new DRAM and new complementary products. (Polzin, Tr. 4049-50). According to Steve Polzin at AMD, during a transition from one DRAM standard to another, alternatives could be incorporated "costlessly." (Polzin, Tr. 4042). There is no reason to believe that coordination difficulties or transition costs would be any greater than those associated with these routine transitions. (Rapp, Tr. 9890-91).

While Complaint Counsel's economic expert admitted that he did not quantify any

switching costs, (McAfee, Tr. 11356), he confessed that the DRAM industry overcomes switching costs at a frequency of more than once a year:

Q. You would agree, wouldn't you, that there are switching costs incurred when you go from SDRAM to DDR?

A. I agree with that.

Q. And there are also switching costs incurred when you go from DDR to DDR-II?

A. I agree with that.

Q. And there would have been switching costs incurred if you went from SDRAM or from DDR to SLDRAM; correct?

A. There would have been.

Q. There also are switching charges incurred when you go from a PC66 to a PC100 or a PC133, aren't there?

A. There are some switching -- you said charges, but there are some switching costs, would be the ordinary term.

Q. And there are switching costs incurred when you go from a 64-meg to a 128-meg to a 256-meg of any particular DRAM design?

A. There are certainly switching costs incurred in those transitions.

Q. The switching costs we've talked about between SDRAM to DDR, for example, and within various SDRAM and DDR product generations are incurred with a frequency of more often than once a year, aren't they?

A. There are some kinds of switching costs that are incurred with a

frequency more often than once a year.

(McAfee, Tr. 11357-58). Even further, Complaint Counsel's economic expert admitted on cross-examination that switching costs to avoid Rambus's technologies would not be greater than those actually experienced by the industry during switches that have actually occurred. (McAfee, Tr. 7714-18).

2554. Customers such as HP would only change the type of DRAM it purchased if the new type of DRAM reduced cost, avoided a perceived customer detriment, or provided an improved performance in some way. (Gross, Tr. 2302 ("I can't think of a significant transition we have made that did not also come with performance improvements.")).

Rambus's Response to Finding No. 2554:

The proposed finding is irrelevant. Complaint Counsel's own proposed findings purport to show that paying Rambus's royalties imposes substantial costs on DRAM manufacturers that could be avoided by designing around Rambus's patents. (*See* CCFF 3100). Accordingly, if acceptable, noninfringing alternatives actually existed, switching to those alternative technologies would *lower* DRAM manufacturers' costs, which is the purpose of much of the redesign work performed by these manufacturers every day. Acceptable alternatives (if they existed) could be incorporated during any of the routine transitions that the DRAM industry goes through on a nearly yearly basis. (*See* RRFF 2553).

2555. A change to the type of DRAM that HP purchases would typically occur only in response to the emergence of new processors or chipsets that can provide additional features to HP's customers. (Gross, Tr. 2286-87 ("Generally our product development teams in developing the next new product would consider microprocessors and chipsets and the features that they would enable for a customer, and that processor and chipset combination that is decided upon dictates the type of memory that needs to be used in combination.").

Rambus's Response to Finding No. 2555:

The proposed finding is incomplete. Acceptable alternatives (if they existed) could be

incorporated during any of the routine transitions that the DRAM industry goes through on a nearly yearly basis. (*See* RRFF 2553).

2556. In the longer term, firms such as Intel and AMD dedicate substantial resources to ensuring that DRAM and the other components develop such that compatible components are available when the PC-OEMs are assembling their computers. It can take a number of years and substantial expense to support the development of these components. (MacWilliams, Tr. 4818-19 ("It typically takes two to four years to do something new in the DRAM industry and something similar to do something new in the chipset, depending on the amount of the change. . . . Basically, it is the latency for designs.")

Rambus's Response to Finding No. 2556:

The proposed finding is not supported by the evidence. The sole evidence cited in support of the proposed finding is the testimony of Peter MacWilliams, who was responding to questions about Intel's plans regarding a switch from SDRAM to an entirely new DRAM architecture – RDRAM. (MacWilliams, Tr. 4818-19). His answer regarding how long it takes to "do something new" was therefore in this context. In contrast, the evidence shows that the DRAM industry transitions to new types of DRAM that require less comprehensive changes on the order of nearly once per year. (*See* RRFF 2553).

2557. One of the results of that transition period was that Intel, when it selected RDRAM, believed it needed to choose a technology that could be a standard in the industry for approximately five years. (RX0904 at 7; MacWilliams, Tr. 4802 (" . . . [I]t was important that we pick a technology that would allow some stability and longevity because we were going to ask the industry to go through a major transition in terms of the infrastructure. The connectors, the boards, the modules would all need to change, and that's not something you can change on a yearly or every-other-year basis....Just the amount of investment to make the changes, to validate the changes are correct, to optimize the results based on the feedback you get from the first designs, will take longer than one year...")).

Rambus's Response to Finding No. 2557:

The proposed finding is misleading and irrelevant. First, there is no evidence that a transition to alternatives for the two Rambus technologies incorporated in the various SDRAM

products or the four technologies incorporated in the various DDR products would require anywhere near the magnitude of change required for the industry to switch to RDRAM. Second, even RDRAM was planned to be produced in various types – PC800, PC1066, PC1200, and PC1600 – in various configurations - e.g., x16 and x18 in 128/144Mb, 256/288Mb, 512/576Mb, 1/1.2Gb densities. (RX 1762 at 54). The evidence shows that new types of SDRAM and new types of DDR products are constantly being produced while older types are retired. (*See* RRFF 2553). Alternatives to Rambus's technologies could be introduced at these times. (*See* RRFF 2553).

2558. AMD also must ensure that it develops the infrastructure, or what it terms a "virtual system" of components, that would all function together with AMD's processors. (Heye, Tr. 3662-63 ("What we have to do is establish an industry-wide business model with many, many partners, and those partners, based on the business model would go off and design north bridges, BIOSes, motherboards, clock chips, VRMs, ... it's a virtual system.")). It took AMD about two years to develop the infrastructure to support the K-7 microprocessor. (Heye, Tr. 3673).

Rambus's Response to Finding No. 2558:

The proposed finding is misleading and incomplete. Prior to its K7 microprocessor, AMD produced microprocessors that were "pin compatible" with Intel processors and used the entire Intel-based infrastructure. (Heye, Tr. 3653). An infrastructure in a computer consists of a north bridge (also called a chipset), which connects the microprocessor via a bus to the memory, graphics, and the south bridge. (Heye, Tr. 3655-58). The south bridge communicates with peripheral devices, such as the keyboard and mouse, and the BIOS, which communicates with the microprocessor. (Heye, Tr. 3655-58). Richard Heye, Vice President and General Manager of the Microprocessor Business Unit at AMD (Heye, Tr. 3615), joined AMD in June 1997 to construct the infrastructure for the K7 processor, which did not exist. (Heye, Tr. 3652-54).

AMD was able to coordinate with vendors for each part of the infrastructure and to launch complete systems by 1999. (Heye, Tr. 3646-47).

Most importantly, *not all of the infrastructure would have to be changed to accommodate changes in DRAM standards such as alternatives to Rambus's technologies*. (Heye, Tr. 3742-43). Thus, once the base infrastructure was created, AMD systems quickly went through multiple transitions to new types of DRAM. Between June 1999 and May 2003, systems using AMD's K7 switched from using PC100 to PC133 to DDR200 and 266 to DDR333 to DDR400. (RPF 1311-20). Each of these transitions has required the development of new DRAM and new complementary products. (Polzin, Tr. 4049-50). According to Steve Polzin at AMD, during a transition from one DRAM standard to another, alternatives (if they exist) could be incorporated "costlessly." (Polzin, Tr. 4042).

2559. One of the things that AMD must do in order to establish its infrastructure is to determine what the commodity DRAM will be when their CPU is ready to launch. (Heye, Tr. 3666 ("You always want to make sure you're riding the commodity curve. You don't want to be different from what I call the Intel-based systems.")).

Rambus's Response to Finding No. 2559:

The proposed finding is misleading and incomplete. (*See* RRFF 2558).

2560. The costs of modifying complementary components after a DRAM standard has been adopted by the industry are substantial. For example, the costs to the manufacturers of chipsets if the DRAM standard is changed late in the process can be high, because chipset manufacturers must design a chipset to interface with a specific memory product up to two years prior to the shipment of the chipset. (Heye, Tr. 3678:13 ("from the time you start thinking about a chipset to implementing it, especially when it's brand new like the one for AMD, it's about two years prior to shipping.")).

Rambus's Response to Finding No. 2560:

The proposed finding is not supported by the evidence. (*See* RRFF 2558).

2561. AMD developed a faster front side bus and a new chipset so that its K7 (or Athlon) CPU would be compatible with a number of different speed SDRAMs and DDR SDRAMs. (Polzin, Tr. 3998- 4005, *see* DX0031). A number of AMD's infrastructure partners also had to make investments to accommodate those faster systems. (Polzin, Tr. 4049-50 ("Our chipset partners needed to design faster circuitry in their chipsets and our motherboard partners needed to adhere to stricter design rules in their manufacture of their motherboards.")).

Rambus's Response to Finding No. 2561:

Rambus has no specific response.

2562. AMD's chipset partners supported AMD's moves to faster front side busses in order to be able to get better prices for their products. (Polzin, Tr. 4050 ("Why they manufacture our chipsets for the faster front-side buses? That's the question? They want to keep up with the latest technology. They can get higher prices for more advanced chipsets. A chipset that supports DDR 333, for example is worth more than a chipset that supports DDR200.")).

Rambus's Response to Finding No. 2562:

Rambus has no specific response.

C. The Entire Industry, Including Manufacturers of Complementary Products, Can Only Switch from the Current JEDEC Standard by Changing the JEDEC Standard.

1. It Is Unlikely That a Standard Can Be Created Outside of JEDEC, Which Is the Body That Has Traditionally Determined Standards in the DRAM Industry.

2563. Each new generation of commodity DRAM, from page mode through fast page mode, EDO, SDRAM and DDR SDRAM, has been a JEDEC standard. (Prince, Tr. 9020-21). The DRAM industry's penchant for standardization was well known to Rambus executives from the company's earliest days. (CX0533 at 9 ("The DRAM industry's penchant for standardization combined with the RamBus marketing strategy of licensing all the major vendors make it extremely unlikely that any potential competitor would be able to gain critical mass enough to challenge an already established and ubiquitous RamBus chip.")).

Rambus's Response to Finding No. 2563:

The proposed finding is misleading and not supported by the evidence. Intel developed the PC100 SDRAM specification in 1996. (MacWilliams, Tr. 4907-09). As stated in that

specification, the "objective of this document is to define a new Synchronous DRAM specification ('PC SDRAM') which will remove extra functionality from the current JEDEC standard SDRAM specification, so that it will be a 'fully compatible' device among all vendor designed parts." (RX 2103-14 at 9). The Intel PC SDRAM specification also set forth the standards for PC66. (MacWilliams, Tr. 4908; RX 2103-14 at 60-61). Later, a small group of DRAM manufacturers and OEMs developed the PC133 standard. (MacWilliams, Tr. 4912-13). Similarly, with DDR, Intel has produced "addendums" for the various sub-standards such as DDR200 that set forth the parameters for such features as "Pin assigments, initialization sequence, Electrical Characteristics and DC operating conditions, AC operating conditions, IDD Spec and conditions, AC timings for DDR 200, etc." (RX 1762 at 17). As Peter MacWilliams of Intel testified, the "spec addendum" was Intel's tool for ensuring that products were made to the standard specifications that Intel wanted:

> Q. What is a spec addendum?
>
> A. It's a process we evolved to after PC100 spec. Since JEDEC started writing the specs for these new technologies and we didn't think the specs captured all the issues that we were concerned about for our system designs, we started creating spec addendums.
>
> Spec addendums document areas of the spec that we would hope would be a JEDEC spec eventually but are conditionally. We used the spec addendum as a tool to work with the DRAM industry to get agreement on how to build the devices to those specs. Once we have agreement, you know, we take those items to JEDEC and see if they want to incorporate them in the spec.

But in parallel with them developing the spec, it's our tool for working with the industry to make sure we have a robust device.

(MacWilliams, Tr. 4916-17).

2. Changing the Prevailing DRAM Standard So That Individual Firms Could Switch from the Rambus Claimed Technologies Would Take Years.

2564. It typically takes two to four years to do something new in the DRAM industry. (MacWilliams, Tr. 4818 ("It typically takes two to four years to do something new in the DRAM industry and something similar to do something new in the chipset, depending on the amount of the change."); CX0711 at 184 (changes to a new technology standard, when they occur, require "fundamentally long lead time efforts," because of "the sort of things that must be done . . . to make . . . technology usable from a deployment perspective (silicon infrastructure, models, modules, etc.")).

Rambus's Response to Finding No. 2564:

The proposed finding is not supported by the evidence. The testimony of Peter MacWilliams cited in support of the finding does not support it; he was responding to questions about Intel's plans regarding a switch from SDRAM to an entirely new DRAM architecture – RDRAM. (MacWilliams, Tr. 4818-19). His answer regarding how long it takes to "do something new" was therefore in this context. The cited email is discussing the device being developed by the SyncLink consortium; again, this reference is to a device that was a fundamental architecture change from existing standards. There is no evidence supporting the notion that changing SDRAM products to avoid two Rambus technologies or changing DDR products to avoid four Rambus technologies would involve anywhere near the time involved for a completely new standard. To the contrary, the evidence shows that the DRAM industry transitions to new types of DRAM that require less comprehensive changes on the order of nearly

once per year. (*See* RRFF 2553). According to Steve Polzin at AMD, if alternatives existed, the Rambus technologies were "pretty simple things to work around," and they could be incorporated "costlessly" during a transition to another iteration of DRAM. (Polzin, Tr. 3989, 4042).

2565. The standard setting process alone can take two to three years. (CX0302 at 22 ("DRAM subsystem standardization. Complete process may take 2-3 years")). Generally, it is the engineering time to solve the problems that takes up most of that time. (Rhoden, Tr. 414 ("[W]hat we've done is we've removed the process itself from the bottleneck, and now the bottleneck is actually the engineering itself.")).

Rambus's Response to Finding No. 2565:

The proposed finding is misleading and incomplete. The cited evidence refers to the time taken in the past to develop entirely new standards through JEDEC. There is no evidence that relates this time frame to avoiding the two Rambus technologies in SDRAM or the four Rambus technologies in DDR. The evidence does show that the DRAM industry transitions to new types of DRAM that require less comprehensive changes on the order of nearly once per year. (*See* RRFF 2553). In contrast to developing an entire standard, the Rambus technologies were "pretty simple things to work around," and acceptable alternatives (if they existed) could be incorporated "costlessly" during a transition to another iteration of DRAM. (Polzin, Tr. 3989, 4042). Further, many changes to DRAM standards occur outside of JEDEC, which is a slow process. For instance, Intel developed the PC100 SDRAM specification in 1996 outside of JEDEC. (MacWilliams, Tr. 4906-09). Later, a small group of DRAM manufacturers and OEMs developed the PC133 standard outside of JEDEC. (MacWilliams, Tr. 4912-13).

2566. JEDEC began considering the SDRAM standard in 1991. The 42.3 committee completed work and it became a standard in 1993. The SDRAM standard only began to become widely adopted in the industry in 1996-97. (CCFF 577; *see,* DX0141).

Rambus's Response to Finding No. 2566:

The proposed finding is misleading and irrelevant. The cited evidence refers to the time taken to develop an entirely new standard (SDRAM) through JEDEC. There is no evidence that relates this time frame to avoiding the two Rambus technologies in SDRAM or the four Rambus technologies in DDR. To the contrary, the evidence shows that it would take substantially less time – likely less than one year. (*See* RRFF 2555).

2567. JEDEC began considering the technologies that became part of the DDR SDRAM standard at the same time it was developing the SDRAM standard as part of its consideration of what technologies should be in that standard. (CCFF 578-584). The 42.3 committee completed work and DDR SDRAM became a standard in 1999. (CCFF 649-652). Although DDR SDRAM was already being used in 1999 by graphics card manufacturers, the DDR SDRAM standard only began to become widely adopted in the industry in 2001-2002. (CCFF 2520; McAfee, Tr. 11344; *see,* DX0141).

Rambus's Response to Finding No. 2567:

The proposed finding is misleading and irrelevant. The cited evidence refers to the time taken to develop an entirely new standard (DDR) through JEDEC. There is no evidence that relates this time frame to avoiding the two Rambus technologies in SDRAM or the four Rambus technologies in DDR. To the contrary, the evidence shows that it would take substantially less time – likely less than one year. (*See* RRFF 2555).

2568. JEDEC began considering the DDR-2 SDRAM standard in April of 1998 when the first meeting of the "Future DRAM Task Group" met. (CX0376A; CX0379A; Macri, Tr. 4582-83; Lee, Tr. 6769). The DDR-2 standard has only recently been completed and has been adopted by firms in the graphics card industry. Graphics chip designers were among the earliest adopters of DDR-2. NVidia was working on designs for a graphics chip intended for use with DRAMs based on the DDR-2 standard in late 2000 to early 2001. (Wagner, Tr. 3838-839). ATI uses both GDDR-2 and GDDR-2m in current products. (Macri, Tr. 4579). GDDR-2m, like GDDR-2 is a variant of the DDR-2 standard. (Macri, Tr. 4577-78).

Rambus's Response to Finding No. 2568:

The proposed finding is misleading and irrelevant. The cited evidence refers to the time taken to develop an entirely new standard (SDRAM) through JEDEC. There is no evidence that relates this time frame to avoiding the two Rambus technologies in SDRAM or the four Rambus technologies in DDR. To the contrary, the evidence shows that it would take substantially less time – likely less than one year. (*See* RRFF 2555).

2569. When transitioning to a new DRAM standard, the industry prefers evolutionary rather than revolutionary change, changing as little as possible between standards to obtain the needed performance increase for the new standard. (*See* CCFF 127-128).

Rambus's Response to Finding No. 2569:

The proposed finding is irrelevant. There is no evidence suggesting that avoiding the two Rambus technologies in SDRAM or the four Rambus technologies in DDR would be "revolutionary."

2570. Because evolutionary change reduces risk during the introduction of the new standard it also eases the introduction of the new DRAM standard. (MacWilliams, Tr. 4823 ("The problem with revolutionary technologies is they're risky. They take a lot of work to get right and time. You have to go through multiple iterations typically."); CCFF 127-128, 3246-250).

Rambus's Response to Finding No. 2570:

The proposed finding is irrelevant. There is no evidence suggesting that avoiding the two Rambus technologies in SDRAM or the four Rambus technologies in DDR would be "revolutionary."

2571. The SDRAM standard was an evolutionary change from the previous standard, EDO. (MacWilliams, Tr. 4822 ("So SDRAM was perceived to be somewhat evolutionary in that it preserved the same pins as the old EDO memory but added the clock."); Sussman, Tr. 1377).

Rambus's Response to Finding No. 2571:

The proposed finding is irrelevant. There is no evidence suggesting that avoiding the two Rambus technologies in SDRAM or the four Rambus technologies in DDR would be "revolutionary."

2572. The DDR SDRAM standard was an evolutionary change from SDRAM, . (Rhoden, Tr. 408; Sussman, Tr. 1428; Peisl, Tr. 4378-79, 4429; MacWilliams, Tr. 4822 ("DDR is perceived to be evolutionary in that it added some strobes for the data bus but preserved most of the paradigms of SDRAM"), 4882; Gross, Tr. 2291).

Rambus's Response to Finding No. 2572:

The proposed finding is irrelevant. There is no evidence suggesting that avoiding the two Rambus technologies in SDRAM or the four Rambus technologies in DDR would be "revolutionary."

2573. The DDR-2 SDRAM standard was an evolutionary change from DDR SDRAM. (Macri, 4611 ("Well, we wanted to -- we didn't want to start with a clean sheet of paper. We wanted to evolve a current DRAM so we could take that user base and move them as seamlessly as possible into the future. So, we needed to pick the DRAM we would start with and then evolve it."); Rhoden, Tr. 408; Kellogg, Tr. 5190 ("DDR-II is what became the name of the evolutionary memory device that followed DDR, or DDR-I as it became known.")).

Rambus's Response to Finding No. 2573:

The proposed finding is irrelevant. There is no evidence suggesting that avoiding the two Rambus technologies in SDRAM or the four Rambus technologies in DDR would be "revolutionary."

3. Even if JEDEC Were Able to Change the Standard, There Is No Guarantee That the New Standard Would Be Able to Displace the Current Standard.

2574. DRAM manufacturers fabrication plants cost over a billion dollars. (CCFF 31). In addition, the inventory of a DRAM manufacturer can be worth hundreds of millions of dollars. (CCFF 2534-535). As a consequence, DRAM manufacturers that lose to Rambus would have

the incentive to agree to license the technologies from Rambus in order to be able to continue to manufacture DRAM. (McAfee, Tr. 7443-44 ("This goes back to the basic economics of the DRAM industry, which is you want – the plants are enormously expensive and you want to run them full out, that is, 24/7, as they say, ... you want to run them full out constantly, and so until you've actually ramped up production, you'll be producing the infringing product and paying royalty.")).

Rambus's Response to Finding No. 2574:

Rambus has no specific response.

2575. DRAM customers are only willing to switch from an existing standard or generation of commodity memory to a new standard when cost or performance justifications exist. (Gross, Tr. 2302-303 ("I can't think of a significant transition we have made that did not also come with performance improvements.")). Suppliers of components that constitute the DRAM infrastructure are willing to develop products compatible with a new standard only if they are able to obtain an economic benefit from that change. (*See* CCFF 2562).

Rambus's Response to Finding No. 2575:

The proposed finding is misleading. Complaint Counsel's own proposed findings purport to show that paying Rambus's royalties imposes substantial costs on DRAM manufacturers that could be avoided by designing around Rambus's patents. (*See* CCFF 3100). Accordingly, if acceptable, noninfringing alternatives actually existed, switching to those alternative technologies would *lower* DRAM manufacturers' costs, which is the purpose of much of the redesign work performed by these manufacturers every day. Acceptable alternatives (if they existed) could be incorporated during any of the routine transitions that the DRAM industry goes through on a nearly yearly basis. (*See* RRFF 2553). Further, suppliers of complementary products would of course have a motivation to produce compatible parts – sales.

4. Reaching Consensus Within JEDEC As To How To Change The Standards Would Be Extremely Difficult.

2576. Because of the amount of work involved and the number of different types of firms at JEDEC, it can take years to change a standard. (CX0302 at 22 ("Complete process may take 2-

3 years"); Polzin, Tr. 3977 ("JEDEC is open to any and all parties, so any and all parties have an opinion and can contribute or delay, or everybody has a vote, so it's not always the most straightforward thing to get a technical specification through. It's sometimes long, laborious, and you have to argue your points endlessly, probably much like Congress down the road, but it's successful and it works."); Peisl, Tr. 4453 ("JEDEC is traditionally a very slowly moving consortium, and there's a reason for that, because there's so many companies involved, it's basically the whole industry that produces parts for the PC and the laptop and the server business, so to try to reach consensus at JEDEC, based on my experience, have been incredibly hard and tough. In the last decade, essentially there were only two standards that emerged for SDR and DDR"); Soderman, Tr. 9511 ("It takes time to have a good engineering standard developed, yes.")).

Rambus's Response to Finding No. 2576:

The proposed finding is misleading and irrelevant. The cited evidence refers to the time taken to develop an entirely new standard through JEDEC. There is no evidence that relates this time frame to avoiding the two Rambus technologies in SDRAM products or the four Rambus technologies in DDR products. To the contrary, the evidence shows that it would take substantially less time – likely less than one year. (*See* RRFF 2555). Moreover, there is no evidence to support a finding that adoption of alternatives to Rambus's two technologies in SDRAM products or Rambus's four technologies in DDR products would have to be accomplished through JEDEC. Changes to DRAM standards routinely occur outside of JEDEC. Intel developed the PC100 SDRAM and the PC66 SDRAM specifications outside of JEDEC. (MacWilliams, Tr. 4907-09). Those standards do precisely what would have to be done to avoid Rambus's technologies; they "remove extra functionality from the current JEDEC standard specification." (RX 2103-14 at 9). Similarly, a small group of DRAM manufacturers and OEMs developed the PC133 standard outside of JEDEC. (MacWilliams, Tr. 4912-13). In fact, Intel routinely develops "addendums" for the various sub-standards that could incorporate alternatives. As Peter MacWilliams of Intel testified, the "spec addendum" was Intel's tool for ensuring that

products were made to the standard specifications that Intel wanted. (MacWilliams, Tr. 4916-17 ("We used the spec addendum as a tool to work with the DRAM industry to get agreement on how to build the devices to those specs. Once we have agreement, you know, we take those items to JEDEC and see if they want to incorporate them in the spec.").

2577. The amount of time it takes develop to a new standard to work around the Rambus patents is one of the reasons for the JEDEC patent disclosure rule. (CX0449 at 3 ("The reason for requiring early disclosure is to give the formulating committee as much time as possible to decide whether to include the patented technology in the standard, to work around the patented technology, or to evaluate other options. Developing a standard can take months or years."); Williams, Tr. 772-73 ("nine months from the time that you introduced an item to the earliest time that it typically could be sent to ballot and voted on.")).

Rambus's Response to Finding No. 2577:

The proposed finding is not supported. There is no evidence that the JEDEC patent disclosure rule (to the extent such a "rule" existed) was influenced at all by the " time it takes develop to a new standard to work around the Rambus patents."

2578. The amount of time it takes JEDEC to complete a standard is the main reason that JEDEC starts standards years before the standards are expected to be needed in the marketplace. (Sussman, Tr. 1402; Macri, Tr. 4607-608) (Regarding DDR-2, "[t]he design cycle was long, so we needed to do this very early so that systems could be started to be designed – DRAMs could be designed such that when the DDR1 standard,... ended its life, the DDR2 standard and its systems would be ready to take over in a seamless fashion...[W]e needed to be proactive purely because you can't build these things in a day. It takes quite a bit of time.")).

Rambus's Response to Finding No. 2578:

The proposed finding is misleading and irrelevant. (*See* RRFF 2576).

2579. Changing the JEDEC standard by removing the allegedly infringing technologies would have been particularly difficult. (Peisl, Tr. 4451 ("Any change, particularly any deduction of standard, if you -- it's very hard to change the rules in the middle of the game. When you have offered certain options, certain features set to the customers, we have no control which customer is using which feature.")).

Rambus's Response to Finding No. 2579:

The proposed standard is not supported by the evidence. (*See* RRFF 2553).

2580. One example how a change in the standard to remove the allegedly infringing technologies would harm the industry is the potential replacement of programmable burst length with fixed burst length. (Peisl, Tr. 4452 ("Removing of features, for instance, as the flexibility of choosing the burst length. As we know, that, for instance, AMD and Intel-based controllers are using different burst length, so removing one would disadvantage one of the companies, which would ... create a noncompetitive situation.")).

Rambus's Response to Finding No. 2580:

The proposed finding is misleading. The evidence shows that fixed burst length is not an acceptable alternative. (*See* RPF 904-21). It would of course harm the industry to replace Rambus's programmable burst length technology with an alternative that is inferior in cost-performance terms. The evidence shows that such an effort would have been rejected by the market. AMD and Intel account for 99% of the microprocessor market. (Heye, Tr. 3642-43). Although Intel uses a burst length of four in its memory systems, AMD elected to use a burst length of eight because doing so increases system performance with the AMD architecture. (Polzin, Tr. 3994). The use of programmable burst length in SDRAM and DDR therefore allowed systems designers to optimize their particular microprocessor architectures for increased system performance. When the preliminary specification for DDR2 specified a single burst length of four (the one used by Intel), none other than Intel insisted that the DDR2 specification be changed to include a programmable burst length so that a burst length of 8 could be used. (RX 1854 at 20 (preliminary specification); CX 174 at 7-8, 37 (Intel proposal to change the specification to allow for burst length of 8)). According to Intel's presentation, the use of programmable burst length would allow Intel (and therefore AMD) to optimize performance

depending on the application. (CX 174 at 37 ("Potential improvement of 4-10% on high-bandwidth applications")). The proposed finding therefore rests on the unsupported premise that the market would accept DRAM using a single burst length; the market would not do so.

2581. Had the industry adopted a fixed burst length of four for the original SDRAM standard, then AMD would have used that burst length. However, since the standard allowed the use of burst lengths of eight, the company optimized their processors to work with a burst length of eight and would now be harmed by a move to a burst length of four. (Polzin Tr. 3994 ("Fixed burst length would have been very, very bad for AMD. AMD designed its microprocessors to have its natural burst length to be 64 bytes, which is eight cycles of data. Knowing that the DRAMs had that capability, we decided to take advantage of that capability for performance reasons. If the work-around was to fix the burst length, the most likely burst length chosen would have been an Intel-compatible burst length or a burst length of four cycles or 32 bytes. That would have been very bad for us. A, it would have required lots of redesign in the memory controllers and also caused us a performance hit.")).

Rambus's Response to Finding No. 2581:

The proposed finding is incomplete and misleading. There is no evidence to support a finding that the market would accept DRAM with a single fixed burst length. (*See* RRFF 2582). Further, had JEDEC adopted a single fixed burst length, microprocessor systems would have suffered performance degradation. (Polzin, Tr. 3994; CX 174 at 37 (Intel presentation insisting on programmable burst length in DDR2 to allow for increased performance in high-bandwidth applications)).

2582. Another example how a change in the standard to remove the allegedly infringing technologies would harm the industry is the potential replacement of on-chip PLL/DLL and dual-edged clocking with alternatives that would have removed those features from the DDR-2 standard. (CCFF 2583-584).

Rambus's Response to Finding No. 2582:

The proposed finding is not supported by the weight of the evidence, which shows that there are no acceptable alternatives to Rambus's dual-edge clocking and on-chip PLL/DLL

technologies. (*See* RPF Section X.B.4; *see also* RRFF 2583-84).

2583. Removing the DLL from the DDR-2 standard would have led to the problem of requiring that firms that had been either designing DDR-2 SDRAMs, or designing products to be compatible with DDR-2, to redesign their systems. (Macri, Tr. 4649) ("[basically the earliest adopters would have had to go back to the design stage. Clocking is not something they can change in a trivial manner.... So, I mean, it's not something you want to go change at that point in time. You really need a gun to your head.")).

Rambus's Response to Finding No. 2583:

The proposed finding is misleading and not supported by the evidence. The Future DRAM Task Group, which is developing the DDR2 standard, *did* seek alternatives to Rambus's on-chip PLL/DLL technology. In late 1998, the Future DRAM Task Group assigned HP to investigate alternatives to the technology. (RX 1306 at 10; Macri, Tr. 4705). Both HP and IBM later proposed alternatives that would eliminate the on-chip PLL in DDR2. (CX 137 at 3, 4, 27). Yet the Task Group rejected this proposal and adopted Rambus's technology. (RX 1854 at 12-14). Further, other evidence confirms that there were no acceptable alternatives to Rambus's on-chip PLL/DLL technology. (*See* RPF 1078-1120).

Finally, the proposed finding is misleading to the extent that it suggests that JEDEC members were somehow "locked in" to using the Rambus technology because of the need to redesign. At the time Rambus's patents issued and it began requesting royalties for its on-chip PLL/DLL technology, *no DDR2 products had been produced*; the DDR2 standard was not nearly complete. (*See* RPF 733-41). There is no evidence that switching to alternatives at that point, or now, would be too costly.

2584. Changing the DDR-2 standard to use single-edged clocking rather than dual-edged clocking would have led to the problem of requiring that firms that had been either designing DDR-2 SDRAMs, or designing products to be compatible with DDR-2, to redesign their systems. (Kellogg, Tr. 5201 (The proposal to eliminate dual edged clocking from the DDR-2

standard "was a significant change to the DDR-II data capture structure, and IBM was already moving down the path of designing our first DDR-II memory controller at this time."); (Macri, Tr. 4649-51); (Wagner, Tr. 3869) ("[They would have,... brought in suggestions to change the technology and we would have said, we already have a standard, we don't really want to change, or we're on a development cycle that cannot tolerate the schedule hit."); Peisl, Tr. 5545-55); (Kellogg, Tr. 5205 ("One [potential impact of Micron's proposal to eliminate dual-edged clocking from DDR-2 on IBM] is our DDR-I controller or interface chip that also included DDR-II would very likely see measurable schedule delay due to the significance of the changes.").

Rambus's Response to Finding No. 2584:

The proposed finding is misleading and incomplete. The Future DRAM Task Group, which is developing the DDR2 standard, sought but could not find acceptable alternatives to Rambus's dual-edge clocking technology. After Rambus's patents issued and began to request royalties for its dual-edge clocking technology, the Task Group considered alternatives to Rambus's technology. In September 2000, Micron proposed that DDR2 incorporate single data rate technology instead of dual-edge clocking. (CX 2769 at 13). In a November 2000 conference call, committee members discussed going to single data rate ("SDR") technology. (Macri, Tr. 4639-42). The minutes of that meeting reflect a consensus to try to adopt SDR if it would work: "Discussion on single data rate clock vs. doble [sic] data rate clock . . . . Fundamentally question is that is single data rate clock possible? Micron believes that SDR has some advantages as it gets [rid] of duty cycle issue, it has old prior art, and the inherent bandwidth is better with write than read. . . . In general, everyone agreed that SDR clock is ok provided that it works." (CX 426 at 4). The overall consensus of the group was: "Single data rate clock is preferred provided we can make it work." (CX 426 at 4). Despite the consensus to use SDR in place of dual-edge clocking "provided we can make it work," JEDEC incorporated dual-edge clocking into DDR2. (Polzin, Tr. 4047).

Finally, the proposed finding is misleading to the extent that it suggests that JEDEC members were somehow "locked in" to using the Rambus technology because of the need to redesign. At the time Rambus's patents issued and it began requesting royalties for its dual-edge clocking technology, *no DDR2 products had been produced*; the DDR2 standard was not nearly complete. (*See* RPF 733-41). There is no evidence that switching to alternatives at that point, or now, would be too costly.

2585. Paragraphs 2585 - 2599 are unused.

XIII. Through its Conduct Rambus Obtained a Monopoly in Several DRAM Technology Markets.

A. Relevant Economic Characteristics of the DRAM Industry.

1. The Basic Economics of the DRAM Industry Tend to Drive the Industry to a Single Standard.

2600. The DRAM industry is characterized by large capital requirements, interoperability requirements, and commodity pricing to price sensitive customers. (CCFF 2602-617).

Rambus's Response to Finding No. 2600:

As addressed below, the proposed finding is contradicted by the evidence and misleading. (*See* RRFF 2601-617).

2601. Because the DRAM industry is characterized by large capital requirements, interoperability requirements, and commodity pricing to price sensitive customers, it tends to be driven to a single dominant commodity standard. (CCFF 2602-617; McAfee, Tr. 11228-229).

Rambus's Response to Finding No. 2601:

The proposed finding is unsupported, misleading, and contradicted by the weight of the evidence. There is no evidence that the "DRAM industry" is characterized by large capital investments. The only cited evidence refers to the cost of DRAM manufacturing facilities, and there is no evidence regarding the capital investments for other members of the DRAM industry. The evidence also does not show that the industry is driven to a "single dominant standard." The DRAM industry is marked by the coexistence of multiple standards with significant market shares at any given time. (*See* RPF 1267-77). For example, the statistics show that in 1996, Fast Page Mode ("FPM") DRAM accounted for 39.4% of the DRAM market revenue, EDO DRAM accounted for 52.7%, and SDRAM for 4.3%. (Rapp, Tr. 10101-04). In 1997, FPM accounted for 8.1% of the market, EDO for 55.2%, and SDRAM for 33.5%. In 1998, FPM accounted for

8.8% of the market, EDO for 27.6%, and SDRAM for 60.8%. (*Id.*) These statistics show a market divided between these three different DRAM standards, each with significant market shares. Even these statistics tell only part of the story, because DRAM standards have multiple, often incompatible, substandards. For instance, "SDRAM" actually comprises three different standards – PC 66, PC 100, and PC 133. (Gross, Tr. 2348-56; Polzin, Tr. 3998-4005; Bechtelsheim, Tr., 5959). Finally, the evidence shows that DRAM manufacturers produce multiple types of DRAM at any given time. For instance, in 2002, Infineon planned to produce 34 different types of DDR, 27 different types of SDRAM, 20 different types of Mobile DRAM, 7 different types of Graphics RAM, and 6 different types of RLDRAM. (CX 2466 at 5-9).

2602. The DRAM technologies at issue are used by DRAM manufacturers as well as by the manufacturers of DRAM-related logic like chip sets. (McAfee, Tr. 7183; *see* DX0132).

Rambus's Response to Finding No. 2602:

The proposed finding impermissibly cites, as evidence, the assumptions made by Complaint Counsel's economic expert. The cited demonstrative is also not in evidence.

2603. Manufacturers of DRAMs and controllers sell products incorporating the DRAM technologies at issue to firms like PC-OEMs that sell their products to consumers. (CCFF 11-16; McAfee, Tr. 7183-84; *see* DX0132).

Rambus's Response to Finding No. 2603:

The proposed finding impermissibly cites, as evidence, the assumptions made by Complaint Counsel's economic expert. The cited demonstrative is also not in evidence.

2604. DRAM customers include PC-OEMs, server-OEMs, manufacturers of workstations, printers, routers, and supercomputers. (McAfee, Tr. 7185-86; *see* DX0133). The largest component of DRAM demand is personal computers, which takes in excess of 60% of DRAM demand. (CCFF 25; McAfee, Tr. 7185; *see* DX0133).

Rambus's Response to Finding No. 2604:

The proposed finding impermissibly cites as evidence assumptions made by Complaint Counsel's economic expert. The cited demonstrative is also not in evidence.

2605. In general, the same types of DRAM devices are used in each of the products made by DRAM customers. (*See* CCFF 2507-508; McAfee, Tr. 7186). Some older products still use older DRAM technologies and some performance sensitive products use technologies that are newer than the current dominant technology. (McAfee, Tr. 7186).

Rambus's Response to Finding No. 2605:

The proposed finding impermissibly cites, as evidence, the assumptions made by Complaint Counsel's economic expert. The proposed finding is also misleading. (*See* RRFF 2507-08).

2606. The reason the same types of DRAM devices are used in a wide variety of products stems from the basic economics of the DRAM industry. (CCFF 2607-617; McAfee, Tr. 7186-87).

Rambus's Response to Finding No. 2606:

The proposed finding is not supported by the evidence. (*See* RRFF 2607-16).

2607. There are large capital requirements to manufacturing DRAMs. (McAfee, Tr. 7187-88; *see* DX0135). The cost of building a DRAM manufacturing facility is in excess of $1.5 billion. (*See* CCFF 31; McAfee, Tr. 7187-88; *see* DX0135).

Rambus's Response to Finding No. 2607:

The proposed finding impermissibly cites, as evidence, the assumptions made by Complaint Counsel's economic expert. The proposed finding is also not supported by the cited evidence and is misleading. (*See* RRFF 31).

2608. Large capital requirements, like those seen in the DRAM industry, leads to increasing returns to scale in the sense that increasing production leads to reduced cost of production because the large fixed investments can be spread over a larger amount of production. (CCFF 104; McAfee, Tr. 7189).

Rambus's Response to Finding No. 2608:

The proposed finding is misleading. Economies of scale occur at the plant level, so increasing production beyond the capacity of a single plant does not necessarily lead to reduced costs. (Rapp, Tr. 9893). Further, the proposed finding miscites the evidence; economies of scale lead to reduced costs of production *per unit*, not to an overall decrease in costs. (McAfee, Tr. 7189).

2609. Increasing returns to scale tends to create a single dominant standard product and makes it difficult to displace an existing standard product because that product will tend to be the lowest cost. (McAfee, Tr. 7472-73).

Rambus's Response to Finding No. 2609:

The proposed finding is not supported by the weight of the evidence. The DRAM industry produces and supports multiple DRAM standards at any given time. (*See* RPF 1267-77). The evidence shows that there is *not* "a single dominant standard product." (*See* RRFF 2601). Moreover, DRAM manufacturers produce multiple types of DRAM at any given time. In 2002, Infineon planned to produce 34 different types of DDR, 27 different types of SDRAM, 20 different types of Mobile DRAM, 7 different types of Graphics RAM, and 6 different types of RLDRAM. (CX 2466 at 5-9). These facts show that scale economies are not so powerful that they drive the industry to a single dominant standard, in part because scale economies occur mainly at the plant level. (Rapp, Tr. 9893-95). The evidence also shows that the DRAM industry routinely moves to new DRAM standards, nearly once a year. (*See* RPF 1308-28).

2610. Interoperability between DRAM chips and other components is important in the DRAM industry. (CCFF 25-28, 2541-542, 2550-562; McAfee, Tr. 7189-90). Interoperability refers to the need for DRAM to work with other components in the system. (CCFF 26; McAfee,

Tr. 7190; *see* DX0030).

Rambus's Response to Finding No. 2610:

The proposed finding is misleading to the extent that it implies that there are interoperability requirements beyond parts compatibility. (*See* RRFF 27).

2611. Interoperability leads to a type of network externality. (McAfee, Tr. 7191). The need for interoperability between DRAM and other components means that as more of a particular type of DRAM is made, more compatible components become available, or become cheaper. The availability of compatible components makes it easier to use that type of DRAM, which increases the production of that type of DRAM. (CCFF 2550-562; McAfee, Tr. 7609-10; 11212-213). This type of network externality is sometimes called "indirect" network effect. (McAfee, Tr. 11212-213).

Rambus's Response to Finding No. 2611:

The proposed finding is misleading. Complaint Counsel's economic expert admitted on cross-examination that the only "network externality" he identified in the DRAM industry is that fixed costs of complementary components may be amortized over a larger volume of units. (McAfee, Tr. 7610-11). The proposed finding is also not supported by the evidence, which shows multiple types of DRAM being produced at any given time. (*See* RRFF 2550-62, 2601).

2612. Network effects have "the effect that, ... the choice of the technology by the marketplace or dominant share of the technology in the marketplace can lead to lock-in and hence confer market power on the technologies incorporated in the standard." (McAfee, Tr. 11216-217)

Rambus's Response to Finding No. 2612:

The proposed finding is not supported by the weight of the evidence. The DRAM industry produces and supports multiple DRAM standards with significant market shares at any given time. (*See* RPF 1267-77; RRFF 2601). This evidence shows that network effects in the DRAM industry do *not* make it impractical to switch to an alternative technology, i.e., they do

not lead to lock in or confer market power. (Rapp, Tr. 9895).

2613. DRAM customers are price sensitive. (CCFF 99; McAfee, Tr. 7192-93). Because PC-OEM customers are generally unwilling to pay increases in price for DRAMs with a higher performance, that makes the PC-OEMs generally unwilling to agree to pay higher prices as well. (McAfee, Tr. 7192). Evidence of the sensitivity of PC-OEM customers to changes in DRAM prices is that when DRAM prices fall, PC consumers buy a large amount of DRAM to upgrade their current computers. (McAfee, Tr. 7193).

Rambus's Response to Finding No. 2613:

The proposed finding is unsupported; it depends on the testimony of Complaint Counsel's economic expert for percipient facts. Prof. McAfee is not competent to testify to the facts in question. He also admitted on cross-examination that he had done no study of consumer price sensitivity. (McAfee, Tr. 7566). The documents cited in the cross-reference reflect a few hearsay comments from some customers and others standing for the unremarkable proposition that they prefer low costs, but this does not mean that all DRAM customers are "price sensitive" in that they would curtail purchasing or forgo performance due to small increases in price. (*See* RRFF 99). The evidence shows a great concern among DRAM customers that DRAM performance was limiting computer system performance. (*See* RPF 35-40; RX 285A ("the DRAM interface has become more and more a problem for system developers")).

2614. DRAMs are generally commodities. (CCFF 93-94, 2548-549; McAfee, Tr. 7200-201). Products that are commodities are perfect substitutes for each other. (McAfee, Tr. 7200). DRAM is nearly a perfect commodity in the sense that the standardized DRAM from any manufacturer is supposed to work in any application that can use that standardized DRAM. (CCFF 2548-549; McAfee, Tr. 7201).

Rambus's Response to Finding No. 2614:

Rambus has no specific response.

2615. It is well understood in the industry that standardized DRAM is a commodity. (CCFF 93-94)

Rambus's Response to Finding No. 2615:

Rambus has no specific response.

2616. Because DRAM is a commodity DRAM customers are able to buy DRAM from multiple sources. That allows them to achieve price competition and reduce risk. (CCFF 117-118, 2547-549; McAfee, Tr. 7201). Another implication is that final consumers are more likely to be able to upgrade their computers. (McAfee, Tr. 7201).

Rambus's Response to Finding No. 2616:

Rambus has no specific response to the first sentence. The second sentence is unsupported, for it relies upon the testimony of Complaint Counsel's economic expert for percipient facts.

2617. Additionally "given the value that's placed on the commodity nature of DRAM, the process by which technologies are selected put an emphasis on standards that applies to all companies that are in the marketplace." (McAfee, Tr. 7202).

Rambus's Response to Finding No. 2617:

The proposed finding is not supported; it relies upon the testimony of Complaint Counsel's economic expert for percipient facts.

2. The Economics of DRAM Production Can Lead to the Dominance of the Industry by a Single Type of Product.

2618. Reducing cost per bit to manufacture DRAM is one of the most important factors relating to the success of a DRAM manufacturer. (CCFF 95-98). DRAM manufacturers reduce costs by various methods, including die shrinks and increasing wafer size. Each of these methods have the effect of encouraging a single product to be the dominant product. (CCFF 2619-2624).

Rambus's Response to Finding No. 2618:

The proposed finding is not supported by the weight of the evidence. Although DRAM manufacturers do seek to reduce costs, the evidence shows that multiple DRAM products with significant market shares coexist at any given time. (*See* RPF 1267-77; RRFF 2601). This

shows that there is no technological or economic force mandating a single dominant standard in the DRAM industry. (Rapp, Tr. 10103-04).

2619. One method that the DRAM industry has of reducing costs is through "die shrinks," which lead to increased production for a DRAM being produced on a wafer of a given size. Once the die size has been reduced, more DRAM chips can be produced on the wafer. (CCFF 103-106; McAfee, Tr. 7217).

Rambus's Response to Finding No. 2619:

Rambus has no specific response.

2620. Because of the high fixed costs of doing a die shrink, DRAM manufacturers will apply die shrinks to the highest volume DRAMs, leading those DRAMs to be low cost relative to the other DRAMs on the market, which increases the sales of that DRAM. (CCFF 105-106; McAfee, Tr. 7218).

Rambus's Response to Finding No. 2620:

The proposed finding is not supported. The proposed finding regarding the application of die shrinks rests on evidence from a non-manufacturer. (*See* RRFF 105). The evidence shows that DRAM manufacturers are constantly redesigning different types of DRAM. (*See* RPF 1278-86). For example, Micron taped out from { } new DRAM designs in each year between 1998 to 2002, and is { } (Shirley, Tr. 4218-29, 4282 (*in camera*)).

2621. The current high volume DRAM product is always the first to experience cost reduction efforts by the DRAM manufacturers. (McAfee, Tr. 7217; CCFF 105-106).

Rambus's Response to Finding No. 2621:

The proposed finding is not supported. (*See* RRFF 105-06).

2622. The emphasis of the industry to reduce costs in this way encourages a single product to be the dominant product. (McAfee, Tr. 7225).

Rambus's Response to Finding No. 2622:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 2618). The evidence shows that multiple DRAM standards with significant market shares coexist at any given time: there is no single dominant standard. (*See* RRFF 2601).

2623. Another method that the DRAM industry has of reducing costs is through increasing the wafer size. That method also reduces marginal costs by the application of substantial fixed investments. (McAfee, Tr. 7218).

Rambus's Response to Finding No. 2623:

The proposed finding is not supported; it rests only on the testimony of Complaint Counsel's economic expert for percipient facts.

2624. Regarding the implications of increasing wafer size, "...it's the feedback effect that's important from an economist's perspective. That is to say, we apply our cost reduction to our majority product and that has a feedback effect of lowering the cost of that product which then through the marketplace leads that product to even grow even larger as a proportion of the total demand." (McAfee, Tr. 7218-19).

Rambus's Response to Finding No. 2624:

The proposed finding is not supported. There is no evidence other than the say-so of Complaint Counsel's economic expert in support of the finding.

3. The Economics of DRAM Demand Tend to Lead to a Single DRAM Standard.

2625. Large DRAM customers require multiple sources for the DRAM that they buy. (CCFF 2626). This has the effect of encouraging a single product to be the dominant standard. (CCFF 2627- 630).

Rambus's Response to Finding No. 2625:

The proposed finding is not supported by the weight of the evidence. Although large DRAM customers do require multiple sources, the evidence shows that multiple DRAM products

with significant market shares coexist at any given time. (*See* RPF 1267-77; RRFF 2601). The evidence also shows that DRAM manufacturers produce multiple types of DRAM simultaneously; they are thus able to accommodate any need for multiple sources without the existence of a single dominant standard. (RPF 1287-1300; Rapp, Tr. 9893-94). This shows that there is no technological or economic force mandating a single dominant standard in the DRAM industry. (Rapp, Tr. 9893-94, 10103-04).

2626. PC-OEMs as well as other large DRAM customers require that the DRAM that they buy have multiple sources. (CCFF 116-118, 2547-549).

Rambus's Response to Finding No. 2626:

Rambus has no specific response.

2627. Multiple sourcing reduces risk and ensures price competition among DRAM suppliers. (CCFF 116-118; McAfee, Tr. 7220).

Rambus's Response to Finding No. 2627:

Rambus has no specific response.

2628. The use of multiple sources by PC-OEMs tends to encourage a single product or not very many products to be a dominant standard. (McAfee, Tr. 7225-226).

Rambus's Response to Finding No. 2628:

The proposed finding is not supported by the weight of the evidence. Although PC-OEMs do use multiple sources, the evidence shows that multiple DRAM products with significant market shares coexist at any given time. (*See* RPF 1267-77; RRFF 2601). The evidence also shows that DRAM manufacturers produce multiple types of DRAM simultaneously; they are thus able to accommodate any need for multiple sources without the existence of a single dominant standard. (RPF 1287-1300; Rapp, Tr. 9893-94). This shows that there is no

technological or economic force mandating a single dominant standard in the DRAM industry. (Rapp, Tr. 9893-94, 10103-04).

2629. An implication of the cost sensitivity of the final consumer is that PC-OEMs are also cost sensitive. As a result, DRAM manufacturers are driven to reduce costs. (CCFF 99-100; McAfee, Tr. 7222).

Rambus's Response to Finding No. 2629:

The proposed finding is not supported. (*See* RRFF 99-100, 2613).

2630. When design, testing and qualification costs are large, firms want to try to use a single or not too many different flavors or varieties of DRAM so that they don't have to go through the whole design, testing and qualification process over and over and over again. This creates more pressure for having a single, dominant flavor of DRAM. (McAfee, Tr. 7223).

Rambus's Response to Finding No. 2630:

The proposed finding is not supported, for it relies solely upon the testimony of Complaint Counsel's economic witness for percipient facts. In addition, although DRAM manufacturers do seek to reduce costs, the evidence shows that multiple DRAM products with significant market shares coexist at any given time. (*See* RPF 1267-77; RRFF 2601). The evidence also shows that DRAM manufacturers produce multiple "flavors" of DRAM at any given time. (*See* RRFF 2601; RPF 1287-1307). This shows that there is no technological or economic force mandating a single standard in the DRAM industry. (Rapp, Tr. 10103-04).

4. The Importance of Standards to the DRAM Industry.

2631. Standards are an essential element in the competitive landscape of the DRAM industry because standards facilitate the use of multiple suppliers, interoperability of DRAMs with other components, and the achievement of economies of scale, all of which tends to lower the total cost to the industry of meeting consumer demand. (McAfee, Tr. 7230; CCFF 2632-639).

Rambus's Response to Finding No. 2631:

While standards may have the economic effects listed in the proposed finding, the

evidence does not fully support finding that such effects occur in the DRAM industry to a great extent, and these economic effects are not so great in the DRAM industry as to require a single dominant standard or to prevent switching to alternative standards. (*See* RRFF 2601; Rapp, Tr. 10103-04; Rapp, Tr. 9894-95). To this extent, standards are not an "essential element."

2632. Because they allow for multiple suppliers, standards are very important for minimizing the total cost of products that use DRAMs. (McAfee, Tr. 7231; CCFF 117).

Rambus's Response to Finding No. 2632:

While standards may have the economic effects listed in the proposed finding, these economic effects are not so great in the DRAM industry as to require a single dominant standard or to prevent switching to alternative standards. (*See* RRFF 2601; Rapp, Tr. 10103-04; Rapp, Tr. 9894-95). To this extent, standards are not "very important."

2633. Because they allow for interoperability, standards are very important for minimizing the total cost of products that use DRAMs. (McAfee, Tr. 7231; CCFF 114-115).

Rambus's Response to Finding No. 2633:

The proposed finding is not supported. (*See* RRFF 114-15). Further, while standards may have the economic effects listed in the proposed finding – although the evidence cited by Complaint Counsel do not fully support a such a finding in this industry (*see* RRFF 114-15) – these economic effects are not so great in the DRAM industry as to require a single dominant standard or to prevent switching to alternative standards. (*See* RRFF 2601; Rapp, Tr. 10103-04; Rapp, Tr. 9894-95).

2634. Because they allow for leveraging the costs of the design, standards are very important for minimizing the total cost of products that use DRAMs. (McAfee, Tr. 7231; CCFF 119, 121).

Rambus's Response to Finding No. 2634:

The proposed finding is not supported. (*See* RRFF 119). Further, while standards may have the economic effects listed in the proposed finding – although the evidence cited by Complaint Counsel do not fully support a such a finding in this industry, especially with regard to JEDEC standards (*see* RRFF 119, 121), these economic effects are not so great in the DRAM industry as to require a single dominant standard or to prevent switching to alternative standards. (*See* RRFF 2601; Rapp, Tr. 10103-04; Rapp, Tr. 9894-95).

2635. By setting a common design, an advantage to the marketplace as a whole of standards is that DRAM customers benefit from price competition. (McAfee, Tr. 7231-32; CCFF 116-117).

Rambus's Response to Finding No. 2635:

The proposed finding is misleading and not supported. (*See* RRFF 116-17). Further, while standards may have the economic effects listed in the proposed finding, these economic effects are not so great in the DRAM industry as to require a single dominant standard or to prevent switching to alternative standards. (*See* RRFF 2601; Rapp, Tr. 10103-04; Rapp, Tr. 9894-95).

2636. Formal standardization can reduce costs by allowing for the achievement of economies of scale. (Rapp, Tr. 10055).

Rambus's Response to Finding No. 2636:

Economics of scale in the DRAM industry occur at the plant level and are not so great in the DRAM industry as to require a single dominant standard or to prevent switching to alternative standards. (*See* RRFF 2601; Rapp, Tr. 10103-04; Rapp, Tr. 9894-95).

2637. Achievement of economies of scale is a benefit of formal standardization in the case of JEDEC's SDRAM standards. (Rapp, Tr. 10055).

Rambus's Response to Finding No. 2637:

Economics of scale in the DRAM industry occur at the plant level and are not so great in the DRAM industry as to require a single dominant standard or to prevent switching to alternative standards. (*See* RRFF 2601; Rapp, Tr. 10103-04; Rapp, Tr. 9894-95).

2638. Standards in the DRAM industry serve to define the characteristics of the DRAM in such a way that compatible component manufacturers know enough about the DRAM to know how to design their products. (McAfee, Tr. 7234; CCFF 115).

Rambus's Response to Finding No. 2638:

The proposed finding is not supported. (*See* RRFF 115). The proposed finding is also misleading in that not all standards in the DRAM industry have achieved the objective of allowing complementary component manufacturers to design compatible products. For example, the JEDEC SDRAM standard failed to achieve compatibility until Intel redefined the standard. (MacWilliams, Tr. 4907-09). Further, there are examples in which JEDEC standards have gone beyond compatibility requirements and unnecessarily standardized other functions. (*See* RRFF 503, 655).

2639. A benefit of formal standardization is that it helps to create a market consensus about which technology to use. (Rapp, Tr. 10054).

Rambus's Response to Finding No. 2639:

The proposed finding is incomplete. The evidence shows that formal standardization is not necessary to create market consensus. (*See* RPF 1517-23).

5. Economic Factors Influencing the Success of DRAM Standards.

2640. The success of DRAM standards is influenced by a number of factors, including the cost of the standardized DRAM, the use of consensus based standard-setting to arrive at the standard, and the use of evolutionary technologies in the standard rather than revolutionary technologies. (CCFF 2641-649).

Rambus's Response to Finding No. 2640:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 2641-49).

2641. One factor important in determining the success of a DRAM standard is its cost compared to the current standard. The way standards tend to succeed each other in the DRAM market is that newer products tend to be higher priced and be used in niche applications that demand higher performance. Over time the cost of production of the new DRAM falls as more of it is produced. Eventually, the industry "tips" toward the newer DRAM as its cost falls in relation to the older DRAM. (McAfee, Tr. 7229-30; CCFF 105-106, 125-126).

Rambus's Response to Finding No. 2641:

The proposed standard is misleading in it undervalues the role of improved performance as the driving factor in new DRAM standards. Complaint Counsel's economic expert admitted that each successive type of DRAM had improved performance over the previous type. (McAfee, Tr. 11347-48).

2642. The DRAM industry experiences periods where there is a dominant standard and periods where there is a transition between dominant standards. For example, in 1994, fast page mode was at 95 percent market penetration and was the dominant standard. (McAfee, Tr. 11227; *see* DX0141). After that, a transition took place from fast page mode to EDO and then from EDO to SDRAM, and, in the latter part of the relevant time period, another transition from SDRAM to DDR took place. (McAfee, Tr. 11227; *see* DX0141; CCFF 85-89).

Rambus's Response to Finding No. 2642:

The proposed finding is misleading, leaves out relevant information, and is not supported. The evidence shows that the DRAM does not tend to have a dominant single standard at any given time. In 1994, fast page mode ("FPM") DRAM accounted for 96.7% of the revenue for DRAM. (Rapp, Tr. 10100, 10248). The remaining 3% of DRAM revenue was accounted for by other DRAM technologies. (Rapp, Tr. 10248). In 1995, FPM accounted for 87.2%, EDO DRAM for 9.9%, and other DRAM for 2.9% of DRAM revenue. (Rapp, Tr. 10100-01, 10248).

In 1996, FPM accounted for 39.4%, EDO for 52.7%, SDRAM for 4.3%, RDRAM for 0.5%, and other DRAM for 3.1% of DRAM revenue. (Rapp, Tr.10101, 10248). In 1997, FPM accounted for 8.1%, EDO for 55.2%, SDRAM for 33.5%, RDRAM for 1.3%, and other DRAM for 1.8% of DRAM revenue. (Rapp, Tr. 10101, 10248). In 1998, FPM accounted for 8.8%, EDO for 27.6%, SDRAM for 60.8%, RDRAM for 1.6%, and other DRAM for 1.3% of DRAM revenue. (Rapp, Tr. 10101, 10249). In 1999, FPM accounted for 10.5%, EDO for 17.5%, SDRAM for 69.3%, RDRAM for 1.1%, and other DRAM for 1.5% of DRAM revenue. (Rapp, Tr. 10102, 10249). In 2000, FPM accounted for 5.2%, EDO for 11.1%, SDRAM for 78.4%, RDRAM for 3%, DDR for 0.4%, and other DRAM for 1.9% of DRAM revenue. (Rapp, Tr. 10101, 10249). In 2001, FPM accounted for 4%, EDO for 7.7%, SDRAM for 69.7%, RDRAM for 12.5%, DDR for 5.3%, and other DRAM for 0.8% of DRAM revenue. (Rapp, Tr. 10101, 10249). These statistics only tell a part of the story. Within these standards there were different substandards (e.g, for SDRAM, PC66, PC100, PC133; for DDR, DDR200, DDR266, DDR333, DDR400). (Rapp, Tr. 10249-50; Gross, Tr. 2348-56; Polzin, Tr. 3998-4005). This evidence thus shows that, rather than a single dominant standard, the DRAM industry supports multiple DRAM standards with significant market shares.

2643. Dr. Rapp agrees that the DRAM industry is an industry that one generation after another has tended in the 1990s to select one standard to the exclusion of others. (Rapp, Tr. 10106).

Rambus's Response to Finding No. 2643:

The proposed finding is misleading. Dr. Rapp testified:

> Q. . . . Now, doesn't this data from your report summarized and rounded off in this exhibit suggest that in the DRAM industry having a

single leading or dominant standard is or has been important?

A. Mr. Royall, I couldn't disagree more because the chart that we have in front of us, it seems to me, without any computation or anything, teaches exactly, exactly the opposite thing.

Just look at the years that you read off to me, 1996 through 1998. In 1996, when – or let me go back a year if I may. In 1995, fast page mode has an 87.2 share. In the following year, it's down to 40 percent, 39 -- sorry -- 39.4 percent, and EDO has taken the lead with 52.7. But there's a difference between them of 12 percentage points. The market in that year is divided between two different standards and it teaches just the opposite. In other words, there was no computer meltdown or anything like that. The following year, just one year later, SDRAM is in the market and has captured, if I'm reading this right, a 33.5 percent share and FPM isn't gone with either.

So what we've got in any given year is the market being divided among incompatible stan FPM and EDO, but it seems to me that it teaches exactly the opposite thing, that there is notechnological requirement that only one standard has to dominate.

(Rapp, Tr. 10103-04).

Dr. Rapp further testified that "[i]t is an industry that one generation after another has tended in the past, in the decade that we're looking at, to select one standard to the exclusion of others. That is not motivated by the economics of the industry or the, as I understand it, the technology requirements associated with compatibility, and there is nothing in economics or

technology that, as I understand it, compels that outcome, and that apparently is true to the analysts at Cahners InStat who are the source of these data because those analysts predicting the future imagined a division of the market between RDRAM and DDR in the same generation." (Rapp, Tr. 10106).

2644. The DRAM industry experiences a coordination problem regarding the adoption of new DRAM standards. This problem can hinder investment in a developing standard. (McAfee, Tr. 7241-42 ("In making investments in a technology one very much wants to forecast which technology will be successful; that is to say, you don't want to make investments in, say, supporting a product that won't ultimately be used by the market.")). For example, in the late 1990s, it was unclear whether the DRAM industry would follow SDRAM with DDR SDRAM or with RDRAM. This made it difficult for firms in the industry to forecast and make appropriate investments. (CCFF 115).

Rambus's Response to Finding No. 2644:

The proposed finding is misleading and it leaves out relevant information. The DRAM industry frequently and routinely overcomes any "coordination problem" and shifts to new DRAM technologies. (*See* RPF 1308-32). For instance, AMD migrated its K7 systems from PC100 to PC133 to DDR200 and 266 to DDR333 to DDR400 in less than four years; each shift required new chipsets and new motherboards. (*See* RPF 1311-20). Similarly, Compaq migrated its systems from EDO to PC66 to PC100 to PC133 to DDR266 to DDR333 in less than seven years. (*See* RPF 1322-28). Coordination issues would not prevent switching to alternatives. (Rapp, Tr. 9889-90).

2645. By involving more market participants, an open, consensus-based process has the advantage of improving the accuracy of the forecast by more of the potential users of the standard. That improves the chances that the standard will ultimately be successful. (McAfee, Tr. 7241-42; CCFF 120).

Rambus's Response to Finding No. 2645:

The proposed finding is not supported. The finding rests entirely on the testimony of

Complaint Counsel's economic expert for percipient facts. The other cited evidence says nothing about "improving the accuracy of the forecast" or increasing success. (*See* CCFF 120). The evidence also shows that the JEDEC standardization process was not an "open, consensus-based process" but was captured by a small group of DRAM manufacturers. (*See* RRFF 206, 244).

2646. One benefit of the fact that there is a diverse group of firms at JEDEC, with diverse interests is that the outcome of the process is more likely to result in a consensus that addresses the needs of the different users of DRAM. (McAfee, Tr. 7251-53; CCFF 120).

Rambus's Response to Finding No. 2646:

The proposed finding is not supported. The finding relies upon the testimony of Complaint Counsel's economic expert for percipient facts. The evidence shows that the JEDEC standardization process was not "diverse" but was captured by a small group of DRAM manufacturers. (*See* RRFF 206, 244).

2647. Royalties have an influence on the success of standards because they are charges for the use of the standard, and so insofar as the standard requires royalties, it's less likely to be successful. And the higher the royalties, the less likely the standard will be successful, other things equal. (McAfee, Tr. 7243; CCFF 107-109).

Rambus's Response to Finding No. 2647:

The proposed finding is contrary to the evidence. The evidence shows that JEDEC routinely standardized royalty bearing technologies. (*See* RPF 1221-38; RRFF 107). Further, the proposed finding is misleading if it implies that royalty bearing technologies are somehow judged by a different standard than other technologies. Royalties are a cost like any other. A competitive market will not allow for any prejudice against royalty bearing technologies; if the best solution in cost-performance terms is patented and involves the payment of royalties, competition will dictate that the royalties be paid and that the patented solution be adopted.

(Rapp, Tr. 9939).

2648. Other things equal, an evolutionary approach to DRAM standards will tend to be more successful than a revolutionary approach. (McAfee, Tr. 7245). One reason is that an evolutionary approach has an advantage of reusing knowledge. The implementation costs will tend to be lower. The risks will tend to be lower with an evolutionary approach. (McAfee, Tr. 7245; *see* DX0146; ***CCFF*** 127-128).

Rambus's Response to Finding No. 2648:

The proposed finding is not supported. (*See* RRFF 127-28). The proposed finding is also misleading in the use of the terms "evolutionary" and "revolutionary." (*See* Response to Finding 2649). The proposed finding is also misleading because it is rarely the case that all other things are equal. Complaint Counsel's economic expert admitted that a significant performance gain would lead to a preference for revolutionary technologies. (McAfee, Tr. 7694).

2649. "Evolutionary" means built on the existing product or existing knowledge base as opposed to a dramatic change from the existing product or knowledge base. "Revolutionary" is a radical departure, a major departure from the existing technologies and products. (McAfee, Tr. 7245-46).

Rambus's Response to Finding No. 2649:

The proposed finding is not supported. (*See* RRFF 127-28). The proposed finding is also misleading in that it adopts Professor McAfee's definitions of "revolutionary" and "evolutionary" - two ill-defined terms - without citing any evidence that these definitions were shared by members of the DRAM industry.

6. JEDEC's Standard Setting Process.

2650. JEDEC is a consensus-based organization. As a result, JEDEC standards will generally be the result of compromise between JEDEC members rather than the best standard in some abstract sense. ((CCFF 2651). Also, because of the need for timely standards in the DRAM industry, JEDEC "satisfices" in choosing technologies to incorporate into the standard. Because JEDEC satisfices, when it chooses technologies, the standard chosen might not have been the best possible standard. (CCFF 2652-2658).

Rambus's Response to Finding No. 2650:

The proposed finding is not supported by the weight of the evidence. The evidence shows that the JEDEC process was not "consensus driven" but has been "captured" by a group of DRAM manufacturers. (*See* RRFF 206, 244). The evidence also shows that JEDEC tried to find the best alternative in cost-performance terms. The chair of JC42.3 testified that JEDEC selected the "best" technologies for its standards. (Kelley, Tr. 2709-09). Micron's representatives testified that "we had long discussions of the pros and cons of various options and tried to determine what was the best standard." (Williams, Tr. 770). IBM's representative testified that his job was to work with the industry to find the "optimal solution, price/performance." (Kellogg, Tr. 5113).

The evidence thus does not support the notion that JEDEC did not seek to find the best solution in cost-performance terms. As Dr. Rapp explained, if "satisficing" means that "manufacturers weren't particularly interested in finding the best solution in cost-performance terms, I guess I dont understand that. And the reason that I don't understand that is that it seems to me that that's what manufacturers are up to in the normal course of business generally, and we see decisions in JEDEC which point to, you know, in the balloting process and so forth, that point to the attempts to find the right cost-performance solution, the best cost-performance solution." (Rapp, Tr. 9806). The proposed finding is also contrary to Complaint Counsel's proposed findings that the DRAM industry was striving for the highest performance at the lowest cost. (*See* CCFF 2629). If the *industry* was concerned about performance and concerned about costs, there is no reason why industry members would ignore these concerns while at JEDEC.

Contemporaneous JEDEC documents show that performance and cost were, indeed,

carefully considered by JEDEC members. (CX 18 at 5 (JEDEC minutes showing Mitsubishi comments regarding performance concerns related to proposal; CX 34 at 9 (JEDEC minutes showing concern that proposed package would have slow performance); CX 47 at 3 ("There was a lot of discussion about the NOPs in all banks idle entry. Mr. Lai (Intel) had strong feelings about it – it was something that gives slightly more performance.")) Further, to the extent that JEDEC standards do represent an effort to meet diverse needs, this would only elevate the importance of flexibility, and the Rambus technologies were the most flexible. (Kellogg, Tr. 5132 (regarding alternatives for burst length: "The proposal that IBM supported to the greatest extent at least was the programmable feature. It offered us the greatest flexibility."); Kellogg, Tr. 5143 (IBM chose programmable CAS latency because of flexibility: "My recollection is the decision was based more on flexibility."); Sussman, Tr. 1375 ("Q. What were the advantages to using these programmable features in an SDRAM? A. I had a range of customers. The largest customer, of course, is the PC, so that's an application, but I also had a number of smaller customers with slightly different requirements. They could all fold and use the PC one, but it would be more convenient for them, the part would become more flexible."))

The proposed finding is also contrary to Complaint Counsel's assertion that JEDEC was adverse to royalty-bearing patented technologies; if satisficing means that JEDEC was indifferent to differences in cost-performance, then it would be indifferent to paying royalties as well. (Rapp, Tr. 9839).

2651. The outcome of the JEDEC process is a consensus product that strikes a balance between the needs of a diverse set of industry participants. (McAfee, Tr. 7252-53; CCFF 206, 211-213, 242-249, 251, 254).

Rambus's Response to Finding No. 2651:

The proposed finding is not supported by the weight of the evidence. The evidence shows that the JEDEC process has been captured by a handful of DRAM manufacturers. (*See* RRFF 206, 244). To the extent that JEDEC standards do represent an effort to meet diverse needs, this would only elevate the importance of flexibility, and the Rambus technologies were the most flexible. (*See* RRFF 2651).

2652. Completing standards in a timely manner is important to JEDEC. (CCFF 122-124).

Rambus's Response to Finding No. 2652:

The proposed finding is not supported. (*See* RRFF 123-24). It is also misleading to the extent that it could be construed to imply that JEDEC did not deliberate on issues of cost and performance. (*See* RRFF 2650).

2653. The importance of having a standard completed rapidly is more important in this industry than in other industries. (McAfee, Tr. 7253 ("There's been a great deal of technical change, technological change, and as a consequence, time to market is more important here than in, say, the automobile industry.")).

Rambus's Response to Finding No. 2653:

The proposed finding is not supported by the evidence. It relies upon Complaint Counsel's economic expert's assumptions as percipient facts. (McAfee, Tr. 7251 ("Q. And does this slide identify factors about the JEDEC process that have formed important assumptions related to your economic analysis? A. It does. It does provide such -- yeah."). It is also misleading to the extent that it could be construed to imply that JEDEC did not deliberate on issues of cost and performance. (*See* RRFF 2650).

2654. The result of the need for timely standards is that there is a stronger incentive for

timely decisions than there would otherwise be. (McAfee, Tr. 7253-54 ("It tends to put pressure on a fast decision over, say, the perfect decision.")).

Rambus's Response to Finding No. 2654:

The proposed finding is not supported by the evidence. It relies upon Complaint Counsel's economic expert's testimony for percipient facts. (McAfee, Tr. 7251 ("Q. And does this slide identify factors about the JEDEC process that have formed important assumptions related to your economic analysis? A. It does. It does provide such -- yeah."). It is also misleading to the extent that it could be construed to imply that JEDEC did not deliberate on issues of cost and performance. (*See* RRFF 2650; *see also* RRFF 123).).

2655. The speed at which the industry moves makes intellectual property more important than it otherwise would be. (McAfee, Tr. 7254-55 ("And I should say the speed at which this industry moves perhaps makes IP more important, again, than in some other industries. Just there's more technological change, more technological advance, in this industry than in many industries.")).

Rambus's Response to Finding No. 2655:

The proposed finding is not supported by the evidence, for it relies upon Complaint Counsel's economic expert's testimony for percipient facts. (McAfee, Tr. 7251 ("Q. And does this slide identify factors about the JEDEC process that have formed important assumptions related to your economic analysis? A. It does. It does provide such -- yeah."). The proposed finding also has no basis for why the purported "speed" of industry movement would necessarily mean that intellectual property is "more important than it otherwise would be."

2656. The term "satisficing" is an economics term that describes the decision-making process of JEDEC in its choices of features and technologies. (McAfee, Tr. 7255). Satisficing refers to the process by which an organization like JEDEC will choose an adequate solution to a problem it faces rather than expending the effort to find the perfect solution. (McAfee, Tr. 7255-56; CCFF 124).

Rambus's Response to Finding No. 2656:

The proposed finding is not supported. (*See* RRFF 2650-55). The evidence shows that JEDEC deliberated constantly on issues of cost and performance. (*See* RRFF 2650).

2657. Satisficing behavior is driven, in part, by the need for timely standards. (McAfee, Tr. 7256).

Rambus's Response to Finding No. 2657:

The proposed finding is not supported. (*See* RRFF 2650-55). The evidence shows that JEDEC deliberated constantly on issues of cost and performance. (*See* RRFF 2650).

2658. One implication of satisficing behavior is that while the technologies actually chosen may have been thought to solve the problems faced by JEDEC, there is no reason to believe that the standard actually chosen was the best standard. (McAfee, Tr. 7256 ("[I]ts importance in terms of the economic analysis is that this says generally you can't conclude from the very choice of the technology that it was necessarily even the best of the available alternatives. It just means it was in the top set or the top group. It had good qualities.")).

Rambus's Response to Finding No. 2658:

The proposed finding is not supported. (*See* RRFF 2650-55). The evidence shows that JEDEC deliberated constantly on issues of cost and performance. (*See* RRFF 2650).

7. Lock in and Hold-Up.

2659. A firm can be held up if that firm is better off paying higher prices to use the investments that it is locked in to rather than switching to new investments. Hold-up for the use of a standard can occur if firms become locked in to the technologies in the standard. (CCFF 2660-673).

Rambus's Response to Finding No. 2659:

The proposed finding is unclear. Lock-in occurs when switching costs prohibit consumers from changing to another product or technology. (Rapp, Tr. 9873-74). Specific investments and switching costs, however, are not identical. (Rapp, Tr. 9875-77). Switching

costs are only those costs necessary for a transition to an alternative. (Rapp, Tr. 9873-74). Not all specific investments qualify as switching costs. (Rapp, Tr. 9873-74).

2660. The hold-up problem arises in general because investments that are specific to another party are vulnerable in renegotiation -- the other party can extract some or all of the value of the investments. The value of specific assets -- those specific to a relationship with another party -- are vulnerable to expropriation by that other party because the assets have low or no value without the other party's participation. (McAfee, Tr. 7258; *see* DX0148).

Rambus's Response to Finding No. 2660:

The proposed finding is misleading and contrary to more reliable evidence. The problem of hold up is related to switching costs, not specific investments, which are not identical. (Rapp, Tr. 9875-77). For instance, in the DRAM industry the specific investments of constructing a DRAM fab are irrelevant to the issue of hold up because a DRAM facility can easily be reconfigured to produce a new type of DRAM. (Rapp, Tr. 9877-78).

2661. A specific investment or a specific asset is one that has low or no value unless another party participates or does something. That is, it requires another party to behave in a certain way. (McAfee, Tr. 7259).

Rambus's Response to Finding No. 2661:

The proposed finding is misleading. (*See* RRFF 2660).

2662. Once a specific investment is made, the economic actor that made the investment is locked into that investment if it is more economical to continue to use the investment or the asset than to switch to an alternative. For example, a power plant operator can become locked in to investments that are required to locate its power plant near a particular coal mine. (McAfee, Tr. 7260- 67; *see* DX0149-154).

Rambus's Response to Finding No. 2662:

The proposed finding is misleading. Lock-in and hold up have to do with switching costs, not specific investments. Suppose that the coal power plant in the example cost the firm a specific investment of $100 million to build. If, in response to an increase in the price by the

mine operator, the only way to avoid the price increase is to shut down the plant and build a new plant in another location for $100 million, the switching costs and the specific investment of $100 million are the same. (Rapp, Tr. 9875-77). If, however, the coal plant can be converted to a gas burning plant for a cost of $5 million, the switching costs are $5 million, not the $100 million to build a new plant. (Rapp, Tr. 9875-77).

2663. Hold-up occurs if the other party changes its prices after the firm becomes locked in by its specific investments. For example, a coal mine operator has an incentive to increase the price of its coal to a power plant operator after the power plant operator has sunk investments by locating its power plant near the coal mine to lower transportation costs. (McAfee, Tr. 7260- 67; *see* DX0149-154).

Rambus's Response to Finding No. 2663:

The proposed finding is misleading. (*See* RRFF 2662).

2664. One way that parties avoid the possibility of being held-up is to contract in advance of making investments that would make them vulnerable to hold-up. This is sometimes called *"ex ante"* contracting. For example, a power plant operator could sign a contract with a coal mine prior to making investments necessary to locate the power plant near the coal mine. (McAfee, Tr. 7267-68; *see* DX-0153-55).

Rambus's Response to Finding No. 2664:

Rambus has no specific response.

2665. The assertion of IP rights on a standard after lock in is a classic case of economic hold-up. After lock in to the standard occurs, it becomes possible for the owner of a patented technology to hold up the industry and expropriate some portion of the specific investments that have been made into the technology. (McAfee, Tr. 7439).

Rambus's Response to Finding No. 2665:

The proposed finding is misleading. Lock-in and hold up depend on switching costs. (*See* RRFF 2660, 2662). Moreover, the evidence shows that in this case the economic conditions for lock-in do not exist. (*See* RPF Section X).

2666. The nature of the expropriation is the charging of royalties that exceed the *ex ante* value of the technology, and instead, are conditioned on the specific investments that have been made in reliance on the standard. (McAfee, Tr. 7307).

Rambus's Response to Finding No. 2666:

The proposed finding is misleading. Lock-in and hold up depend on switching costs. (*See* RRFF 2660, 2662). Moreover, the evidence shows that in this case the economic conditions for lock-in do not exist. (*See* RPF Section X).

2667. The risk of hold-up in standard-setting depends on the size of the specific investments made with respect to a particular standard, the cost of changing the standard, and the importance of intellectual property in the industry. (McAfee, Tr. 7270; *see* DX0157).

Rambus's Response to Finding No. 2667:

The proposed finding is misleading. Lock-in and hold up depend on switching costs. (*See* RRFF 2660, 2663). Moreover, the evidence shows that in this case the economic conditions for lock-in do not exist. (*See* RPF Section X). Further, the evidence shows that the *ex ante* value of Rambus's technologies exceeds Rambus's royalties. (*See* RPF IX.B.3.d, IX.B.4.d).

2668. Specific investments include those investments made by firms to make components that are compatible with the standard. (McAfee, Tr. 7296-97; *see* DX0164).

Rambus's Response to Finding No. 2668:

The proposed finding is misleading. Lock-in and hold up depend on switching costs. (*See* RRFF 2660, 2663). Moreover, the evidence shows that in this case the economic conditions for lock-in do not exist. (*See* RPF Section X).

2669. Firms, in the standard setting context, when hold-up is made possible by the existence of IP, contract for IP in advance of the standard being set. This is a type of *ex ante* contracting. (McAfee, Tr. 7272-73; *see* DX0158).

Rambus's Response to Finding No. 2669:

The proposed finding is not supported by the evidence. The proposed finding cites only to the testimony of Complaint Counsel's economic expert for its percipient facts. The evidence shows that members of the DRAM industry did *not* contract for IP in advance of the standard being set. (*See* RRFF 1204-18).

2670. One method of *ex ante* contracting to avoid hold-up in the standard setting context is a requirement for firms to disclose their IP. (McAfee, Tr. 7273). The disclosure of IP might help the standard-setting organization avoid hold-up by ensuring that if IP was included in the standard, it was done in a conscious and deliberate manner. (McAfee, Tr. 7273).

Rambus's Response to Finding No. 2670:

The proposed finding is misleading to the extent that it implies that JEDEC used this method. The evidence shows that JEDEC's rules encouraged but did not require disclosure of intellectual property that covered a proposed standard. (*See* RPF Section IV.D). Moreover, the evidence shows that when patents were disclosed with respect to a given technology, JC 42.3 often proceeded to adopt the technology with or without receiving a RAND letter. (*See* RPF 1220-38). Further, disclosure of IP does not necessarily lead to *ex ante* contracting. In fact, the evidence shows that JEDEC members did not engage in such contracting when IP was disclosed. (*See* RRFF 1204-18).

2671. Another method of *ex ante* contracting to avoid hold-up in the standard setting context is a requirement for firms to make some sort of licensing commitment regarding their IP prior to the inclusion of the implicated technologies in the standard. (McAfee, Tr. 7273-74).

Rambus's Response to Finding No. 2671:

The proposed finding is misleading to the extent that it implies that JEDEC used this method with any consistency. The evidence shows that the 42.3 committee often adopted

technologies into its standards without receiving a RAND assurance, after intellectual property concerns were raised. (*See* RPF 1220-38).

2672. There is more than one type of potential licensing commitment that can be used by standard setting organizations to mitigate the risk of hold-up. (McAfee, Tr. 7274).

Rambus's Response to Finding No. 2672:

Rambus has no disagreement with this proposed finding and only points out that there is no evidence to show that JEDEC's particular rules or processes are economically efficient or further the antitrust laws. (*See* RPF 1487-99).

2673. One type of licensing is a commitment for a free license. Another type of licensing commitment is for a RAND or "reasonable and nondiscriminatory" license. (McAfee, Tr. 7274). A requirement of a RAND letter will not eliminate the risk of hold-up, but it mitigates or reduces that risk. (McAfee, Tr. 7274).

Rambus's Response to Finding No. 2673:

The proposed finding is misleading to the extent that it implies that JEDEC always required a RAND letter before standardizing a technology when there was a patent issue raised. In fact, the 42.3 committee often adopted technologies into its standards, without receiving a RAND assurance, after intellectual property concerns were raised. (*See* RPF 1220-38).

2674. Dr. Rapp agrees that standard-setting can create market power by making otherwise close substitutes inferior and thereby increasing the royalty rate (price) a technology can command. (Rapp, Tr. 9972).

Rambus's Response to Finding No. 2674:

The proposed finding is misleading because it leaves out the conditions that, Dr. Rapp testified, must exist for standard setting to create market power, which are: (1) high compatibility requirements; (2) the standard setting body is faced with several technologies that are more or less equivalent in cost performance terms; and (3) standard setting elevates one

technology above the others. (Rapp, Tr. 9799-800).

2675. In settings where compatibility requirements are high, the choice of a standard may virtually eliminate, not merely disadvantage, competing technologies. (Rapp, Tr. 9966-67).

Rambus's Response to Finding No. 2675:

The proposed finding is misleading and incomplete. The presence of high compatibility requirements must be combined with the existence of more or less equivalent technologies. (Rapp, Tr. 9966 ("Q. And in those circumstances, in the circumstances that you're referring to here where compatibility requirements are high, you regard that proposition to be a valid proposition from the standpoint of economics? A. Right. Where compatibility requirements are high and we have . . . competing technologies that are more or less equivalent.") Moreover, only a certain type of compatibility requirement ("systems compatibility" not "parts compatibility") could, if combined with the other conditions, lead to this outcome. (Rapp, Tr. 9792).

2676. Formal standard setting creates market power whenever the standard-setting body is faced with several more or less equivalent technologies in terms of cost and performance, and the standard-setting body incorporates one of those technologies into a standard. (Rapp, Tr. 9799). The technologies that are not chosen become inferior alternatives. (Rapp, Tr. 9800).

Rambus's Response to Finding No. 2676:

The proposed finding is misleading and incomplete. Standard setting only creates market power when all three of the following conditions are met: (1) high compatibility requirements; (2) the standard setting body is faced with several technologies that are more or less equivalent in cost performance terms; and (3) standard setting elevates one technology above the others. (Rapp, Tr. 9799-800).

2677. In the context of formal standard setting, the "price of the chosen technology can

change after the standard is determined if the technology owner attempts to extract the value added by the standardization process in royalty fees for the standard technology." (Rapp, Tr. 9973-74).

Rambus's Response to Finding No. 2677:

The proposed finding is misleading and incomplete. The proposed finding selectively quotes one portion of a paper written by Dr. Rapp. As he testified, formal standard setting can only allow a technology owner to raise the price of its technology if certain conditions are met: (1) high compatibility requirements, (2) the standard setting body is faced with several technologies that are more or less equivalent in cost performance terms, and (3) standard setting elevates one technology above the others. (Rapp, Tr. 9799-800).

2678. "In the absence of knowledge about proprietary IP rights in the technologies under consideration, manufacturers may find themselves the victims of opportunism after the standard has been set. That is, the patent holder may charge a royalty that reflects a premium arising from irreversibility, the cost of revising the standard to save the cost of royalty. A patent holder may charge such a premium when the patent emerges after manufacturers have made sunk investment in the patented feature of the standard without have predetermined the license fee. Avoiding a license entails new investment cost if the old (potentially infringing) investments cannot be modified to evade the patents." (Rapp, Tr. 9975-76).

Rambus's Response to Finding No. 2678:

The proposed finding is misleading. The proposed finding selectively quotes one portion of a paper written by Dr. Rapp that describes a certain situation for which a number of conditions must be met. (Rapp, Tr. 9976 ("Q. And am I right that what you were outlining in here in your testimony before the joint FTC-DOJ hearings was a scenario in which the inclusion of a patented technology in a standard could give rise to opportunistic conduct on the part of the owner of the patented technology? A. Right. *And the circumstance as described elsewhere in the paper* where that results in a profitable outcome for the patent owner is when the technology is elevated

by the standard among its – among equivalent alternatives.") (emphasis added)).

2679. "Once the patented technology is adopted as a standard,... firms may commit to the standard and invest in complementary assets needed to make and produce the newly standardized products.... *Ex post*, the cost of switching to the patented alternative may now be much greater as the industry is 'locked-in' to the patented standard." (Teece, Tr. 10509-10).

Rambus's Response to Finding No. 2679:

The proposed finding is misleading and incomplete; it selectively quotes from a "theoretical discussion" in an article written by Professor Teece. (Teece, Tr. 10510). The same article also states that "Ex post, once a standard has been adopted and a patent reading on the standard has been asserted, the accused infringers clearly have a strong incentive to claim that the SSO would have adopted some alternative nonpatented standard had the SSO only known of the existence of the patent. In our experience, such claims rarely articulate which alternative would have been adopted or demonstrate that the SSO would in fact have adopted a different alternative." (Teece, Tr. 10798).

2680. Once firms have committed to a standard and have made the requisite investment in complementary assets to manufacture and sell the standardized product, switching to an alternative may be much less feasible for three reasons. The first reason relates to the presence of sunk costs. The second reason relates to the need for compatibility, especially backwards compatibility, with the existing installed product base. The third reason is that there is often a significant coordination problem in getting all interested parties to switch to an alternative. Coordinating the necessary changes may make it impracticable to switch away from the patented standard. (Teece, Tr. 10489-92; *see* DX0355).

Rambus's Response to Finding No. 2680:

The proposed finding is misleading and incomplete, for it selectively relies on an article written by Professor Teece. The discussion cited in the proposed finding is preceded in the article by the following text: "Clearly it is a *factual question* as to the extent that the chosen standard was superior to available alternatives on an *ex ante* basis. The issue has to be evaluated

on a standard-by-standard basis." (Teece, Tr. 10489) (emphasis added). This passage also refers to the following footnote: "From an economic standpoint, what is important is not the technological feasibility of various alternatives, nor cost considerations (narrowly construed) but rather the overall attractiveness (on a quality/cost-adjusted basis) of the various alternatives." (Teece, Tr. 10796). Professor Teece also testified that he was referring to switching costs when he used the term "sunk costs" in the article. (Teece, Tr. 10799 ("Q. Can you explain what role sunk costs have in connection with any ex post reasons why switching to alternatives may be more or less feasible? A. Yeah. The key question is the switching costs. I mean, just about every industry has got sunk costs of one kind or another, so the key question is not whether there are sunk costs or not but what the switching costs are.")).

2681. "The asymmetry between the low *ex ante* cost of choosing an alternative proposed standard and the higher *ex post* cost of abandoning an existing standard in favor of a new standard causes concerns about the prospect for 'lock in.'" (Teece, Tr. 10500-501). For purposes of analyzing the issues in this case, *ex post* means the time period after a standard is adopted. (Teece, Tr. 10490).

Rambus's Response to Finding No. 2681:

The proposed finding is misleading in that it selectively quotes from an article written by Professor Teece. Other portions of the article expand on the issues discussed in this portion. (*See* RRFF 2679-80). In addition, the cited testimony regarding the "ex post" period refers to a discussion in Professor Teece's article, not to this case. (Teece, Tr. 10490).

8. Lock in and Hold-up Concerns in the DRAM Industry.

2682. DRAM industry standards are characterized by hold-up. Both the rules of JEDEC and the characteristics of production in the DRAM industry illustrate the lock in and hold-up concerns in the industry. (CCFF 2683-2756).

Rambus's Response to Finding No. 2682:

The proposed finding is not supported by the evidence. (*See* RRFF 2683-756).

2683. If JEDEC has a preference to avoid patents, that can be seen as an expression of an interest on the part of JEDEC to avoid the hold-up problem. (McAfee, Tr. 7277).

Rambus's Response to Finding No. 2683:

The proposed finding is misleading and not supported by the evidence, which shows that JEDEC does not have a preference to avoid patents. (*See* RPF 1220-38).

2684. JEDEC has a strong preference to avoid the presence of patented technologies in the JEDEC standards. (CCFF 301-304).

Rambus's Response to Finding No. 2684:

The proposed finding is not supported by the weight of the evidence, which shows that JEDEC does not have a preference to avoid patents. (*See* RPF 1220-38).

2685. If JEDEC has a preference for early disclosure that would also be an expression of an interest in avoiding hold-up because, as an economic matter, the earlier information is obtained, the better decisions will tend to be. (McAfee, Tr. 7277, 7301-04).

Rambus's Response to Finding No. 2685:

The proposed finding is misleading and incomplete. It is not the case that the earlier that information about potential patent issues is obtained, the better a standard will be. (Teece, Tr. 10385). For instance, the theoretical testimony of Complaint Counsel's economic expert on this issue is directly contrary to comments provided by the Institute of Electrical and Electronics Engineers Standards Association to the FTC in April 2002 that: "If disclosure of issued patents is expected too early in the process – i.e., before the draft standard has reached a level of stability – more patents may be disclosed than those that are essential, since it may be too early to determine exactly those that will be required for implementation. This problem would become

even larger if, as some have suggested, patent applications were to be treated in the same manner as issued patents. A 'one size fits all' solution cannot be applied to disclosure." (RX 2011 at 5).

2686. JEDEC has a strong preference for early disclosure of patents or patent applications in the standardization process. (CCFF 339-345).

Rambus's Response to Finding No. 2686:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 339-45).

2687. In the absence of a search requirement, one way of minimizing the potential for hold-up would be a good faith requirement to provide as much information as a member has access to, and to not try to change the outcome of the process by manipulating it. (McAfee, Tr. 7278).

Rambus's Response to Finding No. 2687:

The proposed finding is not supported and impermissibly relies on the "understanding" of Complaint Counsel's economic expert. (McAfee, Tr. 7278 ("that's my understanding of as to good-faith requirement")). Further, the proposed finding is misleading to the extent it implies that JEDEC had *any* requirement to "provide as much information as the member has access to." (*See* RRFF 300-443).

2688. There is a good faith requirement at JEDEC. (CCFF 310-314).

Rambus's Response to Finding No. 2688:

The proposed finding is not supported to the extent it implies that JEDEC had any requirement to "provide as much information as the member has access to." (*See* RRFF 310-14).

2689. A requirement of a standard setting organization that firms disclose patent applications as well as patents is consistent with an interest in avoiding hold-up. (McAfee, Tr. 7278-79).

Rambus's Response to Finding No. 2689:

The proposed finding is misleading to the extent it implies that JEDEC required the

disclosure of patent applications. (*See* RPF Section IV.F).

2690. JEDEC has a requirement that firms disclose patent applications as well as patents relating to the standard-setting work under discussion. (CCFF 318-320).

Rambus's Response to Finding No. 2690:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 318-20; RPF Section IV.F).

2691. Dr. Rapp agrees that "for [lock in] to be a concern, the proprietary technology must be essential to the standard or else it could simply be omitted.... [a]n attempt by the patent owner to charge opportunistic royalties would result in manufacturers leaving that particular technology out of the final product." (Rapp, Tr. 9980-981; *see* DX0323).

Rambus's Response to Finding No. 2691:

Rambus has no specific response.

2692. Dr. Rapp agrees another condition for opportunism to be a concern would be that the costs of changing the standard or manufacturing process must exceed the royalty demanded for the use of the standard. (Rapp, Tr. 9982; *see* DX0323).

Rambus's Response to Finding No. 2692:

The proposed finding is misleading in that it implies that opportunism is at issue in this case. As Dr. Rapp explained, opportunism is not related to whether there has been an antitrust violation:

> Q. Okay. Let me go back to something you were asked about yesterday, the subject of opportunism. Do you recall that subject?
>
> A. Yes.
>
> Q. In your view, how prevalent or common is opportunism, as you were asked about that subject yesterday?
>
> A. Opportunism is everywhere in the economy, and the reason that

opportunism is everywhere is that nobody is able to -- it's very rare that people are able to specify perfect contracts, and as long as contracts are imperfectly specified, people can take advantage of the fact that they are -- that they're imperfect. So it happens a lot.

Q. Is there a necessary relationship between opportunism and anticompetitive behavior from the perspective of an antitrust economist?

A. No. There is no necessary connection because the world would be filled with antitrust violations if there were.

(Rapp, Tr. 10233-34). Further, the evidence in this case shows that the cost to change the standard does *not* exceed the royalty demanded. (*See* RPF Section X).

2693. Dr. Rapp agrees another condition that he believes must be met or must be satisfied for opportunism to be a concern is that there must be alternatives to the chosen patented technology that could plausibly have been adopted had disclosure taken place. (Rapp, Tr. 9982-983; *see* DX0323).

Rambus's Response to Finding No. 2693:

The proposed finding is misleading in that it implies that opportunism is at issue in this case. (*See* RRFF 2692). The evidence also shows that there were no alternatives in this case. (*See* RPF Section IX).

2694. Dr. Rapp agrees that to determine whether these three propositions apply in a real-world example would require a careful assessment of the relevant facts. (Rapp, Tr. 9984; *see* DX0323).

Rambus's Response to Finding No. 2694:

The proposed finding is misleading in that it implies that opportunism is at issue in this case. (*See* RRFF 2692).

2695. Dr. Rapp reviewed no Rambus business records other than Toshiba license agreement and a license term synopsis prepared by his staff. (Rapp, Tr. 9991; *see* DX0324).

Rambus's Response to Finding No. 2695:

The proposed finding is misleading. Dr. Rapp testified that he reviewed the materials necessary to reach his conclusions in this case:

> Q. And do you believe, Dr. Rapp, that in reaching the conclusions reported in your expert report in this case that you did a sufficient amount of work to ensure that your conclusions were well-founded in facts and evidentiary material?
>
> A. Yes, I absolutely do. And the difference between the volume of materials that I reviewed and the volume of material that Professor McAfee reviewed has to do with the differences in our assignment and with material in Professor McAfee's report that have nothing to do with my assignment or for that matter I think anything in the case.

(Rapp, Tr. 10008-09).

2696. Dr. Rapp reviewed no third-party business records. (Rapp, Tr. 9992; *see* DX0324).

Rambus's Response to Finding No. 2696:

The proposed finding is misleading. (*See* RRFF 2695).

2697. Dr. Rapp reviewed no deposition testimony. (Rapp, Tr. 9993; *see* DX0324).

Rambus's Response to Finding No. 2697:

The proposed finding is misleading. (*See* RRFF 2695).

2698. Dr. Rapp reviewed no JEDEC materials/minutes other than two technical specifications. (Rapp, Tr. 9994; *see* DX0324).

Rambus's Response to Finding No. 2698:

The proposed finding is misleading. (*See* RRFF 2695).

2699. Dr. Rapp reviewed no notes/reports on JEDEC activities. (Rapp, Tr. 9995; *see* DX0324).

Rambus's Response to Finding No. 2699:

The proposed finding is misleading. (*See* RRFF 2695).

2700. Dr. Rapp reviewed none of the Rambus / JEDEC / third-party records cited in McAfee's report. (Rapp, Tr. 9999; *see* DX0324).

Rambus's Response to Finding No. 2700:

The proposed finding is misleading. (*See* RRFF 2695).

2701. Dr. Rapp agrees that "[t]he reliability of any example of economic reasoning depends, in part, on the quality of its underlying assumptions. All assumptions are not equal. Reasoning which rests on baseless assumptions is less reliable than reasoning based on assumptions that are well-founded in facts and evidentiary materials." (Rapp, Tr. 10004 ("Not only do I agree with it, I think they are words to live by."); *see* DX0325).

Rambus's Response to Finding No. 2701:

Rambus has no specific response.

2702. Dr. Rapp agrees that it is important for an economist to try to ensure that his or her assumptions and conclusions are well-founded in evidentiary materials. (Rapp, Tr. 10007 ("And may I just add that that refers to the connection between the foundations for assumptions and the specific subject matter that the economist is addressing, not the universe of subject matter.")).

Rambus's Response to Finding No. 2702:

Rambus has no specific response.

2703. Hold-up may be a concern in the DRAM industry if the following circumstances are true: The amount of specific investments into the standard are substantial, the costs of changing standards is high, IP is important in the industry, and it is difficult to reach agreements to change the standard once set. (McAfee, Tr. 7407; *see* DX-0160).

Rambus's Response to Finding No. 2703:

The proposed finding is unclear and ambiguous. First, specific investments do not bear on the issue of hold-up. (*See* RRFF 2660). Second, the finding does not define what are "high" switching costs. Third, the phrases "IP is important" and "difficult to reach agreement" are ambiguous.

2704. The ease of reaching agreement reflects on how difficult it would be to avoid hold-up by changing the standard and can be seen as a cost of changing the standard. (McAfee, Tr. 7411).

Rambus's Response to Finding No. 2704:

Rambus has no specific response.

2705. Based on the evaluation of those factors, hold-up is a problem that arises in the context of the DRAM industry. (McAfee, Tr. 7288; CCFF 2710-756).

Rambus's Response to Finding No. 2705:

The proposed finding is not supported. (*See* RRFF 2710-56).

2706. There is substantial potential for lock in in the DRAM industry, and, as a result, there is potential for the creation of monopoly power by incorporating technologies into DRAM standards. (McAfee, Tr. 11304; CCFF 2710-756).

Rambus's Response to Finding No. 2706:

The proposed finding is not supported. (*See* RRFF 2710-56).

2707. Lock in is a major feature in the DRAM industry, and, as a consequence, the bargaining power of a licensor of proprietary technology that is in the standard grows over time and it becomes ever more difficult for the industry to get out from under patented technology. (McAfee, Tr. 11370).

Rambus's Response to Finding No. 2707:

The proposed finding is not supported by the weight of the evidence. The DRAM industry is not marked by the potential for lock-in. (*See* RPF Section X). The DRAM industry

produces and supports multiple DRAM standards with significant market shares. (*See* RRFF 2601). The DRAM industry is also constantly and routinely switching to new DRAM standards. For instance, AMD migrated its K7 systems through five different types of DRAM in less than four years. (*See* RPF 1311-20). Similarly, Compaq migrated its systems through six types of DRAM in less than seven years. (*See* RPF 1322-28). These conditions show that lock-in is not an issue in the DRAM industry. (*See* RPF Section X.B).

2708. Incorporation of a technology in JEDEC standards is highly likely to lead to dominance of that technology in the marketplace. (McAfee, Tr. 11224).

Rambus's Response to Finding No. 2708:

The proposed finding is not supported by the evidence. Complaint Counsel's economic expert admitted on cross-examination that many technologies standardized by JEDEC fail in the marketplace: "I would agree that there are technologies that were standardized [by JEDEC] that were not adopted by the marketplace, DRAM technologies that were standardized that were not adopted by the marketplace." (McAfee, Tr. 11343). The evidence shows that standardization by JEDEC is neither necessary nor sufficient for success. For example, the design for the latest generation of Video RAM was rejected by JEDEC, yet the standard succeeded in the market. (Prince, Tr. 9021-22). Burst EDO, on the other hand, was standardized by JEDEC but failed in the market. (Williams, Tr. 873). Further, to the extent that JEDEC standardization can be correlated with success in the market place, any conclusion of causation must take into account the evidence that JECEC has been captured by a small group of DRAM manufacturers and the evidence that these same DRAM manufacturers colluded to defeat competing standards. (RPF 1548-1601). (*See* RRFF 206, 244).

2709. The deployment of resources that locks in an industry to a particular standard increases the value of the technology that is incorporated in the standard. (McAfee, Tr. 7438).

Rambus's Response to Finding No. 2709:

The proposed finding is misleading and incomplete. The value of a technology is only enhanced by standardization if certain conditions exist, which are not listed in the proposed finding. (*See* RRFF 2674; Rapp, Tr. 9799-800). Further, the concept of lock-in is related to switching costs, not specific investments. (*See* RRFF 2660).

(A) Specific Investments Are Substantial.

2710. Hold-up in the context of DRAM standardization occurs when the industry learns that the technology that it chose to incorporate into a standard is subject to a patent, and the industry learns this fact after it has already made substantial specific investments into the standard. (McAfee, Tr. 7305-06).

Rambus's Response to Finding No. 2710:

The proposed finding is misleading and incomplete. The value of a technology is only enhanced by standardization if certain conditions exist, which are not listed in the proposed finding. (*See* RRFF 2674; Rapp, Tr. 9799-800). Further, the concept of lock-in is related to switching costs, not specific investments. (*See* RRFF 2660). The evidence also shows that the DRAM industry is not subject to lock-in. (*See* RPF Section X).

2711. Those specific investments may take the form of investments in plant and equipment, complementary goods, and other investments that are specific to the technology. (McAfee, Tr. 7306).

Rambus's Response to Finding No. 2711:

The proposed finding is misleading and incomplete. The concept of lock-in is related to switching costs, not specific investments. (*See* RRFF 2660). Specific investments may often be used with an alternative technology; in that case, those investments are not switching costs and

would not contribute to lock-in. (*See* RRFF 2660).

2712. A substantial amount of investment in the DRAM industry is specific to the DRAM technology and so is specific to the standard that is at issue. (McAfee, Tr. 7407; CCFF 2501-2526, 2528-2540).

Rambus's Response to Finding No. 2712:

The proposed finding is misleading and incomplete. (*See* RRFF 2711).

2713. In the DRAM context, once a standard is issued and adopted over time, there is an increasing level of investment in the standard by manufacturers producing to the standard, including investment by manufacturers of complementary components such as modules, graphic cards, and chip sets. (McAfee, Tr. 7436; *see* DX0221; CCFF 2550-2562).

Rambus's Response to Finding No. 2713:

The proposed finding is misleading and incomplete to the extent that it implies that "investment in the standard" is necessarily related to the issues of switching costs, hold-up, or market power. (*See* RRFF 2711).

2714. Such investments by DRAM manufacturers and by manufacturers of complementary components contributes to lock in. (McAfee, Tr. 7437).

Rambus's Response to Finding No. 2714:

The proposed finding is misleading and incomplete because it implies that generic investments "in the standard," rather than switching costs, are related to the issue of lock-in. (*See* RRFF 2711).

2715. As specific investments in a standard are made, the industry becomes progressively more locked into the standard. (McAfee, Tr. 7435). The switching costs grow over time, and there comes a point when the technology incorporated into the standard obtains monopoly power because the alternatives are no longer commercially viable. (McAfee, Tr. 7435). This phenomenon has occurred in the DRAM industry. (McAfee, Tr. 7435).

Rambus's Response to Finding No. 2715:

The proposed finding is misleading and not supported. First, the proposed finding

incorrectly equates specific investments with switching costs; the two are not the same. (*See* RRFF 2660, 2711). Second, the proposed finding assumes that there were *ex ante* acceptable, noninfringing alternatives; the evidence shows that there were none. (*See* RPF Section IX.B). Third, standardization only contributes to market power if certain conditions are met, which are not included in the proposed finding. (*See* RRFF 2674; Rapp, Tr. 9799-800). Fourth, the evidence shows that the DRAM industry is not locked-in. (*See* RPF Section X).

2716. Industry-wide coordination and resource commitment is part of the specific investment in the DRAM standards that makes the industry locked in to a DRAM standard over time. (McAfee, Tr. 7436-37; *see* DX0221; CCFF 2547-2562).

Rambus's Response to Finding No. 2716:

The proposed finding is misleading and not supported. (*See* RRFF 2715).

2717. Because of the scope and the size of the investments into a standard, there is a relatively large amount of lock in in the DRAM industry to a standard that has been deployed in volume. By the time that DRAM ramp-up occurs, lock in has been accomplished, particularly because of the specific investments made in goods that are complementary to the standard. (McAfee, Tr. 7444-45 ("Because in order to deploy the standardized product in volume, it requires those complementary goods. Things like chipsets and the like are also being produced.")).

Rambus's Response to Finding No. 2717:

The proposed finding is misleading and not supported. (*See* RRFF 2715).

2718. If compatibility requirements are high, there will typically be a dominant product standard. (McAfee, Tr. 11218).

Rambus's Response to Finding No. 2718:

The proposed finding is contrary to the evidence if it refers to "compatibility requirements" between parts (e.g., copiers and toner cartridges) versus compatibility between systems (e.g., a fax machine communicating with another fax machine). If systems compatibility

requirements are high, there will typically be a dominant product standard. (Rapp, Tr. 9792-93). If only parts compatibility requirements are high, then there need not be a single standard. (Rapp, Tr. 9791). In the DRAM industry, which requires only parts compatibility, multiple standards with significant market shares can and do coexist. (*See* RRFF 2601).

2719. Compatibility requirements refers to the requirement that a product be compatible with other products that work with them. (McAfee, Tr. 11210-11).

Rambus's Response to Finding No. 2719:

The proposed finding is misleading in that it does not distinguish between parts compatibility and systems compatibility. (*See* RRFF 2718).

2720. In qualitative terms, compatibility requirements are high in the DRAM industry. (McAfee, Tr. 11211; CCFF 25-28, 2550-562).

Rambus's Response to Finding No. 2720:

The proposed finding is not supported by the weight of the evidence. While compatibility between parts may be high for DRAM products (e.g., compatibility between a DRAM and a chip set), systems compatibility requirements are not high (e.g., a computer with one type of DRAM can communicate with a computer that has a different type of DRAM). (Rapp, Tr. 9793-94). Thus, compatibility requirements are not high in the DRAM industry. (*Id.*) This is evidenced by the fact that multiple DRAM standards with significant market shares coexist at any given time and that DRAM manufacturers produce multiple DRAM types at any given time. (*See* RPF Section X.A; RRFF 2601).

2721. Parts compatibility refers to a requirement that parts inside a system work with other parts. (McAfee, Tr. 11211). Parts compatibility plus a significant range of complementary products leads to high compatibility requirements. (McAfee, Tr. 11212).

Rambus's Response to Finding No. 2721:

The proposed finding is misleading and not supported. Parts compatibility does not lead to high compatibility requirements in the DRAM industry. Complaint Counsel's economic expert stated that the "classic case" of this phenomenon was the example of VHS versus Beta home video recorders. (McAfee, Tr. 11212). He testified that "the understanding of economists of this incident . . . is the edge VHS got caused more – caused Blockbuster and other video rental outlets to have more tapes for rent," which lead to the dominance of VHS. (McAfee, Tr. 11213). The analogy is inapt because the value of a VHS machine depends on how many different tapes can be played on it. The VHS machine, in other words, needs lot of tapes to play to be valuable; that is a type of system compatibility. A DRAM, by contrast, needs to work with only the computer in which it is installed. That is only parts compatibility.

Moreover, the evidence shows that performance, not complementary products, drives DRAM standards. Even with the VHS example, performance may have been a factor. On cross-examination, Professor McAfee admitted that VHS had different features than did Betamax and that "there's a lot of dispute about the feature aspect of this. The VHS – whether features even mattered." (McAfee, Tr. 11346). Further, he admitted that each new DRAM standard had performance advantages over the previous type of DRAM. (McAfee, Tr. 11347). He went on to admit that these performance advantages were significant in driving the changes to the new standard. (McAfee, Tr. 11347 ("Q. And the fact that each of the products as you understand them or that you have assumed them to exist provide a higher level of performance is of significance in deciding which one will become dominant, is it not? A. It is.").

2722. High compatibility requirements have the effect of creating significant lock in to

the existing standards or existing technologies. (McAfee, Tr. 11211) .

Rambus's Response to Finding No. 2722:

The proposed finding is unsupported and misleading. (*See* RRFF 2720-21).

2723. In the DRAM industry, high compatibility requirements have led to lock in and resulting monopoly power in the technologies incorporated into DRAM standards. (McAfee, Tr. 11211).

Rambus's Response to Finding No. 2723:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 2720-21).

2724. If the cost of modifying compatible complementary products is substantial so that when the standard is changed, costs would have to be incurred by makers of complementary products to match the new, then significant network effects are present. (McAfee, Tr. 11216).

Rambus's Response to Finding No. 2724:

The proposed finding is contrary to the definition of network effects given by Complaint Counsel's own economic expert, who defined a network effect as "a situation where increased use of a product either lowers its cost or enhances its value." (McAfee, Tr. 7610; *see also* McAfee, Tr. 11213 (addition of complementary products "gave more value to consumers" of the standard product). The cost of modifying a complementary product does not give more value to consumers of a particular type of DRAM and has nothing to do with increased use.

2725. The long lead times for a number of products means that many manufacturers need to know what the standard will be years in advance. For example, the costs to the manufacturers of chipsets can be high if the DRAM standard is changed late in the process. Workstation and server manufacturers also need to know what the DRAM design will be years prior to shipping their product. (CCFF 115).

Rambus's Response to Finding No. 2725:

The proposed finding is not supported. (*See* RRFF 115).

2726. Coordination costs alone may completely block the switching to a new standard, irrespective of the financial switching costs. (McAfee, Tr. 11300; CCFF 2564-568).

Rambus's Response to Finding No. 2726:

The proposed finding is not supported by the weight of the evidence. First, none of the cited factual evidence supports the proposed finding; that evidence only bears on how long it purportedly takes for the DRAM industry to develop a completely new standard. (*See* RRFF 2564-568). Second, the cited testimony of Complaint Counsel's expert is not supported because there is no example or evidence showing that coordination difficulties have ever completely blocked a standard. Weighing against such a conclusion is the evidence that the DRAM industry routinely and rapidly coordinates changes in DRAM standards. (*See* RPF Section X.A.4 & X.B.2).

2727. DRAM manufacturers will not switch without their customers' simultaneously willing to purchase, and the customers will not be willing to purchase unless the complementary component suppliers are also providing compatible components. (McAfee, Tr. 11301; CCFF 2547-2562).

Rambus's Response to Finding No. 2727:

Rambus has no specific response.

2728. Because DRAM manufacturers will not switch without their customers' simultaneously willing to purchase, and the customers will not be willing to purchase unless the complementary component suppliers are also providing compatible components, it is incumbent to have an industry consensus in order for the industry to switch to an alternative standard, *i.e.*, significant coordination must take place. (McAfee, Tr. 11301).

Rambus's Response to Finding No. 2728:

Rambus has no specific response.

2729. Such coordination is costly and includes costs that goes beyond the direct financial costs of implementing a new standard. (McAfee, Tr. 11303; CCFF 2564-568).

Rambus's Response to Finding No. 2729:

The proposed finding is incomplete and misleading. The evidence shows that the DRAM industry routinely coordinates changes in DRAM standards. (*See* RPF Section X.A.4 & X.B.2).

2730. Even if the actual direct financial switching costs are minimal, it may still be difficult or impossible for the DRAM industry to switch from an existing product standard to an alternative product standard. (McAfee, Tr. 11300).

Rambus's Response to Finding No. 2730:

The proposed finding is not supported by the evidence. There is no evidence that coordination issues have ever prevented the DRAM industry from switching to a new standard; rather, the evidence shows that the DRAM industry routinely overcomes coordination issues. (*See* RPF Section X.A.4 & X.B.2).

2731. From the standpoint of assessing lock in in this case, it is necessary to account for the aggregate switching costs of DRAM manufacturers. (Rapp, Tr. 10124). In addition, to switch successfully to an alternative DRAM technology, manufacturers of other complementary products would also have to make costly changes. (Rapp, Tr. 10124-25). Therefore, for the DRAM industry as a whole to work around Rambus's patents, coordination among DRAM manufacturers and manufacturers of other products such as makers of microprocessors and chipsets would have to take place. (Rapp, Tr. 10125).

Rambus's Response to Finding No. 2731:

The proposed finding is misleading and unsupported to the extent that it characterizes the changes needed to be made by manufacturers of complementary products as "costly." The cited evidence does not support that characterization.

2732. Depending on the alternative technology chosen, makers of hard drive storage, sockets, modems, memory modules, graphics cards, graphics subsystems, and CDROM/DVD drives might have to change their products to accommodate a new DRAM standard. (Rapp, Tr. 10141-42).

Rambus's Response to Finding No. 2732:

The proposed finding is not supported. The only cited evidence is the testimony of Dr. Rapp, who testified only to his understanding of the underlying facts.

2733. The aggregate costs to non-DRAM makers of working around Rambus's patents could actually be higher than the aggregate costs to DRAM makers. (Rapp, Tr. 10136).

Rambus's Response to Finding No. 2733:

The proposed finding is misleading and incomplete. While it is theoretically possible, the evidence weighs against a finding that the aggregate costs of non-DRAM manufacturers exceed the switching costs of manufacturers. The evidence shows that non-DRAM manufacturers often and routinely switch to new DRAM standards. (*See* RPF Section X). The implication of this is that the magnitude of their switching costs is on the same order or less than those of DRAM manufacturers. (Rapp, Tr. 10128).

2734. In order to avoid Rambus's patents, the DRAM manufacturers would have to make changes to each of the densities of SDRAM or DDR that they had in production. (Rapp, Tr. 10144).

Rambus's Response to Finding No. 2734:

The proposed finding is misleading. The evidence shows that DRAM manufacturers routinely phase out their products. (Shirley, Tr. 4282 (*in camera*); Becker, Tr. 1168).

(B) Costs of Changing Standards Are High.

2735. It is difficult and time consuming for the DRAM industry to reach agreements over changing the DRAM standards. (McAfee, Tr. 7410-11; 2564-568; 2576-584).

Rambus's Response to Finding No. 2735:

The proposed finding is misleading and not supported by the evidence. The evidence shows that the DRAM industry is able to reach agreement and complete transitions from one

standard to another with great frequency. Within seven years, for example, Compaq shifted from EDO DRAM to PC66 to PC100 to PC133 to DDR266 to DDR333. (*See* RPF 1322-28). Similarly, between June 1999 and May 2003, systems using AMD's K7 switched from using PC100 to PC133 to DDR200 and 266 to DDR333 to DDR400. (*See* RPF 1311-20). Each of these transitions required the development of new DRAM specification and the coordination, design, and production of new complementary products. (*See* RPF 1311-28). These efforts were often done outside of JEDEC and in a timely manner. The proposed finding ignores, for example, Intel's role in setting standards for the industry; for instance, Intel set the standard for PC100 (which standard defined "a new Synchronous DRAM specification") without obtaining agreement from others. (MacWilliams, Tr. 4907-09; RX 2103-14 at 9). Likewise, the proposed finding ignores that the PC133 standard was developed by PC OEMs and DRAM manufacturers, outside of JEDEC. (MacWilliams, Tr. 4912-13). The facts are critical because alternatives to Rambus's technologies, if they existed, could have been incorporated during these natural transitions. (Geilhufe, Tr. 9675).

2736. Because it is difficult and time consuming for the DRAM industry to reach agreements over changing the DRAM standards there is a high risk of hold-up from patents on DRAM standards. (McAfee, Tr. 7411).

Rambus's Response to Finding No. 2736:

The proposed finding is contrary to the weight of the evidence. The DRAM industry routinely coordinates changes in DRAM standards. (*See* RPF Section X.A.4). New standards are produced and implemented almost once a year. (*Id.*) Many of these changes are accomplished outside of JEDEC, by Intel or by PC OEMs and their suppliers. (MacWilliams, Tr. 4907-09; RX 2103-14 at 9). This shows that the DRAM industry is not subject to hold up.

(*See* RPF Section X.B).

2737. There is a substantial volume of switching costs in the DRAM industry, where switching costs refers to the costs of changing stan-dards. (McAfee, Tr. 7408-409; CCFF 2576-584).

Rambus's Response to Finding No. 2737:

The proposed finding is not supported and is misleading in that it characterizes switching costs as a "substantial volume." Complaint Counsel's economic expert admitted on cross-examination that he did not quantify switching costs. (McAfee, Tr. 7716-17, 11356). The cross-referenced proposed findings say nothing about a "substantial volume." (*See* CCFF 2576-84). The evidence also shows that switching costs do not prevent the DRAM industry from routinely moving to new DRAM standards. (*See* RPF Section X).

2738. The costs of changing the standards today to avoid the Rambus patents includes the cost to: (1) develop new technology standards (McAfee, Tr. 7440); (2) reach consensus after the first standard had been adopted (McAfee, Tr. 7447-52; *see* DX0225); and (3) design, test, and qualify DRAM components and the necessary complements to those DRAM components. (McAfee, Tr. 7453-54). Additional switching costs are the opportunity costs of using resources to change the standard and the cost that delaying the standard can have on the industry. (*See* DX-0223; ***CCFF*** 2537).

Rambus's Response to Finding No. 2738:

The proposed finding is incomplete. While Complaint Counsel's economic expert testified that avoiding Rambus's patents would require the same categories of switching costs as other tranitions in the DRAM industry, he also admitted that those costs would be less than for transitions that did in fact occur. (McAfee, Tr. 7714-18).

2739. From an economic perspective, coordination problems are rightly considered to be an element of overall switching costs. (Teece, Tr. 10828-29)

Rambus's Response to Finding No. 2739:

Rambus has no specific response.

2740. Time is a relevant factor in considering lock in. (Rapp, Tr. 10147).

Rambus's Response to Finding No. 2740:

The proposed finding is incomplete; Dr. Rapp testified, "time isn't a cost, but time is a relevant consideration." (Rapp, Tr. 10147).

2741. One of the most important switching costs in the DRAM industry is the cost of delay in the standard to the DRAM industry. (McAfee, Tr. 7440-41; CCFF 123-124)

Rambus's Response to Finding No. 2741:

The proposed finding is not supported, for it cites the testimony of Complaint Counsel's economic expert for percipient facts. The other cited evidence says nothing about costs. There is no evidence that standards are delayed or that any costs are incurred due to any delay.

2742. Recent standards have taken at least two years to develop and at least another three years before full volume production. (CCFF 2565-568); McAfee, Tr. 7441-42; *see* DX0224). Because the changes that take place between generations of DRAM standards are minimized by JEDEC's need for evolutionary change, that experience is at least suggestive of the amount of time it would take to develop and deploy standards that would avoid Rambus's patents. (McAfee, Tr. 7441-42; *see* DX224; CCFF 127-128, 2569-573).

Rambus's Response to Finding No. 2742:

The proposed finding is misleading, incomplete, and not supported by the weight of the evidence. First, the proposed finding relies on evidence concerning the development of the SDRAM and DDR standards, without any reference to the various subgenerations of those standards. Within the SDRAM standard there is PC66, PC100, and PC133. (*See* RPF 1323-25). Compaq, for example, switched from PC66 to PC100 to PC133 within the period of 1997 to 1999. (*See* RPF 1323-25). Within the DDR standard, there is DDR200, DDR266, DDR333, and

DDR400. (*See* RPF 1313-19). These shifts required the development of new complementary components, such as chip sets and motherboards. (*See, e.g.*, Polzin, Tr. 3998-4005). These standards were quickly developed and adopted. (*See* RPF 1266-77).

Further, the proposed finding is not supported because the only evidence that the cited generational changes are "suggestive" of the time needed to switch away from using Rambus's technologies is the uncorroborated understanding of Complaint Counsel's economic expert. In contrast, Rambus's technical experts testified that, if acceptable alternatives were in fact available, they could have been implemented during a regular DRAM product redesign, which occurs on the order of every 6 to 12 months. (Soderman, Tr. 9418; Geilhufe, Tr. 9615).

2743. It is important to consider the time it would take to ramp up production of the new technology as well as the time it takes to develop the standards because firms cannot avoid paying the royalty to Rambus until they are actually producing the new DRAM that does not infringe the patents in volume. (McAfee, Tr. 7443-44; 7446).

Rambus's Response to Finding No. 2743:

The proposed finding is too ambiguous to permit a response.

2744. It should be more difficult to reach a consensus to change the standard now than it was to reach consensus on the original standard because the interests of the members of JEDEC are not as well aligned now as they were *ex ante.* (McAfee, Tr. 7447-48; CCFF 2745-750).

Rambus's Response to Finding No. 2744:

The proposed finding is not supported. (*See* RRFF 2745-50).

2745. One reason the interests of the JEDEC members are not as well aligned now is because some members of JEDEC have licenses from Rambus and others do not. (CCFF 1999, 2004-11, 2014; McAfee, Tr. 7448).

Rambus's Response to Finding No. 2745:

The proposed finding is not supported. Though Complaint Counsel's economic expert

testified that the fact that some JEDEC members are licensed while others are not might in theory create difficulties, he admitted on cross-examination that he had not reached a conclusion as to whether the interests of the two groups of JEDEC members are, in fact, aligned to avoid Rambus's patents. (McAfee, Tr. 7723). The economic evidence, moreover, is that if there were acceptable alternatives, the interests of the two groups would be aligned because all have an interest in using the best alternative in cost-performance terms. (Rapp, Tr. 9801-02).

2746. Because some JEDEC members have licenses from Rambus they have an incentive to maintain the current standard rather than changing it. (McAfee, Tr. 7449-50; CCFF 1999, 2004-11, 2014).

Rambus's Response to Finding No. 2746:

The proposed finding is not supported. (*See* RRFF 2745).

2747. A second reason the interests of the JEDEC members are not as well aligned now as they were *ex ante,* is that firms have made different types of investments based on the standards that may make them have a different willingness to agree to particular changes. (McAfee, Tr. 7450-51).

Rambus's Response to Finding No. 2747:

The proposed finding is misleading and unsupported. While theoretically possible, there is no evidence of any difference in willingness to change due to investments.

2748. One example of the effect of differing investments on the willingness of firms to adopt a particular technology is the willingness of AMD to adopt a DRAM standard with a fixed burst length of four. (McAfee, Tr. 7451; CCFF 2580-581).

Rambus's Response to Finding No. 2748:

The proposed finding is misleading, incomplete, and contrary to the evidence to the extent that it implies that differences in the burst length utilized by microprocessor companies would create disagreement regarding alternatives. AMD and Intel account for 99% of the

microprocessor market. (Heye, Tr. 3642-43). Although Intel uses a burst length of four in its memory systems, AMD elected to use a burst length of eight because doing so increases system performance with the AMD architecture. (Polzin, Tr. 3994). The use of programmable burst length in SDRAM and DDR therefore allowed systems designers to optimize their particular microprocessor architectures for increased system performance. According to Complaint Counsel's theory, the fact that AMD and Intel used different burst lengths would mean that their incentives would be different with regard to alternatives for that technology. The record evidence undermines that notion. When the preliminary specification for DDR2 specified a single burst length of four (the one used by Intel), Intel nevertheless insisted that the DDR2 specification be changed to include a programmable burst length so that a burst length of 8 could be used. (RX 1854 at 20 (preliminary specification); CX 174 at 7-8, 37 (Intel proposal to change the specification to allow for burst length of 8)). According to Intel's presentation, the use of programmable burst length would allow Intel (and therefore AMD) to optimize performance depending on the application. (CX 174 at 37 ("Potential improvement of 4-10% on high-bandwidth applications")). The proposed finding therefore does not support the notion that there were divergent interests that would have prevented the use of acceptable alternatives, if they existed.

2749. Had the industry adopted a fixed burst length of four for the original SDRAM standard, then AMD would have used that burst length. However, since the standard allowed the use of burst lengths of eight, the company optimized their processors to work with a burst length of eight and would now be harmed by a move to a burst length of four. (McAfee, Tr. 7451; CCFF 2580-581).

Rambus's Response to Finding No. 2749:

The proposed finding is misleading to the extent that it implies any coordination issues

with respect to burst length. (*See* RRFF 2748). Further, had JEDEC adopted a single fixed burst length, microprocessor systems would have suffered performance degradation. (Polzin, Tr. 3994 (fixed burst length would have "caused us a performance hit"); CX 174 at 37 (Intel presentation insisting on programmable burst length in DDR2 to allow for increased performance in high-bandwidth applications)).

2750. The investments that AMD made to exploit a burst length of 8 are specific investments in the programmable burst length features of SDRAM and DDR SDRAM. (McAfee, Tr. 7451-52).

Rambus's Response to Finding No. 2750:

The proposed finding is misleading to the extent that it implies any coordination issues with respect to burst length. (*See* RRFF 2748)

2751. Opportunity costs refers to the opportunities that have been forgone because of an activity. (McAfee, Tr. 7455). The opportunity costs of creating a new standard to avoid the Rambus IP is the fact that the engineering talent, the resources, the testing facilities and all of the resources used are not available to other projects. (CCFF 2537; McAfee, Tr. 7456).

Rambus's Response to Finding No. 2751:

The proposed finding is incomplete. The opportunity costs of designing around Rambus's patents are best measured by the wages of the engineers required. (Rapp, Tr. 10156). Dr. Rapp included those costs in his calculations of switching costs. (Rapp, Tr. 10156).

2752. In the DRAM industry, the opportunity costs of developing products to a new standard includes the costs of diverting teams from potentially profitable projects. In that case, the opportunity costs would exceed the wages of the engineers. (McAfee, Tr. 11294-295; CCFF 2537).

Rambus's Response to Finding No. 2752:

The proposed finding is contrary to the economic evidence. As a matter of basic economics, the referenced opportunity costs are captured in the wages of the engineers. (Rapp,

Tr. 10158). Further, the proposed finding implicitly assumes that there exist other "potentially profitable projects" whose financial impact would be greater than developing new products to a new standard. There is no evidence of such projects.

2753. Opportunity costs would be incurred if DRAM manufacturers and other component makers were to seek to work around Rambus patents. (Rapp, Tr. 10154-55).

Rambus's Response to Finding No. 2753:

Rambus has no specific response.

2754. The desire on the part of buyers to have multiple suppliers tends to encourage a single product to become a dominant standard. (McAfee, Tr. 7225-26).

Rambus's Response to Finding No. 2754:

The proposed finding is misleading and contrary to the evidence. (*See* RRFF 2601).

(C) Intellectual Property Is an Important Concern in the Industry.

2755. Intellectual property is important from an economic standpoint in the DRAM industry. (McAfee, Tr. 7409-410).

Rambus's Response to Finding No. 2755:

The proposed finding is too ambiguous to permit a response.

2756. Industry members have been concerned for years about the potential for the presence of patents or other IP relating to the standards. (CCFF 300-304).

Rambus's Response to Finding No. 2756:

The proposed finding is vague (how many "years?") and is not supported by the weight of the evidence, which shows that JEDEC often adopted standards that incorporated patented technologies. (*See* RRFF 300-04).

B. The Relevant Product Markets Are Technology Markets.

1. Market Definition Methodology.

2757. The normal starting point for any antitrust analysis is to define the relevant antitrust markets. (McAfee, Tr. 7310). Market definition sets the scope of competitive activity, *i.e.,* identifies the technologies, products, and firms that are relevant to the analysis. Market definition defines the context for performing competitive analysis. (McAfee, Tr. 7309).

Rambus's Response to Finding No. 2757:

The proposed finding is misleading to the extent it implies that market definition is always necessary to determine the issue of market power in antitrust cases. (Rapp, Tr. 10036).

2758. Defining a relevant antitrust product market requires identifying products or collections of products that do not have price-constraining alternatives. (McAfee, Tr. 7314).

Rambus's Response to Finding No. 2758:

The proposed finding is ambiguous and unclear in that it does not define "price-constraining alternatives." Alternatives that are "price-constraining" are not necessarily close economic substitutes. (Teece, Tr. 10367, 10371 ("Well, a technology that is price-constraining is certainly not an economic substitute."); Rapp, Tr. 9861-62). Nor are they necessarily in the same relevant market. (*See* RRFF 2764).

2759. There is a well accepted methodology adhered to by economists for defining relevant markets in antitrust cases. (McAfee, Tr. 7312). The accepted methodology for defining markets is embodied in the approach taken by the Federal Trade Commission and Department of Justice Horizontal Merger Guidelines. (McAfee, Tr. 7314). The FTC-DOJ Horizontal Merger Guidelines use what is called the SSNIP test. (McAfee, Tr. 7331). SSNIP stands for a small but significant non-transitory increase in price. (McAfee, Tr. 7331). The SSNIP test is performed by analyzing the willingness of buyers to shift purchases to a competing product in response to a small but significant price increase. (McAfee, Tr. 7331-32).

Rambus's Response to Finding No. 2759:

The proposed finding is ambiguous and therefore misleading. The proposed finding does not specify what to what price the small but significant increase is to be added. A failure to begin the analysis with the proper starting point – the competitive price – leads to erroneous results.

(*See* RRFF 2764).

2760. The approach of the Horizontal Merger Guidelines is to assume that a hypothetical monopolist controls sales of potentially competing products, and ask whether that monopolist can profitably increase price by a small but significant amount and sustain that price increase. (McAfee, Tr. 7314, 7317, 7331-32; see DX0173).

Rambus's Response to Finding No. 2760:

Rambus has no specific response.

2761. If it is determined that the hypothetical monopolist cannot profitably sustain a small but significant non-transitory increase in price, then the market definition process requires that one keep adding additional potential substitutes to the provisional product market until the collection of products is such that the hypothetical monopolist can sustain a small but significant price increase profitably. (McAfee, Tr. 7317-18).

Rambus's Response to Finding No. 2761:

Rambus has no specific response.

2762. If historical price and quantity data are available, an economist can analyze buyer substitution by looking at what buyers have actually done in response to changes in relative prices. (McAfee, Tr. 7320-21). When historical pricing data relating to actual sales or transactions is unavailable, the general economic approach is nonetheless to try to understand buyer substitution. (McAfee, Tr. 7321). One approach to understanding buyer substitution in the absence of historical pricing data is to interview relevant purchasers in the marketplace. (McAfee, Tr. 7322).

Rambus's Response to Finding No. 2762:

The proposed finding is incomplete. A better way to understand buyer substitution is to look at what buyers in the market actually did. (Rapp, Tr. 9803-05; Teece, Tr. 10366).

2. Individual Technology Markets.

2763. Technology markets are markets for ideas or inventions where technology itself is a product. (McAfee, Tr. 7324; *see* DX0174). The demand for DRAM technology is derived from the demand for DRAMs, and the demand for DRAMs is derived from the final products in which DRAM is used. Ultimately the demand for the technology traces back to the demand for the final good. (McAfee, Tr. 7182, 7198-99; *see* DX-0132).

Rambus's Response to Finding No. 2763:

Rambus has no specific response.

2764. In this case the appropriate starting point in the market definition exercise is to assume preliminarily that the challenged technologies comprise a relevant product market. (McAfee, Tr. 7313-14). The next step is to consider the next closest substitutes - that is, the technologies which are the most price-constraining to the challenged technologies. (McAfee, Tr. 7316-19; *see* DX0173).

Rambus's Response to Finding No. 2764:

The proposed finding is ambiguous, unclear, and logically flawed. First, it does not define "most price-constraining." Alternatives that are "price-constraining" are not necessarily close economic substitutes. (Teece, Tr. 10367, 10371 ("Well, a technology that is price-constraining is certainly not an economic substitute."); Rapp, Tr. 9861-62). Second, for purposes of defining a market, one must know what prices are being constrained, i.e., at what point an alternative product will constrain or prevent a price increase. As courts and economists have long recognized, if a firm is charging a monopoly price, alternatives that will constrain or prevent even higher prices are neither close substitutes nor properly included in the relevant market. Including such alternatives in the market is known as the *Cellophane* fallacy. *See United States v. Eastman Kodak Co.*, 63 F.3d 95, 105 (2d Cir. 1995).

The evidence shows that Complaint Counsel's economic expert failed to account for the *Cellophane* fallacy. Complaint Counsel's economic expert testified that Rambus's royalties for its technologies were { }. (McAfee, Tr. 7634 (*in camera*)). Yet in determining which alternatives he believed were "price constraining," he used Rambus's royalty rates as the starting point:

> Q. Earlier today or -- let me phrase it this way. Earlier in your

testimony, you identified certain alternative technologies that you felt were within the technology markets that you defined; correct?

A. The commercially viable technologies.

Q. Yes. Did you consider each of those technologies to be equally efficient or superior to the Rambus technology that was included within that same market?

A. *When you add royalties to the Rambus technology, yes.*

Q. *So in each instance you were able to do a comparison of those other technologies and conclude that the Rambus royalties were such as to make the other technologies equally efficient or superior?*

A. I'm sorry. *I meant to say that I found them to be price-constraining against the Rambus technology,* which is not quite the same thing as you've said, although it's actually closely related.

(McAfee, Tr. 7577) (emphasis added).

2765. One begins by collecting alternative technically feasible technologies, *i.e.*, those technologies that can perform the same tasks as the challenged technologies in this case. (McAfee, Tr. 7327). The technical feasibility of a technology must be determined by engineering experts in the field. (McAfee, Tr. 7327-29).

Rambus's Response to Finding No. 2765:

Rambus has no specific response.

2766. The next step is to ask which of those technically feasible technologies are price-constraining. (McAfee, Tr. 7330). Another way of characterizing that question is to ask which of the technologies are "commercially viable," ones that, in the event of a price increase associated with the technology in question, informed buyers would have adopted or preferred over the technology with the price increase. (McAfee, Tr. 7330, 7333) This approach is parallel to the SSNIP test, except that no historical price data are available for the analysis. (McAfee, Tr. 7331-

7333; *see* DX0176).

Rambus's Response to Finding No. 2766:

The proposed finding is ambiguous, unclear, and contrary to the evidence. First, it does not define "most price-constraining." Alternatives that are "price-constraining" are not necessarily close economic substitutes. (Teece, Tr. 10367, 10371 ("Well, a technology that is price-constraining is certainly not an economic substitute."); Rapp, Tr. 9861-62). The proposed finding therefore defines "commercially viable" alternatives to include alternatives that are not close economic substitutes. Second, it does not define the "price" that is being constrained. If the price for the exercise already reflects monopoly power, the exercise would erroneously designate poor economic alternatives as close economic substitutes. (*See* RRFF 2764). Third, while Complaint Counsel's economic expert asserted that his method is "parallel" to the SSNIP test in the DoJ and FTC Guidelines, he admitted on cross-examination that he was aware of no economic literature that describes the use of a "commercial viability" test to determine market substitutability of alternatives. (McAfee, Tr. 7576).

2767. Often in technology markets, as is true in this case, frequent trades have historically not taken place. Therefore there is little historical price and quantity data. (McAfee, Tr. 7321).

Rambus's Response to Finding No. 2767:

Rambus has no specific response.

2768. In lieu of data pertaining to actual trades, serious consideration of a technology by JEDEC participants suggests that informed buyers of the technology view those technologies as significant substitutes and hence price-constraining substitutes. (McAfee, Tr. 7333-34). Thus, in connection with defining relevant product markets in this case, it is useful to account for the JEDEC standardization and selection process. (McAfee, Tr. 7335).

Rambus's Response to Finding No. 2768:

The proposed finding is misleading and reflects an error that permeates Complaint Counsel's economic evidence. (*See* RRFF 2769).

2769. The relevant purchasers or buyers in this case are the decision-makers at JEDEC, *i.e.*, the participants who choose technology to be incorporated into JEDEC standards (McAfee, Tr. 7323-24). These buyers include DRAM manufacturers. (McAfee, Tr. 7323-24).

Rambus's Response to Finding No. 2769:

The proposed finding and the previous proposed finding are misleading and reflect an error that permeates Complaint Counsel's economic evidence. In effect, the proposed finding substitutes JEDEC for the relevant buyers and substitutes the "JEDEC standardization and selection process" for the market. Complaint Counsel ask Your Honor to find that, "The demand for DRAM technology is derived from the demand for DRAMs, and the demand for DRAMs is derived from the final products in which DRAM is used. Ultimately the demand for the technology traces back to the demand for the final good." (CCFF 2763). Complaint Counsel also ask Your Honor to find that the DoJ and FTC Guidelines focus on the "willingness of buyers to shift purchases to a competing product in response to a small but significant price increase." (CCFF 2759). Yet here, the proposed finding focuses not on buyers of DRAM technology, and not on the demand for DRAM technologies that is derived from the demand for the final good, but on JEDEC.

The finding is therefore misleading and faulty because the evidence shows that JEDEC's "standardization and selection process" is not a reflection of buyer's preferences or of the market. First, standardization by JEDEC does not guarantee market success, which demonstrates that JEDEC's process is not a proxy for buyer preferences. Complaint Counsel's economic expert

admitted that "I would agree that there are technologies that were standardized [by JEDEC] that were not adopted by the marketplace, DRAM technologies that were standardized that were not adopted by the marketplace." (McAfee, Tr. 11343). JEDEC standardized Burst EDO, for example, but it was not accepted in the market. (Williams, Tr. 873). Second, the evidence shows that JEDEC has failed to standardize technologies that were in fact preferred by buyers. For instance, JEDEC rejected the proposal for the latest generation of Video RAM technology. (Prince, Tr. 9021). Yet when Samsung brought the technology to the market, it was accepted and produced in volume. (Prince, Tr. 9021-22). Similarly, RLDRAM was developed outside of JEDEC and has become successful. (Bechtelscheim, Tr. 5965-66). In short, JEDEC is not a surrogate for buyer preferences, and it is not a surrogate for the market.

2770. JEDEC members include chipset manufacturers, microprocessor manufacturers, integrated circuit packaging companies, memory module manufacturers, motherboard manufacturers, DRAM manufacturers, PC-OEMs, printer manufacturers, networking companies and cell phone manufacturers. (CCFF 210-213).

Rambus's Response to Finding No. 2770:

The proposed finding is misleading to the extent that it implies that the JEDEC decision-making process reflects the preferences of these various entities. The evidence instead shows that JEDEC is not a surrogate for buyer preferences for the market (*see* RRFF 2769), and that the JEDEC decision-making process has been captured by a small group of DRAM manufacturers. (*See* RRFF 206, 244).

2771. Here, in particular, DRAM manufacturers are the relevant consumers in the relevant technology markets and are the relevant consumers to consider in evaluating the competitive effects of Rambus's conduct. (Rapp, Tr. 9969-72).

Rambus's Response to Finding No. 2771:

While it is true that DRAM manufacturers are relevant consumers, assuming a competitive market, their preferences are driven by the market demands of consumers DRAM (the final goods). (*See* RRFF 2763). The only circumstance in which DRAM manufacturer preferences would not reflect the demands of their customers would be if the DRAM manufacturers formed a cartel. (Rapp, Tr. 9936-37).

2772. Factors that enter into JEDEC's decision-making process are relevant to the evaluation of commercially viable alternatives. (McAfee, Tr. 7335). For example, if "time to market" is a factor that influences JEDEC's decision-making process, that factor can affect an assessment of commercial viability. (McAfee, Tr. 7335-336).

Rambus's Response to Finding No. 2772:

The proposed finding is misleading and reflects an error that permeates Complaint Counsel's economic evidence. (*See* RRFF 2769).

2773. If "time to market" is an important factor, then economics teaches that decision-makers may not be willing to spend the amount of time necessary to find the perfect solution to the problem. (McAfee, Tr. 7336). Instead, decision-makers may "satisfice" – that is to say, evaluate technologies as equal when the benefit of finding the best solution is outweighed by the cost of the time it would take to find that solution. (McAfee, Tr. 7335-336).

Rambus's Response to Finding No. 2773:

The proposed finding is misleading to the extent that it implies that JEDEC did not deliberate on issues of cost and performance. (*See* RRFF 2650). It is further not supported by the evidence to the extent that it implies that the doctrine of revealed preference is not applicable to JEDEC's behavior. As Dr. Rapp explained:

> Q. Let me ask it this way.
>
> If the time to market is in fact a critical factor for purposes of JEDEC

making its determination as to what DRAM standard to adopt, would that be consistent with an interpretation of satisficing that said that JEDEC was content to settle for something other than the best technology?

A. Not necessarily.

Q. Why not?

A. Because it -- product choices or technology choices have different dimensions. Time to market is certainly one of the dimensions that ought to be taken into account and I'm certain that manufacturers do take into account because of the nature of the industry. But it doesn't follow from that, in my opinion, that there is a less than complete desire to try and find the best technical solution in terms of cost-performance, taking time to market into account.

Q. Would taking time to market into account be consistent with the theory of revealed preference that you've described for us earlier?

A. Entirely consistent with it.

(Rapp, Tr. 9808-09).

2774. In situations before a standard issues, if there exists a range of roughly equivalent alternative technologies, simply picking one and standardizing on it facilitates coordination and avoids fragmentation. In such situations, the chosen alternative may be only slightly superior *ex ante* to other feasible alternatives, and the SSO could just have easily have chosen another alternative. (Teece, Tr. 10484).

Rambus's Response to Finding No. 2774:

The proposed finding is incomplete. The proposed finding selectively quotes from an article written by Professor Teece. The cited passage is preceded by, "The alternative selected as the standard may be significantly superior to the alternatives, and if so, it is likely that the SSO

would have been reluctant to adopt a different standard." (Teece, Tr. 10483). With respect to the complete passage, Professor Teece testified, "I'm saying there's two possibilities. There's obviously a lot more than two, but one is there's a bunch of alternatives and it's a nice -- a knife edge decision as to which one you choose, and in other cases, there may be particular technologies that are clearly preferable, so just about anything is possible as a matter of theory." (Teece, Tr. 10484). Further, in the article, Professor Teece wrote, "Ex post, once a standard has been adopted and a patent reading on the standard has been asserted, the accused infringers clearly have a strong incentive to claim that the SSO would have adopted some alternative nonpatented standard had the SSO only known of the existence of the patent. In our experience, such claims rarely articulate which alternative would have been adopted or demonstrate that the SSO would in fact have adopted a different alternative." (Teece, Tr. 10798).

2775. Completing standards in a timely manner is important to JEDEC.(CCFF 123)

Rambus's Response to Finding No. 2775:

The proposed finding is misleading to the extent that it implies that the doctrine of revealed preference is inapplicable to JEDEC's behavior. (*See* RRFF 2773). The proposed finding is also misleading and reflects an error that permeates Complaint Counsel's economic evidence, in that it implies that JEDEC is a surrogate for buyer preferences and for the market. (*See* RRFF 2769).

2776. Individual JEDEC members differed with respect to the features they wanted to see in the standards. (CCFF 248-249, 251-254, 505-506)

Rambus's Response to Finding No. 2776:

The proposed finding is misleading and reflects an error that permeates Complaint

Counsel's economic evidence, in that it implies that JEDEC is a surrogate for buyer preferences and for the market. (*See* RRFF 2769).

2777. JEDEC members were willing to make compromises in order to have the standards pass more quickly. (CCFF 124)

Rambus's Response to Finding No. 2777:

The proposed finding is not supported. (*See* RRFF 124). The proposed finding is also misleading and reflects an error that permeates Complaint Counsel's economic evidence, in that it implies that JEDEC is a surrogate for buyer preferences and for the market. (*See* RRFF 2769).

2778. Another factor would be if JEDEC has a preference not to adopt technologies to which intellectual property attaches. If so, such a technology would be less likely to be selected and less likely to be considered commercially viable. (McAfee, Tr. 7337).

Rambus's Response to Finding No. 2778:

The proposed finding is misleading and reflects an error that permeates Complaint Counsel's economic evidence, in that it implies that JEDEC is a surrogate for buyer preferences and for the market. (*See* RRFF 2769).

2779. There was a strong preference at JEDEC to avoid standards that included intellectual property. (CCFF 300-304).

Rambus's Response to Finding No. 2779:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 300-304). JEDEC's actual behavior demonstrates that there was no preference to avoid standards that included patented technology. (*See* RPF 1220-38). In fact, the long-time chair of JC 42.3 testified that he could not recall a single instance where JEDEC avoided a patented technology it considered to be best after receiving a RAND letter. (Kelley, Tr. 2707-09). The JEDEC minutes also show numerous instances of JC 42.3 standardizing technolgies despite patent issues, often

without receiving a RAND letter. (*See* RPF 1224-38). The proposed finding also inaccurately implies that JEDEC is a surrogate for buyer preferences and for the market. (*See* RRFF 2769).

2780. In addition, the evaluation of commercial viability should account for the cost of manufacturing and implementing a prospective technology relative to its expected performance, although differences in the positions of the firms in JEDEC might influence what each sees as the best cost/performance solution. (McAfee, Tr. 7337-39; CCFF 125)

Rambus's Response to Finding No. 2780:

While Rambus agrees that cost-performance issues are important for determining substitutes, the proposed finding is misleading and inaccurately implies that JEDEC is a surrogate for buyer preferences and for the market. (*See* RRFF 2769).

2781. Also, in the DRAM marketplace, the technically superior technology may not always win the standards competition, if, for example, the technology's performance improvements are ahead of their time from the standpoint of what customers are demanding at a given point in time. (Rapp, Tr. 10065).

Rambus's Response to Finding No. 2781:

Rambus has no specific response.

2782. For example, a form of dual-edged clocking called "high-speed toggle mode" was presented at JEDEC a number of times in the early 1990s, but was not adopted until the DDR SDRAM standard. (CCFF 129, 508-510, 515-526).

Rambus's Response to Finding No. 2782:

The proposed finding is misleading in that it implies that "high-speed toggle mode" is related to dual-edge clocking or that it was adopted in the DDR standard. (*See* RRFF 129, 508-10, 515-26).

2783. At the time it was first proposed, one issue that the 42.3 committee had with the high speed toggle mode proposal was that it provided performance that was not needed at the time. (CCFF 129, 525-526).

Rambus's Response to Finding No. 2783:

The proposed finding is misleading. (*See* RRFF 129, 525-26).

2784. In assessing "commercial viability," it is also significant that, at the time that the technologies are selected for incorporation into a standard, not all of the facts are known. There may be substantial uncertainty as to all of the implementation costs and problems to be solved. (McAfee, Tr. 7340). The presence of uncertainty tends to blur the distinctions between the technologies, and thus make it more likely that a technology is commercially viable, *i.e.,* increase the likelihood that more technologies would be considered to be commercially viable. (McAfee, Tr. 7341; CCFF 130-131).

Rambus's Response to Finding No. 2784:

The proposed finding is misleading and logically inconsistent. First, the definition of "commercially viable" given by Complaint Counsel is not proper for market definition purposes. (*See* RRFF 2764; *see also* RPF Section XII.A.3). Second, if there is uncertainty as to the implementation costs and problems to be solved for a technologies, this uncertainty is just as likely to cut against a given technology as it is to "blur the distinctions" between technologies. Further, the proposed finding has no application to the facts of this case; the evidence shows that Rambus's technologies were clearly superior to alternatives in cost-performance terms. (*See* RPF Section X.B).

2785. "Commercially viable" alternatives include alternatives not chosen, *i.e.,* alternatives to which customers could shift even though they are not first on the hierarchy of choices and therefore are not initially chosen. (Rapp, Tr. 10231-32).

Rambus's Response to Finding No. 2785:

The proposed finding is fundamentally misleading; it refers to a definition of "commercially viable" given by Dr. Rapp, which is not the same as that given by Complaint Counsel's economic expert (Rapp, Tr. 10231-32), yet the proposed finding does not state this.

2786. The relevant time frame for defining product markets in this case is the time prior

to the issuing of a standard. (McAfee, Tr. 7351).

Rambus's Response to Finding No. 2786:

Rambus has no specific response.

2787. Based on the above-described analytical framework for defining the product markets relevant to analyzing the competitive issues in this case, there are four relevant technology markets. (McAfee, Tr. 7163, 7390). These relevant technology markets are the latency technology market (McAfee, Tr. 7364; *see* DX0187), the burst length technology market (McAfee, Tr. 7373; *see* DX0194), the data acceleration technology market (McAfee, Tr. 7380; *see* DX0200), and the clock synchronization technology market (McAfee, Tr. 7385-86; *see* DX0207).

Rambus's Response to Finding No. 2787:

The proposed finding rests on faulty and misleading definitions and methodology. (*See* RRFF 2764).

2788. Dr. Rapp did not conduct any market definition analysis in this case. (Rapp, Tr. 10032).

Rambus's Response to Finding No. 2788:

The proposed finding is incomplete. Dr. Rapp testified that "the basis for my views of this fundamentally is that relevant market is not crucial to understanding competition and market power in this setting." (Rapp, Tr. 10036).

2789. Dr. Rapp does not have any disagreements with the Professor McAfee's market definitions that merit engagement. (Rapp, Tr. 10044).

Rambus's Response to Finding No. 2789:

The proposed finding is misleading and miscites Dr. Rapp's testimony. He testified that the issue of market definition does not merit engagement, not that he had no disagreements with Professor McAfee's market definitions. (Rapp, Tr. 10044 ("Q. . . you don't disagree with the Professor McAfee's market definitions or you at least don't find that that merit -- that issue merits

engagement? A. It's correct that I do not find that that issue merits engagement."). As Dr. Rapp explained, "the basis for my views of this fundamentally is that relevant market is not crucial to understanding competition and market power in this setting." (Rapp, Tr. 10036).

2790. The relevant time frame for defining the latency and burst length technology markets was roughly 1992. (McAfee, Tr. 7351-52; CCFF 527-544).

Rambus's Response to Finding No. 2790:

Rambus has no specific response.

2791. Technically feasible alternatives for programmable CAS latency include: fixed CAS latency, pin strapping (setting CAS latency with a dedicated pin), programming CAS latency in the read command, and setting CAS latency by fuses. (CCFF 2130-227; *see* DX-0182).

Rambus's Response to Finding No. 2791:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.3; RRFF 2130-227).

2792. Fixed CAS latency, pin strapping (setting CAS latency with a dedicated pin), programming CAS latency in the read command, and setting CAS latency by fuses were all seriously considered by engineers at JEDEC. (CCFF 2131).

Rambus's Response to Finding No. 2792:

The proposed finding is misleading to the extent that it implies that consideration at JEDEC reflects buyer or market preferences. (*See* RRFF 2769).

2793. Prior to the standardization of programmable CAS latency, fixed CAS latency was a commercially viable alternative to programmable CAS latency. (McAfee, Tr. 7354; *see* DX-0183).

Rambus's Response to Finding No. 2793:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.3). The proposed finding is also unsupported in that it rests on a faulty methodology for

defining "commercially viable." (*See* RRFF 2764, 2769; *see also* RPF Section XII.A.3).

2794. Prior to the standardization of programmable CAS latency, pin strapping, or the use of one or more dedicated pins to set CAS latency, was a commercially viable alternative to programmable CAS latency. (McAfee, Tr. 7357, 7359; *see* DX-0184).

Rambus's Response to Finding No. 2794:

The proposed finding is not supported by the weight of the evidence. (See RPF Section IX.B.3). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable." (*See* RRFF 2764, 2769; *see also* RPF Section XII.A.3).

2795. Prior to the standardization of programmable CAS latency, setting CAS latency in the read command was a commercially viable substitute for programmable CAS latency. (McAfee, Tr. 7359; *see* DX-0185).

Rambus's Response to Finding No. 2795:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.3). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable." (*See* RRFF 2764, 2769; *see also* RPF Section XII.A.3).

2796. Prior to the standardization of programmable CAS latency, setting CAS latency by fuses was a commercially viable substitute for programmable CAS latency. (McAfee, Tr. 7361; *see* DX-0186).

Rambus's Response to Finding No. 2796:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.3). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable." (*See* RRFF 2764, 2769).

2797. Because these technologies were commercially viable prior to standardization, they constrained the price of programmable CAS latency in the latency technology market. (McAfee, Tr. 7363-64; CCFF 2766; *see* DX0187).

Rambus's Response to Finding No. 2797:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.3). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable" and "price constraining." (*See* RRFF 2764, 2769; RPF Section XII.A.3).

2798. Insufficient evidence is available to determine whether scaling CAS latency with a clock frequency was a commercially viable alternative to programmable CAS latency. (McAfee, Tr. 7363).

Rambus's Response to Finding No. 2798:

Rambus has no specific response.

2799. Technically feasible alternatives for programmable burst length include: fixed burst length, pin strapping (setting burst length with a dedicated pin), programming burst length in the read command, and using a burst interrupt command. (CCFF 2234-260, 2270-2318; *see* DX-0189).

Rambus's Response to Finding No. 2799:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.3; RRFF 2234-260, 2270-318).

2800. Fixed burst length, pin strapping (setting burst length with a dedicated pin), programming burst length in the read command, and using a burst interrupt command were all seriously considered by engineers at JEDEC. (CCFF 2235).

Rambus's Response to Finding No. 2800:

The proposed finding is misleading to the extent that it implies that consideration at JEDEC reflects buyer or market preferences. (*See* RRFF 2769).

2801. Prior to the standardization of programmable burst length, fixed burst length was a commercially viable alternative to programmable burst length. (McAfee, Tr. 7367; *see* DX-0190).

Rambus's Response to Finding No. 2801:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.3). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable" and "price constraining." (*See* RRFF 2764, 2769; RPF Section XII.A.3).

2802. Prior to the standardization of programmable burst length, setting burst length with one or more dedicated pins was a commercially viable alternative to programmable burst length. (McAfee, Tr. 7368; *see* DX-0191).

Rambus's Response to Finding No. 2802:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.3). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable" and "price constraining." (*See* RRFF 2764, 2769; RPF Section XII.A.3).

2803. Prior to the standardization of programmable burst length, setting burst length in the read command was a commercially viable alternative to programmable burst length. (McAfee, Tr. 7369; *see* DX-0192).

Rambus's Response to Finding No. 2803:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.3). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable" and "price constraining." (*See* RRFF 2764, 2769; RPF Section XII.A.3).

2804. Prior to the standardization of programmable burst length, use of a burst interrupt command to set burst length was a commercially viable alternative to programmable burst length. (McAfee, Tr. 7370; *see* DX-0193).

Rambus's Response to Finding No. 2804:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.3). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable" and "price constraining." (*See* RRFF 2764, 2769; RPF Section XII.A.3).

2805. Because these technologies were commercially viable prior to standardization, they constrained the price of programmable burst length in the burst length technology market. (McAfee, Tr. 7373; CCFF 2766; *see* DX-0194).

Rambus's Response to Finding No. 2805:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.3). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable" and "price constraining." (*See* RRFF 2764, 2769; RPF Section XII.A.3).

2806. Insufficient evidence is available to determine whether using fuses to set burst length was a commercially viable alternative to programmable burst length. (McAfee, Tr. 7372).

Rambus's Response to Finding No. 2806:

Rambus has no specific response.

2807. The relevant time frame for defining the data acceleration technology and the clock synchronization technology markets is roughly 1995. (McAfee, Tr.7376-77; CCFF 2232-234, 2366-367).

Rambus's Response to Finding No. 2807:

Rambus has no specific response.

2808. Technically feasible alternatives for dual-edge clocking include: interleaving banks on the module, doubling the clock frequency, and toggle mode. (CCFF 2322-365; *see* DX0196).

Rambus's Response to Finding No. 2808:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.4; RRFF 2322-365).

2809. Interleaving banks on the module, doubling the clock frequency, and toggle mode were all seriously considered by engineers at JEDEC. (CCFF 2323-24).

Rambus's Response to Finding No. 2809:

The proposed finding is misleading to the extent that it implies that consideration at JEDEC reflects buyer or market preferences. (*See* RRFF 2769).

2810. Prior to the standardization of dual-edge clocking, interleaving banks on the module was a commercially viable alternative to dual-edged clocking. (McAfee, Tr. 7377; *see* DX-0197).

Rambus's Response to Finding No. 2810:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.4). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable" and "price constraining." (*See* RRFF 2764, 2769; RPF Section XII.A.3).

2811. Prior to the standardization of dual-edge clocking, doubling the clock frequency was a commercially viable alternative to dual-edged clocking. (McAfee, Tr. 7379; *see* DX-0199).

Rambus's Response to Finding No. 2811:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.4). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable" and "price constraining." (*See* RRFF 2764, 2769; RPF Section XII.A.3).

2812. Prior to the standardization of dual-edge clocking, toggle mode was a

commercially viable alternative to dual-edged clocking. (McAfee, Tr. 7380; *see* DX-0214).

Rambus's Response to Finding No. 2812:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.4). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable" and "price constraining." (*See* RRFF 2764, 2769; RPF Section XII.A.3).

2813. Because these technologies were commercially viable prior to standardization, they constrained the price of dual-edged clocking in the data acceleration technology market. (McAfee, Tr. 7380, 7402; CCFF 2766; *see* DX-0213).

Rambus's Response to Finding No. 2813:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.4). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable" and "price constraining." (*See* RRFF 2764, 2769; RPF Section XII.A.3).

2814. Professor McAfee did not consider increasing the number of pins per module as a commercially viable alternative to dual-edged clocking. (McAfee, Tr. 7378; *see* DX0198)

Rambus's Response to Finding No. 2814:

Rambus has no specific response.

2815. Technically feasible alternatives for on-chip PLL/DLL include: putting DLL on the memory controller, putting the DLL on the module, using a Vernier technique, and using no DLL at all . (CCFF 2366-2414; *see* DX0202).

Rambus's Response to Finding No. 2815:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.4; RRFF 2366-414).

2816. Putting DLL on the memory controller, putting the DLL on the module, using a Vernier technique, and using no DLL at all were all seriously considered by engineers at JEDEC. (CCFF 2367).

Rambus's Response to Finding No. 2816:

The proposed finding is misleading to the extent that it implies that consideration at JEDEC reflects buyer or market preferences. (*See* RRFF 2769).

2817. Prior to the standardization of on-chip PLL/DLL, putting DLL on the memory controller was a commercially viable alternative to on-chip PLL/DLL. (McAfee, Tr. 7382; *see* DX0203).

Rambus's Response to Finding No. 2817:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.4). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable" and "price constraining." (*See* RRFF 2764, 2769; RPF Section XII.A.3).

2818. Putting the DLL on the module was a commercially viable alternative to on-chip PLL/DLL. (McAfee, Tr. 7383; *see* DX0204).

Rambus's Response to Finding No. 2818:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.4). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable" and "price constraining." (*See* RRFF 2764, 2769; RPF Section XII.A.3).

2819. Using a Vernier technique was a commercially viable alternative to on-chip PLL/DLL. (McAfee, Tr. 7383; *see* DX0205).

Rambus's Response to Finding No. 2819:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section

IX.B.4). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable" and "price constraining." (*See* RRFF 2764, 2769; RPF Section XII.A.3).

2820. Using no DLL at all was a commercially viable alternative to on-chip PLL/DLL. (McAfee, Tr. 7384; *see* DX0206).

Rambus's Response to Finding No. 2820:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.4). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable" and "price constraining." (*See* RRFF 2764, 2769; RPF Section XII.A.3).

2821. Because these technologies were commercially viable prior to standardization, they constrained the price of on-chip PLL/DLL in the clock synchronization technology market. (McAfee, Tr. 7385-86; CCFF 2766; *see* DX-0207).

Rambus's Response to Finding No. 2821:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section IX.B.4). The proposed finding is also unsupported in that it rests on a faulty methodology for defining "commercially viable" and "price constraining." (*See* RRFF 2764, 2769; RPF Section XII.A.3).

2822. Dr. Rapp agrees that potentially one of the lost competitive advantages to Rambus of disclosing patent-related information to JEDEC is that this could induce work-around efforts. (Rapp, Tr. 10171).

Rambus's Response to Finding No. 2822:

The proposed finding is incomplete. Dr. Rapp testified that the potential loss of competitive advantage was a legitimate business justification for not disclosing information

about Rambus's pending or future patent applications. (Rapp, Tr. 9915-18).

2823. In Dr. Rapp's view, the fact that a Rambus disclosure to JEDEC could induce work-around efforts is a reason why it would not have been in Rambus's interest to disclose additional patent-related information to JEDEC. (Rapp, Tr. 10171).

Rambus's Response to Finding No. 2823:

The proposed finding is incomplete. Dr. Rapp testified that the potential loss of competitive advantage was a legitimate business justification for not disclosing information about Rambus's pending or future patent applications. (Rapp, Tr. 9915-18).

2824. Dr. Rapp agrees that it is possible that the effect of Rambus disclosing patent application-related information to JEDEC might have been that it would have caused JEDEC participants to commence efforts to try to work around what they understood the patent applications to cover. (Rapp, Tr. 10175).

Rambus's Response to Finding No. 2824:

While the proposed finding accurately reflect Dr. Rapp's testimony of what "might" have occurred as a theoretical matter, the evidence shows that additional disclosures by Rambus would not have induced any work around efforts by JEDEC. (*See* RPF Section IX.A, IX.C).

2825. In his analysis of whether it would have been economically rational for JEDEC or JEDEC participants to switch to alternatives rather than include the Rambus-claimed technologies, Dr. Rapp assumed that JEDEC would choose the best cost-performance options. (Rapp, Tr. 10196-197).

Rambus's Response to Finding No. 2825:

The proposed finding is incomplete. The evidence shows that JEDEC did make every effort to select the best technology in cost performance terms. (*See* RRFF 2764).

2826. Dr. Rapp did not make any assumptions about the way that the JEDEC process or the JEDEC rules work. (Rapp, Tr. 10197).

Rambus's Response to Finding No. 2826:

While the proposed finding accurately reflects Dr. Rapp's testimony, it is misleading to the extent that it implies that JEDEC's process or rules are a surrogate for buyer preferences or for the market. (*See* RRFF 2769).

2827. Dr. Rapp just assumed that a rational standards organization and rational members of such an organization would choose the best cost-performance options. (Rapp, Tr. 10197).

Rambus's Response to Finding No. 2827:

Rambus has no specific response.

2828. All of the cost information that Dr. Rapp used in his analysis came from Mr. Geilhufe's testimony. (Rapp, Tr. 10201).

Rambus's Response to Finding No. 2828:

The proposed finding is incomplete. Dr. Rapp also testified that he and his staff found no other cost information available. (Rapp, Tr. 10201-03).

2829. In conducting the analysis summarized in his report, Dr. Rapp did not seek to obtain cost information on any alternatives from JEDEC or JEDEC participants or JEDEC-related documents that might cost information. (Rapp, Tr. 10201).

Rambus's Response to Finding No. 2829:

The proposed finding is contrary to the evidence. Dr. Rapp testified, "my staff looked for cost information at the time available. The reason that there was none that I considered in the expert report is that none was available to me." (Rapp, Tr. 10201-02).

2830. Dr. Rapp did not review JEDEC-related materials to see if he could corroborate the cost information that he obtained from Mr. Geilhufe. (Rapp, Tr. 10201).

Rambus's Response to Finding No. 2830:

The proposed finding is contrary to the evidence. Dr. Rapp testified, "my staff looked for

cost information at the time available. The reason that there was none that I considered in the expert report is that none was available to me." (Rapp, Tr. 10201-02).

2831. Dr. Rapp understands that Mr. Geilhufe did not testify as to what cost information JEDEC or JEDEC participants had in this *ex ante* time period. (Rapp, Tr. 10203).

Rambus's Response to Finding No. 2831:

Rambus has no specific response.

2832. Dr. Rapp agrees that if in the relevant time period, JEDEC participants had information about the costs of the alternatives that Dr. Rapp considered that was different from Mr. Geilhufe's cost information, that might undermine the economic conclusions that Dr. Rapp made about what decisions would be rational for JEDEC or JEDEC participants to make in the but-for world. (Rapp, Tr. 10203-204 ("It could, but it would depend greatly on the nature of that cost information and whether it was appropriate to solving the problem that we are solving by the cost analysis, Mr. Geilhufe's and subsequently mine.")).

Rambus's Response to Finding No. 2832:

The proposed finding is incomplete. There is no evidence that JEDEC members had different information; even Complaint Counsel's economic expert testified that there was no contemporaneous cost estimates for alternatives available in the record. (McAfee, Tr. 7576).

2833. Dr. Rapp agrees that if it were the case that JEDEC or JEDEC participants had different information about the costs of the alternatives that Dr. Rapp considered, that might suggest that JEDEC participants could have reached different conclusions than the conclusions that he reached and still have been acting in an economically rational manner. (Rapp, Tr. 10204 ("I will admit to the possibility that it would suggest that, but nothing more. In other words, it would not indicate that. It would raise the possibility of it.")).

Rambus's Response to Finding No. 2833:

The proposed finding is incomplete. Dr. Rapp testified that any effect on his analysis "would depend greatly on the nature of the cost information and whether it was appropriate to solving the problem that we are solving . . ." (Rapp, Tr. 10203-04). Further, there is no evidence that JEDEC members had different information; even Complaint Counsel's economic expert

testified that there was no contemporaneous cost estimates for alternatives that were available in the record. (McAfee, Tr. 7576).

2834. Dr. Rapp agrees that the information JEDEC participants had in the relevant time period about the alternatives that Dr. Rapp considered as part of his analysis could have impacted what choices would have been economically rational for such JEDEC participants to make. (Rapp, Tr. 10204-205).

Rambus's Response to Finding No. 2834:

The proposed finding is incomplete. There is no evidence that JEDEC members had different information; even Complaint Counsel's economic expert testified that there was no contemporaneous cost estimates for alternatives that were available in the record. (McAfee, Tr. 7576).

2835. Dr. Rapp agrees that he does not know what information any individual JEDEC participant in fact did have relating to any specific alternative that he considered. (Rapp, Tr. 10205).

Rambus's Response to Finding No. 2835:

The proposed finding is incomplete. Dr. Rapp also testified, "it is in the nature of the kind of analysis that economists normally do to use available data to make inferences about what individual decision makers would do at a particular time in a particular economic choice even though the data that was -- that were available, even though it's not known that that -- that those data were on the desktop of the individual in question. There's nothing unusual about that situation." (Rapp, Tr. 10205).

2836. Because Dr. Rapp agrees that he does not know what information any individual JEDEC participant had relating to any specific alternative that Dr. Rapp considered, he also agrees that he cannot say as a matter of economic analysis what decision would have been economically rational for any JEDEC participant during the relevant time period based on information that was at the disposal of such JEDEC participants. (Rapp, Tr. 10205 ("But it is in the nature of the kind of analysis that economists normally do to use available data to make

inferences about what individual decision makers would do at a particular time in a particular economic choice even though the data that was -- that were available, even though it's not known that that – that those data were on the desktop of the individual in question. There's nothing unusual about that situation.")).

Rambus's Response to Finding No. 2836:

The proposed finding is incomplete. Dr. Rapp testified that his method is the standard economic procedure. (Rapp, Tr. 10205). There is no evidence that JEDEC members had different information; even Complaint Counsel's economic expert testified that there was no contemporaneous cost estimates for alternatives that were available in the record. (McAfee, Tr. 7576).

2837. Dr. Rapp cannot rule out the possibility that for some of the companies that were participants of JEDEC in the relevant time, based on the information that they possessed, the economically rational thing would have been to support the use of various alternatives over the use of Rambus' technologies. (Rapp, Tr. 10205-206).

Rambus's Response to Finding No. 2837:

The proposed finding is misleading and incomplete. Dr. Rapp testified, "Let me say that I can't rule that out except to the extent that the information isn't available at all, in which case there would be no basis for assuming its existence." (Rapp, Tr. 10206). There is no evidence that JEDEC members had different information; even Complaint Counsel's economic expert testified that there was no contemporaneous cost estimates for alternatives that were available in the record. (McAfee, Tr. 7576).

2838. Dr. Rapp agrees that JEDEC and/or specific JEDEC participants would not have known specifically what royalties Rambus would seek in connection with the technologies that Rambus has claimed in the event that those technologies were adopted as part of JEDEC's standards. (Rapp, Tr. 10206-207).

Rambus's Response to Finding No. 2838:

The proposed finding is misleading and incomplete. Using actual royalty rates is a standard economic assumption: "it's a standard assumption in economics -- that they would have been able to anticipate what turned out to be a market outcome. It doesn't assume they would have known with precision. It assumes that that is the best estimate, that the actual royalty rates ex post are the best estimate *ex ante*." (Rapp, Tr. 10207).

2839. Dr. Rapp agrees that it is possible that in the but-for world JEDEC participants might have been required to make judgments and choices between Rambus' technologies and alternative technologies without knowing what royalties Rambus ultimately might charge for the use of its technologies if they were used in the JEDEC standards. (Rapp, Tr. 10207-208 ("Without knowing with precision but with a certain capacity for anticipation if they had the disclosure at their disposal and if they knew about what the alternatives were.")).

Rambus's Response to Finding No. 2839:

The proposed finding is misleading and incomplete. Dr. Rapp testified that he considered and accounted for the issue of *ex ante* uncertainty: "I assume that there is a kind of confidence interval around the analysis that I've done that nobody would expect an estimate of perfect precision after the fact, but what we have are a set of best estimates, best estimate of the royalty rate and best estimate of costs, and those are the ones to use in that circumstance just as a matter of normal practice." (Rapp, Tr. 10208).

2840. Dr. Rapp agrees that, to the extent that JEDEC participants were uncertain about what royalty would apply, there could be varying projections from JEDEC participant to JEDEC participant regarding what royalty rates would apply to the Rambus technologies and those projections could differ from the royalty rates that he assumed in material ways. (Rapp, Tr. 10209 ("And I think the best single estimate of what the outcome of the variety of different possible forecasts is is the royalty rate that came in fact to be Rambus' royalty rate, the Rambus license royalty rate.")).

Rambus's Response to Finding No. 2840:

The proposed finding is misleading and incomplete. (*See* RRFF 2839).

2841. Dr. Rapp agrees that to the extent that prices are relevant to the analysis of what JEDEC would have done if Rambus had disclosed, the relevant price figures, if this information were available, would be the prices that individual JEDEC participants would have used in making their own calculations about the potential cost of Rambus royalties. (Rapp, Tr. 10211 ("If you'll allow me to say that the anticipations of price that they would have used, then the answer is yes.")).

Rambus's Response to Finding No. 2841:

The proposed finding is misleading and incomplete. There is no evidence of what JEDEC participants projected prices would be. Dr. Rapp testified that "And that's why a good assumption about a piece of information that will substitute for these anticipations in an economic analysis is a weighted average value over a product life cycle, which is what I have used." (Rapp, Tr. 10213).

2842. Dr. Rapp agrees that the reason why anticipated prices are important to his analysis is that prices relating to products in his analysis would not have been for sale at the time the JEDEC members made their decisions. (Rapp, Tr. 10211-212).

Rambus's Response to Finding No. 2842:

Rambus has no specific response.

2843. Dr. Rapp agrees that from the standpoint of the JEDEC participant in 1993 seeking to assess the cost of the Rambus royalties, if they were to do that in anything approaching an accurate sense, they would have to be making projections about the cost of not-yet-standardized devices in the marketplace extending out many years into the future. (Rapp, Tr. 10212).

Rambus's Response to Finding No. 2843:

The proposed finding is incomplete. Dr. Rapp testified: "And that's why a good assumption about a piece of information that will substitute for these anticipations in an economic analysis is a weighted average value over a product life cycle, which is what I have

used." (Rapp, Tr. 10213).

2844. Dr. Rapp is aware that in the real world there have been instances in which JEDEC participants have disclosed patent-related information to JEDEC. (Rapp, Tr.10214).

Rambus's Response to Finding No. 2844:

Rambus has no specific response.

2845. Dr. Rapp has not looked at the factual record in this case to determine whether in instances in which JEDEC participants have disclosed patent-related information to JEDEC, JEDEC participants in deciding what actions to take have applied the same type of analysis or methodology that he applied. (Rapp, Tr. 10214).

Rambus's Response to Finding No. 2845:

The proposed finding is misleading and incomplete. Dr. Rapp testified as follows:

> Q. And would you acknowledge that it's possible that JEDEC participants faced with such situations apply an analysis that is somewhat different from the analysis or methodology that you apply?
>
> A. In its specifics, certainly. In general terms, I believe that the analysis that I applied is very basic and fundamental, and that has to do with the evaluation of cost and performance and the arraying of alternatives in cost-performance terms and for valuation purposes comparing one with the next best alternative. I think that that is very, very widespread and not likely to vary much.

(Rapp, Tr. 10214).

2846. Dr. Rapp relied on only Dr. Soderman for his opinions about whether various alternatives identified by complaint counsel's experts would be subject to Rambus patents. (Rapp, Tr. 10215).

Rambus's Response to Finding No. 2846:

Rambus has no specific response.

2847. Dr. Rapp understands that Dr. Soderman is not a patent lawyer. (Rapp, Tr. 10215).

Rambus's Response to Finding No. 2847:

Rambus has no specific response.

2848. Dr. Rapp is aware that Dr. Soderman has never done design work on synchronous DRAMs. (Rapp, Tr. 10216).

Rambus's Response to Finding No. 2848:

The proposed finding is misleading and incomplete. Regarding Dr. Soderman's experience, Dr. Rapp testified, "I remember his testimony to the effect that he is a designer of products that employ memory and that have the similar circuitry to memory applications, specific integrated circuits among them." (Rapp, Tr. 10216).

2849. Dr. Rapp relied on the work of Mr. Geilhufe to find that there would be a number of different fixed CAS latencies in the event that alternative were chosen to work around the Rambus claims on programmable CAS latency. (Rapp, Tr. 10223).

Rambus's Response to Finding No. 2849:

Rambus has no specific response.

2850. Before completing his expert report, Dr. Rapp did not look at the evidence relating to the process through which JEDEC made the decisions that it made in developing the relevant standards. (Rapp, Tr. 10111).

Rambus's Response to Finding No. 2850:

The proposed finding is misleading to the extent it implies that JEDEC is a substitute for buyer preferences or the market. (*See* RRFF 2769).

2851. Dr. Rapp developed his opinions about the commercial viability of various alternatives without having any understanding as to why JEDEC in fact chose the four Rambus

technologies over any alternatives that it may have considered. (Rapp, Tr. 10111 ("And that is because the commercial viability and substitution qualities of those alternatives are independent of what got said in JEDEC.")).

Rambus's Response to Finding No. 2851:

The proposed finding is misleading to the extent it implies that JEDEC is a substitute for buyer preferences or the market. (*See* RRFF 2769).

2852. Dr. Rapp wrote that "[k]nowing the reasons behind JEDEC's selection of SDRAM as the standard is important for evaluating the economic soundness of the assumption that the members would have switched to an alternative technology if Rambus' potential future royalty demands were disclosed at the time the SDRAM standard was being set." (Rapp, Tr. 10112-113). That was a statement that Dr. Rapp made in the context of criticizing the work or conclusions of another economist in Rambus's case against Micron. (Rapp, Tr. 10113).

Rambus's Response to Finding No. 2852:

The proposed finding is misleading. With regard to this specific criticism of another expert's work, Dr. Rapp testified:

> All of that takes place in the absence of the kind of information that Mr. Geilhufe and Dr. Soderman provided. This critique of Professor Carlton had to do with the fact that the two of us were opposed to one another as experts in this trial and Professor Carlton had proposed that there were alternatives to the Rambus technology without stating what those alternatives were. So there was no discussion of fixed latency and burst and all of the other various alternatives. And in the absence of that information, I said that if he or anybody else was going to reach an ultimate conclusion about what JEDEC would have done in the absence of information, then they would need to know what happened in JEDEC.

> If the -- just a bit more on that. If the door were open for such things, what I would have said is what Professor Carlton needs is Dr. Soderman and Mr. Geilhufe or some equivalent of them in order to be able to make statements, economic statements about the quality of substitution among realistic alternatives.

(Rapp, Tr. 10113-14).

2853. Dr. Rapp's analysis of the alternatives to the disputed technologies is flawed. (McAfee, Tr.11208-209; *see* DX0359).

Rambus's Response to Finding No. 2853:

The proposed finding is not supported by the weight of the evidence. Dr. Rapp's methodology relies on standard economic methodology and standard economic assumptions. (*See* RRFF 2856-60).

2854. Dr. Rapp's analysis of the alternatives relies on a flawed methodology, (CCFF 2856-870) and is not robust to apparently reasonable changes in assumptions. (CCFF 2871-2884).

Rambus's Response to Finding No. 2854:

The proposed finding is not supported by the weight of the evidence. Dr. Rapp's methodology relies on standard economic methodology and standard economic assumptions. (*See* RRFF 2856-60).

2855. Because of the flaws in Dr. Rapp's analysis, it did not change Professor McAfee's opinions regarding the existence of competing alternative technologies *ex ante.* (McAfee, Tr.11279 ("I find his methodology to be flawed and, as a result, I find his criticism of my conclusion that there are commercially viable alternatives to be unfounded and, as a result, I am not inclined to change my conclusion.").

Rambus's Response to Finding No. 2855:

The proposed finding is not supported by the weight of the evidence. Dr. Rapp's methodology relies on standard economic methodology and standard economic assumptions. (*See* RRFF 2856-60).

2856. Dr. Rapp's analysis of alternatives fails to replicate actual JEDEC decision-making behavior. (McAfee, Tr. 11233-34; *see* DX0362).

Rambus's Response to Finding No. 2856:

The proposed finding reveals a fundamental flaw in the analysis of Complaint Counsel's economic expert. Dr. Rapp's task was to determine whether or not there were close economic substitutes for the Rambus technologies. Whether such substitutes existed depends on the cost-performance characteristics preferred by buyers in the market. Complaint Counsel's economic expert erroneously assumed that JEDEC and its standardization processes are a surrogate for the preferences of buyers and the operation of the market. (*See* RRFF 2769).

2857. Simply analyzing what a "rational" DRAM manufacturer or a "rational" standard setting organization would select among alternative technologies cannot lead to an appropriate analysis of how the marketplace decides unless that methodology accounts for how the decisions are made. (McAfee, Tr. 11234-235 ("If you want to actually understand how the marketplace decides, you have to understand how the decisions are made. That is, you have to understand the process by which decisions are actually made, and that is not accounted for in Dr. Rapp's approach.")).

Rambus's Response to Finding No. 2857:

The proposed finding reveals a fundamental flaw in the analysis of Complaint Counsel's economic expert. (*See* RRFF 2769).

2858. An appropriate methodology to determine how JEDEC would select among technologies must take into account the time to market needs of the organization and the resulting satisficing behavior. (McAfee, Tr. 11234-235; *see* DX0362; CCFF 122-124, 2650-658, 2772-777).

Rambus's Response to Finding No. 2858:

The proposed finding reveals a fundamental flaw in the analysis of Complaint Counsel's economic expert. (*See* RRFF 2769). The proposed finding is also unsupported to the extent that it implies that JEDEC did not deliberate on cost-performance issues or that the doctrine of revealed preference is not applicable. (*See* RRFF 2650, 2773).

2859. Failing to take into account the time to market needs of JEDEC makes Dr. Rapp's analysis unreliable. (McAfee, Tr. 11244; *see* DX0362).

Rambus's Response to Finding No. 2859:

The proposed finding reveals a fundamental flaw in the analysis of Complaint Counsel's economic expert. (*See* RRFF 2769). The proposed finding is also unsupported to the extent that it implies that JEDEC did not deliberate on cost-performance issues or that the doctrine of revealed preference is not applicable. (See RRFF 2650, 2773). As Dr. Rapp addressed the issue of time to market:

> Q. Let me ask it this way.
>
> If the time to market is in fact a critical factor for purposes of JEDEC making its determination as to what DRAM standard to adopt, would that be consistent with an interpretation of satisficing that said that JEDEC was content to settle for something other than the best technology?
>
> A. Not necessarily.
>
> Q. Why not?
>
> A. Because it -- product choices or technology choices have different dimensions. Time to market is certainly one of the dimensions that ought to be

taken into account and I'm certain that manufacturers do take into account because of the nature of the industry. But it doesn't follow from that, in my opinion, that there is a less than complete desire to try and find the best technical solution in terms of cost-performance, taking time to market into account.

Q. Would taking time to market into account be consistent with the theory of revealed preference that you've described for us earlier?

A. Entirely consistent with it.

(Rapp, Tr. 9808-09).

2860. An appropriate methodology to determine how JEDEC would select among technologies must take into account the differences between royalties and manufacturing costs. (McAfee, Tr. 11241-242; *see* DX0362 ("A rational manufacturer would not be indifferent between a manufacturing cost and a royalty that were the exact same percentage of their costs generally."); CCFF 107-111).

Rambus's Response to Finding No. 2860:

The proposed finding reveals a fundamental flaw in the analysis of Complaint Counsel's economic expert. (*See* RRFF 2769). The proposed finding is also contrary to the evidence. (*See* RRFF 2861). The proposed finding is also unsupported to the extent that it implies that JEDEC did not deliberate on cost-performance issues or that the doctrine of revealed preference is not applicable. (*See* RRFF 2650, 2773).

2861. One difference between royalties and manufacturing costs is that manufacturing costs are subject to productivity gains that are to some extent under the control of the agent experiencing the costs. (McAfee, Tr. 11242-243; *see* DX0362 ("with manufacturing costs I can seek ways to minimize -- to minimize those costs. That is, I can find ways to actually reduce my costs overall. And that's going to be not possible with a straight percentage royalty.")).

Rambus's Response to Finding No. 2861:

The proposed finding is contrary to the evidence. Complaint Counsel's economic expert

admitted on cross-examination that manufacturing costs are not necessarily "under the control" of the manufacturer:

Q. Okay. We can take that down and bring up if you would DX-362. Let me direct you to the bottom point here where it says, "Royalties and manufacturing costs are not directly comparable." Do you recall testifying about that point earlier today?

A. Yes.

Q. You said one of the things you're able to do is reduce manufacturing costs?

A. That's correct.

Q. You also said that manufacturing costs don't go up with renegotiation, didn't you?

A. That, I did testify, yes.

Q. Have you ever been involved in a labor negotiation?

A. Labor would be the exception that can go up.

Q. What about when your suppliers of materials tell you they've raised the prices? Is that another exception?

A. That could be an exception if you have -- if you aren't facing competitive markets in materials.

Q. Well, even if you're facing markets in your materials, sometimes the costs of materials go up, don't they?

A. Yes, costs of materials can go up.

Q. The costs of manufacturing equipment that you use in your plant can go up, can't it?

A. Yes, the costs of materials in your plants can go up.

(McAfee, Tr. 11348-49).

Complaint Counsel's economic expert also admitted on cross-examination that royalty rates are subject to renegotiation and may go down. (McAfee, Tr. 11350).

Further, the proposed finding is not applicable in this case because the manufacturing costs used in Dr. Rapp's analyses were mature costs, i.e., they were not subject to further productivity gains. (*See* RRFF 2879).

2862. Another difference between royalties based on patents and manufacturing costs is that royalties, unlike manufacturing costs are subject to hold-up, which means that the costs might be increased on renegotiation. (McAfee, Tr. 11243; *see* DX0362 ("Royalties, on the other hand, are subject to hold-up in the sense that if, for example, the contract, the license under which royalties are paid, expires prior to the time that the patents that underlie those royalties expire, you're going to have to renegotiate at some point, and at that point the royalties can be renegotiated upward; that is, the lock-in can be exploited.")).

Rambus's Response to Finding No. 2862:

The proposed finding is not supported by the weight of the evidence. Complaint Counsel's economic expert admitted on cross-examination that royalty rates are subject to renegotiation and may go down. (McAfee, Tr. 11350). Complaint Counsel's economic expert also admitted that manufacturing costs might go up in renegotiation and be subject to hold-up. (*See* RRFF 2861).

2863. Failing to distinguish the differing effects of manufacturing costs and royalties on the decision making of firms at JEDEC has the effect of biasing Dr. Rapp's analysis by understating the importance of royalties compared to manufacturing costs. (McAfee, Tr. 11244).

Rambus's Response to Finding No. 2863:

The proposed finding is contrary to the evidence. On cross-examination, Complaint Counsel's economic expert effectively admitted that the foundation of this proposed finding was erroneous; he admitted that the differences between manufacturing costs and royalties on which he based his opinion had been completely overstated. (*See* RRFF 2861). The proposed finding also is flawed in that it assumes that JEDEC is a substitute for buyer preferences and the market. (*See* RRFF 2769).

2864. An appropriate methodology to determine how JEDEC would select among technologies must take into account the potential impact of IP disclosures on evolution of DRAM technologies in but-for world. (McAfee, Tr. 11245; *see* DX0363).

Rambus's Response to Finding No. 2864:

The proposed finding exposes yet another fundamental flaw in the analysis of Complaint Counsel's economic expert. (*See* RRFF 2868).

2865. Changes in the world can change incentives, which can change the choices that economic actors make. (McAfee, Tr. 11246 ("how changes in the world affect choices that are made is actually a normal economic analysis point, and that changing, for example, the price of some technology, what will that do to demand for technology is right within the core of economic analysis.")).

Rambus's Response to Finding No. 2865:

Rambus has no specific response to the proposed finding as such. The attempted application of this finding exposes yet another fundamental flaw in the analysis of Complaint Counsel's economic expert. (*See* RRFF 2868).

2866. Attempting to recreate the actual world using alternative technologies fails to take into account the fact that, had an alternative technology been selected, the world would have evolved in a different way in that technology would have developed differently. (McAfee, Tr. 11245; *see* DX0363).

Rambus's Response to Finding No. 2866:

The proposed finding exposes yet another fundamental flaw in the analysis of Complaint Counsel's economic expert. (*See* RRFF 2868).

2867. By failing to take into account the effect of changes in the world on the evolution of DRAM technologies, Dr. Rapp in making his cost estimates, for example, makes the mistake of assuming that JEDEC would have made the same choices regarding the number of CAS latencies and burst lengths using the fixed CAS latency and fixed burst length alternative that JEDEC made when using the programmable CAS latency and programmable burst length alternative that JEDEC chose in the actual world. (McAfee, Tr. 11246-247).

Rambus's Response to Finding No. 2867:

The proposed finding exposes yet another fundamental flaw in the analysis of Complaint Counsel's economic expert. (*See* RRFF 2868).

2868. An appropriate assumption regarding the evolution of the world had Rambus disclosed would take into account the effect of changes in the world on the incentives of the firms making the decisions. For example, given the fact that when fixed alternatives were presented at JEDEC they generally included only one or two alternatives, it would be highly unlikely that JEDEC would have chosen a large number of CAS latencies and burst lengths had JEDEC chosen the fixed CAS latency and fixed burst length alternatives. (McAfee, Tr. 11247 ("Given my understanding of the DRAM marketplace and in particular the dominance of a single standard that we've referred to, I would be highly surprised if the outcome of the marketplace was for all twelve of those possibilities to actually be offered in fact. Now, I wouldn't go as far as to say that only one of the twelve would be offered, although that's a possibility, and it's a possibility that was suggested to me by Desi Rhoden, but instead that not all twelve would be offered."); CCFF 2138, 2142-143, 2150-153, 2243-244, 2248-250).

Rambus's Response to Finding No. 2868:

The proposed finding exposes yet another fundamental flaw in the analysis of Complaint Counsel's economic expert. First, the proposed finding rests on the erroneous assumption that JEDEC is a surrogate for buyer preferences and for the market. (*See* RRFF 2769). Second, Complaint Counsel's economic expert is effectively contending that acceptable alternatives include those that permit less performance at the same or greater cost. In the example of a fixed

latency and fixed burst length alternative, the evidence shows that it would cost more to get the same performance as the Rambus technologies. (*See* RPF 969-88). Complaint Counsel's expert suggests that JEDEC would have accepted fewer latency and burst length options. This is contrary to the evidence (*see* RPF 810-35, 904-21), but assuming it were the case, the result would be that users of DRAM would have less performance for the same cost. In other words, Complaint Counsel's economic expert advocates "alternatives" that give less in cost-performance terms, rendering his analysis of alternatives seriously flawed.

2869. One effect of Dr. Rapp's assumption that technology would have evolved the same way it did even if Rambus had disclosed its patents is to overstate the costs of some of the alternatives. (McAfee, Tr. 11248 ("Well, in the choice of -- to be specific, in the choice of fixed CAS latency and fixed burst length, Dr. Rapp has assumed that all twelve of the theoretical combinations would be offered. If instead only two of those combinations were actually offered by the marketplace, then in fact he's overstated the costs by a factor of six.")).

Rambus's Response to Finding No. 2869:

The proposed alternative is directly contrary to the evidence. First, Dr. Rapp did not assume "that all twelve of the theoretical combinations would be offered." Instead, he based his analysis on Mr. Guilhufe's cost estimates, which did not account for the costs of all twelve theoretical combinations. (Guilhufe, Tr. 9601). Second, Dr. Rapp's calculations properly assume that alternatives need to reach the same or similar performance level as the Rambus technologies. (*See* RRFF 2868).

2870. Another effect of Dr. Rapp's assumption, that technology would have evolved the same way it did even if Rambus had disclosed its patents, is that assumption apparently led Dr. Rapp to erroneously ignore asynchronous alternatives entirely. Dr. Rapp apparently dismissed asynchronous alternatives entirely as not having sufficient potential for growth. However had an asynchronous alternative been chosen by JEDEC after Rambus disclosed there would have been an incentive on firms to invest in the further development of that technology. (McAfee, Tr. 11248-249 ("And my understanding of JEDEC behavior is that the burst EDO is actually a serious contender to SDRAM as an alternative and burst EDO is an asynchronous

alternative. Had burst EDO been selected by the marketplace over SDRAM, the likely outcome from an economic perspective is that there would have been further investment in the asynchronous alternatives and that the marketplace might never have gone to synchronous DRAMs at all."); CCFF 568-569, 2233).

Rambus's Response to Finding No. 2870:

The proposed finding is not supported by the weight of the evidence, which shows that asynchronous technology would not have been accepted by the market as a substitute. (*See* RPF 893-902).

2871. Dr. Rapp's analysis is not robust to relatively small changes in the assumptions and changing his assumptions can overturn his conclusion regarding commercial viability. (McAfee, Tr. 11230; *see* DX0364).

Rambus's Response to Finding No. 2871:

The proposed finding is misleading and incomplete. Complaint Counsel's economic expert testified that Dr. Rapp's analysis, as all economic analyses, is dependent on the factual underpinnings for his assumptions: "it's a factual matter which assumptions are actually right." (McAfee, Tr. 11230). The evidence confirms Dr. Rapp's assumptions.

2872. Because he failed to analyze alternatives that Dr. Soderman claimed infringes a Rambus patent, Dr. Rapp excluded what he would have calculated to be the least costly alternative to programmable CAS latency. (McAfee, Tr. 11252; *see* DX0365).

Rambus's Response to Finding No. 2872:

The proposed alternative is misleading and contrary to the evidence. The evidence shows that certain of the alternatives described by Complaint Counsel's economic expert infringe Rambus's patents. (*See* RPF Section IX.B.3.c, IX.B.4.c). Complaint Counsel's economic expert admitted on cross-examination that the presence of patents covering an alternative could overturn his determination that a technology is "commercially viable." (McAfee, Tr. 7582-85). Thus, he

admitted that evidence that an alternative is covered by a patent renders it not an acceptable, noninfringing alternative. Yet he made no effort to determine whether such patents existed, nor did he deal with the evidence that some of his purported alternatives were in fact covered by patents. (*Id.*)

2873. Because he failed to analyze alternatives that Dr. Soderman claimed infringes a Rambus patent, Dr. Rapp excluded what he would have calculated to be the second least costly alternative to programmable burst length. (McAfee, Tr. 11254; *see* DX0365).

Rambus's Response to Finding No. 2873:

The proposed alternative is misleading and contrary to the evidence. (*See* RRFF 2872).

2874. As a consequence of his failure to analyze technologies that Dr. Soderman claimed to infringe Rambus patents, Dr. Rapp failed to identify two combinations of alternatives that his methodology indicates JEDEC would have preferred to the current SDRAM standard with the current Rambus royalties. (McAfee, Tr. 11256-258 ("So this slide has substituted the programming in read command, which is an allegedly infringing technology, for programmable CAS latency. That was the least expensive technology according to ... Mr. Geilhufe.... And that comes out as a total cost of .21 percent, which is substantially less than ... the alleged ... SDRAM royalty that Dr. Rapp used in his testimony. As a result, the consequence is that the conclusion that Dr. Rapp had found is in fact overturned."); *see* DX0366).

Rambus's Response to Finding No. 2874:

The proposed alternative is misleading and contrary to the evidence. (*See* RRFF 2872).

2875. Because he failed to analyze an alternative that Dr. Soderman at one point claimed infringes a Rambus patent, Dr. Rapp excluded what he would have calculated to be the least costly alternative to dual-edged clocking. (McAfee, Tr. 11259-260; *see* DX0365).

Rambus's Response to Finding No. 2875:

The proposed alternative is misleading and contrary to the evidence. (*See* RRFF 2872).

2876. As a consequence of his failure to analyze technologies that Dr. Soderman at one point claimed to infringe Rambus patents, Dr. Rapp failed to identify a combination of alternatives that his methodology indicates JEDEC would have preferred to the current DDR SDRAM standard with the current Rambus royalties. (McAfee, Tr. 11263-264 ("so with this change in assumptions but otherwise following exactly Dr. Rapp's logic, the conclusion is the

reverse of his conclusion, which is to say a rational manufacturer would prefer the alternatives rather than the Rambus license.")); *see* DX0367).

Rambus's Response to Finding No. 2876:

The proposed alternative is misleading and contrary to the evidence. (*See* RRFF 2872).

2877. The effect of Dr. Rapp failing to consider asynchronous alternatives for the technologies in the JEDEC standard also led Dr. Rapp to exclude "toggle mode" which he would have calculated to be a low cost alternative to dual-edged clocking. (McAfee, Tr. 11265-266).

Rambus's Response to Finding No. 2877:

The proposed finding is not supported by the weight of the evidence; "toggle mode" is not an alternative for dual-edge clocking, asynchronous technologies were not acceptable alternatives. (*See* RPF 893-902, 1067-77). Even researchers at the the developer of the technology, IBM, concluded that toggle mode was "very big, very hot, and very nonstandard," which was "disastrous" for a commodity product. (RX 2099-7 at 16).

2878. As a consequence of his failure to analyze toggle mode, Dr. Rapp failed to identify a combination of alternatives that his methodology indicates JEDEC would have preferred to the current DDR SDRAM standard with the current Rambus royalties. (McAfee, Tr. 11266 ("The toggle mode as an alternative for dual-edged clocking is sufficiently inexpensive at 12 cents that it would still leave the overall cost less than the assumed DDR royalty.")).

Rambus's Response to Finding No. 2878:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 2877).

2879. Productivity gains and its effect on the cost of the technologies does not appear to have been considered by either Mr. Geilhufe in arriving at his estimates or Dr. Rapp in making his calculations. (McAfee, Tr. 11267-268; *see* DX0368).

Rambus's Response to Finding No. 2879:

The proposed finding is misleading and contrary to the evidence. Mr. Geilhufe specifically testified that his cost estimates took into account productivity gains: "Further, I had

to make an assumption as to where in the manufacturing life cycle this product stood; that is, is it just starting or is it going already well down the learning curve? And I – my model assumes that the product is already well in – down the learning curve. *It has, if you will, saturated its cost improvement already*." (Geilhufe, Tr. 9562) (emphasis added). Similarly, Dr. Rapp specifically testified that his analysis takes into account the issue of cost improvements:

> Q. Dr. Rapp, I want to ask you a few more questions about some of these cost numbers before we leave them, and let me ask you first whether you have an understanding as to whether DRAM manufacturing costs are in general constant over the life of a particular architecture or specification.
>
> A. They are not.
>
> Q. What is your understanding in that regard?
>
> A. My understanding is that the DRAM manufacturing costs decline steeply over a product life cycle of a particular DRAM architecture.
>
> Q. Does your understanding in that regard cause you to question at all the usefulness, for purposes of your analysis, of Mr. Geilhufe's cost estimates?
>
> A. No.
>
> Q. Why not?
>
> A. Because Mr. Geilhufe was specific about the fact that he produced his cost estimates on the basis of a mature product. That means

one that in his terms and in the terms of the industry has gone down the learning curve and experienced cost reductions.

(Rapp, Tr. 9854).

Further, not all of the costs associated with the purported alternatives are subject to productivity gains:

Q. And is it your understanding that all of the different costs in question here would be ones that would be reduced over time or are some ones that do not experience that change?

A. No. That's a second reason for not being concerned about these life-cycle cost declines. Things like inventory costs, for example, aren't subject to those declines. Those declines come from yield improvement and things – and improvement in manufacturing technology.

(Rapp, Tr. 9854-55). On cross-examination, Complaint Counsel's economic expert agreed with this conclusion. (McAfee, Tr. 11365).

2880. Even granting his methodology and his other assumptions as being correct, if Dr. Rapp is incorrect in his assumption of no productivity gains, the existence of productivity gains can change Dr. Rapp's analysis, depending on the extent of productivity gains. (McAfee, Tr. 11271-272).

Rambus's Response to Finding No. 2880:

The proposed finding is misleading. Both Dr. Rapp and Mr. Geilhufe specifically accounted for productivity gains in producing their analysis. (*See* RRFF 2279). There is no basis to apply *further* productivity gains to Dr. Rapp's analysis.

2881. Substituting alternative cost figures that account for productivity gains reverses the outcome of Dr. Rapp's analysis to both SDRAM and DDR SDRAM. (McAfee, Tr. 11272; *see*

DX0368).

Rambus's Response to Finding No. 2881:

The proposed finding is misleading. Both Dr. Rapp and Mr. Geilhufe specifically accounted for productivity gains in producing their analysis. (*See* RRFF 2279). There is no basis to apply *further* productivity gains to Dr. Rapp's analysis.

2882. If the assumption is made that productivity gains are thirty percent per year then both the least costly and most costly combinations of alternatives described by Dr. Rapp become less costly than the current JEDEC SDRAM standard with the Rambus royalty. (McAfee, Tr. 11272-273 ("what I've done is replicate his analysis but with a 30 percent productivity increase, annual 30 percent productivity increase, to examine what that would do to ... his results for SDRAM. And as you can see,... even the most costly alternative with a 30 percent annual productivity increase winds up being cheaper than the Rambus alleged royalty."); *see* DX0369).

Rambus's Response to Finding No. 2882:

The proposed finding is misleading. Both Dr. Rapp and Mr. Geilhufe specifically accounted for productivity gains in producing their analysis. (*See* RRFF 2279). There is no basis to apply *further* productivity gains to Dr. Rapp's analysis. Further, the thirty percent productivity gain was hand-picked by Complaint Counsel's expert to show a different outcome. He admitted in cross-examination that a ten percent productivity gain would *not* change the conclusions. (McAfee, Tr. 11379). In addition, on cross-examination, Complaint Counsel's economic expert admitted that the thirty percent "productivity gain" he applied was on a cost-per-bit basis. (McAfee, Tr. 11362). The cost estimates given by Mr. Geilhufe were on a cost-per-unit (i.e., cost-per-part) basis. (*See, e.g.*, Geilhufe, Tr. 9579). Because Complaint Counsel's economic expert's "productivity gain" is on a cost-per-bit basis, it can be wholly unrelated to improvements in manufacturing costs. The number of bits is related to the density of a memory device. As DRAM technology matures, manufacturers have increased the density of DRAM products (e.g.,

512Mb to 1Gb). Increased density (i.e., a higher number of bits per DRAM) decreases cost per bit even if there are *no* manufacturing cost improvements. (McAfee, Tr. 11363). For instance, doubling the density of a DRAM could drive the cost per bit down by 50% even if manufacturing costs stayed constant. (*Id.*) Further, Complaint Counsel's economic expert admitted that he could not testify that a productivity gain would apply to any particular of the additional costs associated with his alternatives. (McAfee, Tr. 11363-64 ("I'm not saying it directly applies to each individual technology")). In fact, Complaint Counsel's economic expert admitted that a thirty percent productivity gain would not apply to many of the specific costs of his alternatives:

Q. You do understand that Geilhufe's costs include costs of pins; correct?

A. That's one of the costs, yes.

Q. Costs of packaging; correct?

A. That's -- yes.

Q. Inventory costs; correct?

A. Correct.

Q. Now, for a particular product, a particular DRAM, you don't really think, do you, that the costs of the pins for that product are going to go down 30 percent a year every year for eight years?

A. I actually have looked up what the cost of pins to have been and it has not fallen by 30 percent a year. It has fallen, however.

Q. And you wouldn't expect the costs of packaging to go down 30 percent a year, would you?

A. That's my understanding, packaging has not gone down 30 percent a year.

Q. And you wouldn't expect inventory costs to go down 30 percent a year either, would you?

A. I would be surprised if they did.

(McAfee, Tr. 11364-65).

2883. If the assumption is made that productivity gains are thirty percent per year then both the least costly and most costly combinations of alternatives described by Dr. Rapp become less costly than the current JEDEC DDR SDRAM standard with the Rambus royalty. (McAfee, Tr. 11276-277; *see* DX0370; CCFF 95-98).

Rambus's Response to Finding No. 2883:

The proposed finding is misleading and unfounded. (*See* RRFF 2882).

2884. Dr. Rapp relies on the cost estimates of Mr. Geilhufe to the exclusion of lower cost estimates made by industry participants. If Dr. Rapp instead relied on the cost estimates of industry participants, then his conclusions would be reversed. (McAfee, Tr. 11278 ("The accuracy of Dr. Rapp's conclusions is only as good as the underlying assumptions. And in particular, if the cost assumptions are changed, are lowered, then his conclusions would be reversed.")). For example, Mr. Geilhufe thought than an on-chip PLL would cost $3.80, but there was testimony that such PLLs only cost one dollar. (CCFF 2343).

Rambus's Response to Finding No. 2884:

The proposed finding is not supported by the weight of the evidence, which shows that Mr. Geilhufe's cost estimate for the on-module PLL was accurate. (*See* RRFF 2343).

3. Cluster Market.

2885. In addition, it is analytically useful, as a matter of convenience, to consider a "cluster" market. (McAfee, Tr. 7390-92; *see* DX0210-11). A "cluster" market, in this case, would consider each of the four relevant product markets as a collection, based on the logic that the products are used in the same products, though strictly speaking they are not substitutes for one another. (McAfee, Tr. 7390-92).

Rambus's Response to Finding No. 2885:

The proposed finding is unfounded as it is subject to the flaws in the market definition analysis done by Complaint Counsel's economic expert. (*See* RRFF 2764, 2769).

2886. Here, the "cluster" market is defined as the synchronous DRAM technology market. (McAfee, Tr. 7390-91 *see* DX0210).

Rambus's Response to Finding No. 2886:

The proposed finding is unfounded as it is subject to the flaws in the market definition analysis done by Complaint Counsel's economic expert. (*See* RRFF 2764, 2769).

2887. In addition, asynchronous designs were relevant alternatives through 1995 and probably thereafter as an alternative in the cluster market defined as synchronous DRAM technology. (McAfee, Tr.7386; *see* DX0209).

Rambus's Response to Finding No. 2887:

The proposed finding is unfounded as it is subject to the flaws in the market definition analysis done by Complaint Counsel's economic expert. (*See* RRFF 2764, 2769). The proposed finding is also not supported by the weight of the evidence, which shows that asynchronous technologies were not acceptable alternatives. (*See* RPF 893-902, 1067-77).

2888. Asynchronous DRAM designs were price constraining alternatives to DRAM designs. (McAfee, Tr. 7387-89).

Rambus's Response to Finding No. 2888:

The proposed finding is unfounded and misleading. First, even weak economic substitutes can be "price constraining." (*See* RRFF 2764). Second, the weight of the evidence shows that asynchronous technologies were not acceptable alternatives. (*See* RPF 893-902, 1067-77).

2889. Asynchronous designs would have been more successful if engineering effort had

not been diverted away from them by the choice of JEDEC to standardize SDRAM. (McAfee, Tr. 7388; CCFF 568-569, 2233).

Rambus's Response to Finding No. 2889:

The proposed finding is misleading and contrary to the evidence. The weight of the evidence shows that asynchronous technologies were not acceptable alternatives and could not, by their very nature, have been improved to match the performance of synchronous technologies. (*See* RPF 893-902, 1067-77).

C. The Relevant Geographic Market Is the World.

2890. The relevant geographic market for each relevant product market is the world. (McAfee, Tr. 7393; *see* DX0212).

Rambus's Response to Finding No. 2890:

Rambus has no specific response.

2891. The relevant geographic market for each relevant product market is the world because buyers of technology typically do not care about the geographic source of technology. (McAfee, Tr. 7393-95; *see* DX0212).

Rambus's Response to Finding No. 2891:

Rambus has no specific response.

2892. The relevant geographic market for each relevant product market is the world because technologies tend to be licensed worldwide. (McAfee, Tr. 7393-95; *see* DX0212).

Rambus's Response to Finding No. 2892:

Rambus has no specific response.

2893. The relevant geographic market for each relevant product market is the world because technologies tend to flow across national borders. (McAfee, Tr. 7393-95; *see* DX0212).

Rambus's Response to Finding No. 2893:

Rambus has no specific response.

2894. The relevant geographic market for each relevant product market is the world because the downstream products are produced and used world-wide. (McAfee, Tr. 7393-95; *see* DX0212; CCFF 3189-198).

Rambus's Response to Finding No. 2894:

Rambus has no specific response.

2895. The relevant geographic market for each relevant product market is the world because the transportation costs of both technology and DRAMs are negligible. (McAfee, Tr. 7393-95; *see* DX0212).

Rambus's Response to Finding No. 2895:

Rambus has no specific response.

2896. Technology markets tend to be worldwide markets. (McAfee, Tr. 7393-94).

Rambus's Response to Finding No. 2896:

Rambus has no specific response.

2897. Because transportation costs are low, DRAM is also a world-wide market. (McAfee, Tr. 7394; CCFF 3193-194, 3198).

Rambus's Response to Finding No. 2897:

Rambus has no specific response.

D. Rambus Has Monopoly Power in the Relevant Markets.

2898. Monopoly power is the durable power of a company to maintain prices substantially above competitive levels and is a strong form of market power. (McAfee, Tr. 7419-20; *see* DX0216). By durable, economists mean that market power may be exercised for a significant period of time. It is long lasting. (McAfee, Tr. 7420).

Rambus's Response to Finding No. 2898:

Rambus has no specific response.

2899. Rambus possesses monopoly power in each of the four relevant technology markets, and it also possesses monopoly power in the cluster market. (McAfee, Tr. 7420-21).

Rambus's Response to Finding No. 2899:

The proposed finding is not supported to the extent that the market definition analysis done by Complaint Counsel's economic expert is flawed. (*See* RRFF 2764, 2769).

2900. It is Dr. Rapp's view that Rambus today possesses market power in each of the relevant markets defined by Professor McAfee. (Rapp, Tr. 10046).

Rambus's Response to Finding No. 2900:

The proposed finding is incomplete. Dr. Rapp testified, "My opinion is that the market power that Rambus possesses in these four technologies arises solely out of the distance between the cost-performance qualities of the Rambus technologies and the next best alternative." (Rapp, Tr. 10260).

2901. The source of Rambus's monopoly power derives from the fact that the relevant technologies have been incorporated into the JEDEC DRAM standards. (McAfee, Tr. 7432; *see* DX0218).

Rambus's Response to Finding No. 2901:

The proposed finding is not supported by the weight of the evidence. First, the economic conditions for standardization to enhance Rambus's market power do not exist. (*See* RPF 1503-30). Standardization can only enhance market power where compatibility requirements are exceedingly high and there exist equal or superior alternatives that are excluded by standardization. (Rapp, Tr. 9799-800). The coexistence of multiple DRAM standards, the success of non-JEDEC standards, and the fact that computer systems using different DRAM many still be compatible shows that compatibility requirements in the DRAM industry are not exceedingly high. (*See* RPF 1509-23). Moreover, the evidence shows that Rambus's technologies were superior to alternatives; therefore, standardization by JEDEC did not enhance

Rambus's market power. (Rapp, Tr. 9901-02; RPF Section IX).

Second, the evidence shows that JEDEC would have incorporated Rambus's technologies into the SDRAM and DDR standards even if Rambus had made the additional disclosures that Complaint Counsel allege should have been made. The evidence shows that JEDEC preferred Rambus's technologies over all others and that the additional disclosures would not have changed that revealed preference. (*See* RPF 1532; Section IX.A). The evidence also shows that there were no cost-performance equivalent noninfringing alternatives; rational JEDEC members would have selected Rambus's technologies accounting for Rambus's royalties. (*See* Rapp, Tr. 9907-09; RPF Section IX.B). An analysis of JEDEC's and Rambus's economic incentives and past behavior also shows that JEDEC would have incorporated the Rambus technologies even if Rambus had made the additional disclosures. (*See* RPF Section IX.C). This means that Rambus's alleged conduct did not enhance its market power. (Teece, Tr. 10312-13).

Third, the evidence shows that if there acceptable, noninfringing alternatives, the DRAM industry could switch to those alternatives. Switching costs are not so prohibitively high that DRAM manufacturers could not change to alternatives. (*See* RPF Section X.B.1). Nor are any coordination issues different from those routinely surmounted by the industry. (*See* RPF Section X.B.2). The ability of the industry to switch to noninfringing acceptable alternatives (if they existed) would dissipate any market power Rambus might have gained and prevent the exercise of monopoly power. (Rapp, Tr. 9902-03).

2902. Incorporation of the technologies in the JEDEC standards conferred monopoly power onto Rambus, because the JEDEC standards dominate the DRAM industry. (McAfee, Tr. 7428).

Rambus's Response to Finding No. 2902:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 2901).

2903. If the JEDEC standards have dominated the DRAM industry for most of the last ten years that would indicate that owning patents over the JEDEC standard was likely to confer monopoly power. (McAfee, Tr. 7427-28).

Rambus's Response to Finding No. 2903:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 2601, 2901).

2904. Market share statistics show that the JEDEC standards have dominated the DRAM industry for at least the last ten years. (McAfee, Tr. 7428; *see* DX0141; CCFF 267).

Rambus's Response to Finding No. 2904:

The proposed finding is misleading in that it treats "JEDEC standards" as monolithic. "JEDEC standards" include several incompatible DRAM standards (*e.g.*, EDO, SDRAM, DDR), and the term is sometimes used to include subgenerations of standards that were not developed by JEDEC (*e.g.*, PC100 and PC133 SDRAM). (*See, e.g.*, Gross, Tr. 2348-49 (PC66 is an Intel standard); Gross, Tr. 2348-56 (PC100 and PC133 were Intel standards). The statistics show that multiple DRAM standards, JEDEC and non-JEDEC, coexist at any given time. (*See* RPF Section X.A.1).

1. Indirect Evidence of Monopoly Power.

(A) Rambus Market Share.

2905. Programmable CAS latency using the mode register is a mandatory element of both the SDRAM and DDR SDRAM standards. (CCFF 562-563, 657).

Rambus's Response to Finding No. 2905:

Rambus has no specific response.

2906. Programmable burst length using the mode register is a mandatory element of both the SDRAM and DDR SDRAM standards.(CCFF 562-563, 657).

Rambus's Response to Finding No. 2906:

Rambus has no specific response.

2907. Dual-edged clocking of data is a mandatory element of the DDR SDRAM standard. (***CCFF*** 656).

Rambus's Response to Finding No. 2907:

Rambus has no specific response.

2908. PLL/DLL on the DRAM is a mandatory element of the DDR SDRAM standard. (***CCFF*** 655).

Rambus's Response to Finding No. 2908:

The proposed finding is not supported by the weight of the evidence, which shows that PLL/DLL on a DRAM is not necessary to comply with the performance requirements of the DDR standard. (*See* RRFF 655).

2909. Rambus claims that its patents cover each of these features. (***CCFF*** 1950-974).

Rambus's Response to Finding No. 2909:

Rambus has no specific response.

2910. Rambus has made it clear in negotiations with DRAM manufacturers and the manufacturers of other compatible components that it believes that its patents cover the SDRAM and DDR SDRAM standards. (***CCFF*** 1963-974).

Rambus's Response to Finding No. 2910:

Rambus has no specific response.

2911. Rambus's internal communications indicate that it believes that its patents cover the SDRAM and DDR SDRAM standards. (***CCFF*** 1951-1952; 2039-2042).

Rambus's Response to Finding No. 2911:

Rambus has no specific response.

2912. The JEDEC SDRAM and DDR SDRAM standards determined what features were required to be present in JEDEC-compliant DRAMs. (***CCFF*** 2905-906)

Rambus's Response to Finding No. 2912:

The proposed finding is not supported with respect to on-chip PLL/DLL. (See RRFF 2906).

2913. The percentage of total DRAM production in the world today that is subject to Rambus's patent claims is in the upper nineties. (McAfee, Tr. 7430; *see* DX0219, DX0141; ***CCFF*** 2039-2042).

Rambus's Response to Finding No. 2913:

Rambus has no specific response.

(B) The Industry is Locked In to the JEDEC SDRAM and DDR SDRAM Standards.

2914. The DRAM standards lead to monopoly power in the relevant technology markets. (McAfee, Tr. 11205).

Rambus's Response to Finding No. 2914:

The proposed finding is ambiguous in referring to "DRAM standards." If Complaint Counsel mean "JEDEC standards," the finding is certainly not supported by the weight of the evidence. (*See* RRFF 2901). The proposed finding is unsupported; standardization only increases market power when certain conditions are met – which are not present in the DRAM industry. (*See* RPF Section XII.B.1).

2915. Technologies that were viable in each of the relevant markets before the standards were set are no longer commercially viable because of the incorporation of the technologies into the dominant JEDEC standards. (CCFF 2542, 2546, 2918-922; McAfee, Tr. 7421).

Rambus's Response to Finding No. 2915:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 2901). The evidence shows that there were no acceptable, noninfringing alternatives to Rambus's technologies. (*See* RPF Section X.B).

2916. The DRAM industry is no longer capable of switching from the technologies in the SDRAM standard to alternatives because it is locked in to the current standard. (CCFF 2501-505).

Rambus's Response to Finding No. 2916:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section XI; RRFF 2501-505).

2917. The DRAM industry is no longer capable of switching from the technologies in the DDR SDRAM standard to alternatives because it is locked in to the current standard. (CCFF 2506-526).

Rambus's Response to Finding No. 2917:

The proposed finding is not supported by the weight of the evidence. (*See* RPF Section XI; RRFF 2506-526).

2918. Technologies that were viable substitutes for programmable CAS latency in the *ex ante* period are no longer viable because the industry is locked in to the JEDEC standards. (McAfee, Tr. 7459-61; *see* DX0187; CCFF 2543).

Rambus's Response to Finding No. 2918:

The proposed finding is not supported by the weight of the evidence, which shows that there were no acceptable, noninfringing alternatives *ex ante* (*see* RPF Section X.B.3.a) and that, if there were, the industry is not locked in to using Rambus technologies (*see* RPF Section XI).

2919. Technologies that were viable substitutes for programmable burst length in the *ex ante* period are no longer viable because the industry is locked in to the JEDEC standards. (McAfee, Tr. 7461-63; *see* DX0194; CCFF 2543).

Rambus's Response to Finding No. 2919:

The proposed finding is not supported by the weight of the evidence, which shows that there were no acceptable, noninfringing alternatives *ex ante* (*see* RPF Section X.B.3.b) and that, if there were, the industry is not locked in to using Rambus technologies (*see* RPF Section XI).

2920. Technologies that were viable substitutes for dual-edged clocking in the *ex ante* period are no longer viable because the industry is locked in to the JEDEC standard. (McAfee, Tr. 7463-64; *see* DX0200; CCFF 2544).

Rambus's Response to Finding No. 2920:

The proposed finding is not supported by the weight of the evidence, which shows that there were no acceptable, noninfringing alternatives *ex ante* (*see* RPF Section X.B.4.a) and that, if there were, the industry is not locked in to using Rambus technologies (*see* RPF Section XI).

2921. Technologies that were viable substitutes for on-chip PLL/DLL in the *ex ante* period are no longer viable because the industry is locked in to the JEDEC standard. (McAfee, Tr. 7464-65; *see* DX0207; CCFF 2545).

Rambus's Response to Finding No. 2921:

The proposed finding is not supported by the weight of the evidence, which shows that there were no acceptable, noninfringing alternatives *ex ante* (*see* RPF Section X.B.4.b) and that, if there were, the industry is not locked in to using Rambus technologies (*see* RPF Section XI).

2922. If there were commercially viable alternatives available, the industry would substitute to those rather than pay royalties to Rambus. The fact that such substitution has not taken place demonstrates the absence of commercially viable alternatives today. (McAfee, Tr. 7630, *in camera*).

Rambus's Response to Finding No. 2922:

The proposed finding is incomplete. Because switching costs and coordination issues do not prevent a change to alternatives technologies (*see* RPF Section IX), the evidence that the

industry has not switched to alternatives demonstrates that there were no acceptable, noninfringing alternatives at any time.

2923. Dr. Rapp has not calculated the switching costs that would be associated with changes to any other products other than DRAM products in the event that there were an effort to work around the Rambus patents through alternative JEDEC standards. (Rapp, Tr. 10127).

Rambus's Response to Finding No. 2923:

The proposed finding is misleading and incomplete. Dr. Rapp testified that he did not "calculate" these costs, but he testified that he could infer from the evidence that these costs are on the same order of magnitude as the costs that he calculated for a DRAM manufacturer – a few million dollars. (Rapp, Tr. 10128 ("I think it's appropriate to consider that but that it is also a fair inference that the order of magnitude of those costs are going to be the likes of which I have described in connection with my SDRAM example rather than the magnitudes that Professor McAfee spoke about when he talked about billion-dollar fabs and things like that.")). He further testified, "I haven't quantified those costs, but in my statement that switching costs are low, I haven't seen evidence to the contrary." (Rapp, Tr. 10129).

There is no evidence to the contrary. Complaint Counsel's economic expert admitted that he did not quantify any switching costs. (McAfee, Tr. 11356). He also admitted that the DRAM industry overcomes switching costs at a frequency of more than once a year:

> Q. You would agree, wouldn'' you, that there are switching costs incurred when you go from SDRAM to DDR?
>
> A. I agree with that.
>
> Q. And there are also switching costs incurred when you go from DDR to DDR-II?

A. I agree with that.

Q. And there would have been switching costs incurred if you went from SDRAM or from DDR to SLDRAM; correct?

A. There would have been.

Q. There also are switching charges incurred when you go from a PC66 to a PC100 or a PC133, aren't there?

A. There are some switching -- you said charges, but there are some switching costs, would be the ordinary term.

Q. And there are switching costs incurred when you go from a 64-meg to a 128-meg to a 256-meg of any particular DRAM design?

A. There are certainly switching costs incurred in those transitions.

Q. The switching costs we've talked about between SDRAM to DDR, for example, and within various SDRAM and DDR product generations are incurred with a frequency of more often than once a year, aren't they?

A. There are some kinds of switching costs that are incurred with a frequency more often than once a year.

(McAfee, Tr. 11357-58).

2924. Dr. Rapp has not considered what the costs of changing standards might be to chipset manufacturers, microprocessor manufacturers, socket manufacturers or anyone else. (Rapp, Tr. 10127 ("I have considered that coordination efforts and changes in an industry as dynamic as the computer industry take place all the time, and I infer from that that costs to these other makers of complementary goods would for the most part be accomplished within the framework of continually changing your products.")).

Rambus's Response to Finding No. 2924:

The proposed finding is misleading and contrary to the evidence. (*See* RRFF 2923).

2925. Dr. Rapp's basis to speak to the relative magnitude of the costs that would be borne by non-DRAM manufacturers if there was an attempt to develop alternative standards to work around Rambus' patents is "the understanding that circuitry is subject to continual change in the computer industry and that switching costs are, generally speaking, relatively low when there is -- when change is routine, in the same way as in the DRAM industry." (Rapp, Tr.10128).

Rambus's Response to Finding No. 2925:

The proposed finding is misleading and incomplete. (*See* RRFF 2923).

2926. Dr. Rapp has not quantified the costs that the manufacturers of products other than DRAMs would experience if the JEDEC standards were changed to work around Rambus' technologies.(Rapp, Tr.10128-129).

Rambus's Response to Finding No. 2926:

The proposed finding is misleading and incomplete. (*See* RRFF 2923).

2927. Dr. Rapp is aware that Andy Bechtelsheim testified in this case, but did not read the testimony. (Rapp, Tr.10129).

Rambus's Response to Finding No. 2927:

Rambus has no specific response.

2928. In assessing the lock-in question, Dr. Rapp has, with one exception, not considered the specific type of change that would have to be made to go to any given alternative that's been raised as a possibility in the case. (Rapp, Tr. 10140-141 ("I -- the -- I haven't considered, with the exception of the example that I gave, anything other than the general fact that it would be circuitry design changes.")).

Rambus's Response to Finding No. 2928:

The proposed finding is misleading and incomplete. The context of the cited testimony is "what types of non-DRAM devices might have to be changed in order to accommodate a change in the JEDEC standards." (Rapp, Tr. 10140). Though Dr. Rapp testified that he did not consider

the specific type of change to non-DRAM devices to go to alternatives, Dr. Rapp testified that he could nonetheless infer the magnitude of switching costs from his calculations and the other evidence. (Rapp, Tr. 10128).

2929. In considering how long it would take either the DRAM industry as a whole, or multiple participants in the DRAM industry, to agree upon a single or uniform approach for working around Rambus' patents if that were to be attempted, Dr. Rapp assumed that would take no more time than normal redesign efforts take. (Rapp, Tr. 10148 ("As I've said before, this is an industry, both the DRAM industry and the larger components industry, where technical change happens with high frequency and redesigns occur with high frequency, and I took for my assumption the fact that the changes that would be necessary to create and implement new designs involving the substitution of these alternatives could be done in a time frame of normal redesigns.")).

Rambus's Response to Finding No. 2929:

Rambus has no specific response.

2930. When Dr. Rapp refers to normal redesigns in the DRAM industry, he is referring either to process changes, redesigns in connection with die shrinks, or other sorts of changes. (Rapp, Tr. 10148).

Rambus's Response to Finding No. 2930:

Rambus has no specific response.

2931. In evaluating how long it would take either the DRAM industry as a whole, or multiple participants in the DRAM industry, to agree upon a single or uniform approach for working around Rambus' patents, Dr. Rapp did not consider separately the time it would take multiple DRAM participants to agree upon a uniform approach for working around Rambus' patents, if they were to seek to do that. (Rapp, Tr. 10148-149).

Rambus's Response to Finding No. 2931:

The proposed finding is misleading and incomplete. Dr. Rapp testified that his opinion that the time necessary to switch to alternatives would be similar to that for a normal redesign included *both* the time necessary for agreement and for implementation:

> Q. And again, just to make it clear we're talking about the same

thing, my question was solely focused on the time it would take for multiple DRAM participants to agree upon an approach to working around Rambus' patents, not to implement it but to agree upon it. And did you understand, in your testimony earlier, did you understand my question that way?

A. I thought you were speaking of both agreement and implementation.

(Rapp, Tr. 10148).

Dr. Rapp simply testified that he did not have a opinion on the time it would take to reach agreement, separate and apart from the time it would take to implement the alternatives. (*Id.*)

2932. Dr. Rapp does not know how long it took JEDEC to agree upon the SDRAM specification from the start of the process to the end of the process. (Rapp, Tr. 10149).

Rambus's Response to Finding No. 2932:

The proposed finding is irrelevant. (*See* RRFF 2735).

2933. Dr. Rapp believes that it took JEDEC something on the order of about three years to agree upon the DDR specification from the start of the process to the end of the process. (Rapp, Tr. 10149).

Rambus's Response to Finding No. 2933:

The proposed finding is irrelevant. (*See* RRFF 2735).

2934. Dr. Rapp does not have any specific knowledge as to what features other than dual-edged clocking and on-chip PLL/DLL were added when JEDEC moved from SDRAM to the DDR SDRAM standard. (Rapp, Tr. 10152).

Rambus's Response to Finding No. 2934:

The proposed finding is misleading and incomplete. While Dr. Rapp did not have

personal knowledge of the specific features that were added to DDR, he testified that "I have a sense that although the two are connected generations of DRAMs that the change was very substantial, that it was a major effort because every single feature of the chip, except for the basic memory array, needed to be considered as to whether it would change or whether it would remain the same. That's different from changing a single attribute or two attributes of a standard." (Rapp, Tr. 10149).

2935. Dr. Rapp did not, as part of his lock-in analysis seek to separately quantify any costs associated with the period of time it would take to either agree upon an approach for working around Rambus' patents or to implement such approach. (Rapp, Tr. 10154).

Rambus's Response to Finding No. 2935:

The proposed finding is misleading and incomplete. Dr. Rapp testified that he did not *separately* quantify these costs "[f]or the reasons [he] gave before," (Rapp, Tr. 10154), which were that he did not consider reaching an agreement and implementation separately (Rapp, Tr. 10148), and he inferred the magnitude of the combined costs from the evidence (Rapp, Tr. 10128).

2936. Dr. Rapp agrees that the opportunity costs that might arise in the course of DRAM manufacturers or other component suppliers seeking to work around Rambus' patents is the opportunity cost of engineers and devotion of their activities to working around the Rambus patents. (Rapp, Tr. 10154-155).

Rambus's Response to Finding No. 2936:

Rambus has no specific response.

2937. In assessing lock-in Dr. Rapp did not take into account any testimony that was given by DRAM industry participants during the trial relating to the subject of opportunity costs associated with engineers. (Rapp, Tr. 10155).

Rambus's Response to Finding No. 2937:

The proposed finding is misleading and incomplete to the extent that it implies Dr. Rapp did not take into account opportunity costs. Dr. Rapp testified that his analysis included a quantification of those costs. (Rapp, Tr. 10156).

(C) Barriers to Entry

2938. Barriers to entry are a requirement to a finding of monopoly power. (McAfee, Tr. 7421-422). Barriers to entry allow a firm to increase prices without prompting entry of other firms into the market, which would force the prices back down. (McAfee, Tr. 7421-22, 7465).

Rambus's Response to Finding No. 2938:

Rambus has no specific response.

2939. If, when a firm increases prices, other firms enter that firm's market in a way that forces prices back down, then the firm does not have monopoly power. (McAfee, Tr. 7420). Exploitation of a temporary circumstance is not generally considered to be monopoly power, the power to raise prices must be durable to be considered monopoly power. (McAfee, Tr. 7420).

Rambus's Response to Finding No. 2939:

Rambus has no specific response.

2940. There are significant barriers to entry facing proponents of alternative technologies to the Rambus technologies. (McAfee, Tr. 7467-468).

Rambus's Response to Finding No. 2940:

The proposed finding is unsupported. On cross-examination, Complaint Counsel's economic expert admitted that many of the entry barriers that he testified about were for the DRAM manufacturing market:

> Q. When you talked yesterday about barriers to entry and used DX-226 to help illustrate your testimony, were you referring then to barriers to entry in the DRAM manufacturing business?

A. When I used scale, I was referring to the DRAM manufacturing business.

Q. And when you used sunk costs, were you referring to the DRAM manufacturing business?

A. Yes.

Q. And when you used strong learning curve, were you referring to the DRAM manufacturing business and the manufacturing of related components?

A. Yes.

(McAfee, Tr. 7720-21).

Entry barriers to the DRAM manufacturing market have nothing to do with entry barriers in the DRAM technology market. For instance, the evidence shows that new DRAM technologies are routinely introduced. (*See, e.g.*, RPF Section X.A). It has never taken the entry of a new DRAM manufacturer for these new technologies to enter the market.

2941. Those barriers to entry are the effects on entry of: scale, user switching costs, strong learning curve, sunk costs, and patents. (McAfee, Tr. 7468; *see* DX0226).

Rambus's Response to Finding No. 2941:

The proposed finding is unsupported. (*See* RRFF 2940).

(1) Economies of Scale.

2942. Economies of scale relates to the effect where per unit costs fall as more of a product is manufactured. (McAfee, Tr. 7189).

Rambus's Response to Finding No. 2942:

Rambus has no specific response.

2943. The DRAM industry is an example of an industry with significant economies of scale, part of which flow out of large capital requirements. (McAfee, Tr. 7189; CCFF 104).

Rambus's Response to Finding No. 2943:

The proposed finding is incomplete. Economies of scale in the DRAM industry are at the plant level. (Rapp, Tr. 9893).

2944. As a result of economies of scale, the costs of the DRAM product that has the largest share of demand tends to have its costs fall faster than products with lesser shares. This fact encourages a single product to become the dominant product and to become the industry standard. (McAfee, Tr. 7223, 7225).

Rambus's Response to Finding No. 2944:

The proposed finding is not supported by the weight of the evidence. While there is testimony from a non-DRAM manufacturer that DRAM manufacturers tend to implement cost reductions first to their largest volume products, Complaint Counsel's economic expert admitted that increased performance drives transitions in the DRAM industry. (McAfee, Tr. 11347-48). Further, the evidence shows that multiple DRAM standards with substantial market coexist in the DRAM market. (RPF 1267-77). This evidence means that economies of scale in the DRAM industry are not so great as to compel a single standard. (Rapp, Tr. 9893).

2945. There are two types of economies of scale relevant to the DRAM industry: first, the fact that the minimum efficient scale of a fab is very large; and, second, the fact that as the industry gets larger, the average costs of related components falls. (McAfee, Tr. 7609-10).

Rambus's Response to Finding No. 2945:

Rambus has no specific response.

2946. The first type of economies of scale is where a firm experiences reductions in cost as it increases its output because of large capital requirements. (McAfee, Tr. 7189). One example of the capital requirements that is relevant to economies of scale are the costs of doing a "die shrink" to reduce the costs of a DRAM. (McAfee, Tr. 7217 ("And so the effect of this is, from an economic perspective, if you've got two products that you might apply a die shrink to,

you're going to apply it to the product that you're producing the most of. That is to say, the product... that you're producing the most of will be the product you shrink first and the product you shrink most."); CCFF 105-106).

Rambus's Response to Finding No. 2946:

Rambus has no specific response.

2947. Another example of the capital requirements that is relevant to economies of scale is the cost of design testing and qualification of new DRAM chips. (McAfee, Tr. 7222-23 ("[W]hen design, testing and qualification costs are large, you want to try to use a single or not too many different flavors or varieties of DRAM so that I don't have to go through the whole design, testing and qualification process over and over and over again.")).

Rambus's Response to Finding No. 2947:

Rambus has no specific response.

2948. The second type of economies of scale is also called "network externality." (McAfee, Tr. 7610-11). This relates to the effect that as the volume of a DRAM increases, the costs to produce compatible components will fall as well. (McAfee, Tr. 7472-73 ("[T]he larger the volume that is produced of a chip, the lower the cost per unit not just of the chip itself but also of the complementary goods. That is, the large investments made to produce complementary goods gets amortized over a larger volume of product, which lowers their per unit costs, which makes it even more attractive to the marketplace."), 7611).

Rambus's Response to Finding No. 2948:

The proposed finding is misleading to the extent that it implies that there are strong network effects in the DRAM industry. The evidence shows that there are not. (Rapp, Tr. 9895; RPF 1267-1307).

2949. This effect is one of the main reasons there tends to be one dominant DRAM standard, and it makes it difficult to displace an existing standard. (McAfee, Tr. 7473; CCFF 2605-630).

Rambus's Response to Finding No. 2949:

The proposed finding is not supported by the weight of the evidence. Though economies of scale are important in the DRAM industry, they are not so great as to drive to the industry to a

single dominant standard. (Rapp, Tr. 9893). Further, the evidence shows that multiple DRAM standards with significant market shares have coexisted in the market. (RPF 1267-77; RRFF 2601).

2950. Network effects occur when systems compatibility is required to give value to the product. (Rapp, Tr. 9792-93). Compatibility of DRAM parts is an important issue from the standpoint of DRAM manufacturers. (Rapp, Tr. 10093). When compatibility requirements are substantial, the market or formal standard-setting will allow only one dominant standard to prevail. (Rapp, Tr. 9791).

Rambus's Response to Finding No. 2950:

The proposed finding is misleading and incomplete. The proposed finding confounds parts compatibility (e.g., copiers and toner cartridges) and systems compatibility (e.g., a fax machine communicating with another fax machine). If *systems* compatibility requirements are high, there will typically be a dominant product standard. (Rapp, Tr. 9792-93). If only parts compatibility requirements are high, then there need not be a single standard. (Rapp, Tr. 9791). While DRAM compatibility requirements are important, these requirements are only parts compatibility, not systems compatibility. (Rapp, Tr. 9793-94).

2951. In circumstances where compatibility requirements are high, it is more likely that there will be only one dominant standard. (Rapp, Tr. 10096-97)

Rambus's Response to Finding No. 2951:

The proposed finding is misleading. In circumstances where *systems* compatibility requirements are high, it is more likely that there will be only one dominant standard. (Rapp, Tr. 9792-93). This is not the case for *parts* compatibility requirements such as those in the DRAM industry. (Rapp, Tr. 9793-94).

(2) Switching Costs.

2952. Another entry barrier is user switching costs. User switching costs refers to the costs of switching from the current standard. (McAfee, Tr. 7408, 7468).

Rambus's Response to Finding No. 2952:

The proposed finding is misleading. Several of the entry barriers previously identified applied only to the DRAM manufacturing market. (*See* RRFF 2940).

2953. One type of switching cost is the "opportunity cost" of switching to a new standard. (McAfee, Tr. 7456 ("And so the opportunity cost of creating a new standard and getting out from under the Rambus IP is that the engineering talent,... and all of the resources used are not available to other projects which may be profitable."); CCFF 2537).

Rambus's Response to Finding No. 2953:

Rambus has no specific response.

2954. A substantial volume of cost in the industry are switching costs. (McAfee, Tr. 7409). In addition, switching costs grow over time as the industry becomes progressively more locked in to the standard. (McAfee, Tr. 7435-37; *see* DX0221).

Rambus's Response to Finding No. 2954:

The proposed finding is not supported and is misleading in that it characterizes switching costs as a "substantial volume." Complaint Counsel's economic expert admitted on cross examination that he did not quantify switching costs. (McAfee, Tr. 7716-17, 11356). The evidence also shows that switching costs in the DRAM industry do not cause lock in to standards. (*See* RPF Section X).

2955. Professor Teece agrees that if switching costs are high, the resultant royalty rate will be higher than if switching costs are low. (Teece, Tr. 10707-08).

Rambus's Response to Finding No. 2955:

The proposed finding is misleading and incomplete. Professor Teece testified that the switching costs could lead to a difference between an *ex ante* royalty rate and an *ex post* royalty

rate if certain conditions existed (which are not present in this case):

> Q. Well, the way we got into all this was I was asking you wouldn't you agree that a world in which there are effective economic substitutes by comparison to a scenario in which there weren't would lead to – at the time in which the royalties were negotiated, it would lead to a lower royalty.
>
> A. If there are -- yes. If at the time that you engage in -- if there are negotiations and there are substitutes available that are equally effective and they're available, that will affect the royalty.
>
> Q. Okay. And the extent to which they affect the royalty could differ from the ex ante to the ex post period; right?
>
> A. Depending on the switching costs, yes.

(Teece, Tr. 10707).

2956. Standardization is a factor contributing to barriers to entry because the proponent of an alternative standard or an alternative technology must induce the rest of the industry to switch to the new standards. (CCFF 2547-549). So standardization creates a barrier to entry. (McAfee, Tr. 7458-59, 7470).

Rambus's Response to Finding No. 2956:

The proposed finding is misleading and incomplete. While standardization can under some circumstances create an entry barrier, the evidence in this case demonstrates that it does not do so in the DRAM industry. (*See* RPF Section X). The evidence shows that the DRAM industry routinely switches to new DRAM standards. (*See* RPF Section X.A).

2957. One type of switching cost are sunk costs, also known as specific investments. (McAfee, Tr. 7469). These costs are non-recoverable costs, and they have the effect of discouraging entry because an entrant faces a risk of the loss of these costs in the event of failure. (McAfee, Tr. 7469).

Rambus's Response to Finding No. 2957:

The proposed finding is not supported by the weight of the evidence. Sunk costs are irrelevant to switching costs unless those investments must be replaced to switch. As Dr. Rapp testified, "it is not the sunk costs that matter; it is the going-forward costs associated with substituting for whatever sunk investments are abandoned in some hypothetical." (Rapp, Tr. 10132; *see also* Rapp, Tr. 10135 ("there is a general proposition in economics that sunk costs are irrelevant for economic decision-making"); Teece, Tr. 10799 ("The key question is the switching costs. I mean, just about every industry has got sunk costs of one kind or another, so the key question is not whether there are sunk costs or not but what the switching costs are.")). As Professor Teece explained:

> Q. Just as a matter of economic principle, Professor Teece, if the sunk costs associated with an existing product can be used in connection with the alternative product, do those sunk costs enter into consideration of reasons why switching to alternatives may be more or less feasible?
>
> A. No.
>
> Q. Okay. Are there any costs that would be within the category of sunk costs that you would take into account in considering the feasibility of switching to alternatives if those costs were not required to be incurred in connection with the alternative and had not been incurred in connection with the prior technology?
>
> A. It's only the incremental piece that's implicated.

(Teece, Tr. 10800).

2958. The industry is characterized by such specific investments, particularly because of investments made by firms making complementary parts. (McAfee, Tr. 7296-297; *see* DX0164; CCFF 35-77; 2501-526).

Rambus's Response to Finding No. 2958:

The proposed finding is misleading. Specific investments and switching costs are not the same. (*See* RRFF 2660).

(3) Other Barriers to Entry.

2959. Another entry barrier is the strong learning curve characteristic of the DRAM industry. (McAfee, Tr. 7468) This barrier arises because an incumbent firm that has already gone down the learning curve has an advantage over a firm who has not. (McAfee, Tr. 7468).

Rambus's Response to Finding No. 2959:

The proposed finding is misleading. On cross-examination, Complaint Counsel's economic expert admitted that "the strong learning curve" was a barrier to entry into the DRAM manufacturing market, not the DRAM technology market. (McAfee, Tr. 7720-21). This barrier to entry is therefore not relevant to the issue of market power in the DRAM technology market. (*See* RRFF 2940).

2960. The presence of patents is also a contributor to an analysis of barriers to entry. (McAfee, Tr. 7469) Patents create a legal barrier to entry. (McAfee, Tr. 7470).

Rambus's Response to Finding No. 2960:

Rambus has no specific response.

2961. Patents nearly always confer market power when they protect the right of a technology that is selected as the standard technology either by a standard-setting organization or *de facto* by the marketplace. (Rapp, Tr. 9964).

Rambus's Response to Finding No. 2961:

The proposed finding is incomplete. Dr. Rapp also testified that standard-setting could

only confer market power if certain economic conditions exist. (*See* RRFF 2901).

2. Direct Evidence of Monopoly Power.

2962. Because of Rambus's conduct, it is able to receive substantially higher and discriminatory prices in the relevant technology markets. (McAfee, Tr. 7633, *in camera*).

Rambus's Response to Finding No. 2962:

The proposed finding in not supported by the weight of the evidence. First, Complaint Counsel's economic expert gave *no* specific testimony that Rambus's SDRAM rates were too high or discriminatory. Second, the evidence shows: (1) that Rambus's royalty rates are lower than the cost savings that Rambus's technologies realize over all non-infringing alternatives (*see* RPF Section IX.B.3.d, IX.B.4.d); (2) that had Rambus made the additional disclosures that Complaint Counsel claim should have been given, there would not have been any *ex ante* negotiations for licenses from Rambus (*see* RPF Section IX.D.2.b); and (3) that Rambus's royalty rates are reasonable in the sense that they are in the low end of the range of royalties accepted in the DRAM and semiconductor industries (*see* RPF Section XI.A). From both the standpoint of economics and JEDEC's RAND policy, Rambus's rates were therefore reasonable. (*Id.*) Third, the evidence shows that Rambus's royalty rates are not discriminatory because Rambus offered the same royalty rates to all potential licensees and only charged a higher rate to one company that insisted on litigating with Rambus before taking a license. (*See* RPF Section XI.B). From both the standpoint of economics and JEDEC's RAND policy, Rambus's rates were therefore nondiscriminatory. (*Id.*)

(A) Pricing above Competitive Levels.

2963. One major indicator of Rambus's monopoly power is that *ex post* pricing of Rambus's technologies substantially exceeds their *ex ante* value. That is, the technologies are

priced at a level that is significantly above the *ex ante* value of the technology. (McAfee, Tr. 7422, 7622, *in camera*).

Rambus's Response to Finding No. 2963:

The proposed finding is not supported by the weight of the evidence. First, Complaint Counsel's economic expert never calculated the *ex ante* value of Rambus's technologies. Rather, {

} (McAfee, Tr. 7622-26) (*in camera*). He also based his conclusion on the assumption that {

} (McAfee, Tr. 7626 (*in camera*). Neither basis is supported by the weight of the evidence.

{

} (Teece, Tr. 10534 (*in camera*)). First, {

} (Teece, Tr. 10534-35 (*in camera*); MacWilliams, Tr. 4824-25). Second, {

} (Teece, Tr. 10535 (*in camera*)). The DDR licenses do not include such provisions; they are simply "naked" patent licenses. With RDRAM, therefore, Rambus had an {

} (Teece,

Tr. 10535-36 (*in camera*)). Rambus was able to "participate in future design improvements" of RDRAM, obtain information about the partner's customers for RDRAM, and be "part of the process going forward." (Farmwald, Tr. 8179-80). In effect, Rambus's RDRAM licenses form a partnership; Rambus works with the licensee, and receives valuable feedback and information. (Farmwald, Tr. 8241). For DDR by contrast, there is no partnership, and Rambus receives no additional benefits. (Farmwald, Tr. 8241). Although Complaint Counsel's economic expert admitted that Rambus's RDRAM licenses have benefits to Rambus that its DDR licenses do not, he did not quantify those benefits when comparing the DDR and RDRAM license rates. (McAfee, Tr. 7835).

The notion that the presence of alternatives shows that Rambus's DDR rates are higher than the *ex ante* value of Rambus's technologies is also unsupported. Complaint Counsel's economic expert admitted that he did not quantify any cost or performance differences between Rambus's technologies and his alternatives. (McAfee, Tr. 7581-82, 11340). In contrast, Dr. Rapp did quantify the cost differences, and this analysis shows that the Rambus technologies incorporated in SDRAM and DDR are *less* costly than any of the noninfringing alternatives, even accounting for Rambus's royalties. (*See* RPF Section IX.B.3.d, IX.B.4.d). This means that the *ex ante* value of Rambus's technologies *exceeded* Rambus's royalties.

2964. Pricing at a level that is significantly above the *ex ante* value of the technologies suggests the exercise of monopoly power, which suggests the existence of monopoly power. (McAfee, Tr. 7422).

Rambus's Response to Finding No. 2964:

The proposed finding is misleading and incomplete. The evidence shows that Rambus's royalty rates are *lower* than the *ex ante* value of its technologies. (*See* RRFF 2963).

2965. The *ex ante* value of a technology is the amount that the industry participants would have been willing to pay to use a technology over its next best alternative prior to the incorporation of the technology into a standard. (McAfee, Tr. 7307-08). *Ex post*, the value of a standardized technology is the *ex ante* value of that technology plus the entire specific investment that has been made in the standardized technology. (McAfee, Tr. 7308).

Rambus's Response to Finding No. 2965:

The proposed finding is misleading and incomplete. The evidence shows that Rambus's royalty rates are *lower* than the *ex ante* value of its technologies. (*See* RRFF 2963). Further, the proposed finding is not supported in that it erroneously equates specific investment with switching costs. (*See* RRFF 2660).

2966. Because of the existence of alternatives to the Rambus-claimed technologies *ex ante,* the *ex ante* value of those technologies is limited by the incentive for the firms in JEDEC to engage in *ex ante* negotiations. (McAfee, Tr. 7494-95; 7625, *in camera*).

Rambus's Response to Finding No. 2966:

The proposed finding is misleading. There were no acceptable noninfringing alternatives. (*See* RPF Section IX.B). There is also no evidence of any *ex ante* negotiations in the DRAM industry related to technologies incorporated in standards, and the evidence indicates that there would have been no *ex ante* negotiations for Rambus's technologies. (*See* RPF 1204-18).

2967. The royalties that Rambus would likely to have been able to receive *ex ante* would have been small or zero because of the existence of alternatives. (McAfee, Tr. 7625, *in camera*).

Rambus's Response to Finding No. 2967:

The proposed finding is not supported by the weight of the evidence. The evidence shows that Rambus's royalty rates are *lower* than the *ex ante* value of its technologies. (*See* RRFF 2963).

2968. The RDRAM royalty rate reflects another measure *ex ante* value of all the Rambus technologies. (McAfee, Tr. 7623, *in camera*).

Rambus's Response to Finding No. 2968:

The proposed finding is not supported by the weight of the evidence. For a number of reasons, the RDRAM royalty rate is not indicative of the *ex ante* value of Rambus's technologies. (*See* RRFF 2963).

2969. Rambus was charging { }, depending on volume, for RDRAM. (McAfee, Tr. 7623, *in camera;* CCFF 1612-613).

Rambus's Response to Finding No. 2969:

The proposed finding is incomplete. (*See* RRFF 2450).

2970. The base level royalty rate for DDR, { }, significantly exceeds { }. The higher rate is being charged to { } among others. (McAfee, Tr. 7623, *in camera;* CCFF 2004-11).

Rambus's Response to Finding No. 2970:

The proposed finding is misleading. For a number of reasons, the RDRAM royalty rate is not indicative of the *ex ante* value of Rambus's technologies. (*See* RRFF 2963).

2971. In addition, { } agreed to pay a rate of { }. (McAfee, Tr. 7623, *in camera;* CCFF 1999, 2000).

Rambus's Response to Finding No. 2971:

The proposed finding is misleading. For a number of reasons, the RDRAM royalty rate is not indicative of the *ex ante* value of Rambus's technologies. (*See* RRFF 2963).

2972. These facts about royalty rates indicate that the minimum rate that is being charged on DDR substantially exceeds the rate that was being charged for the manufacture of RDRAM. (McAfee, Tr. 7624, *in camera*).

Rambus's Response to Finding No. 2972:

The proposed finding is misleading. For a number of reasons, the RDRAM royalty rate is not indicative of the *ex ante* value of Rambus's technologies. (*See* RRFF 2963).

2973. This, in turn, suggests that *ex post* pricing exceeds the *ex ante* value of the technologies, even where the *ex ante* value is approximated by the charges for the production of RDRAM. (McAfee, Tr. 7624, *in camera*). Therefore, the rates on DDR are indicia of Rambus's ability to exercise market power. (McAfee, Tr. 7627, *in camera*).

Rambus's Response to Finding No. 2973:

The proposed finding is misleading. For a number of reasons, the RDRAM royalty rate is not indicative of the *ex ante* value of Rambus's technologies. (*See* RRFF 2963).

2974. If there were commercially viable alternatives available, the industry would substitute to those rather than pay royalties to Rambus. The fact that such substitution has not taken place demonstrates the absence of commercially viable alternatives today. (McAfee, Tr. 7630, *in camera*).

Rambus's Response to Finding No. 2974:

The proposed finding is misleading and not supported by the weight of the evidence. The evidence shows that there are no acceptable, noninfringing alternatives. (*See* RPF Section IX.B). Because switching costs and coordination issues do not prevent a change to alternatives technologies (*see* RPF Section IX), the evidence that the industry has not switched to alternatives confirms that there were no acceptable, noninfringing alternatives.

2975. On economic grounds, the DDR royalties reflect monopoly pricing. (McAfee, Tr. 7629, *in camera*).

Rambus's Response to Finding No. 2975:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 2963).

(B) Price Discrimination.

2976. The power to price discriminate also reflects the exercise of market power. (McAfee, Tr. 7636, *in camera*).

Rambus's Response to Finding No. 2976:

The proposed finding is not supported by the evidence. Complaint Counsel's economic

expert admitted that the power to price discriminate is only { }

(McAfee, Tr. 7636-37 (*in camera*)).

2977. Price discrimination refers to charging buyers their willingness to pay rather than the cost of dealing with them. (McAfee, Tr. 7636, *in camera*). The ability to charge customers their willingness to pay reflects the absence of competition and so is direct evidence of the ability to raise prices above the competitive level. (McAfee, Tr. 7636-37, *in camera*).

Rambus's Response to Finding No. 2977:

The proposed finding is not supported. Complaint Counsel's economic expert testified that price discrimination is only { } (McAfee, Tr. 7636-37 (*in camera*)).

2978. The fact that { } is paying a higher royalty rate than { } means that price discrimination is taking place. (McAfee, Tr. 7635, *in camera*).

Rambus's Response to Finding No. 2978:

The proposed finding is not supported by the weight of the evidence. { } (Teece, Tr. 10538 (*in camera*)). { } (Teece, Tr. 10538 (*in camera*)). Rambus offered its SDRAM and DDR licenses to everybody on more or less the same terms. (Farmwald, Tr. 8242). Before litigation, Rambus offered Hitachi a license on essentially the same terms it offered to others. (CX 2059, Karp Dep. at 252). Complaint Counsel's economic expert admitted on cross-examination that Rambus's offers were nondiscriminatory. (McAfee, Tr. 7848).

Further, higher royalties for litigating parties are not discriminatory. { } (Teece, Tr. 10541 (*in camera*)). { }

(Teece, Tr. 10541 (*in camera*)). {

} (Teece, Tr. 10540 (*in camera*)). In other words, the fact that Rambus charged a higher rate after litigation may be justified by changed perceptions regarding the strength of the patents. Moreover, {

} (Teece, Tr. 10542 (*in camera*)). This creates {

} (Teece, Tr. 10542-43 (*in camera*)). {

}

(Teece, Tr. 10542, 10551 (*in camera*)).

{

}

(McAfee, Tr. 7829 (*in camera*)). He went on to admit that {

} (McAfee, Tr. 7829 (*in camera*)). Further, he recognized that { } (McAfee, Tr. 7830 (*in camera*)), and that a {

} (McAfee, Tr. 7831 (*in camera*)).

2979. Even if the rates that { } agreed to pay were competitive, the fact that { } agreed to pay a higher royalty rate than { } suggests that there are no longer any commercially viable alternative technologies available to DRAM users. Otherwise

{ } would have switched to one of the alternatives to get the lower competitive rate. (McAfee, Tr. 7627, *in camera*).

Rambus's Response to Finding No. 2979:

The proposed finding is not supported by the weight of the evidence. The evidence shows that there were no acceptable noninfringing alternatives either before standardization or after standardization. (*See* RPF Section IX.B).

2980. Rambus had a strategy of demanding higher royalty rates from those firms that litigate against Rambus. Rambus also had a strategy that it might not license at all to those companies that litigate against Rambus and lose. (CCFF 1990-994).

Rambus's Response to Finding No. 2980:

Rambus has no specific response.

2981. A refusal by Rambus to license a company that litigated against it and lost would be discriminatory from an economic standpoint. (Teece, Tr. 10565-69, *in camera*).

Rambus's Response to Finding No. 2981:

While the proposed finding accurately reflects the testimony by Prof. Teece, there is no evidence that Rambus will actually refuse to license those who have litigated with it. Rambus licensed its patents to Hitachi despite litigation with it.

2982. The { } pays for the use of the Rambus technologies in SDRAM and DDR are not necessarily justified by costs related to the Rambus/Hitachi litigation. (Teece, Tr. 10556-57, *in camera*).

Rambus's Response to Finding No. 2982:

The proposed finding is unsupported. (*See* RRFF 2978). It also misleading. Professor Teece testified that the { } pays *is* cost justified taking into account { }. (Teece, Tr. 10542, 10551 (*in camera*)). The proposed finding only relies on his testimony that it is not cost justified {"

} (Teece, Tr. 10557 (*in camera*)).

2983. The mere fact that an *ex post* royalty may have resulted from an arm's length negotiation does not mean that that royalty would be reasonable from the standpoint of what might have been negotiated *ex ante*. (Teece, Tr. 10513).

Rambus's Response to Finding No. 2983:

Rambus has no specific response.

2984. Payment caps in license agreements have the effect of altering the effective royalty rate paid under the license. (Teece, Tr. 10616).

Rambus's Response to Finding No. 2984:

The proposed finding is incomplete. Professor Teece testified that although a payment cap in a license agreement might affect the effective royalty rate under some circumstances, such a cap would not affect in-kind consideration in a patent license. (Teece, Tr. 10616-17).

2985. License rates charged by companies that are not pure play technology companies are not entirely comparable to license rates charged by pure play technology companies such as Rambus. (Teece, Tr. 10622-23).

Rambus's Response to Finding No. 2985:

The proposed finding is misleading. The cited testimony was limited to the difference between Kentron and Rambus:

> Q. But you would agree that in your view, license rates charged by companies that are not pure-play technology companies are somewhat less comparable to Rambus than license rates charged by pure-play technology companies? That was the very point you were making in your expert report, is it not?
>
> A. I was making the point that because Kentron is a manufacturer,

its expectations will be different than Rambus', that's correct.

(Teece, Tr. 10622-23).

E. The Rambus Conduct was Anticompetitive.

2986. Exclusionary conduct is behavior or conduct that would exclude an equal or superior competitor from the marketplace. (McAfee, Tr. 7142, 7476). Such conduct harms consumers by reducing their choices and eliminating competition in the marketplace. (McAfee, Tr. 7476).

Rambus's Response to Finding No. 2986:

The proposed finding is incomplete. The fact that conduct excludes equal or superior competitors is not sufficient to define conduct as exclusionary. (Rapp, Tr. 9927-28). Enforcing a patent or other lawful intellectual property can have that effect but is not exclusionary. (Rapp, Tr. 9229-30). For conduct to be exclusionary, not only must equal or superior competitors be excluded, the conduct must consist of short-run actions that do not make sense except in terms of their adverse impact on competition, i.e., the actions cannot have a legitimate business justification. (Rapp, Tr. 9911).

2987. Exclusionary conduct that eliminates equal or superior competitors will harm consumers by reducing their choices and eliminating competition in the marketplace. (McAfee, Tr. 7476).

Rambus's Response to Finding No. 2987:

Rambus does not disagree with this proposed finding as long as "exclusionary conduct" is properly defined.

2988. Exclusionary conduct has no valid efficiency rationale. (McAfee, Tr. 7477).

Rambus's Response to Finding No. 2988:

Rambus does not disagree with this proposed finding.

1. Providing False or Misleading Information.

2989. From an economic perspective, providing false or misleading information to economic decision-makers can have the effect of being exclusionary. (McAfee, Tr. 7167-68).

Rambus's Response to Finding No. 2989:

The proposed finding is misleading. Exclusionary conduct is not defined solely with reference to the effect of the conduct; rather, it is defined also by the character of the conduct, i.e., that it is economically irrational but for its impact on competition. (Rapp, Tr. 9927-28). Thus, false or misleading information is exclusionary only if it is economically irrational absent an effect on competitors. Further, as Complaint Counsel's economic expert admitted, a misrepresentation may not be exclusionary even if it impacts competition. (McAfee, Tr. 7535-36).

2990. The reason that such conduct can be exclusionary is because it causes the decision-makers to evaluate various alternative product choices that they face incorrectly, and thus when decision-makers try to choose the best product they may fail. (McAfee, Tr. 7168). The decision-makers may choose an inferior rather than a superior product because they have incorrect information about the alternatives. (McAfee, Tr. 7168).

Rambus's Response to Finding No. 2990:

The proposed finding is misleading. First, exclusionary conduct is not defined solely with reference to the effect of the conduct; rather, it is defined also by the character of the conduct, i.e., that it is economically irrational but for its impact on competition. (Rapp, Tr. 9927-28). As Complaint Counsel's economic expert also admitted, a misrepresentation may not be exclusionary even if it impacts competition. (McAfee, Tr. 7535-36). Second, the proposed finding is flawed because it does not necessarily follow that providing false information *causes* decision-makers to make incorrect evaluations. The relevant decision-makers may not rely on

the false information, or the false information may not change the outcome of the evaluation. For instance, as Complaint Counsel's economic expert admitted, if the relevant decision-maker receives relevant information from another means, the provision of misleading information will not be exclusionary. (McAfee, Tr. 7686).

2991. Misleading information tends to prevent competition on the merits by distorting consumer choice away from their optimal choices. (McAfee, Tr. 7482). The effect is to benefit inferior products and harm equal or superior products. (McAfee, Tr. 7483). For this reason, the provision of distorted information is often exclusionary. (McAfee, Tr. 7483; *see* DX0232).

Rambus's Response to Finding No. 2991:

The proposed finding is misleading. First, exclusionary conduct is not defined solely with reference to the effect of the conduct; rather, it is defined also by the character of the conduct, i.e., that it is economically irrational but for its impact on competition. (Rapp, Tr. 9927-28). Further, as Complaint Counsel's economic expert admitted, a misrepresentation may not be exclusionary even if it impacts competition. (McAfee, Tr. 7535-36). Second, the proposed finding is flawed because it does not necessarily follow that providing misleading information distorts consumer choice away from optimal choices. The relevant decision-makers may not rely on the information, or the misleading information may not change the outcome of consumer choice. For instance, as Complaint Counsel's economic expert admitted, if the relevant decision-maker receives relevant information from another means, the provision of misleading information will not be exclusionary. (McAfee, Tr. 7686).

2992. Rambus's conduct is exclusionary, because it was false and misleading, if the following assumptions are true: (1) at the time Rambus was at JEDEC, it possessed IP relevant to JEDEC standards / work; (2) Rambus failed to disclose relevant IP as required by JEDEC rules / process; (3) Rambus engaged in other, related misrepresentations while a member of JEDEC; (4) after leaving JEDEC, Rambus continued to conceal its IP; and (5) before during and after JEDEC participation, Rambus planned to enforce JEDEC-related IP. (McAfee, Tr. 7477-79; *see*

DX0230).

Rambus's Response to Finding No. 2992:

The proposed finding is contrary to the evidence and leaves out necessary information. The proposed finding contradicts Complaint Counsel's own economic expert, who testified that to be exclusionary, conduct must exclude an equal or superior competitor. The proposed finding does not include this prerequisite. (McAfee, Tr. 7142, 7476). Second, the proposed finding does not include the condition that the conduct have no valid efficiency rationale, again contradicting Complaint Counsel's own economic expert. (McAfee, Tr. 7477). Third, the proposed finding ignores the evidence that Rambus was motivated by legitimate business justifications not to disclose information about pending or future patent applications. (*See* Rapp, Tr. 9916-18, 9926; RPF 91-107). Fourth, these legitimate business justifications apply even if JEDEC's rules/process required the disclosure of "relevant IP," because Rambus's legitimate business reasons did not depend on misleading JEDEC or on any action or inaction on the part of JEDEC. (Rapp, Tr. 9924). Fifth, the proposed finding fails to require that JEDEC rely on the alleged failure to disclose and alleged related misrepresentations. Complaint Counsel's economic expert admitted that a lack of reliance would render any failure to disclose not exclusionary as a matter of economics. (McAfee, Tr. 7686).

2993. If the first two assumptions, are true, the third assumption is not necessary to find that Rambus engaged in exclusionary conduct. (McAfee, Tr. 7478).

Rambus's Response to Finding No. 2993:

The proposed finding is contrary to the evidence and leaves out necessary information. (*See* RRFF 2992).

2994. The fourth assumption is also not necessary to a finding that Rambus's conduct was exclusionary if the first two are true, but the fourth assumption relates to the magnitude of the effect of Rambus's conduct. (McAfee, Tr. 7478-79).

Rambus's Response to Finding No. 2994:

The proposed finding is contrary to the evidence and leaves out necessary information. (*See* Response to Finding 2992).

2995. The fifth assumption relates to whether Rambus's conduct was intentional rather than inadvertent. (McAfee, Tr. 7479).

Rambus's Response to Finding No. 2995:

The proposed finding is contrary to the evidence and leaves out necessary information. (*See* RRFF 2992). The proposed finding is also flawed in that it attempts to relate intentionality to a plan to enforce intellectual property rather than an intention to knowingly violate JEDEC's rules in order to mislead JEDEC and to gain monopoly power. As Complaint Counsel's own expert testified, an "inadvertent failure to disclose" would not be exclusionary. (McAfee, Tr. 7479). The evidence shows that Rambus did not intend to violate JEDEC's rules or to mislead anyone. (*See* RPF V.F).

2996. If the above assumptions are true, then on economic grounds Rambus's challenged conduct is exclusionary. (McAfee, Tr. 7481-82).

Rambus's Response to Finding No. 2996:

The proposed finding is contrary to the evidence and leaves out necessary information. (*See* RRFF 2992).

2997. At the time Rambus was at JEDEC, it possessed IP relevant to the work JEDEC was undertaking and the JEDEC standards. (CCFF 867-1237).

Rambus's Response to Finding No. 2997:

The proposed finding is contrary to the evidence. (*See* RRFF 867-1237).

2998. Rambus failed to disclose relevant IP as required by JEDEC rules / process. (CCFF 1238-1357).

Rambus's Response to Finding No. 2998:

The proposed finding is contrary to the evidence. (*See* RRFF 1238-1357).

2999. Rambus engaged in other, related misrepresentations while a member of JEDEC. (CCFF 902-909, 968-976, 1062-1068, 1109-114).

Rambus's Response to Finding No. 2999:

The proposed finding is contrary to the evidence. (*See* RRFF 902-09, 968-76, 1109-14).

3000. After leaving JEDEC, Rambus continued to conceal its IP. (CCFF 1259, 1676-1700).

Rambus's Response to Finding No. 3000:

The proposed finding is contrary to the evidence. (*See* RRFF 1259, 1676-1700).

Complaint Counsel's economic expert also testified that Rambus's not disclosing information about its intellectual property would only be exclusionary if it violated a JEDEC rule or process. (McAfee, Tr. 7530-31).

3001. Before, during and after JEDEC participation, Rambus planned to enforce JEDEC-related IP. (CCFF 800-821, 1714-17, 1919-24, 1870-71).

Rambus's Response to Finding No. 3001:

The proposed finding is misleading, contrary to the evidence, and irrelevant. (*See* RRFF 2995, 800-21, 1714-17,1919-24, 1870-71).

3002. Rambus's challenged conduct would be exclusionary because Rambus's provision of misleading or incorrect information to JEDEC decision-makers excluded equal or superior competitors. In this case, the competitors were alternative DRAM technologies. (McAfee,

Tr. 7168).

Rambus's Response to Finding No. 3002:

The proposed finding is contrary to the evidence. First, the proposed finding applies an erroneous definition of exclusionary conduct. (*See* RRFF 2986-96). Second, the evidence shows that there were no equal or superior alternatives that were excluded. (*See* RPF 1448-58, Section IX.B). Third, the evidence shows that the alleged conduct did not affect JEDEC's choices of technologies. (*See* RPF Section IX).

3003. The nature of the exclusionary conduct is the distortion of JEDEC's standardization process. (McAfee, Tr. 7173).

Rambus's Response to Finding No. 3003:

The proposed finding is contrary to the evidence. The evidence shows that the alleged conduct did not affect JEDEC's choices of technologies. (*See* RPF Section IX). Further, the proposed finding does not comport with the economic definition of exclusionary conduct; the finding focuses solely on a purported effect rather than the character of the conduct. (*See* RRFF 2986-96).

3004. The conduct would be exclusionary because it distorted the JEDEC standard-setting process. (McAfee, Tr. 7481). In so doing, it caused JEDEC to make mistakes that it would not have made if JEDEC had accurate information. (McAfee, Tr. 7481-82).

Rambus's Response to Finding No. 3004:

The proposed finding is contrary to the evidence. The evidence shows that the alleged conduct did not affect JEDEC's choices of technologies. (*See* RPF Section IX). Further, the proposed finding does not comport with the economic definition of exclusionary conduct; the finding focuses solely on a purported effect rather than the character of the conduct. (*See* RRFF

2986-96).

3005. According to Dr. Rapp, a failure on the part of Rambus to disclose to JEDEC information about pending or future patent applications that it was required to disclose would be "exclusionary" from the standpoint of antitrust economics, if there were no independent business justification for the failure to disclose. (Rapp, Tr. 9921).

Rambus's Response to Finding No. 3005:

The proposed finding is incomplete. Dr. Rapp testified, "it would only be exclusionary from the perspective of antitrust economics if there were no business justification for it. And as we move from the general to the particular, in this instance I believe that not to be the case. In other words, I believe that there were business justifications." (Rapp, Tr. 9921).

2. Conscious Choice by Rambus to Jeopardize Its Own Rights.

3006. If Rambus was aware of legal risks associated with the assumed conduct, then that provides an additional basis for finding that Rambus's conduct was exclusionary. (McAfee, Tr. 7479-80; *see* DX0230). That basis is that if the assumption is true, then Rambus's conduct entailed a conscious choice to jeopardize the enforceability of patented intellectual property. (McAfee, Tr. 7501; *see* DX0231).

Rambus's Response to Finding No. 3006:

The proposed finding is contrary to the evidence and logically incoherent. Simply incurring risk does not make conduct exclusionary; firms often take risks to achieve legitimate gains. (Rapp, Tr. 9931). The potential gains must be accounted for, and the presence of risks alone says nothing about whether conduct is exclusionary. (Rapp, Tr. 9931). Rather, the question is whether there was a legitimate business justification (i.e., valid efficiency rationale) for the conduct. (Rapp, Tr. 9914). Rambus had such a legitimate business justification. (Rapp, Tr. 9916-18). Further, Complaint Counsel's economic expert admitted that he did not consider any reasons other than monopolization for Rambus's not disclosing information about its

intellectual property. In other words, he simply failed to account for legitimate business justifications. (McAfee, Tr. 7539).

Further, the proposed finding is misleading and unsupported. The theory of the proposed finding is that if Rambus was aware of a legal risk, this shows that Rambus must have intended to mislead JEDEC in order to later obtain a patent on the standard because its conduct was otherwise irrational. As Complaint Counsel's economic expert admitted, by later enforcing its patents, however, Rambus would likely trigger an inquiry into whether it did not disclose required information to JEDEC. (McAfee, Tr. 7547-50). Thus, the culmination of the alleged plan would result in litigation that would render Rambus's patents unenforceable. The implication is that Rambus's conduct does not reflect any strategy to ambush JEDEC, but the fact that Rambus did not perceive any legal risk because its attorneys had advised it that it could avoid legal risks by behaving in certain ways at JEDEC, which advice it followed. (*See* RPF 446-63).

3007. An intentional decision to jeopardize the enforceability of patented intellectual property is potentially exclusionary behavior because it implies that the firm is expecting a substantial compensating benefit. (McAfee, Tr. 7502). The potential expected gain would be the ability to monopolize the relevant markets. (McAfee, Tr. 7502-503).

Rambus's Response to Finding No. 3007:

The proposed finding is contrary to the evidence and logically incoherent. (*See* RRFF 3006). The proposed finding ignores the evidence that there were legitimate business reasons for not disclosing intellectual property interests. (Rapp, Tr. 9916-18; RPF Section III.C.3.d). Complaint Counsel's economic expert admitted that he simply did not consider whether Rambus had legitimate business justifications for its alleged conduct. (McAfee,

Tr. 7539). Further, the proposed finding has no application because Rambus did not engage in an "intentional decision to jeopardize the enforceability of patented intellectual property." (*See* RRFF 3006).

3008. Like predatory pricing, this conduct is irrational absent the expected benefits that would be obtained by excluding competition. (McAfee, Tr. 7502; *see* DX0238).

Rambus's Response to Finding No. 3008:

The proposed finding is contrary to the evidence. (*See* RRFF 3006). Predatory pricing, i.e., pricing below average variable cost, is exclusionary because there is no legitimate business justification for such conduct, i.e., it is irrational except for the prospect of an effect of competition. (Rapp, Tr. 9912). There are, however, legitimate business justifications for not disclosing intellectual property which motivated Rambus's conduct. (Rapp, Tr. 9916-18; RPF Section III.C.3.d). These legitimate business justification apply to Rambus at JEDEC even if there were a rule requiring Rambus to disclose, and a failure to disclose is not exclusionary because there are benefits from not disclosing that are unrelated to any impact on competing technologies. (Rapp, Tr. 9919-24). Complaint Counsel's economic expert admitted that he failed to consider whether legitimate business justifications existed for Rambus's alleged conduct. (McAfee, Tr. 7539). Further, the proposed finding has no application because Rambus did not engage in an "intentional decision to jeopardize the enforceability of patented intellectual property." (*See* RRFF 3006).

3009. If Rambus knowingly incurred a legal risk associated with its conduct, the implication from an economic perspective is that there must have been an expected compensating benefit. (McAfee, Tr. 7502).

Rambus's Response to Finding No. 3009:

Rambus does not disagree with the proposed finding. However, the proposed finding has no application because Rambus did not knowingly incur legal risk. (*See* RRFF 3006).

3010. Rambus incurred a legal risk associated with its conduct. (CCFF 820-821).

Rambus's Response to Finding No. 3010:

The finding is not supported by the weight of the evidence. (*See* RRFF 820-21).

3011. On economic grounds, the prospect of creating a monopoly on the JEDEC standards can be considered to be a compensating gain for undertaking a large risk of jeopardizing the enforceability of patented intellectual property. (McAfee, Tr. 7170-71).

Rambus's Response to Finding No. 3011:

The proposed finding is misleading, incomplete, and not supported by the weight of the evidence. First, there are economic benefits that are independent of monopolizing a JEDEC standard for not disclosing information about intellectual property interests. (Rapp, Tr. 9919-24). Disclosing information about pending or future patent applications may jeopardize the ability to obtain a patent at all. (Rapp, Tr. 9916-18; RPF Section III.C.3.d). And such a disclosure may result in a loss of competitive advantage. (*Id.*) Not disclosing such information, therefore, allows the firm to retain the ability to obtain patent protection and retains competitive advantages. (*Id.*) Not disclosing such information is also procompetitive and benefits consumers. (Rapp, Tr. 9918-19). These legitimate business justifications and benefits apply in the context of a participant in JEDEC – even if JEDEC required the disclosure of information regarding intellectual property interests – and the benefits are independent of what standards are adopted by JEDEC. (Rapp, Tr. 9919-24).

Second, the proposed finding is contradicted by the evidence that it would have been

economically irrational for Rambus to conceal information about its intellectual property interests if it had thought that a failure to disclose would have put its intellectual property at risk. Complaint Counsel's economic expert admitted that had Rambus knowingly concealed information from JEDEC in order to mislead JEDEC into adopting the technologies, any effort to enforce Rambus's later issued patents would have triggered an inquiry into whether Rambus had violated a duty to disclose. (McAfee, Tr. 7547). This inquiry would lead to a risk of challenge that would render the patents unenforceable – preventing any monopoly over the standard. (McAfee, Tr. 7550). Thus, the hope of monopolization cannot be a compensating gain for knowingly putting intellectual property interests at risk by knowingly refusing to disclose patent interests to JEDEC that must be disclosed because the monopolization itself would put the intellectual property at risk.

F. Rambus's Anticompetitive Conduct Led to its Monopoly Power.

3012. The incorporation of Rambus technology in the SDRAM and DDR SDRAM standards contributes to Rambus' monopoly power in the relevant markets. (McAfee, Tr.7427-28).

Rambus's Response to Finding No. 3012:

The proposed finding is not supported by the weight of the evidence. First, the economic conditions for standardization to enhance Rambus's market power do not exist. (*See* RPF 1503-30). Standardization can only enhance market power where compatibility requirements are exceedingly high and there exist equal or superior alternatives that are excluded by standardization. (Rapp, Tr. 9799-800). The coexistence of multiple DRAM standards, the success of non-JEDEC standards, and the fact that computer systems using different DRAM many still be compatible shows that compatibility requirements in the DRAM industry are not

exceedingly high. (*See* RPF 1509-23). Moreover, the evidence shows that Rambus's technologies were superior to alternatives; therefore, standardization by JEDEC did not enhance Rambus's market power. (Rapp, Tr. 9901-02; RPF Section IX).

Second, the evidence shows that JEDEC would have incorporated Rambus's technologies into the SDRAM and DDR standards even if Rambus had made the additional disclosures that Complaint Counsel allege should have been made. The evidence shows that JEDEC preferred Rambus's technologies over all others and that the additional disclosures would not have changed that revealed preference. (*See* RPF 1532; Section IX.A). The evidence also shows that there were no cost-performance equivalent noninfringing alternatives; rational JEDEC members would have selected Rambus's technologies accounting for Rambus's royalties. (*See* Rapp, Tr. 9907-09; RPF Section IX.B). Further, an analysis of JEDEC's and Rambus's economic incentives and past behavior shows that JEDEC would have incorporated the Rambus technologies even if Rambus had made the additional disclosures. (*See* RPF Section IX.C). This means that Rambus's alleged conduct did not enhance its market power. (Teece, Tr. 10312-13).

3013. The distortion of the information available to JEDEC decision-makers is the basis on which Rambus's monopoly power has been obtained. (McAfee, Tr. 7173).

Rambus's Response to Finding No. 3013:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 3012)

3014. One reason for this is the change in the bargaining positions between Rambus and other JEDEC participants that occurred going from the *ex ante* world to the *ex post* world. (McAfee, Tr. 7634, *in camera*).

Rambus's Response to Finding No. 3014:

The proposed finding is not supported by the weight of the evidence. There was no

change in the bargaining positions between Rambus and JEDEC members. Before standardization, there were no noninfringing alternatives that were equivalent to or better than Rambus's technologies in cost-performance terms. (*See* RPF Section IX.B; Rapp, Tr. 9901-02). After standardization, switching costs did not prevent JEDEC members from turning to alternative technologies. (*See* Rapp, Tr. 9902-03; RPF Section X). Further, the evidence shows that Rambus's royalty rates for its SDRAM and DDR license are reasonable and nondiscriminatory. (*See* RPF XI).

3015. At the time before the relevant standards were set, consumers of the technology had a variety of options, and thus Rambus's bargaining power was limited, *i.e.,* the bargaining power was weighted more heavily toward DRAM manufacturers than it was toward Rambus. (McAfee, Tr. 7634, *in camera*).

Rambus's Response to Finding No. 3015:

The proposed finding is not supported by the weight of the evidence. There was no change in the bargaining positions between Rambus and JEDEC members. Before standardization, there were no noninfringing alternatives that were equivalent to or better than Rambus's technologies in cost-performance terms. (*See* RPF Section IX.B; Rapp, Tr. 9901-02).

3016. By contrast, in the *ex post* world, once the industry has been locked into the Rambus technologies, the bargaining power of DRAM manufacturers became limited, and Rambus was in a much stronger bargaining position. (McAfee, Tr. 7634, *in camera*).

Rambus's Response to Finding No. 3016:

The proposed finding is not supported by the weight of the evidence. There was no change in the bargaining positions between Rambus and JEDEC members. After standardization, switching costs did not prevent JEDEC members from turning to alternative technologies. (*See* Rapp, Tr. 9902-03; RPF Section X). Further, the evidence shows that

Rambus's royalty rates for its SDRAM and DDR license are reasonable and nondiscriminatory. (*See* RPF XI).

3017. A standard economic methodology for assessing the effects of exclusionary conduct is known as a "but-for world" analysis. (McAfee, Tr. 7485).

Rambus's Response to Finding No. 3017:

Rambus does not disagree with the proposed finding.

3018. The but-for world analysis is to suppose, as a hypothesis, that Rambus had not engaged in the conduct at issue, and then ask what would have happened under those circumstances. (McAfee, Tr. 7485).

Rambus's Response to Finding No. 3018:

Rambus does not disagree in substance with the proposed finding, although it should refer to "alleged conduct."

3019. In this case, the appropriate but-for hypothesis is that Rambus had not engaged in the challenged exclusionary conduct. (McAfee, Tr. 7485). In defining the but-for world, the appropriate thing is to change nothing except the conduct that is challenged. (Teece, Tr. 10735).

Rambus's Response to Finding No. 3019:

Rambus does not disagree in substance with the proposed finding, although it should refer to "alleged conduct" and should not assume that the "alleged conduct" was exclusionary.

3020. Rambus's business strategy in the but-for world should mimic its business strategy in the actual world. (McAfee, Tr. 11311)

Rambus's Response to Finding No. 3020:

Rambus does not disagree with the proposed finding to the extent that it implies Rambus's business strategy of obtaining revenue through licensing its intellectual property would not be different in the but-for world.

3021. The most likely outcome in the but-for world would be that JEDEC would avoid

Rambus IP or would have licensed Rambus IP at lower royalty rates. (McAfee, Tr. 11304)

Rambus's Response to Finding No. 3021:

The proposed finding is contradicted by the weight of the evidence. The most likely outcome in the but-for world would be that JEDEC would have incorporated Rambus's technologies, negotiated for licenses after Rambus's patents issued, and paid the same royalty rates as paid in the real world. (*See* RPF Section IX, X, XII.B.2).

Three independent lines of evidence show that JEDEC would have adopted Rambus's technologies had Rambus made the additional disclosures Complaint Counsel allege should have been made. First, the evidence shows that the additional disclosures would not have changed JEDEC's revealed preference for Rambus's technologies. It is undisputed that JEDEC elected to adopt those technologies into a new standard even after Rambus's patents issued and it began to seek royalties. (*See* RPF 1532; Section IX.A). Second, there were no noninfringing alternatives with equivalent cost-performance. Thus, rational JEDEC members would have selected Rambus's technologies even accounting for Rambus's royalties. (*See* Rapp, Tr. 9907-09; RPF Section IX.B). Third, an analysis of JEDEC's and Rambus's economic incentives and past behavior shows that JEDEC would have incorporated the Rambus technologies even if Rambus had made the additional disclosures. (*See* RPF Section IX.C). The evidence also shows that after incorporating Rambus's technologies, JEDEC members would not have engaged in *ex ante* negotiations, i.e., negotiations would have occurred after Rambus's patents issued - as they did in the real world. (*See* RPF Section IX.D.2.b). The negotiations would have thus resulted in the same reasonable and nondiscriminatory royalty rates that Rambus not charges. (*See* RPF Section XI).

3022. In the but-for world where Rambus has disclosed relevant intellectual property to JEDEC in a timely fashion, it is first necessary to ask whether or not Rambus would have issued a RAND letter. (McAfee, Tr. 7486).

Rambus's Response to Finding No. 3022:

The proposed finding is misleading and contrary to other more reliable evidence. The first question is whether JEDEC would have sought a RAND letter from Rambus. (Teece, Tr. 10316). The evidence shows that JEDEC might logically not have asked Rambus for a RAND letter, because: (1) JEDEC members thought Rambus's patents would not be valid; (2) JEDEC members believed that Rambus was seeking ways to "torpedo" standards competing with RDRAM; and (3) in a similar situation, an EIA committee, under the guidance of EIA General Counsel John Kelly, did not seek a RAND letter. (*See* RPF 1159-82). On cross-examination, Complaint Counsel's economic expert admitted to this possiblity, (McAfee, Tr. 7708, 11308), and he admitted that if JEDEC did not ask for a RAND letter, JEDEC would have adopted Rambus's technologies in the but-for world. (McAfee, Tr. 11308).

If one assumes that JEDEC would have asked for a RAND letter, it is then appropriate to ask whether Rambus would have agreed to give one. (Teece, Tr. 10317).

3023. It is not consistent with JEDEC behavior that in response to a disclosure of intellectual property by Rambus, it would not have requested a RAND letter. (McAfee, Tr. 11308; *see* DX0377; CCFF 347-348).

Rambus's Response to Finding No. 3023:

The proposed finding is not supported and contradicted by the weight of the evidence. First, the evidence shows that an EIA committee, with the full involvement of EIA General Counsel John Kelly, did not ask for a RAND letter in similar circumstances to those in this case. (*See* RRFF 3022). Second, the evidence shows that on at least seven occasions during the period

from May 1990 to the end of 1995, the 42.3 committee adopted technologies for which there had been patent issues raised, without obtaining a RAND letter. (*See* RPF 1225-37).

3024. There is reason to doubt that Rambus would have issued a RAND letter. (McAfee, Tr. 11311; CCFF 1091, 2419-2432). First, it appears that it was contrary to Rambus's business model for it to have issued a RAND letter because Rambus wanted flexibility to charge different royalty rates. (McAfee, Tr. 7489). Based on their business plan it was more likely than not that Rambus would have refused to issue a RAND letter. (McAfee, Tr. 11311; *see* DX0377)

Rambus's Response to Finding No. 3024:

The proposed finding is not supported by the weight of the evidence. First, Complaint Counsel's economic expert, whose testimony is cited in support of the finding, testified that he could *not* determine "one way or the other" whether it would have been in Rambus's economic interest to give a RAND assurance. (McAfee, Tr. 7730, 7733, 11333). Second, the overwhelming economic evidence shows that it would have been in Rambus's economic interest in the but-for world to do so. (*See* RPF 1184-1203; *see also* Response to Finding 2418-32).

3025. Another reason to doubt that Rambus would have issued a RAND letter is that refusing to issue a RAND letter might help RDRAM succeed in the marketplace by delaying the passage of the JEDEC standard. (CCFF 1616). Not issuing a RAND letter might have stalled the JEDEC standard because of the requirement that JEDEC not include intellectual property in the standard without such a RAND letter. (McAfee, Tr. 7489-90).

Rambus's Response to Finding No. 3025:

The proposed finding is not supported by the weight of the evidence. Giving RAND assurances after being asked by JEDEC to do so would have increased the likelihood that JEDEC would incorporate the Rambus technologies and that Rambus would have received royalty payments. (Teece, Tr. 10341, 10344-45, 10350-51). Any speculation about aiding RDRAM by not giving such assurances would have been outweighed by the prospect of having royalties in hand. (Teece, Tr. 10739-40). Moreover, if Complaint Counsel is correct that there would have

been acceptable, noninfringing alternatives to Rambus's technologies in the but-for world, Rambus would surely have been aware of this fact (McAfee, Tr. 7729), and this would have given Rambus an even greater incentive to give a RAND letter. (Teece, Tr. 10739-40).

3026. In the case where Rambus had not issued a RAND letter, assuming that JEDEC was prohibited by its own rules from including technologies covered by patent rights in a standard, the JEDEC standard would not have incorporated Rambus's intellectual property. (McAfee, Tr. 7487).

Rambus's Response to Finding No. 3026:

The proposed finding is contradicted by the weight of the evidence. The evidence shows that on at least seven occasions during the period from May 1990 to the end of 1995, the 42.3 committee adopted technologies for which there had been patent issues raised, *without* obtaining a RAND letter. (*See* RPF 1225-37).

3027. JEDEC would not have included a technology for standardization if they understood in advance that the technology would not be offered to everyone on a non-discriminatory basis. (CCFF 347-348)

Rambus's Response to Finding No. 3027:

The proposed finding is contradicted by the weight of the evidence. The evidence shows that on at least seven occasions during the period from May 1990 to the end of 1995, the 42.3 committee adopted technologies for which there had been patent issues raised, *without* obtaining a RAND letter – and therefore having no assurance that the technology would be licensed to everyone on non-discriminatory terms. (*See* RPF 1225-37).

3028. Under the assumption that Rambus would have refused to issue a RAND letter, Rambus's failure to disclose its intellectual property in a timely fashion caused the inclusion of the Rambus technology into the JEDEC standard. (McAfee, Tr. 7488). In that case, the misrepresentations matters. (McAfee, Tr. 7487-88 ("In that event, the standard does not incorporate Rambus IP, and as a result, we can conclude that in this branch of the tree Rambus' failure to disclose actually caused the inclusion of the Rambus technology in the JEDEC

standard."); McAfee, Tr.11312; *see* DX0377).

Rambus's Response to Finding No. 3028:

The proposed finding is contradicted by the weight of the evidence. Three independent lines of evidence – evidence of JEDEC's choices, even after Rambus's patents issued; evidence of the inferiority of alternatives; and evidence of JEDEC's and Rambus's incentives and behavior – show that there is no causal link between Rambus's alleged failure to disclose its intellectual property interests and JEDEC's incorporation of Rambus's technologies. (*See* RPF Section IX).

3029. If Rambus would have issued a RAND letter, JEDEC most likely would not have included Rambus's intellectual property in its standards. (McAfee, Tr. 7491; 7496-500; *see* DX0236-37). The reason for this conclusion is that other commercially viable technologies were available to JEDEC. (McAfee, Tr. 7491; CCFF 2433-440).

Rambus's Response to Finding No. 3029:

The proposed finding is contrary to the evidence. First, there were no acceptable, noninfringing technologies. (*See* RPF Section IX.B). Second, JEDEC adopted Rambus's technologies in the real world, even after Rambus's patents issued and it sought royalties. (*See* RPF Section IX.A). Third, JEDEC's behavior was to accept patented technologies, especially after receiving a RAND letter. (*See* RPF 1219-44). The evidence shows that JEDEC preferred Rambus's technologies over all alternatives (*see* RPF Section IX.A), and as the long time chair of JC 42.3 testified, JEDEC invariably adopted a patented technology it thought was best as long as it received a RAND letter. (Kelley, Tr. 2707-09).

3030. In fact, given the existence of alternatives, there is no real probability that JEDEC would have adopted the existing standards had Rambus disclosed its intellectual property, even if it issued a RAND letter. (McAfee, Tr. 11315-316; *see* DX0377).

Rambus's Response to Finding No. 3030:

The proposed finding is contrary to the evidence. (*See* RRFF 3029).

3031. JEDEC members were opposed to the use of royalty bearing technologies in the JEDEC standards. (CCFF 300-304)

Rambus's Response to Finding No. 3031:

The proposed finding is contrary to the evidence. (*See* RRFF 300-04). The evidence shows that during the relevant period, JEDEC routinely adopted royalty-bearing patented technologies into its standards. For instance, in May 1990, JC 42.3 sent a ballot to the JEDEC Council to standardize the 256K x4 MPDRAM technology, knowing that Digital Equipment Corporation had a patent on the technology and had demanded a royalty rate of 1%. (JX 1 at 6, 24). In July 1992, JC 42.3 passed ballots to standardize 2M x8/x9 Sync DRAM in TSOP II, knowing that Motorola had an issued patent on the technology and would demand royalties. (JX 13 at 9-10, 136). Similarly, JEDEC members voted to rescind a hold on TI's Quad CAS technology knowing that TI had required and would require the payment of royalties. (RX 562 at 13; JX 25 at 5). As the long time chair of JC 42.3 testified, JEDEC invariably adopted a patented technology it thought was best as long as it received a RAND letter – which could require royalties. (Kelley, Tr. 2707-09).

3032. Given JEDEC's incentive to avoid royalties because of the price sensitivity of DRAM customers, it would have been difficult to arrive at a consensus to include Rambus's intellectual property into a standard when other commercially viable alternatives existed. (McAfee, Tr. 7492).

Rambus's Response to Finding No. 3032:

The proposed finding is misleading and not supported by the weight of the evidence. First, the evidence shows that JEDEC did not avoid royalty bearing technologies. (*See*

RRFF 3031). Second, the evidence shows that Rambus's technologies were less costly than any noninfringing alternatives and would therefore be chosen by rational DRAM manufacturers. (*See* RPF Section IX.B.3.d, IX.B.4.d). Third, though asserting that JEDEC would avoid royalty bearing technologies because of consumer price sensitivity, Complaint Counsel's economic expert admitted on cross-examination that he had made no study of the elasticity of PC consumer nor of OEM DRAM consumer demand. (McAfee, Tr. 7566, 7614).

3033. One reason why JEDEC would have a preference to avoid including patented technologies in their standards is that the incorporation of proprietary technologies when commercially viable alternatives exist can expose the industry to the threat of hold-up. (McAfee, Tr. 7495-96 ("The incorporation of proprietary technology when commercially viable alternatives exist generally exposes the industry to the threat of hold-up.")).

Rambus's Response to Finding No. 3033:

The proposed finding is misleading and not supported by the weight of the evidence. The evidence shows that JEDEC did not, in practice, avoid patented technologies, especially after receiving a RAND letter. (*See* RPF 1220-37). Moreover, the evidence shows that the DRAM industry is not subject to "hold up," because it switches technologies all the time. (*See* RPF Section X).

3034. Since a RAND letter does not specify royalty rate, firms have an incentive for *ex ante* negotiation. (McAfee, Tr. 7492-93 ("And since a RAND letter doesn't specify a royalty rate, firms are at risk when they've incorporated patented technology that the royalty rates may turn out to be very large. The RAND letter does specify "reasonable," but to a great extent "reasonable" is in the eye of the beholder. .... [T]he firms have an incentive for *ex ante* negotiation; that is to say, the firms that intend to practice the JEDEC standard have an incentive to say, 'Hey, what's this going to cost me'? That is to say, to investigate what does the word 'reasonable' mean in the RAND letter.")).

Rambus's Response to Finding No. 3034:

The proposed finding is misleading. Despite this supposed "incentive" for *ex ante*

negotiation, there is no evidence that such a negotiation has ever occurred in the DRAM industry. Moreover, in the case of Rambus, the negotiations would have been for naked licenses to patent applications. Because of the nature of patent applications, such negotiations would be difficult and costly, and they do not occur. (Teece, Tr. 10354, 10356-60).

3035. In addition, the fact that Rambus was not a manufacturer, but instead a "pure play" technology company would have given JEDEC members additional incentive to attempt to negotiate royalty rates with Rambus *ex ante* rather than *ex post.* As a pure play technology company, Rambus would not have been subject to the restrictions on royalty rates because of cross licenses that limit the royalties of other firms. (McAfee, Tr. 7493-94)

Rambus's Response to Finding No. 3035:

The proposed finding is misleading and incomplete. *Ex ante* negotiation of the sort implied by the finding are costly and do not occur. (*See* RRFF 3034). Moreover, the evidence shows that JEDEC did not engage in *ex ante* negotiations with another pure play company that had patents on one of the very technologies at issue in this case. Specifically, Mosaid is a pure play company. (Tabrizi, Tr. 9130 ("MOSAID is a design house. They don't have their fab.")). A Mosaid patent affecting the on-chip PLL technology was disclosed by Hyundai in 1995. Yet JEDEC members did not seek to negotiate with Mosaid prior to the adoption of that technology in DDr. (CX 400 (May 1999 email from Mosaid responding to RAND request and inquiring how the RAND requirement would affect its licenses). In fact, JEDEC did not ask Mosaid for a RAND letter until four years after the disclosure. (*Id.*)

3036. *Ex ante* negotiation places a limit on the exercise of monopoly power, because, *ex ante,* the users of the technology have alternatives available. (McAfee, Tr. 7494-95). Hence, the technology users will be in a stronger bargaining position than they would be after they become locked into a technology. The effect would be to change the price that is charged for the technologies. (McAfee, Tr. 7495, 11313-314; *see* DX0377).

Rambus's Response to Finding No. 3036:

The proposed finding is misleading and not supported by the weight of the evidence. The evidence shows that there were no acceptable, noninfringing alternatives *ex ante* or *ex post*. (*See* RPF Section IX.B). Moreover, even from a theoretical perspective, the position of technology users *ex ante* as opposed to *ex post* depends on switching costs. (Teece, Tr. 10707). In this case, the switching costs are not so great as to allow for the exercise of market power. (*See* RPF 1340-43).

3037. When Dr. Rapp reached his conclusions regarding the effect of Rambus's non-disclosures to JEDEC on whether JEDEC would have adopted the Rambus technologies anyway, he was not familiar with the details of the process that JEDEC went through in the real world in selecting the Rambus-claimed technologies. (Rapp, Tr. 10106-109).

Rambus's Response to Finding No. 3037:

The proposed finding is misleading. Unlike Complaint Counsel's economic expert who erroneously based his economic opinions on subjective factors such as JEDEC's perceptions (*see* RPF 1459-71), Dr. Rapp testified that he did not study the balloting or discussions within JEDEC because "the commercial viability and substitution qualities of those alternatives are independent of what got said in JEDEC." (Rapp, Tr. 10111).

3038. When Dr. Rapp reached his conclusions regarding the effect of Rambus's non-disclosures to JEDEC on whether JEDEC would have adopted the Rambus technologies anyway, he did not know whether, prior to their ultimate adoption, there was any opposition within JEDEC to the use of any of those technologies. (Rapp, Tr. 10109).

Rambus's Response to Finding No. 3038:

The proposed finding is misleading. (*See* RRFF 3037).

3039. When Dr. Rapp reached his conclusions regarding the effect of Rambus's non-disclosures to JEDEC on whether JEDEC would have adopted the Rambus technologies anyway, he did not know whether any alternatives to those technologies were discussed within JEDEC.

(Rapp, Tr. 10109).

Rambus's Response to Finding No. 3039:

The proposed finding is misleading. (*See* RRFF 3037).

3040. When Dr. Rapp reached his conclusions regarding the effect of Rambus's non-disclosures to JEDEC on whether JEDEC would have adopted the Rambus technologies anyway, he did not know what pros or cons may have been discussed within JEDEC relating to any given alternative. (Rapp, Tr. 10110).

Rambus's Response to Finding No. 3040:

The proposed finding is misleading. (*See* RRFF 3037).

3041. Before completing his expert report, Dr. Rapp did not look at the evidence relating to the process through which JEDEC made the decisions that it made in developing the relevant standards. (Rapp, Tr. 10111).

Rambus's Response to Finding No. 3041:

The proposed finding is misleading. (*See* RRFF 3037).

3042. In developing his opinions regarding the effect of Rambus's non-disclosures to JEDEC on whether JEDEC would have adopted the Rambus technologies anyway, Dr. Rapp did not give consideration to JEDEC's specific processes or rules for dealing with patent disclosure issues. (Rapp, Tr. 10116 ("Well, I understood in general terms what they were, but I didn't delve into them in forming that conclusion.")).

Rambus's Response to Finding No. 3042:

The proposed finding is misleading. (*See* RRFF 3037).

3043. When he developed his opinions as to what JEDEC would have done in a but-for world in which Rambus had made the challenged disclosures or non-disclosures, Dr. Rapp was not aware of anything in JEDEC's rules or in its procedures that might have precluded JEDEC from using Rambus' technologies, as long as they ranked higher on a cost-performance basis than all alternative technologies. (Rapp, Tr. 10119).

Rambus's Response to Finding No. 3043:

Rambus has no specific response.

3044. When he developed his opinions, Dr. Rapp was not aware of whether, in the history of JEDEC, there has ever been a situation in which a company had disclosed a patent or patent application to JEDEC and JEDEC proceeded to adopt that proprietary technology as part of its standard. (Rapp, Tr. 10119).

Rambus's Response to Finding No. 3044:

The proposed finding is misleading. (*See* RRFF 3037). Further, the evidence shows that there have been multiple situations in which a company had disclosed a patent or patent application to JEDEC and JEDEC proceeded to adopt that proprietary technology as part of its standard. (*See* RPF 1220-38).

G. The Anticompetitive Effect of Rambus's Conduct Extends Beyond the Relevant Markets.

3045. One consequence of Rambus's monopolization of the relevant technology markets is that innovation has been misdirected. (McAfee, Tr. 7174). This effect came about because royalties create a disincentive to further innovation. That is, royalties create a dampening of incentives to innovation because part of the benefits flow to Rambus in the form of increased royalty payments. (McAfee, Tr. 7174).

Rambus's Response to Finding No. 3045:

The proposed finding is not supported. First, it assumes that Rambus monopolized relevant markets, which is a legal conclusion unsupported by the evidence or the law. (*See* RPF Section XII). Second, the only evidence cited for this finding is the unsupported assertion of Complaint Counsel's economic expert who testified there was a "disincentive" for further innovation. There is no evidence, however, that actual levels of innovation have decreased. Not a single witness testified that their company did fewer design work, fewer shrinks, or devoted less money to research and development.

3046. Rambus's monopolization has caused misdirection of efforts that otherwise would have taken place. (McAfee, Tr. 7638, *in camera*) That misdirection of efforts shows up in harm to innovation insofar as technology has not been investigated to the extent that it would

otherwise have been investigated. (McAfee, Tr. 7639, *in camera*).

Rambus's Response to Finding No. 3046:

The proposed finding is not supported. (*See* RRFF 3045). There is no evidence that additional innovation would have resulted had JEDEC used alternative technologies.

3047. For example, Rambus's monopolization of the relevant technology markets quite possibly distorted investments related to asynchronous technology. (McAfee, Tr. 7640-41, *in camera*; CCFF 2230-233).

Rambus's Response to Finding No. 3047:

The proposed finding is not supported. (*See* RRFF 3045, 2230-233). The weight of the evidence shows that neither JEDEC nor the market would have adopted asynchronous technologies. (*See* RPF 893-902).

3048. The monopolization also distorted specific design investments, *i.e.*, because of Rambus's monopolization, firms in the industry over-invested in SDRAM and DDR SDRAM under the mistaken hypotheses that they were not going to be held-up for royalties. (McAfee, Tr. 7641-42, *in camera*).

Rambus's Response to Finding No. 3048:

The proposed finding is not supported. (*See* RRFF 3045). Complaint Counsel's economic expert merely testified that the level of investments "under a hypothesis of no royalties is *generally* different than the level that would prevail with royalties." (McAfee, Tr. 7642). There is no evidence that the level of investments is *actually* different from what it would have been.

3049. Innovation is also harmed because when a DRAM manufacturer performs a die shrink or when it increases its wafer size, it increases the number of chips it makes. As a consequence, the royalty payment it must pay to Rambus increases. In that sense, the total level of royalty payments acts like a tax on innovative activity. (McAfee, Tr. 7640, *in camera*).

Rambus's Response to Finding No. 3049:

The proposed finding is not supported. (*See* RRFF 3045). Further, Rambus's royalties are based on selling price; thus, even though a manufacturer produces more chips per wafer, its royalty payments may go down.

3050. Another anticompetitive effect of Rambus's monopolization of the relevant technology markets is the threat of increased prices for the physical DRAM products. (McAfee, Tr. 7175). This effect arises because, in the long-run, the royalty costs can be expected to be passed on to consumers in the form of higher DRAM prices and lower DRAM output. (McAfee, Tr. 7176).

Rambus's Response to Finding No. 3050:

The proposed finding is not supported. (*See* RRFF 3045). Complaint Counsel's economic expert testified that a royalty might "produce a disincentive to further plant building, to going to a larger wafer size and other means of producing more output in the future." (McAfee, Tr. 7176). There is no evidence that Rambus's royalties have or will cause such effects. No witness or document from any DRAM manufacturer stated that Rambus's royalties would curtail their output in any way.

3051. Although, at present, there has not yet been an observable direct impact on DRAM supply and DRAM pricing as a result of Rambus's monopolization of the relevant technology markets, over the long-run, the increased costs due to the royalties paid by DRAM manufacturers can be expected to increase the prices of DRAM. (McAfee, Tr. 7645-46, *in camera*)

Rambus's Response to Finding No. 3051:

The proposed finding is not supported. (*See* RRFF 3045, 3050).

3052. Still another effect of the monopolization is that it increased the difficulty of reaching consensus within JEDEC about whether to develop a new standard and what it should be. This increased difficulty creates costly delay. (McAfee, Tr. 7644, *in camera*).

Rambus's Response to Finding No. 3052:

The proposed finding is not supported. (*See* RRFF 3045). There is no evidence of any increased difficulty of reaching consensus within JEDEC and no evidence of any delay. In fact, the evidence is to the contrary. According to Desi Rhoden, Chairman of JEDEC, Rambus's assertion of its intellectual property right has had no effect on JEDEC: "Rambus is certainly not the first to declare IP in this or any other industry and none has had any net negative impact on standardization. The end users still demand standardization (what they are really asking for is low price). JEDEC has continued to work through several actions amazingly similar to this one." (CX2767 at 4).

3053. Still another consequence of Rambus's monopolization of the relevant technology market is that it threatens to undermine industry confidence in open standards and the standards process. (McAfee, Tr. 7176).

Rambus's Response to Finding No. 3053:

The proposed finding is not supported. (*See* RRFF 3045). There is no evidence of any effect on participation in standards-setting or use of industry standards. In fact, the evidence is to the contrary. According to Desi Rhoden, Chairman of JEDEC, Rambus's assertion of its intellectual property right has had no effect on JEDEC: "Rambus is certainly not the first to declare IP in this or any other industry and none has had any net negative impact on standardization. The end users still demand standardization (what they are really asking for is low price). JEDEC has continued to work through several actions amazingly similar to this one." (CX2767 at 4).

3054. Rambus's hold-up of the DRAM industry threatens the standardization process because it demonstrated that the benefits of standard-setting potentially could be captured by one of the market participants. In the future, this could discourage standard-setting within JEDEC.

(McAfee, Tr. 7646-47, *in camera*; CCFF 2049).

Rambus's Response to Finding No. 3054:

The proposed finding is not supported. (*See* RRFF 3045, 3053).

3055. In addition, resources directed toward working around Rambus's patented technology and creating a subsequent standard delays the roll out of the subsequent standard. (McAfee, Tr. 7644-45, *in camera*).

Rambus's Response to Finding No. 3055:

The proposed finding is not supported. (*See* RRFF 3045). There is no evidence of any delay created by effort to work around Rambus's patents.

3056. Another competitive effect of Rambus's monopolization of the relevant technology markets is the actual and threatened future distortions to competition in those markets. (McAfee, Tr. 7638-639, *in camera*).

Rambus's Response to Finding No. 3056:

The proposed finding is not supported. (*See* RRFF 3045). There is no evidence of any actual or threatened distortions to competition in any relevant markets.

3057. Another effect of Rambus's monopolization of the relevant technology markets is the incurrence of litigation costs. Litigation effort deploys resources that otherwise would have available for other purposes. (McAfee, Tr. 7642, *in camera;* CCFF 1995-2032).

Rambus's Response to Finding No. 3057:

The proposed finding is not supported. (*See* RRFF 3045).

3058. Another effect of the monopolization of the relevant technology markets is the diversion of resources that some firms have undertaken to design around Rambus's patented technologies. (McAfee, Tr. 7643, *in camera*).

Rambus's Response to Finding No. 3058:

The proposed finding is not supported. (*See* RRFF 3045). There is no evidence of any diversion of resources to design around Rambus's patents.

3059. Another competitive effect of Rambus's monopolization of the relevant technology markets is increased market uncertainty. (McAfee, Tr. 7643, *in camera*) From an economic standpoint, uncertainty is inherently costly because it creates difficulties to making good decisions. (McAfee, Tr. 7643, *in camera*).

Rambus's Response to Finding No. 3059:

The proposed finding is not supported. (*See* RRFF 3045). There is no evidence of any increased uncertainty.

3060. Rambus's monopolization of the relevant technology markets has increased the uncertainty prevailing in the marketplace with respect to what the royalties would be, how long they would continue to be paid. The monopolization has also created uncertainty regarding the overall future of standards and their adoption. (McAfee, Tr. 7644, *in camera;* CCFF 2033-2048).

Rambus's Response to Finding No. 3060:

The proposed finding is not supported. (*See* RRFF 3045). There is no evidence of any increased uncertainty regarding "the overall future of standards and their adoption."

3061. Paragraphs 3061 - 3099 are unused.

XIV. A Broad Remedy Is Necessary.

A. The Most Appropriate Available Remedy Is To Prohibit Rambus From Enforcing Any Patents With A Priority Date Prior to June 18, 1996 Against JEDEC-Compliant DRAMs.

3100. The harm resulting from Rambus's conduct amounts to hundreds of millions of dollars per year. (CCFF 3101-3102).

Rambus's Response to Finding No. 3100:

The proposed finding is misleading and unsupported. The evidence shows that had Rambus made the additional disclosures that Complaint Counsel contend should have been made, JEDEC would have adopted Rambus's technologies. (*See* RPF 1147-1245). If JEDEC had done so without seeking a RAND letter (which is a definite possibility (*see* RPF 1159-82)), as Complaint Counsel' economic expert admitted, "it would lead to the same outcome as the actual world," (McAfee, Tr. 11308), no "harm" would have flowed from Rambus's failure to make additional disclosures, and no remedy would be needed (Teece, Tr. 10320). If JEDEC did ask for a RAND letter, Rambus would given one, there would not have been any *ex ante* negotiations, and the only difference caused by Rambus's conduct would have been that Rambus would had issued a formal RAND assurance. (*See* RPF 1183-1244). But the evidence shows that Rambus's SDRAM and DDR license are consistent with JEDEC's RAND requirements (*see* RPF Section XI), and therefore no "harm" has resulted from Rambus's failure to make the additional disclosures (Teece, Tr. 10312-13). Assuming that the Court were to find that Rambus's conduct violated Section 5, therefore, the only "remedy" that could be supported is a requirement that Rambus continue to offer its licenses for the four technologies at issue as incorporated in SDRAM and DDR on RAND terms to those companies that will accept a license

without litigation.

3101. {

} (McAfee, Tr. 7650, *in camera*; see DX0245, *in camera*).

Rambus's Response to Finding No. 3101:

The proposed finding is misleading and unsupported. While Rambus received royalties from its SDRAM and DDR licenses, these royalties did not result from "the conduct" at issue in this case. The evidence shows that had Rambus made the additional disclosures Complaint Counsel contend should have been made, JEDEC and the DRAM industry would have still adopted Rambus's technologies and would still be paying the royalties that are paid for the SDRAM and DDR licenses. (*See* RRFF 3100).

3102. Another rough quantification of the effects of Rambus's conduct is to apply an approximate { } royalty rate to an approximate $20 billion value for DRAM. Applying such a royalty rate results in a rough estimate of { } million a year in royalty payments. (McAfee, Tr. 7653-54, *in camera*); see also CX1391A at 32 (showing average royalty rate increasing from 1% to 5% and annual royalty income increasing from $90 million to $3 billion); CX0527 at 1, *in camera* ({
}); CX1401 at 10, *in camera* ({
}).

Rambus's Response to Finding No. 3102:

The proposed finding is misleading and unsupported. (*See* RRFF 3101).

3103. In assessing what remedies should be to address exclusionary conduct, an economist first asks whether the world can be restored to what it would have been absent the anticompetitive conduct. (McAfee, Tr. 7510).

Rambus's Response to Finding No. 3103:

Rambus has no specific response.

3104. Restoration of the world cannot be achieved because almost a decade's worth of investments in the existing technologies has already occurred. (McAfee, Tr. 7511) An installed base of SDRAM and DDR SDRAM in the devices and complementary devices to those technologies has already been developed. (McAfee, Tr. 7513) Those investments have already been made. There is no way to undo the existence of those investments today. (McAfee, Tr. 7513).

Rambus's Response to Finding No. 3104:

The proposed finding is not supported by the weight of the evidence. The evidence shows that had Rambus made the additional disclosures Complaint Counsel contend should have been made, JEDEC and the DRAM industry would have still adopted Rambus's technologies and therefore would have made the same investments they have made in the real world. (*See* RRFF 3100)

3105. In addition, investments in alternatives like asynchronous technology were not made because SDRAM was believed to be a better alternative than it proved to be, because it was believed not to carry intellectual property from Rambus. (McAfee, Tr. 7516).

Rambus's Response to Finding No. 3105:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 3104).

3106. Because the first best remedy is unacceptable, one must look for a second best remedy, short of restoring the world to the way it would have been. (McAfee, Tr. 7517).

Rambus's Response to Finding No. 3106:

The proposed finding is not supported by the weight of the evidence. The evidence shows that no remedy is needed to restore competition; at most, the only "remedy" that could be supported is requiring Rambus to continue to offer its licenses for the four technologies at issue as incorporated in SDRAM and DDR on RAND terms to those companies that will accept a license without litigation. (*See* RRFF 3100).

3107. The "but-for" world in which Rambus discloses on a timely basis and JEDEC has

the opportunity to either select alternatives or conduct ex ante negotiations between JEDEC members and Rambus, is no longer available. (McAffee, Tr. 7512).

Rambus's Response to Finding No. 3107:

The proposed finding is misleading and incomplete. The evidence shows that had Rambus made the additional disclosures that Complaint Counsel contend should have been made, JEDEC would have still adopted the Rambus technologies and that no *ex ante* negotiations would have taken place. (*See* RPF 1147-1245).

3108. Although prohibition of enforcement of Rambus's patents against JEDEC-compliant DRAM would restore competitive pricing because they eliminate Rambus's ability to exercise monopoly power, they would not fully undo all the harmful effects. (McAfee, Tr. 7179) As a practical matter, in this case, restoration of the world to what it would have been cannot be achieved. (McAfee, Tr. 7511).

Rambus's Response to Finding No. 3108:

The proposed finding is not supported by the weight of the evidence. The evidence shows that had Rambus made the additional disclosures that Complaint Counsel contend should have been made, JEDEC would have still adopted the Rambus technologies, no *ex ante* negotiations would have taken place, JEDEC members would have negotiated licenses from Rambus at the same time they did in the real world (after Rambus's patents issued), and that Rambus's licenses for its four technologies in SDRAM and DDR comply with JEDEC's RAND requirements. (*See* RPF 1147-1245, Section XI).

3109. On economic grounds, undoing the anticompetitive harm resulting from Rambus's conduct requires undoing the monopolization itself. (McAfee, Tr. 7177).

Rambus's Response to Finding No. 3109:

The proposed finding is unclear and ambiguous.

3110. Prohibiting enforcement of the patents against JEDEC-compliant DRAM would

undo most, but not all, of the effects of the monopolization in the relevant technology markets. (McAfee, Tr. 7178-79, 7511).

Rambus's Response to Finding No. 3110:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 3100). The only "remedy" that could be supported by the evidence is a requirement that Rambus continue to offer its licenses for the four technologies at issue as incorporated in SDRAM and DDR on RAND terms to those companies that will accept a license without litigation. (*Id.*)

3111. Based on the practical considerations of the world as its exists today, on economic grounds, Rambus should be prohibited from enforcing any intellectual property that should have been disclosed, whatever that intellectual property might be. (McAfee, Tr. 7521) In particular, the second best remedy should require that Rambus be prohibited from enforcing against JEDEC-compliant DRAMs any patents filed (or based on filings) prior to June 18, 1996. (McAfee, Tr. 7518).

Rambus's Response to Finding No. 3111:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 3100). The only "remedy" that could be supported by the evidence is a requirement that Rambus continue to offer its licenses for the four technologies at issue as incorporated in SDRAM and DDR on RAND terms to those companies that will accept a license without litigation. (*Id.*) Further, the proposed finding is misleading to the extent that it implies that any remedy should extend to "any intellectual property that should have been disclosed," regardless of whether additional disclosures with regard to a particular technology would have made any difference.

3112. The remedy of prohibiting Rambus from enforcing against JEDEC-compliant DRAMs any patents filed (or based on filings) prior to June 18, 1996 will restore competitive pricing in the relevant technology markets and mitigate other anticompetitive effects. (McAfee, Tr. 7522).

Rambus's Response to Finding No. 3112:

The proposed finding is not supported by the weight of the evidence. (*See* RRFF 3100). The only "remedy" that could be supported by the evidence is a requirement that Rambus continue to offer its licenses for the four technologies at issue as incorporated in SDRAM and DDR on RAND terms to those companies that will accept a license without litigation. (*Id.*) The evidence also shows that Rambus's royalty rates for is SDRAM and DDR license are competitively priced. (*See* RPF Section XI.A).

B. The Remedy Should Extend To All Technologies Included in JEDEC-Compliant DRAMs.

3113. Rambus may hold patents containing claims that cover technologies used in SDRAMs and DDR SDRAMs other than programmable cas latency, programmable burst length, dual edged clocking, and on-chip DLL. (CCFF 3114-3182).

Rambus's Response to Finding No. 3113:

The proposed finding is irrelevant and misleading. Any remedy cannot extend to prohibit Rambus from enforcing its patents on technologies other than those for which Complaint Counsel had carried its burden of proving monopolization or attempted monopolization. As Complaint Counsel itself has recognized, this burden requires them to prove not only that Rambus failed to disclose information that it should have disclosed, but that had Rambus disclosed, acceptable alternatives existed and would have been adopted by JEDEC (CCFF Section XI.A), that industry members are now locked in to using the Rambus technologies (CCFF Section XII, XIII.A), that the particular technology competes in a relevant market (CCFF Section XIII.B), that Rambus has acquired monopoly power in the relevant market due to its failure to make additional disclosures to JEDEC (CCFF Section XIII.D), and that Rambus's

conduct was anticompetitive (CCFF Section XIII.E). The proposed finding and those that follow purport to extend Complaint Counsel's remedy to encompass technologies for which there is no evidence of alternatives, no evidence of lock in, no evidence of relevant markets, no evidence of monopoly power, no evidence of anticompetitive conduct, and, as cited below, no evidence that Rambus failed to disclose any information that it should have disclosed.

3114. Rambus has asserted that various features contained in SDRAMs and DDR SDRAMs, in addition to the four technologies identified in the complaint, are Rambus innovations. (CX1363 at 1 (listing "Multi-bank architecture" and "Doubled banks" as Rambus innovations); *id*. at 3 (list indicating that "Low voltage swing signaling" and "Source synchronous signaling" are Rambus innovations contained in DDR SDRAMs); CX1371 at 5 (informing nVidia that "Rambus innovations" include "Low voltage swing signaling" and "Source synchronous signaling"); CX1383 at 4 (informing ATI of same)).

Rambus's Response to Finding No. 3114:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113).

3115. {

}

(CX1681 at 3, *in camera*) ({

}); CX1680 at 16, 19, 24, *in camera*) ({

}); CX1687 at 8, 12, 28, *in camera*) ({
})).

Rambus's Response to Finding No. 3115:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113). That Rambus's licenses incorporate { } is irrelevant because the evidence cannot support a finding of monopolization or attempted monopolization with regard to other technologies. (*See* RRFF 3113).

3116. Rambus has stated publicly that it would seek to enforce patents that allegedly cover technologies used in SDRAMs and DDR SDRAMs that they have not yet asserted in litigation to date. (CX1888 ("In addition [to the 16 or so U.S. and European patents asserted against Infineon, Hyundai and Micron], Rambus holds newly issued U.S. and European patents covering Rambus inventions used by SDRAMs and DDR SDRAMs that have not yet been asserted in any litigation and are not impacted by the [Infineon trial court's] decision."); CX1382 at 29-30 (In a presentation in which Rambus identified that one way to "win" would be to collect royalties on competitive alternatives, Rambus included a chart showing that Rambus's filed U.S. patent applications rose to approximately 200 and issued U.S. patents rose to 94 in 2000.); CX1403 at 30 ("Virginia decision involved only 4 patents; we may have others which are used by SDRAM/DDR.")).

Rambus's Response to Finding No. 3116:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113).

3117. Rambus recently has obtained additional patents that appear to cover a technology that Rambus has not yet asserted patents against. For example, on October 22, 2002 the PTO issued Rambus patent 6,470,405 (the '405 patent), which includes a claim relating to "initiating the precharge operation automatically after the write operation is initiated." (CX1545 at 45).

Rambus's Response to Finding No. 3117:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113). Moreover, the selective quotation from claim 1 of the '405 patent misrepresents the subject matter covered by the claim. Claim 1 contains a number of limitations besides the one quoted such as, "detecting an external strobe signal, wherein the external strobe signal indicates when to begin sampling data." Complaint Counsel have made no showing that Rambus was obligated to make any disclosure to JEDEC with respect to the '405 patent.

3118. The additional technologies as to which Rambus may hold patent rights include technologies that Rambus observed presented at JEDEC while it was a JEDEC member. (CCFF 3123-3124, 3139-3140, 3153-3154, 3163, 3179).

Rambus's Response to Finding No. 3118:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113).

3119. The additional technologies as to which Rambus may hold patent rights include technologies that Rambus representatives, including Richard Crisp, believed might be covered by claims in Rambus's pending patent applications, or could be covered by claims that Rambus could file as amendments to its pending patent applications, at the time that Rambus was a JEDEC member. (CCFF 3132-3133, 3143-3146, 3156-3157, 3166-3170, 3177, 3179).

Rambus's Response to Finding No. 3119:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113).

3120. At the time it was a JEDEC member, Mr. Crisp did not disclose to JEDEC that he believed Rambus had pending patent applications containing claims, or that Rambus could amend its pending patent applications to add claims, covering these additional technologies. (CCFF 3136, 3150, 3160, 3173, 3180).

Rambus's Response to Finding No. 3120:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113).

1. Low Voltage Swing Signaling.

3121. In late 1991, Mr. Crisp had consulted with Rambus concerning Rambus patent applications and the use of "low swing signals on DRAM." (CX1932; CX3125 at 279-80 (Vincent, Dep.) (By December 1991, Rambus may have already drafted patent applications containing claims covering voltage swing levels as low as 2 volts for use with DRAMs.)).

Rambus's Response to Finding No. 3121:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113). In addition, the proposed finding and those that follow regarding low voltage swing signaling are irrelevant because the evidence: (1) does not show that any of the presentations cited by the proposed findings were incorporated in SDRAM or even balloted for inclusion; and (2) does not show that Rambus had any patents or patent applications with claims covering any of the presentations. (*See* RRFF 545). There is no evidence, therefore, that Rambus should have disclosed any information regarding low voltage swing signaling. (*Id.*) Moreover, the proposed finding that Rambus "*may* have drafted patent applications containing claims covering voltage swing levels

as as 2 volts" is, concededly, entirely speculative and the figure of "2 volts" is based on a note of Mr. Vincent's which refers to a termination voltage, not a voltage swing. (CX1932; CX3125, Vincent Dep. at 279-80).

3122. In late 1991-January 1992, Mr. Vincent continued to work with Mr. Crisp and others at Rambus as he drafted and filed patent claims. (CX1933 at 1-9; CX3125 at 279-80, 287-88 (Vincent, Dep.); Crisp, Tr. 3027-28).

Rambus's Response to Finding No. 3122:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3121).

3123. At the February 27, 1992, JC 42.3 meeting, the NEC, Fujitsu, Mosaid, Sun, and Intel proposed a low-voltage swing signaling interface. (JX0012 at 39, 76, 104, 111, 113; Crisp, Tr. 3045-46). At this same meeting, the JC-42.3 Committee discussed GTL technology for use with SDRAM. (JX0012 at 36, 56-58, 60, 101-02, 104, 111).

Rambus's Response to Finding No. 3123:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3221).

3124. On February 27, 1992, Billy Garrett attended a JC 42.3 meeting in which he witnessed SDRAM proposals to the Subcommittee, including low voltage swing signaling relating to LVTTL and GTL technology. (JX0012 at 36-37; CX0672 at 1; Crisp, Tr. 3045-46). After attending the meeting, Mr. Garrett distributed an e-mail to Rambus staff titled, "JEDEC Meeting Notes 2/27, 2/28," explaining that Jedec had discussed these and other technologies at the February 1992 meeting. (CX0672 at 1).

Rambus's Response to Finding No. 3124:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3221).

3125. In his e-mail to Rambus staff about the February 1992 Jedec meeting, Mr. Garrett recognized an opportunity for Rambus to either influence the voltage standard or "use [Rambus] patents to keep current-mode interfaces off of DRAMs." (CX0672 at 1).

Rambus's Response to Finding No. 3125:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3221).

3126. A week after this meeting, Rambus's outside patent counsel, Lester Vincent, filed

a preliminary amendment to a patent application concerning low voltage swing signals. (CX0672 at 1; Crisp, Tr. 3046).

Rambus's Response to Finding No. 3126:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3221).

3127. On March 25, 1992, Rambus Vice President Allen Roberts and outside patent counsel Lester Vincent discussed "JEDEC" and the "need [for] preplanning before accuse others of infringement." (CX1941; CX3125 at 296-302 (Vincent, Dep.)). Mr. Vincent's notes from that meeting contain the reference "Jedec Committee = > Standards for DRAMs" and reflect discussion of "Advising JEDEC of patent applications." (CX1941).

Rambus's Response to Finding No. 3127:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3221).

3128. On March 27, 1992, Mr. Richard Crisp and Vice President Roberts met in person with Mr. Vincent. (CX3125 at 310, 311-313 (Vincent, Dep.; CX1942). Mr. Crisp or Mr. Roberts informed Mr. Vincent that "Rambus attended [a] meeting with a hundred others where JEDEC's proposal to establish [a] standard for small swing signals for sync DRAM was discussed." (CX1942 at 1; CX3125 at 312-313 (Vincent, Dep.)).

Rambus's Response to Finding No. 3128:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3221).

3129. At the April 8, 1992, Special SDRAM Task Group meeting, the JC 42.3 Subcommittee considered SDRAM proposals that included low voltage swing signaling such as LVTTL and/or GTL. (CX0034 at 32 (IBM), 33 (NEC, Fujitsu), 35 (Samsung, Hitachi), 36 (Mitsubishi).

Rambus's Response to Finding No. 3129:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3221).

3130. At the May 7, 1992, JC 42.3 meeting, the Subcommittee considered SDRAM proposals that included low voltage swing signaling such as LVTTL and/or GTL. (CX0034 at 59 (NEC), 122-123 (Fujitsu)).

Rambus's Response to Finding No. 3130:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3221).

3131. At the September 16-17, 1992, JC 42.3 meeting, the Subcommittee considered Sun's 15 meg SDRAM specification which included low voltage swing signaling (CX0042 at 31 ("It is proposed that LVTTL be used for the I/O drivers and receivers.")).

Rambus's Response to Finding No. 3131:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3221).

3132. On June 18, 1993, Mr. Fred Ware of Rambus sent an e-mail stating that he had spoken with Lester Vincent and he was including a list of the current status of the additional claims that Rambus wanted to file on the original patent. Included on the list was a "DRAM using low-voltage-swing signal levels. . . This claim would be directed against GTL technology." (CX0703 at 1; Crisp, Tr. 3165-66 (testifying that CX0703 refreshed his recollection that claims on low voltage swing signaling had been filed by the date of the document, which was June 18, 1993)).

Rambus's Response to Finding No. 3132:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3221).

3133. On July 9, 1993, Mr. Crisp and Mr. Ware met with Mr. Vincent to discuss the status of Rambus's patent claims. (CX3126 at 447-449 (Vincent, Dep.); CX1963 at 1-4). Mr. Vincent's handwritten notes from that meeting indicate that claims on low voltage swing signaling had already been filed. (CX1963 at 4; see also CX3126 at 449-52 (Vincent, Dep.) (Mr. Vincent recalled discussing low voltage swing signaling claims prior July 1993 and may have already filed some low voltage swing signaling claims by then)).

Rambus's Response to Finding No. 3133:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3221).

3134. On May 24, 1995, after being asked by Mr. Kelley to inform the JC-42.3 Subcommittee as to whether Rambus had patents relating to the SyncLink presentation at JEDEC, Mr. Crisp stated to Rambus executives and others (but not to the JC-42.3 Subcommittee), "As far as intellectual property issues go here are a few ideas: . . . 2. DRAM with low swing signaling [sic]." (CX0711 at 68, 73; Crisp, Tr. 3268-71).

Rambus's Response to Finding No. 3134:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3221).

3135. Jedec included low swing signaling technologies in SDRAM and DDR SDRAM standards. (CX0234 at 116, 189-95)

Rambus's Response to Finding No. 3135:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3221).

3136. Mr. Crisp never informed Jedec that Rambus believed it could obtain patent coverage over low voltage swings as they were being discussed at JEDEC. (Crisp, Tr. 3455; *see* DX0028).

Rambus's Response to Finding No. 3136:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3221).

3137. Rambus may intend to assert patents relating to low voltage swing signaling against manufacturers or users of DDR SDRAMs. (CX1363 at 3 (list indicating that "Low voltage swing signaling" is a Rambus innovation contained in DDR SDRAMs); CX1371 at 5 (informing nVidia that "Rambus innovations" include "Low voltage swing signaling"); CX1383 at 4 (informing ATI of same)).

Rambus's Response to Finding No. 3137:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3221).

2. Dual Bank Design.

3138. Mr. Crisp testified that "DRAM with multiple open rows" describes a technology that is related to but broader than the two bank feature discussed within JEDEC. (CX0686; Crisp, Tr. 3122).

Rambus's Response to Finding No. 3138:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113). In addition, the proposed finding and those that follow regarding dual bank design are irrelevant because the evidence does not show that Rambus had any patents or patent applications with claims covering any of the presentations. (*See* RRFF 549). There is no evidence, therefore, that Rambus should have disclosed any information regarding dual bank design. (*Id.*)

3139. At the February 1992 JC 42.3 meeting that Billy Garrett attended, the Subcommittee addressed the topic of "multiple [active] subarrays" in two presentations (JX0012 at 34, 37) and multibank or dual bank design in other presentations (*See, e.g., id.* at 60). At the

February 27, 1992, JC 42.3 meeting, the Subcommittee considered proposals for multibank, or dual bank, design from NEC, Mitsubishi, Fujitsu, and Sun. (JX0012 at 39, 60, 76, 110; CX0672 at 1 (Mr. Garrett's notes from this meeting indicate that JEDEC had reached a "general agreement on two banks.")).

Rambus's Response to Finding No. 3139:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3138).

3140. At the May 7, 1992, JC 42.3 meeting, the Subcommittee considered SDRAM proposals that included both dual bank design and low voltage swing signaling such as LVTTL and/or GTL. (CX0034 at 59 (NEC), 122-123 (Fujitsu)). During that meeting, Mr. Kelley of IBM, prompted by Mr. Meyer of Siemens, asked Mr. Crisp whether Rambus might have patent claims that related to dual bank design. (CX2089 at 130, 131, 136-137 (Meyer, Infineon Tr.). Mr. Crisp gave no verbal response, but rather shook his head. Mr. Kelley then commented to the group that "they don't have anything to say about that." (*Id.*).

Rambus's Response to Finding No. 3140:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3138).

3141. In his email from this JEDEC meeting, Mr. Crisp continued to monitor the progress of dual bank design technology. He wrote in his email back to Rambus that "2 banks appear to still be the route the suppliers are leaning." (CX0673 at 1).

Rambus's Response to Finding No. 3141:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3138).

3142. At the September 16-17, 1992, JC 42.3 meeting, the Subcommittee considered Sun's 15 meg SDRAM specification which included a dual bank design. (CX0042 at 30 ("The 4M x 4 device is organized internally as two banks.")).

Rambus's Response to Finding No. 3142:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3138).

3143. On September 25, 1992, Mr. Crisp met with Mr. Vincent to discuss what claims to add to patent applications that were already on file with the Patent and Trademark Office. (CX1949 at 1; Crisp, Tr. 3096-98). The first item in Mr. Vincent's notes, with a star next to it, referred to a DRAM with "multiple open row addresses." (*Id.*). Under the first three items in his notes, Mr. Vincent wrote, "So cause problems w/ synch DRAM and Ramlink." (*Id.*) According to Mr. Crisp, multiple open row addresses describes a concept that is similar to multiple open

banks or multiple banks. (Crisp, Tr. 3097).

Rambus's Response to Finding No. 3143:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3138).

3144. On February 9, 1993, Richard Crisp responded to a Fred Ware email, in which Ware asked Crisp to provide "a list of claims which were under consideration for addition to the original patent." Among other things, Crisp requested that Ware see that a claim be written up to cover a "DRAM with multiple open rows". (CX0686 at 1). This technology is related to but broader than two banks as discussed within JEDEC. (Crisp, Tr. 3120-22).

Rambus's Response to Finding No. 3144:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3138).

3145. On June 18, 1993, an e-mail from Fred Ware indicated that Rambus was considering claims covering "DRAM with multiple open rows" that would be "directed against SDRAMs." CX0702 at 1). Mr. Vincent was doubtful, however, as to whether the claims could be extracted from the specification of the '898 application. (*Id.*).

Rambus's Response to Finding No. 3145:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3138).

3146. On May 5, 1994, Allen Roberts wrote a letter to Mr. Vincent in which he suggested the addition of new patent claims to existing or new divisional applications. (CX0734 at 1). Mr. Roberts, for example, suggested that Mr. Vincent add claims on the use of "[m]ultiple and independently controlled and addressed internal DRAM memory regions (banks)." (*Id.*).

Rambus's Response to Finding No. 3146:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3138).

3147. Allen Roberts sent a copy of a Vincent's draft preliminary amendment for the '646 application that Roberts characterized as "Lester's attempt to write the claims for the MOST/SDRAM defense" to Rick Barth, Fred Ware and John Dillon. (CX0745 at 1).

Rambus's Response to Finding No. 3147:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3138).

3148. Mr. Vincent's associate, Scot Griffin, filed a Preliminary Amendment to

Application 08/222,646. (Cx1466 at 19). In this application, claim 182 refers to "a plurality of independently addressable memory sections . . ." (CX1466 at 12).

Rambus's Response to Finding No. 3148:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3138).

3149. Both JEDEC SDRAM and DDR SDRAM standards are based on a multiple bank design. (CX0234 at 116, 145).

Rambus's Response to Finding No. 3149:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3138).

3150. Mr. Crisp never informed Jedec that Rambus believed it could obtain patent coverage over dual bank design as it was being discussed at Jedec. (Crisp, Tr. 3456; *see* DX0028).

Rambus's Response to Finding No. 3150:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3138; *see also* RRFF 550).

3151. Rambus may intend to assert patents relating to low voltage swing signaling against manufacturers or users of SDRAMs and DDR SDRAMs. (*See* CX1363 at 1 (listing "Multi-bank architecture" and "Doubled banks" as Rambus innovations)).

Rambus's Response to Finding No. 3151:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3138).

3. Auto-Precharge.

3152. At a number of meetings during the course of 1992, the JC-42.3 Subcommittee discussed using the auto-precharge technology in the SDRAM standard. (February 1992: JX0012 at 37, 39 (NEC), 76 (Fujitsu), 94 (Toshiba), 108 (Sun); April 1992: CX0034 at 32 (IBM), 33 (NEC), 35 (Hitachi); May 1992: CX0034 at 6, 150).

Rambus's Response to Finding No. 3152:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113). In addition, the

proposed finding and those that follow regarding auto precharge are irrelevant because the evidence shows that Rambus only had claims pending regarding auto precharge for a brief four month period, which occurred two years after the presentations cited by Complaint Counsel on this technology. (*See* RRFF 552). There is no evidence, therefore, that Rambus should have disclosed any information regarding auto precharge. (*Id.*)

3153. At the September 16-17, 1992, JC 42.3 meeting, the Subcommittee considered Sun's 15 meg SDRAM specification which included an "autoprecharge" option. (CX0042 at 45).

Rambus's Response to Finding No. 3153:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3152).

3154. On September 21, 1992, Mr. Garrett and Mr. Crisp jointly sent to all Rambus executives and staff an e-mail summarizing the September 16-17, 1992 JC 42.3 meeting that they had just attended. (CX0680 at 1). The e-mail informed Rambus representatives that the Jedec Subcommittee discussed how to implement auto-precharge during this meeting. (*Id.* at 2; Crisp, Tr. 3095-96 (testifying that CX0680 refreshed his recollection that auto-precharge had been discussed at the September 1992 JC 42.3 meeting)).

Rambus's Response to Finding No. 3154:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3152).

3155. JEDEC included the auto-precharge feature in the SDRAM standard. (CX0234 at 145, 151 ("[Section] 3.11.5.1.5. [ ] gives the logic function used to activate the AUTO-PRECHARGE function.")).

Rambus's Response to Finding No. 3155:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3152).

3156. On May 5, 1994, Mr. Roberts wrote a letter to Mr. Vincent that contained a list of ways to "enhance [Rambus's] claim coverage." (CX0734 at 1). One of the ideas that Mr. Roberts proposed to Mr. Vincent for enhanced claim coverage was, "Selective precharging of banks following an access to improve access time." (*Id.*).

Rambus's Response to Finding No. 3156:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3152).

3157. On June 16, 1994, John Dillon wrote to the Rambus e-mail "exec" group, Fred Ware, and Richard Barth that, "I believe we might be able to claim this idea." (CX0738 at 1). At that time, Rambus may have only had a narrow claim that related to auto-precharge. (*Id.*). Mr. Dillon recommended filing a broader claim that the one that was pending at the time that would cover "auto-precharge for *any* DRAM." (*Id.*). He believed that "patenting this feature would have high harassment value." (*Id.*).

Rambus's Response to Finding No. 3157:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3152).

3158. Allen Roberts sent a copy of Vincent's draft preliminary amendment for the '646 application that Roberts characterized as "Lester's attempt to write the claims for the MOST/SDRAM defense" to Rick Barth, Fred Ware and John Dillon. (CX0745 at 1).

Rambus's Response to Finding No. 3158:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3152).

3159. Mr. Vincent's associate, Scot Griffin, filed a Preliminary Amendment to Application 08/222,646. (CX1466 at 19). In this application, claim 193 refers to a "control signal specif[ying] that the plurality of sense amps are to precharge the columns of the array of memory cells immediately after the data has been transferred." (CX1466 at 15).

Rambus's Response to Finding No. 3159:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3152).

3160. Mr. Crisp never informed anyone at Jedec that Rambus believed it could obtain patent coverage over auto-precharge as it was being discussed at Jedec. (Crisp, Tr. 3457; *see* DX0028).

Rambus's Response to Finding No. 3160:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3152).

3161. Rambus may intend to assert patents relating to auto-precharge against manufacturers or users of SDRAMs and DDR SDRAMs. (CX1539 at 964, 967 (recently filed preliminary amendment seeking to add claim 151 which refers to a "plurality of sense amplifiers

[that] are automatically precharged after the data is sensed" and claim 166 which refers to "precharging the plurality of sense amplifiers [ ] automatically after the data has been sensed.")).

Rambus's Response to Finding No. 3161:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3152).

3162. On October 22, 2002 the PTO issued Rambus patent 6,470,405 (the '405 patent), which includes a claim relating to "initiating the precharge operation automatically after the write operation is initiated." (CX1545 at 45).

Rambus's Response to Finding No. 3162:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113). Moreover the selective quotation from claim 1 of the '405 patent mischaracterizes the subject matter of that claim. (*See* RRFF 3117).

4. Externally Supplied Reference Voltage.

3163. At the February 27, 1992, JC 42.3 meeting, Samsung proposed an externally supplied reference voltage. (JX0012 at 58; Crisp, Tr. 3043-3044 (acknowledging that "vref" refers to externally supplied reference voltage)).

Rambus's Response to Finding No. 3163:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113). In addition, the proposed finding and those that follow regarding externally supplied reference voltage are irrelevant because the evidence: (1) does not show that any of the presentations cited by the proposed findings were incorporated in SDRAM or even balloted for inclusion; (2) does not show that an externally supplied reference voltage is part of the SDRAM standard; and (3) does not show that Rambus had any patents or patent applications with claims covering any of the presentations. (*See* RRFF 555). There is no evidence, therefore, that Rambus should have disclosed any information regarding externally supplied reference voltage. (*Id.*)

3164. Mr. Garrett recorded in his notes at this meeting that Jedec had discussed the use of an externally supplied reference voltage. (CX0672 at 1 ("As for I/O, everyone agrees that at about 100MHZ signals will have to be terminated, that it cannot be rail-to-rail, and that it cannot rely on an internal Vref (i.e., that there would be an external Vref).")).

Rambus's Response to Finding No. 3164:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3163).

3165. In 1992, JEDEC had considered both GTL and CTT signaling technology. At the February 1992 JC 42.3 meeting that Billy Garrett attended and informed Rambus staff about, the Subcommittee had discussed GTL technology for use with SDRAM. (JX0012 at 36, 56-58, 60, 101-02, 104, 111 (GTL technology)). At the May 7, 1992, JC 42.3 meeting, Fujitsu gave an SDRAM presentation that outlined set-up and hold timing details for "CTT I/O" signaling technology. (CX0034 at 139, 141).

Rambus's Response to Finding No. 3165:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3163).

3166. On February 20, 1993, Mr. Crisp recommended to Fred Ware in an e-mail that "we get [one additional claim] on the old patents [ ] where the voltage reference is provided to a dynamic memory chip for setting the input receiver's thresholds." (CX0691 at 1; Crisp, Tr. 3123-24 (confirming that this language is "probably very similar [to], if [ ] not the same" as externally supplied reference voltage)). According to Mr. Crisp, "[t]his should help confound the GTL effort." (CX0691 at 1).

Rambus's Response to Finding No. 3166:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3163).

3167. On June 18, 1993, Fred Ware suggested patenting the use of an externally supplied reference voltage in a way that was "directed against CTT technology " and communicating that idea to Mr. Vincent. (CX0702 at 1; Crisp, Tr. 3164-65 (confirming that Rambus considered adding claims to externally supplied reference voltage that were directed against CTT technology)).

Rambus's Response to Finding No. 3167:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3163).

3168. Mr. Vincent's notes from the July 1993 meeting also refer to "externally supplied reference voltage." (CX1963 at 4).

Rambus's Response to Finding No. 3168:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3163).

3169. At the May 1994 JC-42.3 Subcommittee meeting, Mr. Crisp observed various presentations regarding specific SDRAM configurations. Mr. Crisp wrote in an e-mail to Mark Johnson, an attorney for Rambus, "Note that many of the SDRAMs use an externally supplied reference voltage in the input buffers. I believe we have a claim we added to cover this configuration. We should make note of this." (CX0711 at 26, 27; Crisp, Tr. 3190-91).

Rambus's Response to Finding No. 3169:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3163).

3170. Later in the same May 1994 meeting, Mr. Crisp noted, "(again we need to check claims about 'DRAM with input receivers using an externally supplied reference voltage'). We may be able to slow down or stop (or at least collect from) all of the CTT, GTL and HSTL devices if this claim is allowed (Allen, I believe this was one of the claims you, Lester, Tracy and I wrote up in late '91, right?)." (CX0711 at 26, 31; Crisp, Tr. 3192-93 (confirming that CTT, GTL, and HSTL "were acronyms for signaling technologies that were just various different either standards or proposals for standards.")).

Rambus's Response to Finding No. 3170:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3163).

3171. On March 14, 1995, Fujitsu gave a presentation on "STBUS" signaling technology to the JC 16 Subcommittee. (CX0711 at 53, 54; *see also* CX0082 at 13). In an e-mail to Rambus executives and others, Mr. Crisp stated that Rambus had claims that anticipated Fujitsu's STBUS proposal because it was a proposal for a current source device that relied on an externally supplied reference voltage. (CX0711 at 53, 54 ("Taken along with the fact that they rely on an externally bussed reference (this should be anticipated by some of our claims), I would say that proposal may well infringe our work."); Crisp, Tr. 3241 (confirming that the reference to an externally bussed reference is a reference to an externally bussed reference voltage)).

Rambus's Response to Finding No. 3171:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3163).

3172. JEDEC standardized pinouts for both SDRAM and DDR SDRAM parts that provide a pin that can be used, as an option, for an externally supplied reference voltage. (*See, e.g.,* CX0234 at 84 (pin 40); 85 (pin 40); 86 (pin 49); 87 (pin 49)).

Rambus's Response to Finding No. 3172:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3163).

3173. Mr. Crisp never informed Jedec that Rambus believed it could obtain patent coverage over the use of an externally supplied reference voltage as it was being discussed at Jedec. (Crisp, Tr. 3456; *see* DX0028).

Rambus's Response to Finding No. 3173:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3163).

3174. It is unclear whether Rambus might intend to assert patents relating to externally supplied reference voltage against manufacturers or users of SDRAMs and DDR SDRAMs because, although the feature is included as an option in the JEDEC standards, the externally supplied reference voltage feature is rarely used. (Lee, Tr. 11034-35).

Rambus's Response to Finding No. 3174:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3163).

5. Source Synchronous Clocking.

3175. At the April 1992 JC-42.3 Special Task Group meting, Hitachi raised the issue of source synchronous clocking. (CX1708 at 2 ("Hitachi brought up the issue of source synchronous clocking."); Crisp, Tr. 3053-54 (recalling that a discussion on source synchronous clocking had taken place at this meeting)).

Rambus's Response to Finding No. 3175:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113). In addition, the proposed finding and those that follow regarding source synchronous clocking are irrelevant because the evidence does not show that Rambus had any patents or patent applications with claims covering any of the presentations. (*See* RRFF 554). There is no evidence, therefore, that Rambus should have disclosed any information regarding source synchronous clocking. (*Id.*)

3176. In an e-mail sent to all Rambus executives, among others, Mr. Crisp indicated that he thought that source synchronous clocking was a Rambus idea. (CX1708 at 2 ("It appears that someone inside Hitachi is believing that we have some good ideas!")).

Rambus's Response to Finding No. 3176:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3175).

3177. On September 25, 1992, Mr. Crisp met with Mr. Vincent to discuss claims to be added to Rambus's pending divisional applications. Mr. Vincent's handwritten notes reflect an instruction, "must claim source-synch clocking." (CX1949 at 5).

Rambus's Response to Finding No. 3177:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3175).

3178. By March 15, 1995, Rambus may have already had patent claims that related to source synchronous clocking. (CCFF 3179).

Rambus's Response to Finding No. 3178:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3175).

3179. During the March 15, 1995 JC 42.3 meeting, Mr. Crisp recorded a Fujitsu representative's suggestion that it would be necessary to use two clocks, a clock-in and clock-out, for high speed operation. (CX0711 at 58). In an e-mail sent to Rambus executives and others, Mr. Crisp stated, "It appears that they are starting to figure out that we have a very good idea with respect to source synchronous clocking. Of course they may get in to patent trouble if they do this." (*Id.*; Crisp, Tr. 3247-48 (confirming that what he had written to Rambus executives, in March 1995, was that Fujitsu might get into patent trouble if they used source synchronous clocking)).

Rambus's Response to Finding No. 3179:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3175).

3180. Mr. Crisp never informed anyone at JEDEC that Rambus believed it could obtain patent coverage over source synchronous clocking as it was being discussed at JEDEC. (Crisp, Tr. 3457; *see* DX0028).

Rambus's Response to Finding No. 3180:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3175).

3181. JEDEC included a bidirectional data strobe, or DQS strobe, as part of the DDR SDRAM standard. (CX0234 at 164). The data strobe might be considered to be a form of source synchronous clocking. (Lee, Tr. 6682).

Rambus's Response to Finding No. 3181:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3175).

3182. Rambus may intend to assert patents relating to source synchronous clocking against manufacturers or users of SDRAMs and DDR SDRAMs. (CX1363 at 3 (list indicating that "Source synchronous signaling" is a Rambus innovation contained in DDR SDRAMs); CX1371 at 5 (informing nVidia that "Rambus innovations" include "Source synchronous signaling"); CX1383 at 4 (informing ATI of same)).

Rambus's Response to Finding No. 3182:

The proposed finding is misleading and irrelevant. (*See* RRFF 3113, 3175).

C. The Remedy Should Be Worldwide.

3183. The remedy should extend not only to United States patents, but to foreign patents as well. (McAfee, Tr. 7521). This follows because relevant technology markets are worldwide. (McAfee, Tr. 7521, 7178). Thus, to enforce the remedies only on U.S. patents would not fully address the problem. (McAfee, Tr. 7521). The U.S. is a net importer of DRAM, so if patent enforcement occurs outside the U.S., there would actually be harm to U.S. consumers in the long run. (McAfee, Tr. 7521-22).

Rambus's Response to Finding No. 3183:

The proposed finding is misleading and irrelevant. First, Complaint Counsel, based on the testimony of their economic expert, ask the Court to find that any remedy should extend to "any intellectual property that should have been disclosed, whatever that might be." (CCFF 3111 (citing McAfee, Tr. 7521)). The evidence shows that JEDEC did not require the disclosure of foreign patent rights. (RPF 286-87). Yet Complaint Counsel now ask the Court to go beyond the scope of their own rationale to apply the Court's remedial powers to "intellectual property that should not have been disclosed." Second, application of the Courts remedial powers to prevent Rambus from exercising rights granted to it by foreign sovereigns – thereby depriving foreign courts of the ability to assess whether the patent laws of their countries would permit or deny

Rambus from enforcing its patents given the facts of this case – raises serious issues of comity.

(*See* Rambus Post-Trial Reply Brief at Section VII.B).

3184. Rambus has numerous foreign patents that are directly based on its original U.S. patent application no. 07/510,898 (the '898 application). (CX1452 (India); CX1453 (Taiwan)). Many of these foreign patents claim priority based on the '898 application and the benefit of its April 18, 1990 U.S. filing date. (CX1485 (Israel); CX1489 (Israel); CX1496 (Israel); CX1499 (Israel); CX1514 (Korea); CX1515 (Korea); CX1527 (Germany); CX1529 (Europe); CX1533 (Europe); CX1536 (Europe)).

Rambus's Response to Finding No. 3184:

The proposed finding is irrelevant. (*See* RRFF 3183). The proposed finding is also misleading. There is no evidence that all of the cited foreign patents claim priority to the '898 application.

3185. If Rambus can enforce foreign patents, SDRAM and DDR SDRAM manufacturers will find themselves in the same position that they are in today. (McAfee, Tr. 7521; CCFF 3186-3326).

Rambus's Response to Finding No. 3185:

The proposed finding is irrelevant. (*See* RRFF 3183).

3186. Rambus has sought to enforce European patents against DRAM manufacturers in court proceedings in the United Kingdom, Germany, Italy and France. (CCFF 2026-2027).

Rambus's Response to Finding No. 3186:

The proposed finding is irrelevant. (*See* RRFF 3183).

3187. Rambus has stated publicly that it would pursue enforcement of foreign patents against DRAM manufacturers and others "vigorously." (CX1888 ("While the Virginia case against Infineon involves only four Rambus U.S. patents, there are a dozen U.S. and European patents involved in other infringement cases pending against Infineon, Hyundai and Micron. Rambus intends to pursue all these cases vigorously, including a trial against Infineon in Germany . . . .")).

Rambus's Response to Finding No. 3187:

The proposed finding is irrelevant. (*See* RRFF 3183).

3188. Jedec standards are worldwide standards. (CX3037 at 1 ("Although nominally a US body, [JEDEC] is in fact supported by companies world-wide and is the De Facto setter of standards for many matters including memory device packages, pinnings and functions."); Appleton, Tr. 6274-75 (products manufactured by Micron overseas also comply with JEDEC standards and that JEDEC standards are world standards.); Rhoden, Tr. 294 (most of the DRAM production in the world comes from Jedec members, and that "[a]lmost all DRAM manufacturers in the world are members of JEDEC."); Tabrizi, Tr. 9141-42 ("DRAM is a commodity and it's global and there is no -- not such a thing as local standardization. Everything is done on a worldwide basis. . . .")).

Rambus's Response to Finding No. 3188:

The proposed finding is irrelevant. (*See* RRFF 3183).

3189. SDRAM and DDR SDRAM manufacturers have worldwide operations. (Tabrizi, Tr. 9141-42; Bechtelsheim, Tr. 5886; CCFF 3190-3198).

Rambus's Response to Finding No. 3189:

The proposed finding is irrelevant. (*See* RRFF 3183).

3190. Synchronous DRAM is produced throughout the world by various memory manufacturers located or doing business in the U.S. and various foreign countries. Synchronous DRAMs, and products incorporating synchronous DRAMs, are imported and exported throughout the world in large volumes. (Rambus Answer at 44, ¶ 110).

Rambus's Response to Finding No. 3190:

The proposed finding is irrelevant. (*See* RRFF 3183).

3191. Micron ships large volumes of DRAMs internationally at relatively low cost. (Appleton, Tr. 6269-70 ("You know, the fact is that these devices are very, very small, they're not much in weight, and they move around the world pretty freely and at a relatively low cost.")).

Rambus's Response to Finding No. 3191:

The proposed finding is irrelevant. (*See* RRFF 3183).

3192. Hyundai has worldwide sales operations. (CX2107 at 14-15 (Oh, Dep.)).

Rambus's Response to Finding No. 3192:

The proposed finding is irrelevant. (*See* RRFF 3183).

3193. All DRAMs produced by Hynix that are sold to U.S. customers must pass through Korea before they are distributed to U.S. customers in the United States or elsewhere in the world. (CX2107 at 20 (Oh, Dep.)). Although Hynix manufactures DRAMs in the United States, it does not have packaging and test capability in the United States. (CX2107 at 19-20 (Oh, Dep.)). In order to manufacture and sell DRAMs in the United States, Hyundai must first ship completed wafers to Seoul, Korea, where they are tested and packaged before being shipped back to the United States. (*Id.*).

Rambus's Response to Finding No. 3193:

The proposed finding is irrelevant. (*See* RRFF 3183).

3194. Micron has worldwide DRAM design, fabrication, test/assembly, and sales facilities. (Appleton, Tr. 6266-67, 6271-72; *see* DX0111, DX0112). Micron ships parts internationally as part of manufacturing, testing and packaging, with facilities for each in different places across the world. (Appleton, Tr. at 6269). Micron ships DRAM wafers across international boarders "pretty freely and at a relatively low cost." (*Id.* at 6269-70). About half of Micron's DRAM chips, modules, and products that containing DRAMs are sold outside of the United States. (*Id.* at 6272-73; *see* DX0113).

Rambus's Response to Finding No. 3194:

The proposed finding is irrelevant. (*See* RRFF 3183).

3195. Micron has manufacturing operations in Avezzano, Italy; Nishiwaki-City, Japan; Singapore TECH, Singapore; and Singapore AT, Singapore. (CX2735 at 15. ("Micron Around the World"). Micron has overseas design facilities in Avezzano, Italy and Bracknell, England. (*Id.*). Finally, Micron has overseas semiconductor sales units in Munich, Germany; Bracknell, England; Tokyo, Japan; Taipei, Taiwan; and Singapore. (*Id.*).

Rambus's Response to Finding No. 3195:

The proposed finding is irrelevant. (*See* RRFF 3183).

3196. Infineon has worldwide DRAM manufacturing operations. (Reczek, Tr. 4298-4300).

Rambus's Response to Finding No. 3196:

The proposed finding is irrelevant. (*See* RRFF 3183).

3197. The vast majority of PCs sold in the world today use DDR SDRAM. (Wagner, Tr. 3750-51).

Rambus's Response to Finding No. 3197:

The proposed finding is irrelevant. (*See* RRFF 3183).

3198. Products incorporating drams are shipped across borders in large volumes. (Appleton, Tr. 6273 ("[W]e ship [DRAMs or DRAM modules] to that customer, and that customer incorporates that product into an end product, and then they ship it somewhere else in the world.")).

Rambus's Response to Finding No. 3198:

The proposed finding is irrelevant. (*See* RRFF 3183).

3199. Patent enforcement in any country could cause substantial problems for the market. (Appleton, Tr. 6397-98 (testimony that Rambus's German litigation against Micron could cause the company significant harm); Bechtelsheim, Tr. 5886 (testifying that he was concerned that Rambus could cause a "dislocation in the memory market depending on the country" in which it decided to sue a DRAM manufacturer)).

Rambus's Response to Finding No. 3199:

The proposed finding is irrelevant. (*See* RRFF 3183).

3200. Rambus strategically developed foreign patents as part of its overall patent plan. Rambus's 1990 business plan discusses pursuing foreign patent registration in multiple places. (CX0535 at 1, 4 ("The base patent is being filed over the next several months in the European Patent Office, Israel, Korea, Taiwan, Japan, India, and Canada. Five additional inventions have been identified . . . . These will be filed for patents in the US by early 1991 and worldwide by late 1991.")).

Rambus's Response to Finding No. 3200:

The proposed finding is irrelevant. (*See* RRFF 3183).

3201. The first foreign jurisdictions that Rambus chose to file the base patent in were the European Patent Office, Israel, Korea, Taiwan, Japan, India, and Canada. (CX0535 at 1, 4).

Rambus's Response to Finding No. 3201:

The proposed finding is irrelevant. (*See* RRFF 3183).

3202. During the time that Rambus was a JEDEC member, part of the work by Rambus patent counsel Lester Vincent on behalf of Rambus involved work on foreign patent filings, including counseling Rambus representatives with respect to the countries in which they should file patent applications. (Vincent, Tr. 7878-79; see CX1937 at 28). This included providing Rambus with a chart listing countries currently or in the future expected to be involved in semiconductor manufacturing, packaging and assembly and computer production, to help Rambus in making foreign patent filing decisions. (CX1972 at 1, 2).

Rambus's Response to Finding No. 3202:

The proposed finding is irrelevant. (*See* RRFF 3183).

3203. On April 16, 1991, Rambus filed an International Patent Application under the Patent Cooperation Treaty (the PCT application). (CX1451 at 1). A PCT application is a mechanism that permits an applicant to file with the World Intellectual Property Organization ("WIPO") an application based on a United States patent application, and thereafter enter the patent registration process in various foreign countries within a specified period. (Vincent, Tr. 7883; see CX1948).

Rambus's Response to Finding No. 3203:

The proposed finding is irrelevant. (*See* RRFF 3183).

3204. Rambus also filed an application with the European Patent Office ("EPO"). The EPO is an administrative mechanism for centralized examination of patent applications for various European countries. (Vincent, Tr. 7885-86, 7894-97). Rambus pursued examination of patent applications in this fashion in the United Kingdom, France, Germany and Italy. (Vincent, Tr. 7897; RX335).

Rambus's Response to Finding No. 3204:

The proposed finding is irrelevant. (*See* RRFF 3183).

3205. Rambus attempted to conform certain independent claims in the EPO application to the amended claims being prosecuted in the United States. (Vincent, Tr. 7899).

Rambus's Response to Finding No. 3205:

The proposed finding is irrelevant. (*See* RRFF 3183). The proposed finding is also

unsupported in that the cited evidence does not show any attempt to "conform certain independent claims." (Vincent, Tr. 7899-900 ("I don't recall what I actually ended up doing.")).

3206. In the second half of 1994, Rambus executives focused again on ensuring that they obtained patent coverage in key foreign countries. Rambus CFO Gary Harmon wrote to Vice President Allen Roberts, with a copy to CEO Geoff Tate, urging that Rambus "should file [patent applications] in the key foreign jurisdictions." (CX0753 at 1("I think we have to do everything possible to pursue and protect those patents wherever in the world it makes economic sense.")).

Rambus's Response to Finding No. 3206:

The proposed finding is irrelevant. (*See* RRFF 3183).

3207. In a letter dated October 16, 1994, Rambus's outside patent attorney sent Mr. Harmon, Rambus's CFO at the time, a chart identifying current and expected "Semiconductor Manufacturing Countries" and "Packaging and Assembly Countries." (CX1972 at 1-2). The following countries were identified as semiconductor manufacturing countries: United States, Japan, Korea, Taiwan, Germany, Holland, Italy, Malaysia, Thailand, and Ireland. (*Id.* at 2). The chart included Japan, Korea, Malaysia, PRC, Phillippines, India, Mexico, and Thailand as packaging and assembly countries. (*Id.*). Mr. Vincent believed that Mr. Harmon "might find [the chart] helpful in making foreign filing decisions." (*Id* at 1).

Rambus's Response to Finding No. 3207:

The proposed finding is irrelevant. (*See* RRFF 3183).

3208. As of approximately 1995, there were Rambus patent applications based on the original Rambus '898 patent application pending with the EPO (Vincent, Tr. 7885-86), the WIPO (Vincent, Tr. 7883), India (Vincent, Tr. 7882), Israel (Vincent, Tr. 7885), Japan (Vincent, Tr. 7886-87) and Korea (Vincent, Tr. 7887). As of that time, Rambus had also been issued a patent in Taiwan based on the specification contained in the original Rambus '898 patent application. (Vincent, Tr. 7883-85). (See also CX1982).

Rambus's Response to Finding No. 3208:

The proposed finding is irrelevant. (*See* RRFF 3183). The proposed finding is also unsupported with regard to the WIPO application. (Vincent, Tr. 7883 (WIPO expired by 1995)).

3209. After 1996, Rambus continued to work on its foreign patent strategy. (CX1804 at 5-6, 8-10, 12-13). By September 30, 2002, Rambus had thirty-two foreign patents and had seventy-three additional applications pending in Europe and Asia. (CX1782 at 8).

Rambus's Response to Finding No. 3209:

The proposed finding is irrelevant. (*See* RRFF 3183).

3210. Today, Rambus holds foreign patents that claim priority back to its U.S. patent application no. 07/510,898 in Korea, Germany, and Europe. (CCFF 1670-1674).

Rambus's Response to Finding No. 3210:

The proposed finding is irrelevant. (*See* RRFF 3183).

3211. Rambus has foreign patents that it has asserted already or believes it could assert in the future against SDRAM and DDR SDRAM manufacturers in foreign countries. (*See* following # of proposed findings).

Rambus's Response to Finding No. 3211:

The proposed finding is irrelevant. (*See* RRFF 3183).

3212. Rambus has admitted "that it is involved in patent infringement lawsuits in various foreign countries that involve foreign patents that cover some of the same inventions at issue in the U.S. litigation." (Rambus Answer at 42, ¶ 102).

Rambus's Response to Finding No. 3212:

The proposed finding is irrelevant. (*See* RRFF 3183).

3213. {

} (CX2072 at 45-46 (Tate, Dep.), *in camera*).

Rambus's Response to Finding No. 3213:

The proposed finding is irrelevant. (*See* RRFF 3183).

3214. Sometime after April 19, 2000, Rambus prepared a presentation which illustrates how several claims within European patent EP 0 525 068 B1 cover different features described within a Micron 64M DDR SDRAM data sheet. (CX1269). Claims 1, 6, 7, and 8 of the European patent are represented as covering programmable cas latency. (*Id.* at 37-43, 50-51, 52-53, 54-55, respectively). Claim 2 of the European patent is represented as covering a read operation that outputs data with each positive edge of the external clock. (*Id.* at 44-45). Claims 3 and 5 are represented as covering an on-chip DLL. (*Id.* at 46-47, 48-49, respectively). The

presentation then illustrates how all of the aforementioned claims with the exception of claims 3 and 5 cover features described within a Micron 64M SDRAM data sheet. (*Id.* at 58).

Rambus's Response to Finding No. 3214:

The proposed finding is irrelevant. (*See* RRFF 3183). The proposed finding is also incorrect and misleading in stating the claims are "covering" a broadly defined feature such as "programmable cas latency." As is clear from the exhibit (CX1269 at 37) the claim has a number of very specific limitations, none of which is "programmable cas latency." The claim charts of the cited exhibit illustrate how each and every limitation contained in the claims is depicted in the Micron data sheet. The proposed finding is also incorrect and misleading in stating that claim 2 is represented as covering a "read operation that outputs data with each positive edge of the external clock." Claim 2 is a dependent claim that depends from claim 1 and therefore includes every limitation of claim 1. (CX1269 at 44). As such, stating that the claim would be infringed simply by a "read operation that outputs data with each positive edge of the external clock" does not comport with the fact that the claim also includes the limitations of claim 1. (Fliesler, Tr. 8873-74) The proposed finding is also incorrect and misleading with respect to dependent claims 3 and 5 in the same manner. (CX1269 at 46, 48).

3215. Sometime after April 19, 2000, Rambus prepared a presentation which illustrates how several claims within European patent 0 525 968 B1 cover different features described within an Infineon 256M DDR SDRAM. (CX1268 at 3). Claims 1, 6, 7, and 8 of the European patent are represented as covering programmable cas latency. (*Id.* at 2, 15-16, 17-18, 19-29, respectively). Claim 2 of the European patent is represented as covering a read operation that outputs dat with each positive edge of the external clock. (*Id.* at 9-10). Claims 3 and 5 are represented as covering an on-chip DLL. (*Id.* at 11-12, 13-14, respectively).

Rambus's Response to Finding No. 3215:

The proposed finding is irrelevant and misleading. (*See* RRFF 3183). The proposed

finding is also incorrect and misleading in its characterization of how certain claims "cover" broad features without taking into account all of their limitations for the same reasons cited in RRFF 3214.

3216. On August 7, 2000, Rambus sued Infineon Technologies AG in Mannheim, Germany. (CX1866 at 1). In the complaint that it filed against Infineon, Rambus identified which Infineon DDR SDRAM and SDRAM devices it alleged to infringe several of Rambus's foreign patents. (*Id.* at 30, 39, 46).

Rambus's Response to Finding No. 3216:

The proposed finding is irrelevant. (*See* RRFF 3183). The proposed finding is also incorrect in asserting that the in the complaint, Rambus identified Infineon devices that were "alleged to infringe several of Rambus's foreign patents." The complaint cited lists only one patent, EP 0 525 068. (CX1866 at 30).

3217. On August 31, 2000, Rambus sued Micron Semiconductor (Deutschland) GmbH in Mannheim, Germany. (CX1869 at 1). In the complaint that it filed against Micron, Rambus identified which Micron DDR SDRAM and SDRAM devices it alleged to infringe several of Rambus's foreign patents. (*Id.* at 43, 49, 54).

Rambus's Response to Finding No. 3217:

The proposed finding is irrelevant. (*See* RRFF 3183). The proposed finding is also incorrect in stating that Rambus asserted "several" foreign patents in its complaint. Only one patent, EP 0525 068, is asserted in the complaint. (CX1869 at 43).

3218. On September 14, 2000, Rambus sued Micron European Limited in the United Kingdom. (CX1871 at 1). In the complaint it filed against Micron, Rambus identified DDR SDRAM and SDRAM device that it alleged to infringe a European patent. (CX1871 at 1, 6, 7).

Rambus's Response to Finding No. 3218:

The proposed finding is irrelevant. (*See* RRFF 3183).

3219. Rambus has also sued Micron in Italy. (Appleton, Tr. 6396).

Rambus's Response to Finding No. 3219:

The proposed finding is irrelevant. (*See* RRFF 3183).

3220. Rambus has stated publicly that it intends to continue to assert its foreign patents against DRAM manufacturers and others "vigorously." (CX1888 ("Rambus intends to pursue all these cases [involving U.S. and European patents] vigorously, including a trial against Infineon in Germany . . .")).

Rambus's Response to Finding No. 3220:

The proposed finding is irrelevant. (*See* RRFF 3183).

3221. Rambus's litigation against Micron in Germany, Italy, and the United Kingdom has put the company at risk. (Appleton, Tr. 6397; CCFF 3222-3223).

Rambus's Response to Finding No. 3221:

The proposed finding is irrelevant. (*See* RRFF 3183).

3222. Rambus's litigation against Micron in Italy has threatened and still threatens to shut down a large manufacturing plant there. (Appleton, Tr. 6397). Micron's plant in Italy employs 1,500-2,000 people. (*Id.*). It produces products that are shipped across the world. (*Id.* at 6398). As Micron's CEO testified, "We've invested hundreds of millions of dollars in that operation, and to have it not operate would obviously be very detrimental to us." (*Id.*). If Micron could not operate the plant in Italy, it would not longer be able to service customers that are currently purchasing product that originated from Italy. (*Id.* at 6397-98).

Rambus's Response to Finding No. 3222:

The proposed finding is irrelevant. (*See* RRFF 3183).

3223. Micron has several very large customers in Germany that it would not be able to supply product to if Rambus were successful in its German litigation against Micron. (Appleton, Tr. 6398). Rambus's litigation against Micron in Germany also poses risks to Micron that extend beyond German borders. (*Id.*).

Rambus's Response to Finding No. 3223:

The proposed finding is irrelevant. (*See* RRFF 3183).

3224. Mr. Bechtelsheim testified that his concerns were not limited to Rambus's enforcement of U.S. patents, but also extended to the potential enforcement of Rambus's foreign

patents. (Bechtelsheim, Tr. 5886). As Mr. Bechtelsheim explained, "There's an additional issue here that the memory business is of course a worldwide or international business with some manufacturers in Europe, many of them in Asia, and one remaining in the U.S., so depending on the validity of such patent claims, it could have created a dislocation in the memory market depending on the country or area these memory manufacturers were manufacturing the devices. On top of that, Cisco also manufactures their own products all over the world and there could be a secondary issue of Rambus asserting claims against Cisco at the location of manufacturing Cisco Systems' own products." (*Id.*).

Rambus's Response to Finding No. 3224:

The proposed finding is irrelevant. (*See* RRFF 3183).

3225. Rambus may have additional foreign patents that cover SDRAM and DDR SDRAM which it has not yet asserted against DRAM manufacturers. (CX1888 at 1) (Rambus May 2001 press release: "Rambus holds newly issued U.S. and European patents covering Rambus inventions used by SDRAMs and DDR SDRAMs that have not yet been asserted in any litigation and are not impacted by the [Infineon trial] Court's decision."); CX1403 at 30 (the "Virginia decision involved only 4 patents" and that Rambus has "many others which are used by SDRAM/DDR.")).

Rambus's Response to Finding No. 3225:

The proposed finding is irrelevant. (*See* RRFF 3183).

3226. In July 2001, Rambus admitted that even if it lost its efforts to enforce its U.S. patents, it could still achieve its enforcement goals because its litigation strategy only requires success in one major jurisdiction. (CX1890 at 35 (Rambus Senior Vice President of Finance and CFO Bob Eulau: "I'll take a question then which is "What is the likelihood of SDRAM licensees not paying due to the Virginia outcome? We don't think this is very likely. . . .We've said that the litigation requires success in a major jurisdiction, but not in every jurisdiction.")).

Rambus's Response to Finding No. 3226:

The proposed finding is irrelevant. (*See* RRFF 3183).

D. The Remedy Should Extend To Future Standards.

3227. The prohibition on Rambus's enforcement of any patents filed (or based on filings) prior to June 18, 1996 against JEDEC-compliant DRAMs should extend to DDR-II SDRAM as well as SDRAM and DDR SDRAM. (McAfee, Tr. 7519). This follows because in the likely but-for world, DDR SDRAM would not contain Rambus intellectual property. Therefore, JEDEC would not be building DDR-II SDRAM in the but-for world using DDR SDRAM as the

baseline. (McAfee, Tr. 7519-20)

Rambus's Response to Finding No. 3227:

The proposed finding is not supported by the evidence and is fundamentally flawed. The theory of Complaint Counsel's case is that Rambus enjoys market power over relevant technology markets because the DRAM industry is locked in to using Rambus's technologies in the the DDR and SDRAM standards. (*See* CCFF 2916 ("The DRAM industry is no longer capable of switching from the technologies in the SDRAM standard to alternatives because it is locked in to the current standard."); CCFF 2917 ("The DRAM industry is no longer capable of switching from the technologies in the DDR SDRAM standard to alternatives because it is locked in to the current standard.")). For lock in to exist, switching costs must be so high as to prevent DRAM industry members from profitably turning to alternatives. (Rapp, Tr. 9873-74, 9886-87). Absent lock in, incorporation of Rambus's technologies in a JEDEC standards cannot give Rambus market power. (Rapp, Tr. 9902-03).

The proposed finding does not rest on any evidence that switching costs are so high as to prevent DRAM industry members from adopting alternatives to Rambus's technologies. Rather, the proposed finding rests solely on the notion that since DDR2 is based on DDR, the remedy should extend to DDR2. In other words, Complaint Counsel make no effort to prove that the DRAM industry is locked in by excessive switching costs. Instead, Complaint Counsel attempt to improperly extend a remedy to future DRAM standards by arguing that DRAM industry participants should be able to continue to use Rambus's technologies royalty free in successive standards so long as the standard is somehow "based on" DDR. This remedy would apply regardless of the absence of switching costs, regardless of the simplicity of changing the future

standard, and regardless of JEDEC's full knowledge of Rambus's issued patents.

As explained further below, there is no basis for given such a windfall to JEDEC and its members.

3228. Rambus's enforcement of its patents with respect to the DDR II SDRAM standard will continue to cause harm to the industry. (CCFF 3229-3261).

Rambus's Response to Finding No. 3228:

As explained below, the proposed finding is unsupported, misleading, and contrary to the evidence. (*See* RRFF 3229-61).

3229. The technologies claimed by Rambus had already been designated as part of the DDR-2 "baseline" as early as the summer of 1998, and changing them would delay the development of the standard and harm companies who have done work based on the adoption of the standard. (CCFF 3236-3243).

Rambus's Response to Finding No. 3229:

As explained below, the proposed finding is unsupported, misleading, and contrary to the evidence. (*See* RRFF 3236-43).

3230. Development work on DDR II SDRAM began at JEDEC in April of 1998 when the first meeting of the "Future DRAM Task Group" met. (CX0376A; CX0379A; Macri, Tr. 4582-83; Lee, Tr. 6769).

Rambus's Response to Finding No. 3230:

Rambus has no specific response.

3231. JEDEC members believed that it was necessary to begin work on DDR II SDRAM that early, even prior to JEDEC's final adoption of the DDR SDRAM specification, because of the time it was expected to take to finalize the standard. (CX0140 at 3; Rhoden Tr. 412-414; Macri, Tr. 4607-608 ("The design cycle was long, so we needed to do this very early so that systems could be started to be designed – DRAMs could be designed such that when the DDR1 standard,... ended its life, the DDR2 standard and its systems would be ready to take over in a seamless fashion...[W]e needed to be proactive purely because you can't build these things in a day. It takes quite a bit of time.")).

Rambus's Response to Finding No. 3231:

The proposed finding is misleading to the extent it implies that any DRAM industry member had made substantial investments in the DDR2 standard prior to the issuance of Rambus's patents and its requests for royalties in 1999. (*See* RRFF 3238).

3232. In order to allow the main DRAM committee at JEDEC, the 42.3 committee, to continue work on defining DDR, JEDEC formed the Future DRAM Task Group and designated Joe Macri of ArtX (later of ATI Technologies) as its chairman. (CX0376A; Macri, Tr. 4581).

Rambus's Response to Finding No. 3232:

Rambus has no specific response.

3233. The goal of the Task Group was to derive a standard that would follow DDR SDRAM. (Macri, Tr. 4608). That standard was to be no more costly on a system level basis than PC-100 SDRAM. (CX0379A at 2; Macri, Tr. 4609-10).

Rambus's Response to Finding No. 3233:

Rambus has no specific response.

3234. In addition, the new standard was intended to last for at least three DRAM density generations, a period of approximately six years. (CX0379A at 2; Macri, Tr. 4610). The reason that it was important that the new standard last at least three DRAM density generations was that it was necessary to allow the various manufacturers relating to the DRAM industry to amortize the cost of changing the standard over sales for a number of years. (Macri, Tr. 4610-11).

Rambus's Response to Finding No. 3234:

The proposed finding is misleading in that it implies that once set, DRAM industry standards do not change. The evidence shows that the previous DRAM standards, SDRAM and DDR, consisted of a number of sub-standards that required changes to the DRAM, changes to complementary components, and a transition from one sub-standard to the next. (*See* RPF 1308-32). These natural transitions provided opportunities to incorporate alternatives to Rambus's technologies. (Geilhufe, Tr. 9675). The same types of sub-standards and transitions were

foreseen for DDR2. (CX 2451 at 7 (industry roadmap showing different types of DDR2 devices)).

3235. Finally, the new standard was intended to be directed at a large number of markets. (CX0380 at 6 ("Same design must support desktop PC, laptop PC, workstations/small servers, various embedded applications.")). As a result, wide participation in the task group by a variety of different types of firms was encouraged. (Macri, Tr. 4635; CX0378 at 1; CX0387 at 1 ("I have been working hard to involve as many people as possible in the definition of DDRII.")).

Rambus's Response to Finding No. 3235:

Rambus has no specific response.

3236. One of the first tasks of the committee was to determine the "baseline" for the DDR II SDRAM standard. (CX0379A at 9). The baseline was to be used as the starting point for the new standard. (Rhoden, Tr. 409-10). At the first meeting, in April of 1998, in order to determine what was to be the baseline for the new standard, a "straw vote" was taken of the members in attendance. The candidates were DDR SDRAM , SLDRAM (also known as Synclink) and RDRAM. DDR SDRAM received twenty-two votes in favor of it becoming the baseline, SLDRAM received 12 votes and RDRAM received zero votes. (CX0379A at 9; Macri, Tr. 4612-13).

Rambus's Response to Finding No. 3236:

The proposed finding is incomplete. The Task Group also voted on whether to use a packetized or non-packetized architecture. (CX 379A at 9). About one-third of the Task Group voted to use a packetized architecture, which would have broken from the DDR architecture. (CX 379A at 9). The fact that the Task Group seriously considered different architectures as a base demonstrates that there was no technological or economic force compelling the that next generation DRAM standard be based on DDR.

3237. By the summer of 1998, the consensus of the committee was that the new standard should be DDR-based. (CX0132 at 4; CX2745 at 7; Macri, Tr. 4614; Lee, Tr. 6774-5). By February of 1999, work on the basic DRAM device was far enough along that a "DDR-II Module Task Group" was formed to establish the standard for the modules that would be used with the new DRAMs in PC main memory. (Kellogg, Tr. 5194-5; CX0393). By March of 1999, the major functions of the new standard were described. (CX0397 at 6).

Rambus's Response to Finding No. 3237:

The proposed finding is misleading and incomplete. Joe Macri, chairman of the Future DRAM Task Group, testified that the Task Group continued to specify many of the architectural features for DDR2 through June 2000. (Macri, Tr. 4598-99). Rambus's patents issued and it began requesting royalties for the four technologies at issue in this case late 1999. (Complaint, ¶ 92; Rhoden, Tr. 529; CX 1855 (complaint filed against Hitachi in January 2000)). This assertion of patent rights was widely publicized and well-known in the industry. (Rhoden, Tr. 529; Macri, Tr. 4667-8). This initial period of the specification of the DDR2 standard, therefore, continued from late 1999 through June 2000 in full view of Rambus's issued patents.

From June 2000 to June 2001, the Task Group continued to flesh out the DDR2 specification. According to Mr. Macri, this portion of the DDR2 effort was "to create a, you know, a real standard which is in the end a specification." (Macri, Tr. 4598-99). All of this JEDEC work from June 2000 to June 2001 was done in full view of Rambus's patents and in full view of Rambus's assertion that it had patent claims covering the four technologies incorporated in the DDR standard. {

} (Macri, Tr. 4753-56 (*in camera*)).

From June 2001 through September 2001, JEDEC made further architectural changes to the DDR2 standard. (Macri, Tr. 4599). Again, these changes were made with knowledge of Rambus's patents and demands for royalties.

As of May 2003, the DDR2 standard was still not completed. (Rhoden, Tr. 411-12).

3238. At the same time that the future DRAM Task Group was developing the standard for what became DDR II SDRAM, companies that intended to manufacture the DRAM as well as companies that intended to use the DRAM in their systems were working with the proposed

standard as it developed, and giving feedback to the Task Group on the standard. (Macri, Tr. 4588-89; RX2234 at 14). Companies also worked with the proposed DDR II SDRAM standard as it developed because of the long lead time necessary to develop their products to full production. (CX0140 at 3 ("[T]he difference between first DRAM device design and full production is about 4 years.")).

Rambus's Response to Finding No. 3238:

The proposed finding is unclear as to what it means to be "working with the proposed standard," and it is unclear as to the time frame for this activity (whether before or after Rambus's patents issued). There is no evidence that nay company made any substantial investment in the DDR2 standard prior to the issuance of Rambus's patents and its well-known requests for royalties for the use of its technologies. In fact, the evidence shows that DRAM manufacturers do not work on "control features," i.e., the types of features at issue in this case, until late in the design process:

> We could begin the DRAM before JEDEC information became finalized because most of the DRAM is not the control features that are decided at JEDEC. Most of the DRAM is the memory array, and all of that is going to be the same regardless of what the JEDEC feature/function requirements are and we could add those control features as JEDEC began to make decisions late in the design process.

(Kelley, Tr. 2590; Guilhufe, Tr. 9559-60 (four features at issue are in the peripheral circuitry, not the memory array)). Further, the evidence shows that companies that intend to use DDR2 in their systems, such as AMD, have not begun work to use DDR2 products even as late as June 2003. (Polzin, Tr. 4043-44). The finding is therefore irrelevant as it does not bear on the

issue of switching costs.

3239. Design work on DDR II SDRAM at Micron began in the fall of 1999. (Shirley, Tr. 4211). That design was based on DDR II SDRAM specification generated earlier by the marketing group at Micron. (Shirley, Tr. 4211). Micron's first DDR II SDRAM design was taped out in January of 2002. (Shirley, Tr. 4228). By the end of 2002, Micron had taped-out at least one more DDR II SDRAM chips. (Shirley, Tr. 4229). Micron currently fabricates DDR II SDRAMs. (Appleton, Tr. 6264).

Rambus's Response to Finding No. 3239:

The proposed finding is incomplete. Rambus's patents issued and it began requesting royalties for the four technologies at issue in this case late 1999. (Complaint, ¶ 92; Rhoden, Tr. 529). This assertion of patent rights was widely publicized and well-known in the industry. (Rhoden, Tr. 529-30; Macri, Tr. 4667-8). Micron's CEO admitted to becoming aware of Rambus's claims in 2000 when Rambus sued Hitachi (Appleton, Tr. 6384); Rambus filed suit against Hitachi in January 2000. (CX 1855 (complaint filed against Hitachi in January 2000)). Micron, therefore, had only spent a few months at most working on its DDR2 design before knowing of Rambus's issued patents and requests for royalties. It continued that work for over two years despite that knowledge.

3240. By May of 2002, Samsung had finalized a GDDR-2 SGRAM chip. (CX2829 at 2; Wagner, Tr. 3852). GDDR-2 SGRAM was a DDR II like DRAM designed for use with graphics processors. (Wagner, Tr. 3837-38).

Rambus's Response to Finding No. 3240:

The proposed finding is misleading and incomplete. Rambus's patents issued and it began requesting royalties for the four technologies at issue in this case late 1999. (Complaint, ¶ 92; Rhoden, Tr. 529). This assertion of patent rights was widely publicized and well-known in the industry. (Rhoden, Tr. 529-30; Macri, Tr. 4667-8). The evidence shows that Samsung was

aware of Rambus's claims as early as January 2000. (CX 1099 at 1). Yet Samsung continued with the development of its DDR2 devices unabated. Further, Mr. Wagner of nVidia testified that the Samsung "GDDR-2" device was not the same as that being developed as the industry standard. (Wagner, Tr. 3837-38, 3866).

3241. Infineon is currently working on three DDR II SDRAM chips: a 256-megabit, a 512-megabit and a 1-gigabit DDR II SDRAM. (Peisl, Tr. 4387-88).

Rambus's Response to Finding No. 3241:

The proposed finding is incomplete. Rambus's patents issued and it began requesting royalties for the four technologies at issue in this case late 1999. (Complaint, ¶ 92; Rhoden, Tr. 529). This assertion of patent rights was widely publicized and well-known in the industry. (Rhoden, Tr. 529; Macri, Tr. 4667-8). The evidence shows that Infineon was aware of Rambus's claims at least as early as March 2000. (CX 2459 at 1). Yet Infineon's development of its DDR2 devices apparently continued unabated.

3242. Graphics chip designers were among the earliest adopters of DDR II. NVidia was working on designs for a graphics chip intended for use with DRAMs based on the DDR II SDRAM standard in late 2000 to early 2001. (Wagner, Tr. 3869). The Samsung GDDR-2 SGRAM is used with NVidia workstation products currently on the market. (CX2832 at 2; Wagner, Tr. 3838-40). ATI uses both GDDR-2 and GDDR-2m in current products. (Macri, Tr. 4579). GDDR-2m, like GDDR-2 is a variant of the DDR II SDRAM standard. (Macri, Tr. 4577-78).

Rambus's Response to Finding No. 3242:

The proposed finding is misleading and incomplete. Mr. Wagner of nVidia testified that the Samsung "GDDR-2" device used with nVidia's NV-30 produce was not the same as that being developed as the industry standard:

Q. And the first product, am I right that the first product you started to

work on that made use of what you thought would ultimately be a DDR2 product was the one featured in 2832, the nVidia Quadro Fx?

A. Not exactly. It wasn't a – it was the first device that we targeted to be compatible with hopefully what would become a JEDEC DDR2 standard. *The device that we were developing was not being developed in the context of JEDEC, so we knew that it was not true JEDEC DDR2*, we hoped they would be compatible so that we could ultimately have a lower cost version of it also further down the product line.

Q. Let me try and just make sure. Was the first – let me just ask you, what was the first product that you designed that you thought would make use of something which might become DDR2?

A. That was our NV-30 product.

(Wagner, Tr. 3866) (emphasis added).

Moreover, Mr. Wagner admitted that nVidia began working on its DDR2 product after it was aware of Rambus's lawsuits regarding the technologies at issue in this case. (Wagner, Tr. 3867 ("Q. And in any event, you started work on that product [(NV-30)] after you knew about the Rambus lawsuits, correct? A. Yes.").

The reference to ATI's use of GDDR2 and GDDR2m is irrelevant because the evidence does not indicate whether ATI developed its products before or after Rambus's patents issued. The evidence shows that ATI was fully apprised of Rambus's patent claims early in the DDR2 process. { } (CX 1384 (*in camera*)). Yet ATI continued to develop DDR2 products with full knowledge of

Rambus's claims.

3243. Removal of features from the standard after firms began designing products in reliance on the existence of those features in the standard could have been disruptive. (Macri, Tr. 4600). Additions to the standard, while maintaining the earlier functionality, were not as disruptive because they would not endanger the work done to date. (Macri, Tr. 4600).

Rambus's Response to Finding No. 3243:

The proposed finding is unclear and not supported. First, the proposed finding does not define "disruptive." Second, the evidence shows that DRAM manufacturers do not work on "control features," i.e., the types of features at issue in this case, until late in the design process:

> We could begin the DRAM before JEDEC information became finalized because most of the DRAM is not the control features that are decided at JEDEC. Most of the DRAM is the memory array, and all of that is going to be the same regardless of what the JEDEC feature/function requirements are and we could add those control features as JEDEC began to make decisions late in the design process.

(Kelley, Tr. 2590; Guilhufe, Tr. 9559 (four features at issue are in the peripheral circuitry, not the memory array)). Third, users of DRAM have not begun work on products to incorporate DDR; as of June 2003, AMD had not started any work to develop product to use DDR2. (Polzin, Tr. 4043-44).

3244. DDR II SDRAM was intended to be a follow-on to DDR rather than a new stand-alone standard. (CX0140 at 3). One of the main benefits of having DDR as the baseline for the new standard was that it allowed the DDR II SDRAM to be "backward compatible" with DDR. (Macri, Tr. 4611-12 ("One of the most critical really design attributes is backwards compatibility. What we do, we don't want to change everything such that when you would design a new system for this DDR2 SDRAM, that it would be absolutely incompatible with the past.")).

Rambus's Response to Finding No. 3244:

The proposed finding is incomplete and irrelevant. While it is true that the Future DRAM task group sought to create a DDR2 standard that was "[b]ackward compatible" with DDR "if possible" (CX 397 at 6), such a desire or convenience does not show that JEDEC was locked in to using the Rambus technologies in DDR2. The evidence shows that JEDEC examined alternatives for each of the four Rambus technologies at issue in this case but continued to select the four technologies for use in DDR2 despite complete awareness of Rambus's issued patents and its requests for royalties.

In late 1998, the Future DRAM Task Group assigned HP to find a way to eliminate on-chip DLL in DDR2. (RX 1306 at 10; Macri, Tr. 4705). In December 1998, HP proposed a means to accomplish this goal, and IBM proposed another means – using a vernier mechanism in place of on-chip PLL. (CX 137 at 3, 4, 27). Despite this investigation, and despite Rambus's assertion of its patents in 1999, no alternative to on-chip PLL/DLL was adopted. (RX 1854 at 12-14 (preliminary DDR2 specification showing mode register and extended mode register using DLL Reset, and DLL Enable/Disable, "passed committee ballots and went to council at June 2001 meeting")). There is no contemporaneous evidence that these proposals were rejected because of "backward compatibility" concerns. In fact, IBM's Mark Kellogg testified that he would, today, support going to an alternative for on-chip PLL/DLL, indicating that no "backward compatibility" concerns prevent a change. (Kellogg, Tr. 5245-47).

After Rambus's patents had issued, JEDEC looked for alternatives for programmable CAS latency, programmable burst length and dual-edge clocking. (Polzin, Tr. 3988, 3996, 4044). As Complaint Counsel's economic expert conceded that it is unlikely that JEDEC would

discuss alternatives in the year 2000 unless at least some significant number of JEDEC members thought that the adoption of the alternatives was feasible at that point in time. (McAfee, Tr. 7571). Again, this shows that no "backward compatibility" concerns prevented switching to alternatives.

In March and April 2000, JEDEC considered alternatives for programmable CAS latency in DDR2, including a proposal by Micron. (RX 1626 at 6; CX 154A at 27; CX 2758 at 1; Lee, Tr. 6779-80). The proposal was rejected. And the evidence shows that the reasons were because of cost concerns, *not* backward compatibility concerns. As Bob Fusco at Hitachi wrote, "For DDR-2, we have no legacy to live with, so I like the Micron proposal." (RX 1626 at 4). Bill Hovis of IBM, however, rejected the proposals because of cost concerns: "What are we really saving here? . . . Any cost savings has to be off-set with the additional component costs associated with adding new part numbers to satisfy CL=2 and CL=3 demands." (RX 1626 at 3). For DDR, Mr. Hovis still supported programmable CAS latency because "ultimately the flexibility of supporting multiple CAS latencies in one device can result in benefits to the customers that end up buying the memory." (*Id.*) Mr. Hovis similarly insisted that DDR2 retain programmable CAS latency, even though he was "not currently locked in": "On DDR II devices, I still want multiple CAS latencies supported for the same reasons. Obviously here, the situation with the system is that I am not currently locked in, so the ability to deal with an additional limitation is not as compelling . . . . However, the same arguments given above apply here. One part number is a benefit to system users, not a deficit. Unless the cost delta is significant (DRAM cost difference >2%, 5%???), I suggest we drop this as an issue." (RX 1626 at 3-4). JEDEC ultimately opted to use Rambus's programmable CAS latency technology in DDR2.

(Polzin, Tr. 4046; RX 1854 at 12-14 (preliminary DDR2 specification showing mode register and extended mode register using programmable CAS latency has passed committee ballots and went to the JEDEC council in June 2001)). Again, there is no contemporaneous evidence to support the proposition that JEDEC rejected alternatives because of "backward compatibility" concerns.

JEDEC also decided to adopt Rambus's programmable burst length technology even though it was well aware that Rambus's patents covered the technology. The preliminary DDR2 specification, published in July 2001, specified a single fixed burst length of 4. (RX 1854 at 20; Macri, Tr. 4733-34; Krashinsky, Tr. 2834 (JEDEC based preliminary DDR2 specification on single (fixed) burst length)). At the September 2001 JC42.3 meeting, however, both Intel and AMD proposed that DDR2 have burst length of 8 in addition to 4. (CX 174 at 7-8). The vote to ballot this proposal was unanimous. (*Id.*) Again, there is no evidence that JEDEC rejected alternatives to Rambus's programmable burst length technology because of any "backward compatibility" concerns. Yet JEDEC adopted Rambus's programmable burst length technology in DDR2 despite complete awareness of Rambus's issued patents and demands for royalties. (Polzin, Tr. 4046-47).

JEDEC also tried to find viable alternatives to Rambus's dual-edge clocking technology to avoid Rambus patents. (Krashinsky, Tr. 2828). At the September 2000 JEDEC meeting, Micron made a proposal that DDR2 incorporate single data rate technology instead of dual-edge clocking. (CX 2769 at 13). In a November 2000 conference call, committee members discussed going to a single data rate ("SDR") technology. (Macri, Tr. 4639-42). The overall consensus of the group was: "Single data rate clock is preferred provided we can make it work." (CX 426 at 4). Despite the consensus to use SDR in place of dual-edge clocking "provided we can make it

work," JEDEC incorporated dual-edge clocking into DDR2. (Polzin, Tr. 4047). There is no contemporaneous evidence that JEDEC rejected alternatives because of "backward compatibility" concerns.

Further, there is no evidence that switching costs were so high as to lock DRAM industry members in to the use of Rambus's technologies.

3245. The Task Group's goal was that the standard be backward compatible in the sense that a DRAM could be designed and fabricated that complied with both the DDR SDRAM standard as well as the follow-on standard. (Kellogg, Tr. 5193; Macri, Tr. 4627-29; CX0392 at 3 ("DDR Based. This means we stay backward compatible if at all possible with DDR. A controller should be able to support both DDR and DDR-II. Initial RAMs might support DDR and DDR-II on the same die.")).

Rambus's Response to Finding No. 3245:

The proposed finding is incomplete and irrelevant. (*See* RRFF 3244).

3246. The Task Group also intended that the standard be backward compatible in the sense that a memory controller could be fabricated that could be used in motherboards designed for DDR as well as for motherboards designed to be used with the new standard. (CX0380 at 7; CX2717 at 13; CX2767 at 5 ("In every generation so far, we have been able to maintain the possibility of allowing controllers to be designed to support either old or new memory technology."); CX0397 at 2; Lee, Tr. 6770-73; Macri, Tr. 4625-27).

Rambus's Response to Finding No. 3246:

The proposed finding is incomplete and irrelevant. (*See* RRFF 3244).

3247. For DDR II SDRAM, this sort of backward compatibility could solve what is sometimes known as the "chicken and egg" problem that faces the DRAM industry when it transitions from an old standard to a new standard. (Macri, Tr. 4625-29). The problem, which can hinder the acceptance of new DRAM standards like DDR II SDRAM, is that industry acceptance of a new DRAM standard requires the existence of additional compatible components, including particularly memory controllers. Those same considerations dictate that sales of a memory controller depend on the existence of compatible DRAMs. In both cases, unless one is available, the firms making the other will be hesitant to produce their component. (CX2315 at 1; Macri, Tr. 4619-20) ("It is a chicken and an egg problem..... The vendors won't line up to produce the device unless there are users.... but the users won't consider the part unless the suppliers/infrastructure is in place.")).

Rambus's Response to Finding No. 3247:

The proposed finding is incomplete and irrelevant. (*See* RRFF 3244).

3248. The benefit of backward compatibility to DRAM manufacturers is that it solves the chicken and egg problem by allowing them to produce DRAMs compliant with the new standard, but which could be sold as DRAMs compliant with the old standard if the new standard does not get accepted as quickly as expected. (Macri, Tr. 4627-29 (The DRAM manufacturers are "doing a design believing the user community will be there ready to accept it, but they too, don't have control of their destiny. They're dependent on the users and other people to build the infrastructure. So, they want to make sure that the design they do still has a market, and this allows them to ... manage that transition from the previous technology to the new technology with a minimum amount of risk.")).

Rambus's Response to Finding No. 3248:

The proposed finding is incomplete and irrelevant. (*See* RRFF 3244).

3249. Backward compatibility has the same benefit for producers of memory controllers. (Macri, Tr. 4625-26 ("We mitigate the risk in moving ahead to a new technology. A new technology could be delayed, so it's important if you're designing a system to use that new technology, if that technology was delayed for any reason, that it would be easy to use the old technology so you could still bring it to market.") ; Kellogg, Tr. 5191-92; *see also,* Wagner, Tr. 3874-75).

Rambus's Response to Finding No. 3249:

The proposed finding is incomplete and irrelevant. (*See* RRFF 3244).

3250. As a result of the fact that DDR was chosen as the baseline for the new standard, a number of technologies from DDR were imported into that standard. (Macri, Tr. 4613 ("[W]e wanted to pick the base architecture of the device,... the DRAM we would start with, and then modify it to form the standard, the new standard, DDR-2"). Among the technologies imported into the new standard because of the choice of DDR as the baseline were programmable CAS latency, dual-edged clocking of data off of a data strobe, and the use of a DLL on the DRAM to align the clock on the DRAM with the system clock. (Macri, Tr. 4633-35).

Rambus's Response to Finding No. 3250:

The proposed finding is incomplete and irrelevant. (*See* RRFF 3244). The evidence shows that JEDEC considered alternatives for each of these technologies, even after Rambus's

patents issued and Rambus was requesting royalties for the technologies, yet JEDEC still adopted the Rambus technologies. (*Id.*)

3251. One technology that was originally slated for removal from the baseline in the new standard was programmable burst length using the mode register. The new standard was originally set to have a fixed burst length of 4. Another technology that was slated for removal was the SDRAM burst interrupt instruction. (CX0392 at 1). However, in June of 2001, after a series of presentations from Intel, AMD and the ADT group, the task group determined that there were performance benefits for some high bandwidth applications from allowing a burst length of 8 as well as 4. (Macri, Tr. 4601-602; CX0174 at 35 ("Potential Improvement of 4-10% On High-Bandwidth Applications Such As SpecFP2000"); see DX46 at 4). The changes between June of 2001 and September of 2001 to add programmable burst length and burst interrupt were not disruptive to the standard because they added to the functionality of the standard and did not eliminate existing functionality. (Macri, Tr. 4600).

Rambus's Response to Finding No. 3251:

The proposed finding is incomplete. The preliminary DDR2 specification, published in July 2001, specified a single fixed burst length of 4. (RX 1854 at 20; Macri, Tr. 4733-34; Krashinsky, Tr. 2833-34 (JEDEC based preliminary DDR2 specification on single (fixed) burst length)). At the September 2001 JC42.3 meeting, however, both Intel and AMD proposed that DDR2 have burst length of 8 in addition to 4. (CX 174 at 7-8). This meant the use of Rambus's programmable burst length technology. At the time, committee members were well aware of Rambus's issued patents and its demands for royalties. (Polzin, Tr. 4046-47; Rhoden, Tr. 529; Macri, Tr. 4667-8). Yet the vote to ballot this proposal was unanimous. (CX 174 at 7-8).

3252. At some point, replacement of the fixed burst length of 4 with a fixed burst length of 8 would have been disruptive. (Macri, Tr. 4600 ("[S]ome systems take a very long time to design, and it's really important that,... we provide stability to the designers. If we were to make a change that would cause them to go back and essentially tear up their design, we would be forcing companies to incur great expense,... not only on the design period but also on their product lines.") *see also,* 4771-72, *in camera*; Polzin, Tr. 3993-94). In 2002, for example, NVidia was planning for its next generation graphics processor to be compatible with DRAM having a burst length of 4. (Wagner, Tr. 3853). A change in the available burst lengths for DDR II SDRAM that eliminated that burst length in favor of a burst length of 8 would require nearly 2

years of design work for the graphics processor to be able to efficiently operate with that DRAM. (CX2829 at 1; Wagner, Tr. 3852-53).

Rambus's Response to Finding No. 3252:

The proposed finding is misleading and incomplete. The preliminary DDR2 specification used a single fixed burst length of 4 – eliminating the ability to use a burst length of 8; JEDEC members voted unanimously to add Rambus's programmable burst length technology to allow for the use of a burst length of 8 despite complete awareness of Rambus's issued patents and its requests for royalties. (*See* RRFF 3251).

3253. Other changes to the baseline were considered by the Future DRAM Task Group, including the elimination of the use of the on-chip DLL, the elimination of dual edged clocking in favor of a faster single edged clock, and the replacement of programmable CAS latency. CCFF 3254, 3256; CX2758 at 2 (DDR II SDRAM presentation to JEDEC discussing the possibility of eliminating read latency from existing and future SDRAM standards); Lee, Tr. 6777-80 (discussing CX2758)).

Rambus's Response to Finding No. 3253:

The proposed finding is incomplete. Consideration of alternatives for Rambus's dual-edge clocking and programmable CAS latency technologies was made with full knowledge of Rambus's issued patents and requests for royalties. (*See* RRFF 3244).

3254. The elimination of the DLL from the DDR II SDRAM was considered early on in the standard setting process. (RX1306-001 at 8) ("HP will look at removing DLL and its impact on turnaround time."). At the time, the Task Group considered eliminating the DLL from the DRAM as a way to simplify the DRAM. (Macri, Tr. 4623). Eliminating the DLL from the DRAM was rejected because it would have been difficult to design a controller that would be compatible with both the DDR SDRAM that had a DLL and the new standard which would not have a DLL. (Macri, Tr. 4623-24 ("[I]t was decided since we were DDR-based that we should preserve the clock system to keep the backwards compatibility...") , *see also* 4646-48 (DLL on the DRAM "was already in the DDR1 JEDEC standard. Backwards compatibility was extremely important to our products, and we would have then forced ourselves to make a fundamental change in the clocking methodology, ... it's the thing we focus on first, because it is the most important feature of any system.")).

Rambus's Response to Finding No. 3254:

The proposed finding is not supported. The sole basis for the finding is the testimony of Joe Macri, who admitted on cross-examination that {

} (Macri, Tr. 4786 (*in camera*)). In fact, he admitted that {

}. (*Id.*) He also admitted that after {

}. (Macri, Tr. 4783 (*in camera*)). Nor did he {

}. (Macri, Tr. 4783-84 (*in camera*)).

Although there are contemporaneous documents discussing the proposed elimination of on-chip PLL/DLL, none of these documents discusses "backward compatibility" as a reason to reject the alternatives. For instance, HP's proposal to eliminate the on-chip PLL did not make any mention of "backward compatibility" concerns. (CX 137 at 27). Nor do the minutes of the Task Group meeting at which the proposal was discussed. (CX 137 at 3). Similarly, there is no mention of "backward compatibility" concerns with regard to IBM's proposal to use verniers. (CX 137 at 4). Notes from the Task Group discussions, however, list the "pro and con of having dll on ram" as "con is power" and "pro is can update during refresh." (RX 1376 at 4). There is no mention of "backward compatibility" as a concern.

3255. By 2000, removing the DLL would have led to the additional problem of requiring that firms that had been either designing DDR II SDRAMs, or designing products to be compatible with DDR II SDRAM, to redesign their systems. (Macri, Tr. 4649) ("[basically the earliest adopters would have had to go back to the design stage. Clocking is not something they can change in a trivial manner.... So, I mean, it's not something you want to go change at that

point in time. You really need a gun to your head.")).

Rambus's Response to Finding No. 3255:

The proposed finding is misleading and unsupported. There is no evidence of any significant design work done prior to 2000. For instance, Micron began its design work for DDR {

} (Shirley, Tr. 4211 (*in camera*); Rhoden, Tr. 529). It did not complete the "tape out" of its first DDR2 design until { }. (Shirley, Tr. 4228 (*in camera*)). As of June 2003, AMD had not started any work to develop product to use DDR2. (Polzin, Tr. 4043-44). The proposed finding rests solely on the testimony of Joe Macri, who does not work for a DRAM manufacturing company and whose testimony on this issue is not entitled to great weight. (*See* RRFF 3254).

3256. The replacement of dual edged clocking of data was considered in September of 2000 in a proposal by Micron. (CX2769 at 13; Lee, Tr. 6795-6798). The proposal was followed by a "DDRII clocking conference call" in November of 2000 that was set up in response to the proposal by Micron. (CX0426; Lee, Tr. 6798; Macri, Tr. 4639-40). At the conference call and the following JEDEC meeting, participants decided that the faster single-edge clock was feasible, but decided they needed to retain dual-edged clocking in the DDR II SDRAM standard. (Macri, Tr. 4641-42; Lee, Tr. 6799).

Rambus's Response to Finding No. 3256:

The proposed finding is incomplete. The purpose of the discussion in the Task Group of using single data rate technology was to try to avoid Rambus's patents. (Krashinsky, Tr. 2828). In the November 2000 conference call, committee members discussed going to a single data rate ("SDR") technology. (Macri, Tr. 4639-42). The minutes of that meeting reflect a consensus to try to adopt SDR if it would work. Those minutes state, "HP – prefers SDR" and indicate that for IBM, "Single data rate clocks are acceptable provided that it works." (CX 426 at 2). The

minutes also indicate that IBM agreed "with the need to avoid I.P. issues." (CX 426 at 3). The minutes continue, "In general, everyone agreed that SDR clock is ok provided that it works." (CX 426 at 4). The overall consensus of the group was: "Single data rate clock is preferred provided that we can make it work." (CX 426 at 4).

3257. One concern of those opposed to change was the late date of the proposal and the potential for such a change to be disruptive in the sense that it would cause the firms that had been working on designing products compliant with the new standard to have to throw away much of the work they had done. (Kellogg, Tr. 5201 (The proposal to eliminate dual edged clocking from the DDR II SDRAM standard "was a significant change to the DDR-II data capture structure, and IBM was already moving down the path of designing our first DDR-II memory controllers at this time."); (Macri, Tr. 4649-51); (Wagner, Tr. 3869) ("[They would have,... brought in suggestions to change the technology and we would have said, we already have a standard, we don't really want to change, or we're on a development cycle that cannot tolerate the schedule hit."); Peisl, Tr. 5545-55).

Rambus's Response to Finding No. 3257:

The proposed finding is not supported by the weight of the evidence. The proposed finding cites the testimony of Mark Kellogg that he recommended that IBM oppose the proposal to use single data rate instead of Rambus's dual-edge clocking technology. The minutes of the November 2001 Task Group conference call, however, show that for IBM, "Single data rate clocks are acceptable provided that it works." (CX 426 at 2) (emphasis added). Mr. Kellogg's testimony is therefore contrary to the contemporaneous evidence that IBM was in favor of the proposal.

The proposed finding also cites the testimony of Joe Macri. He testified that adopting single data rate would have caused companies who were already designing DDR2 parts to have to revise their designs. Mr. Macri does not work for a DRAM manufacturing company, and his testimony on this issue is not entitled to great weight. (*See* RRFF 3254). The contemporaneous

documents show that ATI was in favor of the single data rate alternative. (CX 426 at 2). Moreover, there is no evidence shows that any company had made significant investments in DDR2 design. (*See* RRFF 3255). And the overall consensus of the Task Group was: "Single data rate clock is preferred provided we can make it work." (CX 426 at 4).

The proposed finding also cites Barry Wagner. But he testified that nVidia left it up to the DRAM manufacturers as to whether they would change the standard to avoid Rambus's patents: "At some point, I don't recall exactly what year, memory vendors came to us and said would you like to change this, we're finding some IP issues over it, *and our feedback was, well, if the industry is going to change, we need to change with it and we basically left it up to them to go off and decide to change or not*." (Wagner, Tr. 3868-69) (emphasis added).

There is no evidence that any firms had made significant design investments by the time of Micron's proposal. (*See* RRFF 3255). There is no evidence that switching costs were so high as to lock the DRAM industry in to using Rambus's technology for DDR2.

3258. By September of 2000, a number of firms were already planning and designing products for use with the new DDR II SDRAM standard. (Macri, Tr. 4648-49). Consequently, a number of participants in the conference call were strongly opposed to changing the clocking of the new DRAM standard to eliminate dual edged clocking. (Kellogg, Tr. 5204 ("One [potential impact of Micron's proposal on IBM] is our DDR-I controller or interface chip that also included DDR-II would very likely see measurable schedule delay due to the significance of the changes.")).

Rambus's Response to Finding No. 3258:

The proposed finding is contrary to the contemporaneous evidence. The minutes of the November 2000 conference call show that the consensus of the committee members was to go to a single data rate technology. The minutes state, "HP – prefers SDR"; IBM "– Single data rate clocks are acceptable provided that it works"; ATI "– Prefers single data rate"; Micron "– Prefers

single data rate clock, if possible." (CX 426 at 2). The minutes continue, "In general, *everyone agreed* that SDR clock is ok provided that it works." (CX 426 at 4) (emphasis added). The "Overall Summary" of the meeting states, "Single data rate clock is preferred provided we can make it work." (CX 426 at 4).

The proposed finding cites the testimony of IBM's Mark Kellogg for the proposition that there was opposition to the proposal. The minutes of the November 2001 Task Group conference call, however, show that for IBM, "Single data rate clocks *are acceptable* provided that it works." (CX 426 at 2) (emphasis added). Mr. Kellogg's testimony is therefore contrary to the contemporaneous evidence that IBM was in favor of the proposal.

Mr. Macri does not work for a DRAM manufacturing company, and his testimony on this issue is not entitled to great weight. (*See* RRFF 3254). Further, the contemporaneous evidence shows that he was in favor of the single data rate proposal. (CX 426 at 2 ("ATI . . .– Prefers single data rate").

There is no evidence that switching costs were so high as to lock the DRAM industry in to using Rambus's technology for DDR2.

3259. A second concern was that the changes proposed by Micron to allow for single data rate clocking had the potential to delay the DDR II SDRAM standard, potentially indefinitely. (Kellogg, Tr. 5204-205 ("[W]e had systems in our product plan planning to use DDR-II and our belief was that the introduction of a total new clock structure would possibly prevent our ability to use DDR-II at all because there were so many new things to consider in the committee and it would slow down DDR-II indefinitely.").

Rambus's Response to Finding No. 3259:

The proposed finding cites the testimony of IBM's Mark Kellogg for the proposition that there was concern about delay due to Micron's proposal. The minutes of the November 2001

Task Group conference call, however, show that for IBM, "Single data rate clocks *are acceptable* provided that it works." (CX 426 at 2) (emphasis added). Mr. Kellogg's testimony is therefore contrary to the contemporaneous evidence that IBM was in favor of the proposal.

There is no evidence that switching costs were so high as to lock the DRAM industry in to using Rambus's technology for DDR2.

3260. A third concern was that the replacement of the DDR-type clocking with the clocking system proposed by Micron was so different from the DDR-type that it would be very difficult to design a controller that would be able to accommodate both technologies, thus eliminating backward compatibility with the DDR standard. (Lee, Tr. 6805-806 ("It is difficult to design a controller to support the future technology and the old technology with this kind of clocking scheme because it's so different from the old technology's clocking scheme. It's a very difficult design to accommodate."); Macri, Tr. 4640, 4649-50).

Rambus's Response to Finding No. 3260:

The proposed finding is unsupported. The proposed finding cites Micron's Kevin Lee for the proposition that there was a concern about the proposal because of a difficulty in designing a controller to work with DDR and DDR2. But this difficulty did not stop Mr. Lee's employer, Micron, from making the proposal. (CX 2769 at 13). Nor did it stop the Future DRAM Task Group from agreeing to use single data rate technology provided it worked. (CX 426 at 4 ("In general, *everyone agreed* that SDR clock is ok provided that it works.") (emphasis added)).

Mr. Macri does not work for a DRAM manufacturing company, and his testimony on this issue is not entitled to great weight. (*See* RRFF 3254). Further, the contemporaneous evidence shows that he was in favor of the single data rate proposal. (CX 426 at 2 ("ATI . . .– Prefers single data rate").

There is no evidence that switching costs were so high as to lock the DRAM industry in to using Rambus's technology for DDR2.

3261. Finally, the use of the Micron proposal in place of the DDR-type clocking scheme was opposed by DRAM customers. (Lee, Tr. 6806) ("We had made customer visits, and they wanted to have one standard that they felt could be designed and controlled to deal with the transition strategies for DDR and DDR2 simultaneously."); Krashinsky, Tr. 2829 ("[W]e already decided how – how DDR is going to look like, the clocking, and if we are going to change DDR-II from DDR-I, the clocking rate is going to be too dramatic to the – its going to be what we call a revolutionary change rather than evolutionary change, and that's why, to my knowledge, the committee decided not to go ahead with it.")).

Rambus's Response to Finding No. 3261:

The proposed finding is not supported by the weight of the evidence. The Future DRAM Task Group included the most important DRAM customers – Intel, HP, AMD, and IBM. (CX 426 at 3). Those customers "*agreed* that SDR clock is ok provided that it works." (CX 426 at 4 (emphasis added)). Mr. Krashinsky's testimony is undermined by the contemporaneous evidence that he, on behalf of HP, favored the proposal. (CX 426 at 2 ("HP . . . – prefers SDR")). There is no contemporaneous evidence supporting the proposed finding.

There is no evidence that switching costs were so high as to lock the DRAM industry in to using Rambus's technology for DDR2.

UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

In the Matter of	)	
	)	Docket No. 9302
RAMBUS INCORPORATED, a corporation.	)	

CERTIFICATE OF SERVICE

I, Jacqueline M. Haberer, hereby certify that on October 1, 2003, I caused a true and correct copy of *Rambus Inc.'s Responses to Complaint Counsel's Proposed Findings of Fact, Volume III (Public)* to be served on the following persons by hand delivery:

Hon. Stephen J. McGuire
Chief Administrative Law Judge
Federal Trade Commission
Room H-112
600 Pennsylvania Avenue, N.W.
Washington, D.C. 20580

Donald S. Clark, Secretary
Federal Trade Commission
Room H-159
600 Pennsylvania Avenue, N.W.
Washington, D.C. 20580

Richard B. Dagen, Esq.
Assistant Director
Bureau of Competition
Federal Trade Commission
601 New Jersey Avenue, N.W.
Washington, D.C. 20001

M. Sean Royall, Esq.
Deputy Director, Bureau of Competition
Federal Trade Commission
Room H-372
600 Pennsylvania Avenue, N.W.
Washington, D.C. 20580

Malcolm L. Catt, Esq.
Attorney
Federal Trade Commission
601 New Jersey Avenue, N.W.
Washington, D.C. 20001

Jacqueline M. Haberer