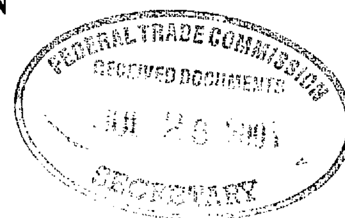
PUBLIC

UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION



In the Matter of **RAMBUS INC.,** **a corporation.**	**Docket No. 9302**

REQUEST FOR OFFICIAL NOTICE OF VARIOUS UNITED STATES PATENTS

I. INTRODUCTION

Respondent Rambus Inc. ("Rambus") respectfully asks the Court to take official notice of various issued United States patents. The existence of these patents, their dates of filing and issuance, and all other material set forth on their face, are indisputable matters of public record. These facts are properly noticed under Commission Rule of Practice 3.43(d), 16 C.F.R. § 3.43(d), and Federal Rule of Evidence 201(b)(2).

II. ARGUMENT

The Commission regularly takes official notice of government records and publications under Commission Rule 3.43(d) and Federal Rule of Evidence 201. *See, e.g.*, *In re Ethyl Corp.*, 101 F.T.C. 425, 1983 FTC LEXIS 91, at *508 n.12 (1983) (presidential economic report); *In re Beauty-Style Modernizers, Inc.*, 83 F.T.C. 1761, 1974 FTC LEXIS 227, at *39 n.7 (1974) (Federal Reserve Board publication); *In re Avnet, Inc.*, 82 F.T.C. 391, 1973 FTC LEXIS 125, at *132 (1973) (U.S. census data).

Like the official government records at issue in those cases, the issued U.S. patents set forth below are official government records and publications suitable for official notice.

Federal Rule of Evidence 201, on which Commission Rule 3.43(d) is based, provides for judicial notice of adjudicative facts that are capable of accurate and ready determination by resort to sources whose accuracy cannot reasonably be questioned. *See* Fed. R. Evid. 201(b)(2).[1]

The patents listed below fall squarely within the scope of judicial notice set forth in Fed. R. Evid. 201(b)(2). The federal courts regularly take judicial notice of issued patents. *See, e.g., Thomas & Betts Corp. v. Panduit Corp.*, 65 F.3d 654, 664 n.12 (Fed. Cir. 1995); *Hoganas AB v. Dresser Indus., Inc.*, 9 F.3d 948, 954 n.27 (Fed. Cir. 1994); *Hay & Forage Indus. v. New Holland North Am., Inc.*, 25 F. Supp. 2d 1170, 1175 n.2 (D. Kan. 1998); *cf. Standard Havens Products, Inc.*, 897 F.2d 511, 514 n.3 (Fed. Cir. 1990) (taking judicial notice of record of reexamination proceeding).

For these reasons, and in the interest of avoiding needless consumption of the Court's time rehearsing these patents during trial, Rambus asks the Court to take official notice of the following issued U.S. patents. Each patents relates to one of three categories: A) Micron's burst EDO patents (discussed with Micron engineer Brett Williams on Day 4 of the Hearing);[2] B) various patents covering JEDEC standards; and C) various Rambus patents.

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[1] The federal courts, under Federal Rule of Evidence 201(d), must take judicial notice if asked by a party and supplied the necessary information. *See* Fed. R. Evid. 201(d).

[2] *See, e.g.,* 4 Tr. 936 (Brett Williams cross examination):

> Q. Okay, let's look at the next patent, if we can. What I'm going to do is let's skip all the way ahead and fill out the demonstrative ... because I can put these patents in through a stipulation or some other fashion if that speeds things up.

Each patent has been assigned an exhibit number, and is attached to this motion at the tab indicated below:

Category	*U.S. Patent number*	*Exhibit*	*Tab*
A	5,526,320	RX730	1
A	5,598,376	RX861	2
A	5,610,864	RX886	3
A	5,640,364	RX947	4
A	5,652,724	RX974	5
A	5,661,695	RX987	6
A	5,668,773	RX999	7
A	5,675,549	RX566	8
A	5,696,732	RX1071	9
A	5,706,247	RX1085	10
A	5,717,654	RX1098	11
A	5,721,859	RX1107	12
A	5,729,503	RX1124	13
A	5,757,703	RX2308	14
A	5,802,010	RX1241	15
A	5,812,488	RX1272	16
A	5,831,932	RX1305	17
A	5,850,368	RX1354	18
A	5,963,504	RX1514	19
B	5,631,871	RX925	20
B	5,808,958	RX2309	21
B	5,838,990	RX1309	22
B	5,982,694	RX2310	23
B	5,986,968	RX2311	24
B	6,028,816	RX2312	25
B	6,289,413	RX1890	26
B	6,356,484	RX2313	27
C	6,591,353	RX2314	28

III. CONCLUSION

For these reasons the Court should take official notice of the aforementioned patents.

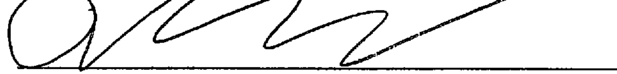
Judge McGuire: That would be helpful.

Mr. Stone: Otherwise, I will ask you to take judicial notice.

Judge McGuire: All right.

DATED: July 28 2003

Respectfully submitted,



Gregory P. Stone
Steven M. Perry
Peter A. Detre
Adam R. Wichman
MUNGER, TOLLES & OLSON LLP
355 South Grand Avenue, 35th Floor
Los Angeles, California 90071
(213) 683-9100
(213) 687-3702 (facsimile)
(202) 663-6158
(202) 457-4943 (facsimile)

Douglas Melamed
Kenneth A. Bamberger
WILMER, CUTLER & PICKERING
2445 M Street, N.W.
Washington, D.C. 20037
(202) 663-6000

Sean C. Cunningham
John M. Guaragna
Gray, Cary, Ware & Freidenrich LLP
401 "B" Street, Suite 2000
San Diego, California 92101
(619) 699-2700

Attorneys for Respondent Rambus Inc.

UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

In the Matter of RAMBUS INC., a corporation.	Docket No. 9302

ORDER GRANTING RESPONDENT RAMBUS INC.'S REQUEST FOR OFFICIAL NOTICE OF VARIOUS UNITED STATES PATENTS

Rambus's Request For Official Notice of Various United States Patents is hereby GRANTED. The Court takes official notice, under Commission Rule of Practice 3.43(d), 16 C.F.R. § 3.43(d), and Federal Rule of Evidence 201(b)(2), of the following issued U.S. patents, which are hereby admitted as trial exhibits:

U.S. Patent number	*Exhibit*
5,526,320	RX730
5,598,376	RX861
5,610,864	RX886
5,640,364	RX947
5,652,724	RX974
5,661,695	RX987
5,668,773	RX999
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5,717,654	RX1098
5,721,859	RX1107
5,729,503	RX1124
5,757,703	RX2308
5,802,010	RX1241
5,812,488	RX1272
5,831,932	RX1305
5,850,368	RX1354
5,963,504	RX1514
5,631,871	RX925

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5,808,958	RX2309
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5,986,968	RX2311
6,028,816	RX2312
6,289,413	RX1890
6,356,484	RX2313
6,591,353	RX2314

IT IS SO ORDERED.

Date: ___________

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Stephen J. McGuire
Chief Administrative Law Judge

US005526320A

United States Patent [19]

Zagar et al.

[11] **Patent Number: 5,526,320**

[45] **Date of Patent: Jun. 11, 1996**

[54] **BURST EDO MEMORY DEVICE**

[75] Inventors: **Paul S. Zagar**, Boise; **Brett L. Williams**, Eagle; **Troy A. Manning**, Boise, all of Id.

[73] Assignee: **Micron Technology Inc.**, Boise, Id.

[21] Appl. No.: **370,761**

[22] Filed: **Dec. 23, 1994**

[51] Int. Cl.^{6} **G11C 8/00**

[52] U.S. Cl. **365/233.5**; 365/230.08; 365/238.5; 365/189.05

[58] Field of Search 365/230.01, 230.06, 365/230.08, 238.5, 233.5, 235, 189.05, 236

[56] **References Cited**

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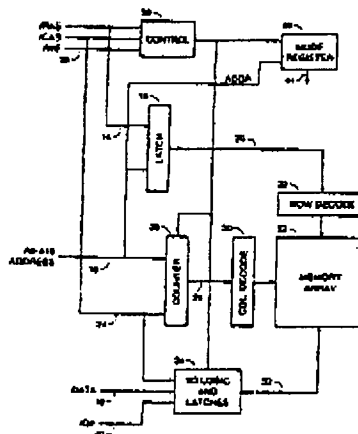
Primary Examiner—David C. Nelms
Assistant Examiner—Tan T. Nguyen
Attorney, Agent, or Firm—Greg A. Blodgett

[57] **ABSTRACT**

An integrated circuit memory device is designed for high speed data access and for compatibility with existing memory systems. An address strobe signal is used to latch a first address. During a burst access cycle the address is incremented internal to the device with additional address strobe transitions. A new memory address is only required at the beginning of each burst access. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at the device cycle frequency. Transitions of the Read/Write control line during a burst access will terminate the burst access, reset the burst length counter and initialize the device for another burst access. The device is compatible with existing Extended Data Out DRAM device pinouts, Fast Page Mode and Extended Data Out Single In-Line Memory Module pinouts, and other memory circuit designs.

49 Claims, 8 Drawing Sheets



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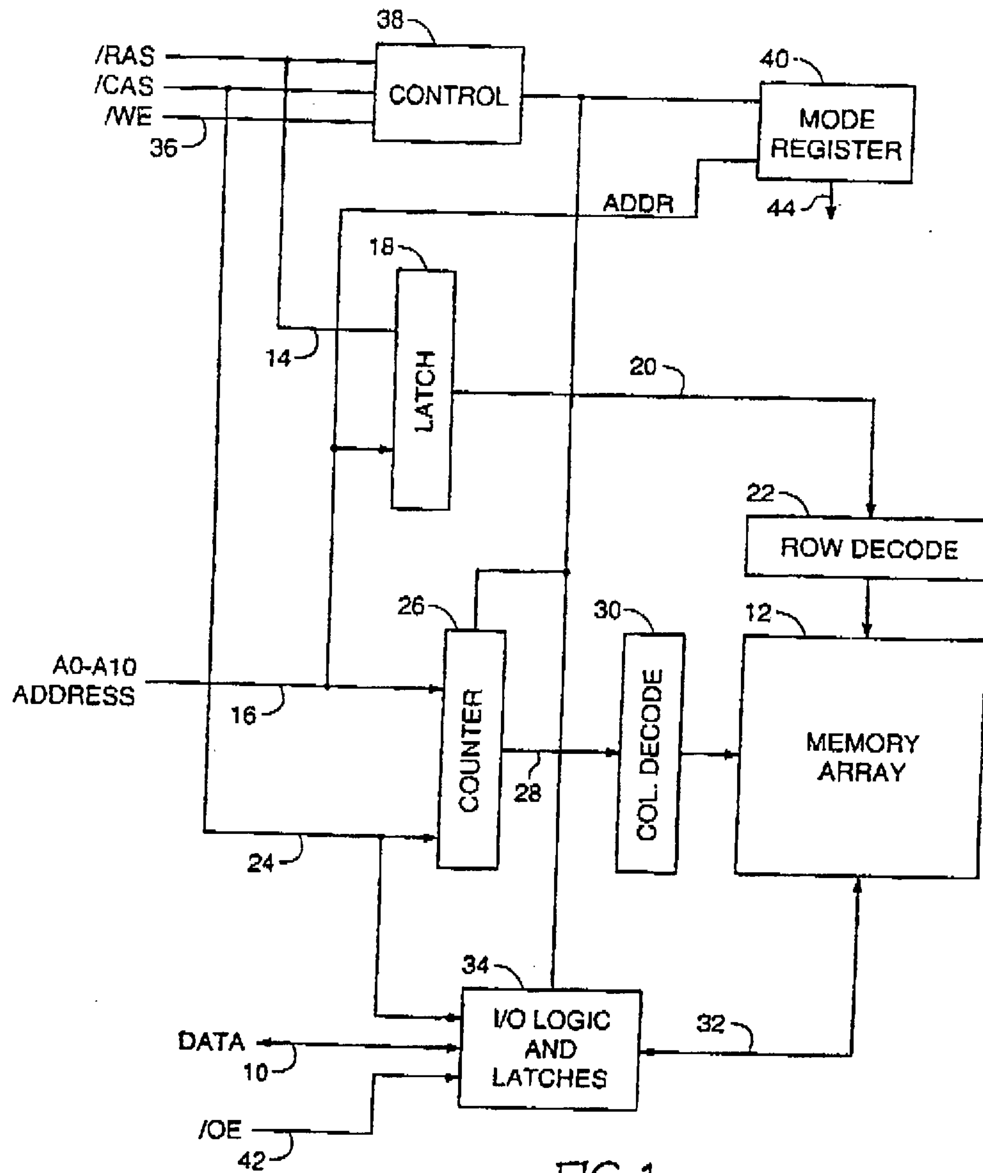


FIG. 1

Burst Length	Starting Column Address			Linear	Interleave
	A_2	A_1	A_0		
2	V	V	0	0-1	0-1
	V	V	1	1-0	1-0
4	V	0	0	0-1-2-3	0-1-2-3
	V	0	1	1-2-3-0	1-0-3-2
	V	1	0	2-3-0-1	2-3-0-1
	V	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

FIG. 2

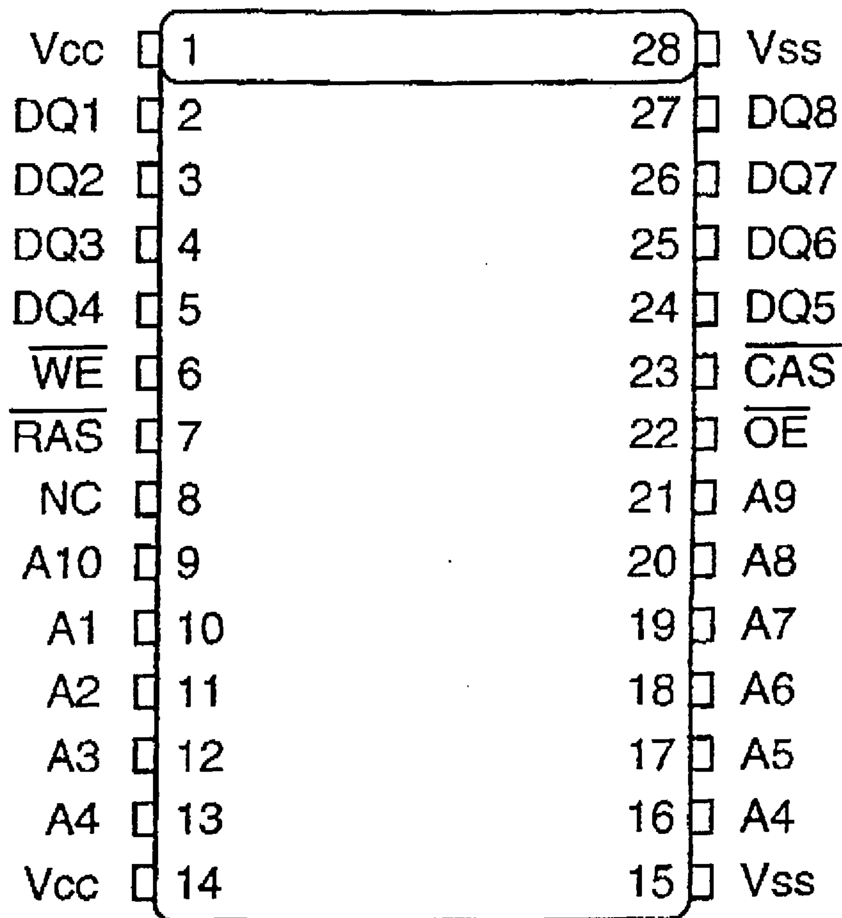


FIG. 3

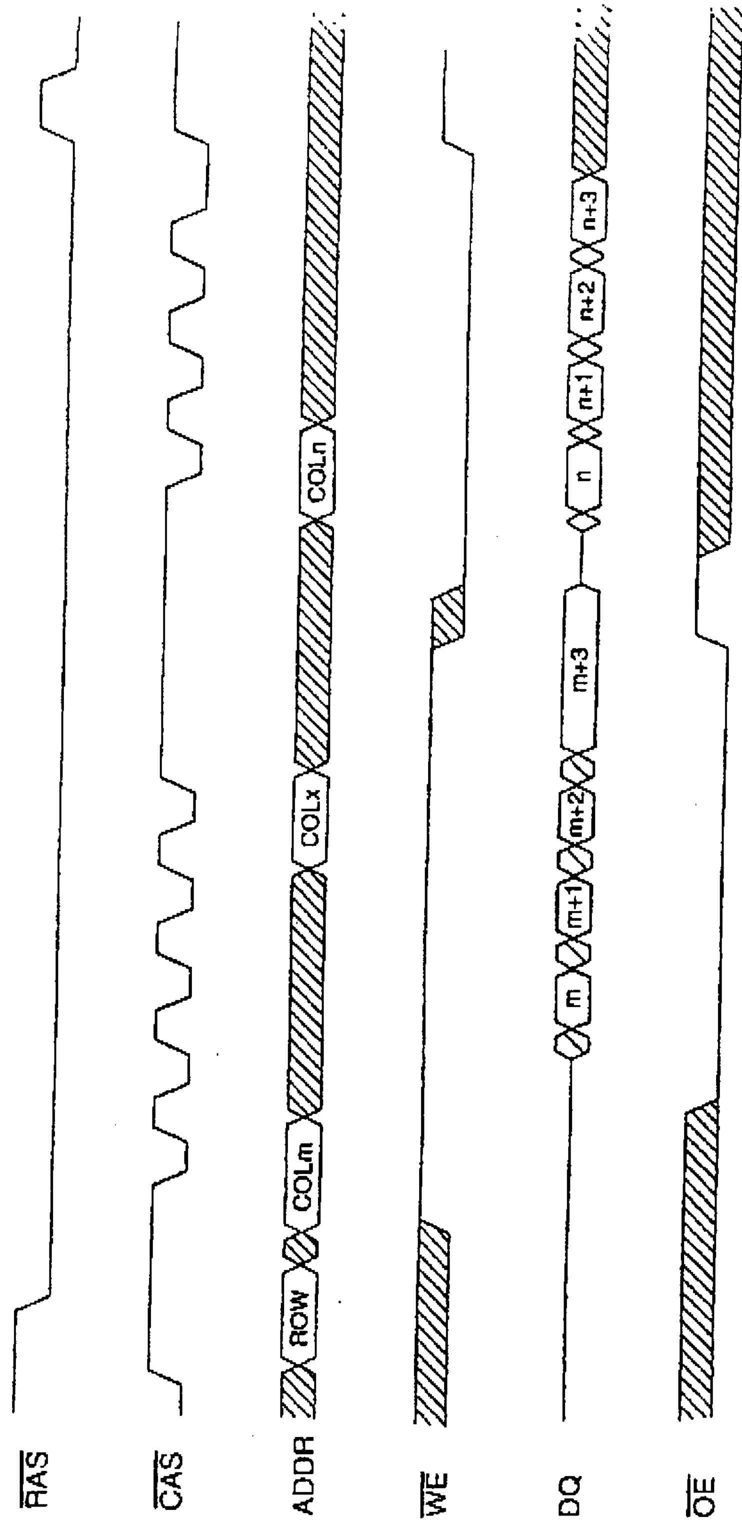


FIG. 4

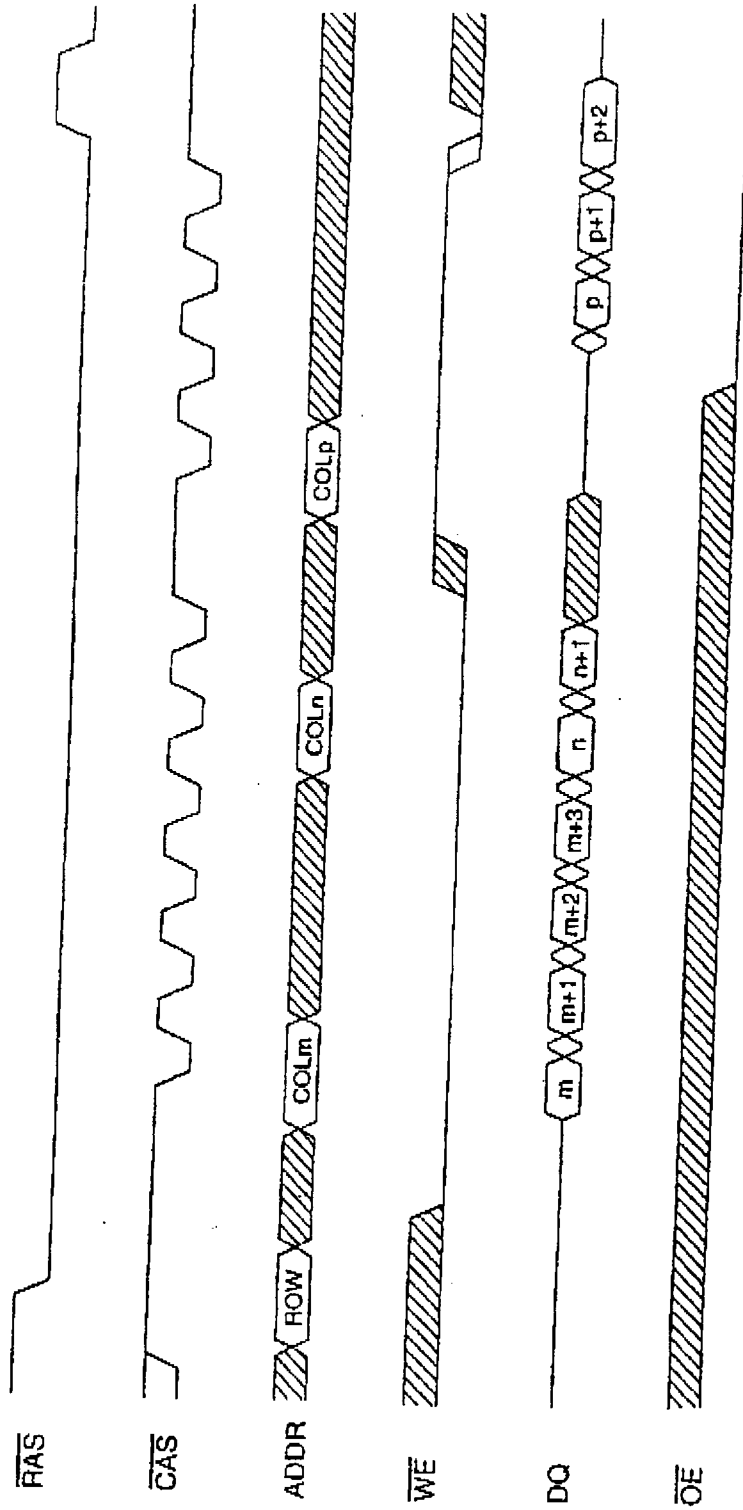


FIG. 5

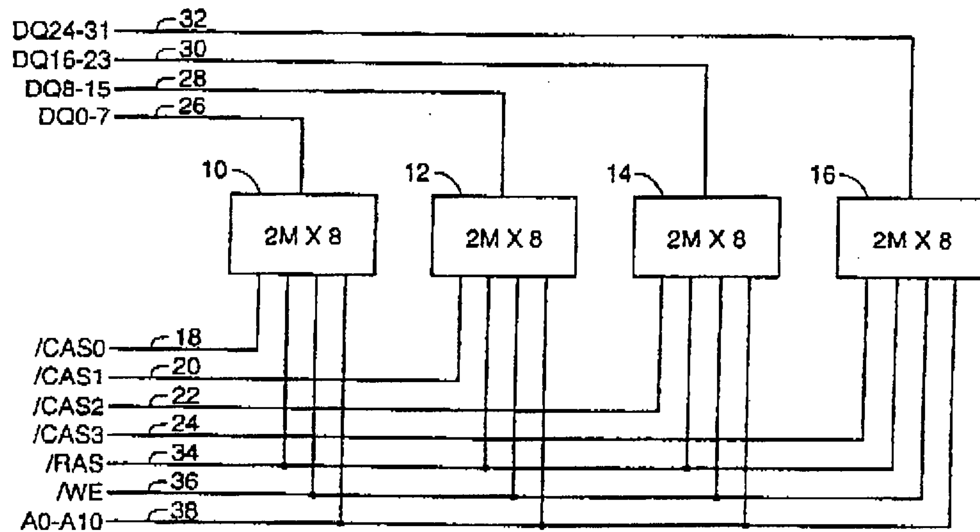


FIG. 6

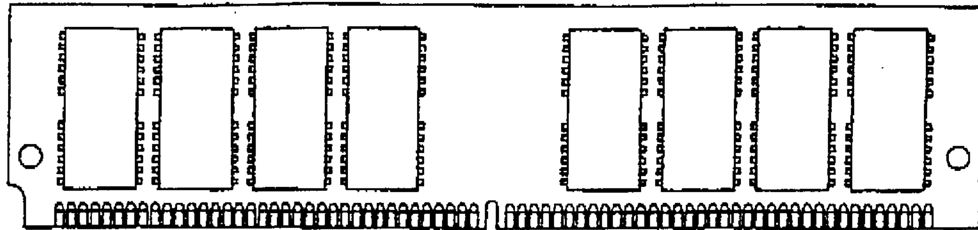


FIG. 7

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	$\overline{RAS1}$	63	DQ15
10	Vcc	28	A7	46	$\overline{OE}$	64	DQ32
11	PD5	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	PD ECC	66	PD EDO
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ25	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	NC	52	DQ26	70	PD4
17	A5	35	NC	53	DQ11	71	PD refresh
18	A6	36	NC	54	DQ27	72	Vss

FIG. 8

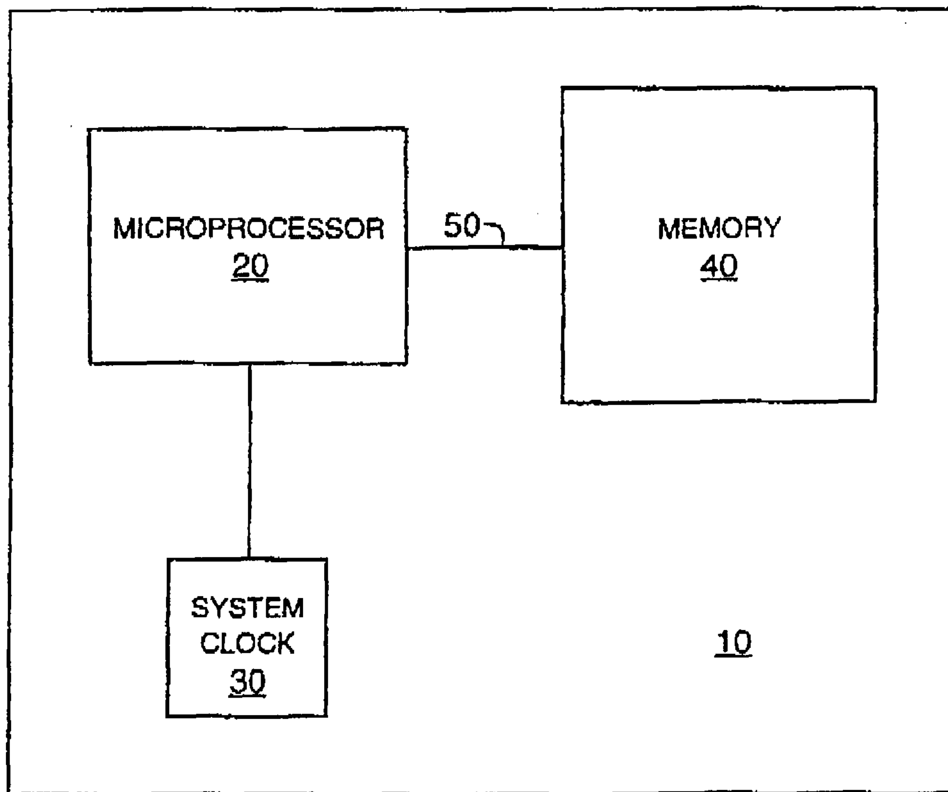


FIG. 9

BURST EDO MEMORY DEVICE

FIELD OF THE INVENTION

This invention relates to memory device architectures designed to provide high density data storage with high speed read and write access cycles.

BACKGROUND OF THE INVENTION

Dynamic Random Access Memory devices (DRAMs) are among the highest volume and most complex integrated circuits manufactured today. Except for their high volume production, the state of the art manufacturing requirements of these devices would cause them to be exorbitantly priced. Yet, due to efficiencies associated with high volume production, the price per bit of these memory devices is continually declining. The low cost of memory has fueled the growth and development of the personal computer. As personal computers have become more advanced, they in turn have required faster and more dense memory devices, but with the same low cost of the standard DRAM. Fast page mode DRAMs are the most popular standard DRAM today. In fast page mode operation, a row address strobe (/RAS) is used to latch a row address portion of a multiplexed DRAM address. Multiple occurrences of the column address strobe (/CAS) are then used to latch multiple column addresses to access data within the selected row. On the falling edge of /CAS an address is latched, and the DRAM outputs are enabled. When /CAS transitions high the DRAM outputs are placed in a high impedance state (tri-state). With advances in the production of integrated circuits, the internal circuitry of the DRAM operates faster than ever. This high speed circuitry has allowed for faster page mode cycle times. A problem exists in the reading of a DRAM when the device is operated with minimum fast page mode cycle times. /CAS may be low for as little as 15 nanoseconds, and the data access time from /CAS to valid output data (tCAC) may be up to 15 nanoseconds; therefore, in a worst case scenario there is no time to latch the output data external to the memory device. For devices that operate faster than the specifications require, the data may still only be valid for a few nanoseconds. On a heavily loaded microprocessor memory bus, trying to latch an asynchronous signal that is valid for only a few nanoseconds is very difficult. Even providing a new address every 35 nanoseconds requires large address drivers which create significant amounts of electrical noise within the system. To increase the data throughput of a memory system, it has been common practice to place multiple devices on a common bus. For example, two fast page mode DRAMs may be connected to common address and data buses. One DRAM stores data for odd addresses, and the other for even addresses. The /CAS signal for the odd addresses is turned off (high) when the /CAS signal for the even addresses is turned on (low). This interleaved memory system provides data access at twice the rate of either device alone.

If the first /CAS is low for 20 nanoseconds and then high for 20 nanoseconds while the second /CAS goes low, data can be accessed every 20 nanoseconds or 50 megahertz. If the access time from /CAS to data valid is fifteen nanoseconds, the data will be valid for only five nanoseconds at the end of each 20 nanosecond period when both devices are operating in fast page mode. As cycle times are shortened, the data valid period goes to zero.

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead, data is held valid after /CAS goes high until sometime after the next /CAS low pulse occurs, or until /RAS or the output enable (/OE) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can be a complex function of when the column address inputs are valid, when /CAS falls, the state of /OE and when /CAS rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially /CAS) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM manufacturers.

Methods to shorten memory access cycles tend to require additional circuitry, additional control pins and nonstandard device pinouts. The proposed industry standard synchronous DRAM (SDRAM) for example has an additional pin for receiving a system clock signal. Since the system clock is connected to each device in a memory system, it is highly loaded, and it is always toggling circuitry in every device. SDRAMs also have a clock enable pin, a chip select pin and a data mask pin. Other signals which appear to be similar in name to those found on standard DRAMs have dramatically different functionality on a SDRAM. The addition of several control pins has required a deviation in device pinout from standard DRAMs which further complicates design efforts to utilize these new devices. Significant amounts of additional circuitry are required in the SDRAM devices which in turn result in higher device manufacturing costs.

In order for existing computer systems to use an improved device having a nonstandard pinout, those systems must be extensively modified. Additionally, existing computer system memory architectures are designed such that control and address signals may not be able to switch at the frequencies required to operate the new memory device at high speed due to large capacitive loads on the signal lines. The Single In-Line Memory Module (SIMM) provides an example of what has become an industry standard form of packaging memory in a computer system. On a SIMM, all address lines connect to all DRAMs. Further, the row address strobe (/RAS) and the write enable (/WE) are often connected to each DRAM on the SIMM. These lines inherently have high capacitive loads as a result of the number of device inputs driven by them. SIMM devices also typically ground the output enable (/OE) pin making /OE a less attractive candidate for providing extended functionality to the memory devices.

There is a great degree of resistance to any proposed deviations from the standard SIMM design due to the vast number of computers which use SIMMs. Industry's resistance to radical deviations from the standard, and the inability of current systems to accommodate the new memory devices will delay their widespread acceptance. Therefore only limited quantities of devices with radically different architectures will be manufactured initially. This limited manufacture prevents the reduction in cost which typically can be accomplished through the manufacturing improvements and efficiencies associated with a high volume product.

SUMMARY OF THE INVENTION

An integrated circuit memory device with a standard DRAM pinout is designed for high speed data access and for compatibility with existing memory systems. A high speed burst mode of operation is provided where multiple sequential accesses occur following a single column address, and read data is output relative to the /CAS control signal. In the burst mode of operation the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at high speeds. Only one control line per memory chip (/CAS) must toggle at the operating frequency in order to clock the internal address counter and the data input/output latches. The load on each /CAS is typically less than the load on the other control signals (/RAS, /WE and /OE) since each /CAS typically controls only a byte width of the data bus. Internal circuitry of the memory device is largely compatible with existing Extended Data Out (EDO) DRAMs. This similarity allows the two part types to be manufactured on one die with a limited amount of additional circuitry. The ability to switch between a standard non-burst mode and a high speed burst mode allows the device to be used to replace standard devices, and eliminates the need to switch to more complex high speed memory devices. Internal address generation provides for faster data access times than is possible with either fast page mode or EDO DRAMs. This high speed operation eliminates the need to interleave memory devices in order to attain a high data throughput. In contrast to the 50 megahertz interleaved memory system described above, the output data from this device will be valid for approximately 15 nanoseconds significantly easing the design of circuitry required to latch the data from the memory. The device is compatible with existing memory module pinouts including Single In-Line Memory Module (SIMM), Multi-Chip Module (MCM) and Dual In-Line Memory Module (DIMM) designs. This combination of features allows for significant system performance improvements with a minimum of design alterations.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention as well as objects and advantages will be best understood by reference to the appended claims, detailed description of particular embodiments and accompanying drawings where:

FIG. 1 is an electrical schematic diagram of a memory device in accordance with one embodiment of the invention;

FIG. 2 is a table showing linear versus interleaved addressing formats;

FIG. 3 is a pinout of the memory device of FIG. 1;

FIG. 4 is a timing diagram for a method of accessing the device of FIG. 1;

FIG. 5 is a further timing diagram for accessing the device of FIG. 1;

FIG. 6 is an electrical schematic diagram of a Single In-Line Memory Module in accordance with another embodiment of the invention;

FIG. 7 is a front view of a Single In-Line Memory Module designed in accordance with the teachings of this invention;

FIG. 8 is a table of the pin numbers and signal names of the Single In-Line Memory Module of FIG. 7; and

FIG. 9 is a block diagram of a computer system in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a schematic representation of a sixteen megabit device designed in accordance with the present invention. The device is organized as a 2 Meg×8 burst EDO DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array 12. The device of FIG. 1 has an industry standard pinout for eight bit wide EDO DRAMs. An active-low row address strobe (/RAS) signal 14 is used to latch a first portion of a multiplexed memory address, from address inputs A0 through A10 16, in latch 18. The latched row address 20 is decoded in row decoder 22. The decoded row address is used to select a row of the memory array 12. A column address strobe (/CAS) signal 24 is used to latch a second portion of a memory address from address inputs 16 into column address counter 26. The latched column address 28 is decoded in column address decoder 30. The decoded column address is used to select a column of the memory array 12.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 32 to output latches 34. Data 10 driven from the burst EDO DRAM may be latched external to the device in synchronization with /CAS after a predetermined number of /CAS cycle delays (latency). For a two cycle latency design, the first /CAS falling edge is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second /CAS falling edge, and remains valid through the third /CAS falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during /CAS high intervals dependent on the state of the output enable and write enable (/OE and /WE) control lines, thus allowing additional time for the system to latch the output data. Once a row and a column address are selected, additional transitions of the /CAS signal are used to advance the column address within the column address counter in a predetermined sequence. The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the /CAS signal provided that /OE is maintained low, and /WE remains high. The output data signal levels may be driven in accordance with standard CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. FIG. 2 is a table which shows linear and interleaved addressing sequences for burst lengths of 2,4 and 8 cycles. The "V" for starting addresses A1 and A2 in the table represent address values that remain unaltered through the burst sequence. The column address may be advanced with each /CAS transition, each pulse, or multiple of /CAS pulses in the event that more than one data word is read from the array with each column address. When the address is advanced with each transition of the /CAS signal, data is also driven from the part after each transition following the device latency which is then referenced to each edge of the /CAS signal. This allows for a burst access cycle where the highest switching control line (/CAS) toggles only once (high to low or low to high) for each memory cycle. This is in contrast to standard DRAMs which require /CAS to go low and then high for each cycle, and synchronous DRAMs which require a full clock cycle (high

and low transitions) for each memory cycle. For maximum compatibility with existing EDO DRAM devices, the invention will be further described in reference to a device designed to latch and advance a column address on falling edges of the /CAS signal.

It may be desirable to latch and increment the column address after the first /CAS falling edge in order to apply both the latched and incremented addresses to the array at the earliest opportunity in an access cycle. For example, a device may be designed to access two data words per cycle (prefetch architecture). The memory array for a prefetch architecture device may be split into odd and even array halves. The column address least significant bit is then used to select between odd and even halves while the other column address bits select a column within each of the array halves. In an interleaved access mode with column address 1, data from columns 0 and 1 would be read and the data from column 1 would be output followed by the data from column 0 in accordance with standard interleaved addressing as described in SDRAM specifications. In a linear access mode column address 1 would be applied to the odd array half, and incremented to address 2 for accessing the even array half to fulfill the two word access. One method of implementing this type of device architecture is to provide a column address incrementing circuit between the column address counter and the even array half. The incrementing circuit would increment the column address only if the initial column address in a burst access cycle is odd, and the address mode is linear. Otherwise the incrementing circuit would pass the column address unaltered. For a design using a prefetch of two data accesses per cycle, the column address would be advanced once for every two active edges of the /CAS signal. Prefetch architectures where more than two data words are accessed are also possible.

Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access may require more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory will approach one access per cycle, but the data out of the memory may be offset by a number of cycles due to the pipeline length and/or the desired latency from /CAS.

In the burst access memory device, each new column address from the column address counter is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16. This burst sequence of data will continue for each /CAS falling edge until a predetermined number of data accesses equal to the burst length has occurred. A /CAS falling edge received after the last burst address has been generated will latch another column address from the address inputs 16 and a new burst sequence will begin. Read data is latched and output with each falling edge of /CAS after the first /CAS latency.

For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the /CAS signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is preferred. Additional input data words for storage at incremented column address locations are latched by /CAS on successive /CAS pulses. Input data from the input latches 34 is passed along data path 32 to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes will occur without the requirement of additional column addresses being provided on the address lines 16. After the predetermined number of burst writes has occurred, a subsequent /CAS pulse will latch a new beginning column address, and another burst read or write access will begin.

The memory device of FIG. 1 may include the option of switching between burst EDO and standard EDO modes of operation. In this case, the write enable signal /WE 36 may be used at the row address latch time (/RAS falling, /CAS high) to determine whether memory accesses for that row will be burst or page mode cycles. If /WE is low when /RAS falls, burst access cycles are selected. If /WE is high at /RAS falling, standard extended data out (EDO) page mode cycles are selected. Both the burst and EDO page mode cycles allow for increased memory device operating frequencies by not requiring the data output drivers 34 to place the data lines 10 in a high impedance state between data read cycles while /RAS is low. DRAM control circuitry 38, in addition to performing standard DRAM control functions, controls the I/O circuitry 34 and the column address counter/latch 26 in accordance with the mode selected by /WE when /RAS falls. In a burst mode only DRAM, or in a device designed with an alternate method of switching between burst and non-burst access cycles, the state of /WE when /RAS falls may be used to switch between other possible modes of operation such as interleaved versus linear addressing modes.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by /CAS. /WE low at the column address latch time selects a burst write access. /WE high at the column address latch time selects a burst read access. The level of the /WE signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on /WE within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. Transitions of the /WE signal may be locked out during critical timing periods within an access cycle order to reduce the possibility of triggering a false write cycle. After the critical timing period the state of /WE will determine whether a burst access continues, is initiated, or is terminated. Termination of a burst access resets the burst length counter and places the DRAM in a state to receive another burst access command. Both /RAS and /CAS going high during a burst access will also terminate the burst access cycle placing the data drivers in a high impedance output state, and resetting the burst length counter. Read data may remain valid at the device outputs if /RAS alone goes high while /CAS is active for compatibility with hidden refresh cycles, otherwise /RAS high alone may be used to terminate a burst access. A minimum write enable pulse width is only required when it is desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses. In the case of burst reads, /WE will transition from high to low to terminate a first burst read, and then /WE will transition back high prior to the next falling edge of /CAS in order to specify a new burst read cycle. For burst writes, /WE would transition high to terminate a current burst write access, then back low prior to the next falling edge of /CAS to initiate another burst write access.

A basic implementation of the device of FIG. 1 may include a fixed burst length of 4, a fixed /CAS latency of 2 and a fixed interleaved sequence of burst addresses. This

basic implementation requires very little additional circuitry to the standard EDO page mode DRAM, and may be mass produced to provide the functions of both the standard EDO page mode and burst EDO DRAMs. This device also allows for the output enable pin (/OE) to be grounded for compatibility with many SIMM module designs. When not disabled (tied to ground), /OE is an asynchronous control which will prevent data from being driven from the part in a read cycle if it is inactive (high) prior to /CAS falling and remains inactive beyond /CAS rising. If these setup and hold conditions are not met, then the read data may be driven for a portion of the read cycle. It is possible to synchronize the /OE signal with /CAS, however this would typically increase the /CAS to data valid delay time and doesn't allow for the read data to be disabled prior to /RAS high without an additional /CAS low pulse which would otherwise be unnecessary. In a preferred embodiment, if /OE transitions high at any time during a read cycle the outputs will remain in a high impedance state until the next falling edge of /CAS despite further transitions of the /OE signal.

Programmability of the burst length, /CAS latency and address sequences may be accomplished through the use of a mode register 40 which latches the state of one or more of the address input signals 16 or data signals 10 upon receipt of a write-/CAS-before-/RAS (WCBR) programming cycle. In such a device, outputs 44 from the mode register control the required circuits on the DRAM. Burst length options of 2, 4, 8 and full page as well as /CAS latencies of 1, 2 and 3 may be provided. Other burst length and latency options may be provided as the operating speeds of the device increase, and computer architectures evolve. The device of FIG. 1 includes programmability of the address sequence by latching the state of the least significant address bit during a WCBR cycle. The burst length and /CAS latency for this particular embodiment are fixed. Other possible alterations in the feature sets of this DRAM include having a fixed burst mode only, selecting between standard fast page mode (non-EDO) and burst mode, and using the output enable pin (/OE) 42 in combination with /RAS to select between modes of operation. Also, a WCBR refresh cycle could be used to select the mode of operation rather than a control signal in combination with /RAS. A more complex memory device may provide additional modes of operation such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of /WE and /OE at /RAS falling time. One mode from a similar set of modes may be selected through the use of a WCBR cycle using multiple address or data lines to encode the desired mode. Alternately, a device with multiple modes of operation may have wire bond locations, or programmable fuses which may be used to program the mode of operation of the device.

A preferred embodiment of a sixteen bit wide burst EDO mode DRAM designed in accordance with the teachings of this invention has two column address strobe input pins /CASH and /CASL. For read cycles only /CASL needs to toggle. /CASH is may be high or may toggle with /CASL during burst read cycles, all sixteen data bits will be driven out of part during a read cycle even if /CASH remains inactive. In a typical system application, a microprocessor will read all data bits on a data bus in each read cycle, but may only write certain bytes of data in a write cycle. Allowing one of the /CAS control signals to remain static during read cycles helps to reduce overall power consumption and noise within the system. For burst write access cycles, each of the /CAS signals (CASH and /CASL) acts as a write enable for an eight bit width of the data. All sixteen data inputs will be latched when the first of the /CAS signals transitions low. If only one /CAS signal transitions low, then the eight bits of data associated with the /CAS that remained high will not be stored in the memory.

The present invention has been described with reference to several preferred embodiments. Just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including x1, x4, x8 and x16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the memory device of the present invention may take the form of many different memory organizations. It is believed that one who is skilled in the art of integrated circuit memory design can, with the aide of this specification design a variety of memory devices which do not depart from the spirit of this invention. It is therefore believed that detailed descriptions of the various memory device organizations applicable to this invention are not necessary.

FIG. 3 shows a preferred pinout for the device of FIG. 1. It should be noted that the pinout for this new burst EDO memory device is identical to the pinout for a standard EDO DRAM. The common pinout allows this new device to be used in existing memory designs with minimum design changes. The common pinout also allows for ease of new designs by those of skill in the art who are familiar with the standard EDO DRAM pinout. Variations of the described invention which maintain the standard EDO DRAM pinout include driving the /CAS pin with a system clock signal to synchronize data access of the memory device with the system clock. For this embodiment, it may be desirable to use the first /CAS active edge after /RAS falls to latch the row address, a later edge may be used to latch the first column address of a burst access cycle. After row and column addresses are latched within the device, the address may be incremented internally to provide burst access cycles in synchronization with the system clock. Other pin function alternatives include driving the burst address incrementing signal on the /OE pin since the part does not require a data output disable function on this pin. Other alternate uses of the /OE pin also allow the device to maintain the standard EDO pinout, but provide increased functionality such as burst mode access. The /OE pin may be used to signal the presence of a valid column starting address, or to terminate a burst access. Each of these embodiments provides for a high speed burst access memory device which may be used in current memory systems with a minimum amount of redesign.

FIG. 4 is a timing diagram for performing a burst read followed by a burst write of the device of FIG. 1. In FIG. 4, a row address is latched by the /RAS signal. /WE is low when /RAS falls for an embodiment of the design where the state of the /WE pin is used to specify a burst access cycle at /RAS time. Next, /CAS is driven low with /WE high to initiate a burst read access, and the column address is latched. The data out signals (DQ's) are not driven in the first /CAS cycle. On the second falling edge of the /CAS signal, the internal address generation circuitry advances the column address and begins another access of the array, and the first data out is driven from the device after a /CAS to data access time (tCAC). Additional burst access cycles continue, for a device with a specified burst length of four, until the fifth falling edge of /CAS which latches a new column address for a new burst read access. /WE falling in the fifth /CAS cycle terminates the burst access, and initializes the device for additional burst accesses. The sixth falling edge of /CAS with /WE low is used to latch a new burst address, latch input data and begin a burst write access of the device. Additional data values are latched on succes-

sive /CAS falling edges until /RAS rises to terminate the burst access.

FIG. 5 is a timing diagram depicting burst write access cycles followed by burst read cycles. As in FIG. 4, the /RAS signal is used to latch the row address. The first /CAS falling edge in combination with /WE low begins a burst write access with the first data being latched. Additional data values are latched with successive /CAS falling edges, and the memory address is advanced internal to the device in either an interleaved or sequential manner. On the fifth /CAS falling edge a new column address and associated write data are latched. The burst write access cycles continue until the /WE signal goes high in the sixth /CAS cycle. The transition of the /WE signal terminates the burst write access. The seventh /CAS low transition latches a new column address and begins a burst read access (/WE is high). The burst read continues until /RAS rises terminating the burst cycles.

It should be noted from FIGS. 3 and 4, that for burst read cycles the data remains valid on the device outputs as long as the /OE pin is low, except for brief periods of data transition. Also, since the /WE pin is low prior to or when /CAS falls, the data input/output lines are not driven from the part during write cycles, and the /OE pin is a "don't care". Only the /CAS signal and the data signals toggle at relatively high frequency, and no control signals other than /CAS are required to be in an active or inactive state for one /CAS cycle time or less. This is in contrast to SDRAMs which often require row address strobes, column address strobes, data mask, and read/write control signals to be valid for one clock cycle or less for various device functions. Typical DRAMs also allow for the column address to propagate through to the array to begin a data access prior to /CAS falling. This is done to provide fast data access from /CAS falling if the address has been valid for a sufficient period of time prior to /CAS falling for the data to have been accessed from the array. In these designs an address transition detection circuit is used to restart the memory access if the column address changes prior to /CAS falling. This method actually requires additional time for performing a memory access since it must allow for a period of time at the beginning of each memory cycle after the last address transition to prepare for a new column address. Changes in the column address just prior to /CAS falling may increase the access time by approximately five nanoseconds. An embodiment of the present invention will not allow the column address to propagate through to the array until after /CAS has fallen. This eliminates the need for address transition detection circuitry, and allows for a fixed array access relative to /CAS.

FIG. 6 is a schematic representation of a single in-line memory module (SIMM) designed in accordance with the present invention. The SIMM has a standard SIMM module pinout for physical compatibility with existing systems and sockets. Functional compatibility with EDO page mode SIMMs is maintained when each of the 2 Meg×8 memory devices 10, 12, 14 and 16 are operated in an EDO page mode. Each of the /CAS signals 18, 20, 22 and 24 control one byte width of the 32 bit data bus 26, 28, 30 and 32. A /RAS 34 signal is used to latch a row address in each of the memory devices, and is used in combination with /WE 36 to select between page mode and burst mode access cycles. Address signals 38 provide a multiplexed row and column address to each memory device on the SIMM. In burst mode, only active /CAS control lines are required to toggle at the operating frequency of the device, or at half the frequency if each edge of the /CAS signal is used as described above. The data lines are required to be switchable at half of the frequency of the /CAS lines or at the same frequency, and the other control and address signals switch at lower frequencies than /CAS and the data lines. As shown in FIG. 6, each /CAS signal and each data line is connected to a single memory device allowing for higher frequency switching than the other control and address signals. Each of the memory devices 10, 12, 14 and 16 is designed in accordance with the present invention allowing for a burst mode of operation providing internal address generation for sequential or interleaved data access from multiple memory address locations with timing relative to the /CAS control lines after a first row and column address are latched.

FIG. 7 shows a front view of another SIMM designed in accordance with the present invention. Each device on the SIMM is a 4 Megabit DRAM organized as 1 Meg×4. In this configuration, a single /CAS controls two memory devices to provide access to a byte width of the data bus. The eight devices shown form a 4 Megabyte SIMM in a 32 bit width. For an 8 Megabyte SIMM in a 32 bit width, there are eight additional devices on the back side (not shown).

FIG. 8 shows a preferred pinout for a memory module designed in accordance with the device of FIG. 7. This pinout is compatible with pinouts for Fast Page Mode SIMMs and EDO SIMMs. A presence detect pin is provided for indication of EDO operation on pin 66, and in accordance with standard EDO part types, an /OE input is provided on pin 46.

Alternate embodiments of the SIMM modules of FIGS. 5, 6 and 7 include the use of two /RAS signals with each controlling a sixteen bit width of the data bus in accordance with standard SIMM module pinouts. Four more 2M×8 EDO Burst Mode DRAMs may be added to the device of FIG. 6 to provide for a 4M×32 bit SIMM. Sixteen bit wide DRAMs may also be used, these will typically have two /CAS signals each of which controls an eight bit data width. The incorporation of parity bits, or error detection and correction circuitry provide other possible SIMM module configurations. Methods of performing error detection and/or correction are well known to those of skill in the art, and detailed descriptions of such circuits are not provided in this application. Additional SIMM designs using the novel memory device of the present invention may be designed by one of skill in the art with the aid of this specification. The invention has been described with reference to SIMM designs, but is not limited to SIMMs. The invention is equally applicable to other types of memory modules including Dual In-Line Memory Modules (DIMMs) and Multi-Chip Modules (MCMs).

FIG. 9 is a block diagram of a computer system 10 in accordance with the present invention. In a preferred embodiment of the present invention, microprocessor 20 is coupled to Burst EDO memory 40 through address, data and control signals 50. A system clock circuit 30 provides a system clock to the microprocessor. The memory 40 is responsive to the microprocessor to perform burst mode read and write access cycles.

What is claimed is:

1. A memory device having a plurality of memory elements, each of the elements having an associated address, the memory device further comprising:

addressing circuitry adapted to receive at least a first portion of an address from a source external to the memory device in response to a transition of an address strobe signal, and further adapted to advance the address in a predetermined address sequence in response to a subsequent transition of the address strobe signal; and

output buffer circuitry adapted to drive data from the memory device only after a plurality of transitions of the address strobe signal in a burst read access.

2. The memory device of claim 1, wherein:

said output buffer circuitry is further adapted to switch between a logic low data value and a logic high data value in response to a single transition of the address strobe signal.

3. The memory device of claim 1, wherein:

said output buffer circuitry is further adapted to drive a logic low data value from the device after a falling edge of the address strobe signal, and then to drive a logic high data value from the device after a rising edge of the address strobe signal.

4. A memory device having a plurality of memory elements, each of the elements having an associated address, the memory device further comprising:

addressing circuitry adapted to provide a series of addresses in a burst mode of operation; and

a write enable signal node for receiving a write enable signal which is adapted to select between read and write cycles of the memory device, wherein a burst access of the memory device is terminated in response to a transition of the write enable signal.

5. A memory device having an address latch node for receiving an address strobe signal, an address latch for receiving at least a portion of a first memory address and an array of memory elements, the memory device comprising:

an address generating circuit responsive to the address strobe signal and to an output of the address latch for generating a second memory address, wherein the second memory address is used to access the array; and

an output circuit in electrical communication with the address latch node for driving data received from the array, out of the memory device after a plurality of transitions of the address strobe signal.

6. The memory device of claim 5, wherein:

said output circuit is adapted to drive data out of the memory device after a programmable number of transitions of the address strobe signal.

7. The memory device of claim 5, further comprising:

an output enable signal node for receiving an output enable signal for enabling data to be driven from the memory device; and

means for performing burst read and burst write access cycles while said output enable signal node is connected to a supply potential node which defines a state of the output enable signal for enabling data to be driven.

8. The memory device of claim 5, wherein said address latch receives a column portion of the first address, the memory device further comprising:

a row address strobe signal node for receiving a row address strobe signal;

a row address latch coupled to said row address strobe signal node for latching a row address in response to the row address strobe signal;

a control signal node for receiving a control signal; and

a mode control latch in electrical communication with said control signal node and said row address strobe signal node, for latching a state of the control signal upon a transition of the row address strobe signal, wherein the state is used to select between a burst mode and a nonburst mode of the memory device.

9. The memory device of claim 8 wherein:

said control signal node is a write cycle enable signal node.

10. The memory device of claim 5, wherein:

said address generating circuit latches a first column address in response to a first transition of the address strobe signal, and advances the first column address to generate a second column address in response to a second transition of the address strobe signal.

11. The memory device of claim 5, wherein:

said address latch comprises a transparent latch.

12. A memory device having an address strobe signal node for receiving an address strobe signal and an array of memory elements, the memory device comprising:

an address latch responsive to a first transition of the address strobe signal to latch at least a portion of a first initial memory address into the memory device;

an address generating circuit adapted to generate a series of burst addresses which are determinable from the first initial memory address, wherein each of the burst addresses is generated in response to a corresponding transition of the address strobe signal; and

a control circuit in electrical communication with said address latch and the address strobe signal node for enabling said address latch to latch at least a portion of a second initial address into the memory device in response to the address strobe signal after a predetermined number of burst access cycles have occurred.

13. The memory device of claim 12, wherein:

the predetermined number of burst access cycles is a programmable number.

14. The memory device of claim 12, further comprising:

a write enable signal node for receiving a write enable signal, wherein a burst access of the memory device is interrupted in response to a transition of the write enable signal.

15. A memory device having a plurality of data nodes for receiving and driving a plurality of data signals, an array of memory elements, and a plurality of address nodes for receiving a row and a column address, the memory device comprising:

a row address strobe node for receiving a row address strobe signal for latching the row address in the memory device;

a write control signal node for receiving a write control signal for selecting between read and write accesses of the memory device; and

first and second column address strobe nodes for receiving first and second column address strobe signals, wherein either of said first and second column address strobe signals latch the column address, and either of said first and second column address strobe signals being active during a read access of the memory device will enable data to be driven on each of the data nodes, and only a first plurality of the data signals will be stored in the array in response to said write control signal selecting a write access and said first column address strobe node being active and said second column address strobe node being inactive.

16. A memory device having an array of memory elements, in which a row address has been selected, comprising:

a means of selecting a first column address and accessing an element of the array of memory elements at the row and first column address, in response to a transition of a column address strobe signal; and

a means for modifying the first column address within the memory device to provide a second column address and for accessing a further element of the array, in response to the column address strobe signal;

an output buffer to provide output data from the memory device only after a plurality of transitions of the column address strobe signal in a burst read access; and

a control circuit responsive to a write enable signal to terminate a burst access of the memory device.

17. The memory device according to claim 16, further comprising:

a burst mode enable means for enabling a burst mode of operation of the memory device.

18. The memory device according to claim 16, further comprising:

a means for disabling a burst mode of operation of the memory device.

19. The memory device according to claim 18, further comprising:

a mode control latch for latching a mode of operation of the memory device when the row address is selected.

20. The memory device according to claim 16, further comprising:

a row address strobe signal node for receiving a row address strobe signal to select the row address;

a write enable input node for receiving the write enable signal; and

a mode control latch circuit coupled to said write enable input node and at least one of said address signal input nodes for latching a mode of operation of the memory device in response to an active state of the write enable signal when the row address strobe signal is activated subsequent to the column address strobe signal being activated.

21. A memory device having external nodes for receiving a plurality of signals consisting essentially of a column address strobe signal a cycle of which defines an access cycle period, a row address strobe signal, a write enable signal, an output enable signal, address signals, data signals and power supply signals, the memory device comprising:

means for performing a burst write access of a first plurality of memory elements in response to a first address and a first plurality of transitions of the column address strobe signal, and for performing a burst read access of a second plurality of memory elements in response to a second address and a second plurality of transitions of the column address strobe signal, wherein a transition of the write enable signal will terminate a burst access of the memory device.

22. The memory device according to claim 21, further comprising:

a data output circuit for driving data from the memory device in the burst read access , wherein a first data signal from a third plurality of memory elements is driven from the memory device in a next burst read access subsequent to a last data signal of the second plurality of memory elements being driven from the memory device, providing for a continuous series of burst read memory cycles.

23. A method of reading data from a memory device having an address latch, an address counter, an address strobe node for receiving a column address strobe, an output data driver and an array of memory elements, the method comprising:

applying a first column address strobe to the address strobe node for latching a first column address;

accessing a first memory element of the array of memory elements at the first column address;

applying a second column address strobe to the address strobe node for advancing the column address within the memory device to specify a second column address;

accessing a second memory element of the array of memory elements at the second column address;

switching data driven to an external data node from a logic low level to a logic high level in response to a single transition of the column address strobe; and

maintaining a high impedance state on the output data driver at least until said step of applying the second column address strobe.

24. The method of reading data from a memory device according to claim 23, further comprising:

applying a third column address strobe to the address strobe node for advancing the column address to specify a third column address; and

latching an output of the memory device from the first column address in synchronization with the third column address strobe.

25. The method of reading data from a memory device according to claim 23, further comprising:

selecting a burst mode of operation of the memory device prior to said applying the first column address strobe.

26. A method of terminating a burst access of a memory device having an array of memory elements, an address generation circuit for providing a plurality of addresses for accessing the array, and a read and write cycle input node for receiving a write enable signal, the method comprising:

toggling the write enable signal during the burst access.

27. The method according to claim 26, further comprising:

resetting a burst length counter in response to said toggling the write enable signal during the burst access.

28. A Single In Line Memory Module comprising:

a memory device having an array of memory elements, each of the memory elements having an associated address;

a plurality of address lines coupled to said memory device; and

an address strobe signal line electrically coupled to said memory device, wherein said memory device is responsive to an address strobe signal received on said address strobe signal line to latch an address within said memory device from said plurality of address lines, and said memory device is responsive to a transition of the address strobe signal received on said address strobe signal line to advance the address within said memory device in a predetermined sequence.

29. The Single In Line Memory Module according to claim 28, wherein said memory chip further comprises:

a data node for driving data from the Single In Line Memory Module, wherein driven data is switched from a first data value to a second data value in response to a single transition of the address strobe signal.

30. The Single In Line Memory Module according to claim 29, wherein:

a first transition of the address strobe signal is used to latch a first address within the memory device; and

the first data value from the first address of the memory device is driven from said data node in response to a second transition of the address strobe signal.

31. The Single In Line Memory Module according to claim 28, further comprising:

a means for inhibiting the address strobe signal from advancing the address.

32. The Single In Line Memory Module according to claim 28, further comprising:

a write cycle control line for selecting a write access of said memory chip when a write enable signal on said write cycle control line is active at a time when said address strobe signal line latches the address, and for terminating a burst access of said memory chip.

33. The Single In Line Memory Module according to claim 28, wherein the memory chip further comprises an output enable signal node coupled to a ground potential node of the Single In Line Memory Module.

34. A Memory Module comprising:

a memory device;

a plurality of address signal lines coupled to said memory device to provide an address to said memory device;

an address strobe signal line coupled to said memory device; and

an address generation circuit within said memory device, coupled to said address strobe signal line, for receiving and advancing the address, to provide multiple data accesses of said memory device in synchronization with multiple transitions of an address strobe signal on said address strobe signal line after only one address is received.

35. The Memory Module according to claim 34, further comprising:

a control signal line; and

a write enable signal line used in combination with said address strobe signal line for selecting between read and write data accesses of said memory device, and used in combination with said control signal line for selecting between a synchronous burst access cycle and an asynchronous nonburst access cycle of said memory device.

36. The Memory Module according to claim 34, further comprising:

a write enable signal line for receiving a write enable signal, wherein a transition of said write enable signal on said write enable signal line during a burst access cycle terminates the burst access cycle.

37. The Memory Module according to claim 34, further comprising:

at least one data node for transferring data to and from the memory module, wherein data from the memory module transitions from a first data value to a second data value in response to a single transition of the signal on said address strobe signal line and data is driven from the memory module only after a plurality of transitions of the signal on said address strobe signal line in a burst read access of the memory module.

38. A computer system which is capable of rapid storage and retrieval of data, comprising:

a microprocessor; and

a memory circuit adapted to store and retrieve data in a burst access in response to a memory address received from said microprocessor and in response to an address strobe signal, wherein said memory circuit is adapted to latch the memory address and perform a first memory access in response to a first transition of the address strobe signal within the burst access and is further adapted to generate an additional memory address and perform a memory access cycle in response to each of a plurality of additional transitions of the address strobe signal within a burst access.

39. The computer system of claim 38, wherein data read from the memory address of said memory circuit is provided by said memory circuit to said microprocessor after at least two transitions of the address strobe signal in the burst access.

40. The computer system of claim 39, wherein additional data values from a predetermined sequence of addresses of said memory circuit are provided to said microprocessor in response to additional transitions of the address strobe signal after said microprocessor receives data from the memory address.

41. The computer system of claim 38, wherein said memory circuit comprises dynamic random access memory elements.

42. A computer system comprising:

a microprocessor that provides an address; and

a memory device containing data at a location corresponding to the address, said memory providing burst access in response to the address, wherein burst access comprises:

a plurality of periods, a column address strobe signal being received by said memory each period;

a column address portion, of the address, being received by said memory device only in a first period of the plurality of periods in response to the column address strobe signal; and

the data at the location corresponding to the address is provided at an output of said memory device after at least two periods.

43. The computer system of claim 42, wherein said memory device is attached to a single in line memory module.

44. The computer system of claim 42, wherein the column address strobe signal is provided to said memory device from the computer system in synchronization with a system clock signal.

45. A computer system which is capable of rapid storage and retrieval of data, comprising:

a microprocessor; and

a burst extended data out memory device to store and retrieve data in a burst access in response to a memory address received from said microprocessor and in response to an address strobe signal, whereby said burst extended data out memory device is operative to latch the memory address and perform a first memory access in response to a first transition of the address strobe signal within the burst access and is further operative to generate an additional memory address and perform a memory access cycle in response to each of a plurality of additional transitions of the address strobe signal within the burst access.

46. The computer system of claim 45, wherein the burst access is terminated in response to a transition of a write enable signal received by said burst extended data out memory device.

47. A burst access memory device comprising:

an array of memory elements;

a column addressing circuit coupled to said array of memory elements, responsive to a column address strobe signal to generate a series of column addresses in a burst access of the memory device; wherein the burst access memory device is responsive to a transition of a write cycle control signal to terminate the burst access.

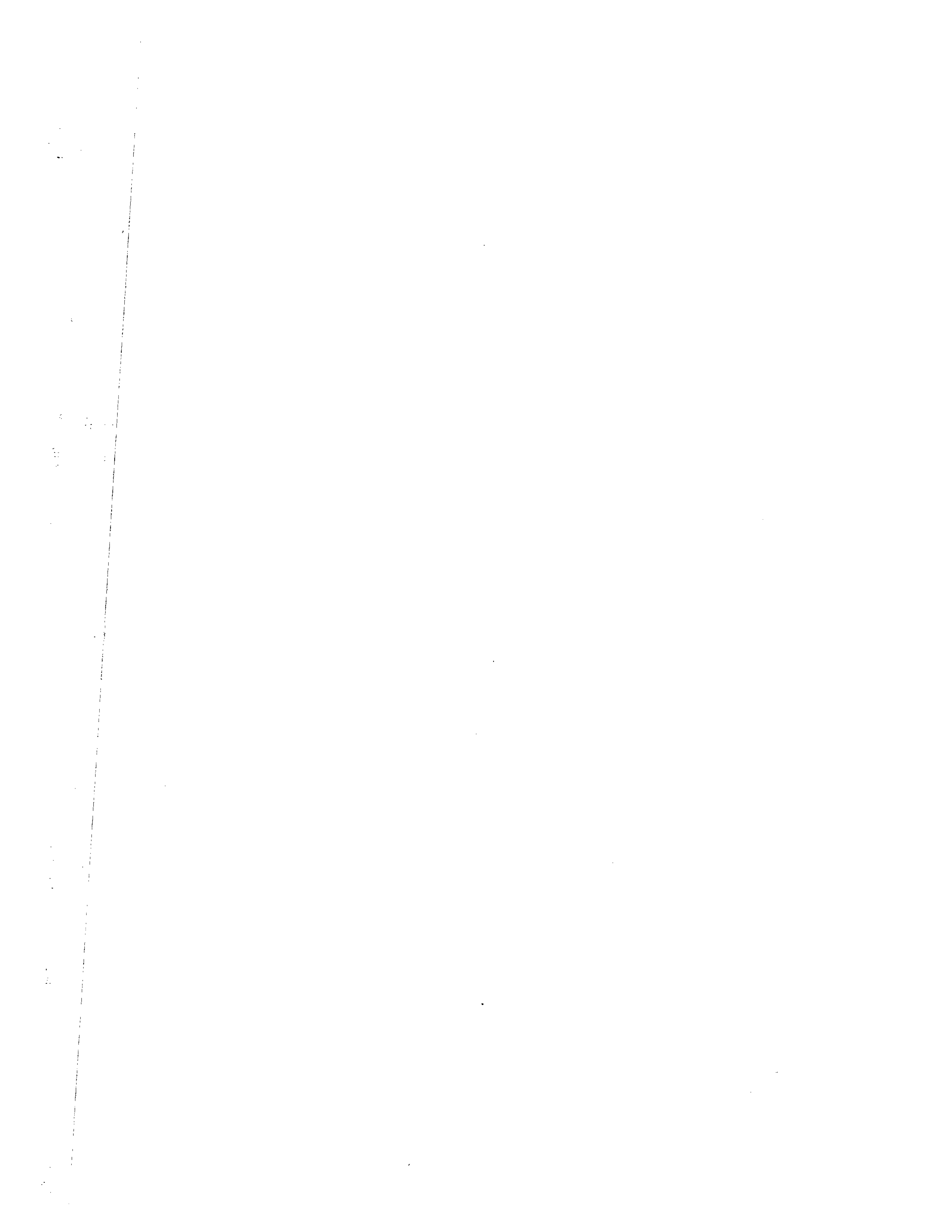
48. The burst access memory device of claim 47, wherein data from said burst access memory device is driven from said burst access memory device only after at least two high to low transitions of the column address strobe signal in a burst read access.

49. The burst access memory device of claim 48, further comprising:

an output enable node adapted to receive an output enable signal; and

a data output node; wherein data from the burst access memory device becomes valid at the data output node within a predetermined period after a high to low transition of the column address strobe signal in the burst read access while the output enable signal is active.

* * * * *



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United States Patent [19]

Merritt et al.

[11] **Patent Number: 5,598,376**

[45] **Date of Patent: Jan. 28, 1997**

[54] **DISTRIBUTED WRITE DATA DRIVERS FOR BURST ACCESS MEMORIES**

[75] Inventors: **Todd A. Merritt; Troy A. Manning,** both of Boise, Id.

[73] Assignee: **Micron Technology, Inc.,** Boise, Id.

[21] Appl. No.: **497,354**

[22] Filed: **Jun. 30, 1995**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 386,894, Feb. 10, 1995, which is a continuation-in-part of Ser. No. 370,761, Dec. 23, 1994.

[51] **Int. Cl.**^{6} **G11C 11/401**

[52] **U.S. Cl.** **365/230.06**; 365/189.05; 365/204; 365/205; 365/233; 365/233.5

[58] **Field of Search** 365/230.01, 189.01, 365/230.06, 189.05, 204, 205, 233.5

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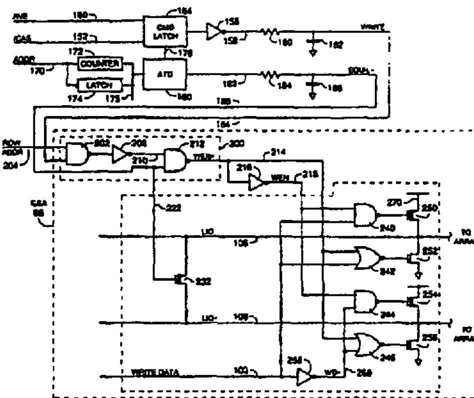
Primary Examiner—Viet Q. Nguyen

Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

An integrated circuit memory device is designed to perform high speed data write cycles. An address strobe signal is used to latch a first address. During a burst access cycle the address is incremented internal to the device with additional address strobe transitions. A new memory address is only required at the beginning of each burst access. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at the device cycle frequency. A transition of the Read/Write control line during a burst access is used to terminate the burst access and initialize the device for another burst access. Write cycle times are maximized to allow for increases in burst mode operating frequencies. Local logic gates near array sense amplifiers are used to control write data drivers to provide for maximum write times without crossing current during input/output line equilibration periods. By gating global write enable signals with global equilibrate signals locally at data sense amp locations, local write cycle control signals are provided which are valid for essentially the entire cycle time minus an I/O line equilibration period in burst access memory devices. For nonburst mode memory devices such as EDO and Fast Page Mode, the write function may begin immediately following the end of the equilibration cycle to provide a maximum write time without interfering with the address setup time of the next access cycle.

19 Claims, 6 Drawing Sheets



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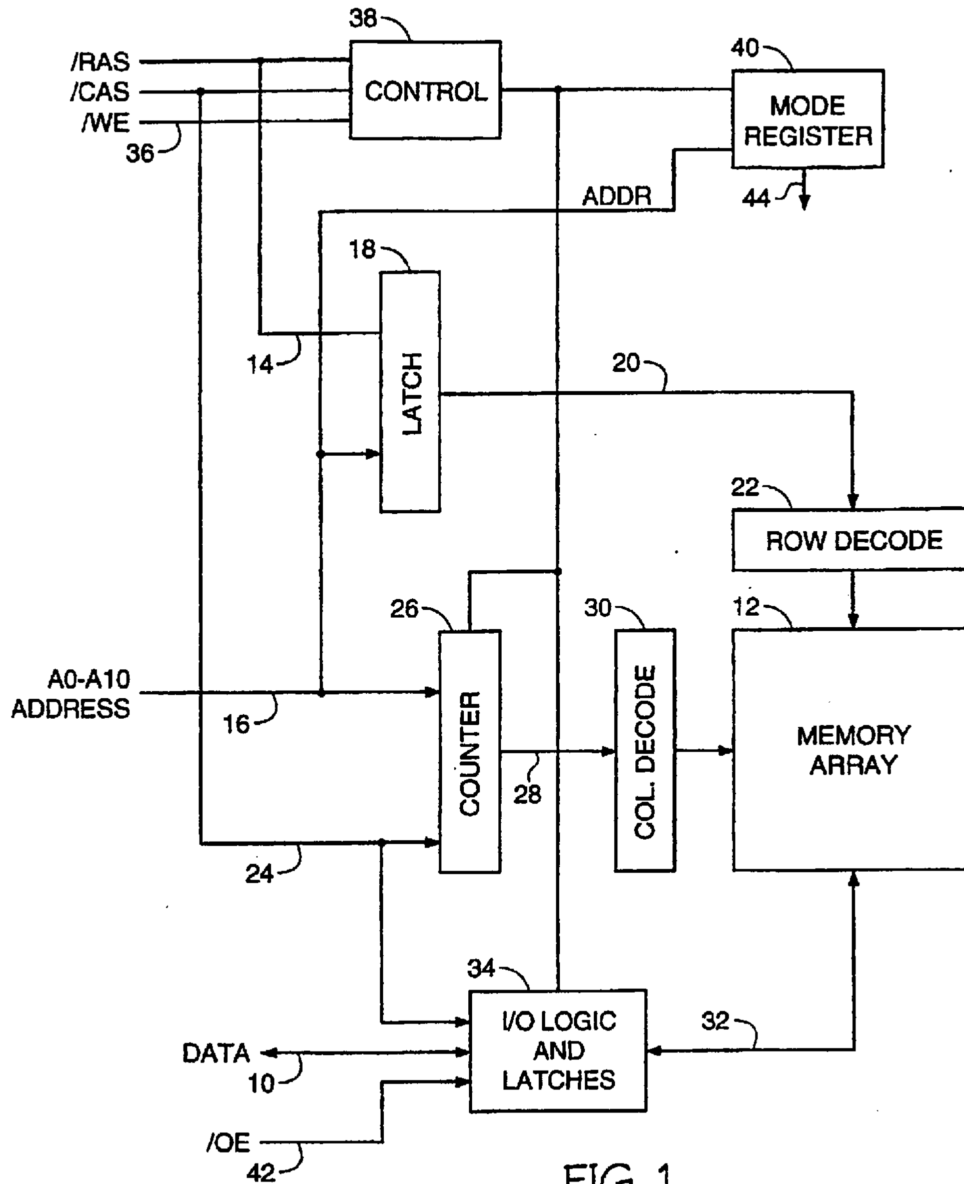

FIG. 1

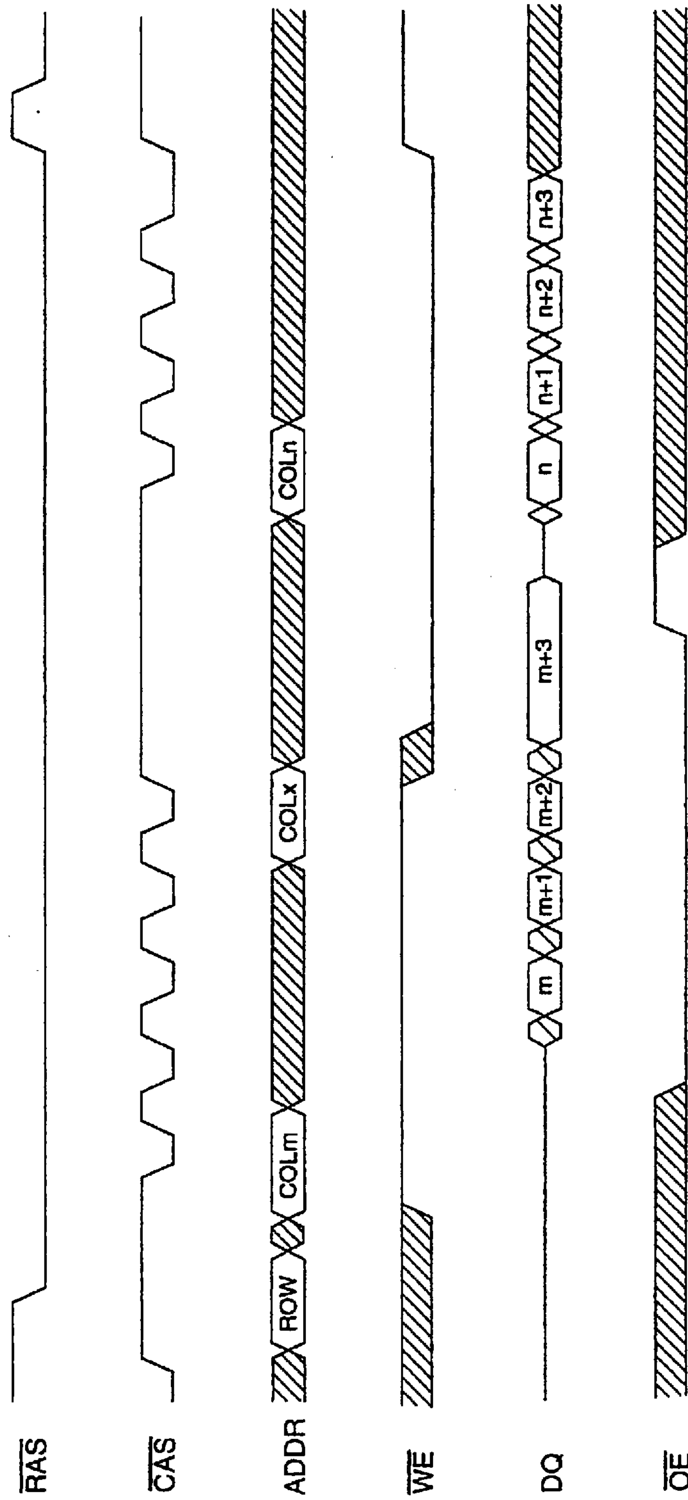

FIG. 2

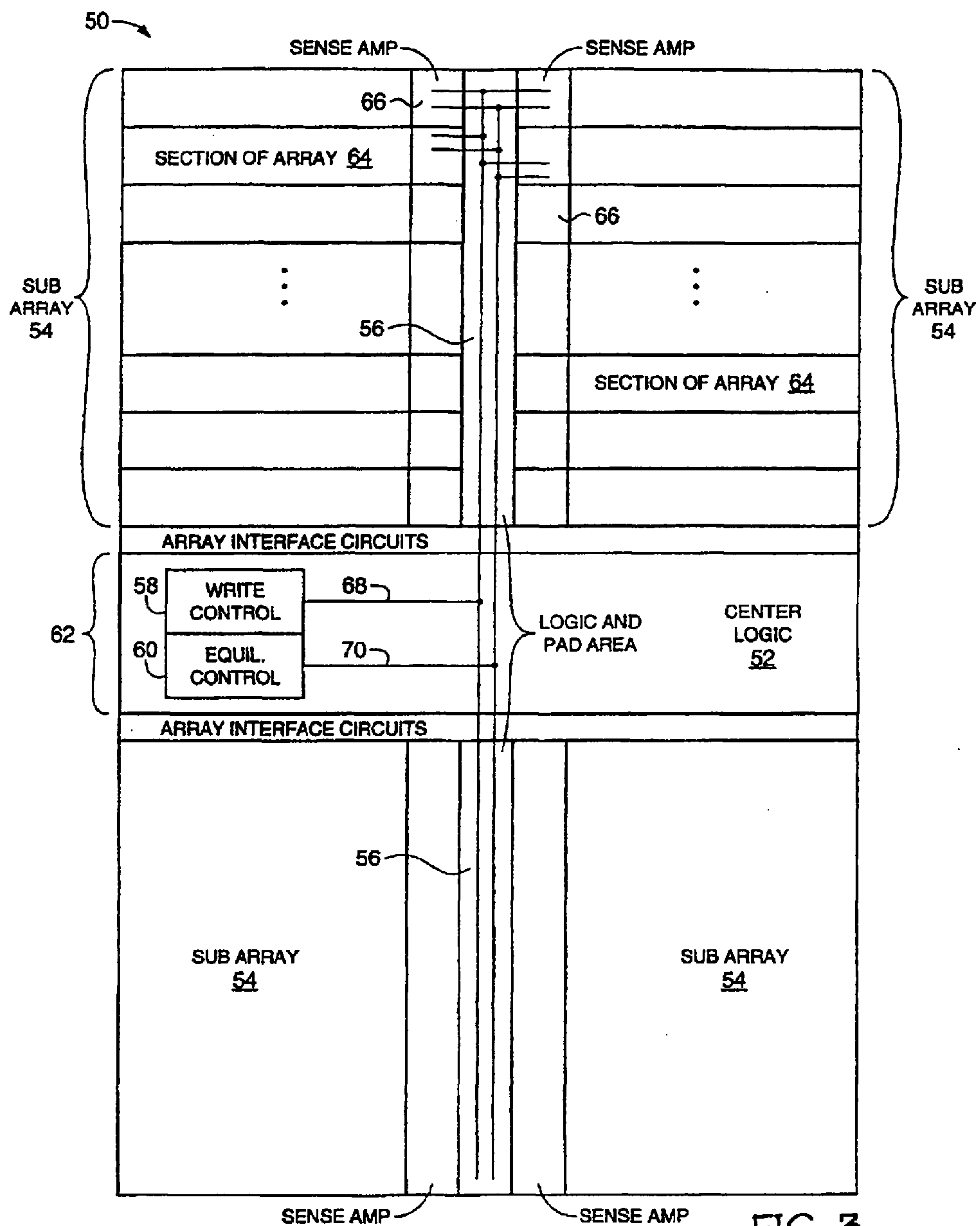

FIG. 3

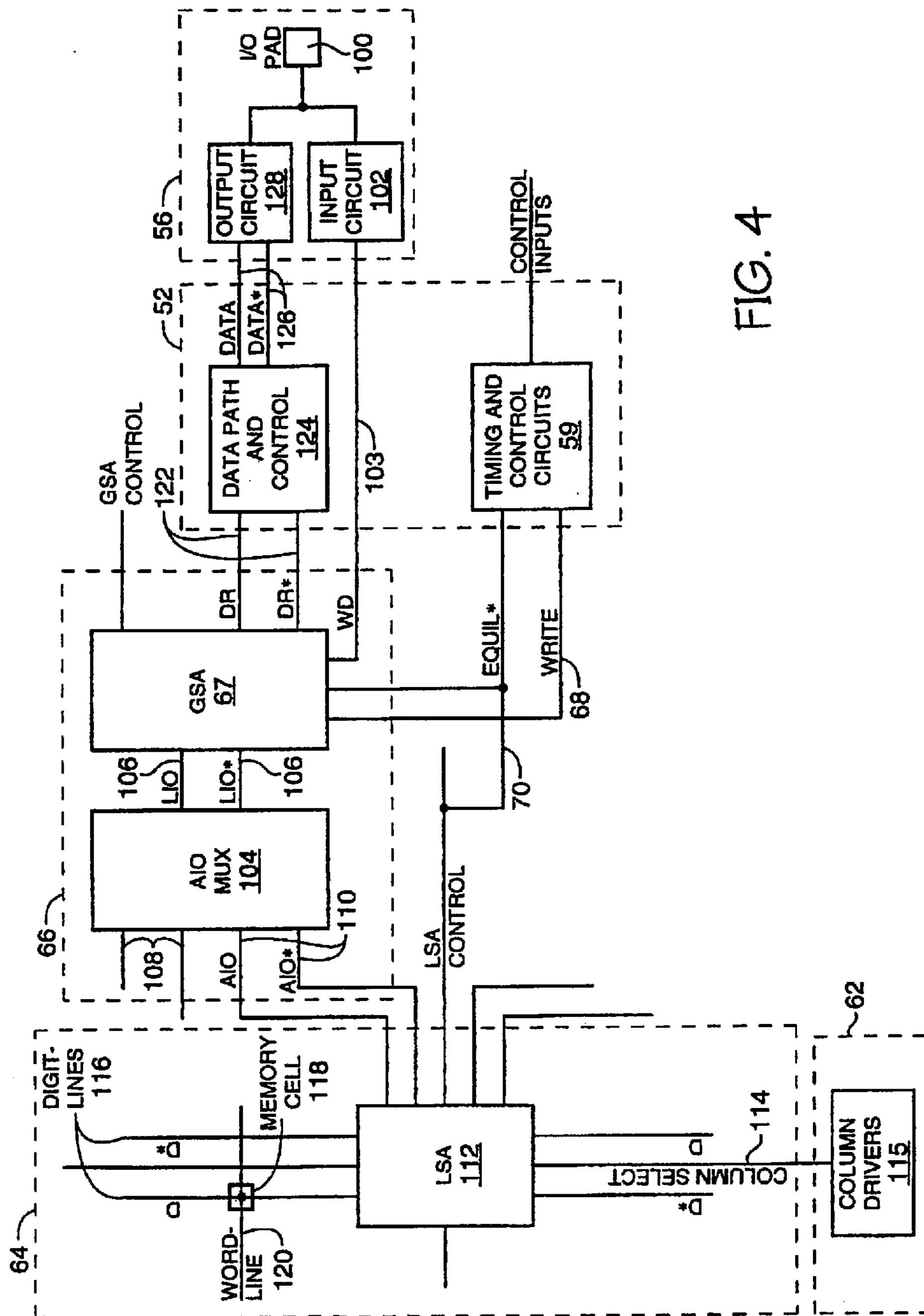

FIG. 4

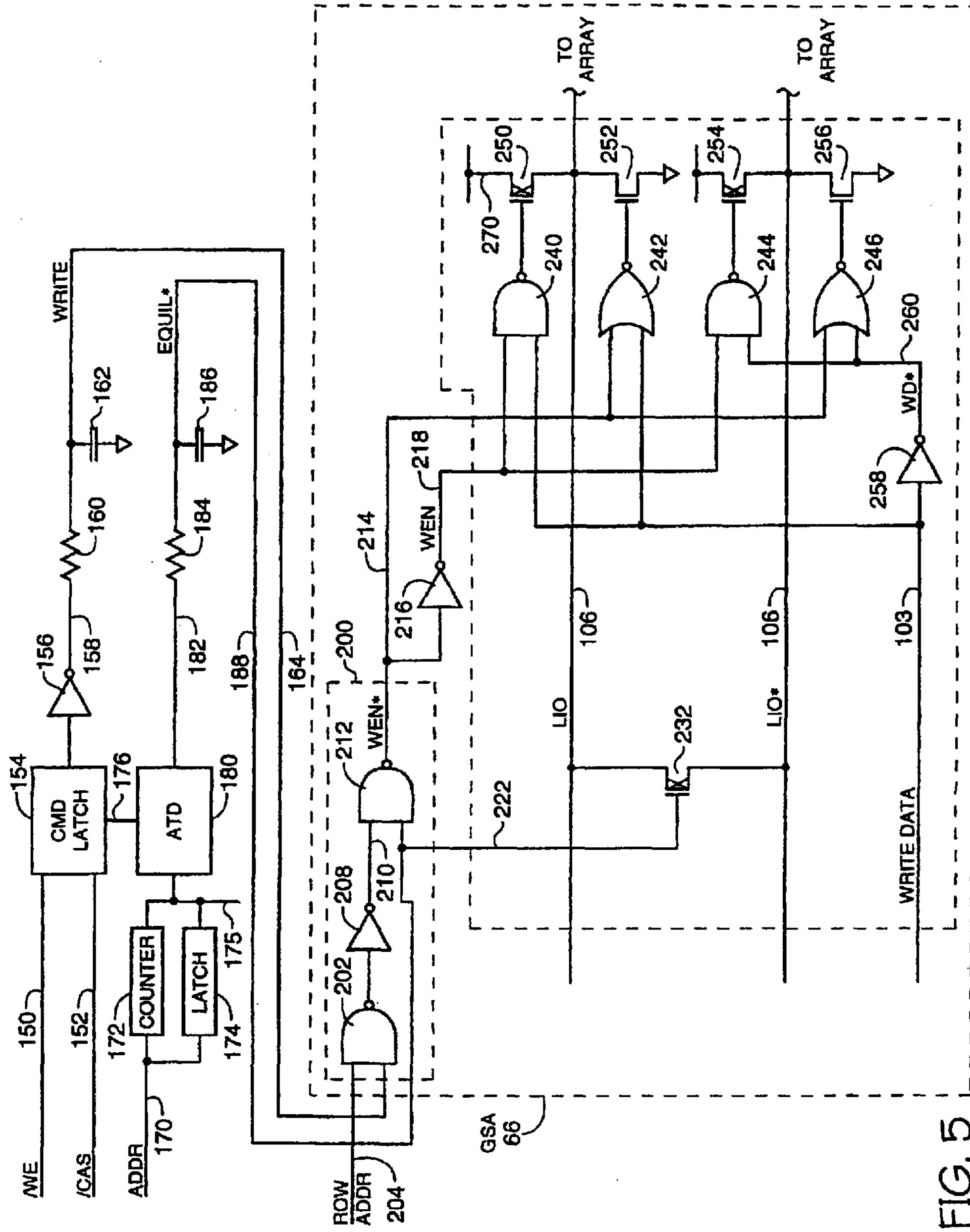

FIG. 5

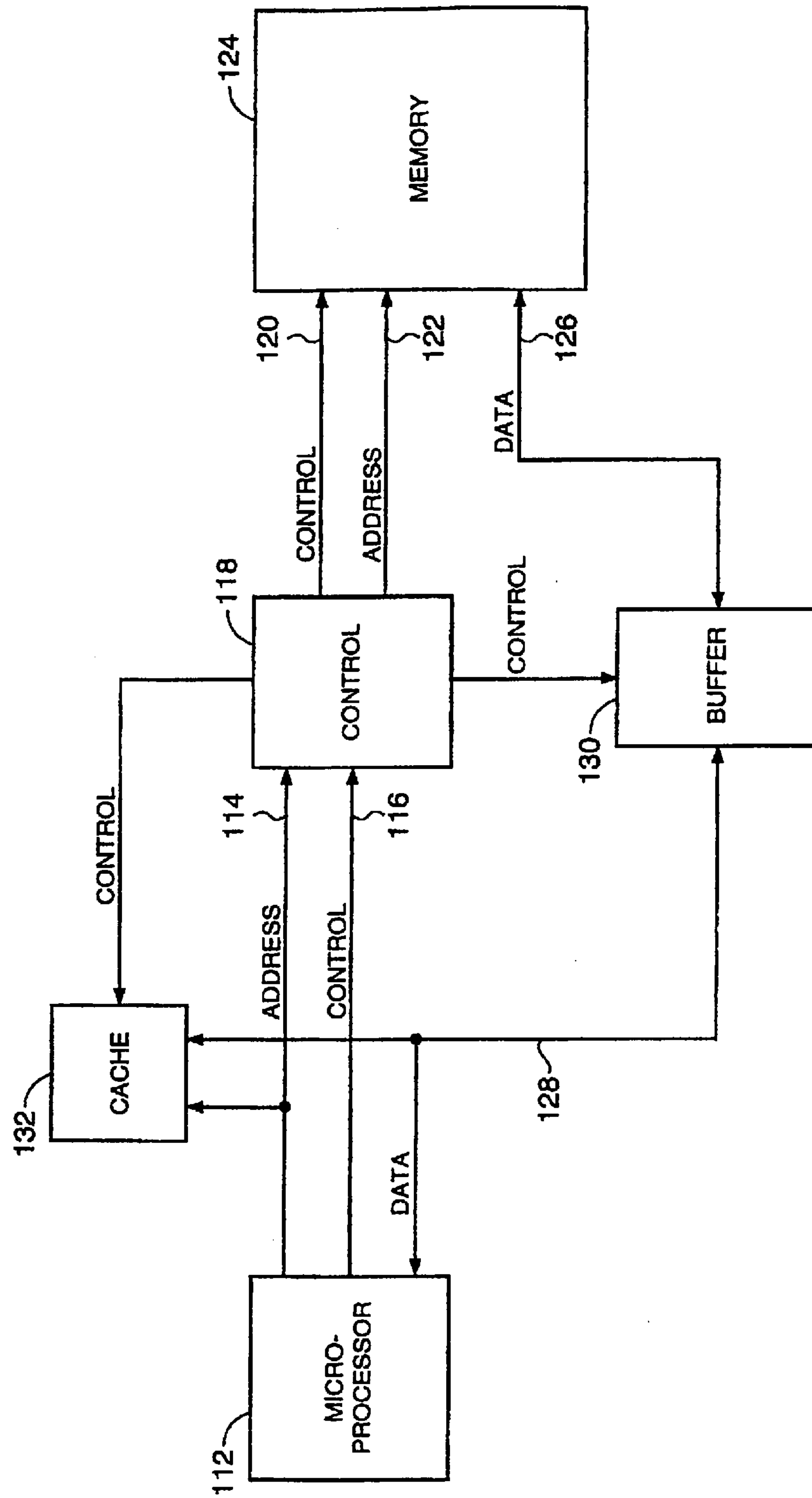

FIG. 6

DISTRIBUTED WRITE DATA DRIVERS FOR BURST ACCESS MEMORIES

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation in part of application Ser. No. 08/386,894 filed Feb. 10, 1995, which is a continuation in part of application Ser. No. 08/370,761 filed Dec. 23, 1994.

FIELD OF THE INVENTION

This invention relates to memory device architectures designed to provide high density data storage with high speed read and write access cycles. This invention relates more specifically to circuits and methods for controlling memory write cycles.

BACKGROUND OF THE INVENTION

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead, data is held valid after /CAS goes high until sometime after the next /CAS low pulse occurs, or until /RAS or the output enable (/OE) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can be a complex function of when the column address inputs are valid, when /CAS falls, the state of /OE and when /CAS rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially /CAS) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM manufacturers.

Methods to shorten memory access cycles tend to require additional circuitry, additional control pins and nonstandard device pinouts. The proposed industry standard synchronous DRAM (SDRAM) for example has an additional pin for receiving a system clock signal. Since the system clock is connected to each device in a memory system, it is highly loaded, and it is always toggling circuitry in every device. SDRAMs also have a clock enable pin, a chip select pin and a data mask pin. Other signals which appear to be similar in name to those found on standard DRAMs have dramatically different functionality on a SDRAM. The addition of several control pins has required a deviation in device pinout from standard DRAMs which further complicates design efforts to utilize these new devices. Significant amounts of additional circuitry are required in the SDRAM devices which in turn result in higher device manufacturing costs.

It is desirable to design and manufacture a memory device having a standard DRAM pinout and a burst mode of operation where multiple data values can be sequentially written to or read from the device in response to a single address location and multiple access strobes. It is also desirable that this new memory device operate at higher frequencies than standard DRAMs.

There is a problem in performing write cycles at high frequencies. In standard Fast Page Mode and EDO mode DRAM devices, write cycles are performed in response to both /CAS and /WE being low after /RAS is low. If an address change occurs at approximately the same time that /CAS falls, then an additional delay is required to equilibrate input/output lines and to fire a new column prior to beginning the write cycle. Data to be written is latched, and the write cycle begins when the latter of /CAS and /WE goes low provided that the equilibrate is complete. Generally, the write time can be considered to be the period of time that /WE and /CAS are simultaneously low. However, in order to allow for maximum page mode operating frequencies, the write cycle is often timed out so that it can continue for a short period of time after /CAS or /WE goes high especially for "late write" cycles. Maintaining the write cycle throughout the time-out period eases the timing specifications for /CAS and /WE that the device user must meet, and reduces susceptibility to glitches on the control lines during a write cycle. The write cycle is terminated after the time out period, and if /WE is high a read access begins based on the address present on the address input lines. The read access will typically begin prior to the next /CAS falling edge so that the column address to data valid specification can be met (tAA). In order to begin the read cycle as soon as possible, it is desirable to minimize the write cycle time while guaranteeing completion of the write cycle. Minimizing the write cycle duration in turn minimizes the margin to some device operating parameters despite the speed at which the device is actually used. Circuits to model the time required to complete the write cycle typically provide an estimate of the time required to write an average memory cell. While it is desirable to minimize the write cycle time, it is also necessary to guarantee that enough time is allowed for the write to complete, so extra delay is added making the write cycle slightly longer than required.

Another aspect of controlling the write cycle timing includes delaying the write enable or write enables to guarantee that the write data drivers are not enabled prior to the completion of the equilibrate function. Equalization of internal data I/O lines is performed in response to column address transitions in preparation for reading or writing data from another memory cell, and also in response to receipt of a write command to reduce the maximum signal transition on the data lines once the write drivers are enabled. If the data lines are each equalized to one half of Vcc for example, then the write data drivers will only need to drive one line from half Vcc to ground, and the other from half Vcc to Vcc. Otherwise, if the write data is not equal to the data previously on the I/O lines, the write data drivers will need to drive both true and compliment I/O lines a full Vcc swing for each data bit being written. Equalization of the data I/O lines reduces the maximum write cycle time by eliminating the worst case signal swing conditions. A simple method of equilibrating the I/O lines is to: disable I/O line drivers; isolate the I/O lines from the digit lines; and couple complimentary I/O lines together. When a true I/O line is coupled to a complimentary I/O line, a logic high will be coupled to a logic low and each line will equalize to a potential approximately half way between a high and a low. It is important to disable the I/O line drivers during equilibration to prevent a true logic driver from being coupled to a complimentary logic driver which will draw excessive current from the logic high source to the logic low source.

Whether /CAS goes low last (early write) or /WE goes low last (late write), the column address will be valid at or before the write command is received. Hence, a delay from

receipt of the write command which is greater than the equilibrate time will guarantee that an equilibrate due to a column address change is complete prior to the enabling the write drivers. If an equilibrate of internal data I/O lines is performed in response to receipt of each write command, a simple delay of the write enables will allow for the equilibrate to complete prior to enabling the write drivers. The delay value for the write cycle to write driver enable delay must account for the worst case signal delays from the equilibrate and write driver enable signal sources to the furthest data I/O line equilibrate devices and write data drivers. Since the equilibrate and write driver enable signal sources are located in a main logic area, a considerable signal propagation delay will result from the transmission of these signals across the chip to the furthest I/O line pair. Timing delays due to routing differences in the two signal paths can be very difficult to accurately model and predict. To overcome these difficulties, extra delay is added for timing margin. Unfortunately, this prevents the write drivers from being enabled as soon as the equilibrate function is complete.

Throughout the memory device product lifetime, manufacturing process advances and circuit enhancements often allow for increases in device operating frequencies. The write cycle timing circuits may need to be adjusted to shorten the minimum write cycle times to match these performance improvements. Adjustments may include shortening the equilibrate time, shortening the write cycle to write driver enable time and shortening the write cycle hold time. Fine tuning of these timing circuits is time consuming and costly. If the write cycles are too short, the device may fail under some or all operating conditions. If the write cycles are too long, the device may not be able to achieve the higher operating frequencies that are more profitable for the device manufacturers. Finally, if the equilibrate is not complete prior to enabling the write drivers, then excessive current may flow through the write drivers from Vcc to ground.

With the increased operating frequencies of burst access memory devices a new method of generating the write cycle timing is desired which will allow for maximum write cycle times despite the operating frequency of the device.

SUMMARY OF THE INVENTION

An integrated circuit memory device with a standard DRAM pinout is designed for high speed data access and for compatibility with existing memory systems. A high speed burst mode of operation is provided where multiple sequential accesses occur following a single column address, and read data is output relative to the /CAS control signal. In the burst mode of operation the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at high speeds. Only one control line per memory chip (/CAS) must toggle at the operating frequency in order to clock the internal address counter and the data input/output latches. The load on each /CAS is typically less than the load on the other control signals (/RAS, /WE and /OE) since each /CAS typically controls only a byte width of the data bus.

A new write cycle timing method and circuit allow for maximized write cycle timing at all operating frequencies to provide maximum write cycle timing margins. Write control is maintained throughout a write cycle such that the write operation time approaches the write cycle time. The write function is only halted between write cycles for a period of time required to select a new column of the array and to equilibrate I/O lines in the array. To maximize write cycle times, a logic device is located near the sense amplifiers of the device to control the write function directly with the use of the I/O line equilibrate signal. It is important to disable the write drivers during the equilibrate time to prevent current flow through the true and compliment data drivers while the I/O lines are coupled together. The local write enable circuit allows the write cycle time to be essentially equal to the access cycle time minus the I/O line equilibrate time in burst access memory devices. For nonburst mode memory devices such as EDO and Fast Page Mode, the write function may begin immediately following the end of the equilibration cycle to provide a maximum write time without interfering with the address setup time of the next cycle.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention as well as objects and advantages are best understood by reference to the appended claims, detailed description of particular embodiments and accompanying drawings where:

FIG. 1 is an electrical schematic diagram of a memory device in accordance with one embodiment of the invention;

FIG. 2 is a timing diagram for a method of accessing the device of FIG. 1;

FIG. 3 is a top view of a general device layout for a device designed in accordance with the teachings of the present invention;

FIG. 4 is block level schematic of a data path portion of the device of FIG. 3;

FIG. 5 is a more detailed schematic of a portion of the circuitry of FIG. 4; and

FIG. 6 is a schematic diagram of a computer system designed in accordance with the teachings of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a schematic representation of a sixteen megabit device designed in accordance with the present invention. The device is organized as a 2 Meg×8 burst EDO DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array 12. The device of FIG. 1 has an industry standard pinout for eight bit wide EDO DRAMs. An active-low row address strobe (/RAS) signal 14 is used to latch a first portion of a multiplexed memory address, from address inputs A0 through A10 16, in latch 18. The latched row address 20 is decoded in row decoder 22. The decoded row address is used to select a row of the memory array 12. A column address strobe (/CAS) signal 24 is used to latch a second portion of a memory address from address inputs 16 into column address counter 26. The latched column address 28 is decoded in column address decoder 30. The decoded column address is used to select a column of the memory array 12.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 32 to output latches 34. Data 10 driven from the burst EDO DRAM may be latched external to the device in synchronization with /CAS after a

predetermined number of /CAS cycle delays (latency). For a two cycle latency design, the first /CAS falling edge is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second /CAS falling edge, and remains valid through the third /CAS falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers 34 continue to drive the data lines without tri-stating the data outputs during /CAS high intervals dependent on the state of the output enable and write enable (/OE and /WE) control lines, thus allowing additional time for the system to latch the output data. Once a row and a column address are selected, additional transitions of the /CAS signal are used to advance the column address within the column address counter in a predetermined sequence. The time at which data becomes valid at the outputs of the burst EDO DRAM is dependent only on the timing of the /CAS signal provided that /OE is maintained low, and /WE remains high. The output data signal levels may be driven in accordance with, but are not limited to, CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. The column address may be advanced with each /CAS transition, each pulse, or multiple of /CAS pulses in the event that more than one data word is read from the array with each column address. When the address is advanced with each transition of the /CAS signal, data is also driven from the part after each transition following the device latency which is then referenced to each edge of the /CAS signal. This allows for a burst access cycle where the highest switching control line (/CAS) toggles only once (high to low or low to high) for each memory cycle. This is in contrast to standard DRAMs which require /CAS to go low and then high for each cycle, and synchronous DRAMs which require a full clock cycle (high and low transitions) for each memory cycle. For maximum compatibility with existing EDO DRAM devices, the invention will be further described in reference to a device designed to initiate access cycles on falling edges of the /CAS signal. For designs where falling edges of the /CAS signal initiate an access cycle, the falling edge may be said to be the active transition of the /CAS signal.

It may be desirable to latch and increment the column address after the first /CAS falling edge in order to apply both the latched and incremented addresses to the array at the earliest opportunity in an access cycle. For example, a device may be designed to access two data words per cycle (prefetch architecture). The memory array for a prefetch architecture device may be split into odd and even array halves. The column address least significant bit is used to select between odd and even halves while the other column address bits select a column within each of the array halves. In an interleaved access mode with column address 1, data from columns 0 and 1 are read and the data from column 1 is output followed by the data from column 0 in accordance with standard interleaved addressing as described in SDRAM specifications. In a linear access mode column address 1 is applied to the odd array half, and incremented to address 2 for accessing the even array half to fulfill the two word access. One method of implementing this type of device architecture is to provide a column address incrementing circuit between the column address counter and the even array half. The incrementing circuit increments the column address only if the initial column address in a burst access cycle is odd, and the address mode is linear. Otherwise the incrementing circuit passes the column address unaltered. For a design using a prefetch of two data accesses per cycle, the column address is advanced once for every two active edges of the /CAS signal. In a write cycle, multiple data words may be temporarily stored as they are input to the device. The actual write of data to the memory cells occurs after the last input data is latched, and may extend slightly into the next memory cycle as long as it ends prior to the next column being activated. Prefetch architectures where more than two data words are accessed are also possible.

Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS.

In the burst access memory device, each new column address from the column address counter is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16. This burst sequence of data continues for each /CAS falling edge until a predetermined number of data accesses equal to the burst length occurs. A /CAS falling edge received after the last burst address has been generated latches another column address from the address inputs 16 and a new burst sequence begins. Read data is latched and output with each falling edge of /CAS after the first /CAS latency.

For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the /CAS signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is preferred. Additional input data words for storage at incremented column address locations are latched by /CAS on successive /CAS active transitions. Input data from the input latches 34 is passed along data path 32 to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes are performed without the requirement of additional column addresses being provided on the address lines 16. After the predetermined number of burst writes occur, a subsequent /CAS pulse latches a new beginning column address, and another burst read or write access begins.

The memory device of FIG. 1 may include the option of switching between burst EDO and standard EDO modes of operation. In this case, the write enable signal /WE 36 is used at the row address latch time (/RAS falling, /CAS high) to determine whether memory accesses for that row are burst or page mode cycles. If /WE is low when /RAS falls, burst access cycles are selected. If /WE is high at /RAS falling, standard extended data out (EDO) page mode cycles are selected. Both the burst and EDO page mode cycles allow for increased memory device operating frequencies by not requiring the data output drivers 34 to place the data lines 10 in a high impedance state between data read cycles while /RAS is low. DRAM control circuitry 38, in addition to performing standard DRAM control functions, controls the I/O circuitry 34 and the column address counter/latch 26 in accordance with the mode selected by /WE when /RAS falls. In a burst mode only DRAM, or in a device designed with an alternate method of switching between burst and non-burst access cycles, the state of /WE when /RAS falls may

be used to switch between other possible modes of operation such as interleaved versus linear addressing modes.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by /CAS. /WE low at the column address latch time selects a burst write access. /WE high at the column address latch time selects a burst read access. The level of the /WE signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access terminates the burst access, preventing further writes from occurring. A high to low transition on /WE within a burst read access likewise terminates the burst read access and places the data output 10 in a high impedance state. Transitions of the /WE signal may be locked out during critical timing periods within an access cycle in order to reduce the possibility of triggering a false write cycle, and/or to guarantee the completion of a write cycle once it has begun. After the critical timing period the state of /WE determines whether a burst access continues, is initiated, or is terminated. Termination of a burst access places the DRAM in a state to receive another burst access command. Both /RAS and /CAS going high during a burst access also terminates the burst access cycle placing the data drivers in a high impedance output state. Read data may remain valid at the device outputs if /RAS alone goes high while /CAS is active for compatibility with hidden refresh cycles, otherwise /RAS high alone may be used to terminate a burst access. A minimum write enable pulse width is only required when it is desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses. In the case of burst reads, /WE transitions from high to low to terminate a first burst read, and then /WE transitions back high prior to the next falling edge of /CAS in order to specify a new burst read cycle. For burst writes, /WE transitions high to terminate a current burst write access, then back low prior to the next falling edge of /CAS to initiate another burst write access. A minimum /WE pulse width may be specified to guarantee recognition of the /WE pulse despite /WE lockout periods. If no /WE lockout circuit is used, termination of a burst access may be edge sensitive to the /WE signal.

A basic implementation of the device of FIG. 1 may include a fixed burst length of 4, a fixed /CAS latency of 2 and a fixed interleaved sequence of burst addresses. This basic implementation requires very little additional circuitry to the standard EDO page mode DRAM, and may be mass produced to provide the functions of both the standard EDO page mode and burst EDO DRAMs. This device also allows for the output enable pin (/OE) to be grounded for compatibility with many SIMM module designs. When not disabled (tied to ground), /OE is an asynchronous control which prevents data from being driven from the part in a read cycle if it is inactive (high) prior to /CAS falling and remains inactive beyond /CAS rising. If these setup and hold conditions are not met, then the read data may be driven for a portion of the read cycle. It is possible to synchronize the /OE signal with /CAS, however this typically increases the /CAS to data valid delay time and doesn't allow for the last output data to be disabled prior to /RAS high without an additional /CAS low pulse which would otherwise be unnecessary. In a preferred embodiment, if /OE transitions high at any time during a read cycle the outputs remain in a high impedance state until the next falling edge of /CAS despite further transitions of the /OE signal.

Programmability of the burst length, /CAS latency and address sequences may be accomplished through the use of a mode register 40 which latches the state of one or more of the address input signals 16 or data signals 10 upon receipt of a write-/CAS-before-/RAS (WCBR) programming cycle. In such a device, outputs 44 from the mode register control the required circuits on the DRAM. Burst length options of 2, 4, 8 and full page as well as /CAS latencies of 1, 2 and 3 may be provided. Other burst length and latency options may be provided as the operating speeds of the device increase, and computer architectures evolve. The device of FIG. 1 includes programmability of the address sequence by latching the state of the least significant address bit during a WCBR cycle. The burst length and /CAS latency for this particular embodiment are fixed. Other possible alterations in the feature sets of this DRAM include having a fixed burst mode only, selecting between standard fast page mode (non-EDO) and burst mode, and using the output enable pin (/OE) 42 in combination with /RAS to select between modes of operation. Also, a WCBR refresh cycle could be used to select the mode of operation rather than a control signal in combination with /RAS. A more complex memory device may provide additional modes of operation such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of /WE and /OE at /RAS falling time. One mode from a similar set of modes may be selected through the use of a WCBR cycle using multiple address or data lines to encode the desired mode. Alternately, a device with multiple modes of operation may have wire bond locations, or programmable fuses which may be used to program the mode of operation of the device.

A preferred embodiment of a sixteen bit wide burst EDO mode DRAM designed in accordance with the teachings of this invention has two column address strobe input pins /CASH and /CASL. For read cycles only one /CAS signal needs to toggle. The second /CAS may remain high or toggle with the other /CAS. During burst read cycles, all sixteen data bits will be driven out of part during a read cycle even if one /CAS remains inactive. In a typical system application, a microprocessor reads all data bits on a data bus in each read cycle, but may only write certain bytes of data in a write cycle. Allowing one of the /CAS control signals to remain static during read cycles helps to reduce overall power consumption and noise within the system. For burst write access cycles, each of the /CAS signals (CASH and /CASL) acts as a write enable for an eight bit width of the data. The two /CAS's are combined in an AND function to provide a single internal /CAS which will go low when the first external /CAS falls, and returns high after the last external /CAS goes high. All sixteen data inputs are latched when the first of the /CAS signals transitions low. If only one /CAS signal transitions low, then the eight bits of data associated with the /CAS that remained high are not stored in the memory.

The present invention has been described with reference to several preferred embodiments. Just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including x1, x4, x8 and x16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the memory device of the present invention may take the form of many different memory organizations. It is believed that one who is skilled in the art of integrated circuit memory design can, with the aide of this specification design a variety of memory devices which do not depart from the spirit of this invention. It is therefore believed that detailed descriptions of the various memory device organizations applicable to this invention are not necessary.

It should be noted that the pinout for this new burst EDO memory device may be identical to the pinout for a standard

EDO DRAM. The common pinout allows this new device to be used in existing memory designs with minimum design changes. The common pinout also allows for ease of new designs by those of skill in the art who are familiar with the standard EDO DRAM pinout. Variations of the described invention which maintain the standard EDO DRAM pinout include driving the /CAS pin with a system clock signal to synchronize data access of the memory device with the system clock. For this embodiment, it may be desirable to use the first /CAS active edge after /RAS falls to latch the row address, a later edge may be used to latch the first column address of a burst access cycle. After row and column addresses are latched within the device, the address may be incremented internally to provide burst access cycles in synchronization with the system clock. Other pin function alternatives include driving the burst address incrementing signal on the /OE pin since the part does not require a data output disable function on this pin. Other alternate uses of the /OE pin also allow the device to maintain the standard EDO pinout, but provide increased functionality such as burst mode access. The /OE pin may be used to signal the presence of a valid column starting address, or to terminate a burst access. Each of these embodiments provides for a high speed burst access memory device which may be used in current memory systems with a minimum amount of redesign.

FIG. 2 is a timing diagram for performing a burst read followed by a burst write of the device of FIG. 1. In FIG. 2, a row address is latched by the /RAS signal. /WE is low when /RAS falls for an embodiment of the design where the state of the /WE pin is used to specify a burst access cycle at /RAS time, otherwise /WE may be a "don't care" at /RAS falls. Next, /CAS is driven low with /WE high to initiate a burst read access, and the initial column address is latched. The data out signals (DQ's) are not driven in the first /CAS cycle. On the second falling edge of the /CAS signal the internal address generation circuitry provides a column address, and another access of the array begins. The first data out is driven from the device following the second /CAS and a /CAS to data access time (tCAC) delay. Additional burst access cycles continue, for a device with a specified burst length of four, until the fifth falling edge of /CAS which latches a new column address for a new burst read access. /WE falling in the fifth /CAS cycle terminates the burst access, and initializes the device for additional burst accesses. The sixth falling edge of /CAS with /WE low is used to latch a new burst address, latch input data and begin a burst write access of the device. Additional data values are latched on successive /CAS falling edges until /RAS rises to terminate the burst access.

It should be noted from FIG. 2 that for burst read cycles the data remains valid on the device outputs as long as the /OE pin is low, except for brief periods of data transition. Also, since the /WE pin is low prior to or when /CAS falls, the data input/output lines are not driven from the part during write cycles, and the /OE pin is a "don't care". Only the /CAS signal and the data signals toggle at relatively high frequency, and no control signals other than /CAS are required to be in an active or inactive state for one /CAS cycle time or less. This is in contrast to SDRAMs which often require row address strobes, column address strobes, data mask, and read/write control signals to be valid for one clock cycle or less for various device functions. Typical DRAMs also allow for the column address to propagate through to the array to begin a data access prior to /CAS falling. This is done to provide fast data access from /CAS falling if the address has been valid for a sufficient period of time prior to /CAS falling for the data to have been accessed from the array. In these designs an address transition detection circuit is used to restart the memory access if the column address changes prior to /CAS falling. This method actually requires additional time for performing a memory access since it must allow for a period of time at the beginning of each memory cycle after the last address transition to prepare for a new column address by equilibrating internal I/O lines, deselecting all columns and selecting a new column. Changes in the column address just prior to /CAS falling may increase the access time by approximately five nanoseconds. An embodiment of the present invention will not allow the column address to propagate through to the array until after /CAS has fallen. This eliminates the need for address transition detection circuitry, and allows for a fixed array access time relative to /CAS. In a preferred embodiment of the design, the address counter is advanced on /CAS rising edges, and the address generated in the counter is then presented to the array on the next /CAS falling edge in a burst access.

FIG. 3 shows a topographic layout view of one embodiment of a memory device designed in accordance with the teachings of the present invention. Memory device **50** has a central logic region **52**, array regions **54**, and logic and pads regions **56**. Circuitry in region **52** includes write control circuitry **58** and equilibration control circuitry **60** in addition to other memory timing control circuits. Circuitry in array interface regions **62** includes array address drivers. Circuitry in the logic and pads areas includes data buffers and I/O pads. I/O pads running through the center of a chip in this fashion is indicative of a Leads Over Chip (LOC) packaging configuration. The layout shown is for example only. Other possible layouts include but are not limited to: a) layouts with pads and central logic circuits located on the sides and/or ends of the memory device with array circuitry occupying the center of the device; b) central logic circuits located centrally along one axis of the device with pads on the sides or ends of the device; or c) central logic in the center of the chip with pads running through the chip and on the sides or ends of the chip for a hybrid of LOC and conventional bonding.

Array regions **54** are broken into **16** subarray regions **64** each of which has an associated data sense amplifier **66** located along one edge of the array. Write enable signal **68** and I/O line equilibrate signal **70** are routed to each data sense amplifier.

FIG. 4 is block level schematic of a data path portion of the device of FIG. 3. Elements in FIG. 4 that have the same or similar function as numbered elements in FIG. 3 are given the same reference numerals. In FIG. 4, data written to the memory device is received on data I/O pad **100**. The write data is passed through input circuit **102** to a global sense amp **66** over write data lines **103**. For this example, the sense amplifier includes an I/O line multiplexer **104** which is used to select a path from local I/O data line pair **106** to one of two pairs of array I/O lines **108** and **110**. Write data is driven from write data lines **103** to I/O lines **106** when enabled by a logical combination of the equilibrate signal **70** and the write enable signal **68** from timing circuit **59** and data path control circuit **124** of central logic circuitry **52**. In this example array I/O lines **108** are coupled to an adjacent section of the array (not shown). Array I/O lines **110** are true and compliment lines coupled to a local array sense amplifier **112** which is part of array section **64**. Column select signal **114** from column driver **115** couples array data I/O lines **110** to a pair of complimentary digit lines **116** inside the local sense amplifier **112**. One of the complimentary digit

lines is coupled to a memory cell **118** through an access device which is selected by a signal on word line **120** from a row address decoder.

Read data follows the same path from the memory cell to the global sense amp where it is then driven on complimentary data read lines **122** to complimentary data lines **126** under control of data path control logic **124** and timing circuits **59**. Complimentary data **126** is driven to an I/O pad **100** through output circuit **128**.

This specific embodiment is not intended to provide an exhaustive description of all forms of the present invention. For example, I/O line multiplexer **104** would not be necessary if there is a global sense amp **67** for each pair of array I/O lines. Alternatively, additional array I/O lines could be multiplexed through the multiplexer **104** to allow for even fewer global sense amplifiers. Another variation is to allow read and write data to share a common path between the global sense amplifiers and the I/O pad. Also, separate input and output data pins can be provided. Numerous additional variations are possible and will be recognized by one of skill in the art.

FIG. 5 is a schematic diagram providing additional detail for portions of the circuitry of FIG. 4. In FIG. 5, /WE and /CAS are logically combined in command latch and control circuit **154**. The write command output of circuit **154** is buffered through driver **156** to write command signal line **158**. The write command is coupled to a plurality of sense amps **66** through a distributed line resistance represented by resistor **160** over a signal line with distributed capacitive load represented by capacitor **162**. Write signal **164** arriving at the sense amplifier will be a delayed version of the output of the write command from the command latch.

Address inputs **170** are coupled to an address counter **172** and/or column address latch **174** which provide a burst column address **175** to the memory array. The column address and a version of the write command **176** are used to generate an equilibrate signal **182** in the address transition detection circuit **180**. For burst accesses, the address transition circuit may generate the equilibrate signal synchronously with an access cycle strobe signal rather than waiting for an actual address transition to be detected, especially if the address is advanced on rising /CAS edges in preparation for the next active falling edge. Equilibration control signal **182** passes through distributed resistance **184**, and is loaded by distributed capacitance **186**. A delayed version of the equilibrate signal **188** is coupled to the sense amp **66**.

The time delay of the write and equilibrate signals **164** and **188** at sense amp **66** will be dependent on which sense amp is being driven, as the distributed resistance and capacitances will vary for each sense amp location. Write command **164** and equilibrate signal **188** are combined at the global sense amp **66** in circuit **200**. In circuit **200**, the write command is gated with a decoded row address signal **204** in circuits **202** and **208**. Gated write command **210** is then combined with the equilibrate signal in logic gate **212** to form a write driver enable signal **214**. Equilibrate signal **188** provides an active low enable signal to data I/O line equilibration device **232**. When the equilibrate signal on line **188** is low, device **232** couples the two data I/O lines **106** together to equalize their potentials. A low on line **188** also disables logic device **212** preventing the write driver enable **214** from going active. When the equilibrate control signal **188** transitions high, the equilibration device **232** is deactivated, and the write driver enable gate **212** is enabled. For write cycles it is beneficial to provide the write command on line **164** before the equilibrate signal **188** goes high, then as soon as the equilibrate signal **188** goes high, the write command will be passed through gate **212** placing the write enable signal **214** in an active low condition without the requirement for an equilibration to write enable delay. Signal **214** is inverted in inverter **216** to provide an active high write enable **218**. The active low write enable goes to two NOR gates **242** and **246**. Active high write enable **218** is coupled to NAND gates **240** and **244**. The NOR and NAND gates pass write data to the I/O lines through devices **250**–**256** when enabled by the write driver enable signals **214** and **218**. For writing a logic "one" for example, the write data on line **103** may be high. A high on signal **103** in combination with a high write driver enable on signal line **218** will provide a low output from NAND gate **240** which will turn on device **250** to drive a logic one on the true I/O line. The high signal on data line **103** will disable NOR gate **242** to eliminate a current path to ground while NAND **250** is turned on. Data line **103** is inverted at inverter **258** to provide compliment data **260**. When data line **103** is high, complimentary data line **260** will be low which will enable NOR gate **246** and disable NAND gate **244**. Enabled NOR gate **246** combined with the active write driver enable signal **214** will provide a high output from NOR **246** to turn on device **256** and drive the complimentary I/O line low. For a maximized data write cycle time, the write command **164** can remain active throughout a burst write access. In this case, the write drivers are enabled and disabled by the equilibrate signal which will occur at the beginning of each access cycle. Multiple write command signals **158** may be utilized in devices with multiple /CAS or multiple /WE inputs to control writes to one of multiple data bytes for example. The decoded row address input prevents the write drivers from driving data on I/O lines in nonselected sections of the array. Multiplexer **104** of FIG. 4 may be turned on during equilibrate and write portions of the cycle to allow array I/O lines to first be equilibrated and then receive write data. For nonburst mode memory devices, it is beneficial to provide the write command prior to the end of the equilibrate function to allow the write to begin as soon as possible. For these devices, the write will typically end prior to the next /CAS falling edge to allow the device to meet the column address to data valid access time in (TAA). For EDO devices in particular, the page mode cycle time is very short, but the address access time begins while /CAS is high, so the write cycles should end as soon as possible. One way to allow the write cycle to end as soon as possible is to begin it immediately after the equilibrate is complete.

It is important to note that devices **250** and **256** will generally be enabled simultaneously, as will devices **252** and **254**. If the enable gate **212** were not locally present, then the write enable signal would need to be delayed from the equilibrate disable time to guarantee that a current path through devices **250**, **232** and **256** or devices **252**, **232** and **254** does not exist.

At the end of a burst write access, the write enable may be deactivated in response to /RAS high and /CAS high, /RAS high alone, or after a time-out period following /CAS high. As stated above, the write command may be held active throughout a burst write access. Alternatively, it may be cleared at the beginning of each access cycle, and then relatched provided that /WE is low on the following /CAS high to low transition. If cleared, the period of time that the write command is inactivated within a burst write access is preferably shorter than the equilibrate time so that the write cycle can be maximized which in turn allows for a minimum cycle time. When a read command is detected (/WE high at /CAS falling), a current burst write access will be terminated

and a burst read access will begin. It may be desirable to gate the equilibrate signal with the read command and the write control signal to ensure that the equilibrate signal does not end prior to the write control signal becoming invalid. This would be done to prevent the write drivers from becoming enabled for a fraction of the first read cycle in a burst read access sequence.

By gating the write command and equilibrate signals at the sense amplifiers, numerous advantages are obtained over the simple write command delay. One advantage is a maximized write time since the write cycle can begin as soon as the equilibrate is complete for all device types, and can last until the next cycle begins in burst access devices. A second advantage is elimination of write driver enable delay circuitry which can have a variable delay dependent on the operating conditions of the memory device (supply voltage, temperature, etc.). Each driver will be fired when the equilibrate signal is locally deactivated, eliminating the possibility of crossing current through complimentary write drivers while complimentary data lines are coupled together for equilibration.

A memory device may be designed with multiple /CAS inputs as described above. For a memory device with two /CAS inputs where each /CAS controls eight bits of a sixteen bit wide data port, a write cycle where only one /CAS is low must not write all data bits from the data input to the memory. A portion of the write data path associated with an inactive /CAS may be interrupted in a number of ways. Each of the two /CAS signals may enable half of the column address decoders such that no column will be selected in half of the memory associated with a high /CAS in a write cycle. In this case the write data drivers can be enabled, but the data I/O lines associated with a disabled column decoder will not be coupled to any memory cells. Alternately, the write control signals may be gated with the appropriate /CAS signal to prevent some of the write data drivers from being enabled. In this case, read data may be coupled from some memory cells to data I/O lines.

FIG. 6 is a schematic representation of a data processing apparatus designed in accordance with the present invention. For the purposes of this specification a microprocessor may be, but is not limited to, a central processing unit (CPU), a microprocessor, a microcontroller, a digital signal processor, or an arithmetic processor. In FIG. 6, microprocessor **112** is connected via address lines **114** and control lines **116** to a memory control circuit **118**. The memory control circuit provides address and control signals on lines **122** and **120** respectively to a burst access memory device **124**. The burst access memory device sends and receives data over data bus **126**. Optional data bus buffer **130** between memory data bus **126** and microprocessor data bus **128** allows for amplification of the data signals, and/or synchronization with the microprocessor and memory control signals. A fast static random access memory (SRAM) cache circuit **132** is also optional and provides higher speed access to data stored in the cache from the memory circuit or the microprocessor. Memory control circuit **118** may be incorporated within the microprocessor. The memory control circuit provides the required address strobe signals and read/write control signals required for burst mode access of the memory circuit. By providing burst access of the memory by the processor, a computer with relatively high memory bandwidth can be designed without the requirement of a fast SRAM cache. SPAMs which are fast enough to provide memory access without wait states can significantly add to the cost of a computer. Thus the burst access memory device of the present invention allows for medium to high performance computers to be manufactured at a cost which is significantly less than those manufactured today. Use of the burst access memory device of the present invention in cooperation with a fast SRAM cache allows for an even higher performance computer design by providing fast access to main memory in the event of a cache miss.

In a burst write operation, the processor **112** provides an initial address and a write command to the memory controller. The memory controller provides a row address to the memory with a row address strobe. The memory controller then provides a write command, a column address and a column address strobe to the memory. The memory will equilibrate internal data I/O lines in response to receipt of the write command and column address. During the equilibrate operation, write data and write command signals are passed to global sense amplifiers within the burst access memory device. At the end of the equilibrate operation, write data drivers are enabled, and write data is stored in the memory array. In a preferred embodiment, positive (low to high) transitions of /CAS will cause an internal address counter of the memory device to advance to the next burst address. Negative (high to low) transitions of /CAS will then end the previous write cycle and equilibrate the I/O lines. The negative transition of /CAS will also allow the burst address from the counter to be applied to the array. Once the equilibration is complete, the next write will be performed at the burst address from the counter. In an alternate embodiment, a clock signal is input to a burst access device to control generation of a burst address from the counter (SDRAMs for example have a clock input pin).

In another embodiment, memory **124** operates in a page mode such as Fast Page Mode or EDO mode. Write commands at memory sense amps are enabled by the equilibrate signal becoming inactive at the sense amp. Using the equilibrate signal at the sense amp to gate the write signal to enable the write drivers eliminates wasted time associated with delaying the write driver enable signal to prevent excessive currents from flowing through the write drivers during the equilibration operation.

For the purposes of this specification a node may be, but is not limited to, an intersection of conductors, a circuit input or output, or any point along a signal path. For example, the write command may be said to enter the global sense amp at node **164** and device **250** of FIG. **5** is said to be connected to a power source at node **270**. Also, the term signal may refer to but is not limited to information transferred along a conductor, or may refer to the conductor itself. For example, It may be said that the equilibrate signal **188** is coupled to the sense amp **66**. In this context, the term signal represents a physical conductor for carrying the electrical information to equilibrate the data I/O lines, and is not limited to the electrical information itself which is not present when the device is not connected to a power source. The term "coupled" refers to but is not limited to a connection which may be made directly, after buffering, or through another element such as a resistor, capacitor, transistor, or logic device. Typically, a device will be responsive at some time to a signal or another device which is coupled to it.

While the present invention has been described with reference to preferred embodiments, numerous modifications and variations of the invention will be apparent to one of skill in the art without departing from the scope of the invention.

What is claimed is:

1. A memory device having a plurality of internal data line pairs, an equilibration control circuit and a write cycle control circuit, the memory device further comprising:

a plurality of data sense amplifiers each coupled to the equilibration control circuit, the write cycle control circuit and at least one of the data line pairs;

a plurality of write data drivers, each write data driver associated with at least one of said data sense amplifiers; and

a plurality of write data driver enable circuits, each write driver enable circuit associated with one of said write data drivers to enable said write data drivers to drive data onto at least one of the data line pairs in response to deassertion of an equilibrate signal from the equilibration control circuit while a write cycle enable signal from the write cycle control circuit is asserted.

2. The memory device of claim 1, further comprising:

a burst access control circuit adapted to receive an initial address in response to an access cycle strobe signal and to generate a series of addresses, each in response to a further transition of the access cycle strobe signal.

3. The memory device of claim 2, further comprising:

an output buffer coupled to at least one of said data sense amplifiers and to the access cycle strobe signal, said output buffer adapted to drive data from the memory device in response to a plurality of transitions of the access cycle strobe signal.

4. The memory device of claim 3, wherein the access cycle strobe signal is a column address strobe signal and the memory device is a burst extended data out dynamic random access memory device.

5. The memory device of claim 1, wherein the memory device is adapted to operate in an Extended Data Out page mode.

6. A memory device comprising:

a plurality of write data drivers comprising an enable input, a data input and a data output;

a plurality of data lines, each of said data lines coupled to the data output of at least one of said write data drivers; and

a plurality of write data driver enable circuits, each of said write data driver enable circuits adapted to receive a write cycle control signal and an equilibrate control signal, each of said write data driver enable circuits located in close proximity and coupled to the enable input of at least one of said write data drivers.

7. The memory device of claim 6, further comprising:

a plurality of data sense amplifiers, each of said data sense amplifiers being associated with one of the plurality of write data drivers.

8. The memory device of claim 7, further comprising:

a plurality of memory element subarrays, each of said subarrays coupled to at least one of said write data drivers by at least one of said data lines, and each of said subarrays coupled to at least one of said data sense amplifiers by at least one of said data lines.

9. The memory device of claim 8, further comprising:

a plurality of equilibration transistors, each of said equilibration transistors responsive to the equilibrate control signal to couple at least two of said data lines together.

10. The memory device of claim 9, wherein said write data drivers are disabled by said write data driver enable circuits while said equilibration transistors couple said data lines together.

11. A memory device comprising:

a memory element array region;

a plurality of data line pairs dispersed within said memory element array region; and

a plurality of write data drivers dispersed along an edge of said memory element array region, each comprising an equilibrate input, a write active input, a write data input and a write data output, each of said write data drivers adapted to drive a data signal from the write data input to at least one of said data line pairs.

12. The memory device of claim 11, further comprising:

a main logic region outside said array region, said main logic region comprising an equilibration control circuit adapted to provide an equilibrate signal to the equilibrate input of said write data drivers.

13. The memory device of claim 12, further comprising:

a pads and logic region outside said array region and outside said main logic region, wherein the equilibrate signal is routed from said main logic region through said pads and logic region to said write data drivers.

14. The memory device of claim 11, further comprising:

a main logic region outside said array region, said main logic region comprising a write cycle control circuit adapted to provide a write active signal to the write active input of said write data drivers.

15. The memory device of claim 14, further comprising:

a pads and logic region outside said array region and outside said main logic region, wherein the write active signal is routed from said main logic region through said pads and logic region to said write data drivers.

16. A memory device comprising:

a memory element array region;

a control circuit region, outside of said memory element array region, for generating memory control signals including an equilibrate signal and a write enable signal;

a plurality of data line pairs dispersed throughout said memory element array region;

a plurality of data sense amplifiers, said data sense amplifiers distributed along an edge of said memory element array region, each amplifier proximately located to at least one of said data line pairs; and

a distributed plurality of write data drivers each comprising an equilibrate inactive input enable responsive to the equilibrate signal and a write active input enable responsive to the write enable signal, each of said write data drivers proximately located to a data sense amplifier and associated with at least one of said data line pairs.

17. The memory device of claim 16, further comprising:

an address strobe input adapted to receive an address strobe signal; and

an address counter responsive to the address strobe signal to generate an address and to provide the address to said memory element array region.

18. A memory device comprising:

a data input;

a plurality of memory element subarrays; and

a plurality of data sense amplifiers coupled to said subarrays, each of said data sense amplifiers comprising a write data driver responsive to an active write enable signal and an inactive equilibration signal, to drive write data received on said data input to a corresponding one of said subarrays.

19. A method of storing data in a system comprising steps of:

providing a memory having a distributed plurality of data driver enable circuits;

addressing the memory;

providing data to the memory;

asserting an equilibration signal at the plurality of data driver enable circuits in response to said step of addressing;

asserting a write enable signal to the plurality of data driver enable circuits;

deasserting the equilibration signal;

gating a write enable signal through at least one of the data driver enable circuits in response to said step of deasserting; and

storing data in a memory cell of the memory in response to said step of gating a write enable signal.

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United States Patent [19]

Manning

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[54] **BURST EDO MEMORY DEVICE WITH MAXIMIZED WRITE CYCLE TIMING**

[75] Inventor: **Troy A. Manning**, Boise, Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **386,894**

[22] Filed: **Feb. 10, 1995**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 370,761, Dec. 23, 1994.

[51] **Int. Cl.**[6] **G11C 7/00**

[52] **U.S. Cl.** **365/193**; 365/233; 365/189.05; 365/189.01

[58] **Field of Search** 365/233, 193, 365/189.05, 189.01, 230.01

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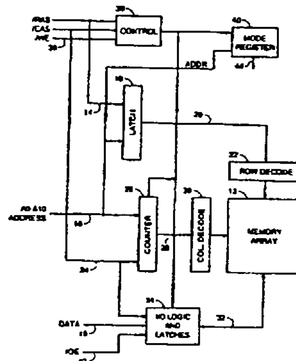
(List continued on next page.)

Primary Examiner—David C. Nelms
Assistant Examiner—Vu A. Le
Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

An integrated circuit memory device is designed for high speed data access and for compatibility with existing memory systems. An address strobe signal is used to latch a first address. During a burst access cycle the address is incremented internal to the device with additional address strobe transitions. A new memory address is only required at the beginning of each burst access. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at the device cycle frequency. A transition of the Read/Write control line during a burst access is used to terminate the burst access, reset the burst length counter and initialize the device for another burst access. Write cycle times are maximized to allow for increases in burst mode operating frequencies.

20 Claims, 8 Drawing Sheets



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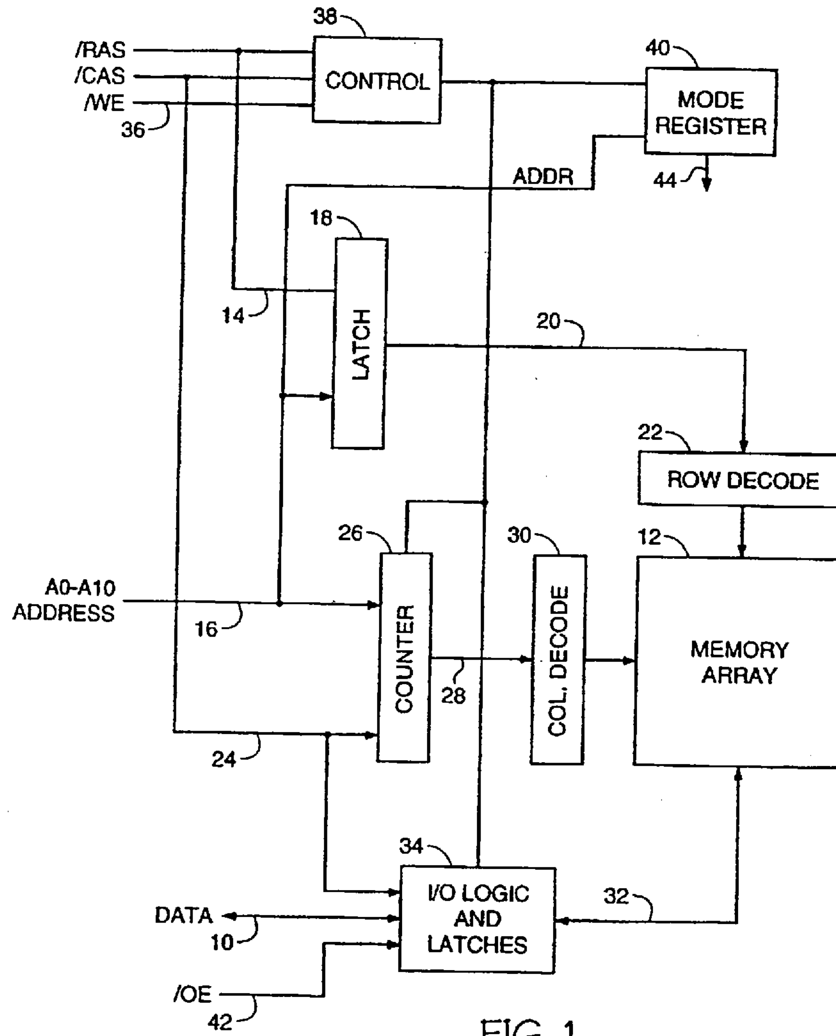

FIG. 1

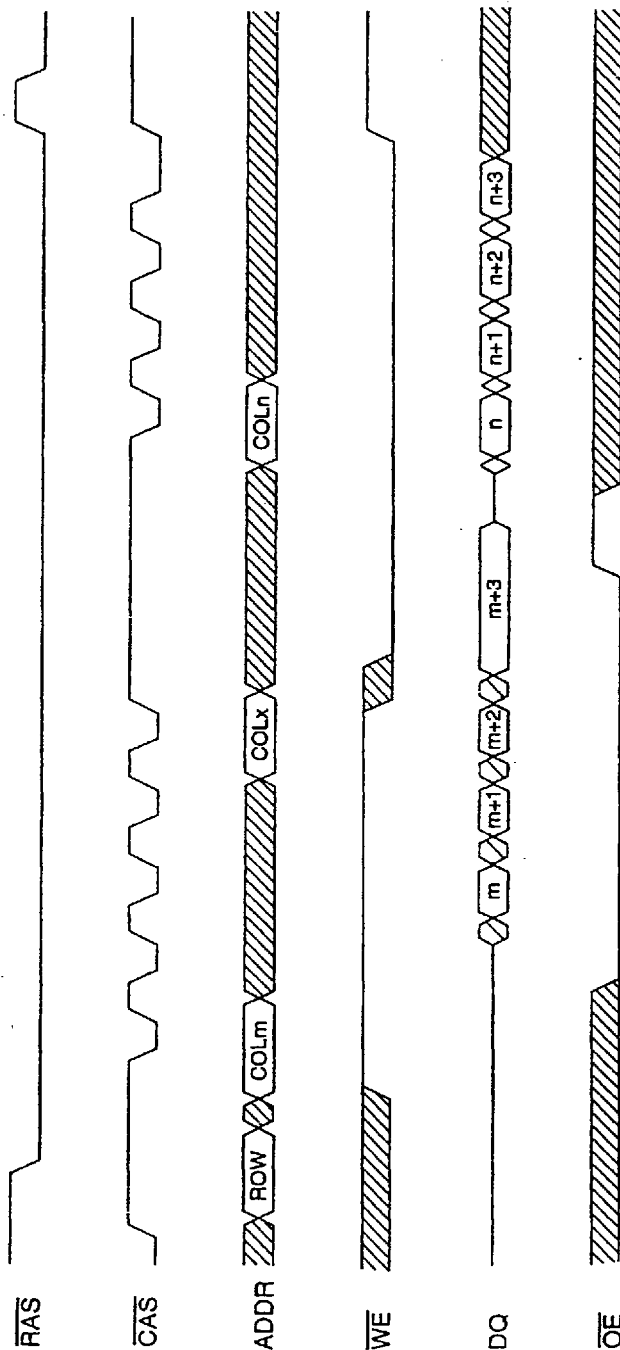

FIG. 2

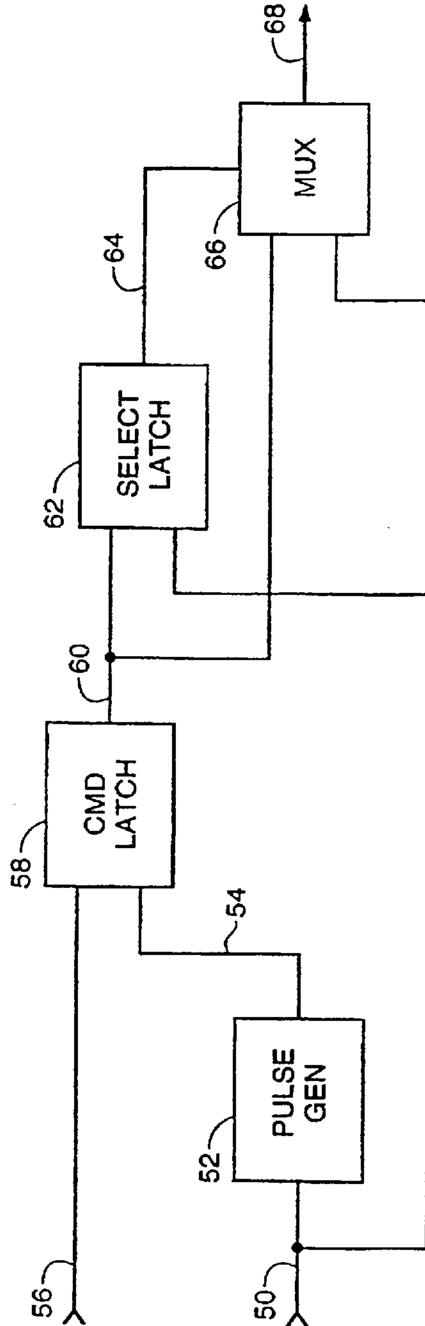

FIG. 3

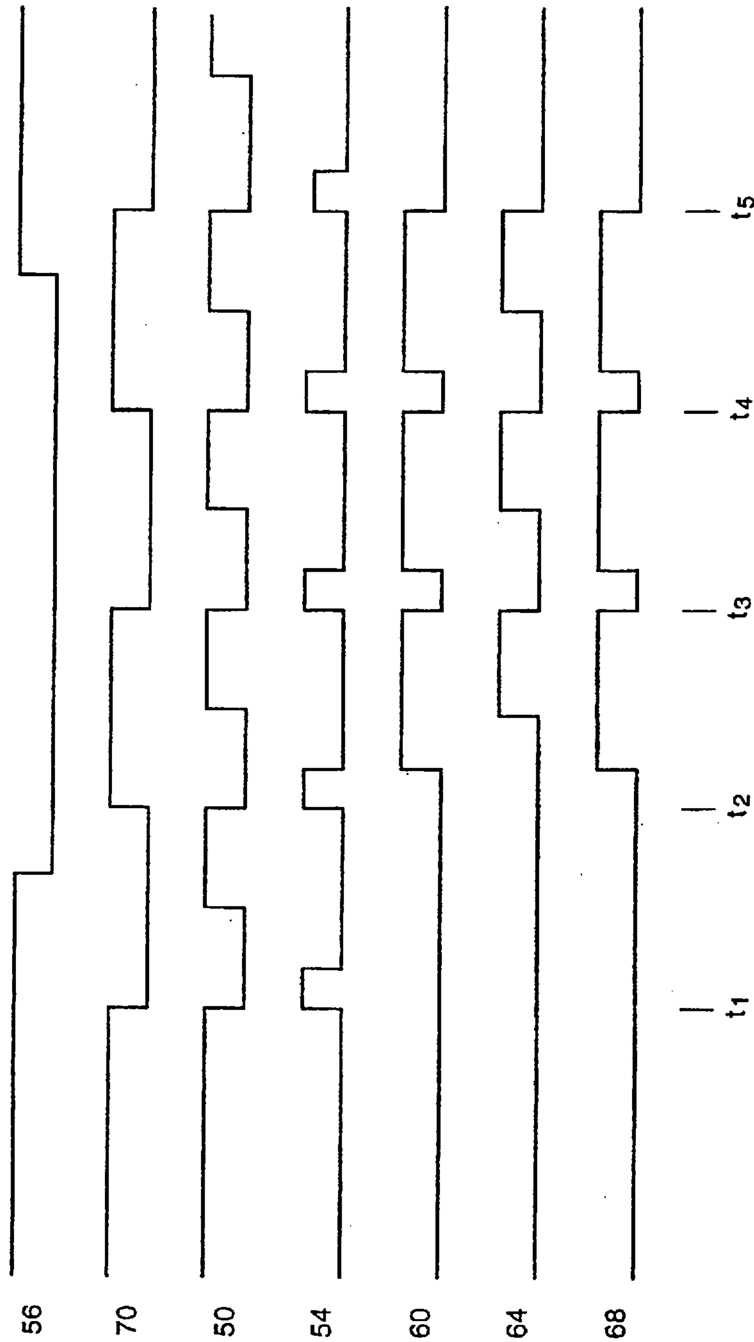

FIG. 4

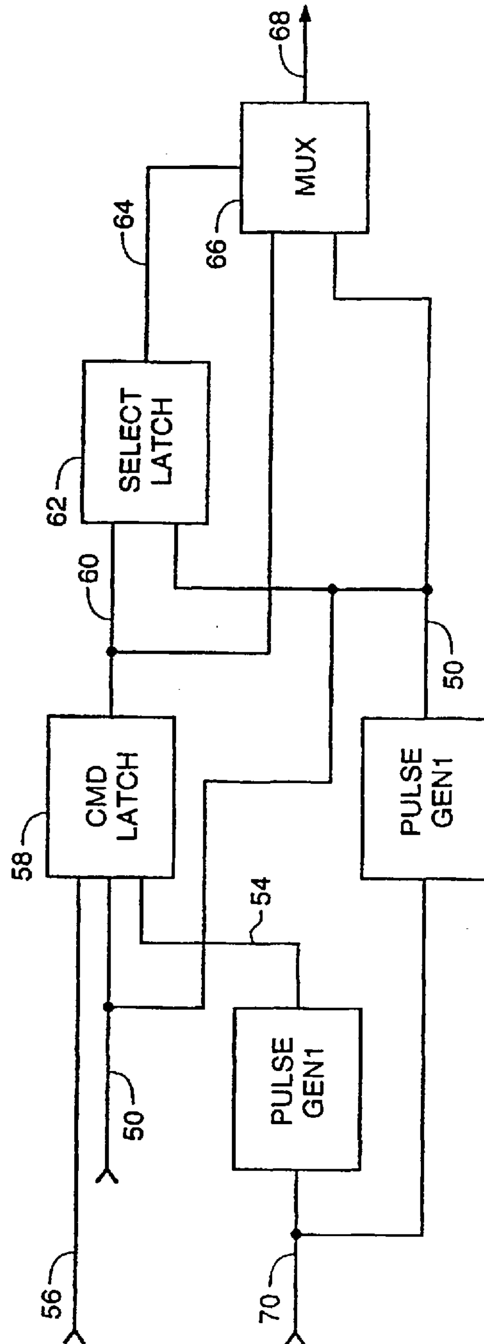

FIG. 5

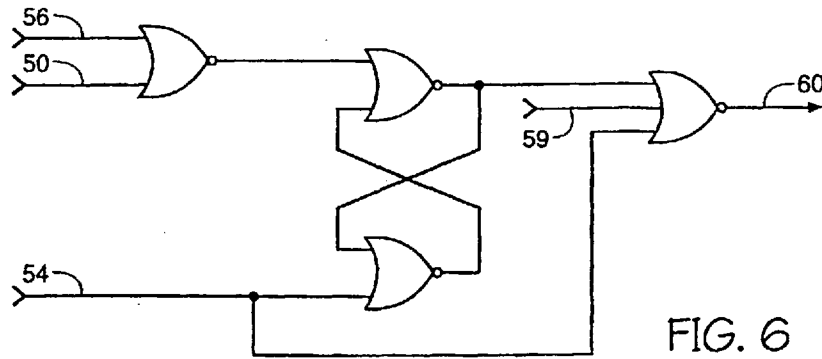

FIG. 6

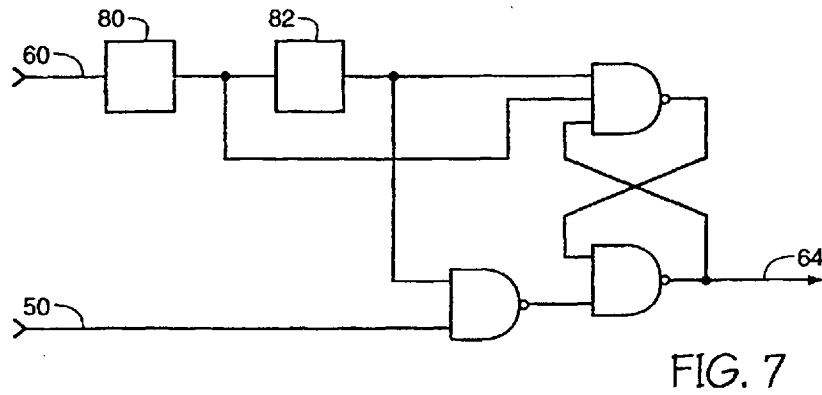

FIG. 7

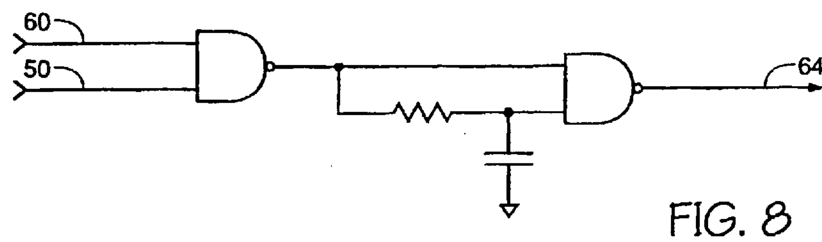

FIG. 8

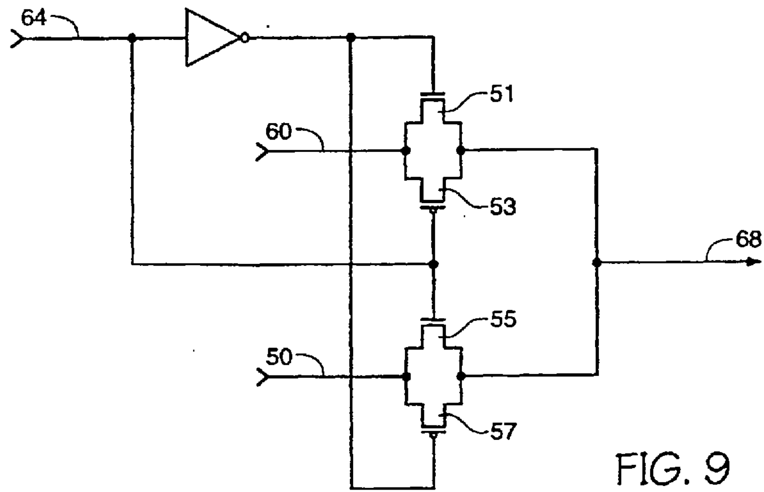

FIG. 9

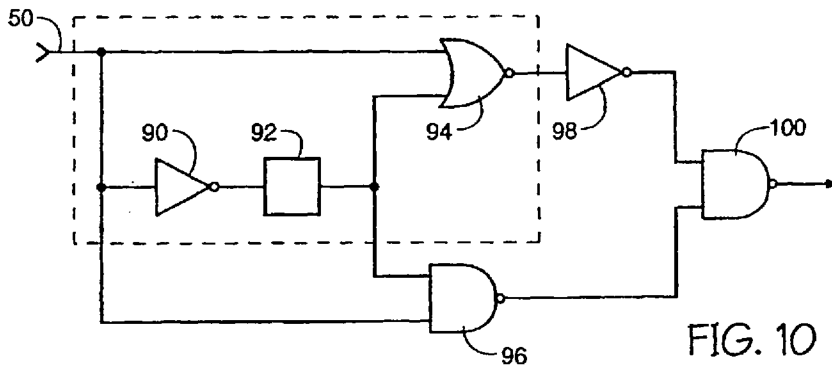

FIG. 10

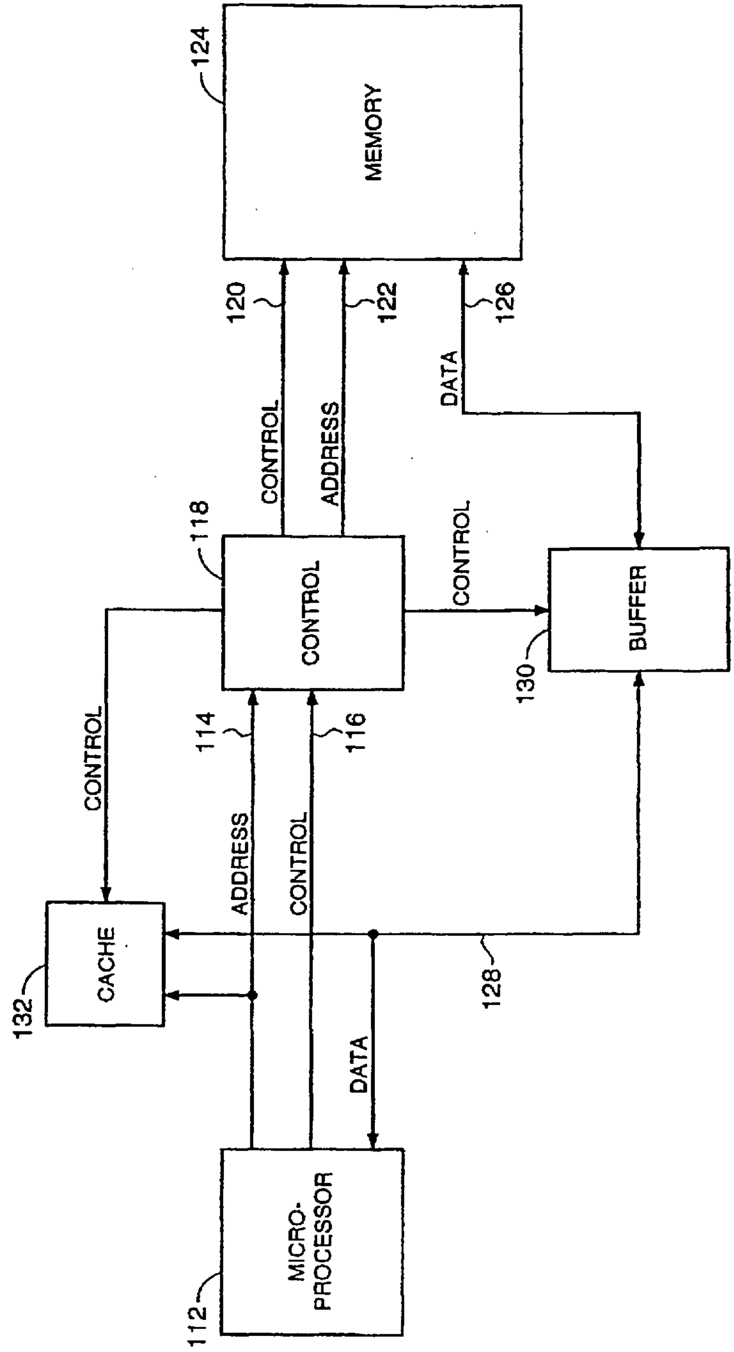

FIG. 11

BURST EDO MEMORY DEVICE WITH MAXIMIZED WRITE CYCLE TIMING

CROSS REFERENCE TO RELATED APPLICATION

This is a continuation-in-part to U.S. patent application Ser. No. 08/370,761, filed Dec. 23, 1994.

FIELD OF THE INVENTION

This invention relates to memory device architectures designed to provide high density data storage with high speed read and write access cycles. This invention relates more specifically to circuits and methods for controlling memory write cycles in burst access memory devices.

BACKGROUND OF THE INVENTION

Dynamic Random Access Memory devices (DRAMs) are among the highest volume and most complex integrated circuits manufactured today. Except for their high volume production, the state of the art manufacturing requirements of these devices would cause them to be exorbitantly priced. Yet, due to efficiencies associated with high volume production, the price per bit of these memory devices is continually declining. The low cost of memory has fueled the growth and development of the personal computer. As personal computers have become more advanced, they in turn have required faster and more dense memory devices, but with the same low cost of the standard DRAM. Fast page mode DRAMs are the most popular standard DRAM today. In fast page mode operation, a row address strobe (/RAS) is used to latch a row address portion of a multiplexed DRAM address. Multiple occurrences of the column address strobe (/CAS) latch multiple column addresses to access data within the selected row. On the falling edge of /CAS an address is latched, and the DRAM outputs are enabled. When /CAS transitions high the DRAM outputs are placed in a high impedance state (tri-state). With advances in the production of integrated circuits, the internal circuitry of the DRAM operates faster than ever. This high speed circuitry has allowed for faster page mode cycle times. A problem exists in the reading of a DRAM when the device is operated with minimum fast page mode cycle times. /CAS may be low for as little as 15 nanoseconds, and the data access time from /CAS to valid output data (tCAC) may be up to 15 nanoseconds; therefore, in a worst case scenario there is no time to latch the output data external to the memory device. For devices that operate faster than the specifications require, the data may still only be valid for a few nanoseconds. On a heavily loaded microprocessor memory bus, trying to latch an asynchronous signal that is valid for only a few nanoseconds is very difficult. Even providing a new address every 35 nanoseconds requires large address drivers which create significant amounts of electrical noise within the system.

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead, data is held valid after /CAS goes high until sometime after

the next /CAS low pulse occurs, or until /RAS or the output enable (/OE) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can be a complex function of when the column address inputs are valid, when /CAS falls, the state of /OE and when /CAS rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially /CAS) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM manufacturers.

Methods to shorten memory access cycles tend to require additional circuitry, additional control pins and nonstandard device pinouts. The proposed industry standard synchronous DRAM (SDRAM)for example has an additional pin for receiving a system clock signal. Since the system clock is connected to each device in a memory system, it is highly loaded, and it is always toggling circuitry in every device. SDRAMs also have a clock enable pin, a chip select pin and a data mask pin. Other signals which appear to be similar in name to those found on standard DRAMs have dramatically different functionality on a SDRAM. The addition of several control pins has required a deviation in device pinout from standard DRAMs which further complicates design efforts to utilize these new devices. Significant amounts of additional circuitry are required in the SDRAM devices which in turn result in higher device manufacturing costs.

It is desirable to design and manufacture a memory device having a standard DRAM pinout and a burst mode of operation where multiple data values can be sequentially written to or read from the device in response to a single address location and multiple access strobes. It is also desirable that this new memory device operate at higher frequencies than standard DRAMs.

There is a problem in performing write cycles at high frequencies. In a standard DRAM device, write cycles are performed in response to both /CAS and /WE being low after /RAS is low. Data to be written is latched, and the write cycle begins when the latter of /CAS and /WE goes low. In order to allow for maximum page mode operating frequencies, the write cycle is often timed out so that it can continue for a short period of time after /CAS goes high especially for "late write" cycles. Maintaining the write cycle throughout the timeout period eases the timing specifications for /CAS and /WE that the device user must meet, and reduces susceptibility to glitches on the control lines during a write cycle. The write cycle is terminated after the time out period, and if /WE is high a read access begins based on the address present on the address input lines. The read access will typically begin prior to the next /CAS falling edge so that the column address to data valid specification can be met (tAA). In order to begin the read cycle as soon as possible, it is desirable to minimize the write cycle time while guaranteeing completion of the write cycle. Minimizing the write cycle duration in turn minimizes the margin to some device operating parameters despite the speed at which the device is actually used. Circuits to model the time required to complete the write cycle typically provide an estimate of the time required to write an average memory cell. While it is desirable to minimize the write cycle time, it is also necessary to guarantee that enough time is allowed for the write to complete, so extra delay is added making the write cycle slightly longer than required. Throughout the memory device product lifetime, manufacturing process advances, and circuit enhancements often allow for increases in device operating frequencies. The write cycle timing circuits may need to be adjusted to shorten the minimum write cycle times to match these performance improvements. Fine tun-

United States Patent [19]

Zagar et al.

[11] Patent Number: 5,661,695

[45] Date of Patent: Aug. 26, 1997

[54] BURST EDO MEMORY DEVICE

[75] Inventors: Paul S. Zagar, Boise; Brett L. Williams, Eagle, both of Id.

[73] Assignee: Micron Technolgy, Inc., Boise, Id.

[21] Appl. No.: 630,279

[22] Filed: Apr. 11, 1996

Related U.S. Application Data

[63] Continuation of Ser. No. 370,761, Dec. 23, 1994, Pat. No. 5,526,320.

[51] Int. Cl.[6] G11C 8/00

[52] U.S. Cl. 365/233.5; 365/238.5; 365/189.01

[58] Field of Search 365/238.5, 233.5, 365/230.01, 230.06, 230.08, 235, 236, 189.01

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Shiva P. Gowni, et al., "A 9NS, 32K X 9, BICMOS TTL Synchronous Cache RAM with Burst Mode Access", *IEEE*, Custom Integrated Circuits Conference, pp. 781-786, (Mar. 3, 1992).

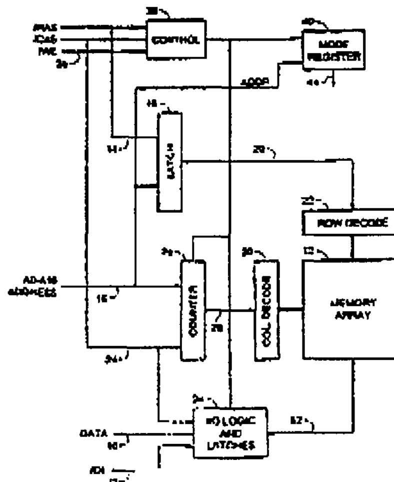
Primary Examiner—Tan T. Nguyen

Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] ABSTRACT

An integrated circuit memory device is designed for high speed data access and for compatibility with existing memory systems. An address strobe signal is used to latch a first address. During a burst access cycle the address is incremented internal to the device with additional address strobe transitions. A new memory address is only required at the beginning of each burst access. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at the device cycle frequency. Transitions of the Read/Write control line during a burst access will terminate the burst access, reset the burst length counter and initialize the device for another burst access. The device is compatible with existing Extended Data Out DRAM device pinouts, Fast Page Mode and Extended Data Out Single In-Line Memory Module pinouts, and other memory circuit designs.

9 Claims, 7 Drawing Sheets



DEPOSITION EXHIBIT 457

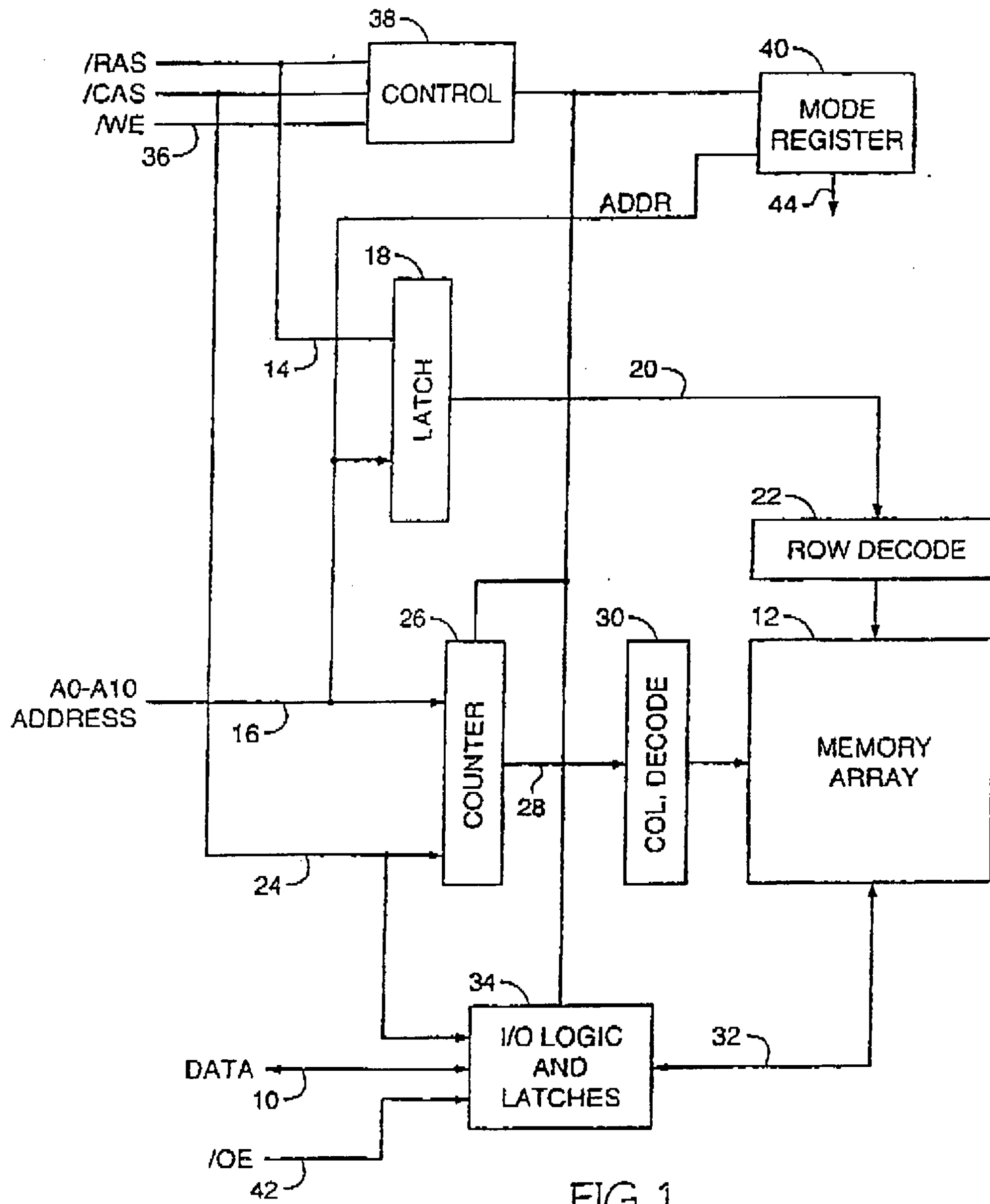


FIG. 1

Burst Length	Starting Column Address A_2	A_1	A_0	Linear	Interleave
2	V	V	0	0-1	0-1
	V	V	1	1-0	1-0
4	V	0	0	0-1-2-3	0-1-2-3
	V	0	1	1-2-3-0	1-0-3-2
	V	1	0	2-3-0-1	2-3-0-1
	V	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

FIG. 2

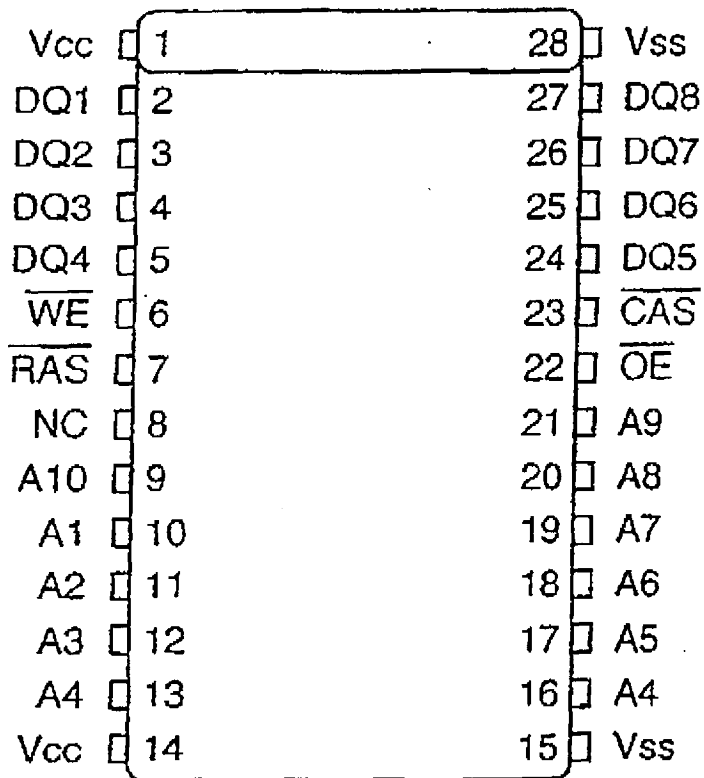


FIG. 3

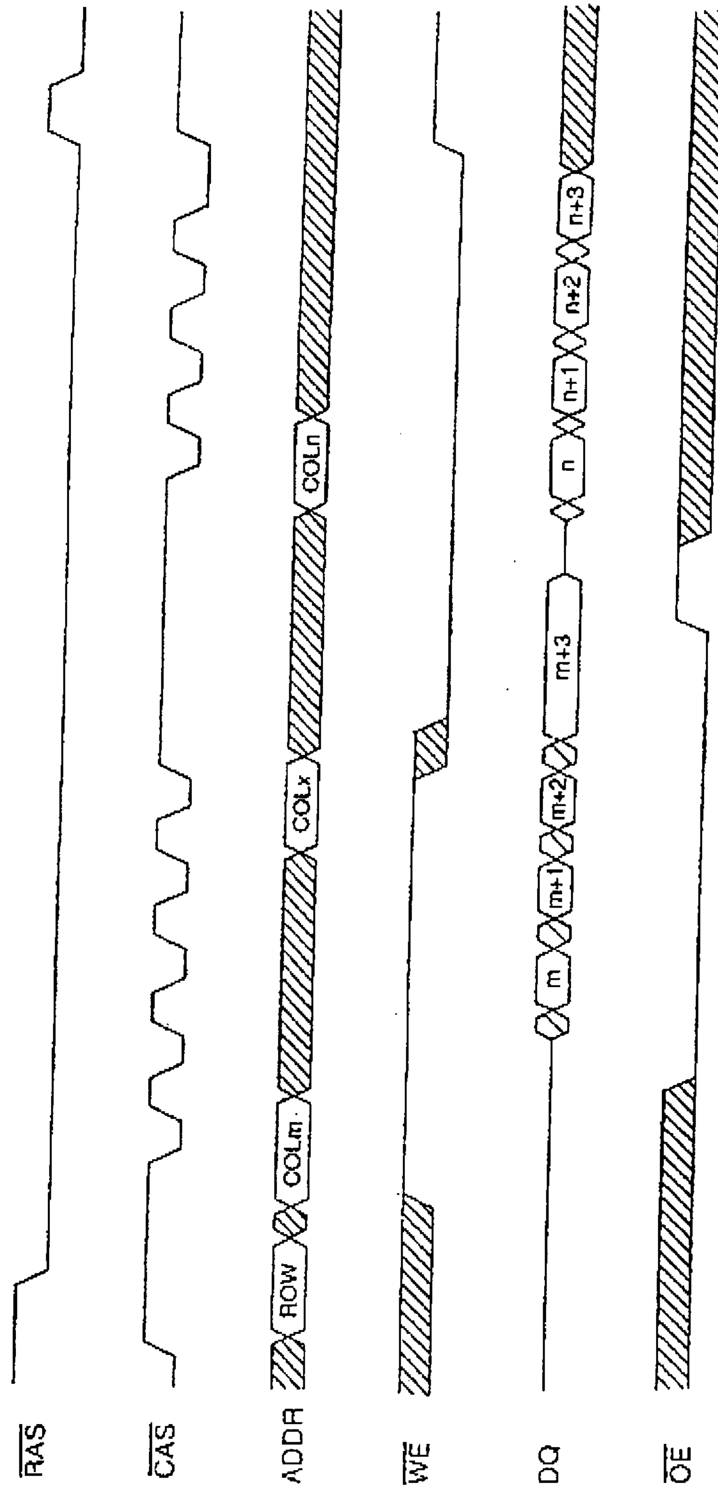


FIG. 4

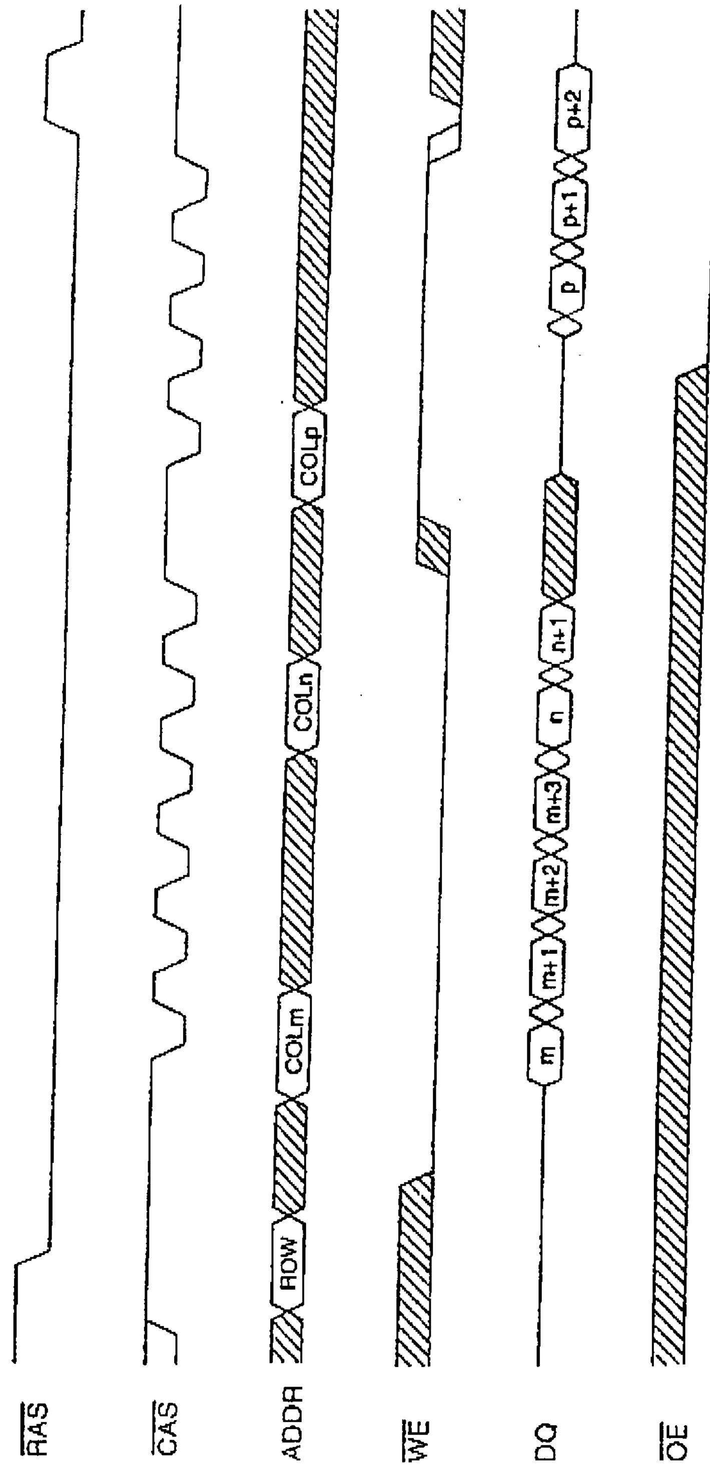


FIG. 5

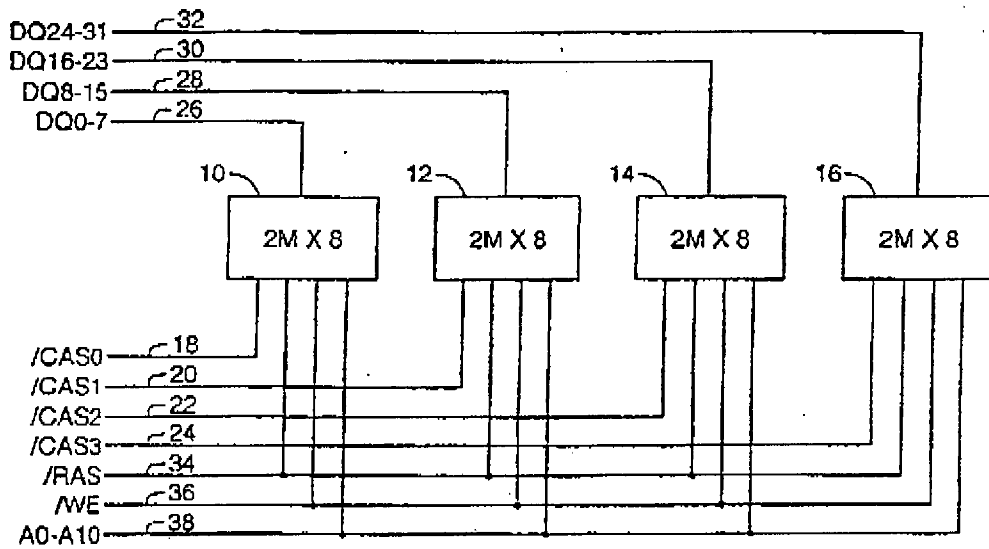


FIG. 6

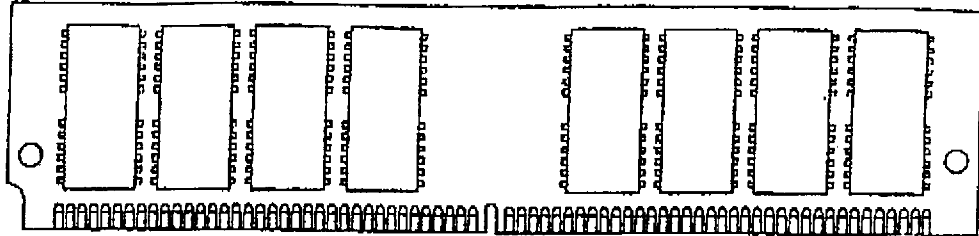


FIG. 7

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	$\overline{RAS1}$	63	DQ15
10	Vcc	28	A7	46	$\overline{OE}$	64	DQ32
11	PD5	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	PD ECC	66	PD EDO
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ25	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	NC	52	DQ26	70	PD4
17	A5	35	NC	53	DQ11	71	PD refresh
18	A6	36	NC	54	DQ27	72	Vss

FIG. 8

BURST EDO MEMORY DEVICE

This application is a continuation of Ser. No. 08/370,761 entitled "Burst EDO Memory Device," filed Dec. 23, 1994 now U.S. Pat. No. 5,526,320.

FIELD OF THE INVENTION

This invention relates to memory device architectures designed to provide high density data storage with high speed read and write access cycles.

BACKGROUND OF THE INVENTION

Dynamic Random Access Memory devices (DRAMs) are among the highest volume and most complex integrated circuits manufactured today. Except for their high volume production, the state of the art manufacturing requirements of these devices would cause them to be exorbitantly priced. Yet, due to efficiencies associated with high volume production, the price per bit of these memory devices is continually declining. The low cost of memory has fueled the growth and development of the personal computer. As personal computers have become more advanced, they in turn have required faster and more dense memory devices, but with the same low cost of the standard DRAM. Fast page mode DRAMs are the most popular standard DRAM today. In fast page mode operation, a row address strobe (/RAS) is used to latch a row address portion of a multiplexed DRAM address. Multiple occurrences of the column address strobe (/CAS) are then used to latch multiple column addresses to access data within the selected row. On the falling edge of /CAS an address is latched, and the DRAM outputs are enabled. When /CAS transitions high the DRAM outputs are placed in a high impedance state (tri-state). With advances in the production of integrated circuits, the internal circuitry of the DRAM operates faster than ever. This high speed circuitry has allowed for faster page mode cycle times. A problem exists in the reading of a DRAM when the device is operated with minimum fast page mode cycle times. /CAS may be low for as little as 15 nanoseconds, and the data access time from /CAS to valid output data (tCAC) may be up to 15 nanoseconds; therefore, in a worst case scenario there is no time to latch the output data external to the memory device. For devices that operate faster than the specifications require, the data may still only be valid for a few nanoseconds. On a heavily loaded microprocessor memory bus, trying to latch an asynchronous signal that is valid for only a few nanoseconds is very difficult. Even providing a new address every 35 nanoseconds requires large address drivers which create significant amounts of electrical noise within the system. To increase the data throughput of a memory system, it has been common practice to place multiple devices on a common bus. For example, two fast page mode DRAMs may be connected to common address and data buses. One DRAM stores data for odd addresses, and the other for even addresses. The /CAS signal for the odd addresses is turned off (high) when the /CAS signal for the even addresses is turned on (low). This interleaved memory system provides data access at twice the rate of either device alone. If the first /CAS is low for 20 nanoseconds and then high for 20 nanoseconds while the second /CAS goes low, data can be accessed every 20 nanoseconds or 50 megahertz. If the access time from /CAS to data valid is fifteen nanoseconds, the data will be valid for only five nanoseconds at the end of each 20 nanosecond period when both devices are operating in fast page mode. As cycle times are shortened, the data valid period goes to zero.

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead, data is held valid after /CAS goes high until sometime after the next /CAS low pulse occurs, or until /RAS or the output enable (/OE) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can be a complex function of when the column address inputs are valid, when /CAS falls, the state of /OE and when /CAS rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially/CAS) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM manufacturers.

Methods to shorten memory access cycles tend to require additional circuitry, additional control pins and nonstandard device pinouts. The proposed industry standard synchronous DRAM (SDRAM) for example has an additional pin for receiving a system clock signal. Since the system clock is connected to each device in a memory system, it is highly loaded, and it is always toggling circuitry in every device. SDRAMs also have a clock enable pin, a chip select pin and a data mask pin. Other signals which appear to be similar in name to those found on standard DRAMs have dramatically different functionality on a SDRAM. The addition of several control pins has required a deviation in device pinout from standard DRAMs which further complicates design efforts to utilize these new devices. Significant amounts of additional circuitry are required in the SDRAM devices which in turn result in higher device manufacturing costs.

In order for existing computer systems to use an improved device having a nonstandard pinout, those systems must be extensively modified. Additionally, existing computer system memory architectures are designed such that control and address signals may not be able to switch at the frequencies required to operate the new memory device at high speed due to large capacitive loads on the signal lines. The Single In-Line Memory Module (SIMM) provides an example of what has become an industry standard form of packaging memory in a computer system. On a SIMM, all address lines connect to all DRAMs. Further, the row address strobe (/RAS) and the write enable (/WE) are often connected to each DRAM on the SIMM. These lines inherently have high capacitive loads as a result of the number of device inputs driven by them. SIMM devices also typically ground the output enable (/OE) pin making /OE a less attractive candidate for providing extended functionality to the memory devices.

There is a great degree of resistance to any proposed deviations from the standard SIMM design due to the vast number of computers which use SIMMs. Industry's resistance to radical deviations from the standard, and the inability of current systems to accommodate the new memory devices will delay their widespread acceptance. Therefore only limited quantities of devices with radically different architectures will be manufactured initially. This limited manufacture prevents the reduction in cost which typically can be accomplished through the manufacturing improvements and efficiencies associated with a high volume product.

SUMMARY OF THE INVENTION

An integrated circuit memory device with a standard DRAM pinout is designed for high speed data access and for compatibility with existing memory systems. A high speed burst mode of operation is provided where multiple sequential accesses occur following a single column address, and read data is output relative to the /CAS control signal. In the burst mode of operation the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at high speeds. Only one control line per memory chip (/CAS) must toggle at the operating frequency in order to clock the internal address counter and the data input/output latches. The load on each /CAS is typically less than the load on the other control signals (/RAS,/WE and /OE) since each /CAS typically controls only a byte width of the data bus. Internal circuitry of the memory device is largely compatible with existing Extended Data Out (EDO) DRAMs. This similarity allows the two part types to be manufactured on one die with a limited amount of additional circuitry. The ability to switch between a standard non-burst mode and a high speed burst mode allows the device to be used to replace standard devices, and eliminates the need to switch to more complex high speed memory devices. Internal address generation provides for faster data access times than is possible with either fast page mode or EDO DRAMs. This high speed operation eliminates the need to interleave memory devices in order to attain a high data throughput. In contrast to the 50 megahertz interleaved memory system described above, the output data from this device will be valid for approximately 15 nanoseconds significantly easing the design of circuitry required to latch the data from the memory. The device is compatible with existing memory module pinouts including Single In-Line Memory Module (SIMM), Multi-Chip Module (MCM) and Dual In-Line Memory Module (DIMM) designs. This combination of features allows for significant system performance improvements with a minimum of design alterations.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention as well as objects and advantages will be best understood by reference to the appended claims, detailed description of particular embodiments and accompanying drawings where:

FIG. 1 is an electrical schematic diagram of a memory device in accordance with one embodiment of the invention;

FIG. 2 is a table showing linear versus interleaved addressing formats;

FIG. 3 is a pinout of the memory device of FIG. 1;

FIG. 4 is a timing diagram for a method of accessing the device of FIG. 1;

FIG. 5 is a further timing diagram for accessing the device of FIG. 1;

FIG. 6 is an electrical schematic diagram of a Single In-Line Memory Module in accordance with another embodiment of the invention;

FIG. 7 is a front view of a Single In-Line Memory Module designed in accordance with the teachings of this invention; and

FIG. 8 is a table of the pin numbers and signal names of the Single In-Line Memory Module of FIG. 7.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a schematic representation of a sixteen megabit device designed in accordance with the present invention. The device is organized as a 2 Meg×8 burst EDO DRAM having an eight bit data input/output path **10** providing data storage for 2,097,152 bytes of information in the memory array **12**. The device of FIG. 1 has an industry standard pinout for eight bit wide EDO DRAMs. An active-low row address strobe (/RAS) signal **14** is used to latch a first portion of a multiplexed memory address, from address inputs A0 through A10 **16**, in latch **18**. The latched row address **20** is decoded in row decoder **22**. The decoded row address is used to select a row of the memory array **12**. A column address strobe (/CAS) signal **24** is used to latch a second portion of a memory address from address inputs **16** into column address counter **26**. The latched column address **28** is decoded in column address decoder **30**. The decoded column address is used to select a column of the memory array **12**.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path **32** to output latches **34**. Data **10** driven from the burst EDO DRAM may be latched external to the device in synchronization with /CAS after a predetermined number of /CAS cycle delays (latency). For a two cycle latency design, the first /CAS falling edge is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second /CAS falling edge, and remains valid through the third /CAS falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers **34** will continue to drive the data lines without tri-stating the data outputs during /CAS high intervals dependent on the state of the output enable and write enable (/OE and/WE) control lines, thus allowing additional time for the system to latch the output data. Once a row and a column address are selected, additional transitions of the /CAS signal are used to advance the column address within the column address counter in a predetermined sequence. The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the /CAS signal provided that /OE is maintained low, and /WE remains high. The output data signal levels may be driven in accordance with standard CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. FIG. 2 is a table which shows linear and interleaved addressing sequences for burst lengths of 2,4 and 8 cycles. The "V" for starting addresses A1 and A2 in the table represent address values that remain unaltered through the burst sequence. The column address may be advanced with each /CAS transition, each pulse, or multiple of /CAS pulses in the event that more than one data word is read from the array with each column address. When the address is advanced with each transition of the /CAS signal, data is also driven from the part after each transition following the device latency which is then referenced to each edge of the /CAS signal. This allows for a burst access cycle where the highest switching control line (/CAS) toggles only once (high to low or low to high) for each memory cycle. This is in contrast to standard DRAMs which require /CAS to go low and then high for each cycle, and synchronous DRAMs which require a full clock cycle (high and low transitions) for each memory cycle. For maximum compatibility with existing EDO DRAM devices, the invention will be further described in reference to a device designed to latch and advance a column address on falling edges of the /CAS signal.

It may be desirable to latch and increment the column address after the first /CAS falling edge in order to apply both the latched and incremented addresses to the array at the earliest opportunity in an access cycle. For example, a device may be designed to access two data words per cycle (prefetch architecture). The memory array for a prefetch architecture device may be split into odd and even array halves. The column address least significant bit is then used to select between odd and even halves while the other column address bits select a column within each of the array halves. In an interleaved access mode with column address 1, data from columns 0 and 1 would be read and the data from column 1 would be output followed by the data from column 0 in accordance with standard interleaved addressing as described in SDRAM specifications. In a linear access mode column address 1 would be applied to the odd array half, and incremented to address 2 for accessing the even array half to fulfill the two word access. One method of implementing this type of device architecture is to provide a column address incrementing circuit between the column address counter and the even array half. The incrementing circuit would increment the column address only if the initial column address in a burst access cycle is odd, and the address mode is linear. Otherwise the incrementing circuit would pass the column address unaltered. For a design using a prefetch of two data accesses per cycle, the column address would be advanced once for every two active edges of the /CAS signal. Prefetch architectures where more than two data words are accessed are also possible.

Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access may require more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory will approach one access per cycle, but the data out of the memory may be offset by a number of cycles due to the pipeline length and/or the desired latency from/CAS.

In the burst access memory device, each new column address from the column address counter is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16. This burst sequence of data will continue for each /CAS falling edge until a predetermined number of data accesses equal to the burst length has occurred. A /CAS falling edge received after the last burst address has been generated will latch another column address from the address inputs 16 and a new burst sequence will begin. Read data is latched and output with each falling edge of /CAS after the first /CAS latency.

For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the /CAS signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is preferred. Additional input data words for storage at incremented column address locations are latched by /CAS on successive/CAS pulses. Input data from the input latches 34 is passed along data path 32 to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes will occur without the requirement of additional column addresses being provided on the address lines 16. After the predetermined number of burst writes has occurred, a subsequent /CAS pulse will latch a new beginning column address, and another burst read or write access will begin.

The memory device of FIG. 1 may include the option of switching between burst EDO and standard EDO modes of operation. In this case, the write enable signal /WE 36 may be used at the row address latch time (/RAS falling, /CAS high) to determine whether memory accesses for that row will be burst or page mode cycles. If /WE is low when /RAS falls, burst access cycles are selected. If /WE is high at /RAS falling, standard extended data out (EDO) page mode cycles are selected. Both the burst and EDO page mode cycles allow for increased memory device operating frequencies by not requiring the data output drivers 34 to place the data lines 10 in a high impedance state between data read cycles while /RAS is low. DRAM control circuitry 38, in addition to performing standard DRAM control functions, controls the I/O circuitry 34 and the column address counter/latch 26 in accordance with the mode selected by /WE when /RAS falls. In a burst mode only DRAM, or in a device designed with an alternate method of switching between burst and non-burst access cycles, the state of /WE when /RAS falls may be used to switch between other possible modes of operation such as interleaved versus linear addressing modes.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by/CAS. /WE low at the column address latch time selects a burst write access. /WE high at the column address latch time selects a burst read access. The level of the /WE signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on /WE within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. Transitions of the /WE signal may be locked out during critical timing periods within an access cycle in order to reduce the possibility of triggering a false write cycle. After the critical timing period the state of /WE will determine whether a burst access continues, is initiated, or is terminated. Termination of a burst access resets the burst length counter and places the DRAM in a state to receive another burst access command. Both /RAS and /CAS going high during a burst access will also terminate the burst access cycle placing the data drivers in a high impedance output state, and resetting the burst length counter. Read data may remain valid at the device outputs if /RAS alone goes high while /CAS is active for compatibility with hidden refresh cycles, otherwise /RAS high alone may be used to terminate a burst access. A minimum write enable pulse width is only required when it is desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses. In the case of burst reads, /WE will transition from high to low to terminate a first burst read, and then /WE will transition back high prior to the next falling edge of /CAS in order to specify a new burst read cycle. For burst writes, /WE would transition high to terminate a current burst write access, then back low prior to the next falling edge of /CAS to initiate another burst write access.

A basic implementation of the device of FIG. 1 may include a fixed burst length of 4, a fixed /CAS latency of 2 and a fixed interleaved sequence of burst addresses. This basic implementation requires very little additional circuitry to the standard EDO page mode DRAM, and may be mass produced to provide the functions of both the standard EDO page mode and burst EDO DRAMs. This device also allows

for the output enable pin (/OE) to be grounded for compatibility with many SIMM module designs. When not disabled (tied to ground), /OE is an asynchronous control which will prevent data from being driven from the part in a read cycle if it is inactive (high) prior to /CAS falling and remains inactive beyond /CAS rising. If these setup and hold conditions are not met, then the read data may be driven for a portion of the read cycle. It is possible to synchronize the /OE signal with/CAS, however this would typically increase the /CAS to data valid delay time and does not allow for the read data to be disabled prior to /RAS high without an additional /CAS low pulse which would otherwise be unnecessary. In a preferred embodiment, if /OE transitions high at any time during a read cycle the outputs will remain in a high impedance state until the next falling edge of /CAS despite further transitions of the /OE signal.

Programmability of the burst length, /CAS latency and address sequences may be accomplished through the use of a mode register **40** which latches the state of one or more of the address input signals **16** or data signals **10** upon receipt of a write-/CAS-before-/RAS (WCBR) programming cycle. In such a device, outputs **44** from the mode register control the required circuits on the DRAM. Burst length options of 2, 4, 8 and full page as well as /CAS latencies of 1, 2 and 3 may be provided. Other Burst length and latency options may be provided as the operating speeds of the device increase, and computer architectures evolve. The device of FIG. 1 includes programmability of the address sequence by latching the state of the least significant address bit during a WCBR cycle. The burst length and/CAS latency for this particular embodiment are fixed. Other possible alterations in the feature sets of this DRAM include having a fixed burst mode only, selecting between standard fast page mode (non-EDO) and burst mode, and using the output enable pin (/OE) **42** in combination with /RAS to select between modes of operation. Also, a WCBR refresh cycle could be used to select the mode of operation rather than a control signal in combination with/RAS. A more complex memory device may provide additional modes of operation such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of /WE and /OE at /RAS falling time. One mode from a similar set of modes may be selected through the use of a WCBR cycle using multiple address or data lines to encode the desired mode. Alternately, a device with multiple modes of operation may have wire bond locations, or programmable fuses which may be used to program the mode of operation of the device.

A preferred embodiment of a sixteen bit wide burst EDO mode DRAM designed in accordance with the teachings of this invention has two column address strobe input pins /CASH and /CASL. For read cycles only /CASL needs to toggle. /CASH is may be high or may toggle with /CASL during burst read cycles, all sixteen data bits will be driven out of part during a read cycle even if /CASH remains inactive. In a typical system application, a microprocessor will read all data bits on a data bus in each read cycle, but may only write certain bytes of data in a write cycle. Allowing one of the /CAS control signals to remain static during read cycles helps to reduce overall power consumption and noise within the system. For burst write access cycles, each of the /CAS signals (CASH and /CASL) acts as a write enable for an eight bit width of the data. All sixteen data inputs will be latched when the first of the /CAS signals transitions low. If only one /CAS signal transitions low, then the eight bits of data associated with the /CAS that remained high will not be stored in the memory.

The present invention has been described with reference to several preferred embodiments. Just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including x1, x4, x8 and x16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the memory device of the present invention may take the form of many different memory organizations. It is believed that one who is skilled in the art of integrated circuit memory design can, with the aide of this specification design a variety of memory devices which do not depart from the spirit of this invention. It is therefore believed that detailed descriptions of the various memory device organizations applicable to this invention are not necessary.

FIG. 3 shows a preferred pinout for the device of FIG. 1. It should be noted that the pinout for this new burst EDO memory device is identical to the pinout for a standard EDO DRAM. The common pinout allows this new device to be used in existing memory designs with minimum design changes. The common pinout also allows for ease of new designs by those of skill in the art who are familiar with the standard EDO DRAM pinout. Variations of the described invention which maintain the standard EDO DRAM pinout include driving the /CAS pin with a system clock signal to synchronize data access of the memory device with the system clock. For this embodiment, it may be desirable to use the first /CAS active edge after/RAS falls to latch the row address, a later edge may be used to latch the first column address of a burst access cycle. After row and column addresses are latched within the device, the address may be incremented internally to provide burst access cycles in synchronization with the system clock. Other pin function alternatives include driving the burst address incrementing signal on the /OE pin since the part does not require a data output disable function on this pin. Other alternate uses of the/OE pin also allow the device to maintain the standard EDO pinout, but provide increased functionality such as burst mode access. The /OE pin may be used to signal the presence of a valid column starting address, or to terminate a burst access. Each of these embodiments provides for a high speed burst access memory device which may be used in current memory systems with a minimum amount of redesign.

FIG. 4 is a timing diagram for performing a burst read followed by a burst write of the device of FIG. 1. In FIG. 4, a row address is latched by the /RAS signal. /WE is low when /RAS falls for an embodiment of the design where the state of the /WE pin is used to specify a burst access cycle at /RAS time. Next, /CAS is driven low with /WE high to initiate a burst read access, and the column address is latched. The data out signals (DQ's) are not driven in the first /CAS cycle. On the second falling edge of the /CAS signal, the internal address generation circuitry advances the column address and begins another access of the array, and the first data out is driven from the device after a /CAS to data access time (tCAC). Additional burst access cycles continue, for a device with a specified burst length of four, until the fifth falling edge of /CAS which latches a new column address for a new burst read access. /WE falling in the fifth /CAS cycle terminates the burst access, and initializes the device for additional burst accesses. The sixth falling edge of /CAS with /WE low is used to latch a new burst address, latch input data and begin a burst write access of the device. Additional data values are latched on successive /CAS falling edges until /RAS rises to terminate the burst access.

FIG. 5 is a timing diagram depicting burst write access cycles followed by burst read cycles. As in FIG. 4, the /RAS

signal is used to latch the row address. The first /CAS falling edge in combination with /WE low begins a burst write access with the first data being latched. Additional data values are latched with successive /CAS falling edges, and the memory address is advanced internal to the device in either an interleaved or sequential manner. On the fifth /CAS falling edge a new column address and associated write data are latched. The burst write access cycles continue until the /WE signal goes high in the sixth /CAS cycle. The transition of the /WE signal terminates the burst write access. The seventh/CAS low transition latches a new column address and begins a burst read access (/WE is high). The burst read continues until /RAS rises terminating the burst cycles.

It should be noted from FIGS. 4 and 5. that for burst read cycles the data remains valid on the device outputs as long as the /OE pin is low, except for brief periods of data transition. The output enable signal, when in an inactive state (high) during a read cycle, is operative to place the DQ output node in a high impedance state. The burst access memory is operative for both read and write burst accesses while the output enable signal is in an active state. Also, since the /WE pin is low prior to or when/CAS falls, the data input/output lines are not driven from the part during write cycles, and the /OE pin is a "don't care". Only the /CAS signal and the data signals toggle at relatively high frequency, and no control signals other than /CAS are required to be in an active or inactive state for one /CAS cycle time or less. This is in contrast to SDRAMs which often require row address strobes, column address strobes, data mask, and read/write control signals to be valid for one clock cycle or less for various device functions. Typical DRAMs also allow for the column address to propagate through to the array to begin a data access prior to /CAS falling. This is done to provide fast data access from /CAS falling if the address has been valid for a sufficient period of time prior to /CAS falling for the data to have been accessed from the array. In these designs an address transition detection circuit is used to restart the memory access if the column address changes prior to /CAS falling. This method actually requires additional time for performing a memory access since it must allow for a period of time at the beginning of each memory cycle after the last address transition to prepare for a new column address. Changes in the column address just prior to /CAS falling may increase the access time by approximately five nanoseconds. An embodiment of the present invention will not allow the column address to propagate through to the array until after /CAS has fallen. This eliminates the need for address transition detection circuitry, and allows for a fixed array access relative to/CAS.

FIG. 6 is a schematic representation of a single in-line memory module (SIMM) designed in accordance with the present invention. The SIMM has a standard SIMM module pinout for physical compatibility with existing systems and sockets. Functional compatibility with EDO page mode SIMMs is maintained when each of the 2 Meg×8 memory devices 10, 12, 14 and 16 are operated in an EDO page mode. Each of the /CAS signals 18, 20, 22 and 24 control one byte width of the 32 bit data bus 26, 28, 30 and 32. A /RAS 34 signal is used to latch a row address in each of the memory devices, and is used in combination with /WE 36 to select between page mode and burst mode access cycles. Address signals 38 provide a multiplexed row and column address to each memory device on the SIMM. In burst mode, only active /CAS control lines are required to toggle at the operating frequency of the device, or at hair the frequency if each edge of the/CAS signal is used as described above. The data lines are required to be switchable at half of the frequency of the /CAS lines or at the same frequency, and the other control and address signals switch at lower frequencies than /CAS and the data lines. As shown in FIG. 6, each /CAS signal and each data line is connected to a single memory device allowing for higher frequency switching than the other control and address signals. Each of the memory devices 10, 12, 14 and 16 is designed in accordance with the present invention allowing for a burst mode of operation providing internal address generation for sequential or interleaved data access from multiple memory address locations with timing relative to the /CAS control lines after a first row and column address are latched.

FIG. 7 shows a front view of another SIMM designed in accordance with the present invention. Each device on the SIMM is a 4 Megabit DRAM organized as 1 Meg×4. In this configuration, a single /CAS controls two memory devices to provide access to a byte width of the data bus. The eight devices shown form a 4 Megabyte SIMM in a 32 bit width. For an 8 Megabyte SIMM in a 32 bit width, there are eight additional devices on the back side (not shown).

FIG. 8 shows a preferred pinout for a memory module designed in accordance with the device of FIG. 7. This pinout is compatible with pinouts for Fast Page Mode SIMMs and EDO SIMMs. A presence detect pin is provided for indication of EDO operation on pin 66, and in accordance with standard EDO part types, an /OE input is provided on pin 46.

Alternate embodiments of the SIMM modules of FIGS. 5,6 and 7 include the use of two /RAS signals with each controlling a sixteen bit width of the data bus in accordance with standard SIMM module pinouts. Four more 2M×8 EDO Burst Mode DRAMs may be added to the device of FIG. 6 to provide for a 4M×32 bit SIMM. Sixteen bit wide DRAMs may also be used, these will typically have two /CAS signals each of which controls an eight bit data width. The incorporation of parity bits, or error detection and correction circuitry provide other possible SIMM module configurations. Methods of performing error detection and/ or correction are well known to those of skill in the art, and detailed descriptions of such circuits are not provided in this application. Additional SIMM designs using the novel memory device of the present invention may be designed by one of skill in the art with the aid of this specification. The invention has been described with reference to SIMM designs, but is not limited to SIMMs. The invention is equally applicable to other types of memory modules including Dual In-Line Memory Modules (DIMMs) and Multi-Chip Modules (MCMs).

What is claimed is:

1. A memory device having an array of memory elements, and an output node for driving data from the memory device, the memory device comprising:

an address generation circuit to provide a plurality of addresses to the array for accessing the array in a burst mode; and

an output enable pin adapted to receive an output enable signal, wherein the output enable signal when in an inactive state during a read cycle is operative to place the output node in a high impedance state, and the memory device is operative for both read and write burst accesses while the output enable signal is in an active state.

2. The memory device of claim 1 wherein the address generation circuit is adapted to receive at least a first portion of an address from a source external to the memory device

in response to a transition of an address latch signal, and further adapted to advance the address in a predetermined address sequence in response to a subsequent transition of the address latch signal.

3. The memory device of claim 2 further comprising:

an output buffer circuitry adapted to switch between a logic low data value and a logic high data value in response to a single transition of the address latch signal.

4. The memory device of claim 1 further comprising:

output buffer circuitry adapted to drive data from the memory device only after a plurality of transitions of the address latch signal in a burst read access.

5. The memory device of claim 1 further comprising output driver circuitry coupled to the output enable pin and the output node for placing the output node in a high impedance state in response to the output enable pin.

6. The memory device of claim 1, wherein:

said output buffer circuitry is further adapted to drive a logic low data value from the device after a falling edge of the address latch signal and then to drive a logic high data value from the device after a rising edge of the address latch signal.

7. A memory device having an output enable pin for enabling data to be driven from the memory device and a data output node for driving data from the memory device, comprising:

means for reading data from the memory device in a burst mode in response to an address strobe signal; and

means for placing the data output node in a high impedance state in response to a transition of an output enable signal on the output enable pin, and for maintaining the data output node in a high impedance state despite additional transitions of the output enable signal prior to an additional transition of the address strobe signal.

8. The memory device of claim 7, further comprising:

a write enable node coupled to the means for reading, wherein a transition of a write enable signal received on the write enable node terminates a burst access of the memory device.

9. The memory device of claim 7, wherein the means for reading comprise:

an address latch node for receiving an address latch signal;

an address latch for receiving at least a portion of a first memory address and an array of memory elements; and

an address generating circuit responsive to the address latch signal and to an output of the address latch for generating a second memory address, wherein the second memory address is used to access the array.

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United States Patent [19]

Zagar et al.

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[54] **SYNCHRONOUS BURST EXTENDED DATA OUT DRAM**

[75] Inventors: **Paul S. Zagar**; **Troy A. Manning**; **Todd Merritt**, all of Boise, Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

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Related U.S. Application Data

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[51] **Int. Cl.**^{6} **G11C 8/00**

[52] **U.S. Cl.** **365/233**; 365/233.5

[58] **Field of Search** 365/233.5, 238.5, 365/239, 235, 236

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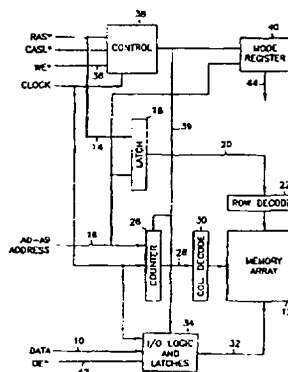
Primary Examiner—Tan T. Nguyen

Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

An integrated circuit memory device is described which can operate at high data speeds. The memory device can either store or retrieve data from the memory in a burst access operation. The burst operations latches a memory address from external address lines and internally generates additioned memory addresses. A clock signed is provided to synchronize the burst operations. The clock signed is independent of an address latch signal used to latch an external address.

2 Claims, 7 Drawing Sheets



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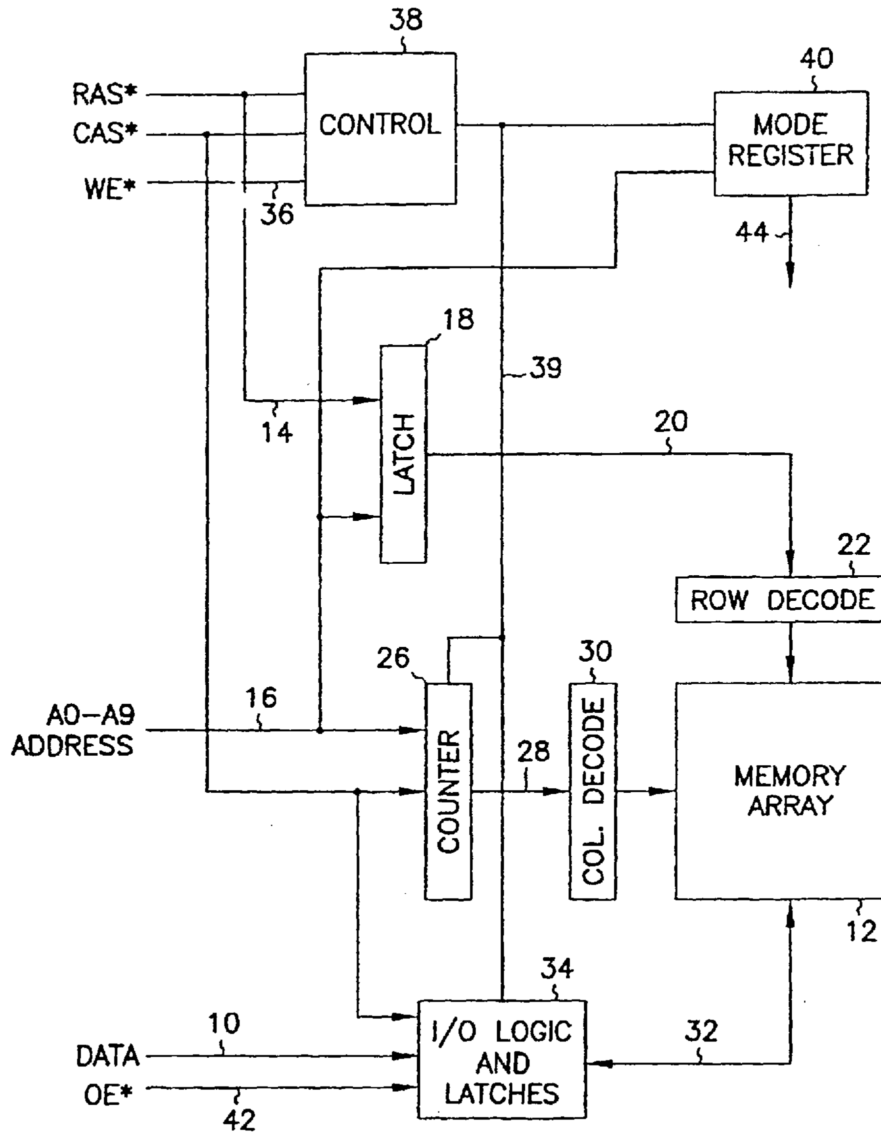

FIG. 1

Burst Length	Starting Column Address A_2	A_1	A_0	Linear	Interleave
2	V	V	0	0-1	0-1
	V	V	1	1-0	1-0
4	V	0	0	0-1-2-3	0-1-2-3
	V	0	1	1-2-3-0	1-0-3-2
	V	1	0	2-3-0-1	2-3-0-1
	V	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

FIG. 2

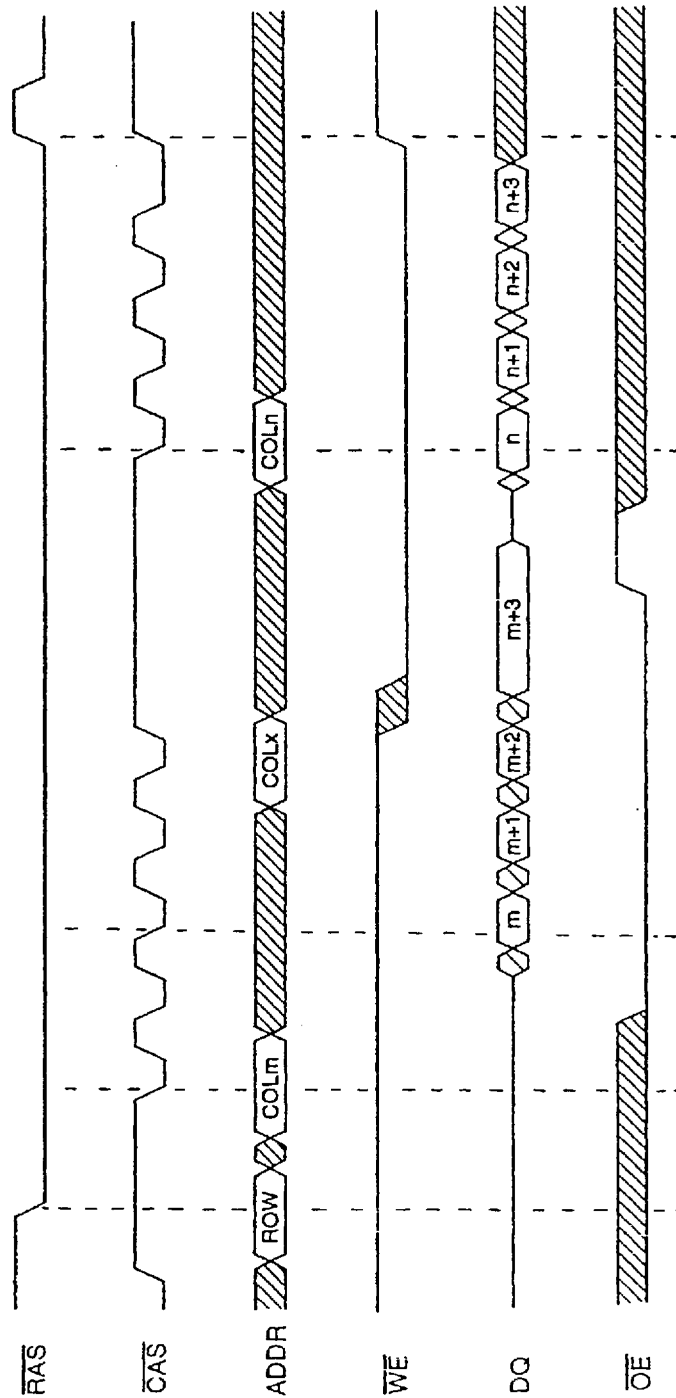

FIG. 3

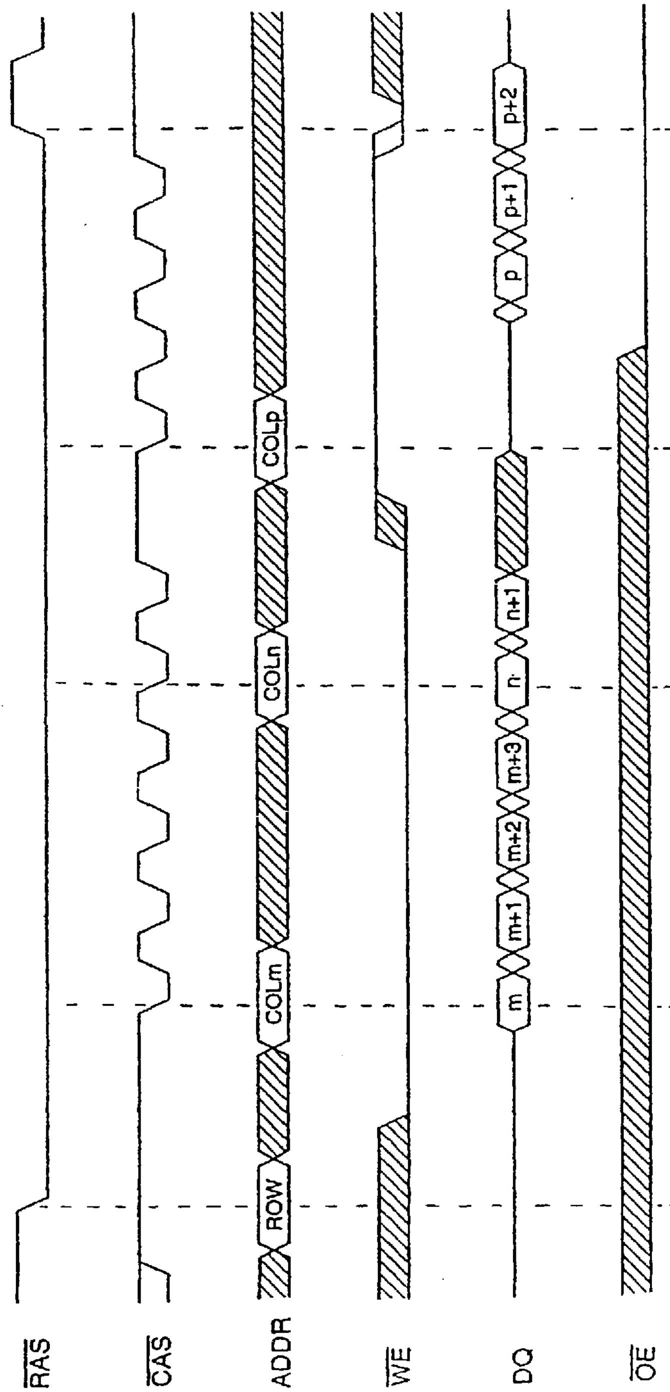

FIG. 4

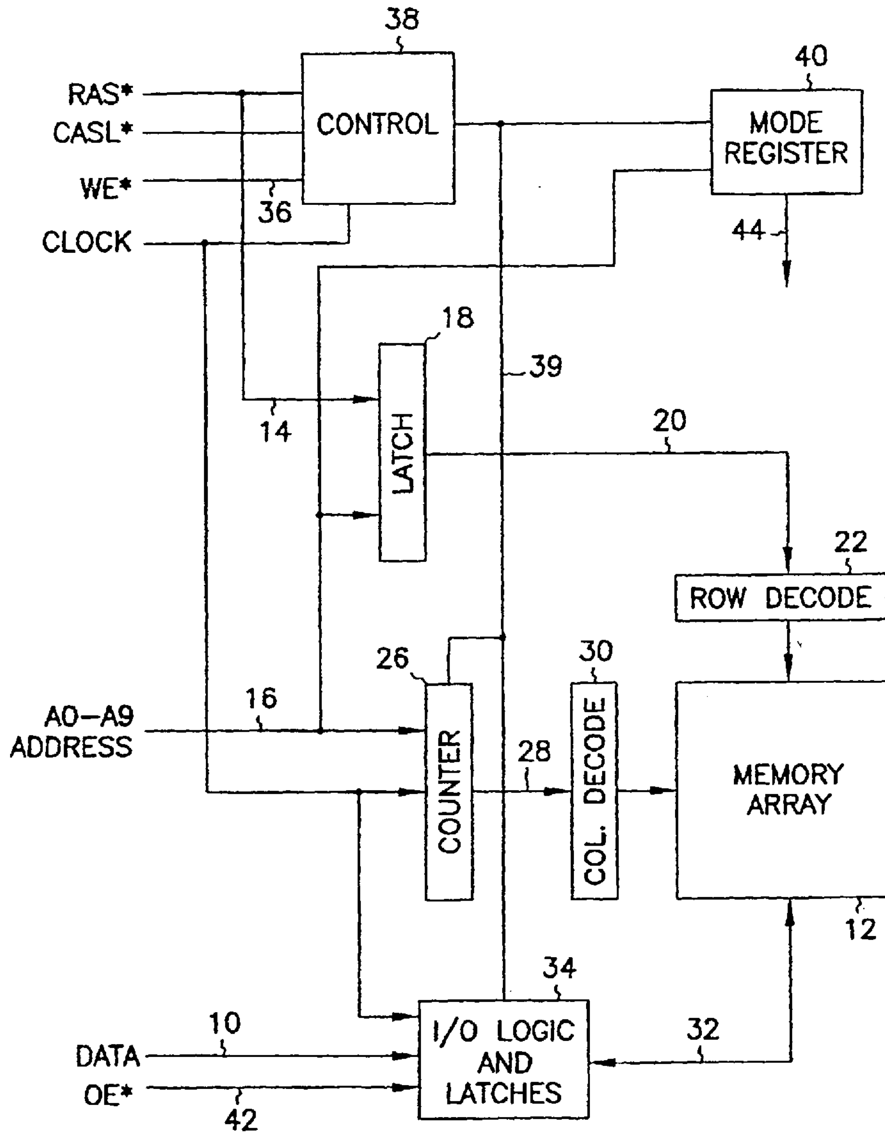

FIG. 5

RX-0999

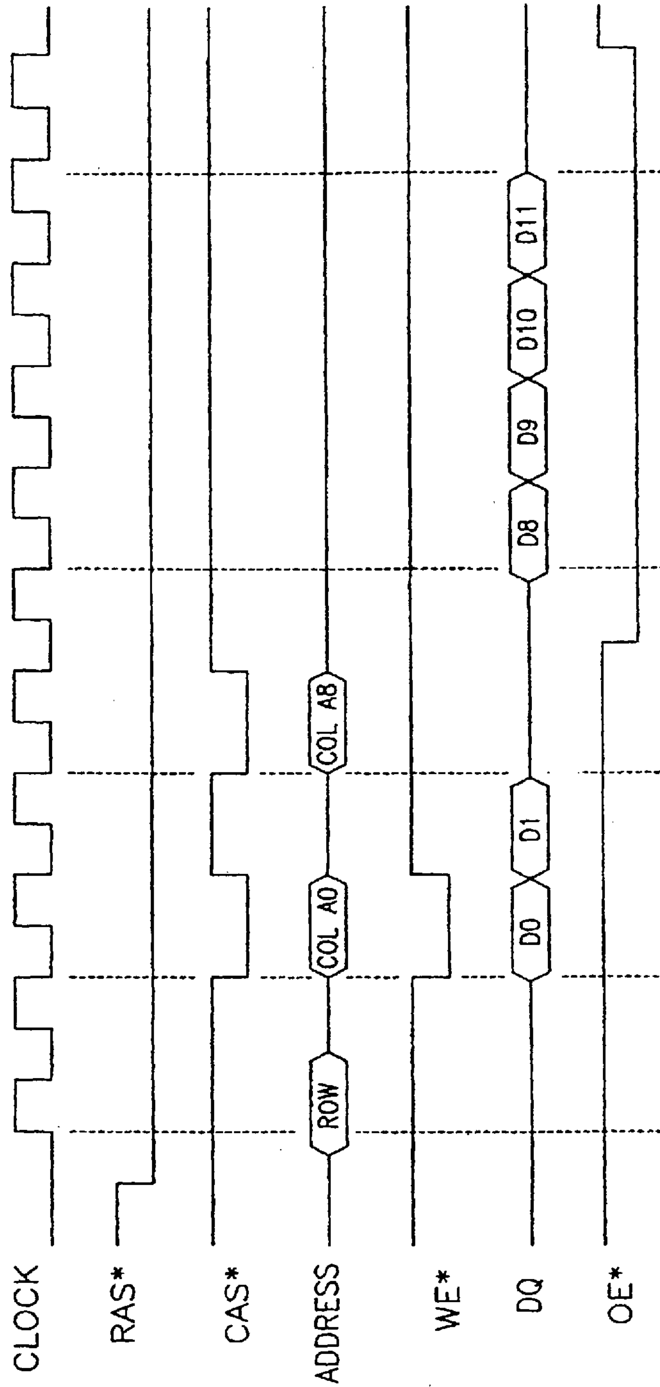

FIG. 6

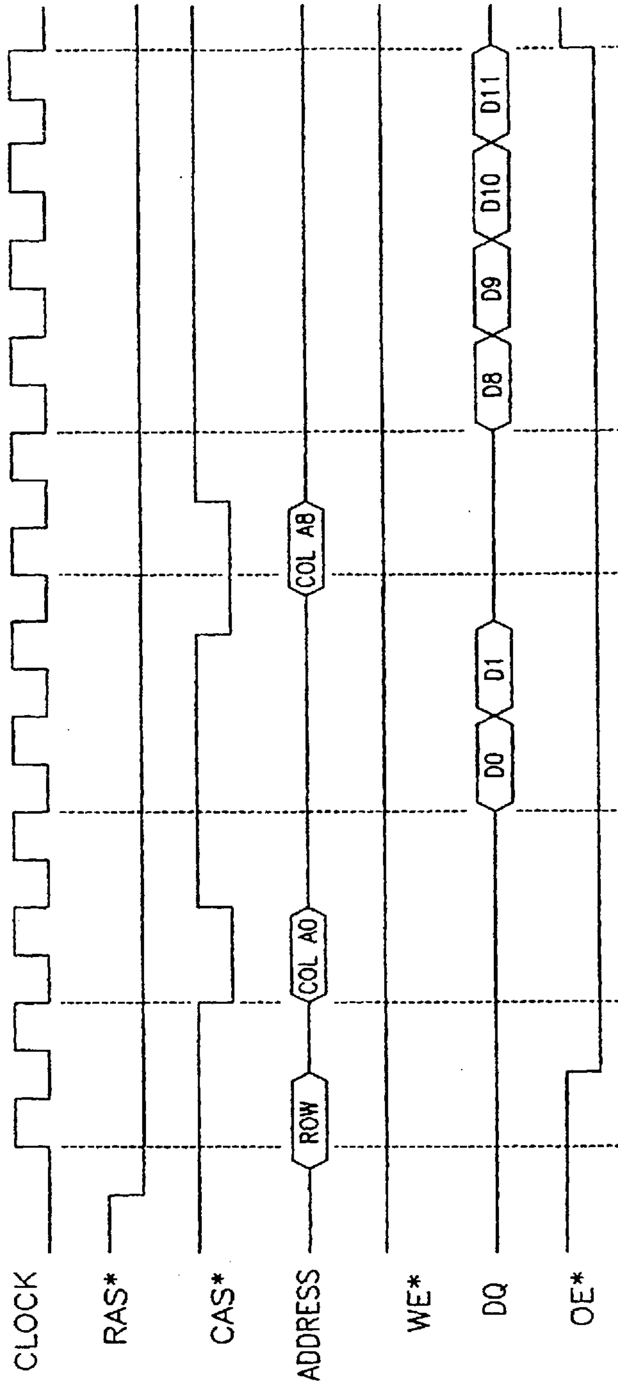

FIG. 7

SYNCHRONOUS BURST EXTENDED DATA OUT DRAM

This application is a continuation-in-part of U.S. application Ser. No. 08/370,761, filed of Dec. 23, 1994, and entitled "Burst EDO Memory Device now U.S. Pat. No. 5,526,320," which is incorporated herein by reference.

FIELD OF THE INVENTION

This invention relates to synchronous memory devices and in particular to memory device architectures designed to provide high density data storage with high speed read and write access cycles.

BACKGROUND OF THE INVENTION

Dynamic Random Access Memory devices (DRAMs) are among the highest volume and most complex integrated circuits manufactured today. Except for their high volume production, the state of the art manufacturing requirements of these devices would cause them to be exorbitantly priced. Yet, due to efficiencies associated with high volume production, the price per bit of these memory devices is continually declining. The low cost of memory has fueled the growth and development of the personal computer. As personal computers have become more advanced, they in turn have required faster and more dense memory devices, but with the same low cost of the standard DRAM. Fast page mode DRAMs are the most popular standard DRAM today. In fast page mode operation, a row address strobe (RAS*) is used to latch a row address portion of a multiplexed DRAM address. Multiple occurrences of the column address strobe (CAS*) are then used to latch multiple column addresses to access data within the selected row. On the falling edge of CAS* an address is latched, and the DRAM outputs are enabled. When CAS* transitions high the DRAM outputs are placed in a high impedance state (tri-state). With advances in the production of integrated circuits, the internal circuitry of the DRAM operates faster than ever. This high speed circuitry has allowed for faster page mode cycle times. A problem exists in the reading of a DRAM when the device is operated with minimum fast page mode cycle times. CAS* may be low for as little as 15 nanoseconds, and the data access time from CAS* to valid output data (t_{CAC}) may be up to 15 nanoseconds; therefore, in a worst case scenario there is no time to latch the output data external to the memory device. For devices that operate faster than the specifications require, the data may still only be valid for a few nanoseconds. On a heavily loaded microprocessor memory bus, trying to latch an asynchronous signal that is valid for only a few nanoseconds is very difficult. Even providing a new address every 35 nanoseconds requires large address drivers which create significant amounts of electrical noise within the system. To increase the data throughput of a memory system, it has been common practice to place multiple devices on a common bus. For example, two fast page mode DRAMs may be connected to common address and data buses. One DRAM stores data for odd addresses, and the other for even addresses. The CAS* signal for the odd addresses is mined off (high) when the CAS* signal for the even addresses is mined on (low). This interleaved memory system provides data access at twice the rate of either device alone. If the first CAS* is low for 20 nanoseconds and then high for 20 nanoseconds while the second CAS* goes low, data can be accessed every 20 nanoseconds or 50 megahertz. If the access time from CAS* to data valid is fifteen nanoseconds, the data will be valid for only five nanoseconds at the end of each 20-nanosecond period when both devices are operating in fast page mode. As cycle times are shortened, the data valid period goes to zero.

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead, data is held valid after CAS* goes high until sometime after the next CAS* low pulse occurs, or until RAS* or the output enable (OE*) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can be a complex function of when the column address inputs are valid, when CAS* falls, the state of OE* and when CAS* rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially CAS*) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM manufacturers.

Yet another type of memory device is a burst EDO memory which adds the ability to address one column of a memory array and then automatically address additional columns in a pre-determined manner without providing the additional column addresses on external address lines. These memory devices use a column access input to access the memory array columns. For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a memory device which can operate at high data rates in a clocked or synchronous manner.

SUMMARY OF THE INVENTION

The above mentioned problems with memory devices and other problems are addressed by the present invention and which will be understood by reading and studying the following specification. A memory device is described which uses a clock signal to synchronize a burst access memory.

In particular one embodiment of the present invention is a memory device comprising a plurality of addressable memory elements, and addressing circuitry. The addressing circuitry is adapted to receive a first memory element address in response to a transition of a clock signal and an address latch signal, and further adapted to generate a second memory element address in response to a subsequent transition of the clock signal.

In another embodiment, a synchronous memory device is described. This memory comprises a memory array having a plurality of addressable memory elements, a plurality of address inputs for receiving memory element addresses, and an address latch input for receiving an address latch signal. The memory also includes an address latch for receiving a first memory element address in response to a transition of a clock signal and the address latch signal, and an address generation circuit responsive to successive transitions of the clock signal and to the first memory element address for generating additional memory element addresses.

In yet another embodiment, a method of accessing a memory device is described. The method comprises the

steps of receiving a first memory element address in response to a transition of a clock signal and an address latch signal, and generating additional memory element addresses in response to subsequent transitions of the clock signal.

In still another embodiment, a method of burst accessing a memory device is described. The method comprising the steps of receiving a first memory element address in response to a transition of a clock signal and an address latch signal, accessing first memory elements having the first memory element address, generating additional memory element addresses in response to subsequent transitions of the clock signal, and accessing additional memory element having the additional memory element addresses.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a memory device incorporating burst access;

FIG. 2 illustrates linear and interleaved addressing sequences for the device of FIG. 1;

FIG. 3 is a timing diagram of a burst read followed by a burst write of the device of FIG. 1;

FIG. 4 is a timing diagram of a burst write followed by a burst read of the device of FIG. 1;

FIG. 5 is a block diagram of a memory device incorporating the feature of the present invention;

FIG. 6 is a timing diagram of the operation of the device of FIG. 5; and

FIG. 7 is another timing diagram of the operation of the device of FIG. 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present inventions is defined only by the appended claims.

FIG. 1 is a schematic representation of a sixteen megabit device designed to operate in a burst access mode. The device is organized as a 2 Meg×8 burst EDO DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array 12. An active-low row address strobe (RAS*) signal 14 is used to latch a first portion of a multiplexed memory address, from address inputs AO through A10 16, in latch 18. The latched row address 20 is decoded in row decoder 22. The decoded row address is used to select a row of the memory array 12. An active-low column address strobe (CAS*) signal 24 is used to latch a second portion of a memory address from address inputs 16 into column address counter 26. The latched column address 28 is decoded in column address decoder 30. The decoded column address is used to select a column of the memory array 12.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 32 to output latches 34. Data 10 driven from the burst EDO DRAM may be latched external to the device in synchronization with a clock signal after a predetermined number of clock cycle delays (latency). For a two cycle latency design, the first clock rising edge during a CAS* cycle is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second clock falling edge, and remains valid through the third clock falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during clock high intervals dependent on the state of the output enable and write enable (OE* and WE*) control lines, thus allowing additional time for the system to latch the output data. Once a row and a column address are selected, additional transitions of the clock signal are used to advance the column address within the column address counter in a predetermined sequence. The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the clock signal provided that OE* is maintained low, and WE* remains high. The output data signal levels may be driven in accordance with standard CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. FIG. 2 is a table which shows linear and interleaved addressing sequences for burst lengths of 2, 4 and 8 cycles. The "V" for starting addresses A1 and A2 in the table represent address values that remain unaltered through the burst sequence. The column address may be advanced with each clock transition, or each pulse. When the address is advanced with each transition of the clock signal, data is also driven from the part after each transition following the device latency which is then referenced to each edge of the clock signal. This allows for a burst access cycle where the clock toggles only once (high to low or low to high) for each memory cycle. This is in contrast to standard DRAMs which require CAS* to go low and then high for each cycle, and synchronous DRAMs which require a full clock cycle (high and low transitions) for each memory cycle.

It may be desirable to latch and increment the column address after the first clock falling edge in order to apply both the latched and incremented addresses to the array at the earliest opportunity in an access cycle. For example, a device may be designed to access two data words per cycle (prefetch architecture). The memory array for a prefetch architecture device may be split into odd and even array halves. The column address least significant bit is then used to select between odd and even halves while the other column address bits select a column within each of the array halves. In an interleaved access mode with column address 1, data from columns 0 and 1 would be read and the data from column 1 would be output followed by the data from column 0 in accordance with standard interleaved addressing as described in SDRAM specifications. In a linear access mode column address 1 would be applied to the odd array half, and incremented to address 2 for accessing the even array half to fulfill the two word access. One method of implementing this type of device architecture is to provide a column address incrementing circuit between the column address counter and the even array half. The incrementing circuit would increment the column address only if the initial column address in a burst access cycle is odd, and the address mode is linear. Otherwise the incrementing circuit would pass the column address unaltered. For a design using

a prefetch of two data accesses per cycle, the column address would be advanced once for every two active edges of the clock signal. Prefetch architectures where more than two data words are accessed are also possible.

In the burst access memory device, each new column address from the column address counter is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16. This burst sequence of data will continue for each clock falling edge until a predetermined number of data accesses equal to the burst length has occurred. A clock falling edge received after the last burst address has been generated will latch another column address from the address inputs 16 if CAS* is low and a new burst sequence will begin. Read data is latched and output with each falling edge of clock after the first clock latency. For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and cola addresses is latched with the clock signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is preferred. Additional input data words for storage at incremented column address locations are latched by clock on successive clock pulses. Input data from the input latches 34 is passed along data path 32 to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes will occur without the requirement of additional column addresses being provided on the address lines 16. After the predetermined number of burst writes has occurred, a subsequent CAS* with a clock pulse will latch a new beginning column address, and another burst read or write access will begin.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by clock. WE* low at the column address latch time selects a burst write access. WE* high at the column address latch time selects a burst read access. The level of the WE* signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. Transitions of the WE* signal may be locked out during critical timing periods within an access cycle in order to reduce the possibility of triggering a false write cycle. After the critical timing period, the state of WE* will determine whether a burst access continues, is initiated, or is terminated. Termination of a burst access resets the burst length counter and places the DRAM in a state to receive another burst access command. Both RAS* and CAS* going high during a burst access will also terminate the burst access cycle placing the data drivers in a high impedance output state, and resetting the burst length counter. A minimum write enable pulse width is only required when it is desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses. In the case of burst reads, WE* will transition from high to low to terminate a first burst read, and then WE* will transition back high prior to the next falling edge of CAS* in order to specify a new burst read cycle. For burst writes, WE* would transition high to terminate a current burst write access, then

back low prior to the next falling edge of CAS* to initiate another burst write access.

A basic implementation of the device of FIG. 1 may include a fixed burst length of 4, a fixed clock latency of 2 and a fixed interleaved sequence of burst addresses. This basic implementation requires very little additional circuitry to the standard EDO page mode DRAM, and may be mass produced to provide the functions of both the standard EDO page mode and burst EDO DRAMs. This device also allows for the output enable pin (OE*) to be grounded for compatibility with many SIMM module designs. When not disabled (tied to ground), OE* is an asynchronous control which will prevent data from being driven from the part in a read cycle if it is inactive (high) prior to CAS* falling and remains inactive beyond CAS* rising. If these setup and hold conditions are not met, then the read data may be driven for a portion of the read cycle. In a preferred embodiment, if OE* transitions high at any time during a read cycle the outputs will remain in a high impedance state until the next falling edge of CAS* despite further transitions of the OE* signal.

The burst access memory has been described with reference to several embodiments. Just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including x1, x4, x8 and x16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the burst access memory device may take the form of many different memory organizations.

FIG. 3 is a timing diagram for performing a burst read followed by a burst write of the device of FIG. 1. In FIG. 3, a row address is latched by the RAS* signal. WE* is low when RAS* falls for an embodiment of the design where the state of the WE* pin is used to specify a burst access cycle at RAS* time. Next, CAS* is driven low with WE* high to initiate a burst read access, and the column address is latched. The data out signals (DQ's) are not driven in the first CAS* cycle. On the second falling edge of the CAS* signal, the internal address generation circuitry advances the column address and begins another access of the array, and the first data out is driven from the device after a CAS* to data access time (tCAC). Additional burst access cycles continue, for a device with a specified burst length of four, until the fifth falling edge of CAS* which latches a new column address for a new burst read access. WE* falling in the fifth CAS* cycle terminates the burst access, and initializes the device for additional burst accesses. The sixth falling edge of CAS* with WE* low is used to latch a new burst address, latch input data and begin a burst write access of the device. Additional data values are latched on successive CAS* falling edges until RAS* rises to terminate the burst access.

FIG. 4 is a timing diagram depicting burst write access cycles followed by burst read cycles. As in FIG. 3, the RAS* signal is used to latch the row address. The first CAS* falling edge in combination with WE* low begins a burst write access with the first data being latched. Additional data values are latched with successive CAS* falling edges, and the memory address is advanced internal to the device in either an interleaved or sequential manner. On the fifth CAS* falling edge a new column address and associated write data are latched. The burst write access cycles continue until the WE* signal goes high in the sixth-CAS* cycle. The transition of the WE* signal terminates the burst write access. The seventh CAS* low transition latches a new column address and begins a burst read access (WE* is high). The burst read continues until RAS* rises terminating the burst cycles.

It should be noted from FIGS. 3 and 4, that for burst read cycles the data remains valid on the device outputs as long as the OE* pin is low, except for brief periods of data transition. Also, since the WE* pin is low prior to or when

CAS* falls, the data input/output lines are not driven from the part during write cycles, and the OE* pin is a "don't care". Only the clock signal, CAS* and the data signals toggle at relatively high frequency, and no control signals are required to be in an active or inactive state for one clock cycle time or less. This is in contrast to SDRAMs which often require row address strobes, column address strobes, data mask, and read/write control signals to be valid for one clock cycle or less for various device functions.

Synchronous BEDO

A BEDO memory device has been described above as using the CAS* input to burst read or write data. It will be recognized that CAS* is a loaded line and cannot be operated efficiently at high frequencies. To reduce access time, an external clock input can be added to operate the BEDO memory in a synchronous, or clocked, mode, as illustrated in FIG. 5. In operation, the internal column address is advanced by the burst counter on the rising edge of the clock signal and the new column is accessed on the falling edge of the clock signal. The burst access memory of the present invention includes the features, options, and configurations of the memory shown in FIG. 1 and described above.

The operation of a synchronous BEDO can be understood in more detail with reference to the timing diagram of FIG. 6. An external memory row address is read on the first clock signal rising edge following the falling edge of RAS*. An external column address is likewise loaded into the burst counter on the first clock signal rising edge following the falling edge of CAS*. The WE* input is also examined on the rising edge of the clock signal.

As shown in the timing diagram, WE* is low during the first CAS* cycle. On the first clock signal during the CAS* cycle, column address A0 is accessed for a burst write operation. Data provided on the DQ inputs is stored at address A0. On the next clock cycle, address A1 is accessed and data presented on the DQ inputs is stored at the new address. The burst write will continue for an entire burst length unless the burst is interrupted.

Because CAS* goes low prior to the next clock cycle and WE* goes high, the burst write operation is terminated. As a result, a burst read operation is initiated. A new column address A8 is read from the external address lines. The Output Enable (OE*) signal goes low and data stored at addresses A8, A9, A10 and A11 are output on the DQ lines. FIG. 5 illustrates a memory which has a burst length of 4 and a burst read clock latency of two. It will be understood that any burst length or clock latency will work in a synchronous BEDO memory circuit.

FIG. 7 illustrates a synchronous burst read operation followed by another synchronous burst read operation. An external memory row address is read on the first clock signal rising edge following the falling edge of RAS*. An external column address is likewise loaded into the burst counter on the first clock signal rising edge following the failing edge of CAS*. The WE* input is also examined on the rising edge of the clock signal. As shown in the timing diagram, WE* is high during the first CAS* cycle. Following a clock latency of two, data stored at column address A0 is provided on the DQ lines in response to the falling edge of the clock signal. On the next clock falling edge, address A1 is output on the DQ lines. The burst read will continue for an entire burst length unless the burst is interrupted. Because CAS* goes low during the burst operation and WE* remains high, the first burst read operation is terminated and a new burst read is initiated. A new column address A8 is read from the external address lines.

Two different synchronous BEDO memories are contemplated. The synchronous memory can be made either with an input pin dedicated to the clock signal, or the clock signal can be provided on the output enable input. This embodiment requires that the internal OE* signal be disabled by coupling to ground. Also, the OE* input pin must be rerouted to the clock function circuitry. Further, the memory operates in a non-burst mode if the CAS* signal is low. That is, when CAS* is low a new column address will be loaded from the external address lines into the burst counter on each rising edge of the clock. After an initial column address is loaded, a burst operation will be initiated on the next rising edge of the clock signal, provided that CAS* transitioned high prior to the clock signal. It will be appreciated, therefore, that a burst operation can be terminated by lowering CAS* prior to a rising transition in the clock signal. The DQ outputs go tristate after the completion of a burst if CAS* remains high.

CONCLUSION

A memory device has been described which can operate at fast data rates in a clocked or synchronous mode. The memory device is a random access memory which allows access to numerous columns of data while requiring only one external column address. A clock signal is used to synchronize access to memory elements.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. For example, the output enable (OE*) signal could be used as the clock input. That is, OE* could function as a clock, thereby eliminating the need for an additional input. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A memory device comprising:

a plurality of addressable memory elements; and

addressing circuitry adapted to receive a first memory element address in response to a transition of a clock signal and an address latch signal, and further adapted to generate a second memory element address in response to a subsequent transition of the clock signal,

wherein the clock signal is provided on an output enable input.

2. A synchronous memory device comprising:

a memory array having a plurality of addressable memory elements;

a plurality of address inputs for receiving memory element addresses;

an address latch input for receiving an address latch signal;

an address latch for receiving a first memory element address in response to a transition of a clock signal and the address latch signal; and

an address generation circuit responsive to successive transitions of the clock signal and to the first memory element address for generating additional memory element addresses,

wherein the clock signal is provided on an output enable input.

* * * * *

US005675549A

United States Patent [19]
Ong et al.

[11] **Patent Number: 5,675,549**
[45] **Date of Patent: *Oct. 7, 1997**

[54] **BURST EDO MEMORY DEVICE ADDRESS COUNTER**

[75] Inventors: **Adrian Ong**; **Paul S. Zagar**, both of Boise; **Brett L. Williams**, Eagle; **Troy A. Manning**, Boise, all of Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,526,320.

[21] Appl. No.: **457,651**

[22] Filed: **Jun. 1, 1995**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 386,894, Feb. 10, 1995, which is a continuation-in-part of Ser. No. 370,761, Dec. 23, 1994, Pat. No. 5,526,320.

[51] **Int. Cl.**[6] **G11C 8/00**
[52] **U.S. Cl.** **365/233.5**; 365/230.02; 365/236.5; 365/236
[58] **Field of Search** 365/238.5, 239, 365/236, 233.5, 230.02, 233

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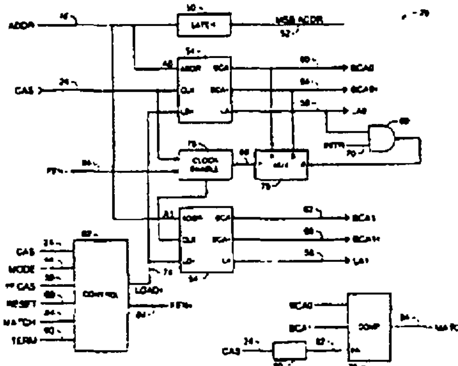
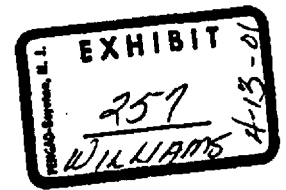
Primary Examiner—Tan T. Nguyen
Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

A counter comprised of two flip flops and a multiplexer produces a sequential or interleaved address sequence. The addresses produced are used to access memory elements in a Burst Extended Data Output Dynamic Random Access Memory (Burst EDO or BEDO DRAM). Input addresses in combination with a sequence select signal are logically combined to produce a multiplexer select input which selects between true and compliment outputs of a first flip flop to couple to an input of a second flip flop to specify a toggle condition for the second flip flop. Outputs of the counter are compared with outputs of an input address latch to detect the end of a burst sequence and initialize the device for another burst access. A transition of the Read/Write control line during a burst access will terminate the burst access and initialize the device for another burst access.

27 Claims, 12 Drawing Sheets





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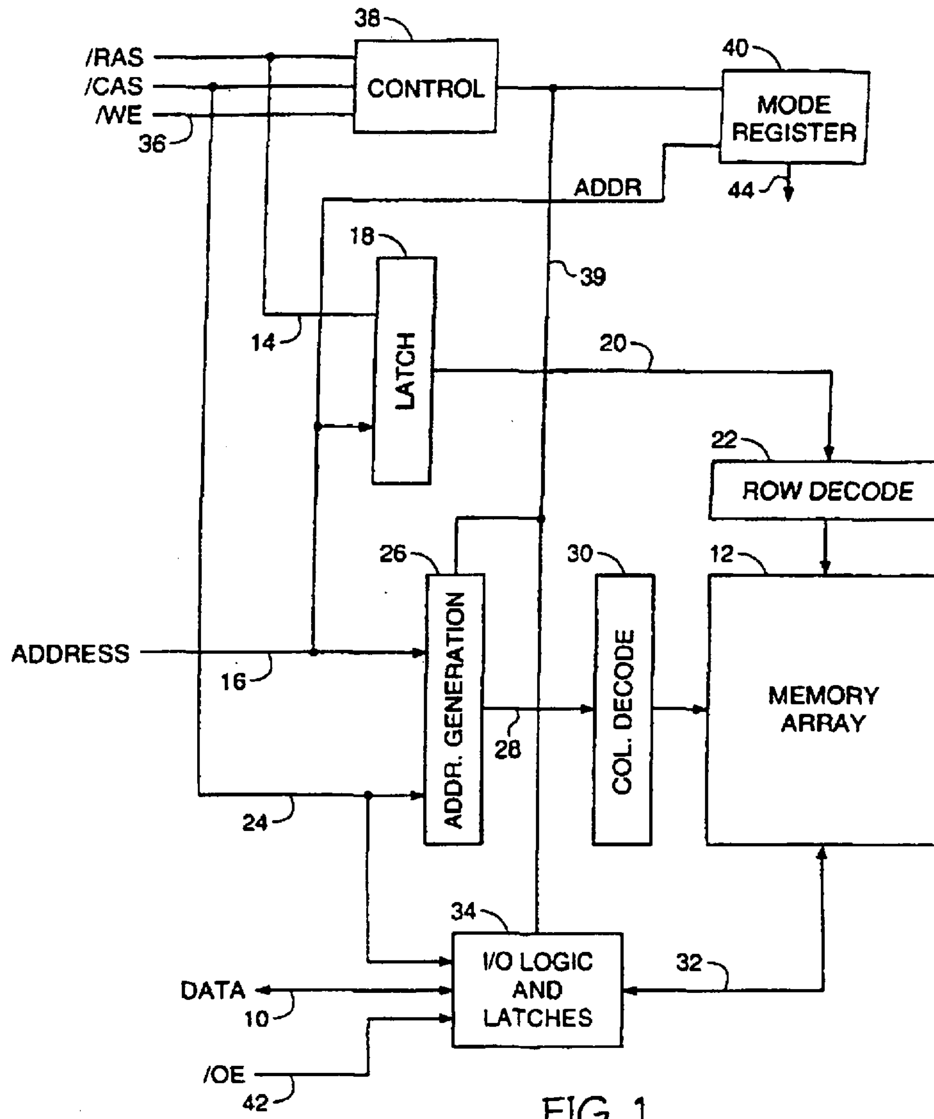

FIG. 1

Burst Length	Starting Column Address A_2	A_1	A_0	Linear	Interleave
2	V	V	0	0-1	0-1
	V	V	1	1-0	1-0
4	V	0	0	0-1-2-3	0-1-2-3
	V	0	1	1-2-3-0	1-0-3-2
	V	1	0	2-3-0-1	2-3-0-1
	V	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

FIG. 2

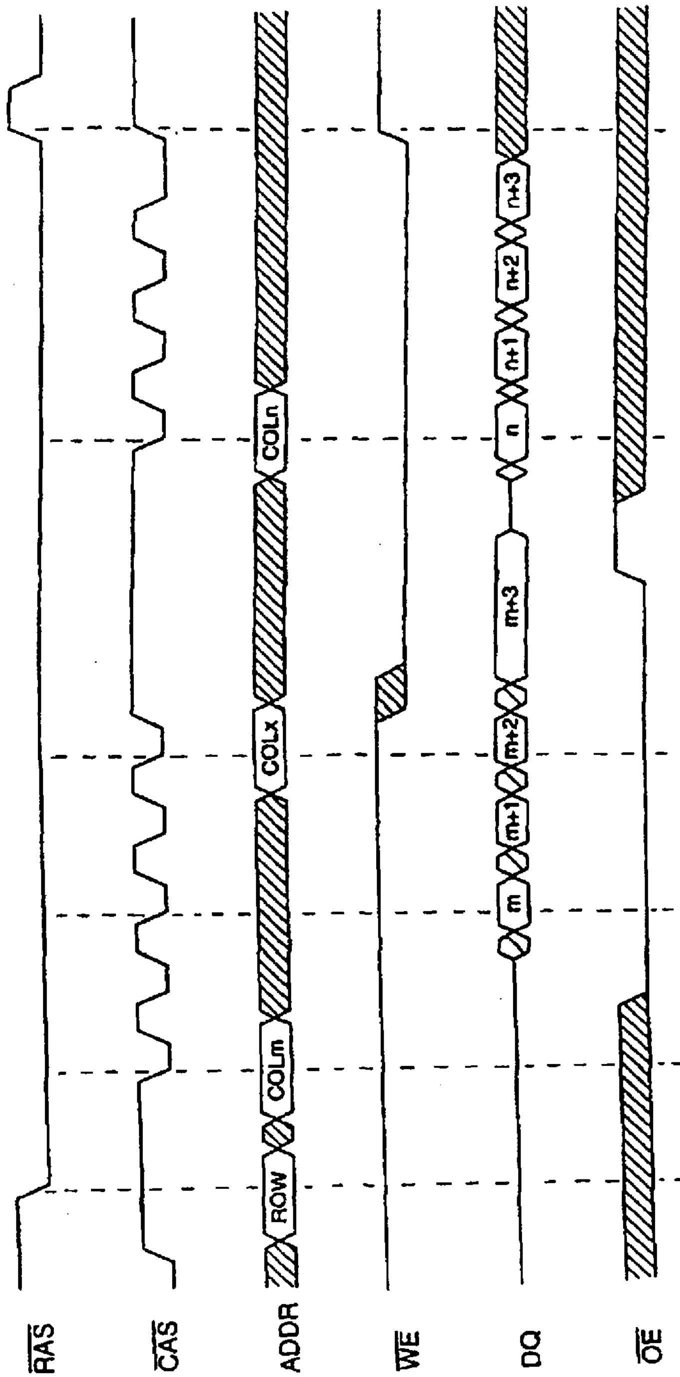

FIG. 3

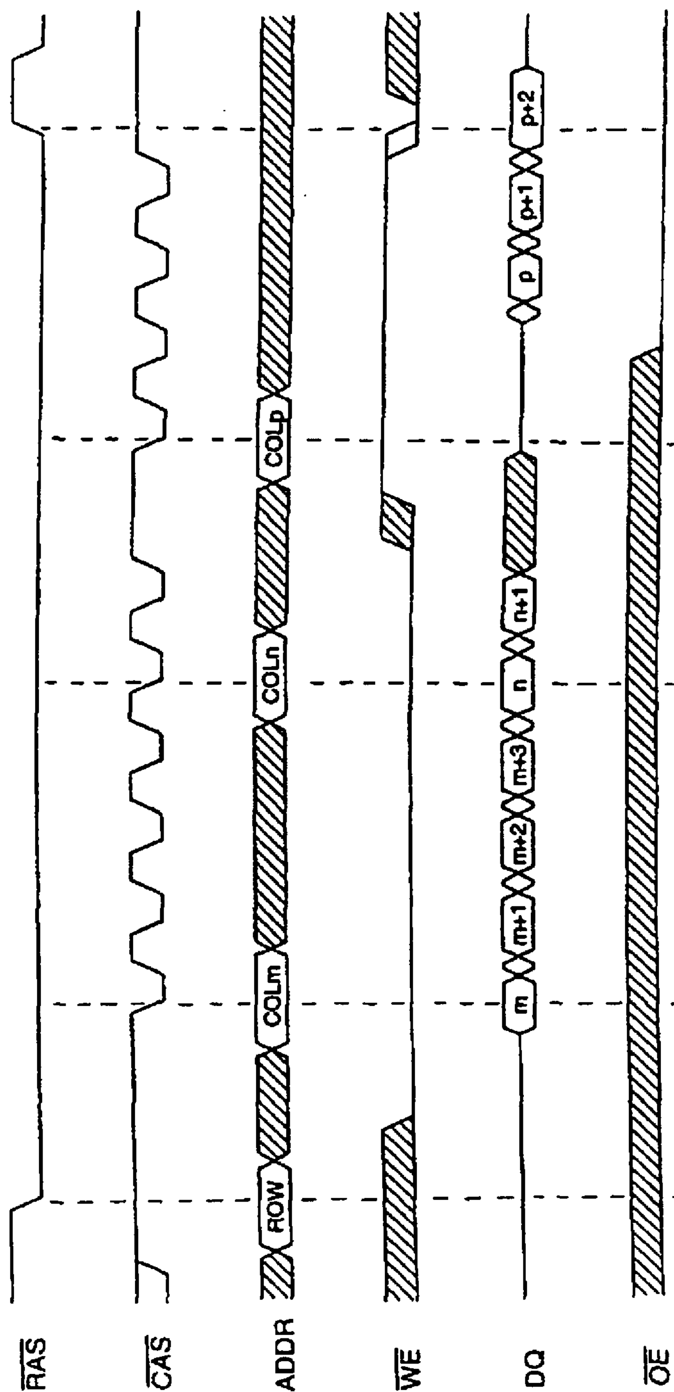

FIG. 4

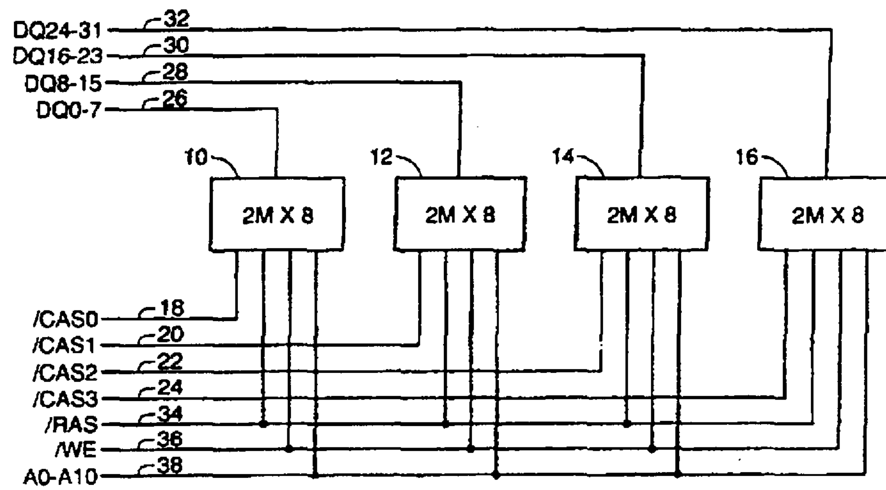

FIG. 5

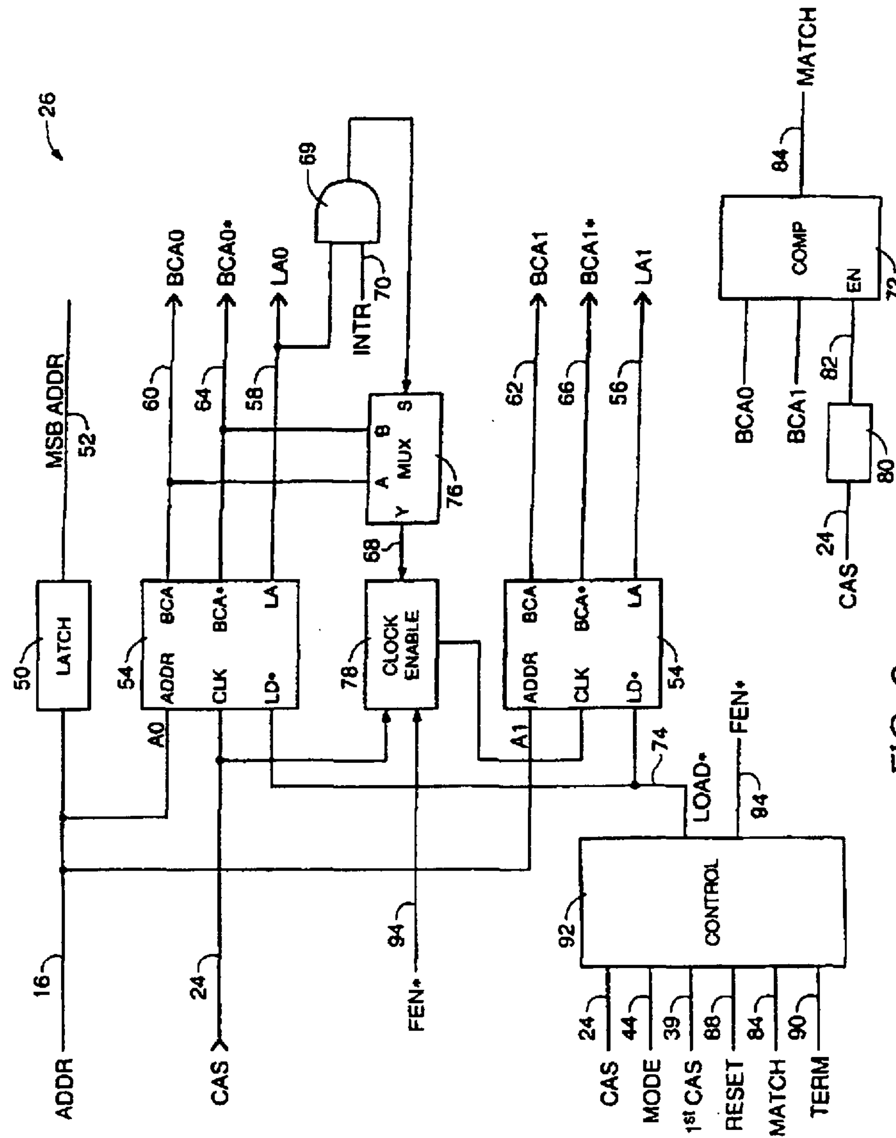

FIG. 6

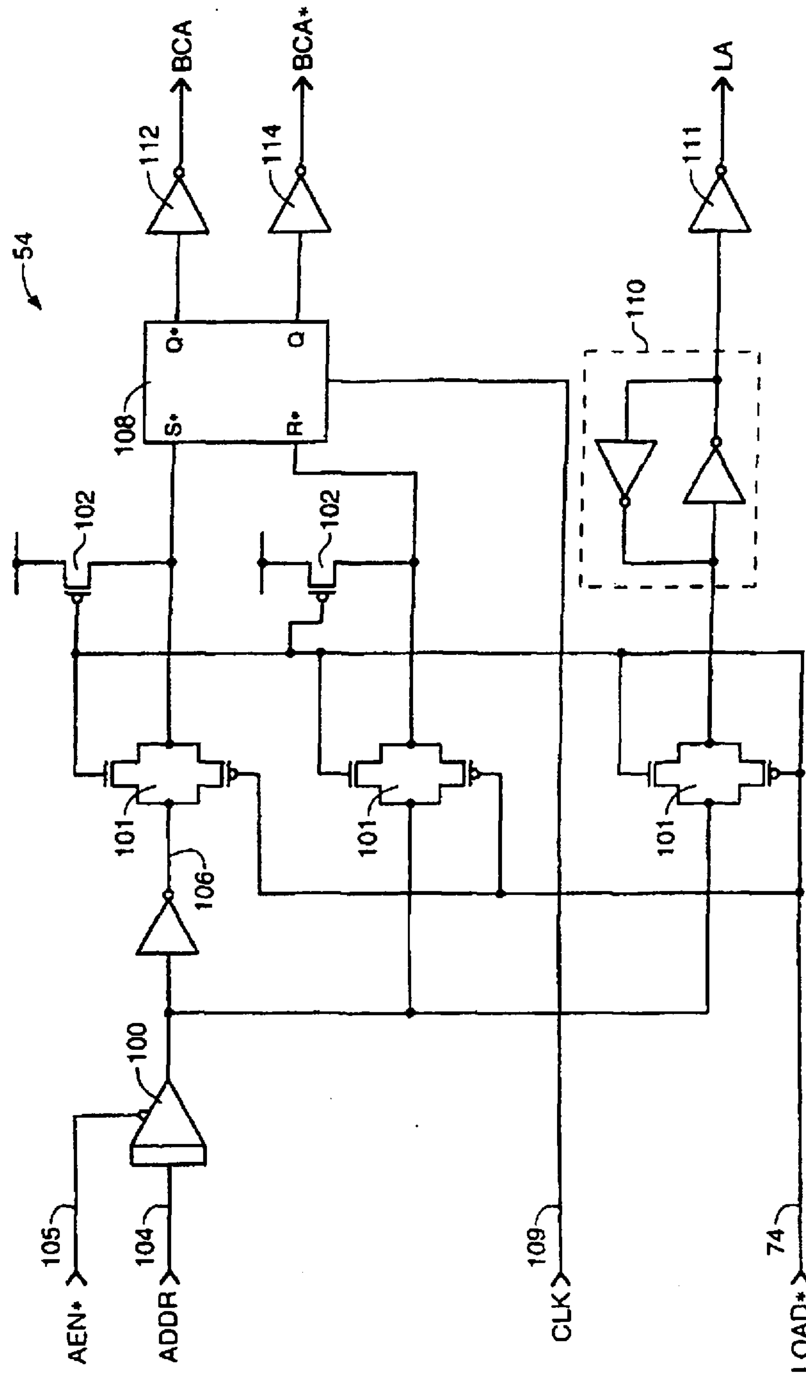

FIG. 7

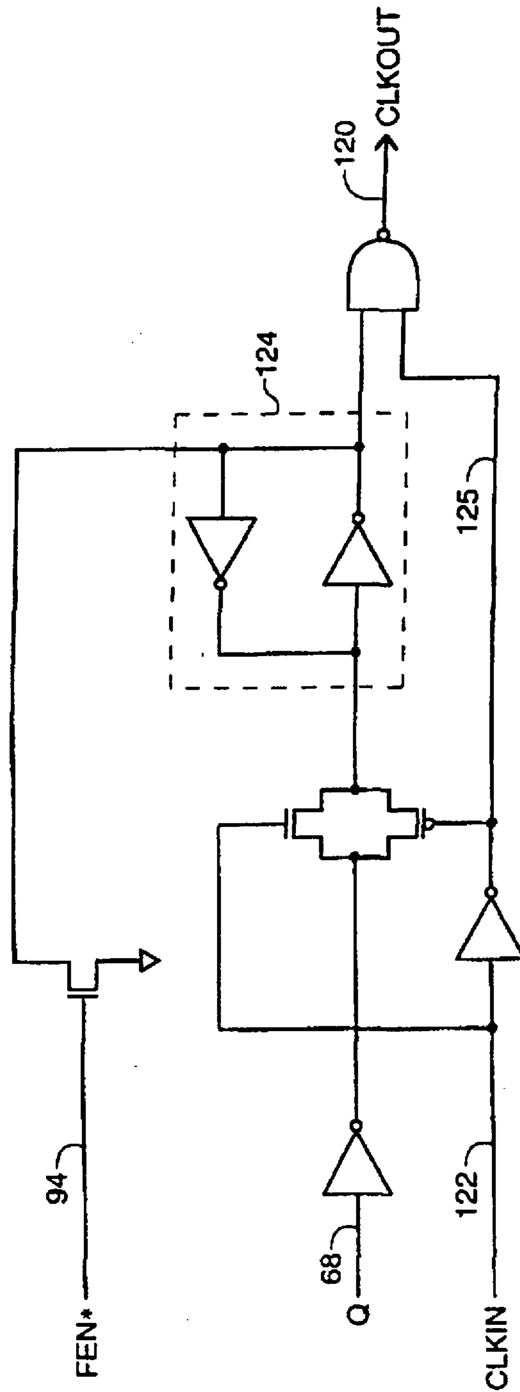

FIG. 8

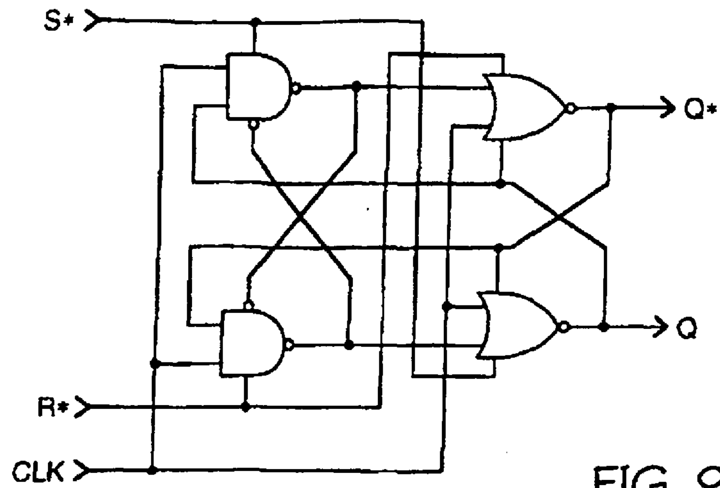

FIG. 9

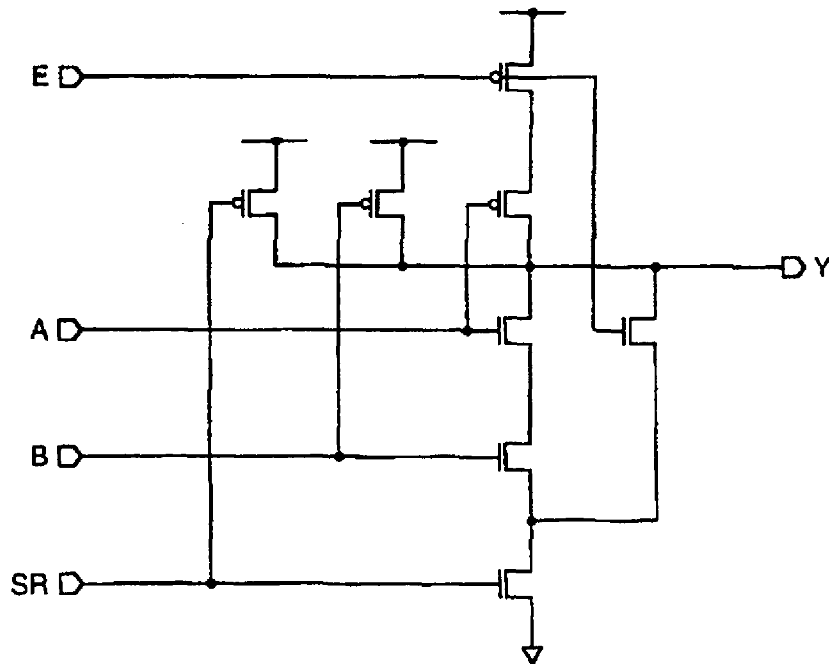

FIG. 10

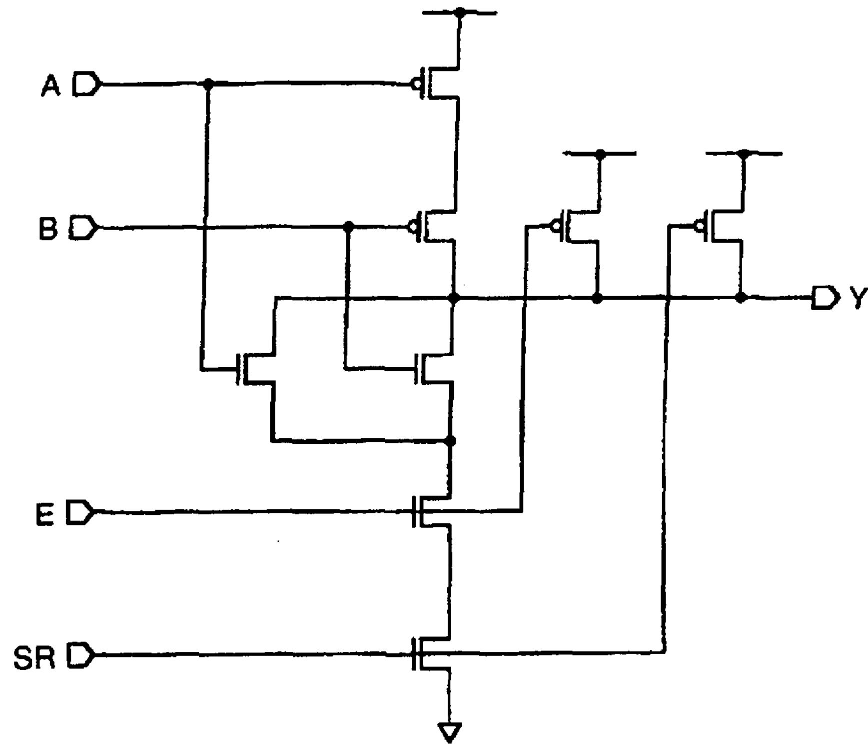

FIG. 11

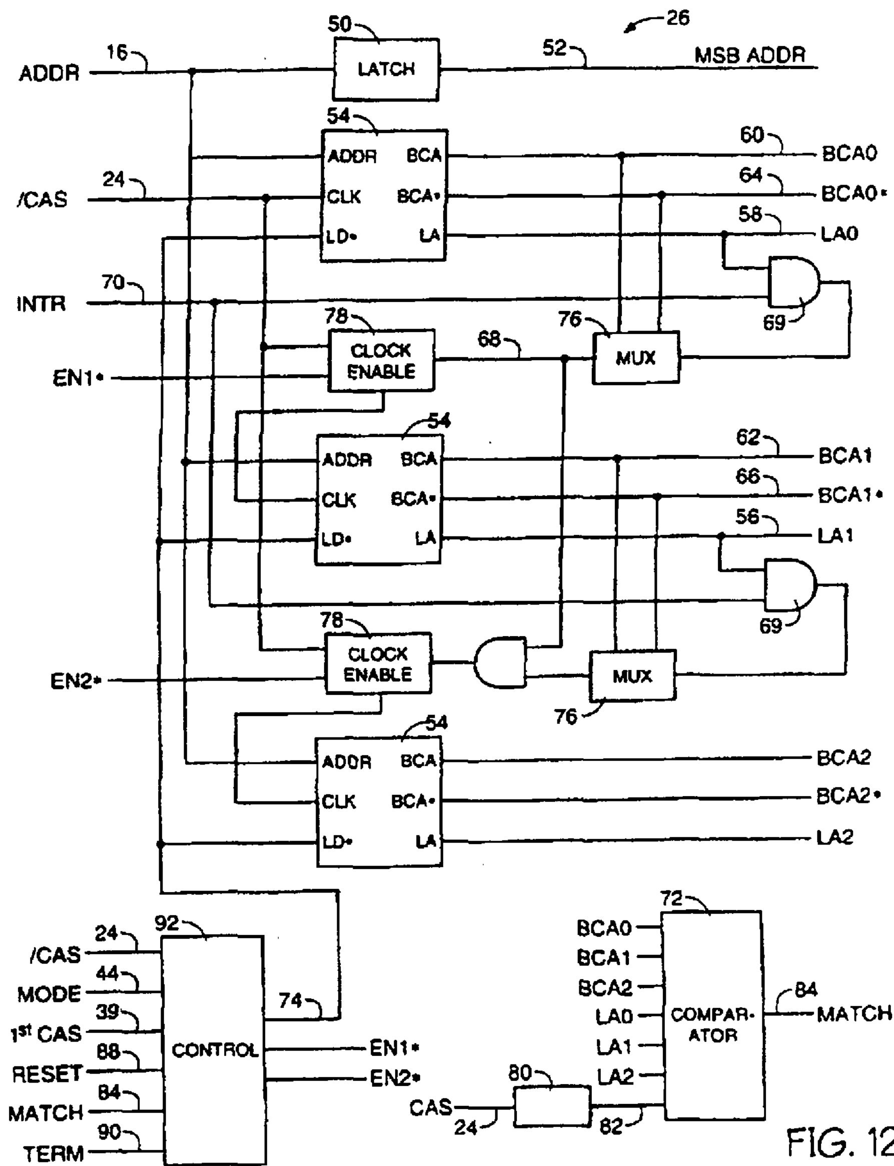

FIG. 12

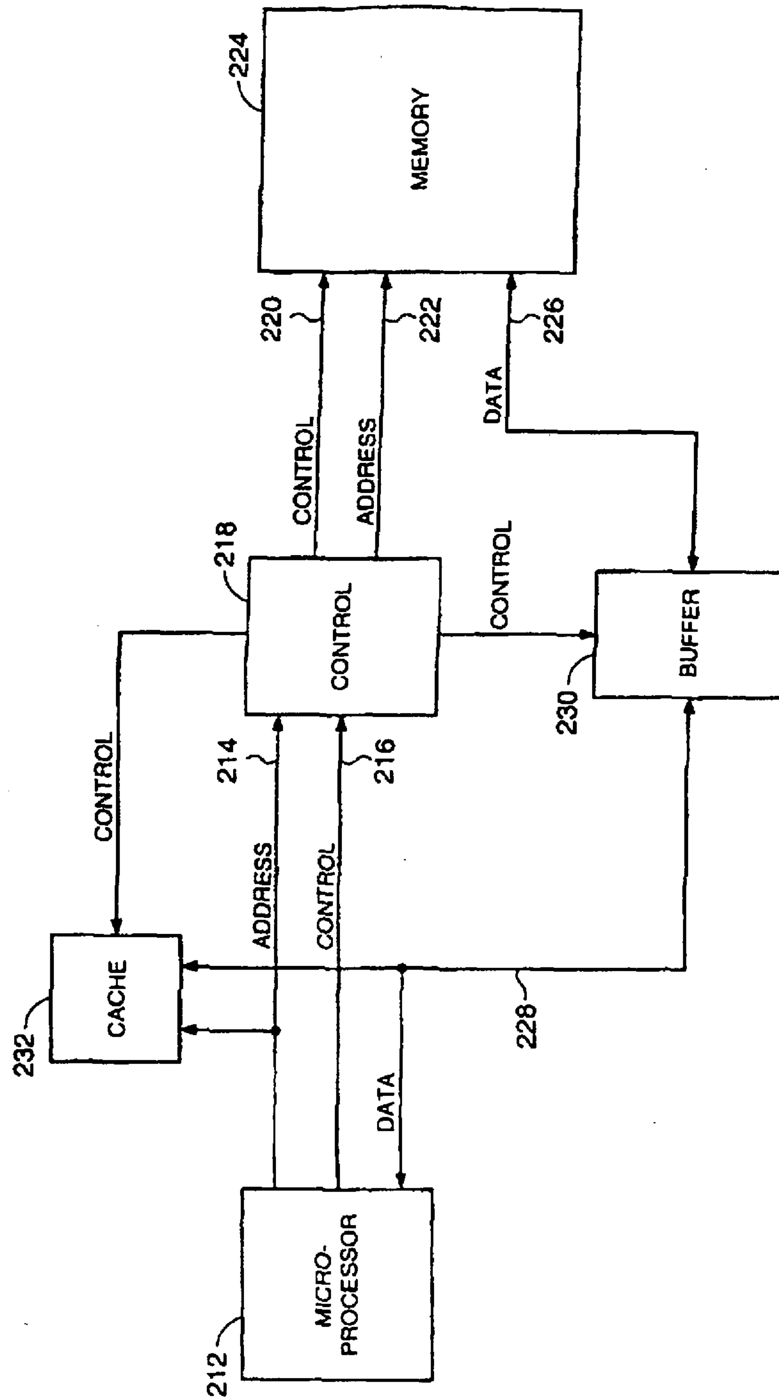

FIG. 13

BURST EDO MEMORY DEVICE ADDRESS COUNTER

CROSS-REFERENCE TO RELATED APPLICATIONS

This is a continuation-in-part of application Ser. No. 08/386,894 filed Feb. 10, 1995 now pending, which is a continuation-in-part of application Ser. No. 08/370,761 filed Dec. 23, 1994 now U.S. Pat. No. 5,526,320.

FIELD OF THE INVENTION

This invention relates to internal address generation circuits and counters for memory devices with burst access capability, and methods of accessing burst access memory devices.

BACKGROUND OF THE INVENTION

Dynamic Random Access Memory devices (DRAMs) are among the highest volume and most complex integrated circuits manufactured today. Except for their high volume production, the state of the art manufacturing requirements of these devices would cause them to be exorbitantly priced. Yet, due to efficiencies associated with high volume production, the price per bit of these memory devices is continually declining. The low cost of memory has fueled the growth and development of the personal computer. As personal computers have become more advanced, they in turn have required faster and more dense memory devices, but with the same low cost of the standard DRAM. Fast page mode DRAMs are the most popular standard DRAM today. In fast page mode operation, a row address strobe (/RAS) is used to latch a row address portion of a multiplexed DRAM address. Multiple occurrences of the column address strobe (/CAS) are then used to latch multiple column addresses to access data within the selected row. On the falling edge of /CAS an address is latched, and the DRAM outputs are enabled. When /CAS transitions high the DRAM outputs are placed in a high impedance state (tri-state). With advances in the production of integrated circuits, the internal circuitry of the DRAM operates faster than ever. This high speed circuitry has allowed for faster page mode cycle times. A problem exists in the reading of a DRAM when the device is operated with minimum fast page mode cycle times. /CAS may be low for as little as 15 nanoseconds, and the data access time from /CAS to valid output data (tCAC) may be up to 15 nanoseconds; therefore, in a worst case scenario with the device operating at minimum cycle times, there is no time to latch the output data external to the memory device. For devices with tCAC as low as 10 nanoseconds, the data is still only valid for a few nanoseconds. On a heavily loaded microprocessor memory bus, trying to latch an asynchronous signal that is only valid for a few nanoseconds is very difficult. Even providing a new address every 35 nanoseconds requires large address drivers which create significant amounts of electrical noise within the system.

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead,

data is held valid after /CAS goes high until sometime after the next /CAS low pulse occurs, or until /RAS or the output enable (/OE) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can be a complex function of when the column address inputs are valid, when /CAS falls, the state of /OE and when /CAS rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially /CAS) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM manufacturers.

Methods to shorten memory access cycles tend to require additional circuitry, additional control pins and nonstandard device pinouts. The proposed industry standard synchronous DRAM (SDRAM) for example has an additional pin for receiving a system clock signal. Since the system clock is connected to each device in a memory system, it is highly loaded, and it is always toggling circuitry in every device. SDRAMs also have a clock enable pin, a chip select pin and a data mask pin. Other signals which appear to be similar in name to those found on standard DRAMs have dramatically different functionality on a SDRAM. The addition of several control pins has required a deviation in device pinout from standard DRAMs which further complicates design efforts to utilize these new devices. Significant amounts of additional circuitry are required in the SDRAM devices which in turn result in higher device manufacturing costs.

In order for existing computer systems to use an improved device having a nonstandard pinout, those systems must be extensively modified. Additionally, existing computer system memory architectures are designed such that control and address signals may not be able to switch at the frequencies required to operate the new memory device at high speed due to large capacitive loads on the signal lines. The Single In-Line Memory Module (SIMM) provides an example of what has become an industry standard form of packaging memory in a computer system. On a SIMM, all address lines connect to all DRAMs. Further, the row address strobe (/RAS) and the write enable (/WE) are often connected to each DRAM on the SIMM. These lines inherently have high capacitive loads as a result of the number of device inputs driven by them. SIMM devices also typically ground the output enable (/OE) pin making /OE a less attractive candidate for providing extended functionality to the memory devices.

There is a great degree of resistance to any proposed deviations from the standard SIMM design due to the vast number of computers which use SIMMs. Industry's resistance to radical deviations from the standard, and the inability of current systems to accommodate new memory devices such as SDRAMs will delay their widespread acceptance. Therefore only limited quantities of devices with radically different architectures will be manufactured initially. This limited manufacture prevents the reduction in cost which typically can be accomplished through the manufacturing improvements and efficiencies associated with a high volume product.

SUMMARY OF THE INVENTION

An integrated circuit memory device with a standard DRAM pinout is designed for high speed data access and for compatibility with existing memory systems. A high speed burst mode of operation is provided where multiple sequential accesses occur following a single column address, and read data is output relative to the /CAS control signal. In the burst mode of operation the address is incremented internal

to the device eliminating the need for external address lines to switch at high frequencies. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at high speeds. Only one control line per memory chip (/CAS) must toggle at the operating frequency in order to clock the internal address counter and the data input/output latches. The load on each /CAS is typically less than the load on the other control signals (/RAS, /WE and /OE) since each /CAS typically controls only a byte width of the data bus. Internal circuitry of the memory device is largely compatible with existing Extended Data Out (EDO) DRAMs. This similarity allows the two part types to be manufactured on one die with a limited amount of additional circuitry. The ability to switch between a standard non-burst mode and a high speed burst mode allows the device to be used to replace standard devices, and eliminates the need to switch to more complex high speed memory devices. Internal address generation provides for faster data access times than is possible with either fast page mode or EDO DRAMs.

A novel counter architecture provides address generation for linear and interleaved addressing sequences. A comparator is used to detect completion of a burst access, and to prepare the device to begin additional burst accesses. The device is compatible with existing memory module designs including Single In-Line Memory Module (SIMM), Multi-Chip Module (MCM) and Dual In-Line Memory Module (DIMM) designs. This combination of features allows for significant system performance improvements with a minimum of design alterations.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention as well as objects and advantages will be best understood by reference to the appended claims, detailed description of particular embodiments and accompanying drawings where:

FIG. 1 is an electrical schematic diagram of a memory device in accordance with one embodiment of the invention;

FIG. 2 is a table showing linear versus interleaved addressing formats;

FIG. 3 is a timing diagram for a method of accessing the device of FIG. 1;

FIG. 4 is a further timing diagram for accessing the device of FIG. 1;

FIG. 5 is an electrical schematic diagram of a Single In-Line Memory Module in accordance with another embodiment of the invention;

FIG. 6 is a schematic diagram of a column address generation and control circuit;

FIG. 7 is a schematic of a one bit counter element;

FIG. 8 is a schematic of a counter element clock enable circuit;

FIG. 9 is a schematic of a flip flop;

FIG. 10 is a schematic of an enable NAND gate;

FIG. 11 is a schematic of an enable NOR gate;

FIG. 12 is a schematic of a three bit address generator circuit; and

FIG. 13 is a schematic diagram of a system designed in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a schematic representation of a sixteen megabit device designed in accordance with the present invention.

The device is organized as a 2 Meg×8 burst EDO DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array 12. The device of FIG. 1 may have an industry standard pinout for eight bit wide EDO DRAMs. An active-low row address strobe (/RAS) signal 14 is used to latch a first portion of a multiplexed memory address, from address inputs 16, in latch 18. The latched row address 20 is decoded in row decoder 22. The decoded row address is used to select a row of the memory array 12. A column address strobe (/CAS) signal 24 is used to latch a second portion of a memory address from address inputs 16 into address generation circuit 26. The latched column address 28 is decoded in column address decoder 30. The decoded column address is used to select a column of the memory array 12.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 32 to output latches 34. Data 10 driven from the burst EDO DRAM may be latched external to the device in synchronization with /CAS after a predetermined number of /CAS cycle delays (latency). For a two cycle latency design, the first /CAS falling edge is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second /CAS falling edge, and remains valid through the third /CAS falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during /CAS high intervals dependent on the state of the output enable and write enable (/OE and /WE) control lines, thus allowing additional time for the system to latch the output data. The data outputs remain valid throughout the burst read cycles with the exception of brief periods of data transition. During these periods of data transition, the output drivers may be turned off momentarily in order to aid data transition. This state of the output buffer should not be confused with the standard DRAM tri-state condition which is intended to release the data bus.

Once a row and a column address are selected, additional transitions of the /CAS signal are used to advance the column address within the address generation circuit in a predetermined sequence. The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the /CAS signal provided that /OE is maintained low, and /WE remains high. The output data signal levels may be but are not limited to being driven in accordance with standard CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. FIG. 2 is a table which shows linear and interleaved addressing sequences for burst lengths of 2, 4 and 8 cycles. The "V" for starting addresses A1 and A2 in the table represent address values that remain unaltered through the burst sequence. The column address may be advanced with each /CAS transition, each pulse, or multiple of /CAS pulses in the event that more than one data word is read from the array with each column address. When the address is advanced with each transition of the /CAS signal, data is also driven from the part after each transition following the device latency which is then referenced to each edge of the /CAS signal. This allows for a burst access cycle where the highest switching control line (/CAS) toggles only once (high to low or low to high) for each memory cycle. This is in contrast to standard DRAMs which require /CAS to go low and then high for each cycle, and

14. The device according to claim 13, further comprising:

an array of dynamic random access memory elements wherein said address counter determines at least a portion of a column address of said array.

15. The device according to claim 13, further comprising:

an address latch to latch an external address signal; and

a multiplexer control circuit, coupled to said multiplexer, responsive to a latched address signal from said address latch to select between the output of said first flip flop and the complement of the output of said first flip flop for coupling to the input of said second flip flop.

16. The device according to claim 13, further comprising:

a multiplexer control circuit, coupled to said multiplexer, responsive to a sequence control signal to select between the output of said first flip flop and the complement of the output of said first flip flop for coupling to the input of said second flip flop.

17. The device according to claim 13, further comprising:

a clock enable circuit coupled to the input of said second flip flop and to said multiplexer.

18. The device according to claim 17, wherein said clock enable circuit comprises:

a latch having an input coupled to said multiplexer; and

a logic gate coupled to an output of said latch and to said second flip flop, said logic gate enabled by the output of said latch to pass a clock signal to said second flip flop.

19. A counter for use in an integrated memory device comprising:

a first flip flop;

a second flip flop; and

a multiplexer coupled to said first flip flop and said second flip flop, said multiplexer responsive to a select signal to couple an output of said first flip flop or a compliment of the output of said first flip flop to an input of said second flip flop to specify a toggle condition for said second flip flop.

20. A control circuit for a counter used in an integrated memory device, comprising:

a sequence control circuit, coupled to the counter and an initial count register, responsive to a sequence control signal for selecting one of a plurality of predetermined address sequences; and

a comparator coupled to an output of the counter and to the initial count register, wherein the counter is loaded in response to an output of said comparator indicating a match between the output of the counter and a corresponding output of the initial count register, and the counter counts in a sequence determined by said sequence control circuit.

21. A method of performing a burst access of a memory device, comprising:

loading a burst address counter with a first initial address;

accessing a first memory element at the first initial address;

advancing the burst address counter;

accessing a second memory element at an address provided by the burst address counter;

comparing the first initial address with the address provided by the burst address counter; and

terminating the burst access in response to a match of the first initial address with the address provided by the burst address counter.

22. The method according to claim 21, further comprising:

loading the burst address counter with a second initial address in response to a match of the first address with the address provided by the burst address counter.

23. In a memory device having an address input, an address strobe input, a write control input and an address counter, the address counter comprising a first flip flop, a second flip flop and a multiplexer, a method of accessing a memory element of the memory device, comprising:

loading a portion of a first address into the first flip flop and the second flip flop in response to an address strobe received on the address strobe input and the first address received on the address input;

coupling an output of the first flip flop to an input of the second flip flop through the multiplexer;

toggling an output of the second flip flop in response to the output of the first flip flop received from the multiplexer; and

accessing the memory element at a second address determined at least in part by the output of the first flip flop and the output of the second flip flop.

24. The method according to claim 23, further comprising:

coupling a compliment of the output of the first flip flop to the input of the second flip flop through the multiplexer in response to an address sequence control signal and a least significant bit of the first address.

25. The method according to claim 23, further comprising:

terminating a burst access of the memory device in response to an output of the first flip flop and an output of the second flip flop matching a corresponding portion of the first address.

26. The method according to claim 23, further comprising:

loading a portion of a third address into the first flip flop and the second flip flop in response to a further address strobe received on the address strobe input, the third address received on the address input, and the output of the first flip flop and the output of the second flip flop matching a corresponding portion of the first address received on the address input.

27. The method according to claim 23, further comprising:

terminating a burst access of the memory device in response to a transition of a write control signal received on the write control input.

* * * * *

US005696732A

United States Patent [19]

Zagar et al.

[11] **Patent Number: 5,696,732**

[45] **Date of Patent: *Dec. 9, 1997**

[54] **BURST EDO MEMORY DEVICE**

[75] Inventors: Paul S. Zagar, Boise; Brett L. Williams, Eagle, both of Id.

[73] Assignee: Micron Technology, Inc., Boise, Id.

[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,526,320.

[21] Appl. No.: 754,780

[22] Filed: Nov. 21, 1996

Related U.S. Application Data

[63] Continuation of Ser. No. 630,279, Apr. 11, 1995, which is a continuation of Ser. No. 370,761, Dec. 23, 1994, Pat. No. 5,526,320.

[51] Int. Cl.[6] G11C 8/00

[52] U.S. Cl. 365/233.5; 365/238.5

[58] Field of Search 365/233.5, 233, 365/238.5, 230.01, 230.08

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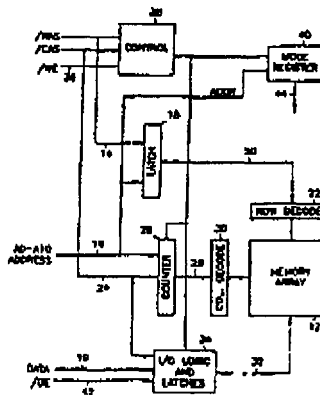
Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

An integrated circuit memory device is designed for high speed data access and for compatibility with existing memory systems. An address strobe signal is used to latch a first address. During a burst access cycle the address is incremented internal to the device with additional address strobe transitions. A new memory address is only required at the beginning of each burst access. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at the device cycle frequency. Transitions of the Read/Write control line during a burst access will terminate the burst access, reset the burst length counter and initialize the device for another burst access. The device is compatible with existing Extended Data Out DRAM device pinouts, Fast Page Mode and Extended Data Out Single In-Line Memory Module pinouts, and other memory circuit designs.

4 Claims, 7 Drawing Sheets



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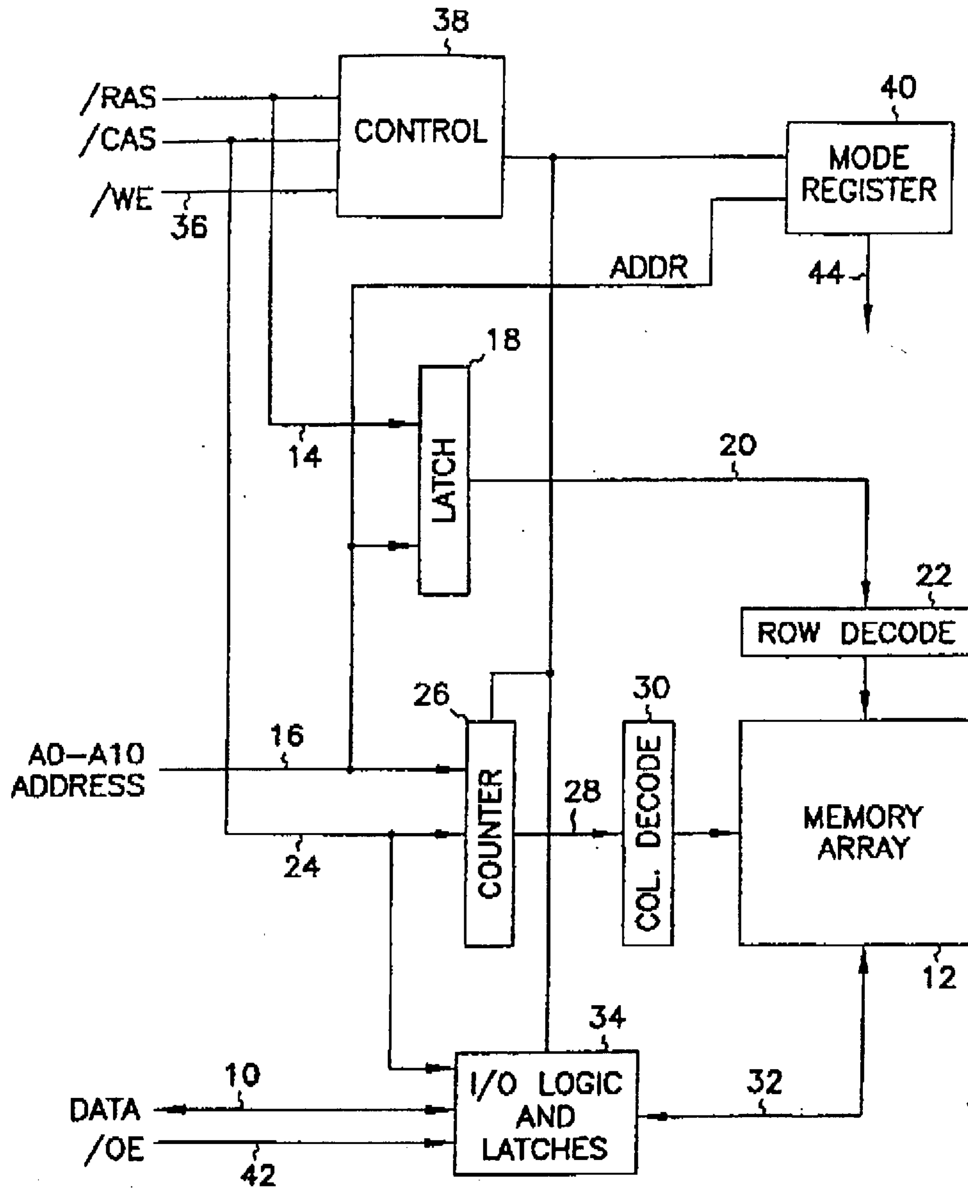

FIG. 1

Burst Length	Starting Column Address A_2	A_1	A_0	Linear	Interleave
2	V	V	0	0-1	0-1
	V	V	1	1-0	1-0
4	V	0	0	0-1-2-3	0-1-2-3
	V	0	1	1-2-3-0	1-0-3-2
	V	1	0	2-3-0-1	2-3-0-1
	V	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

FIG. 2

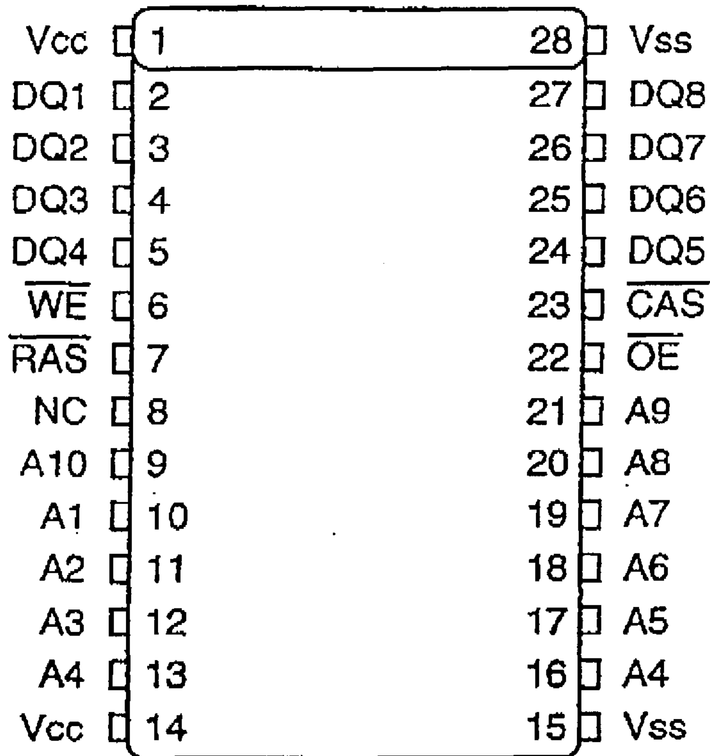

FIG. 3

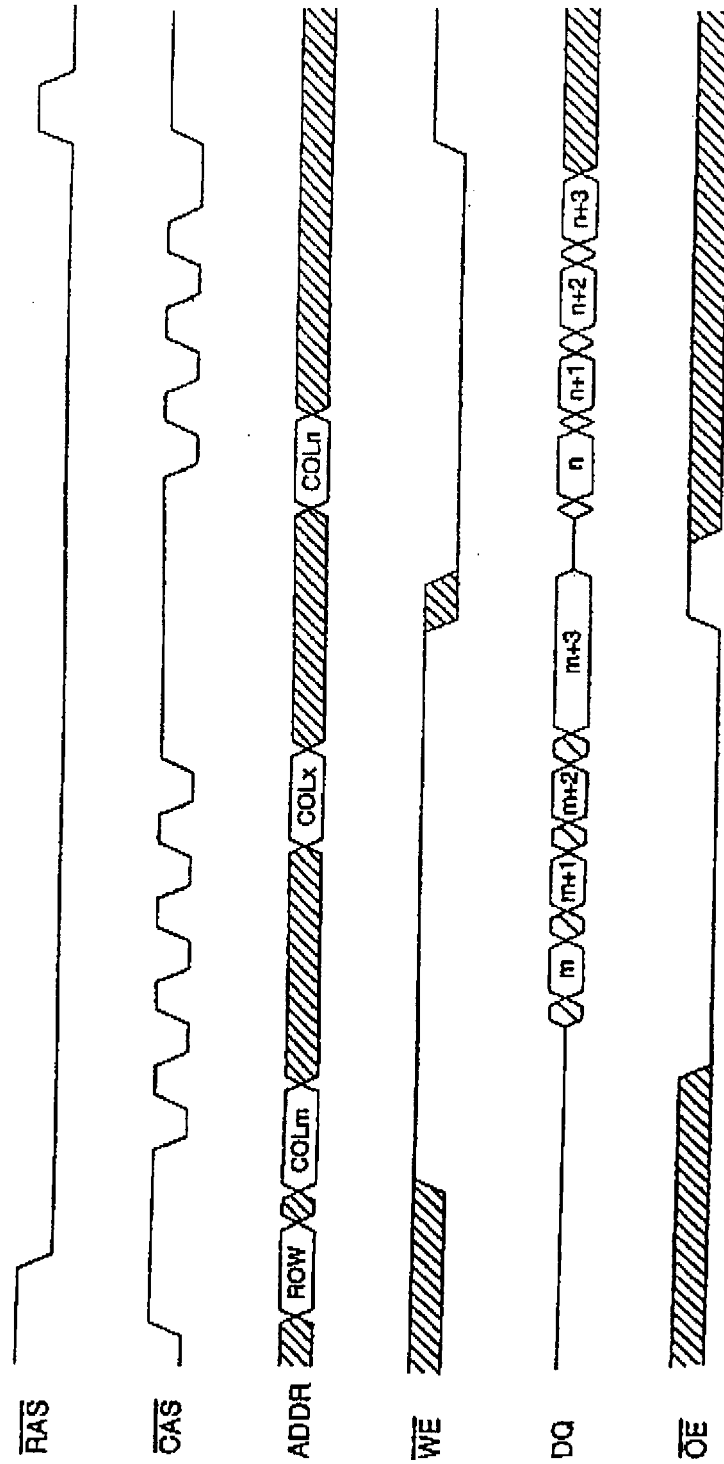

FIG. 4

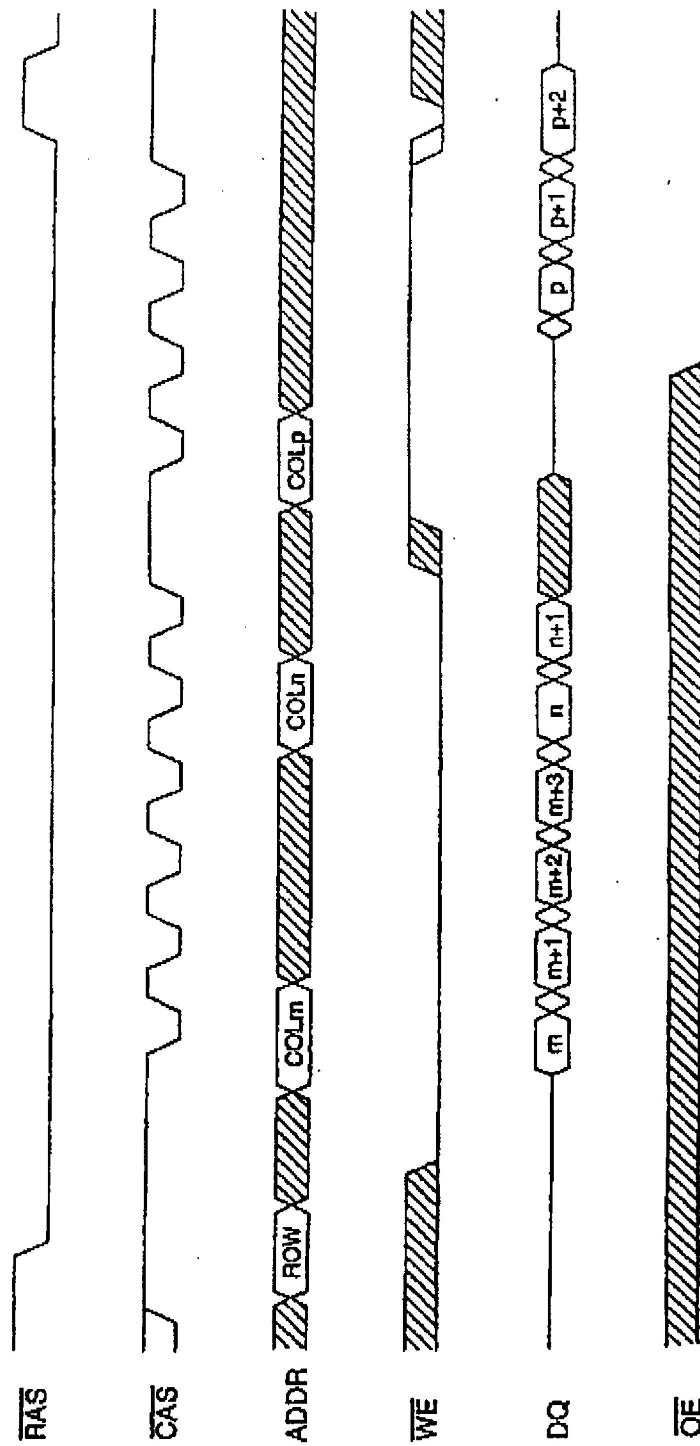

FIG. 5

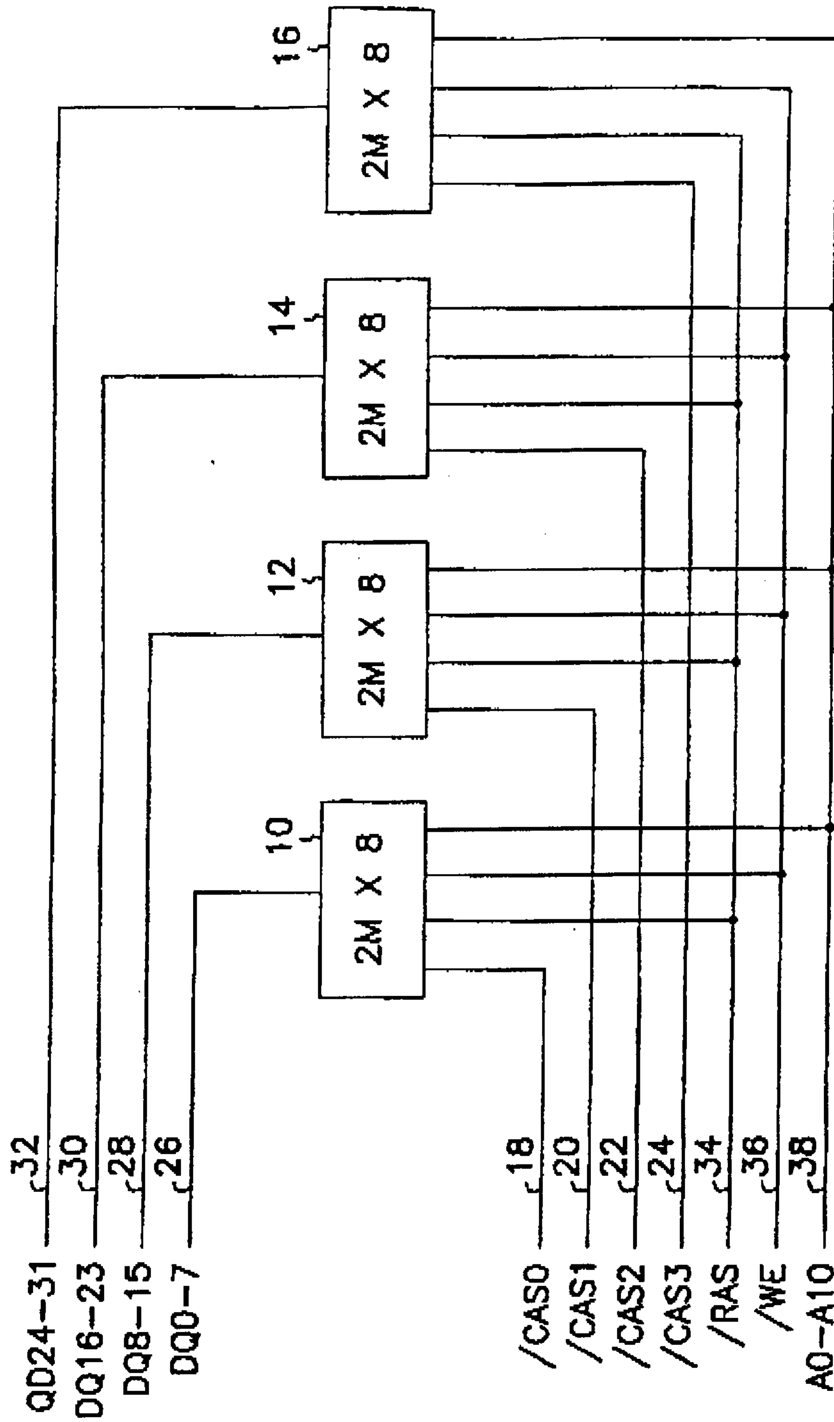

FIG. 6

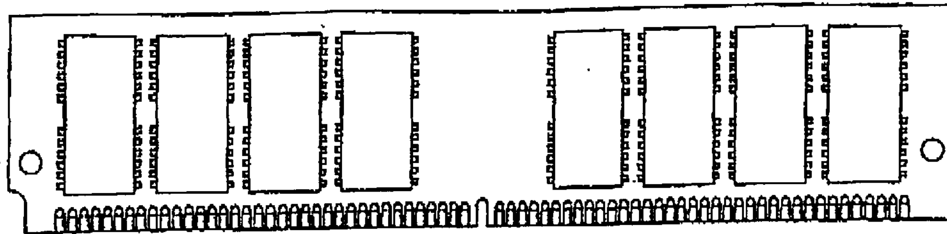

FIG. 7

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{CAS0}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{CAS2}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{CAS3}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{CAS1}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{RAS0}$	62	DQ31
9	DQ20	27	DQ24	45	$\overline{RAS1}$	63	DQ15
10	Vcc	28	A7	46	$\overline{OE}$	64	DQ32
11	PD5	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	Vcc	48	PD ECC	66	PD EDO
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ25	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	NC	52	DQ26	70	PD4
17	A5	35	NC	53	DQ11	71	PD refresh
18	A6	36	NC	54	DQ27	72	Vss

FIG. 8

BURST EDO MEMORY DEVICE

This is a continuation of application Ser. No. 08/630,279, filed Apr. 11, 1995, which is a continuation of U.S. Ser. No. 370,761, filed Dec. 23, 1994, now U.S. Pat. No. 5,526,320 issued Jun. 11, 1996.

FIELD OF THE INVENTION

This invention relates to memory device architectures designed to provide high density data storage with high speed read and write access cycles.

BACKGROUND OF THE INVENTION

Dynamic Random Access Memory devices (DRAMs) are among the highest volume and most complex integrated circuits manufactured today. Except for their high volume production, the state of the art manufacturing requirements of these devices would cause them to be exorbitantly priced. Yet, due to efficiencies associated with high volume production, the price per bit of these memory devices is continually declining. The low cost of memory has fueled the growth and development of the personal computer. As personal computers have become more advanced, they in turn have required faster and more dense memory devices, but with the same low cost of the standard DRAM. Fast page mode DRAMs are the most popular standard DRAM today. In fast page mode operation, a row address strobe (/RAS) is used to latch a row address portion of a multiplexed DRAM address. Multiple occurrences of the column address strobe (/CAS) are then used to latch multiple column addresses to access data within the selected row. On the falling edge of /CAS an address is latched, and the DRAM outputs are enabled. When /CAS transitions high the DRAM outputs are placed in a high impedance state (tri-state). With advances in the production of integrated circuits, the internal circuitry of the DRAM operates faster than ever. This high speed circuitry has allowed for faster page mode cycle times. A problem exists in the reading of a DRAM when the device is operated with minimum fast page mode cycle times. /CAS may be low for as little as 15 nanoseconds, and the data access time from /CAS to valid output data (tCAC) may be up to 15 nanoseconds; therefore, in a worst case scenario there is no time to latch the output data external to the memory device. For devices that operate faster than the specifications require, the data may still only be valid for a few nanoseconds. On a heavily loaded microprocessor memory bus, trying to latch an asynchronous signal that is valid for only a few nanoseconds is very difficult. Even providing a new address every 35 nanoseconds requires large address drivers which create significant amounts of electrical noise within the system. To increase the data throughput of a memory system, it has been common practice to place multiple devices on a common bus. For example, two fast page mode DRAMs may be connected to common address and data buses. One DRAM stores data for odd addresses, and the other for even addresses. The /CAS signal for the odd addresses is turned off (high) when the /CAS signal for the even addresses is turned on (low). This interleaved memory system provides data access at twice the rate of either device alone. If the first /CAS is low for 20 nanoseconds and then high for 20 nanoseconds while the second /CAS goes low, data can be accessed every 20 nanoseconds or 50 megahertz. If the access time from /CAS to data valid is fifteen nanoseconds, the data will be valid for only five nanoseconds at the end of each 20 nanosecond period when both devices are operating in fast page mode. As cycle times are shortened, the data valid period goes to zero.

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead, data is held valid after /CAS goes high until sometime after the next /CAS low pulse occurs, or until /RAS or the output enable (/OE) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can be a complex function of when the column address inputs are valid, when /CAS falls, the state of /OE and when /CAS rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially /CAS) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM manufacturers.

Methods to shorten memory access cycles tend to require additional circuitry, additional control pins and nonstandard device pinouts. The proposed industry standard synchronous DRAM (SDRAM) for example has an additional pin for receiving a system clock signal. Since the system clock is connected to each device in a memory system, it is highly loaded, and it is always toggling circuitry in every device. SDRAMs also have a clock enable pin, a chip select pin and a data mask pin. Other signals which appear to be similar in name to those found on standard DRAMs have dramatically different functionality on a SDRAM. The addition of several control pins has required a deviation in device pinout from standard DRAMs which further complicates design efforts to utilize these new devices. Significant amounts of additional circuitry are required in the SDRAM devices which in turn result in higher device manufacturing costs.

In order for existing computer systems to use an improved device having a nonstandard pinout, those systems must be extensively modified. Additionally, existing computer system memory architectures are designed such that control and address signals may not be able to switch at the frequencies required to operate the new memory device at high speed due to large capacitive loads on the signal lines. The Single In-Line Memory Module (SIMM) provides an example of what has become an industry standard form of packaging memory in a computer system. On a SIMM, all address lines connect to all DRAMs. Further, the row address strobe (/RAS) and the write enable (/WE) are often connected to each DRAM on the SIMM. These lines inherently have high capacitive loads as a result of the number of device inputs driven by them. SIMM devices also typically ground the output enable (/OE) pin making /OE a less attractive candidate for providing extended functionality to the memory devices.

There is a great degree of resistance to any proposed deviations from the standard SIMM design due to the vast number of computers which use SIMMs. Industry's resistance to radical deviations from the standard, and the inability of current systems to accommodate the new memory devices will delay their widespread acceptance. Therefore only limited quantities of devices with radically different architectures will be manufactured initially. This limited manufacture prevents the reduction in cost which typically can be accomplished through the manufacturing improvements and efficiencies associated with a high volume product.

SUMMARY OF THE INVENTION

An integrated circuit memory device with a standard DRAM pinout is designed for high speed data access dad for compatibility with existing memory systems. A high speed burst mode of operation is provided where multiple sequential accesses occur following a single column address, and read data is output relative to the /CAS control signal. In the burst mode of operation the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at high speeds. Only one control line per memory chip (/CAS) must toggle at the operating frequency in order to clock the internal address counter and the data input/output latches. The load on each /CAS is typically less than the load on the other control signals (/RAS, /WE and /OE) since each /CAS typically controls only a byte width of the data bus. Internal circuitry of the memory device is largely compatible with existing Extended Data Out (EDO) DRAMs. This similarity allows the two part types to be manufactured on one die with a limited amount of additional circuitry. The ability to switch between a standard non-burst mode and a high speed burst mode allows the device to be used to replace standard devices, and eliminates the need to switch to more complex high speed memory devices. Internal address generation provides for faster data access times than is possible with either fast page mode or EDO DRAMs. This high speed operation eliminates the need to interleave memory devices in order to attain a high data throughput. In contrast to the 50 megahertz interleaved memory system described above, the output data from this device will be valid for approximately 15 nanoseconds significantly easing the design of circuitry required to latch the data from the memory. The device is compatible with existing memory module pinouts including Single In-Line Memory Module (SIMM), Multi-Chip Module (MCM) and Dual In-Line Memory Module (DIMM) designs. This combination of features allows for significant system performance improvements with a minimum of design alterations.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention as well as objects and advantages will be best understood by reference to the appended claims, detailed description of particular embodiments and accompanying drawings where:

FIG. 1 is an electrical schematic diagram of a memory device in accordance with one embodiment of the invention;

FIG. 2 is a table showing linear versus interleaved addressing formats;

FIG. 3 is a pinout of the memory device of FIG. 1;

FIG. 4 is a timing diagram for a method of accessing the device of FIG. 1;

FIG. 5 is a further timing diagram for accessing the device of FIG. 1;

FIG. 6 is an electrical schematic diagram of a Single In-Line Memory Module in accordance with another embodiment of the invention;

FIG. 7 is a front view of a Single In-Line Memory Module designed in accordance with the teachings of this invention; and

FIG. 8 is a table of the pin numbers and signal names of the Single In-Line Memory Module of FIG. 7.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a schematic representation of a sixteen megabit device designed in accordance with the present invention.

The device is organized as a 2 Meg×8 burst EDO DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array 12. The device of FIG. 1 has an industry standard pinout for eight bit wide EDO DRAMs. An active-low row address strobe (/RAS) signal 14 is used to latch a first portion of a multiplexed memory address, from address inputs A0 through A10 16, in latch 18. The latched row address 20 is decoded in row decoder 22. The decoded row address is used to select a row of the memory array 12. A column address strobe (/CAS) signal 24 is used to latch a second portion of a memory address from address inputs 16 into column address counter 26. The latched column address 28 is decoded in column address decoder 30. The decoded column address is used to select a column of the memory array 12.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 32 to output latches 34. Data 10 driven from the burst EDO DRAM may be latched external to the device in synchronization with /CAS after a predetermined number of /CAS cycle delays (latency). For a two cycle latency design, the first /CAS falling edge is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second /CAS falling edge, and remains valid through the third /CAS falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during /CAS high intervals dependent on the state of the output enable and write enable (/OE and /WE) control lines, thus allowing additional time for the system to latch the output data. Once a row and a column address are selected, additional transitions of the /CAS signal are used to advance the column address within the column address counter in a predetermined sequence. The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the /CAS signal provided that /OE is maintained low, and /WE remains high. The output data signal levels may be driven in accordance with standard CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. FIG. 2 is a table which shows linear and interleaved addressing sequences for burst lengths of 2,4 and 8 cycles. The "V" for starting addresses A1 and A2 in the table represent address values that remain unaltered through the burst sequence. The column address may be advanced with each /CAS transition, each pulse, or multiple of /CAS pulses in the event that more than one data word is read from the array with each column address. When the address is advanced with each transition of the /CAS signal, data is also driven from the part after each transition following the device latency which is then referenced to each edge of the /CAS signal. This allows for a burst access cycle where the highest switching control line (/CAS) toggles only once (high to low or low to high) for each memory cycle. This is in contrast to standard DRAMs which require /CAS to go low and then high for each cycle, and synchronous DRAMs which require a full clock cycle (high and low transitions) for each memory cycle. For maximum compatibility with existing EDO DRAM devices, the invention will be further described in reference to a device designed to latch and advance a column address on falling edges of the /CAS signal.

It may be desirable to latch and increment the column address after the first /CAS falling edge in order to apply both the latched and incremented addresses to the array at the earliest opportunity in an access cycle. For example, a device may be designed to access two data words per cycle (prefetch architecture). The memory array for a prefetch architecture device may be split into odd and even array halves. The column address least significant bit is then used to select between odd and even halves while the other column address bits select a column within each of the array halves. In an interleaved access mode with column address 1, data from columns 0 and 1 would be read and the data from column 1 would be output followed by the data from column 0 in accordance with standard interleaved addressing as described in SDRAM specifications. In a linear access mode column address 1 would be applied to the odd array half, and incremented to address 2 for accessing the even array half to fulfill the two word access. One method of implementing this type of device architecture is to provide a column address incrementing circuit between the column address counter and the even array half. The incrementing circuit would increment the column address only if the initial column address in a burst access cycle is odd, and the address mode is linear. Otherwise the incrementing circuit would pass the column address unaltered. For a design using a prefetch of two data accesses per cycle, the column address would be advanced once for every two active edges of the /CAS signal. Prefetch architectures where more than two data words are accessed are also possible.

Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access may require more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory will approach one access per cycle, but the data out of the memory may be offset by a number of cycles due to the pipeline length and/or the desired latency from /CAS.

In the burst access memory device, each new column address from the column address counter is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16. This burst sequence of data will continue for each /CAS falling edge until a predetermined number of data accesses equal to the burst length has occurred. A /CAS falling edge received after the last burst address has been generated will latch another column address from the address inputs 16 and a new burst sequence will begin. Read data is latched and output with each falling edge of /CAS after the first /CAS latency.

For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the /CAS signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is preferred. Additional input data words for storage at incremented column address locations are latched by /CAS on successive /CAS pulses. Input data from the input latches 34 is passed along data path 32 to the memory array where it is stored at the location selected by the row and column address decoders. As is the burst read cycle previously described, a predetermined number of burst access writes will occur without the requirement of additional column addresses being provided on the address lines 16. After the predetermined number of burst writes has occurred, a subsequent /CAS pulse will latch a new beginning column address, and another burst read or write access will begin.

The memory device of FIG. 1 may include the option of switching between burst EDO and standard EDO modes of operation. In this case, the write enable signal /WE 36 may be used at the row address latch time (/RAS falling, /CAS high) to determine whether memory accesses for that row will be burst or page mode cycles. If /WE is low when /RAS falls, burst access cycles are selected. If /WE is high at /RAS falling, standard extended data out (EDO) page mode cycles are selected. Both the burst and EDO page mode cycles allow for increased memory device operating frequencies by not requiring the data output drivers 34 to place the data lines 10 in a high impedance state between data read cycles while /RAS is low. DRAM control circuitry 38, in addition to performing standard DRAM control functions, controls the I/O circuitry 34 and the column address counter/latch 26 in accordance with the mode selected by /WE when /RAS falls. In a burst mode only DRAM, or in a device designed with an alternate method of switching between burst and non-burst access cycles, the state of /WE when /RAS falls may be used to switch between other possible modes of operation such as interleaved versus linear addressing modes.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by /CAS. /WE low at the column address latch time selects a burst write access. /WE high at the column address latch time selects a burst read access. The level of the /WE signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on /WE within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. Transitions of the /WE signal may be locked out during critical timing periods within an access cycle in order to reduce the possibility of triggering a false write cycle. After the critical timing period the state of /WE will determine whether a burst access continues, is initiated, or is terminated. Termination of a burst access resets the burst length counter and places the DRAM in a state to receive another burst access command. Both /RAS and /CAS going high during a burst access will also terminate the burst access cycle placing the data drivers in a high impedance output state, and resetting the burst length counter. Read data may remain valid at the device outputs if /RAS alone goes high while /CAS is active for compatibility with hidden refresh cycles, otherwise /RAS high alone may be used to terminate a burst access. A minimum write enable pulse width is only required when it is desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses. In the case of burst reads, /WE will transition from high to low to terminate a first burst read, and then /WE will transition back high prior to the next falling edge of /CAS in order to specify a new burst read cycle. For burst writes, /WE would transition high to terminate a current burst write access, then back low prior to the next falling edge of /CAS to initiate another burst write access.

A basic implementation of the device of FIG. 1 may include a fixed burst length of 4, a fixed /CAS latency of 2 and a fixed interleaved sequence of burst addresses. This basic implementation requires very little additional circuitry to the standard EDO page mode DRAM, and may be mass produced to provide the functions of both the standard EDO page mode and burst EDO DRAMs. This device also allows

for the output enable pin (/OE) to be grounded for compatibility with many SIMM module designs. When not disabled (tied to ground), /OE is an asynchronous control which will prevent data from being driven from the part in a read cycle if it is inactive (high) prior to /CAS falling and remains inactive beyond /CAS rising. If these setup and hold conditions are not met, then the read data may be driven for a portion of the read cycle. It is possible to synchronize the /OE signal with /CAS, however this would typically increase the /CAS to data valid delay time and does not allow for the read data to be disabled prior to /RAS high without an additional /CAS low pulse which would otherwise be unnecessary. In a preferred embodiment, if /OE transitions high at any time during a read cycle the outputs will remain in a high impedance state until the next falling edge of /CAS despite further transitions of the /OE signal.

Programmability of the burst length, /CAS latency and address sequences may be accomplished through the use of a mode register 40 which latches the state of one or more of the address input signals 16 or data signals 10 upon receipt of a write-/CAS-before-/RAS (WCBR) programming cycle. In such a device, outputs 44 from the mode register control the required circuits on the DRAM. Burst length options of 2, 4, 8 and full page as well as /CAS latencies of 1, 2 and 3 may be provided. Other burst length and latency options may be provided as the operating speeds of the device increase, and computer architectures evolve. The device of FIG. 1 includes programmability of the address sequence by latching the state of the least significant address bit during a WCBR cycle. The burst length and /CAS latency for this particular embodiment are fixed. Other possible alterations in the feature sets of this DRAM include having a fixed burst mode only, selecting between standard fast page mode (non-EDO) and burst mode, and using the output enable pin (/OE) 42 in combination with /RAS to select between modes of operation. Also, a WCBR refresh cycle could be used to select the mode of operation rather than a control signal in combination with /RAS. A more complex memory device may provide additional modes of operation such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of /WE and /OE at /RAS falling time. One mode from a similar set of modes may be selected through the use of a WCBR cycle using multiple address or data lines to encode the desired mode. Alternately, a device with multiple modes of operation may have wire bond locations, or programmable fuses which may be used to program the mode of operation of the device.

A preferred embodiment of a sixteen bit wide burst EDO mode DRAM designed in accordance with the teachings of this invention has two column address strobe input pins /CASH and /CASL. For read cycles only /CASL needs to toggle. /CASH is may be high or may toggle with /CASL during burst read cycles, all sixteen data bits will be driven out of part during a read cycle even if /CASH remains inactive. In a typical system application, a microprocessor will read all data bits on a data bus in each read cycle, but may only write certain bytes of data in a write cycle. Allowing one of the /CAS control signals to remain static during read cycles helps to reduce overall power consumption and noise within the system. For burst write access cycles, each of the /CAS signals (CASH and /CASL) acts as a write enable for an eight bit width of the data. All sixteen data inputs will be latched when the first of the /CAS signals transitions low. If only one /CAS signal transitions low, then the eight bits of data associated with the /CAS that remained high will not be stored in the memory.

The present invention has been described with reference to several preferred embodiments. Just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including×1,×4,×8 and ×16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the memory device of the present invention may take the form of many different memory organizations. It is believed that one who is skilled in the art of integrated circuit memory design can, with the aide of this specification design a variety of memory devices which do not depart from the spirit of this invention. It is therefore believed that detailed descriptions of the various memory device organizations applicable to this invention are not necessary.

FIG. 3 shows a preferred pinout for the device of FIG. 1. It should be noted that the pinout for this new burst EDO memory device is identical to the pinout for a standard EDO DRAM. The common pinout allows this new device to be used in existing memory designs with minimum design changes. The common pinout also allows for ease of new designs by those of skill in the art who are familiar with the standard EDO DRAM pinout. Variations of the described invention which maintain the standard EDO DRAM pinout include driving the /CAS pin with a system clock signal to synchronize data access of the memory device with the system clock. For this embodiment, it may be desirable to use the first /CAS active edge after /RAS falls to latch the row address, a later edge may be used to latch the first column address of a burst access cycle. After row and column addresses are latched within the device, the address may be incremented internally to provide burst access cycles in synchronization with the system clock. Other pin function alternatives include driving the burst address incrementing signal on the /OE pin since the part does not require a data output disable function on this pin. Other alternate uses of the /OE pin also allow the device to maintain the standard EDO pinout, but provide increased functionality such as burst mode access. The /OE pin may be used to signal the presence of a valid column starting address, or to terminate a burst access. Each of these embodiments provides for a high speed burst access memory device which may be used in current memory systems with a minimum amount of redesign.

FIG. 4 is a timing diagram for performing a burst read followed by a burst write of the device of FIG. 1. In FIG. 4, a row address is latched by the /RAS signal. /WE is low when /RAS falls for an embodiment of the design where the state of the /WE pin is used to specify a burst access cycle at /RAS time. Next, /CAS is driven low with /WE high to initiate a burst read access, and the column address is latched. The data out signals (DQ's) are not driven in the first /CAS cycle. On the second falling edge of the /CAS signal, the internal address generation circuitry advances the column address and begins another access of the array, and the first data out is driven from the device after a /CAS to data access time (tCAC). Additional burst access cycles continue, for a device with a specified burst length of four, until the fifth falling edge of /CAS which latches a new column address for a new burst read access. /WE falling in the fifth /CAS cycle terminates the burst access, and initializes the device for additional burst accesses. The sixth falling edge of /CAS with /WE low is used to latch a new burst address, latch input data and begin a burst write access of the device. Additional data values are latched on successive /CAS falling edges until /RAS rises to terminate the burst access.

FIG. 5 is a timing diagram depicting burst write access cycles followed by burst read cycles. As in FIG. 4, the /RAS

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signal is used to latch the row address. The first /CAS falling edge in combination with /WE low begins a burst write access with the first data being latched. Additional data values are latched with successive /CAS falling edges, and the memory address is advanced internal to the device in either an interleaved or sequential manner. On the fifth /CAS falling edge a new column address and associated write data are latched. The burst write access cycles continue until the /WE signal goes high in the sixth /CAS cycle. The transition of the /WE signal terminates the burst write access. The seventh /CAS low transition latches a new column address and begins a burst read access (/WE is high). The burst read continues until /RAS rises terminating the burst cycles.

It should be noted from FIGS. 3 and 4, that for burst read cycles the data remains valid on the device outputs as long as the /OE pin is low, except for brief periods of data transition. Also, since the /WE pin is low prior to or when /CAS falls, the data input/output lines are not driven from the part during write cycles, and the /OE pin is a "don't care". Only the /CAS signal and the data signals toggle at relatively high frequency, and no control signals other than /CAS are required to be in an active or inactive state for one /CAS cycle time or less. This is in contrast to SDRAMs which often require row address strobes, column address strobes, data mask, and read/write control signals to be valid for one clock cycle or less for various device functions. Typical DRAMs also allow for the column address to propagate through to the array to begin a data access prior to /CAS falling. This is done to provide fast data access from /CAS falling if the address has been valid for a sufficient period of time prior to /CAS falling for the data to have been accessed from the array. In these designs an address transition detection circuit is used to restart the memory access if the column address changes prior to /CAS falling. This method actually requires additional time for performing a memory access since it must allow for a period of time at the beginning of each memory cycle after the last address transition to prepare for a new column address. Changes in the column address just prior to /CAS falling may increase the access time by approximately five nanoseconds. An embodiment of the present invention will not allow the column address to propagate through to the array until after /CAS has fallen. This eliminates the need for address transition detection circuitry, and allows for a fixed array access relative to /CAS.

FIG. 6 is a schematic representation of a single in-line memory module (SIMM) designed in accordance with the present invention. The SIMM has a standard SIMM module pinout for physical compatibility with existing systems and sockets. Functional compatibility with EDO page mode SIMMs is maintained when each of the 2 Meg×8 memory devices 10, 12, 14 and 16 are operated in an EDO page mode. Each of the /CAS signals 18, 20, 22 and 24 control one byte width of the 32 bit data bus 26, 28, 30 and 32. A /RAS 34 signal is used to latch a row address in each of the memory devices, and is used in combination with /WE 36 to select between page mode and burst mode access cycles. Address signals 38 provide a multiplexed row and column address to each memory device on the SIMM. In burst mode, only active /CAS control lines are required to toggle at the operating frequency of the device, or at half the frequency if each edge of the /CAS signal is used as described above. The data lines are required to be switchable at half of the frequency of the /CAS lines or at the same frequency, and the other control and address signals switch at lower frequencies than /CAS and the data lines. As shown in FIG. 6, each /CAS signal and each data line is connected to a single memory device allowing for higher frequency switching than the other control and address signals. Each of the memory devices 10, 12, 14 and 16 is designed in accordance with the present invention allowing for a burst mode of operation providing internal address generation for sequential or interleaved data access from multiple memory address locations with timing relative to the /CAS control lines after a first row and column address are latched.

FIG. 7 shows a front view of another SIMM designed in accordance with the present invention. Each device on the SIMM is a 4 Megabit DRAM organized as 1 Meg×4. In this configuration, a single /CAS controls two memory devices to provide access to a byte width of the data bus. The eight devices shown form a 4 Megabyte SIMM in a 32 bit width. For an 8 Megabyte SIMM in a 32 bit width, there are eight additional devices on the back side (not shown).

FIG. 8 shows a preferred pinout for a memory module designed in accordance with the device of FIG. 7. This pinout is compatible with pinouts for Fast Page Mode SIMMs and EDO SIMMs. A presence detect pin is provided for indication of EDO operation on pin 66, and in accordance with standard EDO part types, an /OE input is provided on pin 46.

Alternate embodiments of the SIMM modules of FIGS. 5, 6 and 7 include the use of two /RAS signals with each controlling a sixteen bit width of the data bus in accordance with standard SIMM module pinouts. Four more 2M×8 EDO Burst Mode DRAMs may be added to the device of FIG. 6 to provide for a 4M×32 bit SIMM. Sixteen bit wide DRAMs may also be used, these will typically have two /CAS signals each of which controls an eight bit data width. The incorporation of parity bits, or error detection and correction circuitry provide other possible SIMM module configurations. Methods of performing error detection and/or correction are well known to those of skill in the art, and detailed descriptions of such circuits are not provided in this application. Additional SIMM designs using the novel memory device of the present invention may be designed by one of skill in the art with the aid of this specification. The invention has been described with reference to SIMM designs, but is not limited to SIMMs. The invention is equally applicable to other types of memory modules including Dual In-Line Memory Modules (DIMMs) and Multi-Chip Modules (MCMs).

What is claimed is:

1. A method of accessing a further memory element of a memory device, the memory device having an array of memory elements, where one of the elements has been identified and accessed, the memory device includes an address latch, an address counter, an address strobe node for receiving a column address strobe, and an output data, the method comprising:

providing the address of the further element from within the memory device and accessing the further element, in response to a transition of an address latch signal the step of providing the address further comprising the sub-steps of:

applying a first column address strobe to the address strobe node for latching a first column address;

accessing a first memory element of the array of memory elements at the first column address;

applying a second column address strobe to the address strobe node for advancing

the column address within the memory device to specify a second column address;

accessing a second memory element of the array of memory elements at the second column address;

switching data driven to an external data node from a logic low level to a logic high level in response to a single transition of the column address strobe; and

maintaining a high impedance state on the output data driver at least until said step of applying the second column address strobe.

2. The method of claim 1, further comprising:

driving data from the one element of the memory device after a plurality of transitions of the address latch signal.

3. The method of claim 1, further comprising the steps of:

applying a third column address strobe to the address strobe node for advancing the column address to specify a third column address; and

latching an output of the memory device from the first column address in synchronization with the third column address strobe.

4. The method of claim 3, further comprising the step of:

selecting a burst mode of operation of the memory device prior to said applying the first column address strobe.

* * * * *

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United States Patent [19]

Merritt et al.

[11] **Patent Number: 5,706,247**

[45] **Date of Patent: Jan. 6, 1998**

[54] **SELF-ENABLING PULSE-TRAPPING CIRCUIT**

[75] Inventors: **Todd Merritt**, Boise; **Brett Williams**, Eagle, both of Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **754,308**

[22] Filed: **Nov. 21, 1996**

Related U.S. Application Data

[63] Continuation of Ser. No. 568,358, Dec. 6, 1995, Pat. No. 5,640,364, which is a continuation-in-part of Ser. No. 370, 761, Dec. 23, 1994, Pat. No. 5,526,320.

[51] **Int. Cl.⁶** **G11C 8/00**

[52] **U.S. Cl.** **365/233.5**; 365/233; 365/230.08

[58] **Field of Search** 365/233.5, 233, 365/230.08

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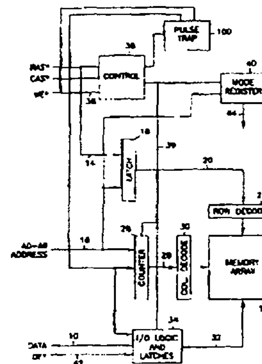
Primary Examiner—Tan T. Nguyen

Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

An integrated circuit memory device is described which can operate at high data speeds. The memory device can either store or retrieve data from the memory in a burst access operation. The burst operations latches a memory address from external address lines and internally generates additional memory addresses. An external input is used to terminate and change a burst operation. Circuitry is provided to monitor the external input during burst operations and provide an appropriate control signal.

18 Claims, 8 Drawing Sheets



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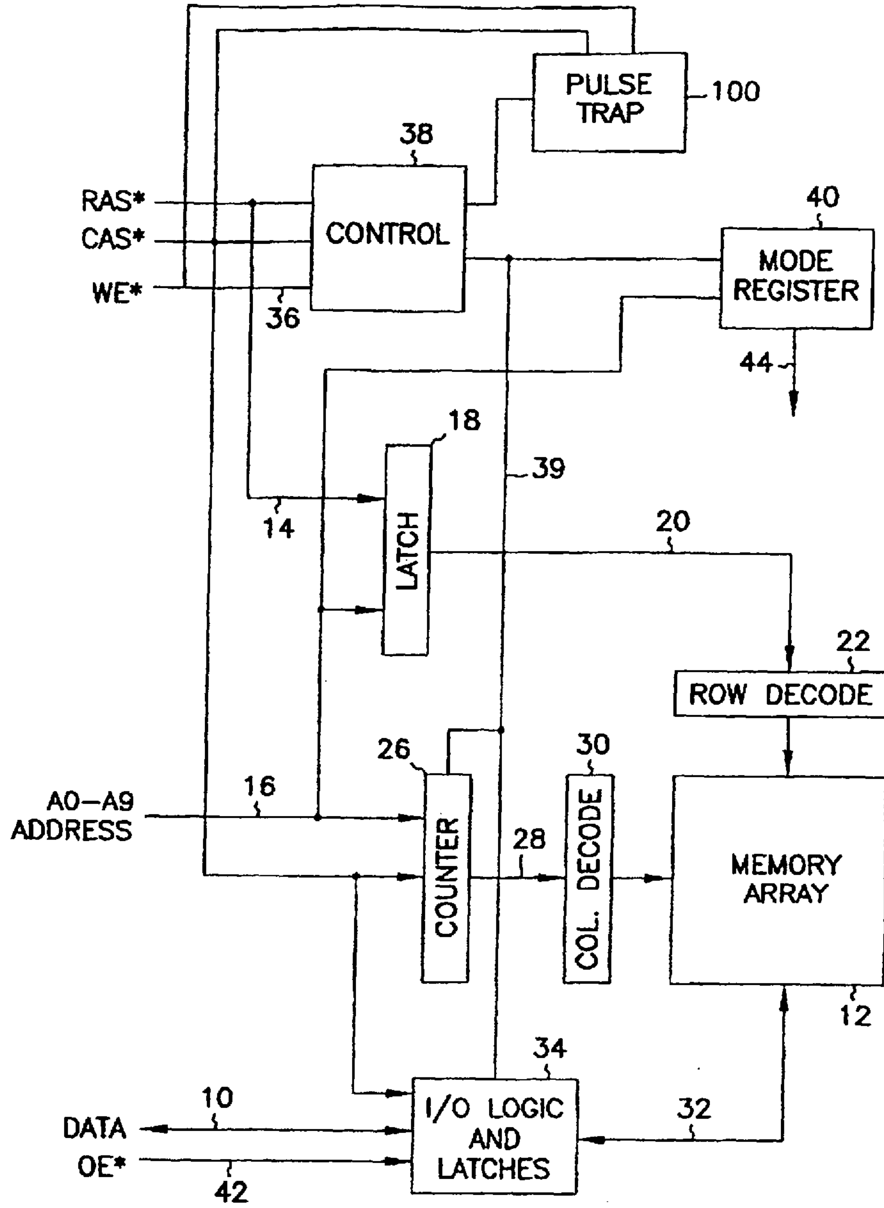

FIG. 1

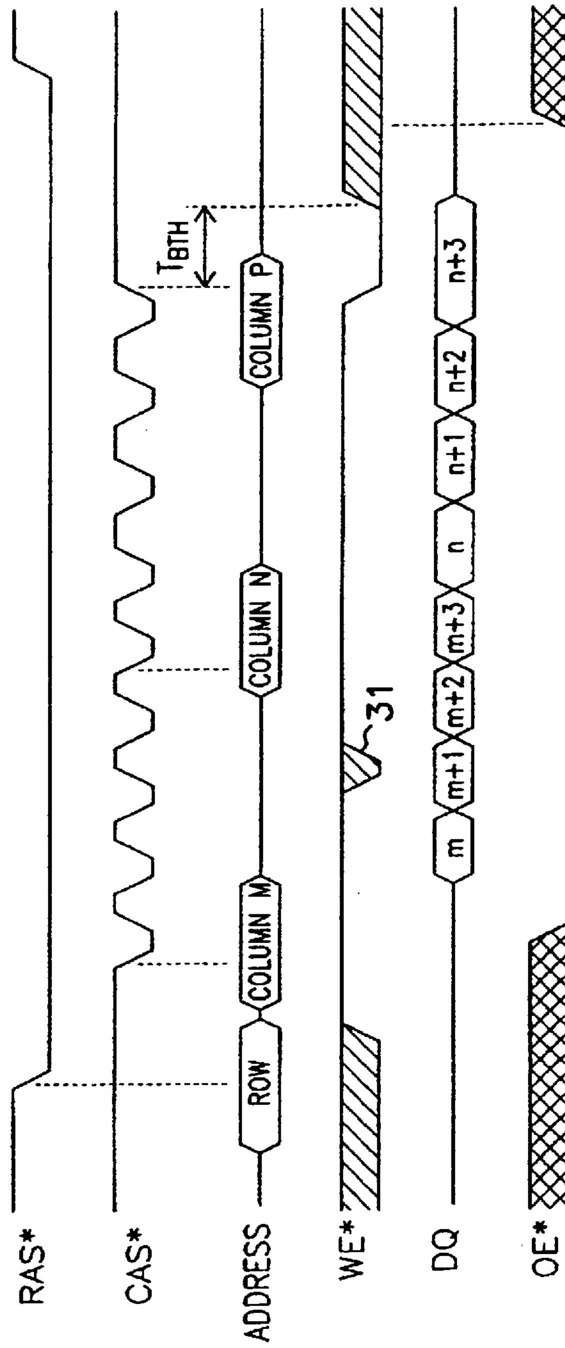

FIG. 2

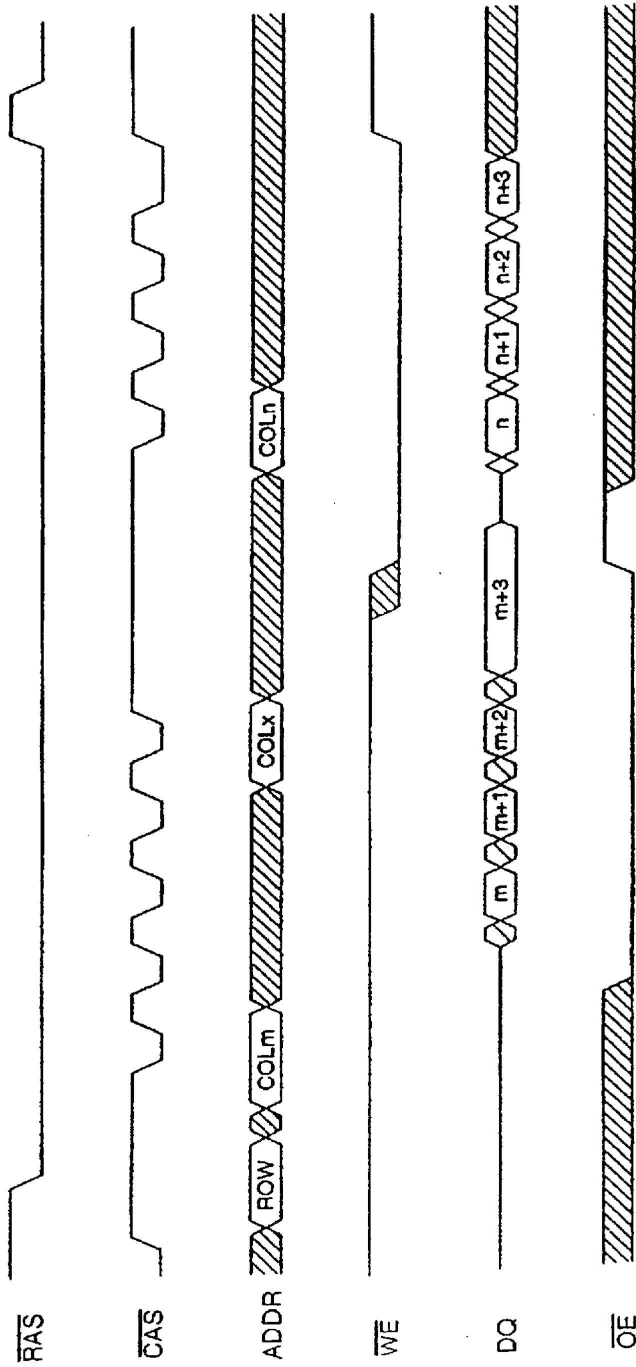

FIG. 3

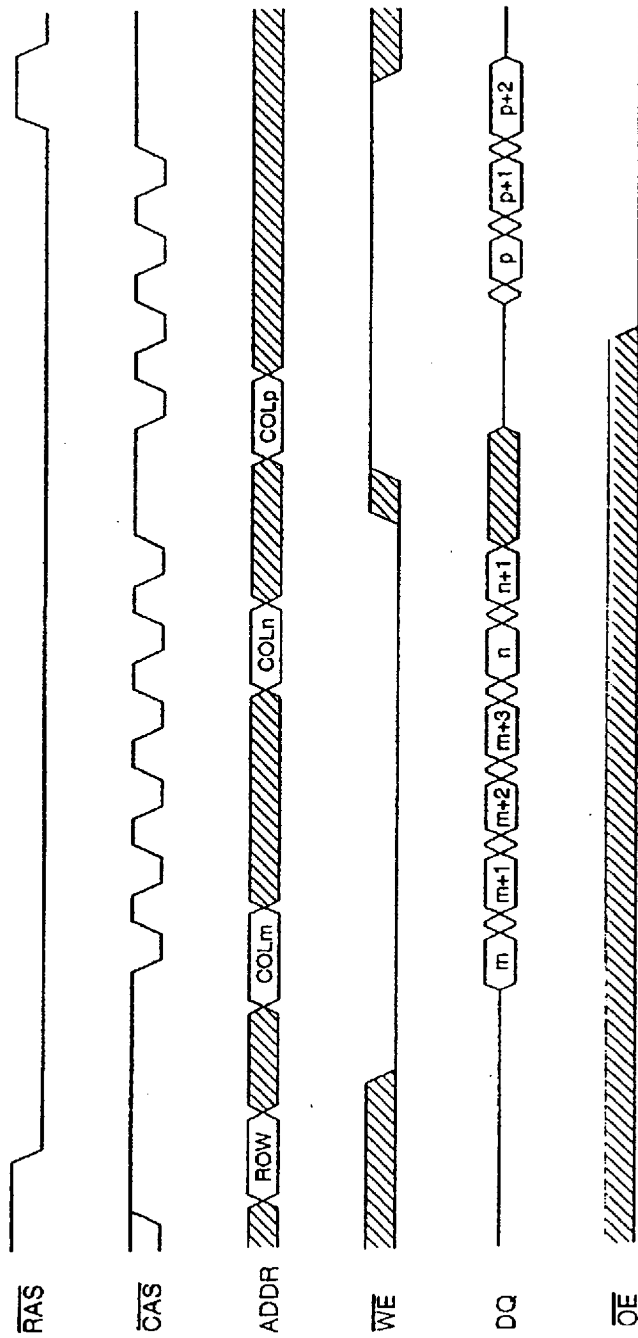

FIG. 4

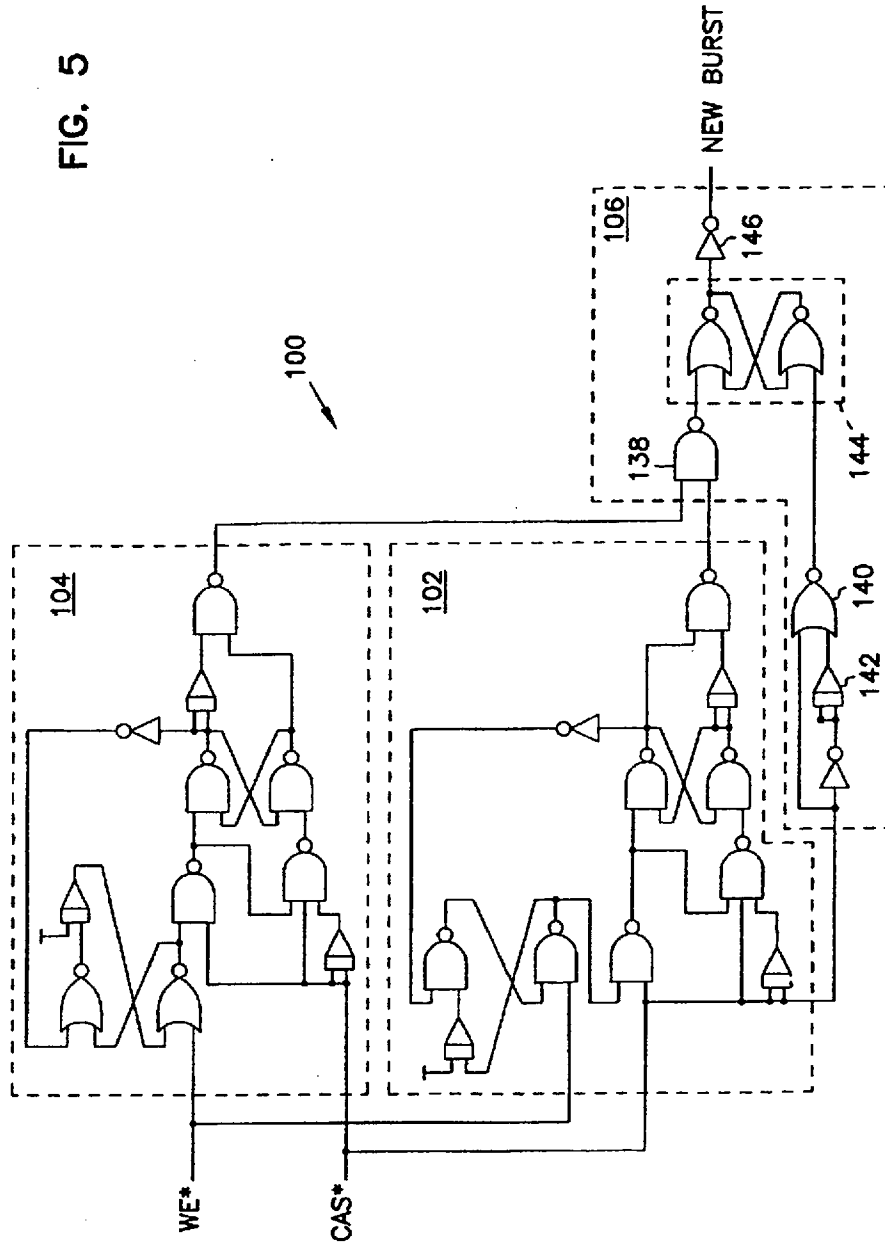
FIG. 5
100
NEW BURST
106
146
144
138
104
102
140
142
WE*
CAS*

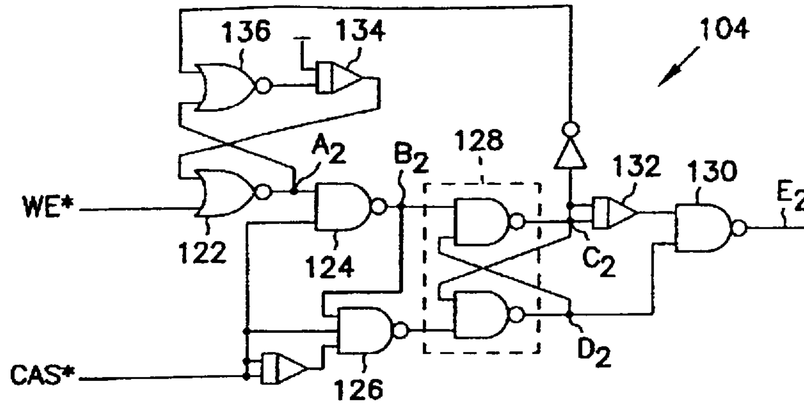

FIG. 6A

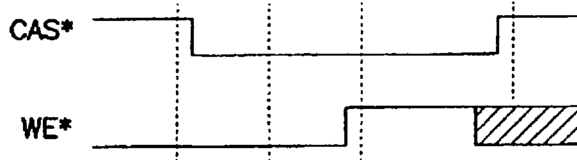

FIG. 6B

	WE* CAS* 0 1	0 0	1 0	X 1
A_2	1	1	0	0
B_2	0	1	1	1
C_2	1	1	1	0
D_2	0	0	0	1
E_2	1	1	1	˥_˥

FIG. 6C

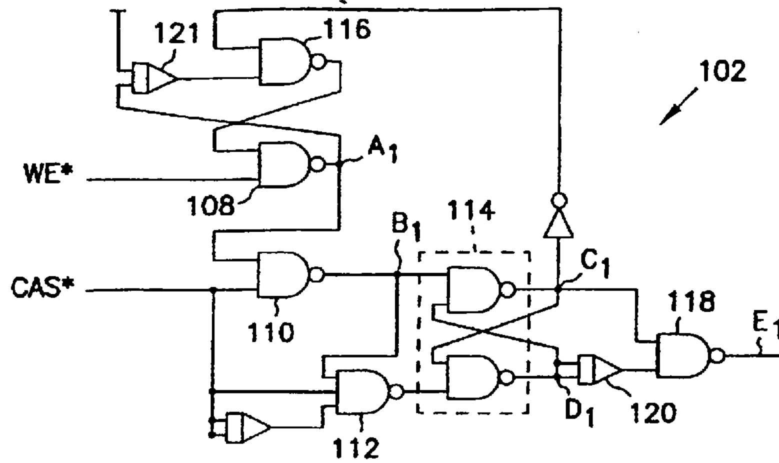

FIG. 7A

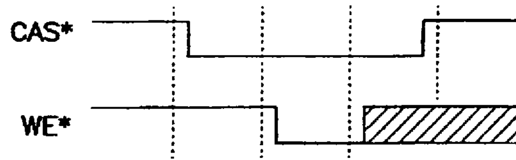

FIG. 7B

WE* CAS*	1 1	1 0	0 0	X 1
A_1	0	0	1	1
B_1	1	1	1	0
C_1	0	0	0	1
D_1	1	1	1	0
E_1	1	1	1	⊔

FIG. 7C

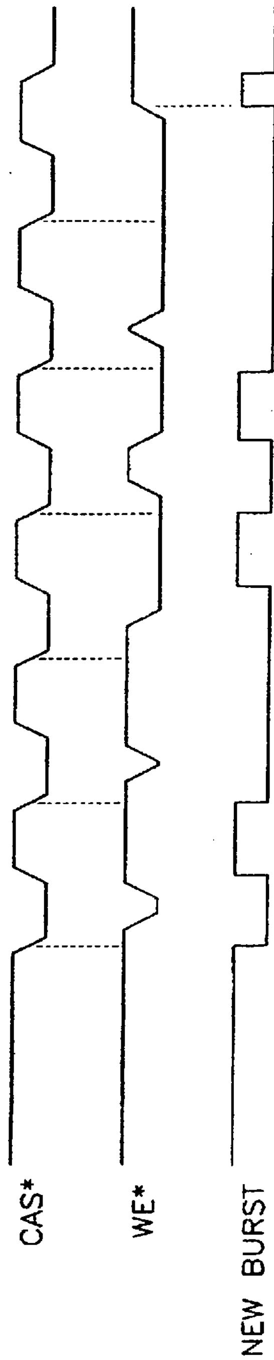

FIG. 8

SELF-ENABLING PULSE-TRAPPING CIRCUIT

This application is a continuation of application Ser. No. 08/568,358, filed Dec. 6, 1995, now issued as U.S. Pat. No. 5,640,364 on Jun. 17, 1997, which is a continuation-in-part of U.S. Ser. No. 08/370,761, filed Dec. 23, 1994, now U.S. Pat. No. 5,526,320.

TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to integrated circuit memories and in particular the present invention relates to a circuit and method of latching an input signal.

BACKGROUND OF THE INVENTION

There are a number of integrated circuit memories commercially available. For example, dynamic memory circuits having memory cells arranged to be accessed in a random fashion are referred to as dynamic random access memories, DRAMs. These memories can be produced in a variety of designs which provide different methods of reading from and writing to the dynamic memory cells. One such method is page mode operations. Page mode operations in a DRAM are defined by the method of accessing a row of a memory cell array and randomly accessing different columns of the array. Data stored at the row and column intersection can be output while that column is accessed. An alternate type of memory access is the extended data output (EDO) memory which allows data stored at a memory array address to be available as output after the addressed column has been closed. A more detailed description of a DRAM having EDO features is provided in the "1995DRAM Data Book" pages 1-1 to 1-30 available from Micron Technology, Inc. Boise, Id., the assignee of the present application and is incorporated herein by reference. Yet another type of operation is included in a burst EDO memory which adds the ability to address one column of a memory array and then automatically address additional columns in a pre-determined manner without providing the additional column addresses on external address lines.

In a burst memory, external inputs can be used to terminate a burst access operation. Timing and pulse width requirements are traditionally placed on signals provided on these external inputs. If the minimum timing or pulse width requirements placed on the external inputs are excessive, an error can occur when a short pulse width signal is provided on the input and a burst operation will not be terminated. For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a circuit which can monitor external inputs by reducing critical timing and substantially independent of signal pulse width.

SUMMARY OF THE INVENTION

The above mentioned problems with memory devices and other problems are addressed by the present invention and which will be understood by reading and studying the following specification. A latching circuit is described which monitors an external input for transitions during a burst access operation.

In particular, one embodiment of the present invention describes an integrated memory device comprising a control signal input for receiving a control signal, an address latch input for receiving an address latch signal, and a signal trapping circuit coupled to the control signal input and the address latch input and adapted to latch a transition in the control signal. The signal trapping circuit can comprise a low transition latch circuit to latch a high to low transition in the control signal when the address latch signal is activated, and a high transition latch circuit to latch a low to high transition in the control signal when the address latch signal is activated.

In another embodiment, an integrated memory circuit is described which can comprise a write enable input for receiving a write enable signal, an address latch input for receiving an address latch signal, and a signal trapping circuit coupled to the write enable input and the address latch input and adapted to latch a transition in the write enable signal. The signal trapping circuit comprises a low transition latch circuit to latch a high to low transition in the write enable signal when the address latch input is activated, a high transition latch circuit to latch a low to high transition in the write enable signal when the address latch input is activated, and a pulse generator circuit coupled to the low transition latch circuit and the high transition latch circuit to generate a pulse in response to an output of the low transition latch circuit and the high transition latch circuit.

In yet another embodiment, a method is described for latching a control signal in a memory circuit having a control signal input and an address latch input. The method comprises the steps of receiving an address latch signal on the address latch input, receiving a control signal on the control signal input, enabling a latch circuit in response to an active transition of the address latch signal, and latching a transition of the control signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a memory circuit incorporating the features of the present invention;

FIG. 2 is a timing diagram of a burst memory not including the features of the present invention;

FIG. 3 is a timing diagram of a burst read followed by burst write operation in the memory if FIG. 1;

FIG. 4 is a timing diagram of burst write access cycles followed by burst read cycles in the memory of FIG. 1;

FIG. 5 is a pulse trapping circuit of FIG. 1;

FIG. 6*a* is a low transition latch of the circuit of FIG. 5;

FIG. 6*b* is a timing diagram of the circuit of FIG. 6*a*;

FIG. 6*c* is a logic table of the timing diagram of FIG. 6*b*;

FIG. 7*a* is a high transition latch of the circuit of FIG. 5;

FIG. 7*b* is a timing diagram of the circuit of FIG. 7*a*;

FIG. 7*c* is a logic table of the timing diagram of FIG. 7*b*; and

FIG. 8 is a timing diagram of the circuit of FIG. 5.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting

sense, and the scope of the present inventions is defined only by the appended claims. The present invention can be implemented in any memory, but is particularly advantageous in a burst access memory.

BURST ACCESS MEMORY

FIG. 1 is a schematic representation of a sixteen megabit device designed in accordance with the present invention. The device is organized as a 2 Meg×8 Burst EDO DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array 12. The device of FIG. 1 may have an industry standard pinout for eight bit wide EDO DRAMs. An active-low row address strobe (RAS*) signal 14 is used to latch a first portion of a multiplexed memory address, from address inputs 16, in latch 18. The latched row address 20 is decoded in row decoder 22. The decoded row address is used to select a row of the memory array 12. A column address strobe (CAS*) signal 24 is used to latch a second portion of a memory address from address inputs 16 into address generation circuit 26. The latched column address 28 is decoded in column address decoder 30. The decoded column address is used to select a column of the memory array 12.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 32 to output latches. Data 10 driven from the burst EDO DRAM may be latched external to the device in synchronization with CAS* after a predetermined number of CAS* cycle delays (latency). For a two cycle latency design, the first CAS* falling edge is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second CAS* falling edge, and remains valid through the third CAS* falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during CAS* high intervals dependent on the state of the output enable and write enable (OE* and WE*) control lines, thus allowing additional time for the system to latch the output data. The data outputs remain valid throughout the burst read cycles with the exception of brief periods of data transition. During these periods of data transition, the output drivers may be turned off momentarily in order to aid data transition. This state of the output buffer should not be confused with the standard DRAM tri-state condition which is intended to release the data bus.

Once a row and a column address are selected, additional transitions of the CAS* signal are used to advance the column address within the address generation circuit in a predetermined sequence. The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the CAS* signal provided that OE* is maintained low, and WE* remains high. The output data signal levels may be but are not limited to being driven in accordance with standard CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

In the burst access memory device, each new column address from the address generation circuit is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16. This burst sequence of data will continue for each CAS* falling edge until a predetermined number of data accesses equal to the burst length has occurred. A CAS* falling edge received after the last burst address has been generated will latch another column address from the address inputs 16 and a new burst sequence will begin. Read data is latched and output with each falling edge of CAS* after the first CAS* latency.

For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the CAS* signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is preferred. Additional input data words for storage at incremented column address locations are latched by CAS* on successive CAS* pulses. Input data from the input latches 34 is passed along data path 32 to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes will occur without the requirement of additional column addresses being provided on the address lines 16. After the predetermined number of burst writes has occurred, a subsequent CAS* pulse will latch a new beginning column address, and another burst read or write access will begin.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by CAS*. WE* low at the column address latch time selects a burst write access. WE* high at the column address latch time selects a burst read access. The level of the signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state.

In a standard burst access memory device, the WE* signal required a minimum pulse width defined by time T_{BTH} following the rising edge of CAS* to terminate a burst access. For a memory not including the present invention, FIG. 2 illustrates both the minimum pulse width T_{BTH}, and a WE* low pulse 31 which is less that T_{BTH}. After the critical timing period, the state of WE* is used to determine whether a burst access continues, is initiated, or is terminated. A minimum write enable pulse width is only required when it is desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses.

Termination of a burst access places the DRAM in a state to receive another burst access command. Both RAS* and CAS* going high during a burst access will also terminate the burst access cycle and place the data drivers in a high impedance output state. Read data may remain valid at the device outputs if RAS* alone goes high while CAS* is active for compatibility with hidden refresh cycles, otherwise RAS* high alone may be used to terminate a burst access. In the case of burst reads, WE* will transition from high to low to terminate a first burst read, and then WE* will transition back high prior to the next falling edge of CAS* in order to specify a new burst read cycle. For burst writes, WE* would transition high to terminate a current burst write access, then back low prior to the next falling edge of CAS* to initiate another burst write access. A basic implementation of the device of FIG. 1 may include a fixed burst length of 4, a fixed CAS* latency of 2 and a programmable sequence of burst addresses.

This basic implementation requires very little additional circuitry to the standard EDO page mode DRAM, and may

be mass produced to provide the functions of both the standard EDO page mode and burst EDO DRAMs. This device also allows for the output enable pin (OE*) to be grounded for compatibility with many SIMM module designs. When not disabled (tied to ground), OE* is an asynchronous control which will prevent data from being driven from the part in a read cycle if it is inactive (high) prior to CAS* falling and remains inactive beyond CAS* rising. If these setup and hold conditions are not met, then the read data may be driven for a portion of the read cycle. It is possible to synchronize the OE* signal with CAS*, however this would typically increase the CAS* to data valid delay time and doesn't allow for the read data to be disabled prior to RAS* high without an additional CAS* low pulse which would otherwise be unnecessary. In a preferred embodiment, if OE* transitions high at any time during a read cycle the outputs will remain in a high impedance state until the next falling edge of CAS* despite further transitions of the OE* signal.

Programmability of the burst length, CAS* latency and address sequences may be accomplished through the use of a mode register 40. Burst length options of 2, 4, 8 and full page as well as CAS* latencies of 1, 2 and 3 may be provided. Other burst length and latency options may be provided as the operating speeds of the device increase, and computer architectures evolve. The burst length and CAS* latency for this particular embodiment are fixed. Other possible alterations in the feature sets of this DRAM include having a fixed burst mode only, selecting between standard fast page mode (non-EDO) and burst mode, and using the output enable (OE*) 42 in combination with RAS* to select between modes of operation. A more complex memory device may provide additional modes of operation such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of WE* and OE* at RAS* falling time. One mode from a similar set of modes may be selected. Alternately, a device with multiple modes of operation may have wire bond locations, or programmable fuses which may be used to program the mode of operation of the device.

The present invention is described with reference to several preferred embodiments. Just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including ×1, ×4, ×8 and ×16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the memory device of the present invention may take the form of many different memory organizations. It is believed that one who is skilled in the art of integrated circuit memory design can, with the aide of this specification design a variety of memory devices which do not depart from the spirit of this invention. It is therefore believed that detailed descriptions of all of the various memory device organizations applicable to this invention are not necessary.

FIG. 3 is a timing diagram for performing a burst read followed by burst write of the device of FIG. 1. In FIG. 3, a row address is latched by the RAS* signal. WE* is low when RAS* falls for an embodiment of the design where the state of the WE* pin is used to specify a burst access cycle at RAS* time. Next, CAS* is driven low with WE* high to initiate a burst read access, and the column address is latched. The data out signals (DQ's) are not driven in the first CAS* cycle. On the second falling edge of the CAS* signal the first data out is driven from the device after a CAS* to data access time (tCAC). Additional burst access cycles continue, for a device with a specified burst length of four, until the fifth falling edge of CAS* which latches a new column address for a new burst read access. WE* falling in the fifth CAS* cycle terminates the burst access, tri-states the data bus, and initializes the device for additional burst accesses. The sixth falling edge of CAS* with WE* low is used to latch a new burst address, latch input data and begin a burst write access of the device. Additional data values are latched on successive CAS* falling edges until RAS* rises to terminate the burst access.

FIG. 4 is a timing diagram depicting burst write access cycles followed by burst read cycles. As in FIG. 3, the RAS* signal is used to latch the row address. WE* is shown as a "don't care" at the time RAS* falls for an embodiment of the present invention that does not utilize the state of WE* at RAS* time to select between burst and non-burst access modes. The first CAS* falling edge in combination with WE* low begins a burst write access with the first data being latched. Additional data values are latched with successive CAS* falling edges, and the memory address is advanced internal to the device in either an interleaved or sequential manner which has been previously programmed. On the fifth CAS* falling edge a new column address and associated write data are latched. The burst write access cycles continue until the WE* signal goes high in the sixth CAS* cycle. The transition of the WE* signal terminates the burst write access. The seventh CAS* low transition latches a new column address and begins a burst read access (WE* is high). The burst read continues until RAS* rises terminating the burst cycles.

It should be noted from FIGS. 3 and 4, that for burst read cycles the data remains valid on the device outputs as long as the OE* pin is low, except for brief periods of data transition. Also, since the WE* pin is low prior to or when CAS* falls, the data input/output lines are not driven from the part during write cycles, and the OE* pin may be grounded. Only the CAS* signal and the data signals toggle at relatively high frequency, and no control signals other than CAS* are required to be in an active or inactive state for one CAS* cycle time or less.

PULSE TRAPPING CIRCUIT

It will be appreciated that the critical timing and minimum pulse width requirement of T_{WTH} on the WE* input can unnecessarily slow the operation of the memory circuit. The elimination of this requirement can be accomplished by including the pulse trapping circuit 100 shown in detail in FIG. 5. The pulse trapping circuit operates to latch either a high transition or a low transition in the WE* signal while CAS* is low. The transition which is latched will depend upon the state of the WE* signal when the CAS* signal transitions low. That is, if WE* is high when CAS* goes low, the pulse trapping circuit will look for and latch a low transition in WE*. If WE* is low when CAS* goes low, the pulse trapping circuit will look for and latch a high transition in WE*.

The pulse trapping circuit 100 includes low transition latch 102, high transition latch 104, and a NEW BURST pulse generator 106. The low transition latch 102 is described in detail with reference to FIGS. 7*a*, 7*b*, and 7*c*. At an initial time when both CAS* and WE* are high, the output of NAND gate 108 (node A_1) would be stabilized at a low logic state (0). The output of NAND gate 110 (Node B_1), therefore, is a high logic state (1). NAND gate 112 in response produces a low output. The outputs of flip-flop 114, Nodes C_1 and D_1, are low and high, respectively. The output, Node E_1, of the low transition latch 102 will be normally high. When the CAS* signal transitions low, NAND gates 110 and 112 are "enabled". That is, Node B_1 will remain high

regardless of the state of Node A_1, and the output of NAND 112 will change to high. With both inputs to flip-flop 114 high, nodes C_1 and D_1 will remain in their prior state. If the WE* signal transitions low while the CAS* signal is low, Node A_1 will latch to a high state and remain at that state even if WE* returns high. When CAS* transitions high, Node B_1 will go low, and Nodes C_1 and D_1 will go high and low, respectively. Delay element 120 will maintain a high output such that both inputs to NAND gate 118 are high. Node E_1, therefore, will pulse low. The length of the pulse is directly dependent upon the length of delay element 120. Thus, low transition latch 102 produces a low pulse if WE* transitions low when CAS* is low. Delay element 121 is included between Node A_1 and NAND gate 116 as a filter for the WE* signal. If WE* pulses low for a time period less than the delay time, Node A_1 will not latch high. This delay therefore reduces the chance that noise on the WE* line will trigger the latch.

The high transition latch 104 is described in detail with reference to FIG. 6a, 6b and 6c. In an initial state when CAS* is high and WE* is low, the output (Node A_2) of NOR gate 122 will be stabilized at a high state (1). NAND gate 124 will hold Node B_2 low. Flip-Flop 128 will, therefore, pull Node C_2 high and hold Node D_2 low. When CAS* transitions low, Node B_2 is held high regardless of the state of Node A_2. Both inputs to flip-flop 128 will be high, and Nodes C_2 and D_2 will remain at their prior states. If WE* transitions high while CAS* is low, Node A_2 will latch low and remain there even if WE* returns low. The output of NAND gate 126 will go low when CAS* transitions high. Nodes C_2 and D_2 will, therefore, go low and high, respectively. Delay element 132 will maintain a high output such that both inputs to NAND gate 130 are high. Node E_2, therefore, will pulse low. The length of the pulse is directly dependent upon the length of delay element 132. Thus, high transition latch 104 produces a low pulse if WE* transitions high when CAS* is low. Delay element 134 is included between NOR gate 136 and NOR gate 122 as a filter for the WE* signal. If WE* pulses high for a time period less than the delay time. Node A_1 will not latch low. This delay therefore reduces the chance that noise on the WE* line will trigger the latch.

Pulse trapping circuit 100 enables either low transition latch 102 or high transition latch 104 when CAS* goes low. If the enabled latch circuit 102 or 104 detects a transition in the WE* signal a low pulse is produced on Node E when the CAS* signal transitions high. NEW BURST pulse generator 106, shown in FIG. 5, is included with the pulse trapping circuit to produce a signal indicating that a new burst access is to be initiated. As stated above, a current burst is to be terminated and a new burst initiated on a CAS* rising transition when the WE* signal transitions states. The NEW BURST signal will pulse high on a CAS* high transition if either E_1 or E_2 are low. That is, if either E_1 or E_2 are low the output of NAND gate 138 will be high. Because the output of NOR gate 140 is normally low, flip-flop 144 will force NEW BURST high via inverter 146. If E_1 and E_2 are high, NEW BURST will remain low. To reset the latch when CAS* goes low, the output of NOR gate 140 pulses high in response to a CAS* low transition. The high pulse length is dictated by delay element 142.

FIG. 8 illustrates the operation of the pulse trapping circuit. On the first CAS* falling edge WE* is high. The low transition latch 102 latches a low pulse such that NEW BURST goes high on the rising edge of CAS*. The current burst operation is terminated and a new burst read is initiated. NEW BURST will return low on the falling edge of CAS* and remain low until the third rising edge of CAS*. The short pulse on WE* is filtered by delay element 121 and NEW BURST is not pulsed. The third CAS* rising edge terminates the burst read operation and initiates a burst write operation. The fourth CAS* falling edge enables the high transition latch circuit 104. A NEW BURST high pulse is produced on the next CAS* rising edge in response to the WE* high pulse. Again, the short WE* pulse is filtered by delay element 134 such that noise on the WE* line does not trigger the latch. Further, if WE* transitions while CAS* is high a NEW BURST signal will be immediately produced, as illustrated in FIG. 8. This provides a direct control of new memory access burst without waiting for a CAS* low transition.

Conclusion

A memory circuit has been described which has burst access capabilities. A write enable signal (WE*) provided on a WE* input can be used to terminate a burst access operation. To facilitate a fast burst termination, circuitry has been described which latches a transition in the WE* line when CAS* is low. The circuitry enables one of two latches based upon the state of WE* when CAS* transitions low. If WE* pulses during the CAS* cycle a NEW BURST signal is produced. The NEW BURST signal is used to terminate a current burst access operation and initiate a new burst read or write operation.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. An integrated memory device comprising:

a control signal input for receiving a control signal;

an address latch input for receiving an address latch signal; and

a signal trapping circuit coupled to the control signal input and the address latch input and adapted to latch a transition in the control signal.

2. An integrated memory device comprising:

a control signal input for receiving a control signal;

an address latch input for receiving an address latch signal; and

a signal trapping circuit coupled to the control signal input and the address latch input and adapted to latch a transition in the control signal, wherein the signal trapping circuit comprises a high transition latch circuit to latch a low to high transition in the control signal when the address latch signal is activated, the high transition latch circuit comprises:

a first flip-flop circuit having first and second inputs, and an output, the first input is coupled to the control signal input,

a first logic gate having a first input connected to the output of the first flip-flop circuit, a second input connected to the address latch input, and an output;

a second flip-flop circuit having a first input connected to the output of the first logic gate, a second input, and first and second outputs;

a second logic gate having an output connected to the second input of the second flip-flop circuit, a first input

connected to the output of the first logic gate, and a second input connected to the address latch input;

a feedback circuit connected to the first output of the second flip-flop circuit and the second input of the first flip-flop circuit; and

an output circuit connected to the first and second outputs of the second flip-flop circuit.

3. The integrated memory of claim 2 further comprising:

a filter circuit coupled to the first flip-flop circuit for filtering a high pulse in the control signal which has a duration less than a predetermine time.

4. The integrated memory of claim 3 wherein the filter circuit is a delay element.

5. The integrated memory of claim 2 wherein the first and second logic gates are NAND gates.

6. The integrated memory of claim 2 wherein the first flip-flop circuit comprises cross coupled NOR gates.

7. The integrated memory of claim 2 wherein the second flip-flop circuit comprises cross coupled NAND gates.

8. The integrated memory of claim 2 wherein the output circuit comprises:

a NAND gate having a first input coupled through a delay circuit to the first output of the second flip-flop circuit, and a second input connected to the second output of the second flip-flop circuit.

9. An integrated memory device comprising:

a control signal input for receiving a control signal;

an address latch input for receiving an address latch signal; and

a signal trapping circuit coupled to the control signal input and the address latch input and adapted to latch a transition in the control signal, wherein the signal trapping circuit comprises a low transition latch circuit to latch a high to low transition in the control signal when the address latch signal is activated, the low transition latch circuit comprises:

a first flip-flop circuit having first and second inputs, and an output, the first input is coupled to the control signal input,

a first logic gate having a first input connected to the output of the first flip-flop circuit, a second input connected to the address latch input, and an output;

a second flip-flop circuit having a first input connected to the output of the first logic gate, a second input, and first and second outputs;

a second logic gate having an output connected to the second input of the second flip-flop circuit, a first input connected to the output of the first logic gate, and a second input connected to the address latch input;

a feedback circuit connected to the first output of the second flip-flop circuit and the second input of the first flip-flop circuit; and

an output circuit connected to the first and second outputs of the second flip-flop circuit.

10. The integrated memory of claim 9 further comprising:

a filter circuit coupled to the first flip-flop circuit for filtering a low pulse in the control signal which has a duration less than a predetermine time.

11. The integrated memory of claim 10 wherein the filter circuit is a delay element.

12. The integrated memory of claim 9 wherein the first and second logic gates are NAND gates.

13. The integrated memory of claim 9 wherein the first flip-flop circuit comprises cross coupled NAND gates.

14. The integrated memory of claim 9 wherein the second flip-flop circuit comprises cross coupled NAND gates.

15. The integrated memory of claim 9 wherein the output circuit comprises:

a NAND gate having a first input coupled through a delay circuit to the second output of the second flip-flop circuit, and a second input connected to the first output of the second flip-flop circuit.

16. A method of latching a control signal in a memory circuit having control signal input and an address latch input, the method comprising the steps of:

receiving an address latch signal on the address latch input;

receiving a control signal on the control signal input;

enabling a latch circuit in response to an active transition of the address latch signal; and

latching a transition of the control signal.

17. The method of claim 16 further including the step of:

producing an output signal in response to the transition of the control signal.

18. The method of claim 16 where in the control signal is a write enable signal.

* * * * *

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United States Patent [19]

Manning

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[45] **Date of Patent:** **Feb. 10, 1998**

[54] **BURST EDO MEMORY DEVICE WITH MAXIMIZED WRITE CYCLE TIMING**

[75] Inventor: **Troy A. Manning**, Boise, Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

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[51] **Int. Cl.⁶** **G11C 7/00**

[52] **U.S. Cl.** **365/233.5**; 365/233; 365/189.05

[58] **Field of Search** 365/233.5, 233, 365/189.05, 189.01, 193, 230.01

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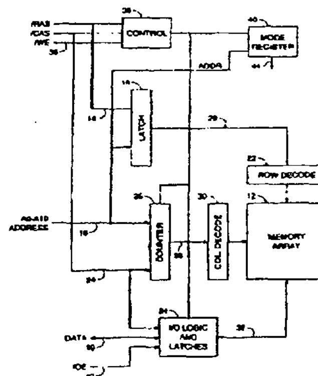
Primary Examiner—David C. Nelms
Assistant Examiner—Vu A. Le
Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

An integrated circuit memory device is designed for high speed data access and for compatibility with existing memory systems. An address strobe signal is used to latch a first address. During a burst access cycle the address is incremented internal to the device with additional address strobe transitions. A new memory address is only required at the beginning of each burst access. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at the device cycle frequency. A transition of the Read/Write control line during a burst access is used to terminate the burst access, reset the burst length counter and initialize the device for another burst access. Write cycle times are maximized to allow for increases in burst mode operating frequencies.

13 Claims, 8 Drawing Sheets



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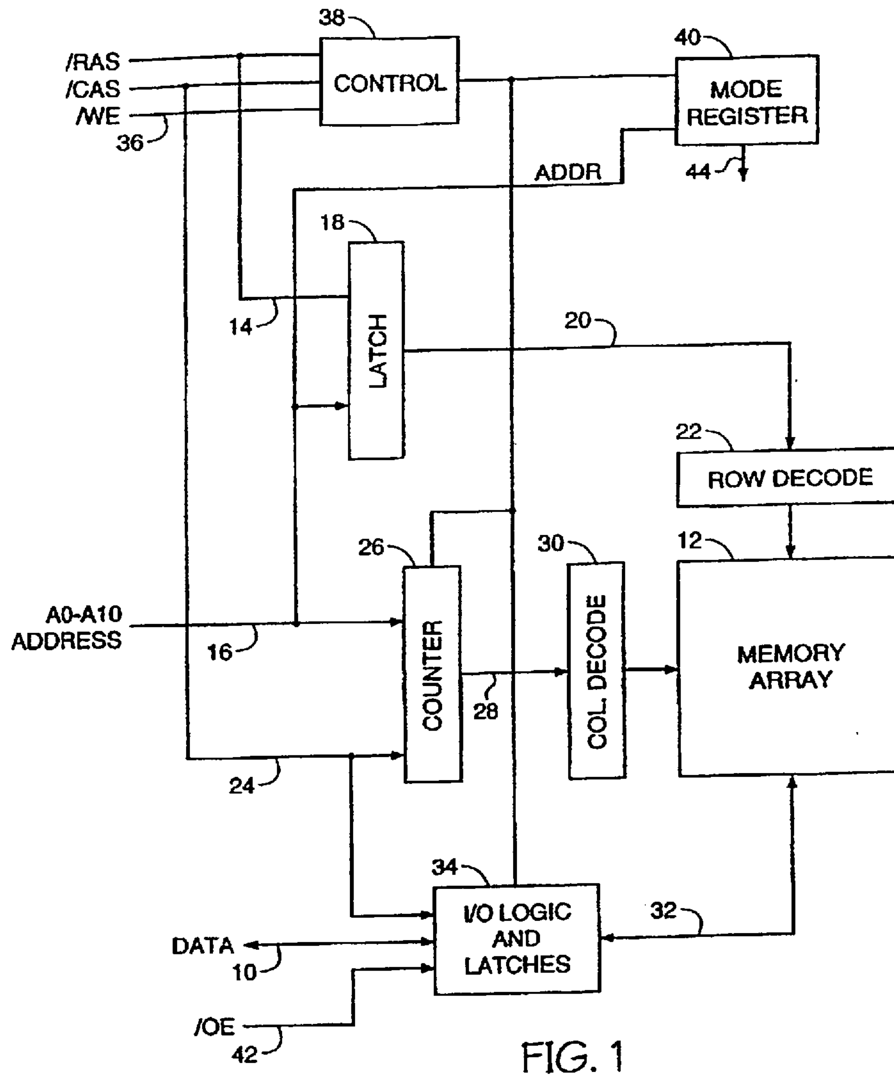

FIG. 1

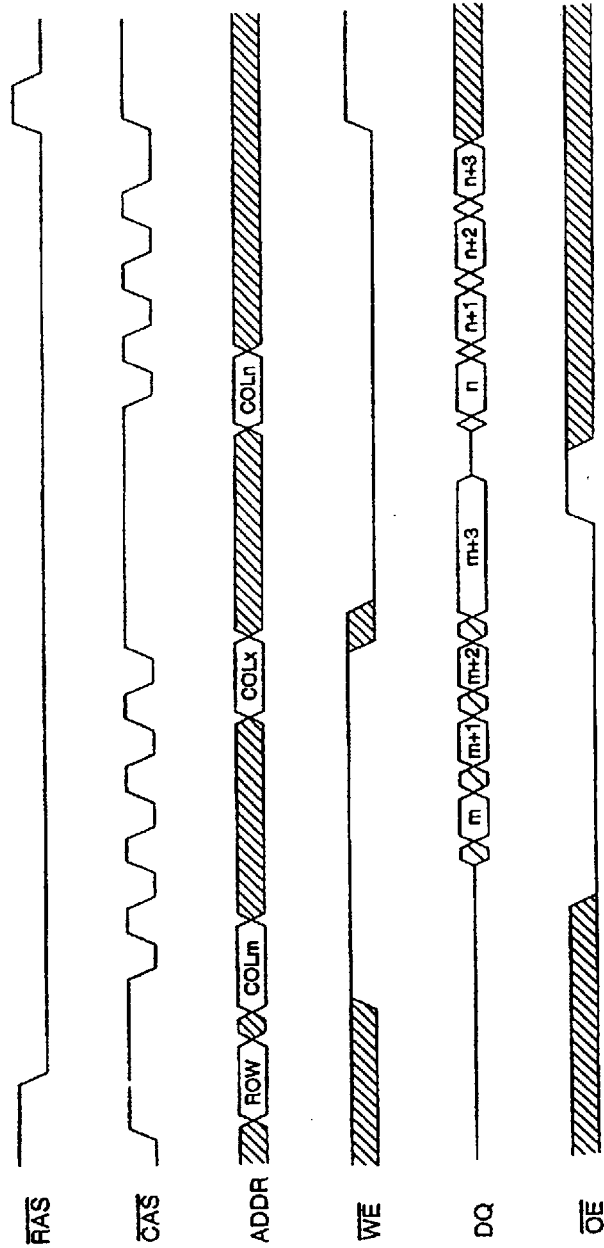

FIG. 2

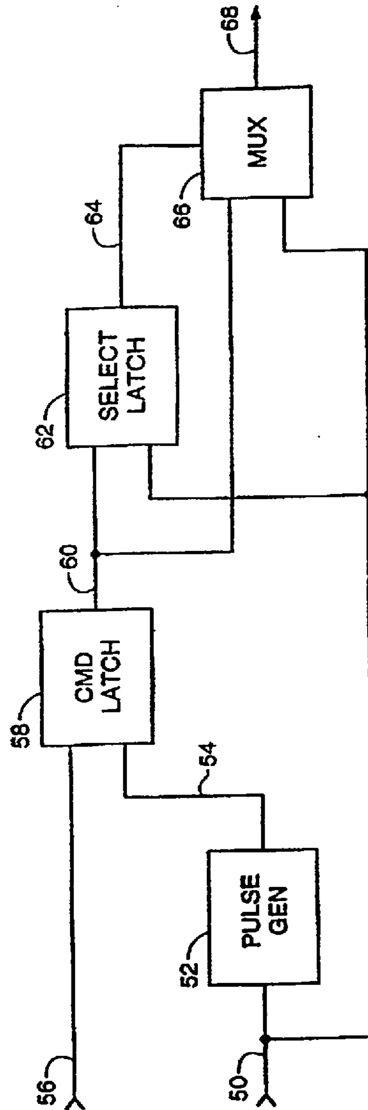

FIG. 3

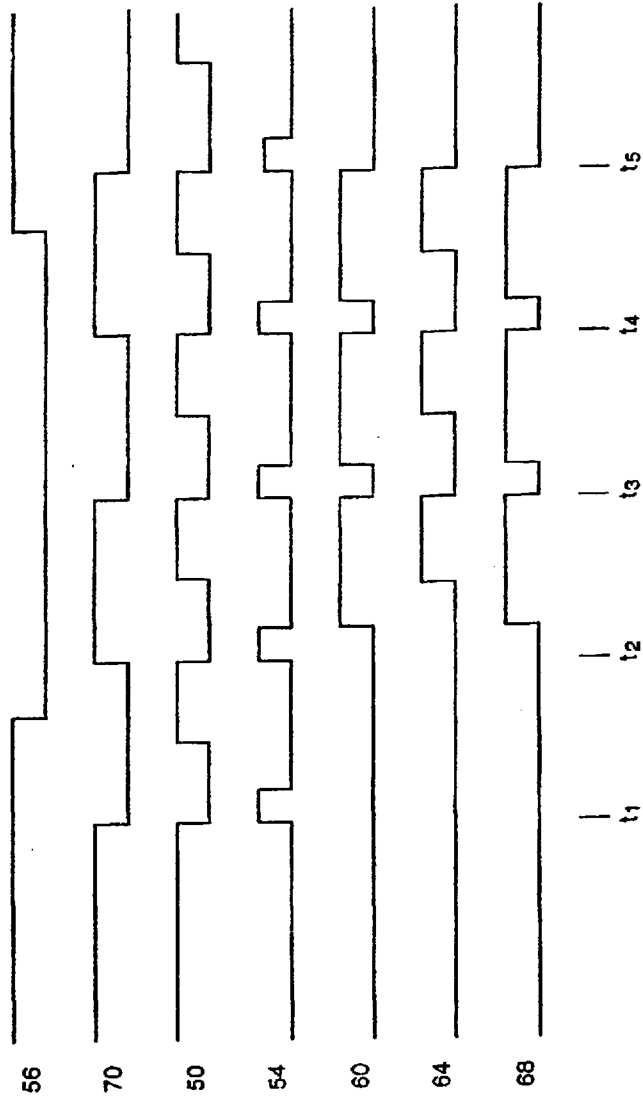

FIG. 4

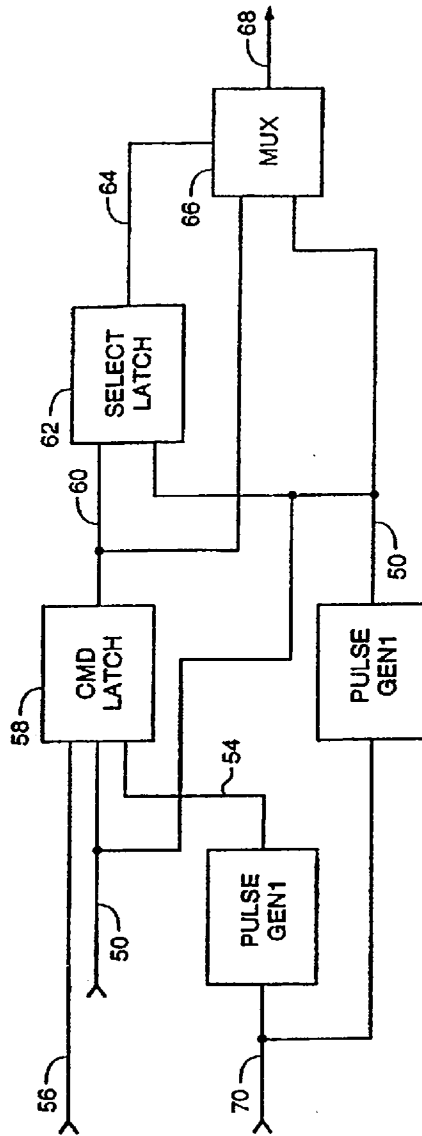

FIG. 5

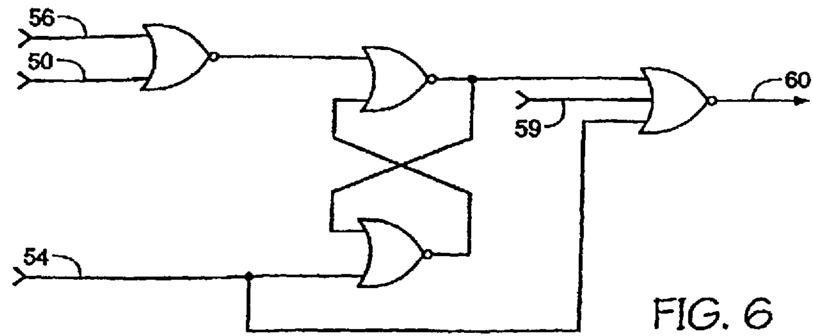

FIG. 6

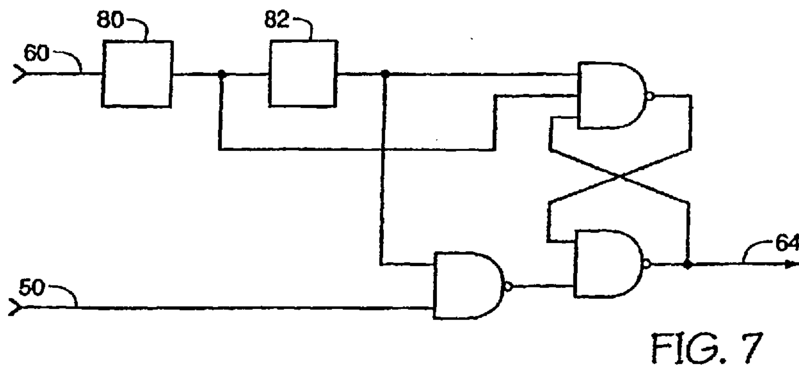

FIG. 7

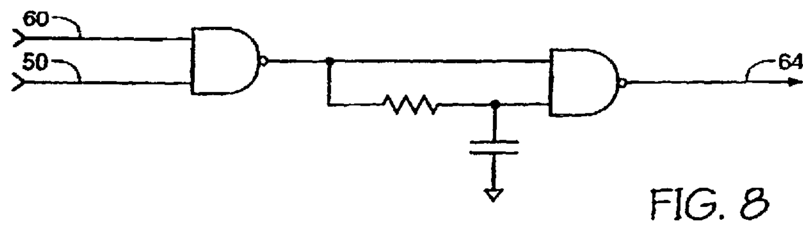

FIG. 8

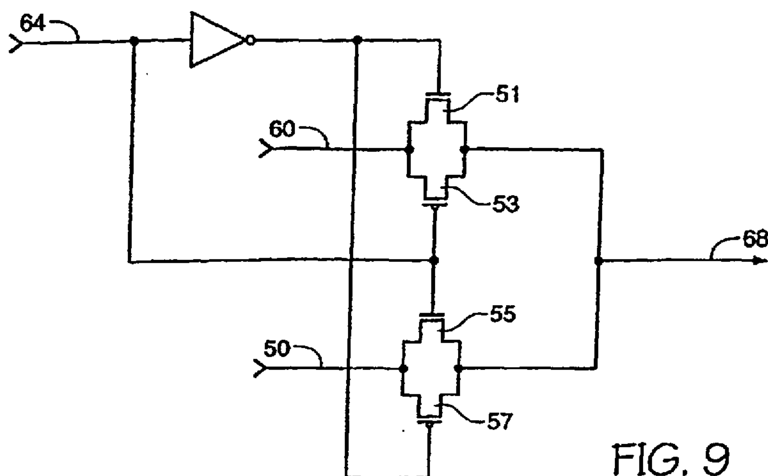

FIG. 9

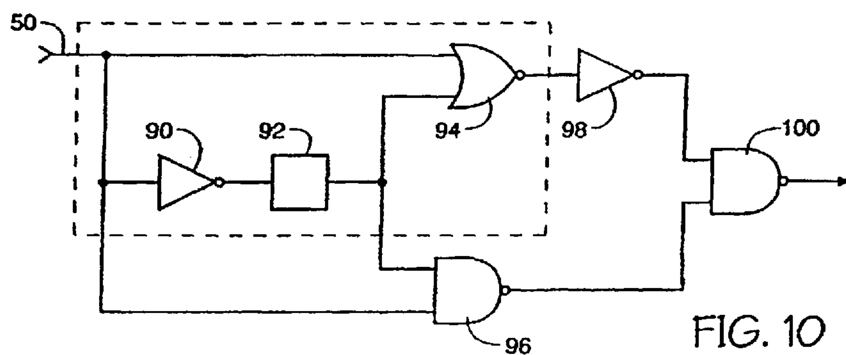

FIG. 10

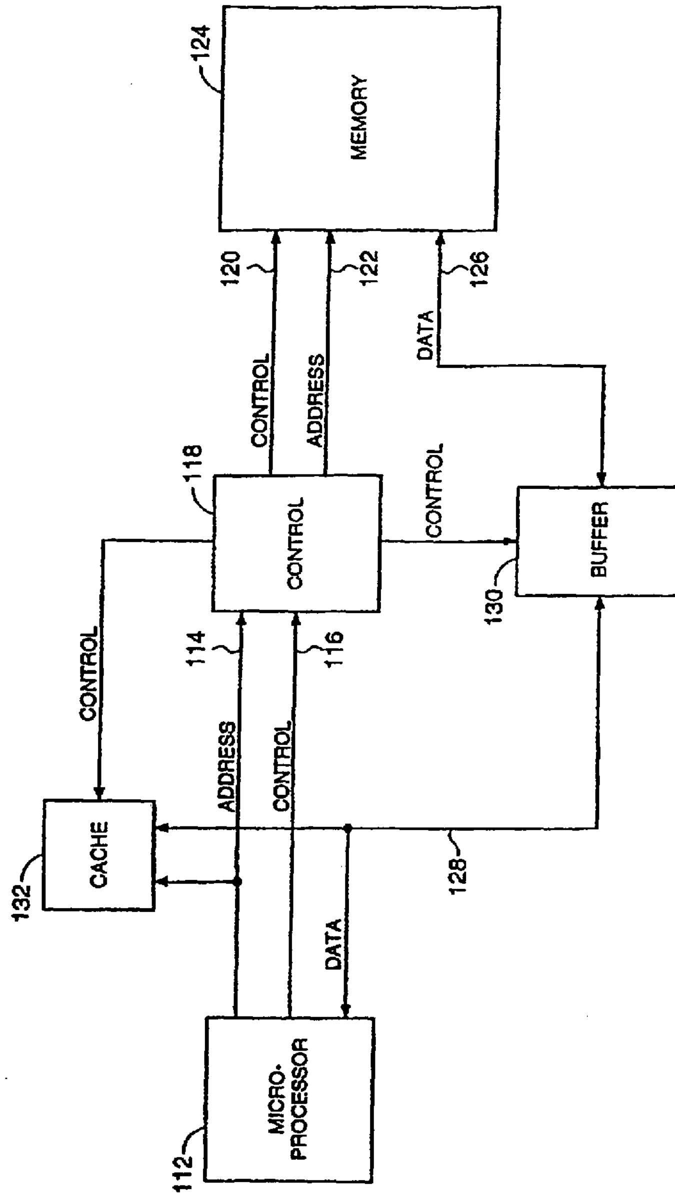

FIG. 11

BURST EDO MEMORY DEVICE WITH MAXIMIZED WRITE CYCLE TIMING

This application is a continuation of application Ser. No. 08/386,894, filed Feb. 10, 1995, U.S. Pat. No. 5,610,864.

FIELD OF THE INVENTION

This invention relates to memory device architectures designed to provide high density data storage with high speed read and write access cycles. This invention relates more specifically to circuits and methods for controlling memory write cycles in burst access memory devices.

BACKGROUND OF THE INVENTION

Dynamic Random Access Memory devices (DRAMs) are among the highest volume and most complex integrated circuits manufactured today. Except for their high volume production, the state of the art manufacturing requirements of these devices would cause them to be exorbitantly priced. Yet, due to efficiencies associated with high volume production, the price per bit of these memory devices is continually declining. The low cost of memory has fueled the growth and development of the personal computer. As personal computers have become more advanced, they in turn have required faster and more dense memory devices, but with the same low cost of the standard DRAM. Fast page mode DRAMs are the most popular standard DRAM today. In fast page mode operation, a row address strobe (/RAS) is used to latch a row address portion of a multiplexed DRAM address. Multiple occurrences of the column address strobe (/CAS) latch multiple column addresses to access data within the selected row. On the falling edge of /CAS an address is latched, and the DRAM outputs are enabled. When /CAS transitions high the DRAM outputs are placed in a high impedance state (tri-state). With advances in the production of integrated circuits, the internal circuitry of the DRAM operates faster than ever. This high speed circuitry has allowed for faster page mode cycle times. A problem exists in the reading of a DRAM when the device is operated with minimum fast page mode cycle times. /CAS may be low for as little as 15 nanoseconds, and the data access time from /CAS to valid output data (tCAC) may be up to 15 nanoseconds; therefore, in a worst case scenario there is no time to latch the output data external to the memory device. For devices that operate faster than the specifications require, the data may still only be valid for a few nanoseconds. On a heavily loaded microprocessor memory bus, trying to latch an asynchronous signal that is valid for only a few nanoseconds is very difficult. Even providing a new address every 35 nanoseconds requires large address drivers which create significant amounts of electrical noise within the system.

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead, data is held valid after /CAS goes high until sometime after the next /CAS low pulse occurs, or until /RAS or the output enable (/OE) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can

be a complex function of when the column address inputs are valid, when /CAS falls, the state of /OE and when /CAS rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially /CAS) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM manufacturers.

Methods to shorten memory access cycles tend to require additional circuitry, additional control pins and nonstandard device pinouts. The proposed industry standard synchronous DRAM (SDRAM) for example has an additional pin for receiving a system clock signal. Since the system clock is connected to each device in a memory system, it is highly loaded, and it is always toggling circuitry in every device. SDRAMs also have a clock enable pin, a chip select pin and a data mask pin. Other signals which appear to be similar in name to those found on standard DRAMs have dramatically different functionality on a SDRAM. The addition of several control pins has required a deviation in device pinout from standard DRAMs which further complicates design efforts to utilize these new devices. Significant amounts of additional circuitry are required in the SDRAM devices which in turn result in higher device manufacturing costs.

It is desirable to design and manufacture a memory device having a standard DRAM pinout and a burst mode of operation where multiple data values can be sequentially written to or read from the device in response to a single address location and multiple access strobes. It is also desirable that this new memory device operate at higher frequencies than standard DRAMs.

There is a problem in performing write cycles at high frequencies. In a standard DRAM device, write cycles are performed in response to both /CAS and /WE being low after /RAS is low. Data to be written is latched, and the write cycle begins when the latter of /CAS and /WE goes low. In order to allow for maximum page mode operating frequencies, the write cycle is often timed out so that it can continue for a short period of time after /CAS goes high especially for "late write" cycles. Maintaining the write cycle throughout the timeout period eases the timing specifications for /CAS and /WE that the device user must meet, and reduces susceptibility to glitches on the control lines during a write cycle. The write cycle is terminated after the time out period, and if /WE is high a read access begins based on the address present on the address input lines. The read access will typically begin prior to the next /CAS falling edge so that the column address to data valid specification can be met (tAA). In order to begin the read cycle as soon as possible, it is desirable to minimize the write cycle time while guaranteeing completion of the write cycle. Minimizing the write cycle duration in turn minimizes the margin to some device operating parameters despite the speed at which the device is actually used. Circuits to model the time required to complete the write cycle typically provide an estimate of the time required to write an average memory cell. While it is desirable to minimize the write cycle time, it is also necessary to guarantee that enough time is allowed for the write to complete, so extra delay is added making the write cycle slightly longer than required. Throughout the memory device product lifetime, manufacturing process advances, and circuit enhancements often allow for increases in device operating frequencies. The write cycle timing circuits may need to be adjusted to shorten the minimum write cycle times to match these performance improvements. Fine tuning of these timing circuits is time consuming and costly. If the write cycles are too short, the device may fail under some or all operating

conditions. If the write cycles are too long, the device may not be able to achieve the higher operating frequencies that are more profitable for the device manufacturers.

With the increased operating frequencies of burst access memory devices a new method of generating the write cycle timing is desired which will allow for maximum write cycle times despite the operating frequency of the device.

SUMMARY OF THE INVENTION

An integrated circuit memory device with a standard DRAM pinout is designed for high speed data access and for compatibility with existing memory systems. A high speed burst mode of operation is provided where multiple sequential accesses occur following a single column address, and read data is output relative to the /CAS control signal. In the burst mode of operation the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at high speeds. Only one control line per memory chip (/CAS) must toggle at the operating frequency in order to clock the internal address counter and the data input/output latches. The load on each /CAS is typically less than the load on the other control signals (/RAS, /WE and /OE) since each /CAS typically controls only a byte width of the data bus. A new write cycle timing method and circuit allow for maximized write cycle timing at all operating frequencies to provide maximum write cycle timing margins. Write control is maintained throughout a write cycle such that the write operation time approaches the write cycle time. The write function is only halted between write cycles for a period of time required to select a new column of the array. Devices which fail write cycle tests at high speed may then be re-tested for functionality at a lower speed grade where the write cycle will be longer.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention as well as objects and advantages are best understood by reference to the appended claims, detailed description of particular embodiments and accompanying drawings where:

FIG. 1 is an electrical schematic diagram of a memory device in accordance with one embodiment of the invention;

FIG. 2 is a timing diagram for a method of accessing the device of FIG. 1;

FIG. 3 is a schematic diagram of a portion of a memory device in accordance with the present invention;

FIG. 4 is a timing diagram of the operation of the circuit of FIG. 3;

FIG. 5 is a schematic diagram of an alternate embodiment of the circuit of FIG. 3;

FIG. 6 is a schematic diagram of a portion of the circuitry of FIGS. 1, 3 and 5;

FIG. 7 is a schematic diagram of a further portion of the circuitry of FIGS. 1, 3 and 5;

FIG. 8 is a schematic diagram of yet a further portion of the circuitry of FIGS. 1, 3 and 5;

FIG. 9 is a schematic diagram of still a further portion of the circuitry of FIGS. 1, 3 and 5;

FIG. 10 is a schematic diagram of yet still a further portion of the circuitry of FIGS. 1, 3 and 5; and

FIG. 11 is a schematic diagram of a computer system designed in accordance with the teachings of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a schematic representation of a sixteen megabit device designed in accordance with the present invention. The device is organized as a 2 Meg×8 burst EDO DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array 12. The device of FIG. 1 has an industry standard pinout for eight bit wide EDO DRAMs. An active-low row address strobe (/RAS) signal 14 is used to latch a first portion of a multiplexed memory address, from address inputs A0 through A10 16, in latch 18. The latched row address 20 is decoded in row decoder 22. The decoded row address is used to select a row of the memory array 12. A column address strobe (/CAS) signal 24 is used to latch a second portion of a memory address from address inputs 16 into column address counter 26. The latched column address 28 is decoded in column address decoder 30. The decoded column address is used to select a column of the memory array 12.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 32 to output latches 34. Data 10 driven from the burst EDO DRAM may be latched external to the device in synchronization with /CAS after a predetermined number of /CAS cycle delays (latency). For a two cycle latency design, the first /CAS falling edge is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second /CAS falling edge, and remains valid through the third /CAS falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers 34 continue to drive the data lines without tri-stating the data outputs during /CAS high intervals dependent on the state of the output enable and write enable (/OE and /WE) control lines, thus allowing additional time for the system to latch the output data. Once a row and a column address are selected, additional transitions of the /CAS signal are used to advance the column address within the column address counter in a predetermined sequence. The time at which data becomes valid at the outputs of the burst EDO DRAM is dependent only on the timing of the /CAS signal provided that /OE is maintained low, and /WE remains high. The output data signal levels may be driven in accordance with standard CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. The column address may be advanced with each /CAS transition, each pulse, or multiple of /CAS pulses in the event that more than one data word is read from the array with each column address. When the address is advanced with each transition of the /CAS signal, data is also driven from the part after each transition following the device latency which is then referenced to each edge of the /CAS signal. This allows for a burst access cycle where the highest switching control line (/CAS) toggles only once (high to low or low to high) for each memory cycle. This is in contrast to standard DRAMs which require /CAS to go low and then high for each cycle, and synchronous DRAMs which require a full clock cycle (high and low transitions) for each memory cycle. For maximum compatibility with existing EDO DRAM devices, the invention will be further described in reference to a device designed to latch and advance a column address on falling edges of the /CAS signal.

It may be desirable to latch and increment the column address after the first /CAS falling edge in order to apply both the latched and incremented addresses to the array at the earliest opportunity in an access cycle. For example, a device may be designed to access two data words per cycle (prefetch architecture). The memory array for a prefetch architecture device may be split into odd and even array halves. The column address least significant bit is used to select between odd and even halves while the other column address bits select a column within each of the array halves. In an interleaved access mode with column address 1, data from columns 0 and 1 are read and the data from column 1 is output followed by the data from column 0 in accordance with standard interleaved addressing as described in SDRAM specifications. In a linear access mode column address 1 is applied to the odd array half, and incremented to address 2 for accessing the even array half to fulfill the two word access. One method of implementing this type of device architecture is to provide a column address incrementing circuit between the column address counter and the even array half. The incrementing circuit increments the column address only if the initial column address in a burst access cycle is odd, and the address mode is linear. Otherwise the incrementing circuit passes the column address unaltered. For a design using a prefetch of two data accesses per cycle, the column address is advanced once for every two active edges of the /CAS signal. In a write cycle, multiple data words may be temporarily stored as they are input to the device. The actual write of data to the memory cells occurs after the last input data is latched, and may extend slightly into the next memory cycle as long as it ends prior to the next column being activated. Prefetch architectures where more than two data words are accessed are also possible.

Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS.

In the burst access memory device, each new column address from the column address counter is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16. This burst sequence of data continues for each /CAS falling edge until a predetermined number of data accesses equal to the burst length occurs. A /CAS falling edge received after the last burst address has been generated latches another column address from the address inputs 16 and a new burst sequence begins. Read data is latched and output with each falling edge of /CAS after the first /CAS latency.

For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the /CAS signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is preferred. Additional input data words for storage at incremented column address locations are latched by /CAS on successive /CAS pulses. Input data from the input latches 34 is passed along data path 32 to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes are performed without the requirement of additional column addresses being provided on the address lines 16. After the predetermined number of burst writes occurs, a subsequent /CAS pulse latches a new beginning column address, and another burst read or write access begins.

The memory device of FIG. 1 may include the option of switching between burst EDO and standard EDO modes of operation. In this case, the write enable signal /WE 36 is used at the row address latch time (/RAS falling, /CAS high) to determine whether memory accesses for that row are burst or page mode cycles. If /WE is low when /RAS falls, burst access cycles are selected. If /WE is high at /RAS falling, standard extended data out (EDO) page mode cycles are selected. Both the burst and EDO page mode cycles allow for increased memory device operating frequencies by not requiring the data output drivers 34 to place the data lines 10 in a high impedance state between data read cycles while /RAS is low. DRAM control circuitry 38, in addition to performing standard DRAM control functions, controls the I/O circuitry 34 and the column address counter/latch 26 in accordance with the mode selected by /WE when /RAS falls. In a burst mode only DRAM, or in a device designed with an alternate method of switching between burst and non-burst access cycles, the state of /WE when /RAS falls may be used to switch between other possible modes of operation such as interleaved versus linear addressing modes.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by /CAS. /WE low at the column address latch time selects a burst write access. /WE high at the column address latch time selects a burst read access. The level of the /WE signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access terminates the burst access, preventing further writes from occurring. A high to low transition on /WE within a burst read access likewise terminates the burst read access and places the data output 10 in a high impedance state. Transitions of the /WE signal may be locked out during critical timing periods within an access cycle in order to reduce the possibility of triggering a false write cycle, and/or to guarantee the completion of a write cycle once it has begun. After the critical timing period the state of /WE determines whether a burst access continues, is initiated, or is terminated. Termination of a burst access resets the burst length counter and places the DRAM in a state to receive another burst access command. Both /RAS and /CAS going high during a burst access also terminate the burst access cycle placing the data drivers in a high impedance output state, and resetting the burst length counter. Read data may remain valid at the device outputs if /RAS alone goes high while /CAS is active for compatibility with hidden refresh cycles, otherwise /RAS high alone may be used to terminate a burst access. A minimum write enable pulse width is only required when it is desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses. In the case of burst reads, /WE transitions from high to low to terminate a first burst read, and then five transitions back high prior to the next falling edge of /CAS in order to specify a new burst read cycle. For burst writes, /WE transitions high to terminate a current burst write access, then back low prior to the next falling edge of /CAS to initiate another burst write access.

A basic implementation of the device of FIG. 1 may include a fixed burst length of 4, a fixed /CAS latency of 2 and a fixed interleaved sequence of burst addresses. This

basic implementation requires very little additional circuitry to the standard EDO page mode DRAM, and may be mass produced to provide the functions of both the standard EDO page mode and burst EDO DRAMs. This device also allows for the output enable pin (/OE) to be grounded for compatibility with many SIMM module designs. When not disabled (tied to ground), /OE is an asynchronous control which prevents data from being driven from the part in a read cycle if it is inactive (high) prior to /CAS falling and remains inactive beyond /CAS rising. If these setup and hold conditions are not met, then the read data may be driven for a portion of the read cycle. It is possible to synchronize the /OE signal with /CAS, however this typically increases the /CAS to data valid delay time and doesn't allow for the read data to be disabled prior to /RAS high without an additional /CAS low pulse which would otherwise be unnecessary. In a preferred embodiment, if /OE transitions high at any time during a read cycle the outputs remain in a high impedance state until the next falling edge of /CAS despite further transitions of the /OE signal.

Programmability of the burst length, /CAS latency and address sequences may be accomplished through the use of a mode register 40 which latches the state of one or more of the address input signals 16 or data signals 10 upon receipt of a write-/CAS-before-/RAS (WCBR) programming cycle. In such a device, outputs 44 from the mode register control the required circuits on the DRAM. Burst length options of 2, 4, 8 and full page as well as /CAS latencies of 1, 2 and 3 may be provided. Other burst length and latency options may be provided as the operating speeds of the device increase, and computer architectures evolve. The device of FIG. 1 includes programmability of the address sequence by latching the state of the least significant address bit during a WCBR cycle. The burst length and /CAS latency for this particular embodiment are fixed. Other possible alterations in the feature sets of this DRAM include having a fixed burst mode only, selecting between standard fast page mode (non-EDO) and burst mode, and using the output enable pin (/OE) 42 in combination with /RAS to select between modes of operation. Also, a WCBR refresh cycle could be used to select the mode of operation rather than a control signal in combination with /RAS. A more complex memory device may provide additional modes of operation such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of /WE and /OE at /RAS falling time. One mode from a similar set of modes may be selected through the use of a WCBR cycle using multiple address or data lines to encode the desired mode. Alternately, a device with multiple modes of operation may have wire bond locations, or programmable fuses which may be used to program the mode of operation of the device.

A preferred embodiment of a sixteen bit wide burst EDO mode DRAM designed in accordance with the teachings of this invention has two column address strobe input pins /CASH and /CASL. For read cycles only one /CAS signal needs to toggle. The second /CAS may remain high or toggle with the other /CAS. During burst read cycles, all sixteen data bits will be driven out of part during a read cycle even if one /CAS remains inactive. In a typical system application, a microprocessor reads all data bits on a data bus in each read cycle, but may only write certain bytes of data in a write cycle. Allowing one of the /CAS control signals to remain static during read cycles helps to reduce overall power consumption and noise within the system. For burst write access cycles, each of the /CAS signals (CASH and /CASL) acts as a write enable for an eight bit width of the data. The two /CAS's are combined in an AND function to provide a single internal /CAS which will go low when the first external /CAS falls, and returns high after the last external /CAS goes high. All sixteen data inputs are latched when the first of the /CAS signals transitions low. If only one /CAS signal transitions low, then the eight bits of data associated with the /CAS that remained high are not stored in the memory.

The present invention has been described with reference to several preferred embodiments. Just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including ×1, ×4, ×8 and ×16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the memory device of the present invention may take the form of many different memory organizations. It is believed that one who is skilled in the art of integrated circuit memory design can, with the aide of this specification design a variety of memory devices which do not depart from the spirit of this invention. It is therefore believed that detailed descriptions of the various memory device organizations applicable to this invention are not necessary.

It should be noted that the pinout for this new burst EDO memory device may be identical to the pinout for a standard EDO DRAM. The common pinout allows this new device to be used in existing memory designs with minimum design changes. The common pinout also allows for ease of new designs by those of skill in the art who are familiar with the standard EDO DRAM pinout. Variations of the described invention which maintain the standard EDO DRAM pinout include driving the /CAS pin with a system clock signal to synchronize data access of the memory device with the system clock. For this embodiment, it may be desirable to use the first /CAS active edge after /RAS falls to latch the row address, a later edge may be used to latch the first column address of a burst access cycle. After row and column addresses are latched within the device, the address may be incremented internally to provide burst access cycles in synchronization with the system clock. Other pin function alternatives include driving the burst address incrementing signal on the /OE pin since the part does not require a data output disable function on this pin. Other alternate uses of the /OE pin also allow the device to maintain the standard EDO pinout, but provide increased functionality such as burst mode access. The /OE pin may be used to signal the presence of a valid column starting address, or to terminate a burst access. Each of these embodiments provides for a high speed burst access memory device which may be used in current memory systems with a minimum amount of redesign.

FIG. 2 is a timing diagram for performing a burst read followed by a burst write of the device of FIG. 1. In FIG. 2, a row address is latched by the /RAS signal. /WE is low when /RAS falls for an embodiment of the design where the state of the /WE pin is used to specify a burst access cycle at /RAS time. Next, /CAS is driven low with /WE high to initiate a burst read access, and the column address is latched. The data out signals (DQ's) are not driven in the first /CAS cycle. On the second falling edge of the /CAS signal, the internal address generation circuitry advances the column address and begins another access of the array, and the first data out is driven from the device after a /CAS to data access time (tCAC). Additional burst access cycles continue, for a device with a specified burst length of four, until the fifth falling edge of /CAS which latches a new column address for a new burst read access. /WE falling in the fifth /CAS cycle terminates the burst access, and initializes the device for additional burst accesses. The sixth

falling edge of /CAS with /WE low is used to latch a new burst address, latch input data and begin a burst write access of the device. Additional data values are latched on successive /CAS falling edges until /RAS rises to terminate the burst access.

It should be noted from FIG. 2 that for burst read cycles the data remains valid on the device outputs as long as the /OE pin is low, except for brief periods of data transition. Also, since the /WE pin is low prior to or when /CAS falls, the data input/output lines are not driven from the part during write cycles, and the /OE pin is a "don't care". Only the /CAS signal and the data signals toggle at relatively high frequency, and no control signals other than /CAS are required to be in an active or inactive state for one /CAS cycle time or less. This is in contrast to SDRAMs which often require row address strobes, column address strobes, data mask, and read/write control signals to be valid for one clock cycle or less for various device functions. Typical DRAMs also allow for the column address to propagate through to the array to begin a data access prior to /CAS falling. This is done to provide fast data access from /CAS falling if the address has been valid for a sufficient period of time prior to /CAS falling for the data to have been accessed from the array. In these designs an address transition detection circuit is used to restart the memory access if the column address changes prior to /CAS falling. This method actually requires additional time for performing a memory access since it must allow for a period of time at the beginning of each memory cycle after the last address transition to prepare for a new column address. Changes in the column address just prior to /CAS falling may increase the access time by approximately five nanoseconds. An embodiment of the present invention will not allow the column address to propagate through to the array until after /CAS has fallen. This eliminates the need for address transition detection circuitry, and allows for a fixed array access time relative to /CAS.

FIG. 3 shows a write timing circuit designed to maximize the amount of time allowed for each write cycle to complete regardless of the device operating frequency. An access cycle strobe signal node 50 is connected to a pulse generator 52. For the purposes of this specification a node may be, but is not limited to, an intersection of conductors, a circuit input or output, or any point along a signal path. At the beginning of each access cycle, the pulse generator produces a pulse signal on signal line 54 in response to an access cycle strobe signal on node 50. A read/write command signal on line 56 is an input to a command latch 58. Upon receipt of an access cycle strobe, the pulse signal clears the command latch. The read/write command on line 56 is latched in the command latch, after the latch is cleared. The read/write command remains latched until the next pulse signal occurs on line 54 clearing the command latch. A latched read/write control signal on line 60 from the command latch goes to a write control select latch 62. The select latch output is connected to a multiplexer select signal line 64 for selecting whether the latched read/write control signal or the access cycle strobe signal controls a data path to allow data to be written into memory. When the select signal 64 is in one state, the read/write control signal will pass through the multiplexer 66 to the write control signal 68. When the select 64 is in a second state, the access cycle strobe signal will pass through the multiplexer to the write control signal 68.

At the beginning of each cycle, the latched read/write control signal is cleared. The cleared read/write control signal causes the multiplexer select signal to select the read/write control signal on line 60. Whenever the latched command indicates that a read cycle is being performed, the select signal continues to select the signal on line 60 throughout the access cycle. For write cycles, after the pulse signal clears the command latch, the latched read/write control signal indicates that a write cycle is being performed. This signal is selected to pass through the multiplexer and initiate a write cycle by driving the write control signal 68. When the access cycle strobe signal changes state, the write control select latch causes the multiplexer select signal to change states and select the access cycle strobe signal to pass through the multiplexer to maintain the write control signal on signal line 68. At the beginning of the next cycle, the access cycle strobe signal again changes state and passes through the multiplexer to terminate the write cycle. The pulse generator produces a pulse signal to clear the command latch, and the select signal changes state to select the read/write control signal to pass through the multiplexer. In this manner, the write control signal is valid for a period of time approximately equal to a cycle time. The write control signal enables data from the input data latches to be applied to memory array for storage at the address specified by row and column address decoders. Data from the input data latches must be applied to a memory element for a minimum amount of time to ensure that a full data level will be stored in the memory element. By enabling the data path for nearly a full cycle time, the amount of time that data is applied to the memory is maximized at all operating frequencies.

The operation of the circuit of FIG. 3 is further described in the timing diagram of FIG. 4. Signals are labeled according to the signal lines on which they are generated from the circuit of FIG. 3. Circuit initialization will occur at the beginning of each access cycle in response to an access cycle strobe signal active edge. In one embodiment of the circuit of FIG. 3, the access cycle strobe signal is a column address strobe (/CAS) for a burst mode DRAM as described in the present invention, and a new cycle begins with each falling edge of /CAS in a burst access. After initialization, a write cycle operation will begin in response to the latched read/write control signal. The write operation will continue until the end of the access cycle (the beginning of a subsequent access). Once the next cycle is begun, a new column will be selected as fast as possible. Rapid termination of the write cycle is important to prevent data at the next column address from being disturbed. By selecting the access cycle strobe signal, the write operation may be rapidly terminated at the beginning of the next cycle without waiting for the command latch to be cleared. The timing diagram of FIG. 4 shows a read cycle followed by three write cycles and then another read cycle. A read access begins at time t1. Signal 56 being high in this embodiment signifies a read access. Once the access cycle strobe signal 50 transitions high, a read state on the read/write command signal is latched in the command latch which generates the latched read/write control signal. The transition to a write command on the read/write command signal line 56 is ignored until time t2. At time t2 a write cycle begins. After the signal pulse on line 54, a write state of the read/write command is latched on signal line 60 until it is cleared by the next signal pulse on line 54 at time t3. For each write cycle, the latched read/write control signal passes through the multiplexer to line 68. The select line 64 switches during each write cycle after the access cycle strobe signal has transitioned high, causing the multiplexer to select the access cycle strobe signal. At the beginning of the next cycle, the access cycle strobe signal transitions low terminating the write, clearing the command latch and resetting the select signal. For burst write access cycles, the write control signal on line 68 is active for a period of time

approaching an access cycle time despite the operating frequency of the memory device. The write control signal is only cleared between burst write cycles for a period of time required to select a new column of the memory array. At time t5, a read cycle begins. The command latch and select line are cleared, and the select line remains low for the read cycle.

FIG. 5 shows an alternate embodiment of the circuit of FIG. 3. In the embodiment of the invention shown in FIG. 5, the memory device is designed to initiate an access cycle after each edge of an access cycle signal (typically /CAS). For this situation, the pulse generator 52 generates a short pulse after each transition of /CAS on line 70. A second pulse generator 72 is placed between signal line 70 and signal line 50 to generate a longer pulse after each transition of /CAS. This longer pulse becomes the access strobe signal 50 as shown in the timing diagram of FIG. 4. The other components of FIG. 5 operate as described for like numbered components of FIG. 3. The timing of the /CAS signal for this design is shown in is FIG. 4 as signal 70.

FIG. 6 shows an example embodiment of command latch 58. A high pulse on signal line 54 at the beginning of each access will force signal line 60 to go low clearing the latch. Also, if the read/write command signal 56 is low indicating a write cycle at the same time that the access cycle strobe signal 50 is low, signal line 60 will go high after the signal pulse on line 54, and will be latched high once the access cycle strobe signal returns high. In addition to the signal pulse clearing the write command, /RAS 59 going high forces signal line 60 to go low clearing the latched write control. An additional write command latch (not shown) may be used to latch a burst access termination as a result of a transition on the read/write control signal since the command latch 58 does not recognize transitions on the read/write command signal line while it is in a latched state.

FIG. 7 shows an example embodiment of the select latch 62. A first delay element 80 guarantees that the latched read/write control signal 60 is cleared prior to unlatching the select signal 64. When a write cycle is terminated at the beginning of a subsequent access cycle, signal 50 will transition low. Signal 60 will go low shortly afterwards, and the output of the select latch will go low. A second delay element 82 ensures that the latch remains cleared until a new command has been latched in the command latch.

It may be possible to replace the latch of FIG. 7 with an AND function and a delay as shown in FIG. 8. In this circuit, if the latched read/write control is high (write command) when the access cycle strobe goes high, the select line will switch to allow the access cycle to terminate the write at the beginning of the next cycle. When the next cycle begins, signal 50 will transition low, and the delay circuitry comprising a resistor and a capacitor will prevent the select signal from transitioning back before the command latch is cleared.

FIG. 9 shows an embodiment of a fast multiplexer circuit 66 for the circuits of FIGS. 3 and 5. Select line 64 determines whether signal 50 or 60 will pass through the CMOS transistors 51, 53, 55, and 57 to signal line 68.

FIG. 10 shows an embodiment of the pulse generators of FIGS. 3 and 5. An inverter 90, a delay element 92 and a NOR gate 94 serve as the high pulse generator 52 of FIG. 3 which will generate a high pulse for each low transition on signal line 50. For the two pulse generators of FIG. 5 which require a pulse in response to each transition on signal line 50, inverter 98 converts the high pulse from NOR gate 94 into a low pulse, and NAND gate 96 generates a low pulse in response to high transitions on signal line 50. NAND gate 100 combines and inverts the outputs of the high and low edge pulse generators to provide a single high pulse signal in response to a high or a low transition on signal line 50.

FIG. 11 is a schematic representation of a data processing apparatus designed in accordance with the present invention. For the purposes of this specification a microprocessor may be, but is not limited to, a microprocessor, a microcontroller, a digital signal processor, or an arithmetic processor. In FIG. 11, microprocessor 112 is connected via address lines 114 and control lines 116 to a memory control circuit 118. The memory control circuit provides address and control signals on lines 122 and 120 respectively to a burst access memory device 124. The burst access memory device sends and receives data over data bus 126. Optional data bus buffer 130 between memory data bus 126 and microprocessor data bus 128 allows for amplification of the data signals, and/or synchronization with the microprocessor and memory control signals. A fast static random access memory (SRAM) cache circuit 132 is also optional and provides higher speed access to data stored in the cache from the memory circuit or the microprocessor. Memory control circuit 118 may be incorporated within the microprocessor. The memory control circuit provides the required address strobe signals and read/write control signals required for burst mode access of the memory circuit by providing burst access of the memory by the processor, a computer with relatively high memory bandwidth can be designed without the requirement of a fast SRAM cache. SRAMs which are fast enough to provide memory access without wait states can significantly add to the cost of a computer. Thus the burst access memory device of the present invention allows for medium to high performance computers to be manufactured at a cost which is significantly less than those manufactured today. Use of the burst access memory device of the present invention in cooperation with a fast SRAM cache allows for an even higher performance computer design by providing fast access to main memory in the event of a cache miss.

While the present invention has been described with reference to preferred embodiments, numerous modifications and variations of the invention will be apparent to one of skill in the art without departing from the scope of the invention.

What is claimed is:

1. A memory device having a plurality of memory elements, each of the elements having an associated address, the memory device adapted to switch control of a write operation between a write command and an address latch signal during a write operation, the memory comprising:

addressing circuitry adapted to receive a first address in response to a first transition of the address latch signal, and further adapted to generate a second address in response to a subsequent transition of the address latch signal; and

a write cycle command latch to store a latched write command in response to the first transition of the address latch signal, the address latch signal initiating a memory access cycle.

2. The memory device of claim 1, wherein the write cycle command latch is cleared in response to the first transition of the address latch signal prior to storing the write command.

3. The memory device of claim 1, wherein the write cycle command latch stores the write command until the subsequent transition of the address latch signal.

4. The memory device of claim 1, further comprising:

a switching circuit, responsive to an output of the write cycle command latch and the address latch signal, to a control a data storage operation of the memory device.

5. The memory device of claim 4, wherein the write cycle command latch and the switching circuit are irresponsive to the write command while the write cycle command latch is in a latched state.

6. A memory device having an array of memory elements, adapted to store data in response to a write operation, and an address latch to receive a first address in response to an address latch signal, the memory device comprising:

an address generating circuit responsive to the address latch signal and to the first address to generate a second address, wherein the second address is used to access the array; and

a write control circuit adapted to switch control of the write operation from a write command signal to the address latch signal during a write operation, wherein the write command signal initiates the write operation, and the access cycle signal terminates the write operation.

7. The memory device of claim 6, wherein the write control circuit is further adapted to initiate a subsequent write operation in response to the address latch signal after terminating a first write operation.

8. A memory system comprising:

a microprocessor; and

a memory circuit adapted to store and retrieve data in a burst access in response to a memory address received from the microprocessor and in response to control signals, wherein the memory circuit is adapted to latch the memory address and perform a first memory access in response to a first transition of the address latch signal within the burst access and is further adapted to generate an additional memory address and perform a memory access cycle in response to each of a plurality of additional transitions of the address latch signal within a burst access, the memory circuit further comprises a write operation control circuit adapted to switch control of a write operation between a write command signal and an address latch signal during a write operation, wherein the write command signal initiates the write operation, and the address latch signal terminates the write operation.

9. The apparatus of claim 8, further comprising a memory access control circuit to generate the address latch signal.

10. The apparatus of claim 8, wherein the microprocessor comprises memory control circuitry to generate the address latch signal.

11. The apparatus of claim 8, wherein data read from the memory address of the memory circuit is provided by the memory circuit to the microprocessor after at least two transitions of the address latch signal in the burst access.

12. The apparatus of claim 11, wherein additional data values from a predetermined sequence of addresses of the memory circuit are provided to the microprocessor in response to additional transitions of the address latch signal after the microprocessor receives data from the memory address.

13. The apparatus of claim 8, wherein the memory circuit comprises dynamic random access memory elements.

* * * * *

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United States Patent [19]

Manning

[11] **Patent Number: 5,721,859**

[45] **Date of Patent: Feb. 24, 1998**

[54] **COUNTER CONTROL CIRCUIT IN A BURST MEMORY**

[75] Inventor: **Troy A. Manning**, Boise, Id.

[73] Assignee: **Micron Technology, Inc.**, Boise., Id.

[21] Appl. No.: **553,156**

[22] Filed: **Nov. 7, 1995**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 457,651, Jun. 1, 1995, which is a continuation-in-part of Ser. No. 386,894, Feb. 10, 1995, Pat. No. 5,610,864, which is a continuation-in-part of Ser. No. 370,761, Dec. 23, 1994, Pat. No. 5,526,320.

[51] **Int. Cl.**[6] **G06F 9/26**; G06F 12/00

[52] **U.S. Cl.** **397/421.07**; 395/421.08; 395/401; 365/233; 365/189.05; 365/230.01

[58] **Field of Search** 395/421.07, 421.08, 395/421.09, 421.1; 365/233, 222, 233.5, 189.05, 230.08, 421.07, 421.08, 401

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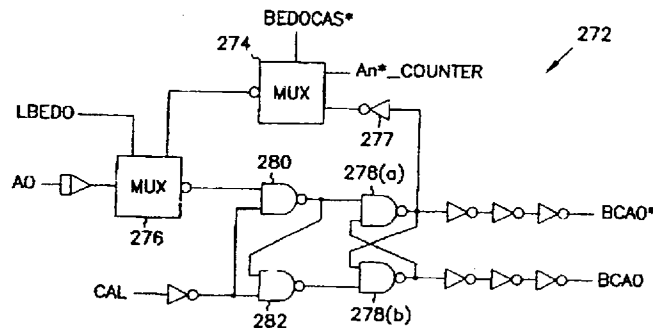
Primary Examiner—David K. Moore
Assistant Examiner—Than V. Nguyen
Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

An integrated memory circuit is described which can be operated in a burst access mode. The memory circuit includes an address counter which changes column addresses in one of a number of predetermined patterns. The column address is changes in response to a rising edge of a column address signal (CAS*). The memory also includes a buffer circuit which latches the output of the address counter in response to the falling edge of the column address signal. Memory cells are accessed in a burst manner on the falling edge of the column address signal using the address latched in the buffer.

22 Claims, 12 Drawing Sheets



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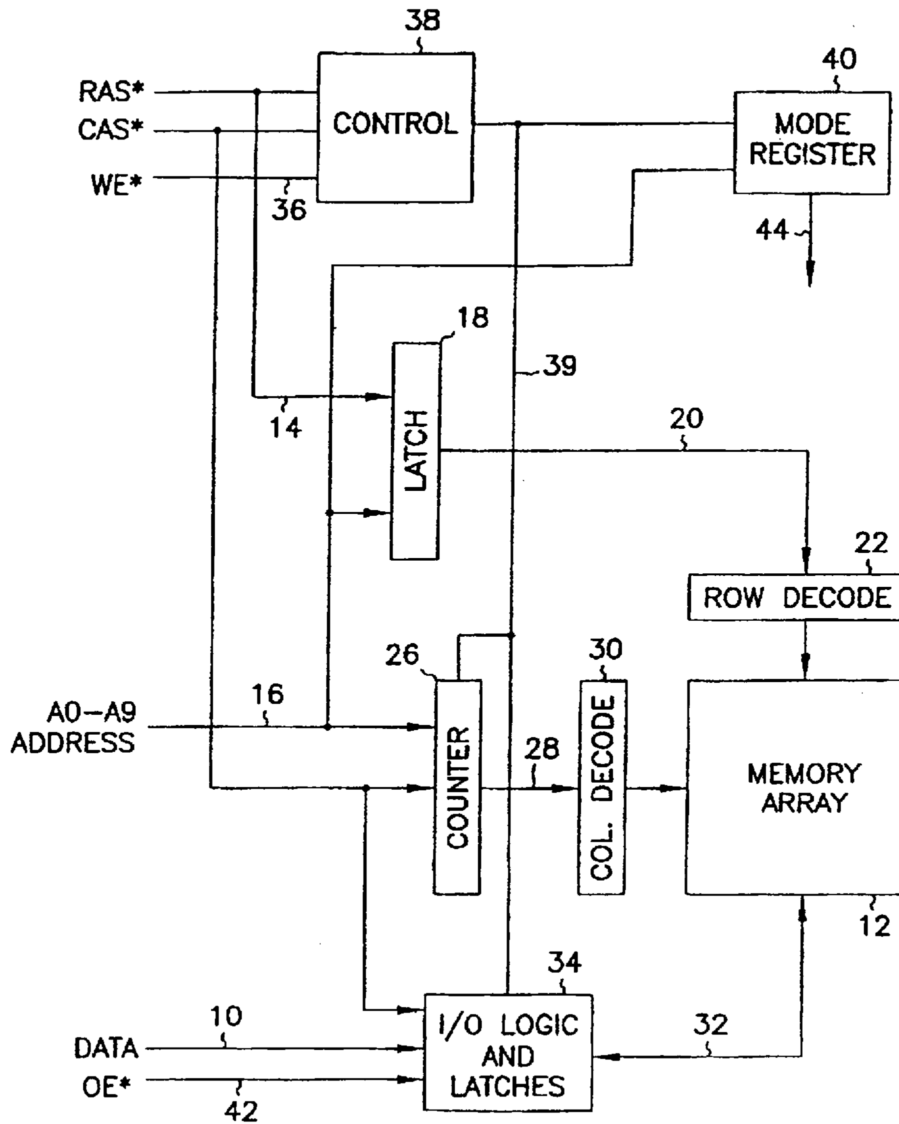

FIG. 1

Burst Length	Starting Column Address A_2	A_1	A_0	Linear	Interleave
2	V	V	0	0-1	0-1
	V	V	1	1-0	1-0
4	V	0	0	0-1-2-3	0-1-2-3
	V	0	1	1-2-3-0	1-0-3-2
	V	1	0	2-3-0-1	2-3-0-1
	V	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

FIG. 2

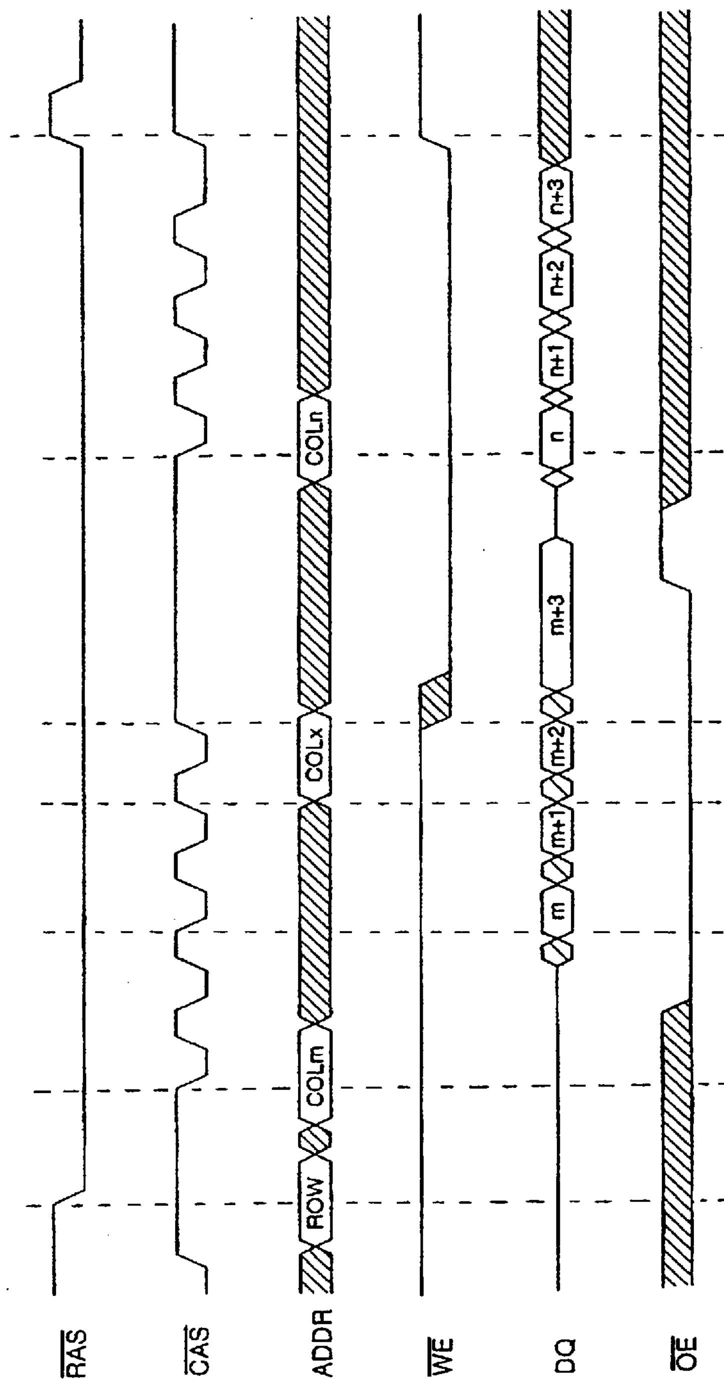

FIG. 3

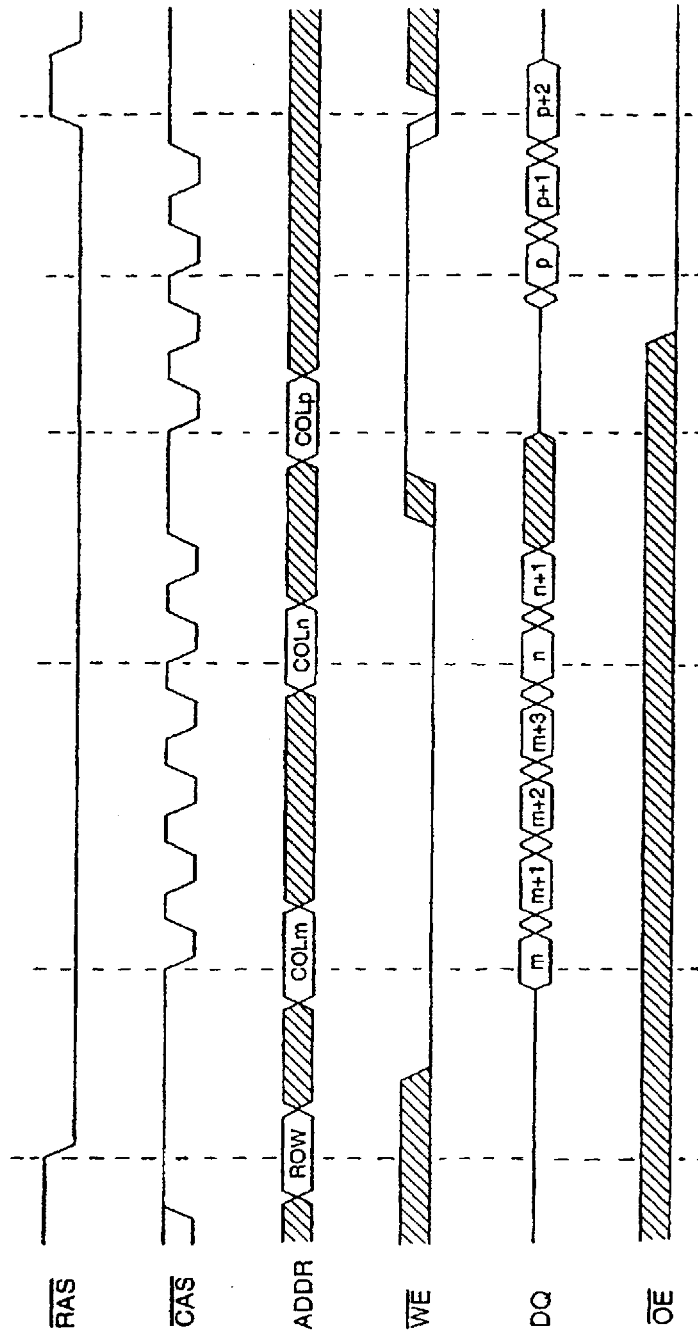

FIG. 4

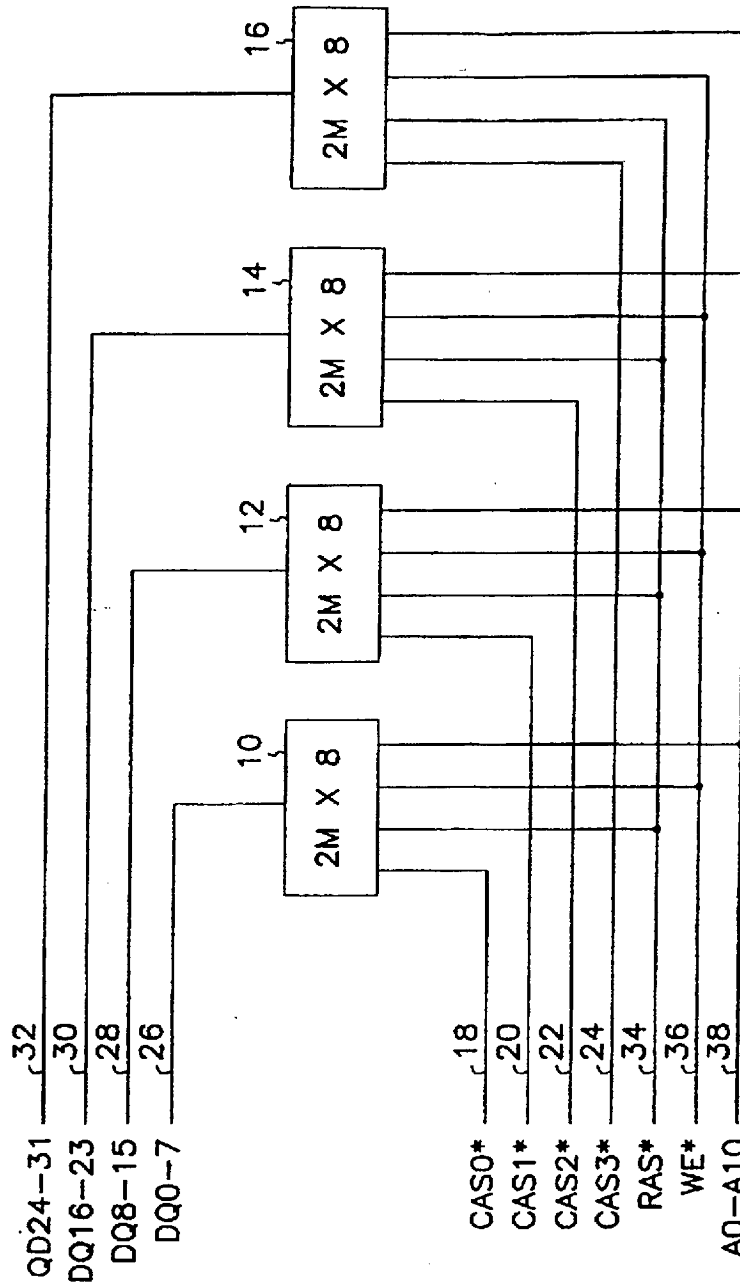

FIG. 5

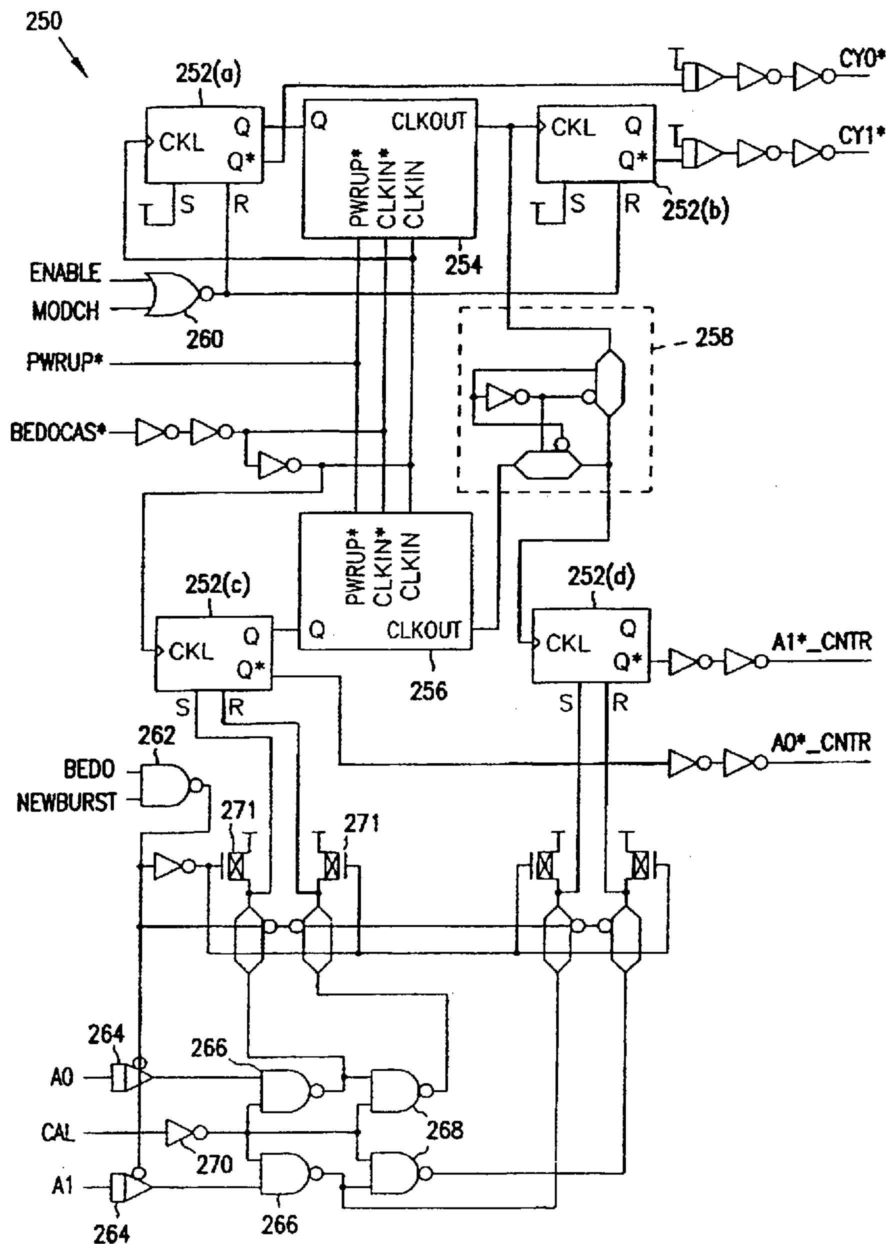

FIG. 6

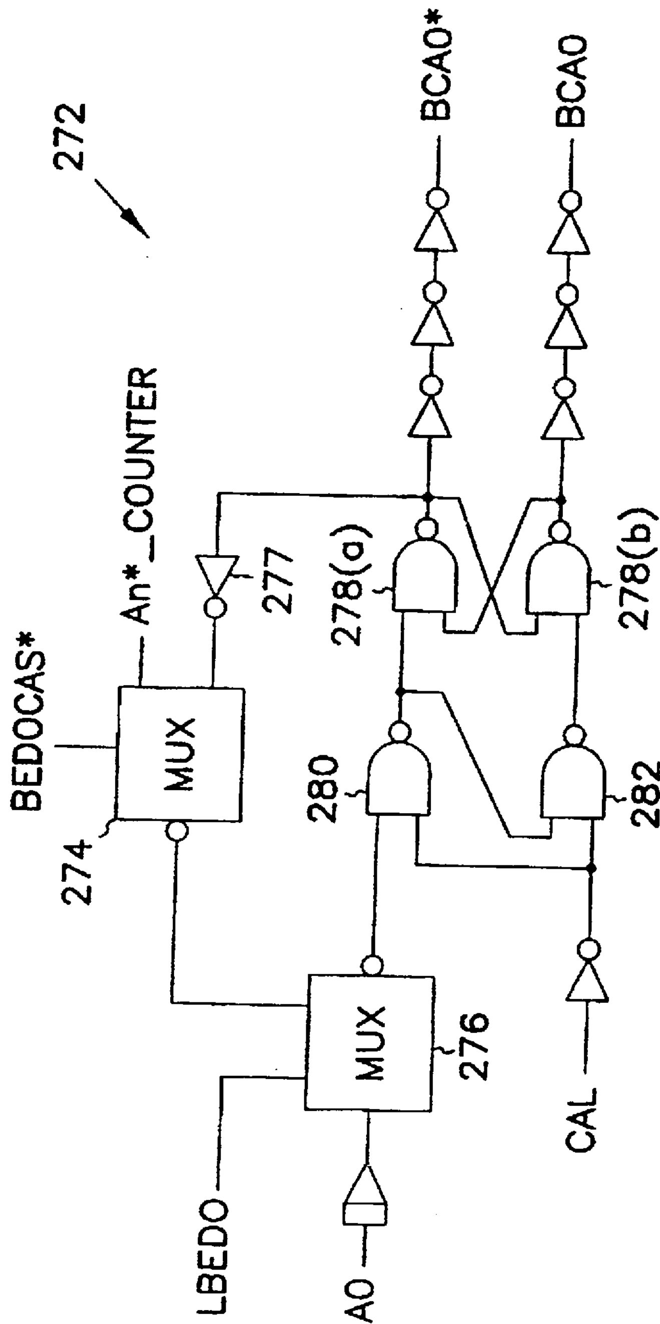

FIG. 7

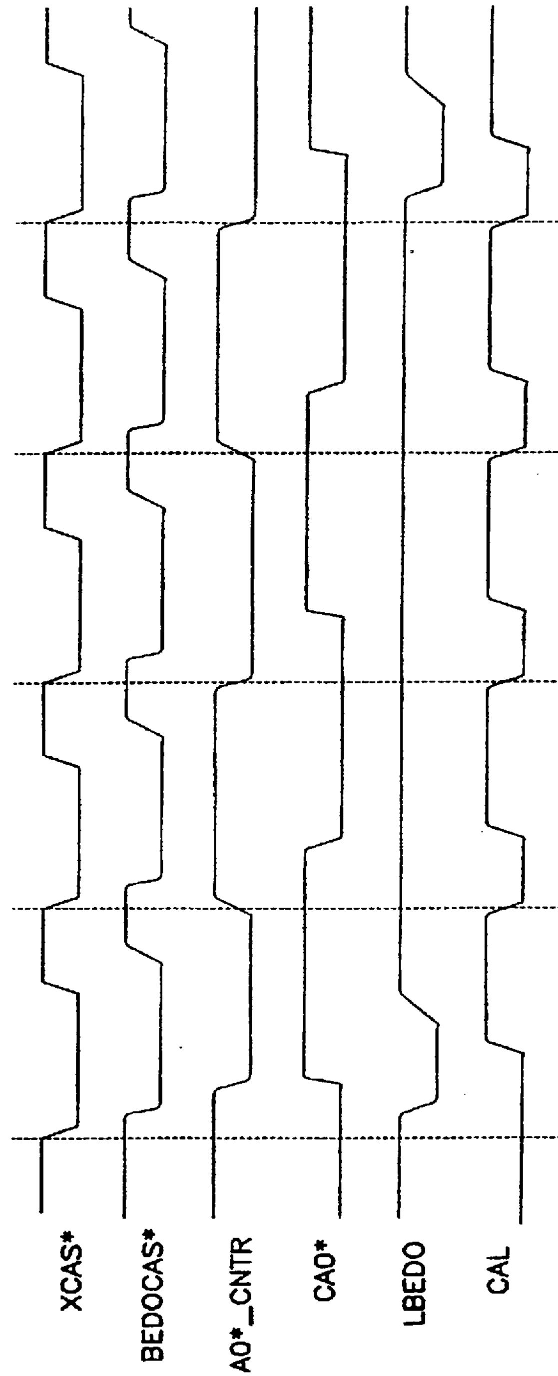

FIG. 8

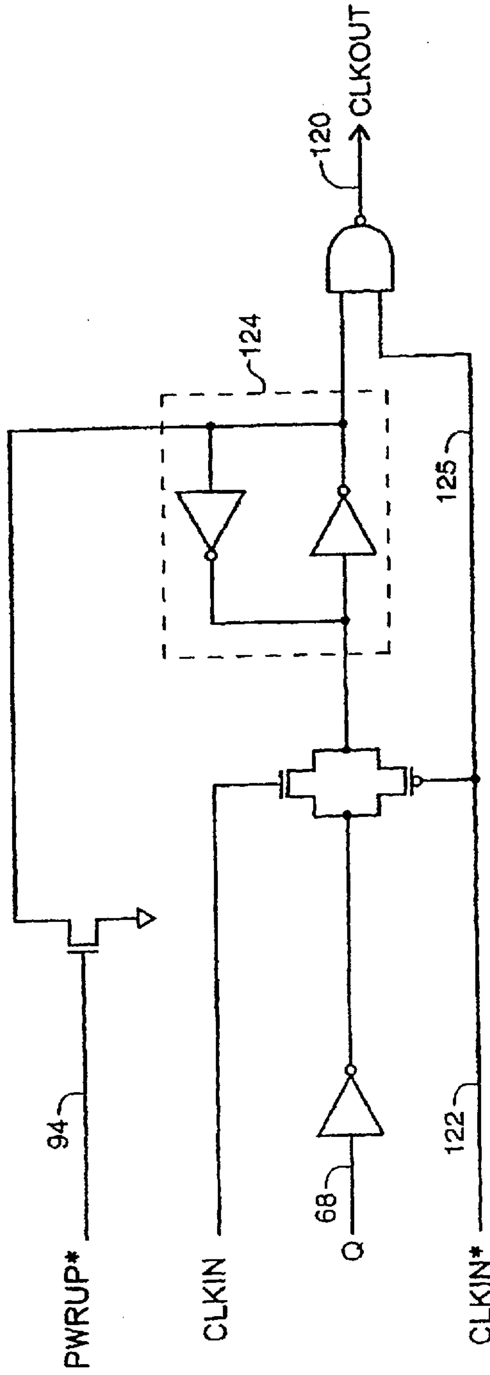

FIG. 9

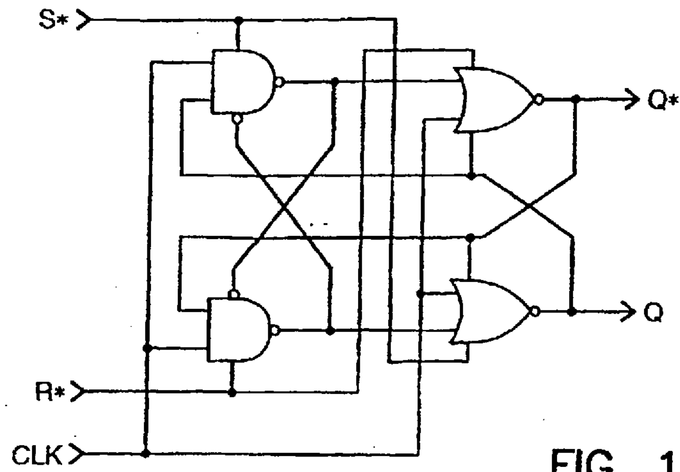

FIG. 10

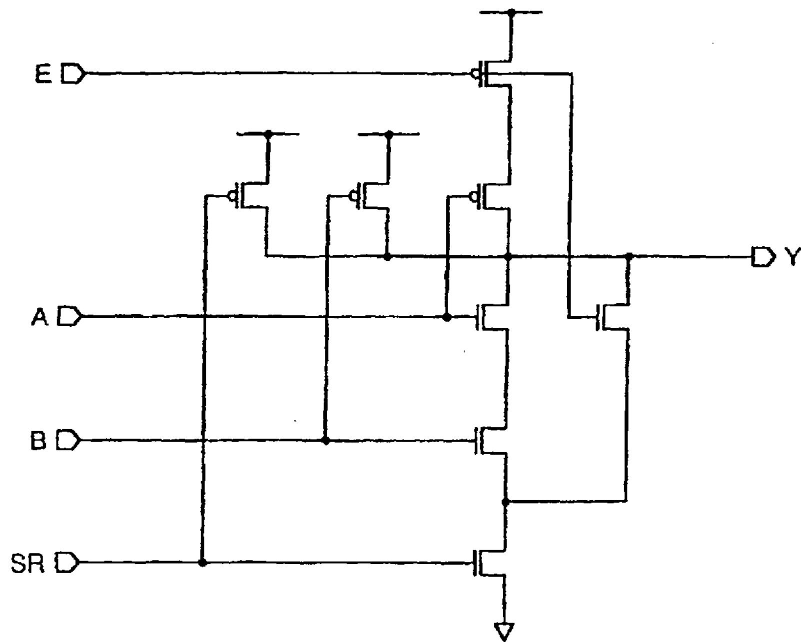

FIG. 11

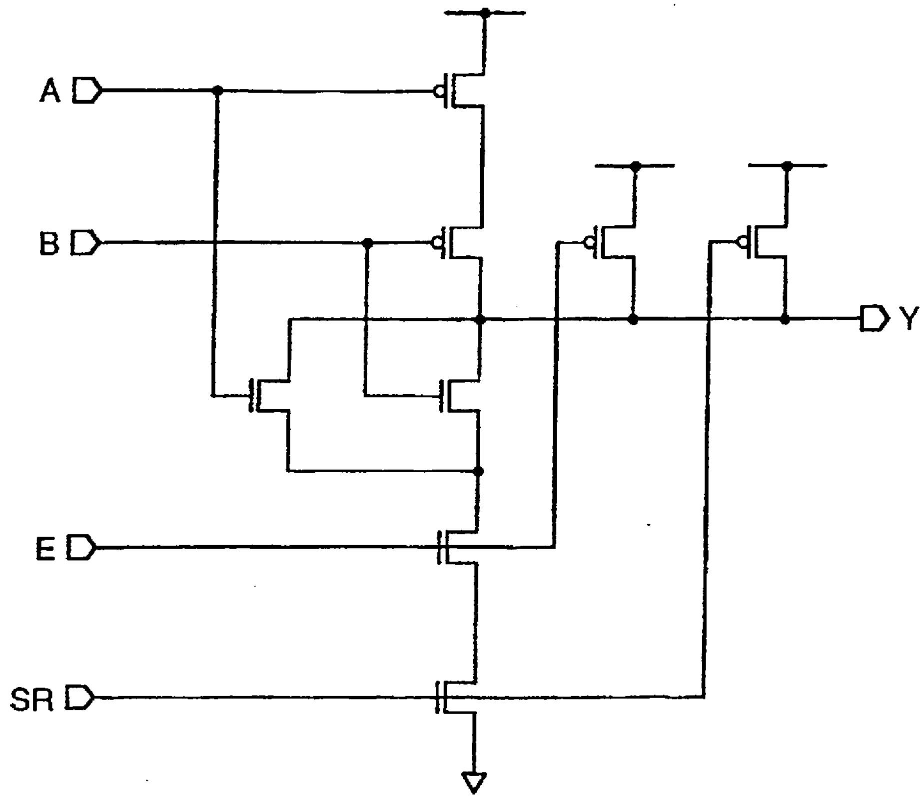

FIG. 12

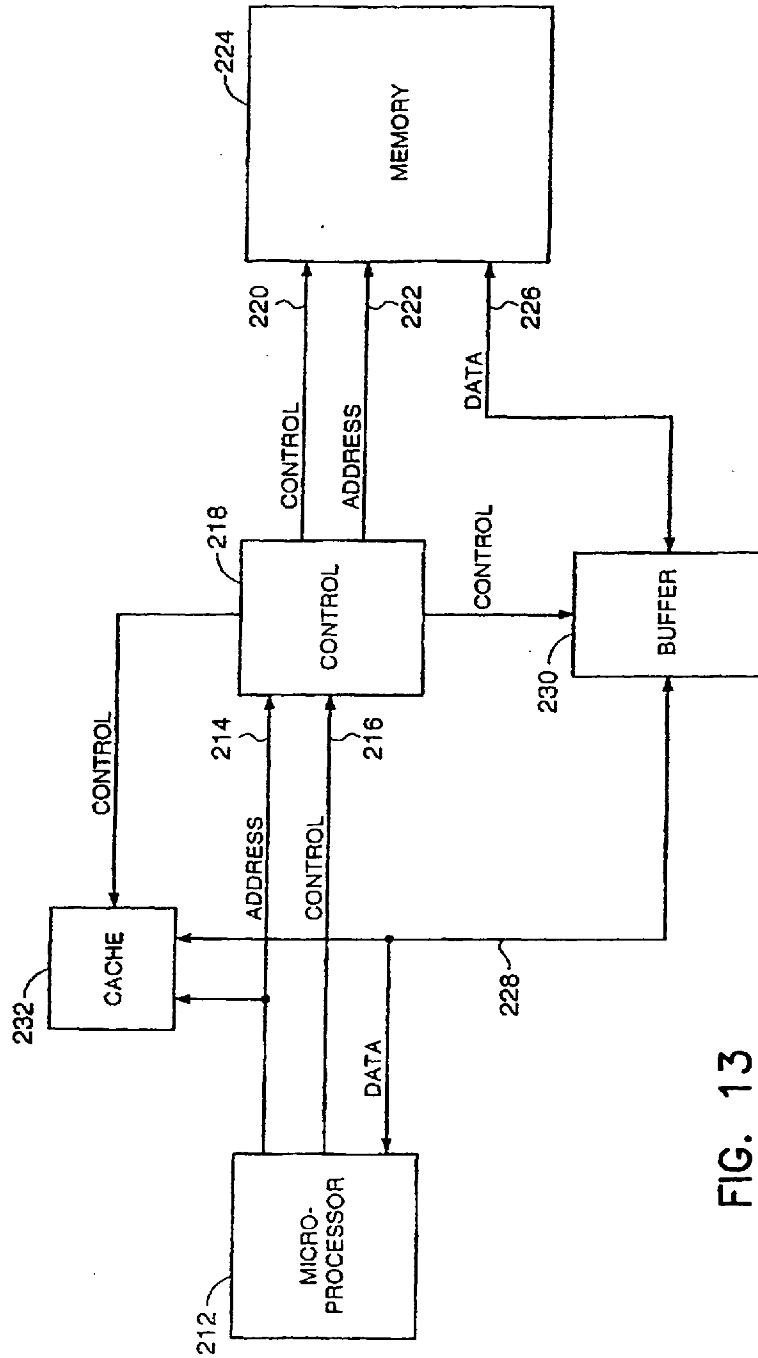

FIG. 13

COUNTER CONTROL CIRCUIT IN A BURST MEMORY

This application is a continuation-in-part of U.S. application Ser. No. 08/457,651, filed Jun. 1, 1995, entitled "Burst EDO Memory Device Address Counter" which is a continuation-in-part of U.S. application Ser. No. 08/386,894, filed Feb. 10, 1995, now U.S. Pat. No. 5,610,864, entitled "Burst EDO Memory Device with Maximum Write Cycle Timing" which is a continuation-in-part of U.S. application Ser. No. 08/370,761, filed of Dec. 23, 1994, now U.S. Pat. No. 5,526,320, and entitled "Burst EDO Memory Device," all of which are incorporated herein by reference.

FIELD OF THE INVENTION

This invention relates to internal address generation circuits and counter circuits for memory devices with burst access capability.

BACKGROUND OF THE INVENTION

Dynamic Random Access Memory devices (DRAMs) are among the highest volume and most complex integrated circuits manufactured today. Except for their high volume production, the state of the art manufacturing requirements of these devices would cause them to be exorbitantly priced. Yet, due to efficiencies associated with high volume production, the price per bit of these memory devices is continually declining. The low cost of memory has fueled the growth and development of the personal computer. As personal computers have become more advanced, they in turn have required faster and more dense memory devices, but with the same low cost of the standard DRAM. Fast page mode DRAMs are the most popular standard DRAM today. In fast page mode operation, a row address strobe (RAS*) is used to latch a row address portion of a multiplexed DRAM address. Multiple occurrences of the column address strobe (CAS*) are then used to latch multiple column addresses to access data within the selected row. On the falling edge of CAS* an address is latched, and the DRAM outputs are enabled. When CAS* transitions high the DRAM outputs are placed in a high impedance state (tri-state). With advances in the production of integrated circuits, the internal circuitry of the DRAM operates faster than ever. This high speed circuitry has allowed for faster page mode cycle times. A problem exists in the reading of a DRAM when the device is operated with minimum fast page mode cycle times. CAS* may be low for as little as 15 nanoseconds, and the data access time from CAS* to valid output data (tCAC) may be up to 15 nanoseconds; therefore, in a worst case scenario there is no time to latch the output data external to the memory device. For devices that operate faster than the specifications require, the data may still only be valid for a few nanoseconds. On a heavily loaded microprocessor memory bus, trying to latch an asynchronous signal that is valid for only a few nanoseconds is very difficult. Even providing a new address every 35 nanoseconds requires large address drivers which create significant amounts of electrical noise within the system. To increase the data throughput of a memory system, it has been common practice to place multiple devices on a common bus. For example, two fast page mode DRAMs may be connected to common address and data buses. One DRAM stores data for odd addresses, and the other for even addresses. The CAS* signal for the odd addresses is turned off (high) when the CAS* signal for the even addresses is turned on (low). This interleaved memory system provides data access at twice the

rate of either device alone. If the first CAS* is low for 20 nanoseconds and then high for 20 nanoseconds while the second CAS* goes low, data can be accessed every 20 nanoseconds or 50 megahertz. If the access time from CAS* to data valid is fifteen nanoseconds, the data will be valid for only five nanoseconds at the end of each 20-nanosecond period when both devices are operating in fast page mode. As cycle times are shortened, the data valid period goes to zero.

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead, data is held valid after CAS* goes high until sometime after the next CAS* low pulse occurs, or until RAS* or the output enable (OE*) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can be a complex function of when the column address inputs are valid, when CAS* falls, the state of OE* and when CAS* rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially CAS*) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM manufacturers.

Methods to shorten memory access cycles tend to require additional circuitry, additional control pins and nonstandard device pinouts. The proposed industry standard synchronous DRAM (SDRAM) for example has an additional pin for receiving a system clock signal. Since the system clock is connected to each device in a memory system, it is highly loaded, and it is always toggling circuitry in every device. SDRAMs also have a clock enable pin, a chip select pin and a data mask pin. Other signals which appear to be similar in name to those found on standard DRAMs have dramatically different functionality on a SDRAM. The addition of several control pins has required a deviation in device pinout from standard DRAMs which further complicates design efforts to utilize these new devices. Significant amounts of additional circuitry are required in the SDRAM devices which in turn result in higher device manufacturing costs.

In order for existing computer systems to use an improved device having a nonstandard pinout, those systems must be extensively modified. Additionally, existing computer system memory architectures are designed such that control and address signals may not be able to switch at the frequencies required to operate the new memory device at high speed due to large capacitive loads on the signal lines. The Single In-Line Memory Module (SIMM) provides an example of what has become an industry standard form of packaging memory in a computer system. On a SIMM, all address lines connect to all DRAMs. Further, the row address strobe (RAS*) and the write enable (WE*) are often connected to each DRAM on the SIMM. These lines inherently have high capacitive loads as a result of the number of device inputs driven by them. SIMM devices also typically ground the output enable (OE*) pin making OE* a less attractive candidate for providing extended functionality to the memory devices.

There is a great degree of resistance to any proposed deviations from the standard SIMM design due to the vast number of computers which use SIMMs. Industry's resis-

tance to radical deviations from the standard, and the inability of current systems to accommodate the new memory devices will delay their widespread acceptance. Therefore only limited quantities of devices with radically different architectures will be manufactured initially. This limited manufacture prevents the reduction in cost which typically can be accomplished through the manufacturing improvements and efficiencies associated with a high volume product.

What is needed, therefore, is an integrated memory device which has a standard DRAM pinout and both operates at high data speed and is compatible with existing memory systems. Further, internal address generation circuits and counters are needed to efficiently operate these high data rate memories.

SUMMARY OF THE INVENTION

The above mentioned problems with high data rate memory devices and other problems are addressed by the present invention and which will be understood by reading and studying the following specification. A memory device is described which operates in a burst access mode which includes counter control circuitry that advances a memory column address on one transition of a latch signal and access the memory column address on another transition of the latch signal.

In particular, the present invention describes a memory device having a plurality of addressable memory elements comprising an address counter to receive a first memory element address and adapted to generate a series of memory element addresses in response to a first transition direction of an address latch signal, and a buffer circuit to latch the series of memory element addresses in response to a second transition direction of the address latch signal. In one embodiment, the address latch signal can be an active low column address signal (CAS*) and the first transition direction of the address latch signal is a low to high transition in the CAS*. The second transition direction of the address latch signal is a high to low transition in the CAS*.

In another embodiment, an integrated memory circuit comprises a memory array having a plurality of addressable memory cells, and an address counter to receive a first memory cell address and adapted to generate a series of memory cell addresses in response to a first transition direction of an address latch signal. The integrated memory also comprises a buffer circuit coupled to the address counter to latch either the first memory cell address or the series of memory cell addresses in response to a second transition direction of the address latch signal, and access circuitry to access the memory array in response to an address latched in the buffer circuit. The buffer circuit can comprise a first multiplexer circuit having a first input coupled to an output of the address counter, a feed back circuit coupled a second input of the first multiplexer circuit, and a latch circuit adapted to receive an output of the first multiplexer. In another embodiment, the buffer circuit further comprises a second multiplexer circuit having a first input coupled to an external address input and a second input coupled to the output of the first multiplexer. In yet another embodiment, the address counter comprises a plurality of flip flips, a shift register coupled to the plurality of flip flops, and a multiplexer for enabling one of a plurality of counting sequences.

In still another embodiment, a method is described for accessing memory elements in a memory device. The method comprises the steps of latching a first memory element address in an address counter, generating a series of memory element addresses with the address counter in response to a first transition direction of an address latch signal, and latching the series of memory element addresses with a buffer circuit in response to a second transition direction of the address latch signal. The method can further include the step of accessing a memory element based upon the series of memory element addresses latched in the buffer in response to the second transition direction of the address latch signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a is a schematic diagram of a memory device in accordance with one embodiment of the present invention;

FIG. 2 is a table showing linear and interleaving addressing formats;

FIG. 3 is a timing diagram for a method of accessing the device of FIG. 1;

FIG. 4 is a timing diagram for a method of accessing the device of FIG. 1;

FIG. 5 is a schematic of a Single In-Line Memory Module (SIMM) in accordance with the present invention;

FIG. 6 is a schematic of a counter circuit of FIG. 1;

FIG. 7 is a buffer circuit of FIG. 1;

FIG. 8 is a timing diagram of the circuit of FIG. 7;

FIG. 9 is a schematic of a shift register circuit of FIG. 7;

FIG. 10 is a schematic of a flip-flop circuit;

FIG. 11 is a schematic of an enabled NAND gate;

FIG. 12 is a schematic of an enabled NOR gate; and

FIG. 13 is a schematic diagram of a system designed in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present inventions is defined only by the appended claims.

FIG. 1 is a schematic representation of a sixteen megabit device designed in accordance with the present invention. The device is organized as a 2 Meg×8 burst EDO DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array 12. The device of FIG. 1 may have an industry standard pinout for eight bit wide EDO DRAMs. An active-low row address strobe (RAS*) signal 14 is used to latch a first portion of a multiplexed memory address, from address inputs 16, in latch 18. The latched row address 20 is decoded in row decoder 22. The decoded row address is used to select a row of the memory array 12. A column address strobe (CAS*) signal 24 is used to latch a second portion of a memory address from address inputs 16 into address generation circuit 26. The latched column address 28 is decoded in column address decoder 30. The decoded column address is used to select a column of the memory array 12.

In a burst read cycle, data within the memory array located at the row and column address selected by the row

and column address decoders is read out of the memory array and sent along data path 32 to output latches. Data 10 driven from the burst EDO DRAM may be latched external to the device in synchronization with CAS* after a predetermined number of CAS* cycle delays (latency). For a two cycle latency design, the first CAS* falling edge is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second CAS* falling edge, and remains valid through the third CAS* falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during CAS* high intervals dependent on the state of the output enable and write enable (OE* and WE*) control lines, thus allowing additional time for the system to latch the output data. The data outputs remain valid throughout the burst read cycles with the exception of brief periods of data transition. During these periods of data transition, the output drivers may be turned off momentarily in order to aid data transition. This state of the output buffer should not be confused with the standard DRAM tri-state condition which is intended to release the data bus.

Once a row and a column address are selected, additional transitions of the CAS* signal are used to advance the column address within the address generation circuit in a predetermined sequence. The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the CAS* signal provided that OE* is maintained low, and WE* remains high. The output data signal levels may be but are not limited to being driven in accordance with standard CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. FIG. 2 is a table which shows linear and interleaved addressing sequences for burst lengths of 2, 4 and 8 cycles. The "V" for starting addresses A1 and A2 in the table represent address values that remain unaltered through the burst sequence. The column address may be advanced with each CAS* transition, each pulse, or multiple of CAS* pulses in the event that more than one data word is read from the array with each column address. When the address is advanced with each transition of the CAS* signal, data is also driven from the part after each transition following the device latency which is then referenced to each edge of the CAS* signal. This allows for a burst access cycle where the highest switching control line (CAS*) toggles only once (high to low or low to high) for each memory cycle. This is in contrast to standard DRAMs which require CAS* to go low and then high for each cycle, and synchronous DRAMs which require a full clock cycle (high and low transitions) for each memory cycle. For maximum compatibility with existing EDO DRAM devices, the invention will be further described in reference to a device designed to latch and advance a column address on falling edges of the CAS* signal.

In the burst access memory device, each new column address from the address generation circuit is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16. This burst sequence of data will continue for each CAS* falling edge until a predetermined number of data accesses equal to the burst length has occurred. A CAS* falling edge received after the last burst address has been generated will latch another column address from the address inputs 16 and a new burst sequence will begin. Read data is latched and output with each falling edge of CAS* after the first CAS* latency.

For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the CAS* signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is preferred. Additional input data words for storage at incremented column address locations are latched by CAS* on successive CAS* pulses. Input data from the input latches 34 is passed along data path 32 to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes will occur without the requirement of additional column addresses being provided on the address lines 16. After the predetermined number of burst writes has occurred, a subsequent CAS* pulse will latch a new beginning column address, and another burst read or write access will begin.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by CAS*. WE* low at the column address latch time selects a burst write access. WE* high at the column address latch time selects a burst read access. The level of the signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. Transitions of the WE* signal may be locked out during critical timing periods within an access cycle in order to reduce the possibility of triggering a false write cycle. After the critical timing period the state of WE* will determine whether a burst access continues, is initiated, or is terminated. Termination of a burst access places the DRAM in a state to receive another burst access command. Both RAS* and CAS* going high during a burst access will also terminate the burst access cycle and place the data drivers in a high impedance output state. Read data may remain valid at the device outputs if RAS* alone goes high while CAS* is active for compatibility with hidden refresh cycles, otherwise RAS* high alone may be used to terminate a burst access. A minimum write enable pulse width is only required when it is desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses. In the case of burst reads, WE* will transition from high to low to terminate a first burst read, and then WE* will transition back high prior to the next falling edge of CAS* in order to specify a new burst read cycle. For burst writes, WE* would transition high to terminate a current burst write access, then back low prior to the next falling edge of CAS* to initiate another burst write access.

A basic implementation of the device of FIG. 1 may include a fixed burst length of 4, a fixed CAS* latency of 2 and a programmable sequence of burst addresses. This basic implementation requires very little additional circuitry to the standard EDO page mode DRAM, and may be mass produced to provide the functions of both the standard EDO page mode and burst EDO DRAMs. This device also allows for the output enable pin (OE*) to be grounded for compatibility with many SIMM module designs. When not disabled (tied to ground), OE* is an asynchronous control which will prevent data from being driven from the part in a read cycle if it is inactive (high) prior to CAS* falling and remains inactive beyond CAS* rising. If these setup and hold con-

ditions are not met, then the read data may be driven for a portion of the read cycle. It is possible to synchronize the OE* signal with CAS*, however this would typically increase the CAS* to data valid delay time and doesn't allow for the read data to be disabled prior to RAS* high without an additional CAS* low pulse which would otherwise be unnecessary. In a preferred embodiment, if OE* transitions high at any time during a read cycle the outputs will remain in a high impedance state until the next falling edge of CAS* despite further transitions of the OE* signal.

Programmability of the burst length, CAS* latency and address sequences may be accomplished through the use of a mode register 40 which latches the state of one or more of the address input signals 16 or data signals 10 upon receipt of a write-CAS*-before-RAS* (WCBR) programming cycle. In such a device, outputs 44 from the mode register control the required circuits on the DRAM. Burst length options of 2, 4, 8 and full page as well as CAS* latencies of 1, 2 and 3 may be provided. Other burst length and latency options may be provided as the operating speeds of the device increase, and computer architectures evolve. The device of FIG. 1 includes programmability of the address sequence by latching the state of the least significant address bit during a WCBR cycle. Additional input signals may be used to decode an enable for setting the address sequence. For example, a specific value received on address lines A1–A7 in a WCBR cycle is decoded to specify that the sequence mode is to be set, and the state of A0 is used to specify which mode is selected. The burst length and CAS* latency for this particular embodiment are fixed. Other possible alterations in the feature sets of this DRAM include having a fixed burst mode only, selecting between standard fast page mode (non-EDO) and burst mode, and using the output enable (OE*) 42 in combination with RAS* to select between modes of operation. Also, a WCBR refresh cycle could be used to select the mode of operation rather than a control signal in combination with RAS*. A more complex memory device may provide additional modes of operation such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of WE* and OE* at RAS* falling time. One mode from a similar set of modes may be selected through the use of a WCBR cycle using multiple address or data lines to encode the desired mode. Alternately, a device with multiple modes of operation may have wire bond locations, or programmable fuses which may be used to program the mode of operation of the device.

The present invention is described with reference to several preferred embodiments. Just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including x1, x4, x8 and x16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the memory device of the present invention may take the form of many different memory organizations. It is believed that one who is skilled in the art of integrated circuit memory design can, with the aide of this specification design a variety of memory devices which do not depart from the spirit of this invention. It is therefore believed that detailed descriptions of all of the various memory device organizations applicable to this invention are not necessary.

A preferred pinout for the device of FIG. 1 is identical to the pinout for a standard EDO DRAM. The common pinout allows this new device to be used in existing memory designs with minimum design changes. The common pinout also allows for ease of new designs by those of skill in the art who are familiar with the standard EDO DRAM pinout. Variations of the described invention which maintain the standard EDO DRAM pinout include driving the CAS* pin with a system clock signal to synchronize data access of the memory device with the system clock. For this embodiment, it may be desirable to use the first CAS* active edge after RAS* falls to latch the row address, a later edge may be used to latch the first column address of a burst access cycle. After row and column addresses are latched within the device, the address may be incremented internally to provide burst access cycles in synchronization with the system clock. Other pin function alternatives include driving the burst address incrementing signal on the OE* pin since the part does not require a data output disable function on this pin. Other alternate uses of the OE* pin also allow the device to maintain the standard EDO pinout, but provide increased functionality such as burst mode access. The OE* pin may be used to signal the presence of a valid column starting address, or to terminate a burst access. Each of these embodiments provides for a high speed burst access memory device which may be used in current memory systems with a minimum amount of redesign.

FIG. 3 is a timing diagram for performing a burst read followed by burst write of the device of FIG. 1. In FIG. 3, a row address is latched by the RAS* signal. WE* is low when RAS* falls for an embodiment of the design where the state of the WE* pin is used to specify a burst access cycle at RAS* time. Next, CAS* is driven low with WE* high to initiate a burst read access, and the column address is latched. The data out signals (DQ's) are not driven in the first CAS* cycle. On the second falling edge of the GAS* signal the first data out is driven from the device after a CAS* to data access time (tCAC). Additional burst access cycles continue, for a device with a specified burst length of four, until the fifth falling edge of CAS* which latches a new column address for a new burst read access. WE* falling in the fifth CAS* cycle terminates the burst access, and initializes the device for additional burst accesses. The sixth falling edge of CAS* with WE* low is used to latch a new burst address, latch input data and begin a burst write access of the device. Additional data values are latched on successive CAS* falling edges until RAS* rises to terminate the burst access.

FIG. 4 is a timing diagram depicting burst write access cycles followed by burst read cycles. As in FIG. 3, the RAS* signal is used to latch the row address. WE* is shown as a "don't care" at the time RAS* falls for an embodiment of the present invention that does not utilize the state of WE* at RAS* time to select between burst and non-burst access modes. The first CAS* falling edge in combination with WE* low begins a burst write access with the first data being latched. Additional data values are latched with successive CAS* falling edges, and the memory address is advanced internal to the device in either an interleaved or sequential manner. On the fifth CAS* falling edge a new column address and associated write data are latched. The burst write access cycles continue until the WE* signal goes high in the sixth CAS* cycle. The transition of the WE* signal terminates the burst write access. The seventh CAS* low transition latches a new column address and begins a burst read access (WE* is high). The burst read continues until RAS* rises terminating the burst cycles.

It should be noted from FIGS. 3 and 4, that for burst read cycles the data remains valid on the device outputs as long as the OE* pin is low, except for brief periods of data transition. Also, since the WE* pin is low prior to or when CAS* falls, the data input/output lines are not driven from the part during write cycles, and the OE* pin may be grounded. Only the CAS* signal and the data signals toggle

at relatively high frequency, and no control signals other than CAS* are required to be in an active or inactive state for one CAS* cycle time or less. This is in contrast to SDRAMs which often require row address strobes, column address strobes, data mask, and read/write control signals to be valid for one clock cycle or less for various device functions. Typical DRAMs also allow for the column address to propagate through to the array to begin a data access prior to CAS* falling. This is done to provide fast data access from CAS* falling if the address has been valid for a sufficient period of time prior to CAS* falling for the data to have been accessed from the array. In these designs an address transition detection circuit is used to restart the memory access if the column address changes prior to CAS* falling. This method actually requires additional time for performing a memory access since it must allow for a period of time at the beginning of each memory cycle after the last address transition to prepare for a new column address. Changes in the column address just prior to CAS* falling may increase the access time by approximately five nanoseconds. An embodiment of the present invention will not allow the column address to propagate through to the array until after CAS* has fallen. This eliminates the need for address transition detection circuitry, and allows for a fixed array access relative to CAS*.

FIG. 5 is a schematic representation of a single in-line memory module (SIMM) designed in accordance with the present invention. The SIMM has a standard SIMM module pinout for physical compatibility with existing systems and sockets. Functional compatibility with EDO page mode SIMMs is maintained when each of the 2 Meg×8 memory devices 10, 12, 14 and 16 are operated in an EDO page mode. Each of the CAS* signals 18, 20, 22 and 24 control one byte width of the 32 bit data bus 26, 28, 30 and 32. A RAS* 34 signal is used to latch a row address in each of the memory devices, and is optionally used in combination with WE* 36 to select between page mode and burst mode access cycles. Address signals 16 provide a multiplexed row and column address to each memory device on the SIMM. In burst mode, only active CAS* control lines are required to toggle at the operating frequency of the device, or at half the frequency if each edge of the CAS* signal is used as described above. The data lines are required to be switchable at half of the frequency of the CAS* lines or at the same frequency, and the other control and address signals switch at lower frequencies than CAS* and the data lines. As shown in FIG. 5, each CAS* signal and each data line is connected to a single memory device allowing for higher frequency switching than the other control and address signals. Each of the memory devices 10, 12, 14 and 16 is designed in accordance with the present invention allowing for a burst mode of operation providing internal address generation for sequential or interleaved data access from multiple memory address locations with timing relative to the CAS* control lines after a first row and column address are latched.

BURST ADDRESS COUNTER

FIGS. 6 and 7 illustrate one embodiment of a two bit address counter included in the address generation circuit 26 of FIG. 1. The two bit burst address counter is comprised of a BEDO counter circuit 250 and two buffer circuits 272. The BEDO counter circuit 250 shown in FIG. 6 produces two counter bits, A0*_CNTR and A1*_CNTR, for a BEDO memory which has a burst length of four. Four clocked flip-flops 252(*a*)-(*d*) are used to produce the linear or interleaved count described above with reference to FIG. 2. The Q and Q* outputs of the flip-flops will toggle, if the R and S inputs are high, on a falling edge of a clock signal provided on the clock input. BEDOCAS is, therefore, used as the clock inputs to flip-flops 252(*a*) and (*c*) so that the flip-flops will advance on the rising edge of BEDOCAS*. Shift registers 254 and 256 are used to generate the clock signals for flip-flops 252(*b*) and (*d*). Multiplexer circuit 258 is used to switch the counter between linear and interleave mode by coupling either shift register 256 or 254 to flip-flop 252(*d*).

The output of NOR gate 260 is connected to the R input of flip-flops 252(*a*) and (*b*) and will be high when both the Enable and MODCH signals are low. The Enable signal is low when the columns of the memory array 12 are powered. The MODCH signal is used to indicate when a change in the BEDO mode (read or write) is initiated. The Q outputs of flip-flop 252 (*a*) will toggle on every clock signal and flip-flop 252(*b*) will toggle on ever-other clock signal. The outputs CY0* and CY1* are used to count to four. These outputs indicate, therefore, when the counter circuit 250 has completed four burst steps.

Flip-flops 252(*c*) and (*d*) operate in a similar manner, but start at an externally input column address and can count either linearly or interleaved. NAND gate 262 is provided as a means to couple the R and S inputs of flip-flops 252(*c*) and (*d*) either the external addresses A0 and A1 or to a high voltage level. The BEDO signal is an internal memory signal which indicates that the memory is operating in a BEDO state, and the NEWBURST signal indicates when a new data burst is initiated. The new data burst can be initiated by a variety of events, such as a mode change, following an interrupt in the burst operation, or after a completed burst sequence. When both BEDO and NEWBURST are high the output of NAND gate 262 is low. Buffers 264 are enable so that addresses A0 and A1 are coupled to NAND gates 266 which in turn are coupled to NAND gates 268. The outputs of NAND gates 266 and 268 are coupled to the S and R inputs of flip-flops 252(*c*) and (*d*) to provide the initial column address for the start of a burst sequence. Column address latch input (CAL) can be selectively used to block changes in the external addresses A0 and A1 from effecting the counter circuit.

The first rising edge of BEDOCAS* couples addresses A0 and A1 to the counter address A0*_CNTR and A1*_CNTR through flip-flops 252(*c*) and (*d*). NEWBURST goes low to isolate the address inputs A0 and A1 from the flip-flops. NEWBURST also activates pull-up transistors 271. On the second, third and fourth clock signals, flip-flops 252(*c*) and (*d*) will advance either linearly or in an interleave pattern from the initial external column address.

Buffer circuit 272 illustrated in FIG. 7 is also included in address generation circuit 26 of FIG. 1. The buffer circuit 272 latches counter address A0*_CNTR, produced by circuit 250 described above, when BEDOCAS* is high. A new A0*_CNTR signal is coupled to outputs BCA0* and BCA0 on the falling edge of BEDOCAS*. While only one buffer circuit 272 is described, it will be understood that the memory includes a buffer circuit for each of the address bits which are advanced by the counter, A0 and A1 in the embodiment shown in FIG. 6.

Multiplexer 276, in response to LBEDO, couples either external address A0 to the input of NAND gate 280 or the output of multiplexer 274. Multiplexer 274, likewise, couples either A0*_CNTR or the output of feed-back inverter 277 to an input of multiplexer 276. The column address latch signal (CAL) described above can be used to selectively block changes in the external address line A0 from effecting BCA0.

Referring to the timing diagram of FIG. 8, the operation of the buffer circuit 272 of FIG. 7 is described. During a BEDO operation the first external CAS* signal is used to load the initial column address, including bit A0. Both counter circuit 250 and buffer circuits 272, therefore, latch an initial column address on the first CAS* falling edge. In this example, initial address A0 is a high logic level. The falling edge of BEDOCAS*, a delayed CAS* signal, couples A0 to A0*_CNTR as a low logic level. LBEDO goes low with CAS* and couples address line A0 to BCA0 through multiplexer 276. LBEDO goes high after a time delay following the first falling edge of CAS* and remains high until the burst sequence is completed or terminated. The rising edge of LBEDO switches multiplexer 276 such that the output of multiplexer 274 is coupled to NAND gate 280.

On the first rising edge of BEDOCAS*, the output of feed-back inverter 277 is connected to the output of multiplexer 274. The rising edge of BEDOCAS* is also used to clock counter circuit 250 as described above. On the falling edge of BEDOCAS*, the new A0*_CNTR signal (high level) produced by circuit 250 is coupled to BCA0 and BCA0*. When the CAL signal goes high, the outputs of NAND gates 280 and 282 also go high to latch a column address in NAND gates 178(*a*) and (*b*). Conversely, when CAL goes low, the output of multiplexer 276 is passed through gates 280, 282, and 278 to outputs BCA0* AND BCA1*.

The BEDO counter circuit 250 and the buffer circuit 272 simplify the timing of the burst EDO memory circuit by allowing a method to be used in which the column address is advanced by the rising edge of CAS* and then the new advanced column address is latched in an access buffer by using the falling edge of CAS*. This circuitry, therefore, eliminates the need to both advance the column address and access the new column on the falling edge of CAS*. Performing both operation on one system clock (CAS*) cycle substantially slows the memory.

FIG. 9 is a schematic representation of an embodiment of the shift registers 254 and 256 of FIG. 6. The output of the clock enable circuit 120 is a logical function of the CLKIN* and the toggle condition signal (Q) received from the multiplexer of FIG. 6. It is desired to provide a glitch free clock signal from the clock enable circuit which will clock a counter element when the clock signal rises (in synchronization with the previous counter element). When the clock signal rises, the input 68 is allowed to pass through to latch 124 and the output is forced high by signal 125. Forcing the output high prevents the output from switching in response to transitions on the input which occur after rising edges of the clock as the counter is advanced. When the input clock signal goes low, if the input 68 was high, the output of latch 124 will be latched high, and the output of the clock enable circuit will go low indicating that the next counter stage is to be clocked on the next rising edge of the clock. When the next rising clock edge occurs, the output of the clock enable circuit will be forced back high, and input 68 which is now low will pass through to hold the output high when the clock transitions back low. Power-up input (PWRUP*) 94 when high will force the clock enable circuit output to a high state, preventing the next counter stage from advancing.

FIG. 10 is a schematic diagram of one embodiment of the flip-flops 252 of FIG. 6. The flip-flop is comprised of two cross coupled Enable NAND gates, and two cross coupled Enable NOR gates. This embodiment of the flip-flop has active low set (S*) and reset (R*) inputs, a clock input, a true output and a compliment output. Examples of Enable NAND and Enable NOR gates are provided in FIGS. 11 and 12 respectively.

FIG. 13 is a schematic representation of a data processing apparatus designed in accordance with the present invention. In FIG. 15, microprocessor 212 is connected via address lines 214 and control lines 216 to a memory control circuit 218. The memory control circuit provides address and control signals on lines 222 and 220 respectively to a burst access memory device 224. The burst access memory device sends and receives data over data bus 226. Optional data bus buffer 230 between memory data bus 226 and microprocessor data bus 228 allows for amplification of the data signals, and/or synchronization with the microprocessor and memory control signals. A fast static random access memory (SRAM) cache circuit 232 is also optional and provides higher speed access to data stored in the cache from the memory circuit or the microprocessor. Memory control circuit 218 may be incorporated within the microprocessor. The memory control circuit provides the required address strobe signals, address signals and read/write control signals required for burst mode access of the memory circuit. The capability of the processor to access the memory in a burst mode allows for the design of a computer with relatively high memory bandwidth without the requirement of a fast SRAM cache. SRAMs which are fast enough to provide memory access without wait states can significantly add to the cost of a computer. Thus the burst access memory device of the present invention allows for medium to high performance computers to be manufactured at a cost which is significantly less than those manufactured today. Use of the burst access memory device of the present invention in cooperation with a fast SRAM cache allows for an even higher performance computer design by providing fast burst access of main memory in the event of a cache miss.

In operation, the microprocessor reads data from the memory device by supplying address and control signals to the memory device through the memory control circuit. In response to an initial address, a read command and an access cycle strobe, the memory device begins to access a first data word at the initial address. A second access cycle strobe advances the address within the memory device in a second access period of the burst access, and initiates a read access of data from a second address. For a latency of two, the first data is driven from the memory device after the second access cycle strobe signal occurs. Typically the first data is latched in the microprocessor in response to a third access cycle strobe which occurs at the beginning of a third access cycle period of the burst access. The third access cycle strobe also causes the second data value to be driven from the memory device. The third access cycle strobe also causes a third address to be generated within the memory device, and a third data access begins. Data is latched in the microprocessor in response to fourth, fifth and sixth access cycle strobes. In this manner four data values are received in the microprocessor in response to a single address and a plurality of access cycle strobes. The microprocessor may provide a second address to the memory device with the fifth access cycle strobe signal if the memory device is designed to perform four word burst sequences and additional data values are required from the memory. In this case, a second four word burst sequence is begun while the microprocessor is receiving data from the first four word burst. The data buffer 230 may be used to synchronize data from the memory device received in response to the access cycle strobe signal with a system clock which is connected to the microprocessor. For write cycles, there is typically no latency. Data for write cycles is provided with each access cycle strobe signal in a burst write sequence.

In an alternate embodiment, initial burst access addresses are latched in the memory in response to falling edges of the address strobe, and additional burst addresses are generated within the memory in response to rising edges of the address strobe. The additional addresses are used to perform memory accesses in response to falling edges of the address strobe. In this manner, generation of the address for the next access cycle is begun in advance. This address may be compared with the initial address to detect an end of burst sequence condition. When the burst access is complete or terminated, a new initial address is latched in response to a falling address strobe signal.

For the purposes of this specification a microprocessor may be, but is not limited to, a microprocessor, a microcontroller, a digital signal processor, or an arithmetic processor. A signal may refer to, but is not limited to, information transferred via a conductor, or a conductor for transferring information. A node may refer to, but is not limited to, an input point, an output point, an intersection of conductors, or a point along a conductor.

CONCLUSION

A memory device has been described in detail which can operate in a burst access mode for fast data access rates. The memory device includes an address counter which advances a column address in a predetermined manner during burst operation. The column address starts at an initial address provided on external address lines and advances to the next column address on the rising edge of a CAS* signal. A buffer circuit is included which latches the column address provided by the address counter for use in accessing the column. The buffer circuit is responsive to the falling edge of the CAS* signal. The memory device, therefore, both advances the column address and accesses the new column on one CAS* cycle. By using both the rising and falling edges of the CAS* signal, the memory device to operate within timing constraints for standard DRAM memory devices.

While the present invention has been described with reference to preferred embodiments, numerous modifications and variations of the invention will be apparent to one of skill in the art without departing from the scope of the invention. For example, the clock signal for the flip-flops of counter circuit 250 could be generated using a timing circuit triggered on the falling edge of CAS*. This alternative embodiment allows the two bit counter to be advanced between the falling edges of successive CAS* cycle.

What is claimed is:

1. A memory device having a plurality of addressable memory elements comprising:

an address counter to receive a first memory element address and adapted to generate a series of memory element addresses in response to a first transition direction of an address latch signal; and

a buffer circuit to latch the series of memory element addresses in response to a second transition direction of the address latch signal;

the buffer circuit comprises:

a first multiplexer circuit having a first input coupled to an output of the address counter;

a feed back circuit coupled between an output of the first multiplexer circuit and a second input of the first multiplexer circuit; and

a latch circuit interposed between the output of the first multiplexer circuit and the feedback circuit, and adapted to receive an output of the first multiplexer circuit.

2. The memory device of claim 1 wherein the address latch signal is an active low column address signal (CAS*).

3. The memory device of claim 2 wherein the first transition direction of the address latch signal is a low to high transition in the CAS*.

4. The memory device of claim 2 wherein the second transition direction of the address latch signal is a high to low transition in the CAS*.

5. The memory device of claim 1 wherein the series of memory element addresses is one of a plurality of predetermined burst address sequences.

6. The memory device of claim 5 where the plurality of predetermined burst address sequences comprises an interleaved address sequence and a linear address sequence.

7. The memory device of claim 1 further comprising an address sequence select circuit electrically coupled to the address counter.

8. The memory device of claim 1 wherein the buffer circuit comprises:

a multiplexer circuit responsive to the address latch signal for receiving and latching the series of memory element addresses.

9. The memory device of claim 8 wherein the buffer circuit further comprises:

a second multiplexer circuit to latch the first memory element address.

10. An integrated memory circuit comprising:

a memory array having a plurality of addressable memory cells;

an address counter to receive a first memory cell address and adapted to generate a series of memory cell addresses in response to a first transition direction of an address latch signal;

a buffer circuit coupled to the address counter to latch either the first memory cell address or the series of memory cell addresses in response to a second transition direction of the address latch signal; and

access circuitry to access the memory array in response to an address latched in the buffer circuit;

the buffer circuit comprises:

a first multiplexer circuit having a first input coupled to an output of the address counter;

a feed back circuit coupled between an output of the first multiplexer circuit and a second input of the first multiplexer circuit; and

a latch circuit interposed between the output of the first multiplexer circuit and the feedback circuit, and adapted to receive an output of the first multiplexer circuit.

11. The integrated memory circuit of claim 10 wherein the address latch signal is an active low column address signal (CAS*).

12. The integrated memory circuit of claim 11 wherein the first transition direction of the address latch signal is a low to high transition in the CAS*.

13. The integrated memory circuit of claim 11 wherein the second transition direction of the address latch signal is a high to low transition in the CAS*.

14. The integrated memory circuit of claim 10 wherein the buffer circuit further comprises:

a second multiplexer circuit having a first input coupled to an external address input and a second input coupled to the output of the first multiplexer circuit.

15. The integrated memory circuit of claim 10 wherein the address counter comprises:

a plurality of flip-flops;

a shift register coupled to the plurality of flip-flops; and

a multiplexer for enabling one of a plurality of counting sequences.

16. A method of accessing memory elements in a memory device, the method comprising the steps of:

receiving a first memory element address on address inputs;

latching the first memory element address in an address counter;

generating a series of memory element addresses with the address counter in response to a first transition direction of an address latch signal; and

latching the series of memory element addresses with a buffer circuit in response to a second transition direction of the address latch signal, the step of latching the series of memory element addresses comprises the sub-steps of:

coupling the first memory element address to a latch in the buffer circuit via a multiplex circuit,

coupling an output of the latch through a feedback circuit and the multiplex circuit to an input of the latch on the first transition direction of the address latch signal, and

coupling a subsequent memory element address from the address counter to the input of the latch on the second transition direction of the address latch signal.

17. The method of claim 16 further including the step of:

accessing a memory element based upon the series of memory element addresses latched in the buffer circuit in response to the second transition direction of the address latch signal.

18. The method of claim 17 wherein the series of memory element addresses is generated in a selectable one of a plurality of predetermined sequences.

19. The method of claim 16 further including the step of:

latching the first memory element address in the buffer circuit simultaneously with the step of latching the first memory element address in the address counter.

20. A method of accessing memory elements in a memory device, the method comprising the steps of:

receiving a first memory element address on address inputs;

latching the first memory element address in an address counter and a buffer circuit on a first active transition of an address latch signal;

generating a series of memory element addresses with the address counter in response to subsequent in-active transitions of the address latch signal; and

latching the series of memory element addresses in the buffer circuit in response to active transitions of the address latch signal, the step of latching the series of memory element addresses comprises the sub-steps of:

coupling the first memory element address to a latch in the buffer circuit via a multiplex circuit,

coupling an output of the latch through a feedback circuit and the multiplex circuit to an input of the latch on the active transition of the address latch signal, and

coupling a subsequent memory element address from the address counter to the input of the latch on the inactive transition of the address latch signal.

21. The method of claim 20 further including the step of:

accessing a memory element based upon the series of memory element addresses latched in the buffer circuit in response to the second transition direction of the address latch signal.

22. The method of claim 20 wherein the series of memory element addresses is generated in a selectable one of a plurality of predetermined sequences.

* * * * *

RECYCLED

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United States Patent [19]

Manning

[11] **Patent Number:** 5,729,503

[45] **Date of Patent:** Mar. 17, 1998

[54] **ADDRESS TRANSITION DETECTION ON A SYNCHRONOUS DESIGN**

[75] Inventor: **Troy A. Manning**, Boise, Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **506,438**

[22] Filed: **Jul. 24, 1995**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 386,894, Feb. 10, 1995, Pat. No. 5,610,864, which is a continuation-in-part of Ser. No. 370,761, Dec. 23, 1994, Pat. No. 5,526,320.

[51] **Int. Cl.**[6] G11C 8/00

[52] **U.S. Cl.** 365/233.5; 365/189.05; 365/202; 365/230.08

[58] **Field of Search** 365/233.5, 230.08, 365/189.05, 202

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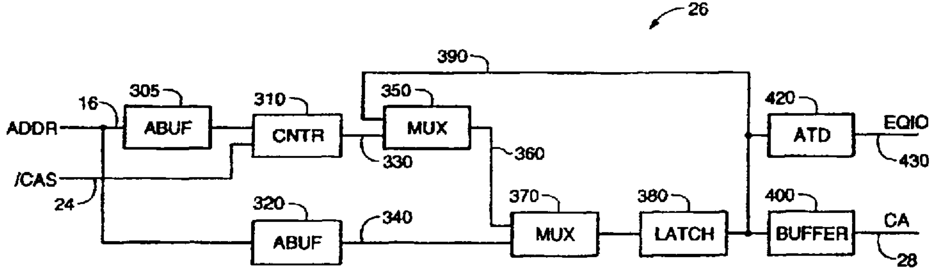
Primary Examiner—Do Hyun Yoo
Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

An integrated circuit memory device is designed to perform high speed burst access read and write cycles. An address strobe signal is used to latch a first address. During a burst access cycle the address is incremented internal to the device with additional address strobe transitions. A new memory address is only required at the beginning of each burst access. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at the device cycle frequency. A transition of the Read/Write control line during a burst access is used to terminate the burst access and initialize the device for another burst access. The memory device maintains compatibility with nonburst mode devices such as Extended Data Out (EDO) and Fast Page Mode through bond option or mode selection circuitry. A multiplexer selects between the input address and the burst address generator output to feed an asynchronous address transition detection circuit. The address transition detection circuit generates an equilibration control signal between memory access cycles.

8 Claims, 7 Drawing Sheets



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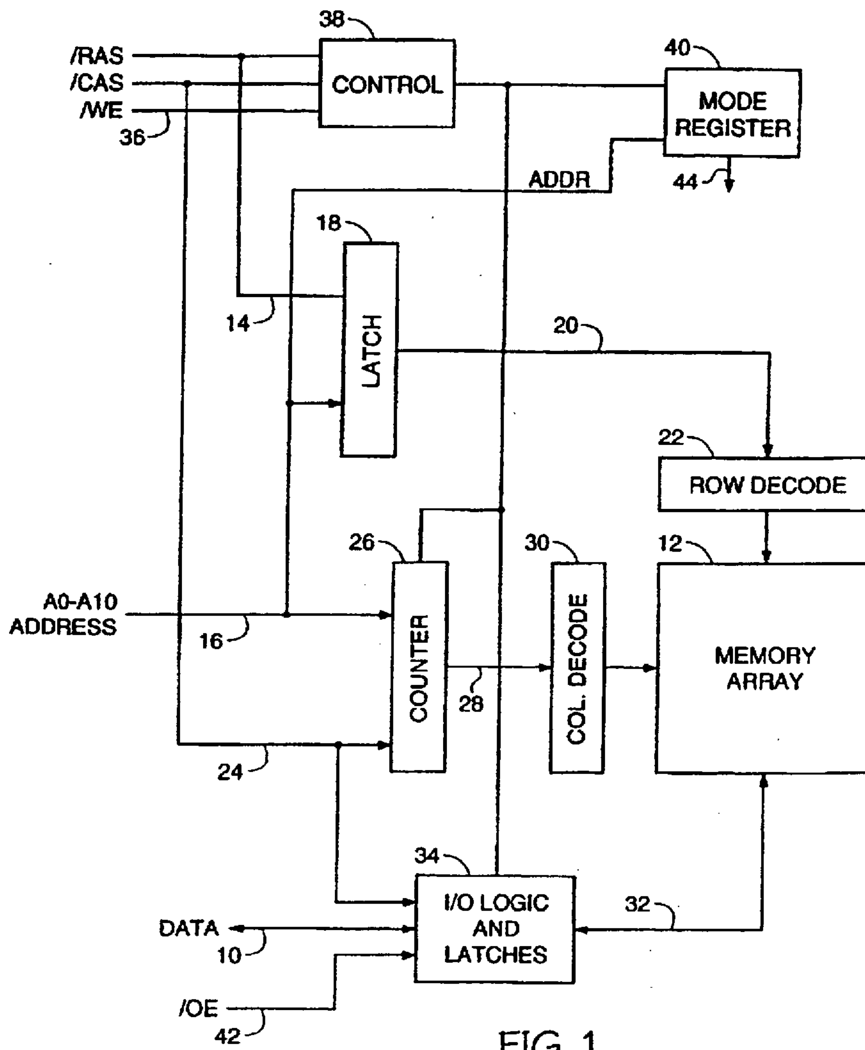

FIG. 1

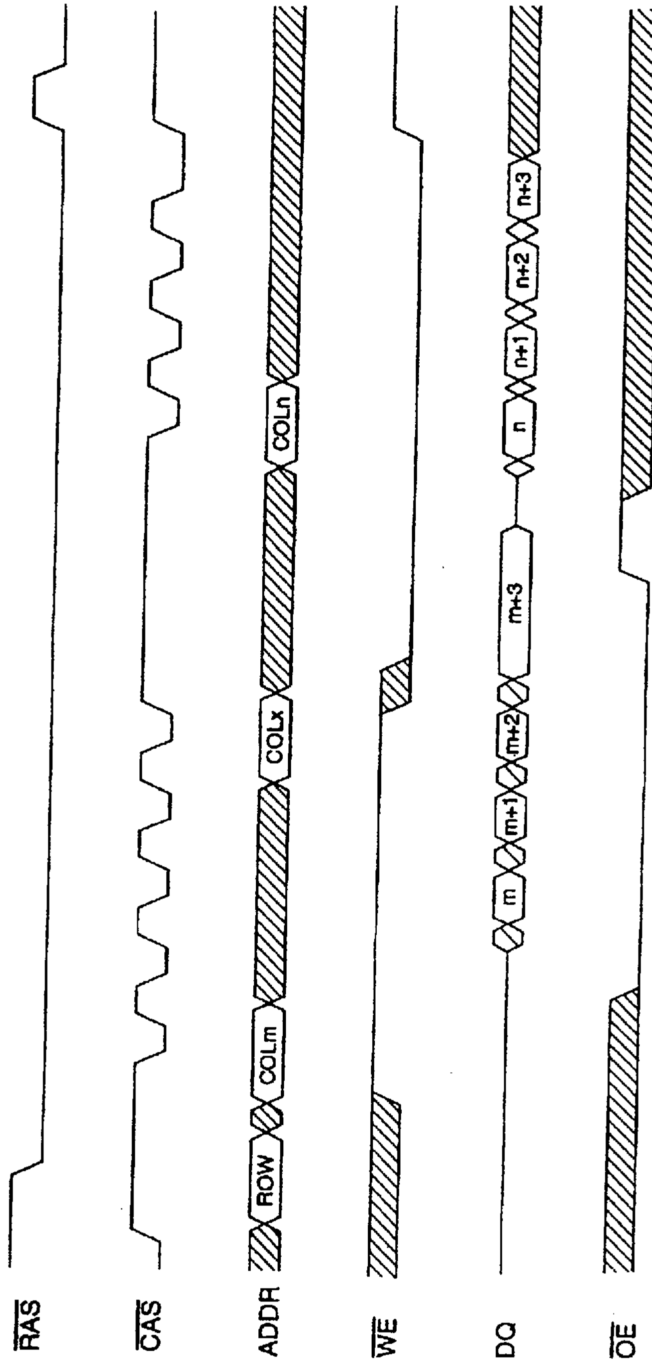

FIG. 2

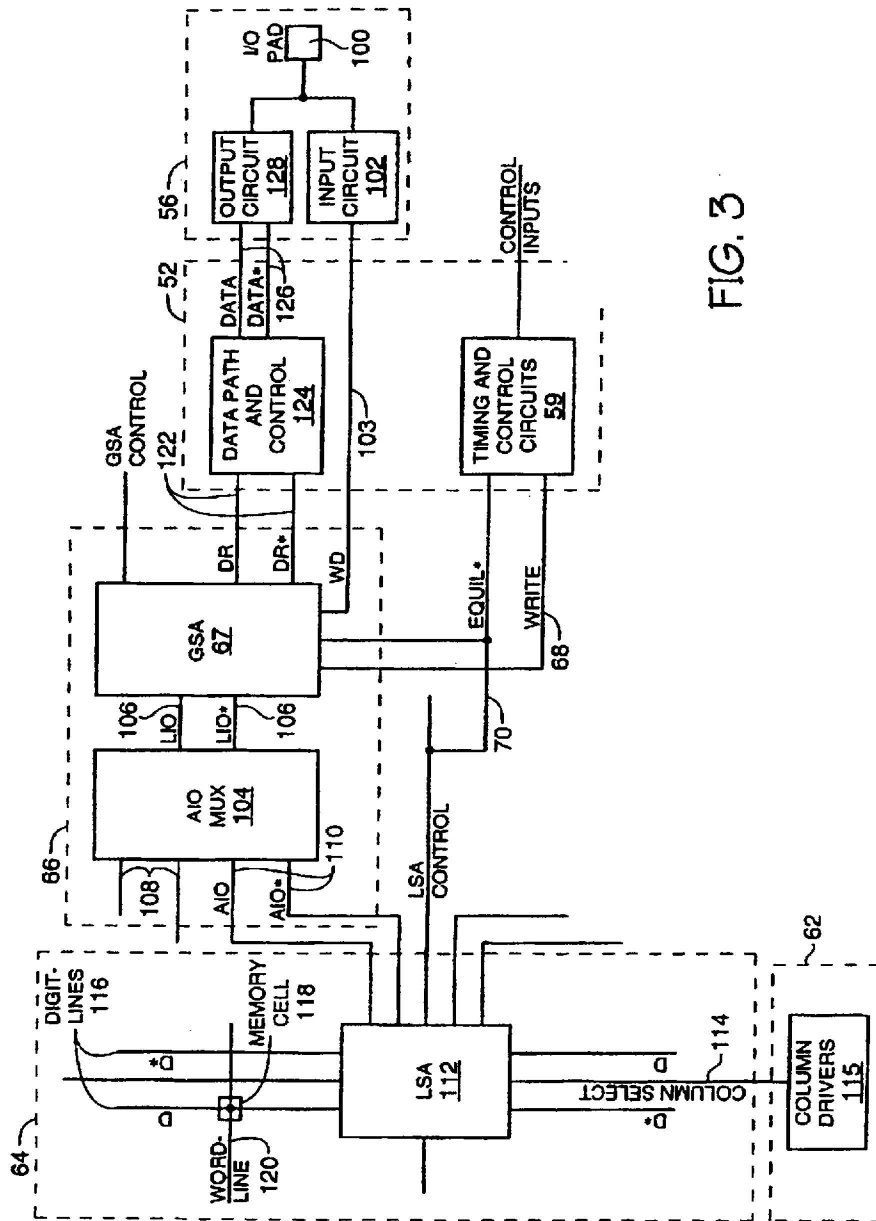

FIG. 3

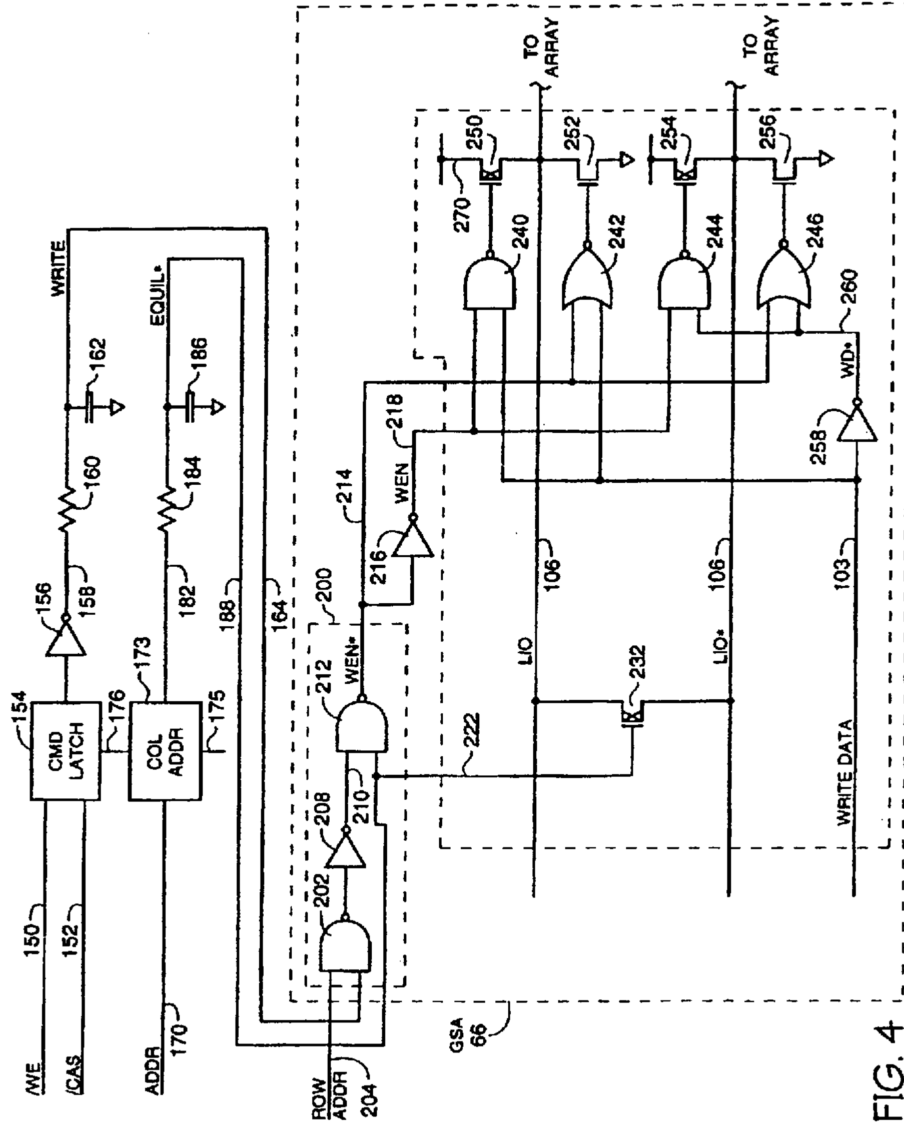

FIG. 4

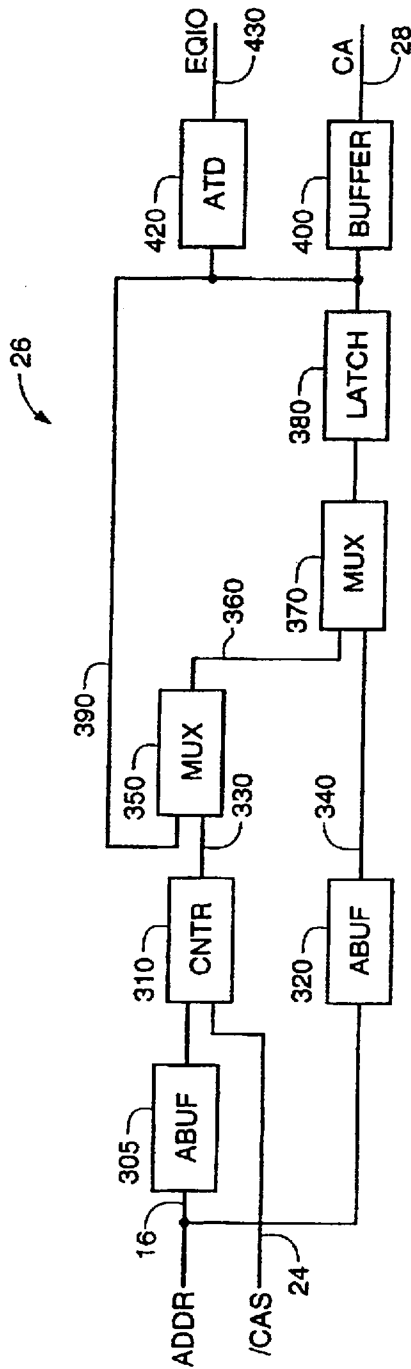

FIG. 5

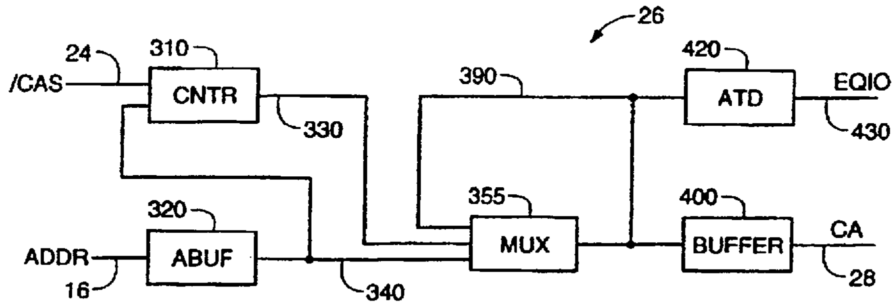

FIG. 6

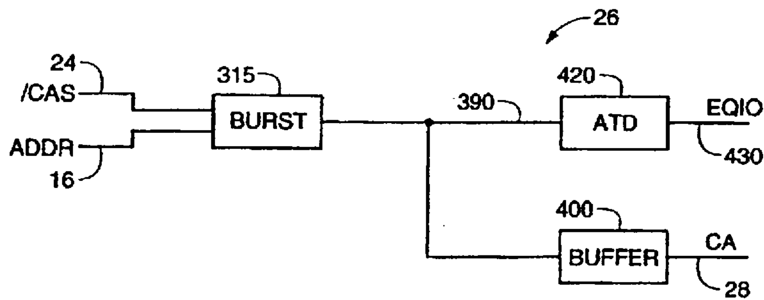

FIG. 7

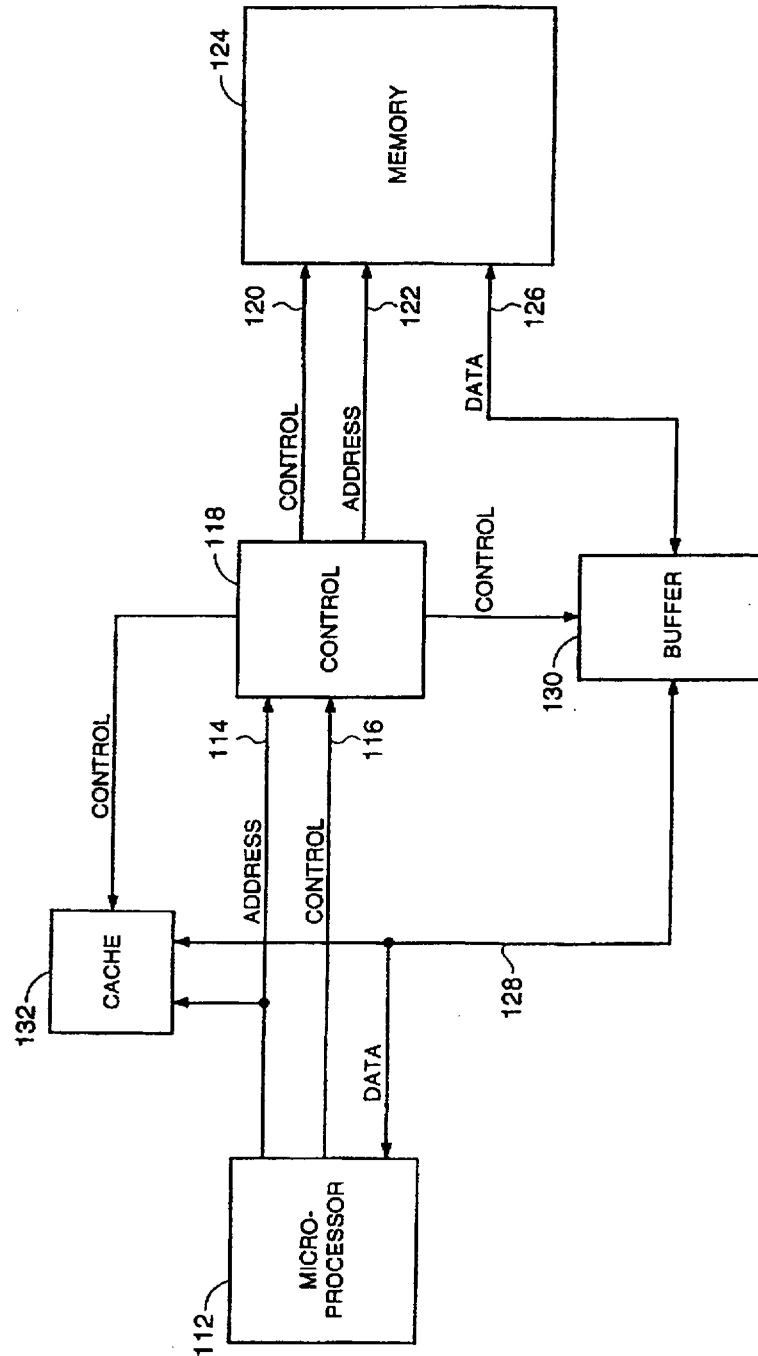

FIG. 8

ADDRESS TRANSITION DETECTION ON A SYNCHRONOUS DESIGN

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation in part of application Ser. No. 08/386,894 filed Feb. 10, 1995, now U.S. Pat. No. 5,610,864 which is a continuation in part of application Ser. No. 08/370,761 filed Dec. 23, 1994 now U.S. Pat. No. 5,526,320.

FIELD OF THE INVENTION

This invention relates to memory device architectures designed to provide high density data storage with high speed read and write access cycles. This invention relates more specifically to equilibration of data lines between memory access cycles in a device designed to operate in a burst access mode.

BACKGROUND OF THE INVENTION

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead, data is held valid after /CAS goes high until sometime after the next /CAS low pulse occurs, or until/RAS or the output enable (/OE) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can be a complex function of when the column address inputs are valid, when /CAS falls, the state of/OE and when /CAS rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially /CAS) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM manufacturers.

Methods to shorten memory access cycles tend to require additional circuitry, additional control pins and nonstandard device pinouts. The proposed industry standard synchronous DRAM (SDRAM) for example has an additional pin for receiving a system clock signal. Since the system clock is connected to each device in a memory system, it is highly loaded, and it is always toggling circuitry in every device. SDRAMs also have a clock enable pin, a chip select pin and a data mask pin. Other signals which appear to be similar in name to those found on standard DRAMs have dramatically different functionality on a SDRAM. The addition of several control pins has required a deviation in device pinout from standard DRAMs which further complicates design efforts to utilize these new devices. Significant amounts of additional circuitry are required in the SDRAM devices which in turn result in higher device manufacturing costs.

It is desirable to design and manufacture a memory device having a standard DRAM pinout and a burst mode of operation where multiple data values can be sequentially written to or read from the device in response to a single address location and multiple access cycle strobes. It is also desirable that this new memory device operate at higher frequencies than standard DRAMs.

In a standard DRAM device, equalization of internal data I/O lines is performed in response to column address transitions in preparation for reading or writing data from another memory cell, and also in response to a receipt of a write command to reduce the maximum signal transition on the data lines once the write drivers are enabled. Since there is a relatively wide time period in which column addresses may become valid, it has been advantageous to use an asynchronous address transition detection circuit to generate an equilibration control signal in response to address transitions. In EDO and fast page mode devices for example, the column address is treated as valid during a page mode cycle while /CAS is high. A read cycle will begin while /CAS is high at the column address indicated by the column address input signals. However, the column address is allowed to change until /CAS falls. Any column address change during the /CAS high time will require a new equilibration of I/O lines and the selection of the new column. When CAS falls, the column address is latched and further transitions are masked. Equilibration of I/O lines allows for faster sensing of read data, and for faster writing of input data. If the data lines are each equalized to one half of Vcc for example, then the write data drivers will only need to drive one line from half Vcc to ground, and the other from half Vcc to Vcc. Otherwise, if the write data is not equal to the data previously on the I/O lines, the write data drivers will need to drive both true and compliment I/O lines a full Vcc swing for each data bit being written. Equalization of the data I/O lines reduces the maximum write cycle time by eliminating the worst case signal swing conditions. A similar situation exists during read cycles. In a read cycle, data sense amplifiers only need to drive an equilibrated I/O line from half Vcc to Vcc or ground. If the I/O lines were not equilibrated, the sense amplifiers would need to be large enough to overcome the full data signals on the I/O lines in a read cycle in a short period of time to allow for fast data access. A simple method of equilibrating the I/O lines is to: disable I/O line drivers; isolate the I/O lines from the digit lines; and couple complimentary I/O lines together. When a true I/O line is coupled to a complimentary I/O line, a logic high will be coupled to a logic low and each line will equalize to a potential approximately half way between a high and a low. It is important to disable the I/O line drivers during equilibration to prevent a true logic driver from being coupled to a complimentary logic driver which will draw excessive current from the logic high source to the logic low source.

In a burst access memory device, each access cycle can begin at a fixed point in time relative to the access cycle strobe or clock signal. In this case, an asynchronous address detection circuit is not required since address changes can be restricted to a fixed point in time relative to the access cycle strobe.

SUMMARY OF THE INVENTION

An integrated circuit memory device with a standard DRAM pinout is designed for high speed data access and for compatibility with existing memory systems. A high speed burst mode of operation is provided where multiple sequential accesses occur following a single column address, and read data is output relative to the /CAS control signal. In the burst mode of operation the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at high speeds. Only one control line per memory chip (/CAS) must toggle at the operating frequency in order to clock the internal address counter and the data input/output latches. The load on each /CAS is typically less than the load on the other control signals

(/RAS, /WE and /OE) since each /CAS typically controls only a byte width of the data bus.

A single integrated circuit die has both burst mode access and page mode access capabilities. In page mode operation, the equilibrate signal is generated asychronously in response to column address transitions while /CAS is high. In burst mode, the equilibrate control signal is generated synchronously in response to /CAS transitions which control the generation of burst addresses. A multiplexer is used to direct the input address or the burst address to the address transition detection circuit. Among other benefits, use of the asynchronous address transition detection circuit in the burst mode eliminates the requirement for a synchronous equilibration control signal generation circuit, and minimizes the impact of the burst address path on the optimized asynchronous address path. In operation, at the beginning of a burst access, the initial burst address is fed through the asynchronous address path to the address transition detection circuit to generate an equilibrate signal, then the address path is switched to the burst address generator. At the beginning of each access cycle within the burst access the burst address will generate an equilibrate signal through the address transition detection circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention as well as objects and advantages are best understood by reference to the appended claims, detailed description of particular embodiments and accompanying drawings where:

FIG. 1 is an electrical schematic diagram of a memory device in accordance with one embodiment of the invention;

FIG. 2 is a timing diagram for a method of accessing the device of FIG. 1;

FIG. 3 is block level schematic of a data path portion of the device of FIG. 1;

FIG. 4 is a more detailed schematic of a portion of the circuitry of FIG. 3;

FIG. 5 is schematic diagram of a portion of the column address path of the device of FIG. 1;

FIG. 6 is an alternate schematic diagram of a portion of the column address path of the device of FIG. 1;

FIG. 7 is another alternate schematic diagram of a portion of the column address path of the device of FIG. 1; and

FIG. 8 is a schematic diagram of a computer system designed in accordance with the teachings of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a schematic representation of a sixteen megabit device designed in accordance with the present invention. The device is organized as a 2 Meg×8 burst EDO DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array 12. The device of FIG. 1 has an industry standard pinout for eight bit wide EDO DRAMs. An active-low row address strobe (/RAS) signal 14 is used to latch a first portion of a multiplexed memory address, from address inputs A0 through A10 16, in latch 18. The latched row address 20 is decoded in row decoder 22. The decoded row address is used to select a row of the memory array 12. A column address strobe (/CAS) signal 24 is used to latch a second portion of a memory address from address inputs 16 into column address counter 26. The latched column address 28 is decoded in column address decoder 30. The decoded column address is used to select a column of the memory array 12.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 32 to output latches 34. Data 10 driven from the burst EDO DRAM may be latched external to the device in synchronization with /CAS after a predetermined number of /CAS cycle delays (latency). For a two cycle latency design, the first /CAS falling edge is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second /CAS falling edge, and remains valid through the third /CAS falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers 34 continue to drive the data lines without tri-stating the data outputs during /CAS high intervals dependent on the state of the output enable and write enable (/OE and /WE) control lines, thus allowing additional time for the system to latch the output data. Once a row and a column address are selected, additional transitions of the /CAS signal are used to advance the column address within the column address counter in a predetermined sequence. The time at which data becomes valid at the outputs of the burst EDO DRAM is dependent only on the timing of the /CAS signal provided that/OE is maintained low, and/WE remains high. The output data signal levels may be driven in accordance with, but are not limited to, CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. The column address may be advanced with each /CAS transition, each pulse, or multiple of /CAS pulses in the event that more than one data word is read from the array with each column address. When the address is advanced with each transition of the /CAS signal, data is also driven from the part after each transition following the device latency which is then referenced to each edge of the /CAS signal. This allows for a burst access cycle where the highest switching control line (/CAS) toggles only once (high to low or low to high) for each memory cycle. This is in contrast to standard DRAMs which require /CAS to go low and then high for each cycle, and synchronous DRAMs which require a full clock cycle (high and low transitions) for each memory cycle. For maximum compatibility with existing EDO DRAM devices, the invention will be further described in reference to a device designed to initiate access cycles on falling edges of the /CAS signal. For designs where falling edges of the /CAS signal initiate an access cycle, the falling edge may be said to be the active transition of the /CAS signal.

In the burst access memory device, each new column address from the column address counter is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16. This burst sequence of data continues for each /CAS falling edge until a predetermined number of data accesses equal to the burst length occurs. A /CAS falling edge received after the last burst address has been generated latches another column address from the address inputs 16 and a new burst sequence begins. Read data is latched and output with each falling edge of /CAS after the first /CAS latency.

For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the /CAS signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is

preferred. Additional input data words for storage at incremented column address locations are latched by /CAS on successive /CAS active transitions. Input data from the input latches 34 is passed along data path 32 to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes are performed without the requirement of additional column addresses being provided on the address lines 16. After the predetermined number of burst writes occur, a subsequent /CAS pulse latches a new beginning column address, and another burst read or write access begins.

The memory device of FIG. 1 may include the option of switching between burst EDO and standard EDO modes of operation. In this case, the write enable signal /WE 36 is used at the row address latch time (/RAS falling, /CAS high) to determine whether memory accesses for that row are burst or page mode cycles. If /WE is low when /RAS falls, burst access cycles are selected. If /WE is high at /RAS falling, standard extended data out (EDO) page mode cycles are selected. Both the burst and EDO page mode cycles allow for increased memory device operating frequencies by not requiring the data output drivers 34 to place the data lines 10 in a high impedance state between data read cycles while /RAS is low. DRAM control circuitry 38, in addition to performing standard DRAM control functions, controls the I/O circuitry 34 and the column address counter/latch 26 in accordance with the mode selected by /WE when /RAS falls. In a burst mode only DRAM, or in a device designed with an alternate method of switching between burst and non-burst access cycles, the state of /WE when /RAS falls may be used to switch between other possible modes of operation such as interleaved versus linear addressing modes.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by /CAS. /WE low at the column address latch time selects a burst write access. /WE high at the column address latch time selects a burst read access. The level of the /WE signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access terminates the burst access, preventing further writes from occurring. A high to low transition on /WE within a burst read access likewise terminates the burst read access and places the data output 10 in a high impedance state. Transitions of the /WE signal may be locked out during critical timing periods within an access cycle in order to reduce the possibility of triggering a false write cycle, and/or to guarantee the completion of a write cycle once it has begun. After the critical timing period the state of /WE determines whether a burst access continues, is initiated, or is terminated. Termination of a burst access places the DRAM in a state to receive another burst access command. Both /RAS and /CAS going high during a burst access also terminates the burst access cycle placing the data drivers in a high impedance output state. Read data may remain valid at the device outputs if /RAS alone goes high while /CAS is active for compatibility with hidden refresh cycles, otherwise /RAS high alone may be used to terminate a burst access. A minimum write enable pulse width is only required when it is desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses. In the case of burst reads, /WE transitions from high to low to terminate a first burst read, and then /WE transitions back high prior to the next falling edge of /CAS in order to specify a new burst read cycle. For burst writes, /WE transitions high to terminate a current burst write access, then back low prior to the next falling edge of /CAS to initiate another burst write access. A minimum /WE pulse width may be specified to guarantee recognition of the /WE pulse despite /WE lockout periods. If no /WE lockout circuit is used, termination of a burst access may be edge sensitive to the /WE signal.

A basic implementation of the device of FIG. 1 may include a fixed burst length of 4, a fixed /CAS latency of 2 and a fixed interleaved sequence of burst addresses. This basic implementation requires very little additional circuitry to the standard EDO page mode DRAM, and may be mass produced to provide the functions of both the standard EDO page mode and burst EDO DRAMs. This device also allows for the output enable pin (/OE) to be grounded for compatibility with many SIMM module designs. When not disabled (tied to ground), /OE is an asynchronous control which prevents data from being driven from the part in a read cycle if it is inactive (high) prior to /CAS falling and remains inactive beyond /CAS rising. If these setup and hold conditions are not met, then the read data may be driven for a portion of the read cycle. It is possible to synchronize the /OE signal with /CAS, however this typically increases the /CAS to data valid delay time and doesn't allow for the last output data to be disabled prior to /RAS high without an additional /CAS low pulse which would otherwise be unnecessary. In a preferred embodiment, if /OE transitions high at any time during a read cycle the outputs remain in a high impedance state until the next falling edge of /CAS despite further transitions of the /OE signal.

Programmability of the burst length, /CAS latency and address sequences may be accomplished through the use of a mode register 40 which latches the state of one or more of the address input signals 16 or data signals 10 upon receipt of a write-/CAS-before-/RAS (WCBR) programming cycle. In such a device, outputs 44 from the mode register control the required circuits on the DRAM. Burst length options of 2, 4, 8 and full page as well as /CAS latencies of 1, 2 and 3 may be provided. Other burst length and latency options may be provided as the operating speeds of the device increase, and computer architectures evolve. The device of FIG. 1 includes programmability of the address sequence by latching the state of the least significant address bit during a WCBR cycle. The burst length and /CAS latency for this particular embodiment are fixed. Other possible alterations in the feature sets of this DRAM include having a fixed burst mode only, selecting between standard fast page mode (non-EDO) and burst mode, and using the output enable pin (/OE) 42 in combination with /RAS to select between modes of operation. Also, a WCBR refresh cycle could be used to select the mode of operation rather than a control signal in combination with /RAS. A more complex memory device may provide additional modes of operation such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of /WE and /OE at /RAS falling time. One mode from a similar set of modes may be selected through the use of a WCBR cycle using multiple address or data lines to encode the desired mode. Alternately, a device with multiple modes of operation may have wire bond locations, or programmable fuses which may be used to program the mode of operation of the device.

A preferred embodiment of a sixteen bit wide burst EDO mode DRAM designed in accordance with the teachings of this invention has two column address strobe input pins /CASH and /CASL. For read cycles only one /CAS signal needs to toggle. The second /CAS may remain high or toggle

with the other /CAS. During burst read cycles, all sixteen data bits will be driven out of part during a read cycle even if one /CAS remains inactive. In a typical system application, a microprocessor reads all data bits on a data bus in each read cycle, but may only write certain bytes of data in a write cycle. Allowing one of the /CAS control signals to remain static during read cycles helps to reduce overall power consumption and noise within the system. For burst write access cycles, each of the /CAS signals (CASH and /CASL) acts as a write enable for an eight bit width of the data. The two /CAS's are combined in an AND function to provide a single internal /CAS which will go low when the first external /CAS falls, and returns high after the last external /CAS goes high. All sixteen data inputs are latched when the first of the /CAS signals transitions low. If only one /CAS signal transitions low, then the eight bits of data associated with the /CAS that remained high are not stored in the memory.

The present invention has been described with reference to several preferred embodiments. Just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including x1, x4, x8 and x16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the memory device of the present invention may take the form of many different memory organizations. It is believed that one who is skilled in the art of integrated circuit memory design can, with the aide of this specification design a variety of memory devices which do not depart from the spirit of this invention. It is therefore believed that detailed descriptions of the various memory device organizations applicable to this invention are not necessary.

It should be noted that the pinout for this new burst EDO memory device may be identical to the pinout for a standard EDO DRAM. The common pinout allows this new device to be used in existing memory designs with minimum design changes. The common pinout also allows for ease of new designs by those of skill in the art who are familiar with the standard EDO DRAM pinout. Variations of the described invention which maintain the standard EDO DRAM pinout include driving the /CAS pin with a system clock signal to synchronize data access of the memory device with the system clock. For this embodiment, it may be desirable to use the first /CAS active edge after /RAS falls to latch the row address, a later edge may be used to latch the first column address of a burst access cycle. After row and column addresses are latched within the device, the address may be incremented internally to provide burst access cycles in synchronization with the system clock. Other pin function alternatives include driving the burst address incrementing signal on the /OE pin since the part does not require a data output disable function on this pin. Other alternate uses of the /OE pin also allow the device to maintain the standard EDO pinout, but provide increased functionality such as burst mode access. The /OE pin may be used to signal the presence of a valid column starting address, or to terminate a burst access. Each of these embodiments provides for a high speed burst access memory device which may be used in current memory systems with a minimum amount of redesign.

FIG. 2 is a timing diagram for performing a burst read followed by a burst write of the device of FIG. 1. In FIG. 2, a row address is latched by the /RAS signal. /WE is low when /RAS falls for an embodiment of the design where the state of the /WE pin is used to specify a burst access cycle at /RAS time, otherwise /WE may be a "don't care" when /RAS falls. Next, /CAS is driven low with /WE high to initiate a burst read access, and the initial column address is latched. The data out signals (DQ's) are not driven in the first /CAS cycle. On the second falling edge of the /CAS signal the internal address generation circuitry provides a column address, and another access of the array begins. The first data out is driven from the device following the second /CAS and a /CAS to data access time (tCAC) delay. Additional burst access cycles continue, for a device with a specified burst length of four, until the fifth falling edge of /CAS which latches a new column address for a new burst read access. /WE falling in the fifth /CAS cycle terminates the burst access, and initializes the device for additional burst accesses. The sixth falling edge of /CAS with /WE low is used to latch a new burst address, latch input data and begin a burst write access of the device. Additional data values are latched on successive /CAS falling edges until /RAS rises to terminate the burst access.

It should be noted from FIG. 2 that for burst read cycles the data remains valid on the device outputs as long as the /OE pin is low, except for brief periods of data transition. Also, since the /WE pin is low prior to or when /CAS falls, the data input/output lines are not driven from the part during write cycles, and the /OE pin is a "don't care". Only the /CAS signal and the data signals toggle at relatively high frequency, and no control signals other than /CAS are required to be in an active or inactive state for one /CAS cycle time or less. This is in contrast to SDRAMs which often require row address strobes, column address strobes, data mask, and read/write control signals to be valid for one clock cycle or less for various device functions. Typical page mode DRAMs also allow for the column address to propagate through to the array to begin a data access prior to /CAS falling. This is done to provide fast data access from /CAS falling if the address has been valid for a sufficient period of time prior to /CAS falling for the data to have been accessed from the array. In these designs an address transition detection circuit is used to restart the memory access if the column address changes prior to /CAS falling. In a preferred embodiment of the design, the address counter is advanced on /CAS rising edges, and the address generated in the counter is then presented to the array on the next /CAS falling edge when the device is in a burst access mode.

FIG. 3 is block level schematic of a data path portion of the device of FIG. 1. In FIG. 3, data written to the memory device is received on data I/O pad 100. The write data is passed through input circuit 102 to a global sense amp 66 over write data lines 103. For this example, the sense amplifier includes an I/O line multiplexer 104 which is used to select a path from local I/O data line pair 106 to one of two pairs of array I/O lines 108 and 110. Write data is driven from write data lines 103 to I/O lines 106 when enabled by a logical combination of the equilibrate signal 70 and the write enable signal 68 from timing circuit 59 and data path control circuit 124 of central logic circuitry 52. In this example array I/O lines 108 are coupled to an adjacent section of the array (not shown). Array I/O lines 110 are true and compliment lines coupled to a local array sense amplifier 112 which is part of array section 64. Column select signal 114 from column driver 115 couples array data I/O lines 110 to a pair of complimentary digit lines 116 inside the local sense amplifier 112. One of the complimentary digit lines is coupled to a memory cell 118 through an access device which is selected by a signal on word line 120 from a row address decoder.

Read data follows the same path from the memory cell to the global sense amp where it is then driven on complimentary data read lines 122 to complimentary data lines 126 under control of data path control logic 124 and timing

circuits 59. Output circuit 128 drives data from the memory device in accordance with the mode of operation (burst EDO mode, EDO mode, fast Page Mode, etc.).

This specific embodiment is not intended to provide an exhaustive description of all forms of the present invention. For example, I/O line multiplexer 104 would not be necessary if there is a global sense amp 67 for each pair of array I/O lines. Alternatively, additional array I/O lines could be multiplexed through the multiplexer 104 to allow for even fewer global sense amplifiers. Another variation is to allow read and write data to share a common path between the global sense amplifiers and the I/O pad. Also, separate input and output data pins can be provided. Numerous additional variations are possible and will be recognized by one of skill in the art.

FIG. 4 is a schematic diagram providing additional detail for portions of the circuitry of FIG. 3. In FIG. 4, /WE and /CAS are logically combined in command latch and control circuit 154. The write command output of circuit 154 is buffered through driver 156 to write command signal line 158. The write command is coupled to a plurality of sense amps 66 through a distributed line resistance represented by resistor 160 over a signal line with distributed capacitive load represented by capacitor 162. Write signal 164 arriving at the sense amplifier will be a delayed version of the output of the write command from the command latch.

Address inputs 170 are coupled to burst address generator 173 which provides a column address 175 to the memory array. The column address and a version of the write command 176 are used to generate an equilibrate signal 182. Equilibration control signal 182 passes through distributed resistance 184, and is loaded by distributed capacitance 186. A delayed version of the equilibrate signal 188 is coupled to the sense amp 66. Local write driver enable circuit 200 allows write cycle data 103 to be driven for a maximum write cycle time by disabling the write data drivers 240–256 during equilibration of the complimentary data I/O lines 106. The data I/O lines are equilibrated when equilibration device 232 couples the true and compliment lines together in response to the equilibration control signal 222.

For a maximized data write cycle time, the write command 164 can remain active throughout a burst write access. In this case, the write drivers are enabled and disabled by the equilibrate signal which will occur at the beginning of each access cycle. For nonburst mode operation, it is beneficial to provide the write command prior to the end of the equilibrate function to allow the write to begin as soon as possible. For these devices, the write will typically end prior to the next /CAS falling edge to allow the device to meet the column address to data valid access time in (TAA). For EDO devices in particular, the page mode cycle time is very short, but the address access time begins while /CAS is high, so the write cycles should end as soon as possible. One way to allow the write cycle to end as soon as possible is to begin it immediately after the equilibrate is complete.

It is important to note that devices 250 and 256 will generally be enabled simultaneously, as will devices 252 and 254. If the enable gate 212 were not locally present, then the write enable signal would need to be delayed from the equilibrate disable time to guarantee that a current path through devices 250, 232 and 256 or devices 252, 232 and 254 does not exist.

FIG. 5 is a schematic diagram of a portion of the column address path of the device of FIG. 1 shown generally as block 26. In FIG. 5 address 16 is coupled to address buffers 305 and 320 which may be located within block 26 of FIG. 1 or at a remote location of the integrated circuit (near address input pads for example). The output of address buffer 305 is coupled to burst address generator 310. Burst address 330 from the burst address generator is coupled to multiplexer 370 through multiplexer 350 and address lines 360. Multiplexer 370 selects either the buffered address 340 from address buffer 320 or the burst address 360 to be latched in latch 380. Latched column address 390 is coupled to a column address buffer 400 which drives the column address to the column address decoder 30 of FIG. 1 to select a column of the memory array. The output of latch 380 is also coupled to an asynchronous address transition detection circuit 420 which generates an equilibration control signal 430 at the beginning of each memory access in response to detected changes in the column address 390. Latched address 390 is also fed back to multiplexer 350. In page mode operation, the multiplexer 370 selects the address from the address buffer 320, and the output of the burst address generator 310 is ignored.

In burst mode, the initial burst address is passed to the latch 370 from the address buffer 340 in response to the first falling /CAS transition. The multiplexer 370 will select the address from address lines 360 for subsequent column addresses within the burst access. The address generator 310 may advance the burst address on rising edges of /CAS. Multiplexer 350 will select the burst address from counter 310 in response to subsequent /CAS falling edges. After an address is latched, the multiplexers 350 and 370 select the address feedback path from 390 through 350, 360 and 370 until the next address is required. This allows the burst address generator to advance on each /CAS rising edge of the burst access.

In an alternate embodiment, the two multiplexers 350 and 370 may be combined into a single multiplexer to select the address from 330, 340 or 390. Another alternative embodiment eliminates the feedback path from address lines 390 to multiplexer 350 while providing additional control of latch 380 to latch the burst address except for a brief period of time after /CAS falls when a new burst address is allowed to pass through.

FIG. 6 is an alternate embodiment of the portion of the address path shown in FIG. 5. In FIG. 6, elements which have common functions with those of FIG. 5 have been given corresponding reference numbers. In FIG. 6, a single set of address buffers 320 are coupled to the address counter 310 and multiplexer 355. The latch 380 of FIG. 5 is no longer present, and multiplexers 350 and 370 of FIG. 5 have been combined into a single multiplexer 355. In page mode operation, the multiplexer 355 selects address lines 340 from the address buffer 320 while /CAS is high. This provides an asynchronous address path from the address buffer to the address transition detection circuit 420 so that the equilibration control signal 430 can be generated for each column address transition while /CAS is high. When /CAS falls, the multiplexer 355 selects feedback path 390 to effectively latch the column address. In burst mode, the initial burst address is passed through the multiplexer 355 in response to the first /CAS falling edge. The initial address is then latched by selecting feedback path 390. The initial address is also loaded into address generator 310 where it may be advanced on rising edges of /CAS. For each subsequent falling edge of /CAS within a burst access, the multiplexer will select lines 330 to provide the next burst address to buffer 400 and address transition detection circuit 420. Then address path 390 is again selected to latch the address which allows the address generator to again advance on the next rising edge of /CAS without disturbing the latched column address 390.

Variations on this embodiment which fall within the scope of the present invention include elimination of the feedback path 390 to the multiplexer in combination with the addition of an address latch between the address buffer 320 and the multiplexer. In this configuration, the latch will store the column address while /CAS is low in page mode, and the address generator will increment in response to falling edges of /CAS eliminating the requirement for a burst address latch or feedback path. The multiplexer may then simply select between a burst address path and a page mode address path. If the address generator is designed to pass the initial burst address from input address 16 through to address lines 330 for each new burst access, then the multiplexer select will only need to be changed when the part is switched between page mode and burst mode.

FIG. 7 is yet another embodiment of the portion of the address path shown in FIG. 5. In FIG. 7, input address 16 feeds page mode and burst mode address generator 315. In page mode operation, the input address is passed through address generator 315 while /CAS is high, and is latched within address generator while /CAS is low. In burst mode, an initial burst address is passed through the address generator in response to the first /CAS low of the burst access. Subsequent burst addresses are generated within the address generator and passed to address lines 390 on successive /CAS falling edges. Address generator 315 may comprise a counter which advances the burst address on rising /CAS edges, and a latch which drives the burst addresses to lines 390 in response to /CAS falling edges.

FIG. 8 is a schematic representation of a data processing apparatus designed in accordance with the present invention. For the purposes of this specification a microprocessor may be, but is not limited to, a central processing unit (CPU), a microprocessor, a microcontroller, a digital signal processor, or an arithmetic processor. In FIG. 8, microprocessor 112 is connected via address lines 114 and control lines 116 to a memory control circuit 118. The memory control circuit provides address and control signals on lines 122 and 120 respectively to a burst access memory device 124. The burst access memory device sends and receives data over data bus 126. Optional data bus buffer 130 between memory data bus 126 and microprocessor data bus 128 allows for amplification of the data signals, and/or synchronization with the microprocessor and memory control signals. A fast static random access memory (SRAM) cache circuit 132 is also optional and provides higher speed access to data stored in the cache from the memory circuit or the microprocessor. Memory control circuit 118 may be incorporated within the microprocessor. The memory control circuit provides the required address strobe signals and read/write control signals required for burst mode access of the memory circuit. By providing burst access of the memory by the processor, a computer with relatively high memory bandwidth can be designed without the requirement of a fast SRAM cache. SRAMs which are fast enough to provide memory access without wait states can significantly add to the cost of a computer. Thus the burst access memory device of the present invention allows for medium to high performance computers to be manufactured at a cost which is significantly less than those manufactured today. Use of the burst access memory device of the present invention in cooperation with a fast SRAM cache allows for an even higher performance computer design by providing fast access to main memory in the event of a cache miss.

In a burst write operation, the processor 112 provides an initial address and a write command to the memory controller. The memory controller provides a row address to the memory with a row address strobe. The memory controller then provides a write command, a column address and a column address strobe to the memory. The memory will equilibrate internal data I/O lines in response to receipt of the write command and column address. During the equilibrate operation, write data and write command signals are passed to global sense amplifiers within the burst access memory device. At the end of the equilibrate operation, write data drivers are enabled, and write data is stored in the memory array. In a preferred embodiment, positive (low to high) transitions of /CAS will cause an internal address counter of the memory device to advance to the next burst address. Negative (high to low) transitions of /CAS will then end the previous write cycle, and pass the burst address to the address transition detection circuit which will generate an equilibrate signal to equilibrate the I/O lines. The negative transition of /CAS will also allow the burst address from the counter to select a column of the array. Once the equilibration is complete, the next write will be performed at the burst address from the counter. In an alternate embodiment, a clock signal is input to a burst access device to control generation of a burst address from the counter (SDRAMs for example have a clock input pin).

In a burst read operation, the processor 112 provides an initial address and a read command to the memory controller. The memory controller provides a row address to the memory with a row address strobe. The memory controller then provides a read command, a column address and a column address strobe to the memory. The memory will equilibrate internal data I/O lines in response to receipt of the read command and column address. At the end of the equilibrate operation, data from the specified column of the array will be amplified and driven on the data I/O lines to the output buffer. In a preferred embodiment, positive (low to high) transitions of /CAS will cause an internal address counter of the memory device to is advance to the next burst address. Negative (high to low) transitions of /CAS will then allow the burst address to pass to the address transition detection circuit which will generate an equilibrate signal to equilibrate the I/O lines. The negative transition of /CAS will also allow the burst address from the counter to select a column of the array. Once the equilibration is complete, the next read will be performed at the burst address from the counter. In an alternate embodiment, a clock signal is input to a burst access device to control generation of the burst address within the memory device.

Memory 124 may also operate in a page mode such as Fast Page Mode or EDO mode. Write commands at memory sense amps are enabled by the equilibrate signal becoming inactive at the sense amp. Using the equilibrate signal at the sense amp to gate the write signal to enable the write drivers eliminates wasted time associated with delaying the write driver enable signal to prevent excessive currents from flowing through the write drivers during the equilibration operation. In page mode, the column address is allowed to flow from the microprocessor asynchronously through to the address transition detection circuit while /CAS is high in order to generate an equilibration signal.

For the purposes of this specification a node may be, but is not limited to, an intersection of conductors, a circuit input or output, or any point along a signal path. For example, the write command may be said to enter the global sense amp at node is 164 and device 250 of FIG. 4 is said to be connected to a power source at node 270. Also, the term signal may refer to but is not limited to information transferred along a conductor, or may refer to the conductor itself. For example, It may be said that the equilibrate signal 188 is coupled to

the sense amp 66. In this context, the term signal represents a physical conductor for carrying the electrical information to equilibrate the data I/O lines, and is not limited to the electrical information itself which is not present when the device is not connected to a power source. The term "coupled" refers to but is not limited to a connection which may be made directly, after buffering, or through another element such as a resistor, capacitor, transistor, or logic device. Typically, a device will be responsive at some time to a signal or another device which is coupled to it.

While the present invention has been described with reference to preferred embodiments, numerous modifications and variations of the invention will be apparent to one of skill in the art without departing from the scope of the invention.

What is claimed is:

1. A circuit comprising:

an address buffer providing a first address;

an input adapted to receive an access cycle strobe signal;

a memory array;

an address generator coupled to said address buffer and to said input, said address generator adapted to provide a series of addresses in response to receipt of the first address and receipt of the access cycle strobe signal; and

an address transition detection circuit coupled to said address buffer and to said address generator, said address transition detection circuit having an output coupled to said memory array, providing a first equilibration signal to said memory array in response to the first address in a first mode of operation, and said address transition detection circuit providing a second equilibration signal to said memory array in response to each subsequent address of the series of addresses in a second mode of operation.

2. The circuit of claim 1 further comprising:

a mode select circuit coupled to said address generator.

3. The circuit of claim 1 wherein said memory array comprises a plurality of dynamic random access memory elements.

4. The circuit of claim 1 further comprising:

a pair of complimentary data lines coupled to said memory array; and

an equilibration circuit coupled to said complimentary data lines, responsive to the first or second equilibration signal to equilibrate said complimentary data lines.

5. A circuit comprising:

a memory array comprising a plurality of rows and a plurality of columns;

a column address generator, operable in a burst mode and a page mode, coupled to said memory array;

a mode select circuit coupled to said column address generator to select the burst mode or the page mode;

an address transition detection circuit coupled to said column address generator;

a pair of complimentary data lines coupled to said memory array; and

an equilibration circuit coupled to said complimentary data lines and to said address transition detection circuit.

6. A circuit comprising:

an address generator responsive to a first polarity of transitions of a control signal to provide a series of addresses;

an address latch responsive to a second polarity of transitions of the control signal to latch each of the series of addresses; and

an address transition detection circuit responsive to the latched addresses, said address transition detection circuit providing an equilibration control signal.

7. A method of operating a memory device having an address generation circuit, comprising steps of:

receiving an address from a source external to the memory device;

latching the address;

generating a next address in the address generation circuit;

latching the next address;

detecting a difference between the address and the next address; and

generating an equilibration signal in response to said step of detecting a difference.

8. A method of supplying data to a microprocessor comprising steps of:

addressing a memory circuit with an address from the microprocessor;

latching the address within the memory circuit;

generating a next address within the memory circuit;

detecting a difference between the address and the next address;

generating an equilibration signal within the memory circuit in response to said step of detecting a difference;

supplying data to the microprocessor from the address of the memory circuit; and

supplying data to the microprocessor from the next address of the memory circuit.

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[54] **DISTRIBUTED WRITE DATA DRIVERS FOR BURST ACCESS MEMORIES**

[75] Inventors: **Todd A. Merritt; Troy A. Manning**, both of Boise, Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **785,867**

[22] Filed: **Jan. 21, 1997**

Related U.S. Application Data

[63] Continuation of Ser. No. 497,354, Jun. 30, 1995, Pat. No. 5,598,376, which is a continuation of Ser. No. 386,894, Feb. 10, 1995, Pat. No. 5,610,864, which is a continuation of Ser. No. 370,761, Dec. 23, 1994, Pat. No. 5,526,320.

[51] **Int. Cl.**[6] **G11C 11/401**; G11C 8/00

[52] **U.S. Cl.** **365/189.05**; 365/193; 365/233; 365/202; 365/204

[58] **Field of Search** 365/189.01, 189.05, 365/193, 233, 230.01, 202, 204

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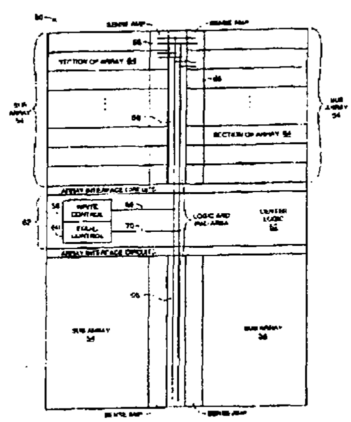
Primary Examiner—Viet Q. Nguyen

Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

An integrated circuit memory device is designed to perform high speed data write cycles. An address strobe signal is used to latch a first address. During a burst access cycle the address is incremented internal to the device with additional address strobe transitions. A new memory address is only required at the beginning of each burst access. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at the device cycle frequency. A transition of the Read/Write control line during a burst access is used to terminate the burst access and initialize the device for another burst access. Write cycle times are maximized to allow for increases in burst mode operating frequencies. Local logic gates near array sense amplifiers are used to control write data drivers to provide for maximum write times without crossing current during input/output line equilibration periods. By gating global write enable signals with global equilibrate signals locally at data sense amp locations, local write cycle control signals are provided which are valid for essentially the entire cycle time minus an I/O line equilibration period in burst access memory devices. For nonburst mode memory devices such as EDO and Fast Page Mode, the write function may begin immediately following the end of the equilibration cycle to provide a maximum write time without interfering with the address setup time of the next access cycle.

5 Claims, 6 Drawing Sheets



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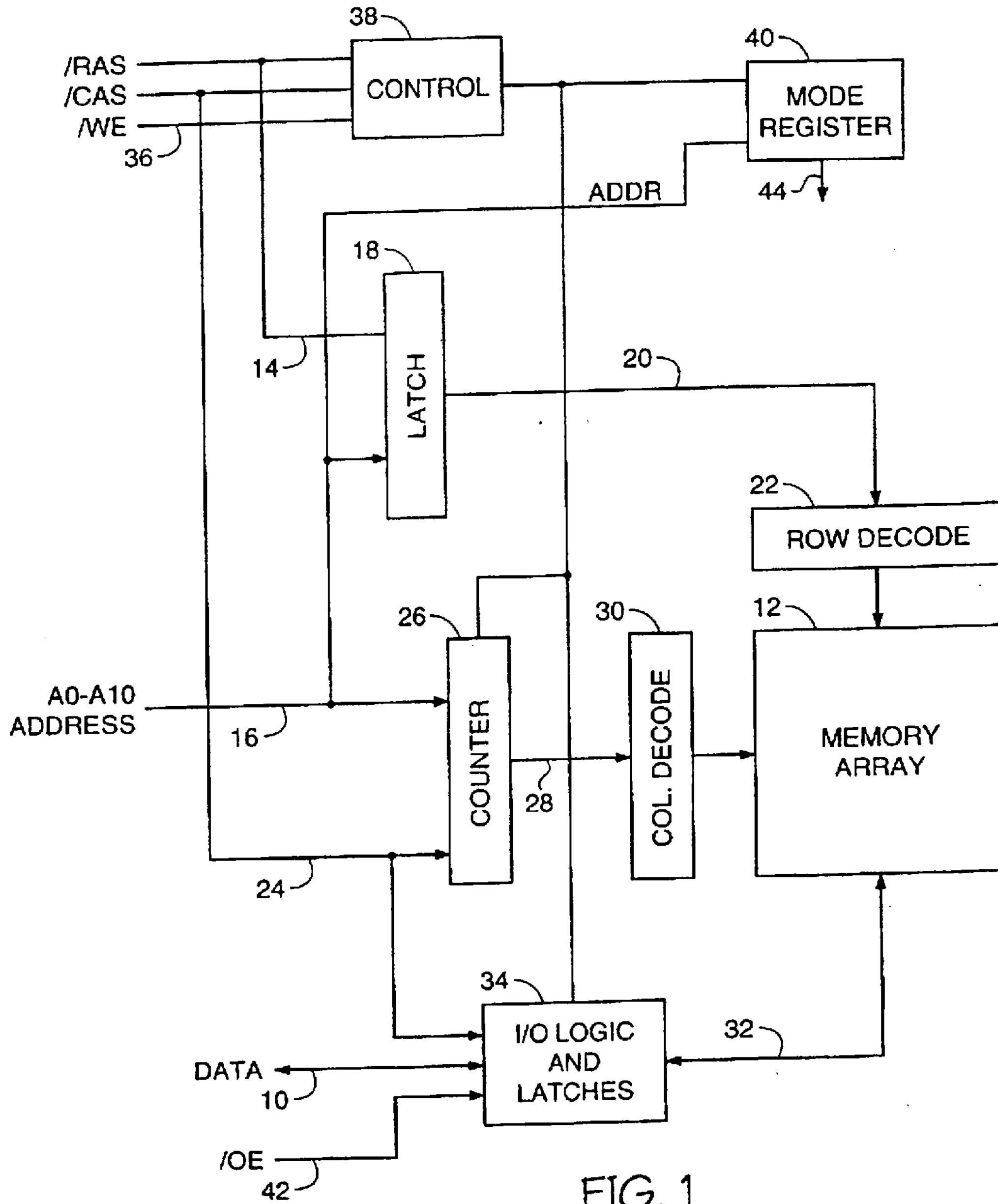

FIG. 1

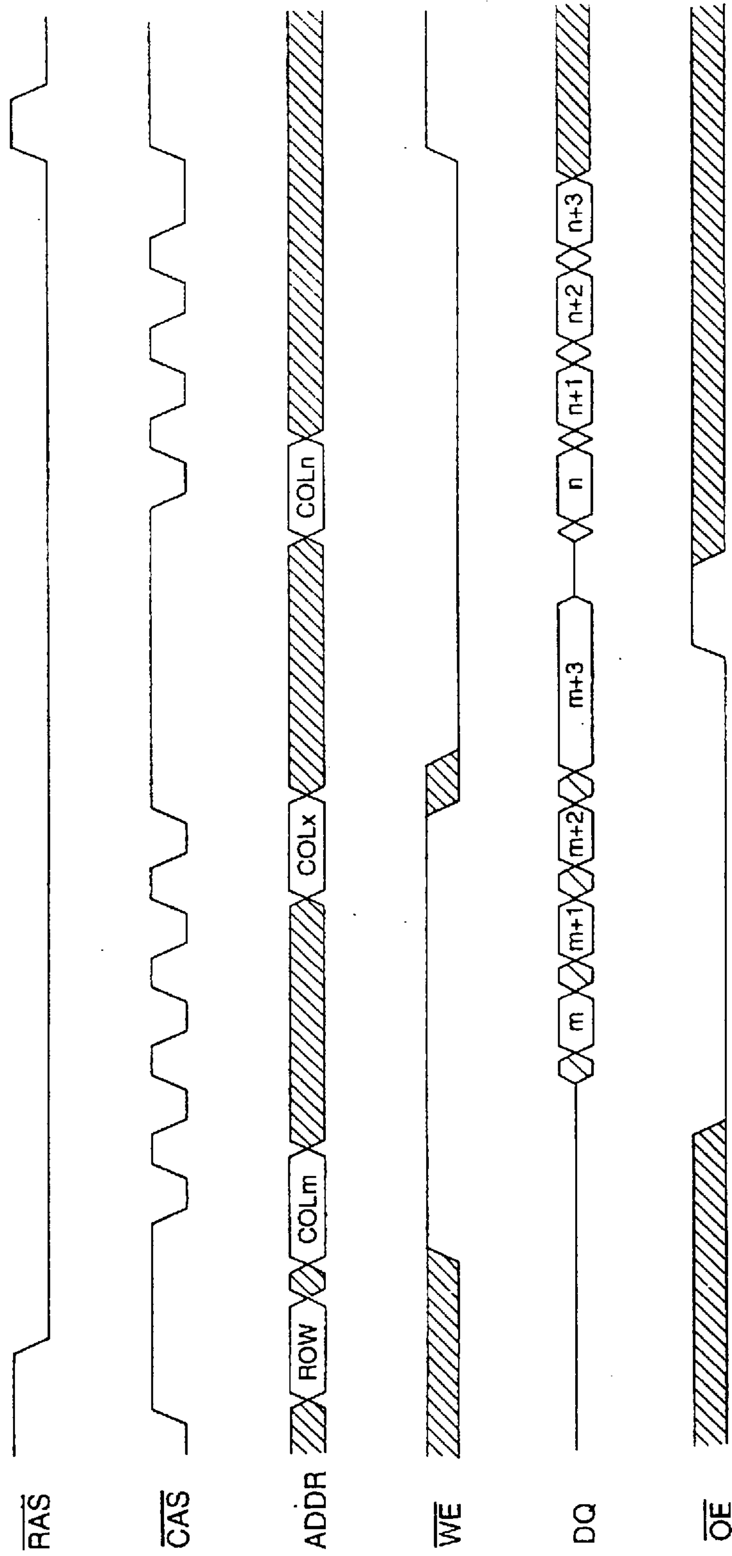

FIG. 2

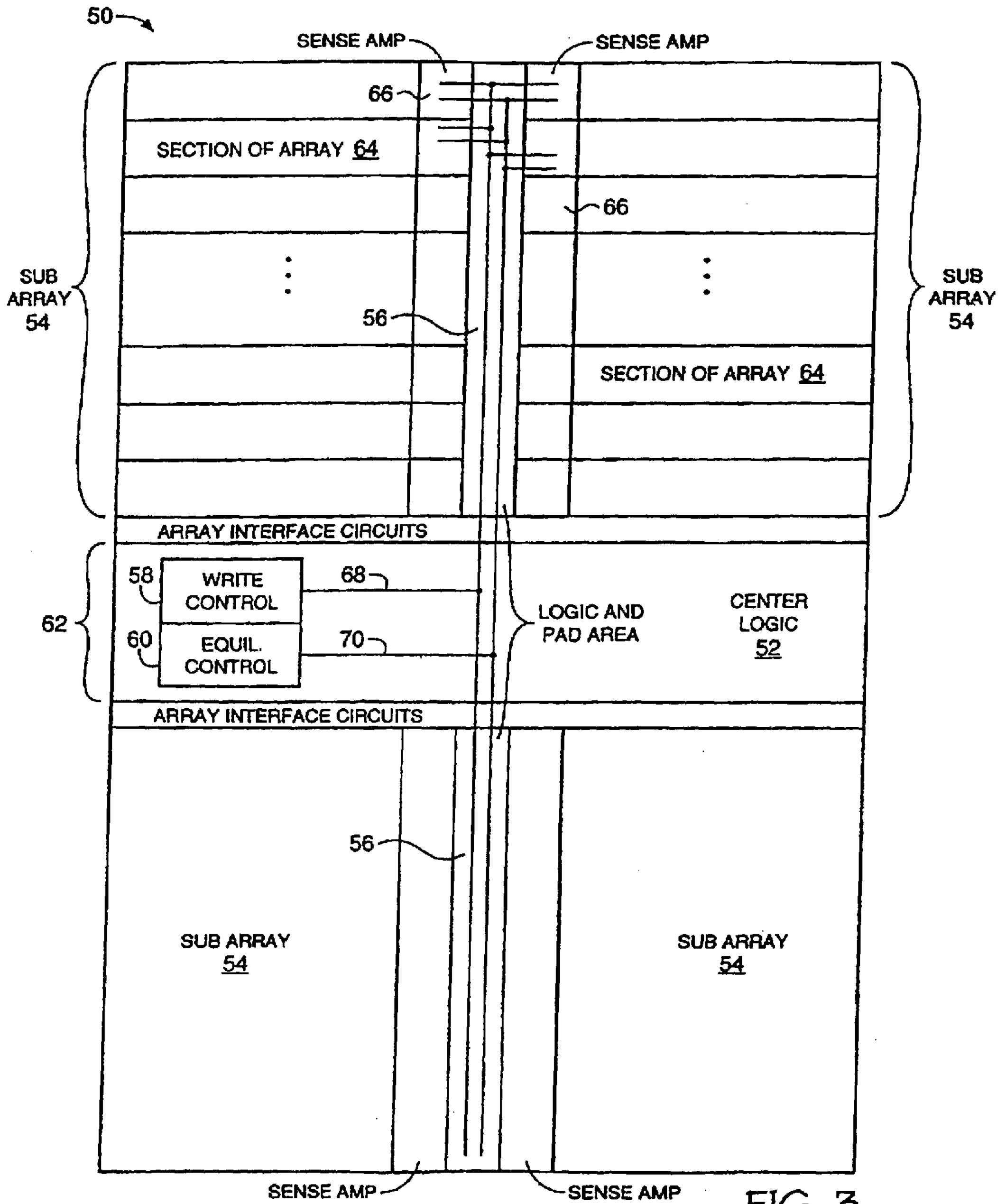

FIG. 3

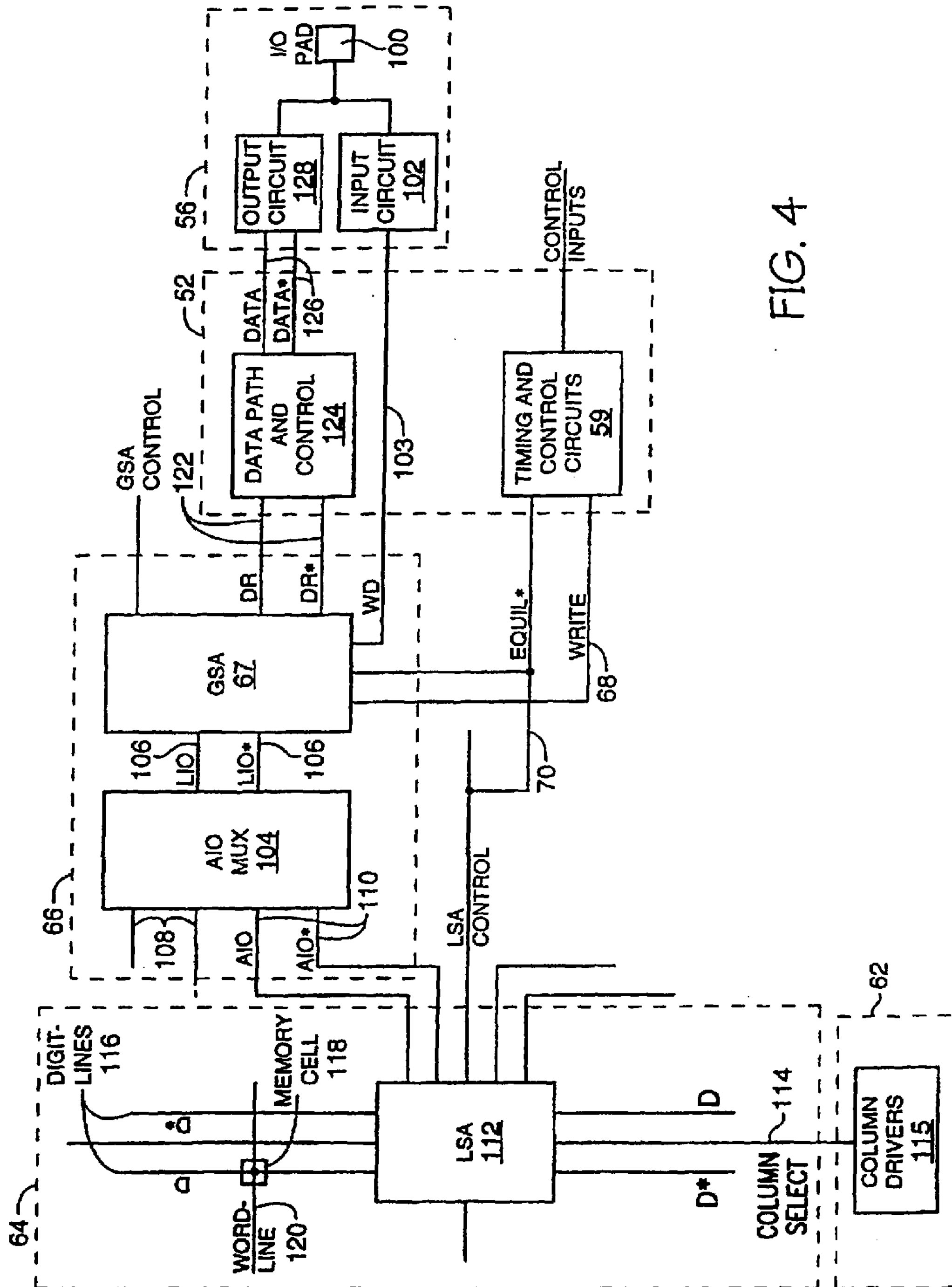

FIG. 4

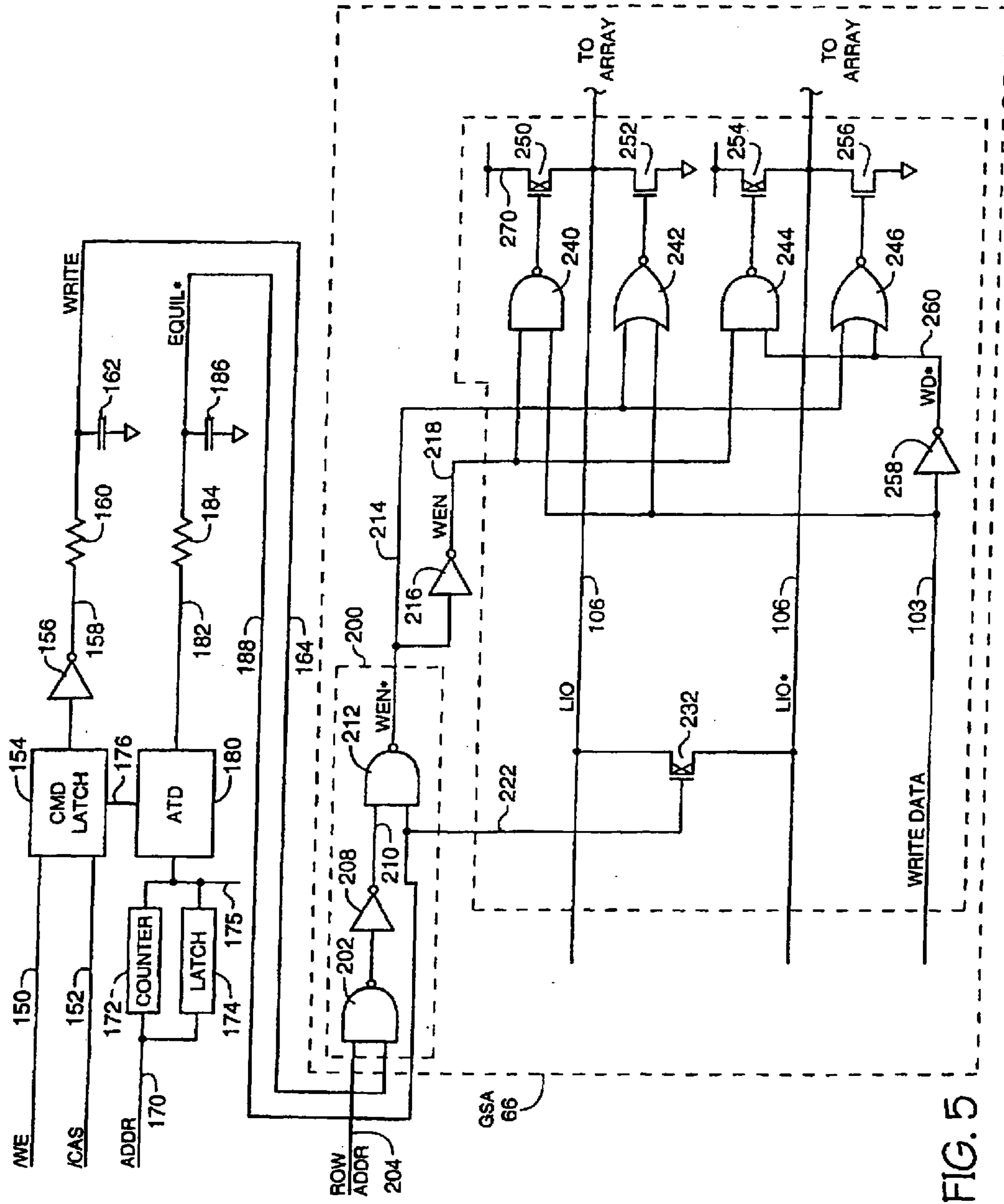

FIG. 5

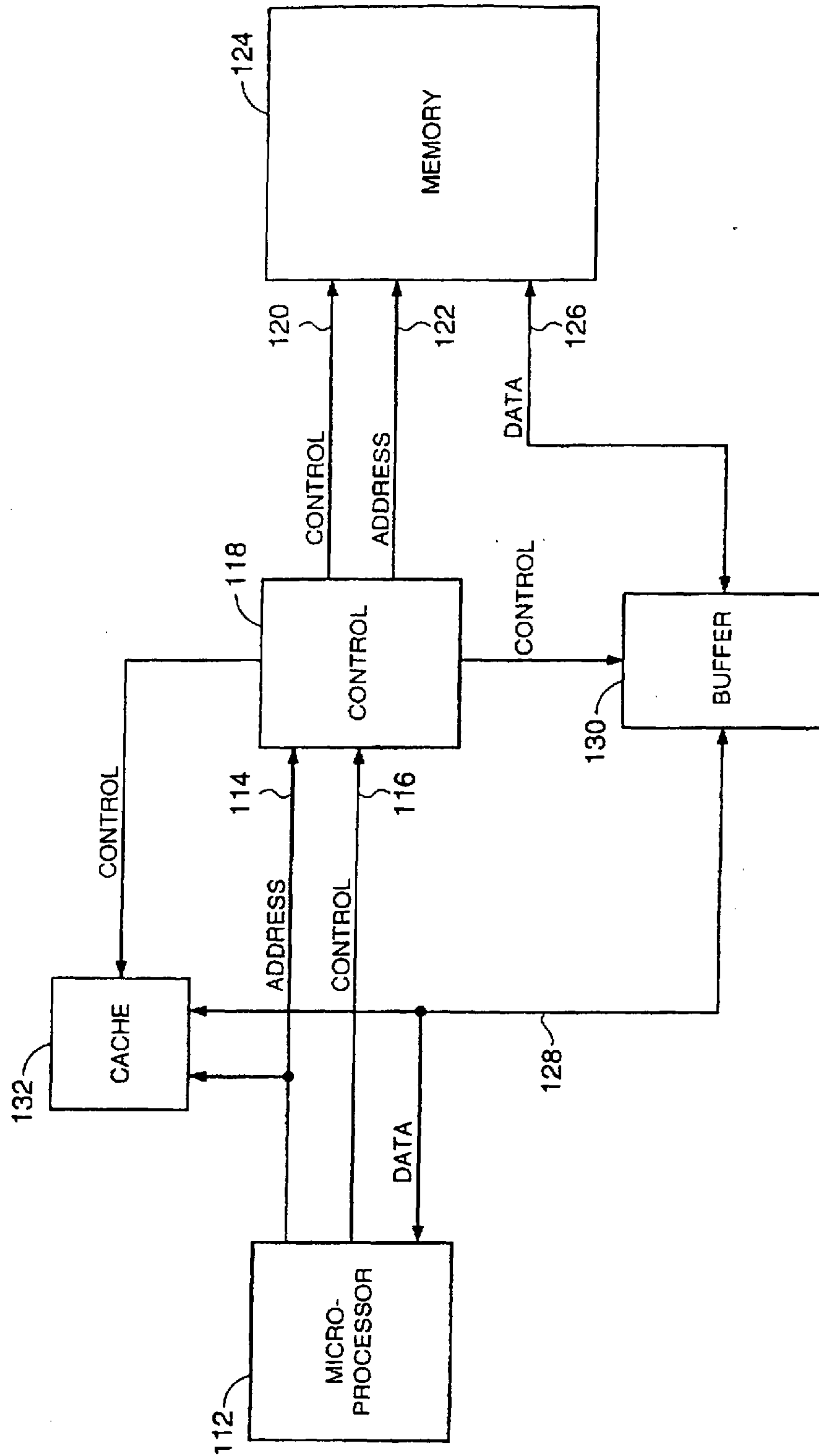

FIG. 6

DISTRIBUTED WRITE DATA DRIVERS FOR BURST ACCESS MEMORIES

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of application Ser. No. 08/497,354, filed Jun. 30, 1995, issued as U.S. Pat. No. 5,598,376 on Jan. 28, 1997, which is a continuation in part of application Ser. No. 08/386,894 filed Feb. 10, 1995, now U.S. Pat. No. 5,610,864, which is a continuation in part of application Ser. No. 08/370,761 filed Dec. 23, 1994; now U.S. Pat. No. 5,526,320.

FIELD OF THE INVENTION

This invention relates to memory device architectures designed to provide high density data storage with high speed read and write access cycles. This invention relates more specifically to circuits and methods for controlling memory write cycles.

BACKGROUND OF THE INVENTION

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead, data is held valid after /CAS goes high until sometime after the next /CAS low pulse occurs, or until /RAS or the output enable (/OE) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can be a complex function of when the column address inputs are valid, when /CAS falls, the state of /OE and when /CAS rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially /CAS) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM manufacturers.

Methods to shorten memory access cycles tend to require additional circuitry, additional control pins and nonstandard device pinouts. The proposed industry standard synchronous DRAM (SDRAM)for example has an additional pin for receiving a system clock signal. Since the system clock is connected to each device in a memory system, it is highly loaded, and it is always toggling circuitry in every device. SDRAMs also have a clock enable pin, a chip select pin and a data mask pin. Other signals which appear to be similar in name to those found on standard DRAMs have dramatically different functionality on a SDRAM. The addition of several control pins has required a deviation in device pinout from standard DRAMs which further complicates design efforts to utilize these new devices. Significant amounts of additional circuitry are required in the SDRAM devices which in turn result in higher device manufacturing costs.

It is desirable to design and manufacture a memory device having a standard DRAM pinout and a burst mode of operation where multiple data values can be sequentially written to or read from the device in response to a single address location and multiple access strobes. It is also desirable that this new memory device operate at higher frequencies than standard DRAMs.

There is a problem in performing write cycles at high frequencies. In standard Fast Page Mode and EDO mode DRAM devices, write cycles are performed in response to both /CAS and /WE being low after /RAS is low. If an address change occurs at approximately the same time that /CAS falls, then an additional delay is required to equilibrate input/output lines and to fire a new column prior to beginning the write cycle. Data to be written is latched, and the write cycle begins when the latter of /CAS and /WE goes low provided that the equilibrate is complete. Generally, the write time can be considered to be the period of time that /WE and /CAS are simultaneously low. However, in order to allow for maximum page mode operating frequencies, the write cycle is often timed out so that it can continue for a short period of time after /CAS or /WE goes high especially for "late write" cycles. Maintaining the write cycle throughout the time-out period eases the timing specifications for /CAS and /WE that the device user must meet, and reduces susceptibility to glitches on the control lines during a write cycle. The write cycle is terminated after the time out period, and if /WE is high a read access begins based on the address present on the address input lines. The read access will typically begin prior to the next /CAS falling edge so that the column address to data valid specification can be met (tAA). In order to begin the read cycle as soon as possible, it is desirable to minimize the write cycle time while guaranteeing completion of the write cycle. Minimizing the write cycle duration in turn minimizes the margin to some device operating parameters despite the speed at which the device is actually used. Circuits to model the time required to complete the write cycle typically provide an estimate of the time required to write an average memory cell. While it is desirable to minimize the write cycle time, it is also necessary to guarantee that enough time is allowed for the write to complete, so extra delay is added making the write cycle slightly longer than required.

Another aspect of controlling the write cycle timing includes delaying the write enable or write enables to guarantee that the write data drivers are not enabled prior to the completion of the equilibrate function. Equalization of internal data I/O lines is performed in response to column address transitions in preparation for reading or writing data from another memory cell, and also in response to receipt of a write command to reduce the maximum signal transition on the data lines once the write drivers are enabled. If the data lines are each equalized to one half of Vcc for example, then the write data drivers will only need to drive one line from half Vcc to ground, and the other from half Vcc to Vcc. Otherwise, if the write data is not equal to the data previously on the I/O lines, the write data drivers will need to drive both true and compliment I/0 lines a full Vcc swing for each data bit being written. Equalization of the data I/0 lines reduces the maximum write cycle time by eliminating the worst case signal swing conditions. A simple method of equilibrating the I/0 lines is to: disable I/O line drivers; isolate the I/O lines from the digit lines; and couple complimentary I/O lines together. When a true I/O line is coupled to a complimentary I/O line, a logic high will be coupled to a logic low and each line will equalize to a potential approximately half way between a high and a low. It is important to disable the I/O line drivers during equilibration to prevent a true logic driver from being coupled to a complimentary logic driver which will draw excessive current from the logic high source to the logic low source.

Whether /CAS goes low last (early write) or /WE goes low last (late write), the column address will be valid at or before the write command is received. Hence, a delay from

receipt of the write command which is greater than the equilibrate time will guarantee that an equilibrate due to a column address change is complete prior to the enabling the write drivers. If an equilibrate of internal data I/O lines is performed in response to receipt of each write command, a simple delay of the write enables will allow for the equilibrate to complete prior to enabling the write drivers. The delay value for the write cycle to write driver enable delay must account for the worst case signal delays from the equilibrate and write driver enable signal sources to the furthest data I/O line equilibrate devices and write data drivers. Since the equilibrate and write driver enable signal sources are located in a main logic area, a considerable signal propagation delay will result from the transmission of these signals across the chip to the furthest I/O line pair. Timing delays due to routing differences in the two signal paths can be very difficult to accurately model and predict. To overcome these difficulties, extra delay is added for timing margin. Unfortunately, this prevents the write drivers from being enabled as soon as the equilibrate function is complete.

Throughout the memory device product lifetime, manufacturing process advances and circuit enhancements often allow for increases in device operating frequencies. The write cycle timing circuits may need to be adjusted to shorten the minimum write cycle times to match these performance improvements. Adjustments may include shortening the equilibrate time, shortening the write cycle to write driver enable time and shortening the write cycle hold time. Fine tuning of these timing circuits is time consuming and costly. If the write cycles are too short, the device may fail under some or all operating conditions. If the write cycles are too long, the device may not be able to achieve the higher operating frequencies that are more profitable for the device manufacturers. Finally, if the equilibrate is not complete prior to enabling the write drivers, then excessive current may flow through the write drivers from Vcc to ground.

With the increased operating frequencies of burst access memory devices a new method of generating the write cycle timing is desired which will allow for maximum write cycle times despite the operating frequency of the device.

SUMMARY OF THE INVENTION

An integrated circuit memory device with a standard DRAM pinout is designed for high speed data access and for compatibility with existing memory systems. A high speed burst mode of operation is provided where multiple sequential accesses occur following a single column address, and read data is output relative to the /CAS control signal. In the burst mode of operation the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at high speeds. Only one control line per memory chip (/CAS) must toggle at the operating frequency in order to clock the internal address counter and the data input/output latches. The load on each /CAS is typically less than the load on the other control signals (/RAS, /WE and /OE) since each /CAS typically controls only a byte width of the data bus.

A new write cycle timing method and circuit allow for maximized write cycle timing at all operating frequencies to provide maximum write cycle timing margins. Write control is maintained throughout a write cycle such that the write operation time approaches the write cycle time. The write function is only halted between write cycles for a period of time required to select a new column of the array and to equilibrate I/O lines in the array. To maximize write cycle times, a logic device is located near the sense amplifiers of the device to control the write function directly with the use of the I/O line equilibrate signal. It is important to disable the write drivers during the equilibrate time to prevent current flow through the true and compliment data drivers while the I/O lines are coupled together. The local write enable circuit allows the write cycle time to be essentially equal to the access cycle time minus the I/O line equilibrate time in burst access memory devices. For nonburst mode memory devices such as EDO and Fast Page Mode, the write function may begin immediately following the end of the equilibration cycle to provide a maximum write time without interfering with the address setup time of the next cycle.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention as well as objects and advantages are best understood by reference to the appended claims, detailed description of particular embodiments and accompanying drawings where:

FIG. 1 is an electrical schematic diagram of a memory device in accordance with one embodiment of the invention;

FIG. 2 is a timing diagram for a method of accessing the device of FIG. 1;

FIG. 3 is a top view of a general device layout for a device designed in accordance with the teachings of the present invention;

FIG. 4 is block level schematic of a data path portion of the device of FIG. 3;

FIG. 5 is a more detailed schematic of a portion of the circuitry of FIG. 4; and

FIG. 6 is a schematic diagram of a computer system designed in accordance with the teachings of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a schematic representation of a sixteen megabit device designed in accordance with the present invention. The device is organized as a 2 Meg×8 burst EDO DRAM having an eight bit data input/output path **10** providing data storage for 2,097,152 bytes of information in the memory array **12**. The device of FIG. 1 has an industry standard pinout for eight bit wide EDO DRAMs. An active-low row address strobe (/RAS) signal **14** is used to latch a first portion of a multiplexed memory address, from address inputs A0 through A10 **16**, in latch **18**. The latched row address **20** is decoded in row decoder **22**. The decoded row address is used to select a row of the memory array **12**. A column address strobe (/CAS) signal **24** is used to latch a second portion of a memory address from address inputs **16** into column address counter **26**. The latched column address **28** is decoded in column address decoder **30**. The decoded column address is used to select a column of the memory array **12**.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path **32** to output latches **34**. Data **10** driven from the burst EDO DRAM may be latched external to the device in synchronization with /CAS after a predetermined number of /CAS cycle delays (latency). For a two cycle latency design, the first /CAS falling edge is used

to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second /CAS falling edge, and remains valid through the third /CAS falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers 34 continue to drive the data lines without tri-stating the data outputs during /CAS high intervals dependent on the state of the output enable and write enable (/OE and /WE) control lines, thus allowing additional time for the system to latch the output data. Once a row and a column address are selected, additional transitions of the /CAS signal are used to advance the column address within the column address counter in a predetermined sequence. The time at which data becomes valid at the outputs of the burst EDO DRAM is dependent only on the timing of the /CAS signal provided that /OE is maintained low, and /WE remains high. The output data signal levels may be driven in accordance with, but are not limited to, CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. The column address may be advanced with each /CAS transition, each pulse, or multiple of /CAS pulses in the event that more than one data word is read from the array with each column address. When the address is advanced with each transition of the /CAS signal, data is also driven from the part after each transition following the device latency which is then referenced to each edge of the /CAS signal. This allows for a burst access cycle where the highest switching control line (/CAS) toggles only once (high to low or low to high) for each memory cycle. This is in contrast to standard DRAMs which require /CAS to go low and then high for each cycle, and synchronous DRAMs which require a full clock cycle (high and low transitions) for each memory cycle. For maximum compatibility with existing EDO DRAM devices, the invention will be further described in reference to a device designed to initiate access cycles on falling edges of the /CAS signal. For designs where falling edges of the /CAS signal initiate an access cycle, the falling edge may be said to be the active transition of the /CAS signal.

It may be desirable to latch and increment the column address after the first /CAS falling edge in order to apply both the latched and incremented addresses to the array at the earliest opportunity in an access cycle. For example, a device may be designed to access two data words per cycle (prefetch architecture). The memory array for a prefetch architecture device may be split into odd and even array halves. The column address least significant bit is used to select between odd and even halves while the other column address bits select a column within each of the array halves. In an interleaved access mode with column address 1, data from columns 0 and 1 are read and the data from column 1 is output followed by the data from column 0 in accordance with standard interleaved addressing as described in SDRAM specifications. In a linear access mode column address 1 is applied to the odd array half, and incremented to address 2 for accessing the even array half to fulfill the two word access. One method of implementing this type of device architecture is to provide a column address incrementing circuit between the column address counter and the even array half. The incrementing circuit increments the column address only if the initial column address in a burst access cycle is odd, and the address mode is linear. Otherwise the incrementing circuit passes the column address unaltered. For a design using a prefetch of two data accesses per cycle, the column address is advanced once for every two active edges of the /CAS signal. In a write cycle, multiple data words may be temporarily stored as they are input to the device. The actual write of data to the memory cells occurs after the last input data is latched, and may extend slightly into the next memory cycle as long as it ends prior to the next column being activated. Prefetch architectures where more than two data words are accessed are also possible.

Other memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete. In a pipelined architecture the overall throughput of the memory approaches one access per cycle, but the data out of the memory is offset by a number of cycles equal to the pipeline length and/or the desired latency from /CAS.

In the burst access memory device, each new column address from the column address counter is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16. This burst sequence of data continues for each /CAS falling edge until a predetermined number of data accesses equal to the burst length occurs. A /CAS falling edge received after the last burst address has been generated latches another column address from the address inputs 16 and a new burst sequence begins. Read data is latched and output with each falling edge of /CAS after the first /CAS latency.

For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the /CAS signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is preferred. Additional input data words for storage at incremented column address locations are latched by /CAS on successive /CAS active transitions. Input data from the input latches 34 is passed along data path 32 to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes are performed without the requirement of additional column addresses being provided on the address lines 16. After the predetermined number of burst writes occur, a subsequent /CAS pulse latches a new beginning column address, and another burst read or write access begins.

The memory device of FIG. 1 may include the option of switching between burst EDO and standard EDO modes of operation. In this case, the write enable signal /WE 36 is used at the row address latch time (/RAS falling, /CAS high) to determine whether memory accesses for that row are burst or page mode cycles. If /WE is low when /RAS falls, burst access cycles are selected. If /WE is high at /RAS falling, standard extended data out (EDO) page mode cycles are selected. Both the burst and EDO page mode cycles allow for increased memory device operating frequencies by not requiring the data output drivers 34 to place the data lines 10 in a high impedance state between data read cycles while /RAS is low. DRAM control circuitry 38, in addition to performing standard DRAM control functions, controls the I/O circuitry 34 and the column address counter/latch 26 in accordance with the mode selected by /WE when /RAS falls. In a burst mode only DRAM, or in a device designed with an alternate method of switching between burst and non-burst access cycles, the state of /WE when /RAS falls may be used to switch between other possible modes of operation such as interleaved versus linear addressing modes.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by /CAS. /WE low at the column address latch time selects a burst write access. /WE high at the column address latch time selects a burst read access. The level of the /WE signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access terminates the burst access, preventing further writes from occurring. A high to low transition on /WE within a burst read access likewise terminates the burst read access and places the data output 10 in a high impedance state. Transitions of the /WE signal may be locked out during critical timing periods within an access cycle in order to reduce the possibility of triggering a false write cycle, and/or to guarantee the completion of a write cycle once it has begun. After the critical timing period the state of /WE determines whether a burst access continues, is initiated, or is terminated. Termination of a burst access places the DRAM in a state to receive another burst access command. Both /RAS and /CAS going high during a burst access also terminates the burst access cycle placing the data drivers in a high impedance output state. Read data may remain valid at the device outputs if /RAS alone goes high while /CAS is active for compatibility with hidden refresh cycles, otherwise /RAS high alone may be used to terminate a burst access. A minimum write enable pulse width is only required when it is desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses. In the case of burst reads, /WE transitions from high to low to terminate a first burst read, and then /WE transitions back high prior to the next falling edge of /CAS in order to specify a new burst read cycle. For burst writes, /WE transitions high to terminate a current burst write access, then back low prior to the next falling edge of /CAS to initiate another burst write access. A minimum /WE pulse width may be specified to guarantee recognition of the /WE pulse despite /WE lockout periods. If no /WE lockout circuit is used, termination of a burst access may be edge sensitive to the /WE signal.

A basic implementation of the device of FIG. 1 may include a fixed burst length of 4, a fixed /CAS latency of 2 and a fixed interleaved sequence of burst addresses. This basic implementation requires very little additional circuitry to the standard EDO page mode DRAM, and may be mass produced to provide the functions of both the standard EDO page mode and burst EDO DRAMs. This device also allows for the output enable pin (/OE) to be grounded for compatibility with many SIMM module designs. When not disabled (tied to ground), /OE is an asynchronous control which prevents data from being driven from the part in a read cycle if it is inactive (high) prior to /CAS falling and remains inactive beyond /CAS rising. If these setup and hold conditions are not met, then the read data may be driven for a portion of the read cycle. It is possible to synchronize the /OE signal with /CAS, however this typically increases the /CAS to data valid delay time and doesn't allow for the last output data to be disabled prior to /RAS high without an additional /CAS low pulse which would otherwise be unnecessary. In a preferred embodiment, if /OE transitions high at any time during a read cycle the outputs remain in a high impedance state until the next falling edge of /CAS despite further transitions of the /OE signal.

Programmability of the burst length, /CAS latency and address sequences may be accomplished through the use of a mode register 40 which latches the state of one or more of the address input signals 16 or data signals 10 upon receipt of a write-/CAS-before-/RAS (WCBR) programming cycle. In such a device, outputs 44 from the mode register control the required circuits on the DRAM. Burst length options of 2, 4, 8 and full page as well as /CAS latencies of 1, 2 and 3 may be provided. Other burst length and latency options may be provided as the operating speeds of the device increase, and computer architectures evolve. The device of FIG. 1 includes programmability of the address sequence by latching the state of the least significant address bit during a WCBR cycle. The burst length and /CAS latency for this particular embodiment are fixed. Other possible alterations in the feature sets of this DRAM include having a fixed burst mode only, selecting between standard fast page mode (non-EDO) and burst mode, and using the output enable pin (/OE) 42 in combination with /RAS to select between modes of operation. Also, a WCBR refresh cycle could be used to select the mode of operation rather than a control signal in combination with /RAS. A more complex memory device may provide additional modes of operation such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of /WE and /OE at /RAS falling time. One mode from a similar set of modes may be selected through the use of a WCBR cycle using multiple address or data lines to encode the desired mode. Alternately, a device with multiple modes of operation may have wire bond locations, or programmable fuses which may be used to program the mode of operation of the device.

A preferred embodiment of a sixteen bit wide burst EDO mode DRAM designed in accordance with the teachings of this invention has two column address strobe input pins /CASH and /CASL. For read cycles only one /CAS signal needs to toggle. The second /CAS may remain high or toggle with the other /CAS. During burst read cycles, all sixteen data bits will be driven out of part during a read cycle even if one /CAS remains inactive. In a typical system application, a microprocessor reads all data bits on a data bus in each read cycle, but may only write certain bytes of data in a write cycle. Allowing one of the /CAS control signals to remain static during read cycles helps to reduce overall power consumption and noise within the system. For burst write access cycles, each of the /CAS signals (CASH and /CASL) acts as a write enable for an eight bit width of the data. The two /CAS's are combined in an AND function to provide a single internal /CAS which will go low when the first external /CAS falls, and returns high after the last external /CAS goes high. All sixteen data inputs are latched when the first of the /CAS signals transitions low. If only one /CAS signal transitions low, then the eight bits of data associated with the /CAS that remained high are not stored in the memory.

The present invention has been described with reference to several preferred embodiments. Just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including x1, x4, x8 and x16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the memory device of the present invention may take the form of many different memory organizations. It is believed that one who is skilled in the art of integrated circuit memory design can, with the aide of this specification design a variety of memory devices which do not depart from the spirit of this invention. It is therefore believed that detailed descriptions of the various memory device organizations applicable to this invention are not necessary.

It should be noted that the pinout for this new burst EDO memory device may be identical to the pinout for a standard

EDO DRAM. The common pinout allows this new device to be used in existing memory designs with minimum design changes. The common pinout also allows for ease of new designs by those of skill in the art who are familiar with the standard EDO DRAM pinout. Variations of the described invention which maintain the standard EDO DRAM pinout include driving the /CAS pin with a system clock signal to synchronize data access of the memory device with the system clock. For this embodiment, it may be desirable to use the first /CAS active edge after /RAS falls to latch the row address, a later edge may be used to latch the first column address of a burst access cycle. After row and column addresses are latched within the device, the address may be incremented internally to provide burst access cycles in synchronization with the system clock. Other pin function alternatives include driving the burst address incrementing signal on the /OE pin since the part does not require a data output disable function on this pin. Other alternate uses of the /OE pin also allow the device to maintain the standard EDO pinout, but provide increased functionality such as burst mode access. The /OE pin may be used to signal the presence of a valid column starting address, or to terminate a burst access. Each of these embodiments provides for a high speed burst access memory device which may be used in current memory systems with a minimum amount of redesign.

FIG. 2 is a timing diagram for performing a burst read followed by a burst write of the device of FIG. 1. In FIG. 2, a row address is latched by the /RAS signal. /WE is low when /RAS falls for an embodiment of the design where the state of the /WE pin is used to specify a burst access cycle at /RAS time, otherwise /WE may be a "don't care" at /RAS falls. Next, /CAS is driven low with /WE high to initiate a burst read access, and the initial column address is latched. The data out signals (DQ's) are not driven in the first /CAS cycle. On the second falling edge of the /CAS signal the internal address generation circuitry provides a column address, and another access of the array begins. The first data out is driven from the device following the second /CAS and a /CAS to data access time (tCAC) delay. Additional burst access cycles continue, for a device with a specified burst length of four, until the fifth falling edge of /CAS which latches a new column address for a new burst read access. /WE falling in the fifth /CAS cycle terminates the burst access, and initializes the device for additional burst accesses. The sixth falling edge of /CAS with /WE low is used to latch a new burst address, latch input data and begin a burst write access of the device. Additional data values are latched on successive /CAS falling edges until /RAS rises to terminate the burst access.

It should be noted from FIG. 2 that for burst read cycles the data remains valid on the device outputs as long as the /OE pin is low, except for brief periods of data transition. Also, since the /WE pin is low prior to or when /CAS falls, the data input/output lines are not driven from the part during write cycles, and the /OE pin is a "don't care". Only the /CAS signal and the data signals toggle at relatively high frequency, and no control signals other than /CAS are required to be in an active or inactive state for one /CAS cycle time or less. This is in contrast to SDRAMs which often require row address strobes, column address strobes, data mask, and read/write control signals to be valid for one clock cycle or less for various device functions. Typical DRAMs also allow for the column address to propagate through to the array to begin a data access prior to /CAS falling. This is done to provide fast data access from /CAS falling if the address has been valid for a sufficient period of time prior to /CAS falling for the data to have been accessed from the array. In these designs an address transition detection circuit is used to restart the memory access if the column address changes prior to /CAS falling. This method actually requires additional time for performing a memory access since it must allow for a period of time at the beginning of each memory cycle after the last address transition to prepare for a new column address by equilibrating internal I/O lines, deselecting all columns and selecting a new column. Changes in the column address just prior to /CAS falling may increase the access time by approximately five nanoseconds. An embodiment of the present invention will not allow the column address to propagate through to the array until after /CAS has fallen. This eliminates the need for address transition detection circuitry, and allows for a fixed array access time relative to /CAS. In a preferred embodiment of the design, the address counter is advanced on /CAS rising edges, and the address generated in the counter is then presented to the array on the next /CAS falling edge in a burst access.

FIG. 3 shows a topographic layout view of one embodiment of a memory device designed in accordance with the teachings of the present invention. Memory device **50** has a central logic region **52**, array regions **54**, and logic and pads regions **56**. Circuitry in region **52** includes write control circuitry **58** and equilibration control circuitry **60** in addition to other memory timing control circuits. Circuitry in array interface regions **62** includes array address drivers. Circuitry in the logic and pads areas includes data buffers and I/O pads. I/O pads running through the center of a chip in this fashion is indicative of a Leads Over Chip (LOC) packaging configuration. The layout shown is for example only. Other possible layouts include but are not limited to: a) layouts with pads and central logic circuits located on the sides and/or ends of the memory device with array circuitry occupying the center of the device; b) central logic circuits located centrally along one axis of the device with pads on the sides or ends of the device; or c) central logic in the center of the chip with pads running through the chip and on the sides or ends of the chip for a hybrid of LOC and conventional bonding.

Array regions **54** are broken into **16** subarray regions **64** each of which has an associated data sense amplifier **66** located along one edge of the array. Write enable signal **68** and I/O line equilibrate signal **70** are routed to each data sense amplifier.

FIG. 4 is block level schematic of a data path portion of the device of FIG. 3. Elements in FIG. 4 that have the same or similar function as numbered elements in FIG. 3 are given the same reference numerals. In FIG. 4, data written to the memory device is received on data I/O pad **100**. The write data is passed through input circuit **102** to a global sense amp **66** over write data lines **103**. For this example, the sense amplifier includes an I/O line multiplexer **104** which is used to select a path from local I/O data line pair **106** to one of two pairs of array I/O lines **108** and **110**. Write data is driven from write data lines **103** to I/O lines **106** when enabled by a logical combination of the equilibrate signal **70** and the write enable signal **68** from timing circuit **59** and data path control circuit **124** of central logic circuitry **52**. In this example array I/O lines **108** are coupled to an adjacent section of the array (not shown). Array I/O lines **110** are true and compliment lines coupled to a local array sense amplifier **112** which is part of array section **64**. Column select signal **114** from column driver **115** couples array data I/O lines **110** to a pair of complimentary digit lines **116** inside the local sense amplifier **112**. One of the complimentary digit

lines is coupled to a memory cell **118** through an access device which is selected by a signal on word line **120** from a row address decoder.

Read data follows the same path from the memory cell to the global sense amp where it is then driven on complimentary data read lines **122** to complimentary data lines **126** under control of data path control logic **124** and timing circuits **59**. Complimentary data **126** is driven to an I/O pad **100** through output circuit **128**.

This specific embodiment is not intended to provide an exhaustive description of all forms of the present invention. For example, I/O line multiplexer **104** would not be necessary if there is a global sense amp **67** for each pair of array I/O lines. Alternatively, additional array I/O lines could be multiplexed through the multiplexer **104** to allow for even fewer global sense amplifiers. Another variation is to allow read and write data to share a common path between the global sense amplifiers and the I/O pad. Also, separate input and output data pins can be provided. Numerous additional variations are possible and will be recognized by one of skill in the art.

FIG. **5** is a schematic diagram providing additional detail for portions of the circuitry of FIG. **4**. In FIG. **5**, /WE and /CAS are logically combined in command latch and control circuit **154**. The write command output of circuit **154** is buffered through driver **156** to write command signal line **158**. The write command is coupled to a plurality of sense amps **66** through a distributed line resistance represented by resistor **160** over a signal line with distributed capacitive load represented by capacitor **162**. Write signal **164** arriving at the sense amplifier will be a delayed version of the output of the write command from the command latch.

Address inputs **170** are coupled to an address counter **172** and/or column address latch **174** which provide a burst column address **175** to the memory array. The column address and a version of the write command **176** are used to generate an equilibrate signal **182** in the address transition detection circuit **180**. For burst accesses, the address transition circuit may generate the equilibrate signal synchronously with an access cycle strobe signal rather than waiting for an actual address transition to be detected, especially if the address is advanced on rising /CAS edges in preparation for the next active falling edge. Equilibration control signal **182** passes through distributed resistance **184**, and is loaded by distributed capacitance **186**. A delayed version of the equilibrate signal **188** is coupled to the sense amp **66**.

The time delay of the write and equilibrate signals **164** and **188** at sense amp **66** will be dependent on which sense amp is being driven, as the distributed resistance and capacitances will vary for each sense amp location. Write command **164** and equilibrate signal **188** are combined at the global sense amp **66** in circuit **200**. In circuit **200**, the write command is gated with a decoded row address signal **204** in circuits **202** and **208**. Gated write command **210** is then combined with the equilibrate signal in logic gate **212** to form a write driver enable signal **214**. Equilibrate signal **188** provides an active low enable signal to data I/O line equilibration device **232**. When the equilibrate signal on line **188** is low, device **232** couples the two data I/O lines **106** together to equalize their potentials. A low on line **188** also disables logic device **212** preventing the write driver enable **214** from going active. When the equilibrate control signal **188** transitions high, the equilibration device **232** is deactivated, and the write driver enable gate **212** is enabled. For write cycles it is beneficial to provide the write command on line **164** before the equilibrate signal **188** goes high, then as soon as the equilibrate signal **188** goes high, the write command will be passed through gate **212** placing the write enable signal **214** in an active low condition without the requirement for an equilibration to write enable delay. Signal **214** is inverted in inverter **216** to provide an active high write enable **218**. The active low write enable goes to two NOR gates **242** and **246**. Active high write enable **218** is coupled to NAND gates **240** and **244**. The NOR and NAND gates pass write data to the I/O lines through devices **250–256** when enabled by the write driver enable signals **214** and **218**. For writing a logic "one" for example, the write data on line **103** may be high. A high on signal **103** in combination with a high write driver enable on signal line **218** will provide a low output from NAND gate **240** which will turn on device **250** to drive a logic one on the true I/O line. the high signal on data line **103** will disable NOR gate **242** to eliminate a current path to ground while NAND **250** is turned on. Data line **103** is inverted at inverter **258** to provide compliment data **260**. When data line **103** is high, complimentary data line **260** will be low which will enable NOR gate **246** and disable NAND gate **244**. Enabled NOR gate **246** combined with the active write driver enable signal **214** will provide a high output from NOR **246** to turn on device **256** and drive the complimentary I/O line low. For a maximized data write cycle time, the write command **164** can remain active throughout a burst write access. In this case, the write drivers are enabled and disabled by the equilibrate signal which will occur at the beginning of each access cycle. Multiple write command signals **158** may be utilized in devices with multiple /CAS or multiple /WE inputs to control writes to one of multiple data bytes for example. The decoded row address input prevents the write drivers from driving data on I/O lines in nonselected sections of the array. Multiplexer **104** of FIG. **4** may be turned on during equilibrate and write portions of the cycle to allow array I/O lines to first be equilibrated and then receive write data. For nonburst mode memory devices, it is beneficial to provide the write command prior to the end of the equilibrate function to allow the write to begin as soon as possible. For these devices, the write will typically end prior to the next /CAS falling edge to allow the device to meet the column address to data valid access time in (TAA). For EDO devices in particular, the page mode cycle time is very short, but the address access time begins while /CAS is high, so the write cycles should end as soon as possible. One way to allow the write cycle to end as soon as possible is to begin it immediately after the equilibrate is complete.

It is important to note that devices **250** and **256** will generally be enabled simultaneously, as will devices **252** and **254**. If the enable gate **212** were not locally present, then the write enable signal would need to be delayed from the equilibrate disable time to guarantee that a current path through devices **250**, **232** and **256** or devices **252**, **232** and **254** does not exist.

At the end of a burst write access, the write enable may be deactivated in response to /RAS high and /CAS high, /RAS high alone, or after a time-out period following /CAS high. As stated above, the write command may be held active throughout a burst write access. Alternatively, it may be cleared at the beginning of each access cycle, and then relatched provided that /WE is low on the following /CAS high to low transition. If cleared, the period of time that the write command is inactivated within a burst write access is preferably shorter than the equilibrate time so that the write cycle can be maximized which in turn allows for a minimum cycle time. When a read command is detected (/WE high at /CAS falling), a current burst write access will be terminated

and a burst read access will begin. It may be desirable to gate the equilibrate signal with the read command and the write control signal to ensure that the equilibrate signal does not end prior to the write control signal becoming invalid. This would be done to prevent the write drivers from becoming enabled for a fraction of the first read cycle in a burst read access sequence.

By gating the write command and equilibrate signals at the sense amplifiers, numerous advantages are obtained over the simple write command delay. One advantage is a maximized write time since the write cycle can begin as soon as the equilibrate is complete for all device types, and can last until the next cycle begins in burst access devices. A second advantage is elimination of write driver enable delay circuitry which can have a variable delay dependent on the operating conditions of the memory device (supply voltage, temperature, etc.). Each driver will be fired when the equilibrate signal is locally deactivated, eliminating the possibility of crossing current through complimentary write drivers while complimentary data lines are coupled together for equilibration.

A memory device may be designed with multiple /CAS inputs as described above. For a memory device with two /CAS inputs where each /CAS controls eight bits of a sixteen bit wide data port, a write cycle where only one /CAS is low must not write all data bits from the data input to the memory. A portion of the write data path associated with an inactive /CAS may be interrupted in a number of ways. Each of the two /CAS signals may enable half of the column address decoders such that no column will be selected in half of the memory associated with a high /CAS in a write cycle. In this case the write data drivers can be enabled, but the data I/O lines associated with a disabled column decoder will not be coupled to any memory cells. Alternately, the write control signals may be gated with the appropriate /CAS signal to prevent some of the write data drivers from being enabled. In this case, read data may be coupled from some memory cells to data I/O lines.

FIG. 6 is a schematic representation of a data processing apparatus designed in accordance with the present invention. For the purposes of this specification a microprocessor may be, but is not limited to, a central processing unit (CPU), a microprocessor, a microcontroller, a digital signal processor, or an arithmetic processor. In FIG. 6, microprocessor **112** is connected via address lines **114** and control lines **116** to a memory control circuit **118**. The memory control circuit provides address and control signals on lines **122** and **120** respectively to a burst access memory device **124**. The burst access memory device sends and receives data over data bus **126**. Optional data bus buffer **130** between memory data bus **126** and microprocessor data bus **128** allows for amplification of the data signals, and/or synchronization with the microprocessor and memory control signals. A fast static random access memory (SRAM) cache circuit **132** is also optional and provides higher speed access to data stored in the cache from the memory circuit or the microprocessor. Memory control circuit **118** may be incorporated within the microprocessor. The memory control circuit provides the required address strobe signals and read/write control signals required for burst mode access of the memory circuit. By providing burst access of the memory by the processor, a computer with relatively high memory bandwidth can be designed without the requirement of a fast SRAM cache. SRAMs which are fast enough to provide memory access without wait states can significantly add to the cost of a computer. Thus the burst access memory device of the present invention allows for medium to high performance computers to be manufactured at a cost which is significantly less than those manufactured today. Use of the burst access memory device of the present invention in cooperation with a fast SRAM cache allows for an even higher performance computer design by providing fast access to main memory in the event of a cache miss.

In a burst write operation, the processor **112** provides an initial address and a write command to the memory controller. The memory controller provides a row address to the memory with a row address strobe. The memory controller then provides a write command, a column address and a column address strobe to the memory. The memory will equilibrate internal data I/O lines in response to receipt of the write command and column address. During the equilibrate operation, write data and write command signals are passed to global sense amplifiers within the burst access memory device. At the end of the equilibrate operation, write data drivers are enabled, and write data is stored in the memory array. In a preferred embodiment, positive (low to high) transitions of /CAS will cause an internal address counter of the memory device to advance to the next burst address. Negative (high to low) transitions of /CAS will then end the previous write cycle and equilibrate the I/O lines. The negative transition of /CAS will also allow the burst address from the counter to be applied to the array. Once the equilibration is complete, the next write will be performed at the burst address from the counter. In an alternate embodiment, a clock signal is input to a burst access device to control generation of a burst address from the counter (SDRAMs for example have a clock input pin).

In another embodiment, memory **124** operates in a page mode such as Fast Page Mode or EDO mode. Write commands at memory sense amps are enabled by the equilibrate signal becoming inactive at the sense amp. Using the equilibrate signal at the sense amp to gate the write signal to enable the write drivers eliminates wasted time associated with delaying the write driver enable signal to prevent excessive currents from flowing through the write drivers during the equilibration operation.

For the purposes of this specification a node may be, but is not limited to, an intersection of conductors, a circuit input or output, or any point along a signal path. For example, the write command may be said to enter the global sense amp at node **164** and device **250** of FIG. **5** is said to be connected to a power source at node **270**. Also, the term signal may refer to but is not limited to information transferred along a conductor, or may refer to the conductor itself. For example, It may be said that the equilibrate signal **188** is coupled to the sense amp **66**. In this context, the term signal represents a physical conductor for carrying the electrical information to equilibrate the data I/O lines, and is not limited to the electrical information itself which is not present when the device is not connected to a power source. The term "coupled" refers to but is not limited to a connection which may be made directly, after buffering, or through another element such as a resistor, capacitor, transistor, or logic device. Typically, a device will be responsive at some time to a signal or another device which is coupled to it.

While the present invention has been described with reference to preferred embodiments, numerous modifications and variations of the invention will be apparent to one of skill in the art without departing from the scope of the invention.

What is claimed is:

1. A memory device comprising:

a memory element array region;

a control circuit region;

a plurality of data line pairs dispersed throughout the memory element array region, each of the data line pairs comprising a true data line and a compliment data line;

a plurality of equilibration devices, each of the equilibration devices coupled to the true data line and the compliment data line of one of the plurality of data line pairs, and each of the equilibration devices responsive to an equilibrate signal from the control circuit region to couple the true data line to the compliment data;

a plurality of data sense amplifiers, each proximately located at least one of the data line pairs; and

a distributed plurality of write data drivers each comprising an equilibrate inactive input responsive to the equilibrate signal, a write active input responsive to a write enable signal from the control circuit region, a true write data output coupled to the true data line of one of the data line pairs and a compliment write data output coupled to the compliment data line of one of the data line pairs for driving data on the data line pairs in response to the equilibrate and write enable signals, each of the write data drivers proximately located to at least one of the data sense amplifiers.

2. The memory device of claim 1, further comprising:

a mode select circuit adapted to select between a mode of operation from at least EDO and Burst EDO modes,

wherein the distributed plurality of write data drivers are each responsive to the mode.

3. A method of writing data into a memory device comprising steps of:

providing an address for the memory device;

asserting an equilibrate signal which is coupled to an equilibration device in order to equilibrate internal data lines of the memory device in response to the step of providing an address;

coupling the equilibrate signal to a plurality of data driver enable circuits;

coupling a write enable signal to the plurality of data driver enable circuits;

deasserting the equilibrate signal after the internal data lines are equilibrated;

gating the write enable signal through at least one of the data driver enable circuits in response to the step of deasserting the equilibrate signal;

driving data onto the internal data lines in response to the step of gating; and

storing data in a memory cell in response to the step of driving data.

4. The method of claim 3 wherein the step of providing an address is completed using an external microprocessor.

5. The method of claim 4 wherein the data is provided from the external microprocessor.

* * * * *

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[45] **Date of Patent: *Sep. 1, 1998**

[54] **BURST EDO MEMORY DEVICE**

[75] Inventors: **Paul S. Zagar**, Boise; **Brett L. Williams**, Eagle; **Troy A. Manning**, Boise, all of Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

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Related U.S. Application Data

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[51] **Int. Cl.**^{6} **G11C 8/00**

[52] **U.S. Cl.** **365/233.5**; 365/238.5

[58] **Field of Search** 365/233.5, 238.5, 365/230.06, 230.08

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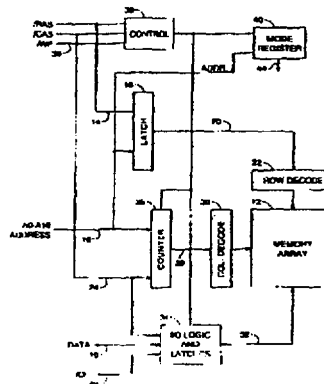
Primary Examiner—Tan T. Nguyen

Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

An integrated circuit memory device is designed for high speed data access and for compatibility with existing memory systems. An address strobe signal is used to latch a first address. During a burst access cycle the address is incremented internal to the device with additional address strobe transitions. A new memory address is only required at the beginning of each burst access. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at the device cycle frequency. Transitions of the Read/Write control line during a burst access will terminate the burst access, reset the burst length counter and initialize the device for another burst access. The device is compatible with existing Extended Data Out DRAM device pinouts, Fast Page Mode and Extended Data Out Single In-Line Memory Module pinouts, and other memory circuit designs.

2 Claims, 7 Drawing Sheets



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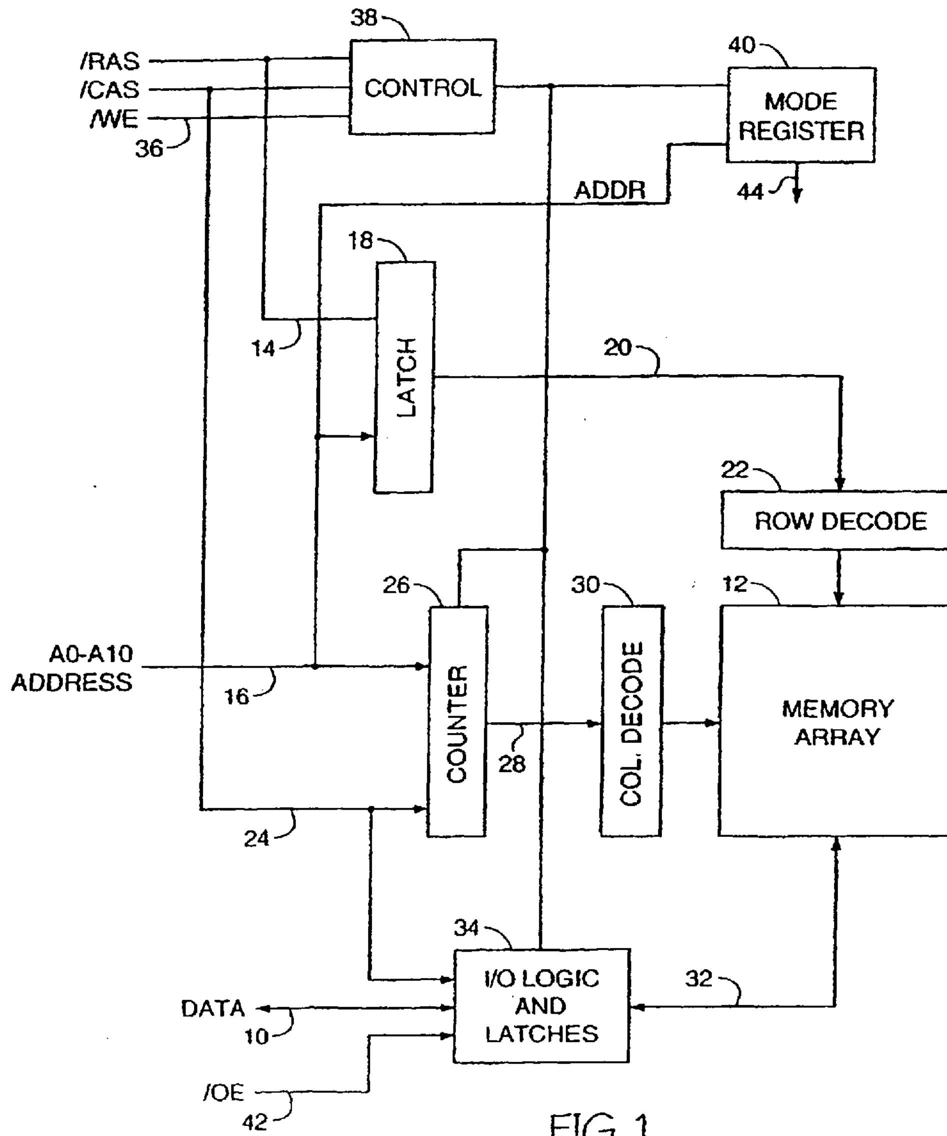

FIG. 1

Burst Length	Starting Column Address A_2	A_1	A_0	Linear	Interleave
2	V	V	0	0-1	0-1
	V	V	1	1-0	1-0
4	V	0	0	0-1-2-3	0-1-2-3
	V	0	1	1-2-3-0	1-0-3-2
	V	1	0	2-3-0-1	2-3-0-1
	V	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

FIG. 2

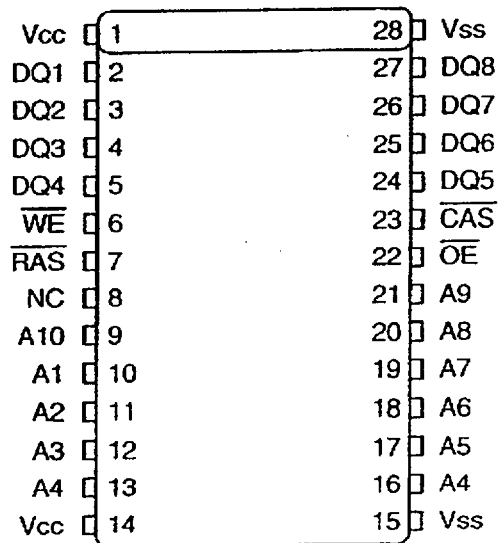

FIG. 3

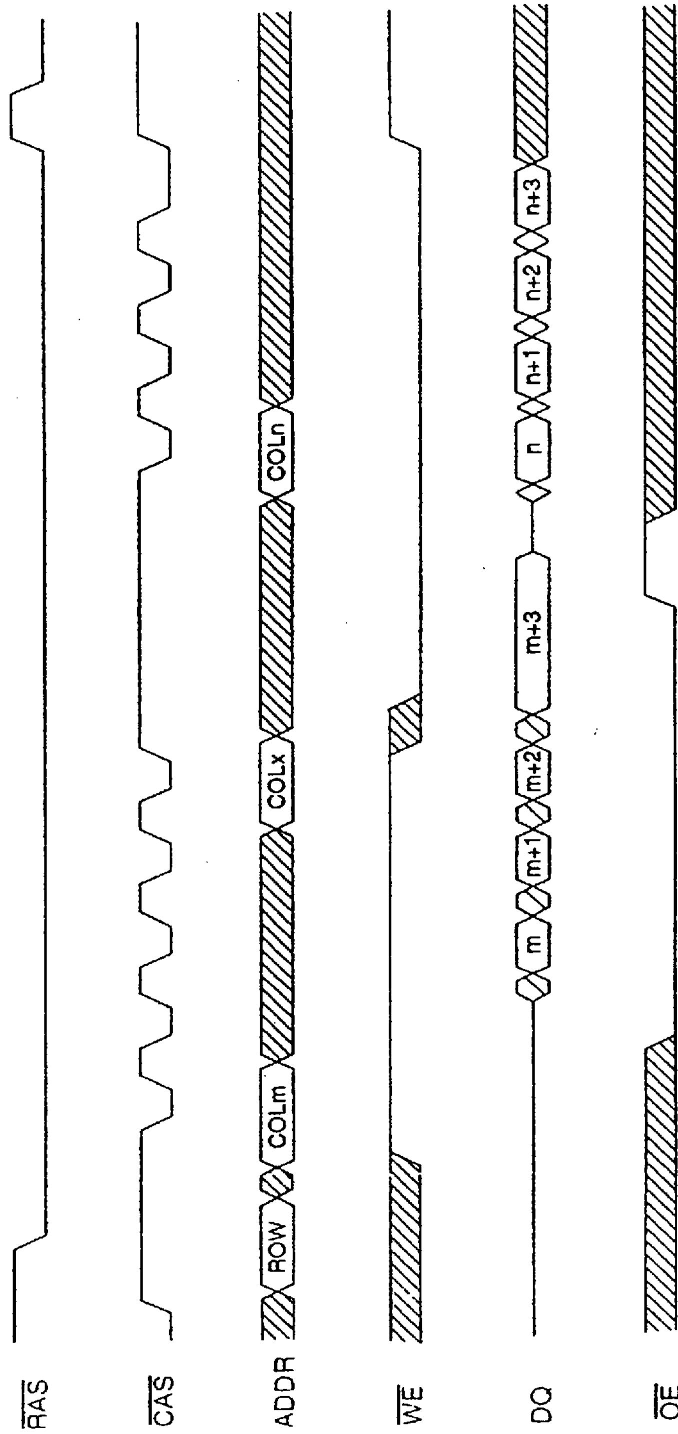

FIG. 4

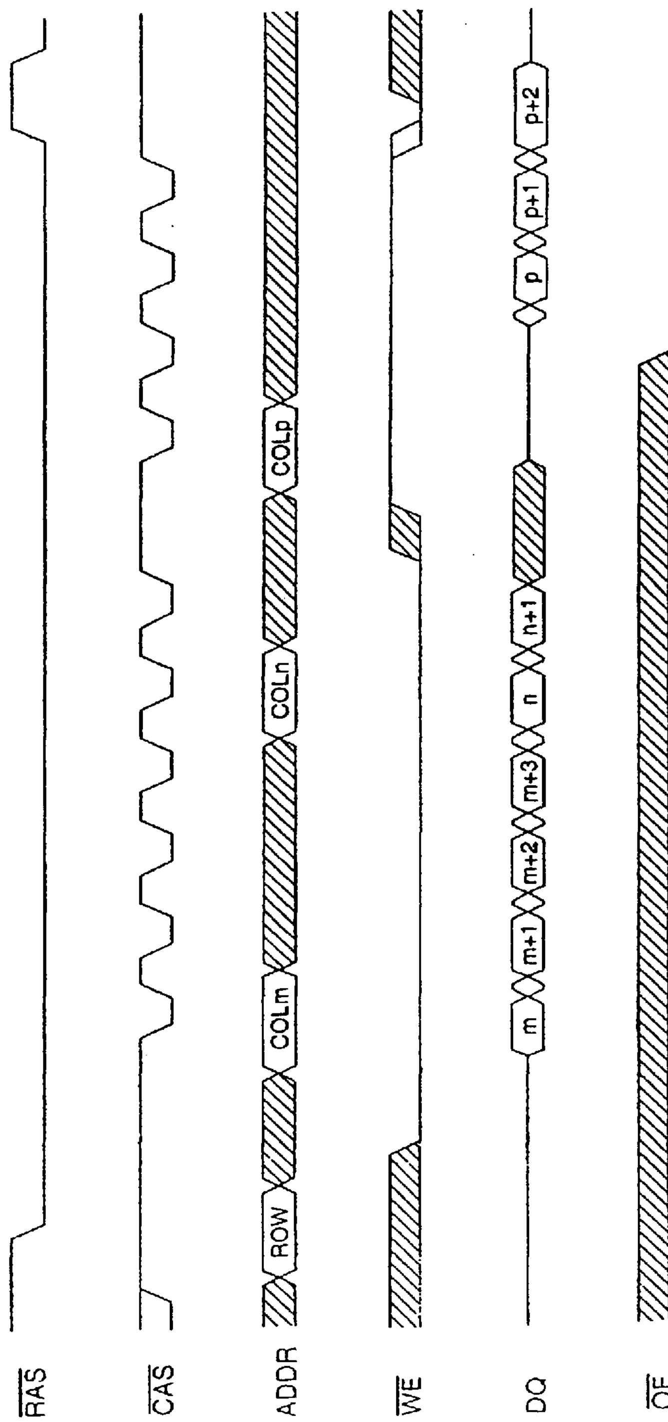

FIG. 5

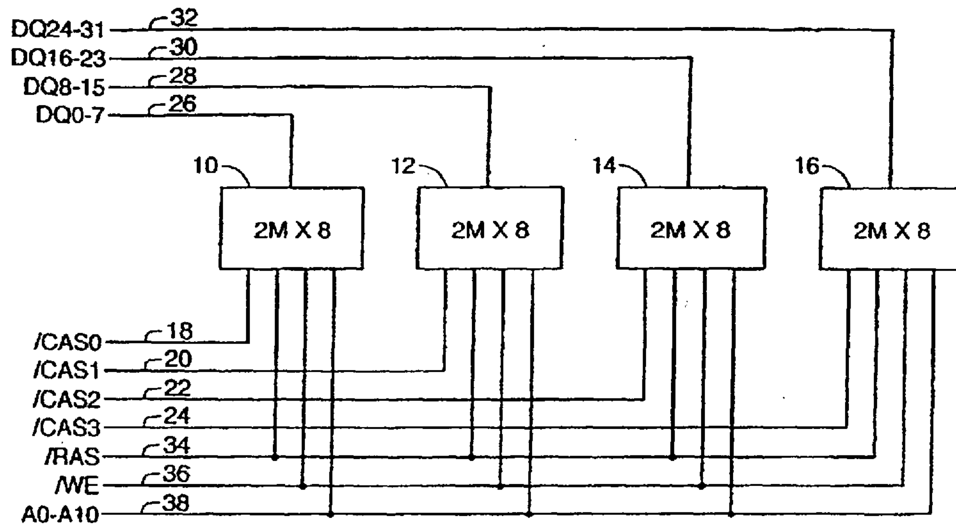

FIG. 6

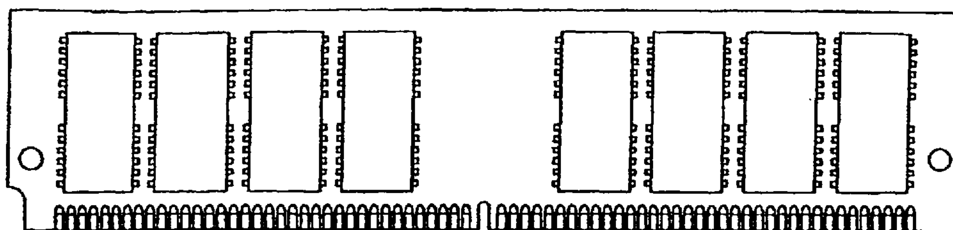

FIG. 7

PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	$\overline{\text{CAS0}}$	58	DQ29
5	DQ18	23	DQ22	41	$\overline{\text{CAS2}}$	59	Vcc
6	DQ3	24	DQ7	42	$\overline{\text{CAS3}}$	60	DQ30
7	DQ19	25	DQ23	43	$\overline{\text{CAS1}}$	61	DQ14
8	DQ4	26	DQ8	44	$\overline{\text{RAS0}}$	62	DQ31
9	DQ20	27	DQ24	45	$\overline{\text{RAS1}}$	63	DQ15
10	Vcc	28	A7	46	$\overline{\text{OE}}$	64	DQ32
11	PD5	29	NC	47	$\overline{\text{WE}}$	65	DQ16
12	A0	30	Vcc	48	PD ECC	66	PD EDO
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ25	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	NC	52	DQ26	70	PD4
17	A5	35	NC	53	DQ11	71	PD refresh
18	A6	36	NC	54	DQ27	72	Vss

FIG. 8

RX-1241

BURST EDO MEMORY DEVICE

This is a continuation of application Ser. No. 08/370,761, filed Dec. 23, 1994 now U.S. Pat. No. 5,526,320.

FIELD OF THE INVENTION

This invention relates to memory device architectures designed to provide high density data storage with high speed read and write access cycles.

BACKGROUND OF THE INVENTION

Dynamic Random Access Memory devices (DRAMs) are among the highest volume and most complex integrated circuits manufactured today. Except for their high volume production, the state of the art manufacturing requirements of these devices would cause them to be exorbitantly priced. Yet, due to efficiencies associated with high volume production, the price per bit of these memory devices is continually declining. The low cost of memory has fueled the growth and development of the personal computer. As personal computers have become more advanced, they in turn have required faster and more dense memory devices, but with the same low cost of the standard DRAM. Fast page mode DRAMs are the most popular standard DRAM today. In fast page mode operation, a row address strobe (/RAS) is used to latch a row address portion of a multiplexed DRAM address. Multiple occurrences of the column address strobe (/CAS) are then used to latch multiple column addresses to access data within the selected row. On the falling edge of /CAS an address is latched, and the DRAM outputs are enabled. When /CAS transitions high the DRAM outputs are placed in a high impedance state (tri-state). With advances in the production of integrated circuits, the internal circuitry of the DRAM operates faster than ever. This high speed circuitry has allowed for faster page mode cycle times. A problem exists in the reading of a DRAM when the device is operated with minimum fast page mode cycle times. /CAS may be low for as little as 15 nanoseconds, and the data access time from /CAS to valid output data (tCAC) may be up to 15 nanoseconds; therefore, in a worst case scenario there is no time to latch the output data external to the memory device. For devices that operate faster than the specifications require, the data may still only be valid for a few nanoseconds. On a heavily loaded microprocessor memory bus, trying to latch an asynchronous signal that is valid for only a few nanoseconds is very difficult. Even providing a new address every 35 nanoseconds requires large address drivers which create significant amounts of electrical noise within the system. To increase the data throughput of a memory system, it has been common practice to place multiple devices on a common bus. For example, two fast page mode DRAMs may be connected to common address and data buses. One DRAM stores data for odd addresses, and the other for even addresses. The /CAS signal for the odd addresses is turned off (high) when the /CAS signal for the even addresses is turned on (low). This interleaved memory system provides data access at twice the rate of either device alone. If the first /CAS is low for 20 nanoseconds and then high for 20 nanoseconds while the second /CAS goes low, data can be accessed every 20 nanoseconds or 50 megahertz. If the access time from /CAS to data valid is fifteen nanoseconds, the data will be valid for only five nanoseconds at the end of each 20 nanosecond period when both devices are operating in fast page mode. As cycle times are shortened, the data valid period goes to zero.

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead, data is held valid after /CAS goes high until sometime after the next /CAS low pulse occurs, or until /RAS or the output enable (/OE) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can be a complex function of when the column address inputs are valid, when /CAS falls, the state of /OE and when /CAS rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially /CAS) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM manufacturers.

Methods to shorten memory access cycles tend to require additional circuitry, additional control pins and nonstandard device pinouts. The proposed industry standard synchronous DRAM (SDRAM)for example has an additional pin for receiving a system clock signal. Since the system clock is connected to each device in a memory system, it is highly loaded, and it is always toggling circuitry in every device. SDRAMs also have a clock enable pin, a chip select pin and a data mask pin. Other signals which appear to be similar in name to those found on standard DRAMs have dramatically different functionality on a SDRAM. The addition of several control pins has required a deviation in device pinout from standard DRAMs which further complicates design efforts to utilize these new devices. Significant amounts of additional circuitry are required in the SDRAM devices which in turn result in higher device manufacturing costs.

In order for existing computer systems to use an improved device having a nonstandard pinout, those systems must be extensively modified. Additionally, existing computer system memory architectures are designed such that control and address signals may not be able to switch at the frequencies required to operate the new memory device at high speed due to large capacitive loads on the signal lines. The Single In-Line Memory Module (SIMM) provides an example of what has become an industry standard form of packaging memory in a computer system. On a SIMM, all address lines connect to all DRAMs. Further, the row address strobe (/RAS) and the write enable (/WE) are often connected to each DRAM on the SIMM. These lines inherently have high capacitive loads as a result of the number of device inputs driven by them. SIMM devices also typically ground the output enable (/OE) pin making /OE a less attractive candidate for providing extended functionality to the memory devices.

There is a great degree of resistance to any proposed deviations from the standard SIMM design due to the vast number of computers which use SIMMs. Industry's resistance to radical deviations from the standard, and the inability of current systems to accommodate the new memory devices will delay their widespread acceptance. Therefore only limited quantities of devices with radically different architectures will be manufactured initially. This limited manufacture prevents the reduction in cost which typically can be accomplished through the manufacturing improvements and efficiencies associated with a high volume product.

SUMMARY OF THE INVENTION

An integrated circuit memory device with a standard DRAM pinout is designed for high speed data access and for compatibility with existing memory systems. A high speed burst mode of operation is provided where multiple sequential accesses occur following a single column address, and read data is output relative to the /CAS control signal. In the burst mode of operation the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at high speeds. Only one control line per memory chip (/CAS) must toggle at the operating frequency in order to clock the internal address counter and the data input/output latches. The load on each /CAS is typically less than the load on the other control signals (/RAS, /WE and /OE) since each /CAS typically controls only a byte width of the data bus. Internal circuitry of the memory device is largely compatible with existing Extended Data Out (EDO) DRAMs. This similarity allows the two part types to be manufactured on one die with a limited amount of additional circuitry. The ability to switch between a standard non-burst mode and a high speed burst mode allows the device to be used to replace standard devices, and eliminates the need to switch to more complex high speed memory devices. Internal address generation provides for faster data access times than is possible with either fast page mode or EDO DRAMs. This high speed operation eliminates the need to interleave memory devices in order to attain a high data throughput. In contrast to the 50 megahertz interleaved memory system described above, the output data from this device will be valid for approximately 15 nanoseconds significantly easing the design of circuitry required to latch the data from the memory. The device is compatible with existing memory module pinouts including Single In-Line Memory Module (SIMM), Multi-Chip Module (MCM) and Dual In-Line Memory Module (DIMM) designs. This combination of features allows for significant system performance improvements with a minimum of design alterations.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention as well as objects and advantages will be best understood by reference to the appended claims, detailed description of particular embodiments and accompanying drawings where:

FIG. 1 is an electrical schematic diagram of a memory device in accordance with one embodiment of the invention;

FIG. 2 is a table showing linear versus interleaved addressing formats;

FIG. 3 is a pinout of the memory device of FIG. 1;

FIG. 4 is a timing diagram for a method of accessing the device of FIG. 1;

FIG. 5 is a further timing diagram for accessing the device of FIG. 1;

FIG. 6 is an electrical schematic diagram of a Single In-Line Memory Module in accordance with another embodiment of the invention;

FIG. 7 is a front view of a Single In-Line Memory Module designed in accordance with the teachings of this invention; and

FIG. 8 is a table of the pin numbers and signal names of the Single In-Line Memory Module of FIG. 7.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a schematic representation of a sixteen megabit device designed in accordance with the present invention. The device is organized as a 2 Meg×8 burst EDO DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array 12. The device of FIG. 1 has an industry standard pinout for eight bit wide EDO DRAMs. An active-low row address strobe (/RAS) signal 14 is used to latch a first portion of a multiplexed memory address, from address inputs A0 through A10 16, in latch 18. The latched row address 20 is decoded in row decoder 22. The decoded row address is used to select a row of the memory array 12. A column address strobe (/CAS) signal 24 is used to latch a second portion of a memory address from address inputs 16 into column address counter 26. The latched column address 28 is decoded in column address decoder 30. The decoded column address is used to select a column of the memory array 12.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 32 to output latches 34. Data 10 driven from the burst EDO DRAM may be latched external to the device in synchronization with /CAS after a predetermined number of /CAS cycle delays (latency). For a two cycle latency design, the first /CAS falling edge is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second /CAS falling edge, and remains valid through the third /CAS falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during /CAS high intervals dependent on the state of the output enable and write enable (/OE and /WE) control lines, thus allowing additional time for the system to latch the output data. Once a row and a column address are selected, additional transitions of the /CAS signal are used to advance the column address within the column address counter in a predetermined sequence. The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the /CAS signal provided that /OE is maintained low, and /WE remains high. The output data signal levels may be driven in accordance with standard CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. FIG. 2 is a table which shows linear and interleaved addressing sequences for burst lengths of 2,4 and 8 cycles. The "V" for starting addresses A1 and A2 in the table represent address values that remain unaltered through the burst sequence. The column address may be advanced with each /CAS transition, each pulse, or multiple of /CAS pulses in the event that more than one data word is read from the array with each column address. When the address is advanced with each transition of the /CAS signal, data is also driven from the part after each transition following the device latency which is then referenced to each edge of the /CAS signal. This allows for a burst access cycle where the highest switching control line (/CAS) toggles only once (high to low or low to high) for each memory cycle. This is in contrast to standard DRAMs which require /CAS to go low and then high for each cycle, and synchronous DRAMs which require a full clock cycle (high and low transitions) for each memory cycle. For maximum compatibility with existing EDO DRAM devices, the invention will be further described in reference to a device designed to latch and advance a column address on falling edges of the /CAS signal.

United States Patent [19]

Zagar et al.

[11] **Patent Number: 5,812,488**

[45] **Date of Patent: *Sep. 22, 1998**

[54] **SYNCHRONOUS BURST EXTENDED DATA OUT DRAM**

[75] Inventors: **Paul S. Zagar; Troy A. Manning; Todd Merritt**, all of Boise, Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,668,773.

[21] Appl. No.: **811,696**

[22] Filed: **Mar. 5, 1997**

Related U.S. Application Data

[63] Continuation of Ser. No. 552,199, Nov. 21, 1995, Pat. No. 5,668,773, and a continuation-in-part of Ser. No. 370,761, Dec. 23, 1994, Pat. No. 5,526,320.

[51] **Int. Cl.**[6] **G11C 8/00**

[52] **U.S. Cl.** **365/233**; 365/233.5; 365/236; 395/855

[58] **Field of Search** 365/233, 233.5, 365/238.5, 236; 395/855

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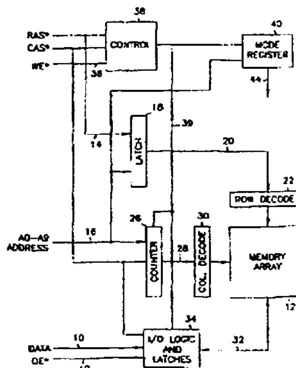
Primary Examiner—Tan T. Nguyen
Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

An integrated circuit memory device is described which can operate at high data speeds. The memory device can either store or retrieve data from the memory in a burst access operation. The burst operations latches a memory address from external address lines and internally generates additional memory addresses. A clock signal is provided to synchronize the burst operations. The clock signal is independent of an address latch signal used to latch an external address.

18 Claims, 7 Drawing Sheets



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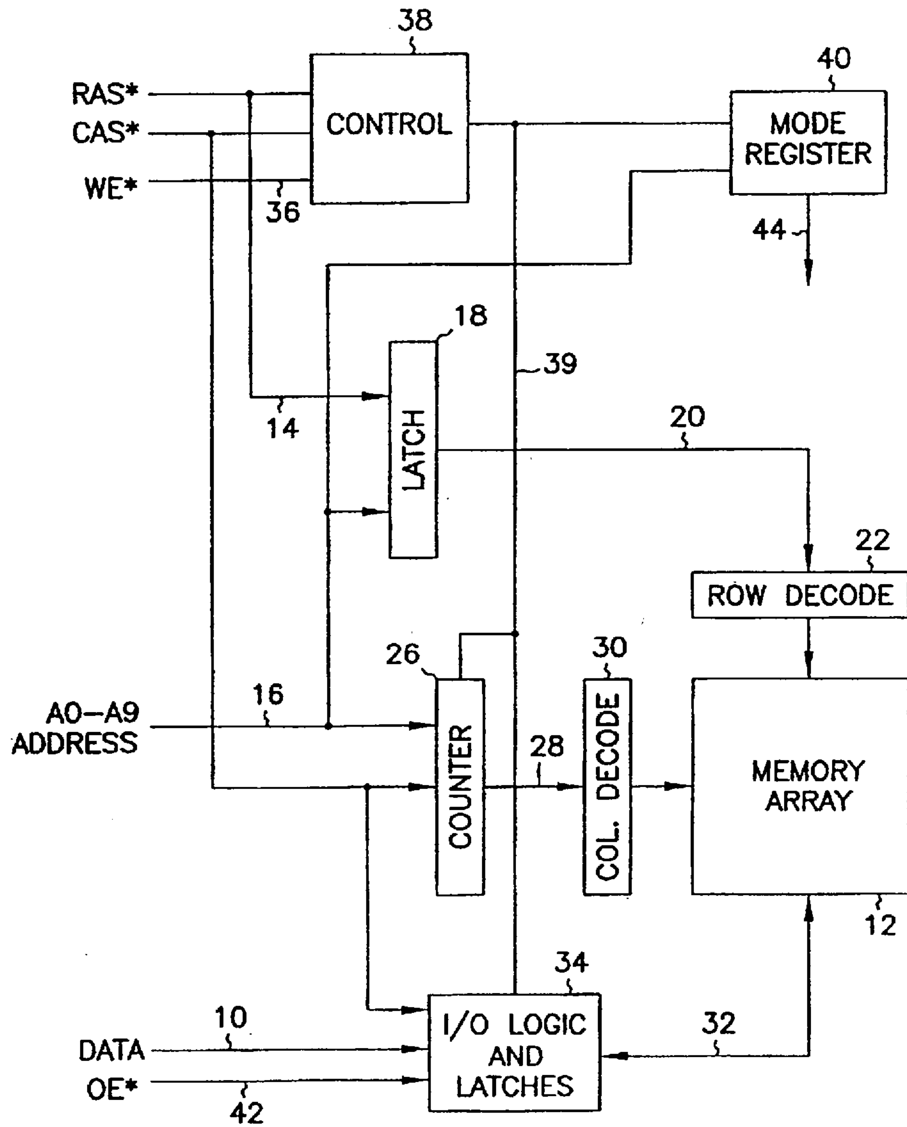

FIG. 1

Burst Length	Starting Column Address A_2	A_1	A_0	Linear	Interleave
2	V	V	0	0-1	0-1
	V	V	1	1-0	1-0
4	V	0	0	0-1-2-3	0-1-2-3
	V	0	1	1-2-3-0	1-0-3-2
	V	1	0	2-3-0-1	2-3-0-1
	V	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

FIG. 2

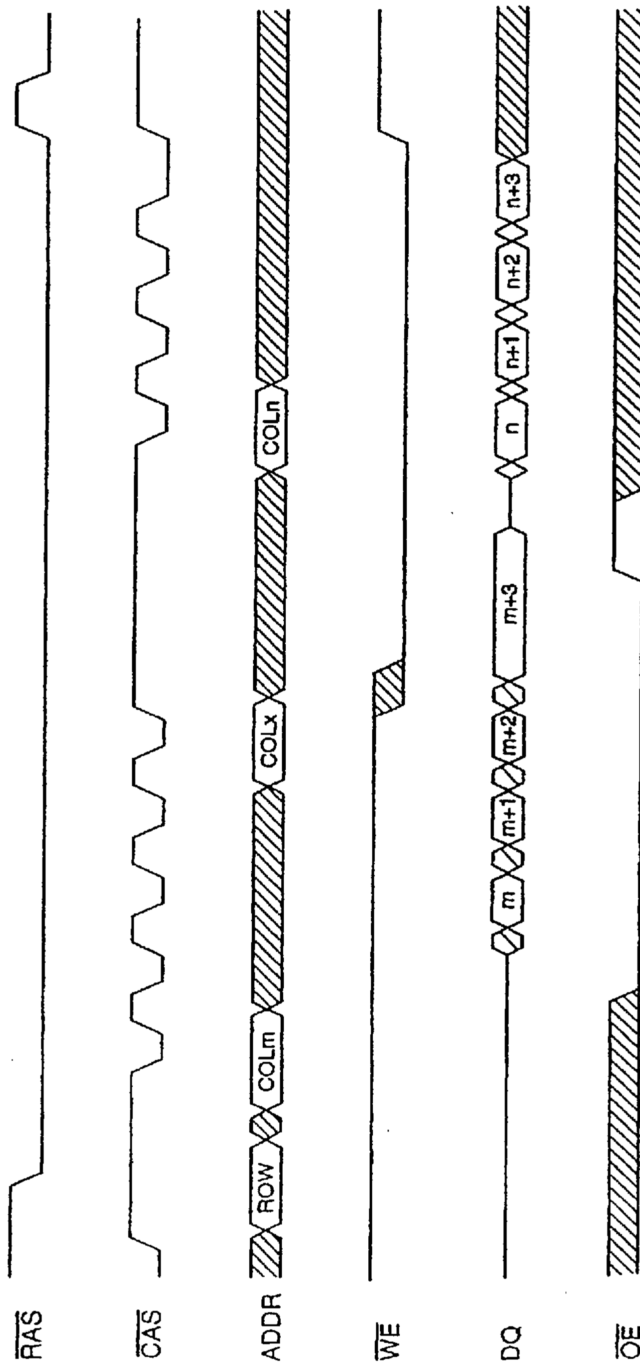

FIG. 3

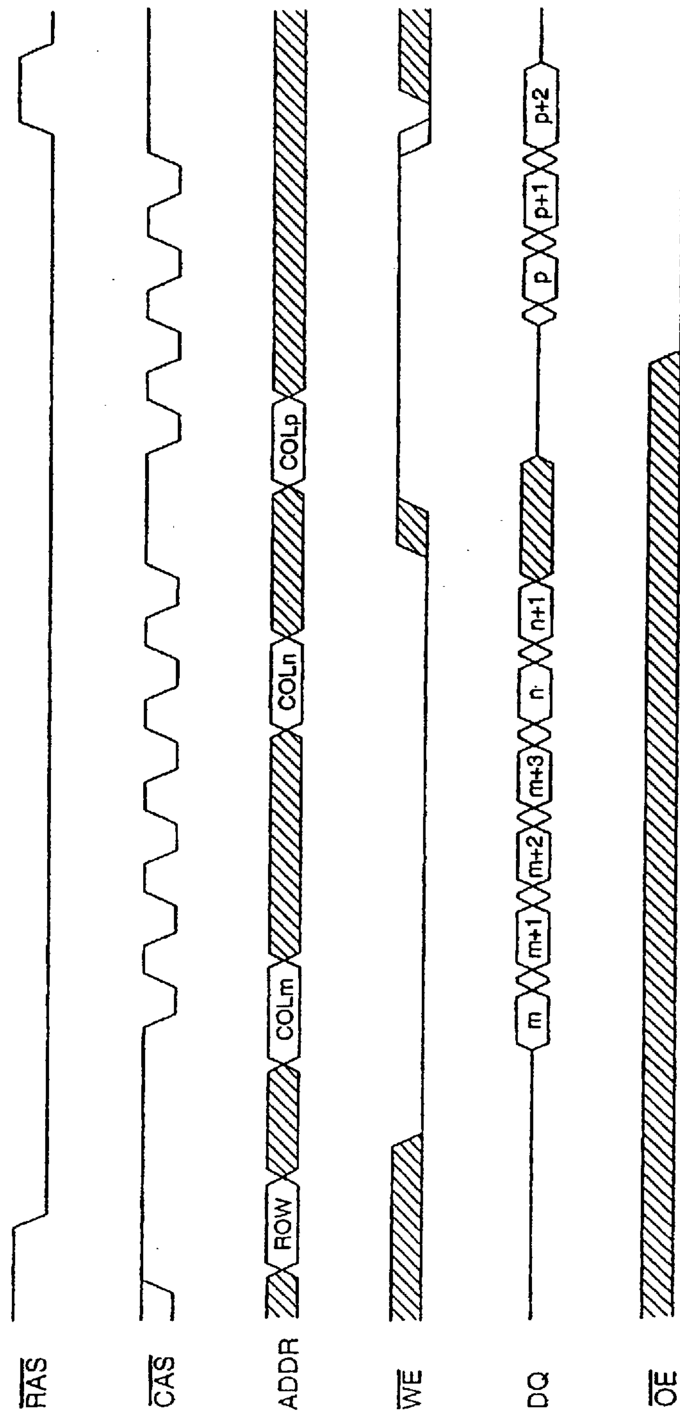

FIG. 4

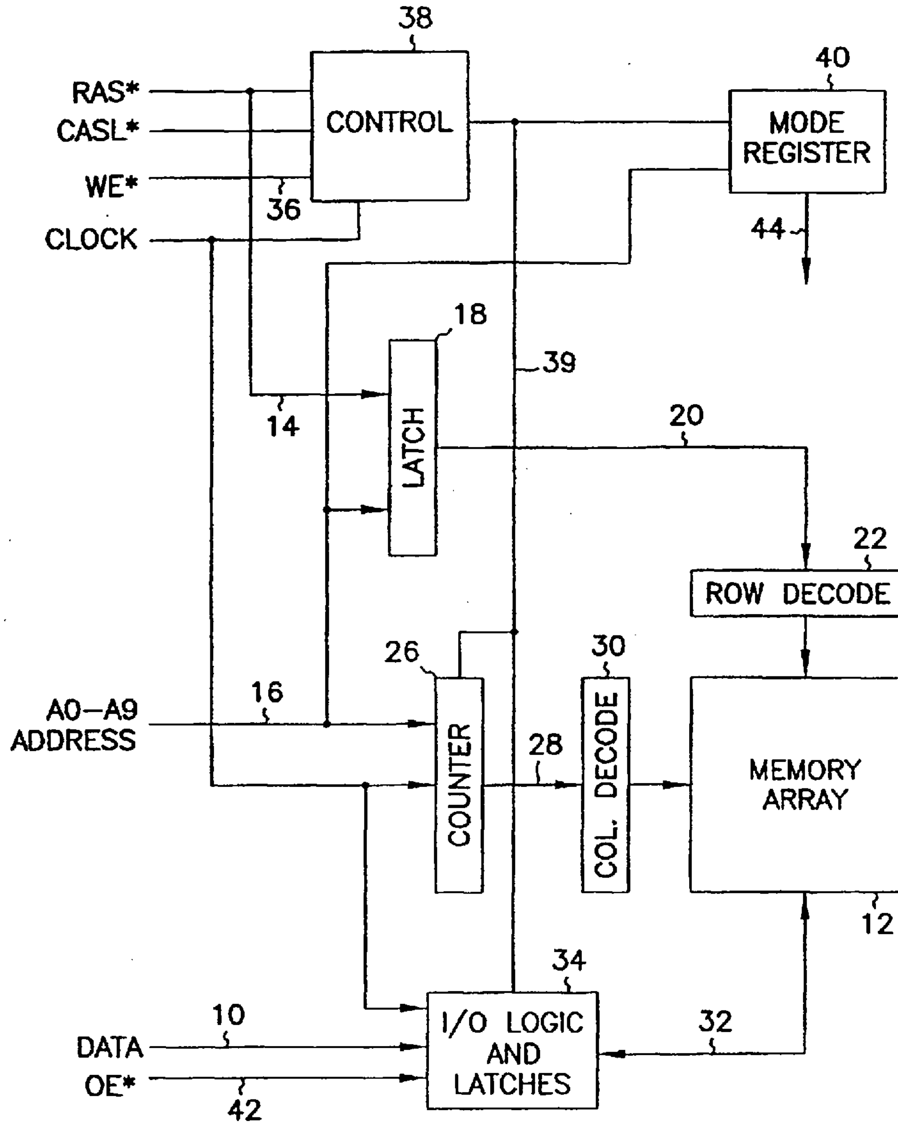

FIG. 5

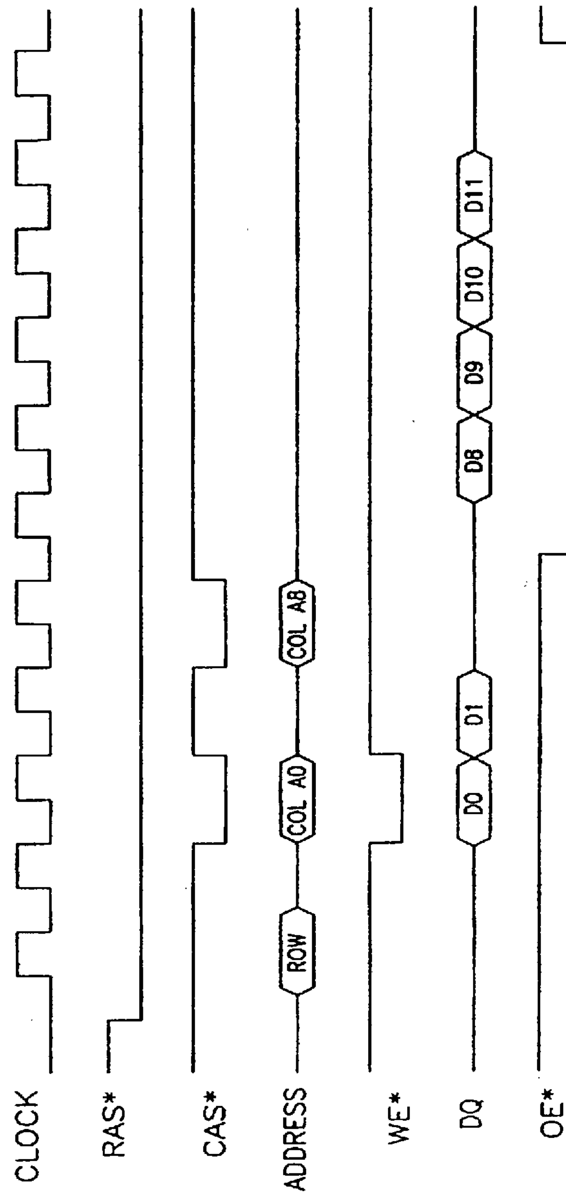

FIG. 6

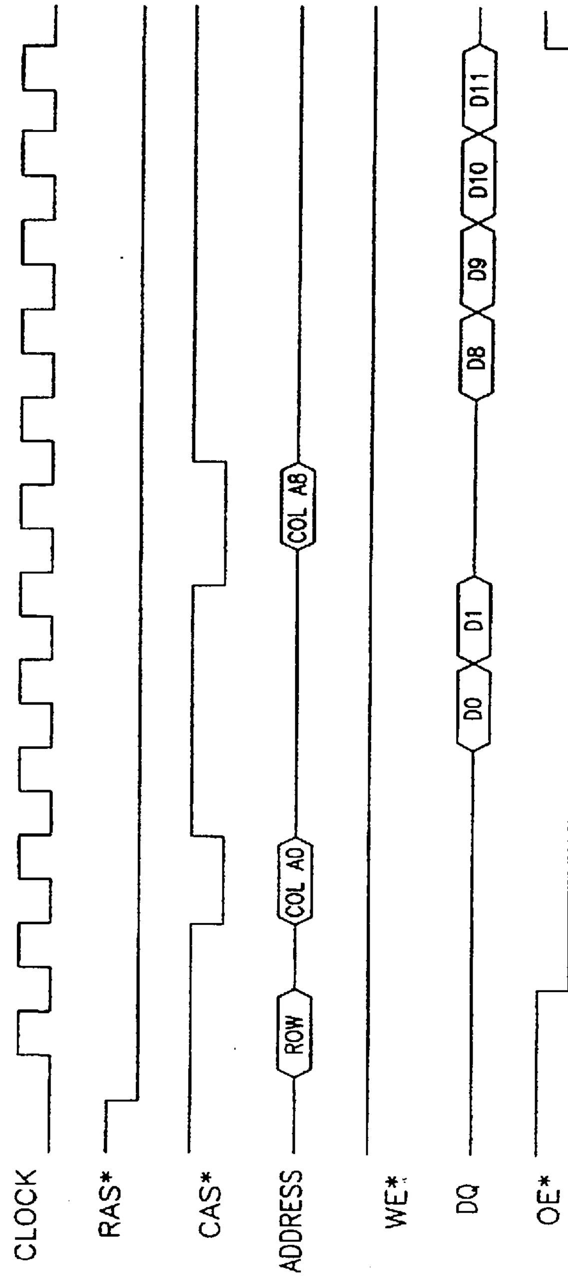

FIG. 7

SYNCHRONOUS BURST EXTENDED DATA OUT DRAM

This Application is a continuation of U.S. patent application Ser. No. 08/552,199 filed Nov. 2, 1995, now U.S. Pat. No. 5,668,773 and is a continuation-in-part of U.S. application Ser. No. 08/370,761, filed of Dec. 23, 1994, now U.S. Pat. No. 5,526,320, and entitled "Burst EDO Memory Device," which is incorporated herein by reference.

FIELD OF THE INVENTION

This invention relates to synchronous memory devices and in particular to memory device architectures designed to provide high density data storage with high speed read and write access cycles.

BACKGROUND OF THE INVENTION

Dynamic Random Access Memory devices (DRAMs) are among the highest volume and most complex integrated circuits manufactured today. Except for their high volume production, the state of the art manufacturing requirements of these devices would cause them to be exorbitantly priced. Yet, due to efficiencies associated with high volume production, the price per bit of these memory devices is continually declining. The low cost of memory has fueled the growth and development of the personal computer. As personal computers have become more advanced, they in turn have required faster and more dense memory devices, but with the same low cost of the standard DRAM. Fast page mode DRAMs are the most popular standard DRAM today. In fast page mode operation, a row address strobe (RAS*) is used to latch a row address portion of a multiplexed DRAM address. Multiple occurrences of the column address strobe (CAS*) are then used to latch multiple column addresses to access data within the selected row. On the falling edge of CAS* an address is latched, and the DRAM outputs are enabled. When CAS* transitions high the DRAM outputs are placed in a high impedance state (tri-state). With advances in the production of integrated circuits, the internal circuitry of the DRAM operates faster than ever. This high speed circuitry has allowed for faster page mode cycle times. A problem exists in the reading of a DRAM when the device is operated with minimum fast page mode cycle times. CAS* may be low for as little as 15 nanoseconds, and the data access time from CAS* to valid output data (t_{CAC}) may be up to 15 nanoseconds; therefore, in a worst case scenario there is no time to latch the output data external to the memory device. For devices that operate faster than the specifications require, the data may still only be valid for a few nanoseconds. On a heavily loaded microprocessor memory bus, trying to latch an asynchronous signal that is valid for only a few nanoseconds is very difficult. Even providing a new address every 35 nanoseconds requires large address drivers which create significant amounts of electrical noise within the system. To increase the data throughput of a memory system, it has been common practice to place multiple devices on a common bus. For example, two fast page mode DRAMs may be connected to common address and data buses. One DRAM stores data for odd addresses, and the other for even addresses. The CAS* signal for the odd addresses is turned off (high) when the CAS* signal for the even addresses is turned on (low). This interleaved memory system provides data access at twice the rate of either device alone. If the first CAS* is low for 20nanoseconds and then high for 20 nanoseconds while the second CAS* goes low, data can be accessed every 20 nanoseconds or 50 megahertz, If the access time from CAS* to data valid is fifteen nanoseconds, the data will be valid for only five nanoseconds at the end of each 20 nanosecond period when both devices are operating in fast page mode. As cycle times are shortened, the data valid period goes to zero.

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead, data is held valid after CAS* goes high until sometime after the next CAS* low pulse occurs, or until RAS* or the output enable (OE*) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can be a complex function of when the column address inputs are valid, when CAS* falls, the state of OE* and when CAS* rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially CAS*) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM manufacturers.

Yet another type of memory device is a burst EDO memory which adds the ability to address one column of a memory array and then automatically address additional columns in a pre-determined manner without providing the additional column addresses on external address lines. These memory devices use a column access input to access the memory array columns. For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a memory device which can operate at high data rates in a clocked or synchronous manner.

SUMMARY OF THE INVENTION

The above mentioned problems with memory devices and other problems are addressed by the present invention and which will be understood by reading and studying the following specification. A memory device is described which uses a clock signal to synchronize a burst access memory.

In particular one embodiment of the present invention is a memory device comprising a plurality of addressable memory elements, and addressing circuitry. The addressing circuitry is adapted to receive a first memory element address in response to a transition of a clock signal and an address latch signal, and further adapted to generate a second memory element address in response to a subsequent transition of the clock signal.

In another embodiment, a synchronous memory device is described. This memory comprises a memory array having a plurality of addressable memory elements, a plurality of address inputs for receiving memory element addresses, and an address latch input for receiving an address latch signal. The memory also includes an address latch for receiving a first memory element address in response to a transition of a clock signal and the address latch signal, and an address generation circuit responsive to successive transitions of the clock signal and to the first memory element address for generating additional memory element addresses.

In yet another embodiment, a method of accessing a memory device is described. The method comprises the steps of receiving a first memory element address in response to a transition of a clock signal and an address latch signal, and generating additional memory element addresses in response to subsequent transitions of the clock signal.

In still another embodiment, a method of burst accessing a memory device is described. The method comprising the steps of receiving a first memory element address in response to a transition of a clock signal and an address latch signal, accessing first memory elements having the first memory element address, generating additional memory element addresses in response to subsequent transitions of the clock signal, and accessing additional memory elements having the additional memory element addresses.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a memory device incorporating burst access;

FIG. 2 illustrates linear and interleaved addressing sequences for the device of FIG. 1;

FIG. 3 is a timing diagram of a burst read followed by a burst write of the device of FIG. 1;

FIG. 4 is a timing diagram of a burst write followed by a burst read of the device of FIG. 1;

FIG. 5 is a block diagram of a memory device incorporating the features of the present invention;

FIG. 6 is a timing diagram of the operation of the device of FIG. 5; and

FIG. 7 is another timing diagram of the operation of the device of FIG. 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present inventions is defined only by the appended claims.

FIG. 1 is a schematic representation of a sixteen megabit device designed to operate in a burst access mode. The device is organized as a 2 Meg×8 burst EDO DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array 12. An active-low row address strobe (RAS*) signal 14 is used to latch a first portion of a multiplexed memory address, from address inputs A0 through A10 16, in latch 18. The latched row address 20 is decoded in row decoder 22. The decoded row address is used to select a row of the memory array 12. An active-low column address strobe (CAS*) signal 24 is used to latch a second portion of a memory address from address inputs 16 into column address counter 26. The latched column address 28 is decoded in column address decoder 30. The decoded column address is used to select a column of the memory array 12.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 32 to output latches 34. Data 10 driven from the burst EDO DRAM may be latched external to the device in synchronization with a clock signal after a predetermined number of clock cycle delays (latency). For a two cycle latency design, the first clock rising edge during a CAS* cycle is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second clock falling edge, and remains valid through the third clock falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during clock high intervals dependent on the state of the output enable and write enable (OE* and WE*) control lines, thus allowing additional time for the system to latch the output data. Once a row and a column address are selected, additional transitions of the clock signal are used to advance the column address within the column address counter in a predetermined sequence. The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the clock signal provided that OE* is maintained low, and WE* remains high. The output data signal levels may be driven in accordance with standard CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. FIG. 2 is a table which shows linear and interleaved addressing sequences for burst lengths of 2, 4 and 8 cycles. The "V" for starting addresses A1 and A2 in the table represent address values that remain unaltered through the burst sequence. The column address may be advanced with each clock transition, or each pulse. When the address is advanced with each transition of the clock signal, data is also driven from the part after each transition following the device latency which is then referenced to each edge of the clock signal. This allows for a burst access cycle where the clock toggles only once (high to low or low to high) for each memory cycle. This is in contrast to standard DRAMs which require CAS* to go low and then high for each cycle, and synchronous DRAMs which require a full clock cycle (high and low transitions) for each memory cycle.

It may be desirable to latch and increment the column address after the first clock falling edge in order to apply both the latched and incremented addresses to the array at the earliest opportunity in an access cycle. For example, a device may be designed to access two data words per cycle (prefetch architecture). The memory array for a prefetch architecture device may be split into odd and even array halves. The column address least significant bit is then used to select between odd and even halves while the other column address bits select a column within each of the array halves. In an interleaved access mode with column address 1, data from columns 0 and 1 would be read and the data from column 1 would be output followed by the data from column 0 in accordance with standard interleaved addressing as described in SDRAM specifications. In a linear access mode column address 1 would be applied to the odd array half, and incremented to address 2 for accessing the even array half to fulfill the two word access. One method of implementing this type of device architecture is to provide a column address incrementing circuit between the column address counter and the even array half. The incrementing circuit would increment the column address only if the initial column address in a burst access cycle is odd, and the

address mode is linear. Otherwise the incrementing circuit would pass the column address unaltered. For a design using a prefetch of two data accesses per cycle, the column address would be advanced once for every two active edges of the clock signal. Prefetch architectures where more than two data words are accessed are also possible.

In the burst access memory device, each new column address from the column address counter is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16. This burst sequence of data will continue for each clock falling edge until a predetermined number of data accesses equal to the burst length has occurred. A clock falling edge received after the last burst address has been generated will latch another column address from the address inputs 16 if CAS* is low and a new burst sequence will begin. Read data is latched and output with each falling edge of clock after the first clock latency. For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the clock signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is preferred. Additional input data words for storage at incremented column address locations are latched by clock on successive clock pulses. Input data from the input latches 34 is passed along data path 32 to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes will occur without the requirement of additional column addresses being provided on the address lines 16. After the predetermined number of burst writes has occurred, a subsequent CAS* with a clock pulse will latch a new beginning column address, and another burst read or write access will begin.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by clock. WE* low at the column address latch time selects a burst write access. WE* high at the column address latch time selects a burst read access. The level of the WE* signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. Transitions of the WE* signal may be locked out during critical timing periods within an access cycle in order to reduce the possibility of triggering a false write cycle. After the critical timing period, the state of WE* will determine whether a burst access continues, is initiated, or is terminated. Termination of a burst access resets the burst length counter and places the DRAM in a state to receive another burst access command. Both RAS* and CAS* going high during a burst access will also terminate the burst access cycle placing the data drivers in a high impedance output state, and resetting the burst length counter. A minimum write enable pulse width is only required when it is desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses. In the case of burst reads, WE* will transition from high to low to terminate a first burst read, and then WE* will transition back high prior to the next falling edge of CAS* in order to specify a new burst read cycle. For burst writes, WE* would transition high to terminate a current burst write access, then back low prior to the next falling edge of CAS* to initiate another burst write access.

A basic implementation of the device of FIG. 1 may include a fixed burst length of 4, a fixed clock latency of 2 and a fixed interleaved sequence of burst addresses. This basic implementation requires very little additional circuitry to the standard EDO page mode DRAM, and may be mass produced to provide the functions of both the standard EDO page mode and burst EDO DRAMs. This device also allows for the output enable pin (OE*) to be grounded for compatibility with many SIMM module designs. When not disabled (tied to ground), OE* is an asynchronous control which will prevent data from being driven from the part in a read cycle if it is inactive (high) prior to CAS* falling and remains inactive beyond CAS* rising. If these setup and hold conditions are not met, then the read data may be driven for a portion of the read cycle. In a preferred embodiment, if OE* transitions high at any time during a read cycle the outputs will remain in a high impedance state until the next falling edge of CAS* despite further transitions of the OE* signal.

The burst access memory has been described with reference to several embodiments. Just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including x1, x4, x8 and x16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the burst access memory device may take the form of many different memory organizations.

FIG. 3 is a timing diagram for performing a burst read followed by a burst write of the device of FIG. 1. In FIG. 3, a row address is latched by the RAS* signal. WE* is low when RAS* falls for an embodiment of the design where the state of the WE* pin is used to specify a burst access cycle at RAS* time. Next, CAS* is driven low with WE* high to initiate a burst read access, and the column address is latched. The data out signals (DQ's) are not driven in the first CAS* cycle. On the second falling edge of the CAS* signal, the internal address generation circuitry advances the column address and begins another access of the array, and the first data out is driven from the device after a CAS* to data access time (tCAC). Additional burst access cycles continue, for a device with a specified burst length of four, until the fifth falling edge of CAS* which latches a new column address for a new burst read access. WE* falling in the fifth CAS* cycle terminates the burst access, and initializes the device for additional burst accesses. The sixth falling edge of CAS* with WE* low is used to latch a new burst address, latch input data and begin a burst write access of the device. Additional data values are latched on successive CAS* falling edges until RAS* rises to terminate the burst access.

FIG. 4 is a timing diagram depicting burst write access cycles followed by burst read cycles. As in FIG. 3, the RAS* signal is used to latch the row address. The first CAS* falling edge in combination with WE* low begins a burst write access with the first data being latched. Additional data values are latched with successive CAS* falling edges, and the memory address is advanced internal to the device in either an interleaved or sequential manner. On the fifth CAS* falling edge a new column address and associated write data are latched. The burst write access cycles continue until the WE* signal goes high in the sixth- CAS* cycle. The transition of the WE* signal terminates the burst write access. The seventh CAS* low transition latches a new column address and begins a burst read access (WE* is high). The burst read continues until RAS* rises terminating the burst cycles.

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United States Patent [19]

Merritt et al.

[11] **Patent Number: 5,831,932**

[45] **Date of Patent: *Nov. 3, 1998**

[54] **SELF-ENABLING PULSE-TRAPPING CIRCUIT**

[75] Inventors: **Todd Merritt**, Boise; **Brett Williams**, Eagle, both of Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. Nos. 5,706,247 and 5,640,364.

[21] Appl. No.: **914,659**

[22] Filed: **Aug. 19, 1997**

Related U.S. Application Data

[63] Continuation of Ser. No. 754,308, Nov. 21, 1996, Pat. No. 5,706,247, which is a continuation of Ser. No. 568,358, Dec. 6, 1995, Pat. No. 5,640,364, which is a continuation-in-part of Ser. No. 370,761, Dec. 23, 1994, Pat. No. 5,526,320.

[51] **Int. Cl.**^{6} **G11C 8/00**

[52] **U.S. Cl.** 365/233.5; 365/233; 365/230.08

[58] **Field of Search** 365/233.5, 230.08, 365/238.5, 189.05, 206, 230.06

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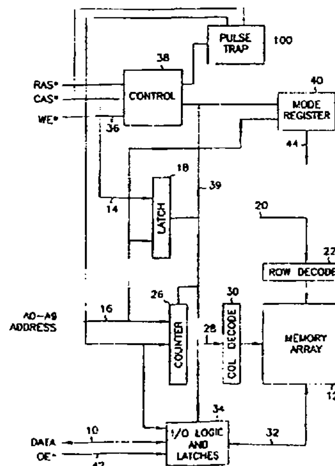
Primary Examiner—Tan T. Nguyen
Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

An integrated circuit memory device is described which can operate at high data speeds. The memory device can either store or retrieve data from the memory in a burst access operation. The burst operations latches a memory address from external address lines and internally generates additional memory addresses. An external input is used to terminate and change a burst operation. Circuitry is provided to monitor the external input during burst operations and provide an appropriate control signal.

23 Claims, 8 Drawing Sheets



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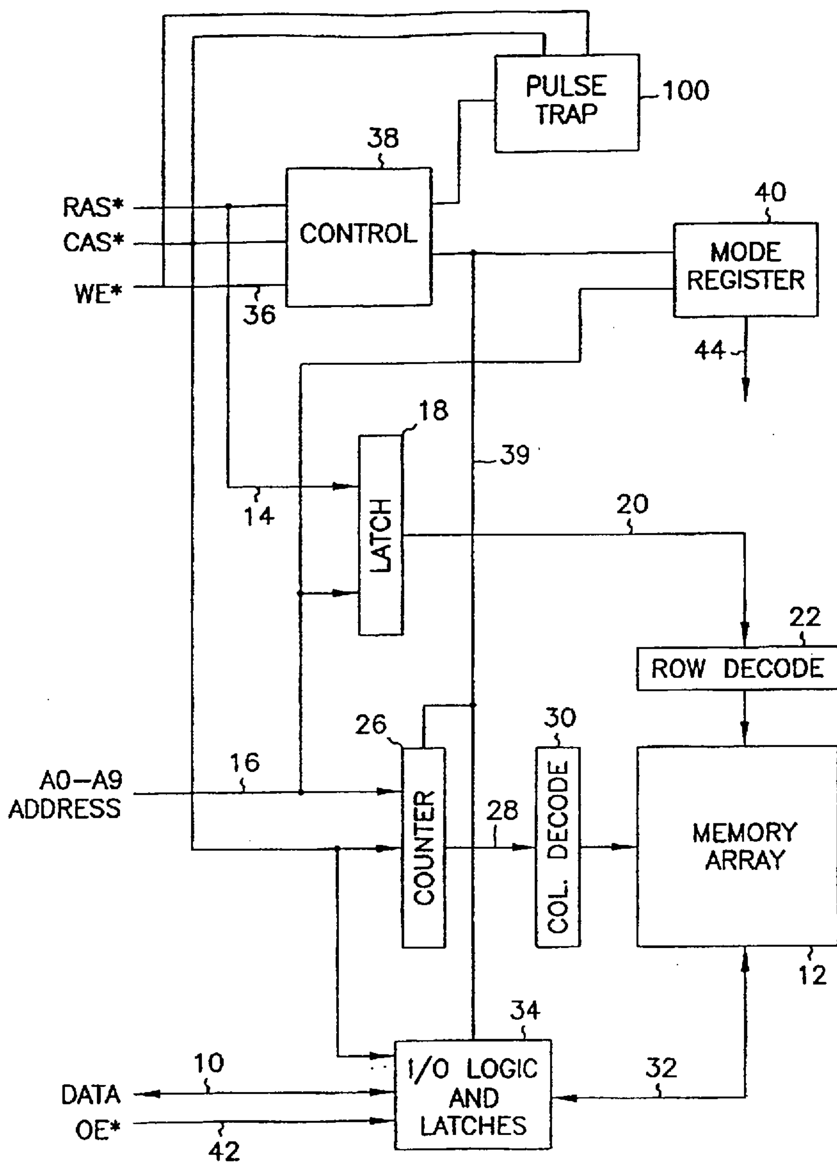

FIG. 1

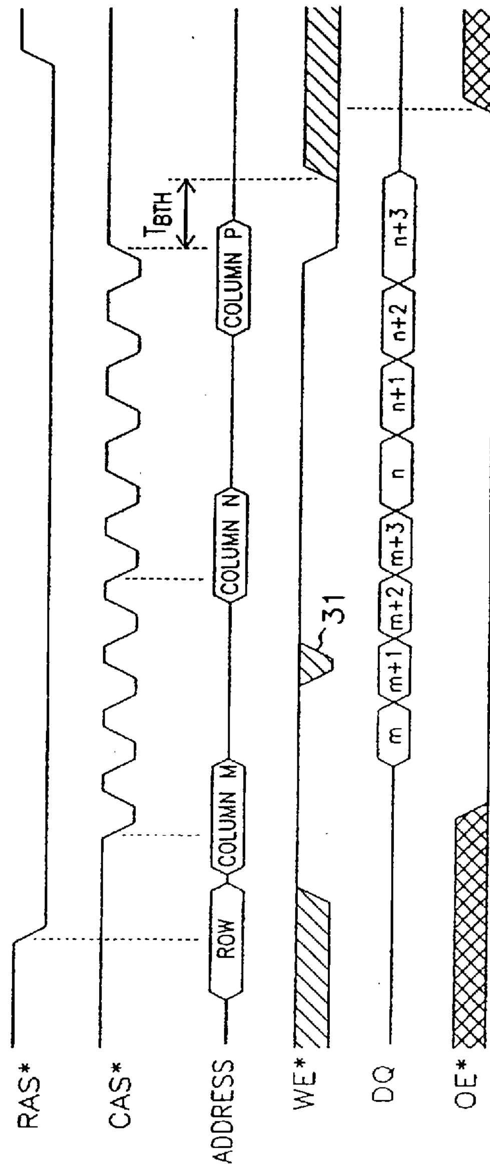

FIG. 2

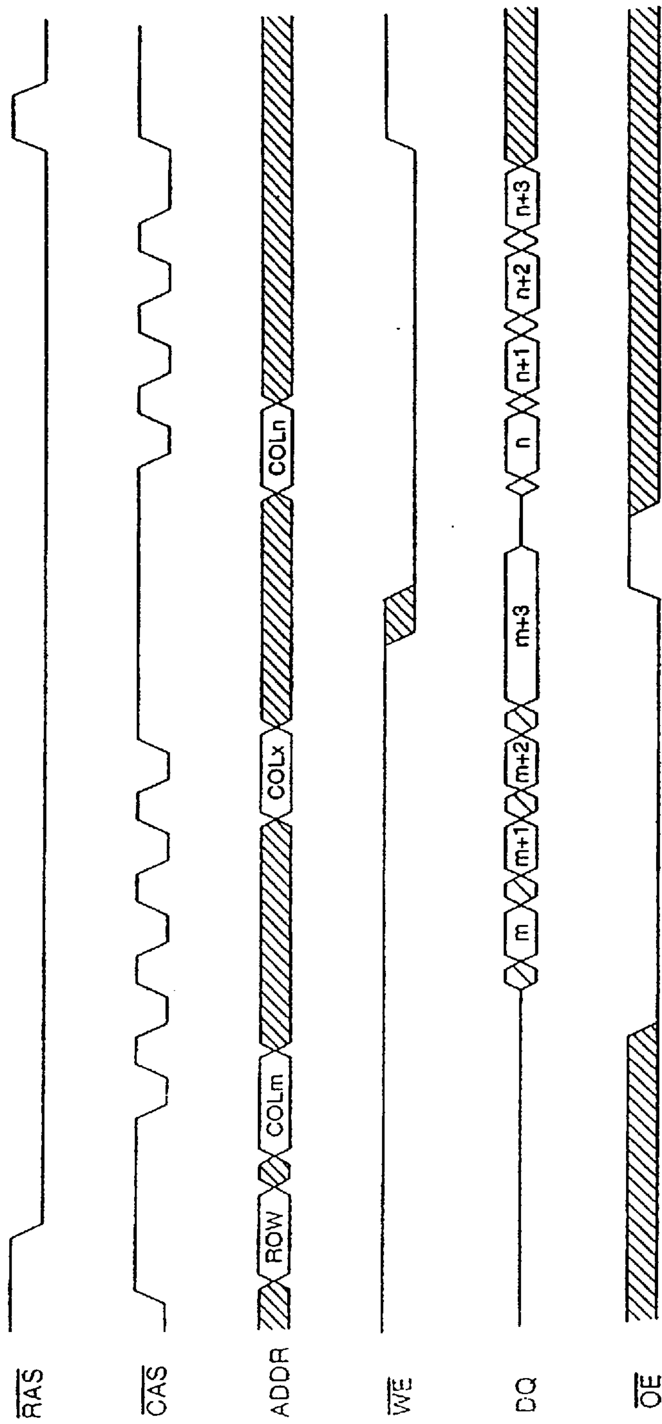

FIG. 3

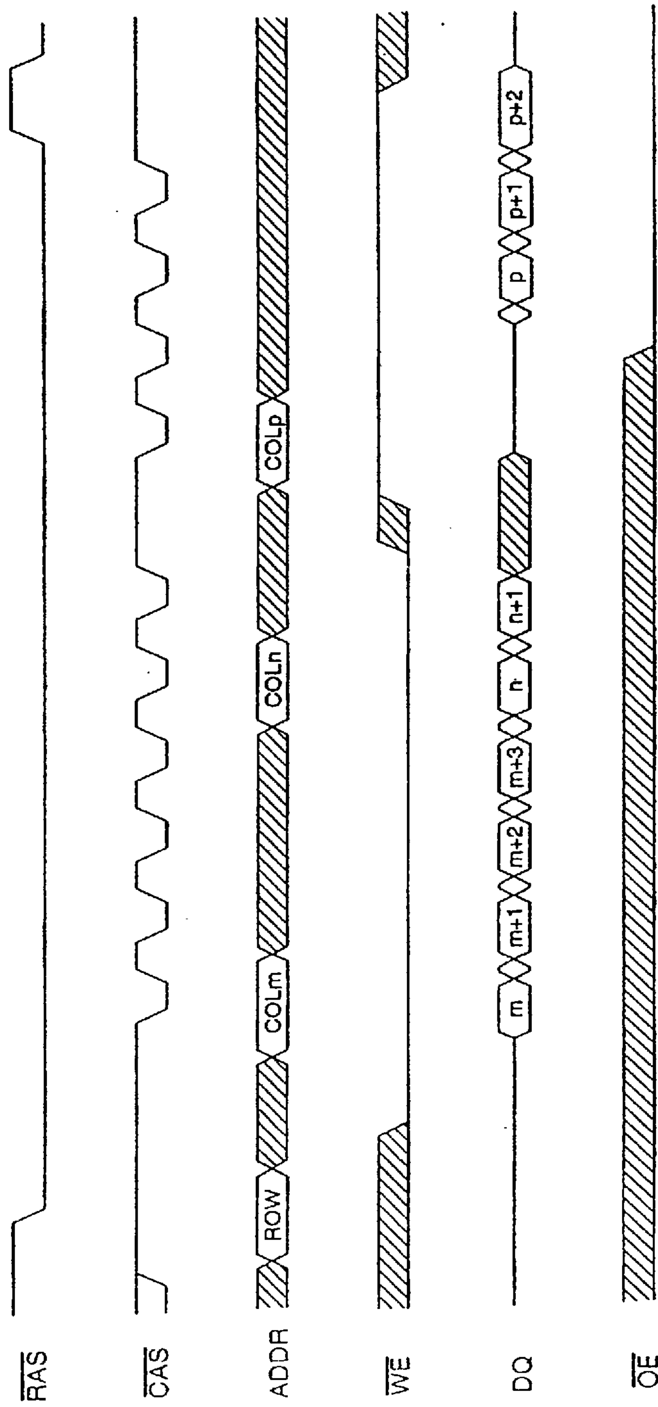

FIG. 4

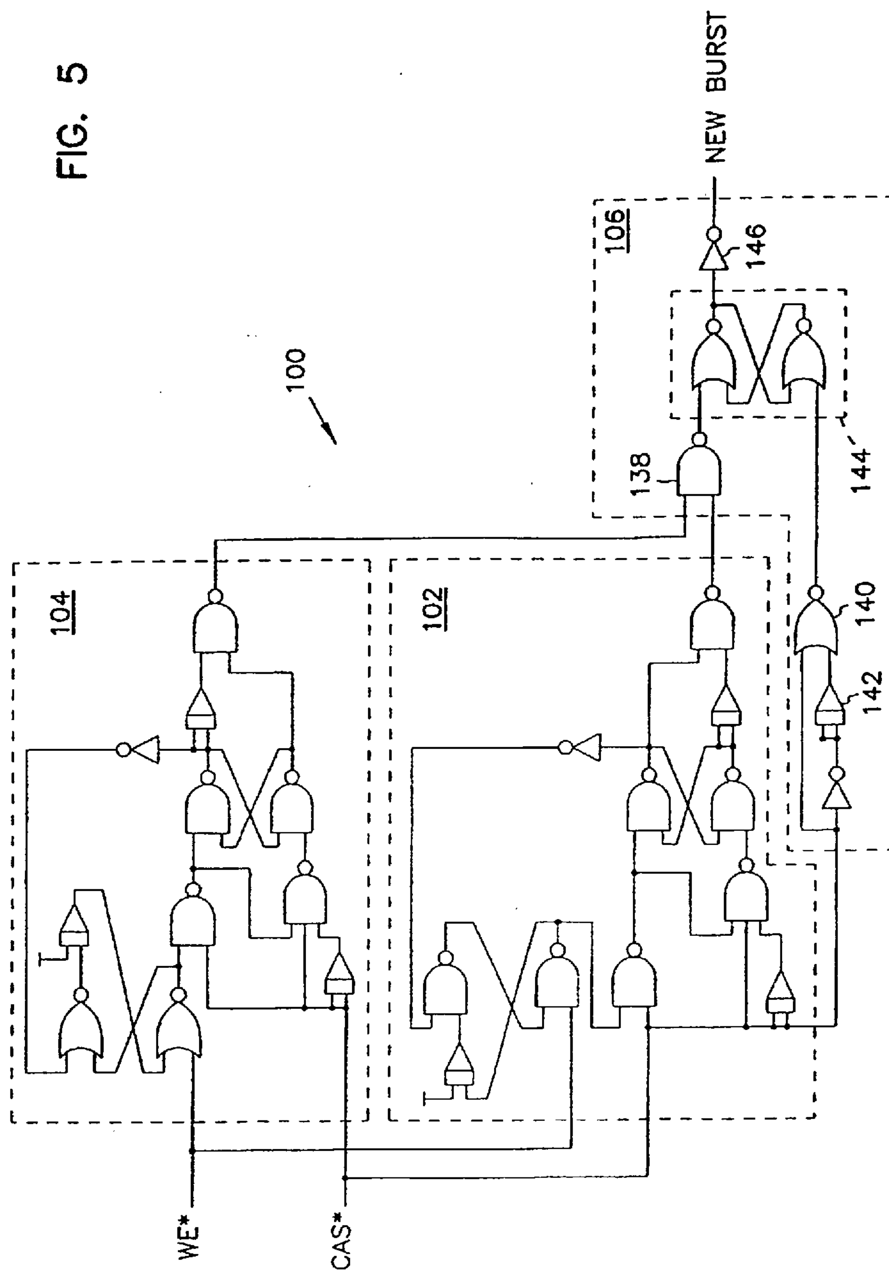
FIG. 5
NEW BURST
106
146
100
138
144
104
102
140
142
WE*
CAS*

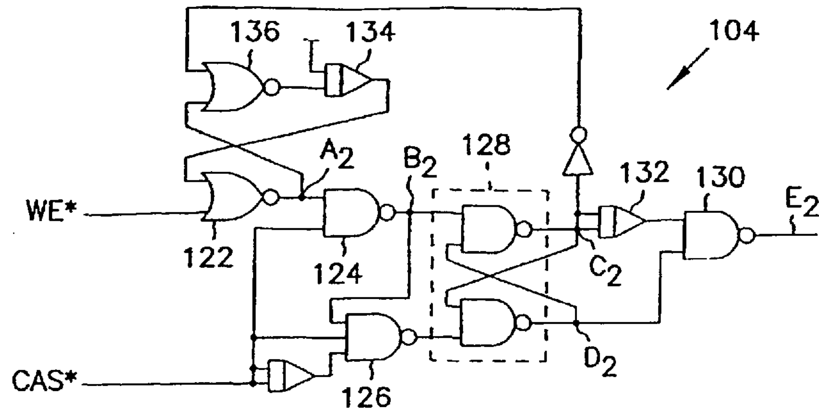

FIG. 6A

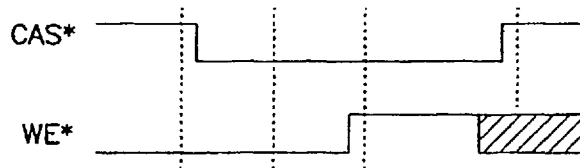

FIG. 6B

WE* CAS*	0 1	0 0	1 0	X 1
A_2	1	1	0	0
B_2	0	1	1	1
C_2	1	1	1	0
D_2	0	0	0	1
E_2	1	1	1	⌐⌊⌐

FIG. 6C

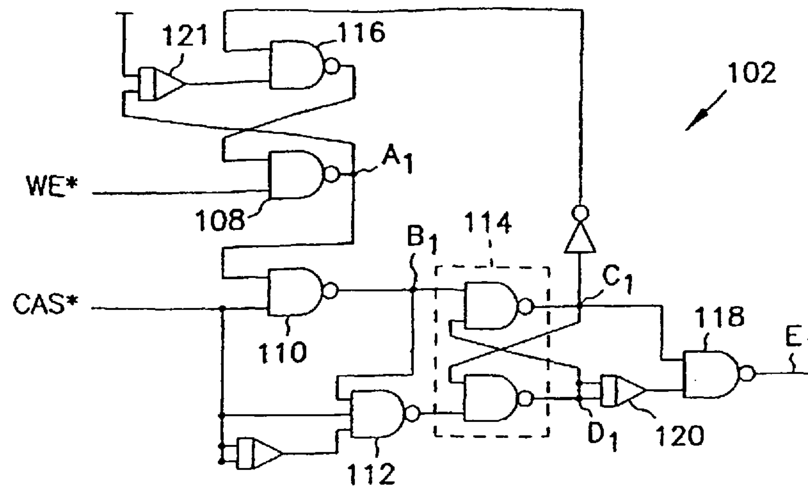

FIG. 7A

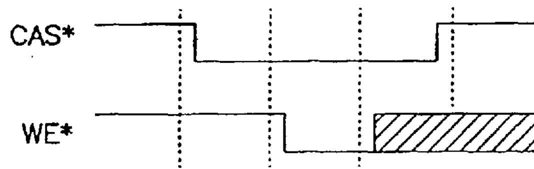

FIG. 7B

WE* CAS*	1 1	1 0	0 0	X 1
A_1	0	0	1	1
B_1	1	1	1	0
C_1	0	0	0	1
D_1	1	1	1	0
E_1	1	1	1	‾_‾

FIG. 7C

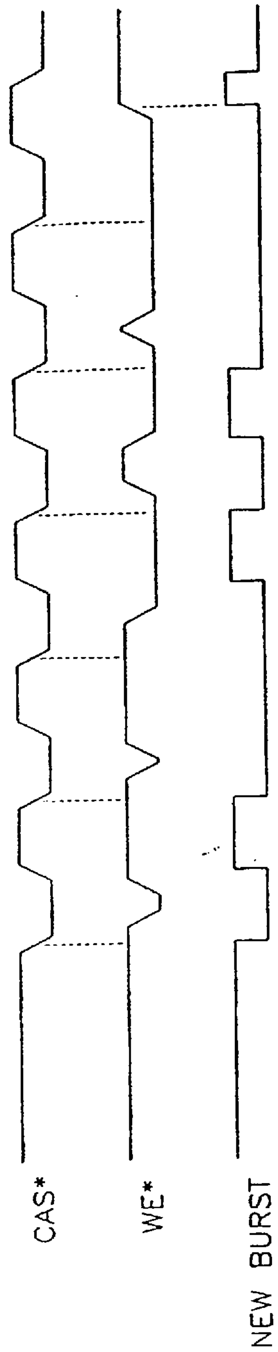

FIG. 8

SELF-ENABLING PULSE-TRAPPING CIRCUIT

This application is a continuation of U.S. patent application Ser. No. 08/754,308, filed Nov. 21, 1996, now U.S. Pat. No. 5,706,247 which is a continuation of Ser. No. 568,358, filed Dec. 6, 1995, now U.S. Pat. No. 5,640,364, issued on Jun. 17, 1997, which is a continuation-in-part of U.S. application Ser. No. 08/370,761, filed Dec. 23, 1994, now U.S. Pat. No. 5,526,320.

TECHNICAL FIELD OF THE INVENTION

The present invention relates generally to integrated circuit memories and in particular the present invention relates to a circuit and method of latching an input signal.

BACKGROUND OF THE INVENTION

There are a number of integrated circuit memories commercially available. For example, dynamic memory circuits having memory cells arranged to be accessed in a random fashion are referred to as dynamic random access memories, DRAMs. These memories can be produced in a variety of designs which provide different methods of reading from and writing to the dynamic memory cells. One such method is page mode operations. Page mode operations in a DRAM are defined by the method of accessing a row of a memory cell array and randomly accessing different columns of the array. Data stored at the row and column intersection can be output while that column is accessed. An alternate type of memory access is the extended data output (EDO) memory which allows data stored at a memory array address to be available as output after the addressed column has been closed. A more detailed description of a DRAM having EDO features is provided in the "1995 DRAM Data Book" pages 1-1 to 1-30 available from Micron Technology, Inc. Boise, Idaho, the assignee of the present application and is incorporated herein by reference. Yet another type of operation is included in a burst EDO memory which adds the ability to address one column of a memory array and then automatically address additional columns in a pre-determined manner without providing the additional column addresses on external address lines.

In a burst memory, external inputs can be used to terminate a burst access operation. Timing and pulse width requirements are traditionally placed on signals provided on these external inputs. If the minimum timing or pulse width requirements placed on the external inputs are excessive, an error can occur when a short pulse width signal is provided on the input and a burst operation will not be terminated. For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a circuit which can monitor external inputs by reducing critical timing and substantially independent of signal pulse width.

SUMMARY OF THE INVENTION

The above mentioned problems with memory devices and other problems are addressed by the present invention and which will be understood by reading and studying the following specification. A latching circuit is described which monitors an external input for transitions during a burst access operation.

In particular, one embodiment of the present invention describes an integrated memory device comprising a control signal input for receiving a control signal, an address latch input for receiving an address latch signal, and a signal trapping circuit coupled to the control signal input and the address latch input and adapted to latch a transition in the control signal. The signal trapping circuit can comprise a low transition latch circuit to latch a high to low transition in the control signal when the address latch signal is activated, and a high transition latch circuit to latch a low to high transition in the control signal when the address latch signal is activated.

In another embodiment, an integrated memory circuit is described which can comprise a write enable input for receiving a write enable signal, an address latch input for receiving an address latch signal, and a signal trapping circuit coupled to the write enable input and the address latch input and adapted to latch a transition in the write enable signal. The signal trapping circuit comprises a low transition latch circuit to latch a high to low transition in the write enable signal when the address latch input is activated, a high transition latch circuit to latch a low to high transition in the write enable signal when the address latch input is activated, and a pulse generator circuit coupled to the low transition latch circuit and the high transition latch circuit to generate a pulse in response to an output of the low transition latch circuit and the high transition latch circuit.

In yet another embodiment, a method is described for latching a control signal in a memory circuit having a control signal input and an address latch input. The method comprises the steps of receiving an address latch signal on the address latch input, receiving a control signal on the control signal input, enabling a latch circuit in response to an active transition of the address latch signal, and latching a transition of the control signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a memory circuit incorporating the features of the present invention;

FIG. 2 is a timing diagram of a burst memory not including the features of the present invention;

FIG. 3 is a timing diagram of a burst read followed by burst write operation in the memory if FIG. 1;

FIG. 4 is a timing diagram of burst write access cycles followed by burst read cycles in the memory of FIG. 1;

FIG. 5 is a pulse trapping circuit of FIG. 1;

FIG. *6a* is a low transition latch of the circuit of FIG. 5;

FIG. *6b* is a timing diagram of the circuit of FIG. *6a;*

FIG. *6c* is a logic table of the timing diagram of FIG. *6b;*

FIG. *7a* is a high transition latch of the circuit of FIG. 5;

FIG. *7b* is a timing diagram of the circuit of FIG. *7a;*

FIG. *7c* is a logic table of the timing diagram of FIG. *7b;* and

FIG. 8 is a timing diagram of the circuit of FIG. 5.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from

the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present inventions is defined only by the appended claims. The present invention can be implemented in any memory, but is particularly advantageous in a burst access memory.

BURST ACCESS MEMORY

FIG. 1 is a schematic representation of a sixteen megabit device designed in accordance with the present invention. The device is organized as a 2 Meg × 8 Burst EDO DRAM having an eight bit data input/output path **10** providing data storage for 2,097,152 bytes of information in the memory array **12**. The device of FIG. 1 may have an industry standard pinout for eight bit wide EDO DRAMs. An active-low row address strobe (RAS*) signal **14** is used to latch a first portion of a multiplexed memory address, from address inputs **16**, in latch **18**. The latched row address **20** is decoded in row decoder **22**. The decoded row address is used to select a row of the memory array **12**. A column address strobe (CAS*) signal **24** is used to latch a second portion of a memory address from address inputs **16** into address generation circuit **26**. The latched column address **28** is decoded in column address decoder **30**. The decoded column address is used to select a column of the memory array **12**.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path **32** to output latches. Data **10** driven from the burst EDO DRAM may be latched external to the device in synchronization with CAS* after a predetermined number of CAS* cycle delays (latency). For a two cycle latency design, the first CAS* falling edge is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second CAS* falling edge, and remains valid through the third CAS* falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers **34** will continue to drive the data lines without tri-stating the data outputs during CAS* high intervals dependent on the state of the output enable and write enable (OE* and WE*) control lines, thus allowing additional time for the system to latch the output data. The data outputs remain valid throughout the burst read cycles with the exception of brief periods of data transition. During these periods of data transition, the output drivers may be turned off momentarily in order to aid data transition. This state of the output buffer should not be confused with the standard DRAM tri-state condition which is intended to release the data bus.

Once a row and a column address are selected, additional transitions of the CAS* signal are used to advance the column address within the address generation circuit in a predetermined sequence. The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the CAS* signal provided that OE* is maintained low, and WE* remains high. The output data signal levels may be but are not limited to being driven in accordance with standard CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

In the burst access memory device, each new column address from the address generation circuit is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs **16**. This burst sequence

of data will continue for each CAS* falling edge until a predetermined number of data accesses equal to the burst length has occurred. A CAS* falling edge received after the last burst address has been generated will latch another column address from the address inputs **16** and a new burst sequence will begin. Read data is latched and output with each falling edge of CAS* after the first CAS* latency.

For a burst write cycle, data **10** is latched in input data latches **34**. Data targeted at the first address specified by the row and column addresses is latched with the CAS* signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is preferred. Additional input data words for storage at incremented column address locations are latched by CAS* on successive CAS* pulses. Input data from the input latches **34** is passed along data path **32** to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes will occur without the requirement of additional column addresses being provided on the address lines **16**. After the predetermined number of burst writes has occurred, a subsequent CAS* pulse will latch a new beginning column address, and another burst read or write access will begin.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by CAS*. WE* low at the column address latch time selects a burst write access. WE* high at the column address latch time selects a burst read access. The level of the signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on WE* within a burst read access will likewise terminate the burst read access and will place the data output **10** in a high impedance state.

In a standard burst access memory device, the WE* signal required a minimum pulse width defined by time T_{BTH} following the rising edge of CAS* to terminate a burst access. For a memory not including the present invention, FIG. 2 illustrates both the minimum pulse width T_{BTH}, and a WE* low pulse **31** which is less that T_{BTH}. After the critical timing period, the state of WE* is used to determine whether a burst access continues, is initiated, or is terminated. A minimum write enable pulse width is only required when it is desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses.

Termination of a burst access places the DRAM in a state to receive another burst access command. Both RAS* and CAS* going high during a burst access will also terminate the burst access cycle and place the data drivers in a high impedance output state. Read data may remain valid at the device outputs if RAS* alone goes high while CAS* is active for compatibility with hidden refresh cycles, otherwise RAS* high alone may be used to terminate a burst access. In the case of burst reads, WE* will transition from high to low to terminate a first burst read, and then WE* will transition back high prior to the next falling edge of CAS* in order to specify a new burst read cycle. For burst writes, WE* would transition high to terminate a current burst write access, then back low prior to the next falling edge of CAS* to initiate another burst write access. A basic implementation of the device of FIG. 1 may include a fixed burst length of 4, a fixed CAS* latency of 2 and a programmable sequence of burst addresses.

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United States Patent [19]

Ong et al.

[11] **Patent Number: 5,850,368**

[45] **Date of Patent: *Dec. 15, 1998**

[54] **BURST EDO MEMORY ADDRESS COUNTER**

[75] Inventors: **Adrian E. Ong**, San Jose, Calif.; **Paul S. Zagar**, Woodinville, Wash.; **Brett L. Williams**, Eagle; **Troy A. Manning**, Meridian, both of Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[*] Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,675,549.

[21] Appl. No.: **922,194**

[22] Filed: **Sep. 2, 1997**

Related U.S. Application Data

[63] Continuation of Ser. No. 457,651, Jun. 1, 1995, Pat. No. 5,675,549.

[51] **Int. Cl.**[6] **G11C 8/00**

[52] **U.S. Cl.** **365/238.5**; 365/236

[58] **Field of Search** 365/238.5, 236, 365/235, 230.08

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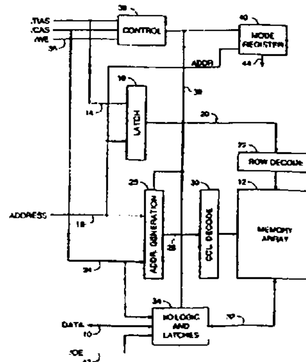
Primary Examiner—Tan T. Nguyen
Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.

[57] **ABSTRACT**

A counter comprised of two flip flops and a multiplexer produces a sequential or interleaved address sequence. The addresses produced are used to access memory elements in a Burst Extended Data Output Dynamic Random Access Memory (Burst EDO or BEDO DRAM). Input addresses in combination with a sequence select signal are logically combined to produce a multiplexer select input which selects between true and compliment outputs of a first flip flop to couple to an input of a second flip flop to specify a toggle condition for the second flip flop. Outputs of the counter are compared with outputs of an input address latch to detect the end of a burst sequence and initialize the device for another burst access. A transition of the Read/Write control line during a burst access will terminate the burst access and initialize the device for another burst access.

17 Claims, 12 Drawing Sheets



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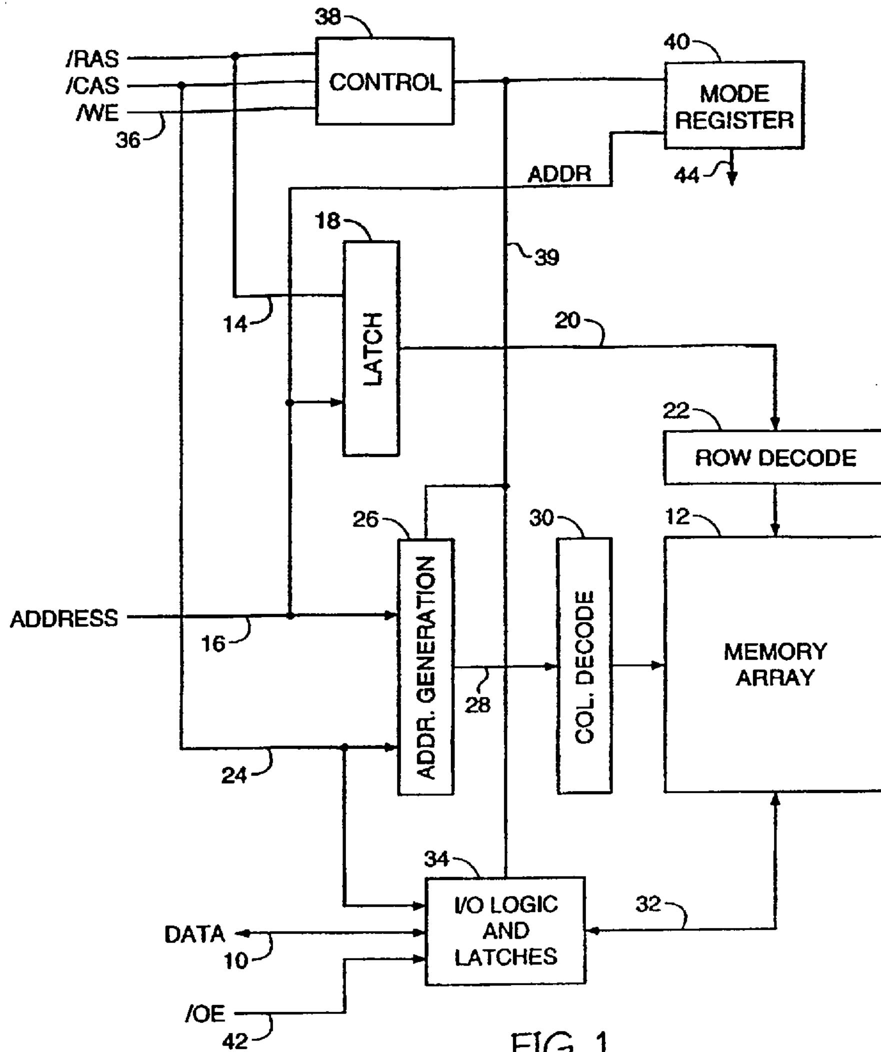

FIG. 1

Burst Length	Starting Column Address			Linear	Interleave
	A_2	A_1	A_0		
2	V	V	0	0-1	0-1
	V	V	1	1-0	1-0
4	V	0	0	0-1-2-3	0-1-2-3
	V	0	1	1-2-3-0	1-0-3-2
	V	1	0	2-3-0-1	2-3-0-1
	V	1	1	3-0-1-2	3-2-1-0
8	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

FIG. 2

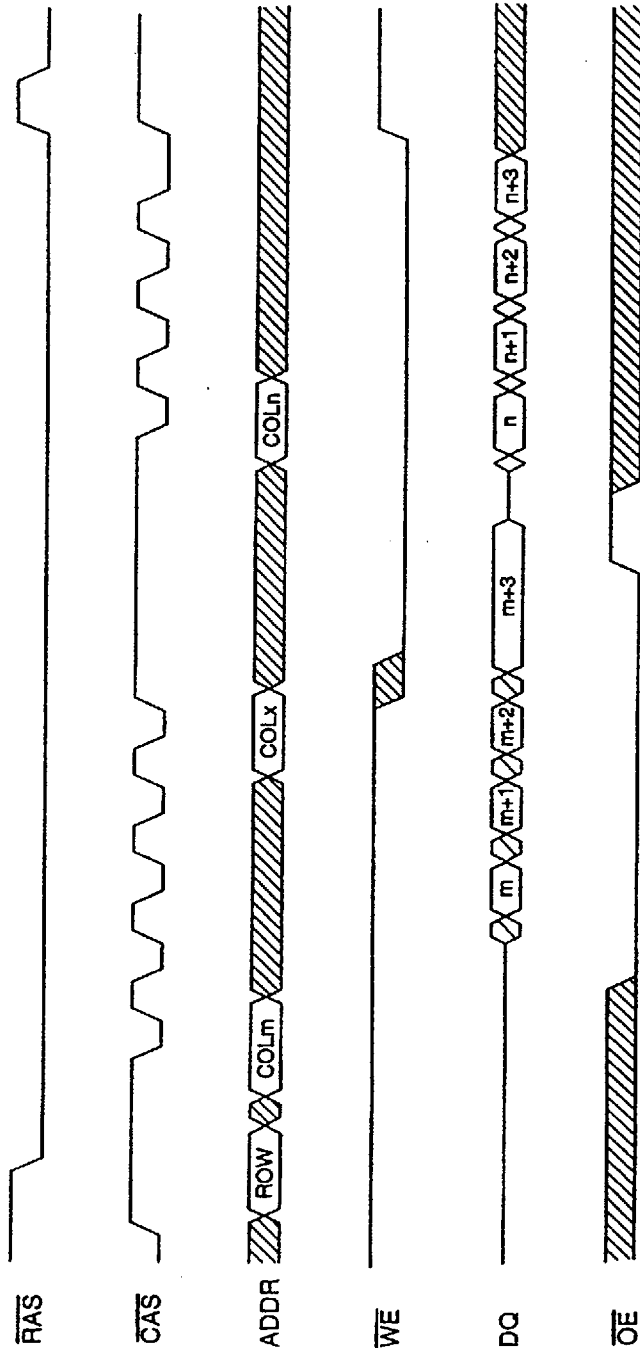

FIG. 3

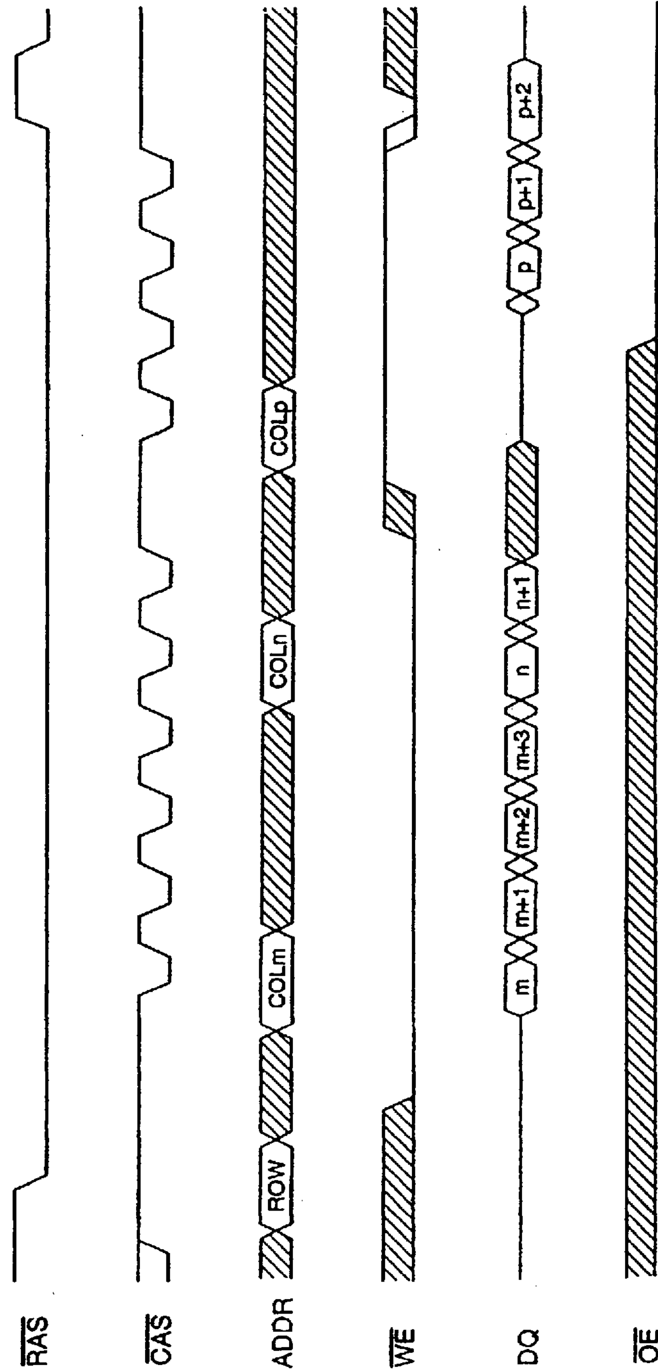

FIG. 4

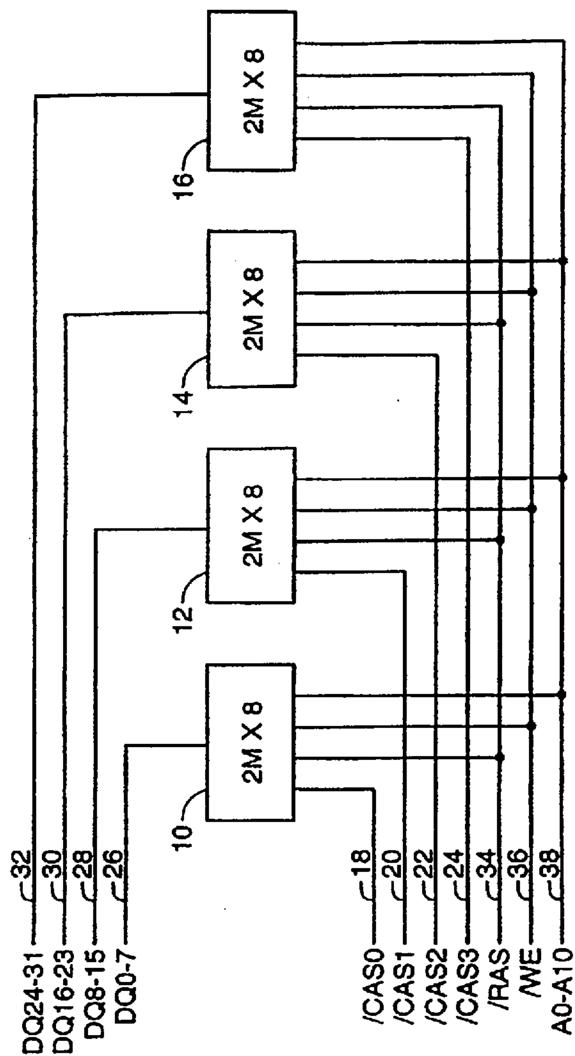

FIG. 5

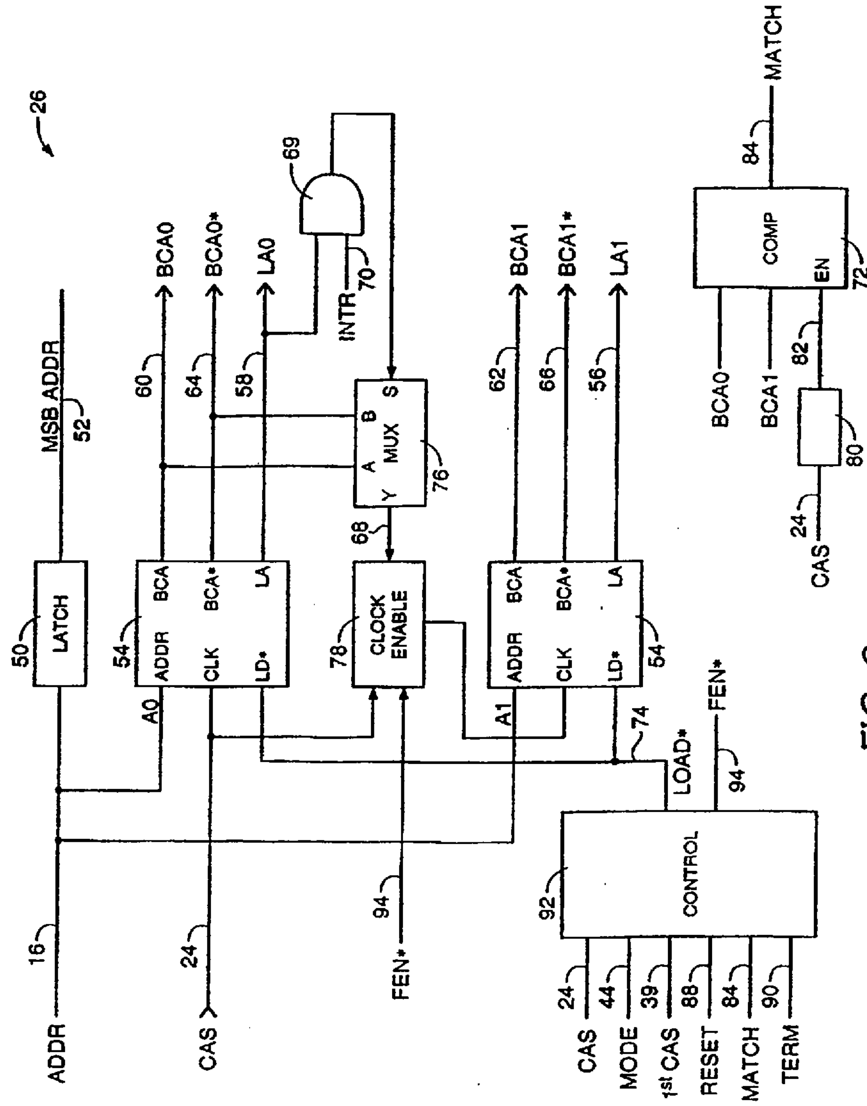

FIG. 6

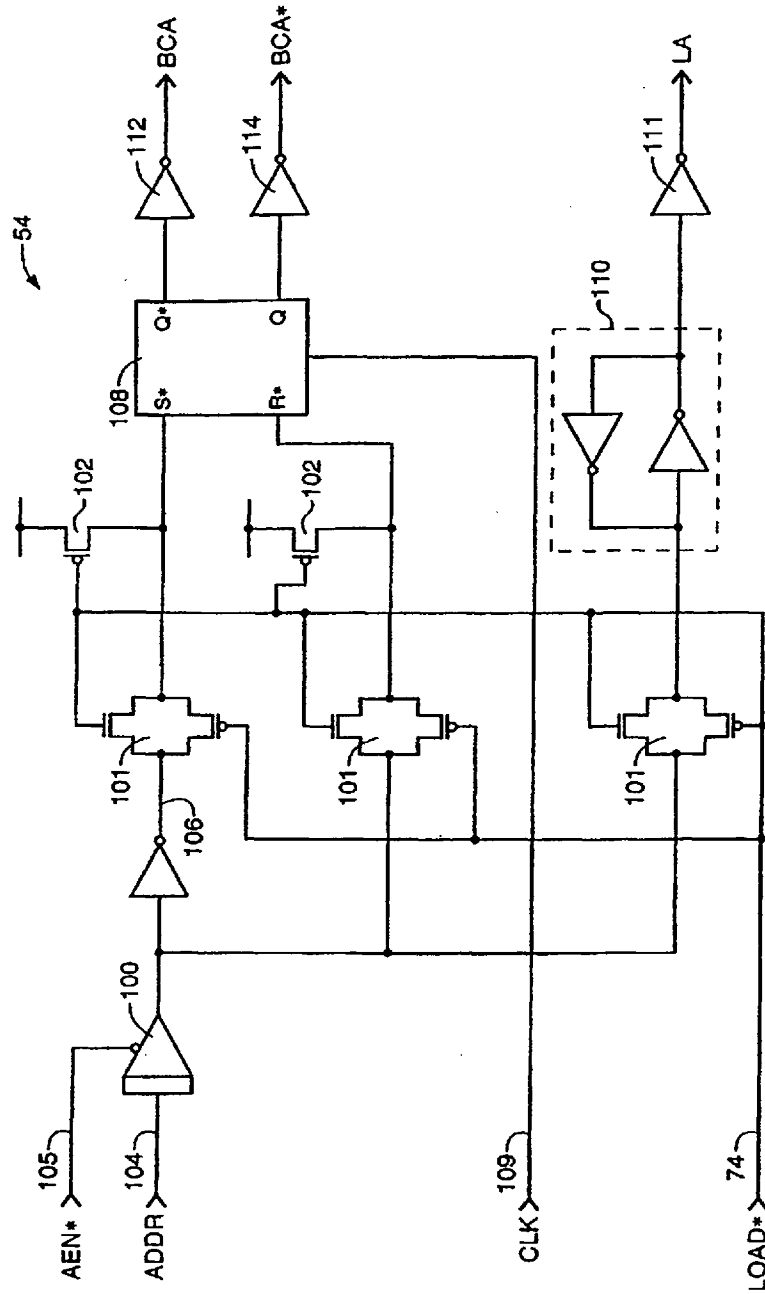

FIG. 7

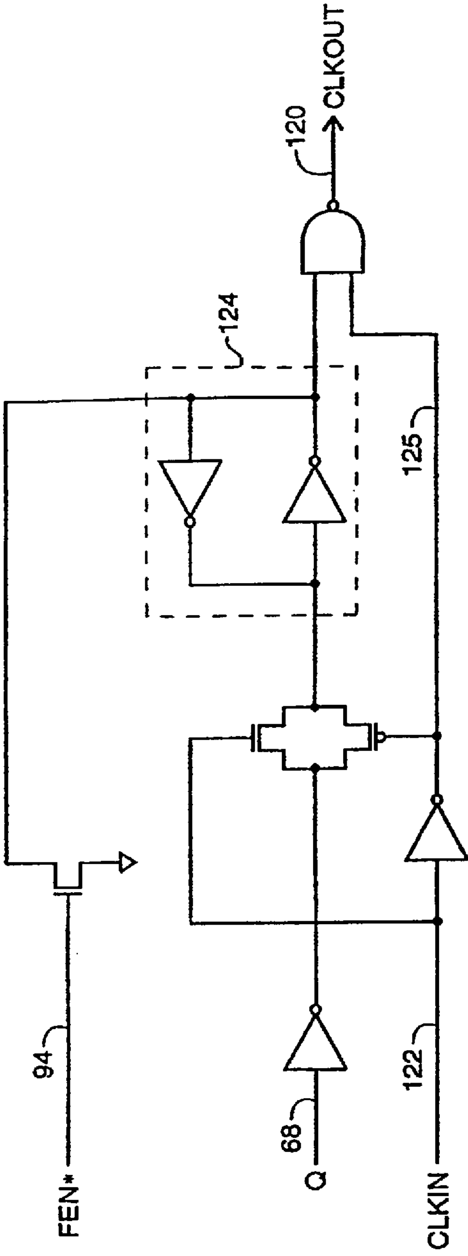

FIG. 8

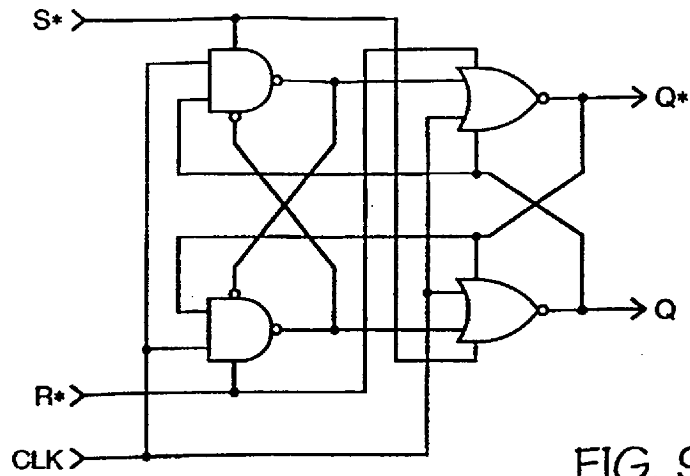

FIG. 9

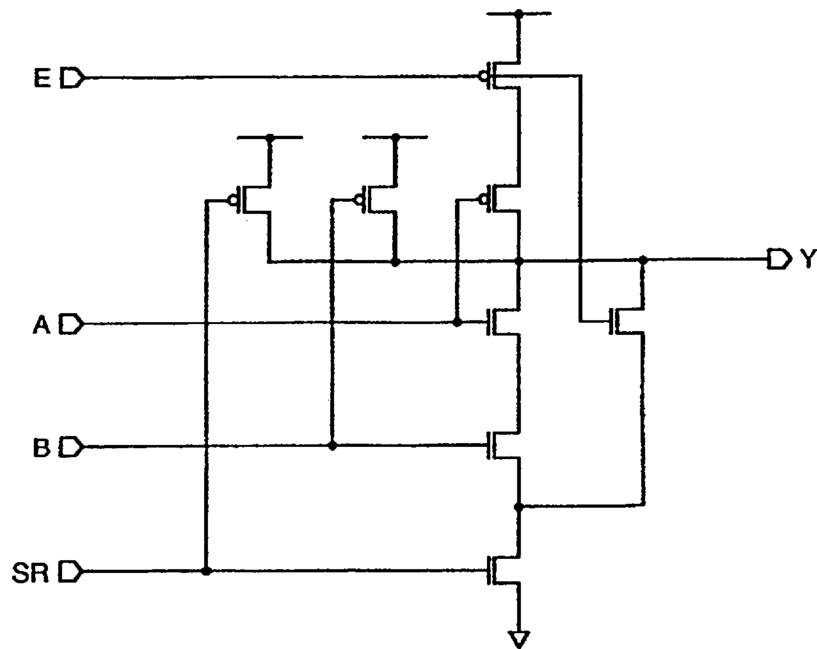

FIG. 10

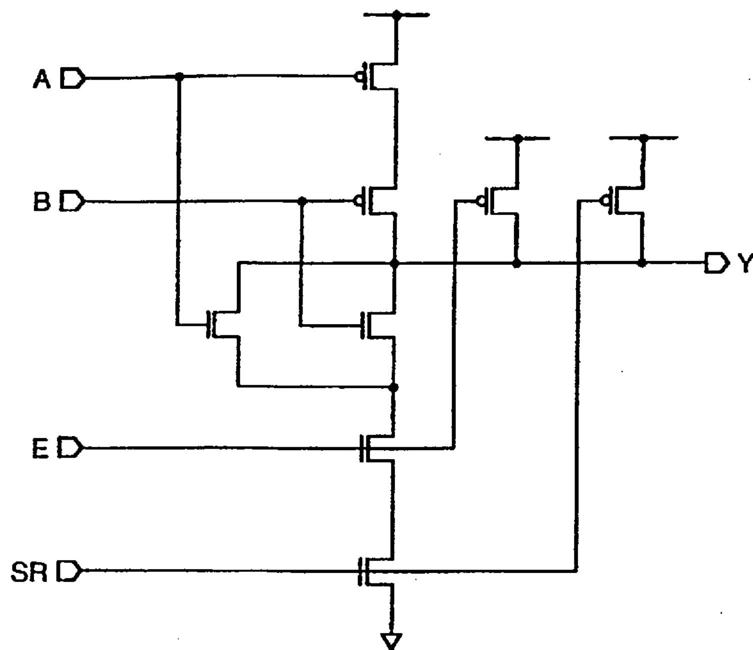

FIG. 11

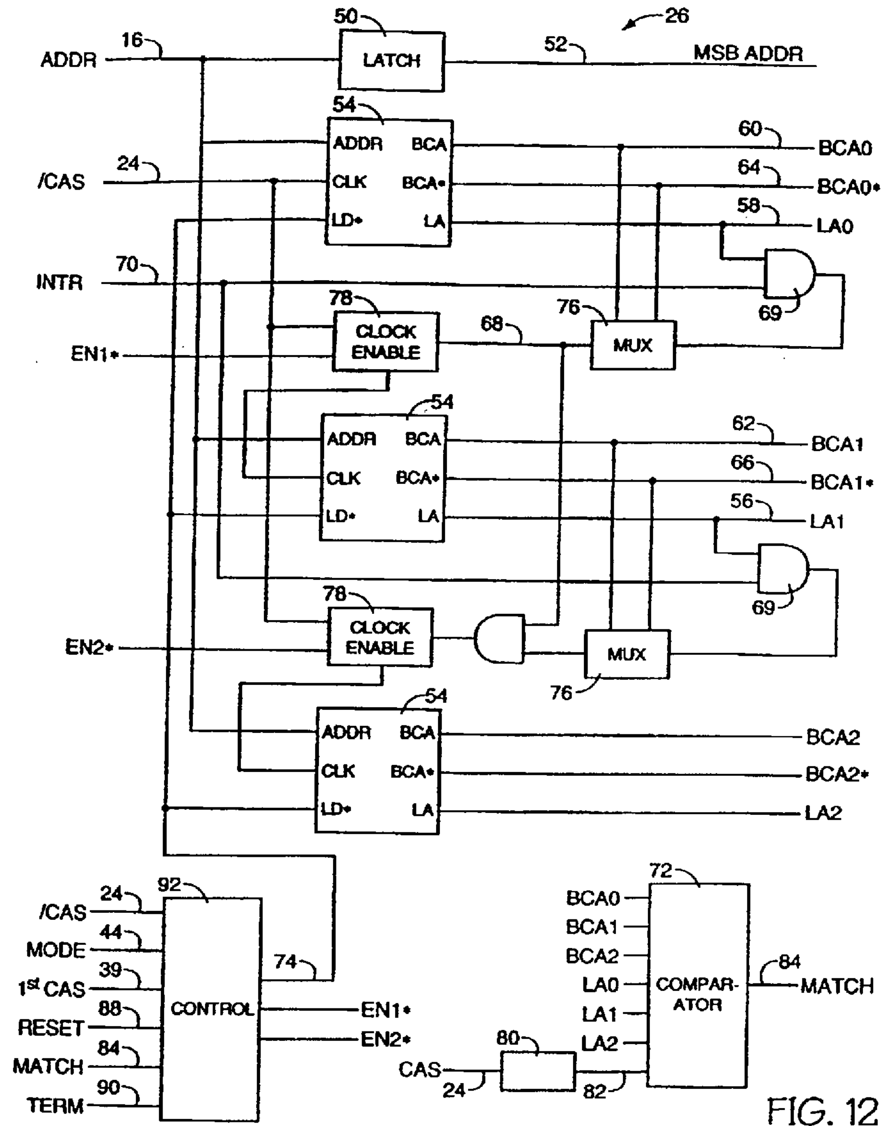

FIG. 12

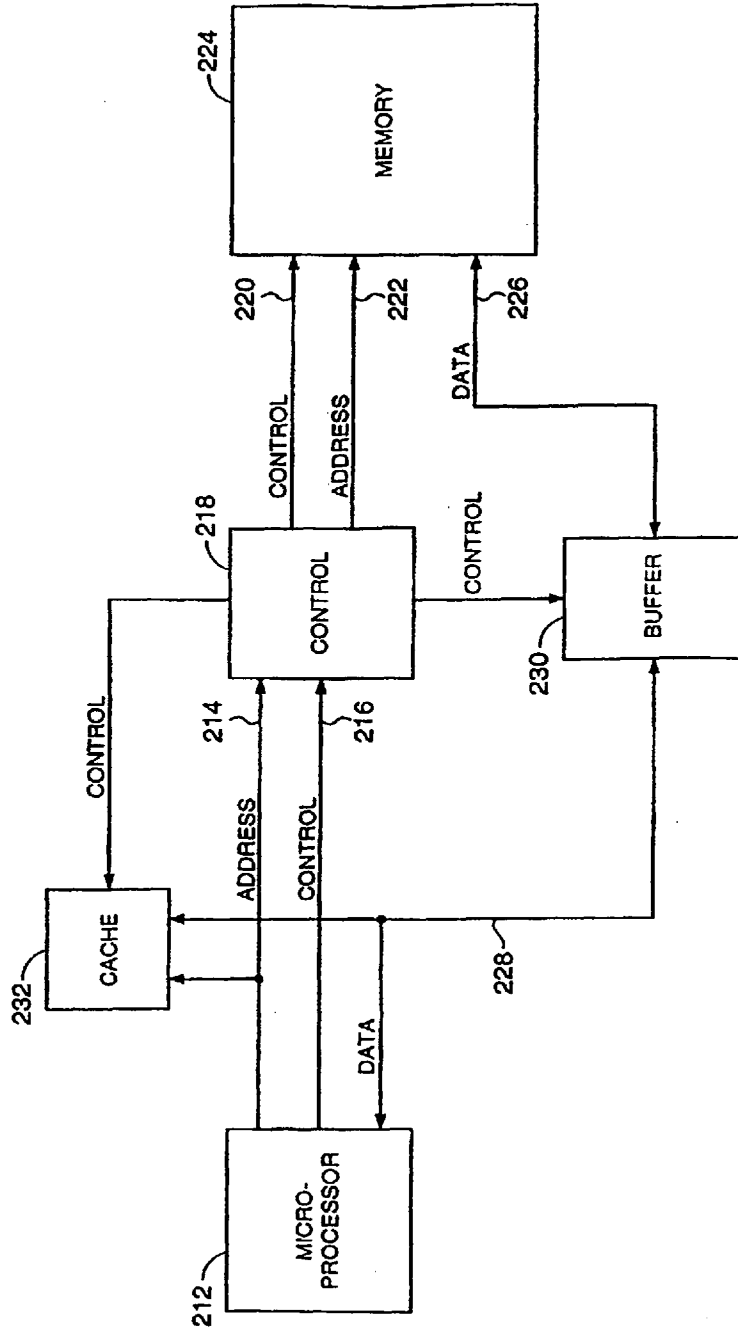

FIG. 13

BURST EDO MEMORY ADDRESS COUNTER

This application is a continuation of U.S. patent application Ser. No. 08/457,651, filed Jun. 1, 1995, now U.S. Pat. No. 5,675,549.

FIELD OF THE INVENTION

This invention relates to internal address generation circuits and counters for memory devices with burst access capability, and methods of accessing burst access memory devices.

BACKGROUND OF THE INVENTION

Dynamic Random Access Memory devices (DRAMs) are among the highest volume and most complex integrated circuits manufactured today. Except for their high volume production, the state of the art manufacturing requirements of these devices would cause them to be exorbitantly priced. Yet, due to efficiencies associated with high volume production, the price per bit of these memory devices is continually declining. The low cost of memory has fueled the growth and development of the personal computer. As personal computers have become more advanced, they in turn have required faster and more dense memory devices, but with the same low cost of the standard DRAM. Fast page mode DRAMs are the most popular standard DRAM today. In fast page mode operation, a row address strobe (/RAS) is used to latch a row address portion of a multiplexed DRAM address. Multiple occurrences of the column address strobe (/CAS) are then used to latch multiple column addresses to access data within the selected row. On the falling edge of /CAS an address is latched, and the DRAM outputs are enabled. When /CAS transitions high the DRAM outputs are placed in a high impedance state (tri-state). With advances in the production of integrated circuits, the internal circuitry of the DRAM operates faster than ever. This high speed circuitry has allowed for faster page mode cycle times. A problem exists in the reading of a DRAM when the device is operated with minimum fast page mode cycle times. /CAS may be low for as little as 15 nanoseconds, and the data access time from /CAS to valid output data (tCAC) may be up to 15 nanoseconds; therefore, in a worst case scenario with the device operating at minimum cycle times, there is no time to latch the output data external to the memory device. For devices with tCAC as low as 10 nanoseconds, the data is still only valid for a few nanoseconds. On a heavily loaded microprocessor memory bus, trying to latch an asynchronous signal that is only valid for a few nanoseconds is very difficult. Even providing a new address every 35 nanoseconds requires large address drivers which create significant amounts of electrical noise within the system.

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead, data is held valid after /CAS goes high until sometime after the next /CAS low pulse occurs, or until /RAS or the output enable (/OE) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can be a complex function of when the column address inputs are valid, when /CAS falls, the state of /OE and when /CAS rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially /CAS) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM manufacturers.

Methods to shorten memory access cycles tend to require additional circuitry, additional control pins and nonstandard device pinouts. The proposed industry standard synchronous DRAM (SDRAM) for example has an additional pin for receiving a system clock signal. Since the system clock is connected to each device in a memory system, it is highly loaded, and it is always toggling circuitry in every device. SDRAMs also have a clock enable pin, a chip select pin and a data mask pin. Other signals which appear to be similar in name to those found on standard DRAMs have dramatically different functionality on a SDRAM. The addition of several control pins has required a deviation in device pinout from standard DRAMs which further complicates design efforts to utilize these new devices. Significant amounts of additional circuitry are required in the SDRAM devices which in turn result in higher device manufacturing costs.

In order for existing computer systems to use an improved device having a nonstandard pinout, those systems must be extensively modified. Additionally, existing computer system memory architectures are designed such that control and address signals may not be able to switch at the frequencies required to operate the new memory device at high speed due to large capacitive loads on the signal lines. The Single In-Line Memory Module (SIMM) provides an example of what has become an industry standard form of packaging memory in a computer system. On a SIMM, all address lines connect to all DRAMs. Further, the row address strobe (/RAS) and the write enable (/WE) are often connected to each DRAM on the SIMM. These lines inherently have high capacitive loads as a result of the number of device inputs driven by them. SIMM devices also typically ground the output enable (/OE) pin making /OE a less attractive candidate for providing extended functionality to the memory devices.

There is a great degree of resistance to any proposed deviations from the standard SIMM design due to the vast number of computers which use SIMMs. Industry's resistance to radical deviations from the standard, and the inability of current systems to accommodate new memory devices such as SDRAMs will delay their widespread acceptance. Therefore only limited quantities of devices with radically different architectures will be manufactured initially. This limited manufacture prevents the reduction in cost which typically can be accomplished through the manufacturing improvements and efficiencies associated with a high volume product.

SUMMARY OF THE INVENTION

An integrated circuit memory device with a standard DRAM pinout is designed for high speed data access and for compatibility with existing memory systems. A high speed burst mode of operation is provided where multiple sequential accesses occur following a single column address, and read data is output relative to the /CAS control signal. In the burst mode of operation the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at high speeds. Only one control

line per memory chip (/CAS) must toggle at the operating frequency in order to clock the internal address counter and the data input/output latches. The load on each /CAS is typically less than the load on the other control signals (/RAS, /WE and /OE) since each /CAS typically controls only a byte width of the data bus. Internal circuitry of the memory device is largely compatible with existing Extended Data Out (EDO) DRAMs. This similarity allows the two part types to be manufactured on one die with a limited amount of additional circuitry. The ability to switch between a standard non-burst mode and a high speed burst mode allows the device to be used to replace standard devices, and eliminates the need to switch to more complex high speed memory devices. Internal address generation provides for faster data access times than is possible with either fast page mode or EDO DRAMs.

A novel counter architecture provides address generation for linear and interleaved addressing sequences. A comparator is used to detect completion of a burst access, and to prepare the device to begin additional burst accesses. The device is compatible with existing memory module designs including Single In-Line Memory Module (SIMM), Multi-Chip Module (NCM) and Dual In-Line Memory Module (DIMN) designs. This combination of features allows for significant system performance improvements with a minimum of design alterations.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention as well as objects and advantages will be best understood by reference to the appended claims, detailed description of particular embodiments and accompanying drawings where:

FIG. 1 is an electrical schematic diagram of a memory device in accordance with one embodiment of the invention;

FIG. 2 is a table showing linear versus interleaved addressing formats;

FIG. 3 is a timing diagram for a method of accessing the device of FIG. 1;

FIG. 4 is a further timing diagram for accessing the device of FIG. 1;

FIG. 5 is an electrical schematic diagram of a Single In-Line Memory Module in accordance with another embodiment of the invention;

FIG. 6 is a schematic diagram of a column address generation and control circuit;

FIG. 7 is a schematic of a one bit counter element;

FIG. 8 is a schematic of a counter element clock enable circuit;

FIG. 9 is a schematic of a flip flop;

FIG. 10 is a schematic of an enable NAND gate;

FIG. 11 is a schematic of an enable NOR gate;

FIG. 12 is a schematic of a three bit address generator circuit; and

FIG. 13 is a schematic diagram of a system designed in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a schematic representation of a sixteen megabit device designed in accordance with the present invention. The device is organized as a 2 Meg×8 burst EDO DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array 12. The device of FIG. 1 may have an industry standard pinout for eight bit wide EDO DRAMs. An active-low row address strobe (/RAS) signal 14 is used to latch a first portion of a multiplexed memory address, from address inputs 16, in latch 18. The latched row address 20 is decoded in row decoder 22. The decoded row address is used to select a row of the memory array 12. A column address strobe (/CAS) signal 24 is used to latch a second portion of a memory address from address inputs 16 into address generation circuit 26. The latched column address 28 is decoded in column address decoder 30. The decoded column address is used to select a column of the memory array 12.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 32 to output latches 34. Data 10 driven from the burst EDO DRAM may be latched external to the device in synchronization with /CAS after a predetermined number of /CAS cycle delays (latency). For a two cycle latency design, the first /CAS falling edge is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second /CAS falling edge, and remains valid through the third /CAS falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers 34 will continue to drive the data lines without tri-stating the data outputs during /CAS high intervals dependent on the state of the output enable and write enable (/OE and /WE) control lines, thus allowing additional time for the system to latch the output data. The data outputs remain valid throughout the burst read cycles with the exception of brief periods of data transition. During these periods of data transition, the output drivers may be turned off momentarily in order to aid data transition. This state of the output buffer should not be confused with the standard DRAM tri-state condition which is intended to release the data bus.

Once a row and a column address are selected, additional transitions of the /CAS signal are used to advance the column address within the address generation circuit in a predetermined sequence. The time at which data will be valid at the outputs of the burst EDO DRAM is dependent only on the timing of the /CAS signal provided that /OE is maintained low, anid /WE remains high. The output data signal levels may be but are not limited to being driven in accordance with standard CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. FIG. 2 is a table which shows linear and interleaved addressing sequences for burst lengths of 2,4 and 8 cycles. The "V" for starting addresses A1 and A2 in the table represent address values that remain unaltered through the burst sequence. The column address may be advanced with each /CAS transition, each pulse, or multiple of /CAS pulses in the event that more than one data word is read from the array with each column address. When the address is advanced with each transition of the /CAS signal, data is also driven from the part after each transition following the device latency which is then referenced to each edge of the /CAS signal. This allows for a burst access cycle where the highest switching control line (/CAS) toggles only once (high to low or low to high) for each memory cycle. This is in contrast to standard DRAMs which require /CAS to go low and then high for each cycle, and synchronous DRAMs which require a full clock cycle (high and low transitions) for each memory cycle. For maximum compatibility with existing EDO DRAM devices, the invention will be further described in reference to a device

designed to latch and advance a column address on falling edges of the /CAS signal.

In the burst access memory device, each new column address from the address generation circuit is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16. This burst sequence of data will continue for each /CAS falling edge until a predetermined number of data accesses equal to the burst length has occurred. A /CAS falling edge received after the last burst address has been generated will latch another column address from the address inputs 16 and a new burst sequence will begin. Read data is latched and output with each falling edge of /CAS after the first /CAS latency.

For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the row and column addresses is latched with the /CAS signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is preferred. Additional input data words for storage at incremented column address locations are latched by /CAS on successive /CAS pulses. Input data from the input latches 34 is passed along data path 32 to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes will occur without the requirement of additional column addresses being provided on the address lines 16. After the predetermined number of burst writes has occurred, a subsequent /CAS pulse will latch a new beginning column address, and another burst read or write access will begin.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by /CAS. /WE low at the column address latch time selects a burst write access. /WE high at the column address latch time selects a burst read access. The level of the /WE signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access will terminate the burst access, preventing further writes from occurring. A high to low transition on /WE within a burst read access will likewise terminate the burst read access and will place the data output 10 in a high impedance state. Transitions of the /WE signal may be locked out during critical timing periods within an access cycle in order to reduce the possibility of triggering a false write cycle. After the critical timing period the state of /WE will determine whether a burst access continues, is initiated, or is terminated. Termination of a burst access places the DRAM in a state to receive another burst access command. Both /RAS and /CAS going high during a burst access will also terminate the burst access cycle and place the data drivers in a high impedance output state. Read data may remain valid at the device outputs if /RAS alone goes high while /CAS is active for compatibility with hidden refresh cycles, otherwise /RAS high alone may be used to terminate a burst access. A minimum write enable pulse width is only required when it is desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses. In the case of burst reads, /WE will transition from high to low to terminate a first burst read, and then /WE will transition back high prior to the next falling edge of /CAS in order to specify a new burst read cycle. For burst writes, /WE would transition high to terminate a current burst write access, then back low prior to the next falling edge of /CAS to initiate another burst write access. A basic implementation of the device of FIG. 1 may include a fixed burst length of 4, a fixed /CAS latency of 2 and a programmable sequence of burst addresses. This basic implementation requires very little additional circuitry to the standard EDO page mode DRAM, and may be mass produced to provide the finctions of both the standard EDO page mode and burst EDO DRAMs. This device also allows for the output enable pin (/OE) to be grounded for compatibility with many SIMM module designs. When not disabled (tied to ground), /OE is an asynchronous control which will prevent data from being driven from the part in a read cycle if it is inactive (high) prior to /CAS falling and remains inactive beyond /CAS rising. If these setup and hold conditions are not met, then the read data may be driven for a portion of the read cycle. It is possible to synchronize the /OE signal with /CAS, however this would typically increase the /CAS to data valid delay time and doesn't allow for the read data to be disabled prior to /RAS high without an additional /CAS low pulse which would otherwise be unnecessary. In a preferred embodiment, if /OE transitions high at any time during a read cycle the outputs will remain in a high impedance state until the next falling edge of /CAS despite firther transitions of the /OE signal.

Programmability of the burst length, /CAS latency and address sequences may be accomplished through the use of a mode register 40 which latches the state of one or more of the address input signals 16 or data signals 10 upon receipt of a write-/CAS-before-/RAS (WCBR) programming cycle. In such a device, outputs 44 from the mode register control the required circuits on the DRAM. Burst length options of 2, 4, 8 and full page as well as /CAS latencies of 1, 2 and 3 may be provided. Other burst length and latency options may be provided as the operating speeds of the device increase, and computer architectures evolve. The device of FIG. 1 includes programmability of the address sequence by latching the state of the least significant address bit during a WCBR cycle. Additional input signals may be used to decode an enable for setting the address sequence. For example, a specific value received on address lines A1–A7 in a WCBR cycle is decoded to specify that the sequence mode is to be set, and the state of AO is used to specify which mode is selected. The burst length and /CAS latency for this particular embodiment are fixed. Other possible alterations in the feature sets of this DRAM include having a fixed burst mode only, selecting between standard fast page mode (non-EDO) and burst mode, and using the output enable (/OE) 42 in combination with /RAS to select between modes of operation. Also, a WCBR refresh cycle could be used to select the mode of operation rather than a control signal in combination with /RAS. A more complex memory device may provide additional modes of operation such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of /WE and /OE at /RAS falling time. One mode from a similar set of modes may be selected through the use of a WCBR cycle using multiple address or data lines to encode the desired mode. Alternately, a device with multiple modes of operation may have wire bond locations, or programmable fuses which may be used to program the mode of operation of the device.

The present invention is described with reference to several preferred embodiments. Just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including x1, x4, x8 and x16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the memory device of the present invention may take the

form of many different memory organizations. It is believed that one who is skilled in the art of integrated circuit memory design can, with the aide of this specification design a variety of memory devices which do not depart from the spirit of this invention. It is therefore believed that detailed descriptions of all of the various memory device organizations applicable to this invention are not necessary.

A preferred pinout for the device of FIG. 1 is identical to the pinout for a standard EDO DRAM. The common pinout allows this new device to be used in existing memory designs with minimum design changes. The common pinout also allows for ease of new designs by those of skill in the art who are familiar with the standard EDO DRAM pinout. Variations of the described invention which maintain the standard EDO DRAM pinout include driving the ICAS pin with a system clock signal to synchronize data access of the memory device with the system clock. For this embodiment, it may be desirable to use the first /CAS active edge after /RAS falls to latch the row address, a later edge may be used to latch the first column address of a burst access cycle. After row and column addresses are latched within the device, the address may be incremented internally to provide burst access cycles in synchronization with the system clock. Other pin fuiction alternatives include driving the burst address incrementing signal on the /OE pin since the part does not require a data output disable function on this pin. Other alternate uses of the /OE pin also allow the device to maintain the standard EDO pinout, but provide increased finctionality such as burst mode access. The /OE pin may be used to signal the presence of a valid column starting address, or to terminate a burst access. Each of these embodiments provides for a high speed burst access memory device which may be used in current memory systems with a minimum amount of redesign.

FIG. 3 is a timing diagram for performing a burst read followed by a burst write of the device of FIG. 1. In FIG. 3, a row address is latched by the /RAS signal. JWE is low when /RAS falls for an embodiment of the design where the state of the /WE pin is used to specify a burst access cycle at /RAS time. Next, /CAS is driven low with /WE high to initiate a burst read access, and the column address is latched. The data out signals (DQ's) are not driven in the first /CAS cycle. On the second falling edge of the /CAS signal, the internal address generation circuitry advances the column address and begins another access of the array, and the first data out is driven from the device after a /CAS to data access time (tCAC). Additional burst access cycles continue, for a device with a specified burst length of four, until the fifth falling edge of /CAS which latches a new column address for a new burst read access. /WE falling in the fifth /CAS cycle terminates the burst access, and initializes the device for additional burst accesses. The sixth falling edge of /CAS with /WE low is used to latch a new burst address, latch input data and begin a burst write access of the device. Additional data values are latched on successive /CAS falling edges until /RAS rises to terminate the burst access.

FIG. 4 is a timing diagram depicting burst write access cycles followed by burst read cycles. As in FIG. 3, the /RAS signal is used to latch the row address. /WE is shown as a "don't care" at the time /RAS falls for an embodiment of the present invention that does not utilize the state of /WE at /RAS time to select between burst and non-burst access modes. The first /CAS falling edge in combination with /WE low begins a burst write access with the first data being latched. Additional data values are latched with successive /CAS falling edges, and the memory address is advanced internal to the device in either an interleaved or sequential manner. On the fifth /CAS falling edge a new column address and associated write data are latched. The burst write access cycles continue until the /WE signal goes high in the sixth /CAS cycle. The transition of the /WE signal terminates the burst write access. The seventh /CAS low transition latches a new column address and begins a burst read access (/WE is high). The burst read continues until /RAS rises terminating the burst cycles.

It should be noted from Figs. 3 and 4, that for burst read cycles the data remains valid on the device outputs as long as the /OE pin is low, except for brief periods of data transition. Also, since the /WE pin is low prior to or when /CAS falls, the data input/output lines are not driven from the part during write cycles, and the /OE pin may be grounded. Only the /CAS signal and the data signals toggle at relatively high frequency, and no control signals other than /CAS are required to be in an active or inactive state for one /CAS cycle time or less. This is in contrast to SDRAMs which often require row address strobes, column address strobes, data mask, and read/write control signals to be valid for one clock cycle or less for various device functions. Typical DRAMs also allow for the column address to propagate through to the array to begin a data access prior to /CAS falling. This is done to provide fast data access from /CAS falling if the address has been valid for a sufficient period of time prior to /CAS falling for the data to have been accessed from the array. In these designs an address transition detection circuit is used to restart the memory access if the column address changes prior to /CAS falling. This method actually requires additional time for performing a memory access since it must allow for a period of time at the beginning of each memory cycle after the last address transition to prepare for a new column address. Changes in the column address just prior to /CAS falling may increase the access time by approximately five nanoseconds. An embodiment of the present invention will not allow the column address to propagate through to the array until after /CAS has fallen. This eliminates the need for address transition detection circuitry, and allows for a fixed array access relative to /CAS.

FIG. 5 is a schematic representation of a single in-line memory module (SIMM) designed in accordance with the present invention. The SIMM has a standard SIMM module pinout for physical compatibility with existing systems and sockets. Functional compatibility with EDO page mode SIMMs is maintained when each of the 2 Megx8 memory devices **10**, **12**, **14** and **16** are operated in an EDO page mode. Each of the /CAS signals **18**, **20**, **22** and **24** control one byte width of the 32 bit data bus **26**, **28**, **30** and **32**. A /RAS **34** signal is used to latch a row address in each of the memory devices, and is optionally used in combination with /WE **36** to select between page mode and burst mode access cycles. Address signals **38** provide a multiplexed row and column address to each memory device on the SIMM. In burst mode, only active /CAS control lines are required to toggle at the operating frequency of the device, or at half the frequency if each edge of the /CAS signal is used as described above. The data lines are required to be switchable at half of the frequency of the /CAS lines or at the same frequency, and the other control and address signals switch at lower frequencies than /CAS and the data lines. As shown in FIG. 5, each /CAS signal and each data line is connected to a single memory device allowing for higher frequency switching than the other control and address signals. Each of the memory devices **10**, **12**, **14** and **16** is designed in accordance with the present invention allowing for a burst

mode of operation providing internal address generation for sequential or interleaved data access from multiple memory address locations with timing relative to the /CAS control lines after a first row and column address are latched.

FIG. 6 is a schematic representation of the address generation circuit 26 of FIG. 1. FIG. 6 by way of example shows a two bit address generator for a Burst EDO memory device with a fixed burst length of four. Electrical signals and circuit elements in FIG. 6 which are common or derivatives of elements of FIG. 1 are labeled with the same reference numbers. As shown in FIG. 1, address 16, address strobe 24, and control 39 from control circuitry 38 provide inputs to address generation circuit 26. Mode control information 44 from the mode control register of FIG. 6 is also received by address generation circuit 26. For the two bit address generator shown, the most significant bits (MSBs) of the address are latched in latch 50 to provide the column address MSBs 52 which form a portion of address 28 of FIG. 1. The two least significant bits A0 and A1 of address 16 are each coupled to a one bit counter element 54. The two one bit counter elements together make up a two bit burst address counter. The outputs of the one bit counter elements are latched initial address bits 56 and 58, burst address bits 60 and 62 and compliments of the burst address bits 64 and 66. The latched initial address 52, 56 and 58 will reflect the initial burst address until it is overwritten with a new initial burst address. The latched initial address is used in determining when the terminal burst address has been reached. The LSB latched initial address 58 is also used to determine the toggle condition 68 for the next higher counter bit. The clock for the least significant address counter element is derived from the address strobe signal 24. The clock for the next least significant bit is derived from the address strobe signal in combination with either the true 60 or compliment 64 burst address output of the LSB counter element as selected by a logical fiction, in this embodiment AND gate 69, of the addressing mode 70 and the latched initial address of the LSB counter element. This embodiment of the address generation circuit also comprises a comparator circuit 72 which compares the burst address signals with the initial latched address signals after the counter is first advanced.

In operation, a burst access command 39, a burst terminate command (write enable transition for example) on line 90, a reset condition on line 88, or a match signal on line 84, in combination with an address strobe signal, will cause an initial address to be latched in response to load signal 74 from load control circuit 92. After the initial address is latched, a burst access will be initiated. The initial address is latched in address latch 50 and in the address counter elements. Each address strobe active edge transition will cause the LSB counter element burst address outputs 60 and 64 to toggle in accordance with the addressing sequences described in FIG. 2. The second address bit will conditionally toggle in response to the address strobe dependent upon the state of the true or compliment output of the next lower order counter element. In a linear addressing mode, the second counter element will toggle as the LSB 60 toggles from a high to a low, and will maintain its state as the LSB toggles from a low to a high. In an interleaved addressing mode, the second LSB will likewise toggle as the LSB toggles from a high to a low, and will maintain its state as the LSB toggles from a low to a high, but only if the latched address LSB 58 is low (all even initial addresses). For the case of interleaved addressing from an odd (LSB high) initial address, the second LSB counter output will toggle as the LSB 60 toggles from a low to a high. As the LSB counter true output toggles from low to high, the compliment output 64 will toggle from high to low. A multiplexer 76 is used to select between the true and compliment outputs of the LSB counter to provide the toggle condition for the next counter bit. The multiplexer output is selected by logic circuit 70.

In a preferred embodiment a clock enable circuit 78 receives the toggle signal via signal line 68. It also receives the address strobe signal and provides a glitch free clock signal to the second counter element. Enable signal 94 is used to initialize or disable the clock enable circuit. An additional counter element can be added to provide addresses for burst lengths up to eight. The toggle condition of the additional stage would be dependent upon a logical combination of the previous stage latched initial address output 56 and the addressing mode in the same manner that the second stage is dependent upon the first. The initial latched address bit from the second stage in combination with the interleaved versus linear mode control determines whether the second stage true or compliment output controls the toggle condition for the third stage. For full page burst capability, the counter can be expanded without additional multiplexers for selecting toggle conditions since full page burst sequences are typically defined for linear addressing only.

The comparator is used to detect the endpoint of a burst sequence. The comparator is disabled when an initial address is loaded. After the counter is incremented, the comparator is enabled. After the terminal burst address is reached, the counter will be incremented to a value which matches the initial value. This condition results in an address match within the comparator. The match signal is coupled to the counter load control circuit and causes a new burst access initial address to be loaded, at which time the comparator is again disabled until the address is advanced.

In a preferred embodiment, memory accesses begin in response to a high to low transition of the /CAS signal, and the address counter is advanced in response to a low to high transition of /CAS. When a new burst access is begun, the address latch and counter are loaded, an access cycle is begun at the initial address and the comparator is disabled. When /CAS rises, the counter is incremented, and the comparator is enabled. Additional access cycles occur in response to successive /CAS falling edges. The /CAS rising edge following the last access of a burst cycle will cause the counter to advance and wrap around to an address which matches the initial address. The comparator will output a match signal 84 which causes a new initial burst address to be latched in response to the following /CAS falling edge. The comparator only needs to be enabled while /CAS is high, and preferably from a time delay after /CAS goes high at least until /CAS goes low. Delay circuit 80 provides the delayed /CAS signal to the comparator to enable the match signal output of the comparator.

FIG. 7 is a schematic representation of one embodiment of the one bit counter element 54 of FIG. 6. Pass devices 101 are enabled in response to load control signal 74 from the load control circuit 92 of FIG. 6. When the pass devices are enabled, pull up devices 102 are disabled, and an address bit 104, from address bus 16 of FIG. 6, along with its compliment 106 are used to set or reset the SR flip flop 108. When the load control signal is in the inactive state (high for this embodiment), the pull up devices place the SR flip flops in a toggle flip flop configuration by pulling the set and reset inputs high with the pass devices disabled. While in the toggle flip flop configuration, the flip flop outputs will toggle with each positive transition of the input clock 109. The initial address is also latched in latch 110 and buffered out of the counter element through buffer 111. The SR flip flop outputs are also buffered by buffers 112 and 114.

FIG. 8 is a schematic representation of the clock enable circuit of FIG. 6. The output of the clock enable circuit 120 is a logical function of the clocking signal 122 (typically the column address strobe 24 of FIG. 6) and the toggle condition signal 68 received from the multiplexer of FIG. 6. It is desired to provide a glitch free clock signal from the clock enable circuit which will clock a counter element when the clock signal rises (in synchronization with the previous counter element). When the clock signal rises, the input 68 is allowed to pass through to latch 124 and the output is forced high by signal 125. Forcing the output high prevents the output from switching in response to transitions on the input which occur after rising edges of the clock as the counter is advanced. When the input clock signal goes low, if the input 68 was high, the output of latch 124 will be latched high, and the output of the clock enable circuit will go low indicating that the next counter stage is to be clocked on the next rising edge of the clock. When the next rising clock edge occurs, the output of the clock enable circuit will be forced back high, and input 68 which is now low will pass through to hold the output high when the clock transitions back low. A clock enable circuit input for a third counter element clock input can be designed in a similar fashion where the input is a logical AND of the input 68 for the first clock enable circuit and the multiplexer output of the second counter element as shown in FIG. 12. Gating the input in this manner ensures that the input will only be high for one cycle when the next counter stage is to be toggled. Enable input 94 when high will force the clock enable circuit output to a high preventing the next counter stage from advancing. This input may be driven high for a reset condition, to disable burst mode addressing, or to control the burst length in an embodiment such as that shown in FIG. 12.

FIG. 9 is a schematic diagram of one embodiment of the flip flop 108 of FIG. 7. The flip flop is comprised of two cross coupled Enable NAND gates, and two cross coupled Enable NOR gates. This embodiment of the flip flop has active low set (S*) and reset (R*) inputs, a clock input, a true output and a compliment output. Examples of Enable NAND and Enable NOR gates are provided in FIGS. 10 and 11 respectively.

FIG. 12 is a schematic diagram of a three bit counter designed in accordance with the teachings of the present invention. Many of the elements of FIG. 12 have reference numbers which correspond to similar or identical elements found in FIG. 6. As described above, a third counter element may be added to the circuit of FIG. 6 to provide a three bit counter for linear and interleaved eight cycle burst sequences. The MSB address latch 50 is one bit narrower than the latch of FIG. 6, and the comparator 72 is one bit wider. Additional clock control may be added to individually mask the clock inputs of the second and third counter stages to provide for a programmable burst length of 2 (second and third clocks masked), 4 (third stage clock masked) and 8 (all clocks enabled). The clock masking of the second and third stages may be accomplished through independent control of the clock enable circuit enable inputs in response to burst length control 44 from mode register 40 of FIG. 1. If the higher order counter stages are prevented from advancing, the comparator will detect an address match as the LSBs wrap around, and the burst access will be terminated at the appropriate time as described in reference to the embodiment of FIG. 6.

FIG. 13 is a schematic representation of a data processing apparatus designed in accordance with the present invention. In FIG. 13, microprocessor 212 is connected via address lines 214 and control lines 216 to a memory control circuit 218. The memory control circuit provides address and control signals on lines 222 and 220 respectively to a burst access memory device 224. The burst access memory device sends and receives data over data bus 226. Optional data bus buffer 230 between memory data bus 226 and microprocessor data bus 228 allows for amplification of the data signals, and/or synchronization with the microprocessor and memory control signals. A fast static random access memory (SRAM) cache circuit 232 is also optional and provides higher speed access to data stored in the cache from the memory circuit or the microprocessor. Memory control circuit 218 may be incorporated within the microprocessor. The memory control circuit provides the required address strobe signals, address signals and read/write control signals required for burst mode access of the memory circuit. The capability of the processor to access the memory in a burst mode allows for the design of a computer with relatively high memory bandwidth without the requirement of a fast SRAM cache. SRAMs which are fast enough to provide memory access without wait states can significantly add to the cost of a computer. Thus the burst access memory device of the present invention allows for medium to high performance computers to be manufactured at a cost which is significantly less than those manufactured today. Use of the burst access memory device of the present invention in cooperation with a fast SRAM cache allows for an even higher performance computer design by providing fast burst access of main memory in the event of a cache miss.

In operation, the microprocessor reads data from the memory device by supplying address and control signals to the memory device through the memory control circuit. In response to an initial address, a read command and an access cycle strobe, the memory device begins to access a first data word at the initial address. A second access cycle strobe advances the address within the memory device in a second access period of the burst access, and initiates a read access of data from a second address. For a latency of two, the first data is driven from the memory device after the second access cycle strobe signal occurs. Typically the first data is latched in the microprocessor in response to a third access cycle strobe which occurs at the beginning of a third access cycle period of the burst access. The third access cycle strobe also causes the second data value to be driven from the memory device. The third access cycle strobe also causes a third address to be generated within the memory device, and a third data access begins. Data is latched in the microprocessor in response to fourth, fifth and sixth access cycle strobes. In this manner four data values are received in the microprocessor in response to a single address and a plurality of access cycle strobes. The microprocessor may provide a second address to the memory device with the fifth access cycle strobe signal if the memory device is designed to perform four word burst sequences and additional data values are required from the memory. In this case, a second four word burst sequence is begun while the microprocessor is receiving data from the first four word burst. The data buffer 230 may be used to synchronize data from the memory device received in response to the access cycle strobe signal, with a system clock which is connected to the microprocessor. For write cycles, there is typically no latency. Data for write cycles is provided with each access cycle strobe signal in a burst write sequence.

In an alternate embodiment, initial burst access addresses are latched in the memory in response to falling edges of the address strobe, and additional burst addresses are generated within the memory in response to rising edges of the address strobe. The additional addresses are used to perform

memory accesses in response to falling edges of the address strobe. In this manner, generation of the address for the next access cycle is begun in advance. This address may be compared with the initial address to detect an end of burst sequence condition. When the burst access is complete or terminated, a new initial address is latched in response to a falling address strobe signal.

For the purposes of this specification a microprocessor may be, but is not limited to, a microprocessor, a microcontroller, a digital signal processor, or an arithmetic processor. A signal may refer to, but is not limited to, information transferred via a conductor, or a conductor for transferring information. A node may refer to, but is not limited to, an input point, an output point, an intersection of conductors, or a point along a conductor.

While the present invention has been described with reference to preferred embodiments, numerous modifications and variations of the invention will be apparent to one of skill in the art without departing from the scope of the invention.

What is claimed is:

1. A memory device comprising a plurality of addressable memory elements, the memory device further comprising:

a two bit address generation circuit adapted to receive a first memory address in response to a transition of an address latch signal, and further adapted to generate two least significant bits in a series of memory addresses in a selectable one of a plurality of predetermined burst address sequences in response to subsequent transitions of the address latch signal, the two bit address generation circuit comprising,

a latch circuit for latching most significant bits in the first memory address,

two one-bit counter circuits for incrementing the two least significant bits,

a control circuit for controlling the two one-bit counter circuits, and

a comparator circuit for comparing the first memory address with the series of memory addresses.

2. The memory device of claim 1 wherein the two one-bit counter circuits each comprise:

an input connection for receiving a bit of the first memory address;

a flip flop circuit adapted to receive the bit of the first memory address;

pass circuitry connected to the input connection and the flip flop circuit; and

a latch for latching the bit of the first memory address.

3. The memory device according to claim 1 wherein the plurality of predetermined burst address sequences comprises an interleaved address sequence and a linear address sequence, and any one of the plurality of predetermined burst address sequences may be selected for performing a burst access of the memory device.

4. The memory device according to claim 1 further comprising an address sequence select circuit electrically coupled to the two bit address generation circuit for selecting one of the plurality of predetermined burst address sequences.

5. A memory device comprising a plurality of addressable memory elements, the memory device fuirther comprising:

a three bit address generation circuit adapted to receive a first memory address in response to a transition of an address latch signal, and further adapted to generate three least significant bits in a series of memory addresses in a selectable one of a plurality of predetermined burst address sequences in response to subsequent transitions of the address latch signal, the three bit address generation circuit comprising,

a latch circuit for latching most significant bits in the first memory address,

three one-bit counter circuits for incrementing the three least significant bits,

a control circuit for controlling the three one-bit counter circuits, and

a comparator circuit for comparing the first memory address with the series of memory addresses.

6. The memory device according to claim 5 wherein the comparator terminates a burst access of the memory device in response to a match of the first input address from the address latch with an address of the series of memory addresses from the address counter.

7. The memory device according to claim 5 further comprising:

an output buffer responsive to transitions of the address latch signal to output data after a latency of at least one cycle of the address latch signal.

8. The memory device according to claim 5 further comprising:

a sequence select circuit responsive to a sequence control signal for selecting one of a plurality of predetermined address sequences.

9. The memory device according to claim 5 wherein the three one-bit counter circuits each comprise:

a first flip flop having an output;

a second flip flop having an input.

10. The memory device according to claim 9 wherein a first counter circuit comprises a multiplexer having a first input coupled to the output of the first flip flop, a second input coupled to a compliment of the output of the first flip flop, a third input coupled to the sequence select circuit and an output coupled to the input of the second flip flop.

11. A control circuit for a two bit address generation circuit used in an integrated memory device and adapted to generate two least significant bits in a series of memory addresses in a selectable one of a plurality of predetermined address sequences, comprising:

a sequence control circuit responsive to a sequence control signal for selecting one of a plurality of predetermined address sequences, the sequence control circuit is coupled to the two bit address generation circuit and an initial count register, the two bit address generation circuit generates the two least significant bits in the series of memory addresses as determined by the sequence control circuit; and

a comparator coupled to an output of the two bit address generation circuit and to the initial count register, wherein the two bit address generation circuit is loaded in response to an output of the comparator indicating a match between the output of the two bit address generation circuit and a corresponding output of the initial count register.

12. A method of performing a burst access of a memory device, comprising:

loading a burst address counter with a first initial address;

accessing a first memory element at the first initial address;

advancing two least significant bits of the first initial address using the burst address counter;

accessing a second memory element at an address provided by the burst address counter;

comparing the first initial address with the address provided by the burst address counter; and

terminating the burst access in response to a match of the first initial address with the address provided by the burst address counter.

13. A data processing system comprising:

a microprocessor; and

a memory controller coupled to the microprocessor and a memory device;

the memory device comprising a plurality of addressable memory elements, the memory device further comprising:

an address counter adapted to receive a first memory address from the memory controller in response to a transition of an address latch signal, and further adapted to generate a series of memory addresses in a selectable one of a plurality of predetermined burst address sequences in response to subsequent transitions of the address latch signal.

14. The data processing system of claim 13, wherein:

the plurality of predetermined burst address sequences comprises an interleaved address sequence and a linear address sequence, and any one of the plurality of predetermined burst address sequences may be selected for performing a burst access of the memory device.

15. The data processing system of claim 13, further comprising:

an address sequence select circuit electrically coupled to the address counter for selecting one of the plurality of predetermined burst address sequences.

16. The data processing system of claim 15, wherein:

the address latch signal is a column address latch signal, and the address sequence select circuit is responsive to a row address latch signal to select an address sequence from the plurality of address sequences.

17. The memory device according to claim 3, further comprising:

an output buffer, electrically coupled to the memory elements, responsive to the address latch signal to output data from the memory device after a latency of at least one cycle of the address latch signal in a burst read access.

* * * * *

United States Patent [19]

Manning

[11] **Patent Number:** **5,963,504**

[45] **Date of Patent:** ***Oct. 5, 1999**

[54] **ADDRESS TRANSITION DETECTION IN A SYNCHRONOUS DESIGN**

[75] Inventor: **Troy A. Manning**, Meridian, Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[*] Notice: This patent is subject to a terminal disclaimer.

[21] Appl. No.: **08/994,180**

[22] Filed: **Dec. 19, 1997**

Related U.S. Application Data

[63] Continuation of application No. 08/506,438, Jul. 24, 1995, Pat. No. 5,729,503, which is a continuation-in-part of application No. 08/386,894, Feb. 10, 1995, Pat. No. 5,610,864, which is a continuation-in-part of application No. 08/370,761, Dec. 23, 1994, Pat. No. 5,526,320.

[51] **Int. Cl.**^{6} **G11C 8/00**

[52] **U.S. Cl.** **365/233.5**; 365/202; 365/230.02; 365/230.08

[58] **Field of Search** 365/233.5, 230.08, 365/189.05, 202, 230.02, 189.02, 193

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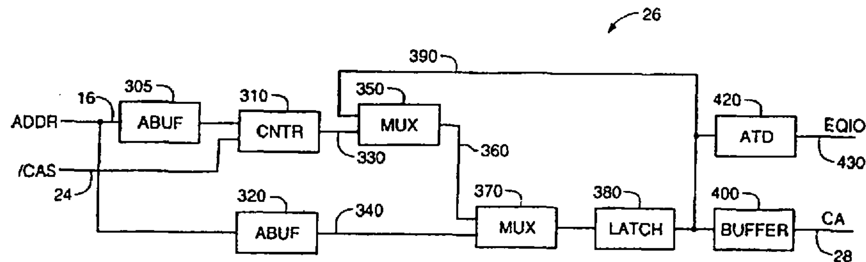
Primary Examiner—Don Hyun Yoo

Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth P.A.

[57] **ABSTRACT**

An integrated circuit memory device is designed to perform high speed burst access read and write cycles. An address strobe signal is used to latch a first address. During a burst access cycle the address is incremented internal to the device with additional address strobe transitions. A new memory address is only required at the beginning of each burst access. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at the device cycle frequency. A transition of the Read/Write control line during a burst access is used to terminate the burst access and initialize the device for another burst access. The memory device maintains compatibility with nonburst mode devices such as Extended Data Out (EDO) and Fast Page Mode through bond option or mode selection circuitry. A multiplexer selects between the input address and the burst address generator output to feed an asynchronous address transition detection circuit. The address transition detection circuit generates an equilibration control signal between memory access cycles.

5 Claims, 7 Drawing Sheets



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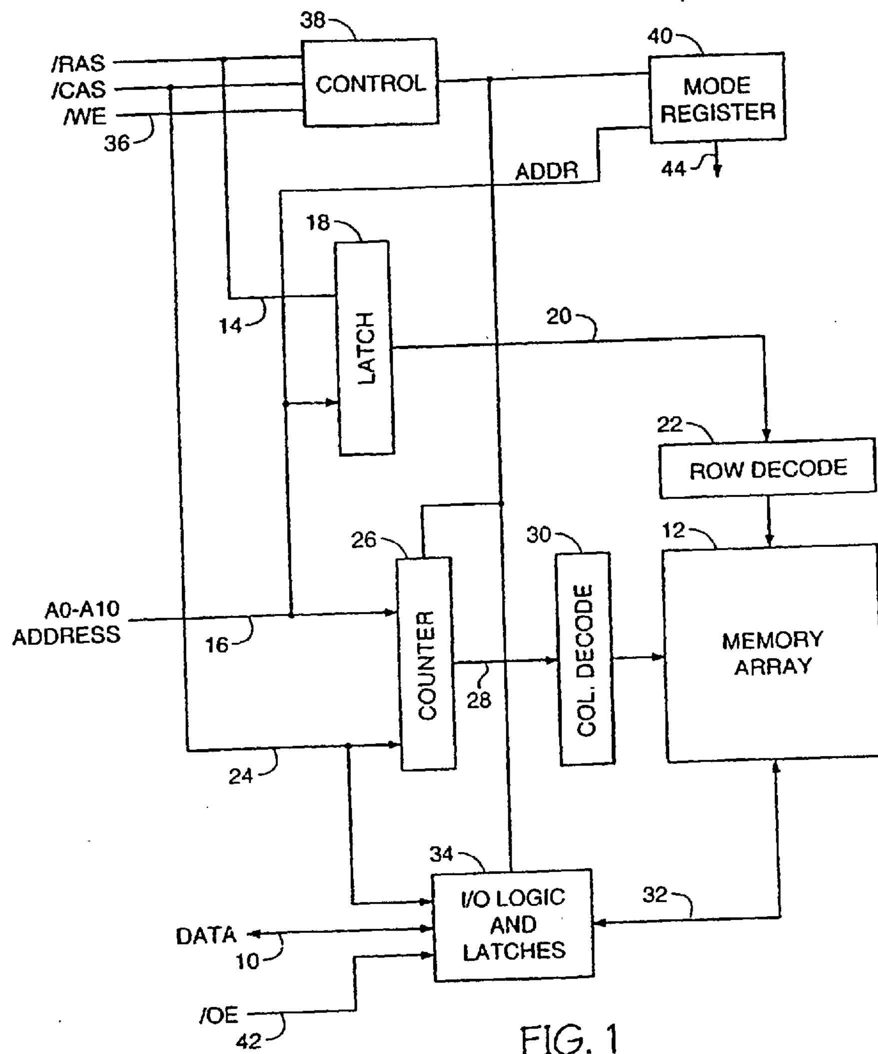

FIG. 1

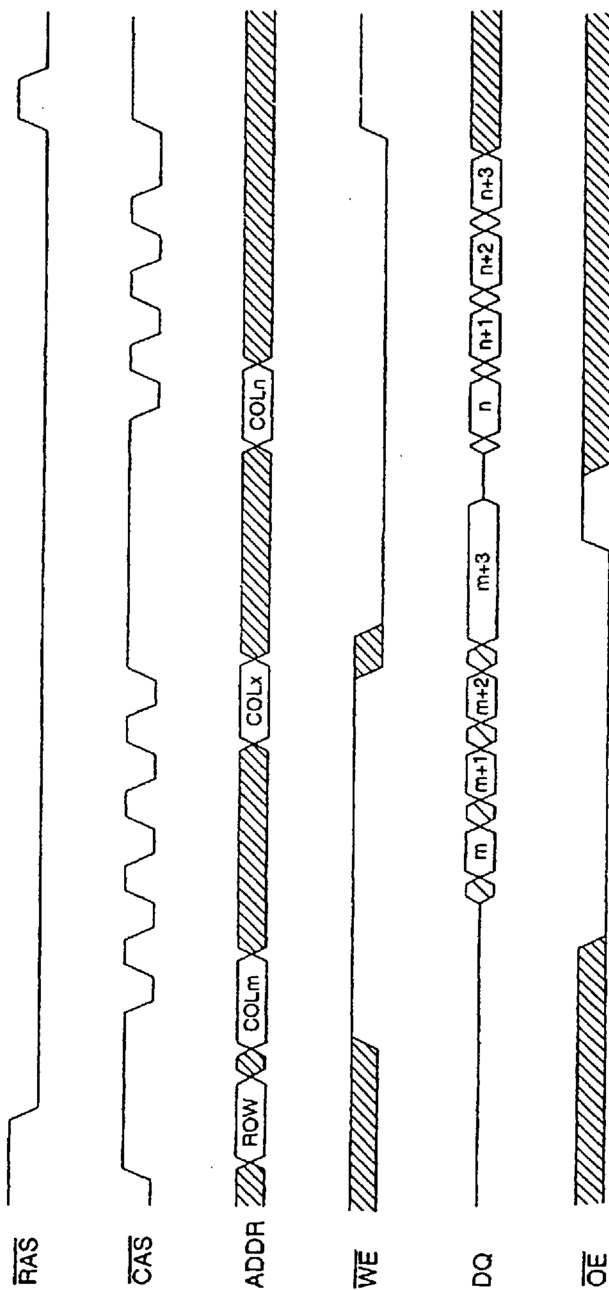

FIG. 2

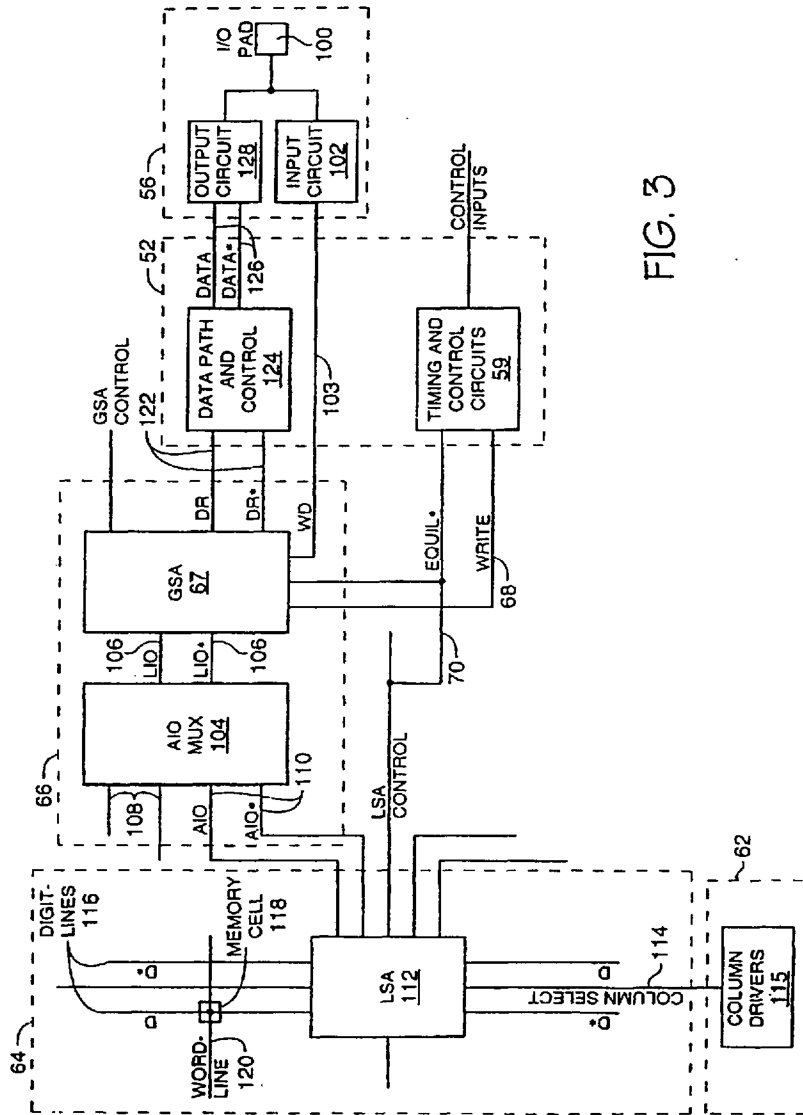

FIG. 3

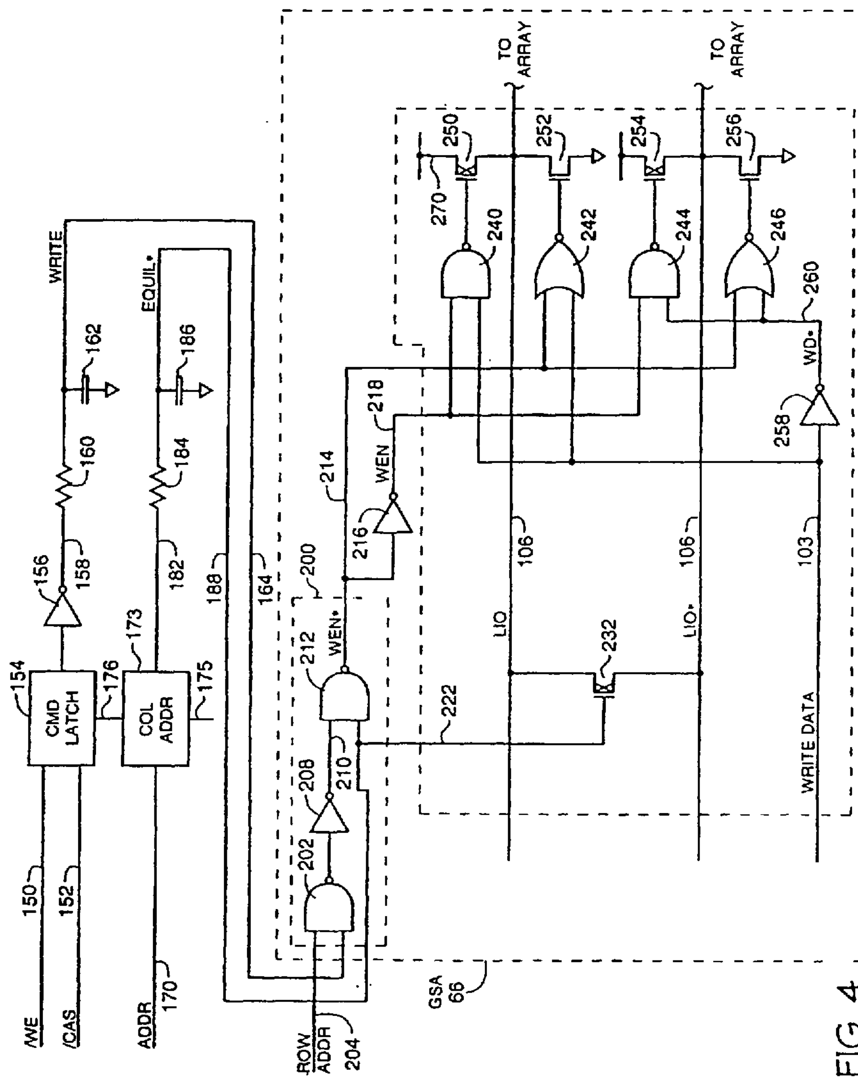

FIG. 4

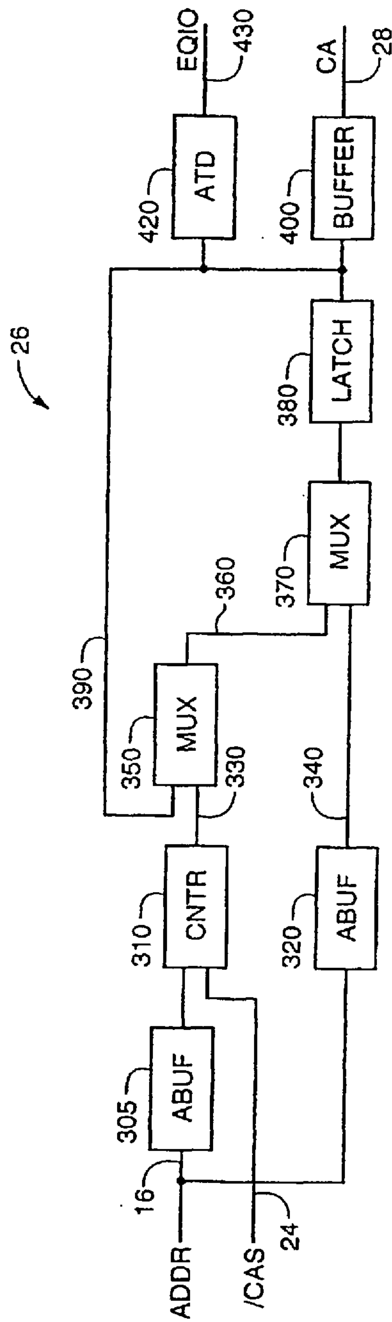

FIG. 5

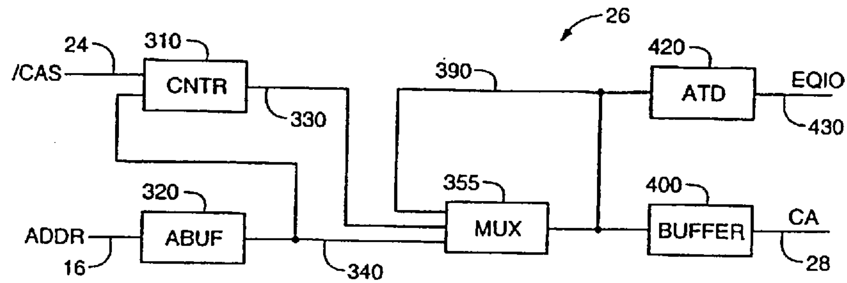

FIG. 6

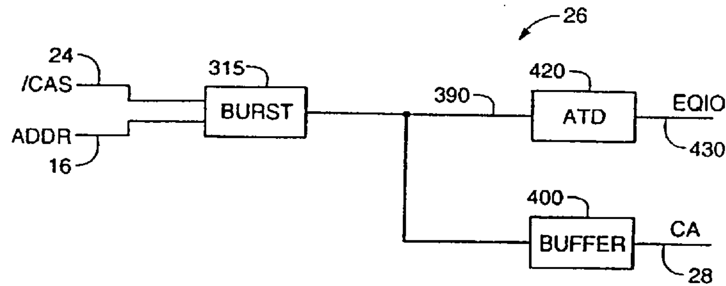

FIG. 7

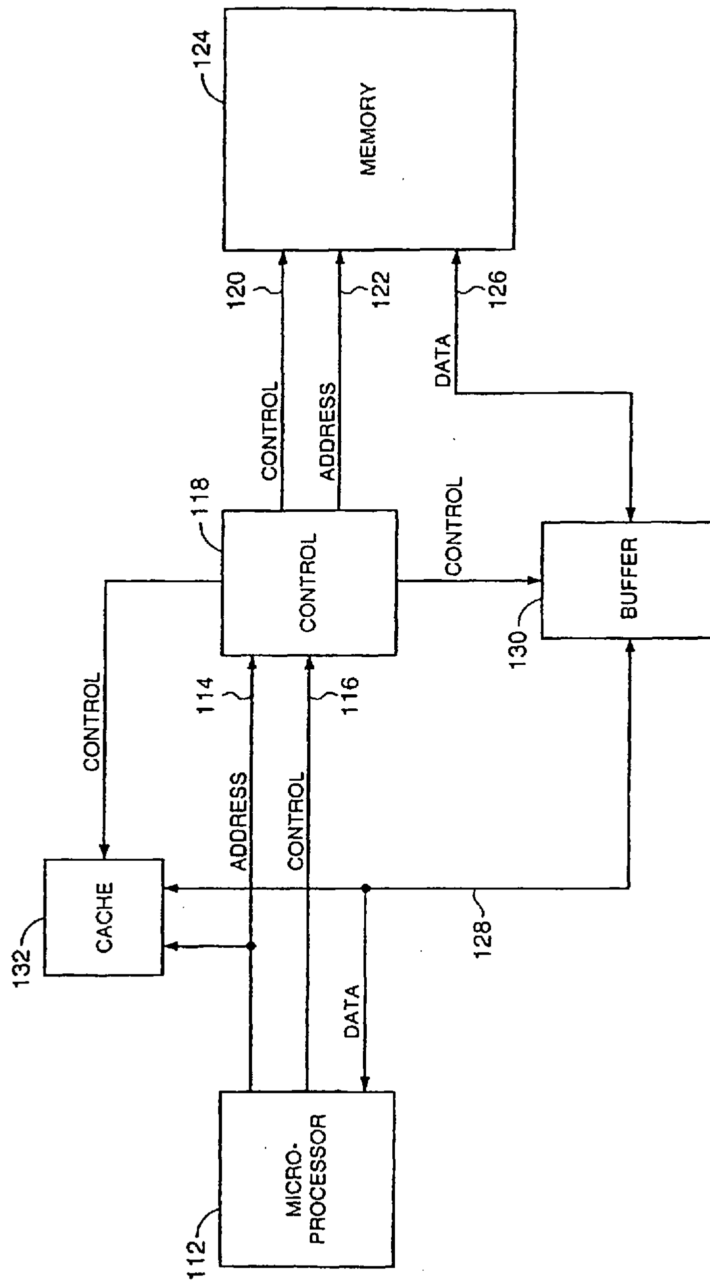

FIG. 8

ADDRESS TRANSITION DETECTION IN A SYNCHRONOUS DESIGN

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 08/506,438, filed Jul. 24, 1995, now U.S. Pat. No. 5,729,503, which, in turn, is a continuation in part of application Ser. No. 08/386,894 filed Feb. 10, 1995, now U.S. Pat. No. 5,610,864, which is a continuation in part of application Ser. No. 08/370,761 filed Dec. 23, 1994, now U.S. Pat. No. 5,526,320.

FIELD OF THE INVENTION

This invention relates to memory device architectures designed to provide high density data storage with high speed read and write access cycles. This invention relates more specifically to equilibration of data lines between memory access cycles in a device designed to operate in a burst access mode.

BACKGROUND OF THE INVENTION

There is a demand for faster, higher density, random access memory integrated circuits which provide a strategy for integration into today's personal computer systems. In an effort to meet this demand, numerous alternatives to the standard DRAM architecture have been proposed. One method of providing a longer period of time when data is valid at the outputs of a DRAM without increasing the fast page mode cycle time is called Extended Data Out (EDO) mode. In an EDO DRAM the data lines are not tri-stated between read cycles in a fast page mode operation. Instead, data is held valid after /CAS goes high until sometime after the next /CAS low pulse occurs, or until /RAS or the output enable (/OE) goes high. Determining when valid data will arrive at the outputs of a fast page mode or EDO DRAM can be a complex function of when the column address inputs are valid, when /CAS falls, the state of /OE and when /CAS rose in the previous cycle. The period during which data is valid with respect to the control line signals (especially /CAS) is determined by the specific implementation of the EDO mode, as adopted by the various DRAM manufacturers.

Methods to shorten memory access cycles tend to require additional circuitry, additional control pins and nonstandard device pinouts. The proposed industry standard synchronous DRAM (SDRAM) for example has an additional pin for receiving a system clock signal. Since the system clock is connected to each device in a memory system, it is highly loaded, and it is always toggling circuitry in every device. SDRAMs also have a clock enable pin, a chip select pin and a data mask pin. Other signals which appear to be similar in name to those found on standard DRAMs have dramatically different functionality on a SDRAM. The addition of several control pins has required a deviation in device pinout from standard DRAMs which further complicates design efforts to utilize these new devices. Significant amounts of additional circuitry are required in the SDRAM devices which in turn result in higher device manufacturing costs.

It is desirable to design and manufacture a memory device having a standard DRAM pinout and a burst mode of operation where multiple data values can be sequentially written to or read from the device in response to a single address location and multiple access cycle strobes. It is also desirable that this new memory device operate at higher frequencies than standard DRAMs.

In a standard DRAM device, equalization of internal data I/O lines is performed in response to column address transitions in preparation for reading or writing data from another memory cell, and also in response to a receipt of a write command to reduce the maximum signal transition on the data lines once the write drivers are enabled. Since there is a relatively wide time period in which column addresses may become valid, it has been advantageous to use an asynchronous address transition detection circuit to generate an equilibration control signal in response to address transitions. In EDO and fast page mode devices for example, the column address is treated as valid during a page mode cycle while /CAS is high. A read cycle will begin while /CAS is high at the column address indicated by the column address input signals. However, the column address is allowed to change until /CAS falls. Any column address change during the /CAS high time will require a new equilibration of I/O lines and the selection of the new column. When /CAS falls, the column address is latched and further transitions are masked. Equilibration of I/O lines allows for faster sensing of read data, and for faster writing of input data. If the data lines are each equalized to one half of Vcc for example, then the write data drivers will only need to drive one line from half Vcc to ground, and the other from half Vcc to Vcc. Otherwise, if the write data is not equal to the data previously on the I/O lines, the write data drivers will need to drive both true and compliment I/O lines a full Vcc swing for each data bit being written. Equalization of the data I/O lines reduces the maximum write cycle time by eliminating the worst case signal swing conditions. A similar situation exists during read cycles. In a read cycle, data sense amplifiers only need to drive an equilibrated I/O line from half Vcc to Vcc or ground. If the I/O lines were not equilibrated, the sense amplifiers would need to be large enough to overcome the full data signals on the I/O lines in a read cycle in a short period of time to allow for fast data access. A simple method of equilibrating the I/O lines is to: disable I/O line drivers; isolate the I/O lines from the digit lines; and couple complimentary I/O lines together. When a true I/O line is coupled to a complimentary I/O line, a logic high will be coupled to a logic low and each line will equalize to a potential approximately half way between a high and a low. It is important to disable the I/O line drivers during equilibration to prevent a true logic driver from being coupled to a complimentary logic driver which will draw excessive current from the logic high source to the logic low source.

In a burst access memory device, each access cycle can begin at a fixed point in time relative to the access cycle strobe or clock signal. In this case, an asynchronous address detection circuit is not required since address changes can be restricted to a fixed point in time relative to the access cycle strobe.

SUMMARY OF THE INVENTION

An integrated circuit memory device with a standard DRAM pinout is designed for high speed data access and for compatibility with existing memory systems. A high speed burst mode of operation is provided where multiple sequential accesses occur following a single column address, and read data is output relative to the /CAS control signal. In the burst mode of operation the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies. Read/Write commands are issued once per burst access eliminating the need to toggle the Read/Write control line at high speeds. Only one control line per memory chip (/CAS) must toggle at the operating frequency in order to clock the internal address counter and

the data input/output latches. The load on each /CAS is typically less than the load on the other control signals (/RAS, /WE and /OE) since each /CAS typically controls only a byte width of the data bus.

A single integrated circuit die has both burst mode access and page mode access capabilities. In page mode operation, the equilibrate signal is generated asychronously in response to column address transitions while /CAS is high. In burst mode, the equilibrate control signal is generated synchronously in response to /CAS transitions which control the generation of burst addresses. A multiplexer is used to direct the input address or the burst address to the address transition detection circuit. Among other benefits, use of the asynchronous address transition detection circuit in the burst mode eliminates the requirement for a synchronous equilibration control signal generation circuit, and minimizes the impact of the burst address path on the optimized asynchronous address path. In operation, at the beginning of a burst access, the initial burst address is fed through the asynchronous address path to the address transition detection circuit to generate an equilibrate signal, then the address path is switched to the burst address generator. At the beginning of each access cycle within the burst access the burst address will generate an equilibrate signal through the address transition detection circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention as well as objects and advantages are best understood by reference to the appended claims, detailed description of particular embodiments and accompanying drawings where:

FIG. 1 is an electrical schematic diagram of a memory device in accordance with one embodiment of the invention;

FIG. 2 is a timing diagram for a method of accessing the device of FIG. 1;

FIG. 3 is block level schematic of a data path portion of the device of FIG. 1;

FIG. 4 is a more detailed schematic of a portion of the circuitry of FIG. 3;

FIG. 5 is schematic diagram of a portion of the column address path of the device of FIG. 1;

FIG. 6 is an alternate schematic diagram of a portion of the column address path of the device of FIG. 1;

FIG. 7 is another alternate schematic diagram of a portion of the column address path of the device of FIG. 1; and

FIG. 8 is a schematic diagram of a computer system designed in accordance with the teachings of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a schematic representation of a sixteen megabit device designed in accordance with the present invention. The device is organized as a 2 Megx8 burst EDO DRAM having an eight bit data input/output path 10 providing data storage for 2,097,152 bytes of information in the memory array 12. The device of FIG. 1 has an industry standard pinout for eight bit wide EDO DRAMs. An active-low row address strobe (/RAS) signal 14 is used to latch a first portion of a multiplexed memory address, from address inputs A0 through A10 16, in latch 18. The latched row address 20 is decoded in row decoder 22. The decoded row address is used to select a row of the memory array 12. A column address strobe (/CAS) signal 24 is used to latch a second portion of a memory address from address inputs 16 into column address counter 26. The latched column address 28 is decoded in column address decoder 30. The decoded column address is used to select a column of the memory array 12.

In a burst read cycle, data within the memory array located at the row and column address selected by the row and column address decoders is read out of the memory array and sent along data path 32 to output latches 34. Data 10 driven from the burst EDO DRAM may be latched external to the device in synchronization with /CAS after a predetermined number of /CAS cycle delays (latency). For a two cycle latency design, the first /CAS falling edge is used to latch the initial address for the burst access. The first burst data from the memory is driven from the memory after the second /CAS falling edge, and remains valid through the third /CAS falling edge. Once the memory device begins to output data in a burst read cycle, the output drivers 34 continue to drive the data lines without tri-stating the data outputs during /CAS high intervals dependent on the state of the output enable and write enable (/OE and /WE) control lines, thus allowing additional time for the system to latch the output data. Once a row and a column address are selected, additional transitions of the /CAS signal are used to advance the column address within the column address counter in a predetermined sequence. The time at which data becomes valid at the outputs of the burst EDO DRAM is dependent only on the timing of the /CAS signal provided that /OE is maintained low, and /WE remains high. The output data signal levels may be driven in accordance with, but are not limited to, CMOS, TTL, LVTTL, GTL, or HSTL output level specifications.

The address may be advanced linearly, or in an interleaved fashion for maximum compatibility with the overall system requirements. The column address may be advanced with each /CAS transition, each pulse, or multiple of /CAS pulses in the event that more than one data word is read from the array with each column address. When the address is advanced with each transition of the /CAS signal, data is also driven from the part after each transition following the device latency which is then referenced to each edge of the /CAS signal. This allows for a burst access cycle where the highest switching control line (/CAS) toggles only once (high to low or low to high) for each memory cycle. This is in contrast to standard DRAMs which require /CAS to go low and then high for each cycle, and synchronous DRAMs which require a full clock cycle (high and low transitions) for each memory cycle. For maximum compatibility with existing EDO DRAM devices, the invention will be further described in reference to a device designed to initiate access cycles on falling edges of the /CAS signal. For designs where falling edges of the /CAS signal initiate an access cycle, the falling edge may be said to be the active transition of the /CAS signal.

In the burst access memory device, each new column address from the column address counter is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16. This burst sequence of data continues for each /CAS falling edge until a predetermined number of data accesses equal to the burst length occurs. A /CAS falling edge received after the last burst address has been generated latches another column address from the address inputs 16 and a new burst sequence begins. Read data is latched and output with each falling edge of /CAS after the first /CAS latency.

For a burst write cycle, data 10 is latched in input data latches 34. Data targeted at the first address specified by the

row and column addresses is latched with the /CAS signal when the first column address is latched (write cycle data latency is zero). Other write cycle data latency values are possible; however, for today's memory systems, zero is preferred. Additional input data words for storage at incremented column address locations are latched by /CAS on successive /CAS active transitions. Input data from the input latches 34 is passed along data path 32 to the memory array where it is stored at the location selected by the row and column address decoders. As in the burst read cycle previously described, a predetermined number of burst access writes are performed without the requirement of additional column addresses being provided on the address lines 16. After the predetermined number of burst writes occur, a subsequent /CAS pulse latches a new beginning column address, and another burst read or write access begins.

The memory device of FIG. 1 may include the option of switching between burst EDO and standard EDO modes of operation. In this case, the write enable signal /WE 36 is used at the row address latch time (/RAS falling, /CAS high) to determine whether memory accesses for that row are burst or page mode cycles. If /WE is low when /RAS falls, burst access cycles are selected. If /WE is high at /RAS falling, standard extended data out (EDO) page mode cycles are selected. Both the burst and EDO page mode cycles allow for increased memory device operating frequencies by not requiring the data output drivers 34 to place the data lines 10 in a high impedance state between data read cycles while /RAS is low. DRAM control circuitry 38, in addition to performing standard DRAM control functions, controls the I/O circuitry 34 and the column address counter/latch 26 in accordance with the mode selected by /WE when /RAS falls. In a burst mode only DRAM, or in a device designed with an alternate method of switching between burst and non-burst access cycles, the state of /WE when /RAS falls may be used to switch between other possible modes of operation such as interleaved versus linear addressing modes.

The write enable signal is used in burst access cycles to select read or write burst accesses when the initial column address for a burst cycle is latched by /CAS. /WE low at the column address latch time selects a burst write access. /WE high at the column address latch time selects a burst read access. The level of the /WE signal must remain high for read and low for write burst accesses throughout the burst access. A low to high transition within a burst write access terminates the burst access, preventing further writes from occurring. A high to low transition on /WE within a burst read access likewise terminates the burst read access and places the data output 10 in a high impedance state. Transitions of the /WE signal may be locked out during critical timing periods within an access cycle in order to reduce the possibility of triggering a false write cycle, and/or to guarantee the completion of a write cycle once it has begun. After the critical timing period the state of /WE determines whether a burst access continues, is initiated, or is terminated. Termination of a burst access places the DRAM in a state to receive another burst access command. Both /RAS and /CAS going high during a burst access also terminates the burst access cycle placing the data drivers in a high impedance output state. Read data may remain valid at the device outputs if /RAS alone goes high while /CAS is active for compatibility with hidden refresh cycles, otherwise /RAS high alone may be used to terminate a burst access. A minimum write enable pulse width is only required when it is desired to terminate a burst read and then begin another burst read, or terminate a burst write prior to performing another burst write with a minimum delay between burst accesses. In the case of burst reads, /WE transitions from high to low to terminate a first burst read, and then /WE transitions back high prior to the next falling edge of /CAS in order to specify a new burst read cycle. For burst writes, /WE transitions high to terminate a current burst write access, then back low prior to the next falling edge of /CAS to initiate another burst write access. A minimum /WE pulse width may be specified to guarantee recognition of the /WE pulse despite /WE lockout periods. If no /WE lockout circuit is used, termination of a burst access may be edge sensitive to the /WE signal.

A basic implementation of the device of FIG. 1 may include a fixed burst as length of 4, a fixed /CAS latency of 2 and a fixed interleaved sequence of burst addresses. This basic implementation requires very little additional circuitry to the standard EDO page mode DRAM, and may be mass produced to provide the functions of both the standard EDO page mode and burst EDO DRAMs. This device also allows for the output enable pin (/OE) to be grounded for compatibility with many SIMM module designs. When not disabled (tied to ground), /OE is an asynchronous control which prevents data from being driven from the part in a read cycle if it is inactive (high) prior to /CAS falling and remains inactive beyond /CAS rising. If these setup and hold conditions are not met, then the read data may be driven for a portion of the read cycle. It is possible to synchronize the /OE signal with /CAS, however this typically increases the /CAS to data valid delay time and doesn't allow for the last output data to be disabled prior to /RAS high without an additional /CAS low pulse which would otherwise be unnecessary. In a preferred embodiment, if /OE transitions high at any time during a read cycle the outputs remain in a high impedance state until the next falling edge of /CAS despite further transitions of the /OE signal.

Programmability of the burst length, /CAS latency and address sequences may be accomplished through the use of a mode register 40 which latches the state of one or more of the address input signals 16 or data signals 10 upon receipt of a write-/CAS-before-/RAS (WCBR) programming cycle. In such a device, outputs 44 from the mode register control the required circuits on the DRAM. Burst length options of 2, 4, 8 and full page as well as /CAS latencies of 1, 2 and 3 may be provided. Other burst length and latency options may be provided as the operating speeds of the device increase, and computer architectures evolve. The device of FIG. 1 includes programmability of the address sequence by latching the state of the least significant address bit during a WCBR cycle. The burst length and /CAS latency for this particular embodiment are fixed. Other possible alterations in the feature sets of this DRAM include having a fixed burst mode only, selecting between standard fast page mode (non-EDO) and burst mode, and using the output enable pin (/OE) 42 in combination with /RAS to select between modes of operation. Also, a WCBR refresh cycle could be used to select the mode of operation rather than a control signal in combination with /RAS. A more complex memory device may provide additional modes of operation such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of /WE and /OE at /RAS falling time. One mode from a similar set of modes may be selected through the use of a WCBR cycle using multiple address or data lines to encode the desired mode. Alternately, a device with multiple modes of operation may have wire bond locations, or programmable fuses which may be used to program the mode of operation of the device.

A preferred embodiment of a sixteen bit wide burst EDO mode DRAM designed in accordance with the teachings of

this invention has two column address strobe input pins /CASH and /CASL. For read cycles only one /CAS signal needs to toggle. The second /CAS may remain high or toggle with the other /CAS. During burst read cycles, all sixteen data bits will be driven out of part during a read cycle even if one /CAS remains inactive. In a typical system application, a microprocessor reads all data bits on a data bus in each read cycle, but may only write certain bytes of data in a write cycle. Allowing one of the /CAS control signals to remain static during read cycles helps to reduce overall power consumption and noise within the system. For burst write access cycles, each of the /CAS signals (CASH and /CASL) acts as a write enable for an eight bit width of the data. The two /CAS's are combined in an AND function to provide a single internal /CAS which will go low when the first external /CAS falls, and returns high after the last external /CAS goes high. All sixteen data inputs are latched when the first of the /CAS signals transitions low. If only one /CAS signal transitions low, then the eight bits of data associated with the /CAS that remained high are not stored in the memory.

The present invention has been described with reference to several preferred embodiments. Just as fast page mode DRAMs and EDO DRAMs are available in numerous configurations including x1, x4, x8 and x16 data widths, and 1 Megabit, 4 Megabit, 16 Megabit and 64 Megabit densities; the memory device of the present invention may take the form of many different memory organizations. It is believed that one who is skilled in the art of integrated circuit memory design can, with the aide of this specification design a variety of memory devices which do not depart from the spirit of this invention. It is therefore believed that detailed descriptions of the various memory device organizations applicable to this invention are not necessary.

It should be noted that the pinout for this new burst EDO memory device may be identical to the pinout for a standard EDO DRAM. The common pinout allows this new device to be used in existing memory designs with minimum design changes. The common pinout also allows for ease of new designs by those of skill in the art who are familiar with the standard EDO DRAM pinout. Variations of the described invention which maintain the standard EDO DRAM pinout include driving the /CAS pin with a system clock signal to synchronize data access of the memory device with the system clock. For this embodiment, it may be desirable to use the first /CAS active edge after /RAS falls to latch the row address, a later edge may be used to latch the first column address of a burst access cycle. After row and column addresses are latched within the device, the address may be incremented internally to provide burst access cycles in synchronization with the system clock. Other pin function alternatives include driving the burst address incrementing signal on the /OE pin since the part does not require a data output disable function on this pin. Other alternate uses of the /OE pin also allow the device to maintain the standard EDO pinout, but provide increased functionality such as burst mode access. The /OE pin may be used to signal the presence of a valid column starting address, or to terminate a burst access. Each of these embodiments provides for a high speed burst access memory device which may be used in current memory systems with a minimum amount of redesign.

FIG. 2 is a timing diagram for performing a burst read followed by a burst write of the device of FIG. 1. In FIG. 2, a row address is latched by the /RAS signal. /WE is low when /RAS falls for an embodiment of the design where the state of the /WE pin is used to specify a burst access cycle at /RAS time, otherwise /WE may be a "don't care" when /RAS falls. Next, /CAS is driven low with /WE high to initiate a burst read access, and the initial column address is latched. The data out signals (DQ's) are not driven in the first /CAS cycle. On the second falling edge of the /CAS signal the internal address generation circuitry provides a column address, and another access of the array begins. The first data out is driven from the device following the second /CAS and a /CAS to data access time (tCAC) delay. Additional burst access cycles continue, for a device with a specified burst length of four, until the fifth falling edge of /CAS which latches a new column address for a new burst read access. /WE falling in the fifth /CAS cycle terminates the burst access, and initializes the device for additional burst accesses. The sixth falling edge of /CAS with /WE low is used to latch a new burst address, latch input data and begin a burst write access of the device. Additional data values are latched on successive /CAS falling edges until /RAS rises to terminate the burst access.

It should be noted from FIG. 2 that for burst read cycles the data remains valid on the device outputs as long as the /OE pin is low, except for brief periods of data transition. Also, since the /WE pin is low prior to or when /CAS falls, the data input/output lines are not driven from the part during write cycles, and the /OE pin is a "don't care". Only the /CAS signal and the data signals toggle at relatively high frequency, and no control signals other than /CAS are required to be in an active or inactive state for one /CAS cycle time or less. This is in contrast to SDRAMs which often require row address strobes, column address strobes, data mask, and read/write control signals to be valid for one clock cycle or less for various device functions. Typical page mode DRAMs also allow for the column address to propagate through to the array to begin a data access prior to /CAS falling. This is done to provide fast data access from /CAS falling if the address has been valid for a sufficient period of time prior to /CAS falling for the data to have been accessed from the array. In these designs an address transition detection circuit is used to restart the memory access if the column address changes prior to /CAS falling. In a preferred embodiment of the design, the address counter is advanced on /CAS rising edges, and the address generated in the counter is then presented to the array on the next /CAS falling edge when the device is in a burst access mode.

FIG. 3 is block level schematic of a data path portion of the device of FIG. 1. In FIG. 3, data written to the memory device is received on data I/O pad 100. The write data is passed through input circuit 102 to a global sense amp 66 over write data lines 103. For this example, the sense amplifier includes an I/O line multiplexer 104 which is used to select a path from local I/O data line pair 106 to one of two pairs of array I/O lines 108 and 110. Write data is driven from write data lines 103 to I/O lines 106 when enabled by a logical combination of the equilibrate signal 70 and the write enable signal 68 from timing circuit 59 and data path control circuit 124 of central logic circuitry 52. In this example array I/O lines 108 are coupled to an adjacent section of the array (not shown). Array I/O lines 110 are true and compliment lines coupled to a local array sense amplifier 112 which is part of array section 64. Column select signal 114 from column driver 115 couples array data I/O lines 110 to a pair of complimentary digit lines 116 inside the local sense amplifier 112. One of the complimentary digit lines is coupled to a memory cell 118 through an access device which is selected by a signal on word line 120 from a row address decoder.

Read data follows the same path from the memory cell to the global sense amp where it is then driven on complimen-

tary data read lines 122 to complimentary data lines 126 under control of data path control logic 124 and timing circuits 59. Output circuit 128 drives data from the memory device in accordance with the mode of operation (burst EDO mode, EDO mode, Fast Page Mode, etc.).

This specific embodiment is not intended to provide an exhaustive description of all forms of the present invention. For example, I/O line multiplexer 104 would not be necessary if there is a global sense amp 67 for each pair of array I/O lines. Alternatively, additional array I/O lines could be multiplexed through the multiplexer 104 to allow for even fewer global sense amplifiers. Another variation is to allow read and write data to share a common path between the global sense amplifiers and the I/O pad. Also, separate input and output data pins can be provided. Numerous additional variations are possible and will be recognized by one of skill in the art.

FIG. 4 is a schematic diagram providing additional detail for portions of the circuitry of FIG. 3. In FIG. 4, /WE and /CAS are logically combined in command latch and control circuit 154. The write command output of circuit 154 is buffered through driver 156 to write command signal line 158. The write command is coupled to a plurality of sense amps 66 through a distributed line resistance represented by resistor 160 over a signal line with distributed capacitive load represented by capacitor 162. Write signal 164 arriving at the sense amplifier will be a delayed version of the output of the write command from the command latch.

Address inputs 170 are coupled to burst address generator 173 which provides a column address 175 to the memory array. The column address and a version of the write command 176 are used to generate an equilibrate signal 182. Equilibration control signal 182 passes through distributed resistance 184, and is loaded by distributed capacitance 186. A delayed version of the equilibrate signal 188 is coupled to the sense amp 66. Local write driver enable circuit 200 allows write cycle data 103 to be driven for a maximum write cycle time by disabling the write data drivers 240–256 during equilibration of the complimentary data I/O lines 106. The data I/O lines are equilibrated when equilibration device 232 couples the true and compliment lines together in response to the equilibration control signal 222.

For a maximized data write cycle time, the write command 164 can remain active throughout a burst write access. In this case, the write drivers are enabled and disabled by the equilibrate signal which will occur at the beginning of each access cycle. For nonburst mode operation, it is beneficial to provide the write command prior to the end of the equilibrate function to allow the write to begin as soon as possible. For these devices, the write will typically end prior to the next /CAS falling edge to allow the device to meet the column address to data valid access time in (TAA). For EDO devices in particular, the page mode cycle time is very short, but the address access time begins while /CAS is high, so the write cycles should end as soon as possible. One way to allow the write cycle to end as soon as possible is to begin it immediately after the equilibrate is complete.

It is important to note that devices 250 and 256 will generally be enabled simultaneously, as will devices 252 and 254. If the enable gate 212 were not locally present, then the write enable signal would need to be delayed from the equilibrate disable time to guarantee that a current path through devices 250, 232 and 256 or devices 252, 232 and 254 does not exist.

FIG. 5 is a schematic diagram of a portion of the column address path of the device of FIG. 1 shown generally as block 26. In FIG. 5 address 16 is coupled to address buffers 305 and 320 which may be located within block 26 of FIG. 1 or at a remote location of the integrated circuit (near address input pads for example). The output of address buffer 305 is coupled to burst address generator 310. Burst address 330 from the burst address generator is coupled to multiplexer 370 through multiplexer 350 and address lines 360. Multiplexer 370 selects either the buffered address 340 from address buffer 320 or the burst address 360 to be latched in latch 380. Latched column address 390 is coupled to a column address buffer 400 which drives the column address to the column address decoder 30 of FIG. 1 to select a column of the memory array. The output of latch 380 is also coupled to an asynchronous address transition detection circuit 420 which generates an equilibration control signal 430 at the beginning of each memory access in response to detected changes in the column address 390. Latched address 390 is also fed back to multiplexer 350. In page mode operation, the multiplexer 370 selects the address from the address buffer 320, and the output of the burst address generator 310 is ignored.

In burst mode, the initial burst address is passed to the latch 370 from the address buffer 340 in response to the first falling /CAS transition. The multiplexer 370 will select the address from address lines 360 for subsequent column addresses within the burst access. The address generator 310 may advance the burst address on rising edges of /CAS. Multiplexer 350 will select the burst address from counter 310 in response to subsequent /CAS falling edges. After an address is latched, the multiplexers 350 and 370 select the address feedback path from 390 through 350, 360 and 370 until the next address is required. This allows the burst address generator to advance on each /CAS rising edge of the burst access.

In an alternate embodiment, the two multiplexers 350 and 370 may be combined into a single multiplexer to select the address from 330, 340 or 390. Another alternative embodiment eliminates the feedback path from address lines 390 to multiplexer 350 while providing additional control of latch 380 to latch the burst address except for a brief period of time after /CAS falls when a new burst address is allowed to pass through.

FIG. 6 is an alternate embodiment of the portion of the address path shown in FIG. 5. In FIG. 6, elements which have common functions with those of FIG. 5 have been given corresponding reference numbers. In FIG. 6, a single set of address buffers 320 are coupled to the address counter 310 and multiplexer 355. The latch 380 of FIG. 5 is no longer present, and multiplexers 350 and 370 of FIG. 5 have been combined into a single multiplexer 355. In page mode operation, the multiplexer 355 selects address lines 340 from the address buffer 320 while /CAS is high. This provides an asynchronous address path from the address buffer to the address transition detection circuit 420 so that the equilibration control signal 430 can be generated for each column address transition while /CAS is high. When /CAS falls, the multiplexer 355 selects feedback path 390 to effectively latch the column address. In burst mode, the initial burst address is passed through the multiplexer 355 in response to the first /CAS falling edge. The initial address is then latched by selecting feedback path 390. The initial address is also loaded into address generator 310 where it may be advanced on rising edges of /CAS. For each subsequent falling edge of /CAS within a burst access, the multiplexer will select lines 330 to provide the next burst address to buffer 400 and address transition detection circuit 420. Then address path 390 is again selected to latch the address which allows the

address generator to again advance on the next rising edge of /CAS without disturbing the latched column address 390.

Variations on this embodiment which fall within the scope of the present invention include elimination of the feedback path 390 to the multiplexer in combination with the addition of an address latch between the address buffer 320 and the multiplexer. In this configuration, the latch will store the column address while /CAS is low in page mode, and the address generator will increment in response to falling edges of /CAS eliminating the requirement for a burst address latch or feedback path. The multiplexer may then simply select between a burst address path and a page mode address path. If the address generator is designed to pass the initial burst address from input address 16 through to address lines 330 for each new burst access, then the multiplexer select will only need to be changed when the part is switched between page mode and burst mode.

FIG. 7 is yet another embodiment of the portion of the address path shown in FIG. 5. In FIG. 7, input address 16 feeds page mode and burst mode address generator 315. In page mode operation, the input address is passed through address generator 315 while /CAS is high, and is latched within address generator while /CAS is low. In burst mode, an initial burst address is passed through the address generator in response to the first /CAS low of the burst access. Subsequent burst addresses are generated within the address generator and passed to address lines 390 on successive /CAS falling edges. Address generator 315 may comprise a counter which advances the burst address on rising /CAS edges, and a latch which drives the burst addresses to lines 390 in response to /CAS falling edges.

FIG. 8 is a schematic representation of a data processing apparatus designed in accordance with the present invention. For the purposes of this specification a microprocessor may be, but is not limited to, a central processing unit (CPU), a microprocessor, a microcontroller, a digital signal processor, or an arithmetic processor. In FIG. 8, microprocessor 112 is connected via address lines 114 and control lines 116 to a memory control circuit 118. The memory control circuit provides address and control signals on lines 122 and 120 respectively to a burst access memory device 124. The burst access memory device sends and receives data over data bus 126. Optional data bus buffer 130 between memory data bus 126 and microprocessor data bus 128 allows for amplification of the data signals, and/or synchronization with the microprocessor and memory control signals. A fast static random access memory (SRAM) cache circuit 132 is also optional and provides higher speed access to data stored in the cache from the memory circuit or the microprocessor. Memory control circuit 118 may be incorporated within the microprocessor. The memory control circuit provides the required address strobe signals and read/write control signals required for burst mode access of the memory circuit. By providing burst access of the memory by the processor, a computer with relatively high memory bandwidth can be designed without the requirement of a fast SRAM cache. SRAMs which are fast enough to provide memory access without wait states can significantly add to the cost of a computer. Thus the burst access memory device of the present invention allows for medium to high performance computers to be manufactured at a cost which is significantly less than those manufactured today. Use of the burst access memory device of the present invention in cooperation with a fast SRAM cache allows for an even higher performance computer design by providing fast access to main memory in the event of a cache miss.

In a burst write operation, the processor 112 provides an initial address and a write command to the memory controller. The memory controller provides a row address to the memory with a row address strobe. The memory controller then provides a write command, a column address and a column address strobe to the memory. The memory will equilibrate internal data I/O lines in response to receipt of the write command and column address. During the equilibrate operation, write data and write command signals are passed to global sense amplifiers within the burst access memory device. At the end of the equilibrate operation, write data drivers are enabled, and write data is stored in the memory array. In a preferred embodiment, positive (low to high) transitions of /CAS will cause an internal address counter of the memory device to advance to the next burst address. Negative (high to low) transitions of /CAS will then end the previous write cycle, and pass the burst address to the address transition detection circuit which will generate an equilibrate signal to equilibrate the I/O lines. The negative transition of /CAS will also allow the burst address from the counter to select a column of the array. Once the equilibration is complete, the next write will be performed at the burst address from the counter. In an alternate embodiment, a clock signal is input to a burst access device to control generation of a burst address from the counter (SDRAMs for example have a clock input pin).

In a burst read operation, the processor 112 provides an initial address and a read command to the memory controller. The memory controller provides a row address to the memory with a row address strobe. The memory controller then provides a read command, a column address and a column address strobe to the memory. The memory will equilibrate internal data I/O lines in response to receipt of the read command and column address. At the end of the equilibrate operation, data from the specified column of the array will be amplified and driven on the data I/O lines to the output buffer. In a preferred embodiment, positive (low to high) transitions of /CAS will cause an internal address counter of the memory device to advance to the next burst address. Negative (high to low) transitions of /CAS will then allow the burst address to pass to the address transition detection circuit which will generate an equilibrate signal to equilibrate the I/O lines. The negative transition of /CAS will also allow the burst address from the counter to select a column of the array. Once the equilibration is complete, the next read will be performed at the burst address from the counter. In an alternate embodiment, a clock signal is input to a burst access device to control generation of the burst address within the memory device.

Memory 124 may also operate in a page mode such as Fast Page Mode or EDO mode. Write commands at memory sense amps are enabled by the equilibrate signal becoming inactive at the sense amp. Using the equilibrate signal at the sense amp to gate the write signal to enable the write drivers eliminates wasted time associated with delaying the write driver enable signal to prevent excessive currents from flowing through the write drivers during the equilibration operation. In page mode, the column address is allowed to flow from the microprocessor asynchronously through to the address transition detection circuit while /CAS is high in order to generate an equilibration signal.

For the purposes of this specification a node may be, but is not limited to, an intersection of conductors, a circuit input or output, or any point along a signal path. For example, the write command may be said to enter the global sense amp at node 164 and device 250 of FIG. 4 is said to be connected to a power source at node 270. Also, the term signal may refer to but is not limited to information transferred along a conductor, or may refer to the conductor itself. For example,

It may be said that the equilibrate signal **188** is coupled to the sense amp **66**. In this context, the term signal represents a physical conductor for carrying the electrical information to equilibrate the data I/O lines, and is not limited to the electrical information itself which is not present when the device is not connected to a power source. The term "coupled" refers to but is not limited to a connection which may be made directly, after buffering, or through another element such as a resistor, capacitor, transistor, or logic device. Typically, a device will be responsive at some time to a signal or another device which is coupled to it.

While the present invention has been described with reference to preferred embodiments, numerous modifications and variations of the invention will be apparent to one of skill in the art without departing from the scope of the invention.

What is claimed is:

1. A method of operating address circuitry in a memory device, the method comprising:

receiving a first address from a source external to the memory device;

latching the first address;

generating a next address using an address generation circuit, the next address being generated based upon the first address;

providing a multiplexed signal by multiplexing either the first address or the next address to an address transition detection circuit for detecting a difference between a current address and a prior address;

latching the multiplexed signal; and

generating an equilibration signal if a difference is detected between the current address and the prior address.

2. The method of claim 1 wherein latching the multiplexed signal is performed by coupling an output of a multiplex circuit to an input of the multiplex circuit.

3. The method of claim 1 wherein the memory device is a synchronous dynamic random access memory (SDRAM).

4. The method of claim 1 wherein the next address is generated while the memory device is in a burst mode.

5. The method of claim 1 wherein the equilibration signal equilibrates input/output data communication lines.

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United States Patent [19]

Park et al.

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[45] **Date of Patent: May 20, 1997**

[54] **SYSTEM FOR SELECTING ONE OF A PLURALITY OF MEMORY BANKS FOR USE IN AN ACTIVE CYCLE AND ALL OTHER BANKS FOR AN INACTIVE PRECHARGE CYCLE**

[75] Inventors: **Churoo Park**, Suwon; **Hyun-Soon Jang**, Seoul; **Chull-Soo Kim**, Suwon; **Myung-Ho Kim**, Suwon; **Seung-Hun Lee**, Suwon; **Si-Yeol Lee**, Kyungki-do; **Ho-Cheol Lee**; **Tae-Jin Kim**, both of Seoul; **Yun-Ho Choi**, Suwon, all of Rep. of Korea

[73] Assignee: **Samsung Electronics Co., Ltd.**, Suwon, Rep. of Korea

[21] Appl. No.: **578,151**

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Oct. 2, 1992	[KR]	Rep. of Korea	18131
Apr. 27, 1993	[KR]	Rep. of Korea	7127

[51] **Int. Cl.**[6] **B01F 7/00**; B01F 13/00

[52] **U.S. Cl.** **365/203**; 365/228; 375/405; 375/475; 364/DIG. 1

[58] **Field of Search** 395/475, 405; 365/203, 228; 364/DIG. 1

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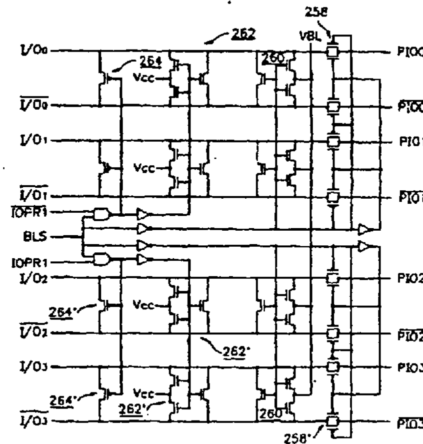
Primary Examiner—Reba I. Elmore
Assistant Examiner—J. Peikari
Attorney, Agent, or Firm—Cushman Darby & Cushman IP Group of Pillsbury Madison & Sutro LLP

[57] **ABSTRACT**

A synchronous dynamic random access memory capable of accessing data in a memory cell array therein in synchronism with a system clock from an external system such as a central processing unit (CPU). The synchronous DRAM receives an external clock and includes a plurality of memory banks each including a plurality of memory cells and operable in either an active cycle or a precharge cycle, a circuit for receiving a row address strobe signal and latching a logic level of the row address strobe signal in response to the clock, an address input circuit for receiving an externally generated address selecting one of the memory banks, and a circuit for receiving the latched logic level and the address from the address input circuit and for outputting an activation signal to the memory bank selected by the address and an inactivation signals to unselected memory banks when the latched logic level is a first logic level, so that the selected memory bank responsive to the activation signal operates in the active cycle while the unselected memory banks responsive to the inactivation signals operate in the precharge cycle.

1 Claim, 66 Drawing Sheets



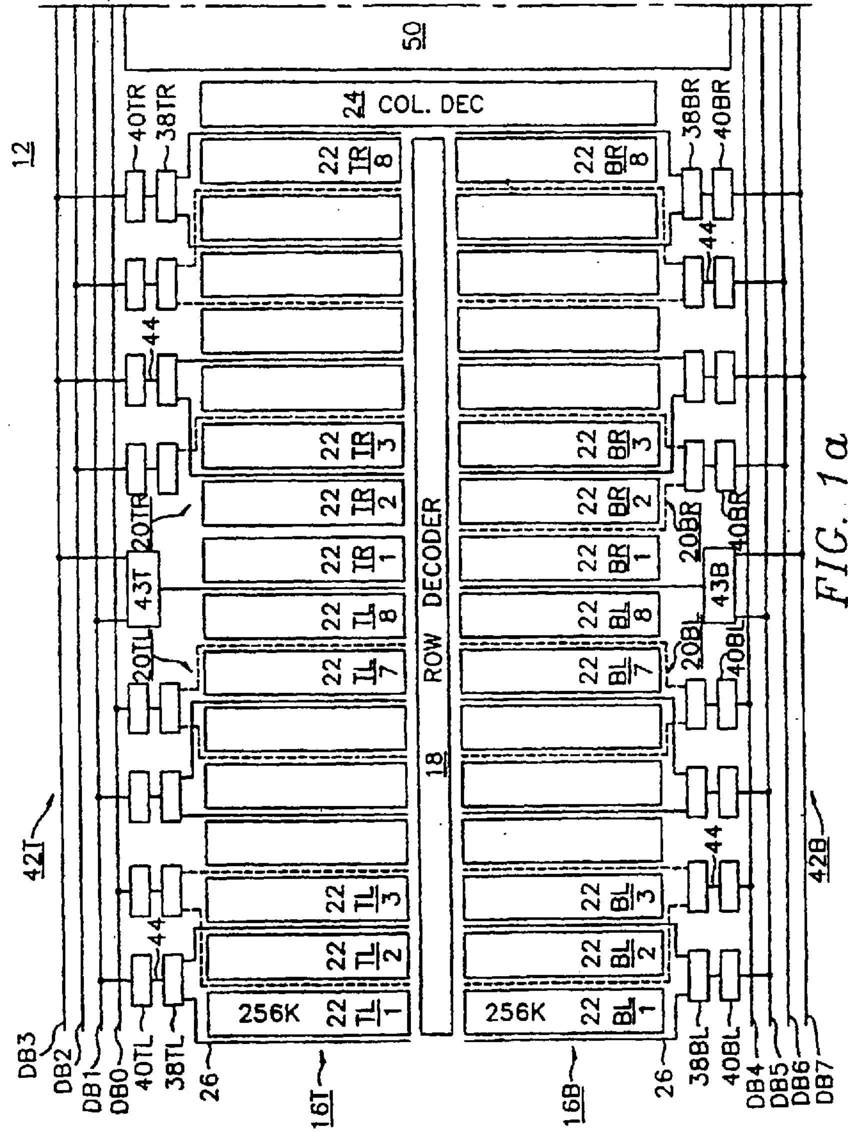


FIG. 1a

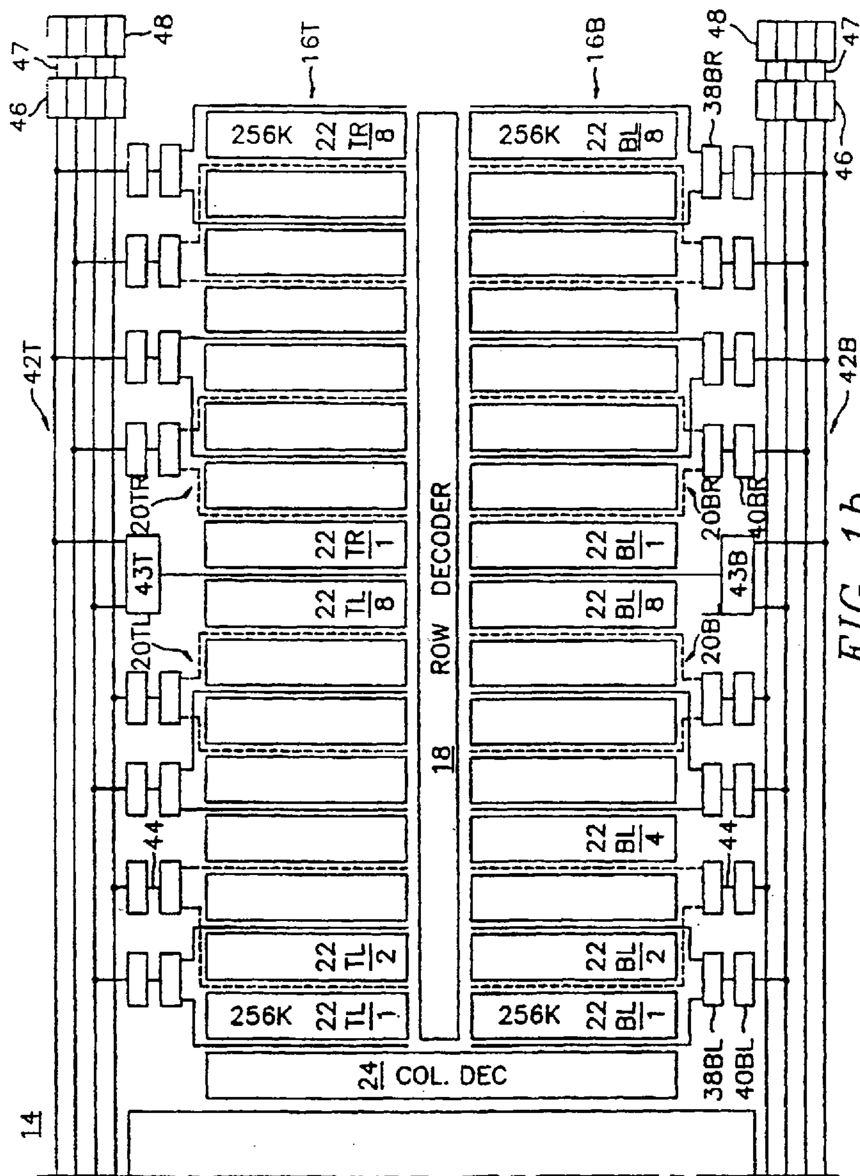


FIG. 1b

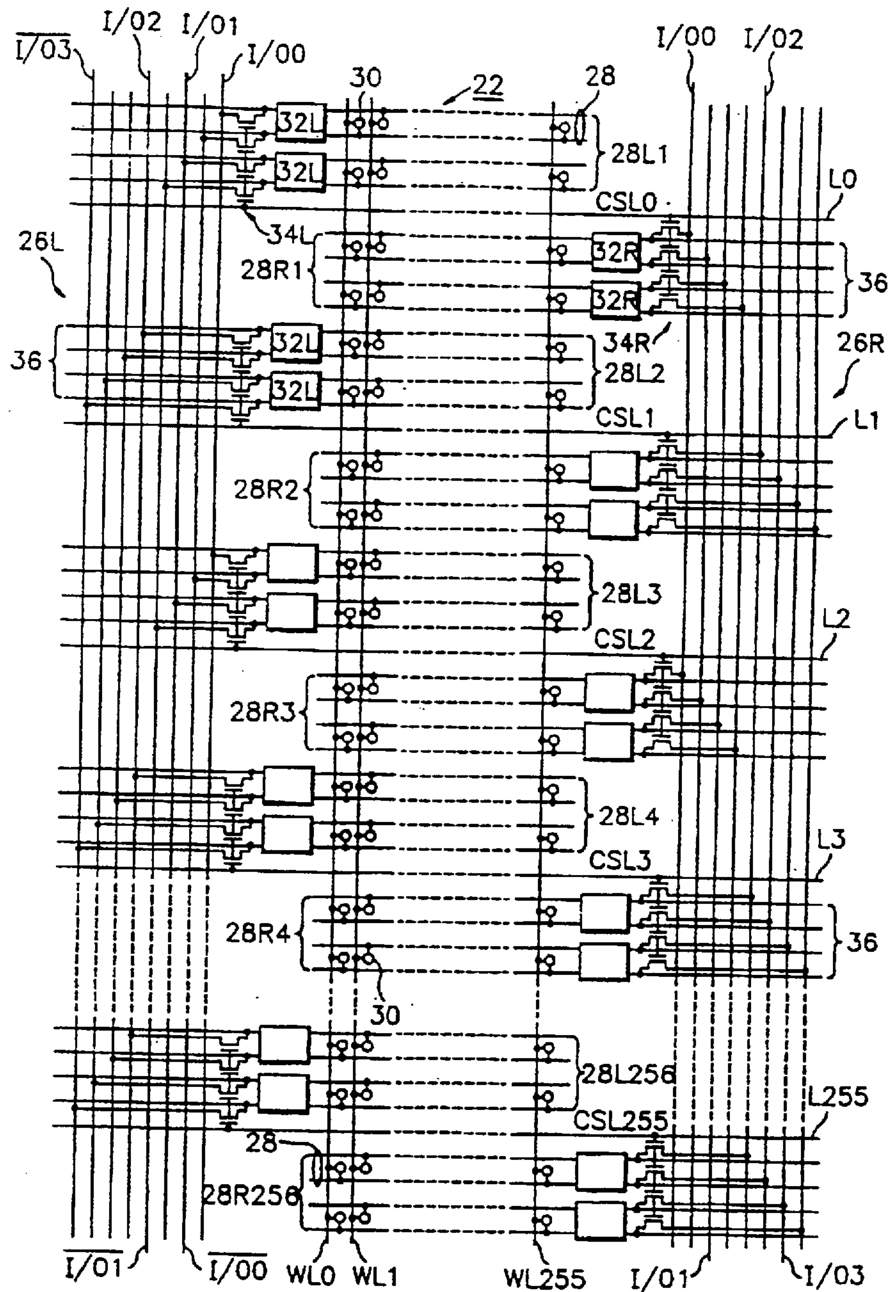


FIG. 2

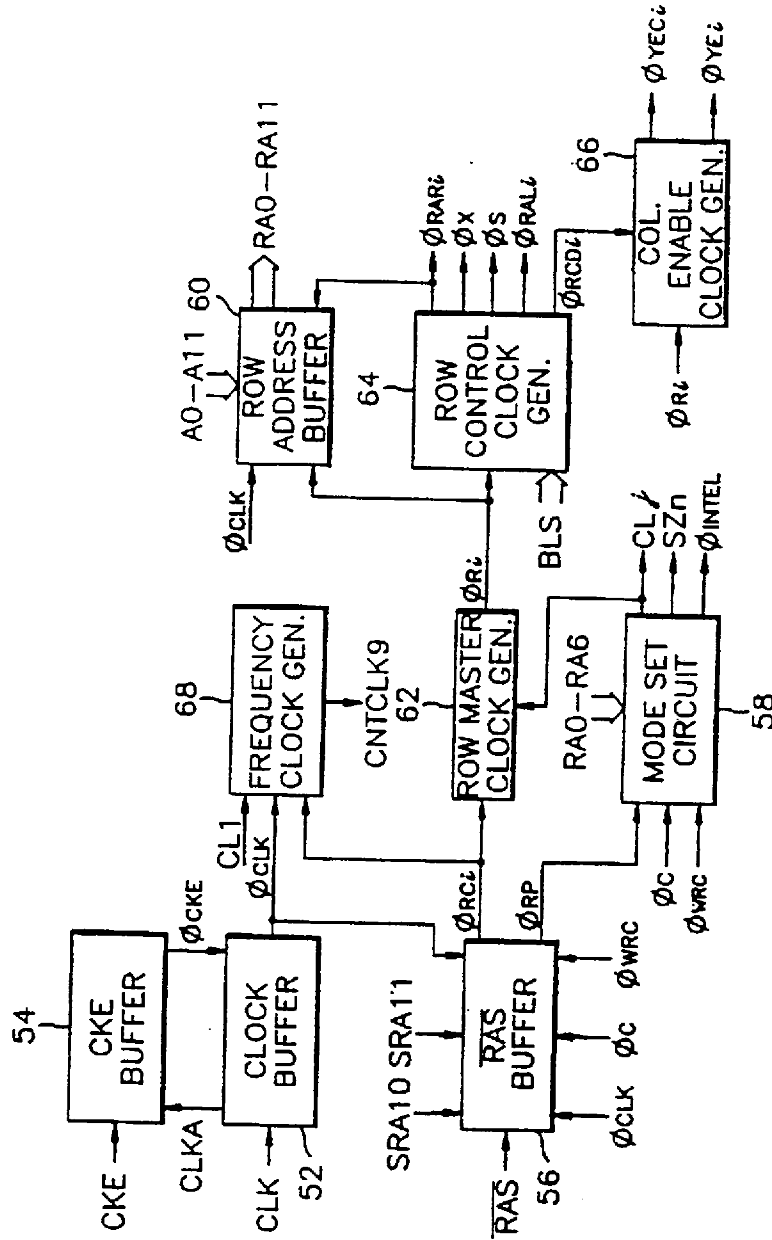
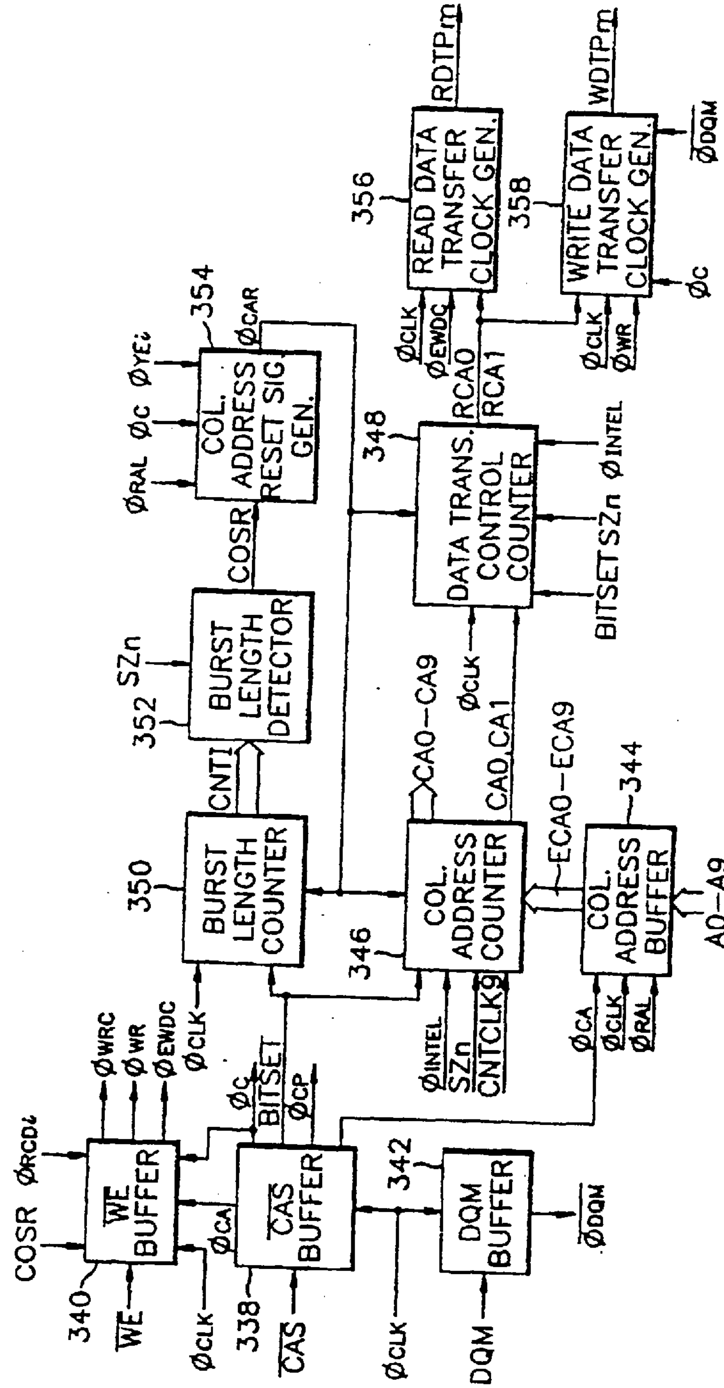


FIG. 3


WE BUFFER
CAS BUFFER
DQM BUFFER
BURST LENGTH COUNTER
BURST LENGTH DETECTOR
COL. ADDRESS RESET SIG. GEN.
COL. ADDRESS COUNTER
COL. ADDRESS BUFFER
DATA TRANS. CONTROL COUNTER
READ DATA TRANSFER CLOCK GEN.
WRITE DATA TRANSFER CLOCK GEN.
340
338
342
344
346
348
350
352
354
356
358
COSR
CNTI
SZn
RDTPm
WDTPm
RCA0
RCA1
CA0—CA9
CA0,CA1
ECA0—ECA9
A0—A9
BITSET
DQM
FIG. 4

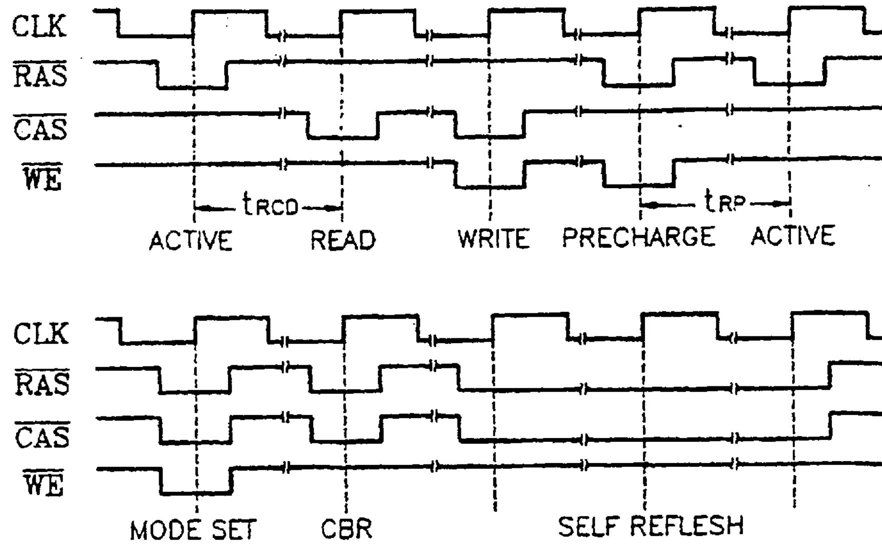


FIG. 5a

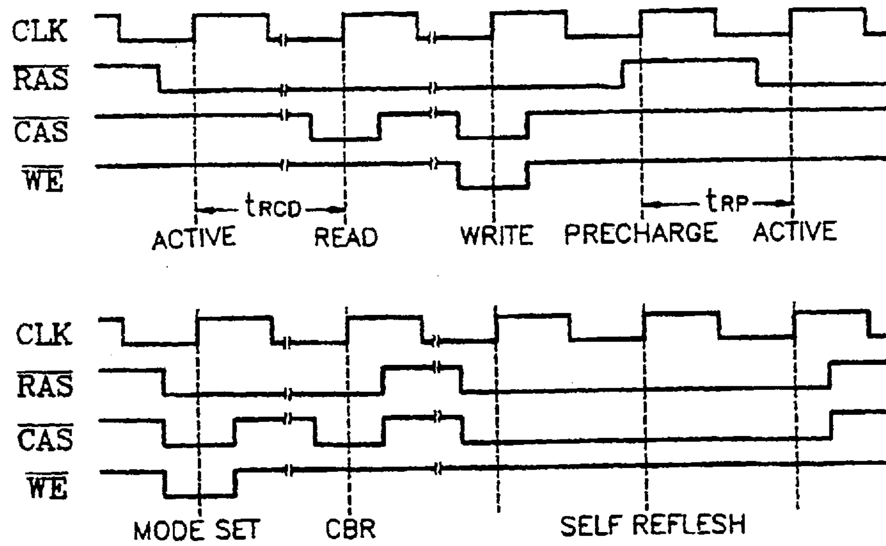


FIG. 5b

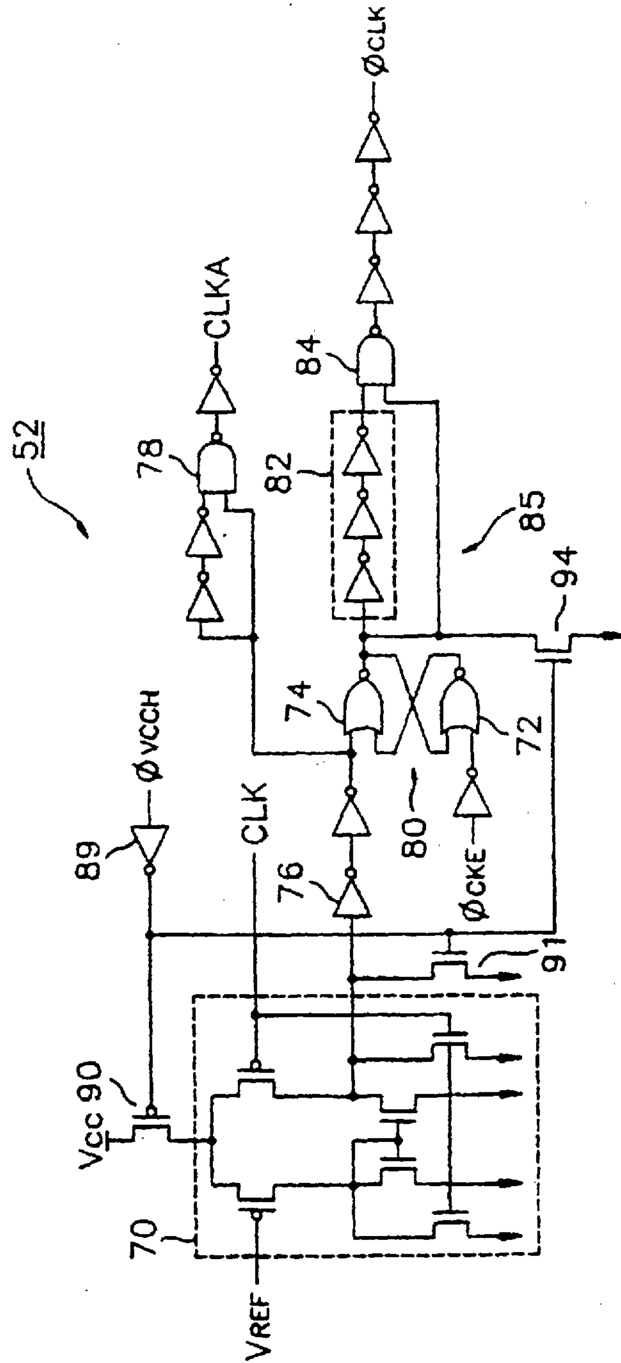


FIG. 6

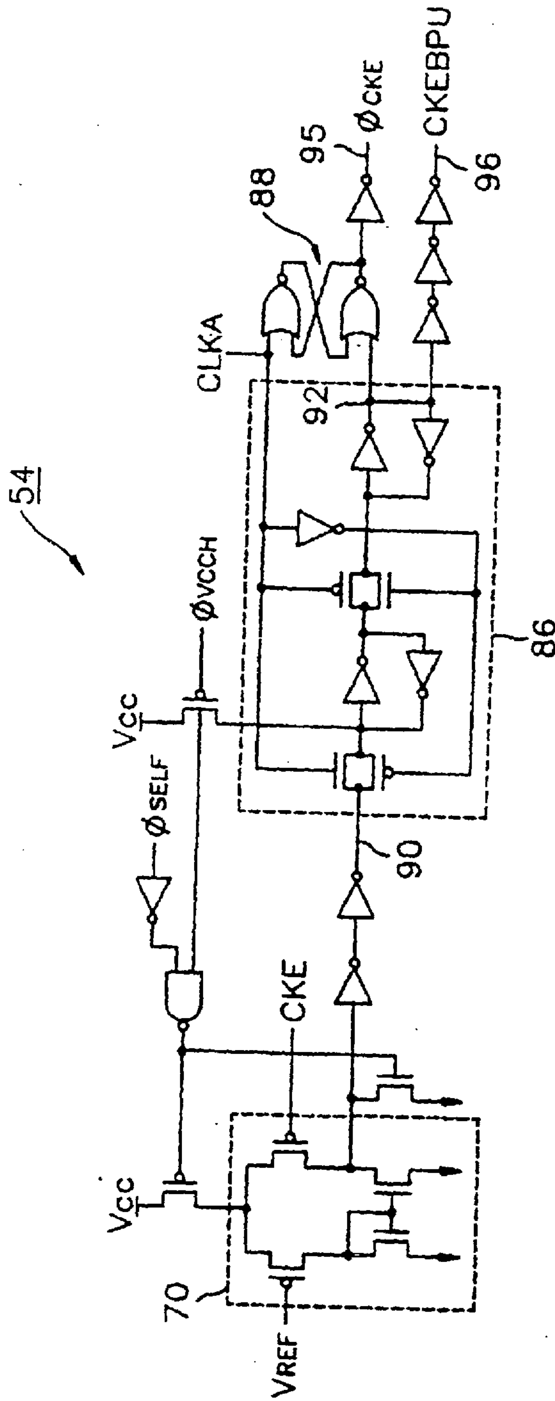


FIG. 7

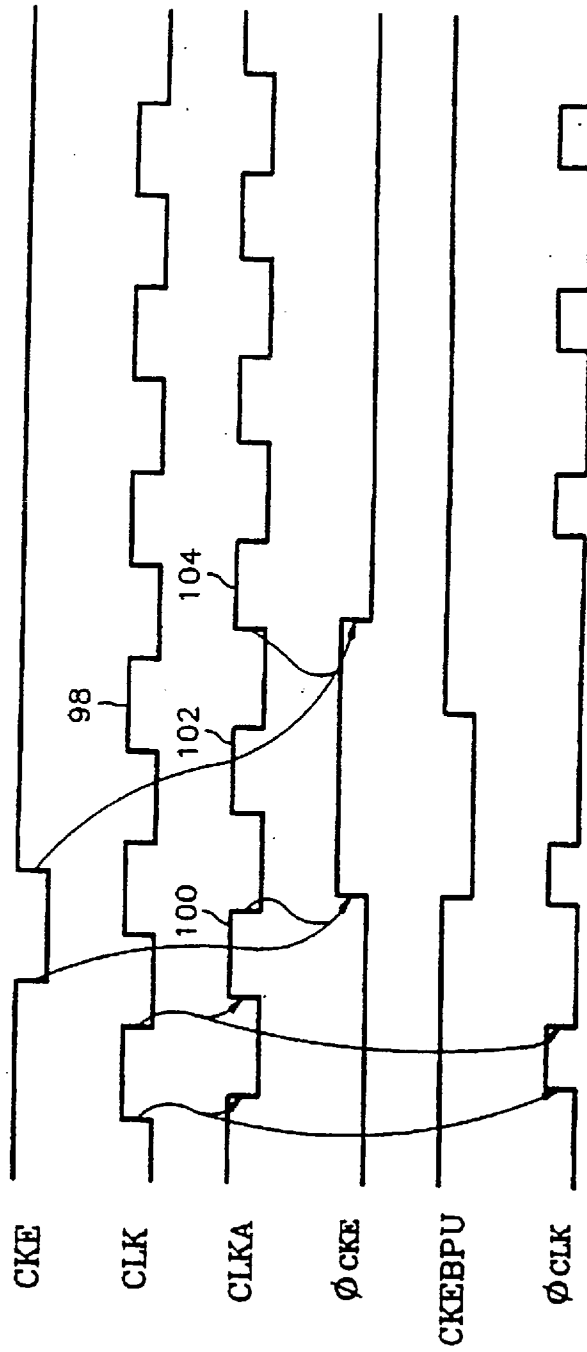


FIG. 8

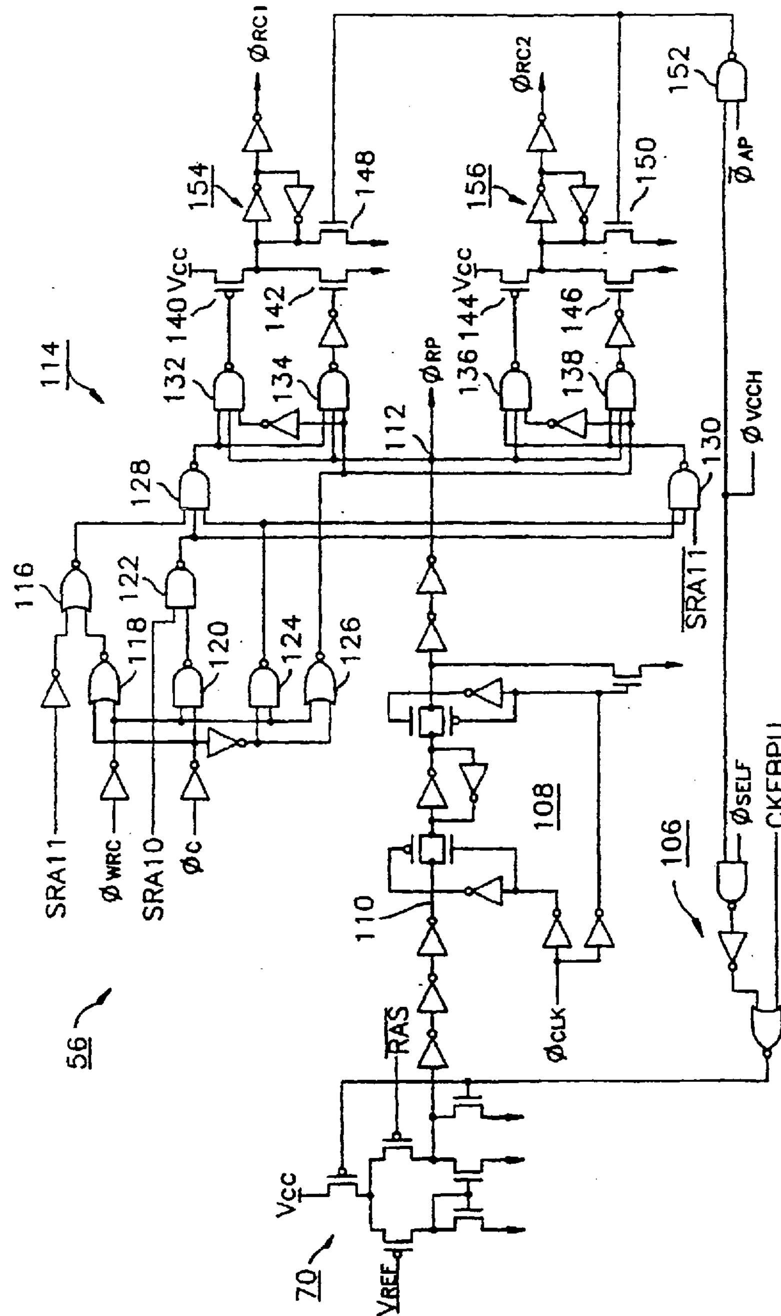


FIG. 9

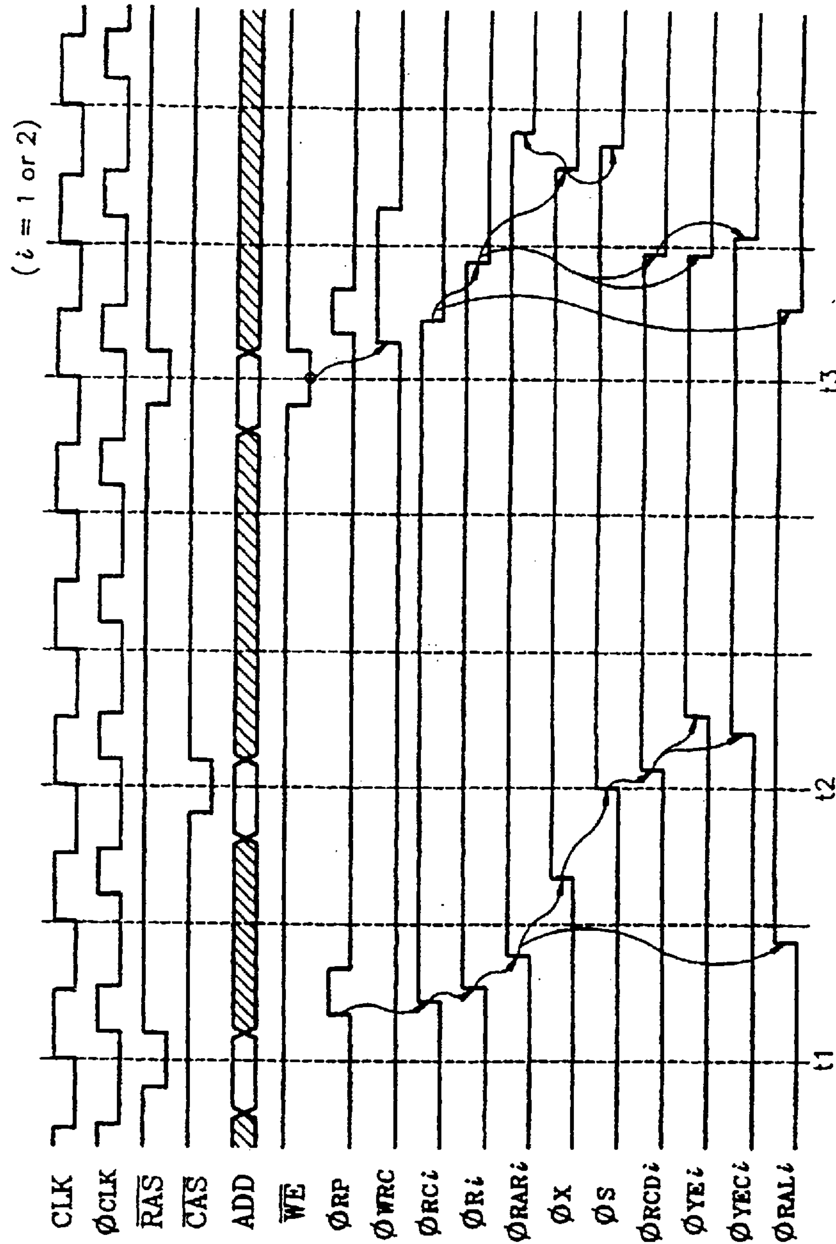


FIG. 10

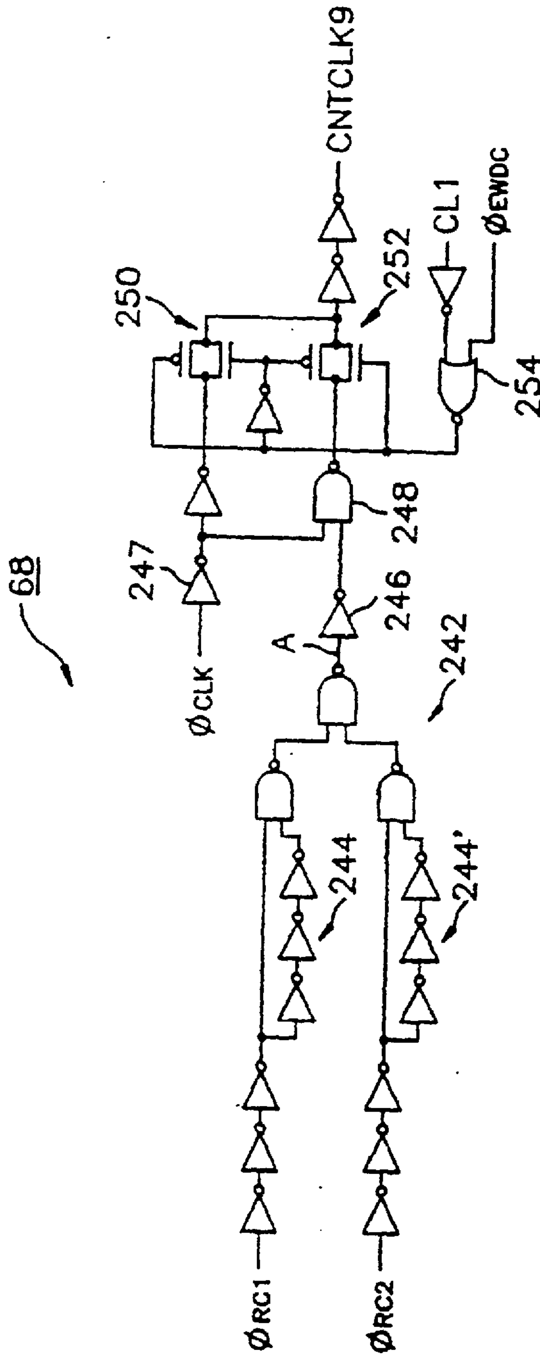


FIG. 11

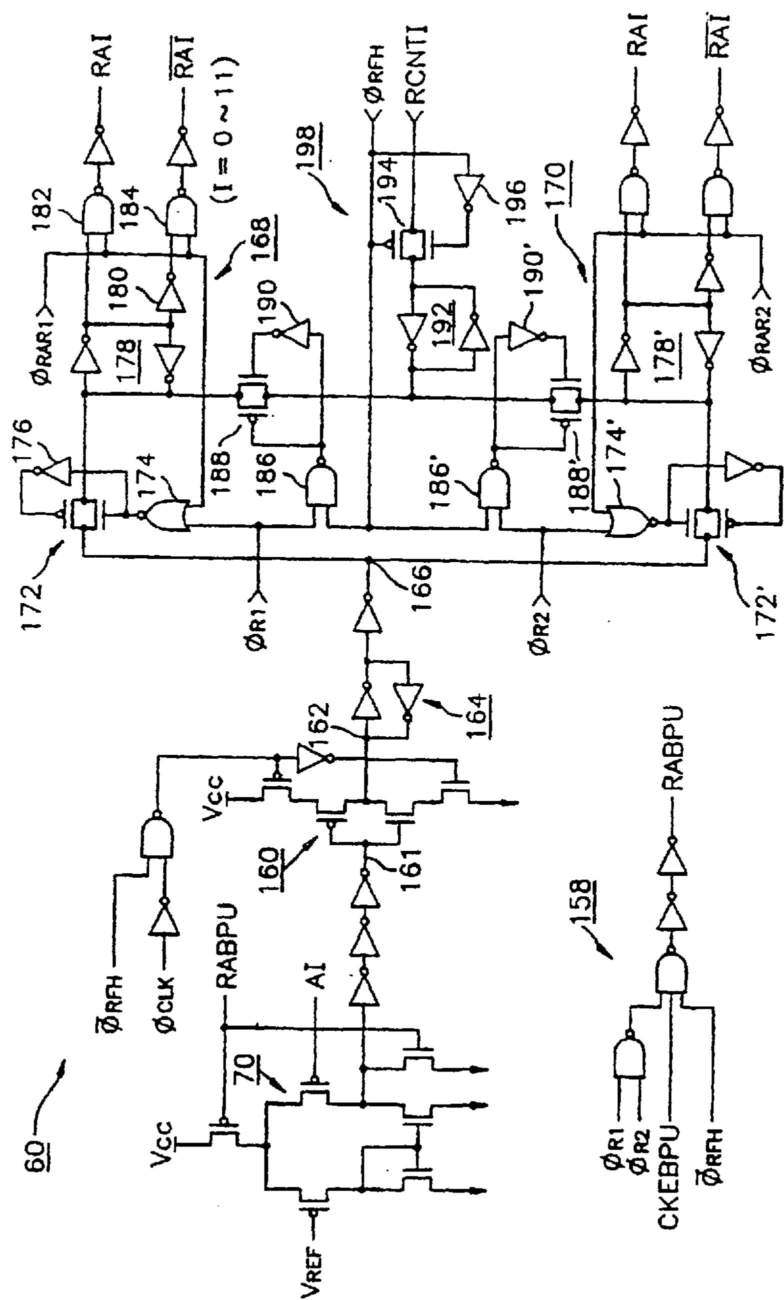


FIG. 12

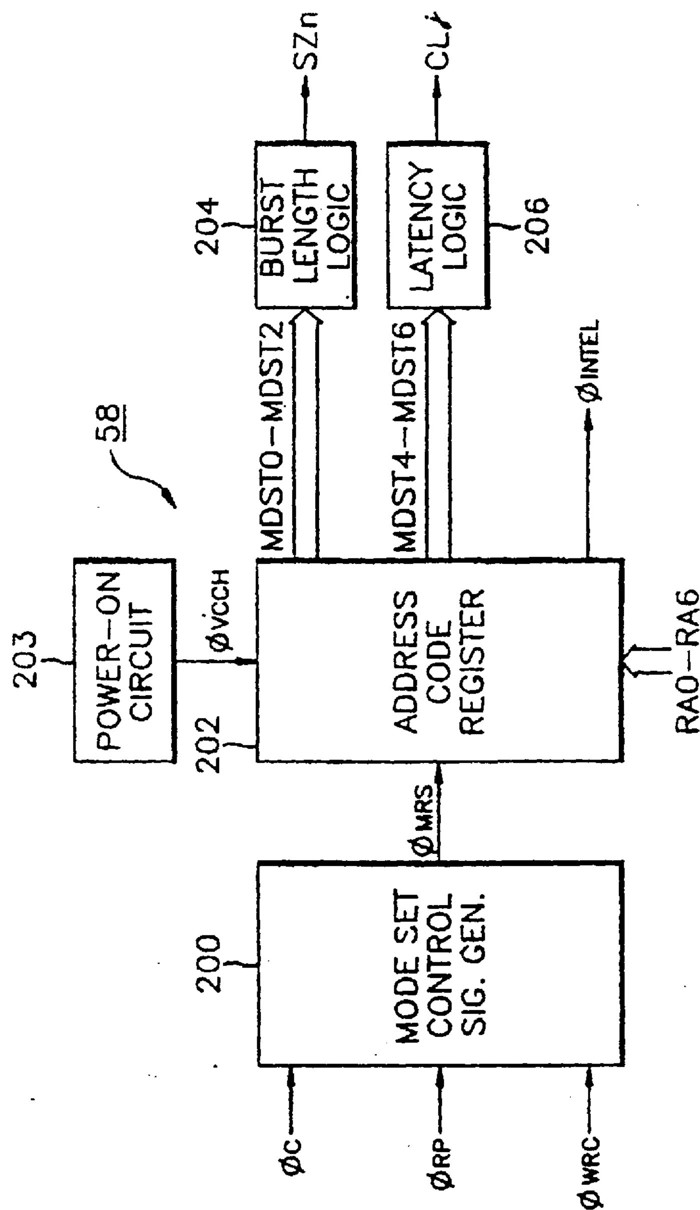


FIG. 13

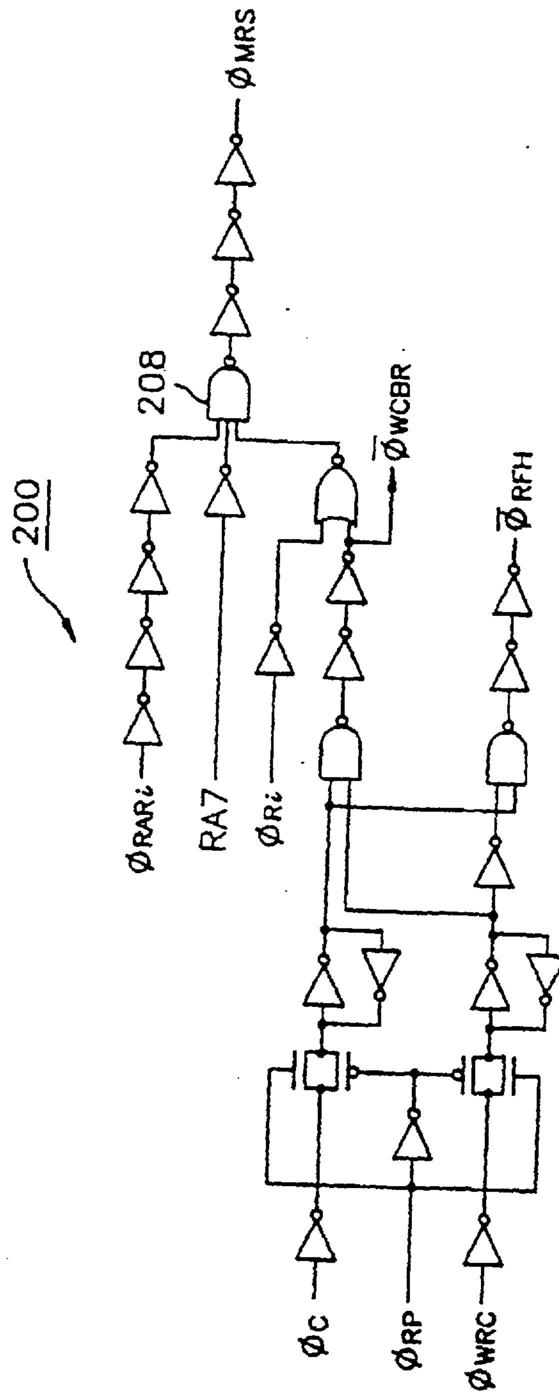


FIG. 14

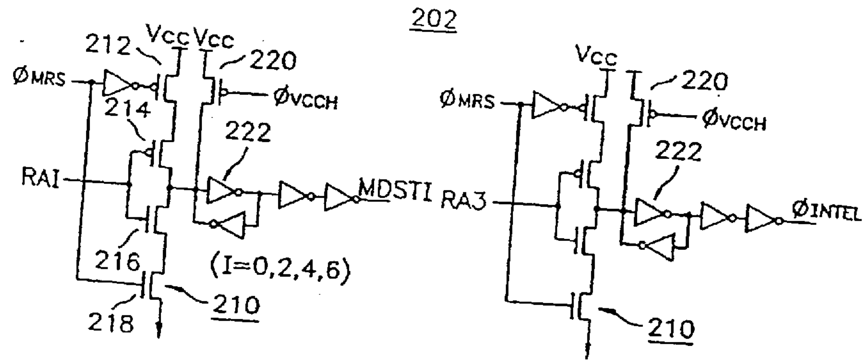


FIG. 15A

FIG. 15B

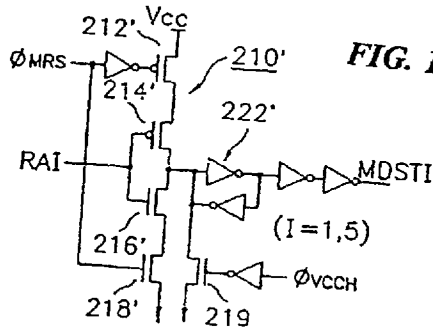


FIG. 15C

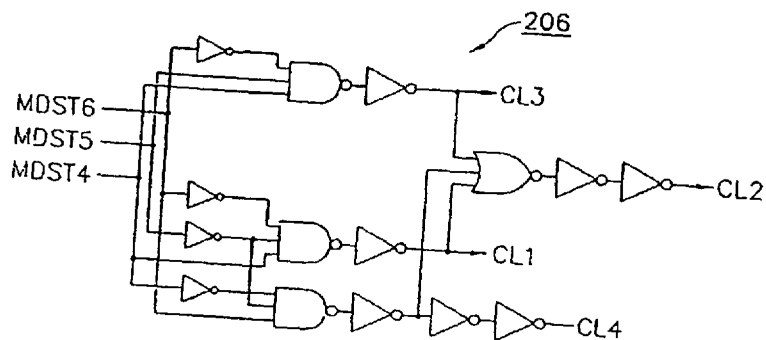


FIG. 16

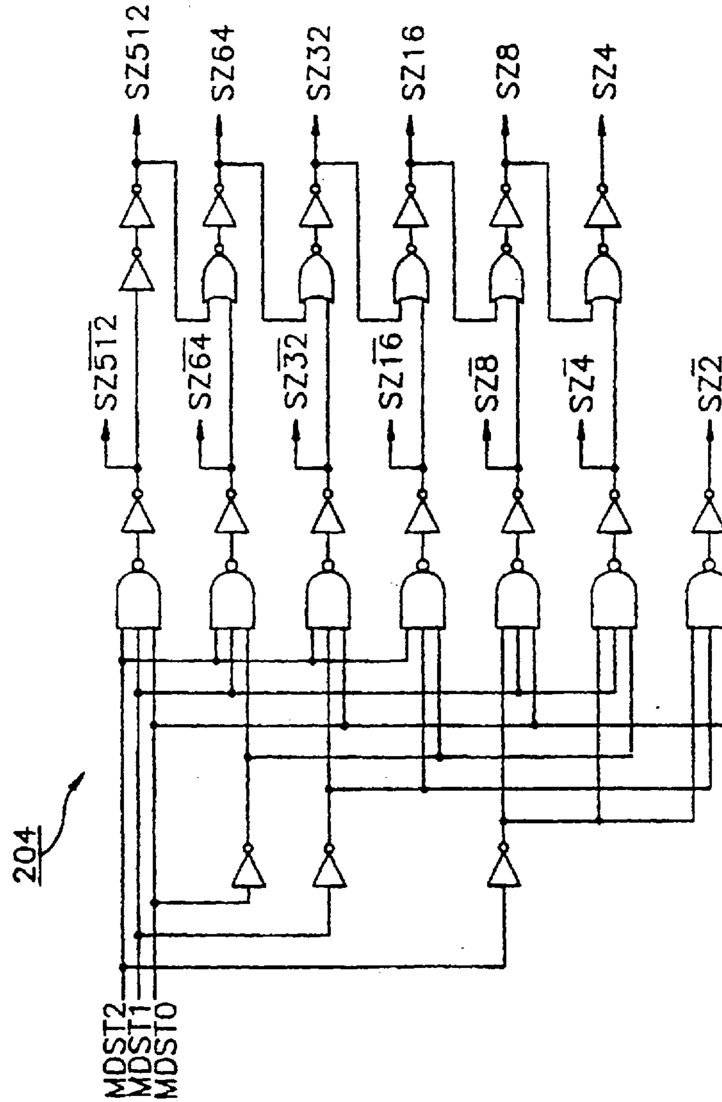


FIG. 17

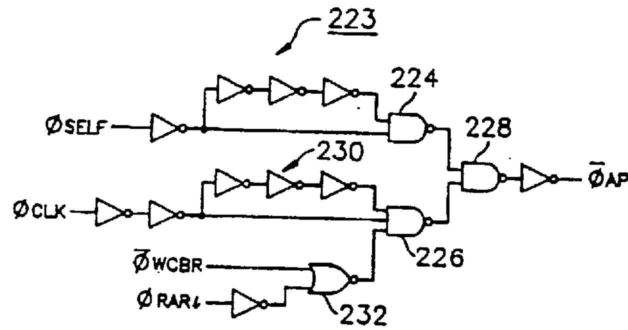


FIG. 18

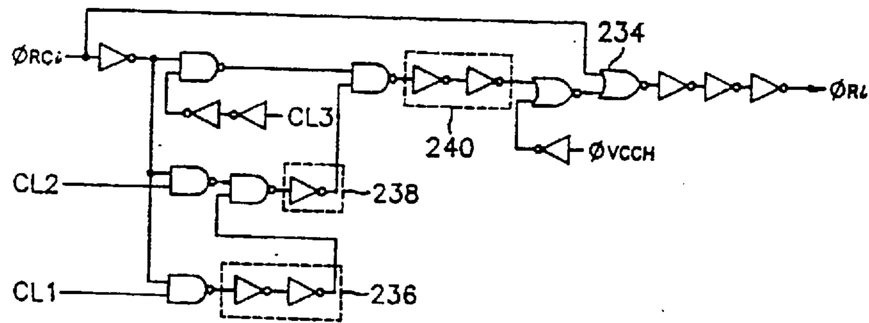


FIG. 19

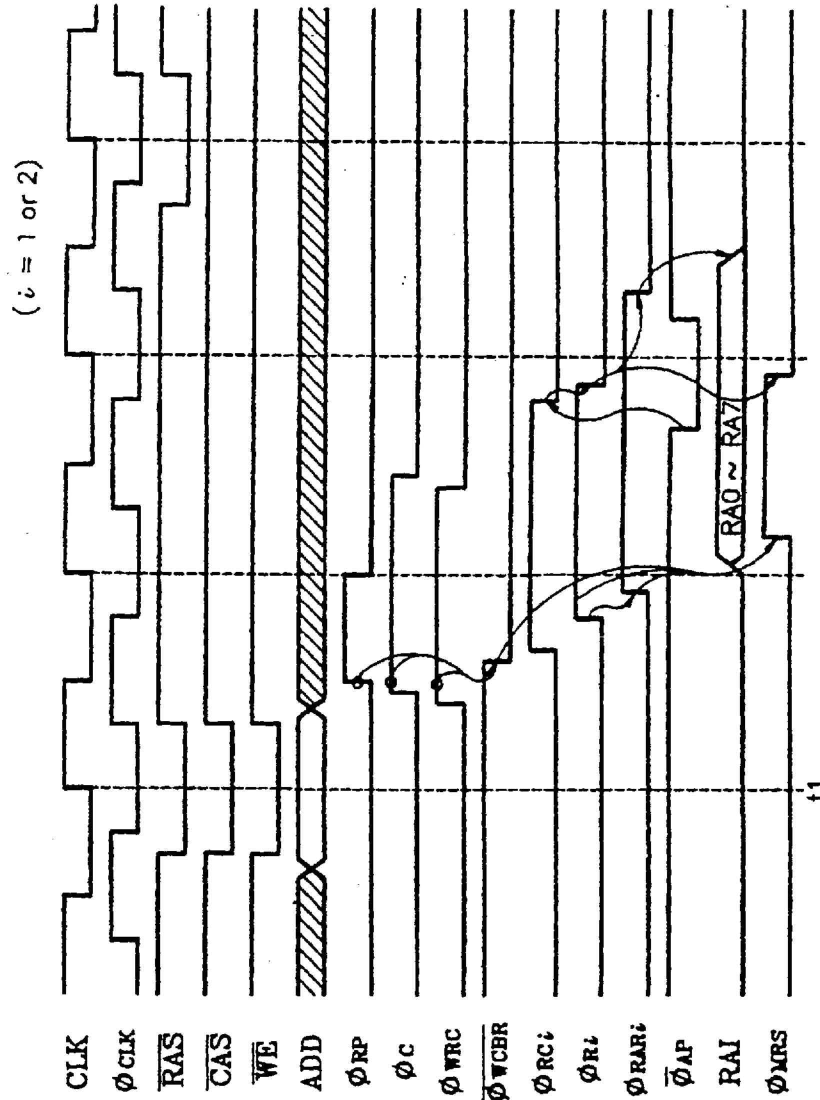


FIG. 20

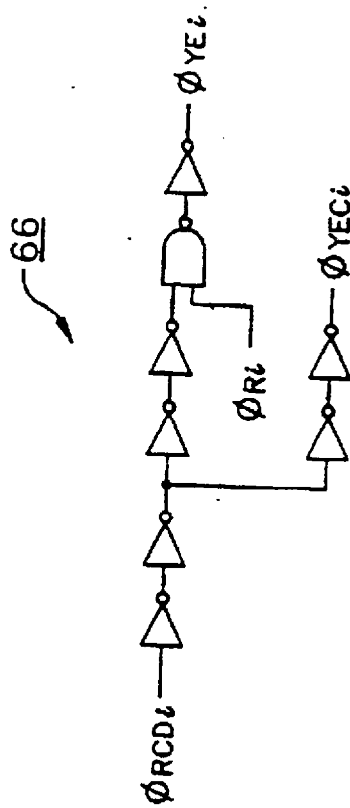


FIG. 21

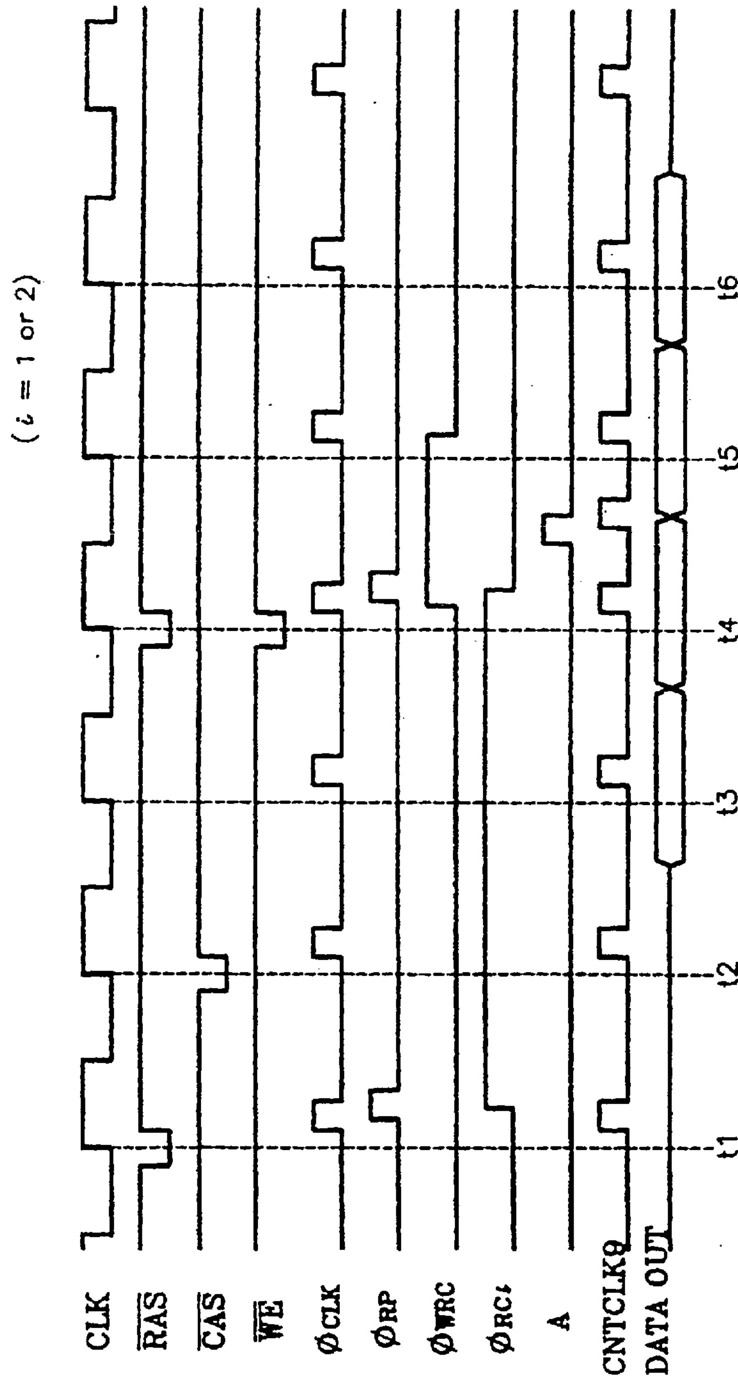
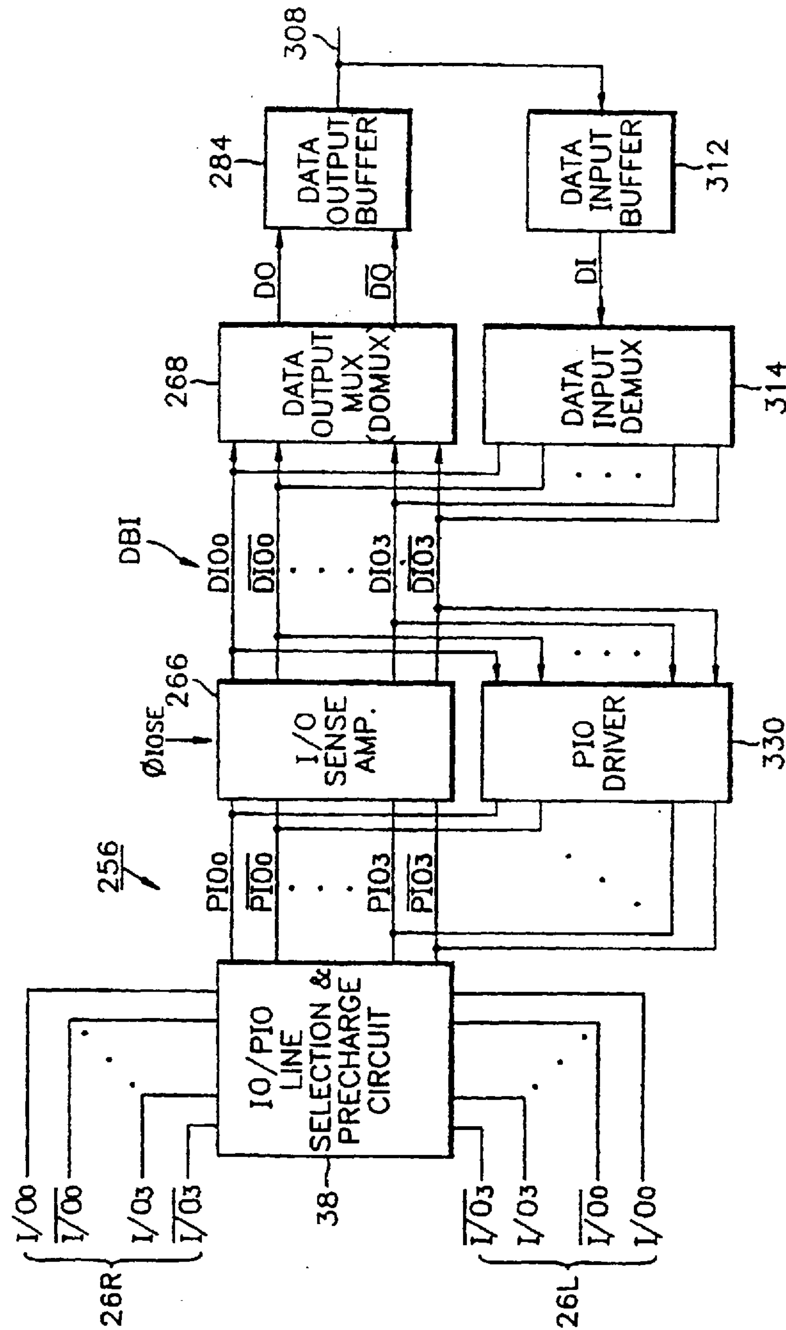


FIG. 22


308
DATA OUTPUT BUFFER
284
DATA INPUT BUFFER
312
DO
DO
DI
268
DATA OUTPUT MUX (DOMUX)
DATA INPUT DEMUX
314
DBI
DIO0
DIO0
DIO3
DIO3
ØIOSE
266
I/O SENSE AMP.
PIO DRIVER
330
256
PIO0
PIO0
PIO3
PIO3
IO/PIO LINE SELECTION & PRECHARGE CIRCUIT
38
I/O0
I/O0
I/O3
I/O3
26R
26L
FIG. 23

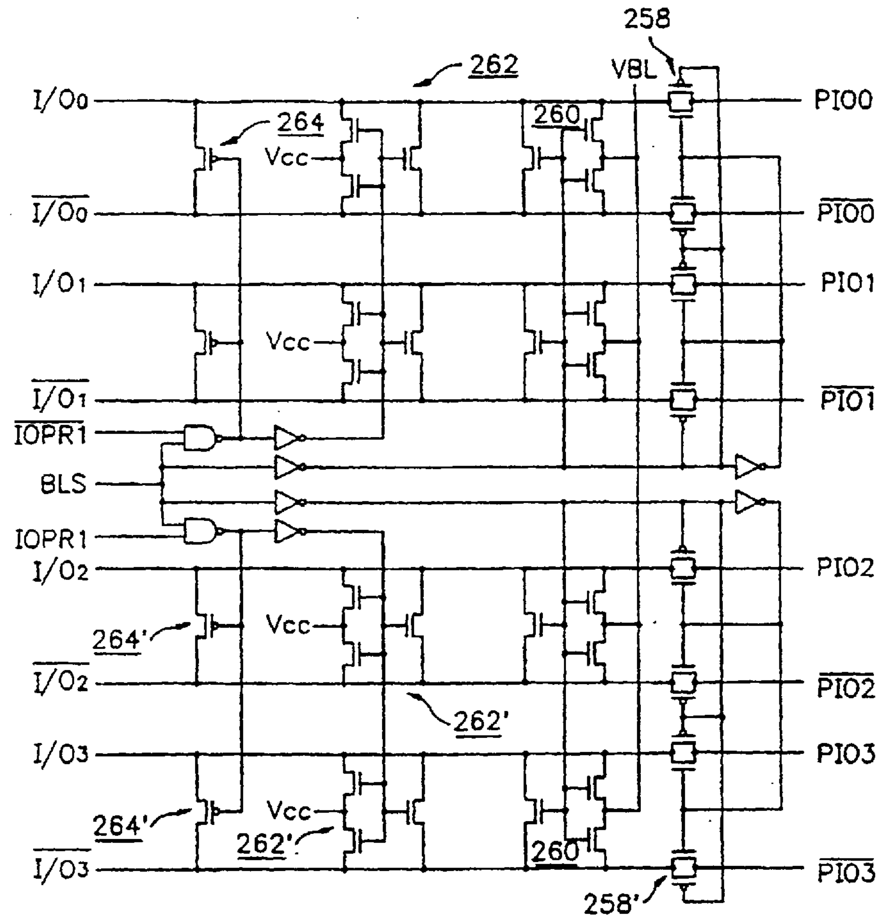


FIG. 24

RX-092

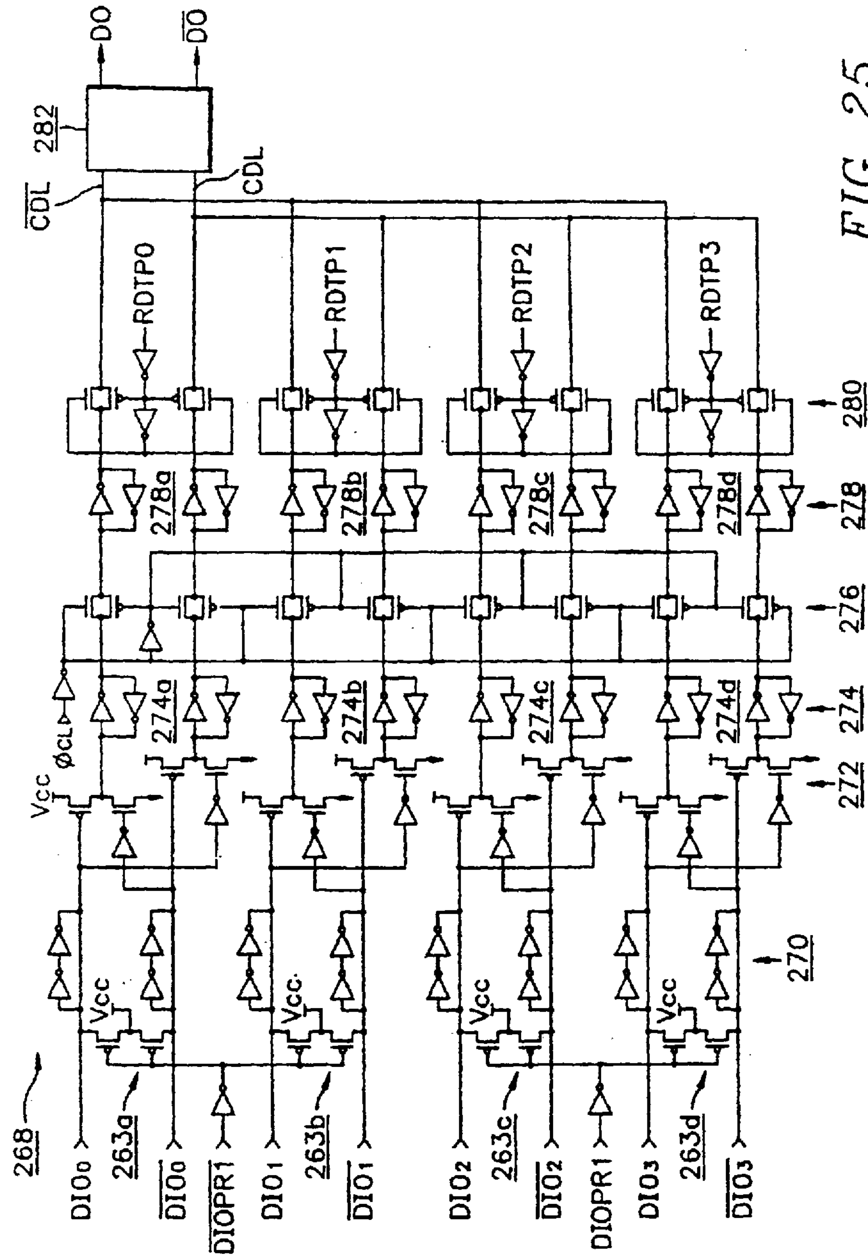


FIG. 25

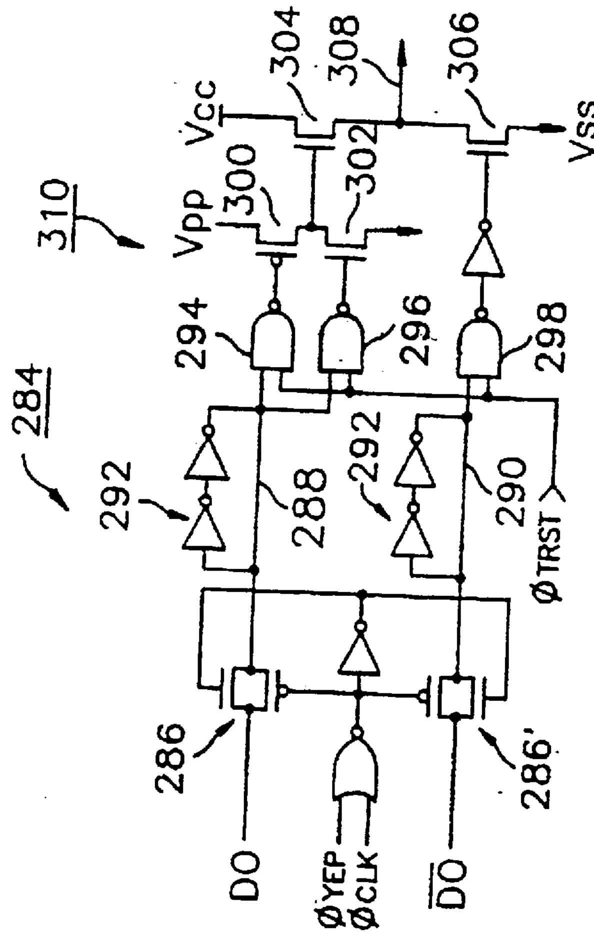


FIG. 26

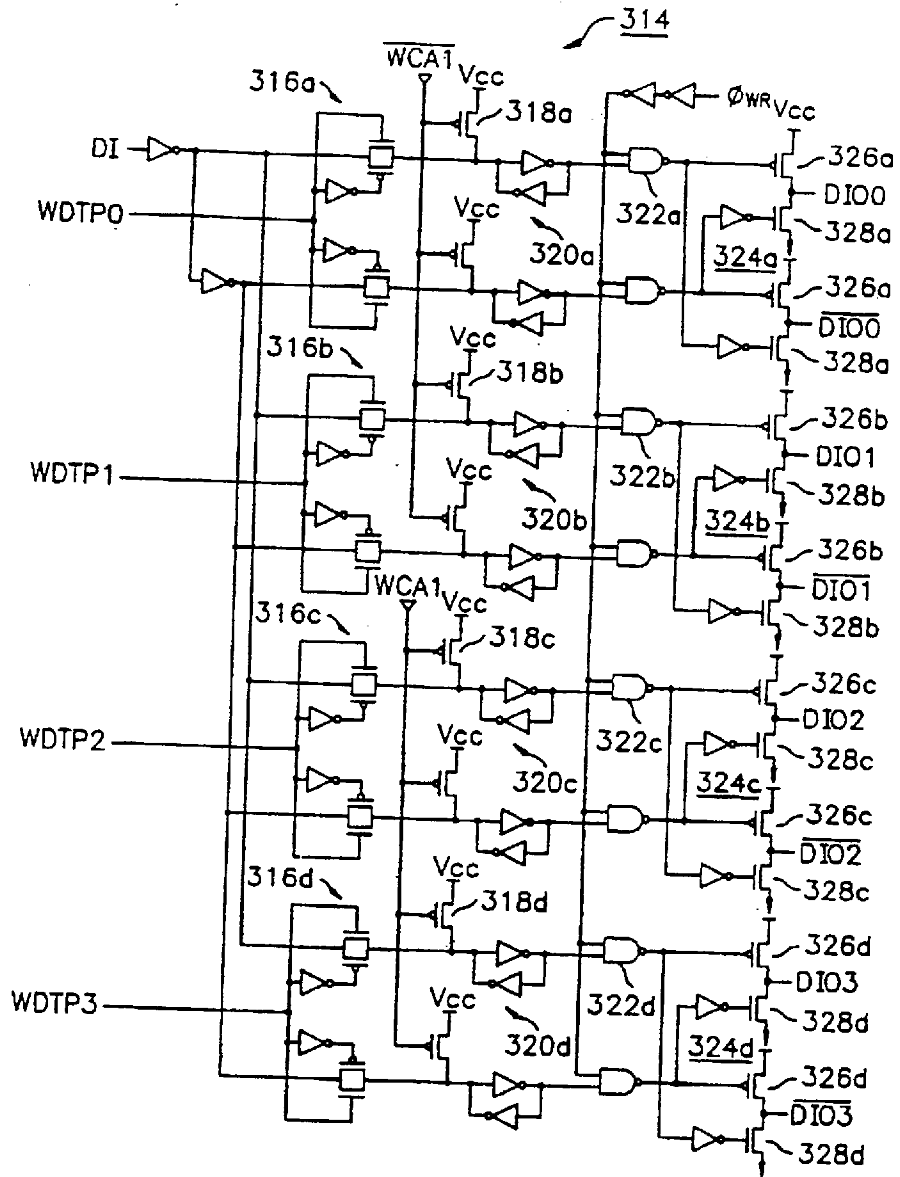


FIG. 27

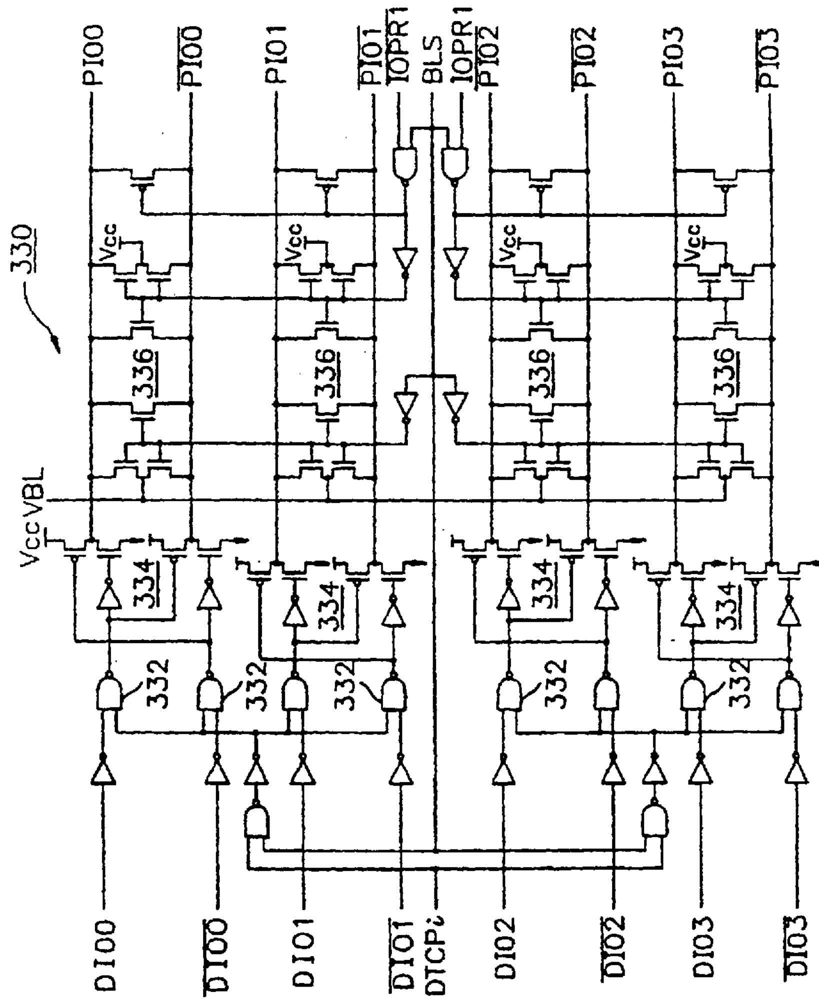


FIG. 28

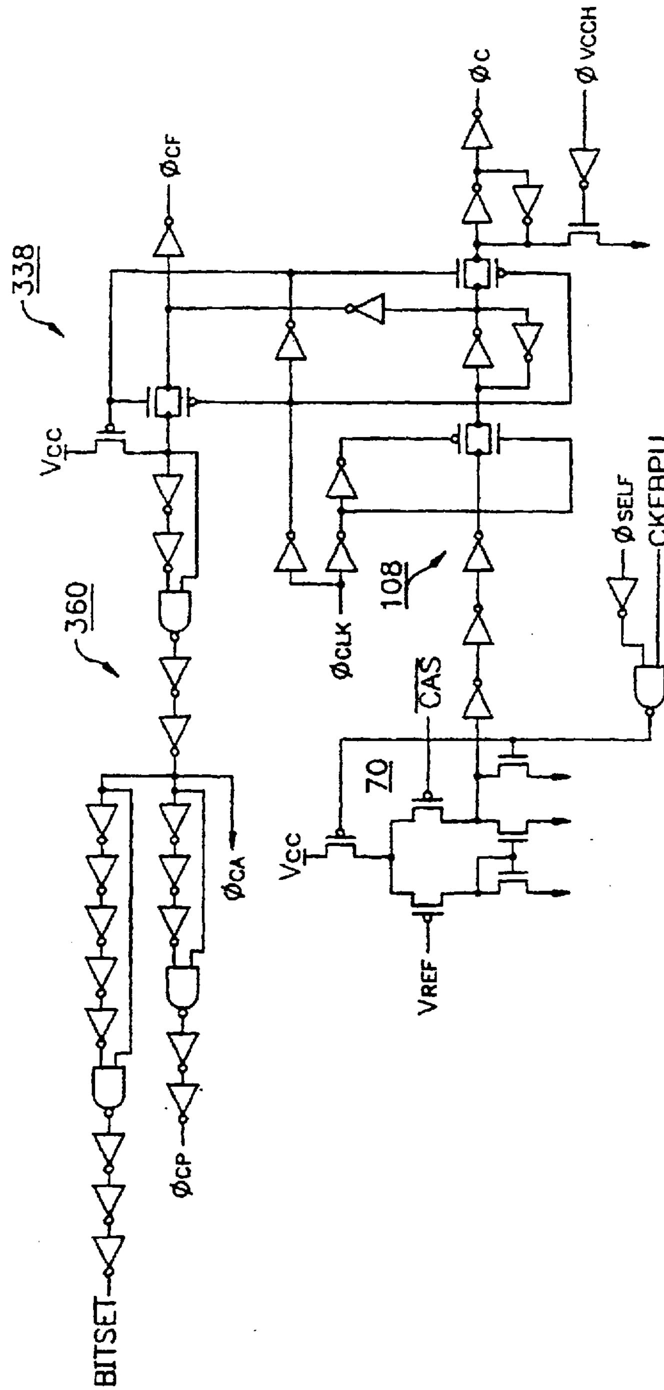


FIG. 29

RX-092

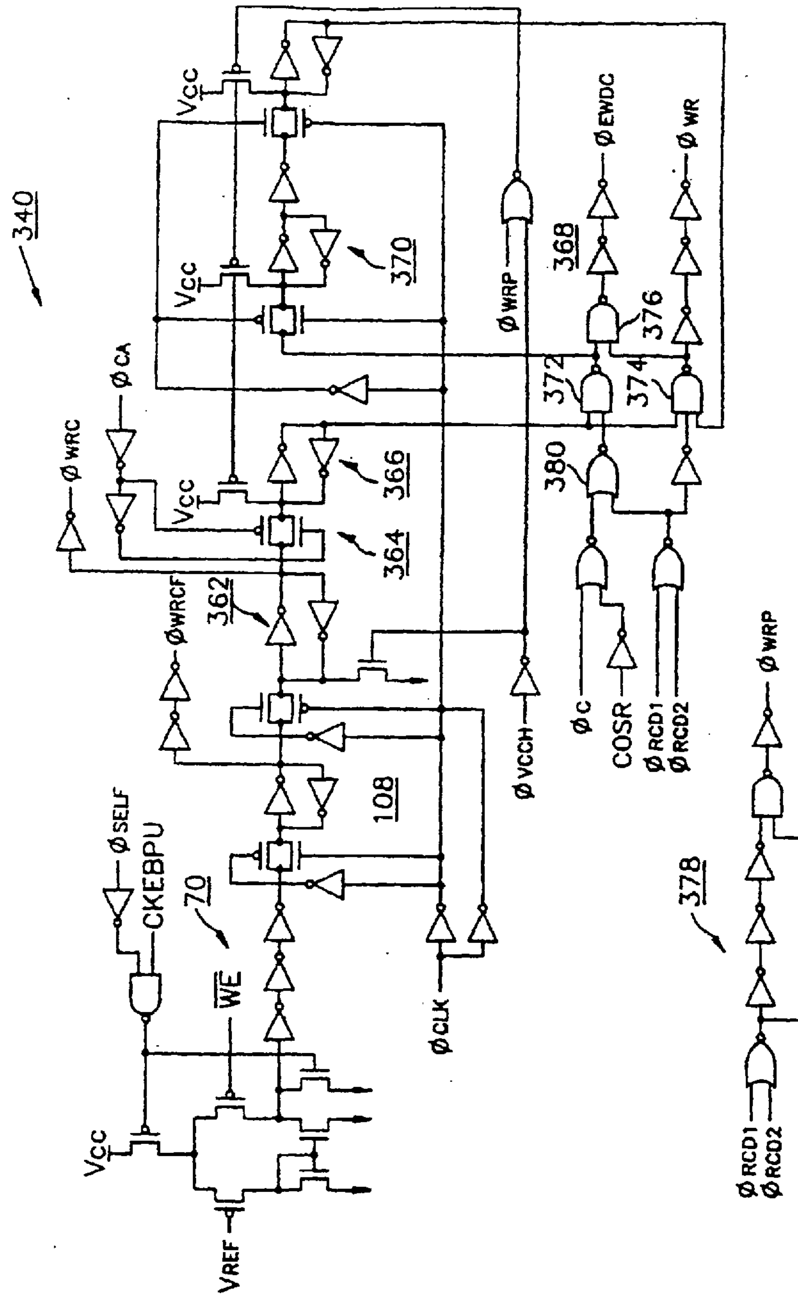


FIG. 30

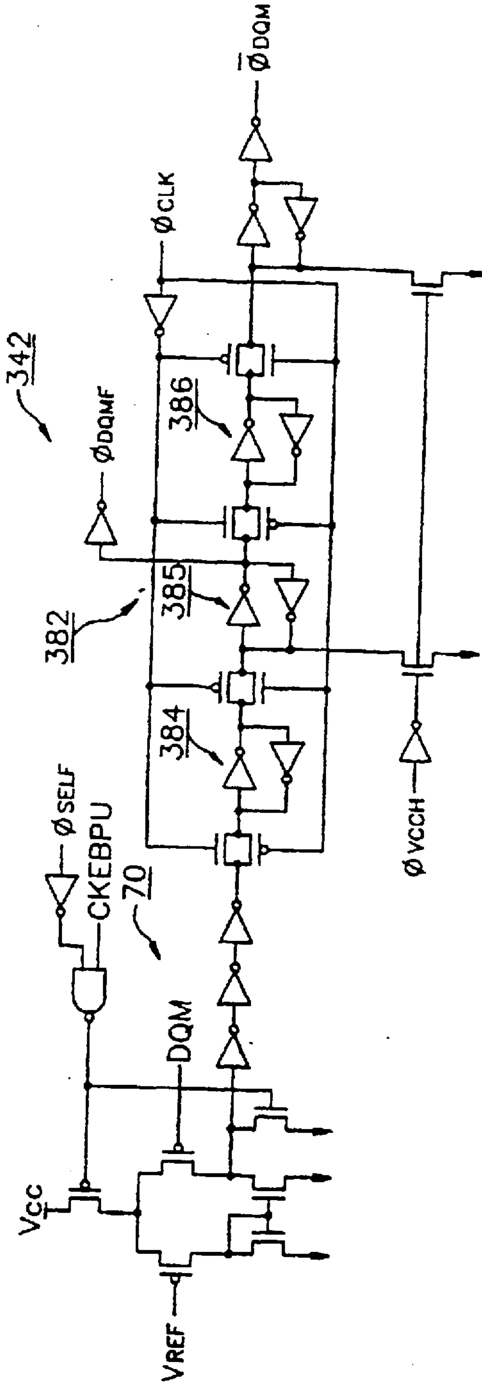


FIG. 31

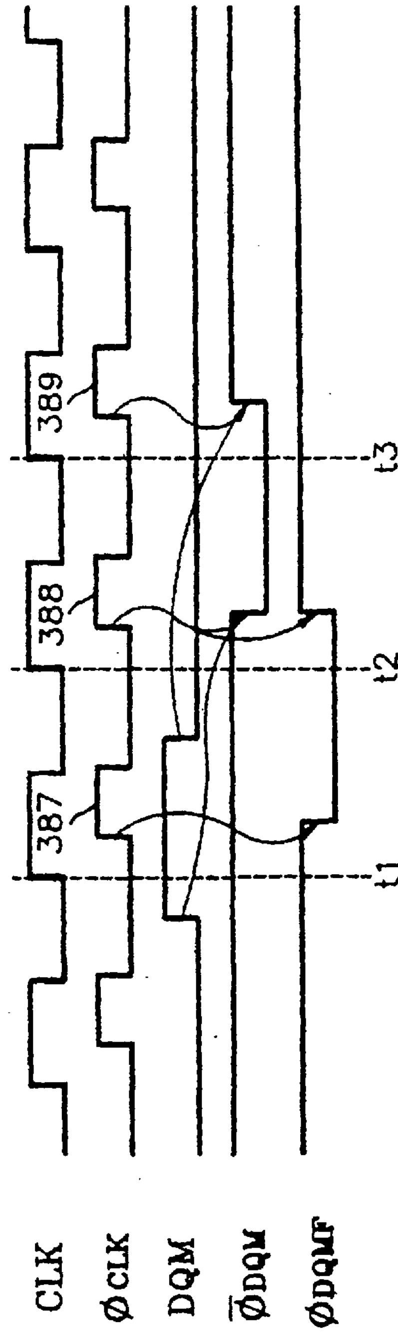


FIG. 32

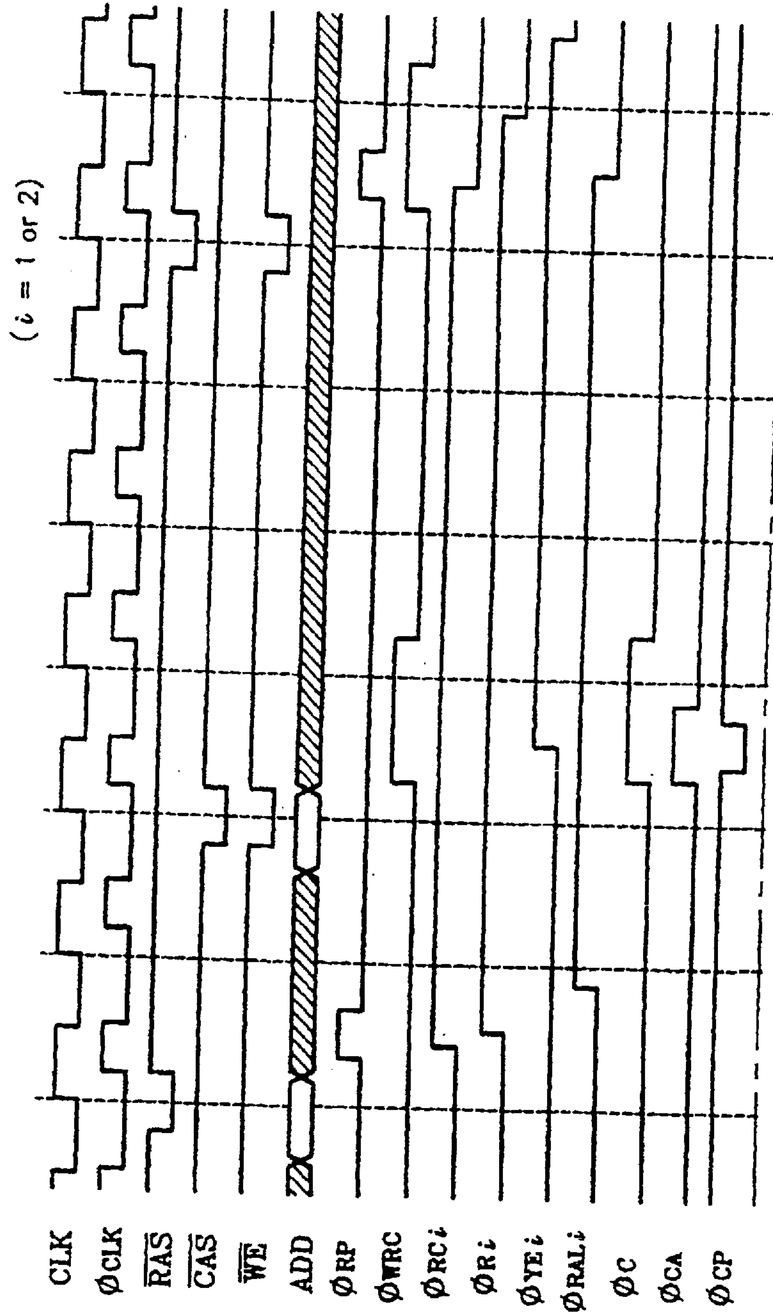


FIG. 33a

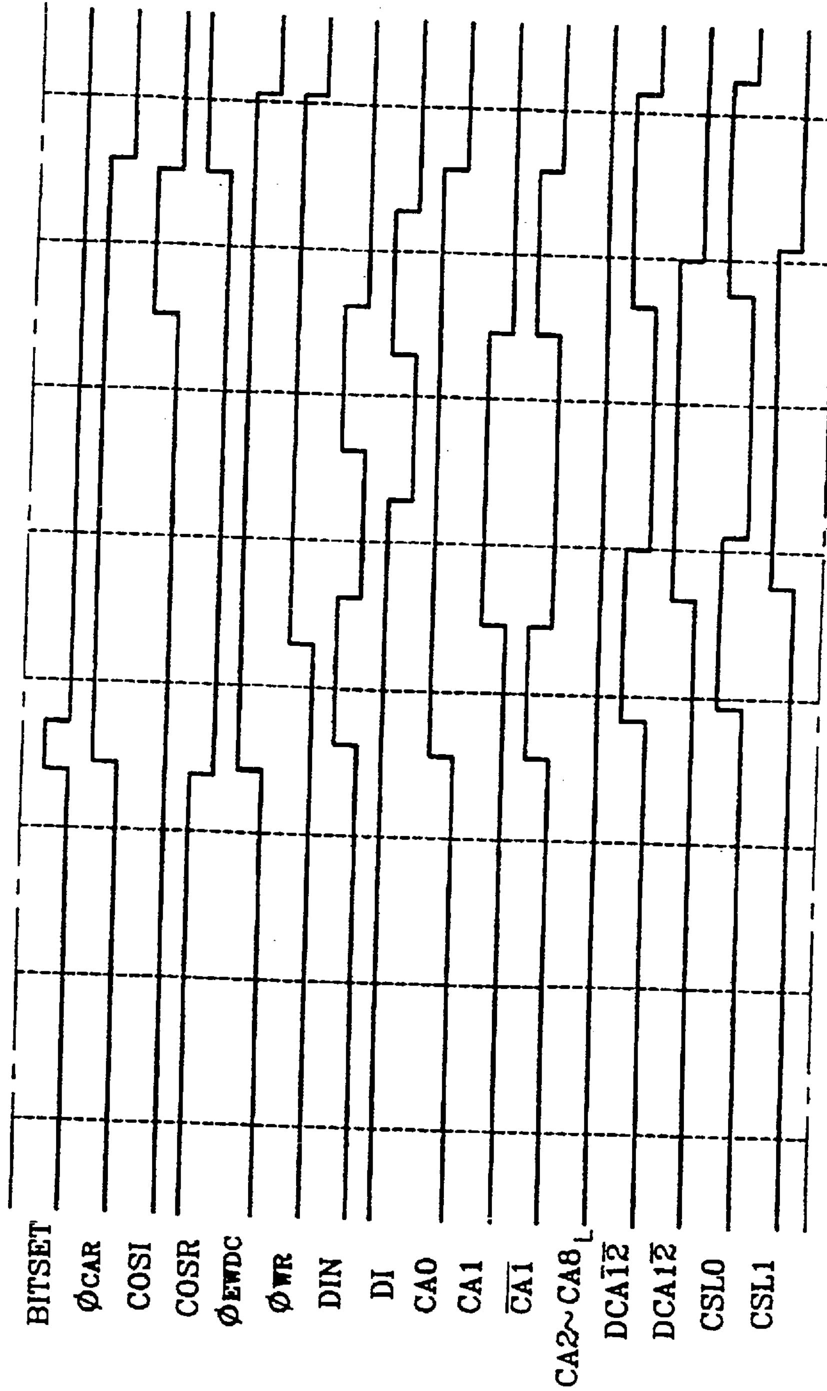


FIG. 33b

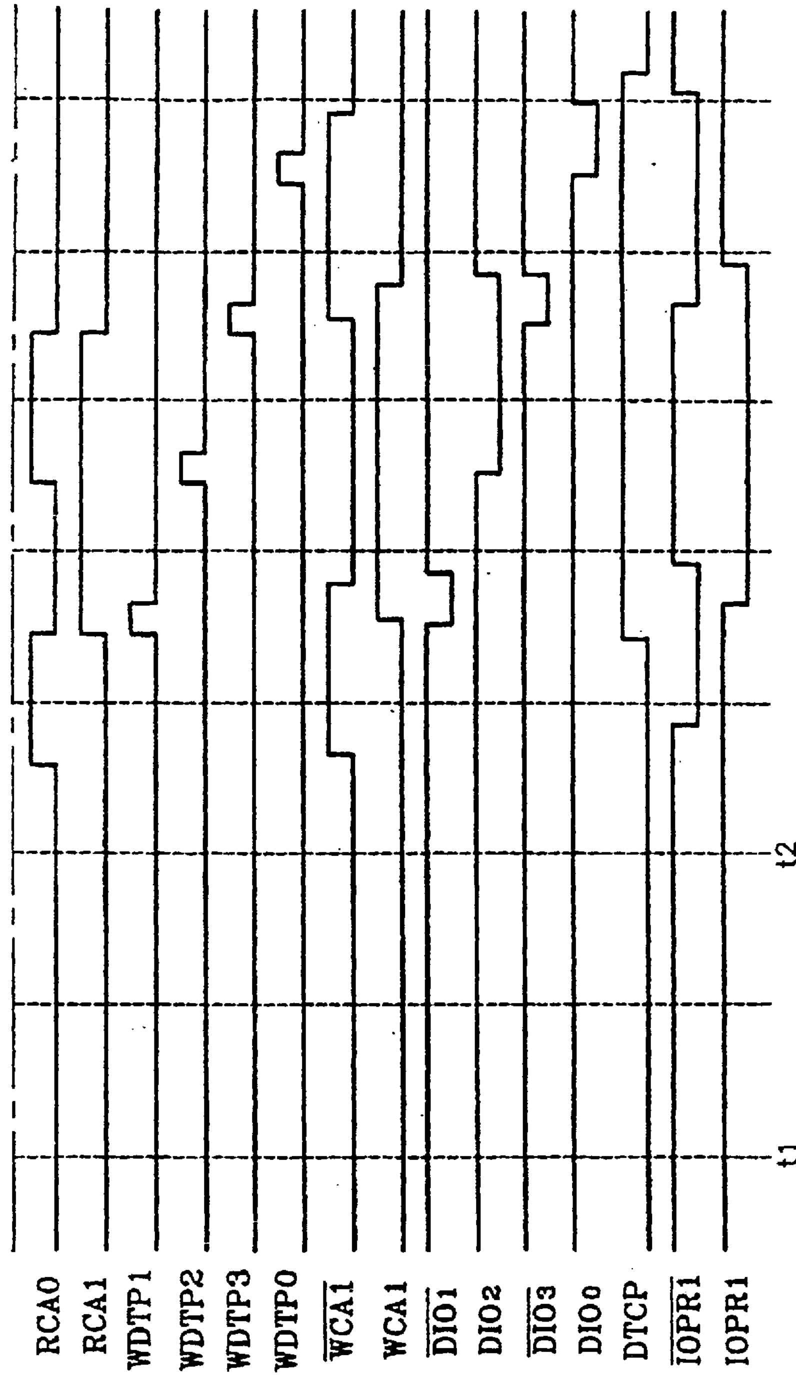


FIG. 33c

RX-09:

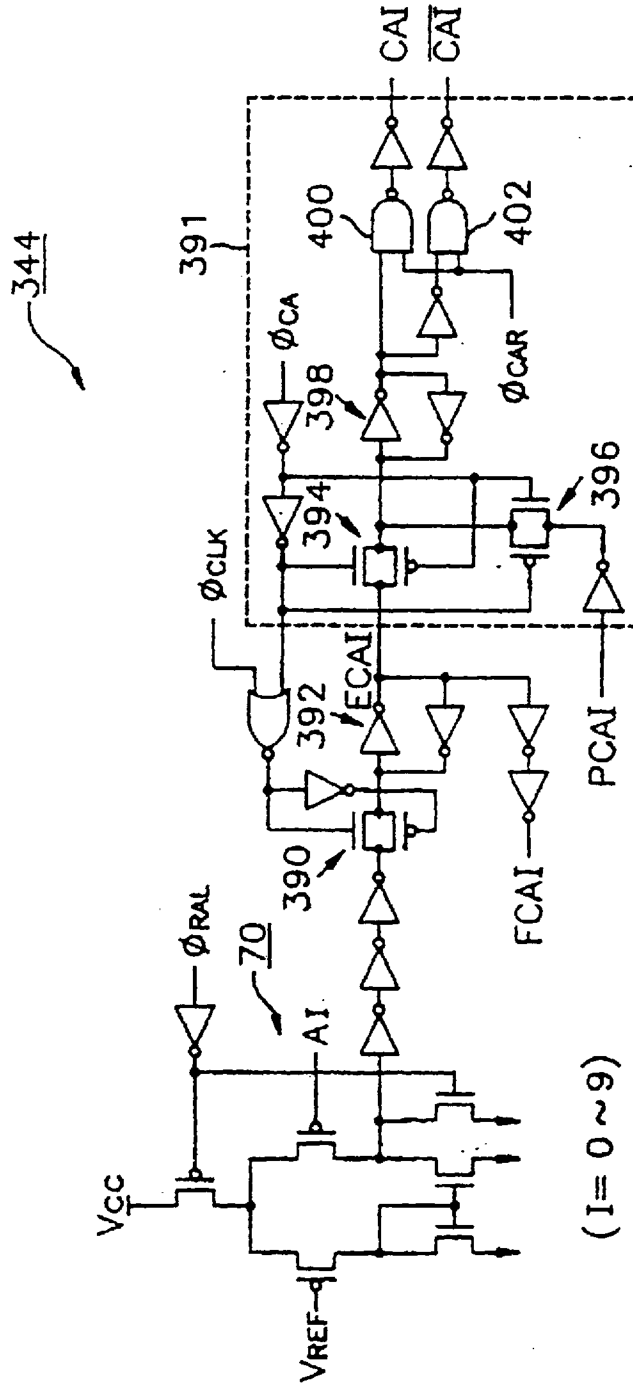


FIG. 34

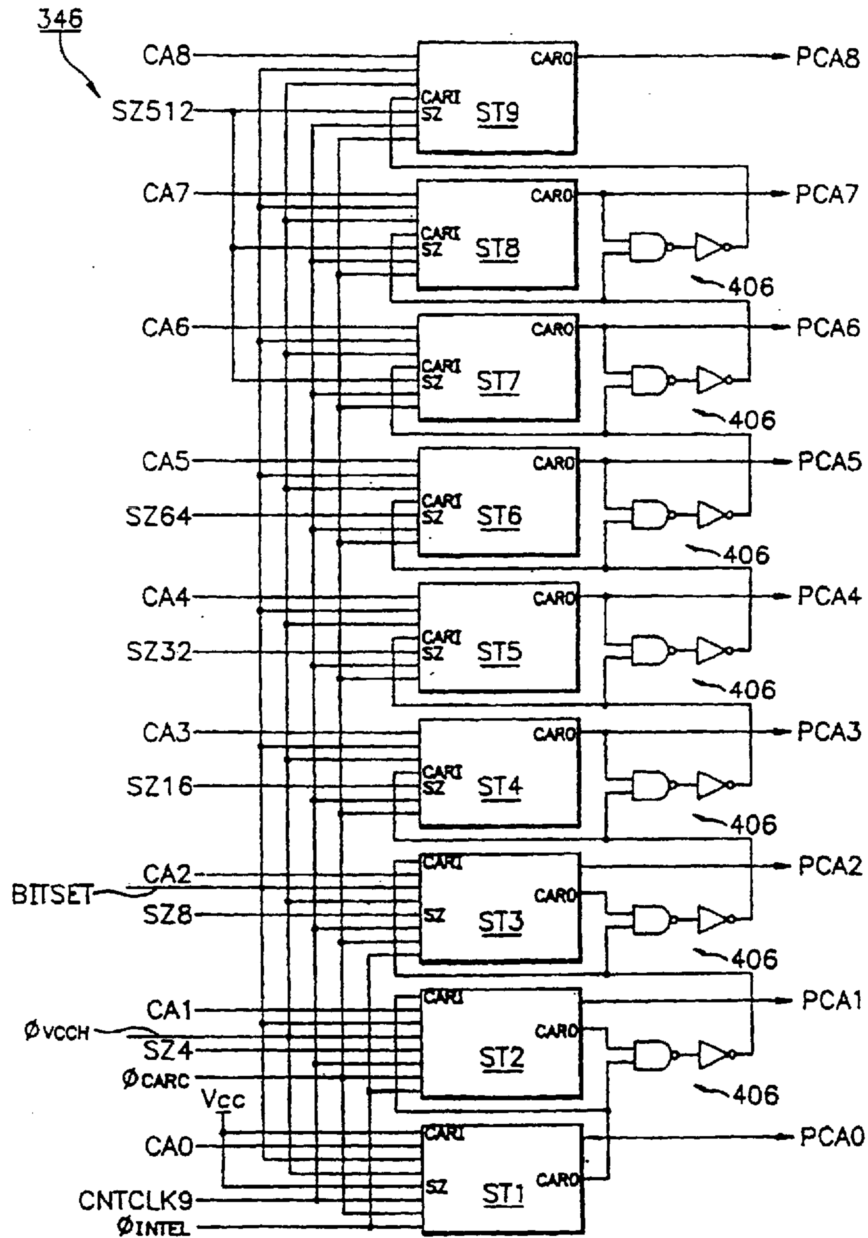


FIG. 35

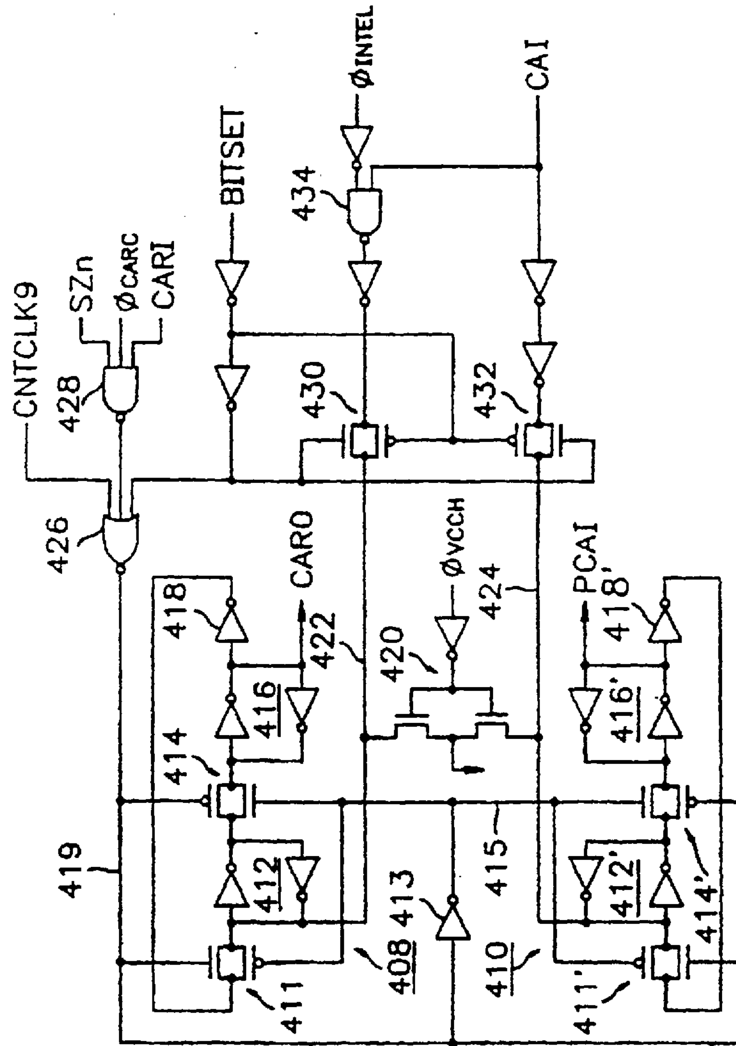


FIG. 36a

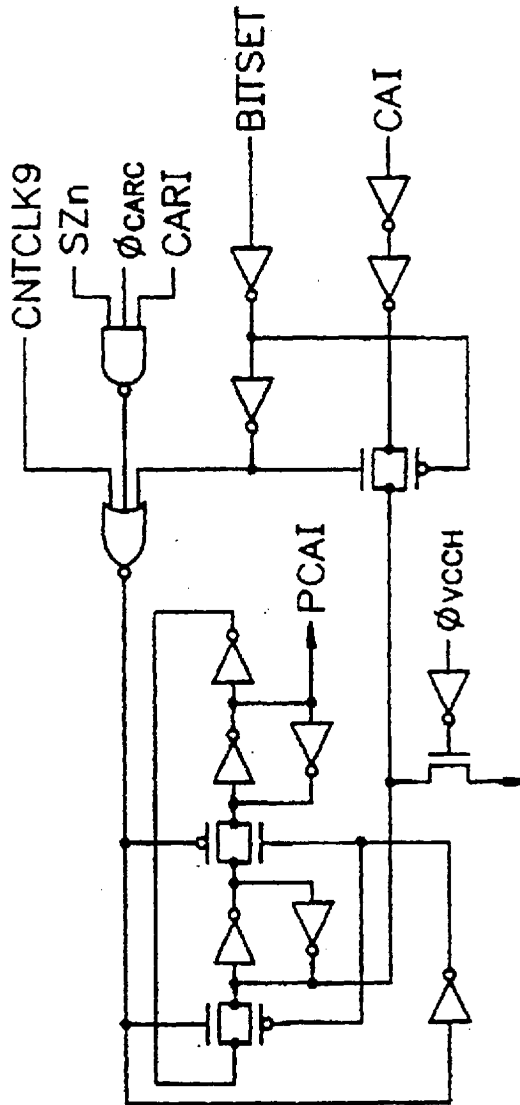


FIG. 36b

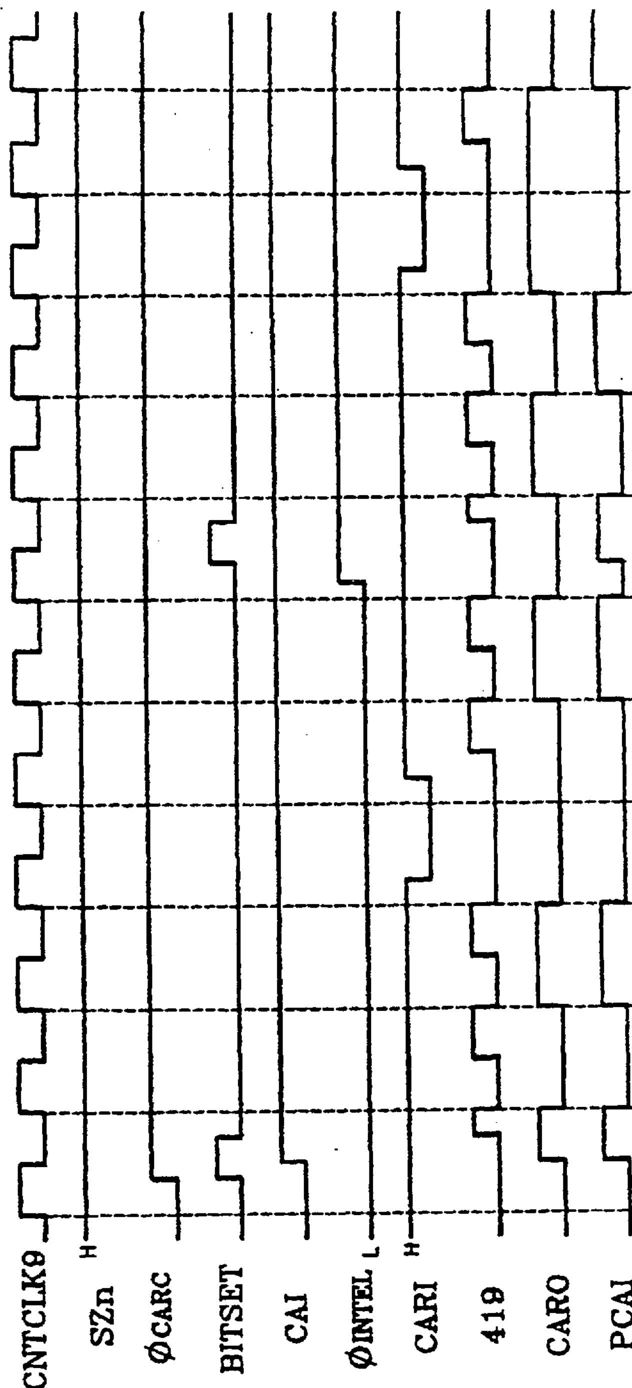


FIG. 37

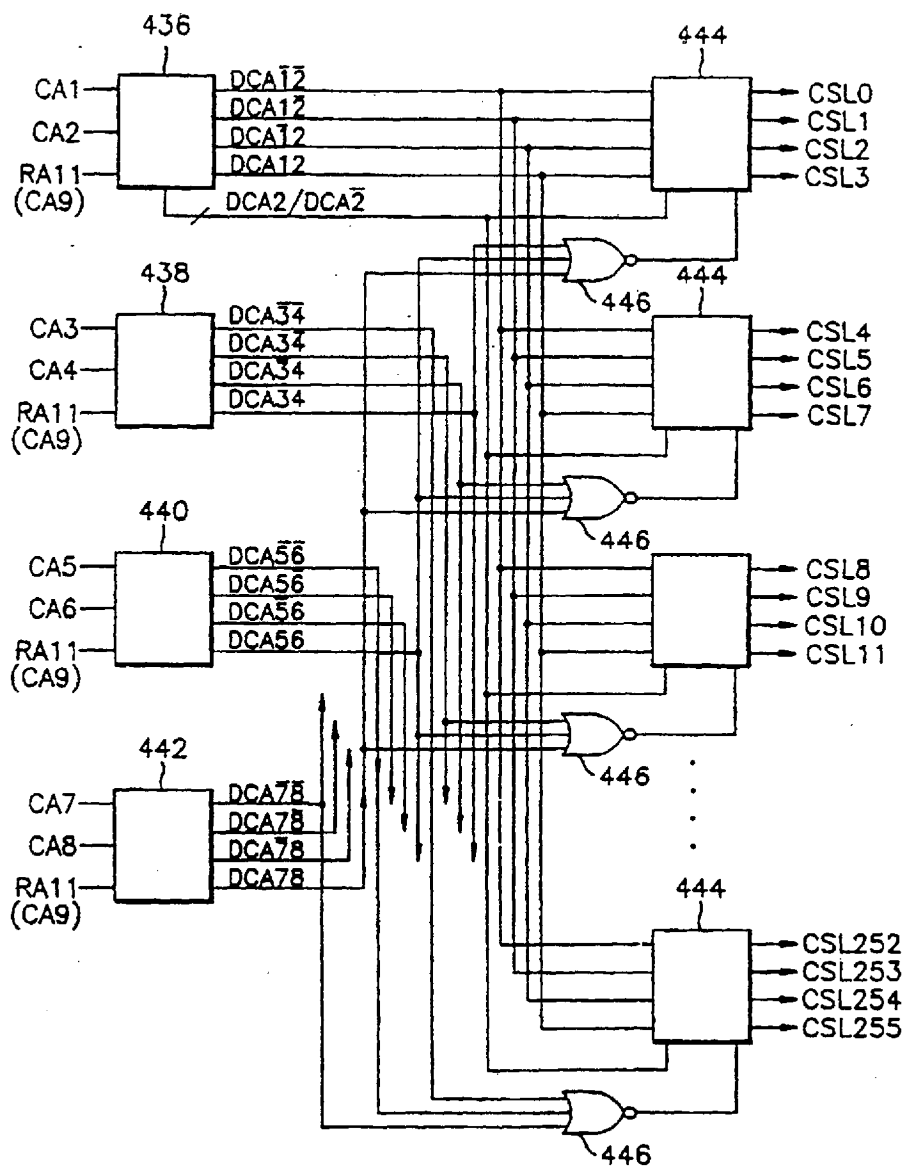


FIG. 38

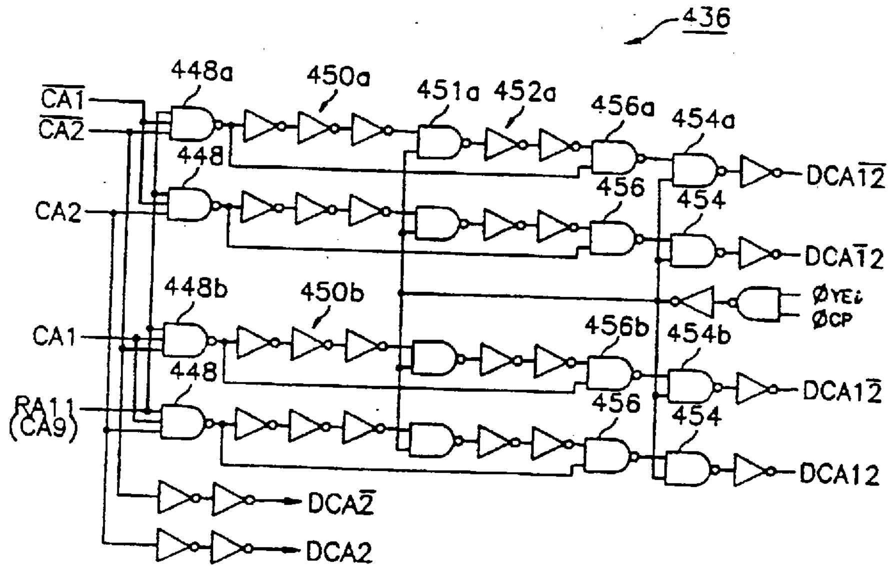


FIG. 39a

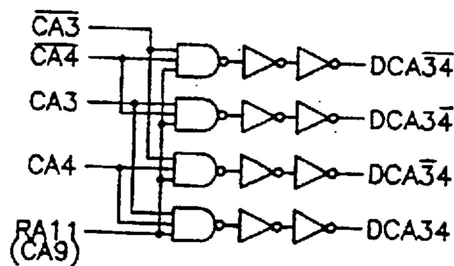


FIG. 39b

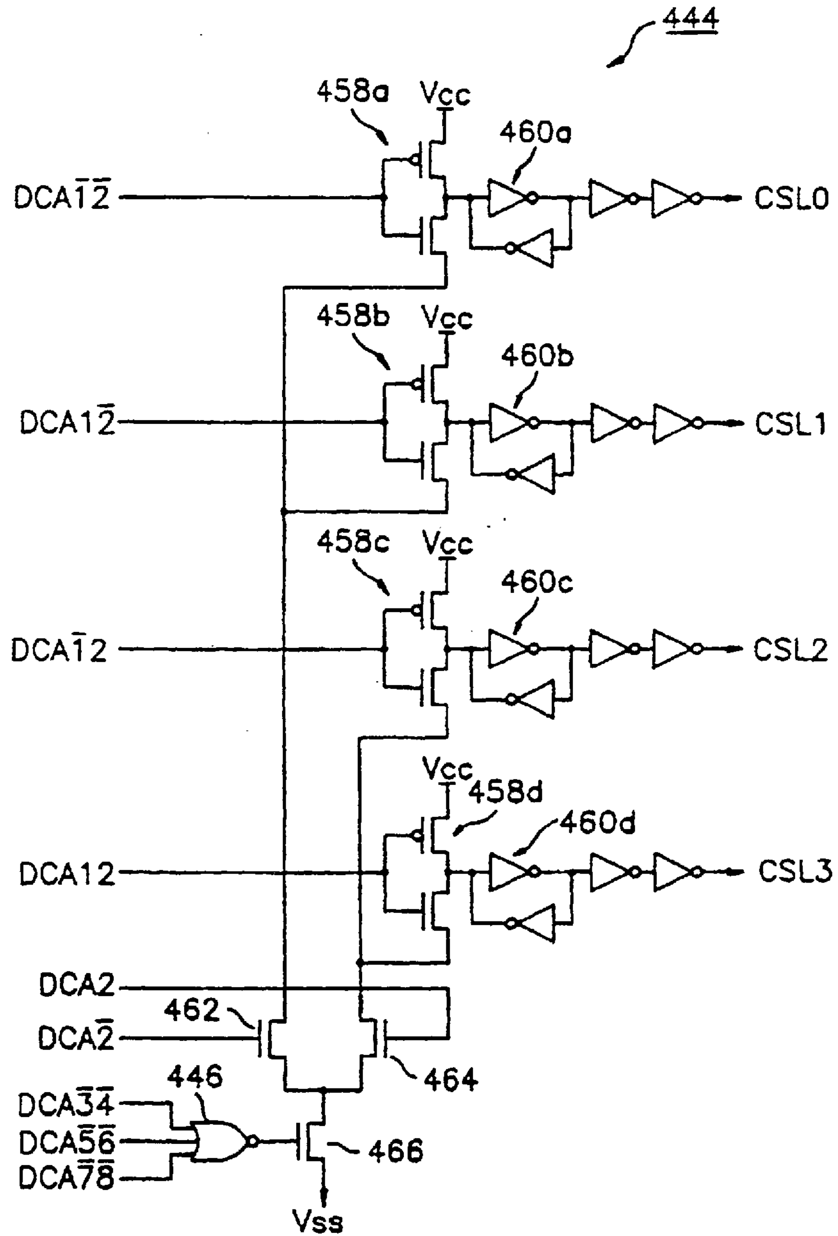


FIG. 40

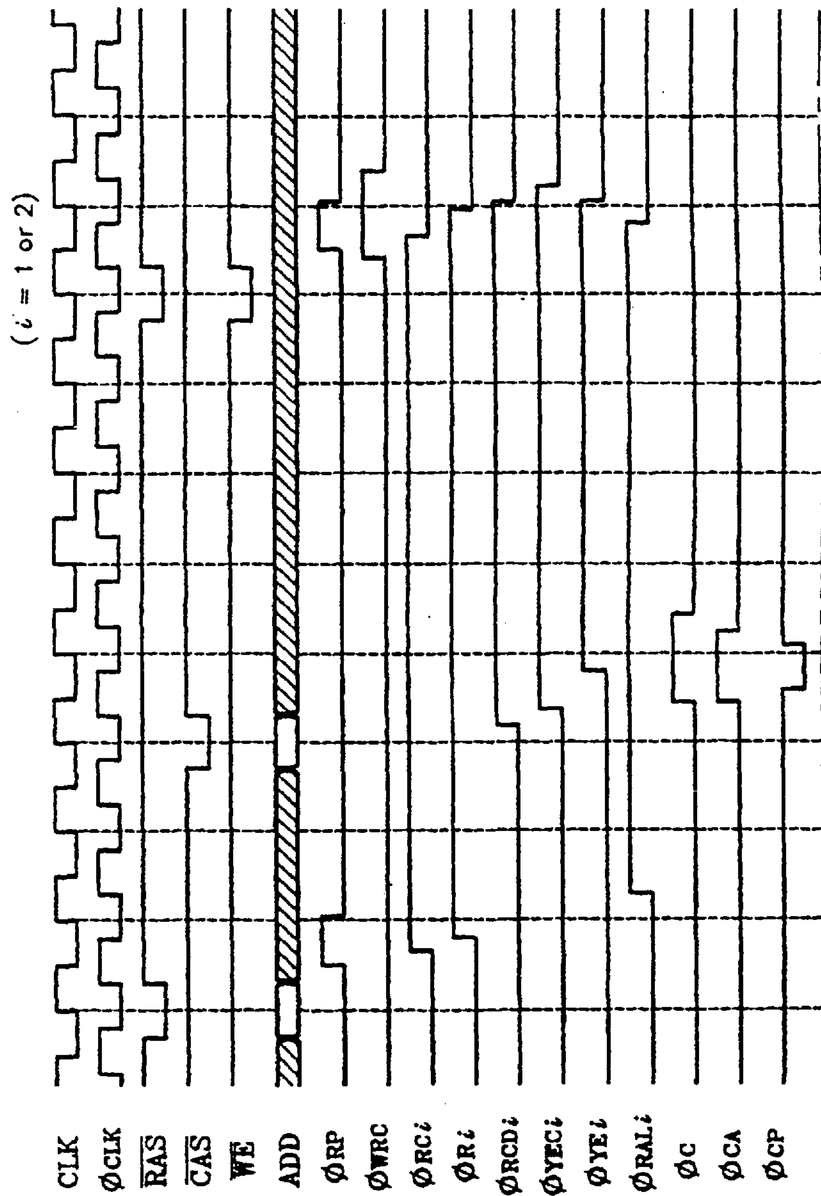


FIG. 41a

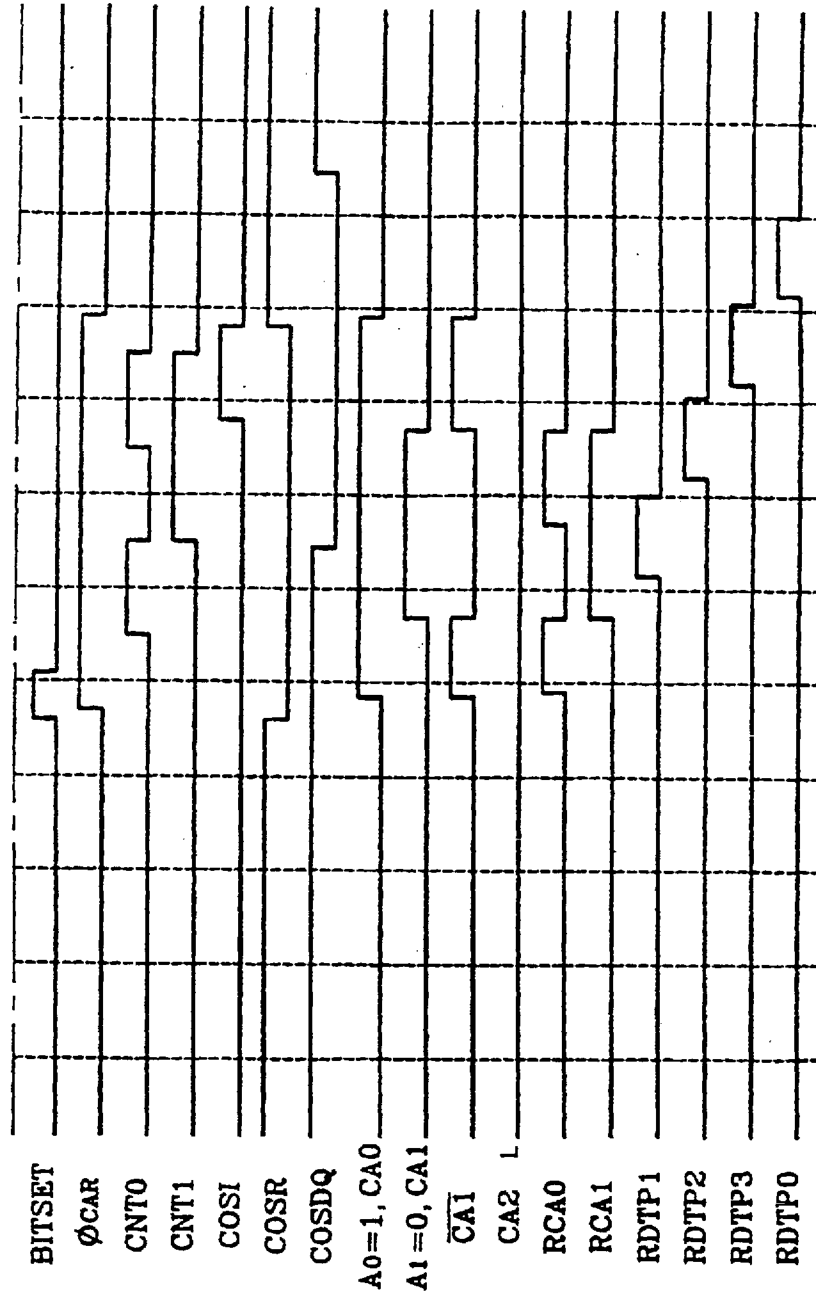


FIG. 41b

RX-0925

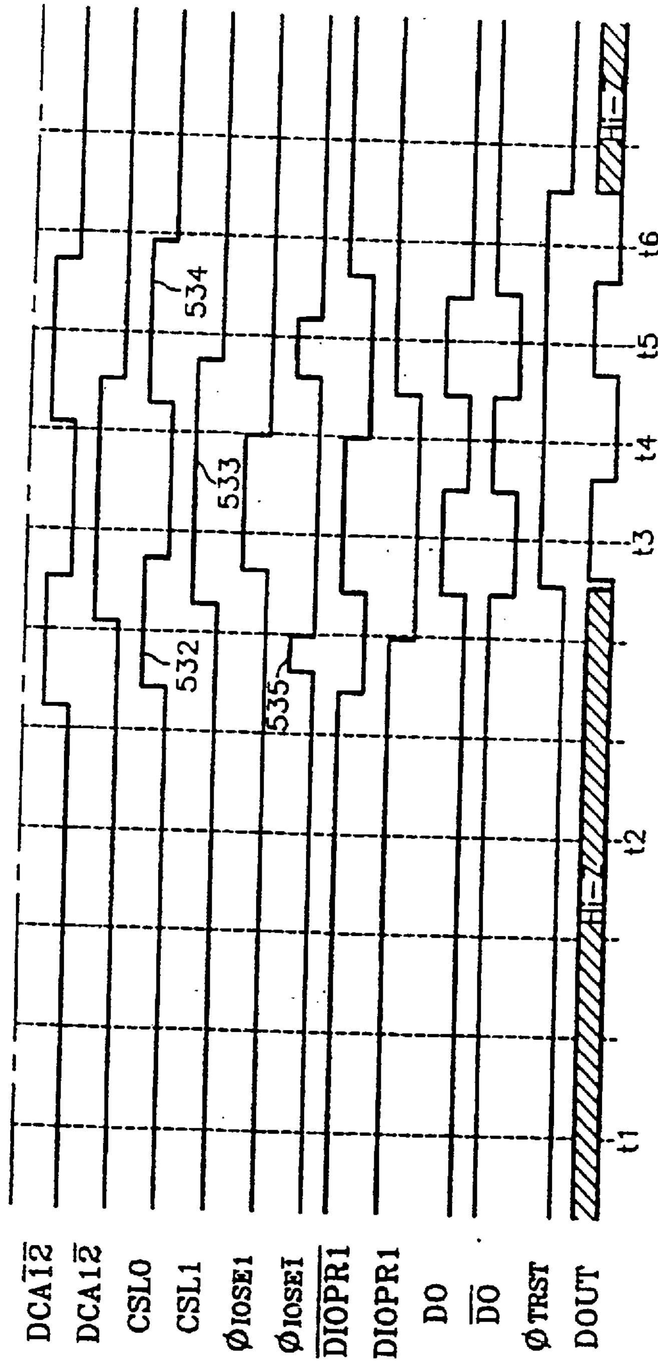


FIG. 41c

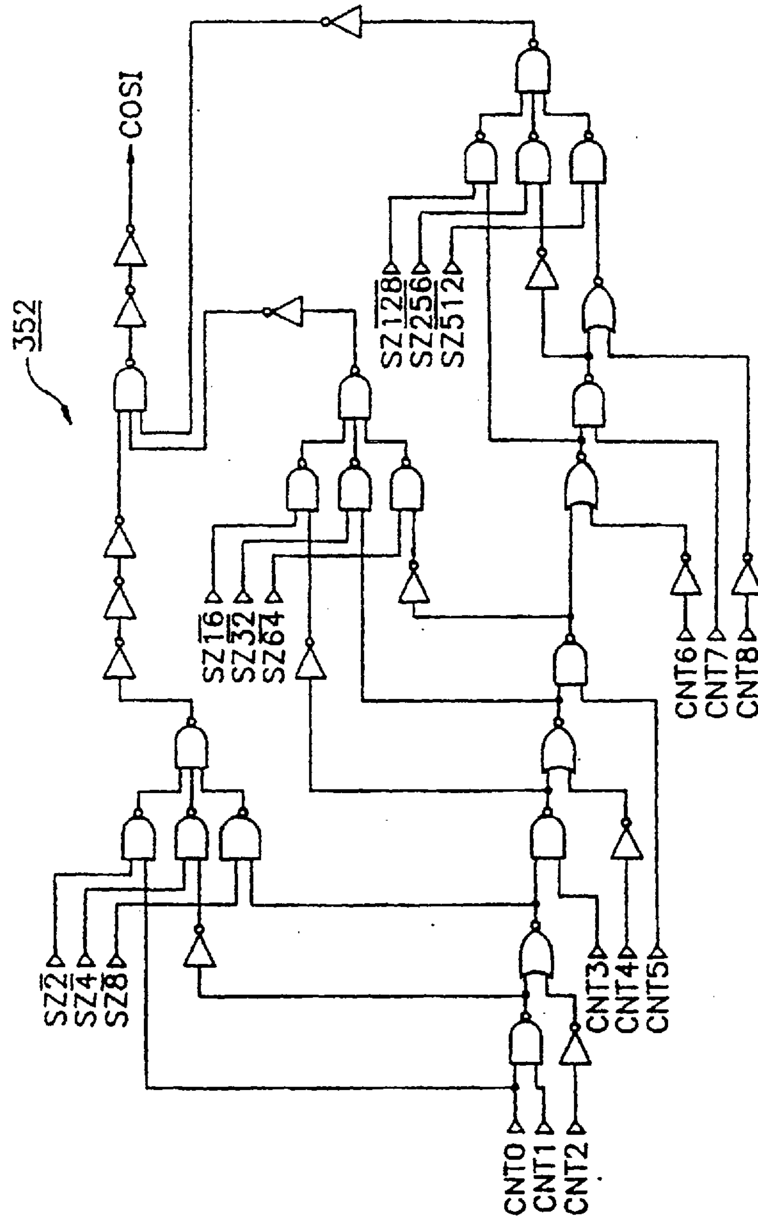


FIG. 42

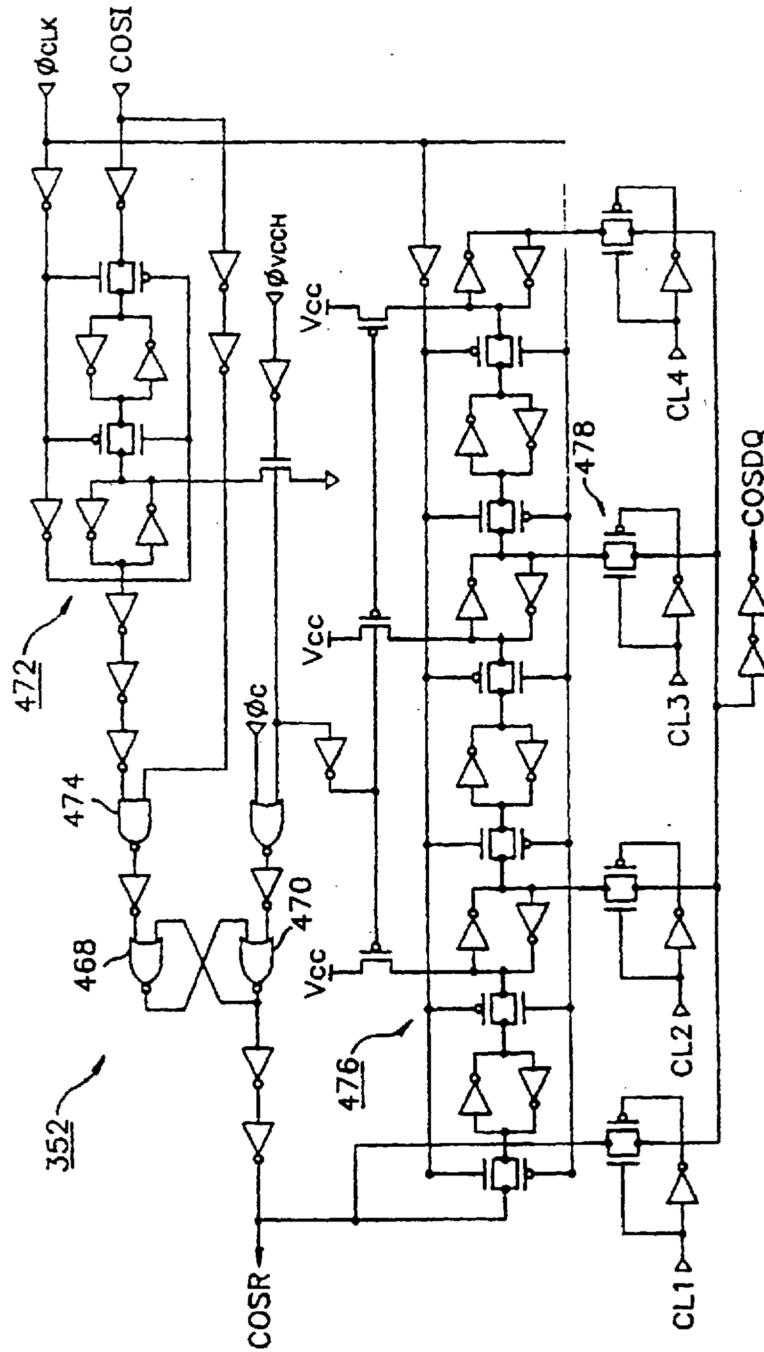


FIG. 43

RX-0925

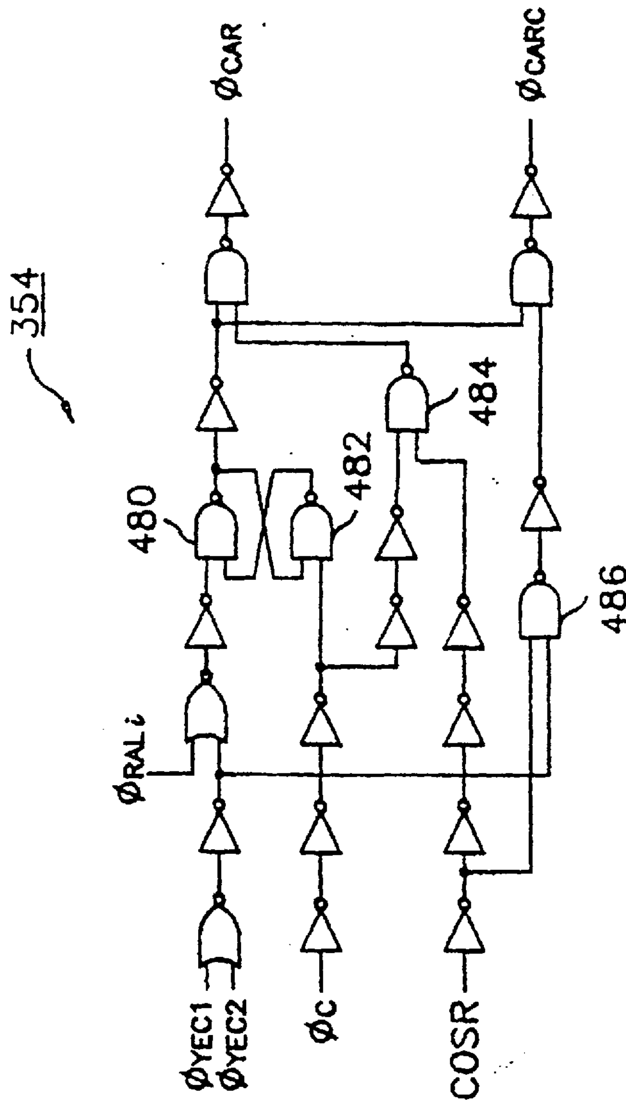


FIG. 44

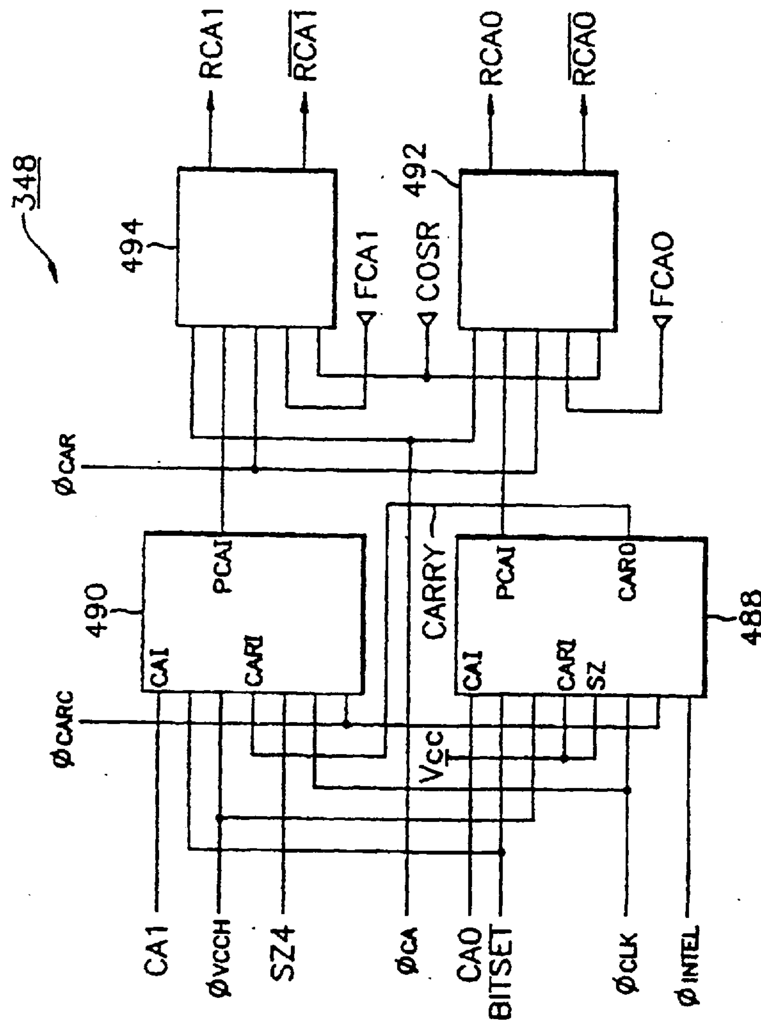


FIG. 45

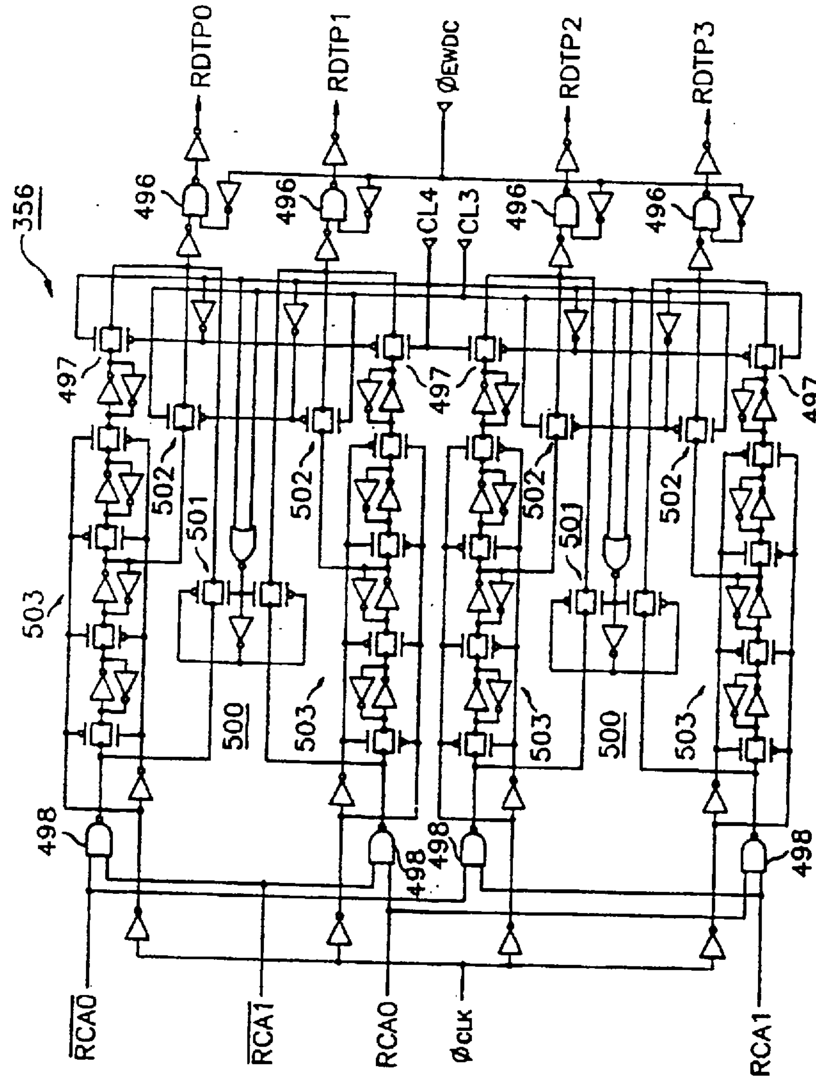


FIG. 46

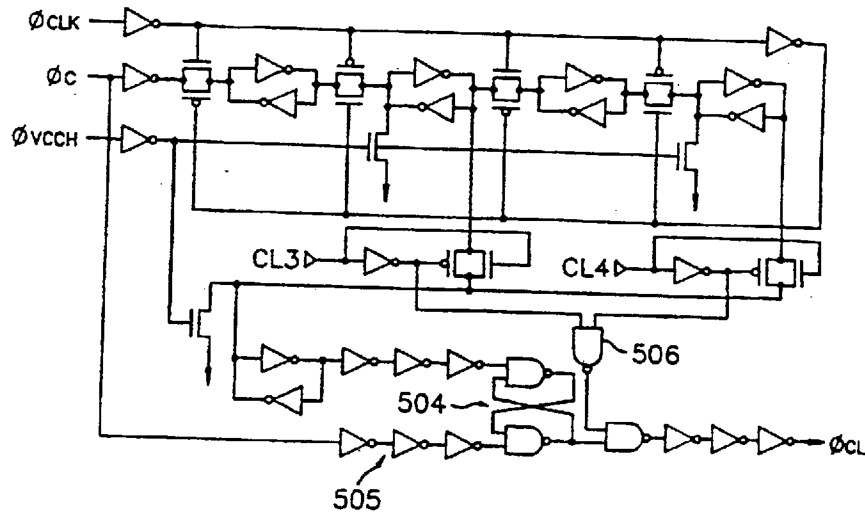


FIG. 47

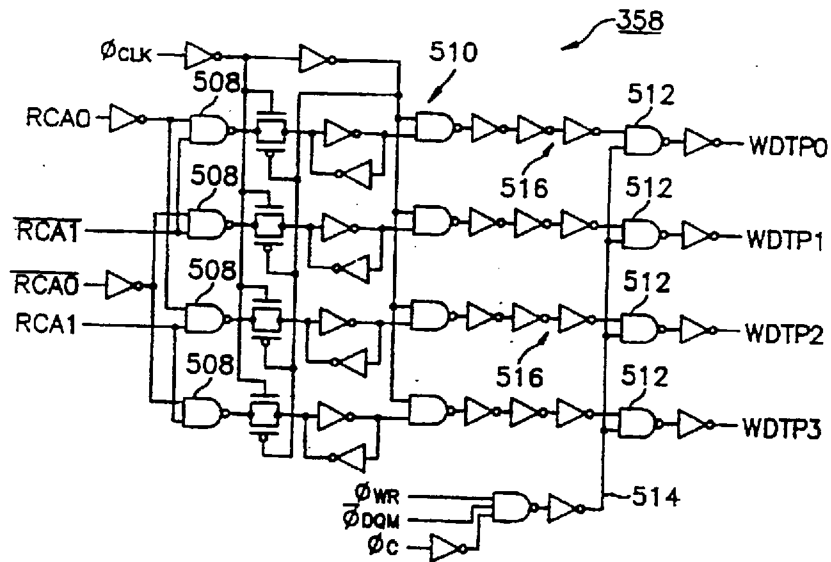


FIG. 48

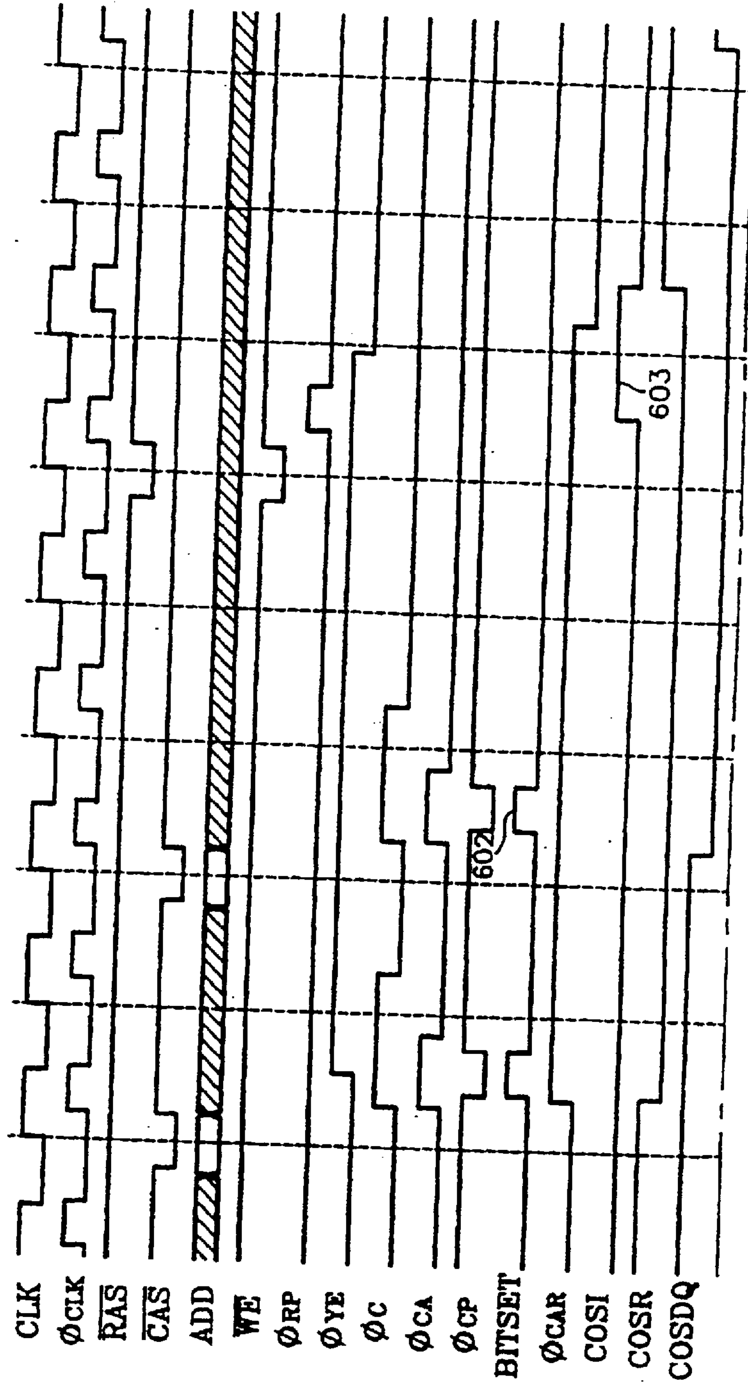


FIG. 49a

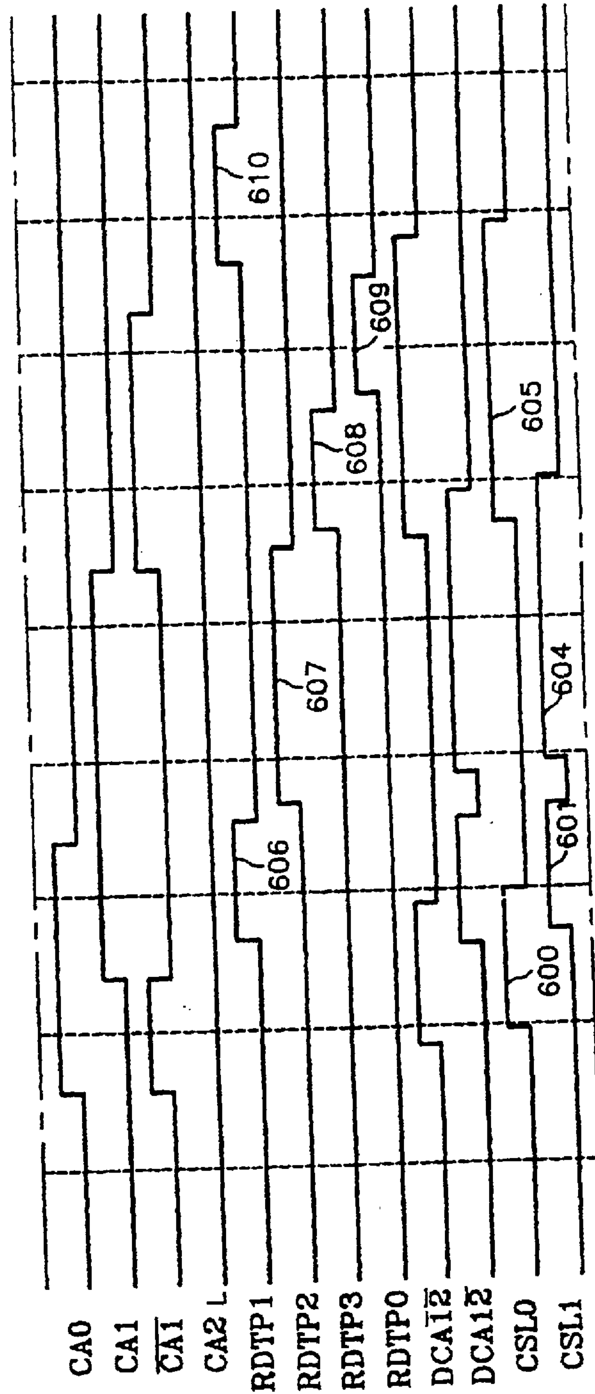


FIG. 49b

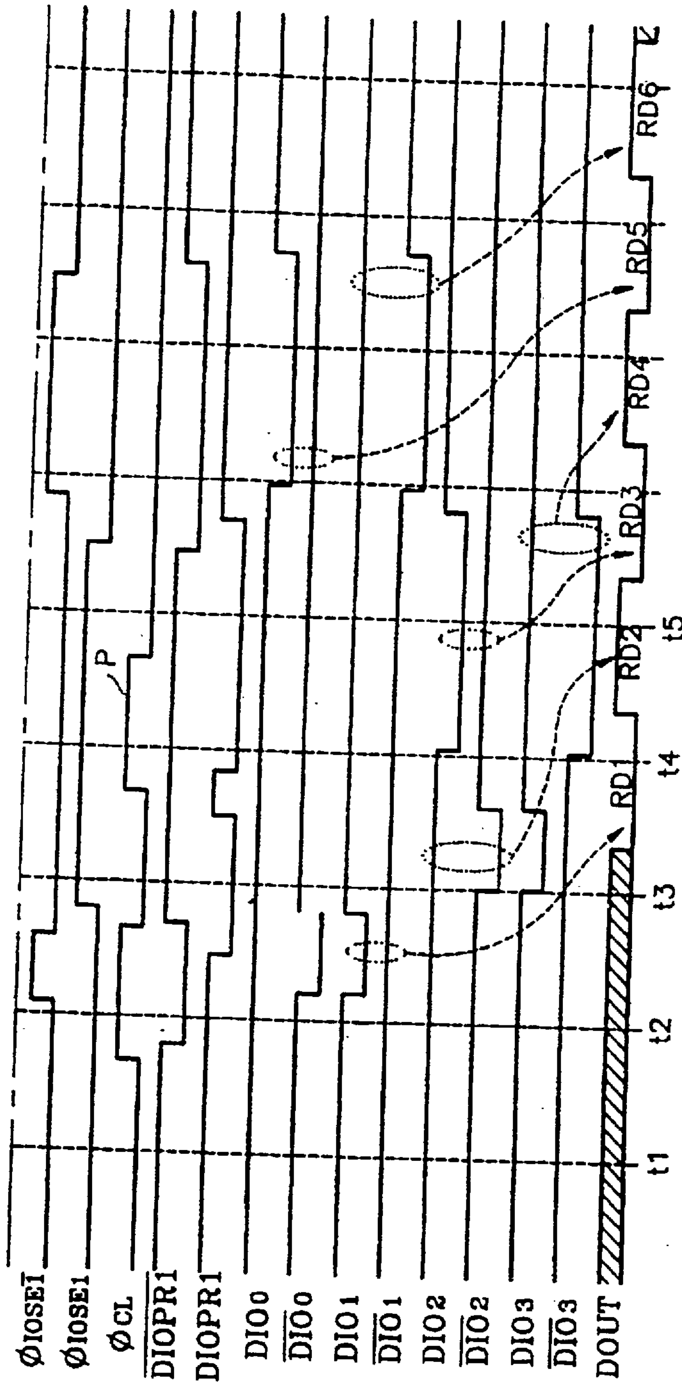


FIG. 49c

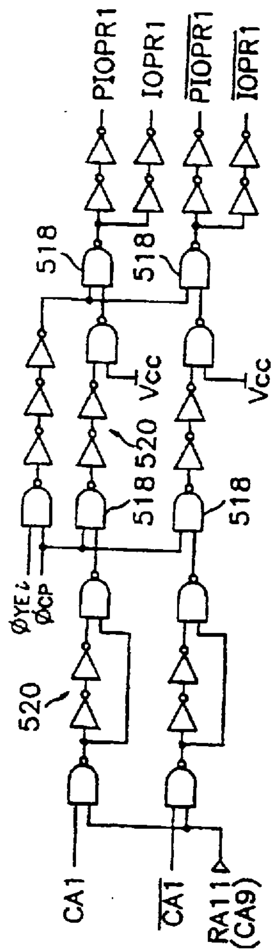


FIG. 50

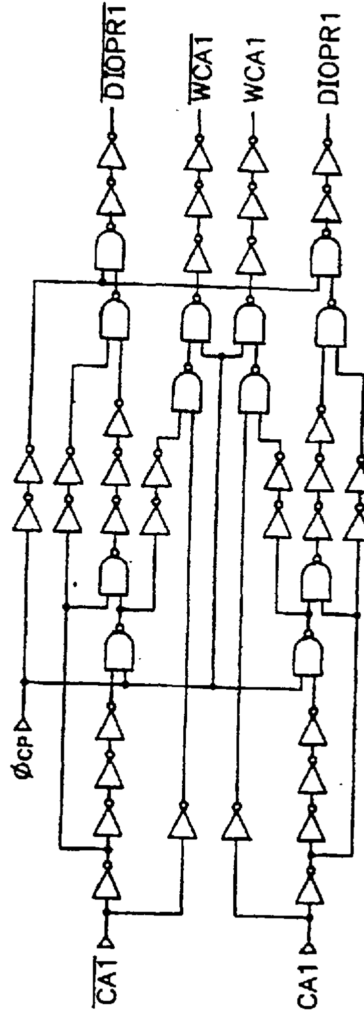


FIG. 51

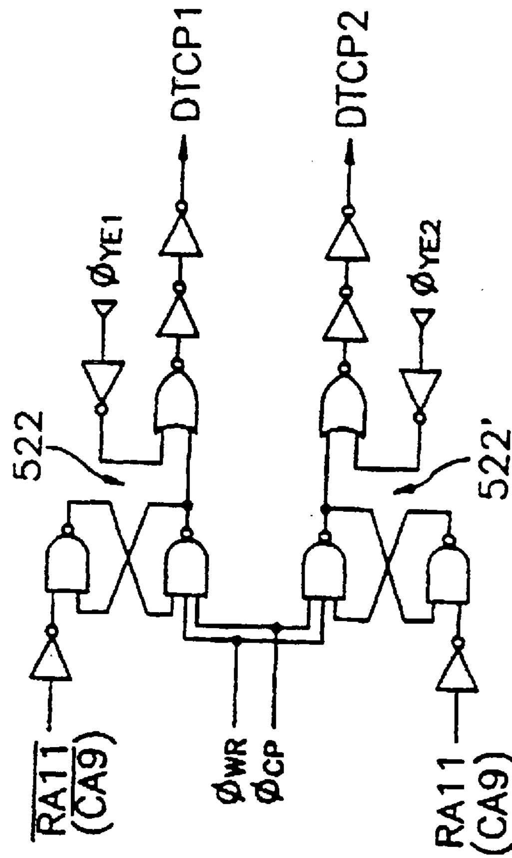


FIG. 52

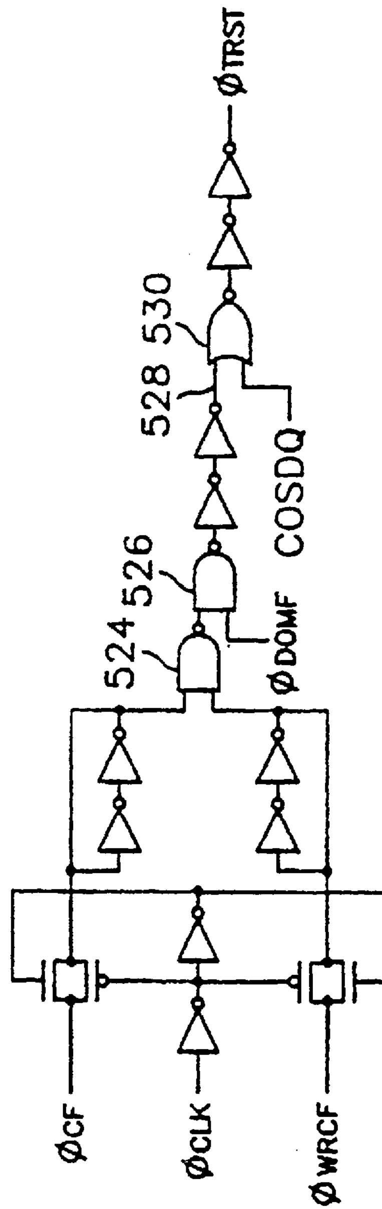


FIG. 53

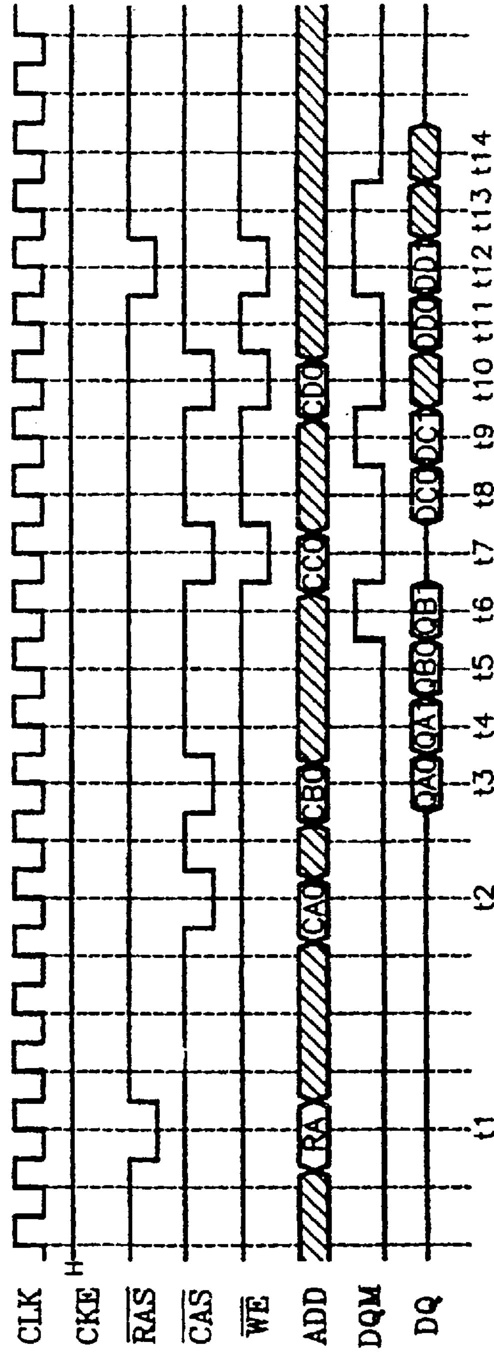


FIG. 54

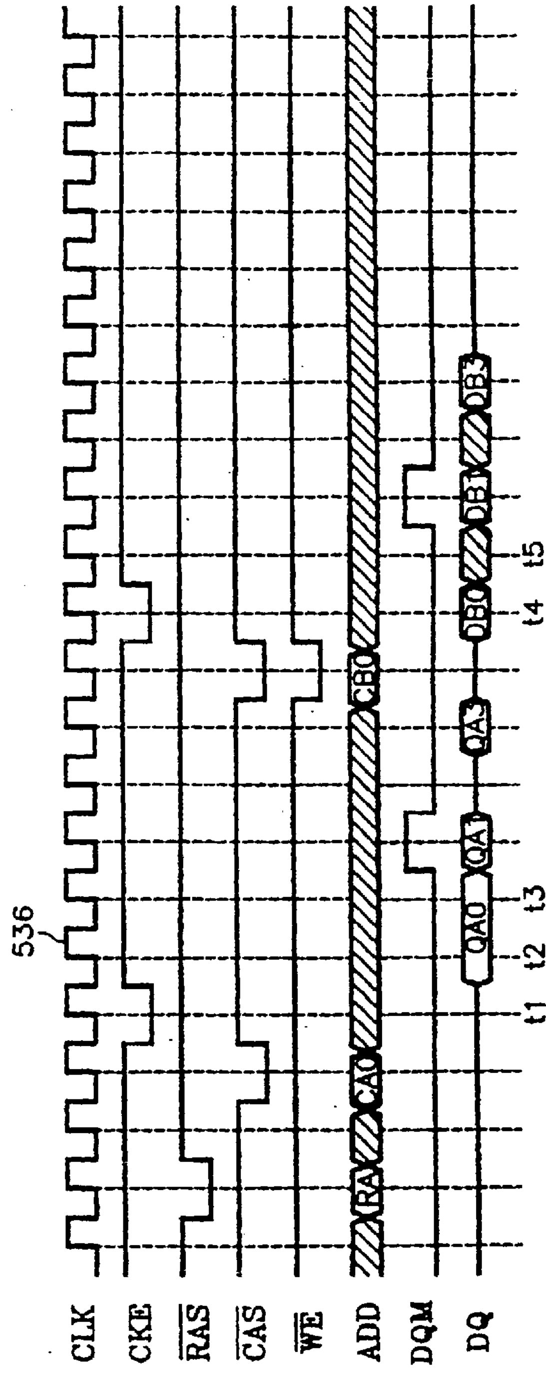


FIG. 55

RX-0925

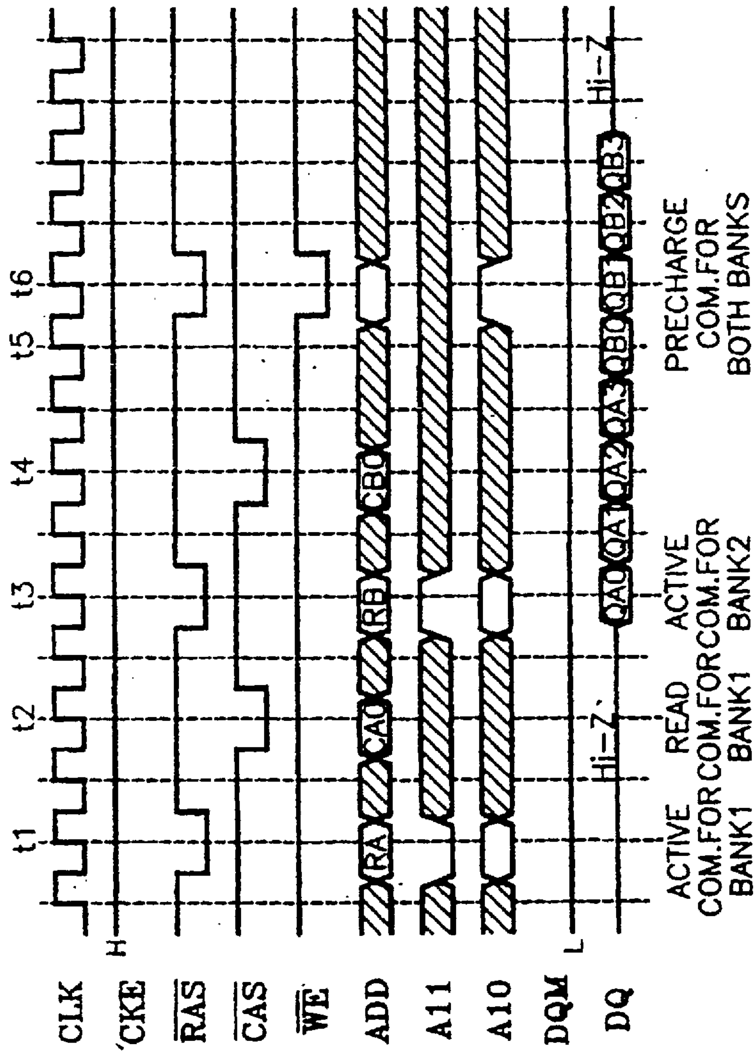


FIG. 56

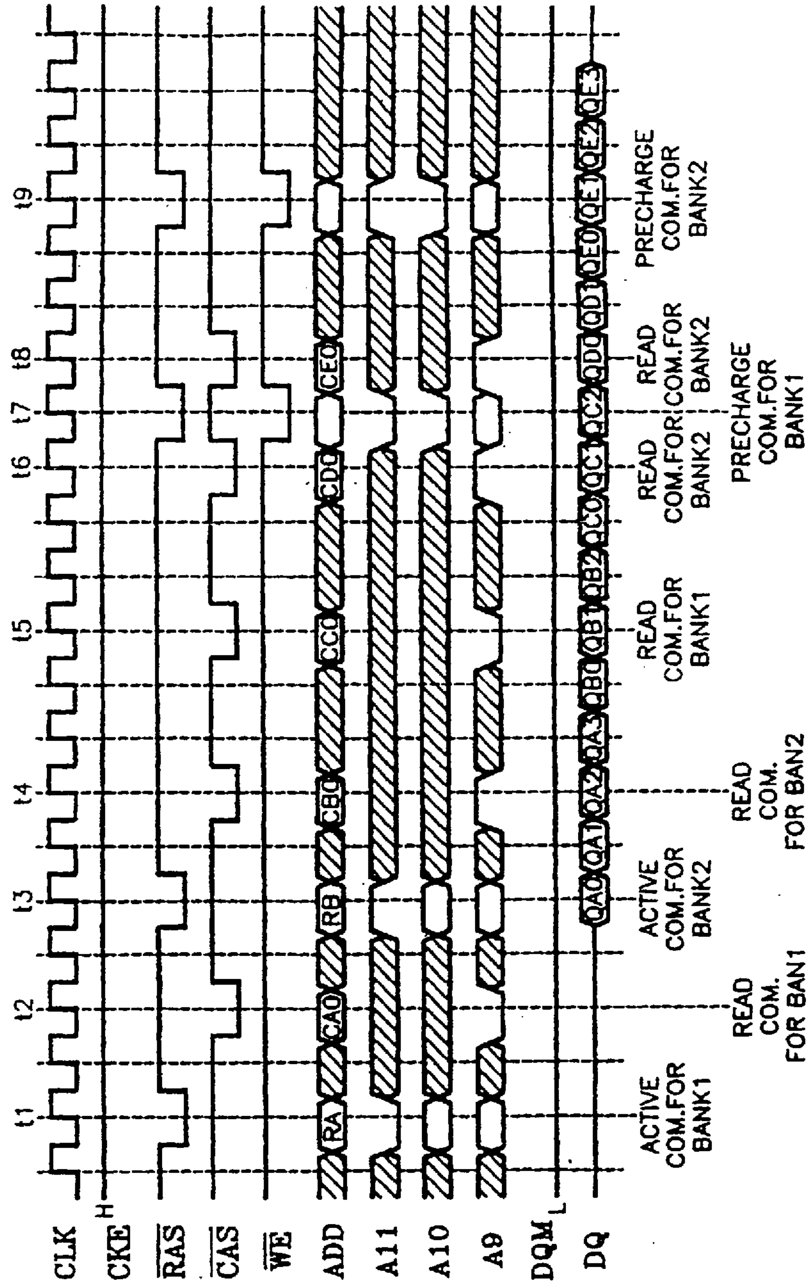


FIG. 57

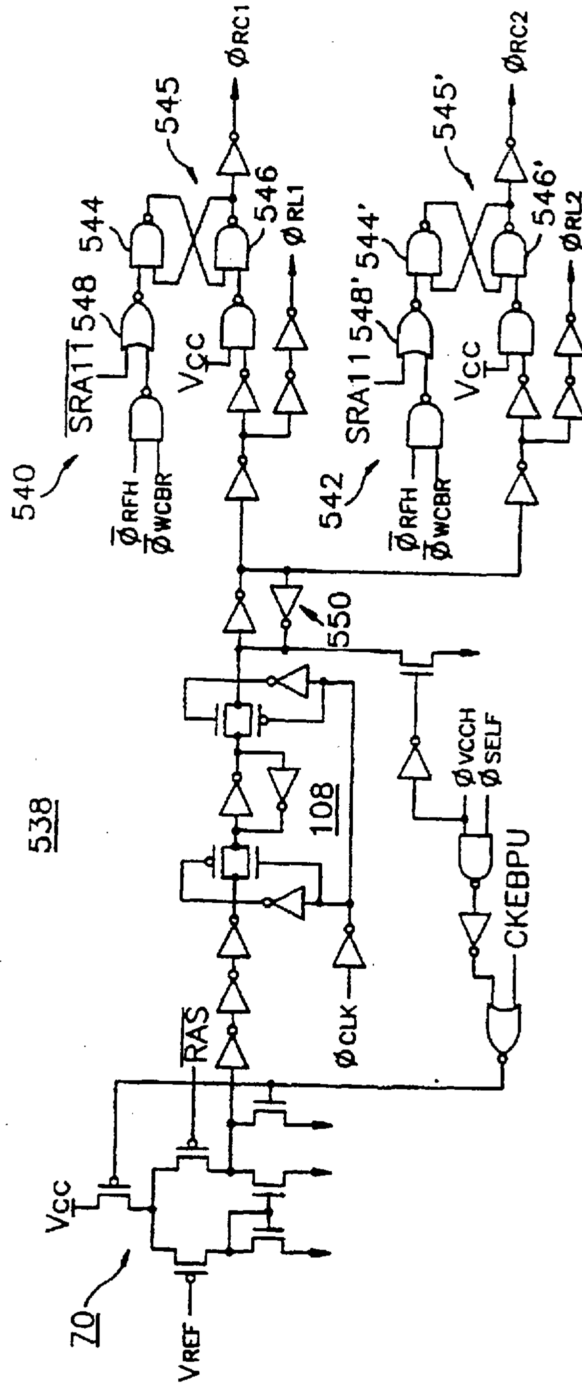


FIG. 58

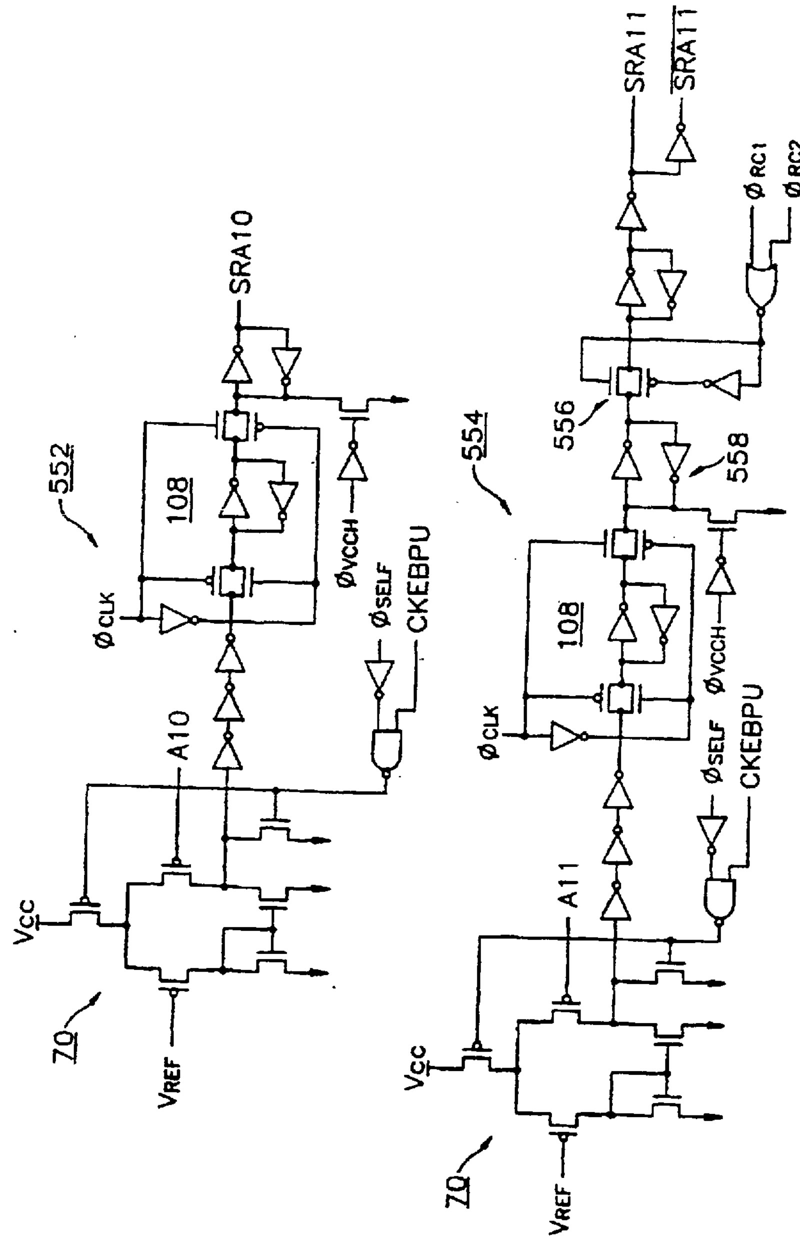


FIG. 59

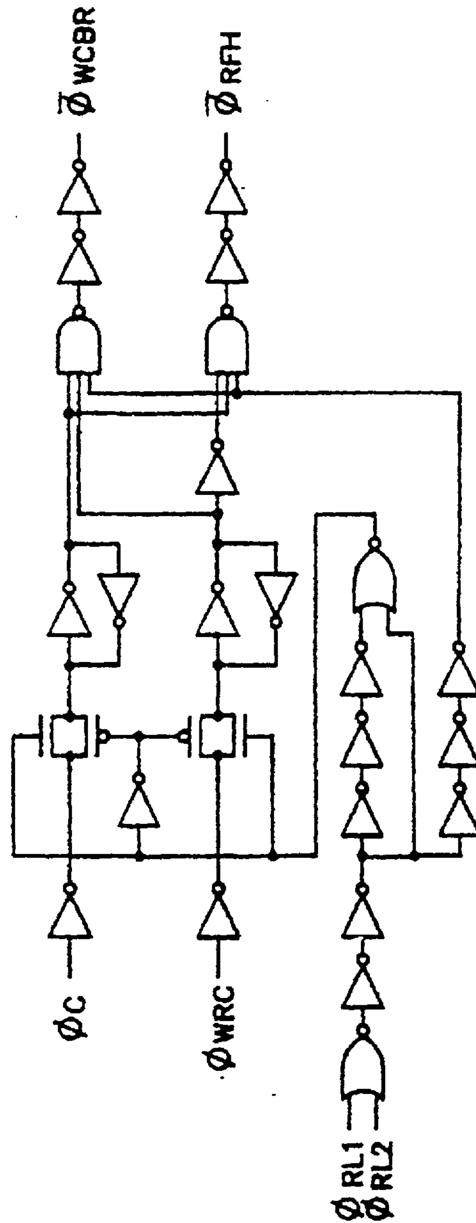


FIG. 60

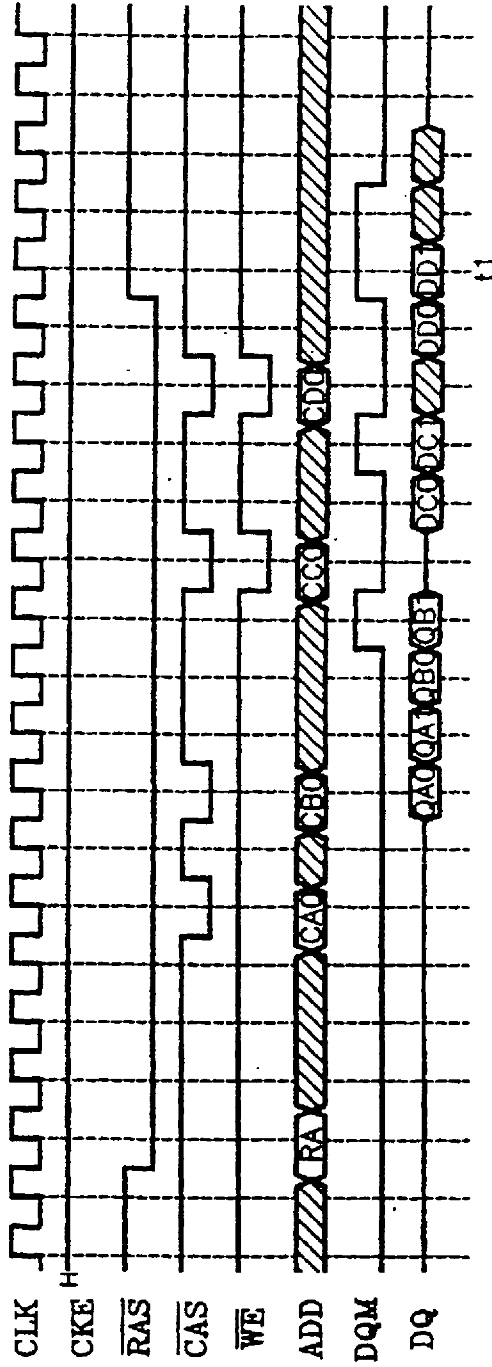


FIG. 61

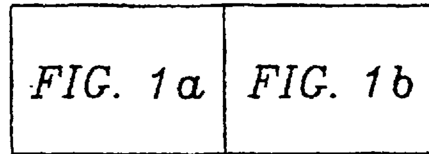


FIG. 1

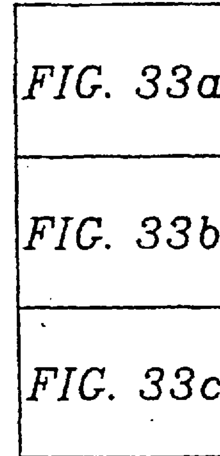


FIG. 33

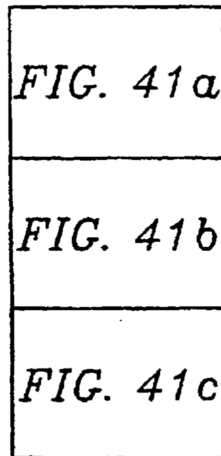


FIG. 41

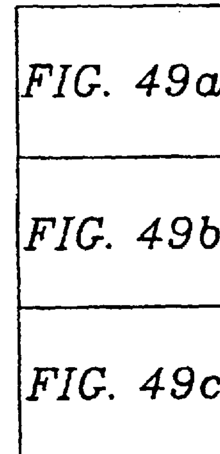


FIG. 49

FIG. 62

SYSTEM FOR SELECTING ONE OF A PLURALITY OF MEMORY BANKS FOR USE IN AN ACTIVE CYCLE AND ALL OTHER BANKS FOR AN INACTIVE PRECHARGE CYCLE

This is a division of application Ser. No. 08/130,138, filed Oct. 4, 1993.

FIELD OF THE INVENTION

The present invention relates to a semiconductor memory and, more particularly, to a synchronous dynamic random access memory which is capable of accessing data in a memory cell array disposed therein in synchronism with a system clock from an external system such as a central processing unit (CPU).

BACKGROUND INFORMATION

A computer system generally includes a CPU for executing instructions on given tasks and a main memory for storing data, programs or the like requested by the CPU. To enhance the performance of the computer system, it is basically requested to increase the operating speed of the CPU and also make an access time to the main memory as short as possible, so that the CPU can operate at least with no wait states. Operation clock cycles of modern CPUs such as recent microprocessors are shortening more and more as clock frequencies of 33, 66, 100 MHZ or the like. However, the operating speed of a high density DRAM, which is still the cheapest memory on a price-per-bit base and using as a main memory device, has not been able to keep up with that of the CPU being speeded up. DRAM inherently has a minimum $\overline{RAS}$ access time, i.e., the minimum period of time between activation of $\overline{RAS}$, upon which the signal $\overline{RAS}$ changes from a high level to a low level, and the output of data from a chip thereof with column addresses latched by activation of $\overline{CAS}$. Such a $\overline{RAS}$ access time is called a $\overline{RAS}$ latency, and the time duration between the activation of the signal $\overline{CAS}$ and the output of data therefrom called a $\overline{CAS}$ latency. Moreover, a precharging time is required prior to re-access following the completion of a read operation or cycle. These factors decrease the total amount of operation speed of the DRAM, thereby causing the CPU to have wait states.

To compensate for the gap between the operation speed of the CPU and that of the main memory like the DRAM, the computer system includes an expensive high-speed buffer memory such as a cache memory which is arranged between the CPU and the main memory. The cache memory stores information data from the main memory which is requested by the CPU. Whenever the CPU issues the request for the data, a cache memory controller intercepts it and checks the cache memory to see if the data is stored in the cache memory. If the requested data exists therein, it is called a cache hit, and high-speed data transfer is immediately performed from the cache memory to the CPU. Whereas if there is no presence therein, it is called a cache miss, and the cache memory controller reads out the data from the slower main memory. The read-out data is stored in the cache memory and sent to the CPU. Thus, a subsequent request for this data may be immediately read out from the cache memory. That is, in case of the cache hit, the high-speed data transfer may be accomplished from the cache memory. However, in case of the cache miss, the high-speed data transfer from the main memory to the CPU cannot be expected, thereby incurring wait states of the CPU. Thus, it is extremely important to

design DRAMs serving as the main memory to accomplish high-speed operations.

The data transfer between DRAMs and the CPU or the cache memory is accomplished with sequential information or data blocks. To transfer the continuous data at a high speed, various kinds of operating modes such as page, static column, nibble mode or the like have implemented in the DRAM. These operating modes are disclosed in U.S. Pat. Nos. 3,969,706 and 4,750,839. The memory cell array of the DRAM with the nibble mode is divided into four equal parts so that a plurality of memory cells can be made access with the same address. Data is temporarily stored in a shift register to be sequentially read out or written into. However, since the DRAM with the nibble mode cannot continuously transfer more than 5-bit data, the flexibility of the system design cannot be offered upon the application to high-speed data transfer systems. The page mode and the static column mode, after the selection of the same row address in a $\overline{RAS}$ timing, can sequentially access column addresses in synchronism with $\overline{CAS}$ toggling or cycles and with the transition detections of column addresses, respectively. However, since the DRAM with the page or the static column mode needs extra time, such as a setup and a hold times of the column address, for receiving the next new column address after the selection of a column address, it is impossible to access the continuous data at a memory bandwidth higher than 100 Mbits/sec., i.e., to reduce a $\overline{CAS}$ cycle time below 10 nsec. Also, since the arbitrary reduction of the $\overline{CAS}$ cycle time in the page mode cannot guarantee a sufficient column selection time to write data into selected memory cells during a write operation, error data may be written thereinto. However, since these high-speed operation modes are not operations synchronous to the system clock of the CPU, the data transfer system must use a newly designed DRAM controller whenever a CPU having higher speed is replaced. Thus, to keep up with high-speed microprocessors such as CISC and RISC types, the development of a synchronous DRAM is required which is capable of accessing the data synchronous to the system clock of the microprocessor at a high speed. An introduction to synchronous DRAMs appears with no disclosure of detailed circuits in the NIKKEI MICRODEVICES in April, 1992, Pages 158–161.

To increase the convenience of use and also enlarge the range of applications, it is more desirable to allow an on-chip synchronous DRAM to not only operate at various frequencies of the system clock, but also be programmed to have various operation modes such as a latency depending on each clock frequency, a burst length or size defining the number of output bits, a column addressing way or type, and so on. Examples for selecting an operation mode in DRAM are disclosed in U.S. Pat. No. 4,833,650 issued on May 23, 1989, as well as in U.S. Pat. No. 4,987,325 issued on Jan. 22, 1991 and assigned to the same assignee. These prior art patents disclose technologies to select one operation mode, such as page, static column and nibble modes. Selection of the operation mode in these prior art patents is performed by cutting off fuse elements by means of a laser beam from an external laser apparatus or an electric current from an external power supply, or by selectively wiring bonding pads. However, in these prior technologies, once the operation mode had been selected, the selected operation mode cannot be changed into another operation mode. Thus, the prior art does not permit changes between operation modes even if subsequently required.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a synchronous dynamic random access memory in which input/output of data is synchronous with an external system clock.

Another object of the present invention is to provide a synchronous dynamic random access memory with high performance.

Still another object of the present invention is to provide a synchronous dynamic random access memory which is capable of operating at a high data transfer rate.

A further object of the present invention is to provide a synchronous dynamic random access memory which is able of operating at various system clock frequencies.

Still a further object of the present invention is to provide a synchronous dynamic random access memory in which the number of input or output data may be programmed.

Another object of the present invention is to provide a counter circuit in which a counting operation can be performed in either binary or interleave mode.

Still another object of the present invention is to provide a semiconductor memory which can prohibit unnecessary internal operations of the memory chip regardless of the number of input or output data.

A further object of the present invention is to provide a semiconductor memory which can set various operation modes.

Still a further object of the present invention is to provide a semiconductor memory including a data transfer circuit for providing precharge and data transfer operable at a high data transfer rate.

Another object of the present invention is to provide a semiconductor memory which includes at least two memory banks whose operation modes can be set in on-chip semiconductor memory.

According to an aspect of the present invention, a semiconductor memory formed on a semiconductor chip having various operation modes, includes address input circuit for receiving external address designating at least one of the operation modes to the chip, a circuit for generating a mode set control signal in a mode set operation; and a circuit for storing codes based on the external address in response to the mode set control signal and producing an operation mode signal representing the operation mode determined by the codes.

According to another aspect of the present invention, a semiconductor memory having a plurality of internal operation modes includes a circuit for producing a power-on signal upon reaching of a power supply potential at a predetermined value after the application of the power supply potential, and a circuit for automatically storing a plurality of code signals in response to the power-on signal and producing internal operation mode signals indicating selected ones of the internal operation modes which are defined by the code signals.

According to another aspect of the present invention, a dynamic random access memory includes a plurality of memory banks, each bank including a plurality of memory cells and operable in either an active cycle indicating a read cycle or a write cycle, or a precharge cycle, a first circuit for receiving a row address strobe signal and producing a first signal, a second circuit for receiving a row address strobe signal and producing a first signal, a second circuit for receiving a column address strobe signal and producing a second signal, a third circuit for receiving a write enable signal and producing a third signal, an address input circuit for receiving address indicating the selection of the memory banks, and a logic circuit responsive to the first, second and third signals and the address signals including a latch circuit corresponding to the respective banks for storing data representing the active cycle for the bank selected by the address and data representing the precharge cycle for unselected banks.

According to still another aspect of the present invention, a dynamic random access memory receiving an external clock includes a plurality of memory banks each including a plurality of memory cells and operable in either an active cycle indicating a read cycle or a write cycle, or a precharge cycle, a circuit for receiving a row address strobe signal and latching a logic level of the row address strobe signal in response to one of a rising edge and a falling edge of the clock, an address input circuit for receiving an externally generated address selecting one of the memory banks, and a circuit for receiving the latched logic level from the receiving and latching circuit and the address from the address input circuit and for outputting an activation signal to the memory bank selected by the address and an inactivation signals to unselected memory banks when the latched logic level is a first logic level, so that the selected memory bank responsive to the activation signal operates in the active cycle while the unselected memory banks responsive to the inactivation signals operate in the precharge cycle.

According to still another aspect of the present invention, a semiconductor memory formed on a semiconductor chip receiving an external clock to the chip and outputting data read out from memory cells via data output buffer circuit, includes a circuit for generating a burst length signal representing the time interval of output of data and outputting data in synchronism with the clock via the data output buffer circuit during the time interval corresponding to the burst length signal.

According to further still another aspect of the present invention, a semiconductor memory includes a memory array having a plurality of memory cells arranged in rows and columns, a plurality of sub-arrays provided by partitioning the memory cell array in the row direction, each of the sub-arrays having a plurality of word lines respectively connected to associated columns of the memory cells and a plurality of bit lines respectively connected to associated rows of the memory cells, the bit lines of each sub-array divided into first groups of bit lines and second groups of bit lines, the respective ones of which are divided into first sub-groups of bit lines and second sub-groups of bit lines, the first groups of each sub-array alternately arranged with the second groups thereof, the first sub-groups of each sub-array alternately arranged with the second sub-groups thereof, and I/O buses respectively disposed in parallel to the word lines between the sub-arrays and on outer sides of the sub-arrays, and divided into first I/O buses and second I/O buses respectively arranged at odd and even positions, each I/O bus divided into first I/O lines and second I/O lines, the first and the second I/O lines of the respective first I/O buses respectively connected via column selection switches with the bit lines of the first and the second sub-groups of the first groups of sub-arrays adjacent thereto, the first and the second I/O lines of the respective second I/O buses respectively connected via column selection switches with the bit lines of the first and the second sub-groups of the second groups of sub-arrays adjacent thereto.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features, and advantages of the present invention are better understood by reading the

following detailed description of the invention, taken in conjunction with the accompanying drawings, wherein:

FIGS. 1*a* and 1*b* show a schematic plane view of various component parts formed on the same semiconductor chip of a synchronous DRAM according to the present invention;

FIG. 2 is a diagram showing an arrangement relationship with one of sub-arrays in FIG. 1 and input/output line pairs coupled thereto;

FIG. 3 is a schematic block diagram showing a row control circuit according to the present invention;

FIG. 4 is a schematic block diagram showing a column control circuit according to the present invention;

FIG. 5*a* and FIG. 5*b* are diagrams showing various commands used in operations of a pulse $\overline{RAS}$ and a level $\overline{RAS}$, respectively;

FIG. 6 is a schematic circuit diagram showing a clock (CLK) buffer according to the present invention;

FIG. 7.is a schematic circuit diagram showing a clock enable (CKE) buffer according to the present invention;

FIG. 8 is an operation timing diagram for the CLK buffer and the CKE buffer respectively showing in FIG. 6 and FIG. 7;

FIG. 9 is a schematic circuit diagram showing a multi-function pulse $\overline{RAS}$ input buffer according to the present invention;

FIG. 10 is a timing diagram for column control signals or clocks used in the present invention;

FIG. 11 is a schematic circuit diagram for a high frequency clock generator for generating multiplied clocks upon precharging according to the present invention;

FIG. 12 is a schematic circuit diagram for a column address buffer according to the present invention;

FIG. 13 is a schematic block diagram for an operation mode setting circuit according to the present invention;

FIG. 14 is a schematic circuit diagram for a mode set control signal generating circuit in FIG. 13;

FIGS. 15*a*, 15*b* and 15*c* are a schematic circuit diagram for an address code register in FIG. 13;

FIG. 16 is a schematic circuit diagram for a latency logic circuit in FIG. 13;

FIG. 17 is a schematic circuit diagram for a burst length logic circuit in FIG. 13;

FIG. 18 is a circuit diagram showing an auto-precharge control signal generating circuit according to the present invention;

FIG. 19 is a schematic circuit diagram for a row master clock generating circuit for generating a row master clock ϕ_{Ri} according to the present invention;

FIG. 20 is a timing diagram showing timing relationship for a mode set and an auto-precharge according to the present invention;

FIG. 21 is a circuit diagram showing a circuit for producing signals to enable the generation of column control signals;

FIG. 22 is an operation timing diagram for the high frequency clock generator of FIG. 11;

FIG.23 is a diagram showing a circuit block diagram on a data path associated with one of data buses according to the present invention;

FIG. 24 is a schematic circuit diagram for an I/O precharge and selection circuit according to the present invention;

FIG. 25 is a schematic circuit diagram for a data output multiplexer according to the present invention;

FIG. 26 is a schematic circuit diagram for a data output buffer according to the present invention;

FIG. 27 is a detail circuit diagram for a data input demultiplexes according to the present invention;

FIG. 28 is a schematic circuit diagram for a PIO line driver according to the present invention;

FIG. 29 is a schematic circuit diagram for a $\overline{CAS}$ buffer according to the present invention;

FIG. 30 is a schematic circuit diagram for a $\overline{WE}$ buffer according to the present invention;

FIG. 31 is a schematic circuit diagram for a DQM buffer according to the present invention;

FIG. 32 is a timing diagram showing the operation of the DQM buffer if FIG. 31;

FIGS. 33*a*, 33*b* and 33*c* are a timing diagram showing a writing operation according to the present invention;

FIG. 34 is a schematic circuit diagram for a column address buffer according to the present invention;

FIG. 35 is a schematic block diagram for a column address counter according to the present invention;

FIG. 36*a* and 36*b* are schematic circuit diagram for each stage which constitutes a first counting portion in FIG. 35;

FIG. 37 is a timing diagram showing the operation of the circuit of FIG. 36*a*;

FIG. 38 is a schematic block diagram for a column decoder according to the present invention;

FIG. 39*a* is a schematic circuit diagram for a first predecoder in FIG. 38;

FIG. 39*b* is a schematic circuit diagram for a second predecoder in FIG. 38;

FIG. 40 is a schematic circuit diagram for one of main decoders in FIG. 38;

FIGS. 41*a*, 41*b* and FIG. 41*c* are a timing diagram showing a reading operation according to the present invention;

FIG. 42 and FIG. 43 are schematic circuit diagrams for a burst length detection circuit in FIG. 4;

FIG. 44 is a schematic circuit diagram for a column address reset signal generator in FIG. 4;

FIG. 45 is a schematic block diagram for a transfer control counter in FIG. 4;

FIG. 46 is a schematic circuit diagram for a read data transfer clock generator in FIG. 4;

FIG. 47 is a schematic circuit diagram showing a circuit for generating a signal ϕ_{CL} using in the data output multiplexer of FIG. 25;

FIG. 48 is a schematic circuit diagram for a write data transfer clock generator in FIG. 4;

FIGS. 49*a*, 49*b* and FIG. 49*c* are a timing diagram for a $\overline{CAS}$ interrupt write operation according to the present invention;

FIG. 50 is a schematic circuit diagram showing a circuit for generating control signals precharging I/O lines and PIO lines according to the present invention;

FIG. 51 is a schematic circuit diagram showing a circuit for generating control signals precharging DIO lines according to the present invention;

FIG. 52 is a schematic circuit diagram showing a circuit for generating bank selection signals using in the PIO line driver of FIG. 28;

FIG. 53 is a schematic circuit diagram showing a control circuit for generating control signals being used in the data output buffer of FIG. 26;

FIGS. 54, 55, 56 and FIG. 57 are timing diagrams showing the timing relationship according to various operation modes in the synchronous DRAM using the pulse $\overline{RAS}$;

FIG. 58 is a schematic circuit diagram for a $\overline{RAS}$ buffer using in the level $\overline{RAS}$;

FIG. 59 is a schematic circuit diagram for a special address buffer according to the present invention;

FIG. 60 is a schematic circuit diagram showing a control circuit for generating a mode set master clock and a refresh master clock which use in the level $\overline{RAS}$;

FIG. 61 is a timing diagram showing the operation timing relationship in the synchronous DRAM using the level $\overline{RAS}$; and

FIG. 62 is a diagram showing the manner in which the separate sheets of drawings of FIG. 1*a* and FIG. 1*b*, FIG. 33*a* to FIG. 33*c*, FIG. 41*a* to FIG. 41, and. FIG. 49*a* to FIG. 49*c* are combined.

DETAILED DESCRIPTION OF THE INVENTION

Preferred embodiments of the present invention will be discussed referring to the accompanying drawings. In the drawings, it should be noted that like elements represent like symbols or reference numerals, wherever possible.

In the following description, numerous specific details are set forth such as the number of memory cells, memory cell arrays or memory banks, specific voltages, specific circuit elements or parts and so on in order to provide a thorough understanding of the present invention. It will be obvious to those skilled in the art that the invention may be practiced without these specific details.

The synchronous DRAM in its presently preferred embodiment is fabricated employing a twin well CMOS technology and uses n-channel MOS transistors having a threshold voltage of 0.6 to 0.65 volts, p-channel MOS transistors having a threshold voltage of −0.8 to −0.85 volts and power supply voltage Vcc of approximately 3.3 volts.

CHIP ARCHITECTURE

Referring to FIG. 1 comprising FIG. 1*a* and FIG. 1*b*, illustration is made on a schematic plane view for various element portions formed on the same semiconductor chip of a synchronous DRAM according to the present invention. The DRAM in the present embodiment is a 16,777,216 bit (16-Mbit) synchronous DRAM made up of 2,097,152 (2M) ×8 bits. Memory cell arrays are partitioned into a first bank 12 and a second bank 14, as respectively shown in FIG. 1*a* and FIG. 1*b*, in order to increase a data transfer rate. Each bank comprises an upper memory cell array 16T and a lower memory cell array 16B respectively positioned at upper and lower portions, each of which contains memory cells of 4,194,304 bits (4-Mbit). The upper and the lower memory cell arrays are respectively divided into left memory cell arrays 20TL and 20BL and right memory cell arrays 20TR and 20BR of 2-Mbit memory cells each, neighboring on their lateral sides. The left and the right memory cell arrays of the upper memory cell array 16T of each bank will be respectively referred to as a upper left memory cell array or a first memory cell array 20TL and a upper right memory cell array or a third memory cell array 20TR. Likewise, the left and the right memory cell arrays of the lower memory cell array 16B of each bank will be respectively referred to as a lower left memory cell array or a fourth memory cell array 20BR. Thus, each bank is divided into four memory

cell arrays consisting of the first to the fourth memory cell arrays. The upper left and right memory cell arrays and the lower left and right memory cell arrays are respectively divided into 8 upper left submemory cell arrays (or upper left sub-arrays) 22TL1 to 22TL8, 8 upper right submemory cell arrays (or upper right sub-arrays) 22TR1 to 22TR8 and 8 lower right submemory cell arrays (or lower right sub-arrays) 22BR1 to 22BR8. Each of the sub-arrays has 256K-bit memory cells arranged in a matrix form of 256 rows and 1,024 columns. Each memory cell is of a known one-transistor one-capacitor type.

In each bank, a row decoder 18 is arranged between the upper memory cell array 16T and the lower memory cell array 16B. The row decoder 18 of each bank is connected with 256 row lines (word lines) of each sub-array. Word lines of respective one of the upper and the lower sub-array pairs 22TL1, 22BL1; 22TL2, 22BL2; . . . ; 22TR8, 22BR8 arranged in a symmetrical relationship with respect to the row decoder 18 are extending in opposite directions therefrom in parallel with a vertical direction. The row decoder 18 responsive to row addresses from a row address buffer selects one of sub-arrays and one of word lines of the respectively selected sub-arrays and provides a row driving potential on each selected word line. Thus, in response to given row addresses in each bank, the row decoder 18 selects total four word lines: one word line selected in a selected one of the upper left sub-arrays 22TL1–22TL8, one word line selected in a selected one of the lower left sub-arrays 22BL1–22BL8, one word line selected in a selected one of the upper right sub-arrays 22TR1–22TR8 and one word line selected in a selected one of the lower right sub-arrays 22BR1–22BR8.

Column decoders 24 are respectively positioned adjacent to right side ends of the upper and the lower memory cell arrays 16T and 16B in the first bank 12 and to left side ends of the upper and lower memory cell arrays 16T and 16B in the second bank 14. Each of the column decoders 24 is connected to 256 column selection lines which are parallel in the horizontal direction and perpendicular to the word lines, serving as selecting one of the column selection lines in response to a column address.

I/O buses 26 are located adjacent to both side ends of the respective sub-arrays 22TL, 22BL, 22TR and 22BR, extending in parallel with the word lines. The I/O buses 26 between opposite side ends of sub-arrays are shared by these two adjacent sub-arrays. Each of the I/O buses 26 is composed of our pairs of I/O lines, each pair of which consists of two signal lines in the complementary relation and is connected with corresponding bit line pair via a column selection switch and a sense amplifier.

Referring now to FIG. 2, for purposes of simplicity, the drawing is represented which illustrates the arrangement of an odd numbered one of sub-arrays 22TL1 to 22TR8 in the upper memory cell array 16T and that of I/O buses associated therewith. A first or left I/O bus 26L and a second or right I/O bus 26R respectively run in parallel with wordlines WL0–WL255 at left and right ends of the sub-array 22. Each of the first and the second I/O buses 26L and 26R consists of first I/O line pairs which are composed of I/O line pairs I/O0, $\overline{I/O0}$ and I/O1, $\overline{I/O1}$, and second I/o line pairs which are composed of I/O line pairs I/O2, $\overline{I/O2}$ and I/O3, $\overline{I/O3}$. The sub-array 22 contains 1,024 bit line pairs 28 perpendicular to the word lines WL0–WL255 which are arranged in a folded bit line fashion. Memory cells 30 are located at crosspoints of word lines and bit lines. The bit line pairs 28 constituting the sub-array 22 are divided into a plurality of first bit line groups 28L1 to 28L256 arranged at odd loca-

tions and a plurality of second bit line groups 28R1 to 28R256 arranged at even locations. Each of the bit line groups has a given number of bit line pairs (2 bit line pairs in the present embodiment). The first bit line groups 28L are arranged to alternate with the second bit line groups 28R. Odd numbered bit line pairs (or first sub-groups) 28L1, 28L3, . . . , 28L255 and even numbered bit line pairs (or second sub-groups) 28L2, 28L4, . . . , 28L256 of the first bit line groups 28L are respectively connected with the first I/O line pairs and the second I/O line pairs of the first I/O bus 26L via corresponding sense amplifiers 32L and column selection switches 34L. In the same manner, odd numbered bit line pairs (or first sub-groups) 28R1, 28R3, . . . , 28R255 and even numbered bit line pairs (or second sub-groups) 28R2, 28R4, . . . , 28R256 of the second bit line groups 28R are respectively connected with the first I/O line pairs and the second I/O line pairs of the second I/O bus 28R via corresponding amplifiers 32R and column selection switches 34R. First column selection lines L0, L2, . . . and L254, which are connected with column selection switches associated with the first I/O line pairs I/O0, $\overline{I/O0}$ and I/O1, $\overline{I/O1}$ in left and right I/O buses 26L and 26R, are arranged in parallel to alternate with second column selection lines L1, L3, . . . and L255 which are connected to column selection switches associated with the second I/O line pairs I/O2, $\overline{I/O2}$ and I/O3, $\overline{I/O3}$ therein. Thus, in a read operation, after the selection of one word line, i.e., one page with row addresses, the first and the second I/O line pairs in the left and right I/o buses 26L and 26R provide continuous data, alternating data of two bits each by sequentially selecting column selection lines L0 to L255. Line pairs 36, which are connected with corresponding sense amplifiers 32L and 32R and are alternately running in opposite directions, are respectively connected with corresponding bit line groups 28L and 28R via corresponding sense amplifiers within sub-arrays adjacent to the first and second I/O buses 26L and 26R. That is, the first I/O line pairs and the second I/O line pairs of the first I/O bus 26L are respectively connected with odd numbered bit line pairs (or first sub-groups) and even numbered bit line pairs (or second sub-groups) of the first bit line groups of a left adjacent sub-array (not shown) via corresponding column selection switches 32L and corresponding sense amplifiers. In the same manner, the first I/O line pairs and the second I/O line pairs of the second I/O bus 26R are respectively connected with odd numbered bit line pairs (or first sub-groups) and even numbered bit line pairs (or second sub-groups) of the second bit line groups of a right adjacent sub-array (not shown) via corresponding column selection switches 32R and corresponding sense amplifiers. Thus, since bit line pairs of the respective sub-arrays are divided in the same manner as the first and second bit line groups of the sub-array 22 as shown in FIG. 2, I/O buses associated with the first bit line groups are alternately arranged with I/O buses associated with the second bit line groups. That is, each of first I/O buses positioned at odd locations is associated with the first bit line groups in two sub-arrays adjacent thereto while each of second I/O buses positioned at even locations is associated with the second bit line groups in two sub-arrays adjacent thereto. Regarding to the respective ones of the sub-arrays of FIG. 1, the connection relationship with the first and second I/O line pairs of the first and second I/O buses will be incorporated by the explanation made in connection with FIG. 2. The sense amplifier 32L and 32R may be of a known circuit which is composed of a P-channel sense amplifier, transfer transistors for isolation, an N-channel sense amplifier and an equalizing and precharging circuit. Thus, I/O buses 26 between adjacent two sub-arrays are common I/O buses for reading or writing data from/to the sub-array which is selected by the control of the isolation transfer transistors.

Returning to FIG. 1, in each bank, at the upper portion of the first and the third memory cell arrays 20TL and 20TR are respectively located I/O line selection and precharge circuits 38TL and 38TR and I/O sense amplifiers and line drivers 40TL and 40TR correspondingly connected, thereto, and likewise, at the lower portion of the second and the fourth memory cell arrays 20BL and 20BR are respectively located I/O line selection and precharge circuits 38BL and 38BR and I/O sense amplifiers and line drivers 40BL and 40BR correspondingly connected thereto. I/O line selection and precharge circuits 38TL, 38TR, 38BL and 38BR are respectively connected to alternating I/O buses 26 in corresponding memory cell arrays 20TL, 20TR, 20BL and 20BR. That is, I/O line selection and precharge circuits positioned at odd locations are respectively connected with I/O bus pairs of I/O buses disposed at odd locations in corresponding memory cell arrays, and I/O line selection and precharge circuits positioned at even locations are respectively connected with I/O bus pairs of even located I/O buses in corresponding memory cell arrays. Therefore, in each bank, each of circuits at the outer most side of the I/O line selection and precharge circuits may access data to/from memory cells which are connected with first bit line groups in three sub-arrays, and odd positioned I/O line selection and precharge circuits and even positioned I/O line selection and precharge circuits, which are excluding the outer most I/O line selection and precharge circuits, are respectively associated with the first bit line groups and the second bit line groups. Each I/O line selection and precharge circuit 38 comprises an I/O bus selection circuit for selecting one of a pair of I/O buses connected thereto and an I/O line precharge circuit for precharging, when any one of first I/O line pairs I/O0, $\overline{I/O0}$ and I/O1, $\overline{I/O1}$ and second I/O line pairs I/O2, $\overline{I/O2}$ and I/O3, $\overline{I/O3}$ which constitute the selected I/O bus is transferring data, the other I/O line pairs.

I/o line selection and precharge circuits 38 are respectively connected to corresponding I/O sense amplifiers and line drivers 40 via PIO buses 44. Each PIO bus 44 is connected with an I/O bus selected by corresponding I/O bus selection circuit. Thus, PIO buses 44 comprise four pairs of PIO lines like I/O buses 26. Each I/O sense amplifier and line driver 40 comprises an I/O sense amplifier for amplifying data inputting via corresponding I/O bus selection circuit and PIO bus in a read operation, and a line driver for driving to an I/O bus selected by the I/O bus selection circuit data inputting via corresponding I/O bus selection circuit and PIO bus in a write operation. Thus, as discussed above, if data on any ones of the first and the second I/O line pairs inputs to the sense amplifier via corresponding PIO line pairs, PIO line pairs connected to the other I/O line pairs are precharged together with the I/O line pairs. Also, in the writing operation, when the driver 40 drives data to corresponding I/O line pairs via selected PIO line pairs, unselected PIO line pairs and their corresponding I/O line pairs start precharging.

At the upper most and the lower most ends of the synchronous DRAM chip, upper data buses 42T and lower data buses 42B are respectively running in parallel with the horizontal direction. Each of upper data buses 42T and lower data buses 42B consist of four data buses, each of which comprises four pairs of data lines which are the same number as above mentioned I/O bus and PIO bus. One side ends of four data buses DB0-DB3 constituting upper data buses 42T and four data buses DB4-DB7 constituting lower

data buses are respectively connected to data input/output multiplexers 46 coupled to input/output pads (not shown in the drawing) via input/output lines 47 and data input/output buffers 48.

In each bank, I/O sense amplifiers and line drivers 40TL associated with the first memory cell array 20TL are alternately connected to first and second data buses DB0 and DB1, and I/O sense amplifiers and line drivers 40TR associated with the third memory cell array 20TR are interleavely connected to third and fourth data buses DB2 and DB3. Likewise, I/O sense amplifiers and line drivers 40BL associated with the second memory cell array 20BL are interleavely connected to fifth and sixth data buses DB 4 and DB5, and I/O sense amplifiers and line drivers 40BR associated with the fourth memory cell array 20BR are interleavely connected to seventh and eighth data buses. Center I/O sense amplifiers and line drivers 43T and 43B are respectively connected to I/O buses between the first memory cell array 20TL and the third memory cell array 20TR and between the second memory cell array 20BL and the fourth memory cell array 20BR in each bank. In each bank, center I/O sense amplifier and line driver 43T at the upper portion comprises an I/O sense amplifier for amplifying data on corresponding I/O bus to couple to the data bus DB1 or DB3 in response to a control signal in a write operation. Likely, center I/O sense amplifier and line driver 43 at the lower portion is connected to the fourth and the eighth data buses DB5 and DB7.

Now, assuming that sub-arrays 22TL3, 22BL3, 22TR3 and 22BR3 in the first bank 12 and one word line in their respective sub-arrays would be selected by the row decoder 18 responded by a row address, the row decoder 18 provides block information signals designating respective sub-arrays 22TL3, 22BL3, 22TR3 and 22BR3. Then, in a read operation, a control circuit, as will be discussed hereinbelow, generates sequential column addresses in response to an external column address and the column decoder 24 generates sequential column selection signals in response to this column address stream. Assuming that the first column selection signal is to select a column selection line L0, corresponding column selection switch 34 shown in FIG. 2 is turned on and data developed on corresponding bit line pairs is transferred to first I/O line pairs I/O0, $\overline{I/O0}$ and I/O1, $\overline{I/O1}$ of left and right I/O buses arranged at both ends of the respective selected sub-arrays. I/O line selection and precharge circuits 38TL, 38BL, 38TR and 38BR respond to the block information signals, and I/O line selection and precharge circuits associated with the selected sub-arrays 22TL3, 22B13, 22TR3 and 22BR3 thereby select the left and the right I/O buses associated therewith. Data on the first I/O line pairs in the left and the right I/O buses is transferred to corresponding data line pairs in corresponding data buses DB0-DB7 via corresponding PIO line pairs and corresponding sense amplifiers turned on by a control signal which is generated in response to the block information signals. However, at this time, I/O line pairs not transferring data, i.e., the second I/O line pairs and PIO line pairs connected thereto are all held in a precharging state by the I/O precharge circuits. Also, data line pairs not transferring data are being precharged by data input/output multiplexers 46 as will be explained hereinbelow. Then, if by the second column selection signal CSL1 on the column line L1 of the column address stream are turned on corresponding column selection switches, in the same manner as preciously discussed, data on corresponding bit lies is transferred via the second I/O line pairs in the left and the right I/O buses and corresponding PIO line pairs to data line pairs, whereas the first I/O line pairs, PIO line pairs and data line pairs connected thereto are precharged to transfer data from now on. If column selection signals CSL2 to CSL255 on column lines L2 to L255 following the column selection signal CSL1 on the column line L1 are sequentially received, the same operations as data transfer operations in case of the column selection signals CSL0 and CSL1 are performed repetitively. Thus, all data on bit line pairs which is developed from all memory cells coupled to selected word lines can be read out. That is, full page read-out is available. In the read operation, the first I/O line pairs and the second I/O line pairs transfer a plurality of data, alternating data transfer and precharge, and the first and the second data line pairs associated with the first and the second I/O line pairs, also, repeat data transfer and precharge periodically. The data output multiplexer connected to each data bus not only stores a plurality of data transferred in parallel via any one of the first and the second data line pairs, but also precharges the other data line pairs. Thus, each data output multiplexer provides continuous serial data in response to data selection signals, prefetching a plurality of data on the first and the second data line pairs with a predetermined period. The serial data outputs via corresponding data output buffer to data input/output pads in synchronism with a system clock. Therefore, 8-bit parallel data continuously outputs every clock cycle thereof.

Write operation is performed in the inverse order of the read operation as discussed above. As will be explained in brief, serial input data outputs in synchronism with the system clock from data input buffers via data interleavely pads. The serial data from the data input buffers is interleavely transferred to the first and the second data line pairs of corresponding data buses in a plurality of parallel data every clock cycles of the system clock by means of respective data input demultiplexers. Data on the first and the second data line pairs is sequentially written into selected memory cells via corresponding line drivers, I/O buses selected by the I/O line selection circuits and corresponding bit line pairs. Data transfer and precharge of the first and the second line pairs are alternately effected every clock cycles in the same manner as those in the read operation.

Between the first and the second banks is arranged the control circuit 50 for controlling operations of the synchronous DRAM according to the present invention. The control circuit 50 serves to generate control clocks or signals for controlling the row and the column decoders 18 and 24, I/O line selection and precharge circuits 38, I/O sense amplifiers and line drivers 40 and 43, data input/output multiplexers 46 and data input/output buffers 48. The control circuit 50 may be classified into a row control circuit and a column control circuit. The row control circuit, the data path and the column control circuit will be separately discussed hereinbelow.

ROW CONTROL CIRCUIT

Conventional DRAMs are activated to perform the operation of read, write or the like by a logic level of $\overline{RAS}$, for example, a low level. This will be referred to as a level RAS. The level $\overline{RAS}$ gives a certain information, for example, such information as the transition of $\overline{RAS}$ from high to low level indicates the activation thereof and the transition of $\overline{RAS}$ from low to high level indicates precharging. However, since the synchronous DRAM has to operate in synchronism with the system clock, above-mentioned commands using in the conventional DRAM cannot be employed in the synchronous DRAM. That is, since the synchronous DRAM needs to sample a command information at the leading edge or the falling edge of the system

clock (sampling the command information in this embodiment is accomplished at the leading edge thereof), even if the level $\overline{RAS}$ is applied in the synchronous DRAM, commands of the conventional level $\overline{RAS}$ cannot be used therein.

FIG. 5a and FIG. 5b are timing diagrams representative of commands used in the synchronous DRAM of the present invention. FIG. 5a represents various commands in case that $\overline{RAS}$ signal of pulse (hereinafter referred to as a pulse $\overline{RAS}$) is used, and FIG. 5b various commands in case of the use of level $\overline{RAS}$. As can be seen in the drawings, when $\overline{RAS}$ is low and $\overline{CAS}$ signal and write enable signal $\overline{WE}$ are high at the leading edge of the system clock CLK, this means an activation. After the activation, at the leading edge of the system clock, the high level $\overline{RAS}$, the low level $\overline{CAS}$ and the high level $\overline{WE}$ indicate a read command. Also, after activation, at the leading edge of the system clock CLK, the high level $\overline{RAS}$, the low level $\overline{CAS}$ and low level $\overline{WE}$ represent a write command. When the low level $\overline{RAS}$, the high level $\overline{CAS}$ CAS and the low level $\overline{WE}$ have been sampled at the leading edge of the clock CLK, a precharging operation is performed. An establishment of operation mode set command according to the feature of the present invention is accomplished at low levels of $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ at the leading edge of the clock CLK. A $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh command inputs when $\overline{RAS}$ and $\overline{CAS}$ hold at low levels and $\overline{WE}$ holds at a high level at the leading edge of the clock CLK. A self refresh command, which is a variation of the CBR refresh, inputs when $\overline{RAS}$ and $\overline{CAS}$ line at low levels and $\overline{WE}$ stays at a high level at successive three leading edges of the clock CLK.

In the same manner as conventional DRAM, the synchronous DRAM, also, inherently has the time period from the activation of $\overline{RAS}$ until the activation of $\overline{CAS}$, i.e. $\overline{RAS}$-$\overline{CAS}$ delay time t_{RCD} and the precharging time period prior to the activation of $\overline{RAS}$, i.e. $\overline{RAS}$ precharge time t_{RP}. To guarantee the read-out and the write-in of valid data, minimum values of tRCD and t_{RP} (respectively 20 ns and 30 ns in the synchronous DRAM of the present invention) are very important to memory system designers. To promote the convenience for system designers, it may be more preferred that the minimum values of t_{RCD} and t_{RP} are provided in the number of system clock cycle. For example, in case that the system clock frequency is 100 MHZ and the minimum values of t_{RCD} and t_{RP} are respectively 20 ns and 30 ns, clock cycles of t_{RCD} and t_{RP} respectively become 2 and 3. The row control circuit is means for generating signals or clocks for selecting word lines during the time period of t_{RCD}, developing to bit lines information data from memory cells in a read operation and precharging during the time period of t_{RP}.

FIG. 3 is a diagram representing a schematic block diagram for generating row control clocks or signals. Referring to the drawing, a clock buffer (hereinafter referred to a CLK buffer) 52 is a buffer for converting into an internal system clock ϕ_{CLK} of CMOS level in response to an external system clock CLK of TTL level. The synchronous DRAM executes various internal operations which are sampling signals from the external chip or data to the external chip at the leading edge of the clock CLK. The CLK buffer 52 generates a clock CLK faster than the phase of the clock CLK in response to CLK.

A clock enable (CKE) buffer 54 is a circuit for generating a clock masking signal ϕ_{CKE} in order to make the generation of the clock ϕ_{CKE} in response to an external clock enable signal CKE and the clock CLK. As will be discussed hereinbelow, the internal system clock ϕ_{CKE} disabled by the signal ϕ_{CKE} causes the internal operation of the chip to be frozen and input and output of data is thereby blocked.

$\overline{RAS}$ buffer 56 receives the external signal $\overline{RAS}$, address signals SRA10 and SRA11, a signal ϕ_C from a $\overline{CAS}$ buffer and a signal ϕ_{WRC} from a $\overline{WE}$ buffer, thereby generating $\overline{RAS}$ clock ϕ_{RCi} for selectively activating bands in synchronous with the clock ϕ_{CLK}, selectively or totally precharging the banks and automatically precharging after refreshing or operation mode programming. Wherein i is a symbol for representing bank. Also, the $\overline{RAS}$ buffer 56 generates signal ϕ_{RP} which represents the activation of $\overline{RAS}$ with the clock ϕ_{CKE}.

An operation mode set circuit 58 is responsive to the operation mode set command, signals ϕ_{RP}, ϕ_C and ϕ_{WRC} and address signals RA0–RA6f so as to set various operation modes, for example, operation modes for establishing a $\overline{CAS}$ latency, a burst length representing the number of continuous output data and an address mode ϕ_{INTEL} representing a scrambling way of internal column address. The operation mode set circuit 58 sets a default operation mode in which predetermined $\overline{CAS}$ latency, burst length and address mode are automatically selected upon the absence of the operation mode set command.

A row master clock generator 62 is responsive to the control signal ϕ_{RCi} and a latency signal CLj and generates a row master clock ϕ_{Ri} which is based on the generation of clocks or signals associated with $\overline{RAS}$ chain in a selected bank. According to the characteristics of the present invention, the row master clock ϕ_{Ri} has time a delay depending on a designated $\overline{CAS}$ latency and such a time delay guarantees 2-bit data output synchronous to the system clock after the precharge command.

A row address buffer 60 receives the row master clock ϕ_{Ri}, external address signals A0–A11 and a row address reset signal ϕ_{RARi} to generate row address signals RA0–RA11 in synchronism with the clock ϕ_{CLK}. The buffer 60 receive a count signal from a refresh counter in a refresh operation to provide row address signals RA0–RA11 for refreshing.

A row control signal generator 64 receives the row master clock ϕ_{Ri} and a block information signal BLS from the row decoder 18 to generate a boosted word line driving signal ϕ_{x}, a sensing start signal ϕ_s for activating the selected sense amplifier, a row address reset signal ϕ_{RARi} for resetting the column address buffer, a signal ϕ_{RARi} for powering on the row address buffer 60 and a signal ϕ_{RCDi} for informing the completion of clocks or signals associated with rows.

A column enable clock generator 66 receives the signal ϕ_{RCDi} and the row master clock ϕ_{Ri} to generate signals ϕ_{YECi} and ϕ_{YEi} for enabling column related circuits.

A high frequency clock generator 68 generates, in case that the frequency of the external system clock CLK is low and the 2-bit data output is also required in a read operation after a precharge command, a clock CNTCLK9 with a higher frequency than the clock CLK to prevent the reduction of precharge period. As will be discussed hereinbelow, since the column address generator generates column addresses with the clock CNTCLK9, the reduction of precharge period is prevented.

Hereinbelow, explanation will be made in detail on preferred embodiments of elements constituting the $\overline{RAS}$ chain clock generator.

1. CLK Buffer & CKE Buffer

FIG. 6 is a diagram representing a schematic circuit diagram for the CLK buffer 52 according to the present invention, and FIG. 7 is a schematic circuit diagram for CKE buffer 54 according to the present invention. FIG. 8 depicts an operation timing diagram for the CLK buffer 52 and the CKE buffer 54.

Referring to FIG. 6, a differential amplifier 70 compares the external system clock CLK with a reference potential V_{REF} (=1.8 volts) and thereby converts the external signal CLK of TTL level into an internal signal of CMOS level, for example, a high level of 3 volts or a low level of 0 volt. Instead of the differential amplifier 70, another input buffers can be used which can level shift from the TTL to the CMOS signal. As can be seen in FIG. 8, the clock CLKA is of the signal inverted to the system clock CLK via the input buffer 70, such as the differential amplifier, and gates, i.e., inverters 76 and NAND gate 78. A flip-flop or a latch 80 which is composed of NOR gates 72 and 74 outputs a system clock of CMOS level when a clock masking signal ϕ_{CKE} is low. The output clock from the flip-flop 80 is supplied to a pulse width adjusting circuit 85 which is composed of a delay circuit 82 and a NAND gate 84. Although the delay circuit 82 illustrates only inverters for the purpose of simplicity, a circuit comprising inverter and capacitor or other delay circuits may be used. Thus, when the signal ϕ_{CKE} is low, the internal system clock ϕ_{CKE} as shown in FIG. 8 outputs from the CLK buffer. However, when the signal ϕ_{CKE} is high, the output of the flip-flop 80 becomes low thereby to stop the generation of the clock ϕ_{CLK}. In FIG. 6, inverter 89, p-channel MOS transistor 90 and n-channel MOS transistors 91 and 94 are elements for providing an initial condition to proper nodes in response to a power-on (or power-up) signal ϕ_{VCCH} from a known power-on circuit. The power-on signal ϕ_{VCCH} maintains a low level until the power supply voltage Vcc reaches a sufficient level after the application of the supply voltage.

Referring to FIG. 7, input buffer 70 converts the external clock enable signal CKE into a CMOS level signal. To prevent power consumption, operation of the input buffer 70 is inhibited by a self-refresh operation. The input buffer 70 provides an inverted CMOS level signal of the signal CKE on a line 90. The inverted CKE signal is coupled to a shift register 86 for shifting with an inverted clock CLKA of the clock CLK. The output of the shift register 86 is coupled to the output terminal of the signal ϕ_{CKE} via a flip-flop 88 of NOR type and an inverter. The output terminal of the shift register 86 is coupled to the output terminal of a signal CKEBPU via inverters.

The clock enable signal CKE is of inhibiting the generation of the system clock ϕ_{CLK} with a low level of CKE, thereby to freeze the internal operation of the chip. Referring again to FIG. 8, illustration is made on the signal CKE with a low level pulse for masking the CLK clock 98. By the low level of CKE, the input line 90 of the shift register 86 maintains a high level. After a CLKA clock 100 goes to a low level, the output of the shift register 86 goes to a high level. Thus, ϕ_{CKE} and CKEBPU become a high level and a low level, respectively. Then, after a next CLKA clock 102 goes to a low level, the output of the shift register 86 changes to a low level, thereby causing the signal CKEBPU to go high. At this time, since the output of the flip-flop 88 is keeping a low level, ϕ_{CKE} maintains a high level. However, after a next CLKA clock 104 goes to a high level, ϕ_{CKE} goes to a low level. Thus, as discussed with FIG. 6, ϕ_{CLK} clock corresponding to the clock 98 is masked with the high level of ϕ_{CKE}.

Since the internal operation of the synchronous DRAM operates in synchronism with the clock ϕ_{CLK}, the masking of ϕ_{CLK} causes the internal operation to be in a standby state. Thus, to prevent power consumption in the standby state, the signal CKEBPU is used to disable input buffers synchronous to ϕ_{CLK}. Accordingly, it should be appreciated that the signal CKE needs to be applied prior to at least one cycle of the masked clock CLK in order to mask it and has to hold a high level in order to carry out a normal operation.

2. $\overline{RAS}$ Buffer

The synchronous DRAM includes two memory banks 12 and 14 on the same chip to achieve a high speed data transfer rate. To achieve a high performance of the synchronous DRAM, control circuits need which is selectively controlling various operations for each bank. Accordingly, the $\overline{RAS}$ buffer is an input buffer combined with multifunctions according to a feature of the present invention.

FIG. 9 is a schematic circuit diagram showing the multifunction pulse $\overline{RAS}$ input buffer according to the present invention. Referring to FIG. 9, in the same manner as above discussed input buffers, input buffer 70 converts an external row address strobe signal $\overline{RAS}$ into an internal CMOS level signal. The input buffer 70 is disabled by a gate circuit 106 for gating system clock masking, self-refresh and power-on signals CKEBPU, ϕ_{VCCH} and ϕ_{SELF}. The CMOS level signal from the input buffer 70 is supplied to an input terminal 110 of a synchronization circuit 108 for providing to an output terminal 112 the $\overline{RAS}$ pulse ϕ_{RP} which synchronizes the CMOS level signal to the internal system clock ϕ_{CLK}. Thus, as shown in FIG. 10, at times t_1 and t_3, $\overline{RAS}$ being at low levels generates a $\overline{RAS}$ pulse ϕ_{RP} with high levels after a predetermined delay at the output terminal 112.

In FIG. 9, the remaining circuit excluding the input buffer 70, the synchronization circuit 109 and the gate circuit 106 is a multifunction control circuit 114 combined therewith to control the respective banks. Since n-channel transistors 148 and 150 are all turned on by ϕ_{VCCH} being at a low level during the power-on operation, the first $\overline{RAS}$ clock ϕ_{RC1} for the first bank 12 and the second $\overline{RAS}$ clock ϕ_{RC2} for the second bank 14 are all latched in initial conditions, i.e., low levels by means of latches 154 and 156.

To activate the first bank 12 and at the same time, to inactivate the second bank 14, at a time t_1 as shown in FIG. 10, external address signal ADD with address A_{11} being at a low level is supplied to the chip. Then, an address buffer, as will be discussed hereinbelow, generates an address signal SRA11 of a low level ($\overline{SRA11}$ of a high level) with the address signal ADD. On the other hand, at the time t_1, since both $\overline{CAS}$ and $\overline{WE}$ keep high levels, ϕ_C and ϕ_{WRC} hold low levels as will be discussed hereinbelow. Thus, NOR gates 116 and 126 output low levels and NAND gates 122 and 124 output high levels. Then, NAND gates 128 and 130 output a high level and a low level, respectively. When the pulse ϕ_{RP} goes to a high level, NAND gate 132 goes to a low level and NAND gates 134 to 138 go to high levels. Then, p-channel transistor 140 is turned on and p-channel transistor 144 and n-channel transistors 142 and 146 keep off states. Thus, latch 54 stores a low level. On the other hand, when ϕ_{RP} goes to a low level, all of NAND gates 132 to 138 go to high levels, thereby turning off transistors 140 to 146. As a result, the first $\overline{RAS}$ clock ϕ_{RC2} maintains a low level by means of the latch 156 which had been initially storing the high level. Thus, the first bank 12 is activated by the clock ϕ_{RC1}, thereby performing a normal operation such as a read or a write operation. However, the second bank 14 is not activated by the low level clock ϕ_{RC2}.

On the other hand, to access the synchronous DRAM at a high transfer rate, the second bank can be activated during the activation of the first bank. It can be accomplished by activating the second bank, applying the address A_{11} being at a high level after the activation of the first bank. Then, the address signal SRA11 becomes a high level ($\overline{SRA11}$ becomes a low level). In the same manner as discussed above, NAND gate 136 outputs a low level and all of NAND

gates 132, 134 and 138 output high levels. Thus, ϕ_{RC1} is maintaining the previous state, i.e., the high level and ϕ_{RC2} goes to a high level. As a result, all of the first and the second banks stay in activation states.

During the read or the write operation of the second banks, the first bank may also be precharged. When or before the precharge command is issued at time t_3 as shown in FIG. 10, external address signal A_{10} and A_{11}, which are all low levels, are applied to corresponding address pins of the chip. Then, address signals SRA10 and SRA11 become low levels ($\overline{SRA11}$ becomes a high level). After the command, ϕ_{RP} and ϕ_{WRC} go to high levels and ϕ_C is at a low level. Consequently, when ϕ_{RP} goes high, NAND gate 134 goes to a low level and all of NAND gates 132, 136 and 138 maintain high levels. Thus, the transistor 142 is turned on an transistors 140, 144 and 146 maintain off states. The latch 154 stores a high level and ϕ_{RC1} becomes a low level. However, ϕ_{RC2} maintains the previous state of the high level by means of the latch 156. As a result, ϕ_{RC1} of the low level causes the first bank to be precharged during performing data access from the second bank 14. Likewise, a precharge operation of the second bank may be accomplished by applying the precharge command, address signal A_{10} being at a low level and address signal A_{11} being at a high level.

On the other hand, a simultaneous precharge operation of both the first and the second bank 12 and 14 may be accomplished by applying the precharge command and an address A_{10} being at a high irrespective of a logic level of the address A_{11}. Then, in the same manner as discussed above, NAND gates 134 and 138 output low levels and NAND gates 132 and 136 output high levels. Thus, transistors 142 and 146 are turned on and transistors 140 and 144 maintain off states. As a result, latches 154 and 156 store precharge information being at high levels, respectively and both ϕ_{RC1} and ϕ_{RC2} become low levels.

A CBR refresh command is issued by $\overline{RAS}$ being at the low level and $\overline{CAS}$ being at the high level as shown in FIG. 5a. Thus, the high level signal ϕ_C and the low level signal ϕ_{WRC} input to the multifunction control circuit 114. In this case, NAND gate 124 and NOR gate 126 output low levels irrespective of logic levels of the address A_{10} and A_{11}. Consequently, NAND gates 132 and 136 output low levels and NAND gates 134 and 138 output high levels. Thus, transistors 140 and 144 are turned on and transistors 142 and 146 are turned off. Then, ϕ_{RC1} and ϕ_{RC2} become high levels and both banks thereby perform the CBR refresh operation. On the other hand, a selective CBR refresh operation for both banks can be accomplished by grounding one of two input terminals of NAND gate 124. Then, in the same manner as discussed above, ϕ_{RC1} and ϕ_{RC2} can be selectively enabled according to a logic state of the address A_{11}. That is, a low level address A_{11} under the CBR refresh command causes only the first bank to be refreshed.

3. Row Address Buffer

FIG. 12 is a diagram showing a schematic circuit diagram from the row address buffer 60 according to the present invention. In the drawing, an input buffer 70 converts input address signal AI (I=0, 1, 2, . . . , 11) to address signal of CMOS level in the same way as discussed in connection with above-mentioned input buffers. A logic circuit 158 for generating a control signal RABPU to enable or disable the input buffer 70 is also illustrated in FIG. 12. The control signal RABPU becomes a high level when both banks have activated or the system lock masking operation as enabled or the refresh operation has initiated, and the input buffer 70 is thereby disabled to prevent power consumption. Between the output terminal 161 of the input buffer 70 and a node 162 is connected a tristate inverter 160. The inverter 160 lies in an off state by the refresh signal O_{RFH} being at a low level during the refresh operation. In a normal operation such as a read or a write operation, the inverter 160 outputs a row address signal synchronized with the internal system clock ϕ_{CLK}. The row address signal is stored in a latch 164. A plurality of row address providing circuits, the number of which is determined by that of banks, are connected to a node 166. Since two banks is used in the embodiment of the present invention, it should be appreciated that two row address providing circuits 168 and 170 are connected in parallel to the node 166. The row address providing circuit 168 for the first bank 12 is comprised of a NOR gate 174, inverters 176 and 180, a transmission gate 172, a latch 178 and NAND gates 182 and 184. The row address providing circuit 170 for the second bank 14 has the same construction as the row address providing circuit 168. A refresh address providing circuit 198 is connected to the circuits 168 and 170 and serves to supply to the row address providing circuits 168 and 170 a count value RCNTI from a refresh counter (not shown) in the refresh operation.

It is assumed that the first bank 12 was in inactive state while the second bank 14 was in normal state such as a read or a write operation. In this case, a first bank row master clock ϕ_{R1} and a first bank row address reset signal ϕ_{RAR1} would be at low levels, and a second bank row master clock ϕ_{R2} and a second bank row address reset signal ϕ_{RAR2} would be at high levels. It is now further assumed that the first bank 12 is activated at a time t_1 as illustrated in FIG. 10. Then before the clock ϕ_{R1} goes to a high level, a row address from the external pin AI is stored in the latch 164 as previously described and the stored row address is then stored into the latch 178 via the transmission gate 172 turned on by low level signals of ϕ_{R1} and ϕ_{RAR1}. However, in this case, since the clock ϕ_{R2} continuously remains at the high level, the transmission gate 172' maintains the previous off state, thereby preventing from transferring the stored row address therethrough. When the clock ϕ_{R1} is then at the high level, the row address providing circuit 168 is isolated with the output of the latch 164 by means of the gate 172. When the first bank row address reset signal ϕ_{RAR1} then goes to a high level, NAND Gates 182 and 184 output the row address data stored in the latch 178 and its complementary data therein, respectively. Consequently, a row address RAI and its inverted row address $\overline{RAI}$ from the circuit 172 are fed to the row decoder in the first bank 12. It will be noted that, when ϕ_{R1} and ϕ_{R2} are both at high levels, the control signal RABPU becomes high by means of the logic circuit 158, thereby disabling the input buffer 70 in order to prevent the power consumption due to the active or normal operations of all banks.

On the other hand, in the refresh operation such as a CBR or a self refresh operation, the refresh signal O_{RHF} is at a low level and ϕ_{RFH} is at a high level. In case of 2-bank refresh operation, and ϕ_{R1} and ϕ_{R2} are also at high levels, as will be discussed in detail hereinbelow in connection with FIG. 19. Signals ϕ_{RAR1} and ϕ_{RAR2} are also at high levels. Thus, the input buffer 70 and tristate inverter 160 are both in off states and at the same time, transmission gates 172, 172' and 194 are in off states while transmission gates 188 and 188' are in on states. Thus, a count address signal RCNTI from a known address counter (not shown), which was stored into a latch 192 via the transmission gate 194 turned on by ϕ_{RFH} being at a low level prior to the refresh operation, are fed to the row decoder corresponding to each bank via transmission gates 188 and 188', latches 178 and 178' and NAND gates 182, 184, 182' and 184'. After that time, operations of selecting word lines of each row decoder and then refreshing memory cells thereon are of the same manners as conventional DRAMs.

Addresses SRA10 and SRA11 for use in the multifunction $\overline{RAS}$ buffer may use row addresses RA10 and RA11 from the row address buffer 60. However, since the addresses RA10 and RA11 are generated with some time delays, separated row address buffers which may operate in faster speed may be provided on the same chip for independently generating the addresses SRA10 and SRA11.

4. Operation Mode Set Circuit

The synchronous DRAM of the present invention is designed so that system designers choose desired ones of various operation modes in order to amplify the Convenience of use and enlarge the range of applications.

FIG. 13 is a block diagram for the operation mode set circuit 58. A mode set control signal generator 200 generates a mode set signal ϕ_{MRS} in response to signals ϕ_C, ϕ_{RP} and ϕ_{WRC} generated upon the issuance of the operation mode set command. An address code register 202, in response to the power-on signal ϕ_{VCCH} from the power-on circuit 203 and the mode set signal ϕ_{MRS}, stores address codes MDST0 to MDST6 depending on addresses from the row address buffer and produces the codes MDST0 to MDST2 and MDST4 to MDST6 and a column addressing mode signal ϕ_{INTEL}. A burst length logic circuit 204 produces a burst length signal SZn generated with logic combination of the codes MDST0 to MDST2. Wherein n represents a burst length indicated as the number of system clock cycles. A latency logic circuit 206 produces a $\overline{CAS}$ latency signal CLj generated with logic combinations of the codes MDST4 to MDST6. Wherein J represents a $\overline{CAS}$ latency (or $\overline{CAS}$ latency value) indicated as the number of system clock cycles.

FIG. 14 is a diagram showing a schematic circuit diagram for the mode set control signal generator 200 and FIG. 20 is a timing diagram associated with the operation mode set or program.

In the present embodiment, programming the operation modes is accomplished by applying the operation mode set command and at the same time, addresses A_0 to A_7 to address input pins according to the following Table 1.

TABLE 1

$\overline{CAS}$ latency j				Column Addressing Way		Burst Length			n
A6	A5	A4	j	A3	Way	A2	A1	A0	n
0	0	1	1			0	0	1	2
0	1	0	2	0	Binary	0	1	0	4
0	1	1	3			0	1	1	8
1	0	0	4	1	Interleave	1	1	1	512

The $\overline{CAS}$ latency j related with a maximum system clock frequency is represented as the following Table 2.

TABLE 2

Maximum System Clock Frequency (MHz)	$\overline{CAS}$ Latency j
33	1
66	2
100	3

It will be noted that values of $\overline{CAS}$ latency J in the above Tables represent the number of system clock cycles and $\overline{CAS}$ latency values related to maximum clock frequencies may be changed according to the operation speed of a synchronous DRAM.

For example, if a system designer want to design a memory system with a binary column addressing way and a continuous 8-word data access at 100 MHZ, the minimum selection value of the $\overline{CAS}$ latency j is 3. If the $\overline{CAS}$ latency value of 3 has been chosen, addresses A_0 to A_7 for setting the operation modes is 1, 1, 0, 0, 1, 1, 0 and 0, respectively. It has been already discussed that selecting one of both banks was address A_{11}. Remaining addresses thereof are irrelevant to logic levels.

After the selection of operation modes suitable for a data transfer system and then the determination of addresses for setting the operation modes, mode set programming of the synchronous DRAM is performed, applying the mode set command and the predetermined addresses to corresponding pins of the chip. Referring to FIG. 20, the mode set command and the addresses ADD is applied thereto at a time t_1. Then, ϕ_{RP} from the $\overline{RAS}$ buffer and signals ϕ_C and ϕ_{WRC} from a $\overline{CAS}$ buffer and a $\overline{WE}$ buffer as will be discussed later go to high levels. In the mode set control signal generator 200 as shown in FIG. 14, the signals ϕ_C, ϕ_{RP} and ϕ_{WRC} which are all high render a signal ϕ_{WCBR} to go low. When the row address reset signal ϕ_{RAR} is then at a high level, the row address buffer of NAND gate 208 are all at high levels, thereby causing the mode set signal ϕ_{MRS} to go high.

FIG. 15 is a diagram showing a schematic circuit diagram for the address code register 202. The address code register 202 comprises first register units for storing second logic levels (low levels) upon the power-on and address signals RA_0, RA_2 to RA_4 and RA_6 in the mode set operation after the power-up in response to the node set signal ϕ_{MRS}, and second register units for storing first logic levels (high levels) upon the power-on and address signals RA_1 and RA_5 in the mode set operation after the power-up in response to the mode set signal ϕ_{MRS}. Each of the first register units is comprised of a tristate inverter 210 including p-channel MOS transistors 212 and 214 and n-channel MOS transistors 216 and 218, a latch 222 connected to an output terminal of the inverter 210 and p-channel MOS transistor 220 whose channel is connected between the power supply voltage Vcc and the output terminal and whose gate is coupled to the power-on signal ϕ_{VCCH}. Since the power-on signal ϕ_{VCCH} is low until the supply voltage Vcc reaches minimum voltages to carry on internal normal operation after the application thereof, i.e., on the power-on, each first register unit makes corresponding address code MDSTI or addressing mode signal ϕ_{INTEL} set at a low level on power-on by the conduction of p-channel MOS transistor 220. Each second register unit comprises a tristate inverter 210' including p-channel MOS transistors 212' and 214' and n-channel MOS transistors 216' and 218', an n-channel MOS transistor 219 whose channel is connected between an output terminal of the inverter 210' and the reference potential (ground potential) and whose gate is coupled to an inverted signal of ϕ_{VCCH}, and a latch 222' connected to the output terminal of the inverter 210'. Each second register unit makes the address code MDST1 or MDST5 latched high upon the power-on. However, in the mode set operation after the power-up, i.e., after the supply potential Vcc reaches at least the minimum operating voltages, since ϕ_{VCCH} is high, inverters 210 and 210' are turned on in response to the high level signal ϕ_{MRS} and latches 222 and 222' then store row addresses RAI from the row address buffer 60, thereby outputting address codes MDSTI having the same address values as the row addresses RAI. Thus, if the mode set program is performed, each address code of MDSTI is the same value as the corresponding address: MDST3 corresponding to the address signal RA_3 is the signal ϕ_{INTEL} which represents column addressing way. If A_3=0 (low level), the signal ϕ_{INTEL} becomes low and a column address counter as discussed hereinbelow counts in a binary increasing manner. If A_3=1 (high level), the signal ϕ_{INTEL} becomes high representing an interleave mode.

FIG. 16 is a diagram showing a schematic circuit diagram for the latency logic circuit 206 which selects to send to a high level only one of latency signals CL1 to CL4 with the logic combination of address codes MDST4 to MDST6 associated with the $\overline{CAS}$ latency. Upon the power-on, since MDST5 is high and MDST4 and MDST6 are low, only CL2 becomes high.

FIG. 17 is a diagram showing a schematic circuit diagram for the burst length logic circuit 204 for selecting one of signals $\overline{SZ2}$ to $\overline{SZ512}$, each of which represents a burst length, with the logic combination of address codes MDST0 to MDST2 associated with the burst length. For example, if address codes MDST0 to MDST2 are all at high levels, only the signal $\overline{SZ512}$ of $\overline{SZ2}$ to $\overline{SZ512}$ is high and signals SZ4 to $\overline{SZ512}$ are all high. Thus, as will be discussed hereinbelow, continuous 512-word (full page) outputs via data output buffer in response to the signals. Upon the power-on, since MDST1 is high and MDST0 and MDST2 are low, only the signals SZ4 and $\overline{SZ4}$ are high.

Consequently, selected operation modes are determined by the storage of corresponding addresses to latches 222 and 222' when the mode set signal ϕ_{MRS} is at the high level. After the address codes have been stored to corresponding latches 222 and 222' an auto-charge operation is performed according to one characteristic feature of the present invention. By performing a high speed precharge without any separate precharge commands, precharging time is reduced and next operation such as the active operation is also performed immediately without a standby state.

FIG. 18 is a circuit diagram showing an auto-precharge control signal generator 223 for performing the auto-precharge upon the exit of self refresh or in the mode set program. The self refresh signal ϕ_{SELF} is at a high level in the self refresh operation and at a low level in remaining time excluding the self refresh operation. Thus, the output of NAND gate 224 is at a high level in the mode set program. When ϕ_{RALi} reaches to a high level as seen in FIG. 20, the output of NOR gate 232 goes to a high level. At this time, ϕ_{CLK} is at a low level. When ϕ_{CLK} then goes to a high level, the output of NAND gate 226 goes from a low level to a high level after a time delay determined by a delay circuit 230. Consequently, the auto-precharge control signal generator 223 produces an auto-precharge signal O_{AP} having a short low pulse after O_{MRS} have gone high. Likewise, upon completion of the self refresh operation, O_{SELF} goes from high to low and the circuit 223 then generates the auto-precharge signal O_{AP} having the short low pulse. Returning to FIG. 9, the signal O_{AP} inputs to a NAND gate 152. Thus, the NAND gate 152 produces a short high pulse with the short low pulse O_{AP}, thereby turning on n-channel transistors 148 and 150. The latches 154 and 156 then store high levels, thereby causing ϕ_{SC1} and ϕ_{RC2} to go to low levels. Once either ϕ_{RC1} or ϕ_{RC2} goes to low levels, ϕ_{Ri} and ϕ_{RALi} goes to low levels in sequence and then the precharge operation is performed.

On the other hand, if the synchronous DRAM of the present invention is used without the mode set programming, i.e., in a default mode, p-channel transistors 220 and n-channel transistors 219 as shown in FIG. 15 are all turned on by the power-on signal ϕ_{VCCH} which is low upon the power-on. Thus, latches 222 store low levels and latches 222' store high levels. Address codes MDST0, MDST2, MDST4 and MDST6 and ϕ_{INTEL} then become low levels and the codes MDST1 and MDST5 also become high levels. Consequently, in the default mode, $\overline{CAS}$ latency of 2, binary address mode and burst length of 4 are selected automatically.

5. Column Control Signal Generator

FIG. 19 is a diagram showing a schematic circuit diagram for a row master clock generator 62 for generating the row master clock ϕ_{Ri} in response to the $\overline{RAS}$ clock ϕ_{RCi} from the $\overline{RAS}$ buffer 56. As shown in FIG. 10, if the i-th bank is activated, ϕ_{RCi} goes to a high level and the i-th bank row master clock ϕ_{Ri} then goes to a high level via NOR gate 234 and inverters. However, if ϕ_{RCi} goes to a low level to precharge, ϕ_{Ri} goes to a low level after a different time delay according to each $\overline{CAS}$ latency. That is, when the value of the CAS latency J is 1, i.e., CL1=high and CL2=CL3=low, ϕ_{Ri} goes to the low level after a time delay passing delay circuits 236, 238 and 240 mainly. When the value the $\overline{CAS}$ latency j was set to 2, ϕ_{Ri} goes to the low level after a time delay passing delay circuits 238 and 240 mainly. When the value of the $\overline{CAS}$ latency j was programmed to 3, ϕ_{Ri} goes to the low level after a time delay passing the delay circuit 240 mainly. Thus, the higher the frequency of system clock CLK, the shorter the time delay causing ϕ_{Ri} to go low. Such time delays allow column selection signals to have a sufficient time margin before the beginning of precharge cycle in a write operation, thus correctly writing data into cells and also ensuring that continuous 2-bit data outputs via output pin after precharge command in a read operation. In the present embodiment, the time delay in case of j=1 is about 19 ns and the time delays in case of j=2 and j=3 are respectively about 6 ns and 3 ns.

The row control clock generator 62 as shown in FIG. 3 is a conventional logic circuit for generating clocks showing in the timing diagram of FIG. 10. The row address reset signal ϕ_{RALi} rises to a high level after the rising edge of ϕ_{Ri} and falls to a low level after the falling edge of ϕ_X. The word line driving signal ϕ_X rises to a high level after the rising edge of ϕ_{RALi} and falls to a low level after the falling edge of ϕ_{Ri}. The signal ϕ_S generated by the signal ϕ_X activates sense amplifiers selected with the block information signal BLS which is produced by decoding row addresses. Signal ϕ_{RALi} for enabling the column decoder goes to a high level after the rising edge of ϕ_{RALi} and goes to a low level after the falling edge of ϕ_{RCi}. Signal ϕ_{RCDi} for guaranteeing t_{RCD} goes to a high level after the rising edge of ϕ_S and goes to a low level after the falling edge of ϕ_{Ri}.

FIG. 21 is a schematic circuit diagram showing a logic circuit for generating signals ϕ_{YEi} and ϕ_{YECi} which enable $\overline{CAS}$ chain circuits. The signal ϕ_{YECi} is a delayed signal of ϕ_{RCDi}. Column enable signal ϕ_{YEi} is a signal having a timing as shown in FIG. 10 by gating of ϕ_{RCDi} and ϕ_{Ri}.

FIG. 11 is a schematic circuit diagram showing the high frequency clock generator according to the present invention which serves to multiply the frequency of the internal system clock upon the occurrence of precharge command where a low frequency external system clock such as an external system clock CLK of 33 MHZ or less in the present embodiment is used. The high frequency clock generator 68 comprises a circuit means 242 for generating a pulse depending on the precharge command, a gate 248 for logically summing the generated pulse with the internal system clock ϕ_{CLK} to generate a multiplied system clock and a transmission gate 252 for transferring the multiplied system clock in response to a predetermined latency.

Referring to FIG. 22 showing a timing diagram for read and precharge operations at a system clock CLK of 33 MHZ and a burst length of SZ4, precharge command for read-out bank is issued at time t_4. ϕ_{RCi} then goes from a high level to a low level and the output terminal A of the pulse generator 242 thereby outputs the pulse having a pulse width depending on a given time delay of a delay circuit 244 or 244'. This

pulse is summed with the internal system clock ϕ_{CLK} by means of gates 246 to 248, thereby resulting in outputting a multiplied system clock via NAND gate 248. NOR gate 254 outputs a high level since CL1 is high and ϕ_{EWDC} is high only in a write operation. Thus, the output of the gate 248 outputs via turned-on transmission gate 252. At this time, a transmission gate 250 is off. Thus, since internal circuits operate with an internal system clock CNTCLK9 having the multiplied operation frequency after the precharge command, data output can be accomplished at a high speed and the precharge operation can be completed within a shorter time period after the precharge command. When the system clock CLK is above 33 MHZ, CL1 is at a low level. Thus, NOR gate 254 outputs a low level and the transmission gate 252 is off. Thus, the transmission gate 250 is turned off and CNTCLK9 is equal to the clock ϕ_{CLK}.

DATA PATHS

Data paths mean paths for outputting the developed data on bit lines via data output buffers in a read operation and feeding data being inputting via data input buffer to bit lines in a write operation. FIG. 23 shows circuit blocks associated with the data paths. For purposes of simplicity, it will be noted that the drawing shows circuit blocks on data paths associated with two sub-arrays.

Referring to FIG. 23, an I/O line selection and precharge circuit 38 is connected to the first I/O bus 26R associated with one of sub-arrays in one of memory cell arrays 20TL, 20BL, 20TR and 20BR and to the second I/O bus 26L associated with another sub-array therein as discussed along with FIG. 1. The circuit 38 receives the block information signal BLS for designating a sub-array including a word line selected by the row decoder 18 and in response to this information signal, serves to couple an I/O bus associated with the sub-array to PIO bus 256. Also, in a reading operation, since data presents on two pairs of four pairs of I/O lines in a selected I/O bus, the circuit 38 precharges remaining two pairs of the four pairs and PIO line pairs corresponding thereto.

FIGS. 24 is a diagram showing a schematic circuit diagram for the I/O precharge and selection circuit 38. When the block information signal BLS from the row decoder 18 is at a low level, transfer switches 258 and 258' are all in off states and precharge circuits 260 are all turned on, thereby precharging I/O line pairs I/O_0, $\overline{I/O_0}$ to I/O_3 $\overline{I/O_3}$ to VBL (=½ Vcc). When the block information signal BLS is at a high level to transfer data, the switches 258 and 258' are in on states while the precharge circuits 260 are in off states. Now assume that I/O line pairs being to transfer data is the second I/O line pairs I/O_2, $\overline{I/O_2}$ and I/O_3, $\overline{I/O_3}$. Then, an I/O line precharge signal IOPRI goes to a low level and its complement signal $\overline{\text{IOPRI}}$ goes to a high level. Thus, precharge circuits 262 and equalizing circuits 264 are turned on and the I/O line pairs I/O_0, $\overline{I/O_0}$, and I/O_1, $\overline{I/O_1}$ are then subsequently precharged and equalized to one threshold voltage below the supply voltage (Vcc-V_t). Wherein V_t is a threshold voltage of n-channel MOS transistor. However, since the precharge circuits 262' and equalizing circuits 264' associated with the I/O line pairs transferring data are all in off states, the data thereon is transferred to corresponding second PIO line pairs PIO_2, $\overline{PIO_2}$ and PIO_3, $\overline{PIO_3}$ via transfer switches 258' in the reading operation. In the same manner, data on PIO line pairs can transferred to corresponding I/O line pairs in write operations.

Returning to FIG. 23, an I/O sense amplifier 266 is activated to amplify data On the PIO bus 256 with a control signal ϕ_{IOSE} which is generated in response to the block information signal in a read operation. The I/O sense amplifier 266 is a know circuit which may be further including a latch for storing data at its output terminal.

The output of the I/O sense amplifier 266 is coupled to the data output multiplexer via the data bus DBI. It will be noted that the data bus DBI is one of data buses DB0 to DB7, as shown in FIG. 1. Data line pairs DIO_0, $\overline{DIO_0}$ to DIO_3, $\overline{DIO_3}$ constituting the data bus DBI are correspondingly connected to PIO line pairs PIO_0, $\overline{PIO_0}$ to PIO_3, $\overline{PIO_3}$ constituting the PIO bus 256 via the sense amplifier 266.

FIG. 25 is a diagram showing a schematic circuit diagram for the data output multiplexer 268 which are comprised of precharge circuits 263a and 263d, latches 270, tristate buffers 272, first latches 274a to 274d, isolation switches 276, second latches 278a to 278d and data transfer switches 280, all of which are connected in series between the respective data line pairs and a common data line pair CDL and $\overline{\text{CDL}}$. In the same manner as previously discussed about precharging of I/O line pairs I/O_0, $\overline{I/O_0}$ to I/O_3, $\overline{I/O_3}$, the precharge circuits 263a to 263d respond to a DIO line precharge signal DIOPRI and its complement $\overline{\text{DIOPRI}}$ in a read operation, thereby causing two data line pairs transferring data to be prevented from precharging and the remaining data line pairs to be precharged. Latches 270 are respectively connected to the data lines DIO_3, $\overline{DIO_0}$ to DIO_3, $\overline{DIO_3}$ for storing data thereon. Tristate buffers 272 are respectively connected between the data lines DIO_0, $\overline{DIO_0}$ to DIO_3, $\overline{DIO_3}$ and first latches 274a to 274d for outputting inverted data thereon. However, tristate buffers connected with data lines being precharged are turned off. First latches 274a–274d are respectively connected to output terminals of the tristate buffers 272 for storing data transferred via the data lines and the tristate buffers. Each of second latches 278a to 278d is connected in series with corresponding first latch via corresponding isolation switch. The second latches 278a–278d are connected to a pair of common data lines $\overline{\text{CDL}}$ and CDL via corresponding data transfer switches 280. The data transfer switches 280 are sequentially turned on in response to data transfer signals RDTP0 to RDTP3 which are high level pulses generated in sequence by column address signals, thereby sequentially outputting data stored in the second latches to the common data lines $\overline{\text{CDL}}$ and CDL via the first latches. Thus, as will be discussed in more detail hereinafter, data stored in serial registers 274 and 278 which are comprised of the first and the second latches 274a to 274d and 278a to 278d outputs in sequence on the common data lines $\overline{\text{CDL}}$ and CDL in response to the data transfer signals RDTP0 to RDTP3. In precharge operations of the data line pairs DIO_3, $\overline{DIO_0}$ to DIO_3, $\overline{DIO_0}$, since the tristate buffers 272 are held in off states, there is no destruction of data stored in the first and second registers 274 and 278. However, where data stored in the second register 278 waits a long time before transmission via transfer switches 280, i.e., in case of a long latency, if new data is transferred from data line pairs, the previous data stored in the second register 278 will be destroyed. Also, in case of use of a low frequency system clock, since the data transfer signals RDTP0 to RDTP3 are generated in synchronism with the system clock, such destruction of data may be occurred. Such data destruction due to data contention may substantially occur in a $\overline{\text{CAS}}$ interrupt read operation, i.e., such operation that before the completion of burst operation during a sequential data read operation based on the established burst length, an interrupt request is issued and a next sequential data read operation of the burst length is then carried out with no break or no wait, depending on

the column address signals. Thus, to prevent an erred operation due to such data collection, the isolation switches 276 are connected between the first and the second latches. A control signal ϕ_{CL} for controlling the isolation switches is a high level pulse signal upon the $\overline{CAS}$ interrupt request in case of long $\overline{CAS}$ latency values of 3 and 4. The data lines $\overline{CDL}$ and CDL are connected to a known data output latch 282.

Returning to FIG. 23, the data output buffer 284 is connected with data output lines DO and $\overline{DO}$ from the data output multiplexer 268, serving to feed to an input/output pad (not shown) a sequential data synchronous to the system clock which is defined in dependence upon a burst length in a read operation. There is a circuit diagram for the data output buffer 284 in FIG. 26. In the drawing, transfer switches 286 and 286' respectively transfer data on the lines DO and $\overline{DO}$ to lines 288 and 290 in synchronism with a system clock ϕ_{CLK} of a given frequency (a frequency above 33 MHZ in the present embodiment), but in a synchronism with a system clock ϕ_{CLK} of the given frequency or below the given frequency. As will be explained hereinafter, a control signal ϕ_{YEP} is held high at a system clock of 33 MHZ or below 33 MHZ, i.e., at a $\overline{CAS}$ latency value of 1 and held low at a system clock of a frequency above 33 MH. Latches 92 are respectively connected to the lines 288 and 290 for storing data thereinto. A gate circuit 310 comprised of NAND gates 294 to 298 and transistors 300 and 302 is connected between the lines 288 and 290 and driving transistors 304 and 306. The source of a p-channel MOS transistor 300 is coupled to a boosted Voltage Vpp from a known boost circuit for driving the transistor 304 without loss of its threshold. The gate circuit 310 serves to inhibit the output of data on the data input/out line 308 in response to a control signal ϕ_{TRST} which goes to a low level upon either completion of a burst read operation or occurrence of a data output masking operation.

Returning again to FIG. 23, the data input buffer 312 is connected between a data line DI and the line 308 for converting external input data on the line 308 into CMOS level data and producing internal input data synchronous with the system clock ϕ_{CLK}. The data input buffer 312 may be comprised of previously mentioned input buffer for being enabled by a signal ϕ_{EWDC} which is at a high level in a write operation, and converting an external input data into a CMOS level data; and previously mentioned synchronization circuit for receiving the converted input data from the input buffer and then producing an internal input data synchronous with the system clock ϕ_{CLK}. Thus, whenever the clock ϕ_{CLK} goes to a high level in a write operation, the data input buffer 312 may be a buffer circuit for sequentially sampling a serially inputting data and then outputting a resulting serial data on the data line DI.

A data input demultiplexer 314 serves to sample the serial data on the output line DI of the data input buffer 312 with write data transfer signals being sequentially generated in synchronism with the system clock, thereby grouping into parallel data of predetermined bits (2-bit parallel data in the present embodiment) and supplying the grouping parallel data to corresponding data line pairs.

FIG. 27 is a diagram showing a schematic circuit diagram for the data input demultiplexer 314. The demultiplexer 314 comprises selection switches 316a to 316d connected to the data line DI for sampling to transform the serial data on the data line DI into the parallel data in response to write data transfer signals WDTP0 to WDTP3. Each of latches 320a to 320d are connected to the corresponding selection switch for storing the sampled data. The outputs of the latches 320a to 320d are respectively connected to the data lines DIO_0, $\overline{DIO_0}$ to DIO_3, $\overline{DIO_3}$ via switches 322a to 322d, each of which is a NAND gate enabled in a write operation, and buffers 324a to 324d. The signal ϕ_{WR} gating NAND gates 322a to 322d is a signal being at a high level in a write operation. Each of the buffers 324a and 324d is a tristate inverter which is composed of a p-channel and an n-channel transistors 326 and 328. P-channel transistors 318a to 318d respectively connected between the selection switches 316a and 316d and the latches 320a and 320d allow to, in response to the control signal WCA1 and its complement $\overline{WCA1}$, transfer a 2-bit parallel data, alternating two groups of first data line pairs DIO_0, $\overline{DIO_0}$ and DIO_1, $\overline{DIO_1}$ and DIO_3, $\overline{DIO_3}$, and at the same time, precharge in such a manner as precharging one group thereof while the other group thereof is transferring the parallel data. That is, when the control signal WCA1 is at a high level in a write operation, transistors 318c and 318d are in off states. Thus, data stored in latches 320c and 320d in response to the signals WDTP2 and WDTP3 is transferred to the second data line pairs DIO_2, $\overline{DIO_2}$ and DIO_3, $\overline{DIO_3}$ via switches 322c and 322d and buffers 324c and 324d. At this time, since $\overline{WCA1}$ is low, transistors 318a and 318b are in on states, and buffers 324a and 324b are thereby in off states. Thus, the first data line pairs DIO_0, $\overline{DIO_0}$ and DIO_1, $\overline{DIO_1}$ are precharged to the supply potential Vcc by precharge circuits 263a and 263b shown in FIG. 25. When WCA1 then goes to a low level, the transistors 318c and 318d goes to on states and the tristate buffers 324c and 324d then become off. Thus, likewise, the second data line pairs are precharged and the first data line pairs transfer a 2-bit parallel data.

Returning to FIG. 23, data transferred via the bidirectional data bus DBI from the data input demultiplexer 314 is transferred to PIO line pairs 256 via the PIO line driver 330.

FIG. 28 is a drawing showing a schematic circuit diagram for the PIO line driver 330 which comprises switches 332 responsive to a bank selection signal DTCPi and the block selection signal BLS for passing data on the data line pairs DIO_0, $\overline{DIO_0}$ to DIO_3, $\overline{DIO_3}$, buffers 334 connected between the switches 332 and the PIO line pairs PIO_0, $\overline{PIO_0}$ to PIO_3, $\overline{PIO_0}$ for amplifying data inputting via the switches 332 to supply to corresponding PIO line pairs, and precharge and equalizing circuits 336 each connected between two lines constructing each PIO line pair for precharging and equalizing the PIO line. It should be noted that the buffers 334 and the precharge and equalizing circuits 336 are the same constructions as the buffers 324a to 324d in FIG. 27 and the precharge and equalizing circuits 260, 262, 262', 264 and 264' in FIG. 24, and their operations are also associated with each other in a write operation. The PIO line driver 330 isolates between the data bus DBI and the PIO line pairs 256 with the signal DTCPi being at a low level in a read operation. However, in a write operation, data on the PIO line pairs 256, which is transferred from the data bus DBI by means of the driver 330, is transferred to corresponding I/O line pairs selected by the I/O precharge and selection circuit 38. Since the data transmission is alternately accomplished every two pairs, if first I/O line pairs I/O_0, $\overline{I/O_0}$ and I/O_1, $\overline{I/O_1}$ of the left side I/O bus 26R, which are correspondingly connected with the first PIO line pairs PIO_0, $\overline{PIO_0}$ and PIO_1, $\overline{PIO_1}$, are transferring data thereon, second PIO line pairs PI_2, $\overline{PIO_2}$ and PIO_3, $\overline{PIO_3}$ and second I/O line pairs I/O_2, $\overline{I/O_2}$ and I/O_3, $\overline{I/O_3}$ of the left I/O bus 26R will be precharging.

COLUMN CONTROL CIRCUIT

Column control circuit is a circuit for generating control signals to control circuits related to the data paths.

FIG. 4 is a schematic block diagram showing the column control circuit according to the present invention. In the drawing, a $\overline{CAS}$ buffer 338 receives the external column address strobe signal $\overline{CAS}$ and the internal system clock ϕ_{CLK} and then generates pulse signals ϕ_C, ϕ_{CA}, BITSET and ϕ_{CP}.

A $\overline{WE}$ buffer 340 receives the external write enable signal $\overline{WE}$, the system clock ϕ_{CLK}, the pulse signals ϕ_C and ϕ_{CA} from the $\overline{CAS}$ buffer 338 and various control signals for generating write control signals ϕ_{WR}, ϕ_{EWDC} and ϕ_{WRC} in a write operation.

A DQM buffer 342 receives external signal DQM and the internal system clock ϕ_{CLK}, and then generates a data input/output masking signal O_{DQM} to inhibit the input and the output of data.

A column address buffer 344 receives external column addresses A_0 to A_9 in synchronism with the system clock ϕ_{CLK}, thereby latching the column addresses in response to the pulse signal ϕ_{CA} from the $\overline{CAS}$ buffer 338, and then producing column address signals ECA0 to ECA9.

A column address generator 346 is a counter circuit which is composed of a predetermined number of stages or bits (nine bits in the present embodiment). The counter may carry out counting operation either in a sequential or binary address mode or in an interleave address mode according to the column addressing mode signal ϕ_{INTEL}. Stages of the counter latch the column address signals from the column address buffer 344 in response to the pulse BITSET, and lower stages thereof associated with the burst length signal SZn perform the counting operation with the clock CNTCLK9, starting from the column address signals latched therein, and then produce successive column address signals according to a selected address mode. However, remaining stages produce initial column address signals latched therein. A column address, reset signal ϕ_{CAR} is a signal for resetting the counter at the end of the burst length, i.e., after completion of a valid data output.

A burst length counter 350 is a conventional 9-stage (or 9-bit) binary counter counting pulses of the clock ϕ_{CLK} after being reset by the pulse signal BITSET from the $\overline{CAS}$ buffer. The counter 350 may also be reset by the column address reset signal ϕ_{CAR}. Since the BITSET signal is a pulse generated upon activation of $\overline{CAS}$, the counter 350 is re-count the number of pulses of the clock ϕ_{CLK} after the activation of $\overline{CAS}$. However, the signal ϕ_{CAR} is a signal stopping the counting operation of the counter 350. Thus, in a $\overline{CAS}$ interrupt operation, the activation of $\overline{CAS}$ during the output of valid data renders the counting operation of the counter to restart.

A burst length detector 352 receives the counting value from the counter 350 and the burst length signal $\overline{SZn}$ from previously mentioned mode set circuit 58, and then generates a signal COSR indicating of the end of the burst.

A column address reset signal generator 354 serves to generate the signal ϕ_{CAR} resetting the column address generator 346 in response to the burst end signal COSR.

A data transfer control counter 348 is a counter which receives address signals CA0, CA1, FCA0 and FCA1 and then generates column address signals RCA0 and RCA1 synchronous to the system clock ϕ_{CLK}. The clock CNTCLK9 is a clock artificially generated to shorten the precharge time when the system clock CLK of 33 MHZ or less is employed as previously discussed. Thus, in this case, the column address signals CA0 and CA1 is not signals synchronized with the system clock ϕ_{CLK}. Thus, the counter 348 exists in consideration of the reduction of the precharge time at the system clock of 33 MHZ or less. If unnecessary, the column address generator 346 receives ϕ_{CLK} in place of CNTCLK9, and a read and a write data transfer clock generators 356 and 358 may receive the column address signals CA0 and CA1 instead of the outputs of the counter 348, i.e., RCA0 and RCA1.

The read data transfer clock generator 356 receives the column address signals RCA0 and RCA1 synchronized with the system clock ϕ_{CLK} and then generates read data transfer pulses RDTPm to output a serial data from the data output multiplexer 268 in a read operation.

The write data transfer clock generator 358 receives the signals RCA0 and RCA1 and then generates write data transfer pulses WDTPm to output a time multiplexed parallel data from the data input demultiplexer 314 in a write operation.

The write data transfer clock generator 358 receives the signals RCA0 and RCA1 and then generates write data transfer pulses WDTPm to output a time multiplexed parallel data from the data input demultiplexer 314 in a write operation.

1. $\overline{CAS}$, $\overline{WE}$ and DQM Buffers

FIG. 29 is a drawing showing a schematic circuit diagram for the $\overline{CAS}$ buffer 338, and FIG. 33 is a drawing showing a timing diagram of a write operation employing system clock of 66 MHZ, burst length of 4 and $\overline{CAS}$ latency of 2.

In FIG. 29, an input buffer 70 is a circuit which is disabled in refresh and clock masking operations and converts input signals into internal CMOS level signals in read and write operations. A synchronization circuit 108 is connected to the input buffer 70 to synchronize the CMOS level $\overline{CAS}$ signal from the input buffer with the system clock ϕ_{CLK}. A pulse generator 360 is connected to the synchronization circuit 108 to generated control pulses ϕ_{CA}, ϕ_{CP} and BITSET. Referring to FIG. 33, the pulses ϕ_C, ϕ_{CA}, ϕ_{CP} and BITSET are generated by the $\overline{CAS}$ pulse being at a low level at time t_3. The high level pulse width of ϕ_C is about one cycle of the system clock CLK, and the pulse width of ϕ_{CA} is about one half cycle of the clock CLK while the pulse widths of ϕ_{CP} and BITSET are about 5 to 6 nsec.

FIG. 30 is a drawing showing a schematic circuit diagram for the $\overline{WE}$ buffer 340. In the drawing, an input buffer 70 is a circuit for converting the external write enable signal $\overline{WE}$ into and internal CMOS level signal. A synchronization circuit 108 stores the level shift signal from the input buffer 70 into a latch 362 in synchronism with the system clock ϕ_{CLK}. The input of a latch 366 is coupled to the output of the latch 362 via a transfer switch 364 turned on by the activation of $\overline{CAS}$ for storing a high level thereinto in a write operation. A gate circuit 368 comprised of gates is connected to the output of the latch 366. A shift register 370 is connected to the gate circuit 368 for delaying one cycle of CLK after a write command. A pulse generator 378 generates a short high level pulse ϕ_{WRP} in a precharge cycle for resetting the shift register 370 and the latch 366. Referring to FIG. 33, when ϕ_{CA} is at a high level after issuance of a write command at time t_3, the latch 366 stores a high level. Since ϕ_C and at least one of ϕ_{RCD1} and ϕ_{RCD2} are also at high levels at that time as discussed hereinabove, a NAND gate 372 outputs a low level, thereby forcing a control signal ϕ_{EWDC} to go high. The low level output of the NAND gate 372 inputs to the shift register 370, thereby outputting low level therefrom after a delay of one cycle of ϕ_{CLK}. Then, a NAND gate 374 outputs a high level, thereby causing the control signal ϕ_{WR} to go high. Generating the control signal ϕ_{WR} after a delay of one cycle of CLK is to accept an external input data at a next cycle of CLK after a write

command. Thus, to accept an external input data at a write command cycle, it will be obvious to those skilled in the art that the shift register 370 may be omitted therefrom.

FIG. 31 is a drawing showing a schematic circuit diagram for the DQM buffer 342, and FIG. 32 is a drawing showing an operation timing diagram for the DQM buffer. Referring to FIG. 31, an input buffer 70 is a buffer for converting an external signal DQM into a CMOS level signal. A shift register 382 is connected to the input buffer 70 for generating a data output masking signal O_{DQM} in synchronism with the system clock ϕ_{CLK}. Referring to FIG. 32, a data output masking command is issued at time t_1. At this time, a latch 384 stores a low level. When ϕ_{CLK} 387 is then at a high level, a latch 385 stores a high level. When ϕ_{CLK} 387 is then at a low level, a latch 386 stores a high level. When ϕ_{CLK} 388 is then at a high level, the signal ϕ_{DQM} goes to a low level. Likewise, the signal ϕ_{DQM} goes to a high level when ϕ_{CLK} 389 is at a high level. Thus, inhibiting data output from the data output buffer with O_{DQM} signal being at the low level is accomplished by responding to the rising edge of the second clock of ϕ_{CLK} after the issuance of the data output masking command. It will be obvious to those skilled in the art that the time adjustment of inhibiting data output therefrom may be accomplished by changing the number of shift stages.

2. Column Address Generator

The column address generator comprised of a column address buffer 214 and a column address counter 346.

FIG. 34 is a drawing showing a schematic circuit diagram for the column address buffer 344. The synchronous DRAM of the present embodiment uses ten column address buffers which receive external column addresses A_0 to A_9, respectively. In the drawing, an input buffer 70 is a buffer for converting the external column address signal A_i into a CMOS level address signal. The input buffer 70 is enabled by the signal ϕ_{RAL} and its output is coupled to a latch 392 via a transfer switch 390. Before ϕ_{CA} goes to a high level, the latch 392 stores an input column address signal ECAI and then produces a column address signal FCAI via inverters. Only signals FCA0 and FCA1 are fed to the data transfer control counter 348. When ϕ_{CA} is at the high level due to the activation of $\overline{CAS}$, a transfer switch 394 is turned on, thereby storing complement of the column address signal ECAI into a latch 398. The output of the latch 398 is coupled to switch means comprised of NAND gates 400 and 402 which is enabled by ϕ_{CAR}. The enabled NAND gates 400' and 402 provide column address signal CAI and its complement $\overline{CAI}$, respectively. The column address signals CAI are fed and loaded to the column address counter 346, thereby generating successive column address signals PCAI therefrom with counting operation starting from the loaded column address signal. The signals PCAI output as column address signals CAI and $\overline{CAI}$ via transfer switches 396, latches 398 and switches 400 and 402. Thus, transfer switches 394 and 396, latch 398 and switch 400 and 402 constitute means for providing a starting column address with ϕ_{CA} pulse generated by the activation of $\overline{CAS}$, and providing successive column address signals being counted from the starting column address when the pulse ϕ_{CA} is at a low level. Thus, after the activation of $\overline{CAS}$ the successive column addresses, i.e., serial steam of the external input column address and the internally generated column addresses can be generated at a high speed. It should be noted that in the present embodiment, column address buffers associated with column address signals CA0 and CA9 do not receive signals PCA0 and PCA9. The signals CA9 has no relationship with the column decoder because of using as a bank selection signal in case of executing a $\overline{CAS}$ interrupt operation. Signals CA0 and CA1 are also signals for generating read data transfer clocks RDTPm and write data transfer clocks WDTPm which are respectively used in the data output multiplexer 268 and the data output demultiplexer 314. Signals CA1 to CA8 are utilized for column decoding.

FIG. 35 is a drawing showing a schematic block diagram for the column address counter 346, and FIG. 36 is a drawing showing a schematic circuit diagram for each stage in the column address counter. Referring to the drawings, the column address counter 346 is a 9-bit counter comprised of nine stages ST1 to ST9, and comprises a first counter portion including lower stages ST1 to ST3 and AND gates 404 and a second counter portion including upper stages ST4 to ST9 and AND gates 406. The first counter portion may carry out counting operation in one of binary and interleave modes, and the second counter portion may perform counting operation in the binary mode. In the first counter portion, i.e., 3-bit counter, selection of either the binary or the interleave mode is enforced by the logic level of the address mode signal ϕ_{INTEL}. In the least significant stage ST1, an input terminal of a carry input signal CARI and a burst length input terminal SZ are connected to the supply potential Vcc. Carry output signal CARO of the first stage ST1 inputs to a carry input signal CARI of the second stage ST2, and AND gate 404 corresponding to the second stage ST2 ANDs the carry outputs of the first and second stages ST1 and ST2. AND gate 404 corresponding to the third stage ST3 ANDs a carry output of the third stage ST3 and the output of the AND gate corresponding to the second stage ST2 which is connected to a carry input of the third stage ST3. The output of the AND gate associated with the most significant stage ST3 of the first counter portion is connected to a carry input signal CARI of the least significant stage ST4 of the second counter portion. A carry input signal CARI of each stage in the second counter portion is coupled to the output of the AND gate of the previous stage. Each AND gate 406 of the second counter portion inputs the output of the AND gate of previous stage and the output of the corresponding stage.

The column address counter 346 of the present invention may selectively perform one of both the binary and the interleave modes as an address sequence in order to enhance a design flexibility for memory system designers. The binary addressing mode is a mode representative of generating successive addresses increasing by one from a given starting address, and the interleave addressing mode is a mode representative of generating successive addresses in a specific way. The following Table 3 represents the address sequence representative of the decimal number in case of the burst length of 8.

TABLE 3

Address Sequence (Burst Length n = 8)	
Binary Mode	Interleave Mode
0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
1,2,3,4,5,6,7,0	1,0,2,3,5,4,7,6
2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
7,0,1,2,3,4,5,6	7,6,5,4,3,2,1

FIG. 36a is a drawing showing a schematic circuit diagram for each stage of the first counter portion. Referring to the drawing, each stage of the first counter portion includes

a carry portion 408 for generating a carry and a bit portion 410 for providing a bit output. The carry portion 408 comprises two latches 412 and 416, a transfer switch 414 connected between the latches 412 and 416, an inverter 418 and a transfer switch 411 connected in series between an output terminal of the latch 416 and an input terminal of the latch 412. Likewise, the bit portion 410 also comprises latches 412' and 416', transfer switches 411' and 414' are connected to a line 419 and a line 415 via an inverter 413. Input terminals of latches 412 and 412' are connected to lines 422 and 424, respectively. An initialization circuit 420 is connected between the lines 422 and 424 for providing an initial condition, i.e., a low level upon power-on to the latches 412 and 412'. The line 419 is connected to an output terminal of a NOR gate 426, three input terminals of which are respectively coupled to the clock CNTCLK9, the output of a NAND gate 428 and the signal BITSET. The NAND gate 428 receives the burst length signal SZn, a signal ϕ_{CARC} and the carry signal CARI which is the previous carry output signal CARO. Transfer switches 430 and 432 are turned on in response to the signal BITSET and thereby transfers an initial carry value and an initial column address value (or an initial bit value) on lines 422 and 424, respectively. The mode control signal ϕ_{INTEL} is at a high level in the interleave mode and at a low level in the binary mode, as discussed hereinabove. Thus, the transfer switches 430 and 432 turned on in the interleave mode respectively transfer a low level and the initial bit value CAI, and the switches 430 and 432 both transfer the initial bit value CAI in the binary mode.

FIG. 37 is an operation timing diagram for the circuit diagram of FIG. 36a. Referring to FIGS. 36a and 37, when any one of input signals SZn, ϕ_{CARC} and CARI of NAND gate 428 is at a low level, NOR gate 426 inhibits the output of the clock CNTCLK9, maintaining a low level on the line 419. Thus, transfer switches 414 and 414' are in on states while transfer switches 411 and 411' are in off states. At this time, once transfer gates 430 and 432 are turned on with the pulse signal BITSET at a high level, the carry output signal CARO and the bit output signal PCAI are respectively an initial carry value of a low level and an initial bit value in an interleave mode while the carry output signal CARO and the bit output signal PCAI are both initial bit values CAI in a binary mode. Then the low level signal BITSET turns off the transfer switches 430 and 432 and thereby causes the previously preset initial carry and bit values to be maintain thereon. Thus, the signal BITSET is a signal for respectively presetting initial carry and bit values into the carry portion 408 and the bit portion 410 according to the mode control signal ϕ_{INTEL}.

On the other hand, after the establishment of the initial values with the preset signal BITSET, when the signals SZn, ϕ_{CARC} and CARI are all at high levels, the NOR gate 426 outputs the clock CNTCLK9. Then, the carry portion 408 and the bit portion 410 respectively output binary sequential count values starting from the preset initial values every cycles of the clock CNTCLK9. During such a sequential operation, if a low level carry signal CARI inputs to the NAND gate 428, the line 419 becomes a low level, thereby freezing operations of the carry portion 408 and the bit portion 410. That is, since transfer switches 411 and 411' are turned off, CARO and PCAI are respectively frozen to inverted ones of binary values stored in latches 412 and 412'. When the signal CARI then goes to a high level, sequential operations are re-started beginning from the frozen values.

FIG. 36b is a diagram showing a schematic circuit diagram for each stage constituting the second counter portion of FIG. 35. Constructions of this stage are identical to those excluding the carry portion 408 and the mode control circuit 434 in the stage of FIG. 36a. Its operation is also identical to that of the bit portion 410 of FIG. 36a. Thus, detailed explanation for each of the stages ST4 to ST9 will be omitted.

Returning to FIG. 35, it is assumed that the burst length of n has been set by the operation mode program. Then, since burst length signals associated with burst length of n or less are all at high levels, only stages receiving high level burst length signals SZn are enabled. For example, if the burst length n is 512 (full pages), the column address counter operates as a 9-bit counter. If burst length of n=32 is programmed, five lower stages ST1 to ST5 perform sequential counting operations, and output signals PCA5 to PCA8 of upper stages ST6 to ST9 respectively maintain initial input bit values, i.e., input column address signals CA5 to CA8. Thus, the first counter portion comprised of three lower stages ST1 to ST3 outputs sequential binary or interleave address signals PCA0 to PCA2 according to the mode control signal ϕ_{INTEL}, and the counter comprised of stages ST4 and ST5 outputs sequential binary address signals PCA3 and PCA4 starting from input column addresses CA3 and CA4, receiving carries from the first counter portion.

3. Column Decoder

As discussed hereinabove, the column address buffers 344 output column address signals CA1 to CA8 inputting to the column decoder for selecting columns.

FIG. 38 is a drawing showing a schematic block diagram for the column decoder according to the present invention. In the drawing, predecoders 436 to 442 receive column address signals CA1 and CA2, CA3 and CA4, CA5 and CA6 and CA7 and CA8, respectively and also receive a row address signals RA11 or a column address signal CA9. The column address signal RA11 is used as a bank selection signals in case of performing either an interleave operation Of the first and second banks or an independent operation between both banks such as performing read or write operation and precharge operation of the second bank after performing read or write operation and precharge operation of the first bank. If RA11 is low, the first bank is selected, while if RA11 is high, the second bank is selected. On the other hand, CA9 is a bank selection signal in case of performing a $\overline{CAS}$ interrupt operation. The first bank is selected when CA9 is low, while the second bank is selected when CA9 is high.

The first predecoder 436 decodes column address signals CA1 and CA2, thereby generating predecode signals DCA $\overline{1}\,\overline{2}$ to DCA12 and also generating a signal DCA2 and its complement DCA$\overline{2}$ which are faster than the signals DCA $\overline{1}\,\overline{2}$ to DCA12. Neighboring signals of the predecode signals overlaps a predetermined portion of each end. The output signals of the first predecoder 436 are fed to main decoders 444. NOR gates 446 respectively input combinations of signals choosing one of predecode signals DCA$\overline{3}\,\overline{4}$ to DCA34 from the predecoder 440 and one of predecode signals DCA$\overline{7}\,\overline{8}$ to DCA78 from the predecoder 442, and their outputs are respectively coupled to the main decoder 444 so as to produce column selection signals CSL0 to CSL255.

FIG. 39a is a drawing showing a schematic circuit diagram for the first predecoder 436. In the drawing, NAND gates 448 are enabled by the bank selection signal RA11 or CA9, decode column address signals CA1 and CA2 and their complements $\overline{CA1}$ and $\overline{CA2}$. After activation of $\overline{CAS}$, a short low level pulse ϕ_{CP} resets NAND gates 451 and 454, thereby causing the output signals DCA$\overline{1}\,\overline{2}$ to

DCA12 to become low. When ϕCPis then at a high level (at this time, ϕ_{YE1} is high), the NAND gates **451** and **454** are enabled. It is now assumed that CA1 and CA2 have been at low levels. Then, NAND gate **448***a* outputs a low level, and NAND gate **456***a* then outputs a high level. Thus, DC$\overline{1}$ $\overline{2}$ goes from the low level to a high level, while DCA$\overline{1}$ 2, DCA1$\overline{2}$ and DCA12 remain the low levels. When CA1 then goes to a high level and CA2 maintains the low level, this results in causing DCA1$\overline{2}$ to go high. However, the NAND gate **448***a* outputs a high level, thereby causing DCA$\overline{1}$ $\overline{2}$ to go low after delays via delay circuits **450***a* and **452***a*, NAND gates **451***a*, **456***a* and **454***a* and an inverter. Thus, DCA$\overline{1}$ $\overline{2}$ goes to the low level with the time delay determined by the delay elements after going to the high level. Consequently, overlapped portions occur end portions between successive predecoding signals. These overlapped portions guarantee an error free write time during a write operation.

FIG. **39***b* is a drawing showing a schematic circuit diagram for one of second predecoders **438** to **442**. It should be noted that each second predecoder is a low enable circuit in which a selected predecode signal goes to a low level.

FIG. **40** is a drawing showing a schematic circuit diagram for first one of main decoders **444**. Referring to the drawing, predecode signal DCA$\overline{1}$ $\overline{2}$ to DCA12 are respectively coupled to input terminals of inverters **458***a* to **458***d* which are partitioned into a first inverter group of inverters **458***a* and **458***b* and a second inverter group of inverters **458***c* and **458***d*. One terminal of each of inverters **458***a* and **458***b* constituting the first group is connected in common with a drain of a first transistor **462**, while one terminal of each of inverters **458***c* and **458***d* constituting the second group is connected in common with a drain of a second transistor **464**. The other terminal of each of the inverters **458***a* to **458***d* is connected to the supply potential Vcc. Output terminals of the inverters are respectively connected to latches **406***a* to **460***d*. Sources of first and second transistors **462** and **464** are connected in common with a drain of a third or pull-down transistor **466** whose source is connected to a reference potential Vss such as a ground potential and whose gate is connected with the output of NOR gate **446** inputting predecode signals DCA$\overline{3}$ $\overline{4}$, DCA$\overline{5}$ $\overline{6}$ and DCA$\overline{7}$ $\overline{8}$ from the second predecoders **438** to **442**. Gates of the first and the second transistors **462** and **464** respectively received DCA $\overline{2}$ and DCA2. The input signals are generated in order of predecode signals DCA2 and DCA$\overline{2}$, predecode signals DCA$\overline{3}$ $\overline{4}$, DCA$\overline{5}$ $\overline{6}$ and DCA$\overline{7}$ $\overline{8}$ and overlapped predecode signals DCA$\overline{1}$ $\overline{2}$ to DCA12. Thus, after the transistor **462** or **464** and the pull-down transistor **466** have been turned on, the inverters **458***a* to **458***d* can be turned on. It is now assumed that column address signals CA1 to CA8 have been low. Then, the transistor **462** is turned on and the transistor **466** is then turned on. The inverter **458***a* is then turned on by the high-going signals DCA$\overline{1}$ $\overline{2}$ and thereby the column selection signal CSL0 goes to a high level. Where the column address signal CA1 then changes into a high level, DCA$\overline{1}$ $\overline{2}$ goes to a high level, thereby causing the column selection signal CSL1 to go high. However, the column selection signal CSL**0** becomes from the high level to a low level after a predetermined delay, as discussed above, due to the low-going signal DCA$\overline{1}$ $\overline{2}$. In the same manner as discussed above, column selection signals overlapping predetermined ones of end portions in response to column address signals CA1 to CA8 being sequentially changed. Referring to FIG. **33***b*, where initial external column addresses A_0 and A_1 to A_8 are respectively at a high level and low levels, illustration is made on a timing diagram showing timing relations between column address signals CA to CA8, signals DCA$\overline{1}$ $\overline{2}$ and DCA1$\overline{2}$ and column selection signals CSL**0** and CSL1. It can be understood in the drawing that time periods for selecting columns are sufficiently guaranteed by overlapped portions.

FIG. **41** is a timing diagram showing a read operation at the system clock frequency of 100 MHZ, the burst length of 4 and the $\overline{CAS}$ latency of 3. It can be understood in the drawing that sufficient read-out time periods can be guaranteed by overlapped portions of signals DCA$\overline{1}$ $\overline{2}$, DCA1 $\overline{2}$ and CSL1 where A_0 and A_1 to A_8 are initially at a high level and low levels, respectively.

4. Data Bus Control Circuit

It is very important that Unnecessary internal operations are precluded to eliminate power consumption after completion of the burst length, i.e., after output or input of valid data. Such a control circuit comprises the burst length counter **350**, the burst length detector **352** and the column address reset signal generator **354** as shown in FIG. **4**.

The burst length counter **350** stops its counting operation when the column address reset signal ϕ_{CAR} is at a low level. The counter **350** is reset by a short high level pulse BITSET, thereby re-starting its counting operation. Thus, the burst length counter **350** is a conventional 9-bit binary counter whose clock input terminal is connected to the system clock ϕ_{CLK} and whose reset terminal is connected to the output of a OR gate inputting the signal BITSET and complement of ϕ_{CAR}. Count values CNTI (I=0, 1, . . . 8) of the counter **350** input to the counter **350** input to the burst length detector **362**.

FIGS. **42** and **43** show a schematic circuit diagram for the burst length detector. The burst length detector **352** includes a logic circuit receiving the count values CNTI and burst length signals SZn for generating a signal COSI informing of the completion of burst length after activation of $\overline{CAS}$. For example, referring to FIG. **41**, once the pulse BITSET goes from the high level to the low level after the activation of $\overline{CAS}$, the counter **350** counts clocks of ϕ_{CLK}, thereby producing count signals CNT**0** and CNT1. Since SZ4=1 (high) in case of the burst length of 4, the burst length detector **352** produces the signals COSI having a pulse width of one cycle of ϕ_{CLK} when CNT**0** and CNT1 are all at high levels. On the other hand, the pulse ϕ_C being at the high level after the activation of $\overline{CAS}$ renders to be latched low the output of a flip-flop comprised of NOR gates **468** and **470** as shown in FIG. **43**, thereby causing the signal COSR to go low as shown in FIG. **41***b*. Once COSI then goes to a high level, two inputs of a NAND gate **474** become high after delay of a shift register **472** with the system clock ϕ_{CLK}. Thus, the output of the NOR gate **468** goes low. At this time, since ϕ_C is low, the output of the NOR gate **470** goes to a high level, thereby causing COSR to go to a high level. Thus, it can be understood in FIG. **4***b* that the low level signal COSR is a signal indicating of the burst length, i.e., four pulses of the system clock CLK after the activation of $\overline{CAS}$. A delay circuit **476** for providing time delays depending on $\overline{CAS}$ latency values receives the signal COSR and then outputs a signal COSDQ. Thus, it can be seen that the signal COSDQ is a signal indicating of a burst length considering a $\overline{CAS}$ latency. Referring to FIG. **41***b*, since the $\overline{CAS}$ latency is 3 (CL3 is a high level), a transfer switch **478** is turned on, thereby producing the signal COSDQ that the signal COSR is delayed by two cycles of the clock ϕ_{CLK}. It has been already discussed that the signal COSDQ being at a high level disables the data output buffer.

FIG. **44** is a drawing showing a schematic circuit diagram for the column address generator **354**. Referring to FIG. **41** or FIG. **33**, the signal ϕ_{RALi} had become high prior to the activation or $\overline{CAS}$. Then, after the activation of $\overline{CAS}$, NAND

gates 482 and 484 output high levels in response to the high-going pulse ϕ_C. Thus, a NAND gate 480 constituting a flip-flop is latched to a low level, thereby allowing ϕ_{CAR} to go high. Likewise, a NAND gate 486 outputs a low level in response to the signal COSR going to a low level when ϕ_C is high since one of ϕ_{YEC1} and ϕ_{YEC2} maintains a high level at this time. Thus, ϕ_{CARC} goes to a high level. Then once COSR goes to a high level, ϕ_{CAR} and ϕ_{CARC} goes to low levels. However, in case of using a system clock of a lower frequency such as 66 MHZ or less, signals ϕ_{RAN} and ϕ_{YE1} or ϕ_{YE2} rather than the signal COSR go first to low levels, thereby causing the signal ϕ_{CAR} to go low. Thus, the burst length counter 350 and the column address counter 346 are reset by the low-going signal ϕ_{CAR}, thereby preventing unnecessary operations thereof.

5. Data Transfer Clock Generator

A data transfer Clock generator is a circuit for generating clock for transferring data via the data output multiplexer and the input data demultiplexer. The data transfer clock generator includes the data transfer control counter 348 and the read and write data transfer clock generators 356 and 358.

The column address generator 346 is using the multiplied system clock CNTCLK9 as synchronization clock to assure a faster precharge time in case of using a system clock of 33 MHZ or less, as previously discussed. In such a case, since data must be transferred in synchronism with the system clock CLK, the data transfer control counter 348 is essentially required. However, if such a technique is unnecessary, i.e., if such lower frequency system clock is not used, some modifications are required. Such modifications can be accomplished by the following explanation. That is, the column address counter 346 as shown in FIG. 35 uses the system clock ϕ_{CLK} in place of the clock CNTCLK9 as a synchronous count clock. Selection circuits 391 as shown in FIG. 34 respectively receive the lower 2-bit outputs PCA0 and PCA1 to produce column address signals CA0 and CA1. The read and write data transfer clock generators 356 and 358 directly input the signals CA0 and CA1 instead of outputs RCA0 and RCA1 from the data transfer control counter 348.

FIG. 45 is a drawing showing a schematic block diagram for the data transfer control counter 348 which comprises a 2-bit counter 488 and 490 and selection circuits 492 and 494. The 2-bit counter receives column address signals CA0 and CA1 from the column address buffers 344 for generating internal sequential column address signals starting from the signals CA0 and CA1 in synchronism with the system clock ϕ_{CLK}. The selection circuits 492 and 494 serve to generate serial column address stream with column address signals FCA0 and FCA1 from the column address buffers 344 and the internal sequential column address signals from the 2-bit counter. Stages 488 and 490 constituting the 2-bit counter are respectively identical in constructions to stages shown in FIGS. 36*a* and 36*b*. The difference therebetween is to use the system clock ϕ_{CLK} instead of the clock CNTCLK9. Each of the selection circuits 494 and 492 has the same construction as the selection circuit 391 of FIG. 34. The input signals ECAI of the transfer switch 394 and the input signal PCAI are respectively replaced by FCAI and the output of the corresponding 2-bit counter (wherein I is 0 or 1). The signal COSR is also fed to third inputs of NAND gates 400 and 402. Using the signal COSR in the selection circuits 492 and 494 is preventing unnecessary internal operation thereof upon completion of burst length. Operation explanation for the 2-bit counter and the selection circuits is referred to portions as discussed in connection with FIGS. 36*a*, 36*b* and 34. The outputs RCA0 and RCA1 of the data transfer control counter 348 and their complements $\overline{RCA0}$ and $\overline{RCA1}$ may be properly time delayed signals according to $\overline{CAS}$ latency values or the system clock in order to control a data transfer timing on data lines.

FIG. 46 is a drawing showing a schematic circuit diagram for the read data transfer clock generator 356 for generating read data transfer signal RDTP0 to RDTP3 which are used in the data output multiplexer. Referring to the drawing, the generator 356 comprises NAND gates 498 for decoding column address signals RCA0 and RCA1 and their complements $\overline{RCA0}$ and $\overline{RCA1}$, delay circuits 500 for receiving the decoded signals and producing read data transfer signals with different time delays according to $\overline{CAS}$ latency values, and NAND gates 496 for outputting the read data transfer signals in a read operation and resetting their outputs to low levels in a write operation. The outputs of NAND gates 496 become high in response to the signal ϕ_{EWDC} being at a high level in a write operation. Each of NAND gates 498 serves as a decoder outputting low in response to two inputs of high levels. Each delay circuit 500 includes a shift register 503 having a plurality of data paths and switches 497, 501 and 502 respectively connected to the data paths, and serves to provide a different time delay via a selected switch according to $\overline{CAS}$ latency signals CL3 and CL4. Referring to. FIG. 51*b*, where initial external column addresses A_0 and A_1 are respectively at a high level (=1) and a low level (=0), illustration is made on a timing diagram for column address signals RCA0 and RCA1 for controlling data transfer and read data transfer signal RDTP0 to RDTP3. Since the $\overline{CAS}$ latency value is 3, switches 502 are turned on.

FIG. 47 shows a schematic circuit diagram of a circuit for generating the signal ϕ_{CL} being used in the data output multiplexer 268. Referring to the drawing, after the activation of $\overline{CAS}$, the high-going pulse ϕ_C renders high the output of a flip-flop 504 via a delay circuit 505. On the other hand, if one of $\overline{CAS}$ latency signals CL3 and CL4 is high, the output of a NAND gate 506 maintains high. Thus, the signal ϕ_{CL} goes high. Then if ϕ_C goes low, the signal ϕ_{CL} will go low after a delay of about one cycle of ϕ_{CLK} in case of a high level signal CL3, while the signals ϕ_{CL} will go low after a delay of about 2 cycles of ϕ_{CLK} in case of a high level signal CL4. However, if CL3 and CL4 are all low, i.e., where $\overline{CAS}$ latency is either 1 or 2, ϕ_{CL} is always lOW since the output of NAND gate 506 is low.

FIG. 49 shows a timing diagram of $\overline{CAS}$ interrupt read operation after activation of $\overline{RAS}$. The operation is performed at the $\overline{CAS}$ latency of 3 and the burst length of 4 with system clock of 66 MHZ. At time t_1, a read command is issued with external column addresses $A_0, A_1, A_2, \ldots,$ A8=1, 0, 0, . . . , 0. At time t_3, a $\overline{CAS}$ interrupt read command is issued with external column addresses $A_0, A_1, A_2, \ldots,$ A8=0, 1, 0, . . . , 0. Then, at t_3 and t_4, i.e., just before and after the issuance of the $\overline{CAS}$ interrupt read command, column address signals RCA0 and RCA1 are identical as a low level and a high level. Thus, read-out data is transferred in series via the same data line pairs DIO_2, $\overline{DIO_2}$ at times t_3 and t_4. It may be seen in FIG. 49C that read-out data was high just before the $\overline{CAS}$ interrupt, while read-out data was low immediately after the $\overline{CAS}$ interrupt. Then, as shown in the timing diagram of DIO_2 between t_3 and t_5 in FIG. 49C, serial data, i.e., 1,0 is transferred on the data line DIO_2. Thus, as shown in FIG. 25, if means 276 for isolating between serial registers 274 and 278 are not provided therebetween, the serial data is sequentially latched into the serial registers 274 and 278, and transferred only in series to the data output buffer via transfer switch 280 which is turned

on by the read data transfer signals RDTP2. However, since the operation speed of semiconductor circuit varies according to ambient conditions such as ambient temperature, it is essentially necessary to provide means for preventing serial data contention due to variations of the operation speed of the transfer switch 280 or data output buffer. The signal ϕ_{CL} is used as a signal for isolating between serial registers 274 and 278 to prevent such a data contention. It is to be understood that the data contention between two serial data may be prevented by the high level pulse ϕ_{CL} indicating as P in FIG. 49C.

FIG. 48 shows a schematic circuit diagram of the write data transfer generator write data transfer signals WDTP0 to WDTP3 for use in the data input demultiplexer 314. The generator 358 comprises NAND gates for decoding column address signals RCA0 and RCA1 and their complements $\overline{RCA0}$ and $\overline{RCA1}$, a synchronization circuit 510 for synchronizing the decoding signals from the NAND gates with the system clock ϕ_{CLK} and producing synchronized write data transfer signals, and NAND gates 512 for gating the synchronized write data transfer signals. A line 514 stays at a low level to reset all of the gates 512 during a read operation, a $\overline{CAS}$ interrupt or a data input/output masking operation, thereby causing the signals WDTP10 to WDTP3 to go low. Reference numeral 516 represents a delay circuit. As shown in FIG. 33, by a high level address signal RCA0 and a low level address signal RCA1, a high level pulse signal WDTP1 is generated and next sequential address signals RCA0 and RCA1, which are respectively a low level and a high level, generates a high level pulse signal WDTP2.

6. Data Line Precharge Circuit

Data line precharge circuit is a circuit for generating control signals to precharge I/O lines, PIO lines and DIO lines. According to the present invention, data transfer and precharging between lines on data paths are sequentially performed in turn. To perform such a precharge operation, column address signal CA1 produced from external column address A_1 is utilized.

FIG. 50 shows a schematic circuit diagram of a circuit for generating control signals to precharge I/O lines and PIO lines. RA11 and CA9 are bank selection signals as discussed above, and I/O lines and PIO lines are initialized to precharge states. Thus, PIOPR1 and IOPR1 and their complements $\overline{PIOPR1}$ and $\overline{IOPR1}$ are at high levels. After activation of $\overline{CAS}$, once ϕ_{CP} goes from a low level to a high level (ϕ_{YE1} maintains a high level), NAND gates 518 are then enabled. If CAI is at a low level ($\overline{CAI}$ at a high level), precharge signals PIOPR1 and IOPR1 maintain high levels while $\overline{PIOPR1}$ and $\overline{IOPR1}$ go to low levels. Thus, in FIG. 24, if BLS is high, I/O line pairs I/O_2, $\overline{I/O_2}$ and I/O_3, $\overline{I/O_3}$ are continuously precharged. However, I/O_0, $\overline{I/O_0}$ and I/O_2, $\overline{I/O_2}$ cease precharging to be ready for data transfer. PIO line pairs PIO_2, $\overline{PIO_2}$ and PIO_3, $\overline{PIO_3}$, as shown in FIG. 28, are also precharged in the same, manner. Then, if CAI goes to a high level, lines I/O_0, $\overline{I/O_0}$, I/O_1, $\overline{I/O_1}$, PIO_0, $\overline{PIO_0}$, PIO_1 and $\overline{PIO_1}$ are conversely precharged. On the other hand, a short low level pulse ϕ_{CP} generated after activation of $\overline{CAS}$ in a $\overline{CAS}$ interrupt operation renders all of precharge signals PIOPR1, $\overline{PIOPR1}$ and $\overline{IOPR1}$ to become high level pulses. Thus, prior to receipt of column addresses upon $\overline{CAS}$ interrupt, all of I/O line pairs and PIO line pairs are precharged. By such a $\overline{CAS}$ precharge, internal operations may be performed at a high speed with no wait. Reference numeral 520 represents a delay circuit.

FIG. 51 shows a schematic circuit diagram of a circuit for generating control signals to precharge DIO lines. In the same manner as discussed above, once ϕ_{CP} goes to a low level, DIO line precharge signal DIOPR1 and its complement $\overline{DIOPR1}$ go high, and signal WCA1 and its complement $\overline{WCA1}$ go low, thereby precharging all of DIO lines. That is, this is in case of a $\overline{CAS}$ interrupt operation. If ϕ_{CP} goes to a high level and CA1 is at a low level ($\overline{CA1}$ is at a high level), signals DIOPR1 and WCA1 respectively maintain the high level and the low level while $\overline{DIOPR1}$ and $\overline{WCA1}$ respectively go to a low level and a high level. Thus, during a read or a write operation, precharge circuits 263c and 263d of FIG. 25 maintains on states while the circuits 263a and 263b thereof are turned off. Then, line pairs DIO_2, $\overline{DIO_2}$ and DIO_3, $\overline{DIO_3}$ keep precharging while DIO_0, $\overline{DIO_0}$ and DIO_1, $\overline{DIO_1}$ are ready for data transfer. In case of the write operation, transistors 318c and 318d of FIG. 27 maintain on states and transistors 318a and 318b thereof are turned off, thereby causing buffers 324c and 324d to keep off states and buffers 324a and 324b to transfer data depending on data states stored in latches 320. Then if CA1 goes to a high level, operations contrary to above mentioned ones are performed.

FIG. 52 is a schematic circuit diagram of a circuit for generating bank selection signals for use in the PIO driver 330 shown in FIG. 28. Once a write command is issued, ϕ_{WR} and ϕ_{CP} then go to high levels. At this time, when RA11 or CA9 is at a low level, DTCP1 is latched to a high level and thereby the first bank is selected. Where precharge command is issued to the first bank, ϕ_{YE1} goes to a low level and thereby the first bank selection signal DTCP1 then goes to a low level. On the other hand, where a write command is issued to the second bank during the write operation for the first bank, a flip-flop 522' is latched to a low level and thereby a second bank selection signal DTCP2 then goes to a high level. Each of DTCP1 and DTCP2 is connected to PIO driver 330 associated with corresponding bank. Referring to FIG. 28, when bank selection signal DTCPi and block information signals BLS are all at high levels, switches 332 are enabled, thereby allowing data on corresponding DIO lines to be transferred.

7. Data Output Buffer Control Circuit

Data output buffer control circuit is a circuit for controlling data outputs from the data output buffer 284 shown in FIG. 26. It is required that the data output buffer outputs data at eery predetermined rising edges of the system clock CLK in a read operation. Since the synchronous DRAM must output data information only within a given time period set by the $\overline{CAS}$ latency and the burst length, it is to be preferred that data output therefrom is precluded outside the given time period in order to as well increase the performance of the chip as prevent power consumption. Also, since one cycle time of the system clock of a predetermined frequency (33 MHZ in this embodiment) or less is long, it is meaningless to output data in synchronism with the system clock CLK.

FIG. 53 is a schematic circuit diagram of a control circuit for generating a control signals to inhibit data output of the data output buffer 284. NAND gate 524 outputs a low level in a write operation. A clock signal ϕ_{CF} stays a high level for one clock cycle of ϕ_{CLK} going to the high level at the first rising edge of ϕ_{CLK} after activation of $\overline{CAS}$. Likewise, ϕ_{WRCF} stays a high level for one clock cycle of ϕ_{CLK} after the activation of $\overline{WE}$. Where $\overline{CAS}$ and $\overline{WE}$ are all activated, the NAND gate 524 generates the low level, thereby allowing a signals $\overline{TRST}$ to go low. Also, when data output masking is requested by the external signal DQM, the DQM buffer 342 shown in FIG. 31 generates the low level clock signal ϕ_{DQMP} as shown in FIG. 32. Thus, the NAND gate 526 generates a high level pulse. This results in generating a row level pulse ϕ_{TRST}. Likewise, the signal ϕ_{TRST} also becomes

low with the signals COSDQ being at a high level after the delay depending on $\overline{CAS}$ latency j following the completion of the burst length. Thus, the output of the data output buffer shown in FIG. 26 becomes a high impedance in response to the low level signal ϕ_{TRST}. Consequently, the data output buffer 284 inhibits data output at the rising edge of next system clock CLK after the issuance of the data output masking signal DQM. Also, upon the completion of the burst data output, the output of the buffer 284 becomes the high impedance.

Where external system clock of 33 MHZ or less is used, a control signal ϕ_{YEP} may be coupled to the $\overline{CAS}$ latency signal CL1 so as to output data irrespective of the internal system clock ϕ_{CLK}. Since the $\overline{CAS}$ latency signal CL1 keeps a high level at such a system clock, the signal ϕ_{YEP} is at a high level. Thus, in the data output buffer 284 of FIG. 26, transfer switches 286 and 286' are always turned on and thereby not under the control of the system clock ϕ_{CLK}. However, when system clock of a frequency above 33 MHZ is used, the signal CL1 is at a low level and the signal ϕ_{YEP} is also at a low level. Thus, the transfer switches 286 and 286' are turned on and off under the control of the system clock ϕ_{CLK}.

OPERATION

Explanation will be now made on operation and using way of the present synchronous DRAM.

Referring to FIG. 41, illustration is made on a timing chart showing a read operation at the burst length of 4 and the $\overline{CAS}$ latency of 3, using an external system clock of 100 MHZ. At time t_1, activation command is issued. External addresses input along with the activation of $\overline{RAS}$. Then $\overline{RAS}$ buffer 56 produces the signal ϕ_{RP} and then generates the bank selection $\overline{RAS}$ signal ϕ_{RCi} defining one of the first and second banks 12 and 14 with the external address A_{11}. The row master clock generator 62 of FIG. 19 generates the row master clock ϕ_{Ri} in receipt of the signal ϕ_{RCi}. The row address buffer 60 responds the row master clock ϕ_{Ri} to generate row address signals which are fed to the row decoder 18 of selected bank. In response to the row address signals, the row decoder 18 generates a block information signal BLS representative of a selected sub-array in each of the first to the fourth memory cell arrays and a signal selecting a word line in the selected sub-array. Sensing operation, which drives word lines selected by the word line selection signals and then develops data on corresponding bit lines, is performed by conventional techniques. After the completion of $\overline{RAS}$ chain, the row control clock generator 64 generates the signal ϕ_{RCDi} guaranteeing the $\overline{RAS}$-$\overline{CAS}$ delay time t_{RCD}. At time t_2, read command is issued and column addresses are inputted to the column address buffer 344. In response to the $\overline{CAS}$ signal being at the low level at the time t_2, the buffer 344 generates pulse signals ϕ_C, ϕ_{CA}, ϕ_{CP} and BITSET. The signal ϕ_{CAR} for controlling circuits associated with column address signal generation is generated from the column address reset signal generator 354 in response to the pulse signal ϕ_C and the signal ϕ_{YECi} which is generated from the column enable clock generator 66 in response to ϕ_{RCDi}. The column address buffer 344 outputs column address signals CA0 to CA9 in response to the pulse signal ϕ_{CA} from the $\overline{CAS}$ buffer and the signal ϕ_{CAR}. Thus, since the column address signals generated from the column address buffer 344 responsive to the column address enable/disable signal ϕ_{CAR}, which is generated by the ϕ_{RCDi} signal representative of the completion of $\overline{CAS}$ chain, and the ϕ_C signal representative of the activation of $\overline{CAS}$, the time duration from the activation of $\overline{CAS}$ (time t_2) until the output of the column address signals becomes considerably short. After the transition of the ϕ_{CAR} signal to the high level, the burst length counter 350 carries out counting operation of the system clock ϕ_{CLK} to detect the burst length. In response to count signals CNT0 and CNTI from the burst length counter 350, the burst length detector 352 generates the burst end signal COSI and the COSR signal representative of the burst length after the activation of $\overline{CAS}$. The detector 352 also produces COSDQ signal delayed by given clock cycles depending on a preset $\overline{CAS}$ latency value from the signal COSR to control the data output buffer 284 so as to provide data for the time period of data output which is defined by the burst length. Thus, since the $\overline{CAS}$ latency equals 3, the signal COSDQ is a signal delayed by approximately two cycles of ϕ_{CLK} from the signal COSR. Thus, the COSDQ signal is at the low level for the period of time defined by the $\overline{CAS}$ latency and the burst length (the time duration between t_3 and t_6).

The column address counter 346 loads column address signals from the column address buffer 344 in response to the pulse signal BITSET from the $\overline{CAS}$ buffer and the column address enable signal ϕ_{CARC}, and then generates column address signals PCA0 to PCA8 in sequence, counting the clock CNTCLK9 according to the burst length and the address mode. The column address buffer 344 generates sequential column address signals CA0 to CA8 composed of initial column addresses and the column address signals PCA0 to PCA8.

FIG. 41 shows the timing chart at a binary address mode ((ϕ_{INTEL}=0) where initial external column address A_0 is high and the remaining external column addresses A_1 to A_8 are all low. Since the burst length was set to 4, only the burst length signal SZ_4 stays at a high level. Thus, only the lower two stages ST1 and ST2 of the first counter portion constituting the column address counter 346 of FIG. 35 executes the binary counting operation. Since the counting operation is performed at 100 MHZ, the clock CNTCLK9 is identical to the system clock ϕ_{CLK}. Thus, the outputs RCA0 and RCA1 of the data transfer control counter 348 are identical to the outputs PCA0 and PCA1 of the column address counter 346. The outputs RCA0 and RCA1 of the counter 348 are fed to the read data transfer clock generator 356, thereby generating read data transfer pulses RDTP0 to RDTP3 therefrom.

On the other hand, column address signals CA0 to CA8 from the column address buffer 344 are fed to the column decoder 24, and the column predecoder 436 of FIG. 39a produces partly overlapped predecode signals DCA$\overline{1}$ $\overline{2}$ and DCA1$\overline{2}$ with the successive column address signals CA1 and CA2. The main column decoder 444 of FIG. 40 receives the predecode signals to generate column selection signals CSL0 and CSL1. Since the column selection signal CSL0 allows data developed on bit line pairs to be transferred to the first I/O line pairs I/O_0, $\overline{I/O_0}$ and I/O_1, $\overline{I/O_1}$ data on the first I/O line pairs, which is produced by the first pulse 532 of the column selection signal CSL0, inputs to the I/O sense amplifier via corresponding I/O line selection circuit and corresponding first PIO line pairs. In response to the activating signal 535 as shown in FIG. 41C, the I/O sense amplifier amplifies data on the first PIO line pairs to output to corresponding first data line pairs DIO_0, $\overline{DIO_0}$ and DIO_1, $\overline{DIO_1}$. At this time, since the DIO line precharge signal DIOPR1 is at a high level, the second data line pairs DIO_2, $\overline{DIO_2}$ and DIO_3, $\overline{DIO_3}$ are in precharging states. Data transferred via the first data line pairs is stored into the register 278 in the data output multiplexer 268' of FIG. 25. Data transferred via the data line pair DIO_1, $\overline{DIO_1}$ of the first data line pairs is selected by the pulse RDTP1 and then

inputted to the data output buffer via the common data line pair CDL, $\overline{CDL}$, the data output latch 282 and the data output line pair DO, $\overline{DO}$. In the same manner as discussed above, parallel data on the second I/O line pairs I/O_2, $\overline{I/O_2}$ and I/O_3, $\overline{I/O_3}$, which is generated by the pulse 533 of column selection signal CSL1, is then inputted in series to the data output buffer. Last data on the I/O line pair I/O_0, $\overline{I/O_0}$ of the first I/O line pairs, which is generated by the second pulse 534 of the column selection signal CSL0, is then inputted to the data output buffer. If read-out is 1, 0, 1, 0, the data output buffer is enabled by the high level pulse ϕ_{TRST}, and its output DOUT is like the illustration of FIG. 41C. Thus, when the signal ϕ_{TRST} is lOW, the data output buffer 284 becomes a high impedance and thereby prevents unnecessary operation thereof. It can be seen that the first data is generated at the rising edge of the third clock of the system clock CLK after the activation of $\overline{CAS}$, and continuous 4-bit data is outputted in synchronism with the system clock CLK.

FIG. 33 is the timing chart showing a write operation at the $\overline{CAS}$ latency of 2 and the burst length of 4, using a system clock of 66 MHZ. The timing of FIG. 33 is also of the case where external addresses A_0 and A_1 to A_8 are respectively applied with a high level and low levels in the same manner as above-mentioned read operation, and the input data DIN to the data input buffer is a serial data of 1,0,1,0. The $\overline{RAS}$ chain operation is performed as previously discussed, and the burst length signal COSR is generated by the burst end signal COSI. Sequential column address signals RCA0 and RCA1 for generating write data transfer pulses WDTP0 to WDTP3 are produced by column address signals CA0 and CA1. Write command is issued at time t_2, and write control signals ϕ_{WR} and ϕ_{EWDC} are produced from the $\overline{WE}$ buffer 340 by the low level signal $\overline{WE}$. In response to the signals RCA0 and RCA1, the write data transfer clock generator 358 generates write data transfer pulses WDTP0 to WDTP3 for converting a serial data to a parallel data. The input data DIN inputting via the data input buffer 312 is outputted on the input line DI as the serial data synchronized with ϕ_{CLK} as shown in FIG. 33. The data input demultiplexer 314 produces the parallel data on the data lines $\overline{DIO_1}$, DIO_2, $\overline{DIO_3}$ and DIO_0 under the control of control signals WCA1 and $\overline{WACI}$ and the write data transfer pulses WDTP0 to WDTP3, having the timing as shown in FIG. 33. The parallel data is fed to corresponding I/O bus via the PIO line driver 330 under the control of control signals IOPR1 and $\overline{IOPRI}$, and then written into corresponding memory cells via bit lines selected by the column selection signals.

FIG. 49 is the timing chart showing the $\overline{CAS}$ interrupt read operation at the $\overline{CAS}$ latency of 3 and the burst length of 4, using a system clock of 66 MHZ. At the read command of time t_1, external addresses A_0 and A_1 to A_8 are respectively applied with a high level and low levels, and at the $\overline{CAS}$ interrupt read command of time t_3, external addresses A_1 and A_0 and A_2 to A_8 are respectively applied with a high level and low levels. This $\overline{CAS}$ interrupt read operation is identical to the previously discussed read operation, excepting that the last 2-bit data of the data, which must be read out by the read command issued at time t_1, can never be read out by the $\overline{CAS}$ interrupt command issued at time t_3. Referring to FIG. 49, explanation will be made in brief. The activation command, i.e., the $\overline{RAS}$ activation command is issued at two cycles of CLK before time t_1. Then since operation of $\overline{RAS}$ chain with row addresses is identical to that as previously discussed, explanation of this operation will be omitted. The read command is issued at time t_1, and the column predecode signal DCA$\overline{1}$ $\overline{2}$ from the column predecoder (shown in FIG. 39a) then becomes high with CA1 and CA2 being at low levels. Then, the column selection signal CSL0 includes the high level pulse 600, as shown in FIG. 49b, with CA2 to CA8 being always at low levels. After the transition of CA1 from the low level to the high level, the column predecode signal DCA1$\overline{2}$ becomes high, overlapping one end portion of the signal DCA$\overline{1}$ $\overline{2}$, and thereby the column selection signal CSL1 has the high level pulse 601. Once the $\overline{CAS}$ interrupt read command is issued at time t_3, the $\overline{CAS}$ buffer 338 then generates the signal BITSET of pulse 602. The burst length counter 350 is then reset by the pulse 602 and re-starts a binary counting operation with the system clock ϕ_{CLK}. After counting the burst length of 4, the counter 350 generates the burst end signal COSI of pulse 603. Then, the burst length detector 352 produces the low level signal COSR indicating of a burst length from the first read command with the pulse ϕ_C and the signal COSR, and then outputs the signal COSDQ indicating of a data read-out time period with the signal COSR and the $\overline{CAS}$ latency signal. Thus, it can be seen that a total 6-bit data may be read out. The column address buffer 344 shown in FIG. 34 latches external column addresses inputted upon $\overline{CAS}$ interrupt (at time t_3) by the high level pulse ϕ_{CA} from the $\overline{CAS}$ buffer 338, and produces successive four column address signals with the help of the column address counter 346. Thus, column address signal CA1, which is latched by the external high level address A_1 inputted at time t_3, maintains high for about two clock cycles after the transition of ϕ_{CA} to the low level since the least significant column address signal CA0 stays at the low level. Then, since CA2 to CA8 are all low at this time, the column selection signal CSL1 becomes the high level pulse 604. After the transition of CA1 to the low level, CA1 and its complement $\overline{CA1}$ respectively stay low and high for about two clock cycles. However, the low-going signal ϕ_{CAR} causes CA1 and $\overline{CA1}$ to go low. This results in allowing the column selection signal CSL0 to become the high level pulse 605 on the other hand, with column addresses A_0 and A_1 being respectively high and low at t_1, and with column addresses A_0 and A_1 being respectively low and high at t_3, read data transfer pulses RDTP0 to RDTP3 are generated as shown in FIG. 49b.

Data on bit line pairs is transferred to first I/O line pairs by the pulse 600 of CSL0, and then transferred to first data pairs DIO_0, $\overline{DIO_0}$ and DIO_1, $\overline{DIO_1}$ via first PIO line pairs. FIG. 49c shows where a high level data and a low level data are respectively transferred in parallel on DIO_0 line and DIO_1 line. This parallel data is stored into latches 278a and 278b in the data output multiplexer 268 of FIG. 25, and the pulse 606 of RDTP1 then causes the stored data of the latch 278b associated with the line DIO_1 to output therefrom. Consequently, the data output buffer outputs the low level data RD1. Parallel data selected by the pulse 601 of CSL1 is transferred to second data line pairs DIO_2, $\overline{DIO_2}$ and DIO_3, $\overline{DIO_3}$ via second I/O line pairs and second PIO line pairs. It can be seen that data on DIO_2 and DIO_3 is respectively high and low. The pulse 607 of RDTP2 selects data stored into the latch 278c and the data output buffer then outputs the high level data RD2. Likewise, parallel data selected by the pulse 604 of CSL1 is transferred to data lines DIO_2 and DIO_3. The drawing of FIG. 49c shows that a low level data and a high level data are transferred on data lines DIO_2 and DIO_3, respectively. The transfer switch 276 of FIG. 25 becomes an off state with the high level pulse P of ϕ_{CL}. However, after the data, which was stored into the latch 278c via the line DIO_2 in the previous operation, has been transferred toward the data output buffer by the pulse 607 of RDTP2, the pulse P goes low. Then, the switch 276 becomes

on. Thus, data on the data lines DIO_2 and DIO_3 is respectively stored into latches 278c and 278d. Data stored into the latch 278c is then outputted by the pulse 607 of RDTP2 and thereby the data output buffer 284 outputs the low level data RD3. Data stored into the latch 278d is then outputted by the pulse 608 of RDTP3, thereby resulting in outputting the high level data RD4 from the data output buffer 284. Likewise, data selected by the pulse 605 of CSL0 is transferred to first data line pairs. It can be seen in the drawing that a low level data and a high level data are respectively transferred in parallel on data lines DIO_0 and DIO_1. In the same manner as discussed above, this parallel data is selected in sequence by the pulses 609 and 610 shown in FIG. 49b, and the data output buffer 284 then outputs the low level data RD5 and the high level data RD6 in sequence. The data output buffer 284 then becomes a high impedance with the high level signal COSDQ.

FIG. 54 is a timing chart showing various operations at the $\overline{CAS}$ latency of 2 and the burst length of 4, using only one selected bank. Commands are given as follows: activation command at t_1, read command with external column addresses CA0 at t_2, $\overline{CAS}$ interrupt read command with external column addresses CB0 at t_3, $\overline{CAS}$ interrupt write command with external column addresses CC0 at t_7, $\overline{CAS}$ interrupt write command with external column addresses CD0 at t_{10}, precharge command at t_{12} and data input/output masking command at t_6, t_9, t_{12} and t_{13}. Data QA0 and QA1 respectively output at t_3 and t_4 due to the read command issued at t_2, and data QB0 and QB1 successively output at t_5 and t_6 due to the read command issued at t_3. At t_7, data output is inhibited and stays in a high impedance state due to the data output masking command issued at t_6. At t_8 and t_9, write data DC0 and DC1 respectively input due to the write command at t_7. The data input masking command at t_9, write data DC0 and DC1 respectively input due to the write command at t_7. The data input masking command at t_9 interrupts receipt of write data at time t_{10}. Likewise, at t_{11} and t_{12}, write data DD0 and DD1 are respectively inputted due to the write command at t_{10}. The data input masking command issued at t_{12} and t_{14} after the precharge command at t_{12}.

FIG. 55 is a timing chart showing various operations at the $\overline{CAS}$ latency of 2 and the burst length of 4 with one selected bank. Read, write and data input/output masking operations are the same as those of FIG. 54. After issuance of freeze command at t_1, generation of a pulse of internal system clock ϕ_{CLK} corresponding to the pulse 536 of the system clock CLK is inhibited. Thus, the output of data at t_3 is frozen so as to output the same data as the output of data at t_2. Likewise, the internal system clock, in which the generation of corresponding pulse is precluded, causes operation of the column address counter to be frozen, thereby inhibiting writing of data at t_5.

FIG. 56 is a timing diagram showing a read operation at the $\overline{CAS}$ latency of 2 and the burst length of 4 with two banks. With activation command of the first bank at t_1, and with read command at t_2, successive data QAO to QS3 outputs from time t_3. With activation command of the second bank at t_3, and with read command at t_4, successive data QB0 to QB3 also outputs from time t_5. At time t_6, simultaneous precharge command is issued at t_6.

FIG. 57 is a timing diagram showing an interleave read operation with the $\overline{CAS}$ latency of 2 and the burst length of 4. Activation command for the first bank is issued at time t_1, and that for the second bank is then issued at time t_2. Thus, data QA0 to QA3 is read out from the first bank from time t_3. At the same time, activation command for the second bank is issued at t_3. At time t_4, read command is issued for the second bank selected with the high level column address A_9. Then, after output of successive 4-bit data QA0 to QA3, read-out data QB0 and QB1 outputs from the second bank with no gap. At time t_5, read command is issued for the first bank with the low level column address A_9, thereby successively outputting read-out data QC0 and QC1 from the first bank. Read command is then issued for the second bank at time t_6, thereby outputting read-out data QD0 and QD1. Precharge command is then issued for the first bank at time t_7. Read command is then issued for the second bank at time t_8, thereby outputting read-out data QE0 to QE3. Precharge command is issued for the second bank with external addresses A_{10} and A_{11} at time A_9.

Explanation has been made on various operation modes with a single data input/output pad in connection with FIGS. 54 to 57. However, it should be noted that the present embodiment has eight data input/output pads and various applications are also possible.

OTHER EMBODIMENTS

As discussed hereinabove, the present synchronous DRAM has been modified with pulse $\overline{RAS}$. However, the synchronous DRAM of the present invention may be embodied with the level $\overline{RAS}$. Various operation commands for the level $\overline{RAS}$ have been already explained. In order for the present synchronous DRAM to operate with the level $\overline{RAS}$, some circuits need modifications, but others may be used with no modification.

FIG. 58 is a drawing showing a schematic circuit diagram for a $\overline{RAS}$ buffer using the level $\overline{RAS}$. Referring to the drawing, an input buffer 70 and a synchronization circuit 108 which constitute the level $\overline{RAS}$ buffer 538 are the same in constructions and operations as the $\overline{RAS}$ buffer 56 for the pulse $\overline{RAS}$ showing in FIG. 9. The output of the synchronization circuit 108 is connected in common with a first $\overline{RAS}$ signal generator 540 for the first bank and with a second $\overline{RAS}$ signal generator 542 for the second bank via a latch 550. The first $\overline{RAS}$ signal generator 540 comprises a flip-flop 545 for storing a first bank $\overline{RAS}$ signal in response to a bank selection signal $\overline{SRA11}$ produced by an address A_{11}. The flip-flop 545 is a NAND type flip-flop comprised of NAND gates 544 and 546. One input terminal of the flip-flop 545 is connected to the output Of a NOR gate 548, and the other input terminal of the flip-flop 545 receives a $\overline{RAS}$ signal from the synchronization circuit 108. The NOR gate 548 receives the bank selection signal $\overline{SRA11}$ on its first input terminal and a signal on its second input terminal which is staying at a high level during a refresh, a mode set or a test operation. The construction of the second $\overline{RAS}$ signal generator is the same as that of the first $\overline{RAS}$ signals generator. Thus, Upon the activation of $\overline{RAS}$, if the external address A_{11} is low, i.e., $\overline{RAS}$ signal ϕ_{RC1} is then latched to a high level. At this time, since the NOR gate 548' of the second $\overline{RAS}$ signal generator 542 outputs high, the flip-flop 545' maintains the previous state. That is, if upon the activation of $\overline{RAS}$ in the previous operation, A_{11} was high, i.e., SRA11 was high, the second bank $\overline{RAS}$ signal ϕ_{RC2} keeps high. On the other hand, if $\overline{RAS}$ goes from a low level to a high level, the latch 550 latches a high level at the rising edge of the next system clock ϕ_{CLK}. Thus, NAND gates 546 and 546' each receives a low level, and thereby the signals ϕRC1 and ϕ_{RC2} becomes low. That is, both banks go to precharge states. In addition, since O_{RFH} is low during a refresh, and O_{WCBR} is low during a mode set operation, the signals ϕ_{RC1} and ϕ_{RC2} are all high in such operations. Signals ϕ_{RC1} and ϕ_{RL2} are faster signals than the signals ϕ_{RC1} and ϕ_{RC2}.

FIG. 59 is a drawing showing address buffers for generating special addresses SRA10 and SRA11. These address buffers is independent buffers separated from the row and column address buffers. The address buffer 552 for producing SRA10 in response to an address A_{10} is used in the pulse $\overline{RAS}$, but not in the level $\overline{RAS}$. The address buffer 552 has the same construction as previously mentioned buffers each comprised of the input buffer 70 and the synchronization circuit 108. The address buffer 554 for producing SRA11 in response to an address A11 comprises a transfer switch 556 which is turned on in response to signals ϕ_{RC1} and ϕ_{RC2} produced in case of level $\overline{RAS}$. The transfer switch 556 is turned off by activation of either the first or the second bank and also serves to prevent from changing a logic level of the signal SRA11 with the system clock ϕ_{CLK} after activation of one of both banks. In case that the address buffer 554 is used for the pulse $\overline{RAS}$, it may be modified so that the output of the latch 558 becomes SRA11.

FIG. 60 is a schematic circuit diagram of a level $\overline{RAS}$ control circuit for generating a mode set control signal O_{WCBR} and a refresh clock O_{RFH} in case of the level $\overline{RAS}$. In the mode set control signal generator 200 of FIG. 14 used in the pulse $\overline{RAS}$, the transfer switches are gated by the signal ϕ_{RP}. However, in case of the level $\overline{RAS}$, the transfer switches are gated by a signal being produced by the signals ϕ_{RL1} and ϕ_{RL2} in place of the signals ϕ_{RP}. This is to generate the signals O_{WCBR} and O_{RFH} with faster signals ϕ_{RL1} and ϕ_{RL2} than ϕ_{RC1} and ϕ_{RC2}. Its operation is the same as that explained in connection with FIG. 14.

FIG. 61 is a drawing showing an operation timing charge of the synchronous DRAM using the level $\overline{RAS}$. The operation timing chart as shown in this drawing has relationship with that using the pulse $\overline{RAS}$ as shown in FIG. 54. In the drawing of FIG. 61, a precharge command is issued at time t_1. Remaining operations are the same as those of the pulse $\overline{RAS}$.

As explained hereinabove, the system design and using ways of the present synchronous DRAM have been explained in detail. Although embodiments of the present invention have been explained in connection with a synchronous DRAM, it would be obvious to those skilled in the art that the present invention may also be applied to other semiconductor memories.

What is claimed is:

1. A dynamic random access memory receiving an external clock comprising:

a plurality of memory banks each including a plurality of memory cells having an address associated therewith and operable in either one of an active cycle and a precharge cycle at any one time;

means for receiving a row address strobe signal and latching a logic level of the row address strobe signal in response to one of a rising edge and a falling edge of said clock;

address input means for receiving a portion of one of said addresses to indicate selection of one of the memory banks; and

means, receiving the latched logic level and the one address portion, for outputting an activation signal to said one selected memory bank and an inactivation signal to unselected memory banks when the latched logic level is at a first logic level, so that said one selected memory bank operates in the active cycle while the unselected memory banks operate in the precharge cycle.

* * * * *

US005808958A

United States Patent [19]

Vogley et al.

[11] **Patent Number: 5,808,958**

[45] **Date of Patent: Sep. 15, 1998**

[54] **RANDOM ACCESS MEMORY WITH LATENCY ARRANGED FOR OPERATING SYNCHRONOUSLY WITH A MICRO PROCESSOR AND A SYSTEM INCLUDING A DATA PROCESSOR, A SYNCHRONOUS DRAM, A PERIPHERAL DEVICE, AND A SYSTEM CLOCK**

[75] Inventors: **Wilbur Christian Vogley**, Missouri City; **Anthony Michael Balistreri**, Houston; **Karl M. Guttag**, Missouri City; **Steven D. Krueger**, Houston; **Duy-Loan T. Le**; **Joseph H. Neal**, both of Sugarland; **Kenneth A. Poteet**, Houston; **Joseph P. Hartigan**, Stafford; **Roger D. Norwood**, Houston, all of Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **477,735**

[22] Filed: **Jun. 7, 1995**

Related U.S. Application Data

[60] Continuation of Ser. No. 327,540, Oct. 21, 1994, Pat. No. 5,587,954, which is a division of Ser. No. 184,749, Jan. 21, 1994, Pat. No. 5,390,149, which is a continuation of Ser. No. 690,207, Apr. 23, 1991, abandoned.

[51] **Int. Cl.**[6] **G11C 8/00**

[52] **U.S. Cl.** **365/233**; 365/230.06; 365/230.08; 365/236

[58] **Field of Search** 365/233, 189.05, 365/230.08, 230.06, 51, 221, 230.01, 236

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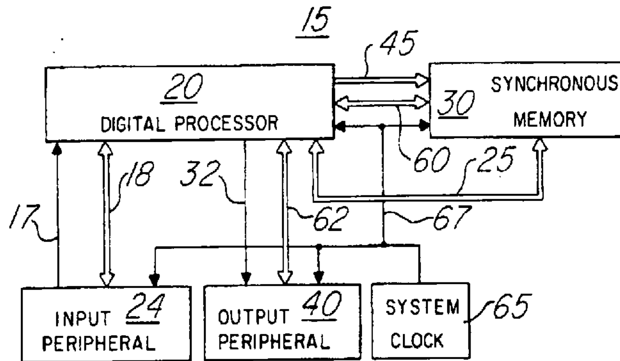
Primary Examiner—Do Hyun Yoo
Attorney, Agent, or Firm—Robert N. Rountree; J. Fred Telecky; Richard L. Donaldson

[57] **ABSTRACT**

A synchronous random access memory is arranged to be responsive directly to a system clock signal for operating synchronously with the associated microprocessor. The synchronous random access memory is further arranged to either write-in or read out data in a synchronous burst operation or synchronous wrap operation in addition to synchronous random access operations. The synchronous random access memory device may be fabricated as a dynamic storage device or as a static storage device.

71 Claims, 12 Drawing Sheets



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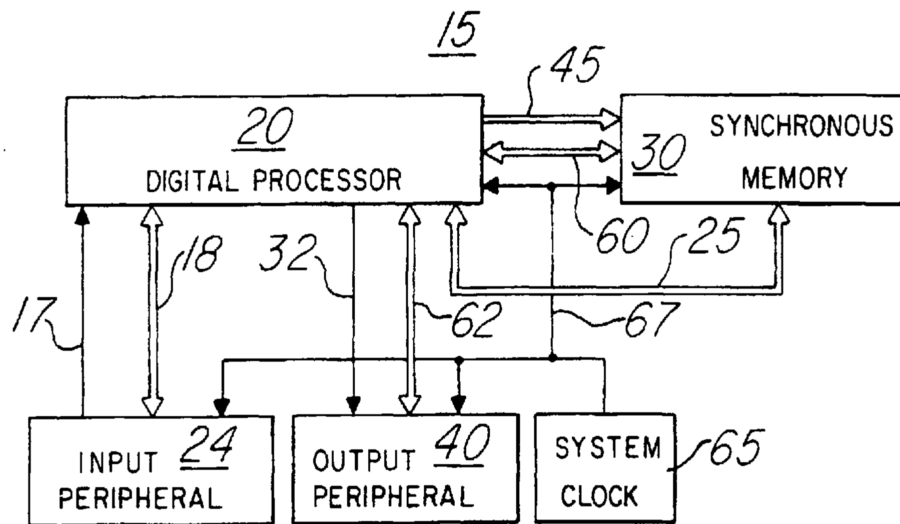

FIG. 1

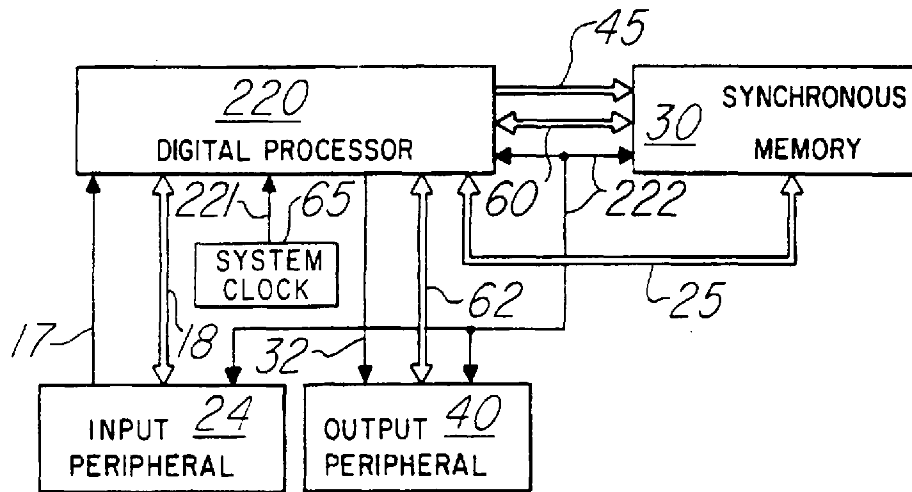

FIG. 24

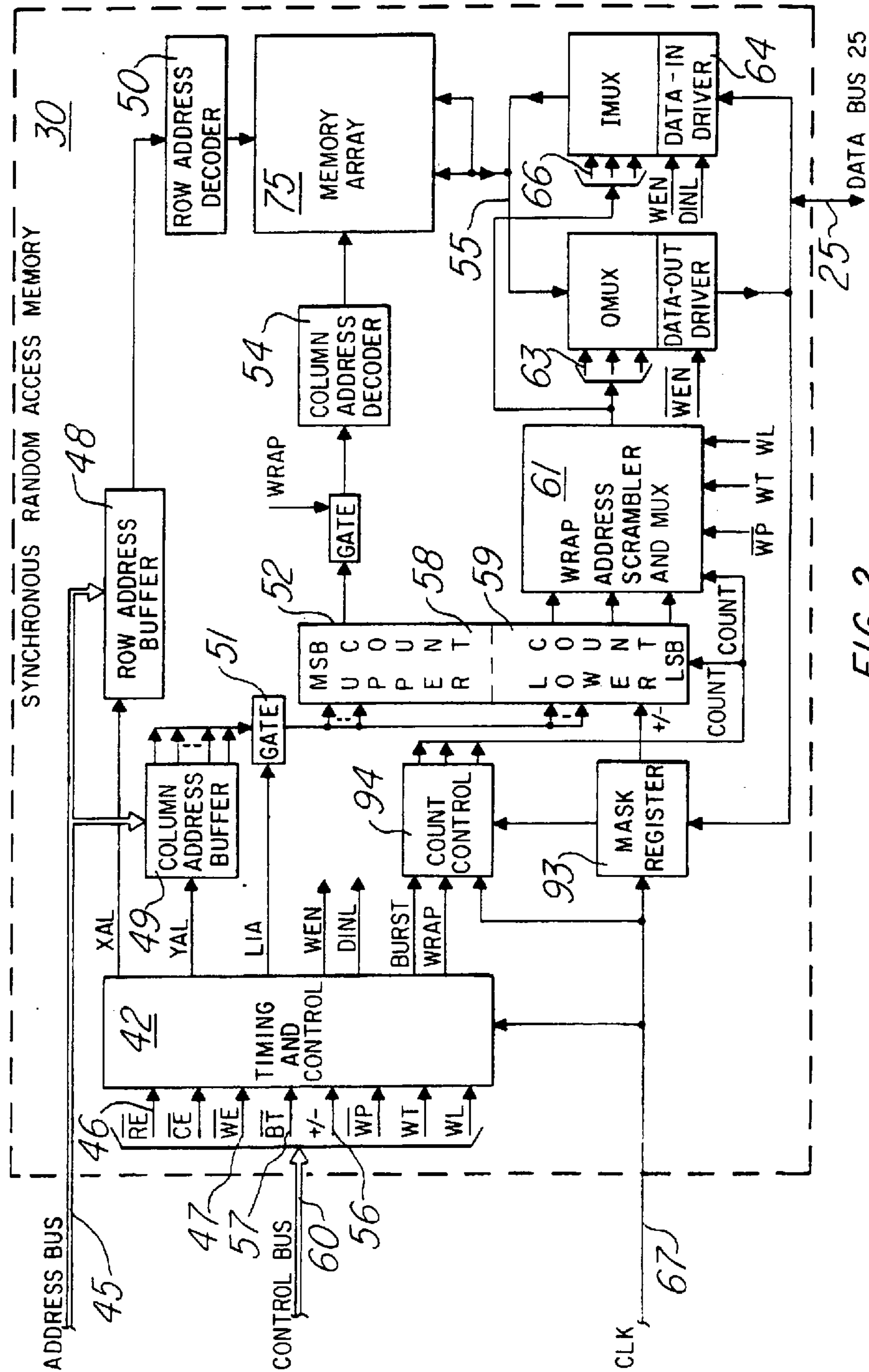

FIG. 2

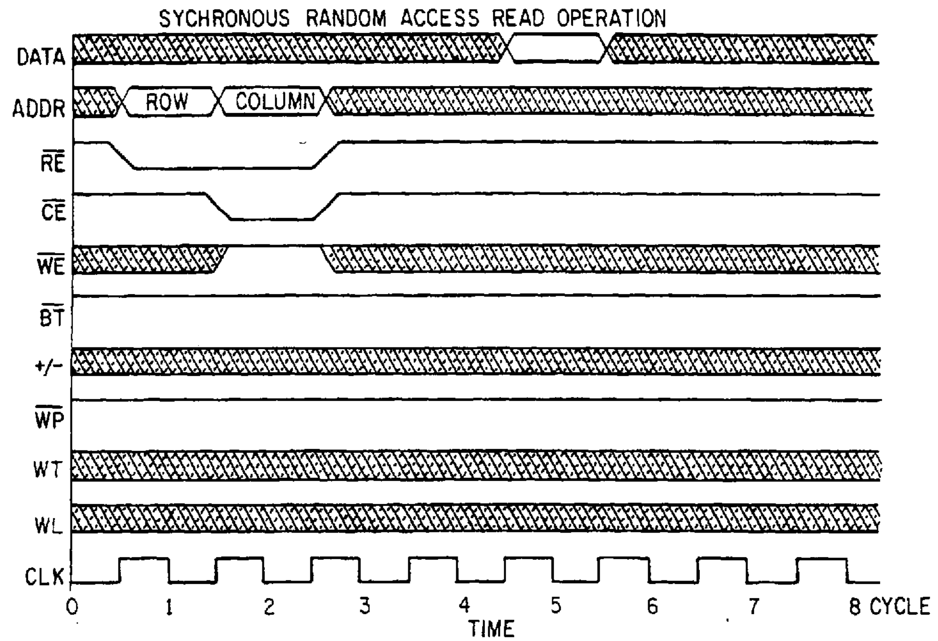

FIG. 3

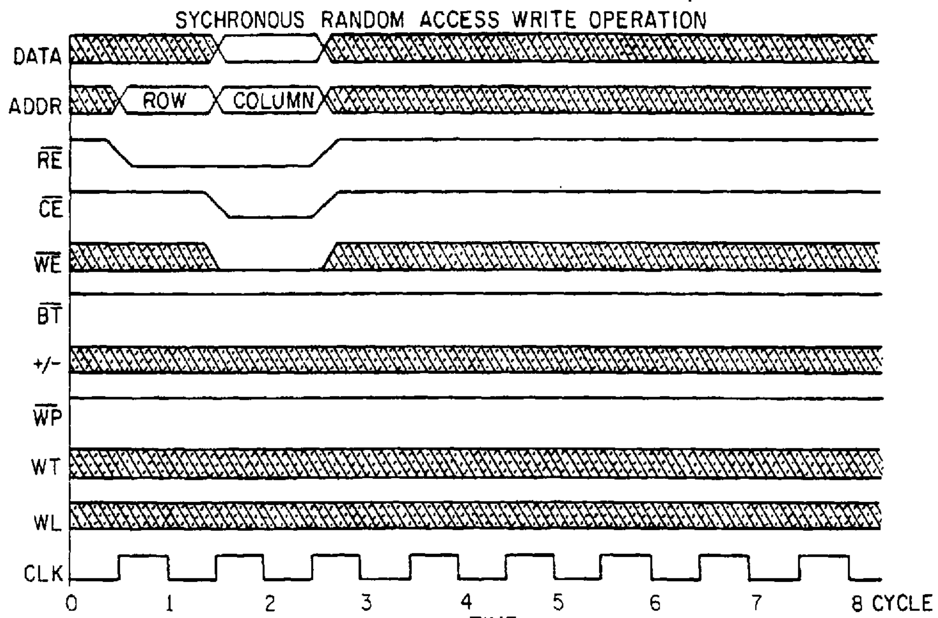

FIG. 4

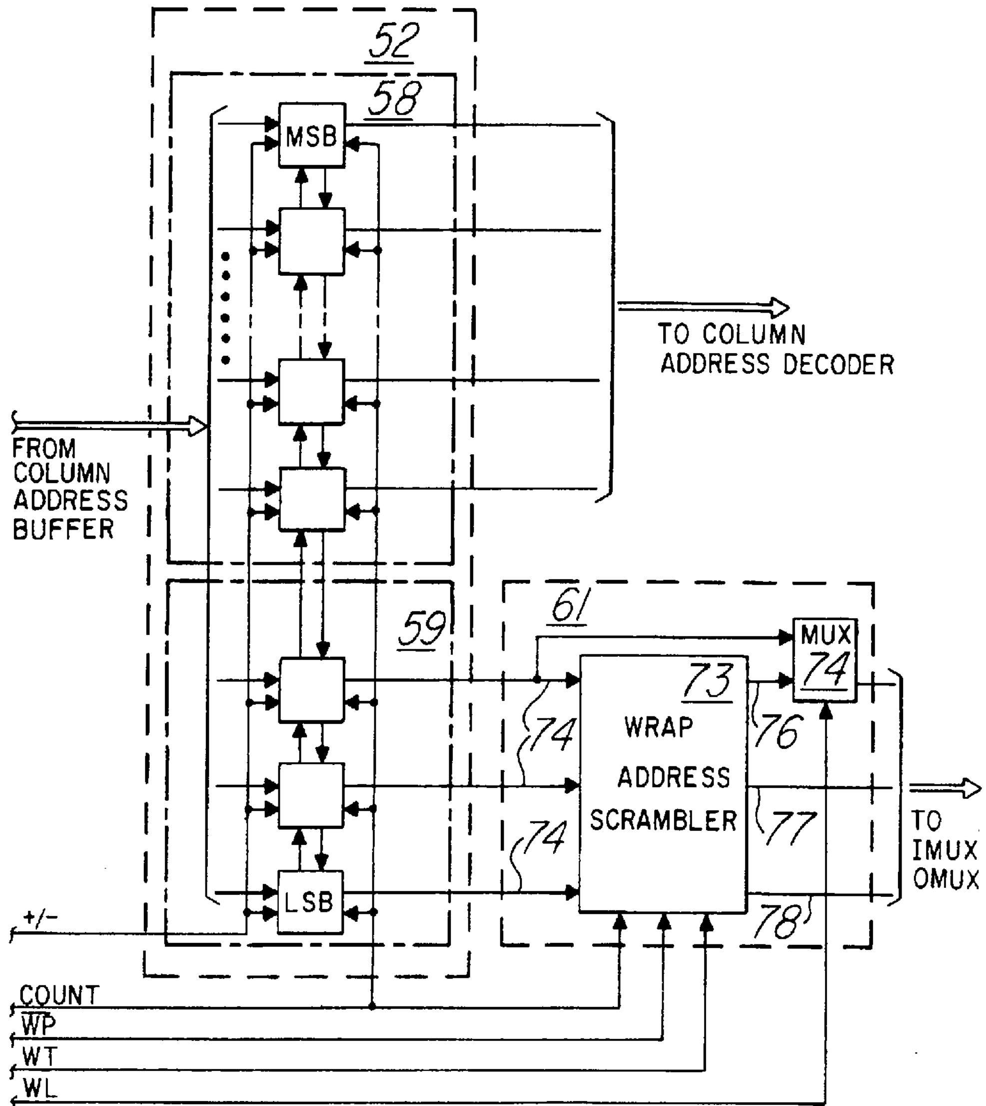

FIG. 6

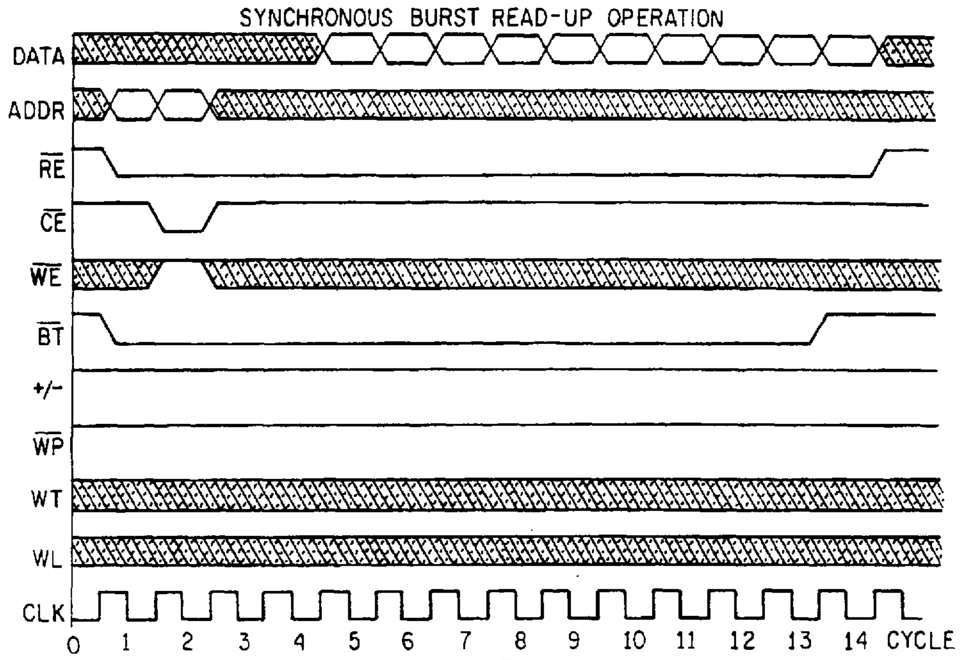

FIG. 5

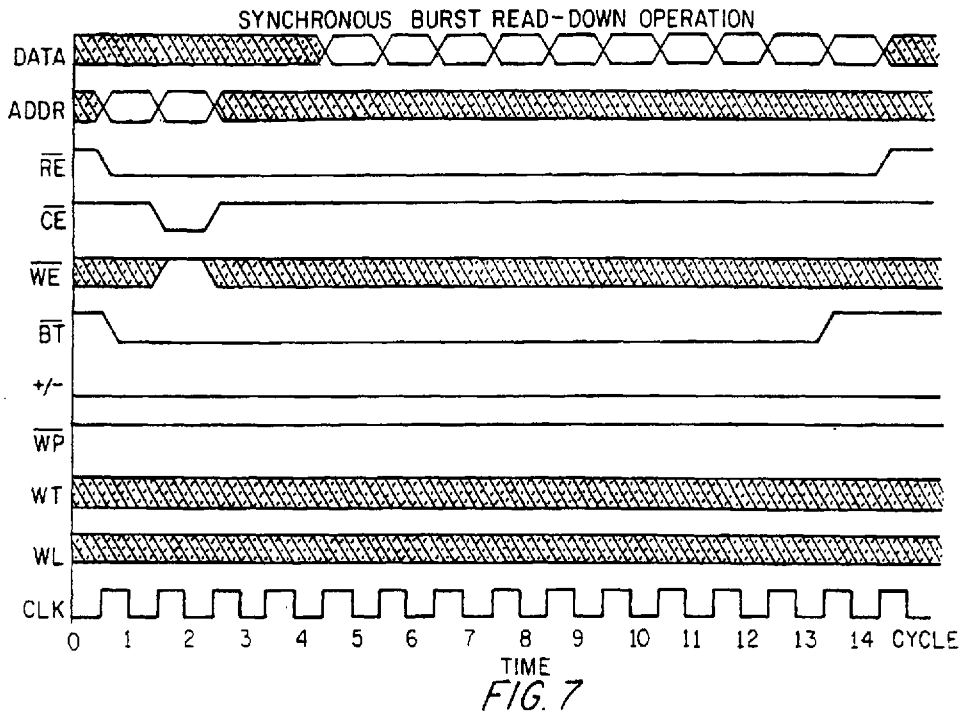

FIG. 7

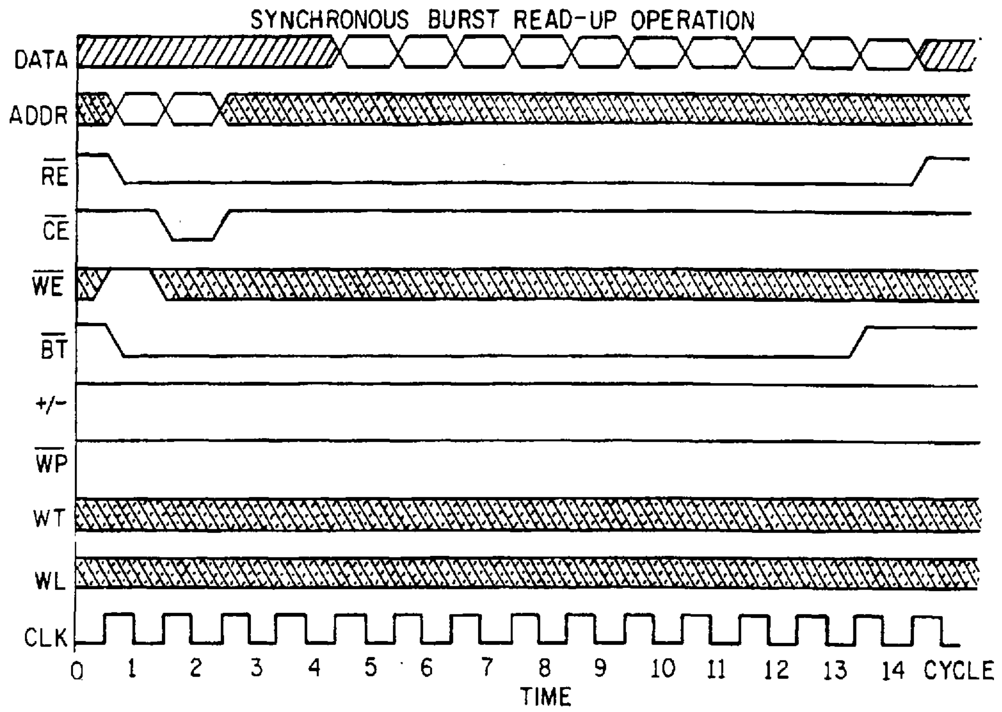

FIG. 8

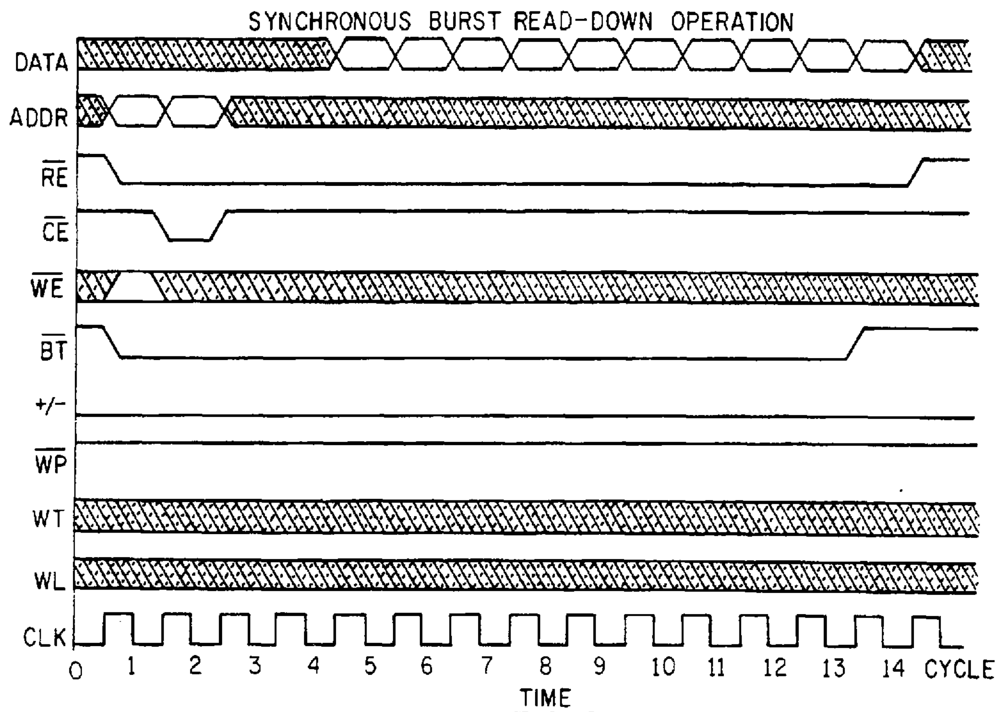

FIG. 9

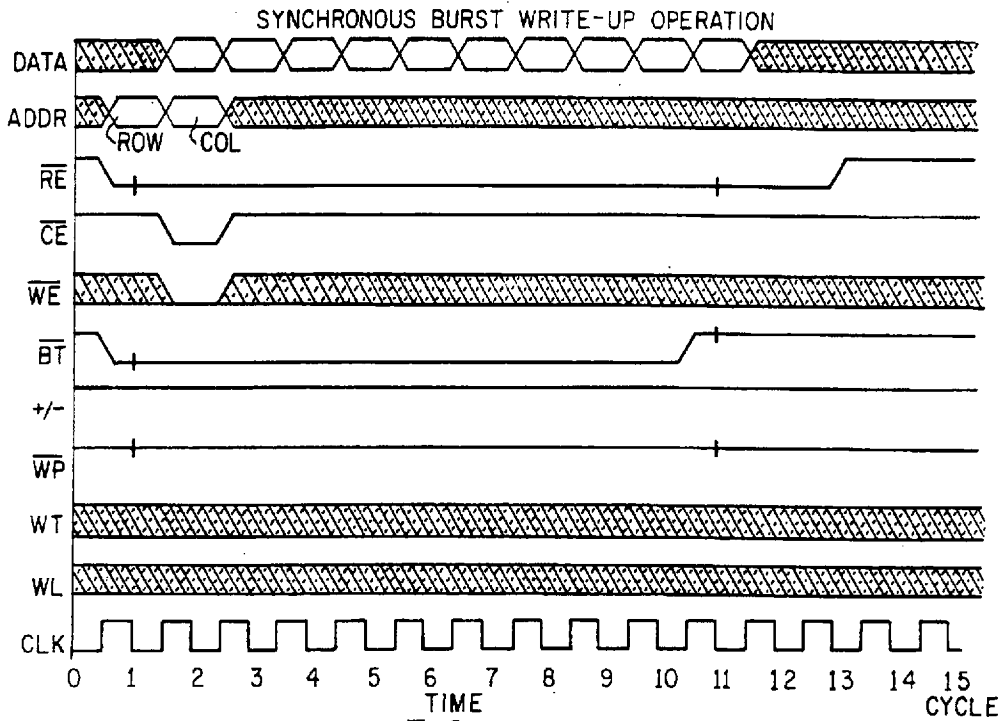

FIG. 10

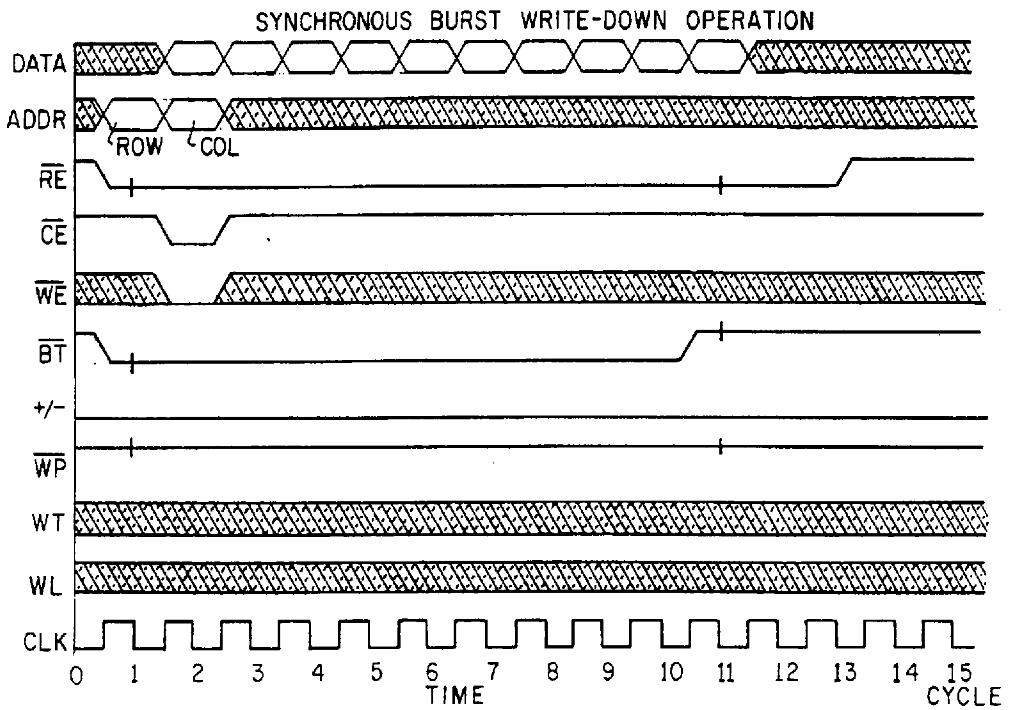

FIG. 11

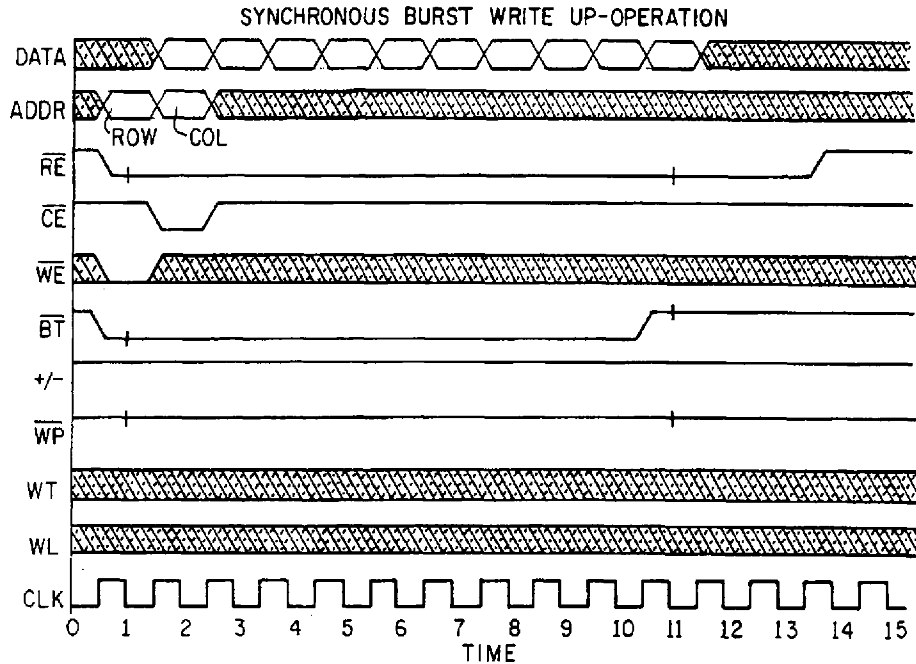

FIG. 12

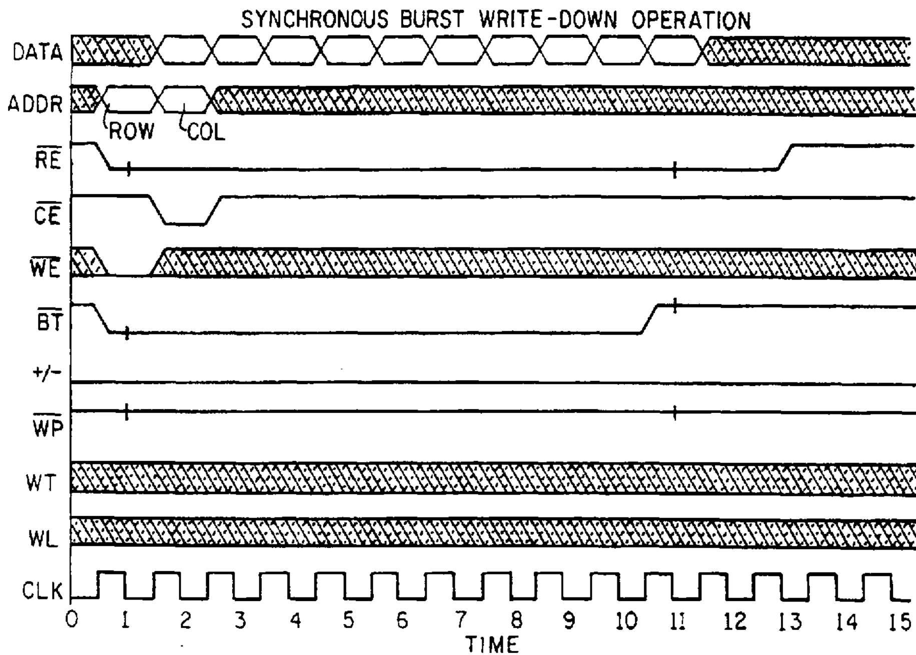

FIG. 13

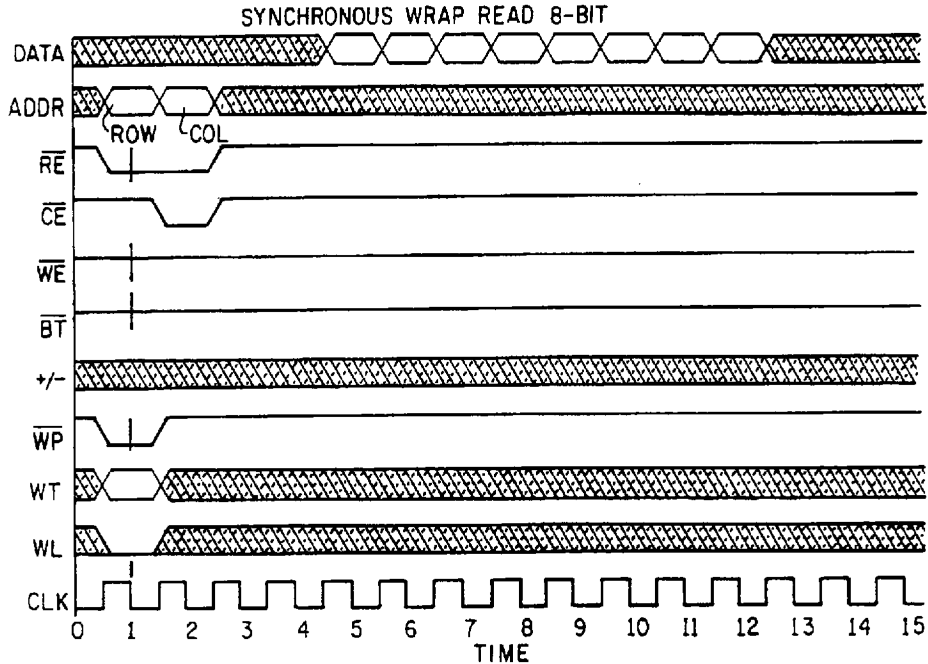

FIG. 14

TABLE I

WRAP LENGTH WL=0				
INITIAL INPUT ADDRESS			OUTPUT ADDRESS SEQUENCE	
A2	A1	A0	WRAP TYPE WT=0	WRAP TYPE WT=1
0	0	0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
0	0	1	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
0	1	0	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
0	1	1	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
1	0	0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
1	0	1	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
1	1	0	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
1	1	1	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0

FIG. 15

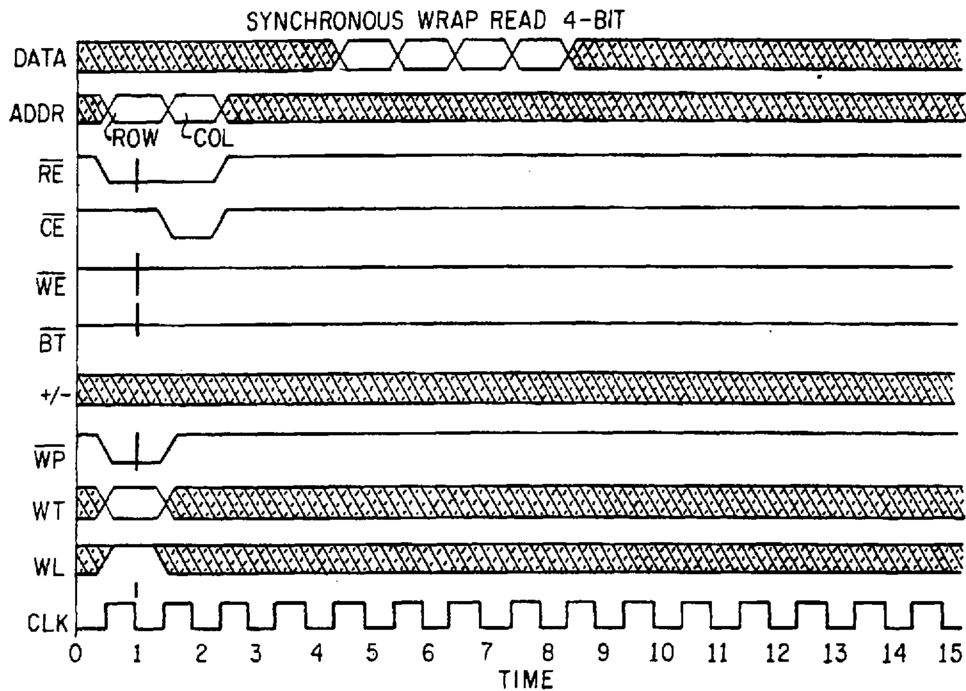

FIG. 16

TABLE II

WRAP LENGTH WL=1			
INITIAL INPUT ADDRESS		OUTPUT ADDRESS SEQUENCE	
A1	A0	WRAP TYPE WT=0	WRAP TYPE WT=1
0	0	0,1,2,3	0,1,2,3
0	1	1,2,3,0	1,0,3,2
1	0	2,3,0,1	2,3,0,1
1	1	3,0,1,2	3,2,1,0

FIG. 17

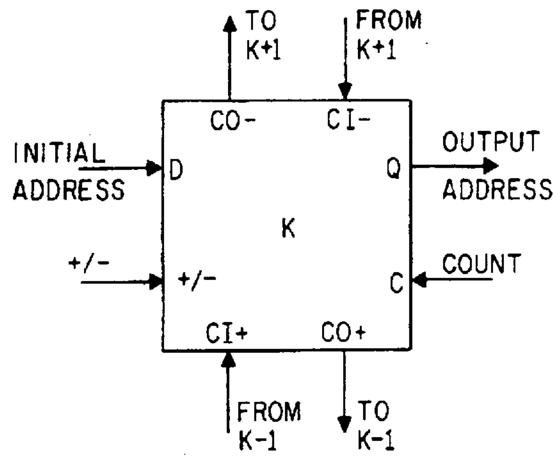

FIG. 18

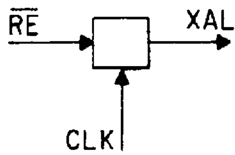

FIG. 19

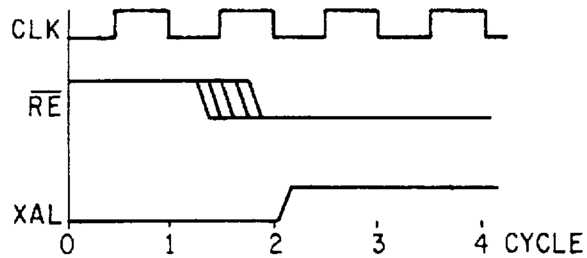

FIG. 20

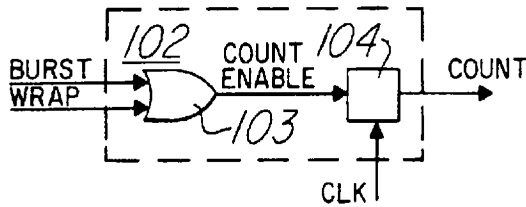

FIG. 21

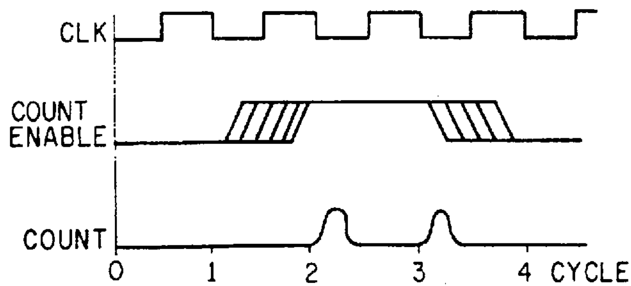

FIG. 22

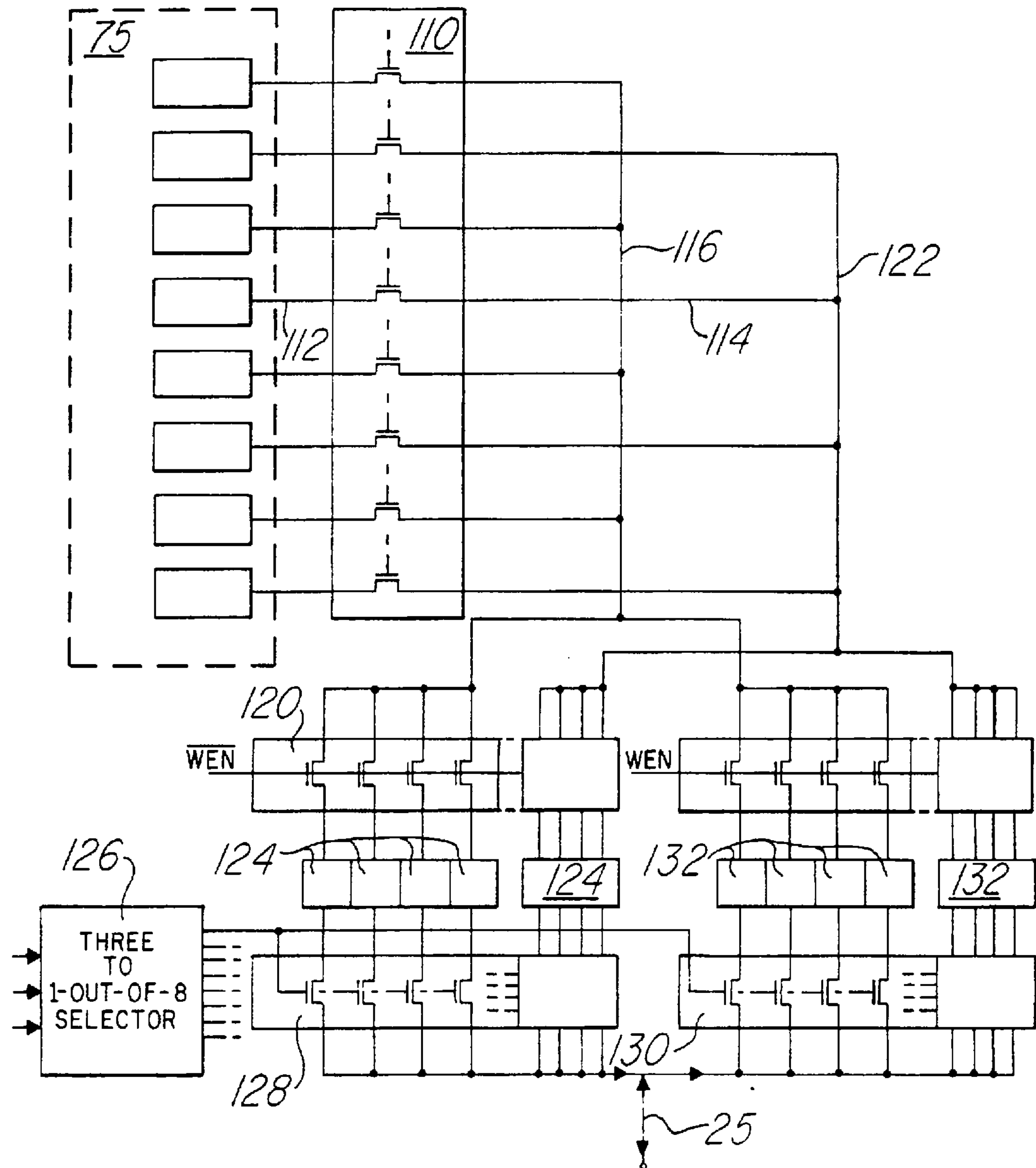

FIG. 23

RANDOM ACCESS MEMORY WITH LATENCY ARRANGED FOR OPERATING SYNCHRONOUSLY WITH A MICRO PROCESSOR AND A SYSTEM INCLUDING A DATA PROCESSOR, A SYNCHRONOUS DRAM, A PERIPHERAL DEVICE, AND A SYSTEM CLOCK

This is a continuation of application Ser. No. 08/327,540, filed Oct. 21, 1994, now U.S. Pat. No. 5,587,954, which is a divisional of Ser. No. 08/184,749, filed Jan. 21, 1994, now U.S. Pat. No. 5,390,149, which is a continuation of 07/690,207, filed Apr. 23, 1991, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates to random access memory (RAM) arranged for operating in a data processing system.

In the past, semiconductor random access memory operated faster than the associated microprocessor. During the late 1970's and early 1980's, the microcomputer market was in the early stages of development. At that time, a microcomputer system included a microprocessor and a dynamic random access memory. In a microcomputer arrangement, the microprocessor ran synchronously in response to a clock signal, but the dynamic random access memory ran asynchronously with respect to the operation of the microprocessor. The microprocessor clock was applied to a controller circuit that was interposed between the microprocessor and the dynamic random access memory. In response to the microprocessor clock signal, the controller derived other control or clock signals which ran the dynamic random access memory operation.

Typical operating speeds of the microprocessor and the dynamic random access memory were different from each other. A microprocessor cycle time was in a range of 400–500 nanoseconds while a dynamic random access memory cycle time was approximately 300 nanoseconds. Thus the dynamic random access memory was able to operate faster than its associated microprocessor. The memory completed all of its tasks with time to spare. As a result, the microprocessor operated at its optimum speed without waiting for the memory to write-in data or read out data.

Subsequently, as the semiconductor art developed, the operating speeds of microprocessors and memory devices have increased. Microprocessor speeds, however, have increased faster than dynamic random access memory speeds. Now microprocessors operate faster than their associated dynamic random access memory. For instance, a microprocessor cycle time is approximately 40 nanoseconds and a dynamic random access memory cycle time is approximately 120 nanoseconds. The microprocessor completes all of its tasks but must wait significant periods of time for the dynamic random access memory.

Having the microprocessor waiting for the memory is a problem that has been attracting the attention of many microcomputer designers. High speed static cache memories have been added to the microcomputer systems to speed up access to data stored in the memory. A significant part of the problem is to speed up access to data in the memory without significantly increasing the cost of the microcomputer system. Cache memory, however, is significantly more expensive than dynamic random access memory.

An existing problem with dynamic random access memory devices is that they require a substantial amount of peripheral circuitry between the microprocessor and the

memory for generating several control signals. So many interdependent control signals are generated by long logic chains within the peripheral circuitry that microcomputer systems designers must resolve very complex timing problems. The delay caused by the timing problems and the fact that memories now are accessed slower than the associated microprocessor cause problems of excessive time delays in microcomputer system operations.

SUMMARY OF THE INVENTION

These and other problems are solved by a random access memory which is arranged to be responsive directly to a system clock signal for operating synchronously with the associated digital processor. The synchronous random access memory is further arranged to write-in or read out data in either a synchronous burst mode or a synchronous wrap mode in addition to synchronous random access operations. Such a synchronous random access memory device may be fabricated as a dynamic or as a static storage device.

Control signals from the digital processor are used for controlling various memory operations. As an alternative, the digital processor may process a clock signal that is used as the system clock for operating both the digital processor and the synchronous random access memory. The digital processor may be a microprocessor.

BRIEF DESCRIPTION OF THE DRAWING

A better understanding of the invention may be derived by reading the following detailed description with reference to the drawing wherein:

FIG. 1 is a block diagram of a data processing system including a synchronous random access memory;

FIG. 2 is a block diagram of a synchronous random access memory;

FIG. 3 is a timing diagram of a synchronous random access read operation;

FIG. 4 is a timing diagram of a synchronous random access write operation;

FIG. 5 is a timing diagram of a synchronous burst read-up operation;

FIG. 6 is a block diagram of a column address counter and the wrap address scrambler;

FIG. 7 is a timing diagram of a synchronous burst read-down operation;

FIG. 8 is a timing diagram of another synchronous burst read-up operation;

FIG. 9 is a timing diagram of another synchronous burst read-down operation;

FIG. 10 is a timing diagram of a synchronous burst write-up operation;

FIG. 11 is a timing diagram of a synchronous burst write-down operation;

FIG. 12 is a timing diagram of another synchronous burst write-up operation;

FIG. 13 is a timing diagram of another synchronous burst write-down operation;

FIG. 14 is a timing diagram of a synchronous wrap read 8-bit operation;

FIG. 15 is a truth table for a wrap address scrambler used in a synchronous wrap read 8-bit operation;

FIG. 16 is a timing diagram of a synchronous wrap read 4-bit operation;

FIG. 17 is a truth table for a wrap address scrambler used in a synchronous wrap read 4-bit operation;

FIG. **18** is a schematic block diagram of a stage for the column address counter of FIG. **17**;

FIG. **19** is a logic schematic diagram of a timing gate circuit;

FIG. **20** is a timing diagram for the operation of the gate circuit of FIG. **19**;

FIG. **21** is a logic schematic diagram for another timing gate circuit;

FIG. **22** is a timing diagram for the operation of the gate circuit of FIG. **20**;

FIG. **23** is a block diagram of an input multiplexer and an output multiplexer arrangement for the synchronous memory of FIG. **2**; and

FIG. **24** is a block diagram of an alternative data processing system including a synchronous random access memory.

DETAILED DESCRIPTION

Referring now to FIG. **1**, a data processing system **15** includes a digital processor **20** which receives digital data by way of a bus **17** from an input peripheral device **24**. The digital processor **20** may be a microprocessor. Control signals pass between the digital processor **20** and the input peripheral device **24** by way of a control bus **18**. The digital processor **20** processes that data and other data, all of which may be transmitted by way of a data bus **25** for storage in and retrieval from a synchronous memory device **30**. The digital processor **20** also sends resulting output data via an output data bus **32** to an output peripheral device **40** where the output data may be displayed or used for reading, viewing or controlling another device that is not shown. Control signals are transmitted between the digital processor **20** and the synchronous memory device **30** by way of a control bus **60**. Control signals also are transmitted between the digital processor **20** and the output peripheral device **40** by way of a control bus **62**. System clock signals are produced by a system clock device **65** and are applied through a clock lead **67** to the digital processor **20**, the synchronous memory device **30**, the input peripheral device **24**, and the output peripheral device **40**.

From time to time during operation of the data processing system **15**, the digital processor **20** accesses the synchronous memory **30** for writing data into storage cells or for reading data from the storage cells thereof. Storage cell row and column addresses, generated by the digital processor **20**, are applied through an address bus **45** to the synchronous memory **30**. Data may be sent by way of the data bus **25** either from the digital processor **20** to be written into the synchronous memory **30** or to be read from the synchronous memory **30** to the digital processor **20**.

Control signals, produced by the digital processor **20** and transmitted by way of the control bus **60** to the synchronous memory **30** include a row address control signal $\overline{RE}$, a column address control signal $\overline{CE}$, a write signal $\overline{WE}$, a burst signal $\overline{BT}$, a burst direction signal +/−, a wrap select signal $\overline{WP}$, a wrap-type signal WT, a wrap-length signal WL, and others. Control signals may also be transmitted from the synchronous memory **30** to the digital processor **20**.

Referring now to FIG. **2**, the synchronous random access memory **30** includes a memory array **75** of metal-oxide-semiconductor (MOS) dynamic storage cells arranged in addressable rows and columns. The memory array **75** of storage cells is similar to the well known arrays of cells used in dynamic random access memory devices. Either complementary metal-oxide-semiconductor (CMOS) or bipolar complementary metal-oxide-semiconductor (BICMOS) technology may be used for fabricating the memory array **75**.

Several other circuit blocks are shown in FIG. **2**. These other circuit blocks are designed and arranged for operating the array of storage cells synchronously with the digital processor **20** of FIG. **1** in response to the common system clock signal CLK, which may be gated by the digital processor, as discussed subsequently with respect to FIG. **20**. The circuit blocks other than the array of storage cells may be fabricated as either CMOS or BICMOS circuits.

The synchronous random access memory **30** is operable for synchronous random access read or write operations, for synchronous burst read or write operations, and for synchronous wrap read or write operations. All types of synchronous operations are to be described fully hereinafter. Such descriptions are to be made in reference to timing diagrams and truth tables presented in FIGS. **3–5** and **7–17**. In the timing diagrams, a DON'T CARE state is represented by cross-hatching.

Referring now to FIGS. **3** and **2** for a synchronous random access read operation, an N bit wide row address and the row address control signal $\overline{RE}$ are applied to the address bus **45** and a lead **46**. Control signals, such as the signal $\overline{RE}$ and others, are active low signals. The write signal $\overline{WE}$ on a lead **47** being high, at clock cycle time 2, designates a read operation. The synchronous read operation commences at a falling edge of the system clock signal CLK at signal time **1**. For this illustrative embodiment, the system clock times operations in synchronism at the negative-going edges of the clock pulses, such as at the cycle times 1, 2, 3, etc. In other embodiments, not shown herein, the system may time operations at the positive-going edges or on both negative-going and positive-going edges of the clock pulses.

When the system clock CLK has a negative-going edge while the row address is applied at the clock cycle time 1 and the row address control signal $\overline{RE}$ is low, the row address is latched into the row address buffer **48**.

Since the illustrative embodiment has an N bit wide address bus, that bus is time shared by row addresses and column addresses. During the clock cycle time 2 following the latching of the row address into the row address buffer **48**, a column address is applied to the address bus **45**. While the column address control signal $\overline{CE}$ is low and the write signal $\overline{WE}$ is high at the clock cycle time 2, the system clock goes low, latching the column address into the column address buffer **49**.

Concurrently with the latching of the column address into the column address buffer, the row address is being decoded through the row address decoder **50**. The row address decoder **50** decodes the binary number row address into a one-out-of-2^n selection. As a result of the one-out-of-2^n selection, an active signal is applied to the wordline of the one selected row. This wordline remains selected throughout the remainder of the random access read operation.

At the next negative-going edge of the system clock CLK, a load initial address signal LIA enables a group of load count transfer gates **51** to move the initial column address into upper count and lower count sections of a column address counter **52**. The most significant bits of the column address are latched into the upper count section **58** and the least significant bits of the column address are latched into the lower count section **59** of the column address counter **52**. All of those address bits in the column address counter **52** represent the initial column address to be applied to the memory array for the read out operation. Since the operation being described is a synchronous random access operation, the initial column address is the only column address to be applied to the memory array during the read operation.

The most significant bits of the initial column address are applied from the upper count section 58 through a gate 53 to the column address decoder 54 for selecting M columns of storage cells of the memory array, from which data are to be read out. These most significant bits of the column address are decoded by the column address decoder 54 to enable a block of M columns of storages cells in the memory array 75.

Data bits are read from a group of M storage cells, determined by a part of the decoded column address, i.e., the decoded most significant bits of the column address. These M data bits are transferred in parallel from the memory array 75 through a group of leads 55 to an output multiplexer OMUX where they are latched for output.

A one-out-of-M selection is made by the output multiplexer OMUX in response to control signals applied to the output multiplexer from the lower count section 59 of the column address counter 52. The least significant bits of the initial column address, residing in the lower count section 59, determine which bit latched in the output multiplexer OMUX is the one-out-of-M bit to be gated through the output multiplexer to a lead in the data bus 25.

Referring now to FIGS. 4 and 2 for a synchronous random access write operation, row addressing and column addressing occur similar to the synchronous random access read operation except that the write signal $\overline{WE}$ is at a low level at the clock cycle time 2 to designate the synchronous random access write operation. The decoded row address from the row decoder 50 enables one row oil storage cells in the memory array 75. The most significant bits of the column address, decoded by the column decoder 54, enable a block of M column leads in the array. The selected set of storage cells at the addressed intersections of the addressed row and the set of M addressed columns are enabled to receive the data that is to be written. The least significant bits of the column address (residing in the lower count section 59 of the column address counter 52) determine control signals that are applied to the input multiplexer IMUX for determining which one-out-of-M bit on the data bus 25 is transmitted through the input multiplexer IMUX to be written into the memory array 75. The one-out-of-M bit is applied to the associated column lead of the selected block of columns of storage cells in the memory array 75. That bit of data is written into the storage cell at the address selected by the row address and the initial column address. The other M−1 bits of data, related to the selected set of M columns, are not written into the memory array 75 because the input multiplexer IMUX does not transmit those M−1 bits to the associated column lines of the memory array 75.

The next subsequent operation of the memory array following either the synchronous read operation or the synchronous write operation may be another synchronous random access operation, i.e., either a synchronous read operation or a synchronous write operation. The same row and column addresses or a different row or column address can be used to select the storage cell for the next access. A synchronous burst or a synchronous wrap operation also may follow the synchronous random access read or write operations.

In the foregoing discussion of the synchronous read and write operations, the illustrative embodiment includes an N bit wide address bus 45 that is time-shared by row and column addresses. In another useful embodiment, not shown, the address bus may be wide enough so that both the row and column addresses are applied concurrently in parallel. As a result, both addresses are latched simultaneously into their respective address buffers, i.e., row address buffer 48 and column address buffer 49. Otherwise the synchronous random access read and write operations proceed, as previously described.

It is noted that for the synchronous random access write operations, the row and column addresses may be latched either before data is latched or at the same time.

In addition to the synchronous random access read and write operations, the embodiment of FIGS. 1 and 2 can perform a synchronous burst read operation and a synchronous burst write operation.

In the synchronous burst read operation, a group of bits is read rapidly from a sequence of column addresses along a common row of storage cells in the memory array 75. The sequence of addresses can be either in an ascending order of column addresses (UP) or in a descending order of column addresses (DOWN). The direction, or polarity, of the sequence of column addresses is determined by a burst direction signal +/− on a lead 56. The length of the burst, i.e., the number of bits in the burst, is determined by the duration of the low burst select signal $\overline{BT}$ that is applied, on a lead 57, by the digital processor 20 of FIG. 1. When the burst select signal $\overline{BT}$ goes high, the synchronous burst read operation is terminated.

Generally a synchronous burst read operation is similar to a random access read operation. There are some differences that will become apparent in the subsequent description of the synchronous burst read operation. Similar aspects of the operations are described minimally so that differences can be fully described without excessive redundant description.

Referring now to FIG. 5, there is shown a timing diagram for a synchronous burst read-up operation of the synchronous memory device 30 of FIG. 2. The row address control signal $\overline{RE}$ and the burst select signal $\overline{BT}$ go active low at clock cycle time 1 to commence the operation. The burst direction signal +/− is at a high level to indicate that the sequence of column addresses is an incremented sequence. A row address is latched into the row address buffer 48 at clock cycle time 1. An initial column address is latched into the column address buffer 49 at clock cycle time 2. The write signal $\overline{WE}$ is at a high level to indicate the read operation. The row address is decoded by the row address decoder 50 to select a row of storage cells in the memory array 75. In response to the load initial address signal LIA, the most significant bits of the initial column address are gated through gates 51 into the upper count section 58 of the column address counter 25 while the least significant bits of the same address are gated into the lower count section 59 of the column address counter 52. The most significant bits are decoded in the column address decoder 54 to select two blocks of M columns for read out from the memory array 75. One of those columns is selected for transmitting its bit through the output multiplexer OMUX as the initial bit of the desired sequence of bits on the data bus 25.

Referring now to FIG. 6, there is a detailed block diagram of the upper count section 58 and the lower count section 59 of the column address counter 52. After the initial address is decoded, the upper count and lower count sections of, the column address counter 52 are incremented by a count clock signal COUNT. The upper and lower counters are organized as a continuous series of binary counter stages. As shown in FIG. 2, a gate 51 is provided for transferring the initial column address into the upper count and lower count sections of the column address 52 in response to the load initial address signal LIA. The up or down direction of the column address sequence is determined by the burst direc-

tion signal +/−. A least significant bit counter stage LSB and a most significant bit counter stage MSB are indicated in FIG. 6. The upper count section **58** includes all of the counter stages except the $\log_2(2M)$ least significant bit counter stages which make up the lower count **59**.

In a synchronous burst read-up operation after the initial column address is decoded, the address residing in the upper and lower count sections **58** and **59** is incremented under control of the clock signal COUNT. The next address produced in the upper and lower count sections **58** and **59** is the initial column address incremented by one. The next sequential bit is transmitted through the output multiplexer OMUX from the column of storage cells of the memory thereby addressed.

A first block of M columns and a next adjacent higher order block of M columns of storage of the memory array **75** are addressed simultaneously by the column address decoder **54**. Bits are transmitted through the output multiplexer OMUX from a first one of those blocks while the bits from the second block of M columns are accessed from the memory array and are applied to the output multiplexer OMUX. When the first set of addresses is exhausted, the sequence of addresses continues through the second set of M addresses while a third set of M addresses is applied to the output multiplexer in place of the first set. By thus alternating sets of addresses in a rising order, the desired burst of bits is read out of the memory array **75**. These alternating sets of addresses for selecting the desired sequence of bits enables the data to be read out through the output multiplexer OMUX to the data bus **25** in a continuous stream without having to wait for each address to be supplied from the digital processor **20** of FIG. **1**. The sequential bits of data transmitted out of the output multiplexer OMUX are in a continuous stream at the rate of the system clock CLK.

In the synchronous burst mode, the number of bits of data read out of the memory array depends upon the duration of the low active burst signal $\overline{BT}$ on the lead **57**. When the burst signal $\overline{BT}$ goes high, the synchronous burst read operation is terminated.

A synchronous burst read operation also can be made from memory cells having a sequence of descending column addresses in the memory array **75**. There are a couple of distinctions between this synchronous burst read-down operation and the synchronous burst read-up operation which was just described.

Referring now to FIGS. **7** and **2** for a synchronous burst read-down operation, the only difference in the control signals is that. the burst direction signal +/− is a low level to signify that the count in the upper and lower count sections of the column address counter **52** is decremented in response to each cycle of the counting clock COUNT. Bits from a first set of M addressable columns and from the next adjacent lower order set of M addressable columns are read from the memory array **75** and are applied to the output multiplexer OMUX. Individual bits are transmitted through the output multiplexer in response to a descending sequence of addresses applied to the output multiplexer OMUX from the lower count section **59** by way of a wrap address scrambler **61** and leads **63**. In the synchronous burst operation, the wrap address scrambler allows the address from the lower count section **59** to be transmitted without change to the multiplexer. Since the count in the column address counter is being decremented in response to the clock signal COUNT, the sequence of bits transmitted out through the output multiplexer OMUX is read from columns having a sequence of descending addresses in the memory array **75**.

Blocks of M column addresses are selected by the count in the upper count section **58** of the column address counter **52**. Bits from alternate ones of those sets of column addresses are selected by the addresses of the individual columns, as determined by the count in the lower count section **59** of the column address counter **52**.

FIGS. **8** and **9**, respectively, are alternative timing diagrams for synchronous burst read-up and synchronous burst read-down operations of the synchronous random access memory **30** of FIG. **2**. The difference in the timing diagrams of FIGS. **8** and **9** with respect to the diagrams of FIGS. **5** and **7** is that the write signal $\overline{WE}$ is sampled at the clock cycle time 1 instead of at the clock cycle time 2. Either timing is acceptable for adequate operation of the synchronous random access memory **30**.

The just described synchronous burst read operations (either read-up or read-down) provide the data processing system of FIG. **1** with a capability to read out of a row of the memory array **75** an entire sequence of data bits (a burst) at a rate of one bit per cycle of the system clock CLK for the active duration of the burst signal $\overline{BT}$. A single row address and only the initial column address are forwarded from the digital processor **20** to the synchronous random access memory **30**. The rest of the sequence of column addresses is produced by the column address counter **52** at the rate of a new address for every cycle of the system clock CLK.

Another important operation of the data processing system **15** is a synchronous burst write operation, which enables the digital processor **20** of FIG. **1** to apply a sequence of data bits onto the data bus **25** in consecutive system time slots with a row address and only an initial column address to determine where they are to be stored in the synchronous random access memory **30**. The upper and lower count sections **58** and **59** determine a sequence of column addresses following the initial column address. The sequence of data bits on the data bus **25** is stored in the addressed storage cells of the memory array **75** in synchronism with system clock cycles.

Referring now to FIG. **10**, there is shown a timing diagram of a synchronous burst write-up operation for storing the sequence of data bits into the memory array **75** of FIG. **2**. In such an operation, data bits are stored in storage cells having the same row address and sequential column addresses in ascending order.

As shown in FIG. **10**, the write signal $\overline{WE}$ and the burst signal $\overline{BT}$ are low, and the wrap signal $\overline{WP}$ is held high. Since this is a synchronous burst write-up operation, the burst direction signal +/− is high to produce an ascending sequence of column addresses. Because the row address control signal $\overline{RE}$ is low, the timing and control circuit of FIG. **2** produces the row address latch signal XAL during the system clock cycle time 1. Because the column address control signal $\overline{CE}$ is low during clock cycle **2**, the timing and control circuit produces the column address latch signal YAL during the system clock cycle time 2. The row address and the initial column address are latched into the respective row and column address buffers **48** and **49** to begin the burst write-up operation. The row address is decoded through the row decoder **50**. The initial column address is transferred into the upper and lower count sections of the column address decoder **52**. The most significant bits go into the upper count section **58**, and the least significant bits into the lower count section **59**. Advantageously a sequence of data bits, starting with the first bit on the data bus **25** during the system clock cycle time 2, is latched, one bit at a time, consecutively into an input multiplexer IMUX in synchro-

nism with the system clock CLK. Data bits are applied through the data bus **25** to the data-in driver circuit **64**. A write enable signal WEN, produced by the timing and control circuit **42**, enables data from the data bus **25** to be transferred to the data-in drivers **64**. A data-in latch signal DINL, also produced by the timing and control circuit **42**, latches data from the data bus **25** into the data-in drivers **64**. For the synchronous burst operation, the most significant bits of the initial column address, in the upper count section **58**, are decoded into a selection of two blocks of M columns. Signals from lower count section **59** pass through to the output of the wrap address scrambler **61** and are applied by way of leads **66** to the control inputs of the input multiplexer IMUX for determining which one-out-of-2M bit is transmitted to the associated column of storage cells in the memory array **75**. The least significant bits of the initial column address are decoded into a one-out-of-2M selection for enabling one of the bits, associated with the initial column address, to be transmitted from the data bus **25** through the input multiplexer IMUX to be stored in the memory array **75**. A storage cell located at the intersection of the row address and the initial column address is the first storage location. Each subsequent cycle of the system clock causes the binary count in the combination of the upper and lower count sections of the column address counter **52** to be incremented. The following data bits, selected from the data bus **25** in synchronism with the system clock, are each stored in the sequence in a separate one of the storage calls along the accessed row in the memory array **75**. In response to the clock signal COUNT, the count in the lower count and upper count sections of the column address counter **52** is incremented (because the burst direction signal +/− high) for directing the following data bits from the data bus **25** into sequentially addressed columns of storage cells of the memory array **75**. The burst of data bits and the generation of the ascending sequence of addresses continues until the burst select signal $\overline{BT}$ returns to the high level.

Referring now to FIG. **11**, there is shown a timing diagram for a synchronous burst write-down operation to store data bits into the memory array **75** of FIG. **2**. This operation is similar to the just described synchronous burst write-up operation. Because the row address control signal $\overline{RE}$ is low, the timing and control circuit **42** of FIG. **2** produces the row address latch signal XAL and latches the row address during the system clock cycle time 1. Because the column address control signal $\overline{CE}$ is low during system clock cycle time 2, the timing and control circuit **42** produces the column address latch signal YAL and latches the initial column address during that system clock cycle.

Different, however, than the previously described synchronous burst write-up operation, the burst direction signal +/− is low causing the upper and lower count sections of the column address counter **52** to decrement the address, residing therein, in response to every cycle of the system clock CLK. Thus the sequence of column addresses starts with the initial column address and decreases in sequential order for each subsequent system clock cycle. Data bits from the data bus **25** are directed through the input multiplexer IMUX to be written into storage cells located along a row at columns having sequentially decreasing addresses in the memory array **75**.

FIGS. **12** and **13**, respectively, are alternative timing diagrams for synchronous burst write-up and write-down operations of the synchronous random access memory **30** of FIG. **2**. The difference in the timing diagrams of FIGS. **12** and **13** with respect to the diagrams of FIGS. **10** and **11** is that the write signal $\overline{WE}$ is sampled at the clock cycle time 1 instead of at the clock cycle time 2. Either timing is acceptable for adequate operation of the synchronous random access memory **30**.

The just described synchronous burst write (either write-up or write-down) operations provide the data processing system of FIG. 1 with a capability to write into a row of the memory array **75** an entire sequence of data bits (a burst) at a rate of one bit per cycle of the system clock CLK for the active duration of the burst signal $\overline{BT}$. A single row address and only the initial column address are forwarded from the digital processor **20** to the synchronous random access memory **30**. The rest of the sequence of column addresses is produced by the column address counter circuitry **52** at the rate of one new column address for every cycle of the system clock CLK.

Referring now to FIG. **14**, there is shown a timing diagram of a synchronous wrap read 8-bit operation of the synchronous random access memory of FIG. **2**. From a row of the memory array **75**, eight bits of data are to be read from a single row and from columns selected by the initial column address latched in the upper count section **58** of the column address counter **52**. Row addressing and initial column addressing occur as previously described. Gate **53** is enabled by a wrap control signal WRAP during system clock cycle time 1 for transmitting the initial column address to the column address decoder for reading out data from the columns of the memory array **75**. Such data is directed through the output multiplexer OMUX in response to a selection made by the least significant bits of the initial column address latched in the lower count section **59** of the column address counter **52**, as modified by a subsequent conversion. The least significant bits of the initial column address are converted into a sequence of addresses generated by the wrap address scrambler and multiplexer **61**.

FIG. 15 is TABLE I showing the logic of the conversion process that is accomplished by the wrap address scrambler and multiplexer. As shown in TABLE I, the wrap length signal WL is zero (WL=0). Headings for the columns of the table include, as an input, the three least significant bits of the initial column address A0, A1, A2. The wrap type signal WT may be either low (WT=0) or high (WT=1). Each line of the truth table presents a sequence of output addresses which are produced by the wrap address scrambler **61** in response to the three least significant bits from the initial column address residing in the column address counter **52**. The wrap address scrambler **61** produces the sequence for which ever wrap type WT is applied in synchronism with the system clock signal CLK.

Thus in the top line for wrap type signal WT equal to zero (WT=0) and initial address A0=0, A1=0, A2=0, the sequence of addresses produced by the wrap address scrambler is 0,1,2,3,4,5,6,7. The translation from the initial input address to the output sequence of address may be accomplished in a number of ways, e.g., by a look-up table. Output addresses from the wrap address scrambler **61** access similarly ordered outputs from the output multiplexer OMUX. Since only eight bits are latched into the output multiplexer, only eight addresses are produced and used for reading those bits to the data bus **25**.

If the wrap type signal equals (WT=1), then the sequence of addresses occurs in the order shown in the right most column. Thus when the wrap type signal WT=1 and the least significant three bits of the initial column address are A0=0, A1=1, A2=0, the order of addresses applied to the output multiplexer is 2,3,0,1,6,7,4,5. Bits from output multiplexer positions, so identified, are read out in that order onto the data bus **25** of FIG. **2**.

Referring now to FIGS. **16** and **17**, there is shown a timing diagram and a truth table for a synchronous wrap read operation that reads out four bits rather than the eight bits read out during the operation represented by FIGS. **14** and **15**. For the four bit wrap read operation, the wrap length signal equals (WL=1). Since there are only four bits to be read through the output multiplexer, only the two least significant initial column address bits A0 and A1 are applied to select the order of output. Selection of the wrap type is made by the state of the wrap type signal WT to determine the order of addresses for reading out of the output multiplexer onto the data bus **25**. The wrap address scrambler and multiplexer **61** converts the least significant two bits of the initial column address into the desired wrap sequence in accordance with the TABLE II presented in FIG. **17**.

The just described synchronous wrap read (either 8-bit or 4-bit) operations provide the data processing system of FIG. **1** with a capability to read from a row of the memory array **75** a group of data bits in an order prescribed by the column address of the first bit accessed. The group of bits is read out at a rate of one bit per cycle of the system clock CLK until the selected eight bits or four bits are read out. A single row address and only the initial column address are forwarded over the address bus from the digital processor **20** to the synchronous random access memory **30**. The rest of the group of column addresses is produced by the column address counter circuitry **52** and the wrap address scrambler and multiplexer **61** at a rate of a new column address for every cycle of the system clock CLK.

A similar synchronous wrap write operation is enabled by applying a low active write signal $\overline{WE}$ to commence the operation.

Referring once again to FIG. **6**, an initial column address is applied in parallel to and is latched into the stages of the column address counter **52**. The burst direction signal +/− is applied to all of the stages to determine whether the count is incremented or decremented in response to each cycle of the clock signal COUNT. The clock signal COUNT also is applied to all stages. Each stage of the column address counter **52** is interconnected with the adjacent stages on both sides. There is a connection path for incrementing the count and a separate path between each pair of adjacent stages for decrementing the count.

FIG. **18** shows one stage K of the column address counter **52** in greater detail. At the top of stage K, there are two terminals that are interconnected with the next higher order stage K+1 of the column address counter **52**. Carry-out decrement terminal CO− and carry-in decrement terminal CI− are connected with the adjacent stage K+1. At the bottom of stage K, there are two terminals connected with the next lower order stage K−1. A carry-in increment terminal CI+ and carry out increment terminal CO+ are interconnected with the adjacent stage K−1. The initial address data is applied to the data input terminal D. The burst direction signal +/− is applied to the increment/decrement terminal +/−. The clock signal COUNT is applied to a clock input terminal C, and output addresses (to be forwarded to the memory array **75** and the input and output multiplexers) occur at the output terminal Q.

Referring once again to FIG. **6**, the wrap address scrambler **73** has three inputs **74** received from the lower count section **59** of the column address counter **52**.

In FIG. **6** for synchronous random access and synchronous burst operations, those three inputs are transmitted directly to three outputs **76**, **77** and **78**. Outputs **77** and **78** are applied directly to control the input multiplexer IMUX and the output multiplexer OMUX. The output **76** is applied to a multiplexer **74** which for the synchronous burst operation transmits the signal to the input and output multiplexers IMUX and OMUX. For synchronous random access and synchronous burst operations, the least significant bits of the count in the column address counter **52** are applied directly to control the input and output multiplexers.

For synchronous wrap operations, the wrap address scrambler **73** and the multiplexer **74** convert the least significant bits of the column address to the desired sequence of addresses for reading bits from the input and output multiplexers IMUX and OMUX. The wrap length signal WL is active all of the time except for a four bit wrap length. Then the wrap length signal WL cuts off the signal on the lead **76** so that the two leads **77** and **78** apply address bits from the column address counter and the multiplexer **74** applies a zero to the input and output multiplexers IMUX and OMUX. The wrap address scrambler produces the desired sequences of bits on the leads **77** and **78**, in accordance with TABLES I and II.

In FIG. **2**, the mask register **93** receives and stores coded mask data from the data bus **25**. Responsive to the system clock signal CLK, the mask register **93** applies the mask data to control the operation of the count control circuit **94**.

Count control circuit **94**, in response to the status of the burst control signal BURST, the wrap control signal WRAP, the mask data, and the system clock CLK, produces the clock signal COUNT for controlling the operation of the column address counter **52** and the wrap address scrambler and multiplexer **61**.

Timing and control circuit **42** of FIG. **2** is responsive to the row address control signal $\overline{RE}$, the column address control signal $\overline{CE}$, the write signal $\overline{WE}$, the burst signal $\overline{BT}$, the burst direction signal +/−, the wrap select signal $\overline{WP}$, the wrap-type signal WT, the wrap-length signal WL, and the system clock signal CLK for producing control signals, such as, the row and column address latching signals XAL and YAL, the latch initial address signal LIA, the write enable signal WEN, the data-in latch signal DINL, the burst control signal BURST, and the wrap control signal WRAP.

In the timing and control circuit **42** of FIG. **2**, all of the signals from the control bus **60** are gated by the system clock signal CLK on lead **67** so that all control signals internal to the synchronous random access memory **30**, such as, the signals XAL, YAL, LIA, WEN, DINL, BURST and WRAP are synchronized directly with the system clock signal CLK. This feature assures that the functions of the synchronous random access are synchronized with that clock. Any logic circuitry external to the synchronous random access memory **30** need not be concerned with any complex timing relationships between the various signals transmitted on the control bus **60**.

Referring now to FIG. **19**, there is shown an exemplary gate **101** of the timing and control circuit **42** of FIG. **2**. In FIG. **19**, the row address control signal $\overline{RE}$ is gated by the system clock signal CLK, i.e., sampled on the negative-going edge of the pulses of the system clock CLK. The resulting output of the gate **101** is t h e row address latch signal XAL.

FIG. **20** is a timing diagram for the operation of the gate **101**. As shown i n FIG. **20**, the output row address latch signal XAL is activated by the negative-going edge of the system clock CLK at the system clock cycle time 2 when the row address control signal $\overline{RE}$ is low. The timing of the negative-going edge of the row address control signal is irrelevant, as long as the level of that signal is low at the negative-going edge of the system clock signal CLK.

Similarly, all of the other internal control signals are responsive to sampled levels of the external control signals on the control bus **60** at times of the negative-going edges of the system clock signal CLK.

Referring now to FIG. **21**, there is shown an exemplary circuit **102** which is responsive to the burst control signal BURST, the wrap control signal WRAP, and the system clock signal within the count control block **94** of FIG. **2** CLK, for producing the count clock signal COUNT. In FIG. **21**, the active high signals BURST and WRAP are applied as inputs to an OR gate **103** to produce a signal COUNT ENABLE for gating the system clock signal. A gate **104** is enabled for transmitting the system clock signal CLK when either the burst control signal BURST or the wrap control signal WRAP is active high.

The timing and control circuit **42** of FIG. **2** produces the burst control signal BURST and wrap control signal WRAP. The burst control signal BURST and the wrap control signal WRAP are normally low and go high active. The initial edges of the burst control signal BURST and the wrap control signal WRAP are aligned with negative-going edges of the system clock signal CLK. Once the burst control signal BURST and the wrap control signal WRAP are activated, they remain active for the duration of their respective operations.

The count clock signal COUNT is a clock pulse sequence synchronized with the system clock CLK and lasting while either the signal BURST or the signal WRAP is active. Pulses of the count clock signal COUNT either increment or decrement the column address residing in the column address counter **52** depending upon the state of the burst direction signal +/−.

Referring now to FIG. **22**, the timing diagram shows an exemplary operation of the count signal gate arrangement **102** of FIG. **21**. The internal control signal COUNT ENABLE goes high active before the system clock cycle time 2 and stays high active until after the system clock cycle time 3. As a result of gating the system clock signal CLK through the gate **104** of FIG. **21** under control of the control signal COUNT ENABLE, the resulting count clock signal COUNT is gated to produce pulses at cycle times 2 and 3 in synchronism with the system clock signal CLK.

Referring now to FIG. **23**, there is shown a block diagram of the output multiplexer OMUX and the input multiplexer IMUX arranged with selection and gating circuits for controlling transfer of data bits read out from the memory array **75** to the data bus **25** and for controlling transfer of data bits to be written from the data bus **25** to the memory array **75**.

With respect to FIG. **23**, the column address decoder **54** of FIG. **2** selects two blocks of four columns by enabling two gates in block gating circuit **110**. Each lead into and out of the block gating circuit represents four leads for a block of data. Every other block of data, i.e., the even order blocks, is connected by way of an even order bus **116** to an output enable gate **120**, which is includes a separate gate for each bit lead and is operated by the complement of the write enable signal WEN. Odd order blocks from the memory array **75** are connected by way of an odd order bus **122** also to the output enable gate **120**. The output enable gate **120** is connected to eight separate output registers **124** for storing individual data bits read out from the memory array **75**.

In FIG. **23**, converter circuit **126** converts the three least significant bits of the column address from the wrap address scrambler and multiplexer **61** into a one-out-of-eight selection code, which is applied to an output transfer selection gate circuit **128**. For each of the eight output registers **124**, there is an output transfer selection gate controlled by a separate one of the one-out-of-eight selection code, which is applied to control the output transfer selection gate circuit **128**. The output transfer selection gates **128** are operated one at a time to allow a data bit to be transmitted from its output register to the data bus **25** in synchronism with the system clock.

Continuing to refer to FIG. **23**, for burst read-up operation of the input and output multiplexers, the column address in the column address counter **52** of FIG. **2** is incremented in response to the clock signal COUNT. Every fourth cycle of the clock signal COUNT, the two column address decoder output signals step up one order of sets, e.g., from n and n+1 to n+1 and n+2. This disables one of two previously open gates and enables one previously open gate and a new gate **110**. Data bits stored in four of the output registers **124** thereby are changed to a new block of data to be read out to the data bus **25**. Thus, the set of four of the output registers **124** exhausted of data is replenished with new data because the next higher order set of column addresses from the memory array **75** is enabled to transfer data into the exhausted output registers **124**.

With respect to FIG. **23** for a burst read-down operation, the output multiplexer OMUX operates, as just described, except that the order of addresses applied to the column address decoder **54** is decrementing. Thus every fourth cycle of the clock signal COUNT, the two enabled blocks of data are the two next lower order blocks of data, e.g., from column sets n and n−1 to n−1 and n−2.

Further with respect to FIG. **23** for a wrap read operation, the output multiplexer OMUX operates similar to the previously described burst read-up operation until the initial address selection is completed. Eight data bits are read out of the memory array and are latched into the eight output register circuits **124**. Thereafter their order of readout to the data bus **25** is determined by two factors. The first and second factors are the wrap length signal WL and the wrap type signal WT. As previously mentioned, combinations of those two signals WL and WT cause the wrap address scrambler **73** of FIG. **6** to produce a series of enabling signal codes for the output gates **128** of the output multiplexer OMUX. In response to that series of enabling signal codes, corresponding bits from the output registers **124** are read out through the output transfer selection gates **128** in the selected order onto the data bus **25**.

In FIG. **23**, a somewhat similar arrangement is provided in the input multiplexer IMUX for writing data from the data bus **25** into the memory array **75**. Input transfer selection gates **130** are selectively enabled by the one-out-of-eight code from the wrap address scrambler and multiplexer **61**. The bits are stored in separate input register circuits **132**. The stored data bits are transferred in blocks of four bits to even and odd order blocks of columns of the memory array **75** as the upper count portion of the column address is either incremented or decremented in response to the clock signal COUNT.

Referring now to FIG. **24**, there is shown a data processing system **215** including a digital processor **220**, which is similar to the data processing system **15** of FIG. **1** except that the system clock **65** produces a clock signal that is applied over a lead **221** to the digital processor **220**. Within the digital processor **220**, the clock signal is gated or otherwise manipulated into a processor clock signal that is applied by way of a lead **222** to the synchronous memory **30**, the input peripheral device **24**, and the output peripheral device **40**. Otherwise the data processing system **215** operates like the

data processing system **15** which was described with respect to FIGS. **1** and **2**.

The foregoing describes some data processing system arrangements which represent illustrative embodiments of the invention. Those embodiments and others made obvious in view thereof are considered to fall within the scope of the appended claims.

What is claimed is:

1. A data processing system comprising:
 - a digital processor;
 - a system clock circuit for producing a system clock signal for controlling operation of the digital processor;
 - a synchronous random access memory, responsive to the system clock signal, for accessing addressable storage cells within the synchronous memory to write data into the storage cells and to read out data from the storage cells; and
 - the synchronous random access memory receiving a first address signal for accessing the storage cells within the synchronous random access memory, responsive to the system clock signal, the synchronous random access memory comprising:
   - a timing and control circuit for producing a first address control signal and a first data control signal;
   - an addressing circuit for latching the first address signal, responsive to the first address control signal and a first clock cycle of the system clock signal; and
   - an output circuit for producing a predetermined number of data bits from the storage cells, responsive to the system clock signal, wherein the first data control signal selects the predetermined number of data bits and the output circuit produces a first datum bit of the predetermined number of data bits, responsive to another clock cycle of the system clock signal.

2. A data processing system, in accordance with claim **1**, wherein the addressing circuit further comprises:
 - row address circuitry, responsive to the first address signal, for accessing a row of the addressable storage cells to write data in or to read data out of the synchronous memory;
 - an address counter circuit for receiving a second address signal, the address counter circuit producing an output address signal, responsive to the system clock signal; and
 - column address circuitry, responsive to the output address signal, for accessing a block of columns of the addressable storage cells to write data in or to read data out of the synchronous memory.

3. A data processing system, in accordance with claim **2**, wherein the addressing circuit latches the second address signal, responsive to a second address control signal and a second clock cycle of the system clock signal, the second clock cycle following the first clock cycle.

4. A data processing system, in accordance with claim **3**, wherein the address counter circuit produces the output address signal by incrementing the second address signal, responsive to the system clock signal.

5. A data processing system, in accordance with claim **3**, wherein the timing and control circuit further determines an order of the predetermined number of data bits in response to a second data control signal.

6. A data processing system, in accordance with claim **5**, wherein the order of the predetermined number of data bits is by sequential column address.

7. A data processing system, in accordance with claim **5**, wherein the order of the predetermined number of data bits is by interleaved wrap sequence.

8. A data processing system, in accordance with claim **5**, wherein the first address control signal is produced in response to a row enable signal, and the second address control signal is produced in response to a column enable signal.

9. A data processing system, in accordance with claim **5**, wherein the another clock cycle is two clock cycles after the second clock cycle.

10. A data processing system, in accordance with claim **1**, wherein the storage cells are dynamic storage cells.

11. A data processing system, in accordance with claim **10**, wherein the predetermined number of data bits is 4.

12. A synchronous random access memory comprising:
 - an array of storage cells arranged in addressable rows and columns;
 - a timing and control circuit for receiving a system clock signal and producing a first address control signal and a first data control signal;
 - an addressing circuit for receiving a first address signal for accessing the storage cells within the synchronous random access memory, the addressing circuit latching the first address signal, responsive to the first address control signal and a first clock cycle of the system clock signal; and
 - an output circuit for producing a predetermined number of data bits from the storage cells, responsive to the system clock signal, wherein the first data control signal selects the predetermined number of data bits and the output circuit produces a first datum bit of the predetermined number of data bits, responsive to another clock cycle of the system clock signal.

13. A synchronous random access memory, in accordance with claim **12**, wherein the storage cells are dynamic storage cells.

14. A synchronous random access memory as in claim **13**, wherein the predetermined number of data bits is 4.

15. A synchronous random access memory, in accordance with claim **13**, wherein the predetermined number of data bits is 8.

16. A synchronous random access memory, in accordance with claim **13**, wherein the addressing circuit further comprises:
 - a row decoding circuit for selecting a row of the storage cells, responsive to the first address signal;
 - an address counter circuit for receiving a second address signal, the address counter circuit producing an output address signal, responsive to the system clock signal; and
 - a column decoding circuit for selecting a column of the storage cells from the row of the storage cells, responsive to the output address signal.

17. A synchronous random access memory in accordance with claim **16**, wherein the addressing circuit latches the second address signal, responsive to a second address control signal and a second clock cycle of the system clock signal, the second clock cycle following the first clock cycle.

18. A synchronous random access memory in accordance with claim **17**, wherein the address counter circuit produces the output address signal by incrementing the second address signal, responsive to the system clock signal.

19. A synchronous random access memory, in accordance with claim **17**, wherein the timing and control circuit further determines an order of the predetermined number of data bits in response to a second data control signal.

20. A synchronous random access memory, in accordance with claim **19**, wherein the order of the predetermined number of data bits is by sequential column address.

21. A synchronous random access memory, in accordance with claim 19, wherein the order of the predetermined number of data bits is by interleaved wrap sequence.

22. A synchronous random access memory, in accordance with claim 19, wherein the first address control signal is produced in response to a row enable signal, and the second address control signal is produced in response to a column enable signal.

23. A synchronous random access memory, in accordance with claim 19, wherein the another clock cycle is two clock cycles after the second clock cycle.

24. A synchronous random access memory, in accordance with claim 12, wherein the first address signal includes a first and a second group of address bits.

25. A synchronous random access memory, in accordance with claim 24, wherein the addressing circuit further comprises:

a row decoding circuit for selecting a row of the storage cells, responsive to the first group of address bits;

an address counter circuit for receiving the second group of address bits, the address counter circuit producing an output address signal, responsive to the system clock signal; and

a column decoding circuit for selecting a column of the storage cells from the row of the storage cells, responsive to the output address signal.

26. A synchronous random access memory, in accordance with claim 25, wherein the address counter circuit produces the output address signal by incrementing the second group of address bits.

27. A synchronous random access memory, in accordance with claim 25, wherein the predetermined number of data bits is 4.

28. A synchronous random access memory, in accordance with claim 25, wherein the predetermined number of data bits is 8.

29. A synchronous random access memory, in accordance with claim 25, wherein the timing and control circuit further determines an order of the predetermined number of data bits in response to a second data control signal.

30. A synchronous random access memory, in accordance with claim 29, wherein the order of the predetermined number of data bits is by sequential column address.

31. A synchronous random access memory, in accordance with claim 29, wherein the order of the predetermined number of data bits is by interleaved wrap sequence.

32. A synchronous random access memory, in accordance with claim 29, wherein the another clock cycle is two clock cycles after the first clock cycle.

33. A synchronous random access memory, in accordance with claim 29, wherein the storage cells are static storage cells.

34. A data processing system comprising

a digital processor;

a system clock circuit for producing a system clock signal for controlling operation of the digital processor, the system clock signal having a sequence of periodic clock cycles; and

a synchronous dynamic random access memory, responsive to the system clock signal, receiving a first and a second address signal for accessing addressable storage cells within the synchronous dynamic random access memory, the synchronous dynamic random access memory comprising:

a timing and control circuit for producing a first address control signal and a first data control signal;

a row decoding circuit for selecting a row of the storage cells, responsive to the first address signal;

an address counter circuit for receiving the second address signal, the address counter circuit producing an output address signal, responsive to the system clock signal; and

a column decoding circuit for selecting a column of the storage cells from the row of the storage cells, responsive to the output address signal; and

an output circuit for producing a plurality of data bits from the storage cells, responsive to the system clock signal, the plurality of data bits having an order determined by the first data control signal, the output circuit producing a first datum bit of the plurality of data bits, responsive to another clock cycle of the system clock signal.

35. A data processing system, in accordance with claim 34, wherein the address counter circuit latches the second address signal, responsive to a second address control signal and a second clock cycle of the system clock signal, the second clock cycle following a first clock cycle.

36. A data processing system as in claim 35, wherein the output circuit produces a predetermined number of data bits from the storage cells, responsive to a second data control signal from the timing and control circuit and the system clock signal.

37. A synchronous random access memory comprising:

an array of addressable storage cells;

a timing and control circuit for receiving a system clock signal and producing a first address control signal and a first data control signal;

an addressing circuit for receiving a first address signal for accessing the storage cells within the synchronous random access memory, the addressing circuit latching the first address signal, responsive to the first address control signal and a first clock cycle of the system clock signal; and

an output circuit for producing a plurality of data bits from the storage cells, responsive to the system clock signal, the plurality of data bits having an order determined by the first data control signal, the output circuit producing a first datum bit of the plurality of data bits, responsive to another clock cycle of the system clock signal.

38. A synchronous random access memory, in accordance with claim 37, wherein the storage cells are dynamic storage cells.

39. A synchronous random access memory as in claim 38, wherein the order of the plurality of data bits is by sequential column address.

40. A synchronous random access memory, in accordance with claim 38, wherein the order of the plurality of data bits is by interleaved wrap sequence.

41. A synchronous random access memory as in claim 38, wherein the addressing circuit further comprises:

a row decoding circuit for selecting a row of the storage cells, responsive to the first address signal;

an address counter circuit for receiving a second address signal, the address counter circuit producing an output address signal, responsive to the system clock signal; and

a column decoding circuit for selecting a column of the storage cells from the row of storage cells, responsive to the output address signal.

42. A synchronous random access memory as in claim 41, wherein the addressing circuit latches the second address signal, responsive to a second address control signal and a

second clock cycle of the system clock signal, the second clock cycle following the first clock cycle.

43. A synchronous random access memory as in claim **42**, wherein the address counter circuit produces the output address signal by incrementing the second address signal, responsive to the system clock signal.

44. A synchronous random access memory as in claim **42**, wherein the first address control signal is produced in response to a row enable signal and the system clock signal, and the second address control signal is produced in response to a column enable signal and the system clock signal.

45. A synchronous random access memory as in claim **42**, wherein the another clock cycle is two clock cycles after the second clock cycle.

46. A synchronous random access memory as in claim **37**, wherein the first address signal includes a first and a second group of address bits.

47. A synchronous random access memory as in claim **46**, wherein the addressing circuit further comprises:

a row decoding circuit for selecting a row of the storage cells, responsive to the first group of address bits;

an address counter circuit for receiving the second group of address bits, the address counter circuit producing an output address signal, responsive to the system clock signal; and

a column decoding circuit for selecting a column of the storage cells from the row of the storage cells, responsive to the output address signal.

48. A synchronous random access memory as in claim **47**, wherein the address counter circuit produces the output address signal by incrementing the second group of address bits.

49. A synchronous random access memory as in claim **47**, wherein the order of the plurality of data bits is by sequential column address.

50. A synchronous random access memory as in claim **47**, wherein the order of the plurality of data bits is by interleaved wrap sequence.

51. A synchronous random access memory as in claim **47**, wherein the another clock cycle is two clock cycles after the first clock cycle.

52. A synchronous random access memory as in claim **47**, wherein the storage cells are static storage cells.

53. A data processing system comprising:

a digital processor;

an input peripheral device interconnected with the digital processor;

an output peripheral device interconnected with the digital processor;

a system clock circuit, producing a system clock signal, for controlling operation of the digital processor, the input peripheral device, and the output peripheral device; and

a synchronous dynamic random access memory including an array of addressable storage cells;

a timing and control circuit for receiving the system clock signal and producing a first address control signal and a first data control signal;

an addressing circuit for receiving a first address signal for accessing the storage cells within the synchronous dynamic random access memory, the addressing circuit latching the first address signal, responsive to the first address control signal and a first clock cycle of the system clock signal; and

an output circuit for producing a predetermined number of data bits from the storage cells, responsive to the system clock signal, wherein the first data control signal selects the predetermined number of data bits and the output circuit produces a first datum bit of the predetermined number of data bits, responsive to another clock cycle of the system clock signal.

54. A data processing system as in claim **53**, wherein the predetermined number of data bits have an order determined by a second data control signal.

55. A data processing system as in claim **54**, wherein the input peripheral device is coupled to the digital processor by a first data bus.

56. A data processing system as in claim **55**, wherein the synchronous dynamic random access memory is coupled to the digital processor by a second data bus.

57. A data processing system as in claim **56**, wherein the output peripheral device is coupled to the digital processor by a third data bus.

58. A data processing system comprising:

a digital processor;

an input peripheral device interconnected with the digital processor;

an output peripheral device interconnected with the digital processor;

a system clock circuit, producing a system clock signal for controlling operation of the digital processor, the digital processor producing a gated clock signal for controlling operation of the input peripheral device and the output peripheral device; and

a synchronous dynamic random access memory including an array of addressable storage cells;

a timing and control circuit for receiving the system clock signal and producing a first address control signal and a first data control signal;

an addressing circuit for receiving a first address signal for accessing the storage cells within the synchronous dynamic random access memory, the addressing circuit latching the first address signal, responsive to the first address control signal and a first clock cycle of the system clock signal; and

an output circuit for producing a predetermined number of data bits from the storage cells, responsive to the system clock signal, wherein the first data control signal selects the predetermined number of data bits and the output circuit produces a first datum bit of the predetermined number of data bits, responsive to another clock cycle of the system clock signal.

59. A data processing system as in claim **58**, wherein the predetermined number of data bits have an order determined by a second data control signal.

60. A data processing system as in claim **59**, wherein the input peripheral device is coupled to the digital processor by a first data bus.

61. A data processing system as in claim **60**, wherein the synchronous dynamic random access memory is coupled to the digital processor by a second data bus.

62. A data processing system as in claim **61**, wherein the output peripheral device is coupled to the digital processor by a third data bus.

63. A data processing system comprising

a digital processor;

a system clock circuit for producing a system clock signal for controlling operation of the digital processor, the system clock signal having a sequence of periodic clock cycles; and

a synchronous random access memory, responsive to the system clock signal, receiving a first address signal for

accessing addressable storage cells within the synchronous random access memory, the synchronous random access memory comprising:

a timing and control circuit for producing a first address control signal and a first data control signal;

an addressing circuit for latching the first address signal, responsive to the first address control signal and a first clock cycle of the system clock signal; and

an output circuit for producing a plurality of data bits from the storage cells, responsive to the system clock signal, the plurality of data bits having an order determined by the first data control signal, the output circuit producing a first datum bit of the plurality of data bits, responsive to another clock cycle of the system clock signal.

64. A data processing system, in accordance with claim **63**, wherein the first address signal includes a first and a second group of address bits.

65. A data processing system as in claim **64**, wherein the addressing circuit further comprises:

a row decoding circuit for selecting a row of the storage cells, responsive to the first group of address bits;

an address counter circuit for receiving the second group of address bits, the address counter circuit producing an output address signal, responsive to the system clock signal; and

a column decoding circuit for selecting a column of the storage cells from the row of storage cells, responsive to the output address signal.

66. A data processing system as in claim **65**, wherein the address counter circuit produces the output address signal by incrementing the second group of address bits.

67. A data processing system as in claim **63**, wherein the order of the plurality of data bits is by sequential column address.

68. A data processing system as in claim **63**, wherein the order of the plurality of data bits is by interleaved wrap sequence.

69. A data processing system as in claim **63**, wherein the another clock cycle is two clock cycles after the first clock cycle.

70. A data processing system as in claim **63**, wherein the storage cells are static storage cells.

71. A data processing system as in claim **63**, wherein the output circuit produces a predetermined number of data bits from the storage cells, responsive to a second data control signal from the timing and control circuit and the system clock signal.

* * * * *

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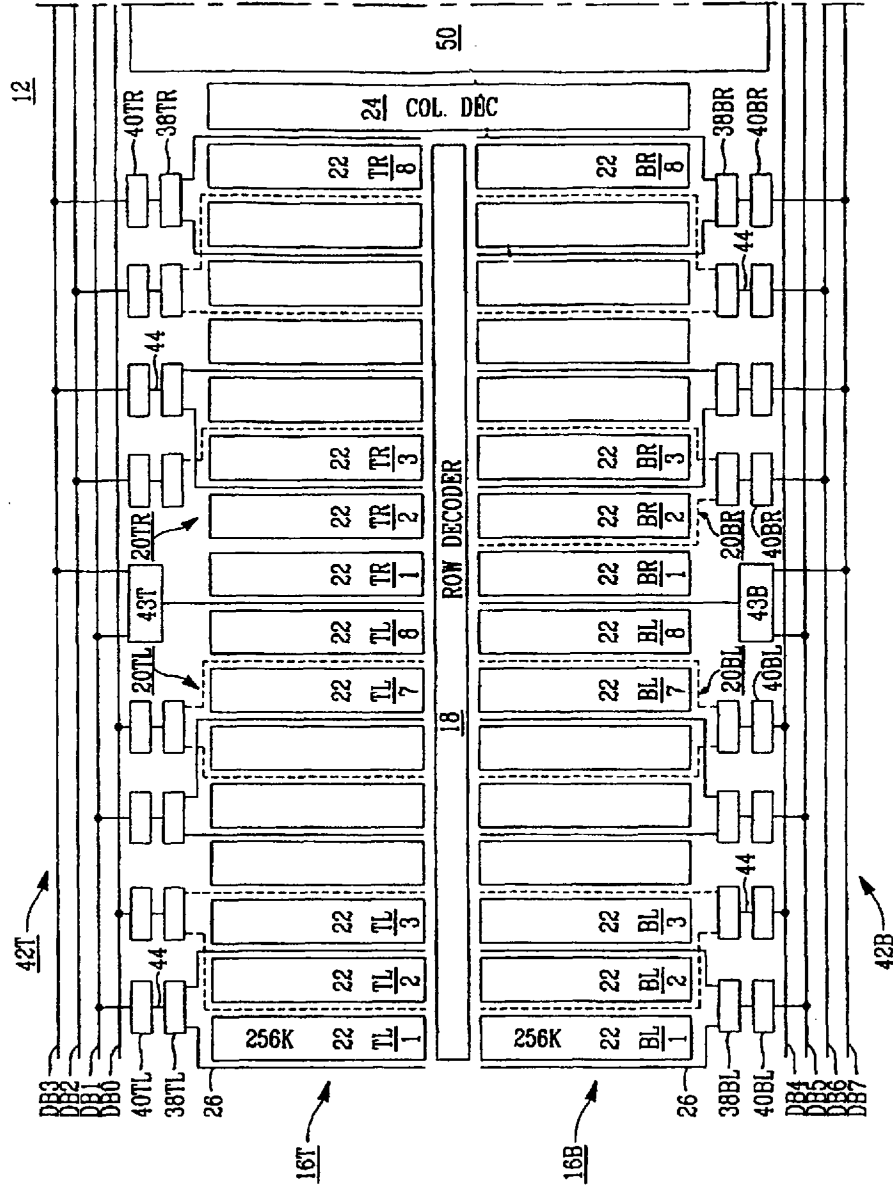

FIG. 1A

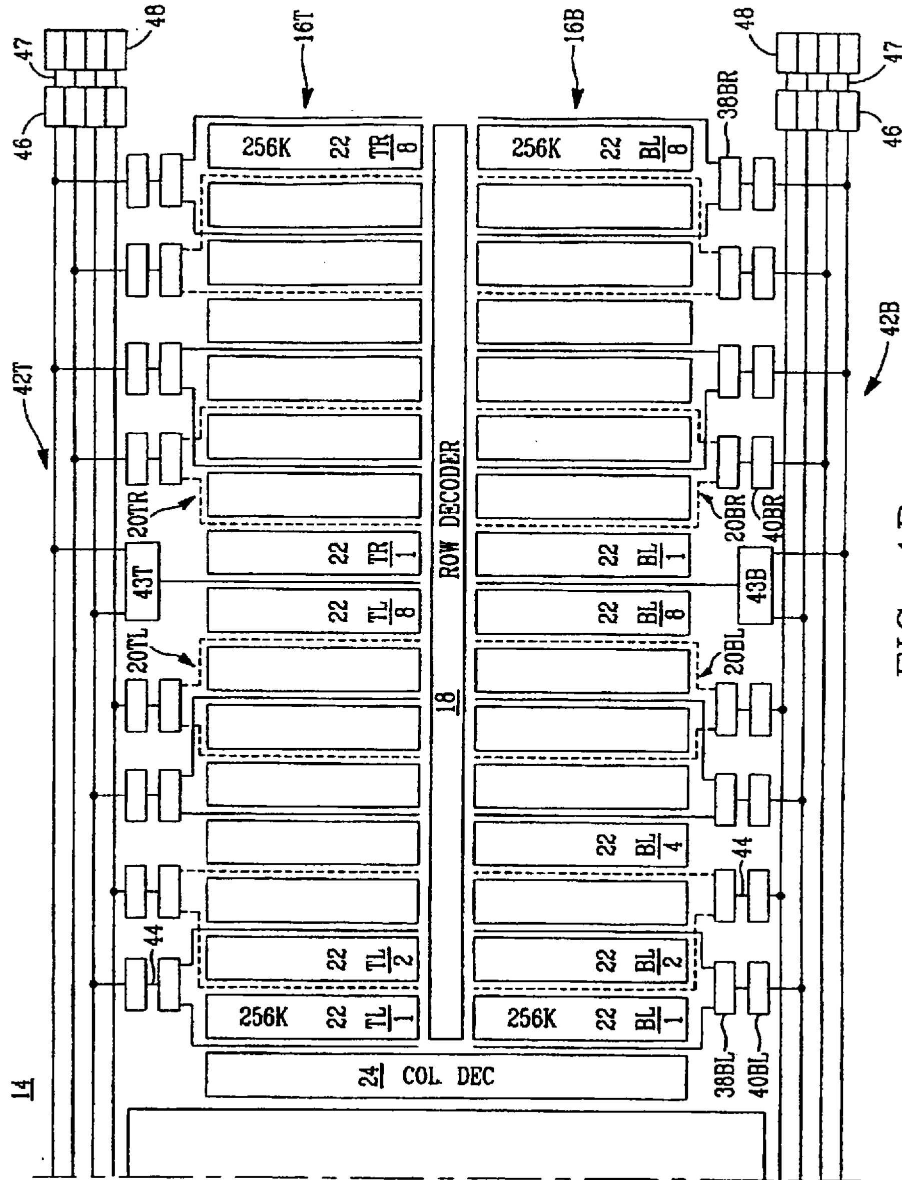

FIG. 1B

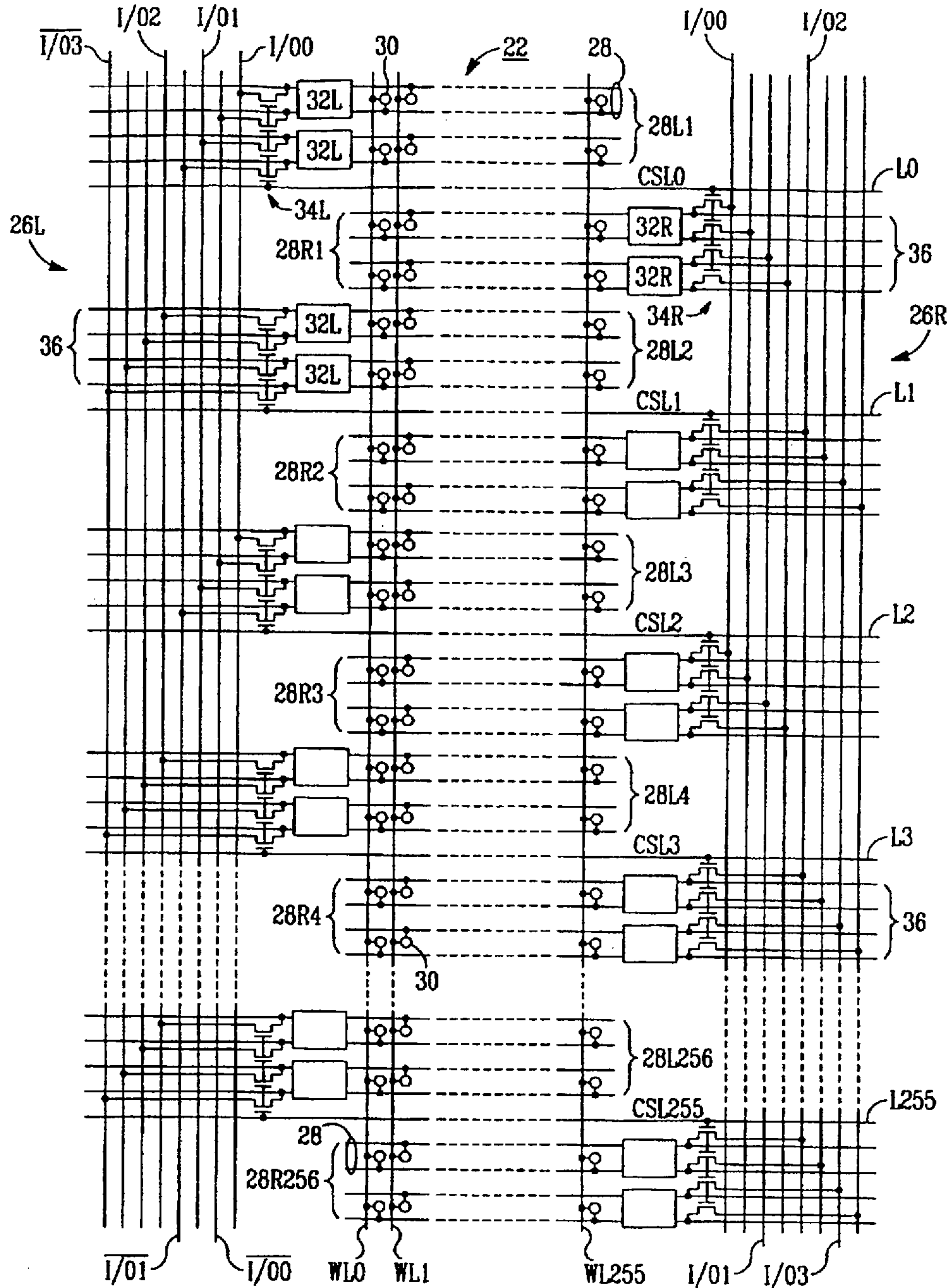

FIG. 2

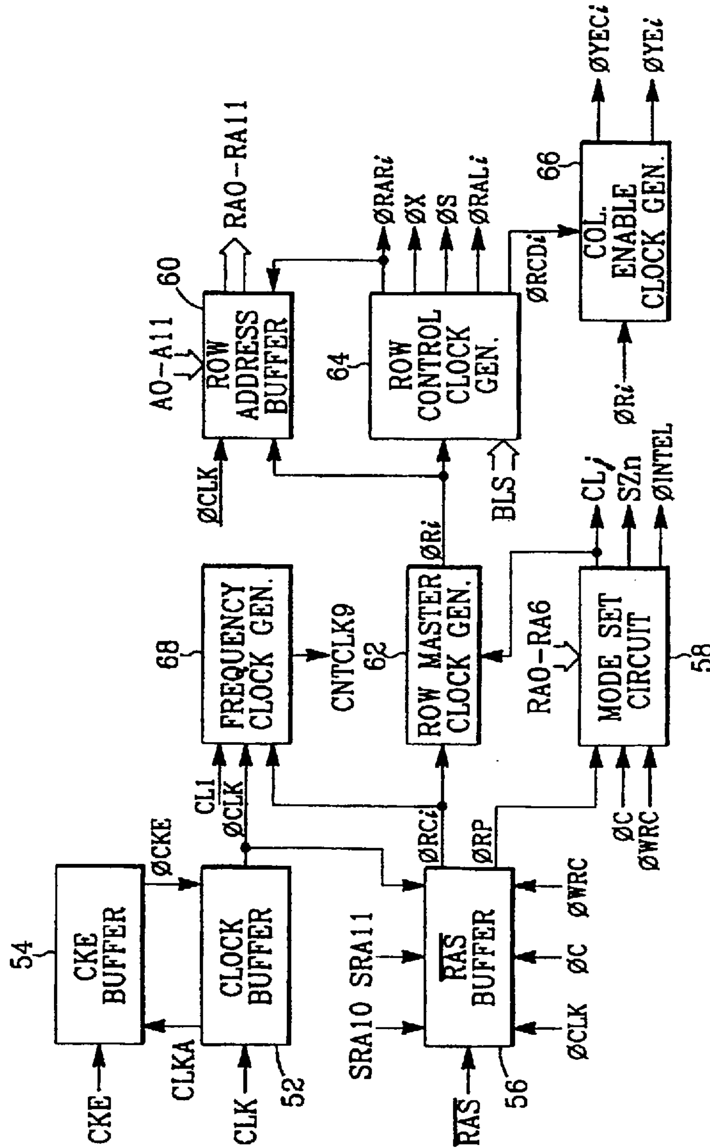

FIG. 3

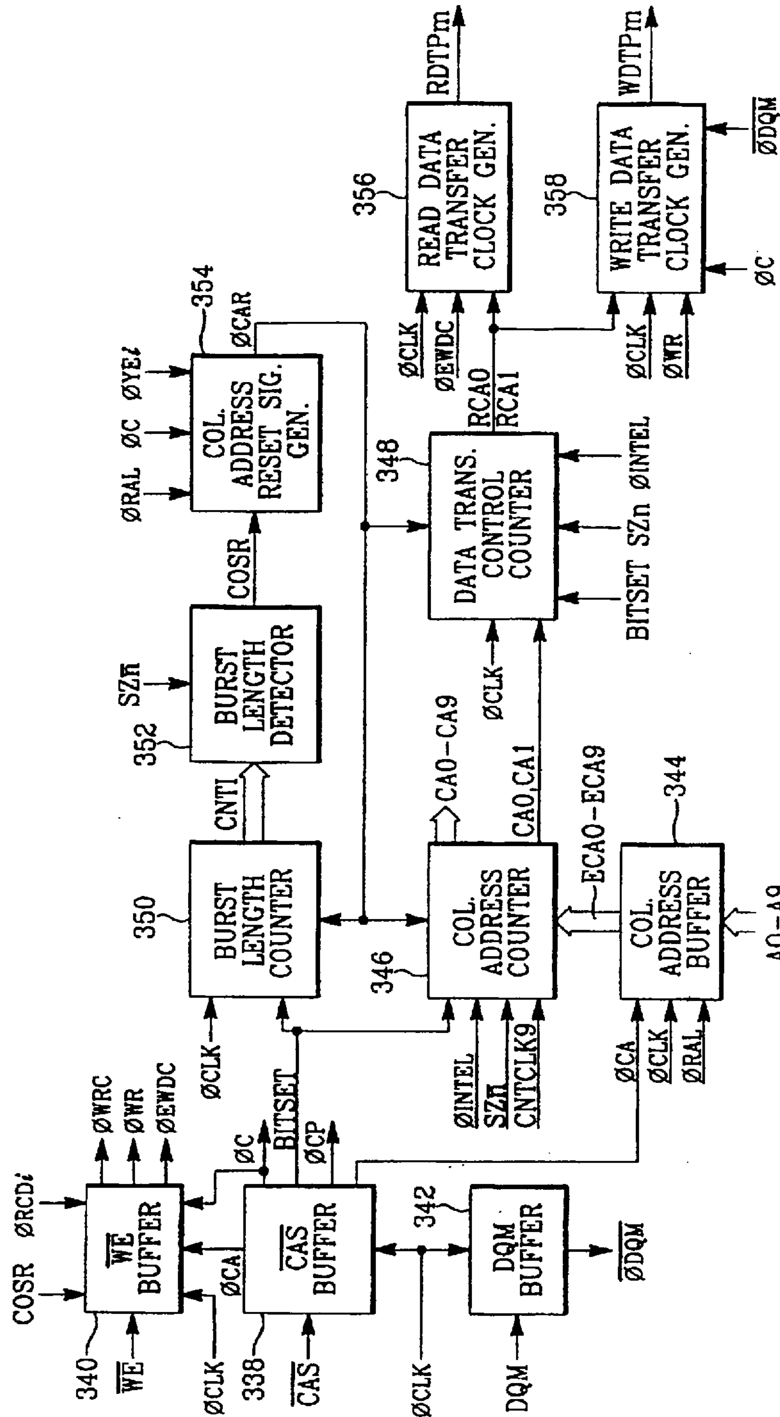

FIG. 4

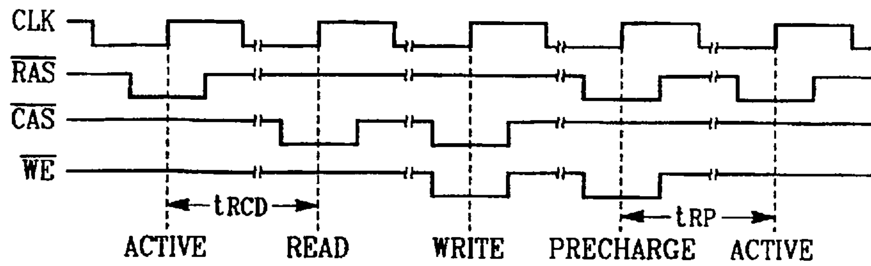

FIG. 5A

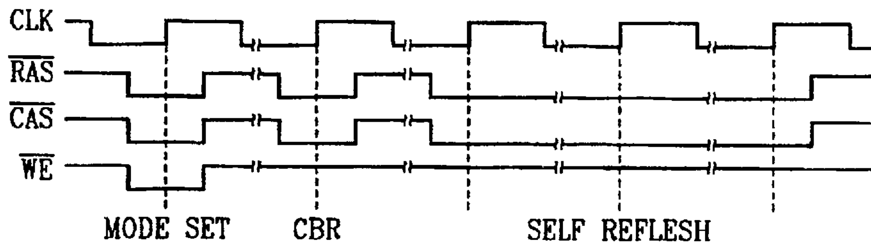

FIG. 5B

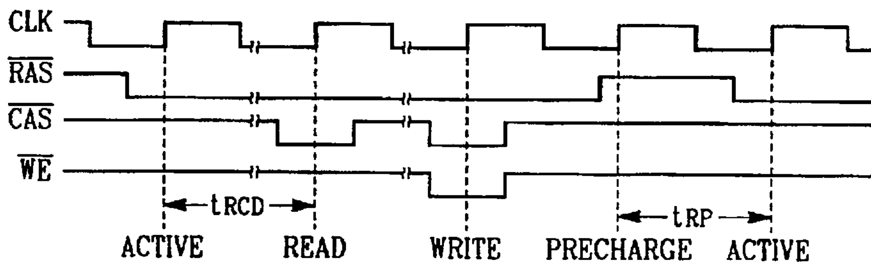

FIG. 5C

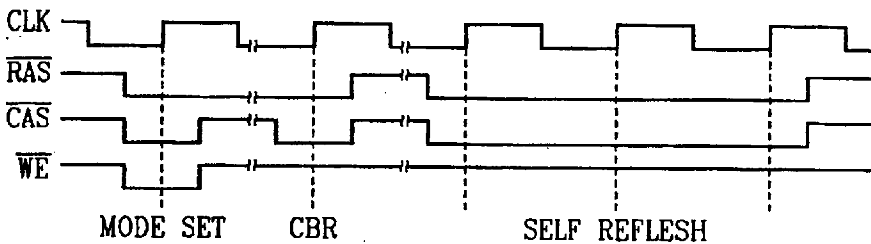

FIG. 5D

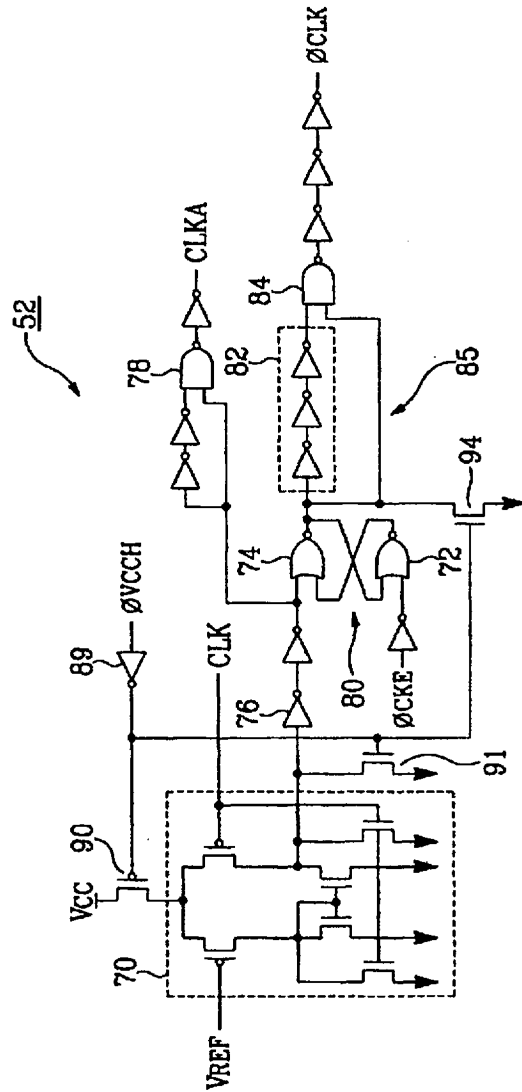

FIG. 6

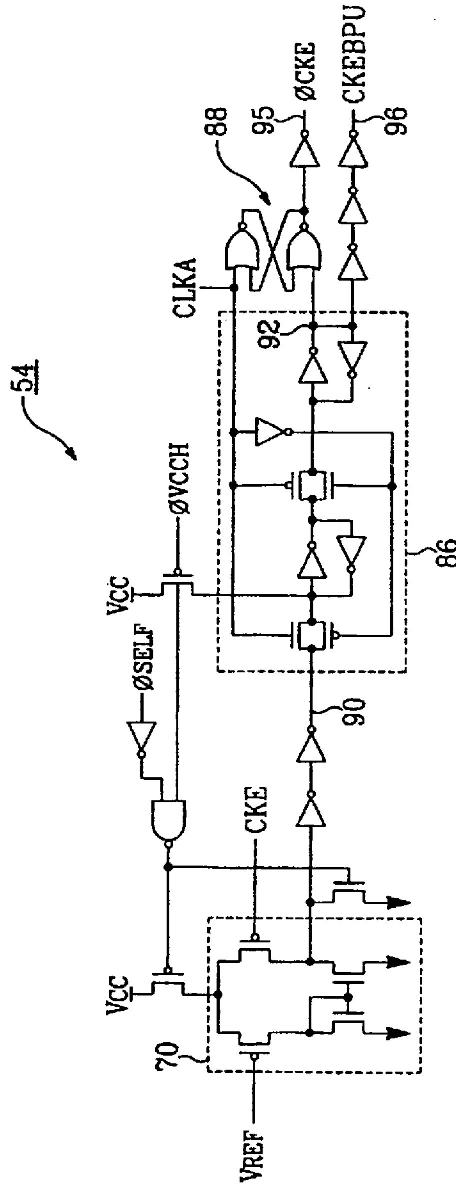

FIG. 7

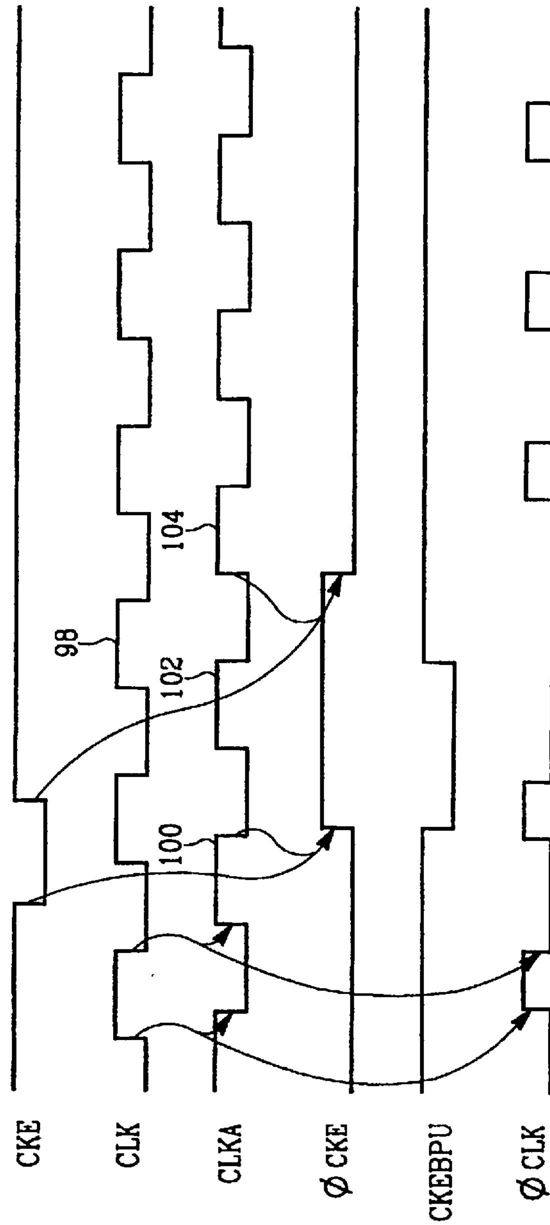

FIG. 8

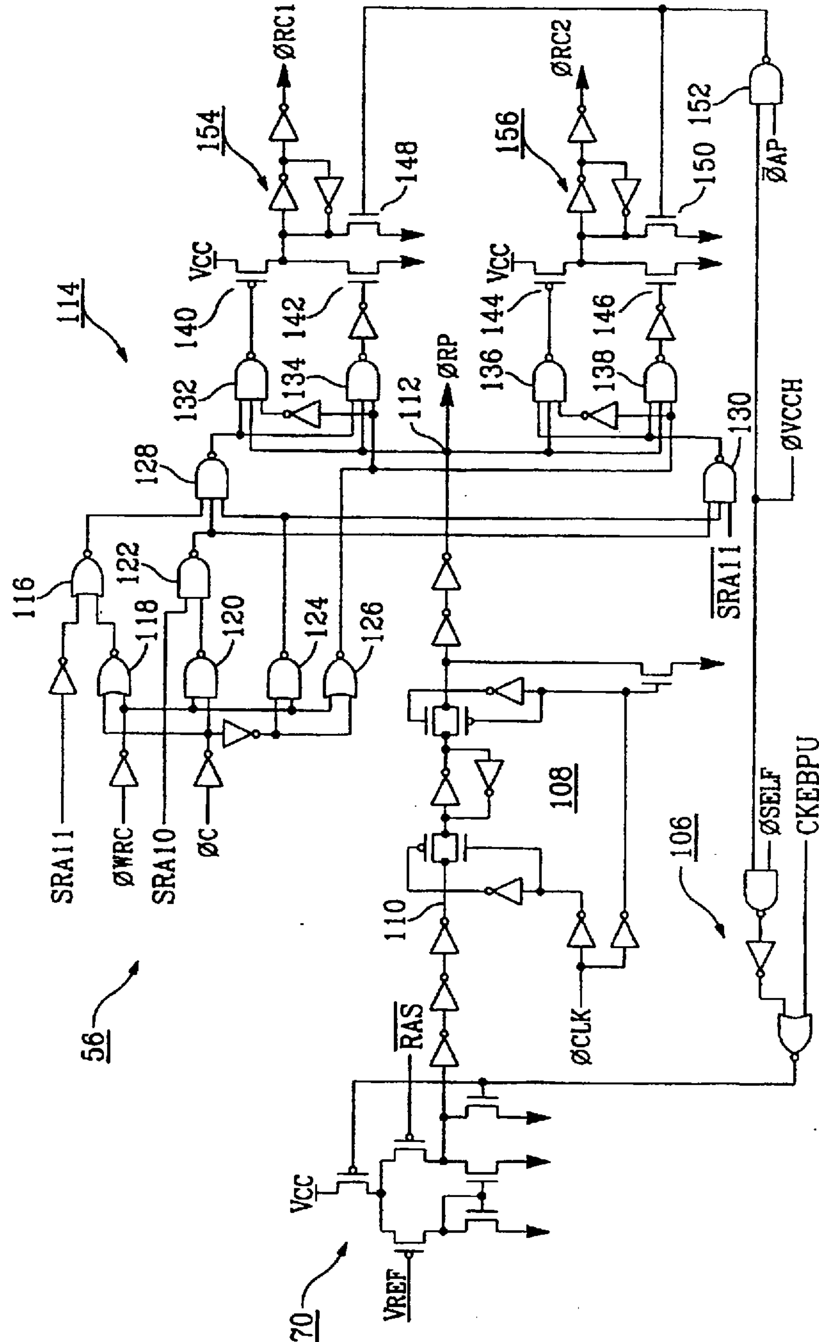

FIG. 9

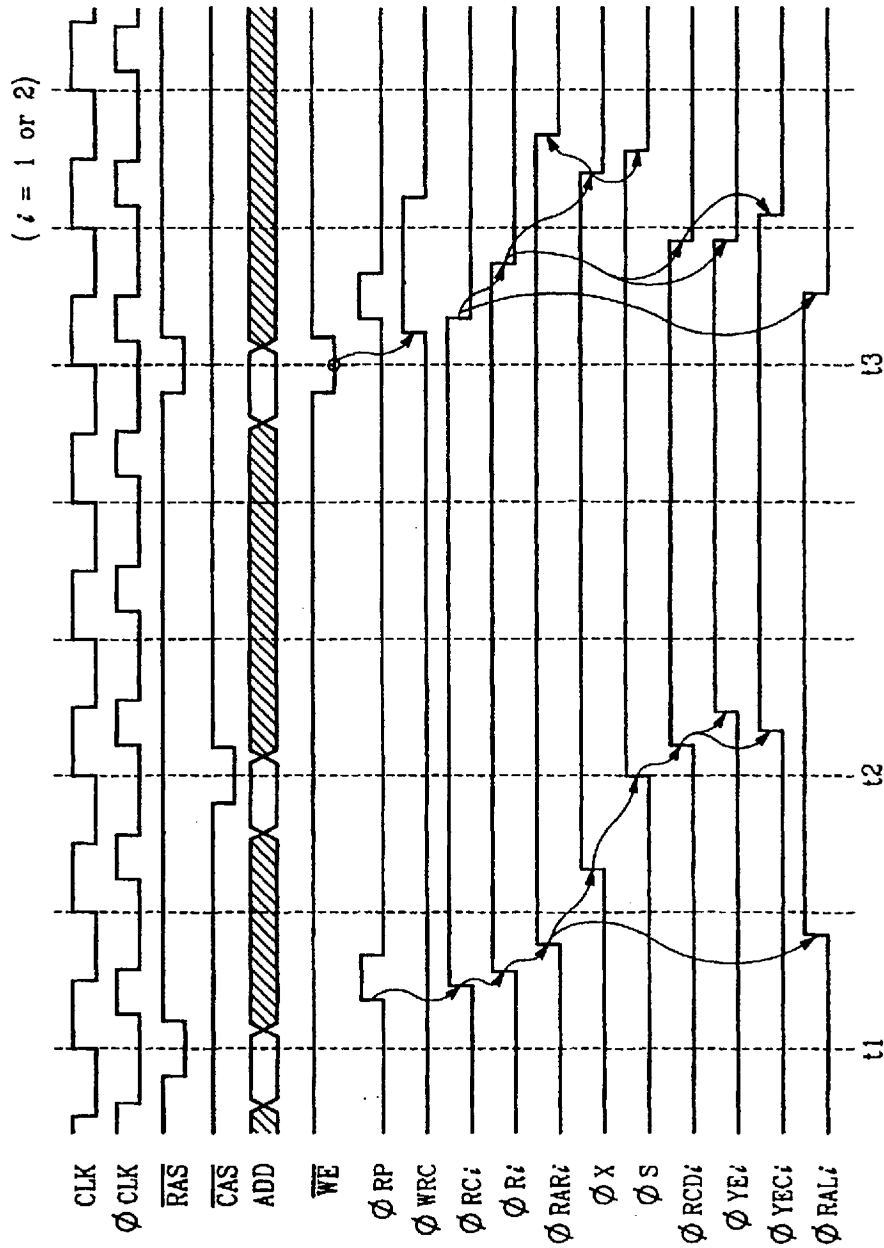

FIG. 10

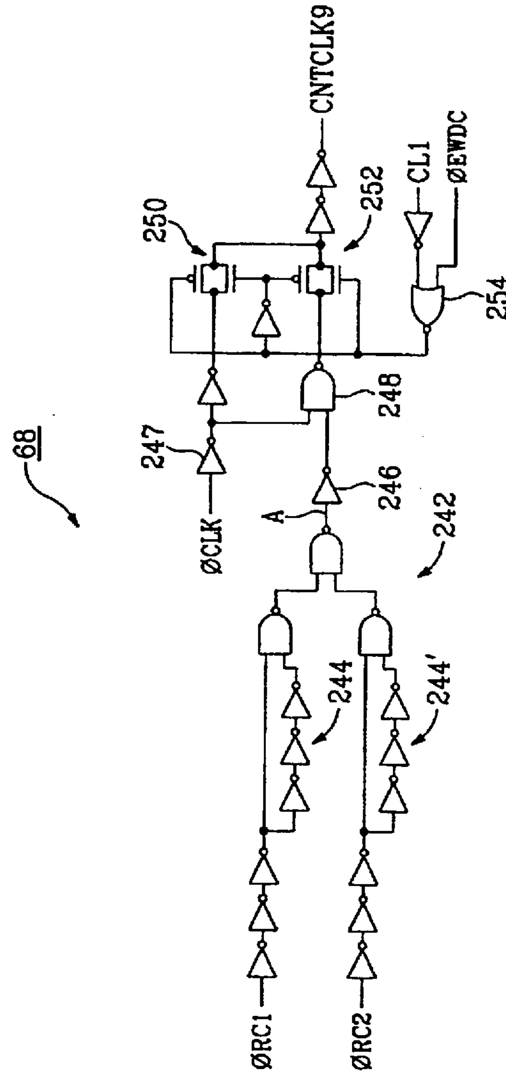

FIG. 11

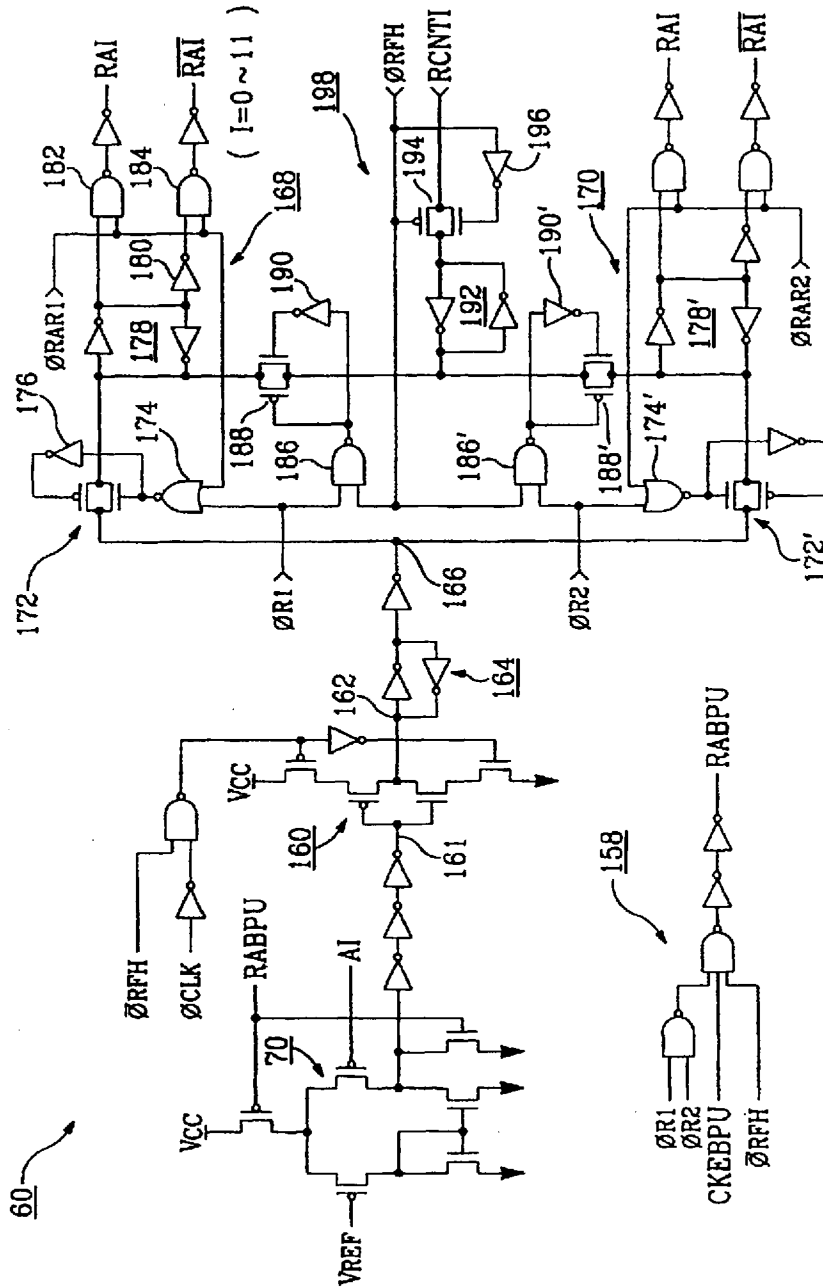

FIG. 12

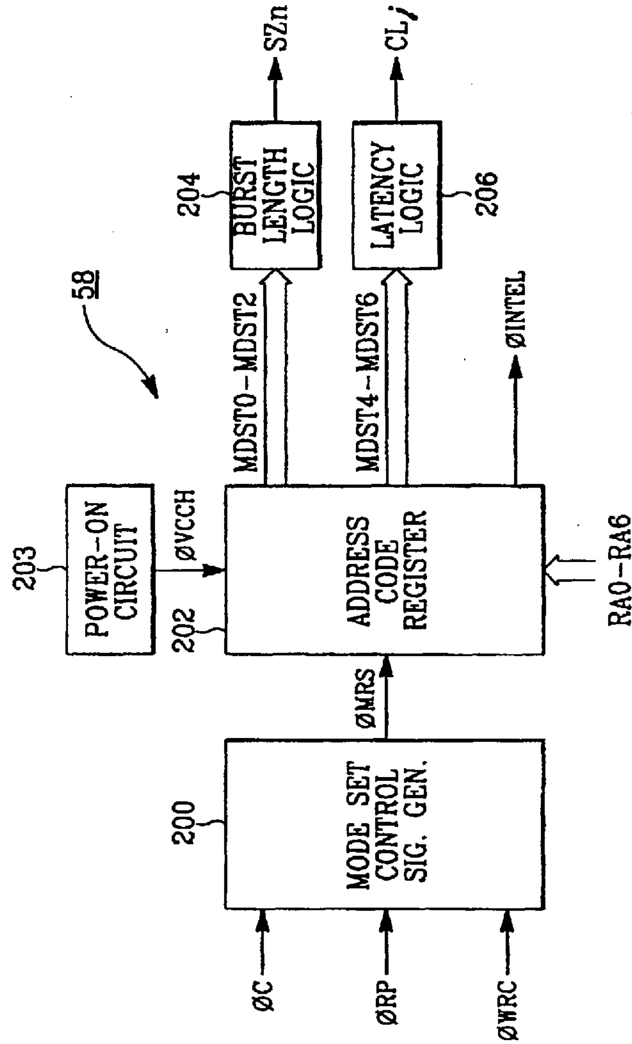

FIG. 13

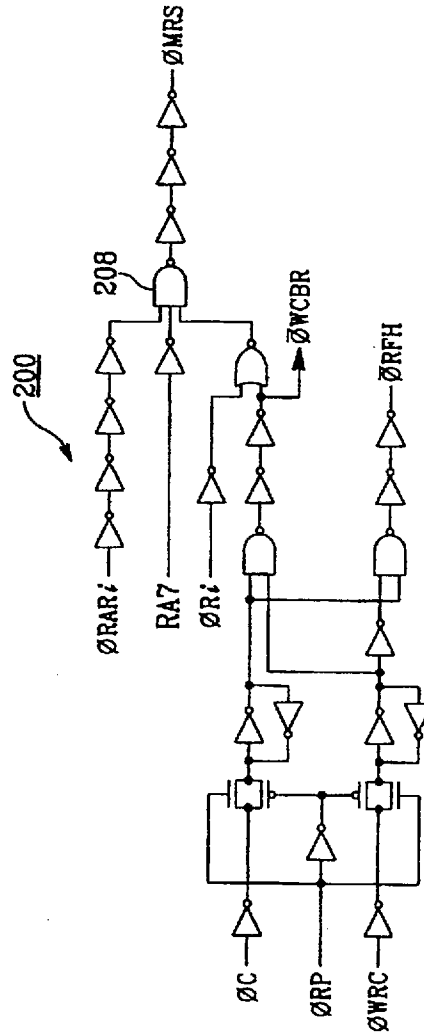

FIG. 14

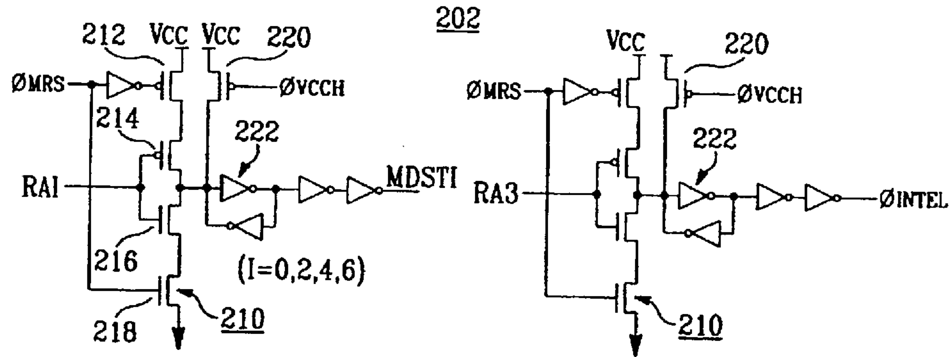

FIG. 15(A) FIG. 15(B)

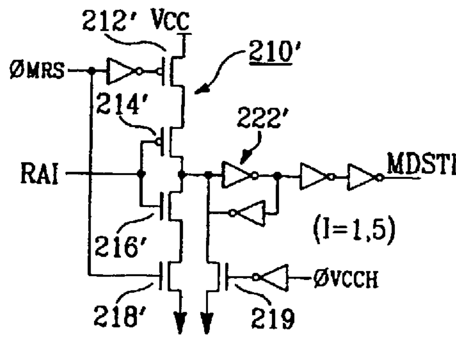

FIG. 15(C)

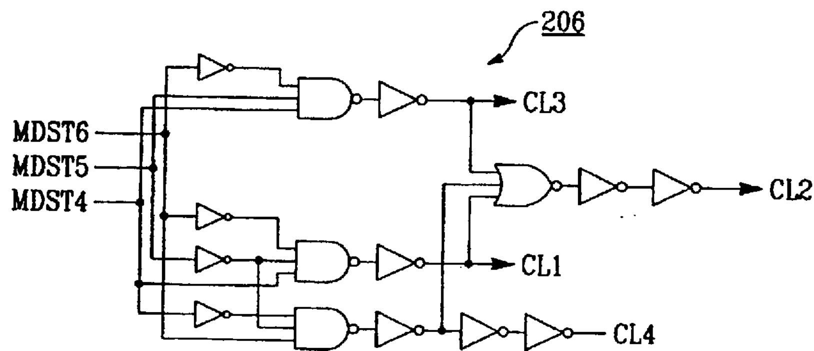

FIG. 16

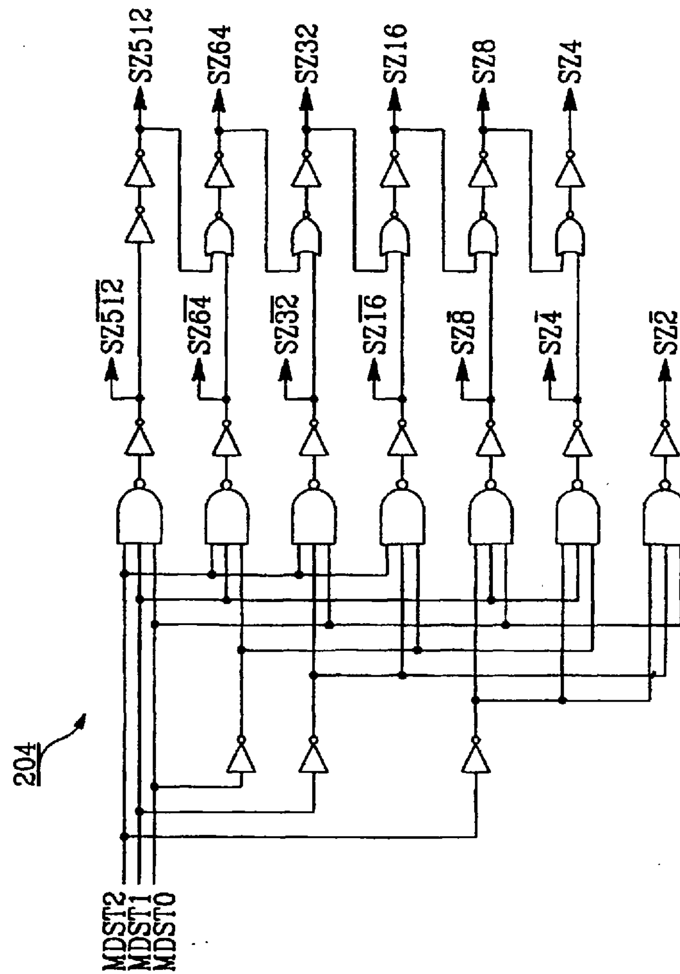

FIG. 17

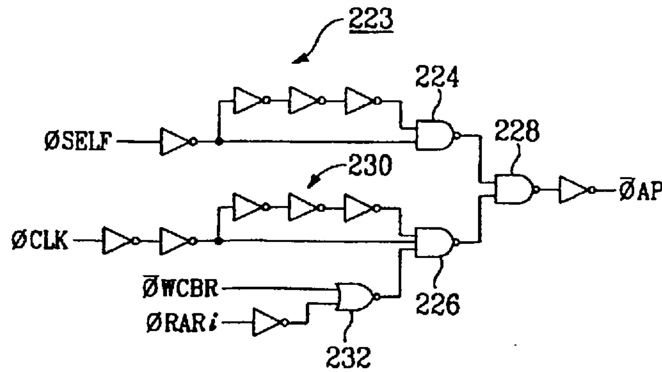

FIG. 18

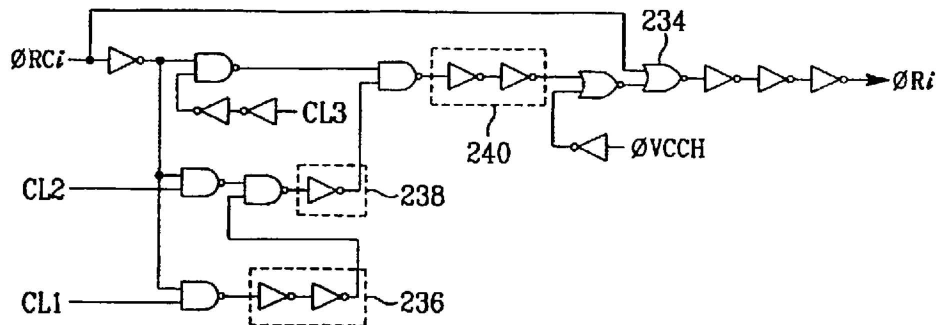

FIG. 19

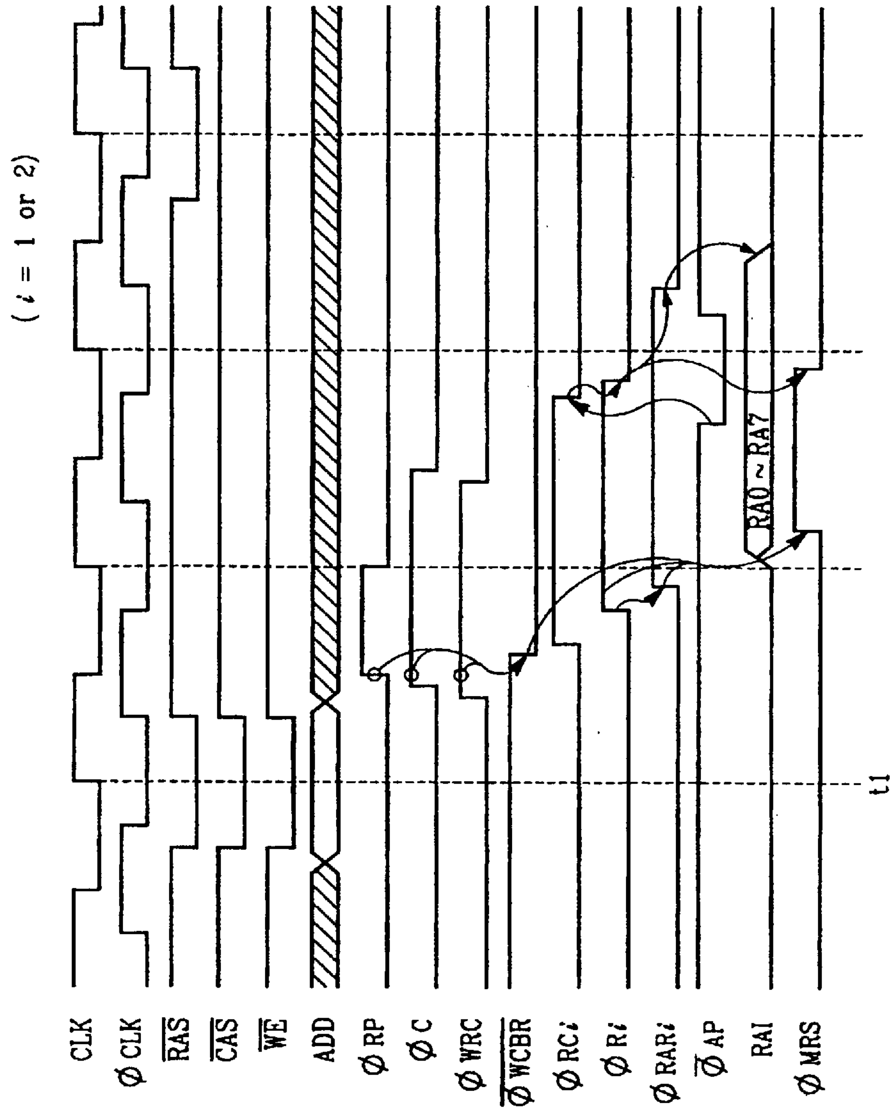

FIG. 20

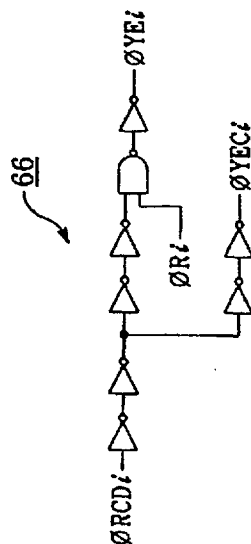

FIG. 21

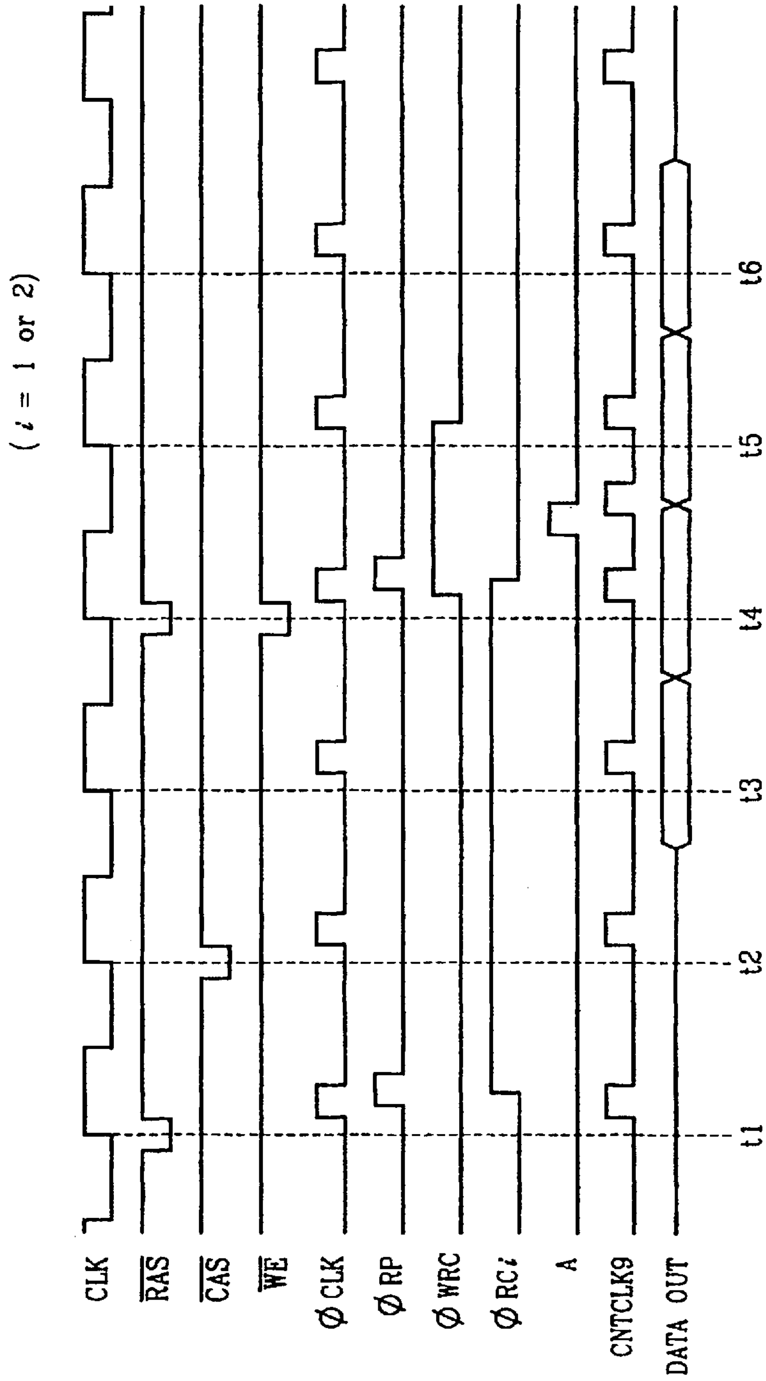

FIG. 22

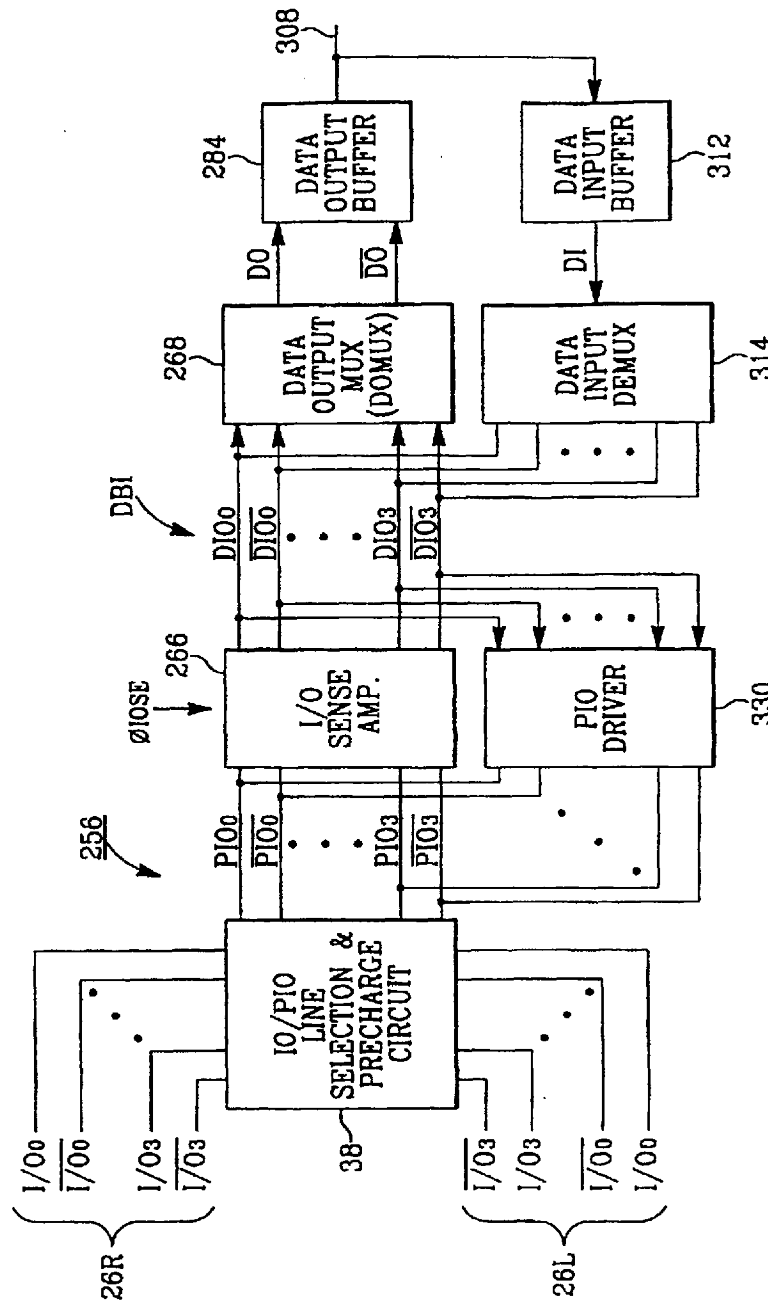

FIG. 23

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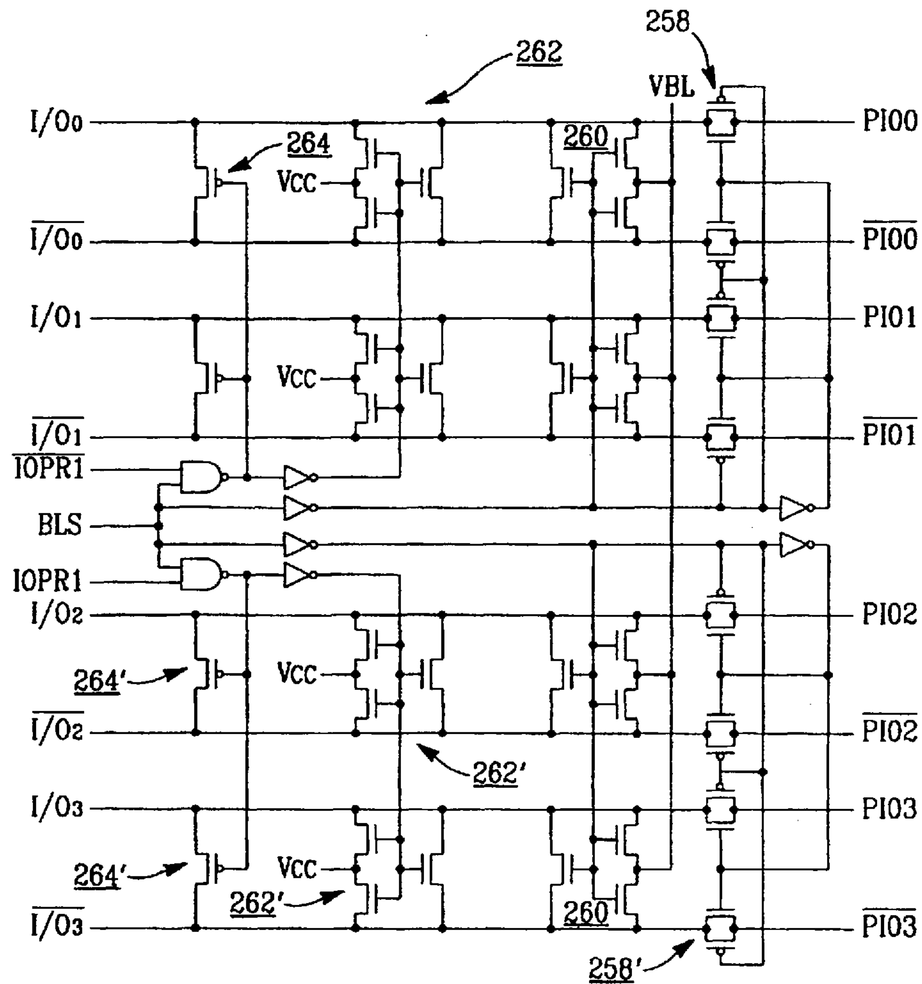

FIG. 24

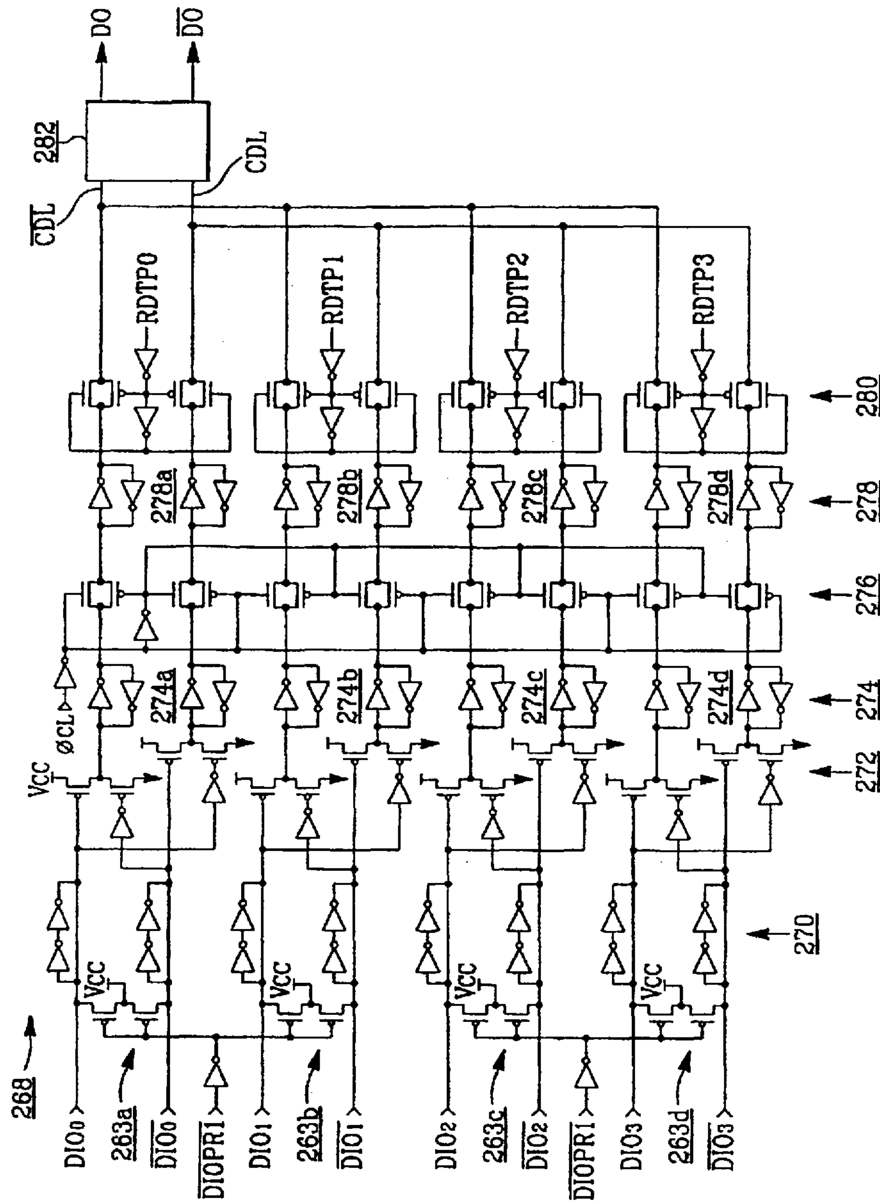

FIG. 25

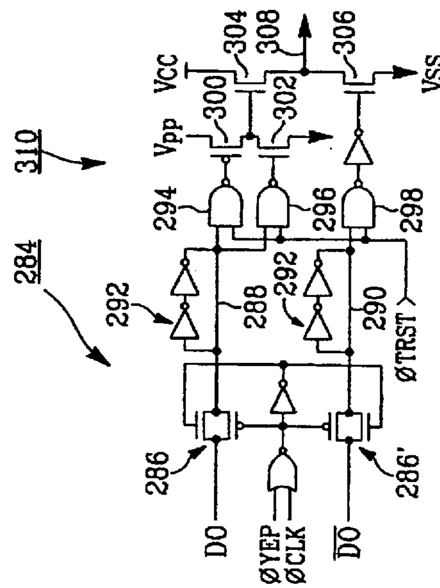

FIG. 26

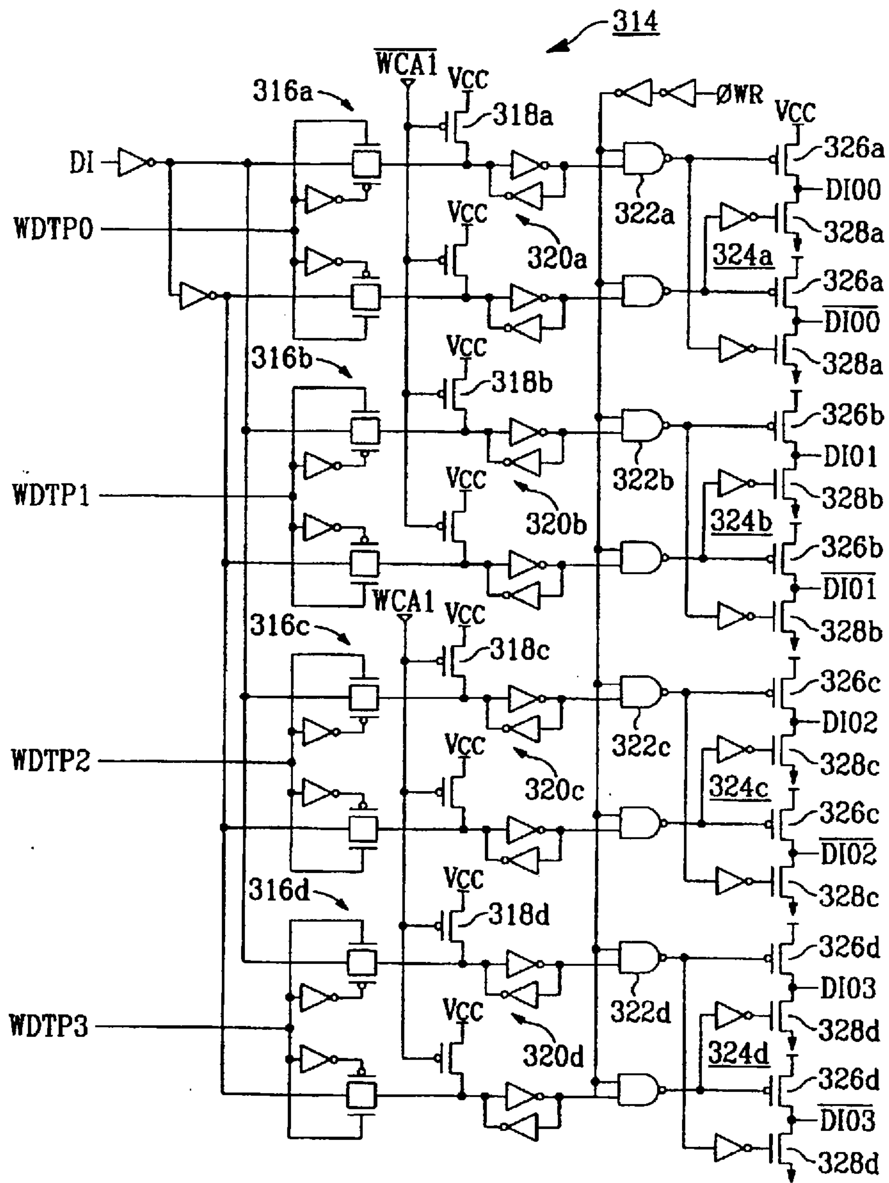

FIG. 27

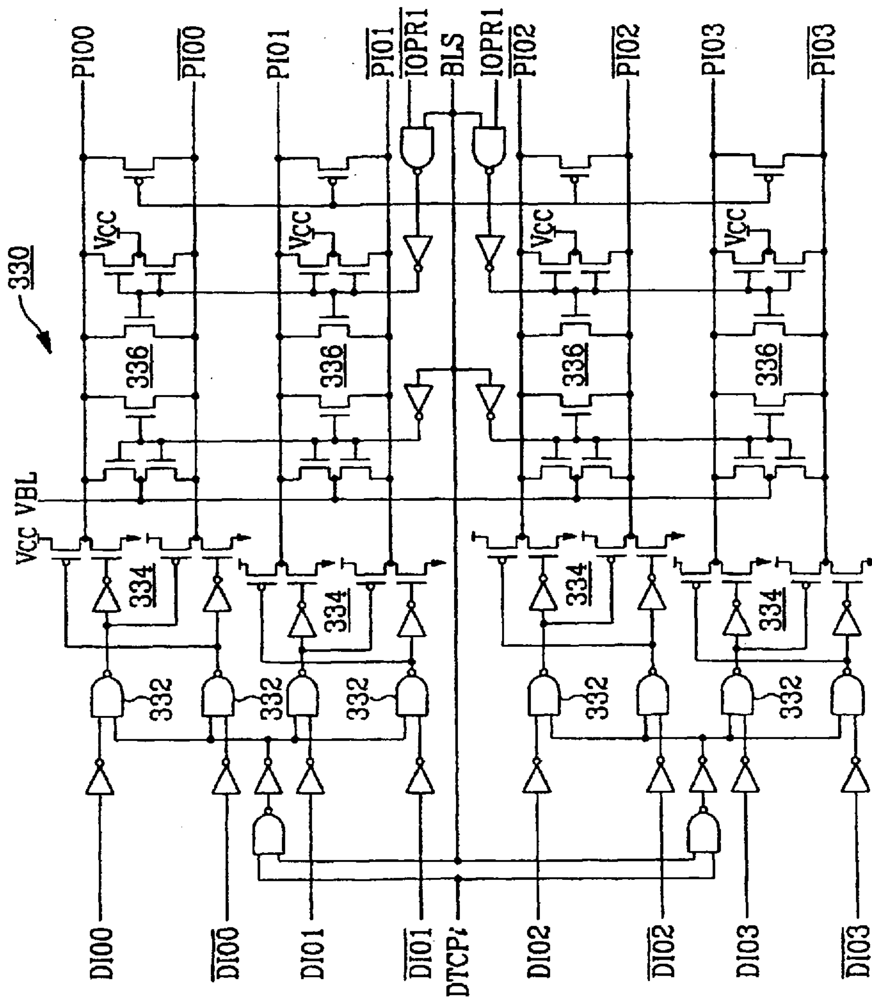

FIG. 28

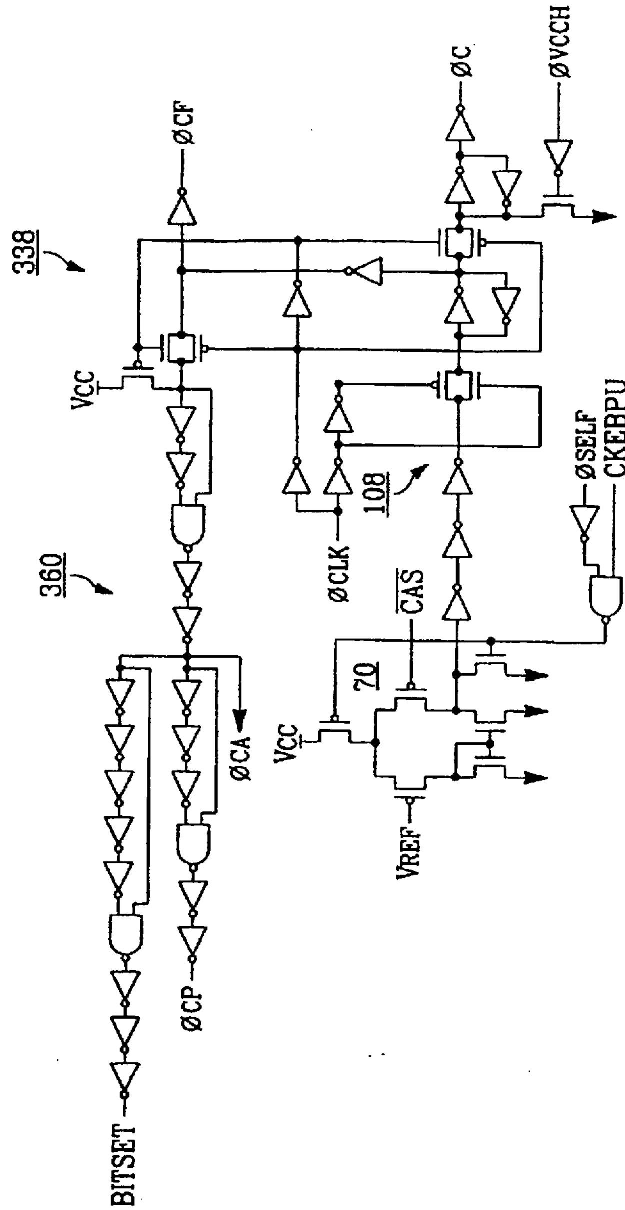

FIG. 29

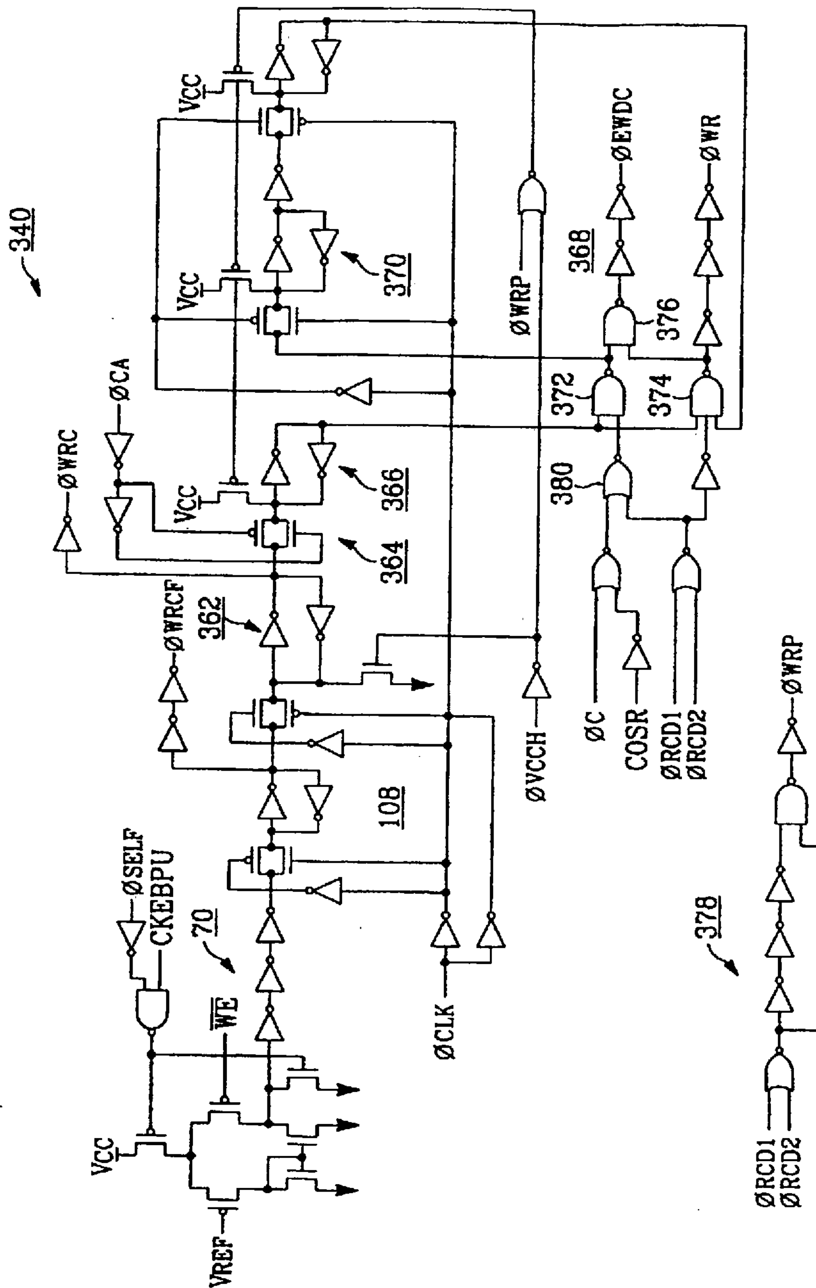

FIG. 30

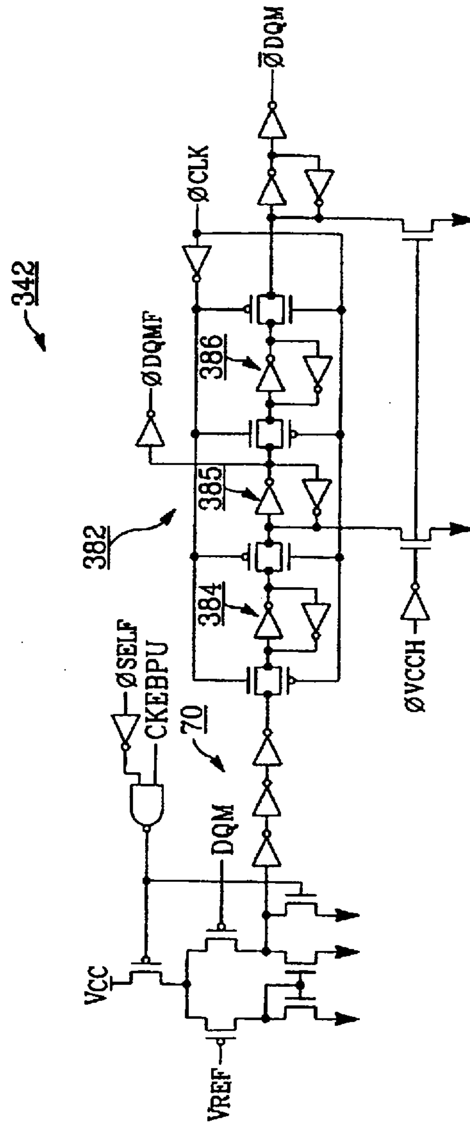

FIG. 31

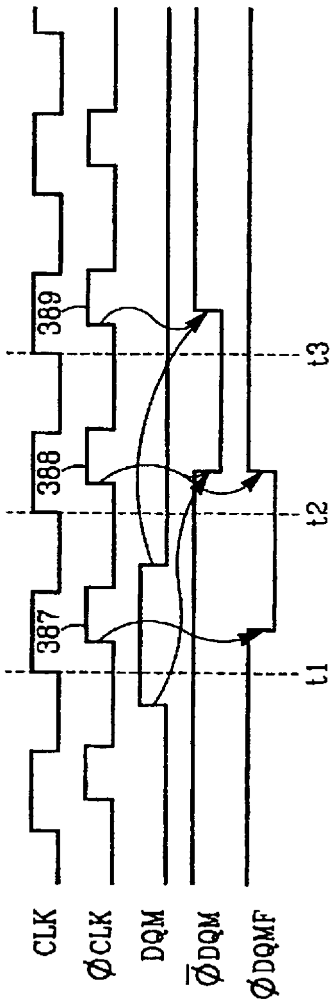

FIG. 32

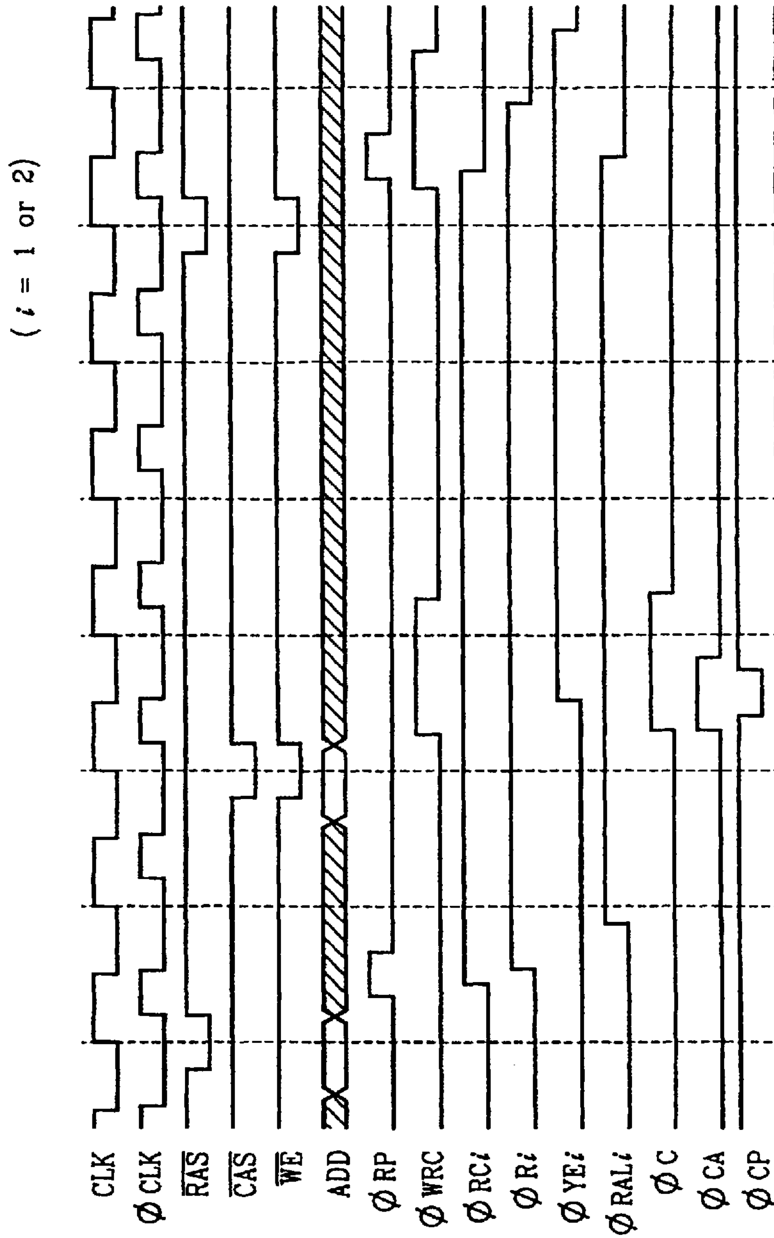

FIG. 33A

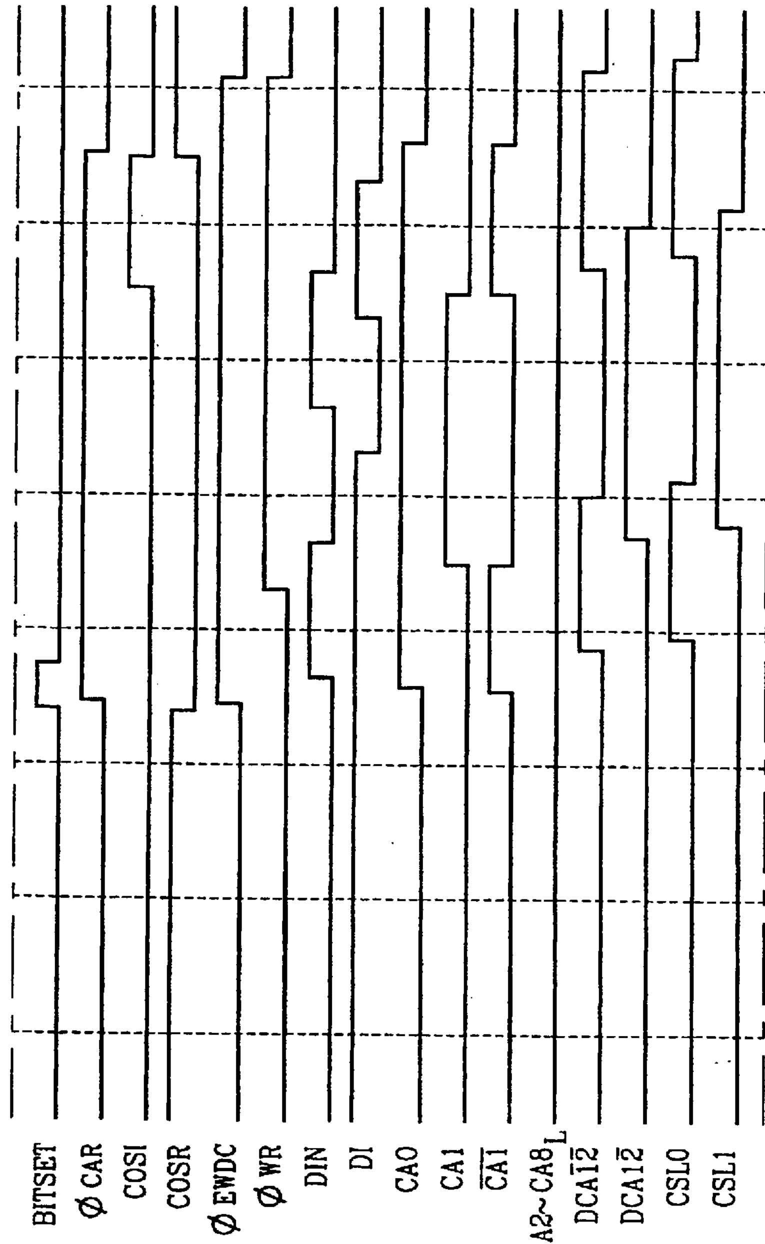

FIG. 33B

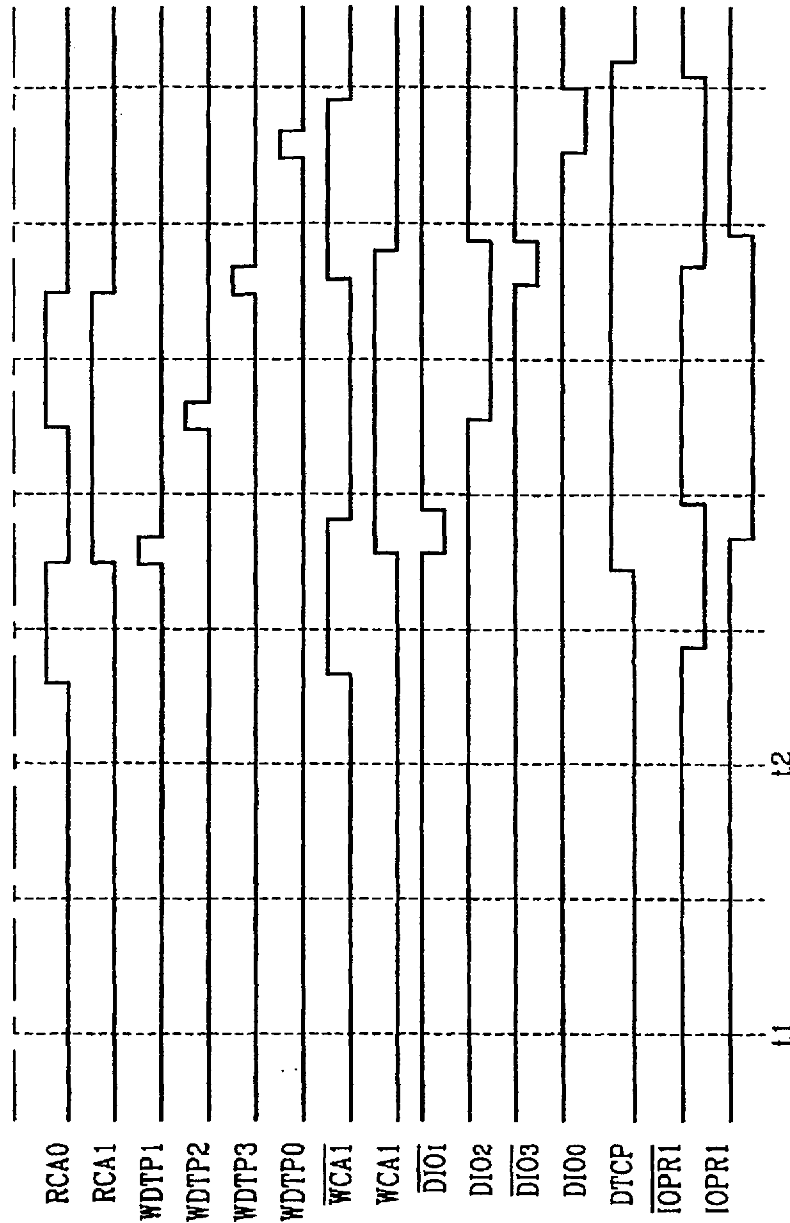

FIG. 33C

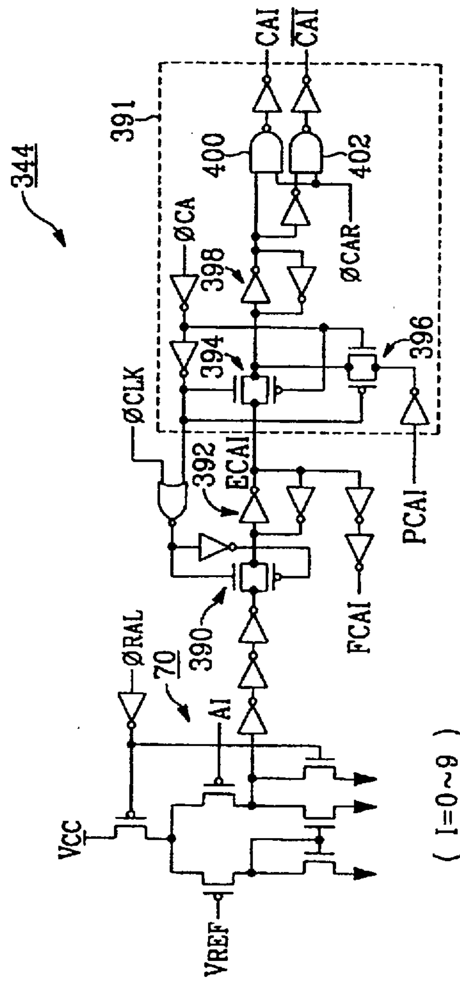

FIG. 34

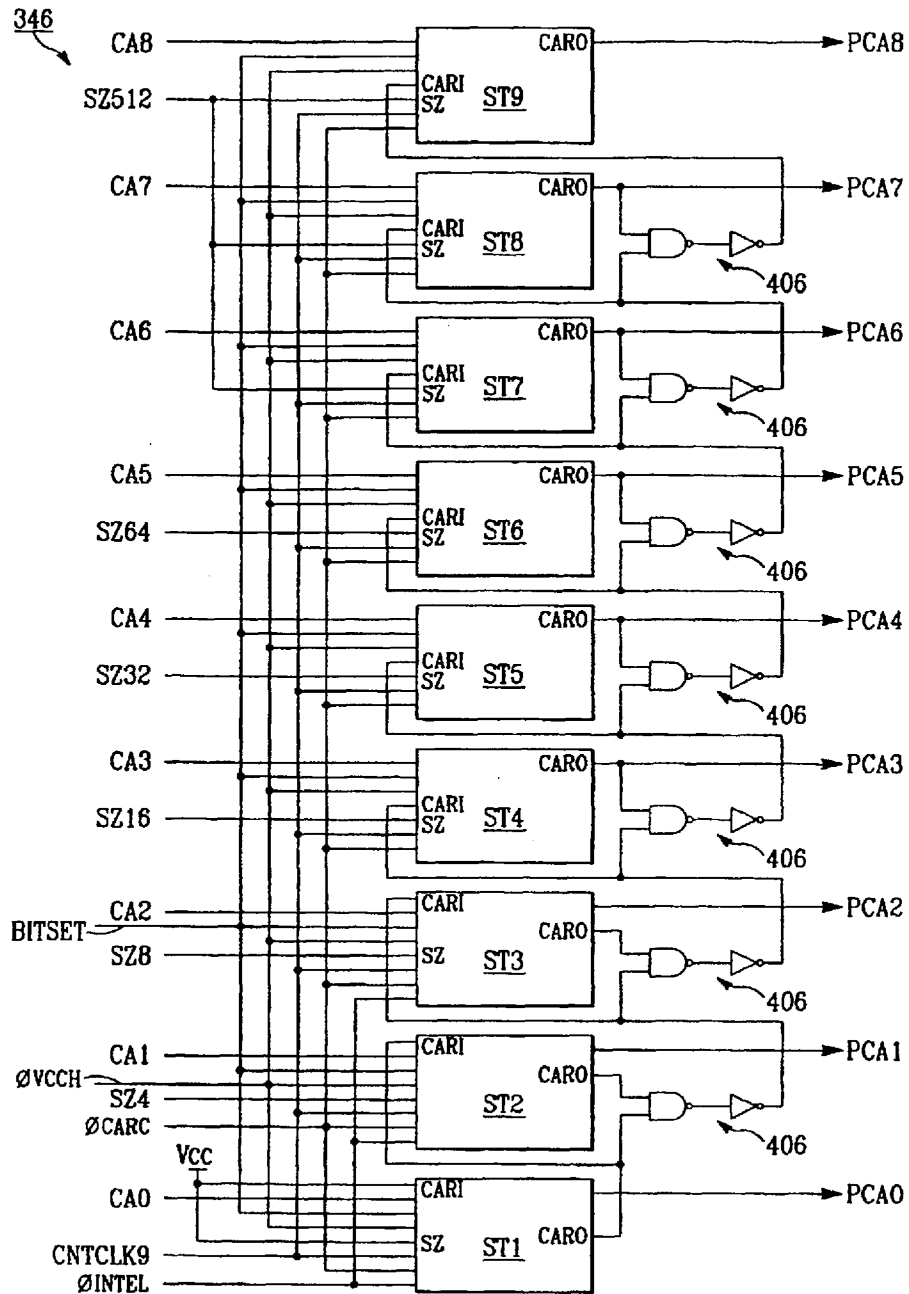

FIG. 35

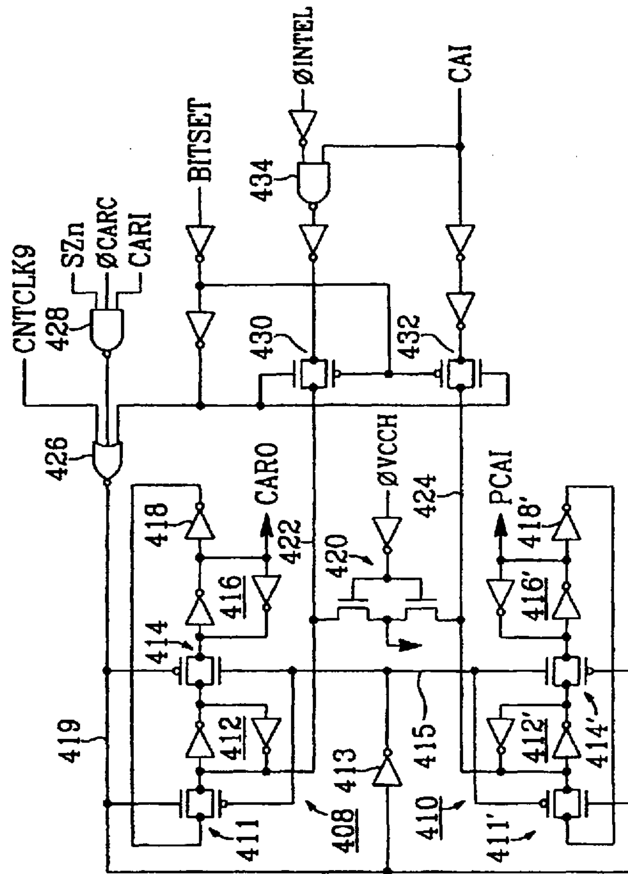

FIG. 36A

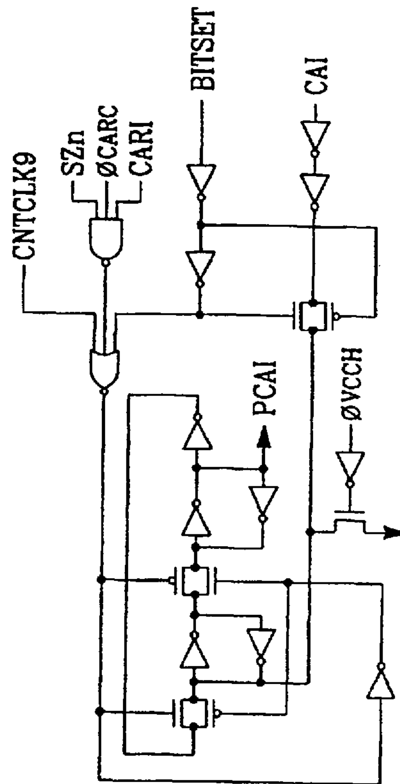

FIG. 36B

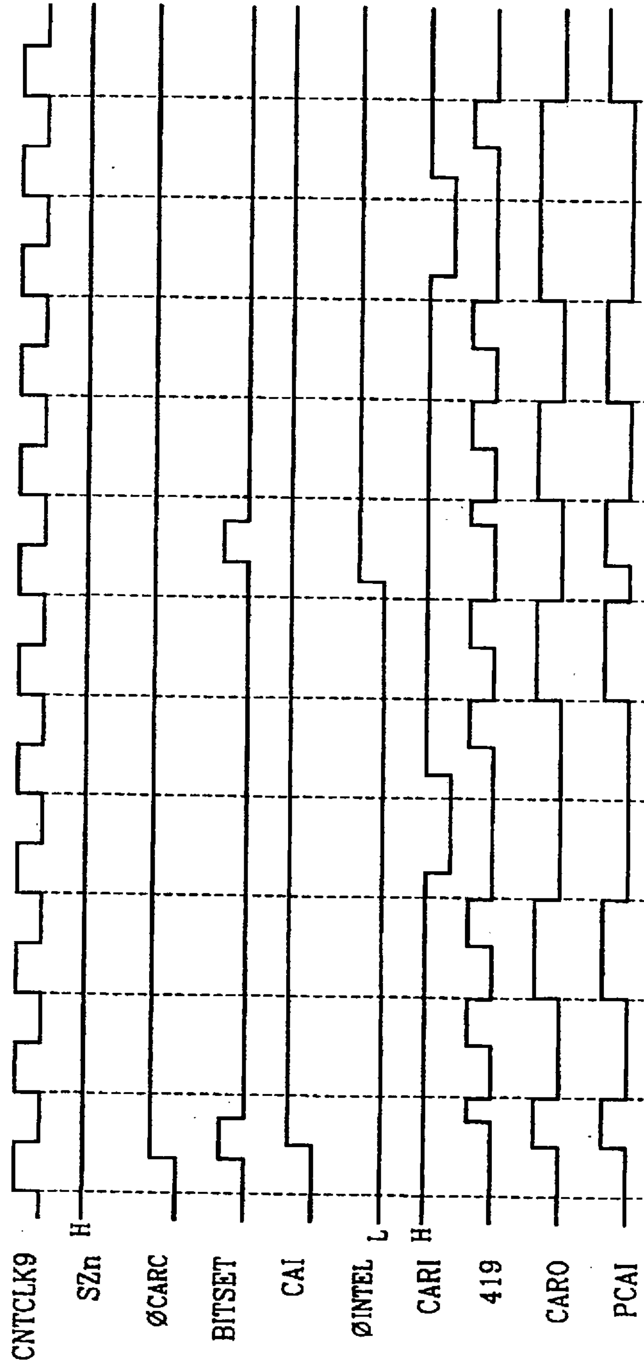

FIG. 37

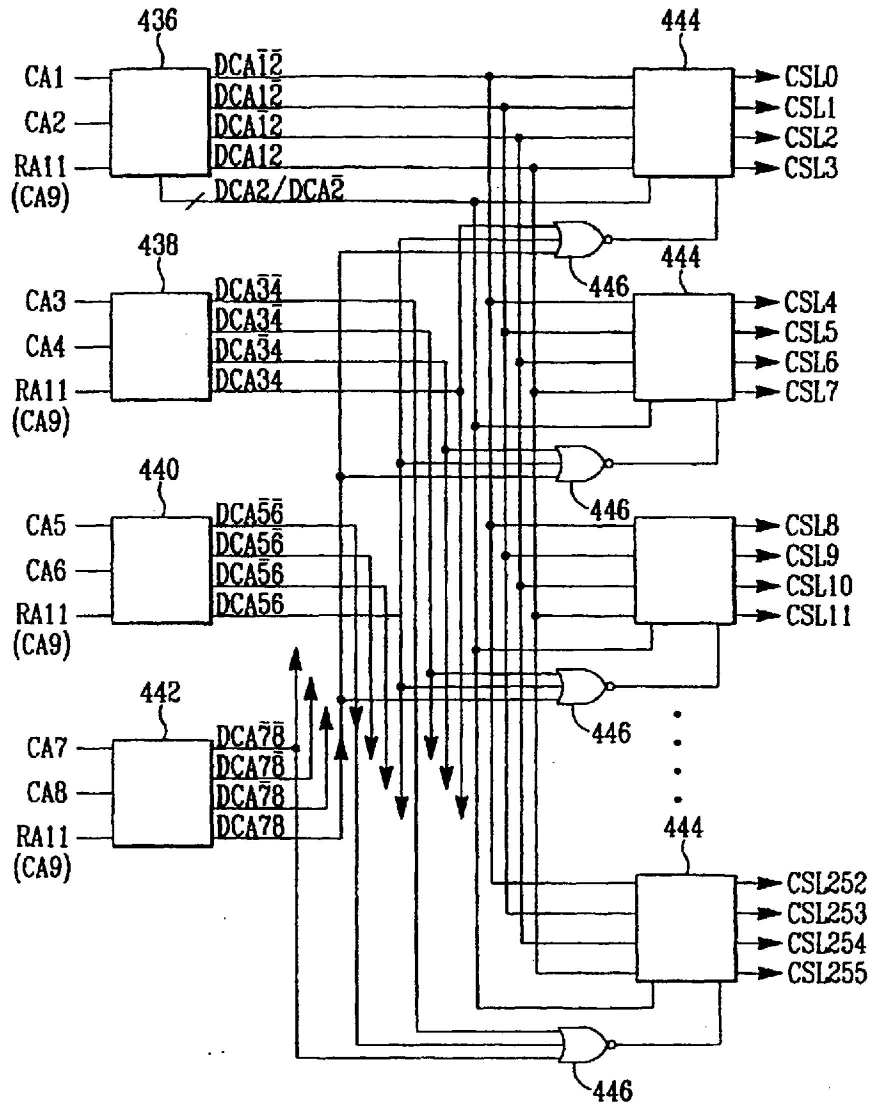

FIG. 38

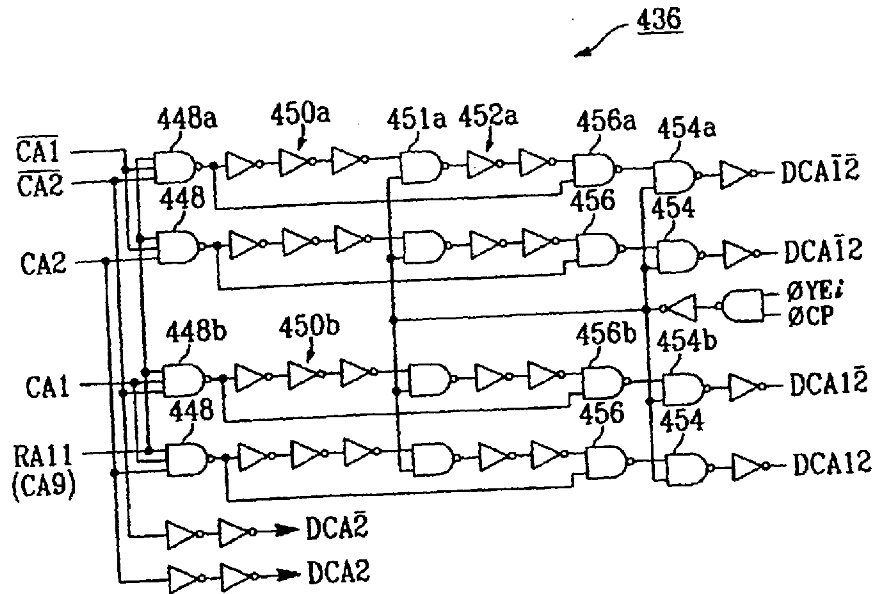

FIG. 39A

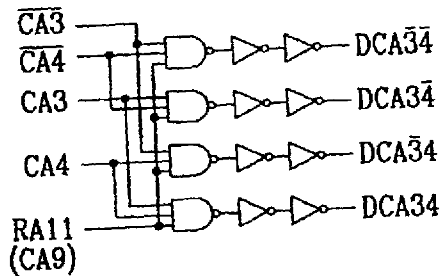

FIG. 39B

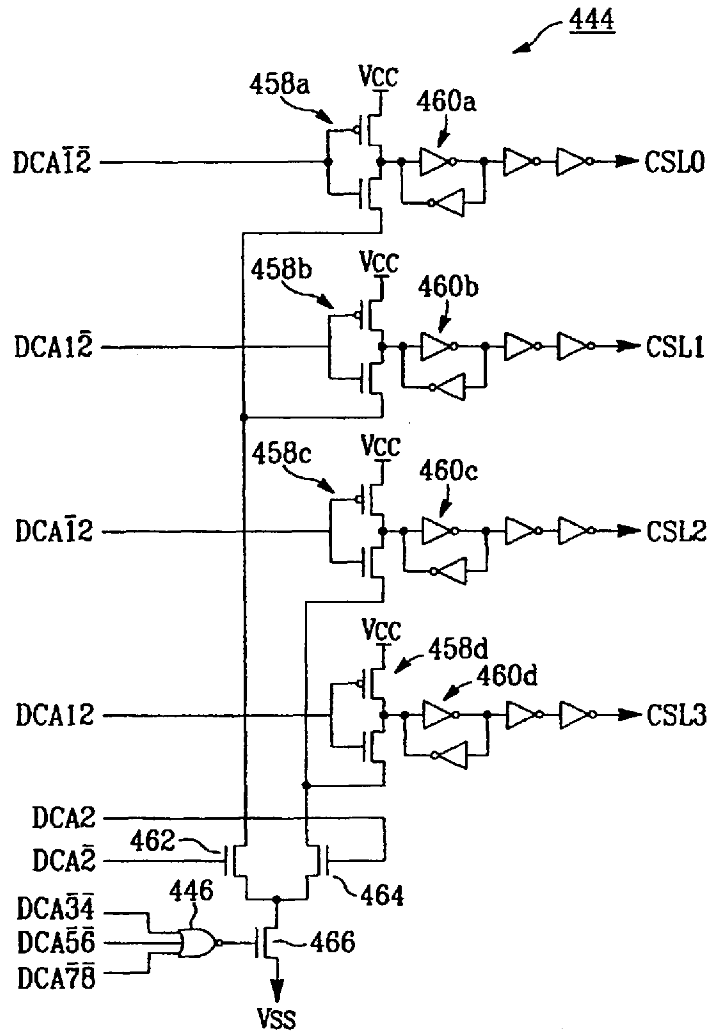

FIG. 40

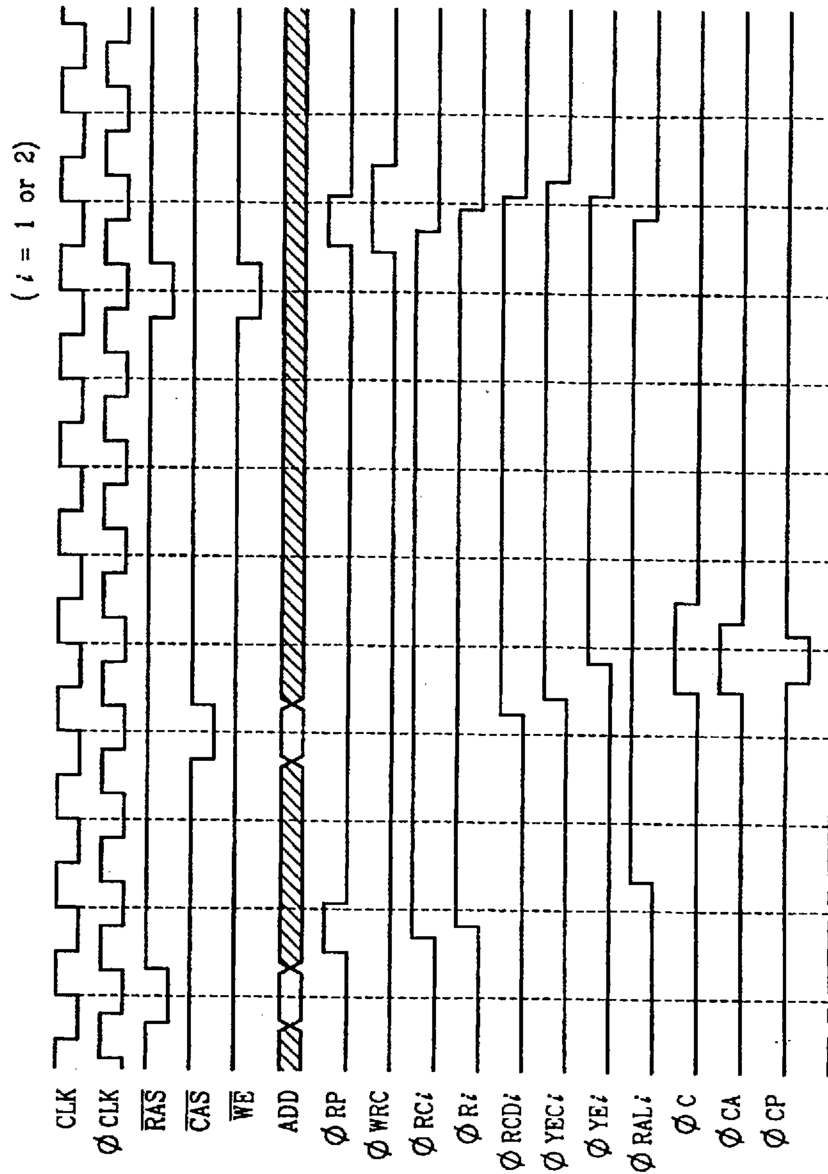

FIG. 41A

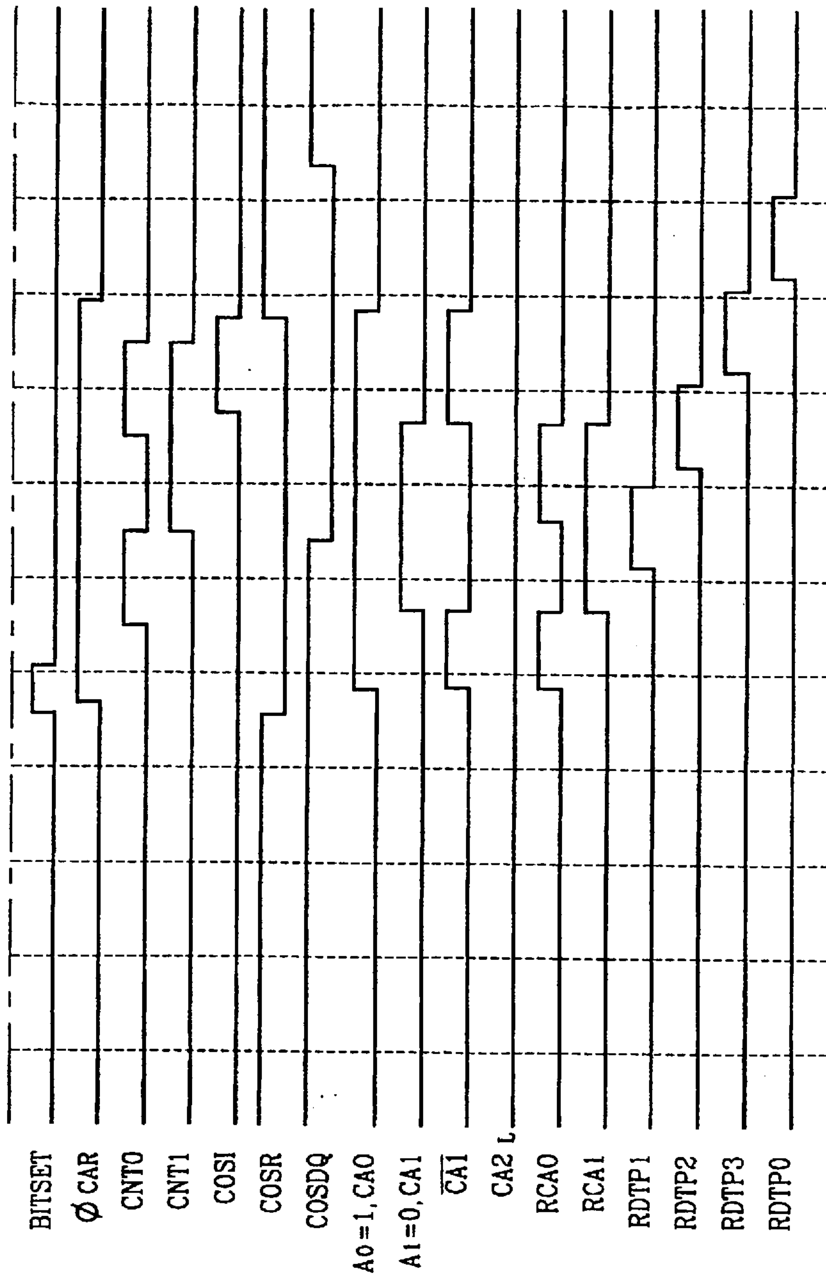

FIG. 41B

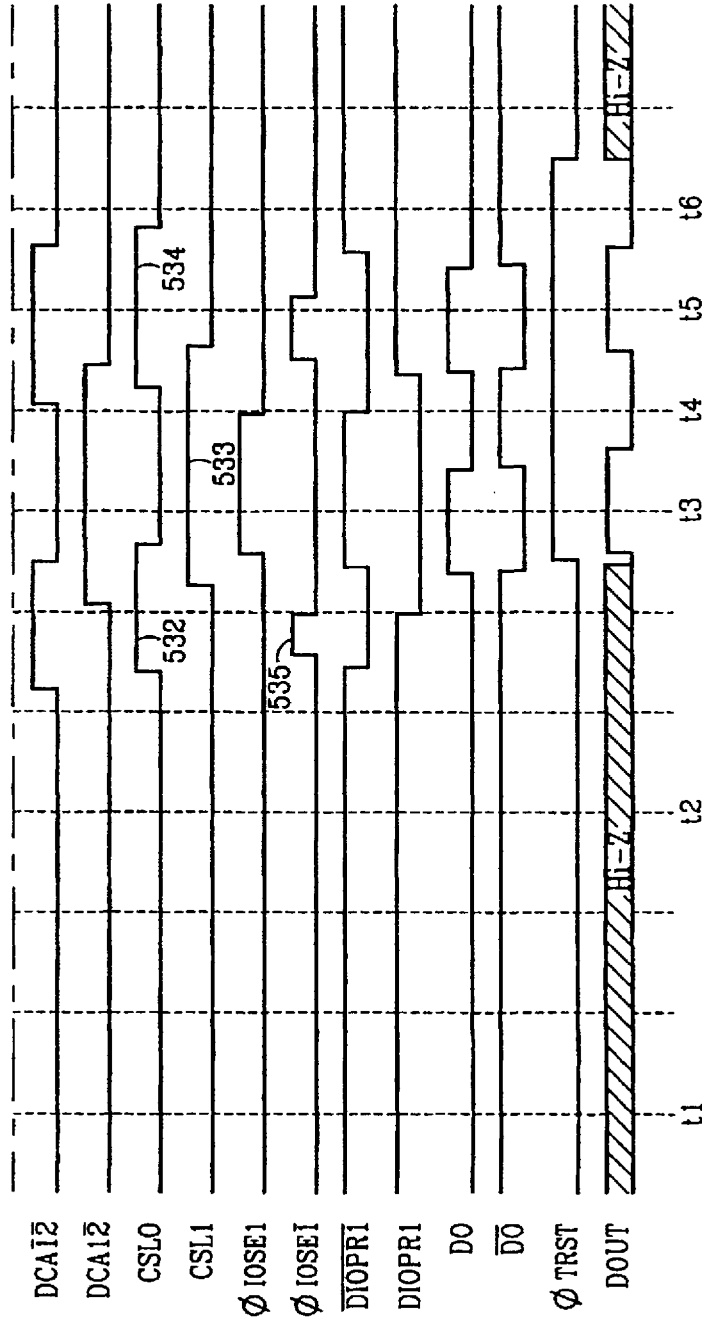

FIG. 41C

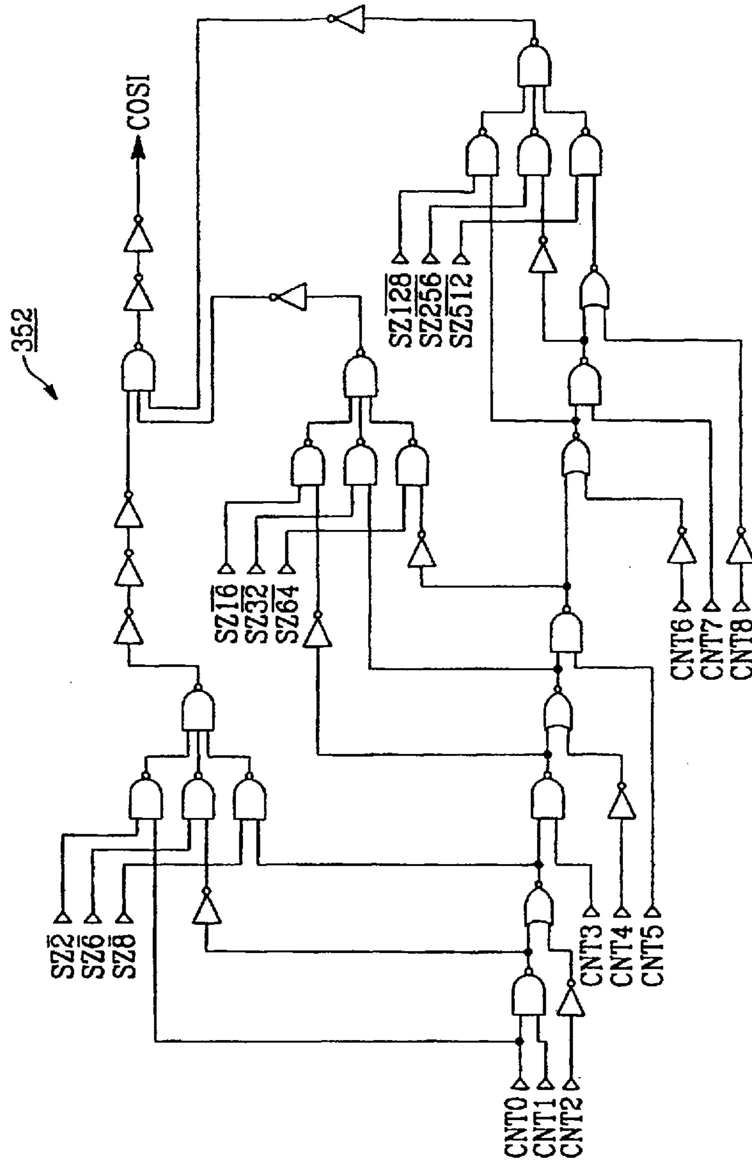

FIG. 42

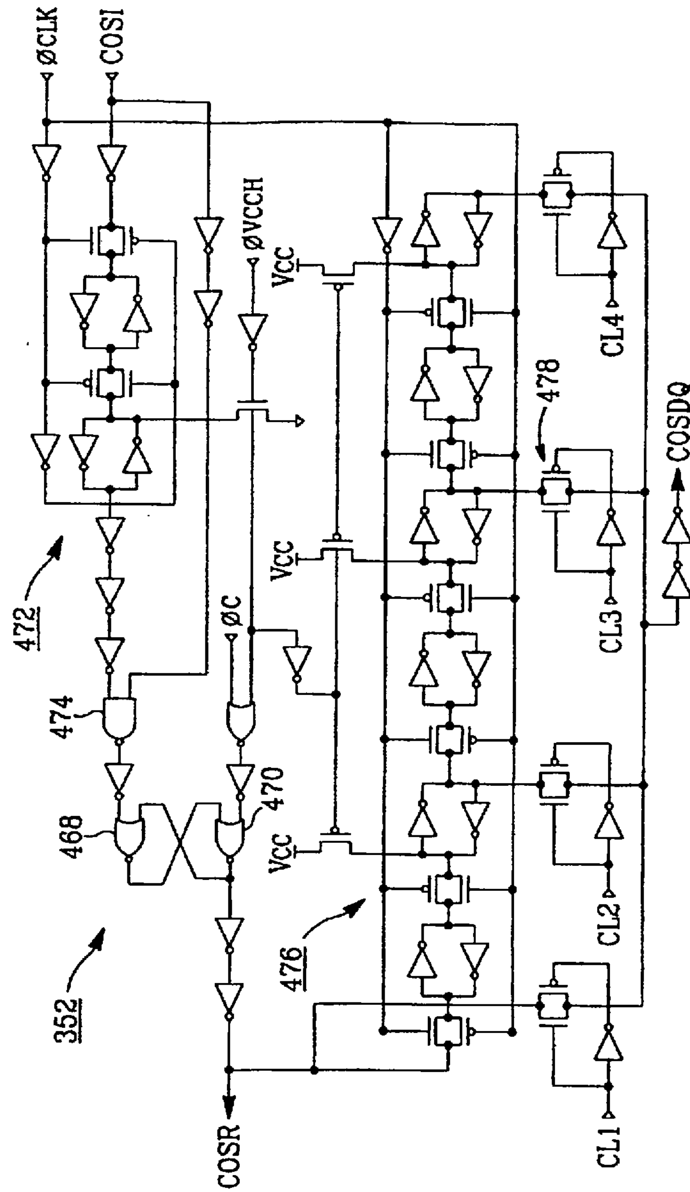

FIG. 43

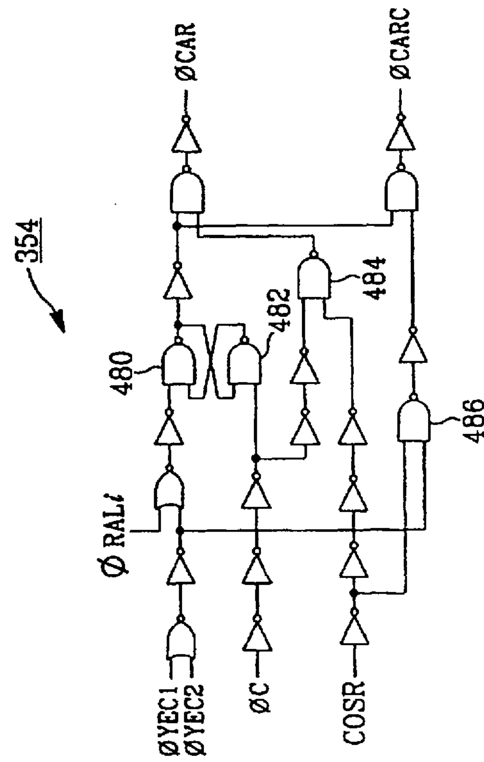

FIG. 44

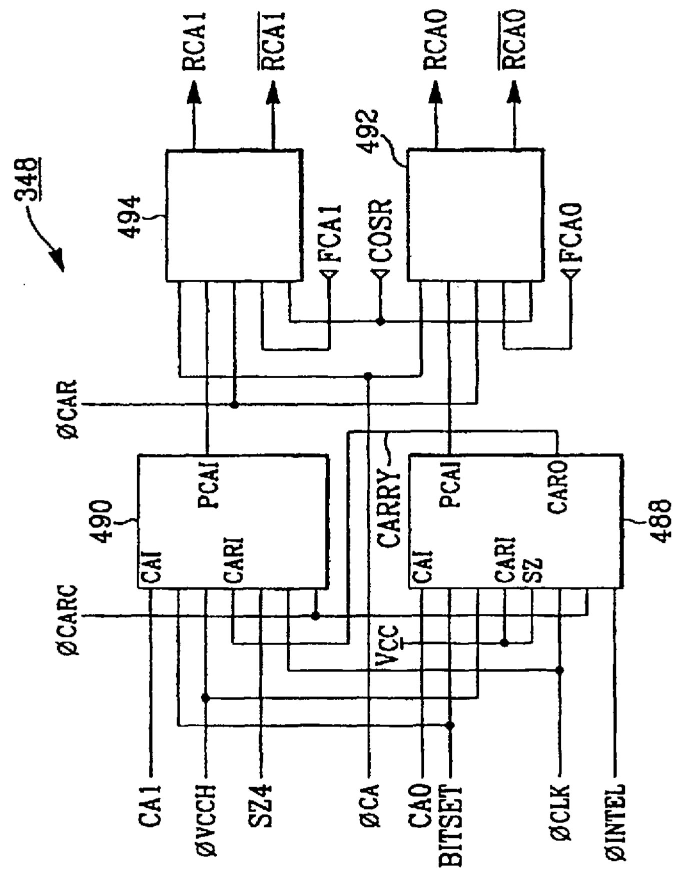

FIG. 45

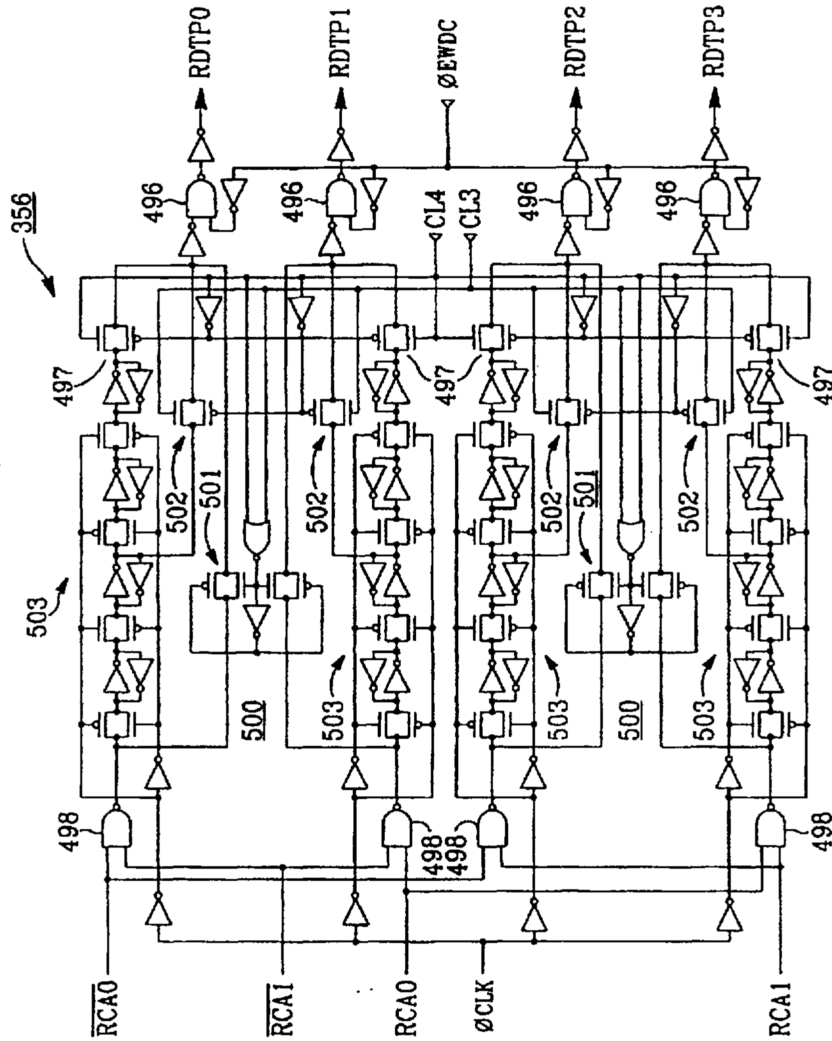

FIG. 46

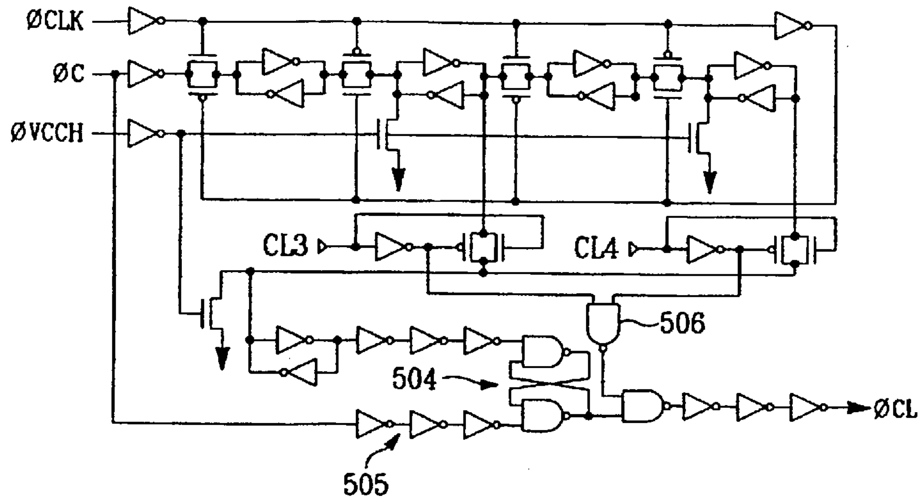

FIG. 47

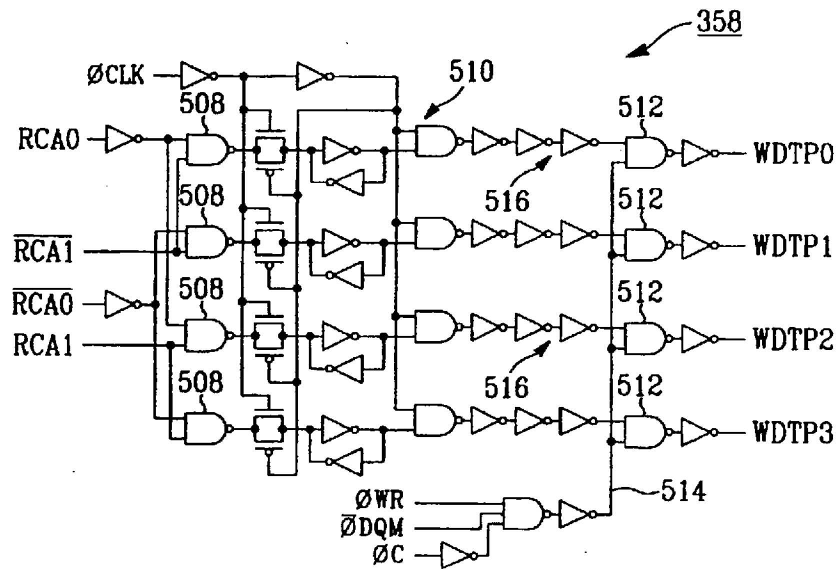

FIG. 48

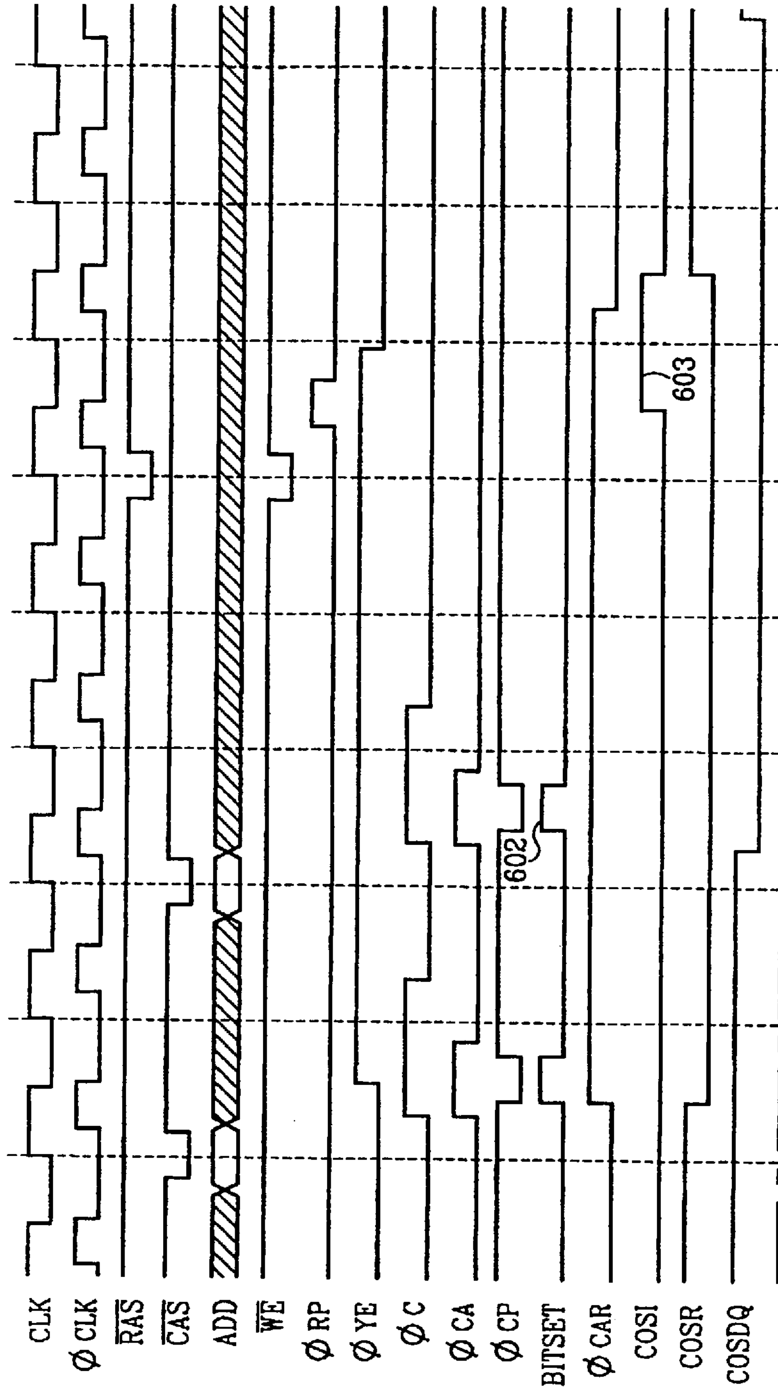

FIG. 49A

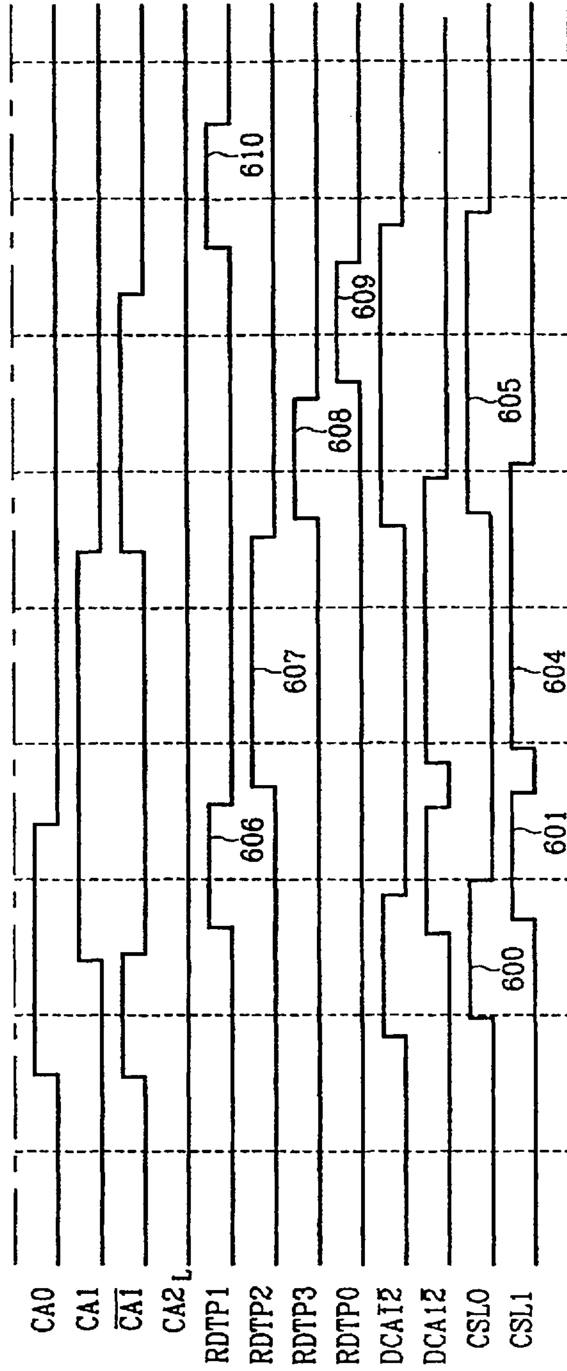

FIG. 49B

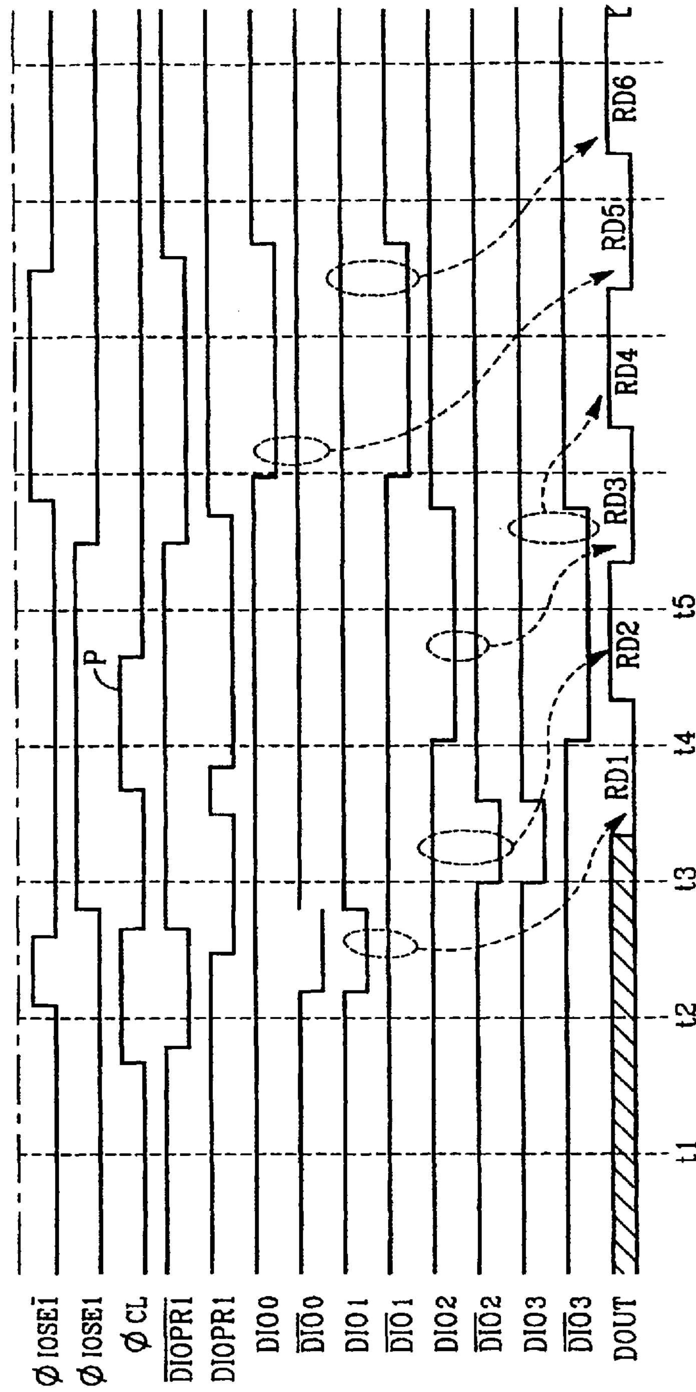

FIG. 49C

RX 1309

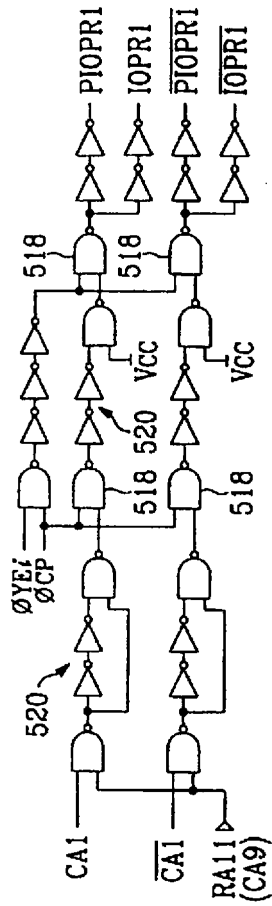

FIG. 50

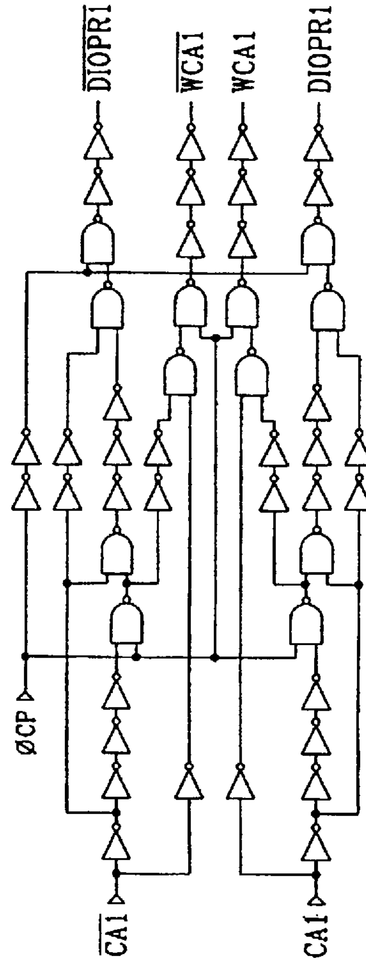

FIG. 51

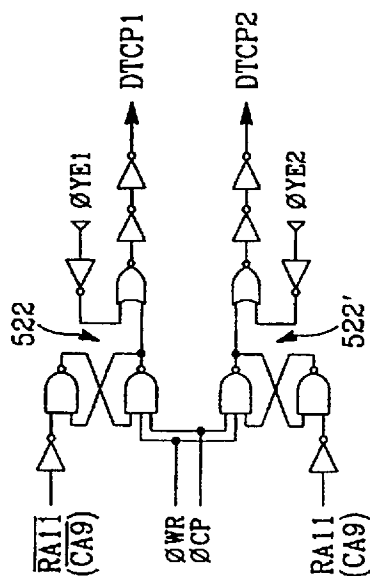

FIG. 52

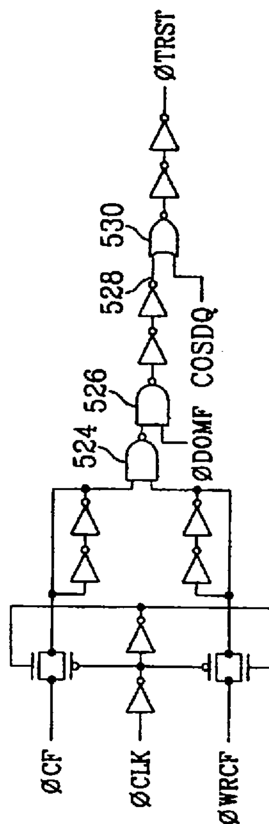

FIG. 53

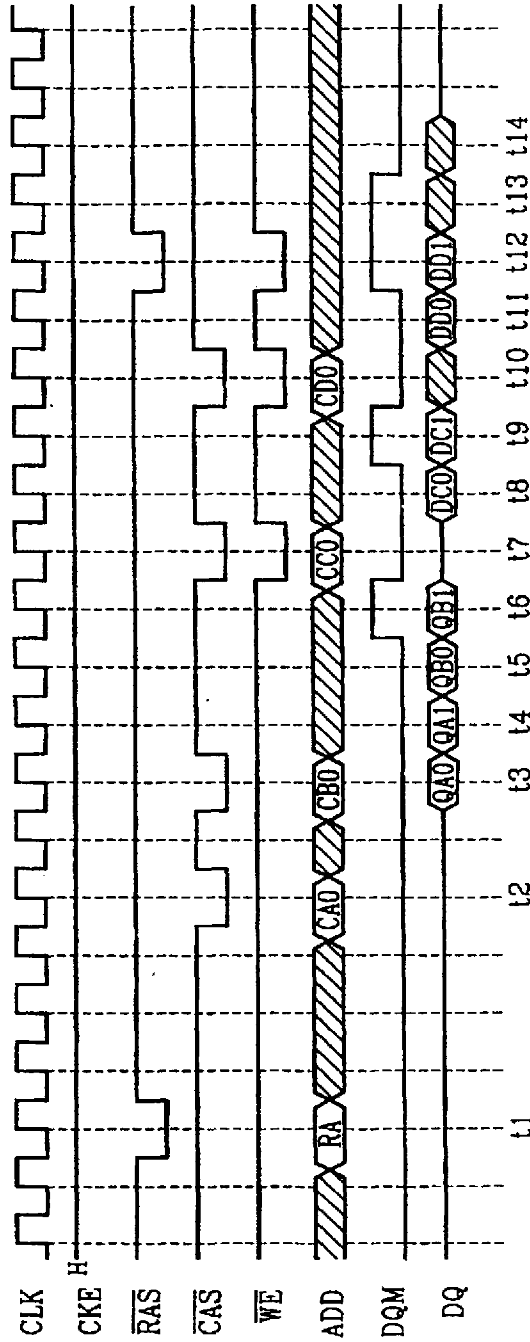

FIG. 54

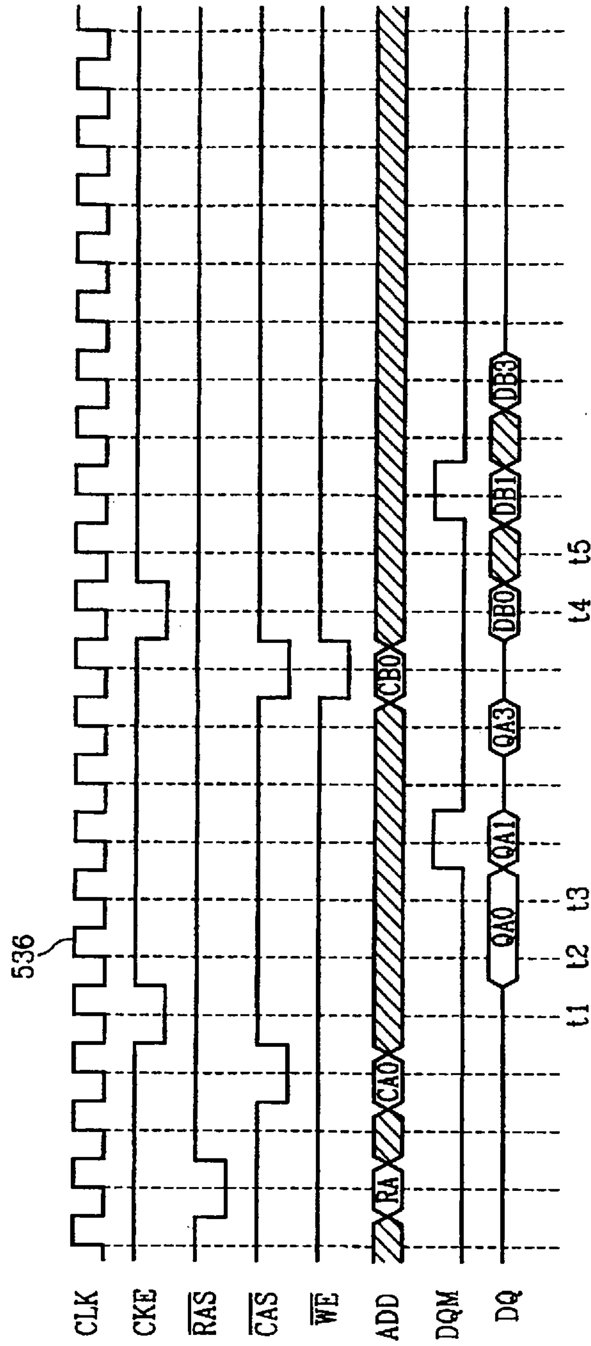

FIG. 55

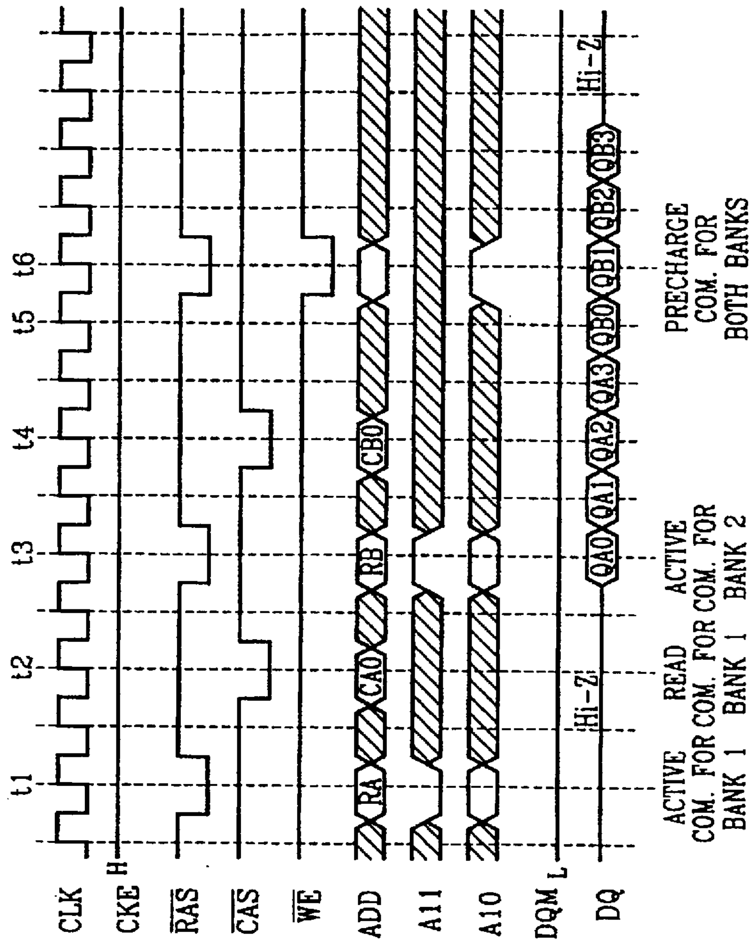

FIG. 56

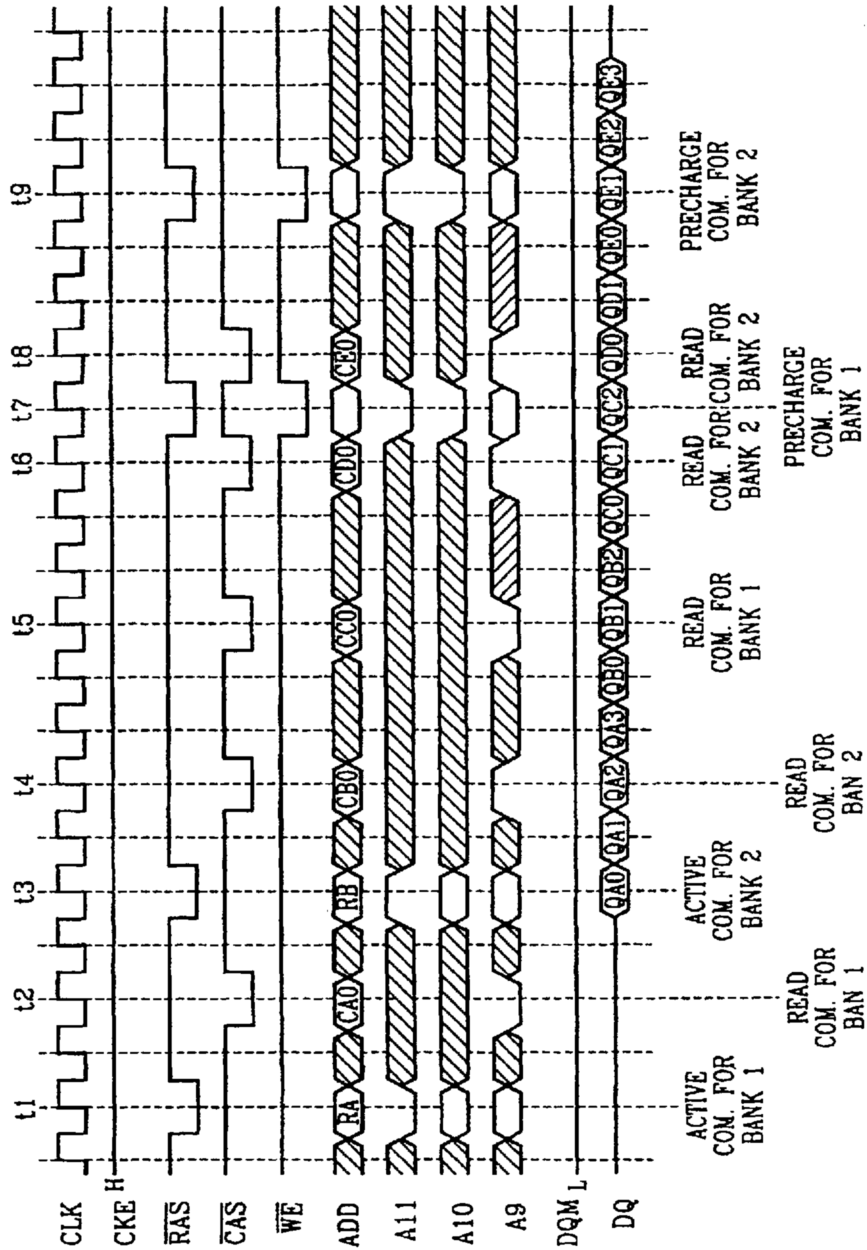

FIG. 57

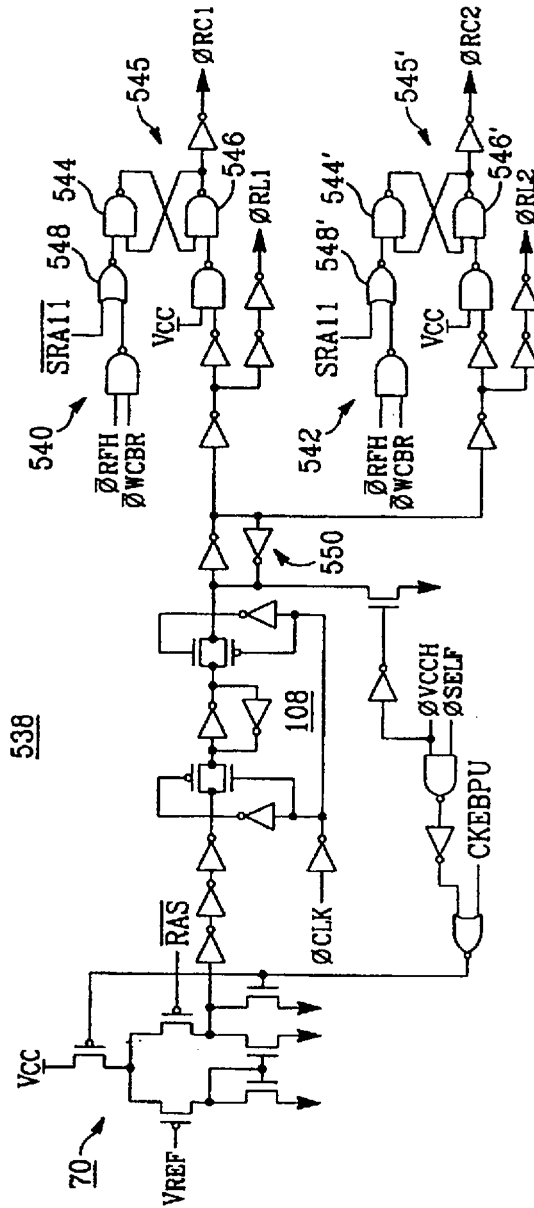

FIG. 58

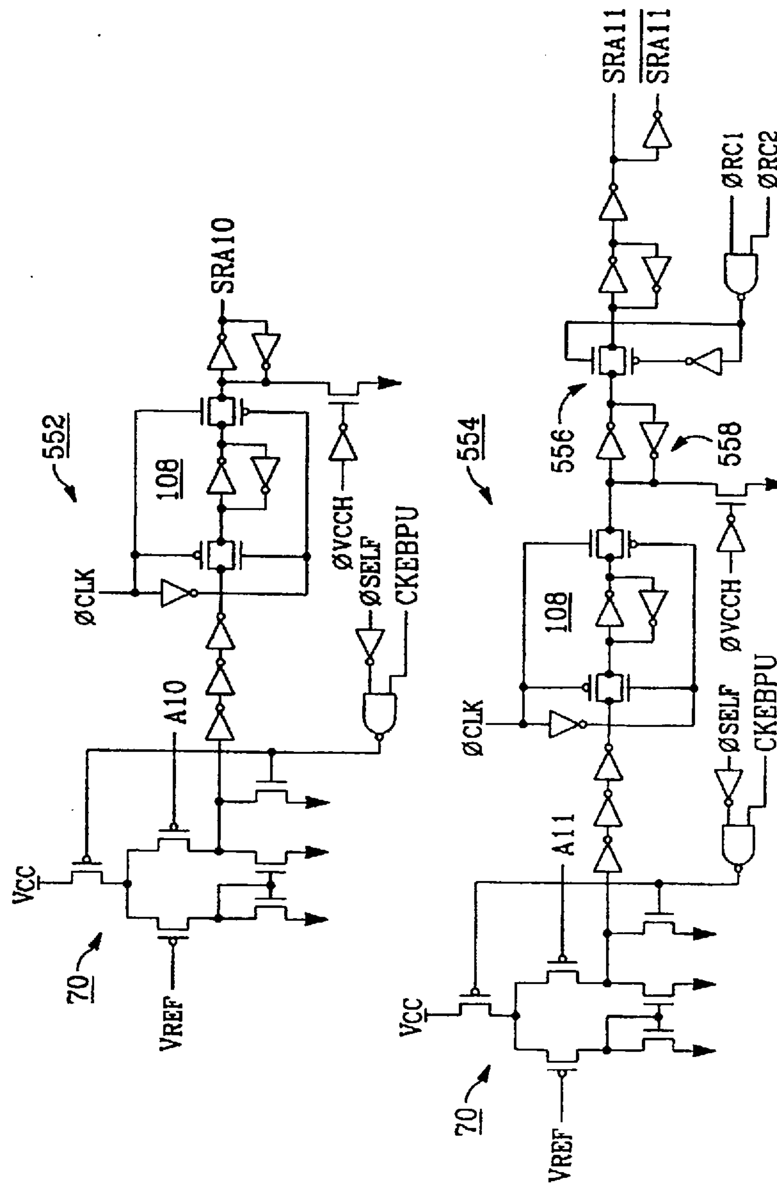

FIG. 59

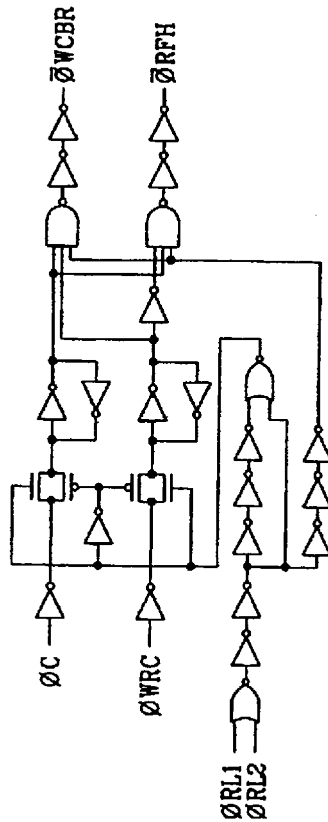

FIG. 60

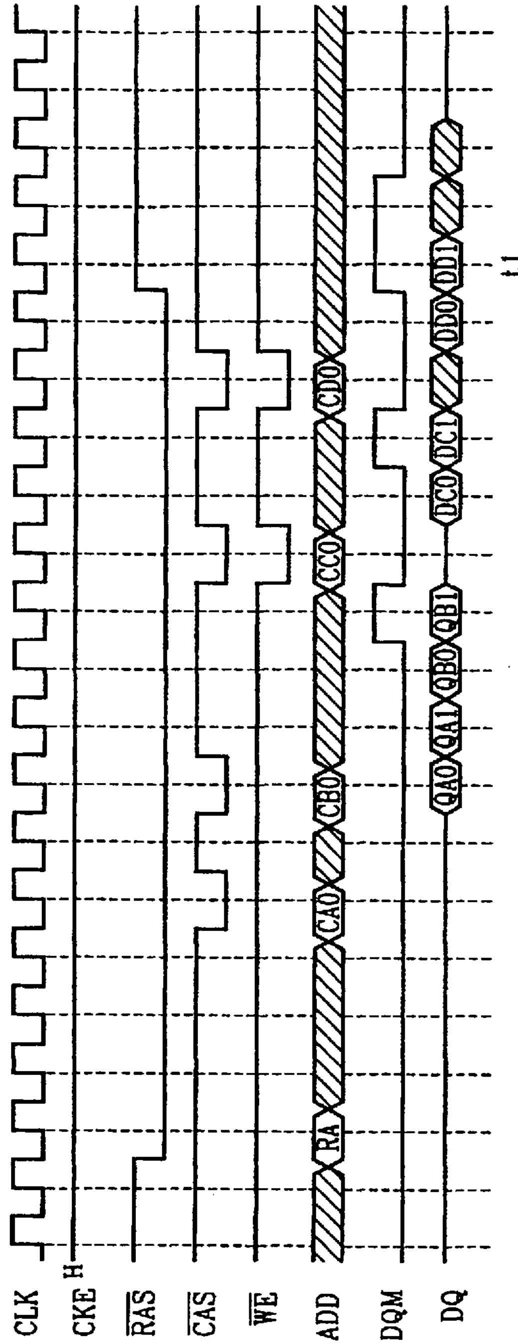

FIG. 61

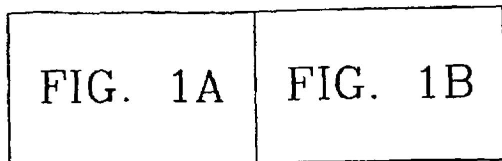

FIG. 1

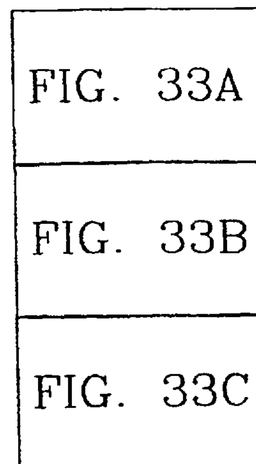

FIG. 33

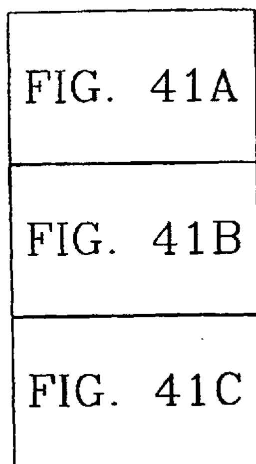

FIG. 41

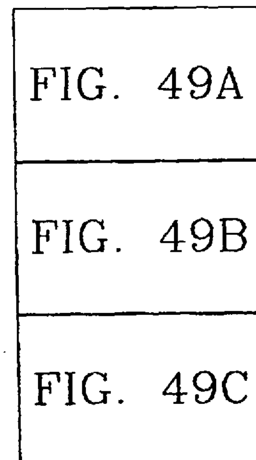

FIG. 49

FIG. 62

RX-13(

CIRCUIT IN A SEMICONDUCTOR MEMORY FOR PROGRAMMING OPERATION MODES OF THE MEMORY

This application is a continuation of application Ser. No. 08/130,138, filed Oct. 4, 1993 which is now abandoned.

FIELD OF THE INVENTION

The present invention relates to a semiconductor memory and, more particularly, to a synchronous dynamic random access memory which is capable of accessing data in a memory cell array disposed therein in synchronism with a system clock from an external system such as a central processing unit (CPU).

BACKGROUND INFORMATION

A computer system generally includes a CPU for executing instructions on given tasks and a main memory for storing data, programs or the like requested by the CPU. To enhance the performance of the computer system, it is basically requested to increase the operating speed of the CPU and also make an access time to the main memory as short as possible, so that the CPU can operate at least with no wait states. Operation clock cycles of modern CPUs such as recent microprocessors are shortening more and more as clock frequencies of 33, 66, 100 MHZ or the like. However, the operating speed of a high density DRAM, which is still the cheapest memory on a price-per-bit base and using as a main memory device, has not been able to keep up with that of the CPU being speeded up. DRAM inherently has a minimum $\overline{RAS}$ access time, i.e., the minimum period of time between activation of $\overline{RAS}$, upon which the signal $\overline{RAS}$ changes from a high level to a low level, and the output of data from a chip thereof with column addresses latched by activation of $\overline{CAS}$. Such a $\overline{RAS}$ access time is called a $\overline{RAS}$ latency, and the time duration between the activation of the signal $\overline{CAS}$ and the output of data therefrom called a $\overline{CAS}$ latency. Moreover, a precharging time is required prior to re-access following the completion of a read operation or cycle. These factors decrease the total amount of operation speed of the DRAM, thereby causing the CPU to have wait states.

To compensate for the gap between the operation speed of the CPU and that of the main memory like the DRAM, the computer system includes an expensive high-speed buffer memory such as a cache memory which is arranged between the CPU and the main memory. The cache memory stores information data from the main memory which is requested by the CPU. Whenever the CPU issues the request for the data, a cache memory controller intercepts it and checks the cache memory to see if the data is stored in the cache memory. If the requested data exists therein, it is called a cache hit, and high-speed data transfer is immediately performed from the cache memory to the CPU. Whereas if there is no presence therein, it is called a cache miss, and the cache memory controller reads out the data from the slower main memory. The read-out data is stored in the cache memory and sent to the CPU. Thus, a subsequent request for this data may be immediately read out from the cache memory. That is, in case of the cache hit, the high-speed data transfer may be accomplished from the cache memory. However, in case of the cache miss, the high-speed data transfer from the main memory to the CPU cannot be expected, thereby incurring wait states of the CPU. Thus, it is extremely important to design DRAMs serving as the main memory to accomplish high-speed operations.

The data transfer between DRAMs and the CPU or the cache memory is accomplished with sequential information or data blocks. To transfer the continuous data at a high speed, various kinds of operating modes such as page, static column, nibble mode or the like have implemented in the DRAM. These operating modes are disclosed in U.S. Pat. Nos. 3,969,706 and 4,750,839. The memory cell array of the DRAM with the nibble mode is divided into four equal parts so that a plurality of memory cells can be made access with the same address. Data is temporarily stored in a shift register to be sequentially read out or written into. However, since the DRAM with the nibble mode cannot continuously transfer more than 5-bit data, the flexibility of the system design cannot be offered upon the application to high-speed data transfer systems. The page mode and the static column mode, after the selection of the same row address in a $\overline{RAS}$ timing, can sequentially access column addresses in synchronism with $\overline{CAS}$ toggling or cycles and with the transition detections of column addresses, respectively. However, since the DRAM with the page or the static column mode needs extra time, such as a setup and a hold times of the column address, for receiving the next new column address after the selection of a column address, it is impossible to access the continuous data at a memory bandwidth higher than 100 Mbits/sec., i.e., to reduce a $\overline{CAS}$ cycle time below 10 nsec. Also, since the arbitrary reduction of the $\overline{CAS}$ cycle time in the page mode cannot guarantee a sufficient column selection time to write data into selected memory cells during a write operation, error data may be written thereinto. However, since these high-speed operation modes are not operations synchronous to the system clock of the CPU, the data transfer system must use a newly designed DRAM controller whenever a CPU having higher speed is replaced. Thus, to keep up with high-speed microprocessors such as CISC and RISC types, the development of a synchronous DRAM is required which is capable of accessing the data synchronous to the system clock of the microprocessor at a high speed. An introduction to synchronous DRAMs appears with no disclosure of detailed circuits in the NIKKEI MICRODEVICES in April, 1992, Pages 158–161.

To increase the convenience of use and also enlarge the range of applications, it is more desirable to allow an on-chip synchronous DRAM to not only operate at various frequencies of the system clock, but also be programmed to have various operation modes such as a latency depending on each clock frequency, a burst length or size defining the number of output bits, a column addressing way or type, and so on. Examples for selecting an operation mode in DRAM are disclosed in U.S. Pat. No. 4,833,650 issued on May 23, 1989, as well as in U.S. Pat. No. 4,987,325 issued on Jan. 22, 1991 and assigned to the same assignee. These prior art patents disclose technologies to select one operation mode, such as page, static column and nibble modes. Selection of the operation mode in these prior art patents is performed by cutting off fuse elements by means of a laser beam from an external laser apparatus or an electric current from an external power supply, or by selectively wiring bonding pads. However, in these prior technologies, once the operation mode had been selected, the selected operation mode cannot be changed into another operation mode. Thus, the prior art does not permit changes between operation modes even if subsequently required.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a synchronous dynamic random access memory in which input/output of data is synchronous with an external system clock.

Another object of the present invention is to provide a synchronous dynamic random access memory with high performance.

Still another object of the present invention is to provide a synchronous dynamic random access memory which is capable of operating at a high data transfer rate.

A further object of the present invention is to provide a synchronous dynamic random access memory which is able of operating at various system clock frequencies.

Still a further object of the present invention is to provide a synchronous dynamic random access memory in which the number of input or output data may be programmed.

Another object of the present invention is to provide a counter circuit in which a counting operation can be performed in either binary or interleave mode.

Still another object of the present invention is to provide a semiconductor memory which can prohibit unnecessary internal operations of the memory chip regardless of the number of input or output data.

A further object of the present invention is to provide a semiconductor memory which can set various operation modes.

Still a further object of the present invention is to provide a semiconductor memory including a data transfer circuit for providing precharge and data transfer operable at a high data transfer rate.

Another object of the present invention is to provide a semiconductor memory which includes at least two memory banks whose operation modes can be set in on-chip semiconductor memory.

According to an aspect of the present invention, a semiconductor memory formed on a semiconductor chip having various operation modes, includes address input circuit for receiving external address designating at least one of the operation modes to the chip, a circuit for generating a mode set control signal in a mode set operation; and a circuit for storing codes based on the external address in response to the mode set control signal and producing an operation mode signal representing the operation mode determined by the codes.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features, and advantages of the present invention are better understood by reading the following detailed description of the invention, taken in conjunction with the accompanying drawings, wherein:

FIGS. **1A** and **1B** show a schematic plane view of various component parts formed on the same semiconductor chip of a synchronous DRAM according to the present invention;

FIG. **2** is a diagram showing an arrangement relationship with one of sub-arrays in FIG. **1** and input/output line pairs coupled thereto;

FIG. **3** is a schematic block diagram showing a row control circuit according to the present invention;

FIG. **4** is a schematic block diagram showing a column control circuit according to the present invention;

FIG. **5A**, **5B**, **5C**, and FIG. **5D** are diagrams showing various commands used in operations of a pulse $\overline{RAS}$ and a level $\overline{RAS}$, respectively;

FIG. **6** is a schematic circuit diagram showing a clock (CLK) buffer according to the present invention;

FIG. **7** is a schematic circuit diagram showing a clock enable (CKE) buffer according to the present invention;

FIG. **8** is an operation timing diagram for the CLK buffer and the CKE buffer respectively showing in FIG. **6** and FIG. **7**;

FIG. **9** is a schematic circuit diagram showing a multifunction pulse $\overline{RAS}$ input buffer according to the present invention;

FIG. **10** is a timing diagram for column control signals or clocks used in the present invention;

FIG. **11** is a schematic circuit diagram for a high frequency clock generator for generating multiplied clocks upon precharging according to the present invention;

FIG. **12** is a schematic circuit diagram for a column address buffer according to the present invention;

FIG. **13** is a schematic block diagram for an operation mode setting circuit according to the present invention;

FIG. **14** is a schematic circuit diagram for a mode set control signal generating circuit in FIG. **13**;

FIG. **15A**, FIG. **15B** and FIG. **15C** are a schematic circuit diagram for an address code register in FIG. **13**;

FIG. **16** is a schematic circuit diagram for a latency logic circuit in FIG. **13**;

FIG. **17** is a schematic circuit diagram for a burst length logic circuit in FIG. **13**;

FIG. **18** is a circuit diagram showing an auto-precharge control signal generating circuit according to the present invention;

FIG. **19** is a schematic circuit diagram for a row master clock generating circuit for generating a row master clock ϕ_{Ri} according to the present invention;

FIG. **20** is a timing diagram showing timing relationship for a mode set and an auto-precharge according to the present invention;

FIG. **21** is a circuit diagram showing a circuit for producing signals to enable the generation of column control signals;

FIG. **22** is an operation timing diagram for the high frequency clock generator of FIG. **11**;

FIG. **23** is a diagram showing a circuit block diagram on a data path associated with one of data buses according to the present invention;

FIG. **24** is a schematic circuit diagram for an I/O precharge and selection circuit according to the present invention;

FIG. **25** is a schematic circuit diagram for a data output multiplexer according to the present invention;

FIG. **26** is a schematic circuit diagram for a data output buffer according to the present invention;

FIG. **27** is a detail circuit diagram for a data input demultiplexes according to the present invention;

FIG. **28** is a schematic circuit diagram for a PIO line driver according to the present invention;

FIG. **29** is a schematic circuit diagram for a $\overline{CAS}$ buffer according to the present invention;

FIG. **30** is a schematic circuit diagram for a $\overline{WE}$ buffer according to the present invention;

FIG. **31** is a schematic circuit diagram for a DQM buffer according to the present invention;

FIG. **32** is a timing diagram showing the operation of the DQM buffer if FIG. **31**;

FIG. **33A** to FIG. **33C** are a timing diagram showing a writing operation according to the present invention;

FIG. **34** is a schematic circuit diagram for a column address buffer according to the present invention;

FIG. **35** is a schematic block diagram for a column address counter according to the present invention;

FIGS. 36A and 36B are schematic circuit diagram for each stage which constitutes a first counting portion in FIG. 35;

FIG. 37 is a timing diagram showing the operation of the circuit of FIG. 36A;

FIG. 38 is a schematic block diagram for a column decoder according to the present invention;

FIG. 39A is a schematic circuit diagram for a first predecoder in FIG. 38;

FIG. 39B is a schematic circuit diagram for a second predecoder in FIG. 38;

FIG. 40 is a schematic circuit diagram for one of main decoders in FIG. 38;

FIG. 41A FIG. 41B and FIG. 41C are a timing diagram showing a reading operation according to the present invention;

FIG. 42 and FIG. 43 are schematic circuit diagrams for a burst length detection circuit in FIG. 4;

FIG. 44 is a schematic circuit diagram for a column address reset signal generator in FIG. 4;

FIG. 45 is a schematic block diagram for a transfer control counter in FIG. 4;

FIG. 46 is a schematic circuit diagram for a read data transfer clock generator in FIG. 4;

FIG. 47 is a schematic circuit diagram showing a circuit for generating a signal ϕ_{CL} using in the data output multiplexer of FIG. 25;

FIG. 48 is a schematic circuit diagram for a write data transfer clock generator in FIG. 4;

FIG. 49A FIG. 49B and FIG. 49C are a timing diagram for a $\overline{CAS}$ interrupt write operation according to the present invention;

FIG. 50 is a schematic circuit diagram showing a circuit for generating control signals precharging I/O lines and PIO lines according to the present invention;

FIG. 51 is a schematic circuit diagram showing a circuit for generating control signals precharging DIO lines according to the present invention;

FIG. 52 is a schematic circuit diagram showing a circuit for generating bank selection signals using in the PIO line driver of FIG. 28;

FIG. 53 is a schematic circuit diagram showing a control circuit for generating control signals being used in the data output buffer of FIG. 26;

FIG. 54, FIG. 55, FIG. 56 and FIG. 57 are timing diagrams showing the timing relationship according to various operation modes in the synchronous DRAM using the pulse $\overline{RAS}$;

FIG. 58 is a schematic circuit diagram for a $\overline{RAS}$ buffer using in the level $\overline{RAS}$;

FIG. 59 is a schematic circuit diagram for a special address buffer according to the present invention;

FIG. 60 is a schematic circuit diagram showing a control circuit for generating a mode set master clock and a refresh master clock which use in the level $\overline{RAS}$;

FIG. 61 is a timing diagram showing the operation timing relationship in the synchronous DRAM using the level $\overline{RAS}$; and

FIG. 62 is a diagram showing the manner in which the separate sheets of drawings of FIG. 1A and FIG. 1B, FIG. 33A to FIG. 33C, FIG. 41A to FIG. 41C, and FIG. 49A to FIG. 49C are combined.

DETAILED DESCRIPTION OF THE INVENTION

Preferred embodiments of the present invention will be discussed referring to the accompanying drawings. In the drawings, it should be noted that like elements represent like symbols or reference numerals, wherever possible.

In the following description, numerous specific details are set forth such as the number of memory cells, memory cell arrays or memory banks, specific voltages, specific circuit elements or parts and so on in order to provide a thorough understanding of the present invention. It will be obvious to those skilled in the art that the invention may be practiced without these specific details.

The synchronous DRAM in its presently preferred embodiment is fabricated employing a twin well CMOS technology and uses n-channel MOS transistors having a threshold voltage of 0.6 to 0.65 volts, p-channel MOS transistors having a threshold voltage of –0.8 to –0.85 volts and power supply voltage Vcc of approximately 3.3 volts.

CHIP ARCHITECTURE

Referring to FIG. 1 comprising FIG. 1A and FIG. 1B, illustration is made on a schematic plane view for various element portions formed on the same semiconductor chip of a synchronous DRAM according to the present invention. The DRAM in the present embodiment is a 16,777,216 bit (16-Mbit) synchronous DRAM made up of 2,097,152 (2M) ×8 bits. Memory cell arrays are partitioned into a first bank 12 and a second bank 14, as respectively shown in FIG. 1A and FIG. 1B, in order to increase a data transfer rate. Each bank comprises an upper memory cell array 16T and a lower memory cell array 16B respectively positioned at upper and lower portions, each of which contains memory cells of 4,194,304 bits (4-Mbit). The upper and the lower memory cell arrays are respectively divided into left memory cell arrays 20TL and 20BL and right memory cell arrays 20TR and 20BR of 2-Mbit memory cells each, neighboring on their lateral sides. The left and the right memory cell arrays of the upper memory cell array 16T of each bank will be respectively referred to as a upper left memory cell array or a first memory cell array 20TL and a upper right memory cell array or a third memory cell array 20TR. Likewise, the left and the right memory cell arrays of the lower memory cell array 16B of each bank will be respectively referred to as a lower left memory cell array or a fourth memory cell array 20BR. Thus, each bank is divided into four memory cell arrays consisting of the first to the fourth memory cell arrays. The upper left and right memory cell arrays and the lower left and right memory cell arrays are respectively divided into 8 upper left submemory cell arrays (or upper left sub-arrays) 22TL1 to 22TL8, 8 upper right submemory cell arrays (or upper right sub-arrays) 22TR1 to 22TR8 and 8 lower right submemory cell arrays (or lower right sub-arrays) 22BR1 to 22BR8. Each of the sub-arrays has 256K-bit memory cells arranged in a matrix form of 256 rows and 1,024 columns. Each memory cell is of a known one-transistor one-capacitor type.

In each bank, a row decoder 18 is arranged between the upper memory cell array 16T and the lower memory cell array 16B. The row decoder 18 of each bank is connected with 256 row lines (word lines) of each sub-array. Word lines of respective one of the upper and the lower sub-array pairs 22TL1, 22BL1; 22TL2, 22BL2; . . . ; 22TR8, 22BR8 arranged in a symmetrical relationship with respect to the row decoder 18 are extending in opposite directions therefrom in parallel with a vertical direction. The row decoder 18 responsive to row addresses from a row address buffer selects one of sub-arrays and one of word lines of the respectively selected sub-arrays and provides a row driving potential on each selected word line. Thus, in response to

given row addresses in each bank, the row decoder 18 selects total four word lines: one word line selected in a selected one of the upper left sub-arrays 22TL1–22TL8, one word line selected in a selected one of the lower left sub-arrays 22BL1–22BL8, one word line selected in a selected one of the upper right sub-arrays 22TR1–22TR8 and one word line selected in a selected one of the lower right sub-arrays 22BR1–22BR8.

Column decoders 24 are respectively positioned adjacent to right side ends of the upper and the lower memory cell arrays 16T and 16B in the first bank 12 and to left side ends of the upper and lower memory cell arrays 16T and 16B in the second bank 14. Each of the column decoders 24 is connected to 256 column selection lines which are parallel in the horizontal direction and perpendicular to the word lines, serving as selecting one of the column selection lines in response to a column address.

I/O buses 26 are located adjacent to both side ends of the respective sub-arrays 22TL, 22BL, 22TR and 22BR, extending in parallel with the word lines. The I/O buses 26 between opposite side ends of sub-arrays are shared by these two adjacent sub-arrays. Each of the I/O buses 26 is composed of our pairs of I/O lines, each pair of which consists of two signal lines in the complementary relation and is connected with corresponding bit line pair via a column selection switch and a sense amplifier.

Referring now to FIG. 2, for purposes of simplicity, the drawing is represented which illustrates the arrangement of an odd numbered one of sub-arrays 22TL1 to 22TR8 in the upper memory cell array 16T and that of I/O buses associated therewith. A first or left I/O bus 26L and a second or right I/O bus 26R respectively run in parallel with wordlines WL0–WL255 at left and right ends of the sub-array 22. Each of the first and the second I/O buses 26L and 26R consists of first I/O line pairs which are composed of I/O line pairs I/O0, $\overline{I/O0}$ and I/O1, $\overline{I/O1}$, and second I/o line pairs which are composed of I/O line pairs I/O2, $\overline{I/O2}$ and I/O3, $\overline{I/O3}$. The sub-array 22 contains 1,024 bit line pairs 28 perpendicular to the word lines WL0–WL255 which are arranged in a folded bit line fashion. Memory cells 30 are located at crosspoints of word lines and bit lines. The bit line pairs 28 constituting the sub-array 22 are divided into a plurality of first bit line groups 28L1 to 28L256 arranged at odd locations and a plurality of second bit line groups 28R1 to 28R256 arranged at even locations. Each of the bit line groups has a given number of bit line pairs (2 bit line pairs in the present embodiment). The first bit line groups 28L are arranged to alternate with the second bit line groups 28R. Odd numbered bit line pairs (or first sub-groups) 28L1, 28L3, . . . , 28L255 and even numbered bit line pairs (or second sub-groups) 28L2, 28L4, . . . , 28L256 of the first bit line groups 28L are respectively connected with the first I/O line pairs and the second I/O line pairs of the first I/O bus 26L via corresponding sense amplifiers 32L and column selection switches 34L. In the same manner, odd numbered bit line pairs (or first sub-groups) 28R1, 28R3, . . . , 28R255 and even numbered bit line pairs (or second sub-groups) 28R2, 28R4, . . . , 28R256 of the second bit line groups 28R are respectively connected with the first I/O line pairs and the second I/O line pairs of the second I/O bus 28R via corresponding amplifiers 32R and column selection switches 34R. First column selection lines L0, L2, . . . and L254, which are connected with column selection switches associated with the first I/O line pairs I/O0, $\overline{I/O0}$ and I/O1, $\overline{I/O1}$ in left and right I/O buses 26L and 26R, are arranged in parallel to alternate with second column selection lines L1, L3, . . . and L255 which are connected to column selection switches associated with the second I/O line pairs I/O2, $\overline{I/O2}$ and I/O3, $\overline{I/O3}$ therein. Thus, in a read operation, after the selection of one word line, i.e., one page with row addresses, the first and the second I/O line pairs in the left and right I/O buses 26L and 26R provide continuous data, alternating data of two bits each by sequentially selecting column selection lines L0 to L255. Line pairs 36, which are connected with corresponding sense amplifiers 32L and 32R and are alternately running in opposite directions, are respectively connected with corresponding bit line groups 28L and 28R via corresponding sense amplifiers within sub-arrays adjacent to the first and second I/O buses 26L and 26R. That is, the first I/O line pairs and the second I/O line pairs of the first I/O bus 26L are respectively connected with odd numbered bit line pairs (or first sub-groups) and even numbered bit line pairs (or second sub-groups) of the first bit line groups of a left adjacent sub-array (not shown) via corresponding column selection switches 32L and corresponding sense amplifiers. In the same manner, the first I/O line pairs and the second I/O line pairs of the second I/O bus 26R are respectively connected with odd numbered bit line pairs (or first sub-groups) and even numbered bit line pairs (or second sub-groups) of the second bit line groups of a right adjacent sub-array (not shown) via corresponding column selection switches 32R and corresponding sense amplifiers. Thus, since bit line pairs of the respective sub-arrays are divided in the same manner as the first and second bit line groups of the sub-array 22 as shown in FIG. 2, I/O buses associated with the first bit line groups are alternately arranged with I/O buses associated with the second bit line groups. That is, each of first I/O buses positioned at odd locations is associated with the first bit line groups in two sub-arrays adjacent thereto while each of second I/O buses positioned at even locations is associated with the second bit line groups in two sub-arrays adjacent thereto. Regarding to the respective ones of the sub-arrays of FIG. 1, the connection relationship with the first and second I/O line pairs of the first and second I/O buses will be incorporated by the explanation made in connection with FIG. 2. The sense amplifier 32L and 32R may be of a known circuit which is composed of a P-channel sense amplifier, transfer transistors for isolation, an N-channel sense amplifier and an equalizing and precharging circuit. Thus, I/O buses 26 between adjacent two sub-arrays are common I/O buses for reading or writing data from/to the sub-array which is selected by the control of the isolation transfer transistors.

Returning to FIG. 1, in each bank, at the upper portion of the first and the third memory cell arrays 20TL and 20TR are respectively located I/O line selection and precharge circuits 38TL and 38TR and I/O sense amplifiers and line drivers 40TL and 40TR correspondingly connected, thereto, and likewise, at the lower portion of the second and the fourth memory cell arrays 20BL and 20BR are respectively located I/O line selection and precharge circuits 38BL and 38BR and I/O sense amplifiers and line drivers 40BL and 40BR correspondingly connected thereto. I/O line selection and precharge circuits 38TL, 38TR, 38BL and 38BR are respectively connected to alternating I/O buses 26 in corresponding memory cell arrays 20TL, 20TR, 20BL and 20BR. That is, I/O line selection and precharge circuits positioned at odd locations are respectively connected with I/O bus pairs of I/O buses disposed at odd locations in corresponding memory cell arrays, and I/O line selection and precharge circuits positioned at even locations are respectively connected with I/O bus pairs of even located I/O buses in corresponding memory cell arrays. Therefore, in each bank, each of circuits at the outer most side of the I/O line selection

and precharge circuits may access data to/from memory cells which are connected with first bit line groups in three sub-arrays, and odd positioned I/O line selection and precharge circuits and even positioned I/O line selection and precharge circuits, which are excluding the outer most I/O line selection and precharge circuits, are respectively associated with the first bit line groups and the second bit line groups. Each I/O line selection and precharge circuit **38** comprises an I/O bus selection circuit for selecting one of a pair of I/O buses connected thereto and an I/O line precharge circuit for precharging, when any one of first I/O line pairs I/O0, $\overline{I/O0}$ and I/O1, $\overline{I/O1}$ and second I/O line pairs I/O2, $\overline{I/O2}$ and I/O3, $\overline{I/O3}$ which constitute the selected I/O bus is transferring data, the other I/O line pairs.

I/O line selection and precharge circuits **38** are respectively connected to corresponding I/O sense amplifiers and line drivers **40** via PIO buses **44**. Each PIO bus **44** is connected with an I/O bus selected by corresponding I/O bus selection circuit. Thus, PIO buses **44** comprise four pairs of PIO lines like I/O buses **26**. Each I/O sense amplifier and line driver **40** comprises an I/O sense amplifier for amplifying data inputting via corresponding I/O bus selection circuit and PIO bus in a read operation, and a line driver for driving to an I/O bus selected by the I/O bus selection circuit data inputting via corresponding I/O bus selection circuit and PIO bus in a write operation. Thus, as discussed above, if data on any ones of the first and the second I/O line pairs inputs to the sense amplifier via corresponding PIO line pairs, PIO line pairs connected to the other I/O line pairs are precharged together with the I/O line pairs. Also, in the writing operation, when the driver **40** drives data to corresponding I/O line pairs via selected PIO line pairs, unselected PIO line pairs and their corresponding I/O line pairs start precharging.

At the upper most and the lower most ends of the synchronous DRAM chip, upper data buses **42T** and lower data buses **42B** are respectively running in parallel with the horizontal direction. Each of upper data buses **42T** and lower data buses **42B** consist of four data buses, each of which comprises four pairs of data lines which are the same number as above mentioned I/O bus and PIO bus. One side ends of four data buses DB0–DB3 constituting upper data buses **42T** and four data buses DB4–DB7 constituting lower data buses are respectively connected to data input/output multiplexers **46** coupled to input/output pads (not shown in the drawing) via input/output lines **47** and data input/output buffers **48**.

In each bank, I/O sense amplifiers and line drivers **40TL** associated with the first memory cell array **20TL** are alternately connected to first and second data buses **DB0** and **DB1**, and I/O sense amplifiers and line drivers **40TR** associated with the third memory cell array **20TR** are interleavely connected to third and fourth data buses DB2 and DB3. Likewise, I/O sense amplifiers and line drivers **40BL** associated with the second memory cell array 20BL are interleavely connected to fifth and sixth data buses DB4 and DB5, and I/O sense amplifiers and line drivers **40BR** associated with the fourth memory cell array **20BR** are interleavely connected to seventh and eighth data buses. Center I/O sense amplifiers and line drivers **43T** and **43B** are respectively connected to I/O buses between the first memory cell array 2OTL and the third memory cell array 2OTR and between the second memory cell array 20BL and the fourth memory cell array **20BR** in each bank. In each bank, center I/O sense amplifier and line driver **43T** at the upper portion comprises an I/O sense amplifier for amplifying data on corresponding I/O bus to couple to the data bus DB1 or DB3 in response to a control signal in a write operation. Likely, center I/O sense amplifier and line driver **43** at the lower portion is connected to the fourth and the eighth data buses DB5 and DB7.

Now, assuming that sub-arrays **22TL3**, **22BL3**, **22TR3** and **22BR3** in the first bank **12** and one word line in their respective sub-arrays would be selected by the row decoder **18** responded by a row address, the row decoder **18** provides block information signals designating respective sub-arrays 22TL3, 22BL3, 22TR3 and 22BR3. Then, in a read operation, a control circuit, as will be discussed hereinbelow, generates sequential column addresses in response to an external column address and the column decoder **24** generates sequential column selection signals in response to this column address stream. Assuming that the first column selection signal is to select a column selection line **L0**, corresponding column selection switch **34** shown in FIG. **2** is turned on and data developed on corresponding bit line pairs is transferred to first I/O line pairs I/O0, $\overline{I/O0}$ and I/O1, $\overline{I/O0}$ of left and right I/O buses arranged at both ends of the respective selected sub-arrays. I/O line selection and precharge circuits **38TL**, **38BL**, **38TR** and **38BR** respond to the block information signals, and I/O line selection and precharge circuits associated with the selected sub-arrays 22TL3, 22B13, 22TR3 and 22BR3 thereby select the left and the right I/O buses associated therewith. Data on the first I/O line pairs in the left and the right I/O buses is transferred to corresponding data line pairs in corresponding data buses DB0–DB7 via corresponding PIO line pairs and corresponding sense amplifiers turned on by a control signal which is generated in response to the block information signals. However, at this time, I/O line pairs not transferring data, i.e., the second I/O line pairs and PIO line pairs connected thereto are all held in a precharging state by the I/O precharge circuits. Also, data line pairs not transferring data are being precharged by data input/output multiplexers **46** as will be explained hereinbelow. Then, if by the second column selection signal CSL1 on the column line L1 of the column address stream are turned on corresponding column selection switches, in the same manner as preciously discussed, data on corresponding bit lies is transferred via the second I/O line pairs in the left and the right I/O buses and corresponding PIO line pairs to data line pairs, whereas the first I/O line pairs, PIO line pairs and data line pairs connected thereto are precharged to transfer data from now on. If column selection signals CSL2 to CSL255 on column lines L2 to L255 following the column selection signal CSL1 on the column line L1 are sequentially received, the same operations as data transfer operations in case of the column selection signals CSL0 and CSL1 are performed repetitively. Thus, all data on bit line pairs which is developed from all memory cells coupled to selected word lines can be read out. That is, full page read-out is available. In the read operation, the first I/O line pairs and the second I/O line pairs transfer a plurality of data, alternating data transfer and precharge, and the first and the second data line pairs associated with the first and the second I/O line pairs, also, repeat data transfer and precharge periodically. The data output multiplexer connected to each data bus not only stores a plurality of data transferred in parallel via any one of the first and the second data line pairs, but also precharges the other data line pairs. Thus, each data output multiplexer provides continuous serial data in response to data selection signals, prefetching a plurality of data on the first and the second data line pairs with a predetermined period. The serial data outputs via corresponding data output buffer to data input/output pads in synchronism with a system clock.

Therefore, 8-bit parallel data continuously outputs every clock cycle thereof.

Write operation is performed in the inverse order of the read operation as discussed above. As will be explained in brief, serial input data outputs in synchronism with the system clock from data input buffers via data interleavely pads. The serial data from the data input buffers is interleavely transferred to the first and the second data line pairs of corresponding data buses in a plurality of parallel data every clock cycles of the system clock by means of respective data input demultiplexers. Data on the first and the second data line pairs is sequentially written into selected memory cells via corresponding line drivers, I/O buses selected by the I/O line selection circuits and corresponding bit line pairs. Data transfer and precharge of the first and the second line pairs are alternately effected every clock cycles in the same manner as those in the read operation.

Between the first and the second banks is arranged the control circuit **50** for controlling operations of the synchronous DRAM according to the present invention. The control circuit **50** serves to generate control clocks or signals for controlling the row and the column decoders **18** and **24**, I/O line selection and precharge circuits **38**, I/O sense amplifiers and line drivers **40** and **43**, data input/output multiplexers **46** and data input/output buffers **48**. The control circuit **50** may be classified into a row control circuit and a column control circuit. The row control circuit, the data path and the column control circuit will be separately discussed hereinbelow.

ROW CONTROL CIRCUIT

Conventional DRAMs are activated to perform the operation of read, write or the like by a logic level of $\overline{RAS}$, for example, a low level. This will be referred to as a level $\overline{RAS}$. The level $\overline{RAS}$ gives a certain information, for example, such information as the transition of $\overline{RAS}$ from high to low level indicates the activation thereof and the transition of $\overline{RAS}$ from low to high level indicates precharging. However, since the synchronous DRAM has to operate in synchronism with the system clock, above-mentioned commands using in the conventional DRAM cannot be employed in the synchronous DRAM. That is, since the synchronous DRAM needs to sample a command information at the leading edge or the falling edge of the system clock (sampling the command information in this embodiment is accomplished at the leading edge thereof), even if the level $\overline{RAS}$ is applied in the synchronous DRAM, commands of the conventional level $\overline{RAS}$ cannot be used therein.

FIG. **5a** and FIG. **5b** are timing diagrams representative of commands used in the synchronous DRAM of the present invention. FIG. **5a** represents various commands in case that $\overline{RAS}$ signal of pulse (hereinafter referred to as a pulse $\overline{RAS}$) is used, and FIG. **5b** various commands in case of the use of level $\overline{RAS}$. As can be seen in the drawings, when $\overline{RAS}$ is low and $\overline{CAS}$ signal and write enable signal $\overline{WE}$ are high at the leading edge of the system clock CLK, this means an activation. After the activation, at the leading edge of the system clock, the high level $\overline{RAS}$, the low level $\overline{CAS}$ and the high level $\overline{WE}$ indicate a read command. Also, after activation, at the leading edge of the system clock CLK, the high level $\overline{RAS}$, the low level $\overline{CAS}$ and low level $\overline{WE}$ represent a write command. When the low level $\overline{RAS}$, the high level $\overline{CAS}$ and the low level $\overline{WE}$ have been sampled at the leading edge of the clock CLK, a precharging operation is performed. An establishment of operation mode set command according to the feature of the present invention is accomplished at low levels of $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ at the leading edge of the clock CLK. A $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh command inputs when $\overline{RAS}$ and $\overline{CAS}$ hold at low levels and $\overline{WE}$ holds at a high level at the leading edge of the clock CLK. A self refresh command, which is a variation of the CBR refresh, inputs when $\overline{RAS}$ and $\overline{CAS}$ line at low levels and $\overline{WE}$ stays at a high level at successive three leading edges of the clock CLK.

In the same manner as conventional DRAM, the synchronous DRAM, also, inherently has the time period from the activation of $\overline{RAS}$ until the activation of $\overline{CAS}$, i.e. $\overline{RAS}$–$\overline{CAS}$ delay time t_{RCD} and the precharging time period prior to the activation of $\overline{RAS}$, i.e. $\overline{RAS}$ precharge time t_{RP}. To guarantee the read-out and the write-in of valid data, minimum values of tRCD and t_{RP} (respectively 20 ns and 30 ns in the synchronous DRAM of the present invention) are very important to memory system designers. To promote the convenience for system designers, it may be more preferred that the minimum values of t_{RCD} and t_{RP} are provided in the number of system clock cycle. For example, in case that the system clock frequency is 100 MHZ and the minimum values of t_{RCD} and t_{RP} are respectively 20 ns and 30 ns, clock cycles of t_{RCD} and t_{RP} respectively become 2 and 3. The row control circuit is means for generating signals or clocks for selecting word lines during the time period of t_{RCD}, developing to bit lines information data from memory cells in a read operation and precharging during the time period of t_{RP}.

FIG. **3** is a diagram representing a schematic block diagram for generating row control clocks or signals. Referring to the drawing, a clock buffer (hereinafter referred to a CLK buffer) **52** is a buffer for converting into an internal system clock ϕ_{CLK} of CMOS level in response to an external system clock CLK of TTL level. The synchronous DRAM executes various internal operations which are sampling signals from the external chip or data to the external chip at the leading edge of the clock CLK. The CLK buffer **52** generates a clock CLK faster than the phase of the clock CLK in response to CLK.

A clock enable (CKE) buffer **54** is a circuit for generating a clock masking signal ϕ_{CKE} in order to make the generation of the clock ϕ_{CLK} in response to an external clock enable signal CKE and the clock CLK. As will be discussed hereinbelow, the internal system clock ϕ_{CLK} disabled by the signal ϕ_{CKE} causes the internal operation of the chip to be frozen and input and output of data is thereby blocked.

A $\overline{RAS}$ buffer **56** receives the external signal $\overline{RAS}$, address signals SRA10 and SRA11, a signal ϕ_c from a $\overline{CAS}$ buffer and a signal ϕ_{WRC} from a $\overline{WE}$ buffer, thereby generating $\overline{RAS}$ clock ϕ_{RCi} for selectively activating banks in synchronous with the clock ϕ_{CLK} selectively or totally precharging the banks and automatically precharging after refreshing or operation mode programming. Wherein i is a symbol for representing bank. Also, the $\overline{RAS}$ buffer **56** generates signal ϕ_{RP} which represents the activation of $\overline{RAS}$ with the clock ϕ_{CLK}.

An operation mode set circuit **58** is responsive to the operation mode set command, signals ϕ_{RP}, ϕ_c and ϕ_{WRC} and address signals RA0–RA6f so as to set various operation modes, for example, operation modes for establishing a $\overline{CAS}$ latency, a burst length representing the number of continuous output data and an address mode ϕ_{INTEL} representing a scrambling way of internal column address. The operation mode set circuit **58** sets a default operation mode in which predetermined $\overline{CAS}$ latency, burst length and address mode are automatically selected upon the absence of the operation mode set command.

A row master clock generator **62** is responsive to the control signal ϕ_{RCi} and a latency signal CLj and generates a

row master clock ϕ_{Ri} which is based on the generation of clocks or signals associated with $\overline{RAS}$ chain in a selected bank. According to the characteristics of the present invention, the row master clock ϕ_{Ri} has time a delay depending on a designated $\overline{CAS}$ latency and such a time delay guarantees 2-bit data output synchronous to the system clock after the precharge command.

A row address buffer **60** receives the row master clock ϕ_{Ri}, external address signals **A0–A11** and a row address reset signal ϕ_{RARi} to generate row address signals RA0–RA11 in synchronism with the clock ϕ_{CLK}. The buffer **60** receive a count signal from a refresh counter in a refresh operation to provide row address signals RA0–RA11 for refreshing.

A row control signal generator **64** receives the row master clock ϕ_{Ri} and a block information signal BLS from the row decoder **18** to generate a boosted word line driving signal ϕ_x, a sensing start signal ϕ_s for activating the selected sense amplifier, a row address reset signal ϕ_{RARi} for resetting the column address buffer, a signal ϕ_{RAL} for powering on the column address buffer **344** and a signal ϕ_{RCDi} for informing the completion of clocks or signals associated with rows.

A column enable clock generator **66** receives the signal φRCDiand the row master clock ϕ_{Ri} to generate signals ϕ_{YECi} and ϕ_{YEi} for enabling column related circuits.

A high frequency clock generator **68** generates, in case that the frequency of the external system clock CLK is low and the 2-bit data output is also required in a read operation after a precharge command, a clock CNTCLK9 with a higher frequency than the clock CLK to prevent the reduction of precharge period. As will be discussed hereinbelow, since the column address generator generates column addresses with the clock CNTCLK9, the reduction of precharge period is prevented.

Hereinbelow, explanation will be made in detail on preferred embodiments of elements constituting the $\overline{RAS}$ chain clock generator.

1. CLK Buffer & CKE Buffer

FIG. 6 is a diagram representing a schematic circuit diagram for the CLK buffer **52** according to the present invention, and FIG. **7** is a schematic circuit diagram for CKE buffer **54** according to the present invention. FIG. **8** depicts an operation timing diagram for the CLK buffer **52** and the CKE buffer **54**.

Referring to FIG. **6**, a differential amplifier **70** compares the external system clock CLK with a reference potential V_{REF} (≈1.8 volts) and thereby converts the external signal CLK of TTL level into an internal signal of CMOS level, for example, a high level of 3 volts or a low level of 0 volt. Instead of the differential amplifier **70**, another input buffers can be used which can level shift from the TTL to the CMOS signal. As can be seen in FIG. **8**, the clock CLKA is of the signal inverted to the system clock CLK via the input buffer **70**, such as the differential amplifier, and gates, i.e., inverters **76** and NAND gate **78**. A flip-flop or a latch **80** which is composed of NOR gates **72** and **74** outputs a system clock of CMOS level when a clock masking signal ϕ_{CKE} is low. The output clock from the flip-flop **80** is supplied to a pulse width adjusting circuit **85** which is composed of a delay circuit **82** and a NAND gate **84**. Although the delay circuit **82** illustrates only inverters for the purpose of simplicity, a circuit comprising inverter and capacitor or other delay circuits may be used. Thus, when the signal ϕ_{CKE} is low, the internal system clock ϕ_{CLK} as shown in FIG. **8** outputs from the CLK buffer. However, when the signal ϕ_{CKE} is high, the output of the flip-flop **80** becomes low thereby to stop the generation of the clock ϕ_{CLK}. In FIG. **6**, inverter **89**, p-channel MOS transistor **90** and n-channel MOS transistors **91** and **94** are elements for providing an initial condition to proper nodes in response to a power-on (or power-up) signal ϕ_{VCCH} from a known power-on circuit. The power-on signal ϕ_{VCCH} maintains a low level until the power supply voltage Vcc reaches a sufficient level after the application of the supply voltage.

Referring to FIG. **7**, input buffer **70** converts the external clock enable signal CKE into a CMOS level signal. To prevent power consumption, operation of the input buffer **70** is inhibited by a self-refresh operation. The input buffer **70** provides an inverted CMOS level signal of the signal CKE on a line **90**. The inverted CKE signal is coupled to a shift register **86** for shifting with an inverted clock CLKA of the clock CLK. The output of the shift register **86** is coupled to the output terminal of the signal ϕ_{CKE} via a flip-flop **88** of NOR type and an inverter. The output terminal of the shift register **86** is coupled to the output terminal of a signal CKEBPU via inverters.

The clock enable signal CKE is of inhibiting the generation of the system clock ϕ_{CLK} with a low level of CKE, thereby to freeze the internal operation of the chip. Referring again to FIG. **8**, illustration is made on the signal CKE with a low level pulse for masking the CLK clock **98**. By the low level of CKE, the input line **90** of the shift register **86** maintains a high level. After a CLKA clock **100** goes to a low level, the output of the shift register **86** goes to a high level. Thus, ϕ_{CKE} and CKEBPU become a high level and a low level, respectively. Then, after a next CLKA clock **102** goes to a low level, the output of the shift register **86** changes to a low level, thereby causing the signal CKEBPU to go high. At this time, since the output of the flip-flop **88** is keeping a low level, ϕ_{CKE} maintains a high level. However, after a next CLKA clock **104** goes to a high level, ϕ_{CKE} goes to a low level. Thus, as discussed with FIG. **6**, ϕ_{CLK} clock corresponding to the clock **98** is masked with the high level of ϕ_{CKE}.

Since the internal operation of the synchronous DRAM operates in synchronism with the clock ϕ_{CLK}, the masking of ϕ_{CLK} causes the internal operation to be in a standby state. Thus, to prevent power consumption in the standby state, the signal CKEBPU is used to disable input buffers synchronous to ϕ_{CLK}. Accordingly, it should be appreciated that the signal CKE needs to be applied prior to at least one cycle of the masked clock CLK in order to mask it and has to hold a high level in order to carry out a normal operation.

2. $\overline{RAS}$ Buffer

The synchronous DRAM includes two memory banks **12** and **14** on the same chip to achieve a high speed data transfer rate. To achieve a high performance of the synchronous DRAM, control circuits need which is selectively controlling various operations for each bank. Accordingly, the $\overline{RAS}$ buffer is an input buffer combined with multifunctions according to a feature of the present invention.

FIG. **9** is a schematic circuit diagram showing the multifunction pulse $\overline{RAS}$ input buffer **56** according to the present invention. Referring to FIG. **9**, in the same manner as above discussed input buffers, input buffer **70** converts an external row address strobe signal $\overline{RAS}$ into an internal CMOS level signal. The input buffer **70** is disabled by a gate circuit **106** for gating system clock masking, self-refresh and power-on signals CKEBPU, ϕ_{VCCH} and ϕ_{SELF}. The CMOS level signal from the input buffer **70** is supplied to an input terminal **110** of a synchronization circuit **108** for providing to an output terminal **112** the $\overline{RAS}$ pulse ϕ_{RP} which synchronizes the CMOS level signal to the internal system clock ϕ_{CLK}. Thus, as shown in FIG. **10**, at times t_1 and t_3, $\overline{RAS}$ being at low

levels generates a $\overline{RAS}$ pulse ϕ_{RP} with high levels after a predetermined delay at the output terminal **112**.

In FIG. 9, the remaining circuit excluding the input buffer **70**, the synchronization circuit **109** and the gate circuit **106** is a multifunction control circuit **114** combined therewith to control the respective banks. Since n-channel transistors **148** and **150** are all turned on by ϕ_{VCCH} being at a low level during the power-on operation, the first $\overline{RAS}$ clock ϕ_{RC1} for the first bank **12** and the second $\overline{RAS}$ clock ϕ_{RC2} for the second bank **14** are all latched in initial conditions, i.e., low levels by means of latches **154** and **156**.

To activate the first bank **12** and at the same time, to inactivate the second bank **14**, at a time t_1 as shown in FIG. **10**, external address signal ADD with address A_{11} being at a low level is supplied to the chip. Then, an address buffer, as will be discussed hereinbelow, generates an address signal SRA11 of a low level ($\overline{SRA11}$ of a high level) with the address signal ADD. On the other hand, at the time t_1, since both $\overline{CAS}$ and $\overline{WE}$ keep high levels, ϕ_c and ϕ_{WRC} hold low levels as will be discussed hereinbelow. Thus, NOR gates **116** and **126** output low levels and NAND gates **122** and **124** output high levels. Then, NAND gates **128** and **130** output a high level and a low level, respectively. When the pulse ϕ_{RP} goes to a high level, NAND gate **132** goes to a low level and NAND gates **134** to **138** go to high levels. Then, p-channel transistor **140** is turned on and p-channel transistor **144** and n-channel transistors **142** and **146** keep off states. Thus, latch **54** stores a low level. On the other hand, when ϕ_{RP} goes to a low level, all of NAND gates **132** to **138** go to high levels, thereby turning off transistors **140** to **146**. As a result, the first $\overline{RAS}$ clock ϕ_{RC2} maintains a low level by means of the latch **156** which had been initially storing the high level. Thus, the first bank **12** is activated by the clock ϕ_{RC1}, thereby performing a normal operation such as a read or a write operation. However, the second bank **14** is not activated by the low level clock ϕ_{RC2}.

On the other hand, to access the synchronous DRAM at a high transfer rate, the second bank can be activated during the activation of the first bank. It can be accomplished by activating the second bank, applying the address A_{11} being at a high level after the activation of the first bank. Then, the address signal SRA11 becomes a high level ($\overline{SRA11}$ becomes a low level). In the same manner as discussed above, NAND gate **136** outputs a low level and all of NAND gates **132**, **134** and **138** output high levels. Thus, ϕ_{RC1} is maintaining the previous state, i.e., the high level and ϕ_{RC2} goes to a high level. As a result, all of the first and the second banks stay in activation states.

During the read or the write operation of the second banks, the first bank may also be precharged. When or before the precharge command is issued at time t_3 as shown in FIG. **10**, external address signal A_{10} and A_{11}, which are all low levels, are applied to corresponding address pins of the chip. Then, address signals SRA10 and SRA11 become low levels ($\overline{SRA11}$ becomes a high level). After the command, ϕ_{RP} and ϕWRC go to high levels and ϕ_c is at a low level. Consequently, when ϕ_{RP} goes high, NAND gate **134** goes to a low level and all of NAND gates **132**, **136** and **138** maintain high levels. Thus, the transistor **142** is turned on an transistors **140**, **144** and **146** maintain off states. The latch **154** stores a high level and ϕ_{RC1} becomes a low level. However, ϕ_{RC2} maintains the previous state of the high level by means of the latch **156**. As a result, ϕ_{RC1} of the low level causes the first bank to be precharged during performing data access from the second bank **14**. Likewise, a precharge operation of the second bank may be accomplished by applying the precharge command, address signal A_{10} being at a low level and address signal A_{11} being at a high level.

On the other hand, a simultaneous precharge operation of both the first and the second bank **12** and **14** may be accomplished by applying the precharge command and an address A_{10} being at a high irrespective of a logic level of the address A_{11}. Then, in the same manner as discussed above, NAND gates **134** and **138** output low levels and NAND gates **132** and **136** output high levels. Thus, transistors **142** and **146** are turned on and transistors **140** and **144** maintain off states. As a result, latches **154** and **156** store precharge information being at high levels, respectively and both ϕ_{RC1} and ϕ_{RC2} become low levels.

A CBR refresh command is issued by $\overline{RAS}$ being at the low level and $\overline{CAS}$ being at the high level as shown in FIG. *5a*. Thus, the high level signal ϕ_c and the low level signal ϕ_{WRC} input to the multifunction control circuit **114**. In this case, NAND gate **124** and NOR gate **126** output low levels irrespective of logic levels of the address A_{10} and A_{11}. Consequently, NAND gates **132** and **136** output low levels and NAND gates **134** and **138** output high levels. Thus, transistors **140** and **144** are turned on and transistors **142** and **146** are turned off. Then, ϕ_{RC1} and ϕ_{RC2} become high levels and both banks thereby perform the CBR refresh operation. On the other hand, a selective CBR refresh operation for both banks can be accomplished by grounding one of two input terminals of NAND gate **124**. Then, in the same manner as discussed above, ϕ_{RC1} and ϕ_{RC2} can be selectively enabled according to a logic state of the address A_{11}. That is, a low level address A_{11} under the CBR refresh command causes only the first bank to be refreshed.

3. Row Address Buffer

FIG. **12** is a diagram showing a schematic circuit diagram from the row address buffer **60** according to the present invention. In the drawing, an input buffer **70** converts input address signal AI (I=0, 1, 2, . . . , 11) to address signal of CMOS level in the same way as discussed in connection with above-mentioned input buffers. A logic circuit **158** for generating a control signal RABPU to enable or disable the input buffer **70** is also illustrated in FIG. **12**. The control signal RABPU becomes a high level when both banks have activated or the system lock masking operation as enabled or the refresh operation has initiated, and the input buffer **70** is thereby disabled to prevent power consumption. Between the output terminal **161** of the input buffer **70** and a node **162** is connected a tristate inverter **160**. The inverter **160** lies in an off state by the refresh signal O_{RFH} being at a low level during the refresh operation. In a normal operation such as a read or a write operation, the inverter **160** outputs a row address signal synchronized with the internal system clock ϕ_{CLK}. The row address signal is stored in a latch **164**. A plurality of row address providing circuits, the number of which is determined by that of banks, are connected to a node **166**. Since two banks is used in the embodiment of the present invention, it should be appreciated that two row address providing circuits **168** and **170** are connected in parallel to the node **166**. The row address providing circuit **168** for the first bank **12** is comprised of a NOR gate **174**, inverters **176** and **180**, a transmission gate **172**, a latch **178** and NAND gates **182** and **184**. The row address providing circuit **170** for the second bank **14** has the same construction as the row address providing circuit **168**. A refresh address providing circuit **198** is connected to the circuits **168** and **170** and serves to supply to the row address providing circuits **168** and **170** a count value RCNTI from a refresh counter (not shown) in the refresh operation.

It is assumed that the first bank **12** was in inactive state while the second bank **14** was in normal state such as a read or a write operation. In this case, a first bank row master clock ϕ_{R1} and a first bank row address reset signal ϕ_{RAR1}

would be at low levels, and a second bank row master clock ϕ_{R2} and a second bank row address reset signal ϕ_{RAR2} would be at high levels. It is now further assumed that the first bank 12 is activated at a time t_1 as illustrated in FIG. 10. Then before the clock ϕ_{R1} goes to a high level, a row address from the external pin AI is stored in the latch 164 as previously described and the stored row address is then stored into the latch 178 via the transmission gate 172 turned on by low level signals of ϕ_{R1} and ϕ_{RAR1}. However, in this case, since the clock ϕ_{R2} continuously remains at the high level, the transmission gate 172' maintains the previous off state, thereby preventing from transferring the stored row address therethrough. When the clock ϕ_{R1} is then at the high level, the row address providing circuit 168 is isolated with the output of the latch 164 by means of the gate 172. When the first bank row address reset signal ϕ_{RAR1} then goes to a high level, NAND Gates 182 and 184 output the row address data stored in the latch 178 and its complementary data therein, respectively. Consequently, a row address RAI and its inverted row address $\overline{RAI}$ from the circuit 172 are fed to the row decoder in the first bank 12. It will be noted that, when ϕ_{R1} and ϕ_{R2} are both at high levels, the control signal RABPU becomes high by means of the logic circuit 158, thereby disabling the input buffer 70 in order to prevent the power consumption due to the active or normal operations of all banks.

On the other hand, in the refresh operation such as a CBR or a self refresh operation, the refresh signal O_{RFH} is at a low level and ϕ_{RFH} is at a high level. In case of 2-bank refresh operation, and ϕ_{R1} and ϕ_{R2} are also at high levels, as will be discussed in detail hereinbelow in connection with FIG. 19. Signals ϕ_{RAR1} and ϕ_{RAR2} are also at high levels. Thus, the input buffer 70 and tristate inverter 160 are both in off states and at the same time, transmission gates 172, 172' and 194 are in off states while transmission gates 188 and 188' are in on states. Thus, a count address signal RCNTI from a known address counter (not shown), which was stored into a latch 192 via the transmission gate 194 turned on by ϕ_{RFH} being at a low level prior to the refresh operation, are fed to the row decoder corresponding to each bank via transmission gates 188 and 188', latches 178 and 178' and NAND gates 182, 184, 182' and 184'. After that time, operations of selecting word lines of each row decoder and then refreshing memory cells thereon are of the same manners as conventional DRAMs.

Addresses SRA10 and SRA11 for use in the multifunction $\overline{RAS}$ buffer may use row addresses RA10 and RA11 from the row address buffer 60. However, since the addresses RA10 and RA11 are generated with some time delays, separated row address buffers which may operate in faster speed may be provided on the same chip for independently generating the addresses SRA10 and SRA11.

4. Operation Mode Set Circuit

The synchronous DRAM of the present invention is designed so that system designers choose desired ones of various operation modes in order to amplify the convenience of use and enlarge the range of applications.

FIG. 13 is a block diagram for the operation mode set circuit 58. A mode set control signal generator 200 generates a mode set signal ϕ_{MRS} in response to signals ϕ_C, ϕ_{RP} and ϕ_{WRC} generated upon the issuance of the operation mode set command. An address code register 202, in response to the power-on signal ϕ_{VCCH} from the power-on circuit 203 and the mode set signal ϕ_{MRS}, stores address codes MDST0 to MDST6 depending on addresses from the row address buffer and produces the codes MDST0 to MDST2 and MDST4 to MDST6 and a column addressing mode signal ϕ_{INTEL}. A burst length logic circuit 204 produces a burst length signal SZn generated with logic combination of the codes MDST0 to MDST2. Wherein n represents a burst length indicated as the number of system clock cycles. A latency logic circuit 206 produces a $\overline{CAS}$ latency signal CLj generated with logic combinations of the codes MDST4 to MDST6. Wherein j represents a $\overline{CAS}$ latency (or $\overline{CAS}$ latency value) indicated as the number of system clock cycles.

FIG. 14 is a diagram showing a schematic circuit diagram for the mode set control signal generator 200 and FIG. 20 is a timing diagram associated with the operation mode set or program.

In the present embodiment, programming the operation modes is accomplished by applying the operation mode set command and at the same time, addresses A_0 to A_7 to address input pins according to the following Table 1.

TABLE 1

$\overline{CAS}$ latency j				Column Addressing Way		Burst Length			n
A6	A5	A4	j	A3	Way	A2	A1	A0	n
0	0	1	1			0	0	1	2
0	1	0	2	0	Binary	0	1	0	4
0	1	1	3			0	1	1	8
1	0	0	4	1	Interleave	1	1	1	512

The $\overline{CAS}$ latency j related with a maximum system clock frequency is represented as the following Table 2.

TABLE 2

Maximum System Clock Frequency (MHZ)	$\overline{CAS}$ Latency j
33	1
66	2
100	3

It will be noted that values of $\overline{CAS}$ latency j in the above Tables represent the number of system clock cycles and $\overline{CAS}$ latency values related to maximum clock frequencies may be changed according to the operation speed of a synchronous DRAM.

For example, if a system designer want to design a memory system with a binary column addressing way and a continuous 8-word data access at 100 MHZ, the minimum selection value of the $\overline{CAS}$ latency j is 3. If the $\overline{CAS}$ latency value of 3 has been chosen, addresses A_0 to A_7 for setting the operation modes is 1, 1, 0, 0, 1, 1, 0 and 0, respectively. It has been already discussed that selecting one of both banks was address A_{11}. Remaining addresses thereof are irrelevant to logic levels.

After the selection of operation modes suitable for a data transfer system and then the determination of addresses for setting the operation modes, mode set programming of the synchronous DRAM is performed, applying the mode set command and the predetermined addresses to corresponding pins of the chip. Referring to FIG. 20, the mode set command and the addresses ADD is applied thereto at a time t_1. Then, ϕ_{RP} from the $\overline{RAS}$ buffer and signals ϕ_C and ϕ_{WRC} from a $\overline{CAS}$ buffer and a $\overline{WE}$ buffer as will be discussed later go to high levels. In the mode set control signal generator 200 as shown in FIG. 14, the signals ϕ_C, ϕ_{RP} and ϕ_{WRC} which are all high render a signal ϕ_{WCBR} to go low. When the row address reset signal ϕ_{RARi} is then at a high level, the row address buffer of NAND gate 208 are all at high levels, thereby causing the mode set signal ϕ_{MRS} to go high.

FIGS. 15A–15C are a diagrams showing circuit diagram for the address code register 202. The address code register

202 comprises first register units for storing second logic levels (low levels) upon the power-on and address signals RA_0, RA_2 to RA_4 and RA_6 in the mode set operation after the power-up in response to the node set signal ϕ_{MRS}, and second register units for storing first logic levels (high levels) upon the power-on and address signals RA_1 and RA_5 in the mode set operation after the power-up in response to the mode set signal ϕ_{MRS}. Each of the first register units illustration in FIG. 15*a* is comprised of a tristate inverter **210** including p-channel MOS transistors **212** and **214** and n-channel MOS transistors **216** and **218**, a latch **222** connected to an output terminal of the inverter **210** and p-channel MOS transistor **220** whose channel is connected between the power supply voltage Vcc and the output terminal and whose gate is coupled to the power-on signal ϕ_{VCCH}. Since the power-on signal ϕ_{VCCH} is low until the supply voltage Vcc reaches minimum voltages to carry on internal normal operation after the application thereof, i.e., on the power-on, each first register unit makes corresponding address code MDSTI or the register unit illustrated in FIG. 15*b* makes addressing mode signal ϕ_{INTEL} set at a low level on power-on by the conduction of p-channel MOS transistor **220**. Each second register unit illustrated in FIG. **15**C comprises a tristate inverter **210'** including p-channel MOS transistors **212'** and **214'** and n-channel MOS transistors **216'** and **218'**, an n-channel MOS transistor **219** whose channel is connected between an output terminal of the inverter **210'** and the reference potential (ground potential) and whose gate is coupled to an inverted signal of ϕ_{VCCH}, and a latch **222'** connected to the output terminal of the inverter **210'**. Each second register unit makes the address code MDST1 or MDST5 latched high upon the power-on. However, in the mode set operation after the power-up, i.e., after the supply potential Vcc reaches at least the minimum operating voltages, since ϕ_{VCCH} is high, inverters **210** and **210'** are turned on in response to the high level signal ϕ_{MRS} and latches **222** and **222'** then store row addresses RAI from the row address buffer **60**, thereby outputting address codes MDSTI having the same address values as the row addresses RAI. Thus, if the mode set program is performed, each address code of MDSTI is the same value as the corresponding address. MDST3 corresponding to the address signal RA_3 is the signal ϕ_{INTEL} which represents a way of column addressing. If A_3=0 (low level), the signal ϕ_{INTEL} becomes low and a column address counter as discussed hereinbelow counts in a binary increasing manner. If A_3=1 (high level), the signal ϕ_{INTEL} becomes high representing an interleave mode.

FIG. **16** is a diagram showing a schematic circuit diagram for the latency logic circuit **206** which selects to send to a high level only one of latency signals CL1 to CL4 with the logic combination of address codes MDST4 to MDST6 associated with the $\overline{CAS}$ latency. Upon the power-on, since MDST5 is high and MDST4 and MDST6 are low, only CL2 becomes high.

FIG. **17** is a diagram showing a schematic circuit diagram for the burst length logic circuit **204** for selecting one of signals $S\overline{Z2}$ to $S\overline{Z512}$, each of which represents a burst length, with the logic combination of address codes MDST0 to MDST2 associated with the burst length. For example, if address codes MDST0 to MDST2 are all at high levels, only the signal $S\overline{Z512}$ of $S\overline{Z2}$ to $S\overline{Z512}$ is high and signals SZ4 to SZ512 are all high. Thus, as will be discussed hereinbelow, continuous **512**-word (full page) outputs via data output buffer in response to the signals. Upon the power-on, since MDST1 is high and MDST0 and MDST2 are low, only the signals SZ4 and $S\overline{Z4}$ are high.

Consequently, selected operation modes are determined by the storage of corresponding addresses to latches **222** and **222'** when the mode set signal ϕ_{MRS} is at the high level. After the address codes have been stored to corresponding latches **222** and **222'**, an auto-charge operation is performed according to one characteristic feature of the present invention. By performing a high speed precharge without any separate precharge commands, precharging time is reduced and next operation such as the active operation is also performed immediately without a standby state.

FIG. **18** is a circuit diagram showing an auto-precharge control signal generator **223** for performing the auto-precharge upon the exit of self refresh or in the mode set program. The self refresh signal ϕ_{SELF} is at a high level in the self refresh operation and at a low level in remaining time excluding the self refresh operation. Thus, the output of NAND gate **224** is at a high level in the mode set program. When ϕ_{RARi} reaches to a high level as seen in FIG. **20**, the output of NOR gate **232** goes to a high level. At this time, ϕ_{CLK} is at a low level. When ϕ_{CLK} then goes to a high level, the output of NAND gate **226** goes from a low level to a high level after a time delay determined by a delay circuit **230**. Consequently, the auto-precharge control signal generator **223** produces an auto-precharge signal o_{AP} having a short low pulse after o_{MRS} have gone high. Likewise, upon completion of the self refresh operation, o_{SELF} goes from high to low and the circuit **223** then generates the auto-precharge signal o_{AP} having the short low pulse. Returning to FIG. **9**, the signal o_{AP} inputs to a NAND gate **152**. Thus, the NAND gate **152** produces a short high pulse with the short low pulse o_{AP}, thereby turning on n-channel transistors **148** and **150**. The latches **154** and **156** then store high levels, thereby causing ϕ_{SC1} and ϕ_{RC2} to go to low levels. Once either ϕ_{RC1} or ϕ_{RC2} goes to low levels, ϕ_{Ri} and ϕ_{RARi} goes to low levels in sequence and then the precharge operation is performed.

On the other hand, if the synchronous DRAM of the present invention is used without the mode set programming, i.e., in a default mode, p-channel transistors **220** and n-channel transistors **219** as shown in FIG. **15** are all turned on by the power-on signal ϕ_{VCCH} which is low upon the power-on. Thus, latches **222** store low levels and latches **222'** store high levels. Address codes MDST0, MDST2, MDST4 and MDST6 and ϕ_{INTEL} then become low levels and the codes MDST1 and MDST5 also become high levels. Consequently, in the default mode, $\overline{CAS}$ latency of 2, binary address mode and burst length of 4 are selected automatically.

5. Column Control Signal Generator

FIG. **19** is a diagram showing a schematic circuit diagram for a row master clock generator **62** for generating the row master clock ϕ_{Ri} in response to the $\overline{RAS}$ clock ϕ_{RCi} from the $\overline{RAS}$ buffer **56**. As shown in FIG. **10**, if the i-th bank is activated, ϕ_{RCi} goes to a high level and the i-th bank row master clock ϕ_{Ri} then goes to a high level via NOR gate **234** and inverters. However, if ϕ_{RCi} goes to a low level to precharge, ϕ_{Ri} goes to a low level after a different time delay according to each $\overline{CAS}$ latency. That is, when the value of the $\overline{CAS}$ latency j is 1, i.e., CL1=high and CL2=CL3=low, ϕ_{Ri} goes to the low level after a time delay passing delay circuits **236**, **238** and **240** mainly. When the value the $\overline{CAS}$ latency j was set to 2, ϕ_{Ri} goes to the low level after a time delay passing delay circuits **238** and **240** mainly. When the value of the $\overline{CAS}$ latency j was programmed to 3, ϕ_{Ri} goes to the low level after a time delay passing the delay circuit **240** mainly. Thus, the higher the frequency of system clock CLK, the shorter the time delay causing ϕ_{Ri} to go low.

Such time delays allow column selection signals to have a sufficient time margin before the beginning of precharge cycle in a write operation, thus correctly writing data into cells and also ensuring that continuous 2-bit data outputs via output pin after precharge command in a read operation. In the present embodiment, the time delay in case of j=1 is about 19 ns and the time delays in case of j=2 and j=3 are respectively about 6 ns and 3 ns.

The row control clock generator 62 as shown in FIG. 3 is a conventional logic circuit for generating clocks showing in the timing diagram of FIG. 10. The row address reset signal ϕ_{RARi} rises to a high level after the rising edge of ϕ_{Ri} and falls to a low level after the falling edge of ϕ_X. The word line driving signal ϕ_X rises to a high level after the rising edge of ϕ_{RARi} and falls to a low level after the falling edge of ϕ_{Ri}. The signal ϕ_S generated by the signal ϕ_X activates sense amplifiers selected with the block information signal BLS which is produced by decoding row addresses. Signal ϕ_{RAL} for enabling the column address buffers 344 goes to a high level after the rising edge of ϕ_{RARi} and goes to a low level after the falling edge of ϕ_{RCi}. Signal ϕ_{RCDi} for guaranteeing t_{RCD} goes to a high level after the rising edge of ϕ_S and goes to a low level after the falling edge of ϕ_{Ri}.

FIG. 21 is a schematic circuit diagram showing a logic circuit for generating signals ϕ_{YEi} and ϕ_{RECi} which enable $\overline{CAS}$ chain circuits. The signal ϕ_{YECi} is a delayed signal of ϕ_{RCDi}. Column enable signal ϕ_{YEi} is a signal having a timing as shown in FIG. 10 by gating of ϕ_{RCDi} and ϕ_{Ri}.

FIG. 11 is a schematic circuit diagram showing the high frequency clock generator according to the present invention which serves to multiply the frequency of the internal system clock upon the occurrence of precharge command where a low frequency external system clock such as an external system clock CLK of 33 MHZ or less in the present embodiment is used. The high frequency clock generator 68 comprises a circuit means 242 for generating a pulse depending on the precharge command, a gate 248 for logically summing the generated pulse with the internal system clock ϕ_{CLK} to generate a multiplied system clock and a transmission gate 252 for transferring the multiplied system clock in response to a predetermined latency.

Referring to FIG. 22 showing a timing diagram for read and precharge operations at a system clock CLK of 33 MHZ and a burst length of SZ4, precharge command for read-out bank is issued at time t_4. ϕ_{RCi} then goes from a high level to a low level and the output terminal A of the pulse generator 242 thereby outputs the pulse having a pulse width depending on a given time delay of a delay circuit 244 or 244'. This pulse is summed with the internal system clock ϕ_{CLK} by means of gates 246 to 248, thereby resulting in outputting a multiplied system clock via NAND gate 248. NOR gate 254 outputs a high level since CL1 is high and ϕ_{EWDC} is high only in a write operation. Thus, the output of the gate 248 outputs via turned-on transmission gate 252. At this time, a transmission gate 250 is off. Thus, since internal circuits operate with an internal system clock CNTCLK9 having the multiplied operation frequency after the precharge command, data output can be accomplished at a high speed and the precharge operation can be completed within a shorter time period after the precharge command. When the system clock CLK is above 33 MHZ, CL1 is at a low level. Thus, NOR gate 254 outputs a low level and the transmission gate 252 is off. Thus, the transmission gate 250 is turned off and CNTCLK9 is equal to the clock ϕ_{CLK}.

DATA PATHS

Data paths mean paths for outputting the developed data on bit lines via data output buffers in a read operation and feeding data being inputting via data input buffer to bit lines in a write operation. FIG. 23 shows circuit blocks associated with the data paths. For purposes of simplicity, it will be noted that the drawing shows circuit blocks on data paths associated with two sub-arrays.

Referring to FIG. 23, an I/O line selection and precharge circuit 38 is connected to the first I/O bus 26R associated with one of sub-arrays in one of memory cell arrays 20TL, 20BL, 20TR and 20BR and to the second I/O bus 26L associated with another sub-array therein as discussed along with FIG. 1. The circuit 38 receives the block information signal BLS for designating a sub-array including a word line selected by the row decoder 18 and in response to this information signal, serves to couple an I/O bus associated with the sub-array to PIO bus 256. Also, in a reading operation, since data presents on two pairs of four pairs of I/O lines in a selected I/O bus, the circuit 38 precharges remaining two pairs of the four pairs and PIO line pairs corresponding thereto.

FIG. 24 is a diagram showing a schematic circuit diagram for the I/O precharge and selection circuit 38. When the block information signal BLS from the row decoder 18 is at a low level, transfer switches 258 and 258' are all in off states and precharge circuits 260 are all turned on, thereby precharging I/O line pairs I/O_0, $\overline{I/O_0}$ to I/O_3 $\overline{I/O_3}$ to

$$VBL=\left(=\frac{1}{2}\ Vcc\right).$$

When the block information signal BLS is at a high level to transfer data, the switches 258 and 258' are in on states while the precharge circuits 260 are in off states. Now assume that I/O line pairs being to transfer data is the second I/O line pairs I/O_2, $\overline{I/O_2}$ and I/O_3, $\overline{I/O_3}$. Then, an I/O line precharge signal IOPR1 goes to a low level and its complement signal $\overline{IOPR1}$ goes to a high level. Thus, precharge circuits 262 and equalizing circuits 264 are turned on and the I/O line pairs I/O_0, $\overline{I/O_0}$ and I/O_1, $\overline{I/O_1}$ are then subsequently precharged and equalized to one threshold voltage below the supply voltage ($Vcc-V_t$). Wherein V_t is a threshold voltage of n-channel MOS transistor. However, since the precharge circuits 262' and equalizing circuits 264' associated with the I/O line pairs transferring data are all in off states, the data thereon is transferred to corresponding second PIO line pairs PIO_2, $\overline{PIO_2}$ and PIO_3, $\overline{PIO_3}$ via transfer switches 258' in the reading operation. In the same manner, data on PIO line pairs can transferred to corresponding I/O line pairs in write operations.

Returning to FIG. 23, an I/O sense amplifier 266 is activated to amplify data on the PIO bus 256 with a control signal ϕ_{IOSE} which is generated in response to the block information signal in a read operation. The I/O sense amplifier 266 is a know circuit which may be further including a latch for storing data at its output terminal.

The output of the I/O sense amplifier 266 is coupled to the data output multiplexer via the data bus DBI. It will be noted that the data bus DBI is one of data buses DBO to DB7, as shown in FIG. 1. Data line pairs DIO_0, $\overline{DIO_0}$ to DIO_3, $\overline{DIO_3}$ constituting the data bus DBI are correspondingly connected to PIO line pairs PIO_0, $\overline{PIO_0}$ to PIO_3, $\overline{PIO_3}$ constituting the PIO bus 256 via the sense amplifier 266.

FIG. 25 is a diagram showing a schematic circuit diagram for the data output multiplexer 268 which are comprised of precharge circuits 263*a* and 263*d*, latches 270, tristate buffers 272, first latches 274*a* to 274*d*, isolation switches 276, second latches 278*a* to 278*d* and data transfer switches 280, all of which are connected in series between the respective

data line pairs and a common data line pair CDL and $\overline{CDL}$. In the same manner as previously discussed about precharging of I/O line pairs I/O_0, $\overline{I/O_0}$ to I/O_3, $\overline{I/O_3}$, the precharge circuits **263***a* to **263***d* respond to a DIO line precharge signal DIOPR1 and its complement $\overline{DIOPR1}$ in a read operation, thereby causing two data line pairs transferring data to be prevented from precharging and the remaining data line pairs to be precharged. Latches **270** are respectively connected to the data lines DIO_3, $\overline{DIO_0}$ to DIO_3, $\overline{DIO_3}$ for storing data thereon. Tristate buffers **272** are respectively connected between the data lines DIO_0, $\overline{DIO_0}$ to DIO_3, $\overline{DIO_3}$ and first latches **274***a* to **274***d* for outputting inverted data thereon. However, tristate buffers connected with data lines being precharged are turned off. First latches **274***a*–**274***d* are respectively connected to output terminals of the tristate buffers **272** for storing data transferred via the data lines and the tristate buffers. Each of second latches **278***a* to **278***d* is connected in series with corresponding first latch via corresponding isolation switch. The second latches **278***a*–**278***d* are connected to a pair of common data lines $\overline{CDL}$ and CDL via corresponding data transfer switches **280**. The data transfer switches **280** are sequentially turned on in response to data transfer signals RDTP0 to RDTP3 which are high level pulses generated in sequence by column address signals, thereby sequentially outputting data stored in the second latches to the common data lines $\overline{CDL}$ and CDL via the first latches. Thus, as will be discussed in more detail hereinafter, data stored in serial registers **274** and **278** which are comprised of the first and the second latches **274***a* to **274***d* and **278***a* to **278***d* outputs in sequence on the common data lines $\overline{CDL}$ and CDL in response to the data transfer signals RDTP0 to RDTP3. In precharge operations of the data line pairs DIO_3, $\overline{DIO_0}$ to DIO_3, $\overline{DIO_3}$, since the tristate buffers **272** are held in off states, there is no destruction of data stored in the first and second registers **274** and **278**. However, where data stored in the second register **278** waits a long time before transmission via transfer switches **280**, i.e., in case of a long latency, if new data is transferred from data line pairs, the previous data stored in the second register **278** will be destroyed. Also, in case of use of a low frequency system clock, since the data transfer signals RDTP0 to RDTP3 are generated in synchronism with the system clock, such destruction of data may be occurred. Such data destruction due to data contention may substantially occur in a $\overline{CAS}$ interrupt read operation, i.e., such operation that before the completion of burst operation during a sequential data read operation based on the established burst length, an interrupt request is issued and a next sequential data read operation of the burst length is then carried out with no break or no wait, depending on the column address signals. Thus, to prevent an erred operation due to such data collection, the isolation switches **276** are connected between the first and the second latches. A control signal ϕ_{CL} for controlling the isolation switches is a high level pulse signal upon the $\overline{CAS}$ interrupt request in case of long $\overline{CAS}$ latency values of 3 and 4. The data lines $\overline{CDL}$ and CDL are connected to a known data output latch **282**.

Returning to FIG. **23**, the data output buffer **284** is connected with data output lines DO and $\overline{DO}$ from the data output multiplexer **268**, serving to feed to an input/output pad (not shown) a sequential data synchronous to the system clock which is defined in dependence upon a burst length in a read operation. There is a circuit diagram for the data output buffer **284** in FIG. 26. In the drawing, transfer switches **286** and **286'** respectively transfer data on the lines DO and $\overline{DO}$ to lines **288** and **290** in synchronism with a system clock ϕ_{CLK} of a given frequency (a frequency above 33 MHZ in the present embodiment), but in a synchronism with a system clock ϕ_{CLK} of the given frequency or below the given frequency. As will be explained hereinafter, a control signal ϕ_{YEP} is held high at a system clock of 33 MHZ or below 33 MHZ, i.e., at a $\overline{CAS}$ latency value of 1 and held low at a system clock of a frequency above 33 MH. Latches **92** are respectively connected to the lines **288** and **290** for storing data thereinto. A gate circuit **310** comprised of NAND gates **294** to **298** and transistors **300** and **302** is connected between the lines **288** and **290** and driving transistors **304** and **306**. The source of a p-channel MOS transistor **300** is coupled to a boosted Voltage Vpp from a known boost circuit for driving the transistor **304** without loss of its threshold. The gate circuit **310** serves to inhibit the output of data on the data input/out line **308** in response to a control signal ϕ_{TRST} which goes to a low level upon either completion of a burst read operation or occurrence of a data output masking operation.

Returning again to FIG. **23**, the data input buffer **312** is connected between a data line DI and the line **308** for converting external input data on the line **308** into CMOS level data and producing internal input data synchronous with the system clock ϕ_{CLK}. The data input buffer **312** may be comprised of previously mentioned input buffer for being enabled by a signal ϕ_{EWDC} which is at a high level in a write operation, and converting an external input data into a CMOS level data; and previously mentioned synchronization circuit for receiving the converted input data from the input buffer and then producing an internal input data synchronous with the system clock ϕ_{CLK}. Thus, whenever the clock ϕ_{CLK} goes to a high level in a write operation, the data input buffer **312** may be a buffer circuit for sequentially sampling a serially inputting data and then outputting a resulting serial data on the data line DI.

A data input demultiplexer **314** serves to sample the serial data on the output line DI of the data input buffer **312** with write data transfer signals being sequentially generated in synchronism with the system clock, thereby grouping into parallel data of predetermined bits (2-bit parallel data in the present embodiment) and supplying the grouping parallel data to corresponding data line pairs.

FIG. 27 is a diagram showing a schematic circuit diagram for the data input demultiplexer **314**. The demultiplexer **314** comprises selection switches **316***a* to **316***d* connected to the data line DI for sampling to transform the serial data on the data line DI into the parallel data in response to write data transfer signals WDTP0 to WDTP3. Each of latches **320***a* to **320***d* are connected to the corresponding selection switch for storing the sampled data. The outputs of the latches **320***a* to **320***d* are respectively connected to the data lines DIO_0, $\overline{DIO_0}$ to DIO_3, $\overline{DIO_3}$ via switches **322***a* to **322***d*, each of which is a NAND gate enabled in a write operation, and buffers **324***a* to **324***d*. The signal ϕ_{WR} gating NAND gates **322***a* to **322***d* is a signal being at a high level in a write operation. Each of the buffers **324***a* and **324***d* is a tristate inverter which is composed of a p-channel and an n-channel transistors **326** and **328**. P-channel transistors **318***a* to **318***d* respectively connected between the selection switches **316***a* and **316***d* and the latches **320***a* and **320***d* allow to, in response to the control signal WCA1 and its complement $\overline{WCA1}$, transfer a 2-bit parallel data, alternating two groups of first data line pairs DIO_0, $\overline{DIO_0}$ and DIO_1, $\overline{DIO_1}$ and DIO_3, $\overline{DIO_3}$, and at the same time, precharge in such a manner as precharging one group thereof while the other group thereof is transferring the parallel data. That is, when the control signal WCA1 is at a high level in a write operation, transistors **318***c* and **318***d* are in off states. Thus, data stored in latches **320***c* and **320***d* in response to the

signals WDTP2 and WDTP3 is transferred to the second data line pairs DIO_2, $\overline{DIO_2}$ and DIO_3, $\overline{DIO_3}$ via switches **322c** and **322d** and buffers **324c** and **324d**. At this time, since $\overline{WCA1}$ is low, transistors **318a** and **318b** are in on states, and buffers **324a** and **324b** are thereby in off states. Thus, the first data line pairs DIO_0, $\overline{DIO_0}$ and DIO_1, $\overline{DIO_1}$ are precharged to the supply potential Vcc by precharge circuits **263a** and **263b** shown in FIG. **25**. When WCA1 then goes to a low level, the transistors **318c** and **318d** goes to on states and the tristate buffers **324c** and **324d** then become off. Thus, likewise, the second data line pairs are precharged and the first data line pairs transfer a 2-bit parallel data.

Returning to FIG. **23**, data transferred via the bidirectional data bus DBI from the data input demultiplexer **314** is transferred to PIO line pairs **256** via the PIO line driver **330**.

FIG. **28** is a drawing showing a schematic circuit diagram for the PIO line driver **330** which comprises switches **332** responsive to a bank selection signal DTCPi and the block selection signal BLS for passing data on the data line pairs DIO_0, $\overline{DIO_0}$ to DIO_3, $\overline{DIO_3}$, buffers **334** connected between the switches **332** and the PIO line pairs PIO_0, $\overline{PIO_0}$ to PIO_3, $\overline{PIO_3}$ for amplifying data inputting via the switches **332** to supply to corresponding PIO line pairs, and precharge and equalizing circuits **336** each connected between two lines constructing each PIO line pair for precharging and equalizing the PIO line. It should be noted that the buffers **334** and the precharge and equalizing circuits **336** are the same constructions as the buffers **324a** to **324d** in FIG. **27** and the precharge and equalizing circuits **260**, **262**, **262'**, **264** and **264'** in FIG. **24**, and their operations are also associated with each other in a write operation. The PIO line driver **330** isolates between the data bus DBI and the PIO line pairs **256** with the signal DTCPi being at a low level in a read operation. However, in a write operation, data on the PIO line pairs **256**, which is transferred from the data bus DBI by means of the driver **330**, is transferred to corresponding I/O line pairs selected by the I/O precharge and selection circuit **38**. Since the data transmission is alternately accomplished every two pairs, if first I/O line pairs I/O_0, $\overline{I/O_0}$ and I/O_1, $\overline{I/O_1}$ of the left side I/O bus **26R**, which are correspondingly connected with the first PIO line pairs PIO_0, $\overline{PIO_0}$ and PIO_1, $\overline{PIO_1}$, are transferring data thereon, second PIO line pairs PI_2, $\overline{PIO_2}$ and PIO_3, $\overline{PIO_3}$ and second I/O line pairs I/O_2, $\overline{I/O_2}$ and I/O_3, $\overline{I/O_3}$ of the left I/O bus **26R** will be precharging.

COLUMN CONTROL CIRCUIT

Column control circuit is a circuit for generating control signals to control circuits related to the data paths.

FIG. **4** is a schematic block diagram showing the column control circuit according to the present invention. In the drawing, a $\overline{CAS}$ buffer **338** receives the external column address strobe signal $\overline{CAS}$ and the internal system clock ϕ_{CLK} and then generates pulse signals ϕ_C, ϕ_{CA}, BITSET and ϕ_{CP}.

A $\overline{WE}$ buffer **340** receives the external write enable signal $\overline{WE}$, the system clock ϕ_{CLK}, the pulse signals ϕ_C and ϕ_{CA} from the $\overline{CAS}$ buffer **338** and various control signals for generating write control signals ϕ_{WR}, ϕ_{EWDC} and ϕ_{WRC} in a write operation.

A DQM buffer **342** receives external signal DQM and the internal system clock ϕ_{CLK}, and then generates a data input/output masking signal ϕ_{DQM} to inhibit the input and the output of data.

A column address buffer **344** receives external column addresses A_0 to A_9 in synchronism with the system clock ϕ_{CLK}, thereby latching the column addresses in response to the pulse signal ϕ_{CA} from the $\overline{CAS}$ buffer **338**, and then producing column address signals ECA0 to ECA9.

A column address generator **346** is a counter circuit which is composed of a predetermined number of stages or bits (nine bits in the present embodiment). The counter may carry out counting operation either in a sequential or binary address mode or in an interleave address mode according to the column addressing mode signal ϕ_{INTEL}. Stages of the counter latch the column address signals from the column address buffer **344** in response to the pulse BITSET, and lower stages thereof associated with the burst length signal SZn perform the counting operation with the clock CNTCLK9, starting from the column address signals latched therein, and then produce successive column address signals according to a selected address mode. However, remaining stages produce initial column address signals latched therein. A column address reset signal ϕ_{CAR} is a signal for resetting the counter at the end of the burst length, i.e., after completion of a valid data output.

A burst length counter **350** is a conventional 9-stage (or 9-bit) binary counter counting pulses of the clock ϕ_{CLK} after being reset by the pulse signal BITSET from the $\overline{CAS}$ buffer. The counter **350** may also be reset by the column address reset signal ϕ_{CAR}. Since the BITSET signal is a pulse generated upon activation of $\overline{CAS}$, the counter **350** is re-count the number of pulses of the clock ϕ_{CLK} after the activation of $\overline{CAS}$. However, the signal ϕ_{CAR} is a signal stopping the counting operation of the counter **350**. Thus, in a $\overline{CAS}$ interrupt operation, the activation of $\overline{CAS}$ during the output of valid data renders the counting operation of the counter to restart.

A burst length detector **352** receives the counting value from the counter **350** and the burst length signal SZn from previously mentioned mode set circuit **58**, and then generates a signal COSR indicating of the end of the burst.

A column address reset signal generator **354** serves to generate the signal ϕ_{CAR} resetting the column address generator **346** in response to the burst end signal COSR.

A data transfer control counter **348** is a counter which receives address signals CA0, CA1, FCA0 and FCA1 and then generates column address signals RCA0 and RCA1 synchronous to the system clock ϕ_{CLK}. The clock CNTCLK9 is a clock artificially generated to shorten the precharge time when the system clock CLK of 33 MHZ or less is employed as previously discussed. Thus, in this case, the column address signals CA0 and CA1 is not signals synchronized with the system clock ϕ_{CLK}. Thus, the counter **348** exists in consideration of the reduction of the precharge time at the system clock of 33 MHZ or less. If unnecessary, the column address generator **346** receives ϕ_{CLK} in place of CNTCLK9, and a read and a write data transfer clock generators **356** and **358** may receive the column address signals CA0 and CA1 instead of the outputs of the counter **348**, i.e., RCA0 and RCA1.

The read data transfer clock generator **356** receives the column address signals RCA0 and RCA1 synchronized with the system clock ϕ_{CLK} and then generates read data transfer pulses RDTPm to output a serial data from the data output multiplexer **268** in a read operation.

The write data transfer clock generator **358** receives the signals RCA0 and RCA1 and then generates write data transfer pulses WDTPm to output a time multiplexed parallel data from the data input demultiplexer **314** in a write operation.

The write data transfer clock generator **358** receives the signals RCA0 and RCA1 and then generates write data

transfer pulses WDTPm to output a time multiplexed parallel data from the data input demultiplexer 314 in a write operation.

1. $\overline{CAS}$, $\overline{WE}$ and DQM Buffers

FIG. 29 is a drawing showing a schematic circuit diagram for the $\overline{CAS}$ buffer 338, and FIG. 33 is a drawing showing a timing diagram of a write operation employing system clock of 66 MHZ, burst length of 4 and $\overline{CAS}$ latency of 2.

In FIG. 29, an input buffer 70 is a circuit which is disabled in refresh and clock masking operations and converts input signals into internal CMOS level signals in read and write operations. A synchronization circuit 108 is connected to the input buffer 70 to synchronize the CMOS level $\overline{CAS}$ signal from the input buffer with the system clock ϕ_{CLK}. A pulse generator 360 is connected to the synchronization circuit 108 to generated control pulses ϕ_{CA}, ϕ_{CP} and BITSET. Referring to FIG. 33 comprised of FIGS. 33A and 33B, the pulses ϕ_C, ϕ_{CA}, ϕ_{CP} and BITSET are generated by the $\overline{CAS}$ pulse being at a low level at time t_3. The high level pulse width of ϕ_C is about one cycle of the system clock CLK, and the pulse width of ϕ_{CA} is about one half cycle of the clock CLK while the pulse widths of ϕ_{CP} and BITSET are about 5 to 6 nsec.

FIG. 30 is a drawing showing a schematic circuit diagram for the $\overline{WE}$ buffer 340. In the drawing, an input buffer 70 is a circuit for converting the external write enable signal $\overline{WE}$ into and internal CMOS level signal. A synchronization circuit 108 stores the level shift signal from the input buffer 70 into a latch 362 in synchronism with the system clock ϕ_{CLK}. The input of a latch 366 is coupled to the output of the latch 362 via a transfer switch 364 turned on by the activation of $\overline{CAS}$ for storing a high level thereinto in a write operation. A gate circuit 368 comprised of gates is connected to the output of the latch 366. A shift register 370 is connected to the gate circuit 368 for delaying one cycle of CLK after a write command. A pulse generator 378 generates a short high level pulse ϕ_{WRP} in a precharge cycle for resetting the shift register 370 and the latch 366. Referring to FIG. 33, when ϕ_{CA} is at a high level after issuance of a write command at time t_3, the latch 366 stores a high level. Since ϕ_C and at least one of ϕ_{RCD1} and ϕ_{RCD2} are also at high levels at that time as discussed hereinabove, a NAND gate 372 outputs a low level, thereby forcing a control signal ϕ_{EWDC} to go high. The low level output of the NAND gate 372 inputs to the shift register 370, thereby outputting low level therefrom after a delay of one cycle of ϕ_{CLK}. Then, a NAND gate 374 outputs a high level, thereby causing the control signal ϕ_{WR} to go high. Generating the control signal ϕ_{WR} after a delay of one cycle of CLK is to accept an external input data at a next cycle of CLK after a write command. Thus, to accept an external input data at a write command cycle, it will be obvious to those skilled in the art that the shift register 370 may be omitted therefrom.

FIG. 31 is a drawing showing a schematic circuit diagram for the DQM buffer 342, and FIG. 32 is a drawing showing an operation timing diagram for the DQM buffer. Referring to FIG. 31, an input buffer 70 is a buffer for converting an external signal DQM into a CMOS level signal. A shift register 382 is connected to the input buffer 70 for generating a data output masking signal o_{DQM} in synchronism with the system clock ϕ_{CLK}. Referring to FIG. 32, a data output masking command is issued at time t_1. At this time, a latch 384 stores a low level. When ϕ_{CLK} 387 is then at a high level, a latch 385 stores a high level. When ϕ_{CLK} 387 is then at a low level, a latch 386 stores a high level. When ϕ_{CLK} 388 is then at a high level, the signal o_{DQM}. goes to a low level. Likewise, the signal o_{DQM} goes to a high level when ϕ_{CLK} 389 is at a high level. Thus, inhibiting data output from the data output buffer with o_{DQM} signal being at the low level is accomplished by responding to the rising edge of the second clock of ϕ_{CLK} after the issuance of the data output masking command. It will be obvious to those skilled in the art that the time adjustment of inhibiting data output therefrom may be accomplished by changing the number of shift stages.

2. Column Address Generator

The column address generator comprised of a column address buffer 214 and a column address counter 346.

FIG. 34 is a drawing showing a schematic circuit diagram for the column address buffer 344. The synchronous DRAM of the present embodiment uses ten column address buffers which receive external column addresses A_0 to A_9, respectively. In the drawing, an input buffer 70 is a buffer for converting the external column address signal A_i into a CMOS level address signal. The input buffer 70 is enabled by the signal ϕ_{RAL} and its output is coupled to a latch 392 via a transfer switch 390. Before ϕ_{CA} goes to a high level, the latch 392 stores an input column address signal ECAI and then produces a column address signal FCAI via inverters. Only signals FCA0 and FCA1 are fed to the data transfer control counter 348. When ϕ_{CA} is at the high level due to the activation of $\overline{CAS}$, a transfer switch 394 is turned on, thereby storing complement of the column address signal ECAI into a latch 398. The output of the latch 398 is coupled to switch means comprised of NAND gates 400 and 402 which is enabled by ϕ_{CAR}. The enabled NAND gates 400 and 402 provide column address signal CAI and its complement $\overline{CAI}$, respectively. The column address signals CAI are fed and loaded to the column address counter 346, thereby generating successive column address signals PCAI therefrom with counting operation starting from the loaded column address signal. The signals PCAI output as column address signals CAI and $\overline{CAI}$ via transfer switches 396, latches 398 and switches 400 and 402. Thus, transfer switches 394 and 396, latch 398 and switch 400 and 402 constitute means for providing a starting column address with ϕ_{CA} pulse generated by the activation of $\overline{CAS}$, and providing successive column address signals being counted from the starting column address when the pulse ϕ_{CA} is at a low level. Thus, after the activation of $\overline{CAS}$ the successive column addresses, i.e., serial steam of the external input column address and the internally generated column addresses can be generated at a high speed. It should be noted that in the present embodiment, column address buffers associated with column address signals CA0 and CA9 do not receive signals PCA0 and PCA9. The signals CA9 has no relationship with the column decoder because of using as a bank selection signal in case of executing a $\overline{CAS}$ interrupt operation. Signals CA0 and CA1 are also signals for generating read data transfer clocks RDTPm and write data transfer clocks WDTPm which are respectively used in the data output multiplexer 268 and the data output demultiplexer 314. Signals CA1 to CA8 are utilized for column decoding.

FIG. 35 is a drawing showing a schematic block diagram for the column address counter 346, and FIG. 36 is a drawing showing a schematic circuit diagram for each stage in the column address counter. Referring to the drawings, the column address counter 346 is a 9-bit counter comprised of nine stages ST1 to ST9, and comprises a first counter portion including lower stages ST1 to ST3 and AND gates 404 and a second counter portion including upper stages ST4 to ST9 and AND gates 406. The first counter portion may carry out counting operation in one of binary and interleave modes, and the second counter portion may perform counting opera-

tion in the binary mode. In the first counter portion, i.e., 3-bit counter, selection of either the binary or the interleave mode is enforced by the logic level of the address mode signal ϕ_{INTEL}. In the least significant stage ST1, an input terminal of a carry input signal CARI and a burst length input terminal SZ are connected to the supply potential Vcc. Carry output signal CARO of the first stage ST1 inputs to a carry input signal CARI of the second stage ST2, and AND gate **404** corresponding to the second stage ST2 ANDs the carry outputs of the first and second stages ST1 and ST2. AND gate **404** corresponding to the third stage ST3 ANDs a carry output of the third stage ST3 and the output of the AND gate corresponding to the second stage ST2 which is connected to a carry input of the third stage ST3. The output of the AND gate associated with the most significant stage ST3 of the first counter portion is connected to a carry input signal CARI of the least significant stage ST4 of the second counter portion. A carry input signal CARI of each stage in the second counter portion is coupled to the output of the AND gate of the previous stage. Each AND gate **406** of the second counter portion inputs the output of the AND gate of previous stage and the output of the corresponding stage.

The column address counter **346** of the present invention may selectively perform one of both the binary and the interleave modes as an address sequence in order to enhance a design flexibility for memory system designers. The binary addressing mode is a mode representative of generating successive addresses increasing by one from a given starting address, and the interleave addressing mode is a mode representative of generating successive addresses in a specific way. The following Table 3 represents the address sequence representative of the decimal number in case of the burst length of 8.

TABLE 3

Address Sequence (Burst Length n = 8)	
Binary Mode	Interleave Mode
0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
1,2,3,4,5,6,7,0	1,0,2,3,5,4,7,6
2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
7,0,1,2,3,4,5,6	7,6,5,4,3,2,1

FIG. **36***a* is a drawing showing a schematic circuit diagram for each stage of the first counter portion. Referring to the drawing, each stage of the first counter portion includes a carry portion **408** for generating a carry and a bit portion **410** for providing a bit output. The carry portion **408** comprises two latches **412** and **416**, a transfer switch **414** connected between the latches **412** and **416**, an inverter **418** and a transfer switch **411** connected in series between an output terminal of the latch **416** and an input terminal of the latch **412**. Likewise, the bit portion **410** also comprises latches **412'** and **416'**, transfer switches **411'** and **414'** are connected to a line **419** and a line **415** via an inverter **413**. Input terminals of latches **412** and **412'** are connected to lines **422** and **424**, respectively. An initialization circuit **420** is connected between the lines **422** and **424** for providing an initial condition, i.e., a low level upon power-on to the latches **412** and **412'**. The line **419** is connected to an output terminal of a NOR gate **426**, three input terminals of which are respectively coupled to the clock CNTCLK9, the output of a NAND gate **428** and the signal BITSET. The NAND gate **428** receives the burst length signal SZn, a signal ϕ_{CARC} and the carry signal CARI which is the previous carry output signal CARO. Transfer switches **430** and **432** are turned on in response to the signal BITSET and thereby transfers an initial carry value and an initial column address value (or an initial bit value) on lines **422** and **424**, respectively. The mode control signal ϕ_{INTEL} is at a high level in the interleave mode and at a low level in the binary mode, as discussed hereinabove. Thus, the transfer switches **430** and **432** turned on in the interleave mode respectively transfer a low level and the initial bit value CAI, and the switches **430** and **432** both transfer the initial bit value CAI in the binary mode.

FIG. **37** is an operation timing diagram for the circuit diagram of FIG. **36***a*. Referring to FIGS. **36***a* and **37**, when any one of input signals SZn, ϕ_{CARC} and CARI of NAND gate **428** is at a low level, NOR gate **426** inhibits the output of the clock CNTCLK9, maintaining a low level on the line **419**. Thus, transfer switches **414** and **414'** are in on states while transfer switches **411** and **411'** are in off states. At this time, once transfer gates **430** and **432** are turned on with the pulse signal BITSET at a high level, the carry output signal CARO and the bit output signal PCAI are respectively an initial carry value of a low level and an initial bit value in an interleave mode while the carry output signal CARO and the bit output signal PCAI are both initial bit values CAI in a binary mode. Then the low level signal BITSET turns off the transfer switches **430** and **432** and thereby causes the previously preset initial carry and bit values to be maintain thereon. Thus, the signal BITSET is a signal for respectively presetting initial carry and bit values into the carry portion **408** and the bit portion **410** according to the mode control signal ϕ_{INTEL}.

On the other hand, after the establishment of the initial values with the preset signal BITSET, when the signals SZn, ϕ_{CARC} and CARI are all at high levels, the NOR gate **426** outputs the clock CNTCLK9. Then, the carry portion **408** and the bit portion **410** respectively output binary sequential count values starting from the preset initial values every cycles of the clock CNTCLK9. During such a sequential operation, if a low level carry signal CARI inputs to the NAND gate **428**, the line **419** becomes a low level, thereby freezing operations of the carry portion **408** and the bit portion **410**. That is, since transfer switches **411** and **411'** are turned off, CARO and PCAI are respectively frozen to inverted ones of binary values stored in latches **412** and **412'**. When the signal CARI then goes to a high level, sequential operations are re-started beginning from the frozen values.

FIG. **36***b* is a diagram showing a schematic circuit diagram for each stage constituting the second counter portion of FIG. **35**. Constructions of this stage are identical to those excluding the carry portion **408** and the mode control circuit **434** in the stage of FIG. **36***a*. Its operation is also identical to that of the bit portion **410** of FIG. **36***a*. Thus, detailed explanation for each of the stages ST4 to ST9 will be omitted.

Returning to FIG. **35**, it is assumed that the burst length of n has been set by the operation mode program. Then, since burst length signals associated with burst length of n or less are all at high levels, only stages receiving high level burst length signals SZn are enabled. For example, if the burst length n is **512** (full pages), the column address counter operates as a 9-bit counter. If burst length of n=32 is programmed, five lower stages ST1 to ST5 perform sequential counting operations, and output signals PCA5 to PCA8 of upper stages ST6 to ST9 respectively maintain initial input bit values, i.e., input column address signals CA5 to CA8. Thus, the first counter portion comprised of three lower stages ST1 to ST3 outputs sequential binary or

interleave address signals PCA0 to PCA2 according to the mode control signal ϕ_{INTEL}, and the counter comprised of stages ST4 and ST5 outputs sequential binary address signals PCA3 and PCA4 starting from input column addresses CA3 and CA4, receiving carries from the first counter portion.

3. Column Decoder

As discussed hereinabove, the column address buffers **344** output column address signals CA1 to CA8 inputting to the column decoder for selecting columns.

FIG. **38** is a drawing showing a schematic block diagram for the column decoder according to the present invention. In the drawing, predecoders **436** to **442** receive column address signals CA1 and CA2, CA3 and CA4, CA5 and CA6 and CA7 and CA8, respectively and also receive a row address signals RA11 or a column address signal CA9. The column address signal RA11 is used as a bank selection signals in case of performing either an interleave operation of the first and second banks or an independent operation between both banks such as performing read or write operation and precharge operation of the second bank after performing read or write operation and precharge operation of the first bank. If RA11 is low, the first bank is selected, while if RA11 is high, the second bank is selected. On the other hand, CA9 is a bank selection signal in case of performing a $\overline{CAS}$ interrupt operation. The first bank is selected when CA9 is low, while the second bank is selected when CA9 is high.

The first predecoder **436** decodes column address signals CA1 and CA2, thereby generating predecode signals DCA$\bar{1}\bar{2}$ to DCA12 and also generating a signal DCA2 and its complement DCA$\bar{2}$ which are faster than the signals DCA$\bar{1}\bar{2}$ to DCA12. Neighboring signals of the predecode signals overlaps a predetermined portion of each end. The output signals of the first predecoder **436** are fed to main decoders **444**. NOR gates **446** respectively input combinations of signals choosing one of predecode signals DCA$\bar{3}\bar{4}$ to DCA34 from the predecoder **440** and one of predecode signals DCA$\bar{7}\bar{8}$ to DCA78 from the predecoder **442**, and their outputs are respectively coupled to the main decoder **444** so as to produce column selection signals CSL0 to CSL255.

FIG. **39***a* is a drawing showing a schematic circuit diagram for the first predecoder **436**. In the drawing, NAND gates **448** are enabled by the bank selection signal RA11 or CA9, decode column address signals CA1 and CA2 and their complements $\overline{CA1}$ and $\overline{CA2}$. After activation of $\overline{CAS}$, a short low level pulse ϕ_{CP} resets NAND gates **451** and **454**, thereby causing the output signals DCA$\bar{1}\bar{2}$ to DCA12 to become low. When ϕ_{CP} is then at a high level (at this time, ϕ_{YEI} is high), the NAND gates **451** and **454** are enabled. It is now assumed that CA1 and CA2 have been at low levels. Then, NAND gate **448***a* outputs a low level, and NAND gate **456***a* then outputs a high level. Thus, DCA$\bar{1}\bar{2}$ goes from the low level to a high level, while DCA$\bar{1}$2, DCA1$\bar{2}$ and DCA12 remain the low levels. When CA1 then goes to a high level and CA2 maintains the low level, this results in causing DCA1$\bar{2}$ to go high. However, the NAND gate **448***a* outputs a high level, thereby causing DCA$\bar{1}\bar{2}$ to go low after delays via delay circuits **450***a* and **452***a*, NAND gates **451***a*, **456***a* and **454***a* and an inverter. Thus, DCA$\bar{1}\bar{2}$ goes to the low level with the time delay determined by the delay elements after going to the high level. Consequently, overlapped portions occur end portions between successive predecoding signals. These overlapped portions guarantee an error free write time during a write operation.

FIG. **39***b* is a drawing showing a schematic circuit diagram for one of second predecoders **438** to **442**. It should be noted that each second predecoder is a low enable circuit in which a selected predecode signal goes to a low level.

FIG. **40** is a drawing showing a schematic circuit diagram for first one of main decoders **444**. Referring to the drawing, predecode signal DCA$\bar{1}\bar{2}$ to DCA12 are respectively coupled to input terminals of inverters **458***a* to **458***d* which are partitioned into a first inverter group of inverters **458***a* and **458***b* and a second inverter group of inverters **458***c* and **458***d*. One terminal of each of inverters **458***a* and **458***b* constituting the first group is connected in common with a drain of a first transistor **462**, while one terminal of each of inverters **458***c* and **458***d* constituting the second group is connected in common with a drain of a second transistor **464**. The other terminal of each of the inverters **458***a* to **458***d* is connected to the supply potential Vcc. Output terminals of the inverters are respectively connected to latches **406***a* to **460***d*. Sources of first and second transistors **462** and **464** are connected in common with a drain of a third or pull-down transistor **466** whose source is connected to a reference potential Vss such as a ground potential and whose gate is connected with the output of NOR gate **446** inputting predecode signals DCA$\bar{3}\bar{4}$, DCA$\bar{5}\bar{6}$ and DCA$\bar{7}\bar{8}$ from the second predecoders **438** to **442**. Gates of the first and the second transistors **462** and **464** respectively received DCA$\bar{2}$ and DCA2. The input signals are generated in order of predecode signals DCA2 and DCA$\bar{2}$, predecode signals DCA$\bar{3}\bar{4}$, DCA$\bar{5}\bar{6}$ and DCA$\bar{7}\bar{8}$ and overlapped predecode signals DCA$\bar{1}\bar{2}$ to DCA12. Thus, after the transistor **462** or **464** and the pull-down transistor **466** have been turned on, the inverters **458***a* to **458***d* can be turned on. It is now assumed that column address signals CA1 to CA8 have been low. Then, the transistor **462** is turned on and the transistor **466** is then turned on. The inverter **458***a* is then turned on by the high-going signals DCA$\bar{1}\bar{2}$ and thereby the column selection signal CSL0 goes to a high level. Where the column address signal CA1 then changes into a high level, DCA1$\bar{2}$ goes to a high level, thereby causing the column selection signal CSL1 to go high. However, the column selection signal CSL0 becomes from the high level to a low level after a predetermined delay, as discussed above, due to the low-going signal DCA$\bar{1}\bar{2}$. In the same manner as discussed above, column selection signals overlapping predetermined ones of end portions in response to column address signals CA1 to CA8 being sequentially changed. Referring to FIG. 33*b*, where initial external column addresses A_0 and A_1 to A_8 are respectively at a high level and low levels, illustration is made on a timing diagram showing timing relations between column address signals CA to CA8, signals DCA$\bar{1}\bar{2}$ and DCA1$\bar{2}$ and column selection signals CSL0 and CSL1. It can be understood in the drawing that time periods for selecting columns are sufficiently guaranteed by overlapped portions.

FIG. **41** is a timing diagram showing a read operation at the system clock frequency of 100 MHZ, the burst length of 4 and the $\overline{CAS}$ latency of 3. It can be understood in the drawing that sufficient read-out time periods can be guaranteed by overlapped portions of signals DCA$\bar{1}\bar{2}$, DCA1$\bar{2}$ and CSL1 where A_0 and A_1 to A_8 are initially at a high level and low levels, respectively.

4. Data Bus Control Circuit

It is very important that unnecessary internal operations are precluded to eliminate power consumption after completion of the burst length, i.e., after output or input of valid data. Such a control circuit comprises the burst length counter **350**, the burst length detector **352** and the column address reset signal generator **354** as shown in FIG. 4.

The burst length counter **350** stops its counting operation when the column address reset signal ϕ_{CAR} is at a low level.

The counter 350 is reset by a short high level pulse BITSET, thereby re-starting its counting operation. Thus, the burst length counter 350 is a conventional 9-bit binary counter whose clock input terminal is connected to the system clock ϕ_{CLK} and whose reset terminal is connected to the output of a OR gate inputting the signal BITSET and complement of ϕ_{CAR}. Count values CNTI (I=0, 1, . . . 8) of the counter 350 input to the counter 350 input to the burst length detector 362.

FIGS. 42 and 43 show a schematic circuit diagram for the burst length detector. The burst length detector 352 includes a logic circuit receiving the count values CNTI and burst length signals SZn for generating a signal COSI informing of the completion of burst length after activation of $\overline{CAS}$. For example, referring to FIG. 41, once the pulse BITSET goes from the high level to the low level after the activation of $\overline{CAS}$, the counter 350 counts clocks of ϕ_{CLK}, thereby producing count signals CNT0 and CNT1. Since SZ4=1 (high) in case of the burst length of 4, the burst length detector 352 produces the signals COSI having a pulse width of one cycle of ϕ_{CLK} when CNT0 and CNT1 are all at high levels. On the other hand, the pulse ϕ_C being at the high level after the activation of $\overline{CAS}$ renders to be latched low the output of a flip-flop comprised of NOR gates 468 and 470 as shown in FIG. 43, thereby causing the signal COSR to go low as shown in FIG. 41*b*. Once COSI then goes to a high level, two inputs of a NAND gate 474 become high after delay of a shift register 472 with the system clock ϕ_{CLK}. Thus, the output of the NOR gate 468 goes low. At this time, since ϕ_C is low, the output of the NOR gate 470 goes to a high level, thereby causing COSR to go to a high level. Thus, it can be understood in FIG. 4*b* that the low level signal COSR is a signal indicating of the burst length, i.e., four pulses of the system clock CLK after the activation of $\overline{CAS}$. A delay circuit 476 for providing time delays depending on $\overline{CAS}$ latency values receives the signal COSR and then outputs a signal COSDQ. Thus, it can be seen that the signal COSDQ is a signal indicating of a burst length considering a $\overline{CAS}$ latency. Referring to FIG. 41*b*, since the $\overline{CAS}$ latency is 3 (CL3 is a high level), a transfer switch 478 is turned on, thereby producing the signal COSDQ that the signal COSR is delayed by two cycles of the clock ϕ_{CLK}. It has been already discussed that the signal COSDQ being at a high level disables the data output buffer.

FIG. 44 is a drawing showing a schematic circuit diagram for the column address generator 354. Referring to FIG. 41 or FIG. 33, the signal ϕ_{RAL} had become high prior to the activation or $\overline{CAS}$. Then, after the activation of $\overline{CAS}$, NAND gates 482 and 484 output high levels in response to the high-going pulse ϕ_C. Thus, a NAND gate 480 constituting a flip-flop is latched to a low level, thereby allowing ϕ_{CAR} to go high. Likewise, a NAND gate 486 outputs a low level in response to the signal COSR going to a low level when ϕ_C is high since one of ϕ_{YEC1} and ϕ_{YEC2} maintains a high level at this time. Thus, ϕ_{CARC} goes to a high level. Then once COSR goes to a high level, ϕ_{CAR} and ϕ_{CARC} goes to low levels. However, in case of using a system clock of a lower frequency such as 66 MHZ or less, signals ϕ_{RAL} and ϕ_{YEI} or ϕ_{YE2} rather than the signal COSR go first to low levels, thereby causing the signal ϕ_{CAR} to go low. Thus, the burst length counter 350 and the column address counter 346 are reset by the low-going signal ϕ_{CAR}, thereby preventing unnecessary operations thereof.

5. Data Transfer Clock Generator

A data transfer clock generator is a circuit for generating clock for transferring data via the data output multiplexer and the input data demultiplexer. The data transfer clock generator includes the data transfer control counter 348 and the read and write data transfer clock generators 356 and 358.

The column address generator 346 is using the multiplied system clock CNTCLK9 as synchronization clock to assure a faster precharge time in case of using a system clock of 33 MHZ or less, as previously discussed. In such a case, since data must be transferred in synchronism with the system clock CLK, the data transfer control counter 348 is essentially required. However, if such a technique is unnecessary, i.e., if such lower frequency system clock is not used, some modifications are required. Such modifications can be accomplished by the following explanation. That is, the column address counter 346 as shown in FIG. 35 uses the system clock ϕ_{CLK} in place of the clock CNTCLK9 as a synchronous count clock. Selection circuits 391 as shown in FIG. 34 respectively receive the lower 2-bit outputs PCA0 and PCA1 to produce column address signals CA0 and CA1. The read and write data transfer clock generators 356 and 358 directly input the signals CA0 and CA1 instead of outputs RCA0 and RCA1 from the data transfer control counter 348.

FIG. 45 is a drawing showing a schematic block diagram for the data transfer control counter 348 which comprises a 2-bit counter 488 and 490 and selection circuits 492 and 494. The 2-bit counter receives column address signals CA0 and CA1 from the column address buffers 344 for generating internal sequential column address signals starting from the signals CA0 and CA1 in synchronism with the system clock ϕ_{CLK}. The selection circuits 492 and 494 serve to generate serial column address stream with column address signals FCA0 and FCA1 from the column address buffers 344 and the internal sequential column address signals from the 2-bit counter. Stages 488 and 490 constituting the 2-bit counter are respectively identical in constructions to stages shown in FIGS. 36*a* and 36*b*. The difference therebetween is to use the system clock ϕ_{CLK} instead of the clock CNTCLK9. Each of the selection circuits 494 and 492 has the same construction as the selection circuit 391 of FIG. 34. The input signals ECAI of the transfer switch 394 and the input signal PCAI are respectively replaced by FCAI and the output of the corresponding 2-bit counter (wherein I is 0 or 1). The signal COSR is also fed to third inputs of NAND gates 400 and 402. Using the signal COSR in the selection circuits 492 and 494 is preventing unnecessary internal operation thereof upon completion of burst length. Operation explanation for the 2-bit counter and the selection circuits is referred to portions as discussed in connection with FIGS. 36*a*, 36*b* and 34. The outputs RCA0 and RCA1 of the data transfer control counter 348 and their complements $\overline{RCA0}$ and $\overline{RCA1}$ may be properly time delayed signals according to $\overline{CAS}$ latency values or the system clock in order to control a data transfer timing on data lines.

FIG. 46 is a drawing showing a schematic circuit diagram for the read data transfer clock generator 356 for generating read data transfer signal RDTP0 to RDTP3 which are used in the data output multiplexer. Referring to the drawing, the generator 356 comprises NAND gates 498 for decoding column address signals RCA0 and RCA1 and their complements $\overline{RCA0}$ and $\overline{RCA1}$, delay circuits 500 for receiving the decoded signals and producing read data transfer signals with different time delays according to $\overline{CAS}$ latency values, and NAND gates 496 for outputting the read data transfer signals in a read operation and resetting their outputs to low levels in a write operation. The outputs of NAND gates 496 become high in response to the signal ϕ_{EWDC} being at a high level in a write operation. Each of NAND gates 498 serves as a decoder outputting low in response to two inputs of high

levels. Each delay circuit **500** includes a shift register **503** having a plurality of data paths and switches **497**, **501** and **502** respectively connected to the data paths, and serves to provide a different time delay via a selected switch according to $\overline{CAS}$ latency signals CL3 and CL4. Referring to FIG. **51***b*, where initial external column addresses A_0 and A_1 are respectively at a high level (=1) and a low level (=0), illustration is made on a timing diagram for column address signals RCA0 and RCA1 for controlling data transfer and read data transfer signals RDTP0 to RDTP3. Since the $\overline{CAS}$ latency value is 3, switches **502** are turned on.

FIG. **47** shows a schematic circuit diagram of a circuit for generating the signal ϕ_{CL} being used in the data output multiplexer **268**. Referring to the drawing, after the activation of $\overline{CAS}$, the high-going pulse ϕ_C renders high the output of a flip-flop **504** via a delay circuit **505**. On the other hand, if one of $\overline{CAS}$ latency signals CL3 and CL4 is high, the output of a NAND gate **506** maintains high. Thus, the signal ϕ_{CL} goes high. Then if ϕ_C goes low, the signal ϕ_{CL} will go low after a delay of about one cycle of ϕ_{CLK} in case of a high level signal CL3, while the signals ϕ_{CL} will go low after a delay of about 2 cycles of ϕ_{CLK} in case of a high level signal CL4. However, if CL3 and CL4 are all low, i.e., where $\overline{CAS}$ latency is either 1 or 2, ϕ_{CL} is always low since the output of NAND gate **506** is low.

FIG. **49** shows a timing diagram of $\overline{CAS}$ interrupt read operation after activation of $\overline{RAS}$. The operation is performed at the $\overline{CAS}$ latency of 3 and the burst length of 4 with system clock of 66 MHZ. At time t_1, a read command is issued with external column addresses $A_0, A_1, A_2, \ldots,$ A8=1, 0, 0, . . . , 0. At time t_3, a $\overline{CAS}$ interrupt read command is issued with external column addresses $A_0, A_1, A_2, \ldots,$ A8=0, 1, 0, . . . , 0. Then, at t_3 and t_4, i.e., just before and after the issuance of the $\overline{CAS}$ interrupt read command, column address signals RCA0 and RCA1 are identical as a low level and a high level. Thus, read-out data is transferred in series via the same data line pairs DIO_2, $\overline{DIO_2}$ at times t_3 and t_4. It may be seen in FIG. 49C that read-out data was high just before the $\overline{CAS}$ interrupt, while read-out data was low immediately after the $\overline{CAS}$ interrupt. Then, as shown in the timing diagram of DIO_2 between t_3 and t_5 in FIG. 49C, serial data, i.e., 1, 0 is transferred on the data line DIO_2. Thus, as shown in FIG. **25**, if means **276** for isolating between serial registers **274** and **278** are not provided therebetween, the serial data is sequentially latched into the serial registers **274** and **278**, and transferred only in series to the data output buffer via transfer switch **280** which is turned on by the read data transfer signals RDTP2. However, since the operation speed of semiconductor circuit varies according to ambient conditions such as ambient temperature, it is essentially necessary to provide means for preventing serial data contention due to variations of the operation speed of the transfer switch **280** or data output buffer. The signal ϕ_{CL} is used as a signal for isolating between serial registers **274** and **278** to prevent such a data contention. It is to be understood that the data contention between two serial data may be prevented by the high level pulse ϕ_{CL} indicating as P in FIG. 49C.

FIG. **48** shows a schematic circuit diagram of the write data transfer generator write data transfer signals WDTP0 to WDTP3 for use in the data input demultiplexer **314**. The generator **358** comprises NAND gates for decoding column address signals RCA0 and RCA1 and their complements $\overline{RCA0}$ and $\overline{RCA1}$, a synchronization circuit **510** for synchronizing the decoding signals from the NAND gates with the system clock ϕ_{CLK} and producing synchronized write data transfer signals, and NAND gates **512** for gating the synchronized write data transfer signals. A line **514** stays at a low level to reset all of the gates **512** during a read operation, a $\overline{CAS}$ interrupt or a data input/output masking operation, thereby causing the signals WDTP10 to WDTP3 to go low. Reference numeral **516** represents a delay circuit. As shown in FIG. **33**, by a high level address signal RCA0 and a low level address signal RCA1, a high level pulse signal WDTP1 is generated and next sequential address signals RCA0 and RCA1, which are respectively a low level and a high level, generates a high level pulse signal WDTP2.

6. Data Line Precharge Circuit

Data line precharge circuit is a circuit for generating control signals to precharge I/O lines, PIO lines and DIO lines. According to the present invention, data transfer and precharging between lines on data paths are sequentially performed in turn. To perform such a precharge operation, column address signal CA1 produced from external column address A_1 is utilized.

FIG. **50** shows a schematic circuit diagram of a circuit for generating control signals to precharge I/O lines and PIO lines. RA11 and CA9 are bank selection signals as discussed above, and I/O lines and PIO lines are initialized to precharge states. Thus, PIOPR1 and IOPR1 and their complements $\overline{PIOPR1}$ and $\overline{IOPR1}$ are at high levels. After activation of $\overline{CAS}$, once ϕ_{CP} goes from a low level to a high level (ϕ_{YEi} maintains a high level), NAND gates **518** are then enabled. If CA1 is at a low level ($\overline{CA1}$ at a high level), precharge signals PIOPR1 and IOPR1 maintain high levels while $\overline{PIOPR1}$ and $\overline{IOPR1}$ go to low levels. Thus, in FIG. **24**, if BLS is high, I/O line pairs I/O_2, $\overline{I/O_2}$ and I/O_3, $\overline{I/O_3}$ are continuously precharged. However, I/O_0, $\overline{I/O_0}$ and I/O_2, $\overline{I/O_2}$ cease precharging to be ready for data transfer. PIO line pairs PIO_2, $\overline{PIO_2}$ and PIO_3, $\overline{PIO_3}$, as shown in FIG. **28**, are also precharged in the same manner. Then, if CA1 goes to a high level, lines I/O_0, $\overline{I/O_0}$, I/O_1, $\overline{I/O_1}$, PIO_0, $\overline{PIO_0}$, PIO_1 and $\overline{PIO_1}$ are conversely precharged. On the other hand, a short low level pulse ϕ_{CP} generated after activation of $\overline{CAS}$ in a $\overline{CAS}$ interrupt operation renders all of precharge signals PIOPR1, $\overline{PIOPR1}$ and $\overline{IOPR1}$ to become high level pulses. Thus, prior to receipt of column addresses upon $\overline{CAS}$ interrupt, all of I/O line pairs and PIO line pairs are precharged. By such a $\overline{CAS}$ precharge, internal operations may be performed at a high speed with no wait. Reference numeral **520** represents a delay circuit.

FIG. **51** shows a schematic circuit diagram of a circuit for generating control signals to precharge DIO lines. In the same manner as discussed above, once ϕ_{CP} goes to a low level, DIO line precharge signal DIOPR1 and its complement $\overline{DIOPR1}$ go high, and signal WCA1 and its complement $\overline{WCA1}$ go low, thereby precharging all of DIO lines. That is, this is in case of a $\overline{CAS}$ interrupt operation. If ϕ_{CP} goes to a high level and CA1 is at a low level ($\overline{CA1}$ is at a high level), signals DIOPR1 and WCA1 respectively maintain the high level and the low level while $\overline{DIOPR1}$ and $\overline{WCA1}$ respectively go to a low level and a high level. Thus, during a read or a write operation, precharge circuits **263***c* and **263***d* of FIG. **25** maintains on states while the circuits **263***a* and **263***b* thereof are turned off. Then, line pairs DIO_2, $\overline{DIO_2}$ and DIO_3, $\overline{DIO_3}$ keep precharging while DIO_0, $\overline{DIO_0}$ and DIO_1, $\overline{DIO_1}$ are ready for data transfer. In case of the write operation, transistors **318***c* and **318***d* of FIG. **27** maintain on states and transistors **318***a* and **318***b* thereof are turned off, thereby causing buffers **324***c* and **324***d* to keep off states and buffers **324***a* and **324***b* to transfer data depending on data states stored in latches **320**. Then if CA1 goes to a high level, operations contrary to above mentioned ones are performed.

FIG. 52 is a schematic circuit diagram of a circuit for generating bank selection signals for use in the PIO driver 330 shown in FIG. 28. Once a write command is issued, ϕ_{WR} and ϕ_{CP} then go to high levels. At this time, when RA11 or CA9 is at a low level, DTCP1 is latched to a high level and thereby the first bank is selected. Where precharge command is issued to the first bank, ϕ_{YE1} goes to a low level and thereby the first bank selection signal DTCP1 then goes to a low level. On the other hand, where a write command is issued to the second bank during the write operation for the first bank, a flip-flop 522' is latched to a low level and thereby a second bank selection signal DTCP2 then goes to a high level. Each of DTCP1 and DTCP2 is connected to PIO driver 330 associated with corresponding bank. Referring to FIG. 28, when bank selection signal DTCPi and block information signals BLS are all at high levels, switches 332 are enabled, thereby allowing data on corresponding DIO lines to be transferred.

7. Data Output Buffer Control Circuit

Data output buffer control circuit is a circuit for controlling data outputs from the data output buffer 284 shown in FIG. 26. It is required that the data output buffer outputs data at eery predetermined rising edges of the system clock CLK in a read operation. Since the synchronous DRAM must output data information only within a given time period set by the $\overline{CAS}$ latency and the burst length, it is to be preferred that data output therefrom is precluded outside the given time period in order to as well increase the performance of the chip as prevent power consumption. Also, since one cycle time of the system clock of a predetermined frequency (33 MHZ in this embodiment) or less is long, it is meaningless to output data in synchronism with the system clock CLK.

FIG. 53 is a schematic circuit diagram of a control circuit for generating a control signals to inhibit data output of the data output buffer 284. NAND gate 524 outputs a low level in a write operation. A clock signal ϕ_{CF} stays a high level for one clock cycle of ϕ_{CLK} going to the high level at the first rising edge of ϕ_{CLK} after activation of $\overline{CAS}$. Likewise, ϕ_{WRCF} stays a high level for one clock cycle of ϕ_{CLK} after the activation of $\overline{WE}$. Where $\overline{CAS}$ and $\overline{WE}$ are all activated, the NAND gate 524 generates the low level, thereby allowing a signals ϕ_{TRST} to go low. Also, when data output masking is requested by the external signal DQM, the DQM buffer 342 shown in FIG. 31 generates the low level clock signal ϕ_{DQMF} as shown in FIG. 32. Thus, the NAND gate 526 generates a high level pulse. This results in generating a row level pulse ϕ_{TRST}. Likewise, the signal ϕ_{TRST} also becomes low with the signals COSDQ being at a high level after the delay depending on $\overline{CAS}$ latency j following the completion of the burst length. Thus, the output of the data output buffer 284 shown in FIG. 26 becomes a high impedance in response to the low level signal ϕ_{TRST}. Consequently, the data output buffer 284 inhibits data output at the rising edge of next system clock CLK after the issuance of the data output masking signal DQM. Also, upon the completion of the burst data output, the output of the buffer 284 becomes the high impedance.

Where external system clock of 33 MHZ or less is used, a control signal ϕ_{YEP} may be coupled to the $\overline{CAS}$ latency signal CL1 so as to output data irrespective of the internal system clock ϕ_{CLK}. Since the $\overline{CAS}$ latency signal CL1 keeps a high level at such a system clock, the signal ϕ_{YEP} is at a high level. Thus, in the data output buffer 284 of FIG. 26, transfer switches 286 and 286' are always turned on and thereby not under the control of the system clock ϕ_{CLK}. However, when system clock of a frequency above 33 MHZ is used, the signal CL1 is at a low level and the signal ϕ_{YEP} is also at a low level. Thus, the transfer switches 286 and 286' are turned on and off under the control of the system clock ϕ_{CLK}.

OPERATION

Explanation will be now made on operation and using way of the present synchronous DRAM.

Referring to FIG. 41, illustration is made on a timing chart showing a read operation at the burst length of 4 and the $\overline{CAS}$ latency of 3, using an external system clock of 100 MHZ. At time t_1, activation command is issued. External addresses input along with the activation of $\overline{RAS}$. Then $\overline{RAS}$ buffer 56 produces the signal ϕ_{RP} and then generates the bank selection $\overline{RAS}$ signal ϕ_{RCi} defining one of the first and second banks 12 and 14 with the external address A_{11}. The row master clock generator 62 of FIG. 19 generates the row master clock ϕ_{Ri} in receipt of the signal ϕ_{RCi}. The row address buffer 60 responds the row master clock ϕ_{Ri} to generate row address signals which are fed to the row decoder 18 of selected bank. In response to the row address signals, the row decoder 18 generates a block information signal BLS representative of a selected sub-array in each of the first to the fourth memory cell arrays and a signal selecting a word line in the selected sub-array. Sensing operation, which drives word lines selected by the word line selection signals and then develops data on corresponding bit lines, is performed by conventional techniques. After the completion of $\overline{RAS}$ chain, the row control clock generator 64 generates the signal ϕ_{RCDi} guaranteeing the $\overline{RAS}$-$\overline{CAS}$ delay time t_{RCD}. At time t_2, read command is issued and column addresses are inputted to the column address buffer 344. In response to the $\overline{CAS}$ signal being at the low level at the time t_2, the buffer 344 generates pulse signals ϕ_C, ϕ_{CA}, ϕ_{CP} and BITSET. The signal ϕ_{CAR} for controlling circuits associated with column address signal generation is generated from the column address reset signal generator 354 in response to the pulse signal ϕ_C and the signal ϕ_{YECi} which is generated from the column enable clock generator 66 in response to ϕ_{RCDi}. The column address buffer 344 outputs column address signals CA0 to CA9 in response to the pulse signal ϕ_{CA} from the $\overline{CAS}$ buffer and the signal ϕ_{CAR}. Thus, since the column address signals generated from the column address buffer 344 responsive to the column address enable/disable signal ϕ_{CAR}, which is generated by the ϕ_{RCDi} signal representative of the completion of $\overline{CAS}$ chain, and the ϕ_C signal representative of the activation of $\overline{CAS}$, the time duration from the activation of $\overline{CAS}$ (time t_2) until the output of the column address signals becomes considerably short. After the transition of the ϕ_{CAR} signal to the high level, the burst length counter 350 carries out counting operation of the system clock ϕ_{CLK} to detect the burst length. In response to count signals CNT0 and CNT1 from the burst length counter 350, the burst length detector 352 generates the burst end signal COSI and the COSR signal representative of the burst length after the activation of $\overline{CAS}$. The detector 352 also produces COSDQ signal delayed by given clock cycles depending on a preset $\overline{CAS}$ latency value from the signal COSR to control the data output buffer 284 so as to provide data for the time period of data output which is defined by the burst length. Thus, since the $\overline{CAS}$ latency equals 3, the signal COSDQ is a signal delayed by approximately two cycles of ϕ_{CLK} from the signal COSR. Thus, the COSDQ signal is at the low level for the period of time defined by the $\overline{CAS}$ latency and the burst length (the time duration between t_3 and t_6).

The column address counter 346 loads column address signals from the column address buffer 344 in response to

the pulse signal BITSET from the $\overline{CAS}$ buffer and the column address enable signal ϕ_{CARC}, and then generates column address signals PCA0 to PCA8 in sequence, counting the clock CNTCLK9 according to the burst length and the address mode. The column address buffer **344** generates sequential column address signals CA0 to CA8 composed of initial column addresses and the column address signals PCA0 to PCA8.

FIG. **41** shows the timing chart at a binary address mode ((ϕ_{INTEL}=0) where initial external column address A_0 is high and the remaining external column addresses A_1 to A_8 are all low. Since the burst length was set to 4, only the burst length signal SZ_4 stays at a high level. Thus, only the lower two stages ST1 and ST2 of the first counter portion constituting the column address counter **346** of FIG. **35** executes the binary counting operation. Since the counting operation is performed at 100 MHZ, the clock CNTCLK9 is identical to the system clock ϕ_{CLK}. Thus, the outputs RCA0 and RCA1 of the data transfer control counter **348** are identical to the outputs PCA0 and PCA1 of the column address counter **346**. The outputs RCA0 and RCA1 of the counter **348** are fed to the read data transfer clock generator **356**, thereby generating read data transfer pulses RDTP0 to RDTP3 therefrom.

On the other hand, column address signals CA0 to CA8 from the column address buffer **344** are fed to the column decoder **24**, and the column predecoder **436** of FIG. **39***a* produces partly overlapped predecode signals DCA$\overline{1}$ $\overline{2}$ and DCA1$\overline{2}$ with the successive column address signals CA1 and CA2. The main column decoder **444** of FIG. **40** receives the predecode signals to generate column selection signals CSL0 and CSL1. Since the column selection signal CSL0 allows data developed on bit line pairs to be transferred to the first I/O line pairs I/O_0, $\overline{I/O_0}$ and I/O_1, $\overline{I/O_1}$, data on the first I/O line pairs, which is produced by the first pulse **532** of the column selection signal CSL0, inputs to the I/O sense amplifier via corresponding I/O line selection circuit and corresponding first PIO line pairs. In response to the activating signal **535** as shown in FIG. **41C**, the I/O sense amplifier amplifies data on the first PIO line pairs to output to corresponding first data line pairs DIO_0, $\overline{DIO_0}$ and DIO_1, $\overline{DIO_1}$. At this time, since the DIO line precharge signal DIOPR1 is at a high level, the second data line pairs DIO_2, $\overline{DIO_2}$ and DIO_3, $\overline{DIO_3}$ are in precharging states. Data transferred via the first data line pairs is stored into the register **278** in the data output multiplexer **268** of FIG. **25**. Data transferred via the data line pair DIO_1, $\overline{DIO_1}$ of the first data line pairs is selected by the pulse RDTP1 and then inputted to the data output buffer via the common data line pair CDL, $\overline{CDL}$, the data output latch **282** and the data output line pair DO, $\overline{DO}$. In the same manner as discussed above, parallel data on the second I/O line pairs I/O_2, $\overline{I/O_2}$ and $I/O1_3$, $\overline{I/O_3}$, which is generated by the pulse **533** of column selection signal CSL1, is then inputted in series to the data output buffer. Last data on the I/O line pair I/O_0, $\overline{I/O_0}$ of the first I/O line pairs, which is generated by the second pulse **534** of the column selection signal CSL0, is then inputted to the data output buffer. If read-out is 1,0,1,0, the data output buffer is enabled by the high level pulse ϕ_{TRST}, and its output DOUT is like the illustration of FIG. **41C**. Thus, when the signal ϕ_{TRST} is low, the data output buffer **284** becomes a high impedance and thereby prevents unnecessary operation thereof. It can be seen that the first data is generated at the rising edge of the third clock of the system clock CLK after the activation of $\overline{CAS}$, and continuous 4-bit data is outputted in synchronism with the system clock CLK.

FIG. **33** is the timing chart showing a write operation at the $\overline{CAS}$ latency of 2 and the burst length of 4, using a system clock of 66 MHZ. The timing of FIG. **33** is also of the case where external addresses A_0 and A_1 to A_8 are respectively applied with a high level and low levels in the same manner as above-mentioned read operation, and the input data DIN to the data input buffer is a serial data of 1,0,1,0. The $\overline{RAS}$ chain operation is performed as previously discussed, and the burst length signal COSR is generated by the burst end signal COSI. Sequential column address signals RCA0 and RCA1 for generating write data transfer pulses WDTP0 to WDTP3 are produced by column address signals CA0 and CA1. Write command is issued at time t_2, and write control signals ϕ_{WR} and ϕ_{EWDC} are produced from the $\overline{WE}$ buffer **340** by the low level signal $\overline{WE}$. In response to the signals RCA0 and RCA1, the write data transfer clock generator **358** generates write data transfer pulses WDTP0 to WDTP3 for converting a serial data to a parallel data. The input data DIN inputting via the data input buffer **312** is outputted on the input line DI as the serial data synchronized with ϕ_{CLK} as shown in FIG. **33**. The data input demultiplexer **314** produces the parallel data on the data lines $\overline{DIO_1}$, DIO_2, $\overline{DIO_3}$ and DIO_0 under the control of control signals WCA1 and $\overline{WCA1}$ and the write data transfer pulses WDTP0 to WDTP3, having the timing as shown in FIG. **33**. The parallel data is fed to corresponding I/O bus via the PIO line driver **330** under the control of control signals IOPR1 and $\overline{IOPR1}$, and then written into corresponding memory cells via bit lines selected by the column selection signals.

FIG. **49** is the timing chart showing the $\overline{CAS}$ interrupt read operation at the $\overline{CAS}$ latency of 3 and the burst length of 4, using a system clock of 66 MHZ. At the read command of time t_1, external addresses A_0 and A_1 to A_8 are respectively applied with a high level and low levels, and at the $\overline{CAS}$ interrupt read command of time t_3, external addresses A_1 and A_0 and A_2 to A_8 are respectively applied with a high level and low levels. This $\overline{CAS}$ interrupt read operation is identical to the previously discussed read operation, excepting that the last 2-bit data of the data, which must be read out by the read command issued at time t_1, can never be read out by the $\overline{CAS}$ interrupt command issued at time t_3. Referring to FIG. **49**, explanation will be made in brief. The activation command, i.e., the $\overline{RAS}$ activation command is issued at two cycles of CLK before time t_1. Then since operation of $\overline{RAS}$ chain with row addresses is identical to that as previously discussed, explanation of this operation will be omitted. The read command is issued at time t_1, and the column predecode signal DCA$\overline{1}$ $\overline{2}$ from the column predecoder (shown in FIG. **39***a*) then becomes high with CA1 and CA2 being at low levels. Then, the column selection signal CSL0 includes the high level pulse **600**, as shown in FIG. **49***b*, with CA2 to CA8 being always at low levels. After the transition of CA1 from the low level to the high level, the column predecode signal DCA1$\overline{2}$ becomes high, overlapping one end portion of the signal DCA$\overline{1}$ $\overline{2}$, and thereby the column selection signal CSL1 has the high level pulse **601**. Once the $\overline{CAS}$ interrupt read command is issued at time t_3, the $\overline{CAS}$ buffer **338** then generates the signal BITSET of pulse **602**. The burst length counter **350** is then reset by the pulse **602** and re-starts a binary counting operation with the system clock ϕ_{CLK}. After counting the burst length of 4, the counter **350** generates the burst end signal COSI of pulse **603**. Then, the burst length detector **352** produces the low level signal COSR indicating of a burst length from the first read command with the pulse ϕ_C and the signal COSR, and then outputs the signal COSDQ indicating of a data read-out time period with the signal COSR and the $\overline{CAS}$ latency signal. Thus, it can be seen that a total 6-bit data may be read out. The column address buffer **344** shown in FIG. **34** latches

external column addresses inputted upon $\overline{CAS}$ interrupt (at time t_3) by the high level pulse ϕ_{CA} from the $\overline{CAS}$ buffer 338, and produces successive four column address signals with the help of the column address counter 346. Thus, column address signal CA1, which is latched by the external high level address A_1 inputted at time t_3, maintains high for about two clock cycles after the transition of ϕ_{CA} to the low level since the least significant column address signal CAO stays at the low level. Then, since CA2 to CA8 are all low at this time, the column selection signal CSL1 becomes the high level pulse 604. After the transition of CA1 to the low level, CA1 and its complement $\overline{CA1}$ respectively stay low and high for about two clock cycles. However, the low-going signal ϕ_{CAR} causes CA1 and $\overline{CA1}$ to go low. This results in allowing the column selection signal CSL0 to become the high level pulse 605. On the other hand, with column addresses A_0 and A_1 being respectively high and low at t_1, and with column addresses A_0 and A_1 being respectively low and high at t_3, read data transfer pulses RDTP0 to RDTP3 are generated as shown in FIG. 49*b*.

Data on bit line pairs is transferred to first I/O line pairs by the pulse 600 of CSL0, and then transferred to first data pairs DIO_0, $\overline{DIO_0}$ and DIO_1, $\overline{DIO_1}$ via first PIO line pairs. FIG. 49*c* shows where a high level data and a low level data are respectively transferred in parallel on DIO_0 line and DIO_1 line. This parallel data is stored into latches 278*a* and 278*b* in the data output multiplexer 268 of FIG. 25, and the pulse 606 of RDTP1 then causes the stored data of the latch 278*b* associated with the line DIO_1 to output therefrom. Consequently, the data output buffer outputs the low level data RD1. Parallel data selected by the pulse 601 of CSL1 is transferred to second data line pairs DIO_2, $\overline{DIO_2}$ and DIO_3, $\overline{DIO_3}$ via second I/O line pairs and second PIO line pairs. It can be seen that data on DIO_2 and DIO_3 is respectively high and low. The pulse 607 of RDTP2 selects data stored into the latch 278*c* and the data output buffer then outputs the high level data RD2. Likewise, parallel data selected by the pulse 604 of CSL1 is transferred to data lines DIO_2 and DIO_3. The drawing of FIG. 49*c* shows that a low level data and a high level data are transferred on data lines DIO_2 and DIO_3, respectively. The transfer switch 276 of FIG. 25 becomes an off state with the high level pulse P of ϕ_{CL}. However, after the data, which was stored into the latch 278*c* via the line DIO_2 in the previous operation, has been transferred toward the data output buffer by the pulse 607 of RDTP2, the pulse P goes low. Then, the switch 276 becomes on. Thus, data on the data lines DIO_2 and DIO_3 is respectively stored into latches 278*c* and 278*d*. Data stored into the latch 278*c* is then outputted by the pulse 607 of RDTP2 and thereby the data output buffer 284 outputs the low level data RD3. Data stored into the latch 278*d* is then outputted by the pulse 608 of RDTP3, thereby resulting in outputting the high level data RD4 from the data output buffer 284. Likewise, data selected by the pulse 605 of CSL0 is transferred to first data line pairs. It can be seen in the drawing that a low level data and a high level data are respectively transferred in parallel on data lines DIO_0 and DIO_1. In the same manner as discussed above, this parallel data is selected in sequence by the pulses 609 and 610 shown in FIG. 49*b*, and the data output buffer 284 then outputs the low level data RD5 and the high level data RD6 in sequence. The data output buffer 284 then becomes a high impedance with the high level signal COSDQ.

FIG. 54 is a timing chart showing various operations at the $\overline{CAS}$ latency of 2 and the burst length of 4, using only one selected bank. Commands are given as follows: activation command at t_1, read command with external column addresses CA0 at t_2, $\overline{CAS}$ interrupt read command with external column addresses CB0 at t_3, $\overline{CAS}$ interrupt write command with external column addresses CC0 at t_7, $\overline{CAS}$ interrupt write command with external column addresses CDO at t_{10}, precharge command at t_{12} and data input/output masking command at t_6, t_9, t_{12} and t_{13}. Data QA0 and QA1 respectively output at t_3 and t_4 due to the read command issued at t_2, and data QB0 and QB1 successively output at t_5 and t_6 due to the read command issued at t_3. At t_7, data output is inhibited and stays in a high impedance state due to the data output masking command issued at t_6. At t_8 and t_9, write data DC0 and DC1 respectively input due to the write command at t_7. The data input masking command at t_9, write data DC0 and DC1 respectively input due to the write command at t_7. The data input masking command at t_9 interrupts receipt of write data at time t_{10}. Likewise, at t_{11} and t_{12}, write data DD0 and DD1 are respectively inputted due to the write command at t_{10}. The data input masking command issued at t_{12} and t_{14} after the precharge command at t_{12}.

FIG. 55 is a timing chart showing various operations at the $\overline{CAS}$ latency of 2 and the burst length of 4 with one selected bank. Read, write and data input/output masking operations are the same as those of FIG. 54. After issuance of freeze command at t_1, generation of a pulse of internal system clock ϕ_{CLK} corresponding to the pulse 536 of the system clock CLK is inhibited. Thus, the output of data at t_3 is frozen so as to output the same data as the output of data at t_2. Likewise, the internal system clock, in which the generation of corresponding pulse is precluded, causes operation of the column address counter to be frozen, thereby inhibiting writing of data at t_5.

FIG. 56 is a timing diagram showing a read operation at the $\overline{CAS}$ latency of 2 and the burst length of 4 with two banks. With activation command of the first bank at t_1, and with read command at t_2, successive data QA0 to QS3 outputs from time t_3. With activation command of the second bank at t_3, and with read command at t_4, successive data QB0 to QB3 also outputs from time t_5. At time t_6, simultaneous precharge command is issued at t_6.

FIG. 57 is a timing diagram showing an interleave read operation with the $\overline{CAS}$ latency of 2 and the burst length of 4. Activation command for the first bank is issued at time t_1, and that for the second bank is then issued at time t_2. Thus, data QA0 to QA3 is read out from the first bank from time t_3. At the same time, activation command for the second bank is issued at t_3. At time t_4, read command is issued for the second bank selected with the high level column address A_9. Then, after output of successive 4-bit data QA0 to QA3, read-out data QB0 and QB1 outputs from the second bank with no gap. At time t_5, read command is issued for the first bank with the low level column address A_9, thereby successively outputting read-out data QC0 and QC1 from the first bank. Read command is then issued for the second bank at time t_6, thereby outputting read-out data QD0 and QD1. Precharge command is then issued for the first bank at time t_7. Read command is then issued for the second bank at time t_8, thereby outputting read-out data QE0 to QE3. Precharge command is issued for the second bank with external addresses A_{10} and A_{11} at time A_9.

Explanation has been made on various operation modes with a single data input/output pad in connection with FIGS. 54 to 57. However, it should be noted that the present embodiment has eight data input/output pads and various applications are also possible.

OTHER EMBODIMENTS

As discussed hereinabove, the present synchronous DRAM has been modified with pulse $\overline{RAS}$. However, the

synchronous DRAM of the present invention may be embodied with the level $\overline{RAS}$. Various operation commands for the level $\overline{RAS}$ have been already explained. In order for the present synchronous DRAM to operate with the level $\overline{RAS}$, some circuits need modifications, but others may be used with no modification.

FIG. 58 is a drawing showing a schematic circuit diagram for a $\overline{RAS}$ buffer using the level $\overline{RAS}$. Referring to the drawing, an input buffer **70** and a synchronization circuit **108** which constitute the level $\overline{RAS}$ buffer **538** are the same in constructions and operations as the $\overline{RAS}$ buffer **56** for the pulse $\overline{RAS}$ showing in FIG. 9. The output of the synchronization circuit **108** is connected in common with a first $\overline{RAS}$ signal generator **540** for the first bank and with a second $\overline{RAS}$ signal generator **542** for the second bank via a latch **550**. The first $\overline{RAS}$ signal generator **540** comprises a flip-flop **545** for storing a first bank $\overline{RAS}$ signal in response to a bank selection signal $\overline{SRA11}$ produced by an address A_{11}. The flip-flop **545** is a NAND type flip-flop comprised of NAND gates **544** and **546**. One input terminal of the flip-flop **545** is connected to the output of a NOR gate **548**, and the other input terminal of the flip-flop **545** receives a $\overline{RAS}$ signal from the synchronization circuit **108**. The NOR gate **548** receives the bank selection signal $\overline{SRA11}$ on its first input terminal and a signal on its second input terminal which is staying at a high level during a refresh, a mode set or a test operation. The construction of the second $\overline{RAS}$ signal generator is the same as that of the first $\overline{RAS}$ signals generator. Thus, upon the activation of $\overline{RAS}$, if the external address A_{11} is low, i.e., $\overline{RAS}$ signal ϕ_{RC1} is then latched to a high level. At this time, since the NOR gate **548'** of the second $\overline{RAS}$ signal generator **542** outputs high, the flip-flop **545'** maintains the previous state. That is, if upon the activation of $\overline{RAS}$ in the previous operation, A_{11} was high, i.e., SRA11 was high, the second bank $\overline{RAS}$ signal ϕ_{RC2} keeps high. On the other hand, if $\overline{RAS}$ goes from a low level to a high level, the latch **550** latches a high level at the rising edge of the next system clock ϕ_{CLK}. Thus,. NAND gates **546** and **546'** each receives a low level, and thereby the signals ϕ_{RC1} and ϕ_{RC2} becomes low. That is, both banks go to precharge states. In addition, since o_{RFH} is low during a refresh, and o_{WCBR} is low during a mode set operation, the signals ϕ_{RC1} and ϕ_{RC2} are all high in such operations. Signals ϕ_{RL1} and ϕ_{RL2} are faster signals than the signals ϕ_{RC1} and ϕ_{RC2}.

FIG. 59 is a drawing showing address buffers for generating special addresses SRA10 and SRA11. These address buffers is independent buffers separated from the row and column address buffers. The address buffer **552** for producing **SRA10** in response to an address A_{10} is used in the pulse $\overline{RAS}$, but not in the level $\overline{RAS}$. The address buffer **552** has the same construction as previously mentioned buffers each comprised of the input buffer **70** and the synchronization circuit **108**. The address buffer **554** for producing SRA11 in response to an address A_{11} comprises a transfer switch 556 which is turned on in response to signals ϕ_{RC1} and ϕ_{RC2} produced in case of level $\overline{RAS}$. The transfer switch **556** is turned off by activation of either the first or the second bank and also serves to prevent from changing a logic level of the signal SRA11 with the system clock ϕ_{CLK} after activation of one of both banks. In case that the address buffer **554** is used for the pulse $\overline{RAS}$, it may be modified so that the output of the latch **558** becomes SRA11.

FIG. **60** is a schematic circuit diagram of a level $\overline{RAS}$ control circuit for generating a mode set control signal o_{WCBR} and a refresh clock o_{RFH} in case of the level $\overline{RAS}$. In the mode set control signal generator **200** of FIG. **14** used in the pulse $\overline{RAS}$, the transfer switches are gated by the signal ϕ_{RP}. However, in case of the level $\overline{RAS}$, the transfer switches are gated by a signal being produced by the signals ϕ_{RL1} and ϕ_{RL2} in place of the signals ϕ_{RP}. This is to generate the signals o_{WCBR} and o_{RFH} with faster signals ϕ_{RL1} and ϕ_{RL2} than ϕ_{RC1} and ϕ_{RC2}. Its operation is the same as that explained in connection with FIG. 14.

FIG. 61 is a drawing showing an operation timing charge of the synchronous DRAM using the level $\overline{RAS}$. The operation timing chart as shown in this drawing has relationship with that using the pulse $\overline{RAS}$ as shown in FIG. 54. In the drawing of FIG. 61, a precharge command is issued at time t_1. Remaining operations are the same as those of the pulse $\overline{RAS}$.

As explained hereinabove, the system design and using ways of the present synchronous DRAM have been explained in detail. Although embodiments of the present invention have been explained in connection with a synchronous DRAM, it would be obvious to those skilled in the art that the present invention may also be applied to other semiconductor memories.

What is claimed is:

1. A circuit in a semiconductor memory for programming operation modes of the semiconductor memory, the circuit comprising:
   - a mode set control signal generator for generating a mode set signal;
   - a plurality of code registers, each code register coupled to the mode set control signal generator to receive the mode set signal and store a code in response to the mode set signal, wherein the codes determine the operation modes of the semiconductor memory.

2. The circuit of claim 1 further including a burst length decoder, coupled to a plurality of the code registers, for decoding a burst length mode of the semiconductor memory based on at least two codes of the plurality of codes stored in the code registers.

3. The circuit of claim 2 wherein the burst length decoder includes a plurality of NAND logic gates and a plurality of inverters electrically interconnected to decode at least two codes of the plurality of codes stored in the code registers.

4. The circuit of claim 1 further including a latency decoder, coupled to a plurality of code registers, for decoding a latency mode of the semiconductor memory based on at least two codes of the plurality of codes stored in the code registers.

5. The circuit of claim 4 wherein the latency decoder includes a plurality of NAND logic gates and a plurality of inverters electrically interconnected to decode at least two codes of the plurality of codes stored in the code register.

6. The circuit of claim 1 further including a column addressing decoder, coupled to at least one of the code registers, for decoding a column addressing mode of the semiconductor memory.

7. The circuit of claim 1 further including:
   - a burst length decoder, coupled to at least two of the plurality of code registers, for decoding a burst length mode of the semiconductor memory; and
   - a latency decoder, coupled to at least two of the plurality of code registers, for decoding a latency mode of the semiconductor memory.

8. The circuit of claim 7 wherein:
   - the burst length decoder includes a plurality of NAND logic gates and a plurality of inverters electrically interconnected to decode three codes stored in the code registers for determining a burst length mode; and

the latency decoder includes a plurality of NAND logic gates and a plurality of inverters electrically interconnected to decode three codes stored in the code registers for determining a latency mode.

9. The circuit of claim 1 further including a plurality of input circuits, each input circuit receives an externally applied signal and, based thereon, generates an internal address signal, each input circuit is coupled to a corresponding code register, and wherein each code register includes a latch that stores a code based on the internal address signal, the latch stores the code in response to the mode set signal.

10. The circuit of claim 9 wherein each code register further includes an enable transistor having a gate electrode that receives a power on signal, the enable transistor enables the latch to store a code based on the internal address in response to a power-on signal.

11. The circuit of claim 9 wherein the latch stores the code in response to a power-on signal.

12. The circuit of claim 1 wherein the mode set control signal generator generates the mode set signal in response to at least two strobe signals selected from a group consisting of a row address strobe, a column address strobe and a write enable strobe.

13. The circuit of claim 1 further including:

an internal clock signal generator for generating an internal clock signal which is synchronized to an externally applied clock signal;

a row address strobe buffer for generating a first internal strobe signal in sync with the internal clock;

a column address strobe buffer for generating a second internal strobe signal in sync with the internal clock;

a write enable strobe buffer for generating a third internal strobe signal in sync with the internal clock; and

wherein the mode set control signal generator includes a mode set control signal decoder which generates the mode set signal in response to the first, second and third internal strobe signals.

14. The circuit of claim 13 wherein:

the row address strobe buffer includes a latch for latching the first internal strobe signal in sync with the internal clock based on a transition of the row address strobe;

the column address strobe buffer includes a latch for latching the second internal strobe signal in sync with the internal clock based on a transition of the column address strobe; and

the write enable strobe buffer includes a latch for latching the third internal strobe signal in sync with the internal clock based on a transition of the write enable address strobe.

15. The circuit of claim 14 wherein the wherein the mode set control signal decoder includes at least one NAND logic gate that generates the mode set signal in response to the first, second and third internal strobe signals.

16. A circuit in a synchronous semiconductor memory for programming operation modes of the synchronous semiconductor memory, the memory being capable of synchronously reading and writing data relative to an external clock signal, the circuit comprising:

a mode set control signal generator for generating a mode set signal in response to a row address strobe, a column address strobe and a write enable strobe;

a plurality of code registers, coupled to the mode set control signal generator to receive the mode set signal, wherein each code register stores a code in response to the mode set signal, the plurality of code registers including:

a first code register for storing a first code;

a second code register for storing a second code;

a third code register for storing a third code;

a fourth code register for storing a fourth code;

a fifth code register for storing a fifth code; and

a sixth code register for storing a sixth code;

wherein the first, second and third codes determine the burst length mode of the semiconductor memory and the fourth, fifth and sixth codes determine the latency mode of the semiconductor memory.

17. The circuit of claim 16 further including:

a burst length decoder, coupled to the first, second and third code registers, for decoding a burst length mode of the semiconductor memory; and

a latency decoder, coupled to the fourth, fifth and sixth code registers, for decoding a latency mode of the semiconductor memory.

18. The circuit of claim 17 wherein:

the burst length decoder includes a plurality of NAND logic gates and a plurality of inverters electrically interconnected to decode the codes in the first, second and third code register; and

the latency decoder includes a plurality of NAND logic gates and a plurality of inverters electrically interconnected to decode the codes in the fourth, fifth and sixth code registers.

19. The circuit of claim 16 further including a plurality of input circuits, each input circuit receives an externally applied signal and, based thereon, generates an internal address signal, each input circuit is coupled to a corresponding code register, and wherein each code register includes a latch that stores a code based on the internal address signal, the latch stores the code in response to the mode set signal.

20. The circuit of claim 19 wherein each code register further includes an enable transistor having a gate electrode that receives a power on signal, the enable transistor enables the latch to store a code based on the internal address in response to a power-on signal.

21. The circuit of claim 19 wherein the latch stores the code in response to a power-on signal.

22. The circuit of claim 16 wherein the mode set control signal generator generates the mode set signal in response to at least two strobe signals selected from a group consisting of a row address strobe, a column address strobe and a write enable strobe.

23. The circuit of claim 16 further including:

an internal clock signal generator for generating an internal clock signal which is synchronized to an externally applied clock signal;

a row address strobe buffer for generating a first internal strobe signal in sync with the internal clock;

a column address strobe buffer for generating a second internal strobe signal in sync with the internal clock;

a write enable strobe buffer for generating a third internal strobe signal in sync with the internal clock; and

wherein the mode set control signal generator includes a mode set control signal decoder which generates the mode set signal in response to the first, second and third internal strobe signals.

24. The circuit of claim 23 wherein:

the row address strobe buffer includes a latch for latching the first internal strobe signal in sync with the internal clock based on a transition of the row address strobe;

the column address strobe buffer includes a latch for latching the second internal strobe signal in sync with

the internal clock based on a transition of the column address strobe;

the write enable strobe buffer includes a latch for latching the third internal strobe signal in sync with the internal clock based on a transition of the write enable address strobe; and

the mode set control signal decoder includes at least one NAND logic gate that generates the mode set signal in response to the first, second and third internal strobe signals.

25. A circuit in a semiconductor memory for programming operation modes of the semiconductor memory, the circuit comprising:

a mode set control signal generator for generating a mode set signal;

a plurality of code registers, each code register stores a code in response to the mode set signal; and

a burst length decoder, coupled to the code registers, to decode a burst length mode of the semiconductor memory based on the codes stored in the code registers.

26. The circuit of claim 25 wherein the burst length decoder includes a plurality of NAND logic gates and a plurality of inverters electrically interconnected to decode the codes stored in the code registers.

27. The circuit of claim 25 further including a plurality of input circuits, each input circuit receives an externally applied signal and, based thereon, generates an internal address signal, each input circuit is coupled to a corresponding code register, and wherein each code register includes a latch that stores a code based on the internal address signal, the latch stores the code in response to the mode set signal.

28. The circuit of claim 27 wherein each code register further includes an enable transistor having a gate electrode that receives a power on signal, the enable transistor allows the latch to store the input in response to the power-on signal.

29. The circuit of claim 27 wherein the latch stores the code in response to a power-on signal.

30. The circuit of claim 25 wherein the mode set control signal generator generates the mode set signal in response to at least two strobe signals selected from a group consisting of a row address strobe, a column address strobe and a write enable strobe.

31. The circuit of claim 25 further including:

an internal clock signal generator for generating an internal clock signal that is synchronized to an externally applied clock signal;

a row address strobe buffer for generating a first internal strobe signal, the row address strobe buffer includes a latch for latching a transition of the row address strobe in sync with the internal clock;

a column address strobe buffer for generating a second internal strobe signal, the column address strobe buffer includes a latch for latching a transition of the column address strobe in sync with the internal clock;

a write enable strobe buffer for generating a third internal strobe signal, the write enable strobe buffer includes a latch for latching a transition of the write enable strobe in sync with the internal clock; and

wherein the mode set control signal generator includes a decoder, the decoder includes at least one NAND logic gate that generates the mode set signal in response to the first, second and third internal strobe signals.

32. A circuit in a semiconductor memory for programming operation modes of the semiconductor memory, the circuit comprising:

a mode set control signal generator for generating a mode set signal;

a plurality of code registers, each code register stores a code in response to the mode set signal; and

a latency decoder, coupled to the code registers, to decode a latency mode of the semiconductor memory based on the codes stored in the code registers.

33. The circuit of claim 32 wherein the latency decoder includes a plurality of NAND logic gates and a plurality of inverters electrically interconnected to decode the codes from the code register.

34. The circuit of claim 32 further including a plurality of input circuits, each input circuit receives an externally applied signal and, based thereon, generates an internal address signal, each internal address signal being stored in a latch in a corresponding code register in response to a mode set signal.

35. The circuit of claim 34 wherein each code register further includes an enable transistor having a gate electrode that receives a power on signal, the enable transistor allows the latch to store the input in response to the power-on signal.

36. The circuit of claim 34 wherein the latch stores the code in response to a power-on signal.

37. The circuit of claim 32 wherein the mode set control signal generator generates the mode set signal in response to at least two strobe signals selected from a group consisting of a row address strobe, a column address strobe and a write enable strobe.

38. The circuit of claim 32 further including:

an internal clock signal generator for generating an internal clock signal that is synchronized to an externally applied clock signal;

a row address strobe buffer for generating a first internal strobe signal, the row address strobe buffer includes a latch for latching a transition of the row address strobe in sync with the internal clock;

a column address strobe buffer for generating a second internal strobe signal, the column address strobe buffer includes a latch for latching a transition of the column address strobe in sync with the internal clock;

a write enable strobe buffer for generating a third internal strobe signal, the write enable strobe buffer includes a latch for latching a transition of the write enable strobe in sync with the internal clock; and

wherein the mode set control signal generator includes a decoder, the decoder includes at least one NAND logic gate that generates the mode set signal in response to the first, second and third internal strobe signals.

39. A circuit in a semiconductor memory for programming operation modes of the memory comprising:

a mode set control signal generator for generating a mode set signal;

a pluralitv of input circuits, each input circuit receives a corresponding externally applied signal and, based thereon, generates an internal signal; and

a plurality of code registers, each code register is coupled to a corresponding input circuit to receive the internal signal and store a codes in response to the mode set signal, based on the internal signal, wherein the codes determine the operation modes of the semiconductor memory.

40. The circuit of claim 39 further including:

a burst length decoder, coupled to at least two of the plurality of the code registers, for decoding a burst length mode of the semiconductor memory; and

a latency decoder, coupled to at least two of the plurality of the code registers, for decoding a latency mode of the semiconductor memory.

41. The circuit of claim **40** wherein:

the burst length decoder includes a plurality of NAND logic gates and a plurality of inverters electrically interconnected to decode the codes from the code register to determine a burst length mode; and

the latency decoder includes a plurality of NAND logic gates and a plurality of inverters electrically interconnected to decode the codes from the code register to determine a latency mode.

42. The circuit of claim **39** wherein each code register further includes a latch far storing the code, an NMOS transistor having a gate electrode for receiving the mode set control signal, and a PMOS transistor having a gate electrode for receiving the inverse of the mode set control signal, wherein the NMOS and PMOS transistors, in response to the mode set control signal allow the code to be stored in the latch.

43. The circuit of claim **42** wherein each code register further includes an enable transistor having a gate electrode that receives a power on signal, the enable transistor allows the latch to store the input in response to the power-on signal.

44. The circuit of claim **42** wherein the latch stores the code in response to a power-on signal.

45. The circuit of claim **39** wherein the mode set control signal generator generates the mode set signal in response to at least two strobe signals selected from a group consisting of a row address strobe, a column address strobe and a write enable strobe.

46. The circuit of claim **39** further including:

an internal clock signal generator for generating an internal clock signal that is synchronized with an externally applied clock signal;

a row address strobe buffer for generating a first internal strobe signal in sync with the internal clock;

a column address strobe buffer for generating a second internal strobe signal in sync with the internal clock;

a write enable strobe buffer for generating a third internal strobe signal in sync with the internal clock; and

wherein the mode set control signal generator includes a decoder which generates the mode set signal in response to the first, second and third internal strobe signals.

47. The circuit of claim **46** wherein:

the row address strobe buffer includes a latch for latching the first internal strobe signal in sync with the internal clock based on a transition of the row address strobe;

the column address strobe buffer includes a latch for latching the second internal strobe signal in sync with the internal clock based on a transition of the column address strobe;

the write enable strobe buffer includes a latch for latching the third internal strobe signal in sync with the internal clock based on a transition of the write enable address strobe; and

the decoder includes at least one NAND logic gate that generate the mode set signal in response to the first, second and third internal strobe signals.

* * * * *

United States Patent [19]
Vogley et al.

[11] **Patent Number: 5,982,694**
[45] **Date of Patent: Nov. 9, 1999**

[54] **HIGH SPEED MEMORY ARRANGED FOR OPERATING SYNCHRONOUSLY WITH A MICROPROCESSOR**

[75] Inventors: **Wilbur Christian Vogley**, Missouri City; **Anthony Michael Balistreri**, Houston; **Karl M. Guttag**, Missouri City; **Steven D. Krueger**, Houston; **Duy-Loan T. Le**; **Joseph H. Neal**, both of Sugarland; **Kenneth A. Poteet**, Houston; **Joseph P. Hartigan**, Stafford; **Roger D. Norwood**, Houston, all of Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **08/747,120**

[22] Filed: **Nov. 8, 1996**

Related U.S. Application Data

[63] Continuation of application No. 08/327,540, Oct. 21, 1994, Pat. No. 5,587,954.

[51] **Int. Cl.**[6] **G11C 13/00**
[52] **U.S. Cl.** **365/221**; 365/233
[58] **Field of Search** 365/189.01, 189.04, 365/189.05, 189.08, 221, 233, 230.01, 230.03, 230.09

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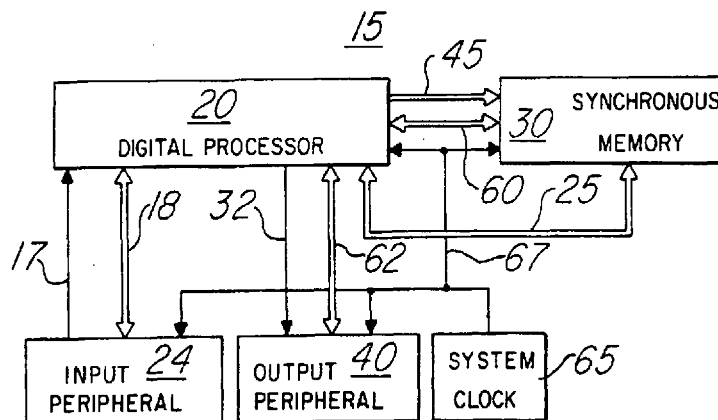
Primary Examiner—Terrell W. Fears
Attorney, Agent, or Firm—Robert N. Rountree; Lawrence J. Bassuk; Richard L. Donaldson

[57] **ABSTRACT**

A synchronous random access memory is arranged to be responsive directly to a system clock signal for operating synchronously with the associated microprocessor. The synchronous random access memory is further arranged to either write-in or read out data in a synchronous burst operation or synchronous wrap operation in addition to synchronous random access operations. The synchronous random access memory device may be fabricated as a dynamic storage device or as a static storage device.

59 Claims, 12 Drawing Sheets



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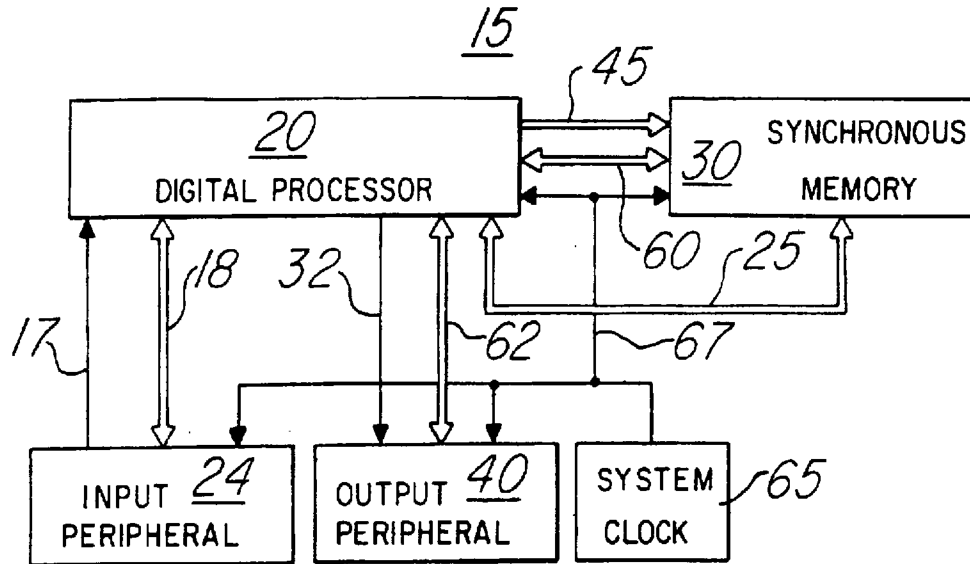

FIG. 1

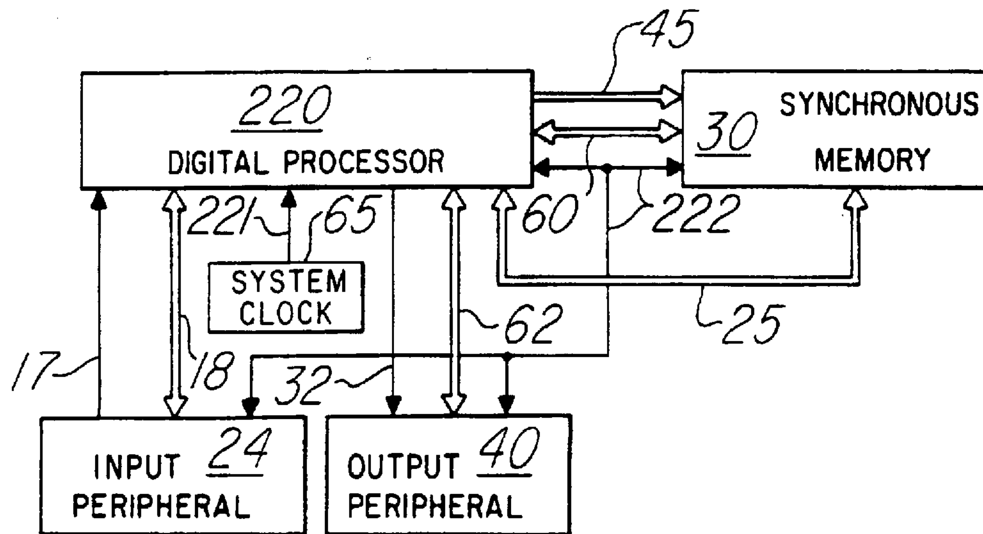

FIG. 24

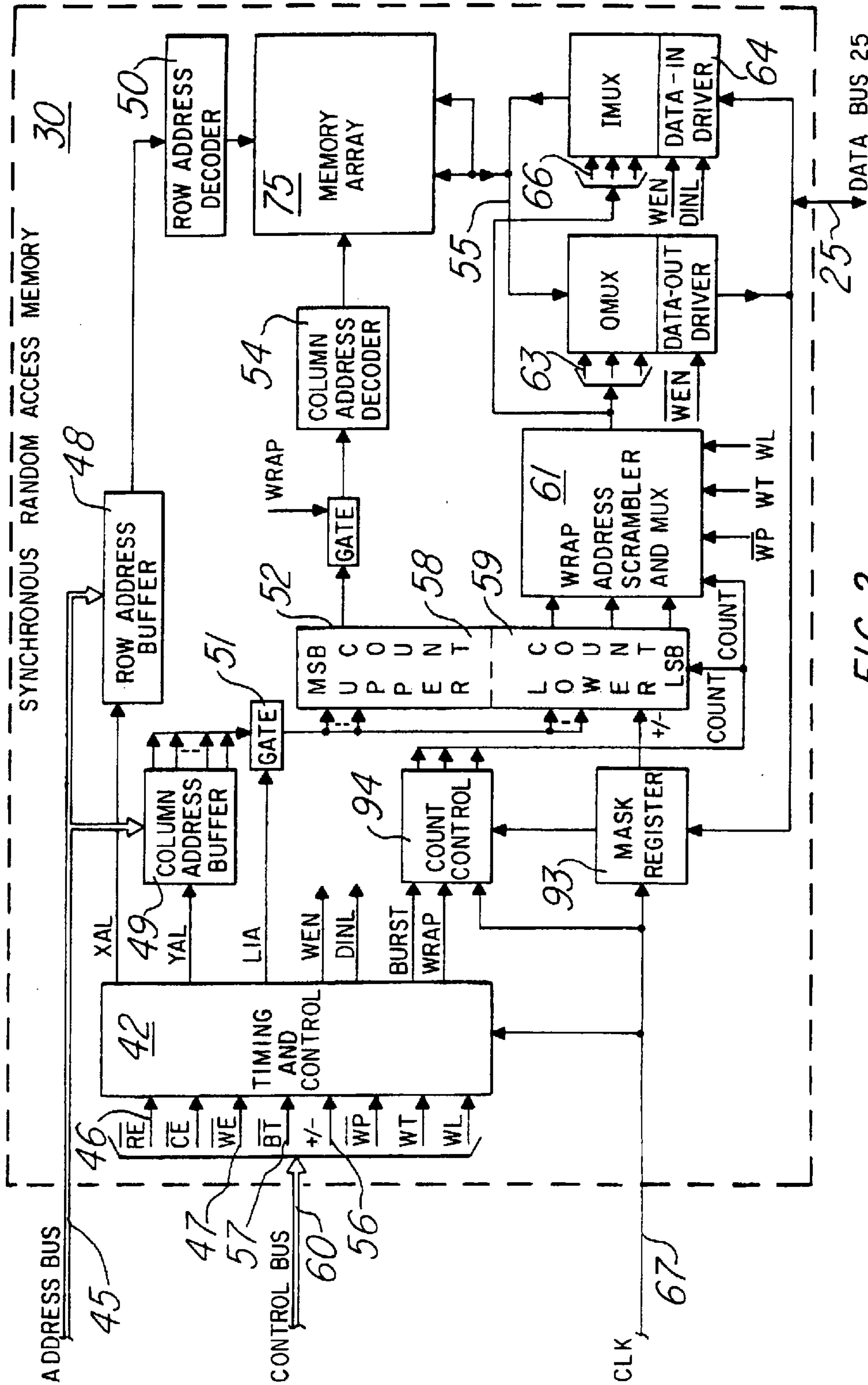

FIG. 2

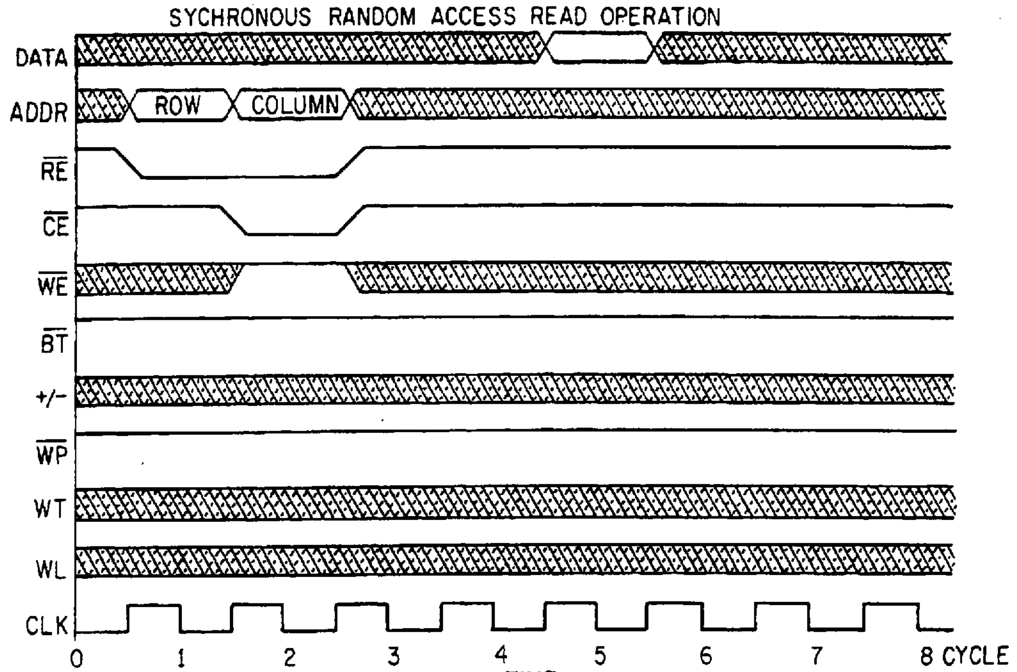

FIG. 3

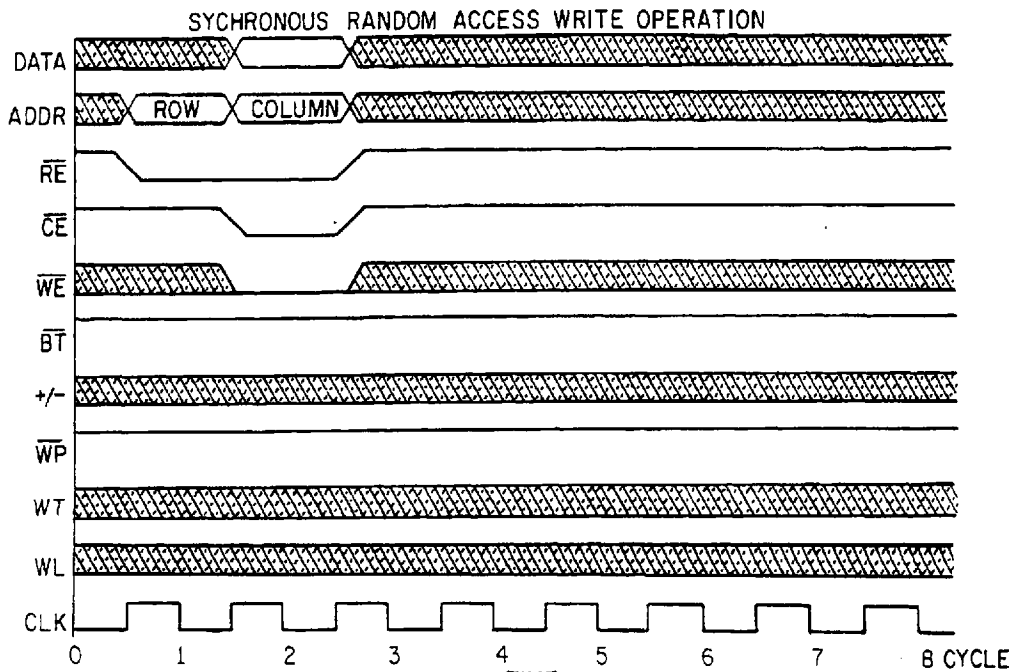

FIG. 4

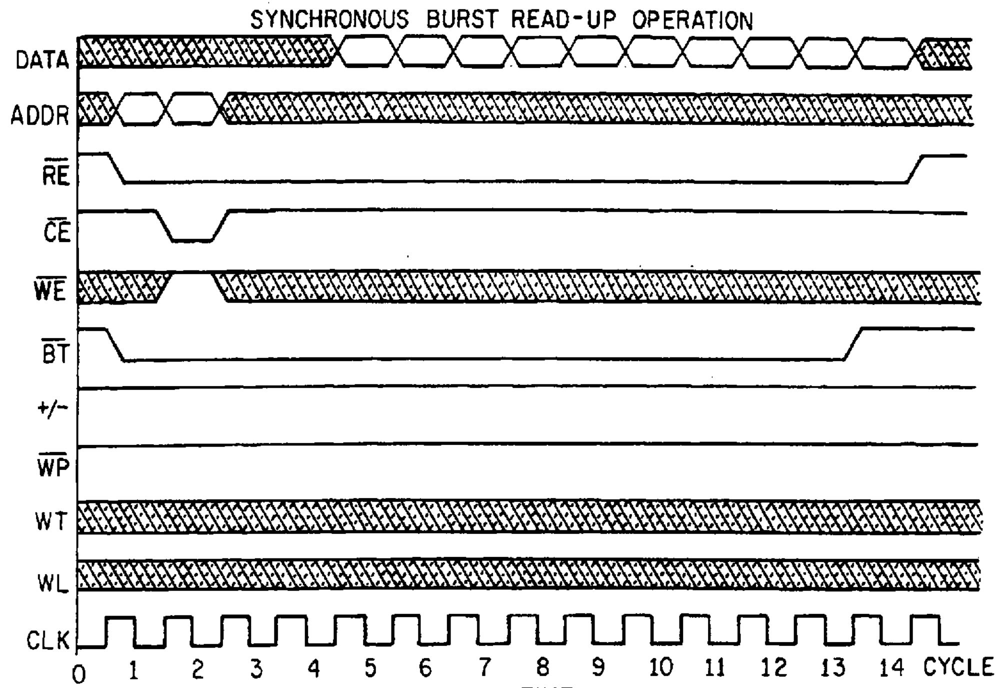

FIG. 5

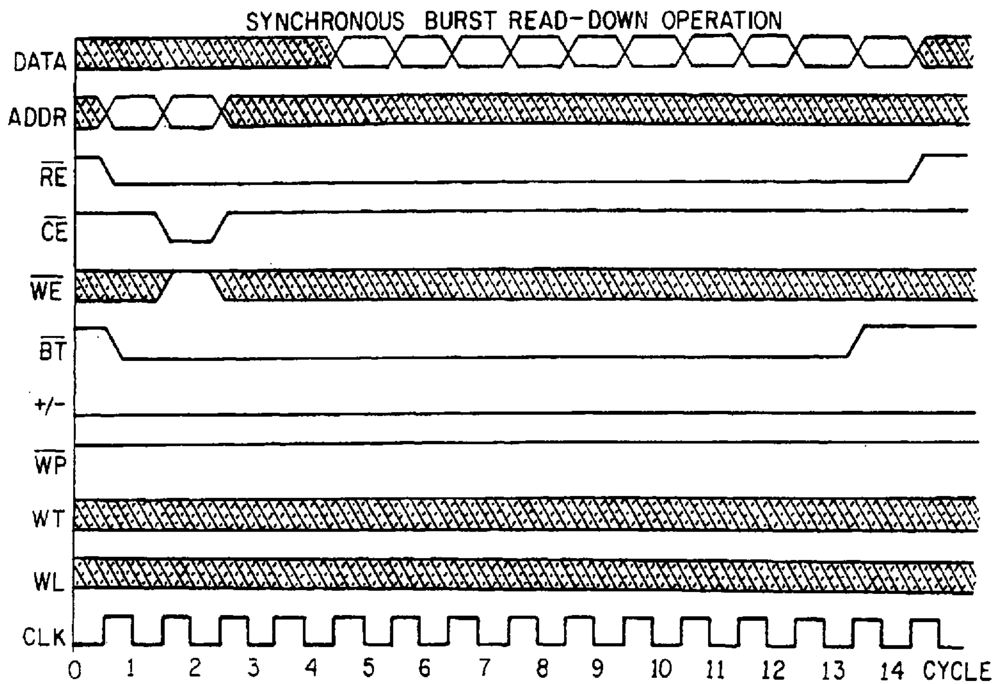

FIG. 7

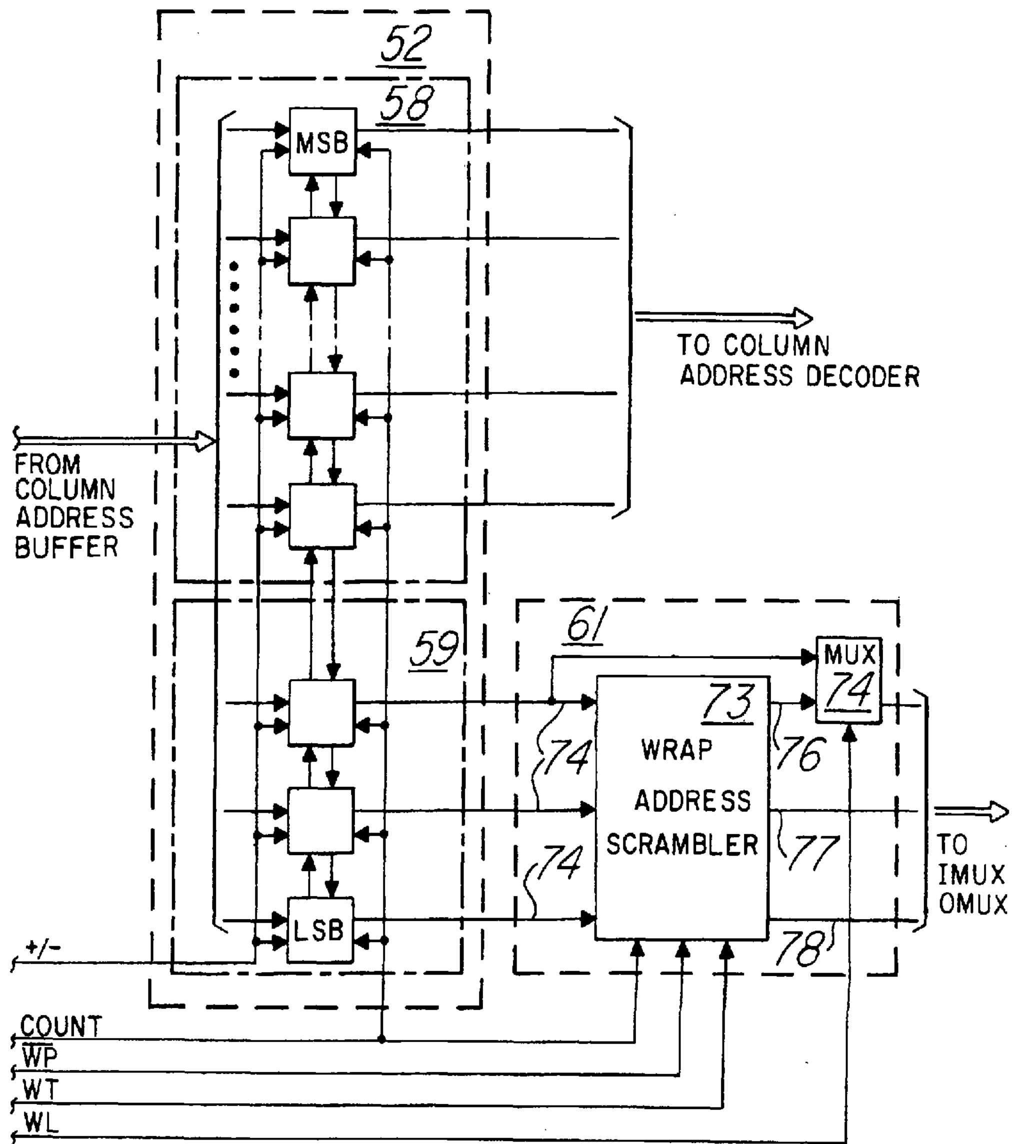

FIG. 6

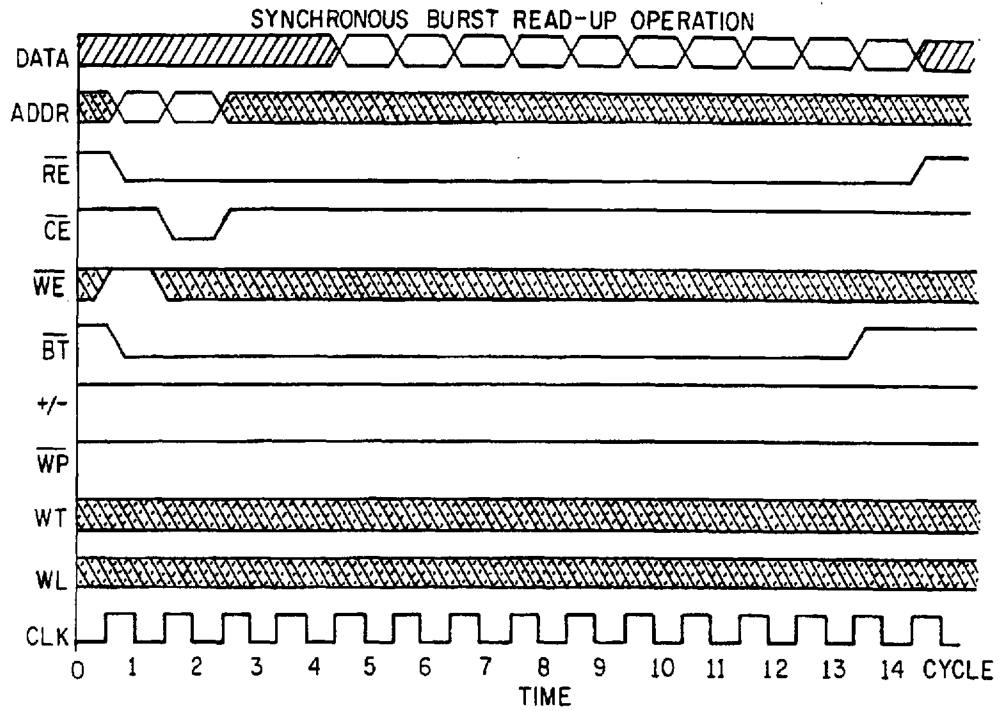

FIG. 8

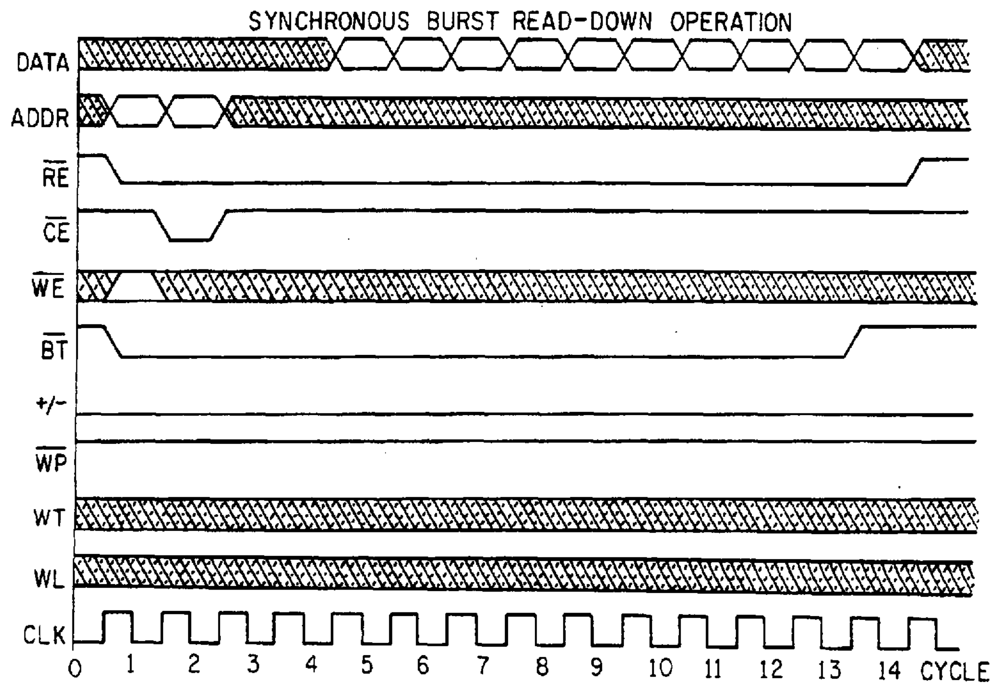

FIG. 9

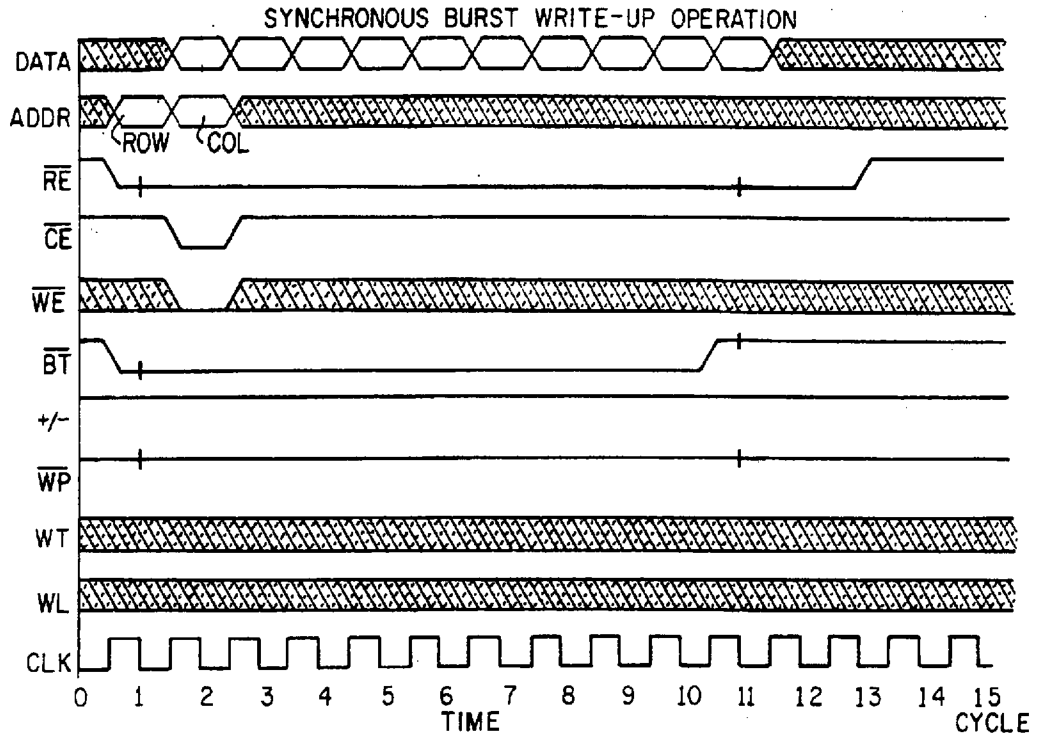

FIG. 10

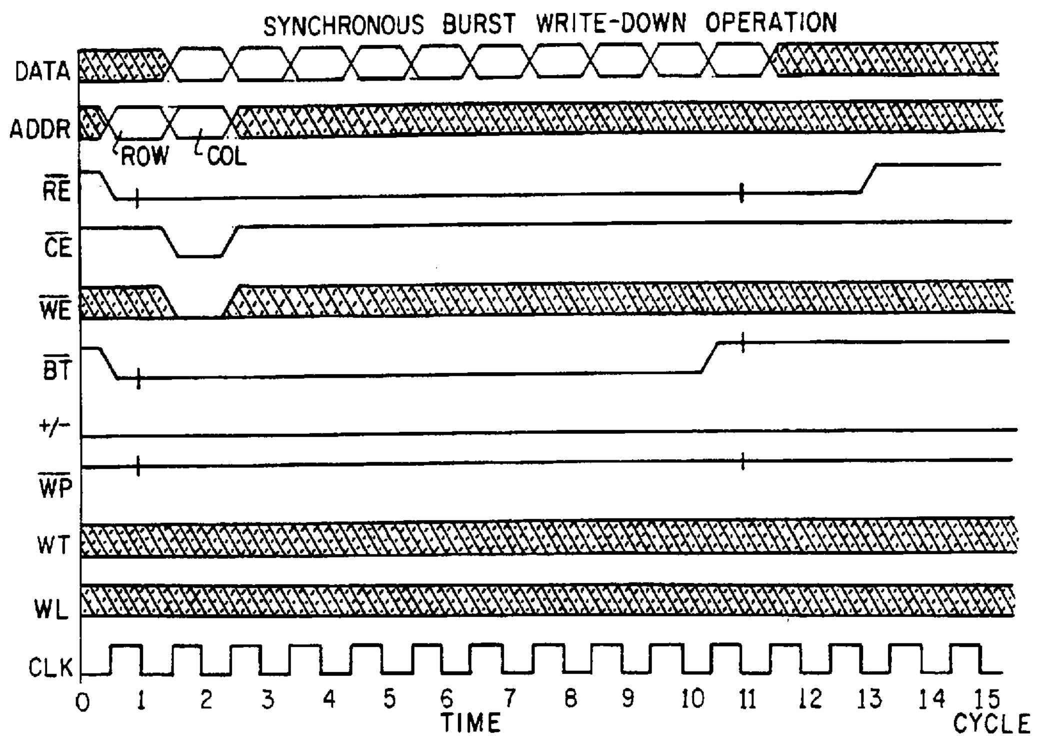

FIG. 11

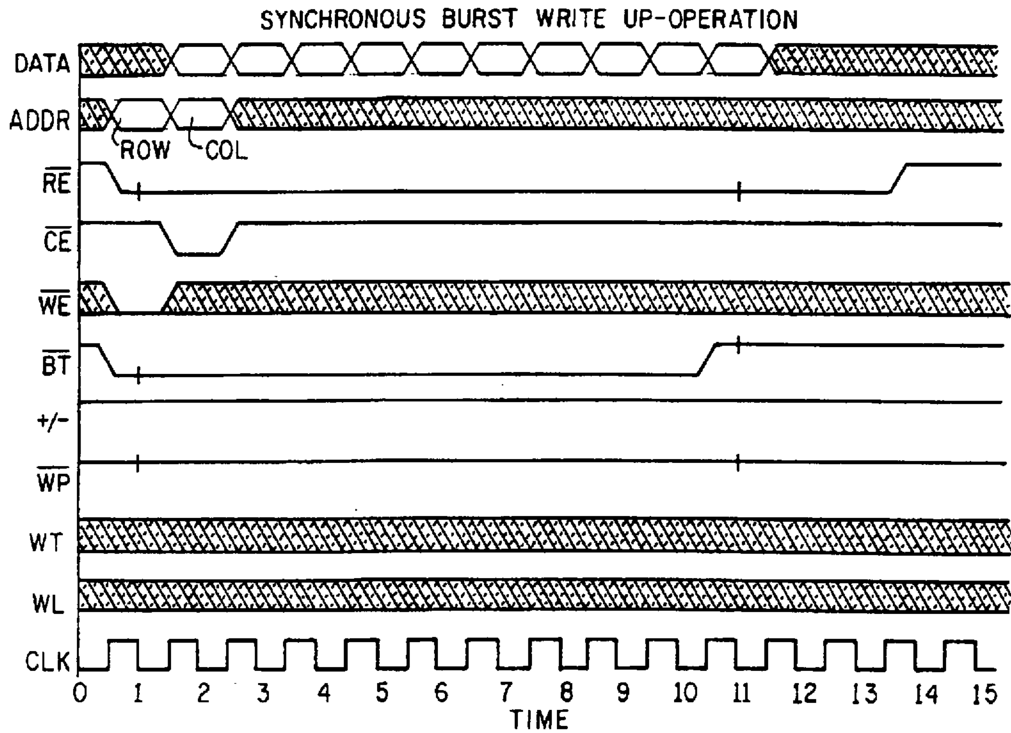

FIG. 12

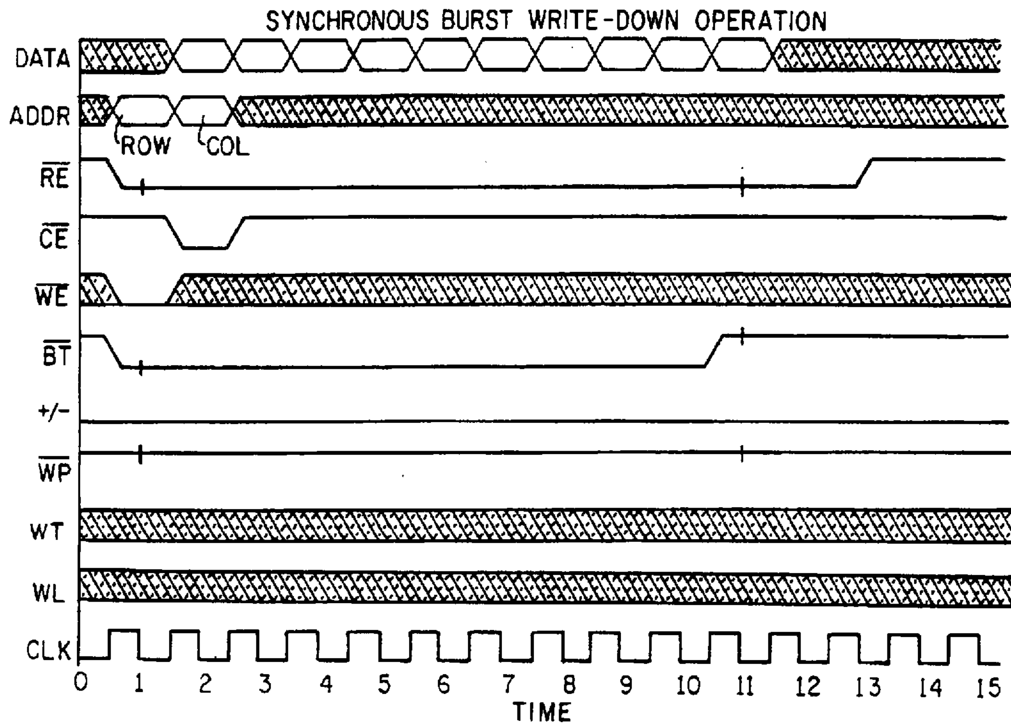

FIG. 13

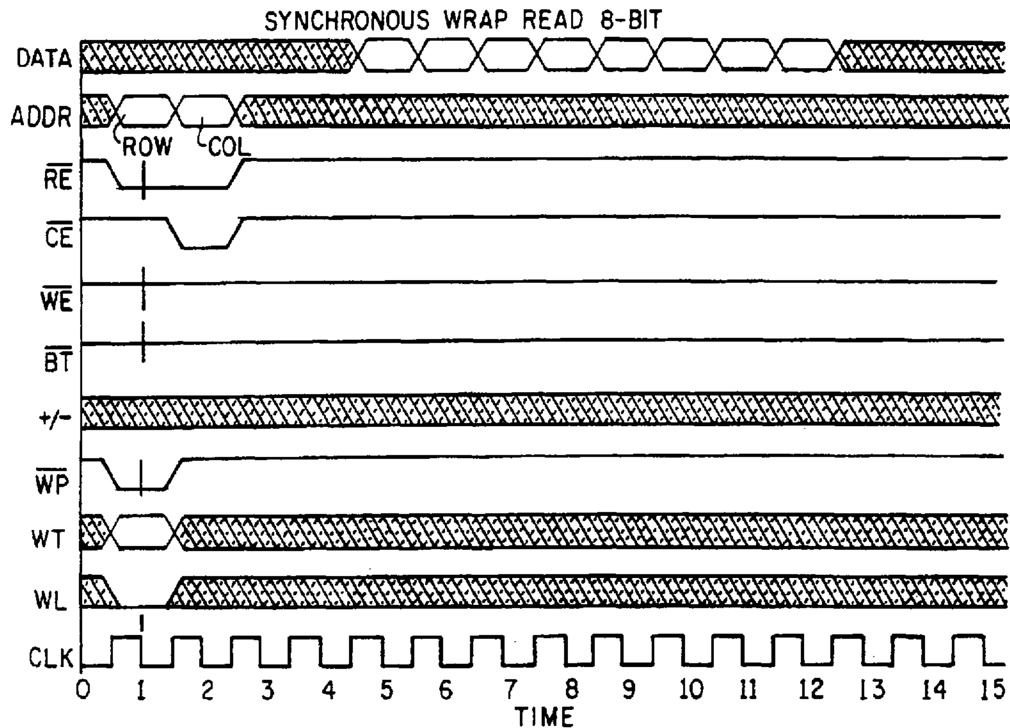

FIG. 14

TABLE I

WRAP LENGTH WL=0				
INITIAL INPUT ADDRESS			OUTPUT ADDRESS SEQUENCE	
A2	A1	A0	WRAP TYPE WT=0	WRAP TYPE WT=1
0	0	0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
0	0	1	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
0	1	0	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
0	1	1	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
1	0	0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
1	0	1	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
1	1	0	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
1	1	1	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0

FIG. 15

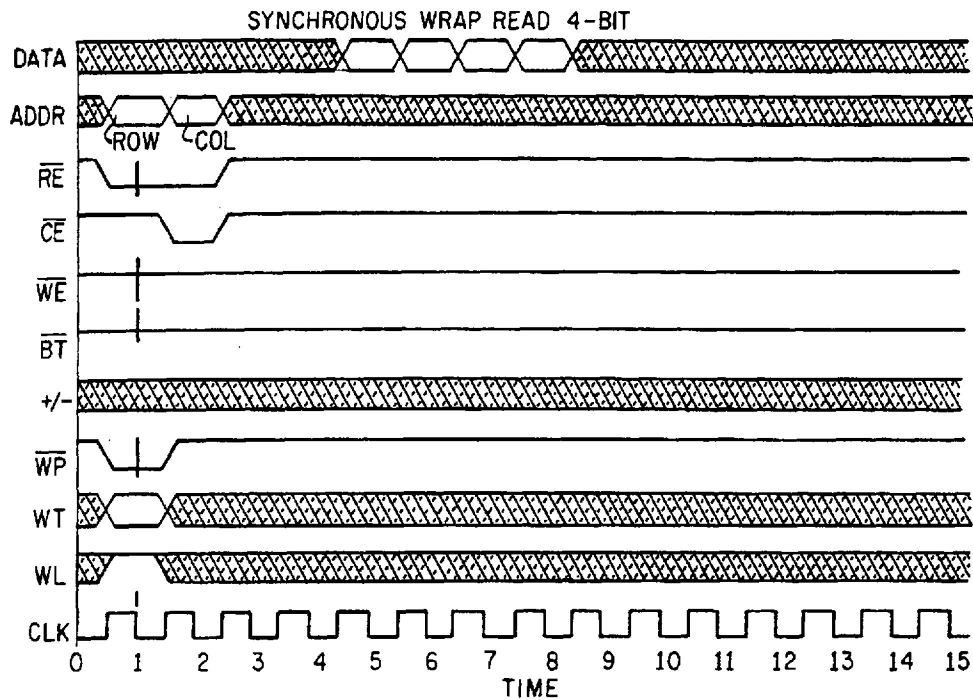

FIG. 16

TABLE II

WRAP LENGTH WL=1			
INITIAL INPUT ADDRESS		OUTPUT ADDRESS SEQUENCE	
A1	A0	WRAP TYPE WT=0	WRAP TYPE WT=1
0	0	0, 1, 2, 3	0, 1, 2, 3
0	1	1, 2, 3, 0	1, 0, 3, 2
1	0	2, 3, 0, 1	2, 3, 0, 1
1	1	3, 0, 1, 2	3, 2, 1, 0

FIG. 17

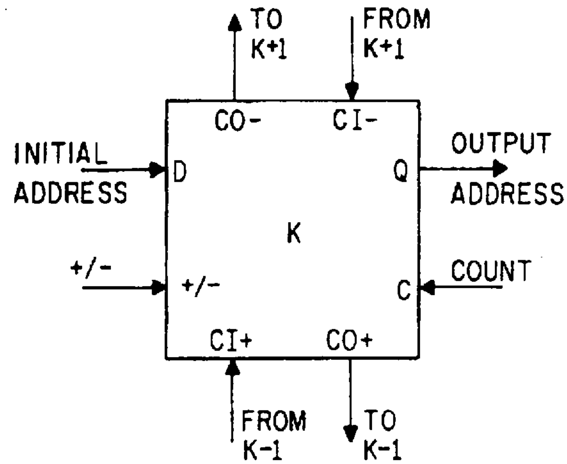

FIG. 18

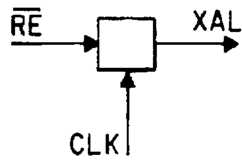

FIG. 19

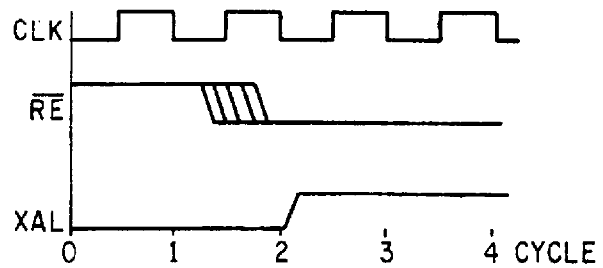

FIG. 20

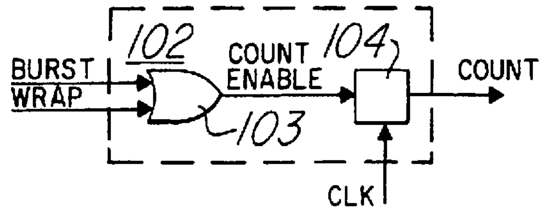

FIG. 21

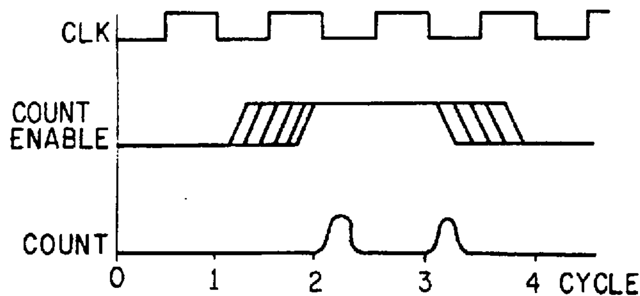

FIG. 22

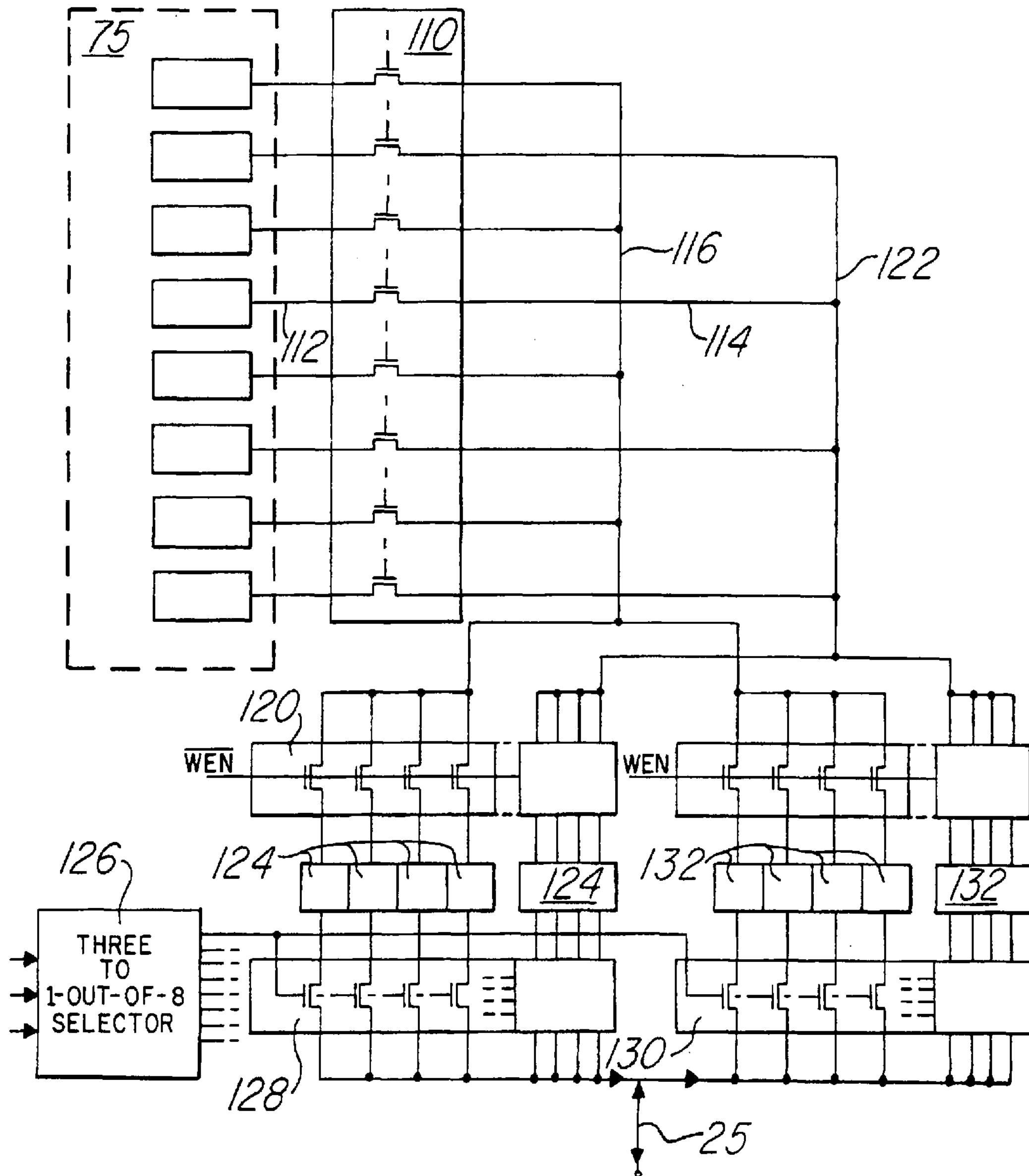

FIG. 23

HIGH SPEED MEMORY ARRANGED FOR OPERATING SYNCHRONOUSLY WITH A MICROPROCESSOR

This is a continuation of application Ser. No. 08/327,540, filed Oct. 21, 1994, U.S. Pat. No. 5,587,954.

BACKGROUND OF THE INVENTION

This invention relates to random access memory (RAM) arranged for operating in a data processing system.

In the past, semiconductor random access memory operated faster than the associated microprocessor. During the late 1970's and early 1980's, the microcomputer market was in the early stages of development. At that time, a microcomputer system included a microprocessor and a dynamic random access memory. In a microcomputer arrangement, the microprocessor ran synchronously in response to a clock signal, but the dynamic random access memory ran asynchronously with respect to the operation of the microprocessor. The microprocessor clock was applied to a controller circuit that was interposed between the microprocessor and the dynamic random access memory. In response to the microprocessor clock signal, the controller derived other control or clock signals which ran the dynamic random access memory operation.

Typical operating speeds of the microprocessor and the dynamic random access memory were different from each other. A microprocessor cycle time was in a range of 400–500 nanoseconds while a dynamic random access memory cycle time was approximately 300 nanoseconds. Thus the dynamic random access memory was able to operate faster than its associated microprocessor. The memory completed all of its tasks with time to spare. As a result, the microprocessor operated at its optimum speed without waiting for the memory to write-in data or read out data.

Subsequently, as the semiconductor art developed, the operating speeds of microprocessors and memory devices have increased. Microprocessor speeds, however, have increased faster than dynamic random access memory speeds. Now microprocessors operate faster than their associated dynamic random access memory. For instance, a microprocessor cycle time is approximately 40 nanoseconds and a dynamic random access memory cycle time is approximately 120 nanoseconds. The microprocessor completes all of its tasks but must wait significant periods of time for the dynamic random access memory.

Having the microprocessor waiting for the memory is a problem that has been attracting the attention of many microcomputer designers. High speed static cache memories have been added to the microcomputer systems to speed up access to data stored in the memory. A significant part of the problem is to speed up access to data in the memory without significantly increasing the cost of the microcomputer system. Cache memory, however, is significantly more expensive than dynamic random access memory.

An existing problem with dynamic random access memory devices is that they require a substantial amount of peripheral circuitry between the microprocessor and the memory for generating several control signals. So many interdependent control signals are generated by long logic chains within the peripheral circuitry that microcomputer systems designers must resolve very complex timing problems. The delay caused by the timing problems and the fact that memories now are accessed slower than the associated microprocessor cause problems of excessive time delays in microcomputer system operations.

SUMMARY OF TEE INVENTION

These and other problems are solved by a random access memory which is arranged to be responsive directly to a system clock signal for operating synchronously with the associated digital processor. The synchronous random access memory is further arranged to write-in or read out data in either a synchronous burst mode or a synchronous wrap mode in addition to synchronous random access operations. Such a synchronous random access memory device may be fabricated as a dynamic or as a static storage device.

Control signals from the digital processor are used for controlling various memory operations. As an alternative, the digital processor may process a clock signal that is used as the system clock for operating both the digital processor and the synchronous random access memory. The digital processor may be a microprocessor.

BRIEF DESCRIPTION OF THE DRAWING

A better understanding of the invention may be derived by reading the following detailed description with reference to the drawing wherein:

FIG. 1 is a block diagram of a data processing system including a synchronous random access memory;

FIG. 2 is a block diagram of a synchronous random access memory;

FIG. 3 is a timing diagram of a synchronous random access read operation;

FIG. 4 is a timing diagram of a synchronous random access write operation;

FIG. 5 is a timing diagram of a synchronous burst read-up operation;

FIG. 6 is a block diagram of a column address counter and the wrap address scrambler;

FIG. 7 is a timing diagram of a synchronous burst read-down operation;

FIG. 8 is a timing diagram of another synchronous burst read-up operation;

FIG. 9 is a timing diagram of another synchronous burst read-down operation;

FIG. 10 is a timing diagram of a synchronous burst write-up operation;

FIG. 11 is a timing diagram of a synchronous burst write-down operation;

FIG. 12 is a timing diagram of another synchronous burst write-up operation;

FIG. 13 is a timing diagram of another synchronous burst write-down operation;

FIG. 14 is a timing diagram of a synchronous wrap read 8-bit operation;

FIG. 15 is a truth table for a wrap address scrambler used in a synchronous wrap read 8-bit operation;

FIG. 16 is a timing diagram of a synchronous wrap read 4-bit operation;

FIG. 17 is a truth table for a wrap address scrambler used in a synchronous wrap read 4-bit operation;

FIG. 18 is a schematic block diagram of a stage for the column address counter of FIG. 17;

FIG. 19 is a logic schematic diagram of a timing gate circuit;

FIG. 20 is a timing diagram for the operation of the gate circuit of FIG. 19;

FIG. 21 is a logic schematic diagram for another timing gate circuit;

FIG. 22 is a timing diagram for the operation of the gate circuit of FIG. 20;

FIG. 23 is a block diagram of an input multiplexer and an output multiplexer arrangement for the synchronous memory of FIG. 2; and

FIG. 24 is a block diagram of an alternative data processing system including a synchronous random access memory.

DETAILED DESCRIPTION

Referring now to FIG. 1, a data processing system **15** includes a digital processor **20** which receives digital data by way of a bus **17** from an input peripheral device **24**. The digital processor **20** may be a microprocessor. Control signals pass between the digital processor **20** and the input peripheral device **24** by way of a control bus **18**. The digital processor **20** processes that data and other data, all of which may be transmitted by way of a data bus **25** for storage in and retrieval from a synchronous memory, device **30**. The digital processor **20** also sends resulting output data via an output data bus **32** to an output peripheral device **40** where the output data may be displayed or used for reading, viewing or controlling another device that is not shown. Control signals are transmitted between the digital processor **20** and the synchronous memory device **30** by way of a control bus **60**. Control signals also are transmitted between the digital processor **20** and the output peripheral device **40** by way of a control bus **62**. System clock signals are produced by a system clock device **65** and are applied through a clock lead **67** to the digital processor **20**, the synchronous memory device **30**, the input peripheral device **24**, and the output peripheral device **40**.

From time to time during operation of the data processing system **15**, the digital processor **20** accesses the synchronous memory **30** for writing data into storage cells or for reading data from the storage cells thereof. Storage cell row and column addresses, generated by the digital processor **20**, are applied through an address bus **45** to the synchronous memory **30**. Data may be sent by way of the data bus **25** either from the digital processor **20** to be written into the synchronous memory **30** or to be read from the synchronous memory **30** to the digital processor **20**.

Control signals, produced by the digital processor **20** and transmitted by way of the control bus **60** to the synchronous memory **30** include a row address control signal $\overline{RE}$, a column address control signal $\overline{CE}$, a write signal $\overline{WE}$, a burst signal $\overline{BT}$, a burst direction signal +/−, a wrap select signal $\overline{WP}$, a wrap-type signal WT, a wrap-length signal WL, and others. Control signals may also be transmitted from the synchronous memory **30** to the digital processor **20**.

Referring now to FIG. 2, the synchronous random access memory **30** includes a memory array **75** of metal-oxide-semiconductor (MOS) dynamic storage cells arranged in addressable rows and columns. The memory array **75** of storage cells is similar to the well known arrays of cells used in dynamic random access memory devices. Either complementary metal-oxide-semiconductor (COOS) or bipolar complementary metal-oxide-semiconductor (BICMOS) technology may be used for fabricating the memory array **75**.

Several other circuit blocks are shown in FIG. 2. These other circuit blocks are designed and arranged for operating the array of storage cells synchronously with the digital processor **20** of FIG. 1 in response to the common system clock signal CLK, which may be gated by the digital processor, as discussed subsequently with respect to FIG. **20**. The circuit blocks other than the array of storage cells may be fabricated as either CMOS or BICMOS circuits.

The synchronous random access memory **30** is operable for synchronous random access read or write operations, for synchronous burst read or write operations, and for synchronous wrap read or write operations. All types of synchronous operations are to be described fully hereinafter. Such descriptions are to be made in reference to timing diagrams and truth tables presented in FIGS. **3–5** and **7–17**. In the timing diagrams, a DON'T CARE state is represented by cross-hatching.

Referring now to FIGS. **3** and **2** for a synchronous random access read operation, an N bit wide row address and the row address control signal $\overline{RE}$ are applied to the address bus **45** and a lead **46**. Control signals, such as the signal $\overline{RE}$ and others, are active low signals. The write signal $\overline{WE}$ on a lead **47** being high, at clock cycle time **2**, designates a read operation. The synchronous read operation commences at a falling edge of the system clock signal CLK at signal time **1**. For this illustrative embodiment, the system clock times operations in synchronism at the negative-going edges of the clock pulses, such as at the cycle times **1**, **2**, **3**, etc.. In other embodiments, not shown herein, the system may time operations at the positive-going edges or on both negative-going and positive-going edges of the clock pulses.

When the system clock CLK has a negative-going edge while the row address is applied at the clock cycle time **1** and the row address control signal $\overline{RE}$ is low, the row address is latched into the row address buffer **48**.

Since the illustrative embodiment has an N bit wide address bus, that bus is time shared by row addresses and column addresses. During the clock cycle time **2** following the latching of the row address into the row address buffer **48**, a column address is applied to the address bus **45**. While the column address control signal $\overline{CE}$ is low and the write signal $\overline{WE}$ is high at the clock cycle time **2**, the system clock goes low, latching the column address into the column address buffer **49**.

Concurrently with the latching of the column address into the column address buffer, the row address is being decoded through the row address decoder **50**. The row address decoder **50** decodes the binary number row address into a one-out-of-2^N selection. As a result of the one-out-of-2^N selection, an active signal is applied to the wordline of the one selected row. This wordline remains selected throughout the remainder of the random access read operation.

At the next negative-going edge of the system clock CLK, a load initial address signal LIA enables a group of load count transfer gates **51** to move the initial column address into upper count and lower count sections of a column address counter **52**. The most significant bits of the column address are latched into the upper count section **58** and the least significant bits of the column address are latched into the lower count section **59** of the column address counter **52**. All of those address bits in the column address counter **52** represent the initial column address to be applied to the memory array for the read out operation. Since the operation being described is a synchronous random access operation, the initial column address is the only column address to be applied to the memory array during the read operation.

The most significant bits of the initial column address are applied from the upper count section **58** through a gate **53** to the column address decoder **54** for selecting M columns of storage cells of the memory array, from which data are to be read out. These most significant bits of the column address are decoded by the column address decoder **54** to enable a block of M columns of storage cells in the memory array **75**.

Data bits are read from a group of M storage cells, determined by a part of the decoded column address, i.e., the

decoded most significant bits of the column address. These M data bits are transferred in parallel from the memory array 75 through a group of leads 55 to an output multiplexer OMUX where they are latched for output.

A one-out-of-M selection is made by the output multiplexer OMUX in response to control signals applied to the output multiplexer from the lower count section 59 of the column address counter 52. The least significant bits of the initial column address, residing in the lower count section 59, determine which bit latched in the output multiplexer OMUX is the one-out-of-M bit to be gated through the output multiplexer to a lead in the data bus 25.

Referring now to FIGS. 4 and 2 for a synchronous random access write operation, row addressing and column addressing occur similar to the synchronous random access read operation except that the write signal $\overline{WE}$ is at a low level at the clock cycle time 2 to designate the synchronous random access write operation. The decoded row address from the row decoder 50 enables one row of storage cells in the memory array 75. The most significant bits of the column address, decoded by the column decoder 54, enable a block of M column leads in the array. The selected set of storage cells at the addressed intersections of the addressed row and the set of M addressed columns are enabled to receive the data that is to be written. The least significant bits of the column address (residing in the lower count section 59 of the column address counter 52) determine control signals that are applied to the input multiplexer IMUX for determining which one-out-of-M bit on the data bus 25 is transmitted through the input multiplexer IMUX to be written into the memory array 75. The one-out-of-M bit is applied to the associated column lead of the selected block of columns of storage cells in the memory array 75. That bit of data is written into the storage cell at the address selected by the row address and the initial column address. The other M−1 bits of data, related to the selected set of M columns, are not written into the memory array 75 because the input multiplexer IMUX does not transmit those M−1 bits to the associated column lines of the memory array 75.

The next subsequent operation of the memory array following either the synchronous read operation or the synchronous write operation may be another synchronous random access operation, i.e., either a synchronous read operation or a synchronous write operation. The same row and column addresses or a different row or column address can be used to select the storage cell for the next access. A synchronous burst or a synchronous wrap operation also may follow the synchronous random access read or write operations.

In the foregoing discussion of the synchronous read and write operations, the illustrative embodiment includes an N bit wide address bus 45 that is time-shared by row and column addresses. In another useful embodiment, not shown, the address bus may be wide enough so that both the row and column addresses are applied concurrently in parallel. As a result, both addresses are latched simultaneously into their respective address buffers, i.e., row address buffer 48 and column address buffer 49. Otherwise the synchronous random access read and write operations proceed, as previously described.

It is noted that for the synchronous random access write operations, the row and column addresses may be latched either before data is latched or at the same time.

In addition to the synchronous random access read and write operations, the embodiment of FIGS. 1 and 2 can perform a synchronous burst read operation and a synchronous burst write operation.

In the synchronous burst read operation, a group of bits is read rapidly from a sequence of column addresses along a common row of storage cells in the memory array 75. The sequence of addresses can be either in an ascending order of column addresses (UP) or in a descending order of column addresses (DOWN). The direction, or polarity, of the sequence of column addresses is determined by a burst direction signal +/− on a lead 56. The length of the burst, i.e., the number of bits in the burst, is determined by the duration of the low burst select signal $\overline{BT}$ that is applied, on a lead 57, by the digital processor 20 of FIG. 1. When the burst select signal $\overline{BT}$ goes high, the synchronous burst read operation is terminated.

Generally a synchronous burst read operation is similar to a random access read operation. There are some differences that will become apparent in the subsequent description of the synchronous burst read operation. Similar aspects of the operations are described minimally so that differences can be fully described without excessive redundant description.

Referring now to FIG. 5, there is shown a timing diagram for a synchronous burst read-up operation of the synchronous memory device 30 of FIG. 2. The row address control signal $\overline{RE}$ and the burst select signal $\overline{BT}$ go active low at clock cycle time 1 to commence the operation. The burst direction signal +/− is at a high level to indicate that the sequence of column addresses is an incremented sequence. A row address is latched into the row address buffer 48 at clock cycle time 1. An initial column address is latched into the column address buffer 49 at clock cycle time 2. The write signal $\overline{WE}$ is at a high level to indicate the read operation. The row address is decoded by the row address decoder 50 to select a row of storage cells in the memory array 75. In response to the load initial address signal LIA, the most significant bits of the initial column address are gated through gates 51 into the upper count section 58 of the column address counter 25 while the least significant bits of the same address are gated into the lower count section 59 of the column address counter 52. The most significant bits are decoded in the column address decoder 54 to select two blocks of M columns for read out from the memory array 75. One of those columns is selected for transmitting its bit through the output multiplexer OMUX as the initial bit of the desired sequence of bits on the data bus 25.

Referring now to FIG. 6, there is a detailed block diagram of the upper count section 58 and the lower count section 59 of the column address counter 52. After the initial address is decoded, the upper count and lower count sections of, the column address counter 52 are incremented by a count clock signal COUNT. The upper and lower counters are organized as a continuous series of binary counter stages. As shown in FIG. 2, a gate 51 is provided for transferring the initial column address into the upper count and lower count sections of the column address 52 in response to the load initial address signal LIA. The up or down direction of the column address sequence is determined by the burst direction signal +/−. A least significant bit counter stage LSB and a most significant bit counter stage MSB are indicated in FIG. 6. The upper count section 58 includes all of the counter stages except the $\log_2(2M)$ least significant bit counter stages which make up the lower count 59.

In a synchronous burst read-up operation after the initial column address is decoded, the address residing in the upper and lower count sections 58 and 59 is incremented under control of the clock signal COUNT. The next address produced in the upper and lower count sections 58 and 59 is the initial column address incremented by one. The next sequential bit is transmitted through the output multiplexer

OMUX from the column of storage cells of the memory thereby addressed.

A first block of M columns and a next adjacent higher order block of M columns of storage of the memory array **75** are addressed simultaneously by the column address decoder **54**. Bits are transmitted through the output multiplexer OMUX from a first one of those blocks while the bits from the second block of M columns are accessed from the memory array and are applied to the output multiplexer OMUX. When the first set of addresses is exhausted, the sequence of addresses continues through the second set of M addresses while a third set of M addresses is applied to the output multiplexer in place of the first set. By thus alternating sets of addresses in a rising order, the desired burst of bits is read out of the memory array **75**. These alternating sets of addresses for selecting the desired sequence of bits enables the data to be read out through the output multiplexer OMUX to the data bus **25** in a continuous stream without having to wait for each address to be supplied from the digital processor **20** of FIG. **1**. The sequential bits of data transmitted out of the output multiplexer OMUX are in a continuous stream at the rate of the system clock CLK.

In the synchronous burst mode, the number of bits of data read out of the memory array depends upon the duration of the low active burst signal $\overline{BT}$ on the lead **57**. When the burst signal $\overline{BT}$ goes high, the synchronous burst read operation is terminated.

A synchronous burst read operation also can be made from memory cells having a sequence of descending column addresses in the memory array **75**. There are a couple of distinctions between this synchronous burst read-down operation and the synchronous burst read-up operation which was just described.

Referring now to FIGS. **7** and **2** for a synchronous burst read-down operation, the only difference in the control signals is that the burst direction signal +/− is a low level to signify that the count in the upper and lower count sections of the column address counter **52** is decremented in response to each cycle of the counting clock COUNT. Bits from a first set of M addressable columns and from the next adjacent lower order set of M addressable columns are read from the memory array **75** and are applied to the output multiplexer OMUX. Individual bits are transmitted through the output multiplexer in response to a descending sequence of addresses applied to the output multiplexer OMUX from the lower count section **59** by way of a wrap address scrambler **61** and leads **63**. In the synchronous burst operation, the wrap address scrambler allows the address from the lower count section **59** to be transmitted without change to the multiplexer. Since the count in the column address counter is being decremented in response to the clock signal COUNT, the sequence of bits transmitted out through the output multiplexer OMUX is read from columns having a sequence of descending addresses in the memory array **75**.

Blocks of M column addresses are selected by the count in the upper count section **58** of the column address counter **52**. Bits from alternate ones of those sets of column addresses are selected by the addresses of the individual columns, as determined by the count in the lower count section **59** of the column address counter **52**.

FIGS. **8** and **9**, respectively, are alternative timing diagrams for synchronous burst read-up and synchronous burst read-down operations of the synchronous random access memory **30** of FIG. **2**. The difference in the timing diagrams of FIGS. **8** and **9** with respect to the diagrams of FIGS. **5** and **7** is that the write signal WE is sampled at the clock cycle time **1** instead of at the clock cycle time **2**. Either timing is acceptable for adequate operation of the synchronous random access memory **30**.

The just described synchronous burst read operations (either read-up or read-down) provide the data processing system of FIG. **1** with a capability to read out of a row of the memory array **75** an entire sequence of data bits (a burst) at a rate of one bit per cycle of the system clock CLK for the active duration of the burst signal $\overline{BT}$. A single row address and only the initial column address are forwarded from the digital processor **20** to the synchronous random access memory **30**. The rest of the sequence of column addresses is produced by the column address counter **52** at the rate of a new address for every cycle of the system clock CLK.

Another important operation of the data processing system **15** is a synchronous burst write operation, which enables the digital processor **20** of FIG. **1** to apply a sequence of data bits onto the data bus **25** in consecutive system time slots with a row address and only an initial column address to determine where they are to be stored in the synchronous random access memory **30**. The upper and lower count sections **58** and **59** determine a sequence of column addresses following the initial column address. The sequence of data bits on the data bus **25** is stored in the addressed storage cells of the memory array **75** in synchronism with system clock cycles.

Referring now to FIG. **10**, there is shown a timing diagram of a synchronous burst write-up operation for storing the sequence of data bits into the memory array **75** of FIG. **2**. In such an operation, data bits are stored in storage cells having the same row address and sequential column addresses in ascending order.

As shown in FIG. **10**, the write signal $\overline{WE}$ and the burst signal $\overline{BT}$ are low, and the wrap signal $\overline{WP}$ is held high. Since this is a synchronous burst write-up operation, the burst direction signal +/− is high to produce an ascending sequence of column addresses. Because the row address control signal $\overline{RE}$ is low, the timing and control circuit of FIG. **2** produces the row address latch signal XAL during the system clock cycle time **1**. Because the column address control signal $\overline{CE}$ is low during clock cycle **2**, the timing and control circuit produces the column address latch signal YAL during the system clock cycle time **2**. The row address and the initial column address are latched into the respective row and column address buffers **48** and **49** to begin the burst write-up operation. The row address is decoded through the row decoder **50**. The initial column address is transferred into the upper and lower count sections of the column address decoder **52**. The most significant bits go into the upper count section **58**, and the least significant bits into the lower count section **59**. Advantageously a sequence of data bits, starting with the first bit on the data bus **25** during the system clock cycle time **2**, is latched, one bit at a time, consecutively into an input multiplexer IMUX in synchronism with the system clock CLK. Data bits are applied through the data bus **25** to the data-in driver circuit **64**. A write enable signal WEN, produced by the timing and control circuit **42**, enables data from the data bus **25** to be transferred to the data-in drivers **64**. A data-in latch signal DINL, also produced by the timing and control circuit **42**, latches data from the data bus **25** into the data-in drivers **64**. For the synchronous burst operation, the most significant bits of the initial column address, in the upper count section **58**, are decoded into a selection of two blocks of M columns. Signals from lower count section **59** pass through to the output of the wrap address scrambler **61** and are applied by way of leads **66** to the control inputs of the input multiplexer

IMUX for determining which one-out-of-2M bit is transmitted to the associated column of storage cells in the memory array **75**. The least significant bits of the initial column address are decoded into a one-out-of-2M selection for enabling one of the bits, associated with the initial column address, to be transmitted from the data bus **25** through the input multiplexer IMUX to be stored in the memory array **75**. A storage cell located at the intersection of the row address and the initial column address is the first storage location. Each subsequent cycle of the system clock causes the binary count in the combination of the upper and lower count sections of the column address counter **52** to be incremented. The following data bits, selected from the data bus **25** in synchronism with the system clock, are each stored in the sequence in a separate one of the storage cells along the accessed row in the memory array **75**. In response to the clock signal COUNT, the count in the lower count and upper count sections of the column address counter **52** is incremented (because the burst direction signal +/− is high) for directing the following data bits from the data bus **25** into sequentially addressed columns of storage cells of the memory array **75**. The burst of data bits and the generation of the ascending sequence of addresses continues until the burst select signal $\overline{BT}$ returns to the high level.

Referring now to FIG. **11**, there is shown a timing diagram for a synchronous burst write-down operation to store data bits into the memory array **75** of FIG. **2**. This operation is similar to the just described synchronous burst write-up operation. Because the row address control signal $\overline{RE}$ is low, the timing and control circuit **42** of FIG. **2** produces the row address latch signal XAL and latches the row address during the system clock cycle time **1**. Because the column address control signal $\overline{CE}$ is low during system clock cycle time **2**, the timing and control circuit **42** produces the column address latch signal YAL and latches the initial column address during that system clock cycle.

Different, however, than the previously described synchronous burst write-up operation, the burst direction signal +/− is low causing the upper and lower count sections of the column address counter **52** to decrement the address, residing therein, in response to every cycle of the system clock CLK. Thus the sequence of column addresses starts with the initial column address and decreases in sequential order for each subsequent system clock cycle. Data bits from the data bus **25** are directed through the input multiplexer IMUX to be written into storage cells located along a row at columns having sequentially decreasing addresses in the memory array **75**.

FIGS. **12** and **13**, respectively, are alternative timing diagrams for synchronous burst write-up and write-down operations of the synchronous random access memory **30** of FIG. **2**. The difference in the timing diagrams of FIGS. **12** and **13** with respect to the diagrams of FIGS. **10** and **11** is that the write signal WE is sampled at the clock cycle time **1** instead of at the clock cycle time **2**. Either timing is acceptable for adequate operation of the synchronous random access memory **30**.

The just described synchronous burst write (either write-up or write-down) operations provide the data processing system of FIG. **1** with a capability to write into a row of the memory array **75** an entire sequence of data bits (a burst) at a rate of one bit per cycle of the system clock CLK for the active duration of the burst signal $\overline{BT}$. A single row address and only the initial column address are forwarded from the digital processor **20** to the synchronous random access memory **30**. The rest of the sequence of column addresses is produced by the column address counter circuitry **52** at the rate of one new column address for every cycle of the system clock CLK.

Referring now to FIG. **14**, there is shown a timing diagram of a synchronous wrap read 8-bit operation of the synchronous random access memory of FIG. **2**. From a row of the memory array **75**, eight bits of data are to be read from a single row and from columns selected by the initial column address latched in the upper count section **58** of the column address counter **52**. Row addressing and initial column addressing occur as previously described. Gate **53** is enabled by a wrap control signal WRAP during system clock cycle time **1** for transmitting the initial column address to the column address decoder for reading out data from the columns of the memory array **75**. Such data is directed through the output multiplexer OMUX in response to a selection made by the least significant bits of the initial column address latched in the lower count section **59** of the column address counter **52**, as modified by a subsequent conversion. The least significant bits of the initial column address are converted into a sequence of addresses generated by the wrap address scrambler and multiplexer **61**.

FIG. **15** is TABLE I showing the logic of the conversion process that is accomplished by the wrap address scrambler and multiplexer. As shown in TABLE I, the wrap length signal WL is zero (WL=0). Headings for the columns of the table include, as an input, the three least significant bits of the initial column address **A0**, **A1**, **A2**. The wrap type signal WT may be either low (WT=0) or high (WT=1). Each line of the truth table presents a sequence of output addresses which are produced by the wrap address scrambler **61** in response to the three least significant bits from the initial column address residing in the column address counter **52**. The wrap address scrambler **61** produces the sequence for which ever wrap type WT is applied in synchronism with the system clock signal CLK.

Thus in the top line for wrap type signal WT equal to zero (WT=0) and initial address **A0=0**, **A1=0**, **A2=0**, the sequence of addresses produced by the wrap address scrambler is 0,1,2,3,4,5,6,7. The translation from the initial input address to the output sequence of address may be accomplished in a number of ways, e.g., by a look-up table. Output addresses from the wrap address scrambler **61** access similarly ordered outputs from the output multiplexer OMUX. Since only eight bits are latched into the output multiplexer, only eight addresses are produced and used for reading those bits to the data bus **25**.

If the wrap type signal equals (WT=1), then the sequence of addresses occurs in the order shown in the right most column. Thus when the wrap type signal WT=1 and the least significant three bits of the initial column address are **A0=0**, **A1=1**, **A2=0**, the order of addresses applied to the output multiplexer is 2,3,0,1,6,7,4,5. Bits from output multiplexer positions, so identified, are read out in that order onto the data bus **25** of FIG. **2**.

Referring now to FIGS. **16** and **17**, there is shown a timing diagram and a truth table for a synchronous wrap read operation that reads out four bits rather than the eight bits read out during the operation represented by FIGS. **14** and **15**. For the four bit wrap read operation, the wrap length signal equals (WL=1). Since there are only four bits to be read through the output multiplexer, only the two least significant initial column address bits **A0** and **A1** are applied to select the order of output. Selection of the wrap type is made by the state of the wrap type signal WT to determine the order of addresses for reading out of the output multiplexer onto the data bus **25**. The wrap address scrambler and multiplexer **61** converts the least significant two bits of the initial column address into the desired wrap sequence in accordance with the TABLE II presented in FIG. **17**.

The just described synchronous wrap read (either 8-bit or 4-bit) operations provide the data processing system of FIG. 1 with a capability to read from a row of the memory array **75** a group of data bits in an order prescribed by the column address of the first bit accessed. The group of bits is read out at a rate of one bit per cycle of the system clock CLK until the selected eight bits or four bits are read out. A single row address and only the initial column address are forwarded over the address bus from the digital processor **20** to the synchronous random access memory **30**. The rest of the group of column addresses is produced by the column address counter circuitry **52** and the wrap address scrambler and multiplexer **61** at a rate of a new column address for every cycle of the system clock CLK.

A similar synchronous wrap write operation is enabled by applying a low active write signal $\overline{WE}$ to commence the operation.

Referring once again to FIG. **6**, an initial column address is applied in parallel to and is latched into the stages of the column address counter **52**. The burst direction signal +/− is applied to all of the stages to determine whether the count is incremented or decremented in response to each cycle of the clock signal COUNT. The clock signal COUNT also is applied to all stages. Each stage of the column address counter **52** is interconnected with the adjacent stages on both sides. There is a connection path for incrementing the count and a separate path between each pair of adjacent stages for decrementing the count.

FIG. **18** shows one stage K of the column address counter **52** in greater detail. At the top of stage K, there are two terminals that are interconnected with the next higher order stage K+1 of the column address counter **52**. Carry-out decrement terminal CO− and carry-in decrement terminal CI− are connected with the adjacent stage K+1. At the bottom of stage K, there are two terminals connected with the next lower order stage K−1. A carry-in increment terminal CI+ and carry out increment terminal CO+ are interconnected with the adjacent stage K−1. The initial address data is applied to the data input terminal D. The burst direction signal +/− is applied to the increment/decrement terminal +/−. The clock signal COUNT is applied to a clock input terminal C, and output addresses (to be forwarded to the memory array **75** and the input and output multiplexers) occur at the output terminal Q.

Referring once again to FIG. **6**, the wrap address scrambler **73** has three inputs **74** received from the lower count section **59** of the column address counter **52**.

In FIG. **6** for synchronous random access and synchronous burst operations, those three inputs are transmitted directly to three outputs **76**, **77** and **78**. Outputs **77** and **78** are applied directly to control the input multiplexer IMUX and the output multiplexer OMUX. The output **76** is applied to a multiplexer **74** which for the synchronous burst operation transmits the signal to the input and output multiplexers IMUX and OMUX. For synchronous random access and synchronous burst operations, the least significant bits of the count in the column address counter **52** are applied directly to control the input and output multiplexers.

For synchronous wrap operations, the wrap address scrambler **73** and the multiplexer **74** convert the least significant bits of the column address to the desired sequence of addresses for reading bits from the input and output multiplexers IMUX and OMUX. The wrap length signal WL is active all of the time except for a four bit wrap length. Then the wrap length signal WL cuts off the signal on the lead **76** so that the two leads **77** and **78** apply address bits from the column address counter and the multiplexer **74** applies a zero to the input and output multiplexers IMUX and OMUX. The wrap address scrambler produces the desired sequences of bits on the leads **77** and **78**, in accordance with TABLES I and II.

In FIG. **2**, the mask register **93** receives and stores coded mask data from the data bus **25**. Responsive to the system clock signal CLK, the mask register **93** applies the mask data to control the operation of the count control circuit **94**.

Count control circuit **94**, in response to the status of the burst control signal BURST, the wrap control signal WRAP, the mask data, and the system clock CLK, produces the clock signal COUNT for controlling the operation of the column address counter **52** and the wrap address scrambler and multiplexer **61**.

Timing and control circuit **42** of FIG. **2** is responsive to the row address control signal $\overline{RE}$, the column address control signal $\overline{CE}$, the write signal $\overline{WE}$, the burst signal $\overline{BT}$, the burst direction signal +/−, the wrap select signal $\overline{WP}$, the wrap-type signal WT, the wrap-length signal WL, and the system clock signal CLK for producing control signals, such as, the row and column address latching signals XAL and YAL, the latch initial address signal LIA, the write enable signal WEN, the data-in latch signal DINL, the burst control signal BURST, and the wrap control signal WRAP.

In the timing and control circuit **42** of FIG. **2**, all of the signals from the control bus **60** are gated by the system clock signal CLK on lead **67** so that all control signals internal to the synchronous random access memory **30**, such as, the signals XAL, YAL, LIA, WEN, DINL, BURST and WRAP are synchronized with the system clock signal CLK. This feature assures that the functions of the synchronous random access are synchronized with that clock. Any logic circuitry external to the synchronous random access memory **30** need not be concerned with any complex timing relationships between the various signals transmitted on the control bus **60**.

Referring now to FIG. **19**, there is shown an exemplary gate **101** of the timing and control circuit **42** of FIG. **2**. In FIG. **19**, the row address control signal $\overline{RE}$ is gated by the system clock signal CLK, i.e., sampled on the negative-going edge of the pulses of the system clock CLK. The resulting output of the gate **101** is the row address latch signal XAL.

FIG. **20** is a timing diagram for the operation of the gate **101**. As shown in FIG. **20**, the output row address latch signal XAL is activated by the negative-going edge of the system clock CLK at the system clock cycle time **2** when the row address control signal $\overline{RE}$ is low. The timing of the negative-going edge of the row address control signal $\overline{RE}$ is irrelevant, as long as the level of that signal is low at the negative-going edge of the system clock signal CLK.

Similarly, all of the other internal control signals are responsive to sampled levels of the external control signals on the control bus **60** at times of the negative-going edges of the system clock signal CLK.

Referring now to FIG. **21**, there is shown an exemplary circuit **102** which is responsive to the burst control signal BURST, the wrap control signal WRAP, and the system clock signal within the count control block **94** of FIG. **2** CLK, for producing the count clock signal COUNT. In FIG. **21**, the active high signals BURST and WRAP are applied as inputs to an OR gate **103** to produce a signal COUNT ENABLE for gating the system clock signal. A gate **104** is enabled for transmitting the system clock signal CLK when either the burst control signal BURST or the wrap control signal WRAP is active high.

The timing and control circuit 42 of FIG. 2 produces the burst control signal BURST and wrap control signal WRAP. The burst control signal BURST and the wrap control signal WRAP are normally low and go high active. The initial edges of the burst control signal BURST and the wrap control signal WRAP are aligned with negative-going edges of the system clock signal CLK. Once the burst control signal BURST and the wrap control signal WRAP are activated, they remain active for the duration of their respective operations.

The count clock signal COUNT is a clock pulse sequence synchronized with the system clock CLK and lasting while either the signal BURST or the signal WRAP is active. Pulses of the count clock signal COUNT either increment or decrement the column address residing in the column address counter 52 depending upon the state of the burst direction signal +/−.

Referring now to FIG. 22, the timing diagram shows an exemplary operation of the count signal gate arrangement 102 of FIG. 21. The internal control signal COUNT ENABLE goes high active before the system clock cycle time 2 and stays high active until after the system clock cycle time 3. As a result of gating the system clock signal CLK through the gate 104 of FIG. 21 under control of the control signal COUNT ENABLE, the resulting count clock signal COUNT is gated to produce pulses at cycle times 2 and 3 in synchronism with the system clock signal CLK.

Referring now to FIG. 23, there is shown a block diagram of the output multiplexer OMUX and the input multiplexer IMUX arranged with selection and gating circuits for controlling transfer of data bits read out from the memory array 75 to the data bus 25 and for controlling transfer of data bits to be written from the data bus 25 to the memory array 75.

With respect to FIG. 23, the column address decoder 54 of FIG. 2 selects two blocks of four columns by enabling two gates in block gating circuit 110. Each lead into and out of the block gating circuit represents four leads for a block of data. Every other block of data, i.e., the even order blocks, is connected by way of an even order bus 116 to an output enable gate 120, which includes a separate gate for each bit lead and is operated by the complement of the write enable signal WEN. Odd order blocks from the memory array 75 are connected by way of an odd order bus 122 also to the output enable gate 120. The output enable gate 120 is connected to eight separate output registers 124 for storing individual data bits read out from the memory array 75.

In FIG. 23, converter circuit 126 converts the three least significant bits of the column address from the wrap address scrambler and multiplexer 61 into a one-out-of-eight selection code, which is applied to an output transfer selection gate circuit 128. For each of the eight output registers 124, there is an output transfer selection gate controlled by a separate one of the one-out-of-eight selection code, which is applied to control the output transfer selection gate circuit 128. The output transfer selection gates 128 are operated one at a time to allow a data bit to be transmitted from its output register to the data bus 25 in synchronism with the system clock.

Continuing to refer to FIG. 23, for burst read-up operation of the input and output multiplexers, the column address in the column address counter 52 of FIG. 2 is incremented in response to the clock signal COUNT. Every fourth cycle of the clock signal COUNT, the two column address decoder output signals step up one order of sets, e.g., from n and n+1 to n+1 and n+2. This disables one of two previously open gates and enables one previously open gate and a new gate 110. Data bits stored in four of the output registers 124 thereby are changed to a new block of data to be read out to the data bus 25. Thus, the set of four of the output registers 124 exhausted of data is replenished with new data because the next higher order set of column addresses from the memory array 75 is enabled to transfer data into the exhausted output registers 124.

With respect to FIG. 23 for a burst read-down operation, the output multiplexer OMUX operates, as just described, except that the order of addresses applied to the column address decoder 54 is decrementing. Thus every fourth cycle of the clock signal COUNT, the two enabled blocks of data are the two next lower order blocks of data, e.g., from column sets n and n−1 to n−1 and n−2.

Further with respect to FIG. 23 for a wrap read operation, the output multiplexer OMUX operates similar to the previously described burst read-up operation until the initial address selection is completed. Eight data bits are read out of the memory array and are latched into the eight output register circuits 124. Thereafter their order of readout to the data bus 25 is determined by two factors. The first and second factors are the wrap length signal WL and the wrap type signal WT. As previously mentioned, combinations of those two signals WL and WT cause the wrap address scrambler 73 of FIG. 6 to produce a series of enabling signal codes for the output gates 128 of the output multiplexer OMUX. In response to that series of enabling signal codes, corresponding bits from the output registers 124 are read out through the output transfer selection gates 128 in the selected order onto the data bus 25.

In FIG. 23, a somewhat similar arrangement is provided in the input multiplexer IMUX for writing data from the data bus 25 into the memory array 75. Input transfer selection gates 130 are selectively enabled by the one-out-of-eight code from the wrap address scrambler and multiplexer 61. The bits are stored in separate input register circuits 132. The stored data bits are transferred in blocks of four bits to even and odd order blocks of columns of the memory array 75 as the upper count portion of the column address is either incremented or decremented in response to the clock signal COUNT.

Referring now to FIG. 24, there is shown a data processing system 215 including a digital processor 220, which is similar to the data processing system 15 of FIG. 1 except that the system clock 65 produces a clock signal that is applied over a lead 221 to the digital processor 220. Within the digital processor 220, the clock signal is gated or otherwise manipulated into a processor clock signal that is applied by way of a lead 222 to the synchronous memory 30, the input peripheral device 24, and the output peripheral device 40. Otherwise the data processing system 215 operates like the data processing system 15 which was described with respect to FIGS. 1 and 2.

The foregoing describes some data processing system arrangements which represent illustrative embodiments of the invention. Those embodiments and others made obvious in view thereof are considered to fall within the scope of the appended claims.

What is claimed is:

1. A synchronous random access memory comprising:

a timing and control circuit for receiving a system dock signal and producing a first address control signal, the system clock signal having a sequence of clock cycles, each clock cycle having positive-going and negative-going edges;

an addressing circuit for latching the first address signal, responsive to the first address control signal and the system clock signal; and

an output circuit for producing a predetermined number of data bits from the storage cells, wherein the output circuit produces a first data bit, responsive to the positive-going edge of the system clock signal, and a second data bit, responsive to the negative-going edge of the system clock signal.

2. A synchronous random access memory as in claim **1**, wherein the storage cells are dynamic storage cells.

3. A synchronous random access memory, as in claim **2**, wherein the predetermined number of data bits is 4.

4. A synchronous random access memory, as in claim **2**, wherein the predetermined number of data bits is 8.

5. A synchronous random access memory as in claim **2**, wherein the addressing circuit further comprises:

a row decoding circuit for selecting a row of storage cells, responsive to the first address signal;

an address counter circuit for receiving a second address signal, the address counter circuit producing an output address signal, responsive to the system clock signal; and

a column decoding circuit for selecting a column of storage cells from the row of storage cells, responsive to the output address signal.

6. A synchronous random access memory as in claim **5**, wherein the addressing circuit latches the second address signal, responsive to a second address control signal and the system clock signal.

7. A synchronous random access memory as in claim **6**, wherein the output circuit farther comprises a multiplex circuit coupled to receive the first data bit and the second data bit, the multiplex circuit producing the first data bit, responsive to the positive-going edge of the system clock signal, and the second data bit, responsive to the negative-going edge of the system clock signal, at a data terminal.

8. A synchronous random access memory as in claim **6**, wherein the timing and control circuit further determines an order of the predetermined number of data bits in response to a data control signal.

9. A synchronous random access memory as in claim **8**, wherein the order of the predetermined number of data bits is by sequential column address.

10. A synchronous random access memory as in claim **8**, wherein the order of the predetermined number of data bits is by interleaved wrap sequence.

11. A data processing system as in claim **8**, wherein the first address control signal is produced in response to a row enable signal, and the second address control signal is produced in response to a column enable signal.

12. A synchronous random access memory as in claim **8**, wherein the output circuit produces two data bits from the predetermined number of data bits at a data terminal for each clock cycle of the sequence of clock cycles.

13. A synchronous random access memory as in claim **1**, wherein the first address signal includes a first and a second group of address bits.

14. A synchronous random access memory as in claim **13**, wherein the addressing circuit further comprises:

a row decoding circuit for selecting a row of storage cells, responsive to the first group of address bits;

an address counter circuit for receiving the second group of address bits, the address counter circuit producing an output address signal, responsive to the system clock signal; and

a column decoding circuit for selecting a column of storage cells from the row of storage cells, responsive to the output address signal.

15. A synchronous random access memory as in claim **14**, wherein the address counter circuit produces the output address signal by incrementing the second group of address bits.

16. A synchronous random access memory, as in claim **14**, wherein the predetermined number of data bits is 4.

17. A synchronous random access memory, as in claim **14**, wherein the predetermined number of data bits is 8.

18. A synchronous random access memory as in claim **14**, wherein the timing and control circuit further determines an order of the predetermined number of data bits in response to a data control signal.

19. A synchronous random access memory as in claim **18**, wherein the order of the predetermined number of data bits is by sequential column address.

20. A synchronous random access memory as in claim **18**, wherein the order of the predetermined number of data bits is by interleaved wrap sequence.

21. A synchronous random access memory as in claim **18**, wherein the output circuit further comprises a multiplex circuit coupled to receive the first data bit and the second data bit, the multiplex circuit producing the first data bit, responsive to the positive-going edge of the system clock signal, and the second data bit, responsive to the negative-going edge of the system dock signal, at a data terminal.

22. A synchronous random access memory as in claim **18**, wherein the storage cells are static storage cells.

23. A synchronous random access memory comprising:

a timing and control circuit for receiving a system clock signal and producing a first address control signal, the system clock signal having a sequence of dock cycles, each clock cycle having positive-going and negative-going edges;

an addressing circuit for latching the first address signal, responsive to the first address control signal and the system clock signal; and

an output circuit for producing a plurality of data bits from the storage cells, the data bits having an order wherein the output circuit produces a first data bit, responsive to the positive-going edge of the system clock signal, and a second data bit, responsive to the negative-going edge of the system dock signal.

24. A synchronous random access memory as in claim **23**, wherein the storage cells are dynamic storage cells.

25. A synchronous random access memory as in claim **24**, wherein the order of the plurality of data bits is by sequential column address.

26. A synchronous random access memory as in claim **24**, wherein the order of the plurality of data bits is by interleaved wrap sequence.

27. A synchronous random access memory as in claim **24**, wherein the addressing circuit further comprises:

a row decoding circuit for selecting a row of storage cells, responsive to the first address signal;

an address counter circuit for receiving a second address signal, the address counter circuit producing an output address signal, responsive to the system dock signal; and

a column decoding circuit for selecting a column of storage cells from the row of storage cells, responsive to the output address signal.

28. A synchronous random access memory as in claim **27**, wherein the addressing circuit latches the second address signal, responsive to a second address control signal and the system clock signal.

29. A synchronous random access memory as in claim **28**, wherein the output circuit further comprises a multiplex

circuit coupled to receive the first data bit and the second data bit, the multiplex circuit producing the first data bit, responsive to the positive-going edge of the system clock signal, and the second data bit, responsive to the negative-going edge of the system clock signal at a data terminal.

30. A synchronous random access memory as in claim **28**, wherein the first address control signal is produced in response to a row enable signal and the system clock signal, and the second address control signal is produced in response to a column enable signal and the system clock signal.

31. A synchronous random access memory as in claim **28**, wherein the output circuit produces two data bits from the plurality of data bits at a data terminal for each clock cycle of the sequence of clock cycles.

32. A synchronous random access memory as in claim **23**, wherein the first address signal includes a first and a second group of address bits.

33. A synchronous random access memory as in claim **32**, wherein the addressing circuit further comprises:

- a row decoding circuit for selecting a row of storage cells, responsive to the first group of address bits;
- an address counter circuit for receiving the second group of address bits, the address counter circuit producing an output address signal, responsive to the system clock signal; and
- a column decoding circuit for selecting a column of storage cells from the row of storage cells, responsive to the output address signal.

34. A synchronous random access memory as in claim **33**, wherein the address counter circuit produces the output address signal by incrementing the second group of address bits.

35. A synchronous random access memory as in claim **33**, wherein the order of the plurality of data bits is by sequential column address.

36. A synchronous random access memory as in claim **33**, wherein the order of the plurality of data bits is by interleaved wrap sequence.

37. A synchronous random access memory as in claim **33**, wherein the output circuit further comprises a multiplex circuit coupled to receive the first data bit and the second data bit, the multiplex circuit producing the first data bit, responsive to the positive-going edge of the system clock signal, and the second data bit, responsive to the negative-going edge of the system dock signal at a data terminal.

38. A synchronous random access memory as in claim **33**, wherein the storage cells are static storage cells.

39. A synchronous dynamic random access memory comprising:

- an array of dynamic storage cells arranged in rows and columns;
- a timing and control circuit for receiving a system clock signal having a plurality of periodic clock cycles, each periodic clock cycle having a positive-going edge and a negative-going edge, the timing and control circuit producing a first address control signal, responsive to a first clock cycle of the plurality of periodic clock cycles, and a second address control signal, responsive to a second clock cycle of the plurality of periodic clock cycles;
- a row address circuit for receiving a first address signal for accessing a row of dynamic storage cells, responsive to the first address control signal and the first clock cycle;
- a column address circuit for receiving a second address signal for accessing at least one column of dynamic storage cells, responsive to the second address control signal and the second clock cycle; and
- an output circuit for producing a plurality of data bits from the storage cells, wherein the output circuit produces a first data bit, responsive to the positive-going edge of the system clock signal, and a second data bit, responsive to the negative-going edge of the system clock signal.

40. A synchronous dynamic random access memory as in claim **39**, wherein the column addressing circuit further comprises:

- an address counter circuit for receiving the second address signal, the address counter circuit producing an output address signal, responsive to the system dock signal; and
- a column decoding circuit for selecting the column of storage cells from the row of storage cells, responsive to the output address signal.

41. A synchronous dynamic random access memory as in claim **40**, wherein the address counter circuit produces the output address signal by incrementing the second address signal, responsive to the system dock signal.

42. A synchronous dynamic random access memory as in claim **40**, wherein the column address circuit latches the second address signal, responsive to the second address control signal.

43. A synchronous dynamic random access memory as in claim **40**, wherein the timing and control circuit further produces a first data control signal for selecting a predetermined number of the plurality of data bits.

44. A synchronous dynamic random access memory, as in claim **43**, wherein the predetermined number of the plurality of data bits is 4.

45. A synchronous dynamic random access memory, as in claim **43**, wherein the predetermined number of the plurality of data bits is 8.

46. A synchronous dynamic random access memory as in claim **43**, wherein the timing and control circuit further produces a second data control signal for selecting an order of the plurality of data bits.

47. A synchronous dynamic random access memory as in claim **46**, wherein the order of the predetermined number of data bits is by sequential column address.

48. A synchronous dynamic random access memory as in claim **46**, wherein the order of the predetermined number of data bits is by interleaved wrap sequence.

49. A synchronous dynamic random access memory as in claim **46**, wherein the output circuit further comprises a multiplex circuit coupled to receive the first data bit and the second data bit, the multiplex circuit producing the first data bit, responsive to the positive-going edge of the system clock signal, and the second data bit, responsive to the negative-going edge of the system clock signal at a data terminal.

50. A synchronous dynamic random access memory as in claim **39**, wherein the column addressing circuit further comprises:

- an address counter circuit for receiving a third address signal, the address counter circuit producing an output address signal, responsive to the system clock signal;
- a first column decode circuit for selecting the at least one column of dynamic storage cells, responsive to the second address signal and one clock cycle of the periodic clock cycles, for producing the plurality of data bits; and
- a second column decode circuit for sequentially producing the plurality of data bits, responsive to the output address signal.

51. A synchronous dynamic random access memory as in claim 50, wherein the address counter circuit produces the output address signal by incrementing the third address signal, responsive to the system clock signal.

52. A synchronous dynamic random access memory as in claim 50, wherein the column address circuit latches the second address signal, responsive to the second address control signal.

53. A synchronous dynamic random access memory as in claim 50, wherein the timing and control circuit further produces a first data control signal for selecting a predetermined number of the plurality of data bits.

54. A synchronous dynamic random access memory, as in claim 53, wherein the predetermined number of the plurality of data bits is 4.

55. A synchronous dynamic random access memory, as in claim 53, wherein the predetermined number of the plurality of data bits is 8.

56. A synchronous dynamic random access memory as in claim 53, wherein the timing and control circuit further produces a second data control signal for selecting an order of the plurality of data bits.

57. A synchronous dynamic random access memory as in claim 56, wherein the order of the predetermined number of data bits is by sequential column address.

58. A synchronous dynamic random access memory as in claim 56, wherein the order of the predetermined number of data bits is by interleaved wrap sequence.

59. A synchronous dynamic random access memory as in claim 56, wherein the output circuit further comprises a multiplex circuit coupled to receive the first data bit and the second data bit, the multiplex circuit producing the first data bit, responsive to the positive-going edge of the system clock signal, and the second data bit, responsive to the negative-going edge of the system clock signal at a data terminal.

* * * * *

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United States Patent [19]

Toda et al.

[11] **Patent Number: 5,986,968**

[45] **Date of Patent: Nov. 16, 1999**

[54] **CLOCK-SYNCHRONOUS SEMICONDUCTOR MEMORY DEVICE AND ACCESS METHOD THEREOF**

[75] Inventors: **Haruki Toda**; **Hitoshi Kuyama**, both of Kanagawa-ken, Japan

[73] Assignee: **Kabushiki Kaisha Toshiba**, Kawasaki, Japan

[21] Appl. No.: **09/113,570**

[22] Filed: **Jul. 10, 1998**

Related U.S. Application Data

[62] Division of application No. 08/457,165, Jun. 1, 1995, Pat. No. 5,818,793, which is a continuation of application No. 08/031,831, Mar. 16, 1993, abandoned.

[30] **Foreign Application Priority Data**

Mar. 19, 1992 [JP] Japan 4-063844

[51] **Int. Cl.**[6] **G11C 7/00**

[52] **U.S. Cl.** **365/233**; 365/189.05; 365/189.12; 365/194; 365/225.7; 365/236; 365/240

[58] **Field of Search** 365/233, 194, 365/225.7, 236, 189.12, 240, 189.05, 230.08

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Primary Examiner—Do Hyun Yoo
Attorney, Agent, or Firm—Foley & Lardner

[57] **ABSTRACT**

A clock-synchronous semiconductor memory device includes many memory cells arranged in matrix, a count section for counting the actual number of cycles of a continuous, externally-supplied basic clock signal, a control section for inputting a row enable control signal (/RE) and the column enable control signal (/CE) provided from an external device, other than the basic clock signal, for which the control signals are at a specified level, synchronized with the basic control signal, and for setting the initial address for data access of the memory cells, and a data I/O section for executing a data access operation for the address set by the control section. In the device, the output of data from the memory cells through the data I/O section is started after the setting of the initial address by the control sections and after a specified number of basic clock signals has been counted by the count section.

46 Claims, 8 Drawing Sheets

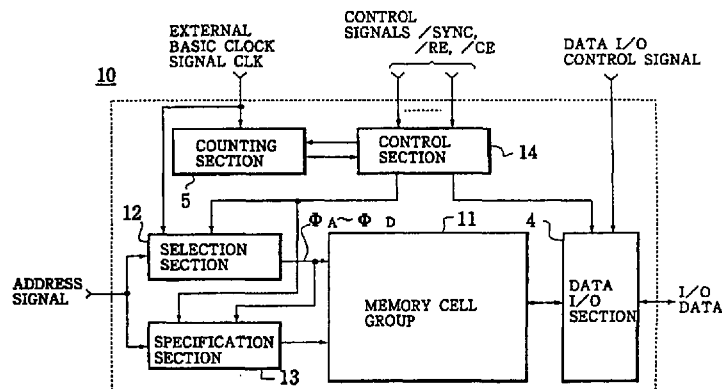

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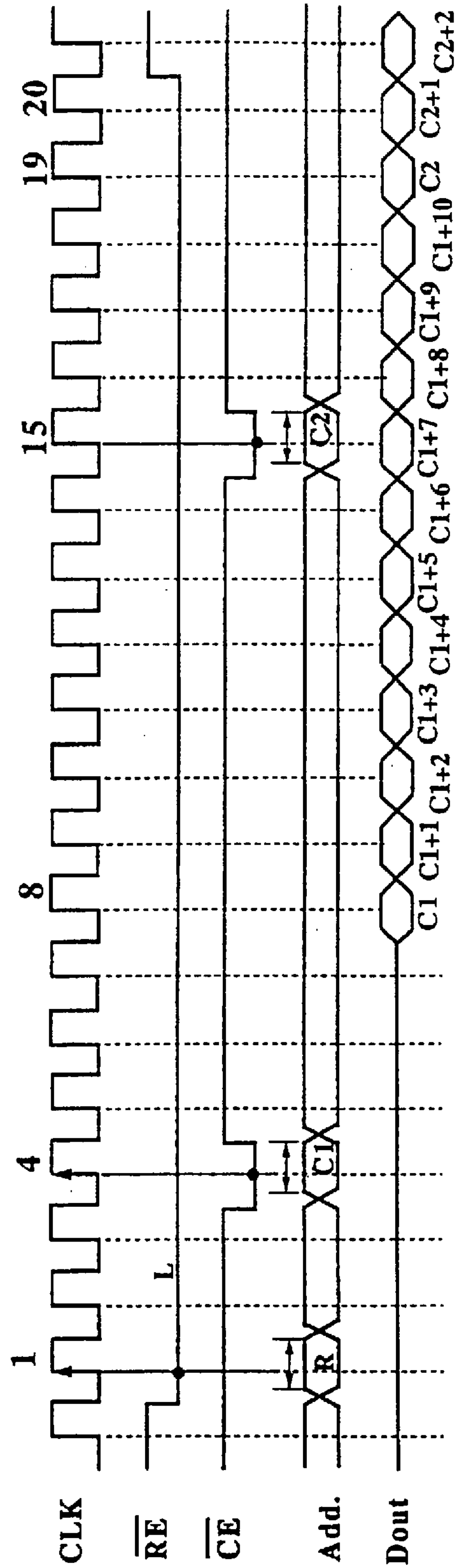
FIG.1



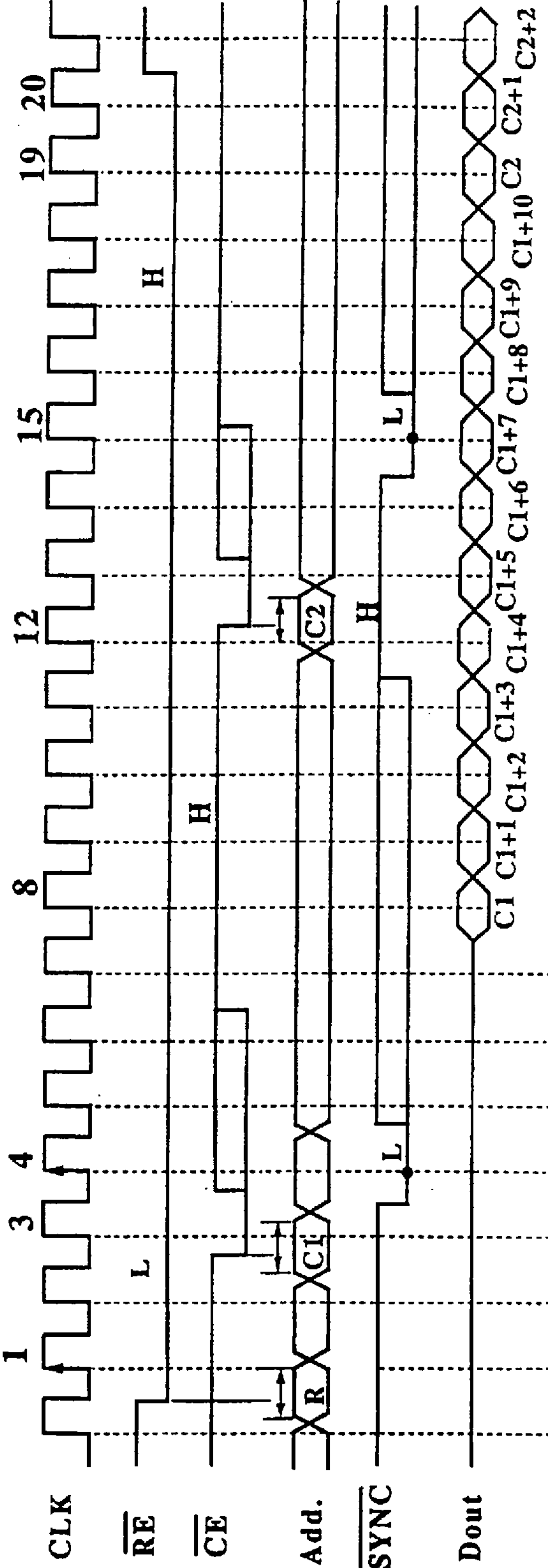


FIG.2
CLK
RE
CE
Add.
SYNC
Dout
1
3
4
8
12
15
19
20
L
H
H
L
H
L
R
C1
C2
C1
C1+1
C1+2
C1+3
C1+4
C1+5
C1+6
C1+7
C1+8
C1+9
C1+10
C2
C2+1
C2+2

FIG.3

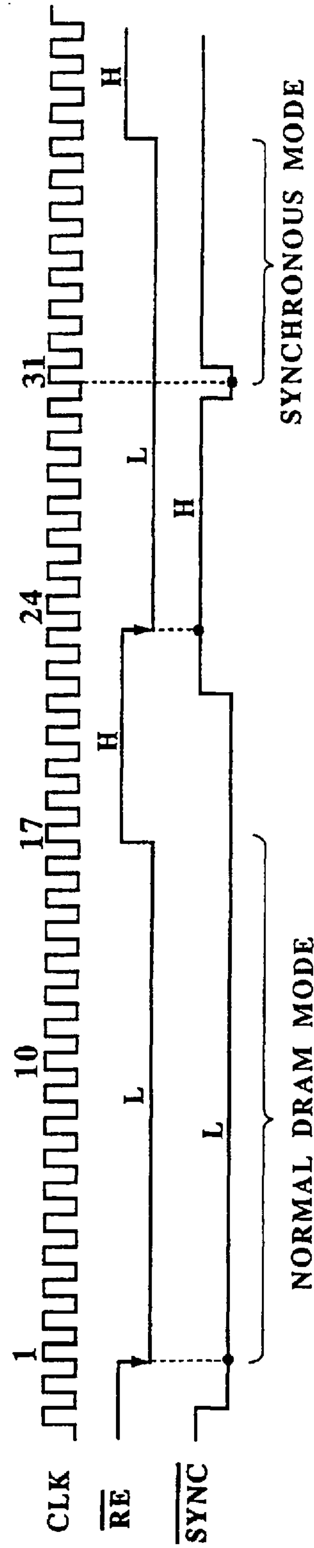
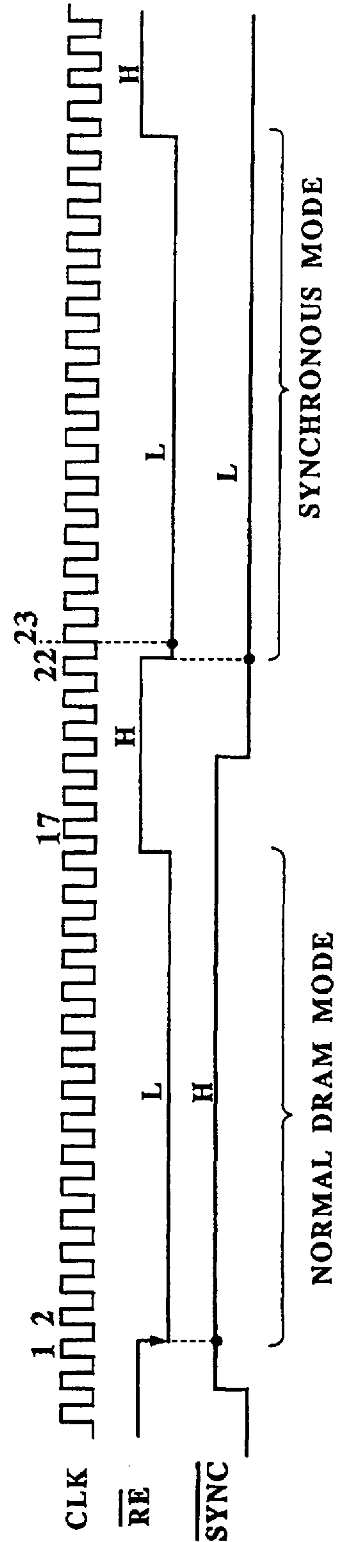


FIG.4



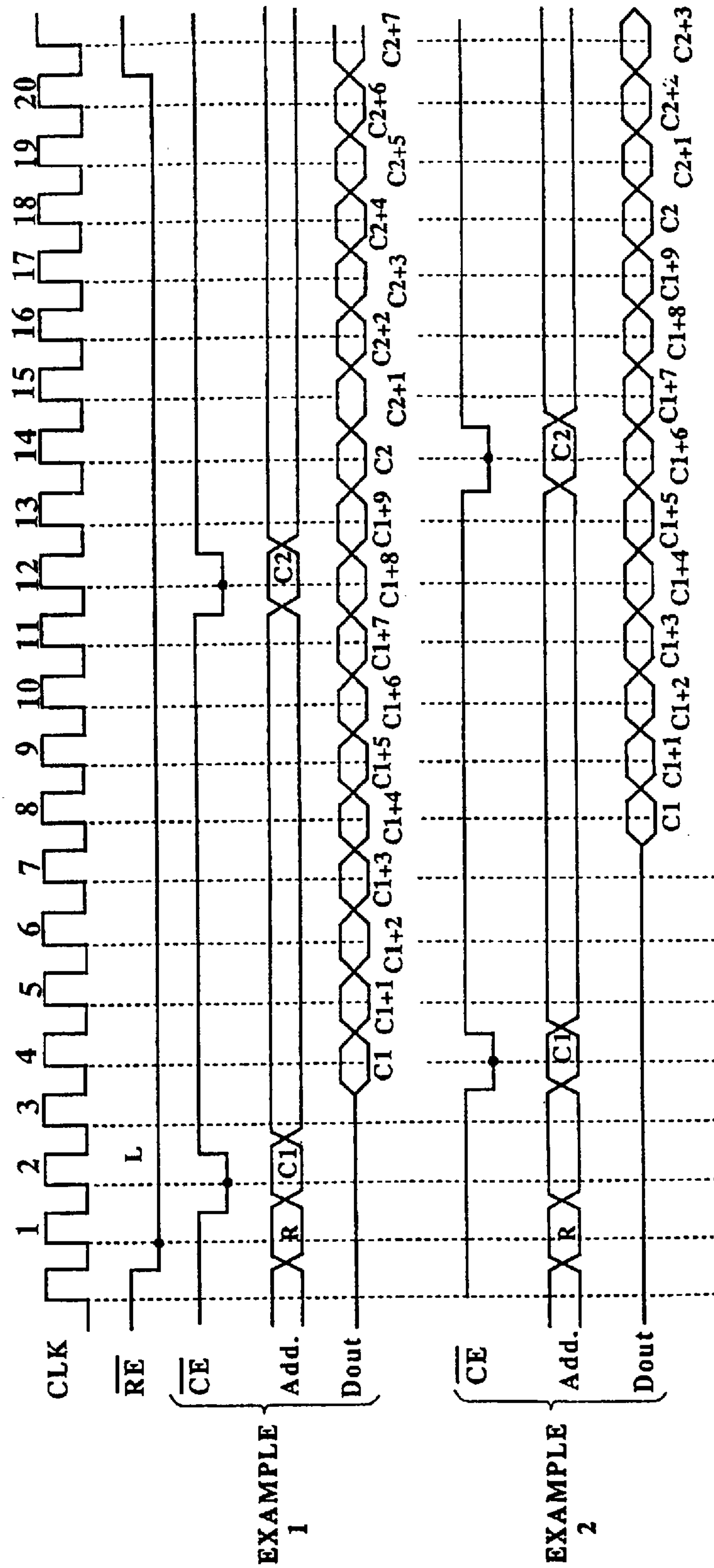


FIG.5
CLK
RE
CE
Add.
Dout
EXAMPLE 1
EXAMPLE 2
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
L
R
C1
C2
C1 C1+1 C1+2 C1+3 C1+4 C1+5 C1+6 C1+7 C1+8 C1+9 C2 C2+1 C2+2 C2+3 C2+4 C2+5 C2+6 C2+7
C1 C1+1 C1+2 C1+3 C1+4 C1+5 C1+6 C1+7 C1+8 C1+9 C2 C2+1 C2+3

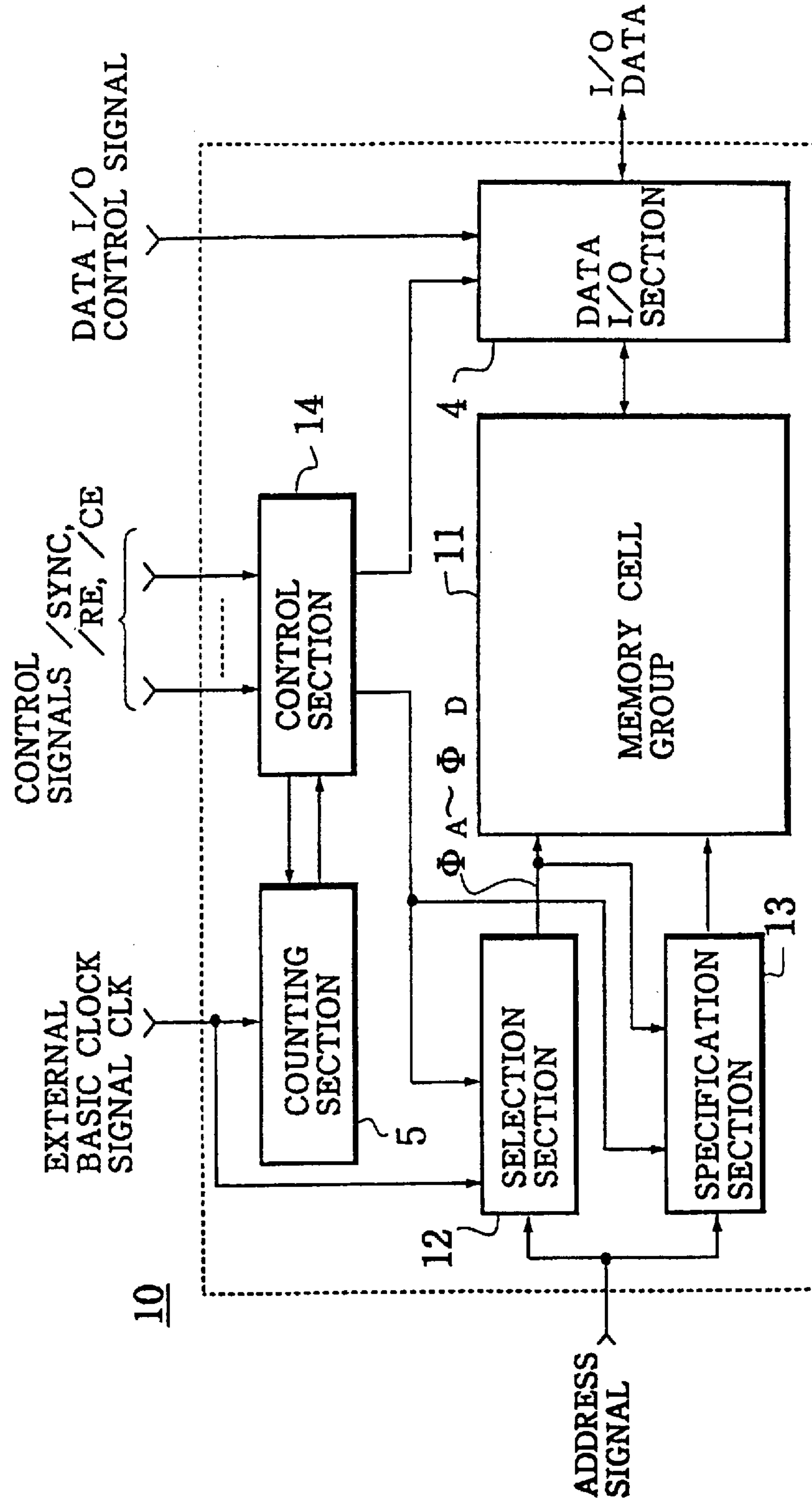


FIG.6

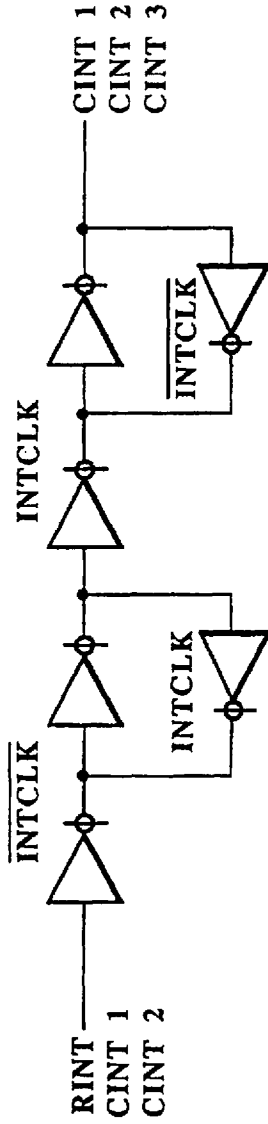


FIG.7

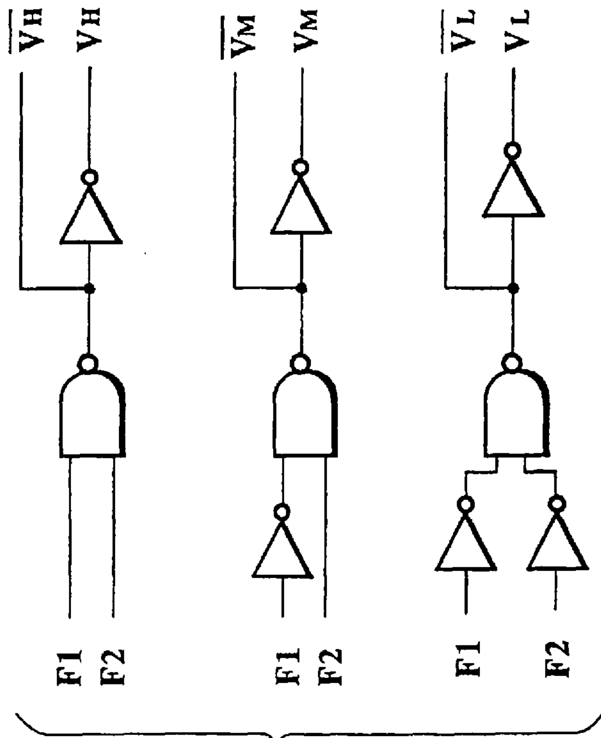


FIG.10

FIG.8

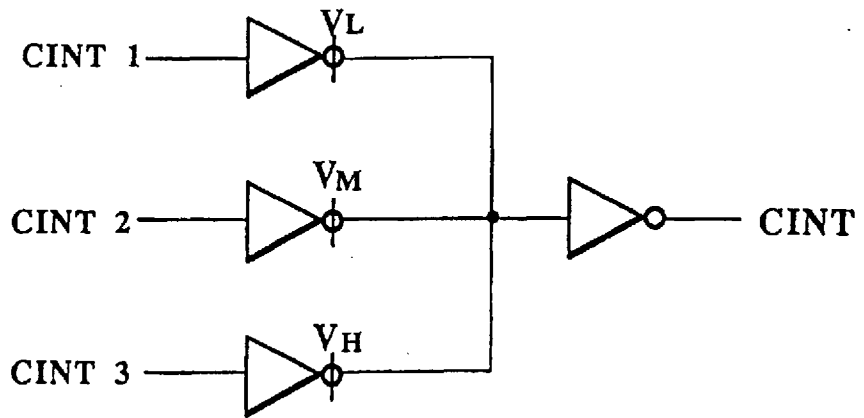
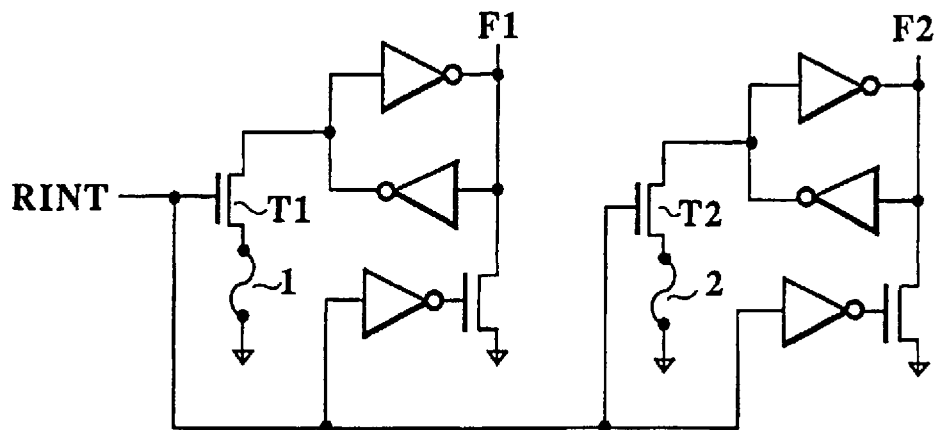


FIG.9



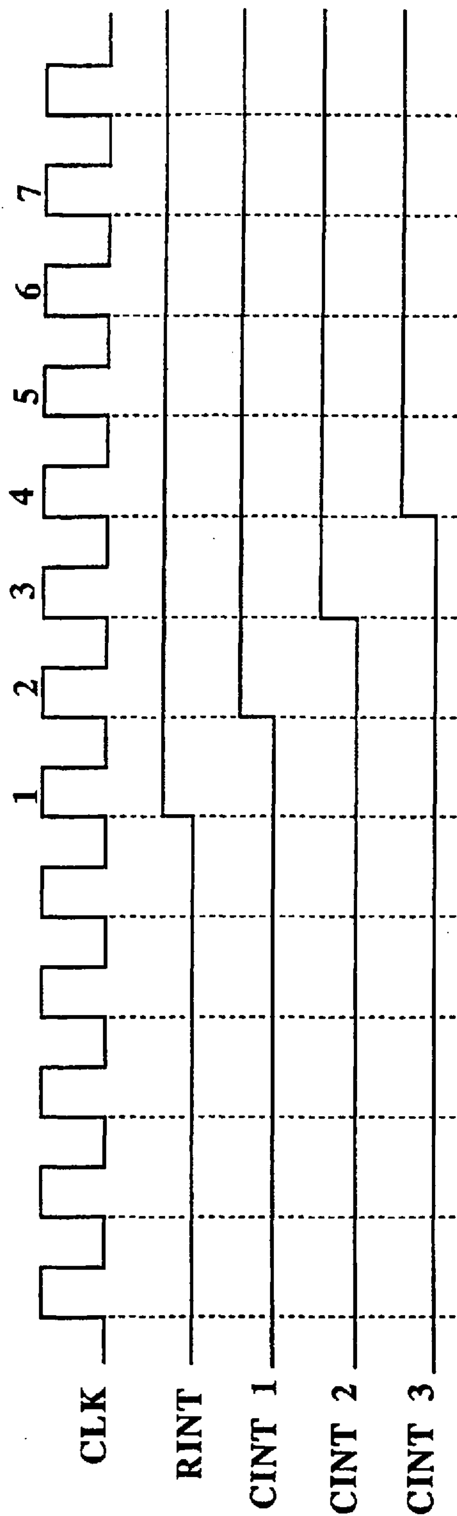


FIG.11

CLOCK-SYNCHRONOUS SEMICONDUCTOR MEMORY DEVICE AND ACCESS METHOD THEREOF

This application is a divisional of application Ser. No. 08/457,165, filed Jun. 1, 1995, now U.S. Pat. No. 5,818,793, which is a continuation of Ser. No. 08/031,831 filed Mar. 16, 1993, now abandoned.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a clock-synchronous semiconductor memory device and access method thereof which operates synchronously with a basic clock signal, and, in particular, to a clock-synchronous semiconductor memory device and access method thereof in which an address for accessing can be set synchronously with a basic clock signal, and a clock-synchronous semiconductor memory device and access method thereof in which an address for accessing can be set when a high-frequency basic clock signal is used.

2. Description of the Prior Art

The inventors of the present invention have previously proposed a basic method for controlling a memory operation for a semiconductor memory device synchronized with a basic clock signal (Japan Application No. 3-255354).

At that time, several methods were illustrated for controlling a memory access by means of an external control signal, but nothing was disclosed as to how to set a external control signals synchronously with a basic clock signal and with respect to setting specific timing for an address signal or the like for the external control signals.

Moreover, there is a problem that it is difficult to access data when a high-frequency basic clock signal is used in a conventional a clock-synchronous semiconductor memory device and access method thereof.

SUMMARY OF THE INVENTION

An object of the present invention, with due consideration to the drawbacks of such conventional semiconductor memory device and method thereof, is to provide a clock-synchronous semiconductor memory device and access method thereof in which an address for accessing can be set by external control signals synchronously with an external basic clock signal.

A further object of the present invention is to provide a clock-synchronous semiconductor memory device and a method thereof for access of a clock-synchronous semiconductor memory device wherein an address for access is easily set for the cases where the basic system cycle is short and where the basic system cycle is long.

A further object of the present invention is to provide a clock-synchronous semiconductor memory device which is capable of switching internal operation to conform to the length of the basic incorporated system cycle.

In accordance with one preferred embodiment, there is a method for accessing a clock-synchronous semiconductor memory device, used for access of data, synchronized with a continuous, external clock signal, comprising the steps of:

setting an initial address for data access of the clock-synchronous semiconductor memory device from the cycle of the clock signal for which a control signal from at least more than one type of clock signal, other than the clock signal, supplied to the semiconductor memory device is maintained at a specified level;

counting output of data from the set initial address after the initial address is set; and

starting from a specified cycle in the cycles of the clock signal.

In accordance with another preferred embodiment, there is a method for accessing a clock-synchronous semiconductor memory device used for access of data, synchronized with a continuous, external clock signal, comprising the steps of:

setting an initial address for data access of the clock-synchronous semiconductor memory device from conditions under which a first control signal from at least more than one type of clock signal, other than the clock signal, supplied to the semiconductor memory device is maintained at a specified level; and

starting the output of data from the set initial address from a specified cycle number of the clock signal, counting from after a second control signal supplied to the semiconductor memory device has been maintained at a specified level.

In accordance with another preferred embodiment, there is a method for accessing a clock-synchronous semiconductor memory device by which access of data is possible, synchronized with a continuous, external clock signal, comprising the steps of:

setting an initial address for data access of the clock-synchronous semiconductor memory device from conditions under which a first control signal from at least more than one type of clock signal, other than the clock signal, supplied to the semiconductor memory device is maintained at a specified level; and

selecting the output of data from the set initial address by either one of two types ((A) or (B)) of access methods by means of external control provided to the semiconductor memory device prior to setting the initial address for the data access by means of the first control signal;

wherein: (A) is an access method by which the output of data from the set initial address is started immediately after the setting of the initial address; and

(B) is an access method by which the output of data from the set initial address is synchronized with a clock signal and is started from a specified cycle number of clock signals, counting after a second control signal supplied to the semiconductor memory device has been maintained at a specified level.

In accordance with another preferred embodiment, there is a method for accessing a clock-synchronous semiconductor memory device with which access of data is possible, synchronized with a continuous, external clock signal, comprising the steps of:

setting an initial address for data access of the clock-synchronous semiconductor memory device from conditions under which a first control signal from at least more than one type of clock signal, other than the clock signal, supplied to the semiconductor memory device is maintained at a specified level; and

selecting the output of data from the set initial address by either one of two types ((A) or (B)) of access methods by means of external control provided to the semiconductor memory device prior to setting the initial address for the data access by means of the first control signal;

wherein: (A) is an access method by which the output of data from the set initial address is started directly after the setting of the initial address; and

(B) is an access method by which the output of data from the set initial address is synchronized with a clock signal and

is started from a specified cycle number of clock signals, counting after the initial address has been set.

In accordance with another preferred embodiment, there is a clock-synchronous semiconductor memory device comprising:

memory means comprising a plurality of memory cells arranged in rows and columns;

count means for counting the actual number of cycles of a continuous, externally-supplied basic clock signal;

control means for inputting at least more than one type of externally-supplied control signal other than the basic clock signal, for which the control signal is at a specified level, synchronized with the basic control signal, and for setting the initial address for data access of the memory means; and

data input/output means for executing a data access operation for the address set by the control means;

wherein: the output of data from the memory means through the data input/output means is started after the setting of the initial address by the control means, and after a specified number of basic clock signals has been counted by the count means.

In accordance with another preferred embodiment, there is a clock-synchronous semiconductor memory device comprising:

memory means comprising a plurality of memory cells arranged in rows and columns;

count means for counting the actual number of cycles of a continuous, externally-supplied basic clock signal;

control means for inputting at least more than one type of externally-supplied control signal, other than the basic clock signal, for which a first control signal is at a specified level, and for setting the initial address for data access of the memory means; and

data input/output means for executing a data access operation for the address set by the control means;

wherein: the output of data from the memory means through the data input/output means is started after the setting of a second control signal of the externally-provided control signals, and after a specified number of basic clock signals has been counted by the count means.

In accordance with another preferred embodiment, there is a clock-synchronous semiconductor memory device comprising:

memory means comprising a plurality of memory cells arranged in rows and columns;

count means for counting the actual number of cycles of a continuous, externally-supplied basic clock signal;

control means for inputting at least more than one type of externally-supplied control signal, other than the basic clock signal, for which a first control signal from among the control signals is at a specified level, and for setting the initial address for data access of the memory means;

data input/output means for executing a data access operation for the address set by the control means; and

selection means for selecting either of the following two operations (A) or (B) from a second control signal level in the control signals;

wherein: in the operation (A), the output of data from the memory means through the data input/output means is started immediately after the setting of the initial address by the control means; and

in the operation (B), the output of data from the memory means through the data input/output means is started after the setting of the initial address by the control means, and after a specified number of basic clock signals has been counted by the count means.

In accordance with another preferred embodiment, there is a clock-synchronous semiconductor memory device comprising:

memory means comprising a plurality of memory cells arranged in rows and columns;

calculation means for counting the actual number of cycles of a continuous, externally-supplied basic clock signal;

control means for inputting at least more than one type of externally-supplied control signal other than the basic clock signal, for which a first control signal from among the control signals is at a specified level, and for setting the initial address for data access of the memory means;

data input/output means for executing a data access operation for the address set by the control means; and

selection means for selecting either of the following two operations (A) or (B) from a second control signal level in the control signals;

wherein: in the operation (A), the output of data from the memory means by the data input/output means is started immediately after the setting of the initial address by the control means; and

in the operation (B), the output of data from the memory means by the data input/output means is started after the setting of the initial address by the control means, after the second control signal has reached a specified level; and after a specified number of basic clock signals has been counted by the count means.

These and other objects, features, and advantages of the present invention will become more apparent from the following description of the preferred embodiment taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an external signal waveform diagram showing a clock-synchronous operation of a clock-synchronous semiconductor memory device relating to an access method according to the first embodiment of the present invention.

FIG. **2** is an external signal waveform diagram for an address-incorporated nonsynchronous-type of clock-synchronous method for a clock-synchronous semiconductor memory device relating to an access method which is another embodiment of the present invention.

FIG. **3** is a chart showing an example of external signal waveforms for switching between a normal access mode and the clock synchronous mode of the present invention.

FIG. **4** is a chart showing an example of external signal waveforms for switching between a normal mode and a conventional clock synchronous mode according to the present invention.

FIG. **5** is a chart comparing external waveforms in the case of modifying the number of clock cycles used in the internal operation, within the same memory.

FIG. **6** is a configuration diagram for a clock-synchronous semiconductor memory device of the present invention which is capable of executing the access methods shown in FIGS. **1** to **5**.

FIG. **7** is a diagram of a clock-synchronous delay circuit for an internal circuit drive signal.

FIG. **8** is a circuit diagram for a delayed signal selection switching circuit.

FIG. 9 is a circuit diagram for a blown fuse signal generating circuit.

FIG. 10 is a circuit diagram for a circuit for generating a drive signal for a delayed signal selection switching circuit.

FIG. 11 is a waveform diagram showing the relationship between each delayed signal in FIG. 8 and the basic clock cycle.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The features of this invention will become apparent in the course of the following description of exemplary embodiments which are given for illustration of the invention and are not intended to be limiting thereof.

Preferred embodiments of the present invention will now be explained with reference to the drawings.

This example will be explained using a timing chart illustrated in FIG. 1.

In the timing chart of FIG. 1, all of the signals are set with respect to the transition of the rising edge of the basic clock signal CLK. For example, at a first clock cycle CLK1, an external signal /RE (Row Enable signal), which is provided from external device, is switched to the "L" level, and a so-called row address which designates a row in a memory cell array is introduced. Accordingly, the setting of the conditions of this address, as shown in the drawing, is asserted based on the rising edge of the basic clock signal CLK.

In the same manner, a column address designating a column in the memory cell array is based on the transition of the rising edge of a clock cycle (CLK4) of the basic clock signal CLK when the external control signal /CE (Column Enable signal) is at "L" level, specified as shown in the drawing.

In a data output operation, for example, a series of access operations is carried out in three clock cycles, and at the fourth cycle (CLK8) data (C1) is output to the outside from the chip in which a semiconductor memory device is formed.

In changing the column address during the course of the serial output, a cycle in which the Column Enable signal /CE as a control signal is at "L" level is made, and the column address is set in the same manner with respect to the timing of the transition of the rising edge (CLK15) of this basic clock signal. After the four cycles later from the setting (CLK19), data is output serially in a predetermined order (C2, C2+1, C2+2, . . .), in which the data at a new column address is output at first.

The case will be considered where the basic clock signal period is short, for example, about 10 ns. In this case, it is difficult to set an address from a particular cycle synchronous with this basic clock signal CLK, while reliably setting the set-up and holding time for maintaining the conditions of the address signal, based on the transition of the rising edge of one cycle of the basic clock signal CLK. Specifically, it is difficult, counting from the next cycle, to select the specified cycle and to set the address within that cycle.

In addition, from an aspect of a circuit operation, it is difficult to specify a cycle and reliably input an address signal or the like in this cycle, then operate this circuit stably with good reliability when the period of the basic clock signal CLK is short. Strict timing control is necessary for both the system aspect side and the chip aspect side, and a complicated circuit design is required to provide this.

Moreover, in the case of a system where the period of the basic clock signal CLK is long, when the memory chip normally performs an internal operation at a specified cycle following the setting cycle for the column address, a large amount of access time is necessary for accessing the head address when accessing from a newly-set column address.

In this manner, when an operating method utilizing a basic clock signal CLK is uniform, or more specifically, invariable, the system cycle time is unchangeable to a certain degree.

There is therefore the problem that this operating method is difficult to apply in practice to a system in a range which can efficiently utilize the cycle.

To solve the problem, the second preferred embodiment of the present invention will now be explained.

There is a case that it is difficult to set an address in one cycle synchronous with a basic clock signal CLK when the cycle time is short.

One method of avoiding this is provided in the embodiment of the present invention shown in FIG. 2.

In this drawing, first, when a Row Enable control signal /RE is at "L" level (immediately prior to a signal CLK1), the operation for introducing the address is activated. However, at this time, the address operation inside a semiconductor memory device synchronized with the basic clock signal CLK has not yet started. The input of this address is the same as setting by means of a conventional DRAM, and in the setting of the address there are no occasional difficult areas. Specifically, the address can be introduced without being restricted by the timing of the basic clock. In this manner, the address is set by means of the Row Enable control signal /RE and a Column Enable control signal /CE (which can be referred to as first control signals), and actual data access for an address introduced into memory synchronized with the basic clock signal CLK is commenced by means of a control signal /SYNC as an external second control signal. If the control signal /SYNC is at "L" level (CLK4) at the transition of the onset of the clock signal, the memory device enters the synchronous mode from that cycle, and an internal access operation proceeds synchronous with the basic clock signal.

As a result, the output of data C1 to the outside begins at the commencement of a synchronized operation (CLK4) in this embodiment at the fourth cycle (CLK8). To change the column address during serial access, with the control signal /SYNC at "H" level (CLK12), a new column address C2 is introduced asynchronously with the basic clock signal, and an address is set and introduced at the falling edge of the control signal /CE (CLK12). Next, the control signal /SYNC is once again switched to "L" level (CLK15) and synchronized access commences at this new address.

In FIG. 2, access to a new column address starts from CLK15, and a switch from address C1 to address C2 is made from CLK19 after four cycles.

On further expanding this concept, it is possible to provide a semiconductor memory device in which an operation mode can be set for each cycle which sets a row address. The operation mode in this case means data output timing and is defined as either a basic clock signal synchronized access mode (hereinafter—synchronous mode) wherein the data output is accessed in synchronism with a state of the basic clock signal CLK after addresses to be accessed are set or a mode in which data output is started after addresses to be accessed are set like a conventional DRAM (hereinafter we call the mode "a normal mode").

FIG. 3 and FIG. 4 are charts showing a method of switching between these two modes.

FIG. 3 illustrates a method for switching between a conventional normal mode and the synchronous mode of the

present invention explained in the second embodiment shown in FIG. 2. The control signal /SYNC is used as a control signal for this switching. If this control signal /SYNC is at "L" level when the control signal /RE falls (CLK1), the normal mode is in effect; if at "H" level, it is the same as the normal mode for address input operation, but the synchronous mode is effected only when the control signal /SYNC is fallen (CLK31). This is an example for the synchronous mode in the present invention.

FIG. 4 shows the case of switching between a conventional normal mode and the synchronous mode illustrated in the first embodiment shown in FIG. 1. In this case, for example, the control signal /SYNC is used, and the condition of the control signal /SYNC when the control signal /RE falls determines whether the normal mode or the synchronous mode is entered.

In FIG. 4, the normal mode occurs when the control signal /SYNC is at "H" level; and the synchronous mode occurs when the control signal /SYNC is at "L" level (CLK22). When the control signal /RE is at the "L" level, synchronous operation commences from the first clock signal (CLK23). In the switch to this mode, it is understood that, even when the control signal /SYNC is not used, the mode setting cycle may be set separately.

In any of the above cases, because it is possible to provide for a conventional normal mode and a synchronous mode of the present invention by using a time sharing method in the same semiconductor memory device, this method is effective in the case where random access and high speed serial access are required in the same semiconductor memory device.

Next, a case will be explained in which the basic clock signal CLK of the system is not necessarily produced at maximum speed. If at a cycle time of 10 ns there is efficient synchronous memory control, while at a cycle time of 20 ns the operation within the memory remains unchanged, the initial access after setting the column address requires twice the time.

Also the time to spare for the operation within the memory becomes large so that there is considerable time during which the operation is idle.

In order to avoid this and achieve an efficient memory operation, it is desirable that the cycle of the internal operation be capable of modification according to the cycle length of the basic clock signal CLK used.

FIG. 5 is a timing chart showing an example of an access timing method with the above-mentioned type of function. This chart shows two cases, each with a different number of cycles required for the internal operation. Also, an example of a conventional type of synchronous mode is illustrated in order to make the explanation more easily understandable.

Example 2 in FIG. 5 illustrates the case where the number of cycles of the synchronous operation corresponds to the first embodiment shown in FIG. 1.

Example 1 in FIG. 5 corresponds to a case in which the number of cycles of the synchronous operation is decreased. In this case, an operation following the internal operation of example 1 cannot be carried out at a short period for a basic clock cycle the same as example 2, but the chart shows two cases with respect to the same clock cycle in order to observe the difference in the number of control cycles. In example 1, the internal operation is performed in half the number of cycles of example 2. Accordingly, in practice, example 2 relates to control of a system in which the period of the basic clock signal is a 10 ns cycle, while example 1 shows a system control method for a 20 ns cycle.

An optimum operation is performed with both these systems. Another embodiment of the present invention will now be explained.

A configuration of a clock-synchronous semiconductor memory device which can execute the access methods shown in FIGS. 1 to 5 described above will be explained referring to FIG. 6.

FIG. 6 shows the configuration of the clock-synchronous semiconductor memory device 10 which can execute effectively the access methods of the present invention.

As one basic operation of the semiconductor memory device 10, a memory access operation of the semiconductor memory device 10 is carried out based on an external basic clock signal CLK and at least one or more external control signals which are provided continuously to the semiconductor memory device.

In FIG. 6, a memory device 10 comprises a counting section 5 and a control section 14, which are main control elements of the semiconductor memory device, in addition to a memory cell group 11, a selection section 12, and a specification section 13.

A dynamic memory cell, a static memory cell, or the non-volatile memory cell of the memory cell group 11 is arranged in the form of a matrix.

The data which is written in and read out is stored in this memory cell.

The data access is carried out between the memory cell group 11 and external devices (not shown) through a data I/O section 4.

The specification section 13 sets consecutive addresses in the memory cell group 11 according to a series of externally-provided address signals under the control of the control section 14, and designates, in order, the memory cells which are to be accessed. Under the control of the control signals /SYNC, /RE, and /CE input into the control section 14, the specification section 13, for example, fetches a row address signal, then fetches a series of column address signals for a string of memory cells in the memory cell group 11 connected to a word line designated by the row address signal. The specification section 13 designates a series of memory cells consecutively by means of the column address signal.

The data I/O section 4 performs a read or write operation on the memory cell group 11 designated by the specification section 13 based on a read/write signal obtained externally.

The read-out data is output to an external destination through the data I/O section 4. The data to be stored is provided to the designated memory cell from an external source through the data I/O section 4 by the specification section 13.

The counting section 5 is a counter for counting the number of cycles of the basic clock signal CLK continuously input at an almost fixed frequency from an external source.

The counter 5 is capable of counting a fixed number of clock cycles of the basic signal CLK and discriminating some clock cycles from other cycles. A circuit having a counter function can be used for the counter 5. Therefore a circuit having counter function described above can be circuit in the semiconductor memory device 10.

The external basic clock signal CLK used in this embodiment is a clock signal with a cycle time of, for example, less than the 30 ns access time of the memory device. The counting section 5 provides the control section 14 with the count of the number of cycles of the clock signal CLK.

The control section 14 sends a selection signal to the selection section 12 based on the level of the control signal /SYNC provided from external.

Based on the selection signal, the selection section **12** selects the access timing of the memory cell group **11**, then sends address activation signal φA to φD to the memory cell group **11**.

The selection section **12** selects either the normal operation mode or the synchronous operation mode which have been already explained and shown in FIGS. **3** and **4** under the control of the control section **14**.

When the selection section **12** is not included in the semiconductor memory device **10**, the semiconductor memory device performs only the access methods shown in FIGS. **1** to **4**.

Configurations of the counting section **5** and the control section **14** will be described below referring to FIGS. **7** to **10**.

Generally, the internal operation is basically controlled with a minimum unit of operation time corresponding to a basic clock signal CLK. Accordingly, the number of basic clock cycles it takes to carry out a series of operations can be selectively determined by controlling the transmission to the section of the circuit in which this operation is carried out, using a number of cycles for a signal to start a certain operation.

FIGS. **7** to **10** show examples of configurations of circuits by which this selection can be set by using an external laser to blow a fuse inside a chip.

FIG. **7** shows an example in which a trigger signal RINT for a certain circuit is delayed only for a time corresponding to a number of parts of the cycles of the basic clock signal CLK. This circuit is a so-called shift register circuit, and transmission is carried out successively in the state where the signal RINT is at the "H" level, according to the change in a signal INTCLK inside the chip, synchronized with the basic clock signal CLK. INTCLK and /INTCLK are of opposite phases. In FIG. **7**, when /INTCLK is at the "H" level, a signal in a latch circuit of the previous step is transmitted, and when INTCLK is at the "H" level, a signal in a latch circuit of the following step is transmitted. Accordingly, a delay circuit in FIG. **7** produces a signal delay at one part of the basic clock cycle, and the signal RINT is delayed by one cycle is output as a signal CINT1.

In addition, by passing through the same type of circuit, CINT2 is produced which is a delay of one cycle from CINT1, and CINT3 is produced which is a delay of one cycle from CINT2. In a clocked inverter such as shown in FIGS. **7** and **8**, the circuit acts as an inverter at the "H" level signal expressed at the output part and at the "L" level signal expressed at the output part, and the output becomes a high impedance and is isolated from a node portion proceeding the output. The relation of the basic clock cycle to the signal is shown in FIG. **11**. In this chart, a plurality of signals CINT1, CINT2, and CINT3 are shown, each of which onsets at the respective cycles CLK2, CLK3, and CLK4, which are successively one cycle delayed respectively from the signal RINT which is risen at the signal CLK1. Depending on which of these signals is used, it is possible to specify at which cycle following a prescribed cycle in the basic clock signal certain operations, for example, I/O operations, will be performed. When observed from a basic configuration portion of a synchronous-type memory, these delayed circuits can be considered as forming counters for the basic clock cycle.

FIG. **8** is a diagram showing a part which selects any delayed signal and supplies this signal to a driven circuit as the signal CINT used in actual control. From the action of the clocked inverter, the signal output as the output signal CINT when VL is at the "H" level is CINT1; when VM is at the "H" level—CINT2; and when VH is at the "H" level—CINT3. The circuit used as the switch, if switched in accordance with the period of the basic clock signal CLK of the system using the memory, can cause the optimum operation to be performed in the system.

Several methods for creating the signal for switching can be considered. Blowing a fuse; modifying a mask pattern for a process for including a wiring layer in the memory IC; a method by which an internal node is given either a floating or a fixed potential using bonding from a power source line pin, which has the same effect as blowing a fuse; a method for distinguishing whether a pin used as a non-connected pin is connected to the power source or is floating, or the like; a programming method for distinguishing the condition of another external signal at the timing when the control signal /RE falls or the like; are examples which can be given.

The following explanation covers a specific case using the blowing of a fuse. FIG. **9** is a diagram showing a circuit for creating a combination of four signal conditions by blowing two fuses. In the case where neither a fuse **1** or a fuse **2** is blown, a signal F1 and a signal F2 are set at the "L" level until the onset of the signal RINT, then, at the onset of the signal RINT both the signals F1 and F2 rise to the "H" level.

On the other hand, when a fuse is blown, because a transistor T1 or a transistor T2 does not become a pass connected to ground or earth, the signal F1 or the signal F2 is maintained at the latch level and is held at the "L" level even on the onset of the signal RINT. According to the method of blowing the fuses **1**, **2**, there are four ways in which conditions of the signals F1 and F2 can be combined.

Three of these four ways for creating a signal for input to the switching circuit of FIG. **8**, are illustrated by the circuits shown in FIG. **10**. The circuits shown in FIG. **10** are logical circuits for creating the signals VH, VM, and VL from the signals F1 and F2 produced by the combination of the blown fuses when the signal RINT is at the "H" level. If neither of the fuses **1** and **2** in the circuits explained above is blown, VH is switched to the "H" level and the onset of the signal CINT occurs at the fourth cycle from the onset of the signal RINT. If the fuse **1** only is blown, VM is switched to the "H" level and the onset of the signal CINT occurs at the third cycle from the onset of the signal RINT. When both fuses are blown, VL is switched to the "H" level and the onset of the signal CINT occurs at the second cycle from the onset of the signal RINT.

In the case where the fuse **2** only is blown, none of the signals onsets, therefore, the signal CINT does not onset.

In all methods such as modifying a mask pattern for a process for introducing another wiring layer in the memory IC; a method using bonding from a power source line pin to a pad for an internal node in place of a fuse, and a method for distinguishing whether a pin used as a non-connecting pin is connected to the power source or is floating, or the like, the structure and the method for grounding the corresponding node of the transistors T1, T2 in place of the fuses **1**, **2** can be easily inferred by one skilled in the art. These particulars are self-evident, therefore further explanation will be omitted here.

On the other hand, in a programming method for distinguishing the condition of several external signals at the timing when the control signal /RE falls, or the like, signals corresponding to the signals F1, F2 are created directly by the internal logic. If the corresponding relationship with the external signal condition is set, it is possible to easily fabricate a logic circuit so that a signal corresponding to F1 and F2, or VH, VM and VL is generated during that condition.

As explained in the foregoing, with the clock-synchronous semiconductor memory device of the present invention, for example, in the case where the address is set in synchronism with the basic clock signal CLK after the control signals /RE and /CE are input, memory access operation can be carried out accurately.

Further, for example, in the case where the period of the basic clock signal CLK for the system is short, it is possible to set an address value using a method unrelated to the length of the period of the basic clock cycle. Accordingly, the design of the system timing and the prerequisites relating to the internal memory operations becomes easier, even in the case where the period of the clock cycle is short.

Further, with respect to access of data, the present invention takes advantage of the special feature of the clock synchronous method of access.

In addition, when random access such as the page mode of a conventional DRAM is necessary, and also in the case where the system is based on a circuit structure in which high speed serial access is synchronous with the clock cycle, it is possible to switch between DRAM mode and synchronous mode on the same chip through time-sharing. Therefore, if other methods are used in the present invention, the system can be efficiently constructed.

In particular, it can be applied in practice to an image memory. Furthermore, in order to cope with optimum operation of memory in systems with various periods shown in other embodiments, it is possible to modify the number of cycles used for the data access operation of the memory, therefore, it is possible to design a single memory for application to many systems. For this reason, a memory can be selected which can demonstrate system performance of maximum scope.

Thus, it is possible to certainly set an address to be accessed, in spite of the length of a period of a basic clock signal, and to output data accurately by the clock-synchronous semiconductor memory device and access methods thereof according to the present invention.

What is claimed is:

1. A semiconductor device, comprising:

a memory cell array having a plurality of memory cells arranged in rows and columns, said memory cells storing data and being selected according to address signals; and

control means for receiving a clock signal and a first control signal, for outputting a plurality of said data in synchronism with said clock signal after said first control signal is asserted, output of said data beginning a number of clock cycles (latency N) of said clock signal (latency N being a positive integer $\geqq 2$) after said first control signal is asserted, a different one of said data being output at each of said clock cycles after said output begins until said plurality of data is output,

wherein said latency N is determined by externally supplying a latency control signal.

2. A semiconductor device according to claim 1, wherein said control means receives said address signals on a transition of said clock signal after said first control signal is asserted.

3. A semiconductor device according to claim 1, wherein said control means further receives row address signals for selecting said memory cells and a second control signal, said control means receiving said row address signals on a transition of said clock signal after said second control signal is asserted.

4. A semiconductor device according to claim 1, wherein said control means further comprises count means for counting said latency N.

5. A semiconductor device according to claim 1, wherein said first control signal is a pulse signal.

6. A semiconductor device according to claim 1, further comprising specification means, to which said address signals are input, for selecting memory cells in said memory cell array.

7. A semiconductor device according to claim 6, wherein

said address signals include row address signals and column address signals; and

said first control signal includes a row enable signal for inputting row address signals into said specification means and a column enable signal for, after a row address is determined in said specification means by an input of said row address signals, inputting said column address signals into said specification means.

8. A semiconductor device according to claim 6, wherein

said address signals include at least row address signals; and

said first control signal includes at least a row enable signal for inputting row address signals into said specification means.

9. A semiconductor device according to claim 6, wherein

said address signals include at least column address signals; and

said first control signal includes at least a column enable signal for inputting column address signals into said specification means.

10. A semiconductor device according to claim 1, further comprising:

delay means for generating delay signals, each of said delay signals having a delay time period equivalent to a different number of cycles of said basic clock signal; and

switching means for receiving the delay signals generated by said delay means, and for selecting one of said delay signals in response to said latency control signal to control said outputting of said data.

11. A semiconductor device according to claim 10, wherein said delay means includes count means for counting the number of cycles of said basic clock signal; and

said count means generates said delay signals and supplies said delay signals to said switching means.

12. A semiconductor device according to claim 11, wherein

said count means includes a series of shift registers for transferring a trigger signal in response to a signal synchronized with said basic clock signal.

13. A semiconductor device according to claim 12, wherein each of said shift registers includes clocked inverters which operate in response to said signal synchronized with said basic clock signal.

14. A semiconductor device according to claim 10, wherein

said switching means includes clocked inverters one of which is selected and then becomes active; and

said number N of said latency is determined by an output signal of a selected clocked inverter.

15. A semiconductor device according to claim 3, wherein said second control signal is a pulse signal.

16. A semiconductor device according to claim 7, wherein

said row enable signal is used for inputting said row address signals into said specification means in response to a transition of said basic clock signal; and

said column enable signal is used for inputting said column address signals into said specification means in response to a transition of said basic clock signal.

17. A semiconductor device according to claim 8, wherein said row enable signal is used for inputting said row address signals into said specification means in response to a transition of said basic clock signal.

18. A semiconductor device according to claim 9, wherein said column enable signal is used for inputting said column address signals into said specification means in response to a transition of said basic clock signal.

19. A semiconductor device, comprising:

a memory cell array having a plurality of memory cells arranged in rows and columns, said memory cells storing data and being selected according to address signals; and

control means for receiving a clock signal and a first control signal, for outputting a plurality of said data in synchronism with said clock signal after said first control signal is asserted, output of said data beginning a number of clock cycles (latency N) of said clock signal (latency N being a positive integer$\geqq$2) after said first control signal is asserted, a different one of said data being output at each of said clock cycles after said output begins until said plurality of data is output,

wherein said latency N is variably programmed.

20. A semiconductor device according to claim 19, wherein said control means receives said address signals on a transition of said clock signals after said first control signal is asserted.

21. A semiconductor device according to claim 19, wherein said control means further receives row address signals for selecting said memory cells and a second control signal, said control means receiving said row address signals on a transition of said clock signal after said second control signal is asserted.

22. A semiconductor device according to claim 19, wherein said control means further comprises count means for counting said latency N.

23. A semiconductor device according to claim 19, wherein said first control signal is a pulse signal.

24. A semiconductor device according to claim 19, further comprising specification means, to which said address signals are input, for selecting memory cells in said memory cell array.

25. A semiconductor device according to claim 24, wherein

said address signals include row address signals and column address signals; and

said first control signal includes a row enable signal for inputting row address signals into said specification means and a column enable signal for, after a row address is determined in said specification means by an input of said row address signals, inputting said column address signals into said specification means.

26. A semiconductor device according to claim 24, wherein

said address signals include at least row address signals; and

said first control signal includes at least a row enable signal for inputting row address signals into said specification means.

27. A semiconductor device according to claim 24, wherein

said address signals include at least column address signals; and

said first control signal includes at least a column enable signal for inputting column address signals into said specification means.

28. A semiconductor device according to claim 19, further comprising:

delay means for generating delay signals, each of said delay signals having a delay time period equivalent to a different number of cycles of said basic clock signal; and

switching means for receiving the delay signals generated by said delay means, and for selecting one of said delay signals to control said outputting of said data.

29. A semiconductor device according to claim 28, wherein

said delay means includes count means for counting the number of cycles of said basic clock signal; and

said count means generates said delay signals and supplies said delay signals to said switching means.

30. A semiconductor device according to claim 29, wherein

said count means includes a series of shift registers for transferring a trigger signal in response to a signal synchronized with said basic clock signal.

31. A semiconductor device according to claim 30, wherein

each of said shift registers includes clocked inverters which operate in response to said signal synchronized with said basic clock signal.

32. A semiconductor device according to claim 28, wherein

said switching means includes clocked inverters one of which is selected and then becomes active; and

said number N of said latency is determined by an output signal of a selected clocked inverter.

33. A semiconductor device according to claim 32, wherein said switching means further comprises a fuse section having a plurality of fuses, and wherein one of said clocked inverters is selected and becomes active in accordance with states of said plurality of fuses.

34. A semiconductor device according to claim 32, wherein

said switching means further comprises a fuse section having a plurality of fuses, and a signal creating section which generates signals in accordance with cutting/non-cutting states of said plurality of fuses, and which supplies said signals to clock input terminals of said clocked inverters to control operation of said clocked inverters; and

one of said clocked inverters is selected and becomes active in accordance with said cutting/non-cutting states of said plurality of fuses.

35. A semiconductor device according to claim 34, wherein

said fuse section further comprises a plurality of latch circuits which are coupled to said plurality of fuses, respectively, and which assume states in accordance with said cutting/non-cutting states of said fuses; and

signals which have been latched by said latch circuits are supplied to said signal creating section.

36. A semiconductor device according to claim 35, wherein

said signal creating section comprises logical circuits, to which output signals of said latch circuits are supplied and which generate combination signals; and

said combination signals are respectively supplied to input terminals of said clocked inverters, one of said clocked inverters being selected by said combination signals.

37. A semiconductor device according to claim 21, wherein said second control signal is a pulse signal.

38. A semiconductor device according to claim 25, wherein

said row enable signal is used for inputting said row address signals into said specification means in response to a transition of said basic clock signal; and

said column enable signal is used for inputting said column address signals into said specification means in response to a transition of said basic clock signal.

39. A semiconductor device according to claim 26, wherein

said row enable signal is used for inputting said row address signals into said specification means in response to a transition of said basic clock signal.

40. A semiconductor device according to claim 27, wherein

said column enable signal is used for inputting said column address signals into said specification means in response to a transition of said basic clock signal.

41. A semiconductor device comprising:

a memory cell array having a plurality of memory cells arranged in rows and columns, said memory cells storing data and being selected according to address signals;

control means for receiving a clock signal and a first control signal, for outputting a plurality of said data in synchronism with said clock signal after said first control signal is asserted, output of said data beginning a number of clock cycles (latency N) of said clock signal (latency N being a positive integer≧2) after said first control signal is asserted, a different one of said data being output at each of said clock cycles after said output begins until said plurality of data is output; and

latency determining means for determining the latency N in response to a latency control signal externally supplied.

42. A semiconductor device comprising:

a memory cell array having a plurality of memory cells arranged in rows and columns, said memory cells storing data and being selected according to address signals;

control means for receiving a clock signal and a first control signal, for outputting a plurality of said data in synchronism with said clock signal after said first control signal is asserted, output of said data beginning a number of clock cycles (latency N) of said clock signal (latency N being a positive integer≧2) after said first control signal is asserted, a different one of said data being output at each of said clock cycles after said output begins until said plurality of data is output; and

programming means for variably programming the latency N.

43. A memory system comprising:

a semiconductor memory device including an internal circuit which is controlled to perform memory access operation in response to a clock signal, a first control signal and a latency control signal; and

signal input means for inputting said clock signal, said first control signal and said latency control signal to said semiconductor memory device, said signal input means being arranged outside of said semiconductor memory device;

wherein said semiconductor memory device includes:

a memory cell array having a plurality of memory cells arranged in rows and columns, said memory cells storing data and being selected according to address signals; and

control means for receiving said clock signal and said first control signal, for outputting a plurality of said data in synchronism with said clock signal after said first control signal is asserted, output of said data beginning a number of clock cycles (latency N) of said clock signal (latency N being a positive integer≧2) after said first control signal is asserted, a different one of said data being output at each of said clock cycles after said output begins until said plurality of data is output,

wherein said latency N is determined by externally supplying the latency control signal.

44. A memory system comprising:

a semiconductor memory device including an internal circuit which is controlled to perform memory access operation in response to a clock signal and a first control signal; and

signal input means for inputting said clock signal said first control signal and said latency control signal to said semiconductor memory device, said signal input means being arranged outside of said semiconductor memory device;

wherein said semiconductor memory device includes:

a memory cell array having a plurality of memory cells arranged in rows and columns, said memory cells storing data and being selected according to address signals; and

control means for receiving said clock signal and said first control signal, for outputting a plurality of said data in synchronism with said clock signal after said first control signal is asserted, output of said data beginning a number of clock cycles (latency N) of said clock signal (latency N being a positive integer≧2) after said first control signal is asserted, a different one of said data being output at each of said clock cycles after said output begins until said plurality of data is output,

wherein said latency N is variably programmed in said semiconductor memory device.

45. A semiconductor device comprising:

a memory cell array having a plurality of memory cell sections each of the memory cell sections having a plurality of memory cell arrays with memory cells arranged in rows and columns, said memory cells storing data and being selected according to address signals;

control means for receiving a clock signal and a first control signal, for outputting a plurality of said data in synchronism with said clock signal after said first control signal is asserted, output of said data beginning a number of clock cycles (latency N) of said clock signal (latency N being a positive integer≧2) after said first control signal is asserted, a different one of said data being output at each of said clock cycles after said output begins until said plurality of data is output; and

latency determining means for determining the latency N in response to a latency control signal externally supplied.

46. A semiconductor device comprising;

a memory cell array having a plurality of memory cell sections each of the memory cell sections having a plurality of memory cell arrays with memory cells arranged in rows and columns, said memory cells storing data and being selected according to address signals;

control means for receiving a clock signal and a first control signal, for outputting a plurality of said data in synchronism with said clock signal after said first control signal is asserted, output of said data beginning a number of clock cycles (latency N) of said clock signal (latency N being a positive integer≧2) after said first control signal is asserted, a different one of said data being output at each of said clock cycles after said output begins until said plurality of data is output; and

programming means for variably programming the latency N.

* * * * *

United States Patent [19]

Takemae et al.

[11] **Patent Number: 6,028,816**

[45] **Date of Patent: Feb. 22, 2000**

[54] **SYSTEM CONFIGURED OF SYNCHRONOUS SEMICONDUCTOR DEVICE FOR ADJUSTING TIMING OF EACH INPUT AND SEMICONDUCTOR DEVICE USED THEREFOR**

[75] Inventors: **Yoshihiro Takemae; Masao Taguchi; Yasurou Matsuzaki; Hiroyoshi Tomita; Hirohiko Mochizuki; Atsushi Hatakeyama; Yoshinori Okajima; Masao Nakano**, all of Kawasaki, Japan

[73] Assignee: **Fujitsu Limited**, Kawasaki, Japan

[21] Appl. No.: **08/924,705**

[22] Filed: **Sep. 5, 1997**

[30] **Foreign Application Priority Data**

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Dec. 13, 1996	[JP]	Japan	8-334208
Jun. 26, 1997	[JP]	Japan	9-170714

[51] **Int. Cl.**^{7} **G11C 8/00**

[52] **U.S. Cl.** **365/233**; 365/230.03; 365/230.06; 365/230.08

[58] **Field of Search** 365/233, 240, 365/230.03, 230.08, 230.06

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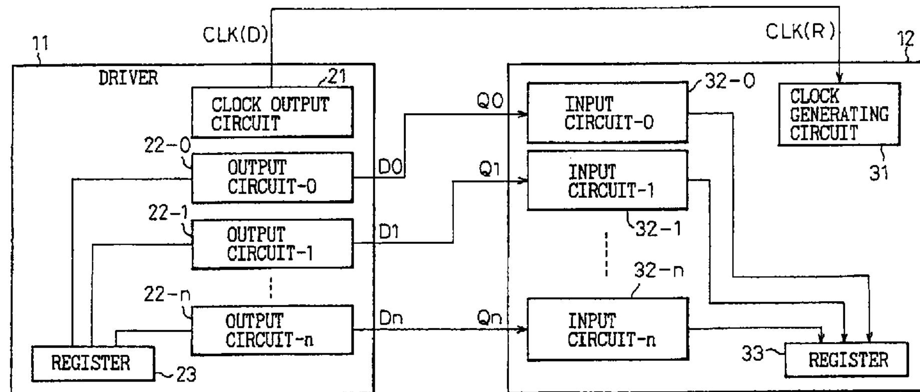
Primary Examiner—David Nelms
Assistant Examiner—Tuan T. Nguyen
Attorney, Agent, or Firm—Nikaido, Marmelstein, Murray & Oram LLP

[57] **ABSTRACT**

A system and a semiconductor device for realizing such a system are disclosed. The system uses at least a semiconductor device for retrieving an input signal in synchronism with an internal clock generated from an external clock, the input signal remaining effectively in synchronism with the external clock. Even in the case where a phase difference develops between a clock and a signal at the receiving end, or even in the case where a phase difference develops between a clock input circuit and other signal input circuits in the semiconductor device at the receiving end, data can be transferred at high speed. Each input circuit of the semiconductor device at the receiving end includes an input timing adjusting circuit for adjusting the phase of the clock applied to the input circuit in such a manner that the input circuit retrieves the input signal in an effective and stable state. In the case where the skew between the input signals is small as compared with the skew between the input signals and the clock, an input timing adjusting circuit is shared by a plurality of the input circuits.

67 Claims, 80 Drawing Sheets



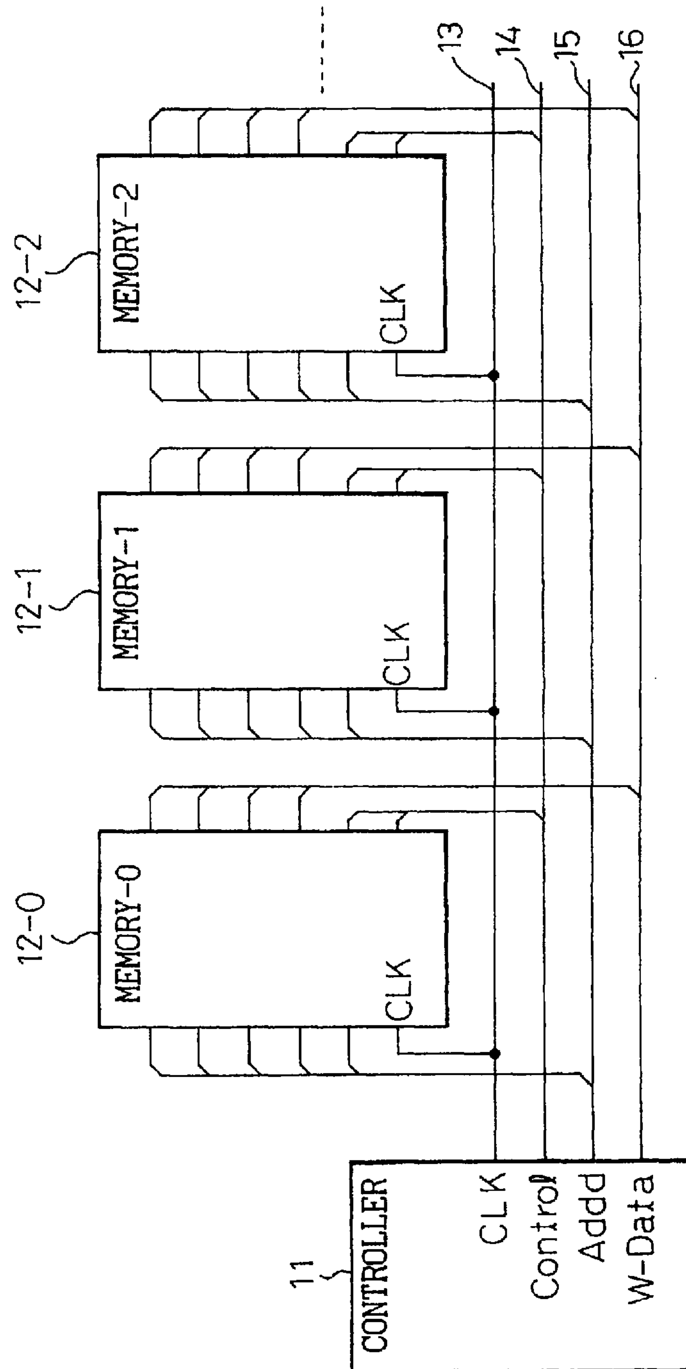
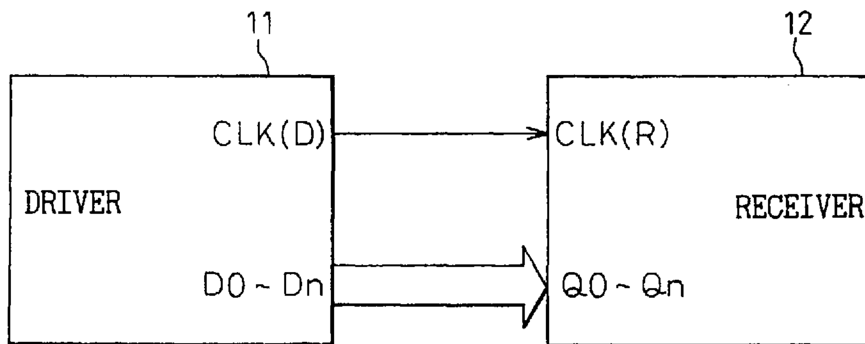


Fig.1
12-0
MEMORY-0
CLK
12-1
MEMORY-1
CLK
12-2
MEMORY-2
CLK
11
CONTROLLER
CLK
Control
Addd
W-Data
13
14
15
16

Fig.2



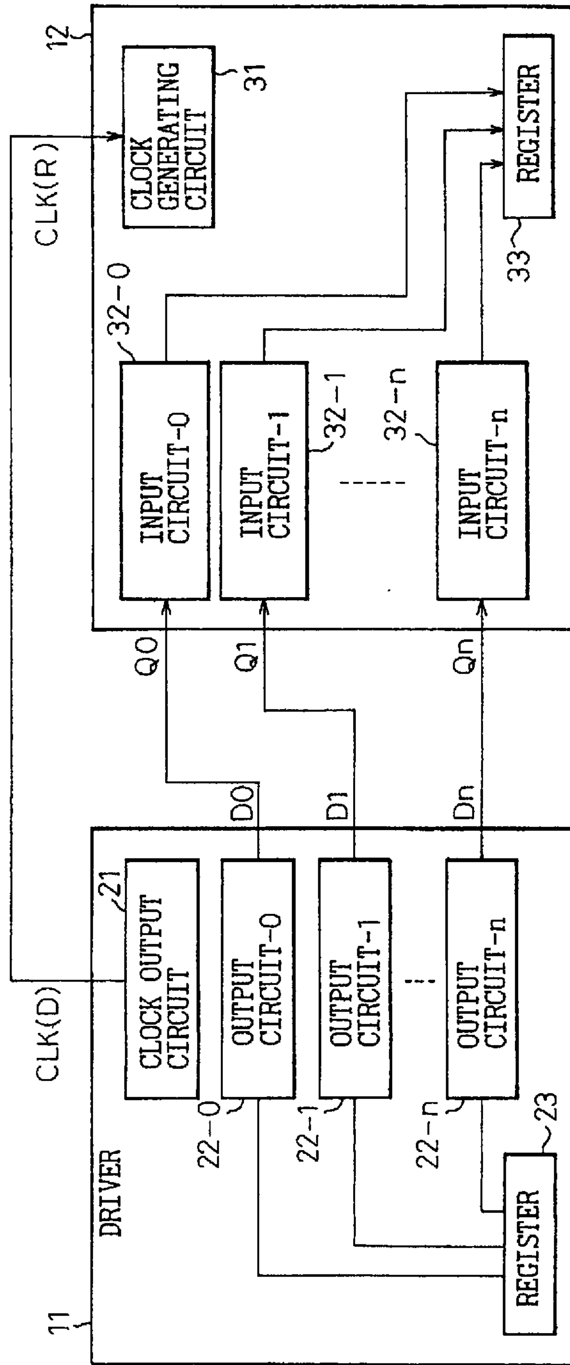


Fig.3

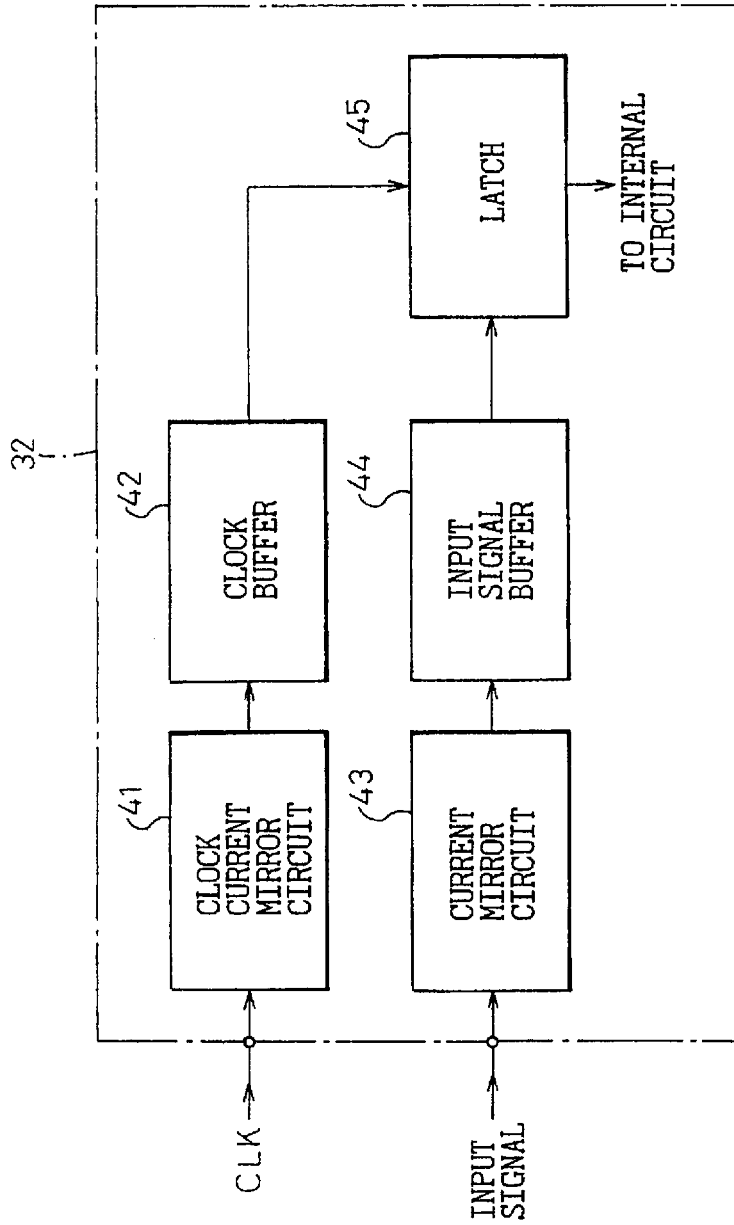
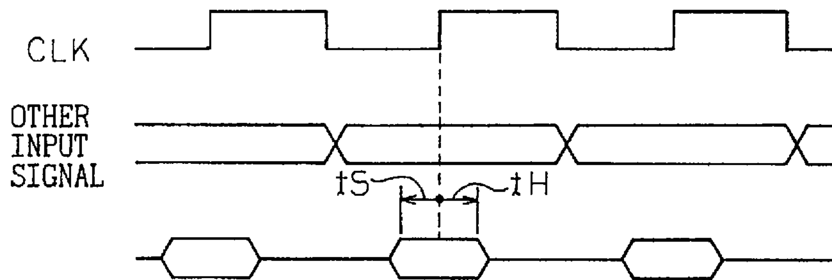


Fig.4
32
CLK
INPUT SIGNAL
41
CLOCK CURRENT MIRROR CIRCUIT
42
CLOCK BUFFER
43
CURRENT MIRROR CIRCUIT
44
INPUT SIGNAL BUFFER
45
LATCH
TO INTERNAL CIRCUIT

Fig.5



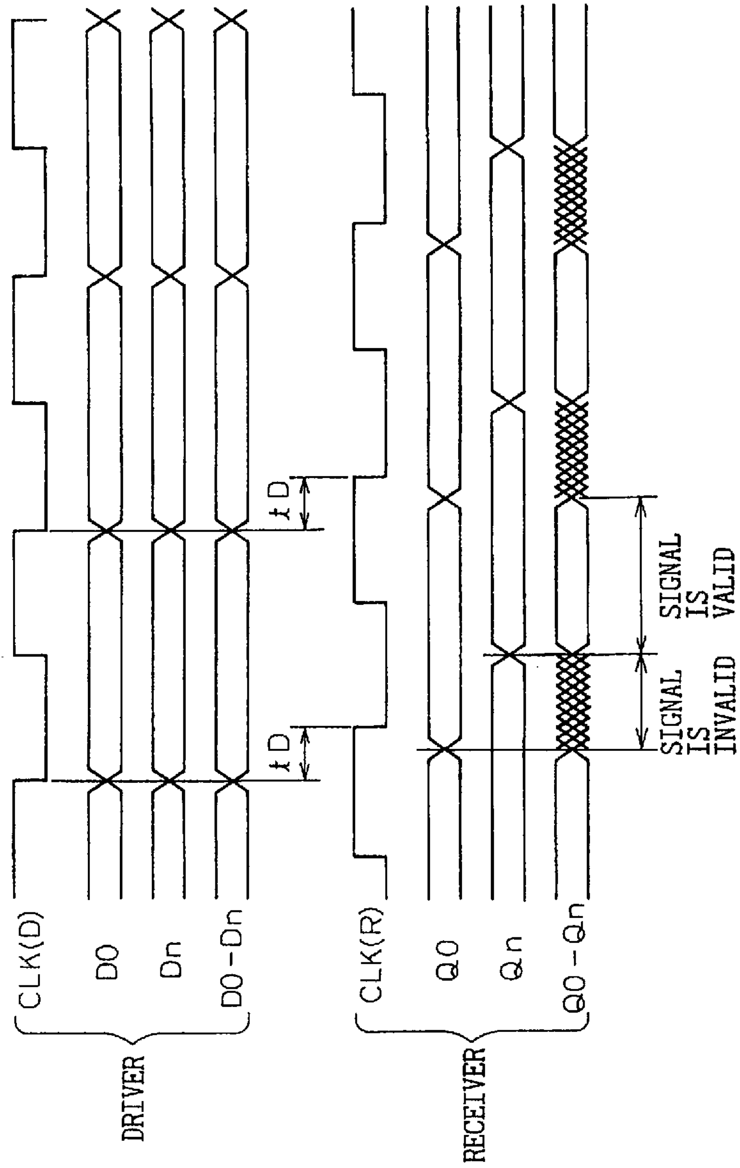


Fig.6
CLK(D)
D0
Dn
D0-Dn
DRIVER
tD
tD
CLK(R)
Q0
Qn
Q0-Qn
RECEIVER
SIGNAL IS VALID
SIGNAL IS INVALID

Fig.7

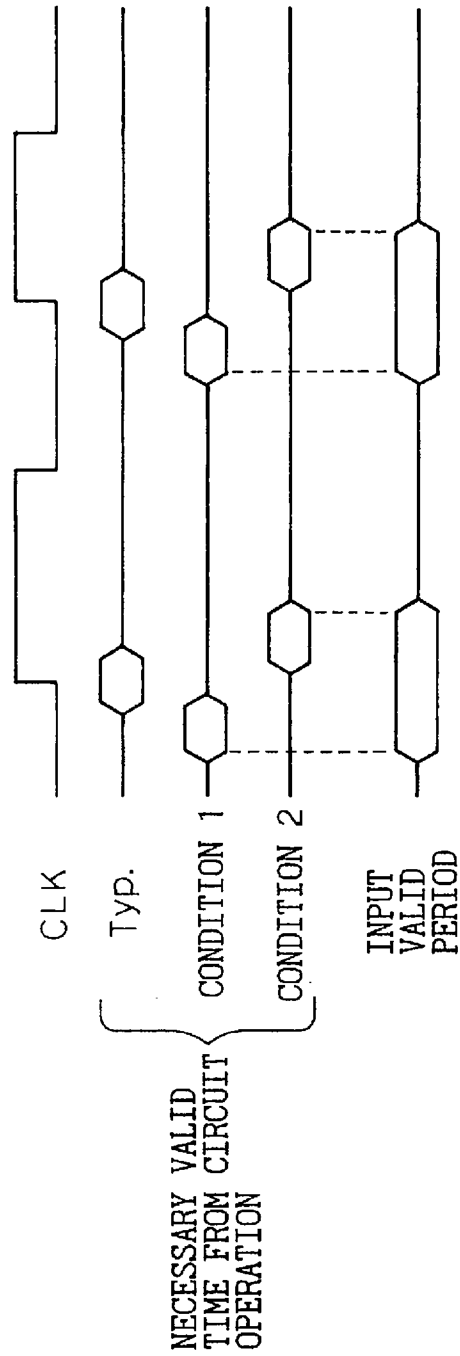


Fig.8

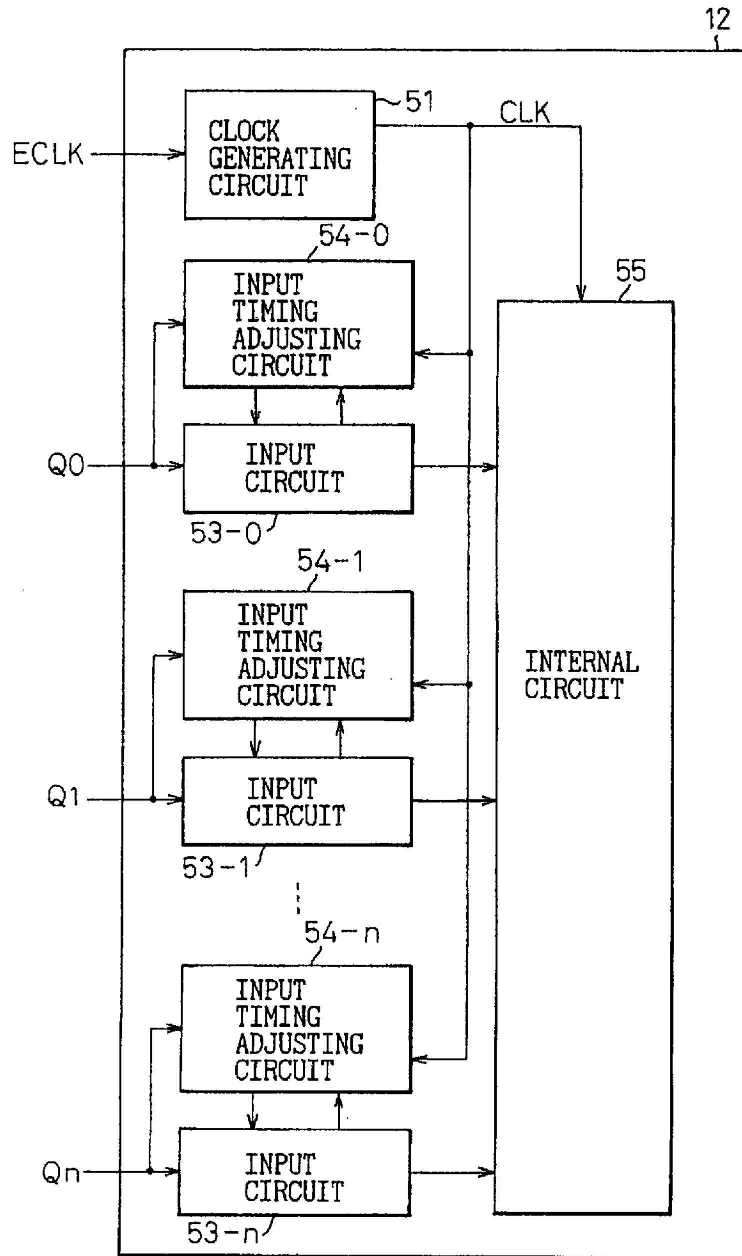
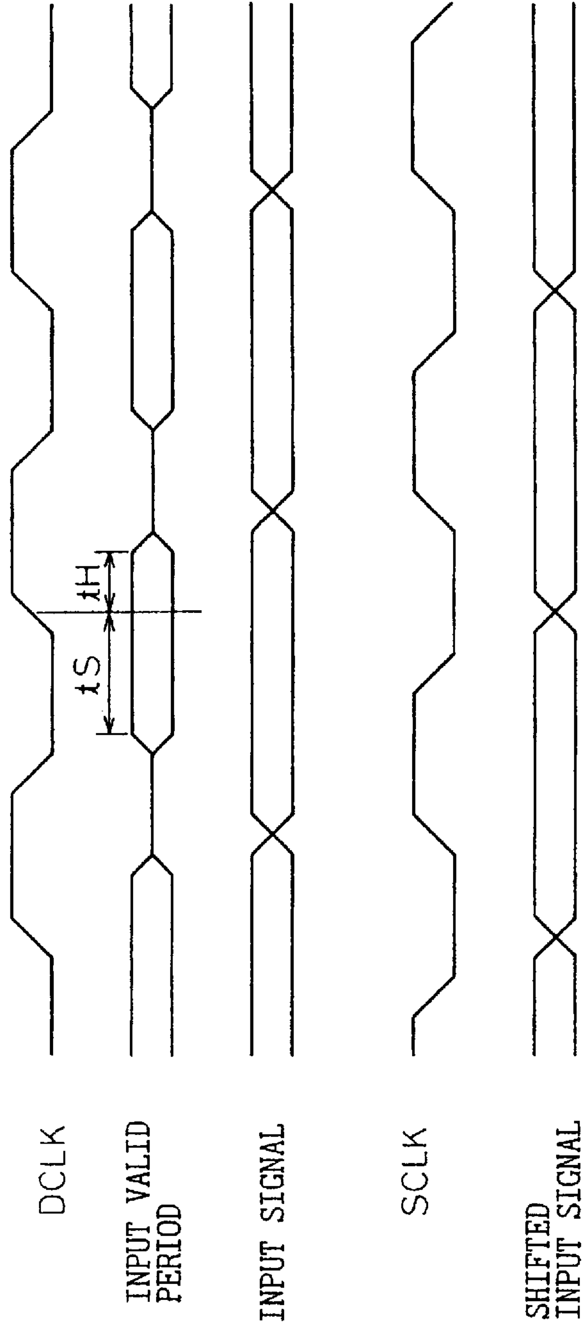


Fig.9



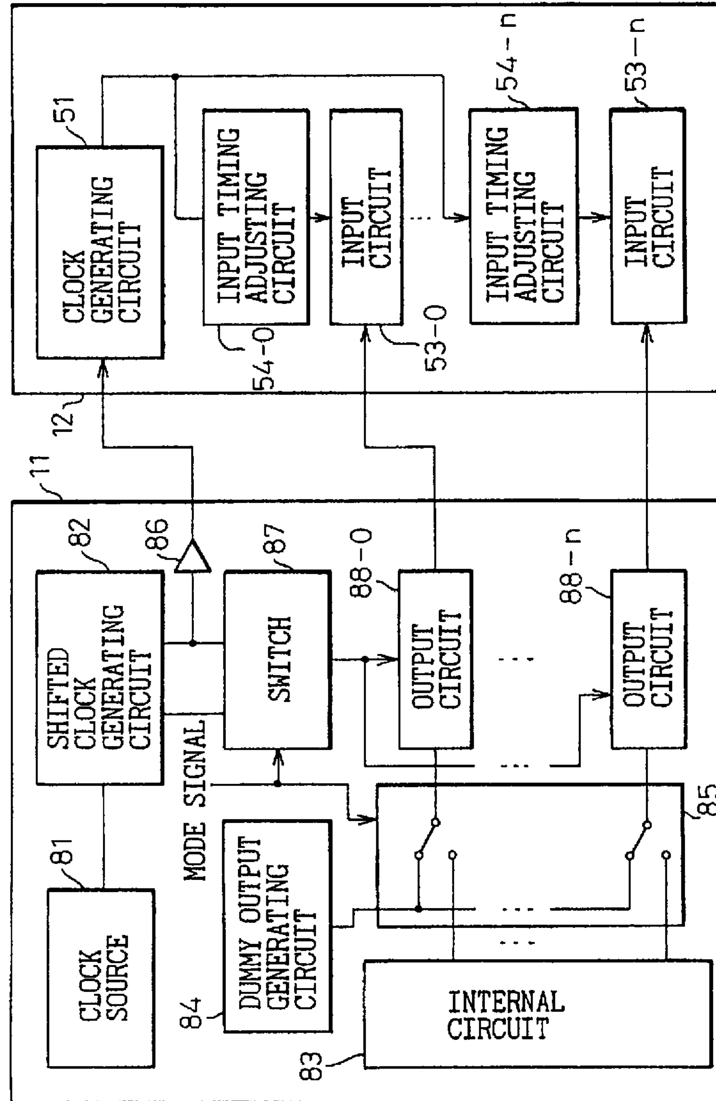


Fig.10

Fig.11

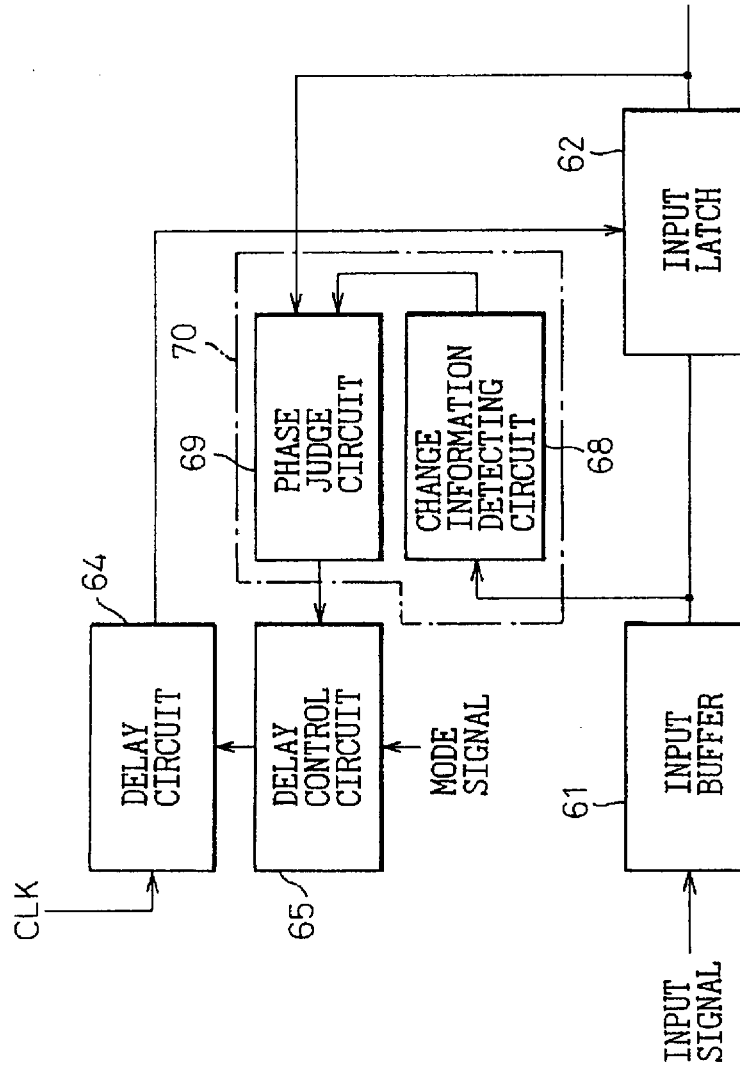
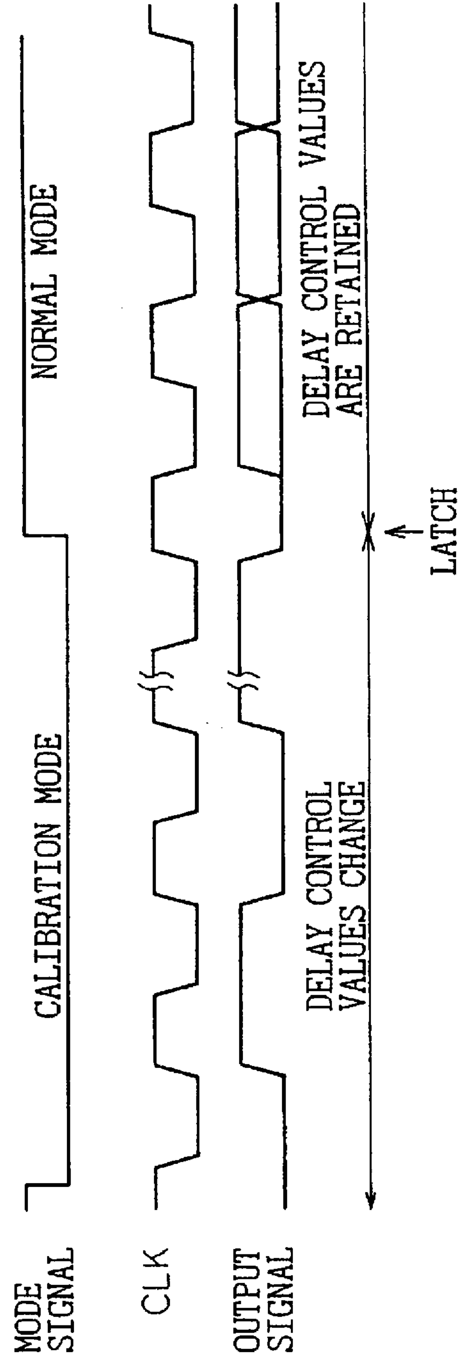


Fig.12



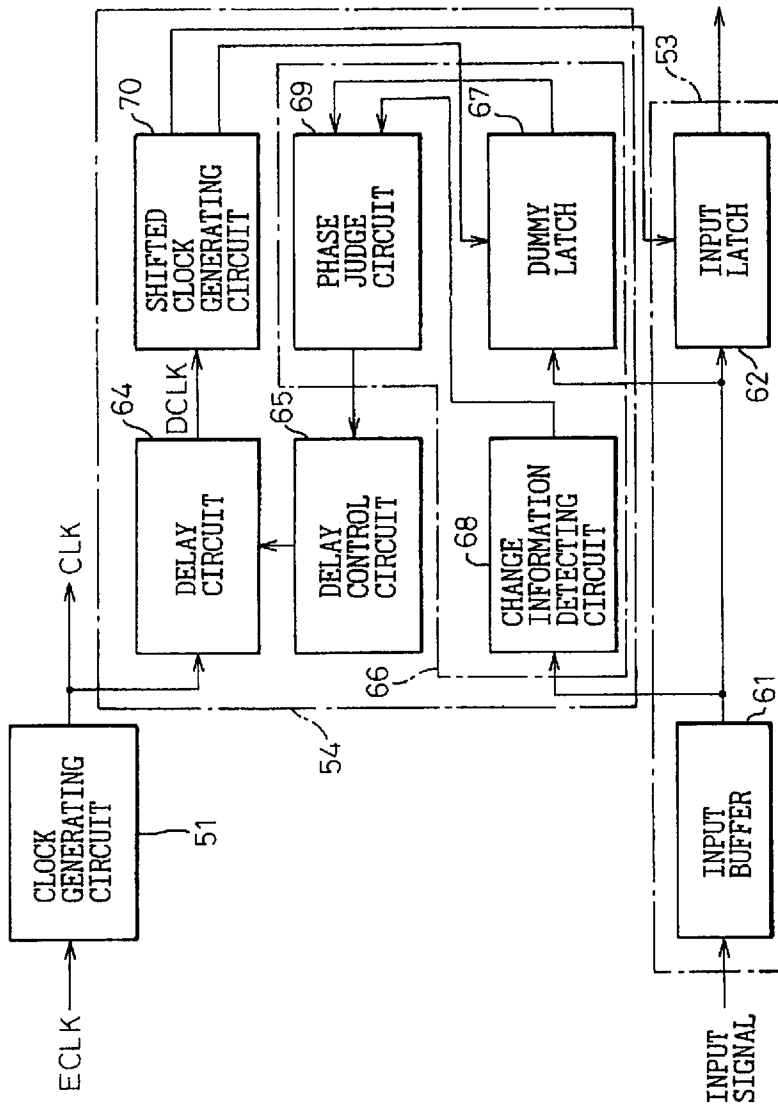


Fig.13
ECLK
CLOCK GENERATING CIRCUIT
51
CLK
DELAY CIRCUIT
64
DCLK
SHIFTED CLOCK GENERATING CIRCUIT
70
DELAY CONTROL CIRCUIT
65
PHASE JUDGE CIRCUIT
69
CHANGE INFORMATION DETECTING CIRCUIT
68
DUMMY LATCH
67
66
54
INPUT SIGNAL
INPUT BUFFER
61
INPUT LATCH
62
53

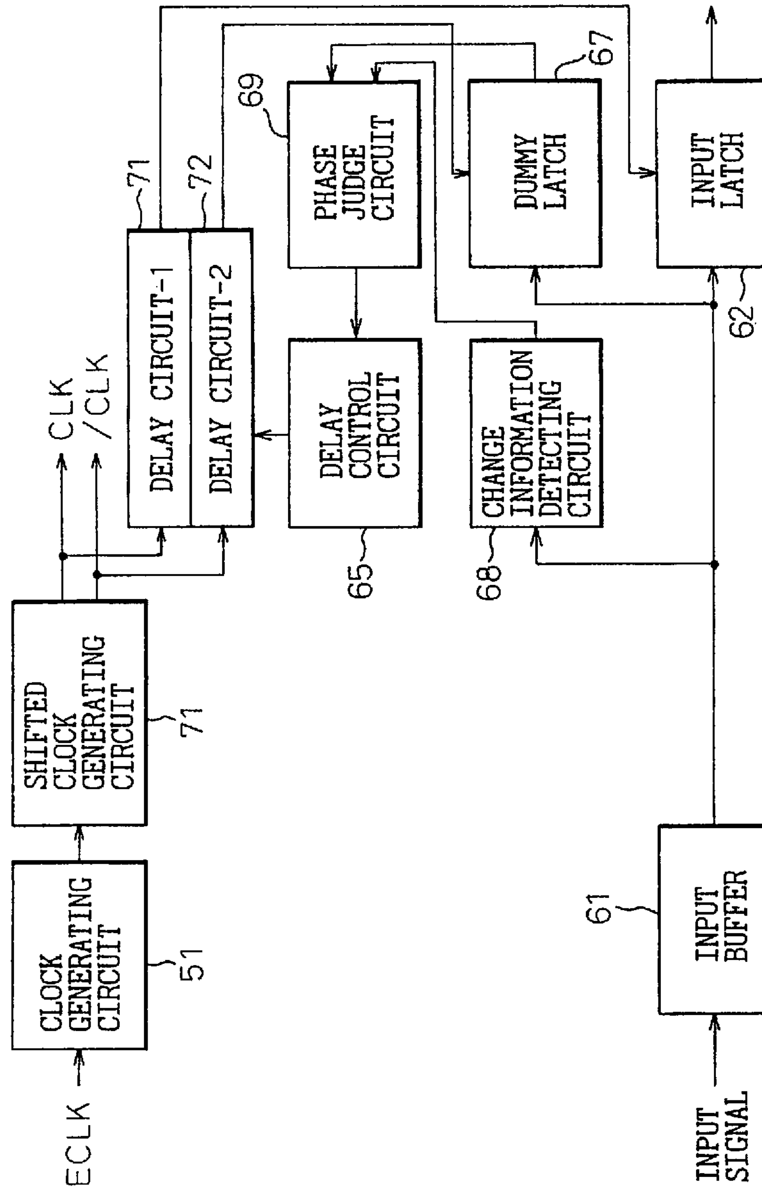


Fig.14

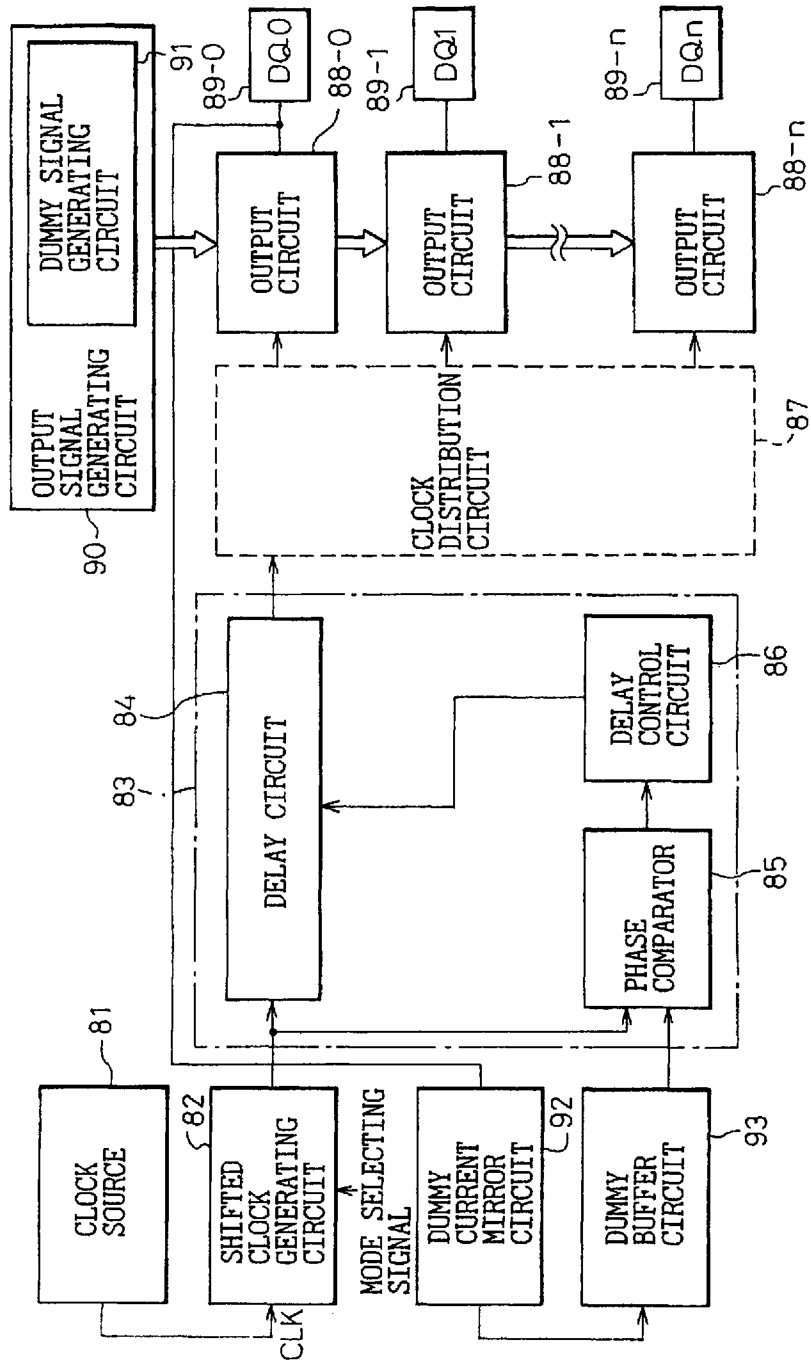


Fig.15
CLOCK SOURCE
81
SHIFTED CLOCK GENERATING CIRCUIT
82
CLK
MODE SELECTING SIGNAL
DUMMY CURRENT MIRROR CIRCUIT
92
DUMMY BUFFER CIRCUIT
93
DELAY CIRCUIT
84
83
PHASE COMPARATOR
85
DELAY CONTROL CIRCUIT
86
CLOCK DISTRIBUTION CIRCUIT
87
OUTPUT SIGNAL GENERATING CIRCUIT
90
DUMMY SIGNAL GENERATING CIRCUIT
91
OUTPUT CIRCUIT
88-0
OUTPUT CIRCUIT
88-1
OUTPUT CIRCUIT
88-n
DQ0
89-0
DQ1
89-1
DQn
89-n

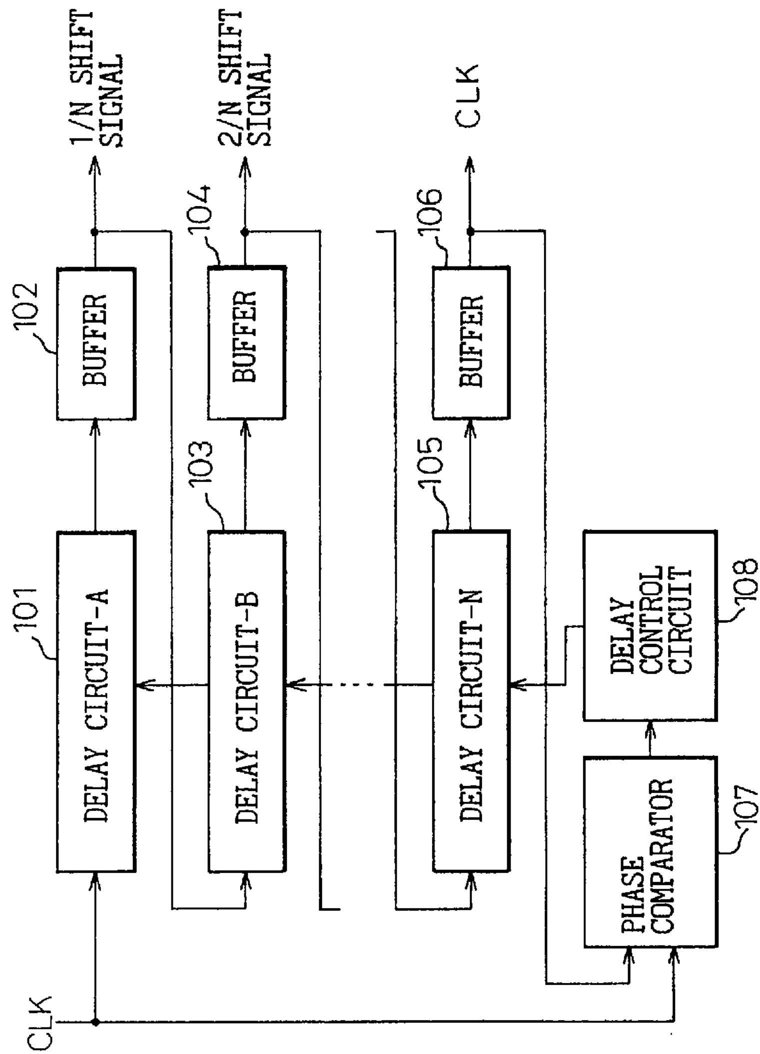


Fig.16
CLK
DELAY CIRCUIT-A
101
BUFFER
102
1/N SHIFT SIGNAL
DELAY CIRCUIT-B
103
BUFFER
104
2/N SHIFT SIGNAL
DELAY CIRCUIT-N
105
BUFFER
106
CLK
PHASE COMPARATOR
107
DELAY CONTROL CIRCUIT
108

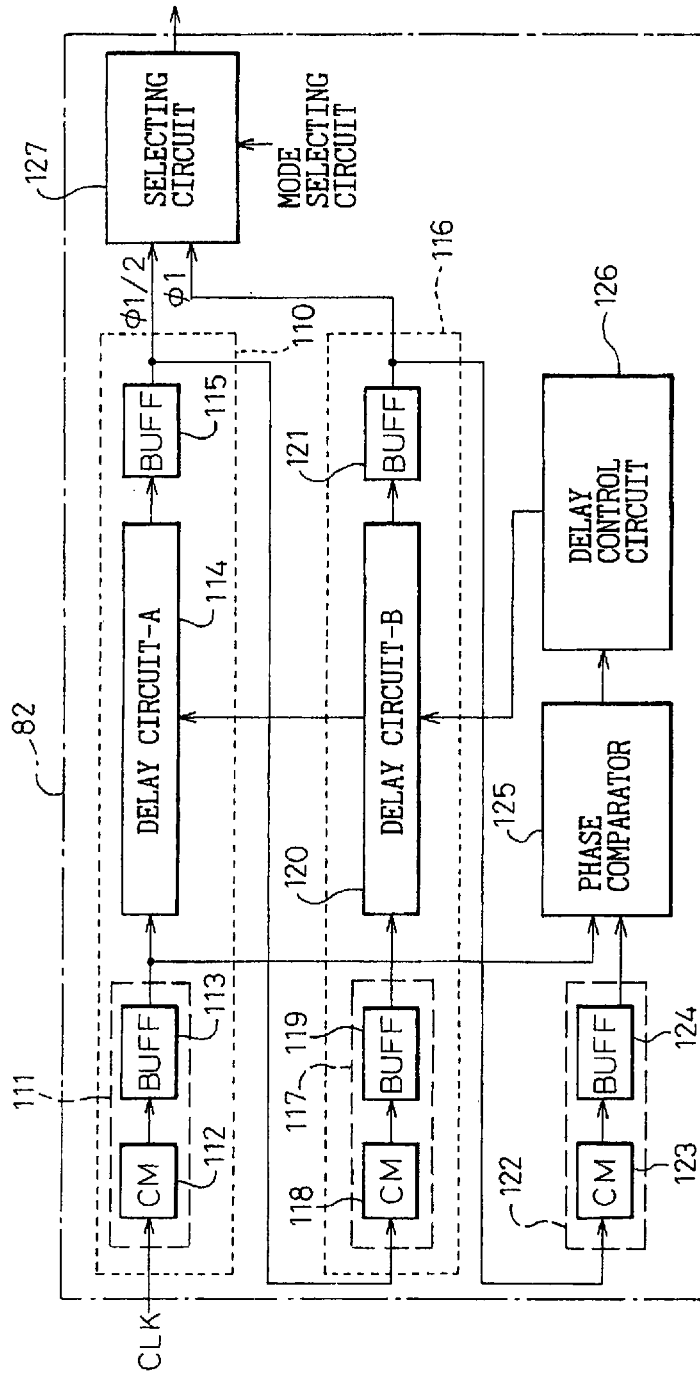


Fig.17

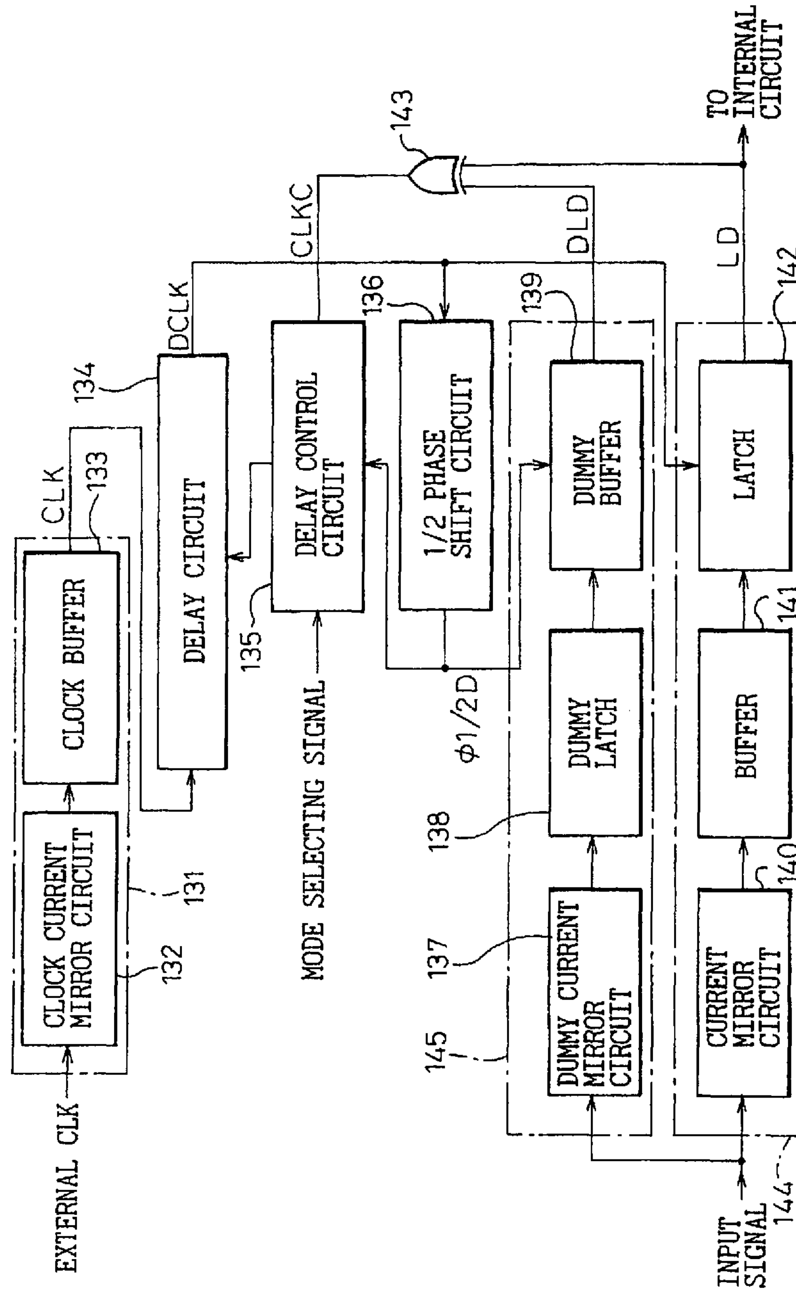


Fig.18
EXTERNAL CLK
CLOCK CURRENT MIRROR CIRCUIT
CLOCK BUFFER
CLK
DELAY CIRCUIT
DCLK
DELAY CONTROL CIRCUIT
CLKC
MODE SELECTING SIGNAL
1/2 PHASE SHIFT CIRCUIT
φ1/2D
DUMMY CURRENT MIRROR CIRCUIT
DUMMY LATCH
DUMMY BUFFER
DLD
CURRENT MIRROR CIRCUIT
BUFFER
LATCH
LD
INPUT SIGNAL
TO INTERNAL CIRCUIT
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145

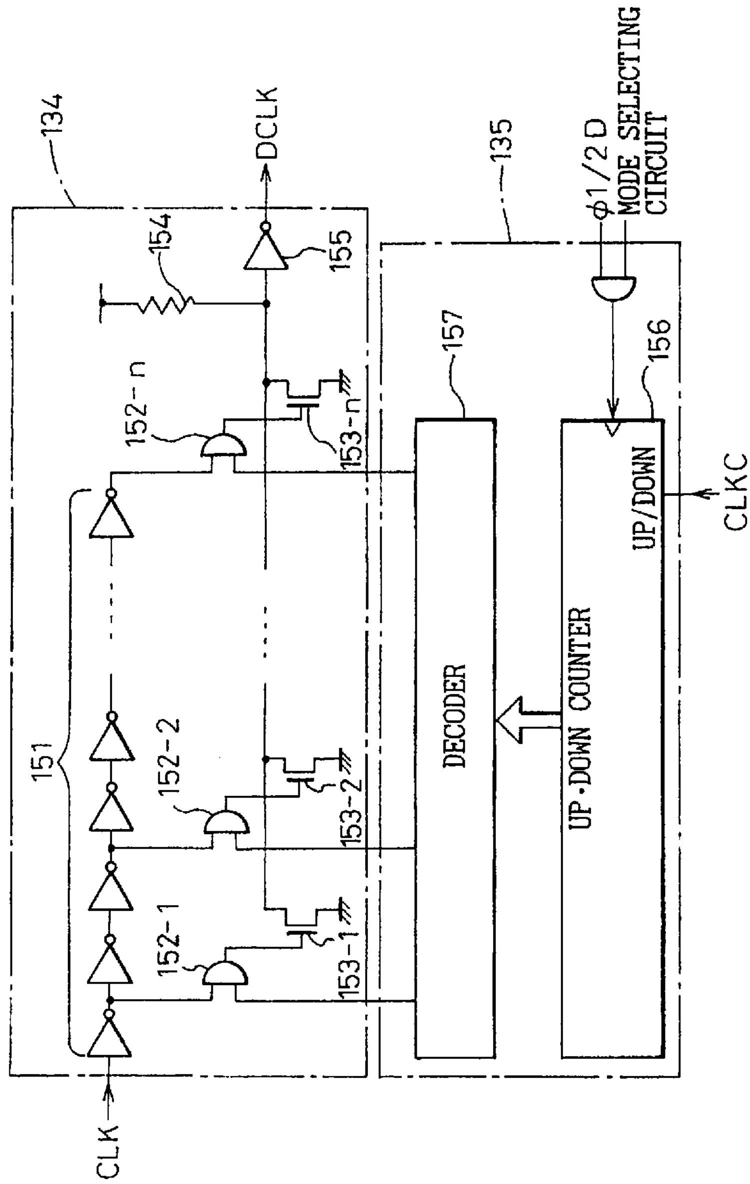


Fig.19
134
135
CLK
DCLK
151
152-1
152-2
152-n
153-1
153-2
153-n
154
155
156
157
DECODER
UP·DOWN COUNTER
UP/DOWN
CLKC
φ1/2 D
MODE SELECTING CIRCUIT

Fig.20

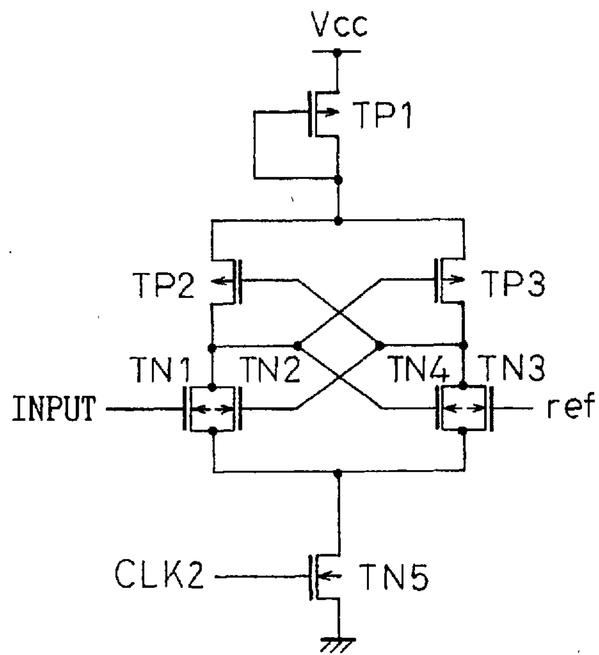


Fig.21

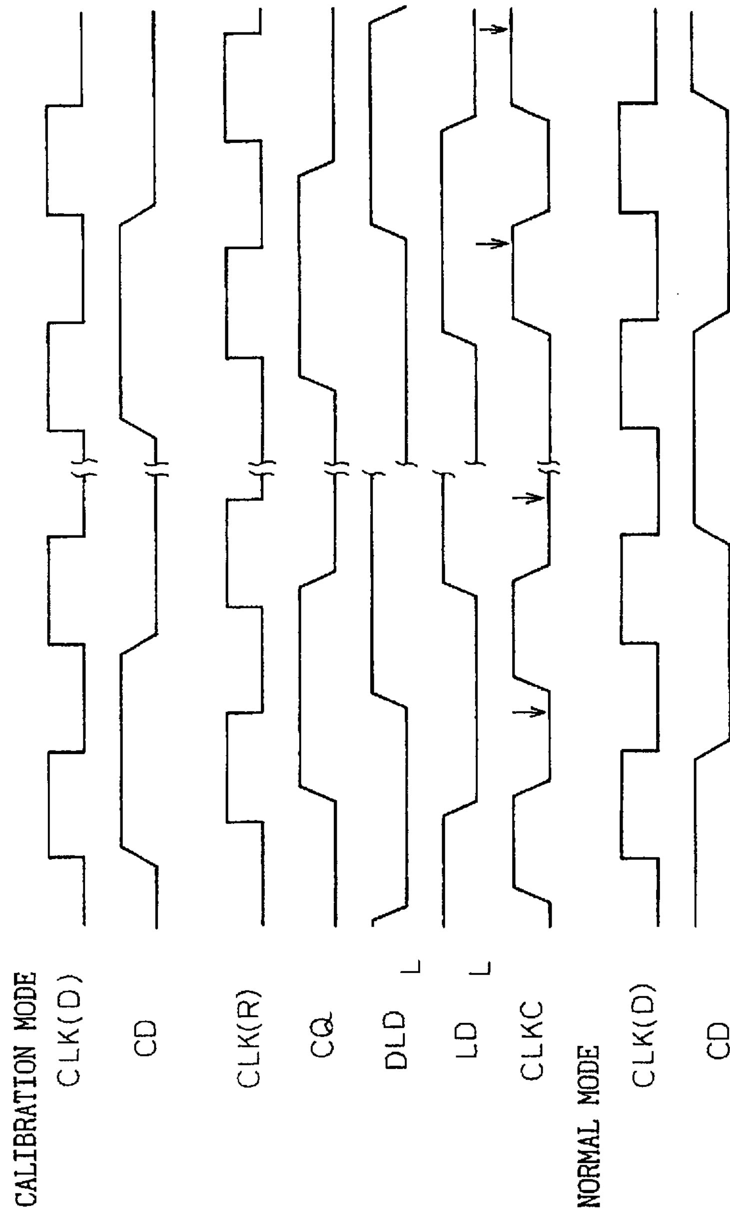
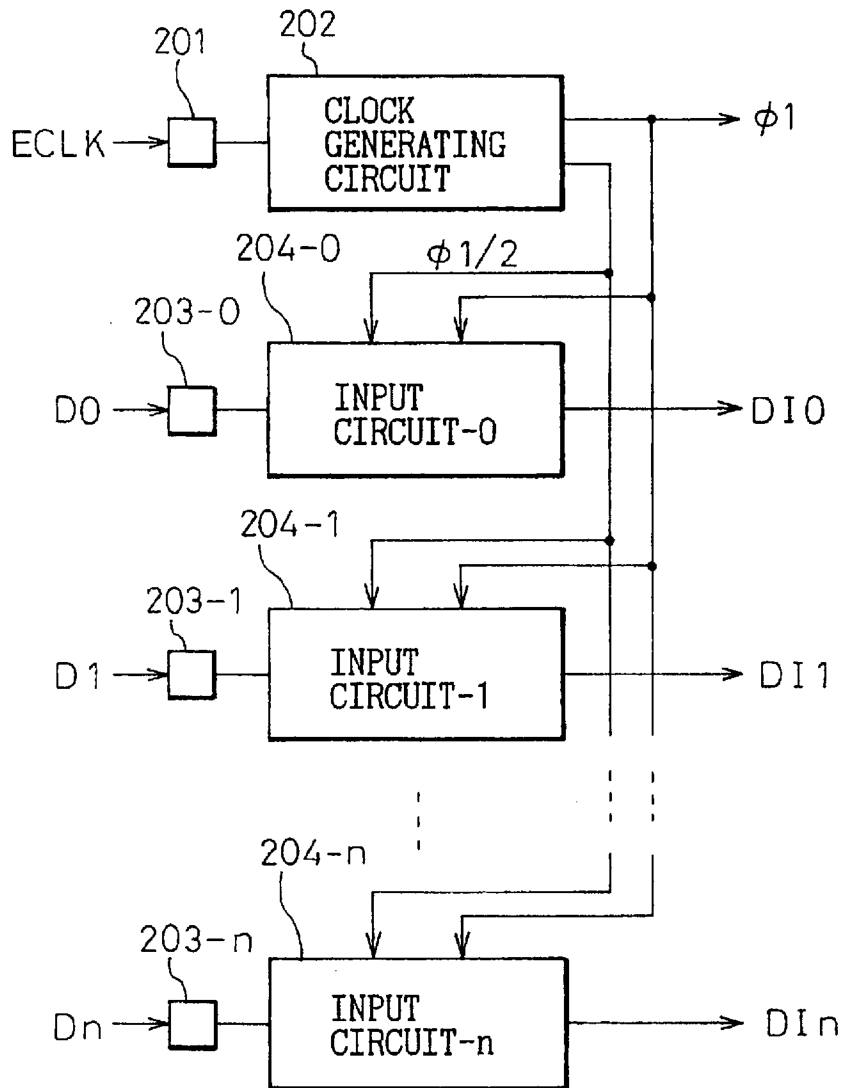


Fig.22



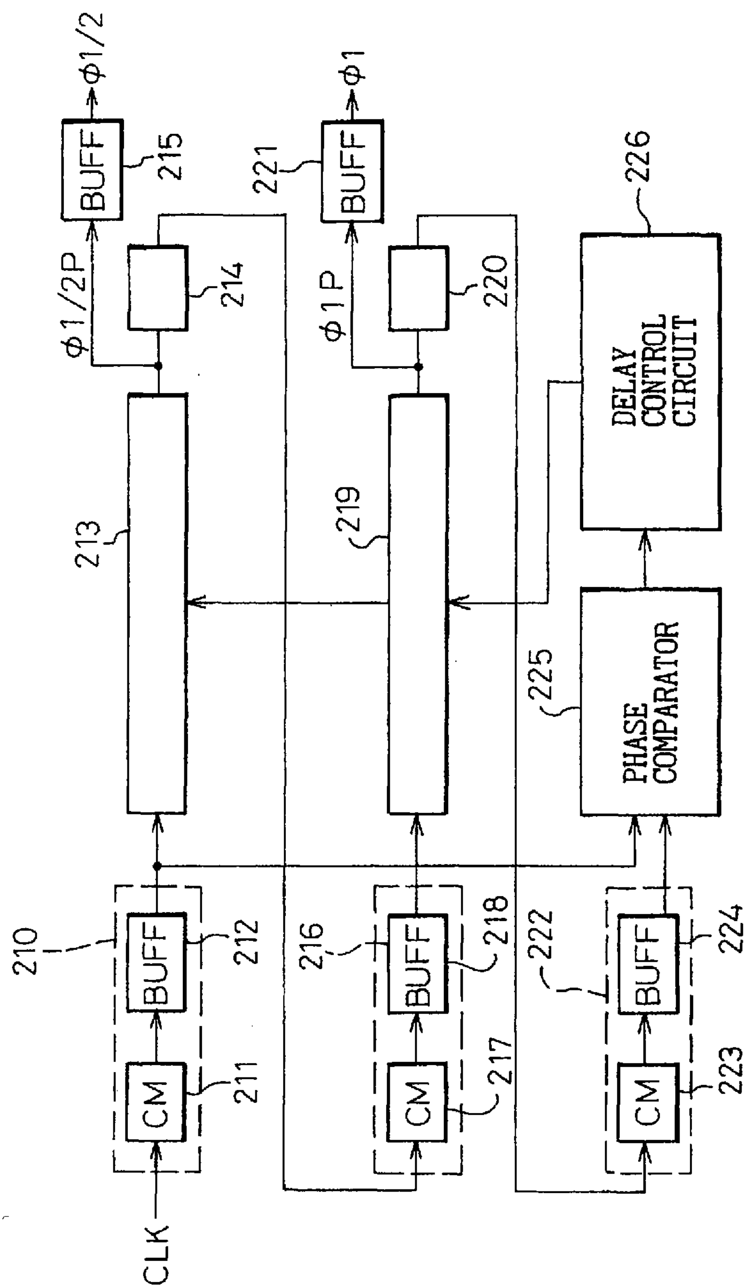


Fig.23
CLK
CM
BUFF
210
211
212
213
214
215
φ1/2P
φ1/2
216
217
218
219
220
221
φ1P
φ1
222
223
224
225
PHASE COMPARATOR
226
DELAY CONTROL CIRCUIT

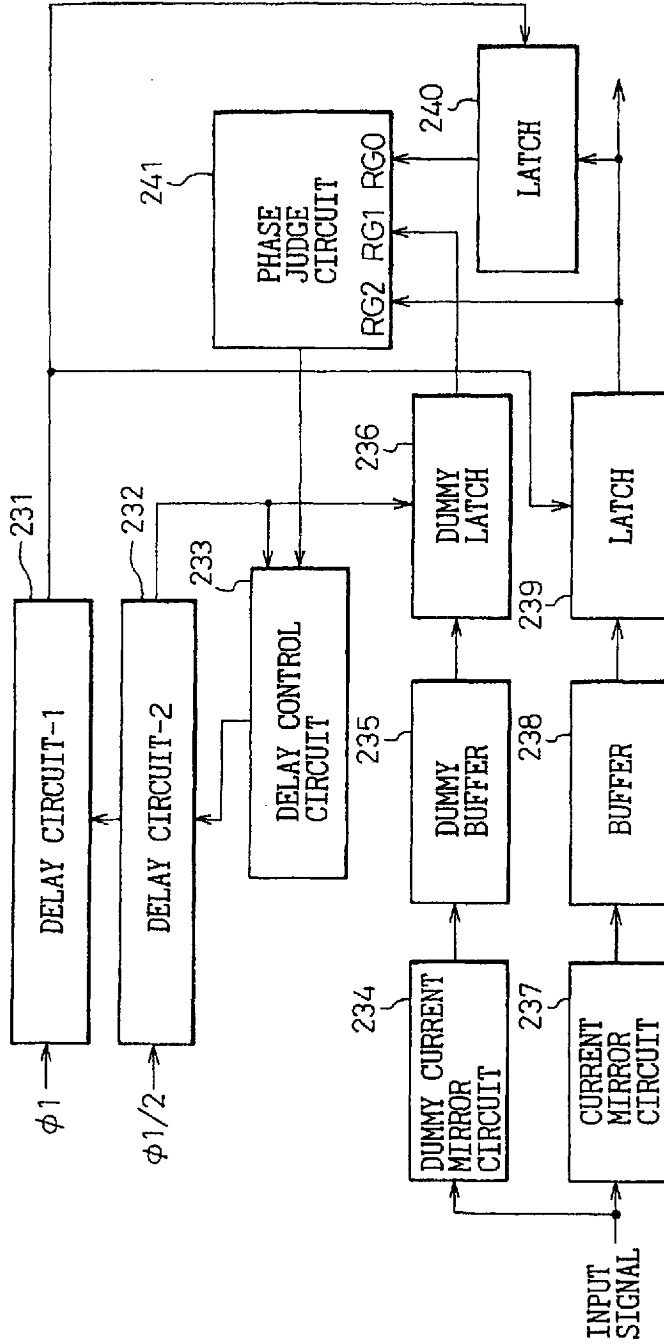


Fig.24
DELAY CIRCUIT-1
DELAY CIRCUIT-2
DELAY CONTROL CIRCUIT
PHASE JUDGE CIRCUIT
RG2 RG1 RG0
LATCH
DUMMY LATCH
LATCH
DUMMY BUFFER
BUFFER
DUMMY CURRENT MIRROR CIRCUIT
CURRENT MIRROR CIRCUIT
INPUT SIGNAL
φ1
φ1/2
231
232
233
234
235
236
237
238
239
240
241

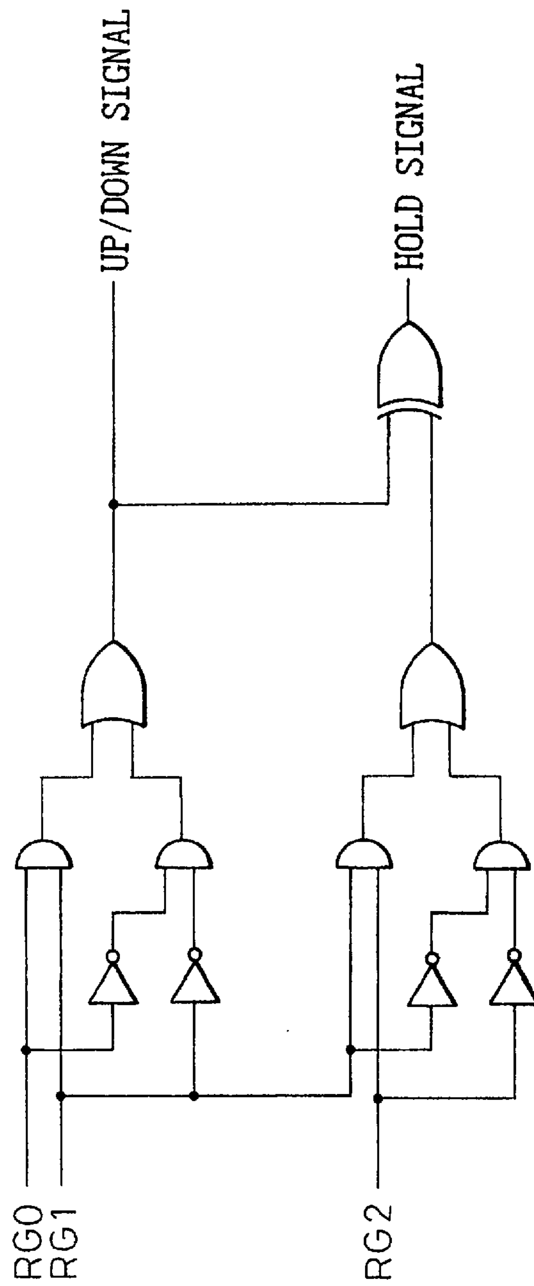


Fig.25

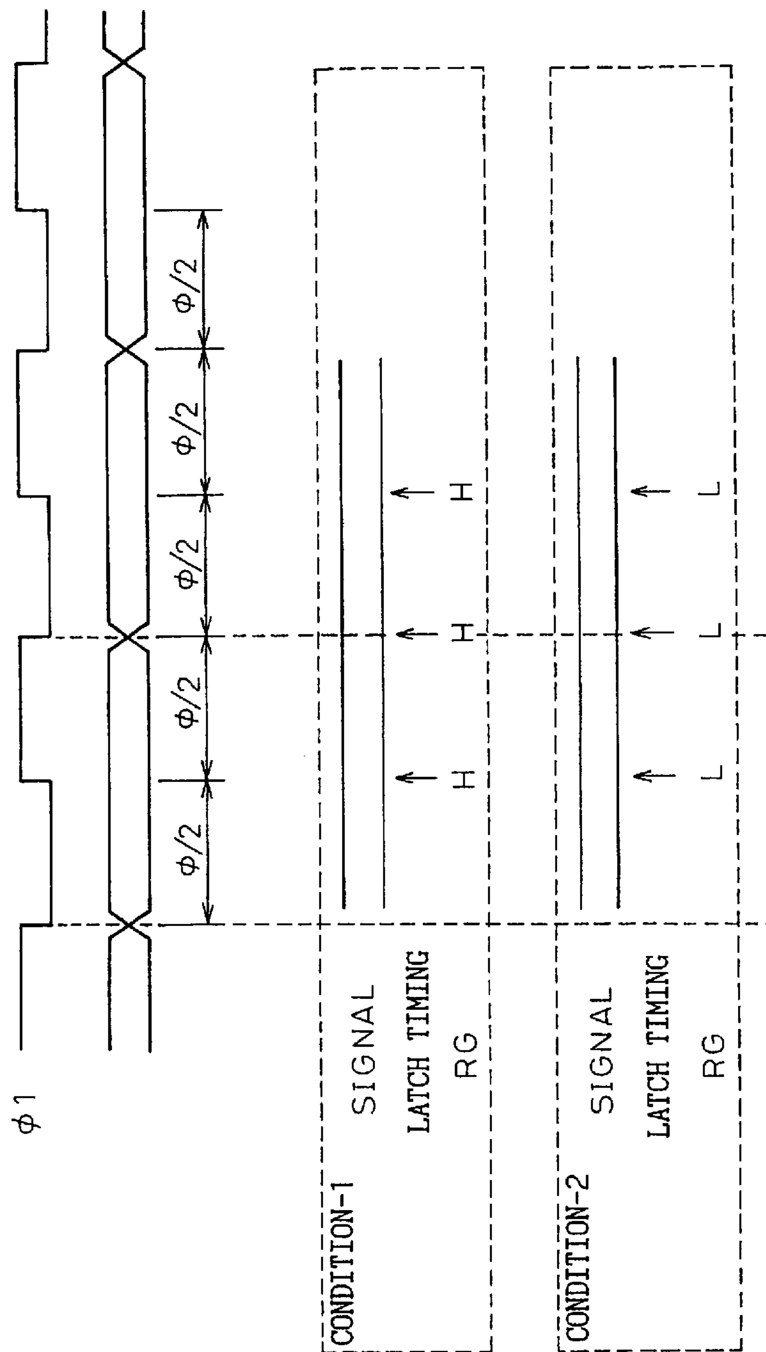
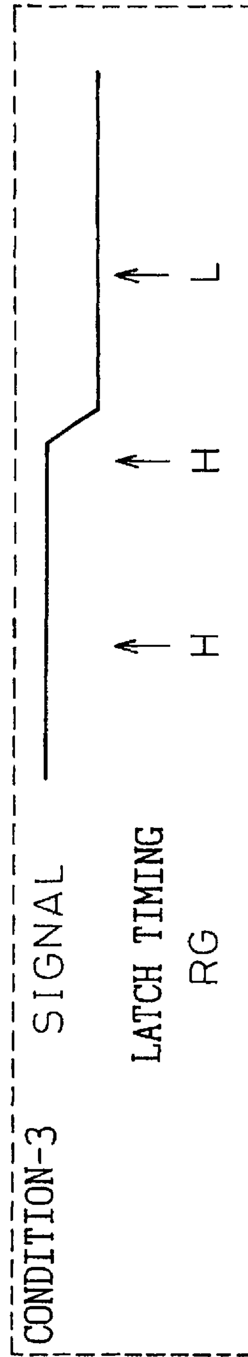


Fig.26

Fig.27



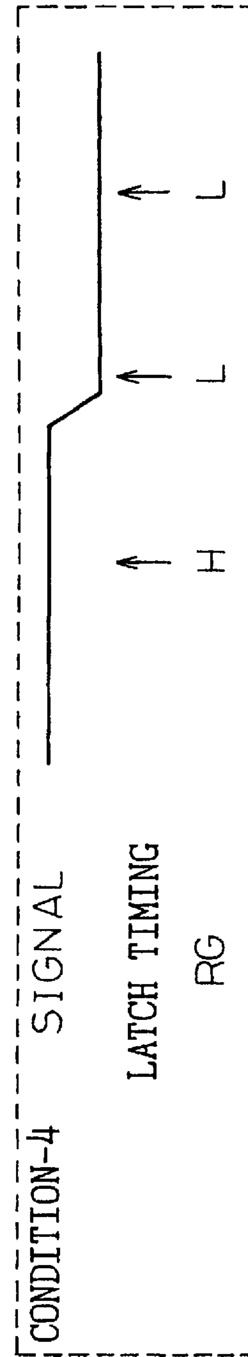
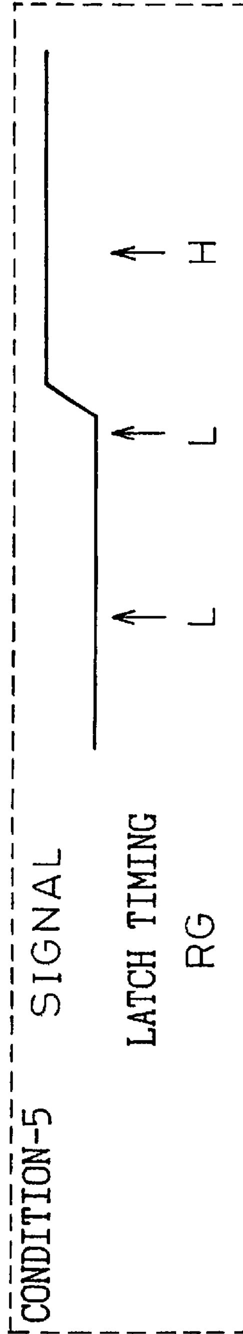


Fig.28



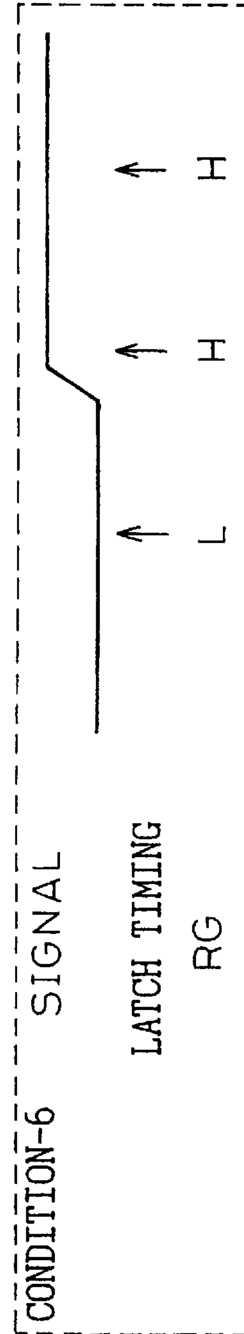


Fig.29

CONDITION	REGISTER			OPERATION
	RG0	RG1	RG2	
1	H	H	H	HOLD
2	L	L	L	
3	H	H	L	DELAY CLOCK
4	H	L	L	FORWARD CLOCK
5	L	L	H	DELAY CLOCK
6	L	H	H	FORWARD CLOCK

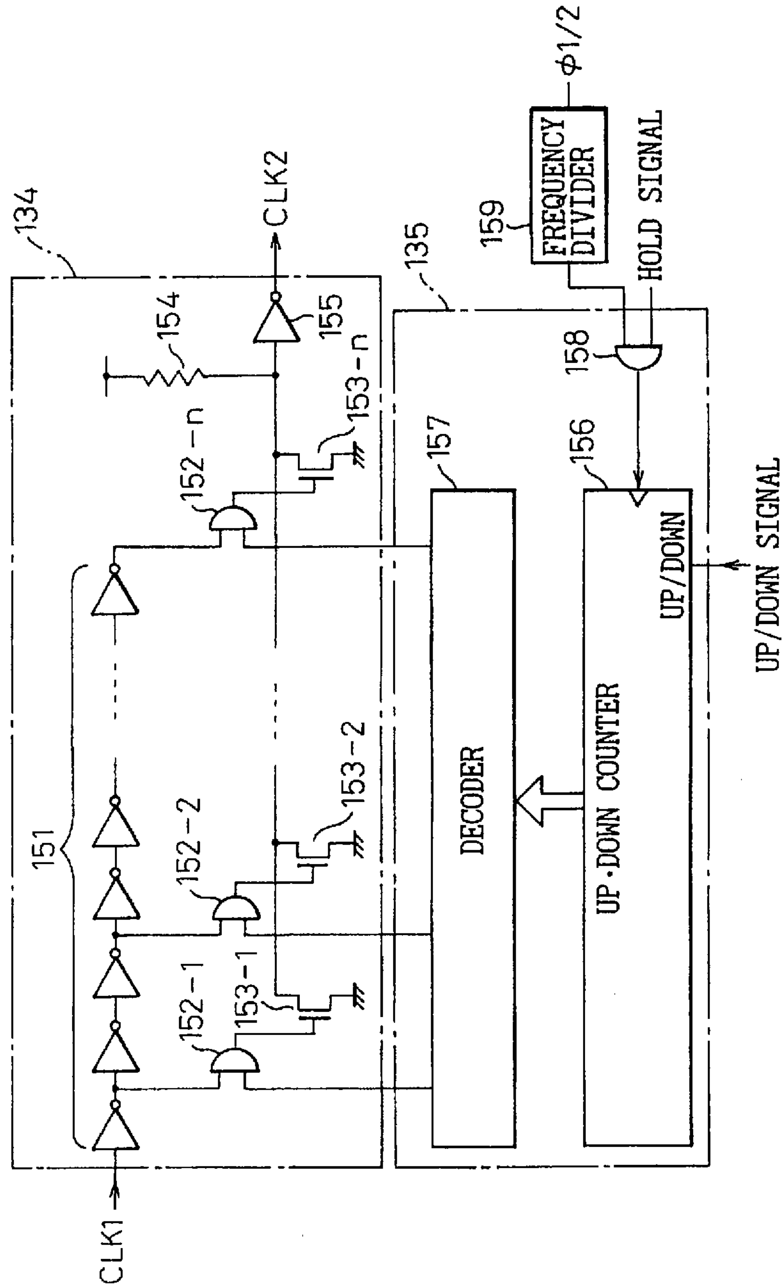


Fig.30
CLK1
CLK2
134
135
151
152-1
152-2
152-n
153-1
153-2
153-n
154
155
156
157
158
159
FREQUENCY DIVIDER
φ1/2
HOLD SIGNAL
DECODER
UP·DOWN COUNTER
UP/DOWN
UP/DOWN SIGNAL

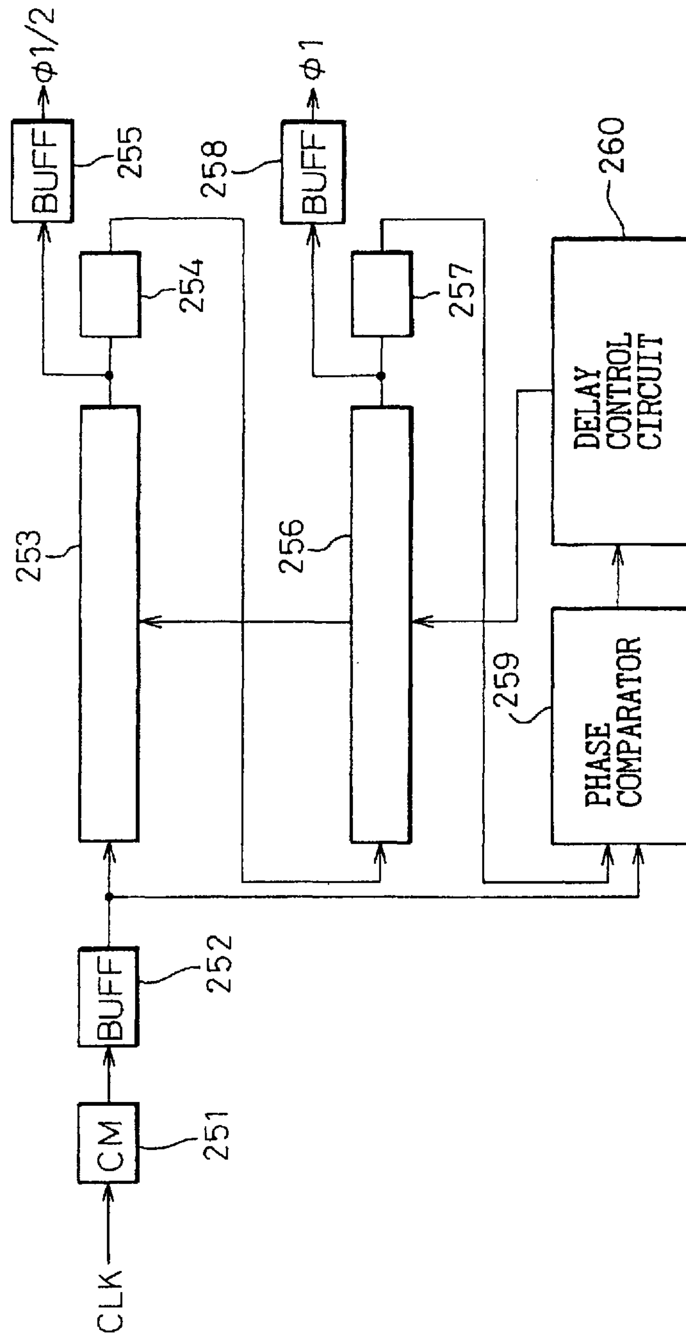


Fig.31

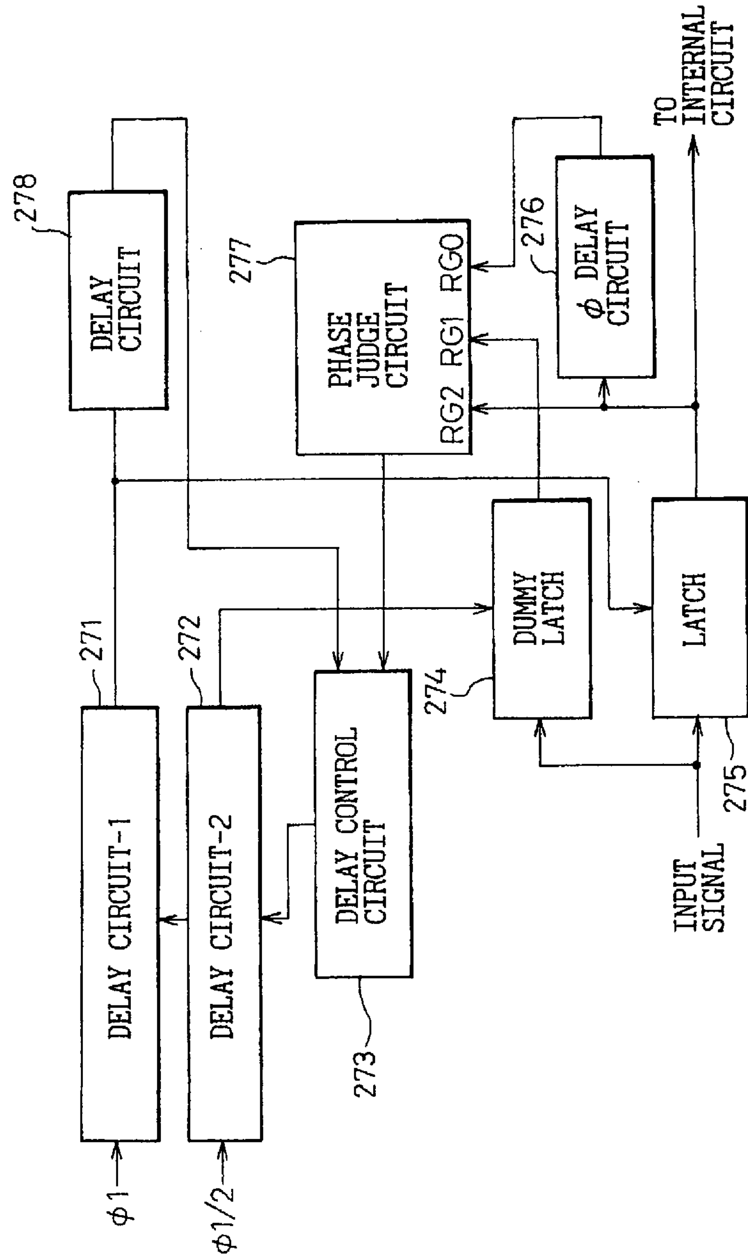


Fig.32
DELAY CIRCUIT
278
PHASE JUDGE CIRCUIT
277
RG2 RG1 RG0
276
φ DELAY CIRCUIT
TO INTERNAL CIRCUIT
271
272
DUMMY LATCH
LATCH
274
DELAY CONTROL CIRCUIT
DELAY CIRCUIT-1
DELAY CIRCUIT-2
273
275
INPUT SIGNAL
φ1
φ1/2

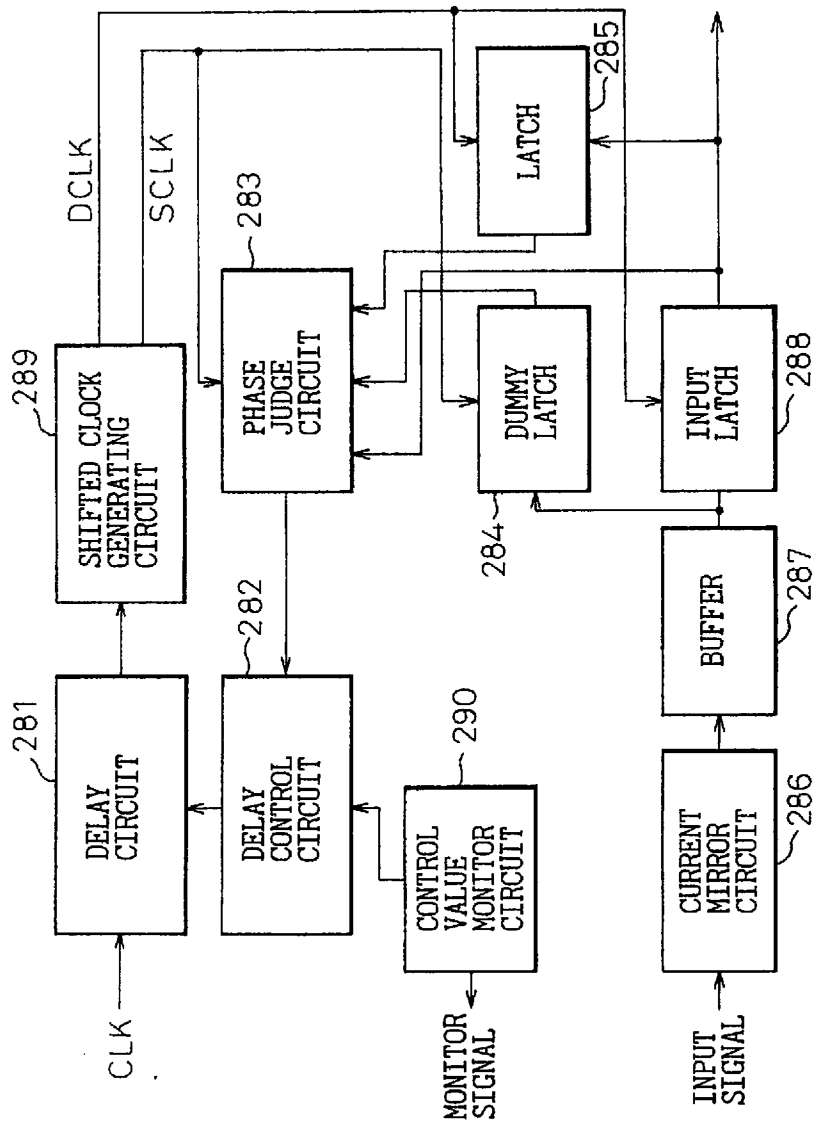


Fig.33
CLK
DELAY CIRCUIT
281
SHIFTED CLOCK GENERATING CIRCUIT
289
DCLK
SCLK
DELAY CONTROL CIRCUIT
282
PHASE JUDGE CIRCUIT
283
CONTROL VALUE MONITOR CIRCUIT
290
MONITOR SIGNAL
DUMMY LATCH
284
LATCH
285
INPUT SIGNAL
CURRENT MIRROR CIRCUIT
286
BUFFER
287
INPUT LATCH
288

Fig.34

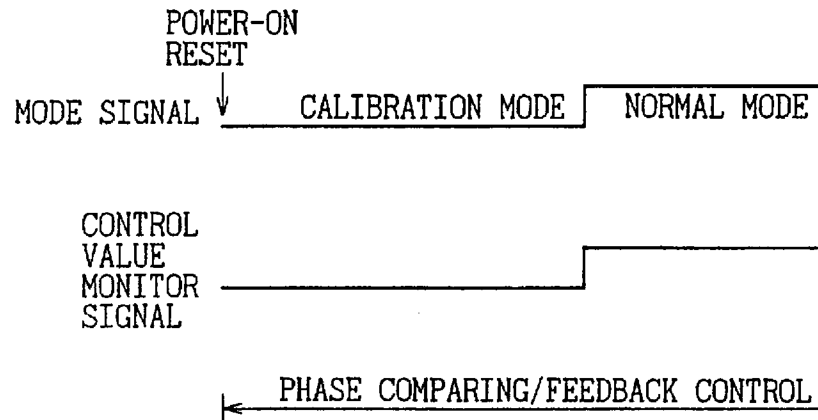
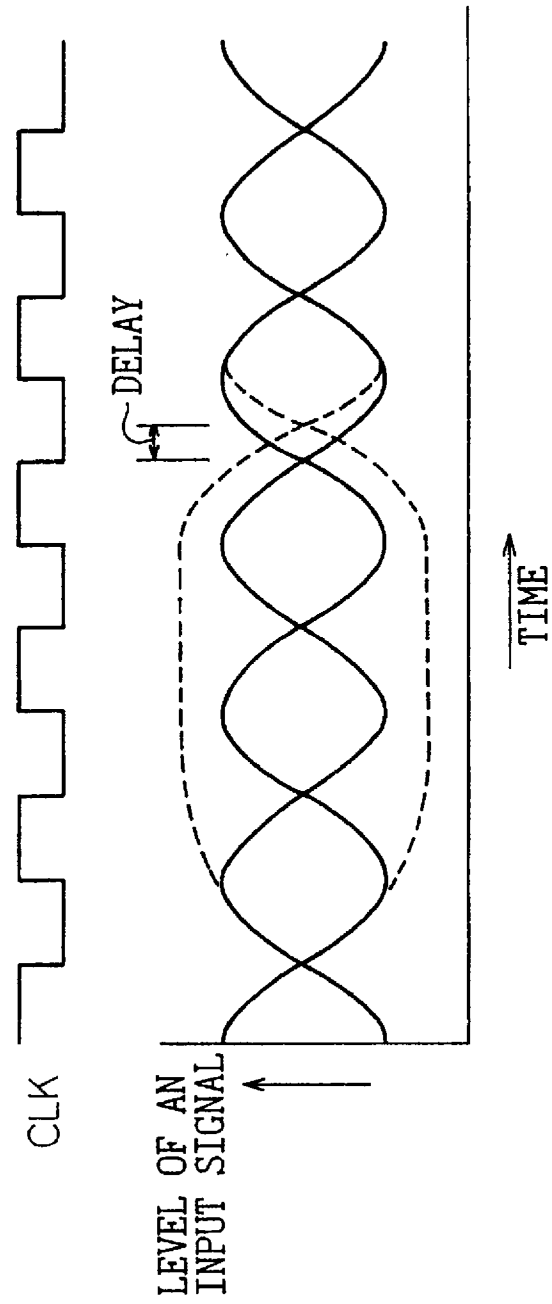


Fig.35



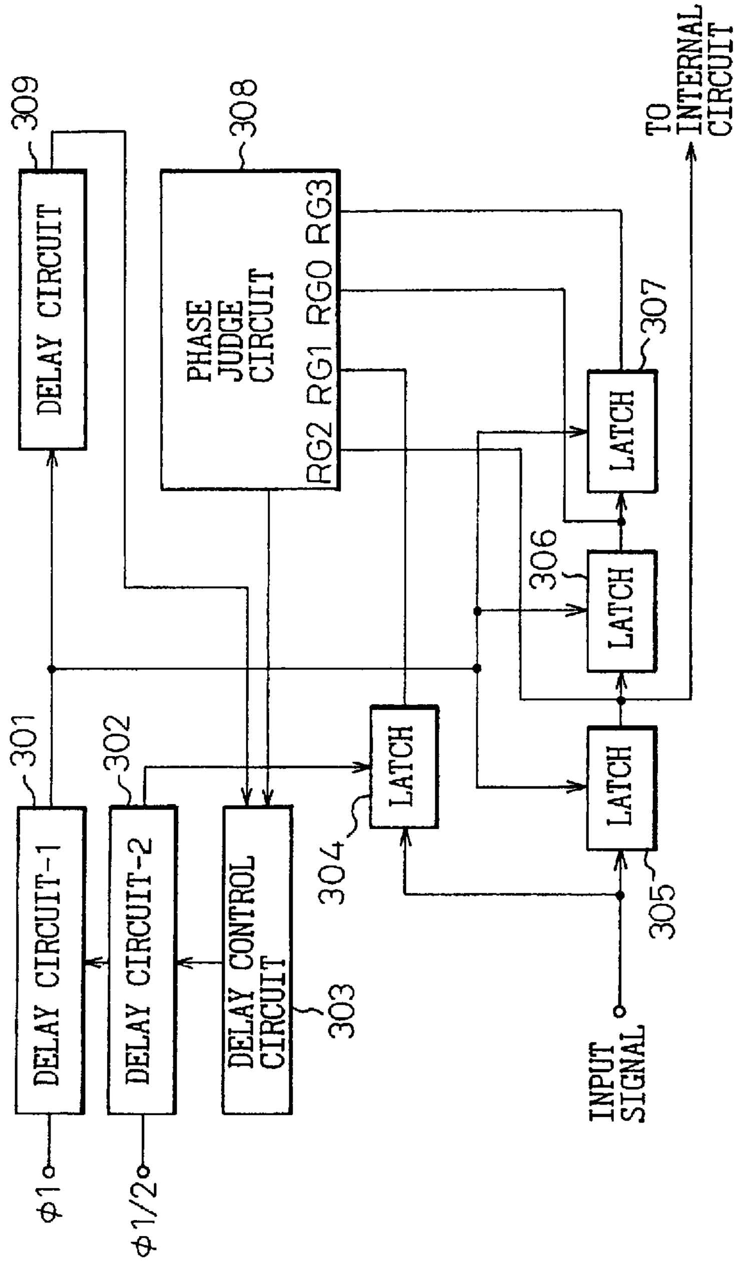


Fig.36
DELAY CIRCUIT-1
301
DELAY CIRCUIT-2
302
DELAY CONTROL CIRCUIT
303
LATCH
304
LATCH
305
LATCH
306
LATCH
307
PHASE JUDGE CIRCUIT
308
RG2 RG1 RG0 RG3
DELAY CIRCUIT
309
φ1
φ1/2
INPUT SIGNAL
TO INTERNAL CIRCUIT

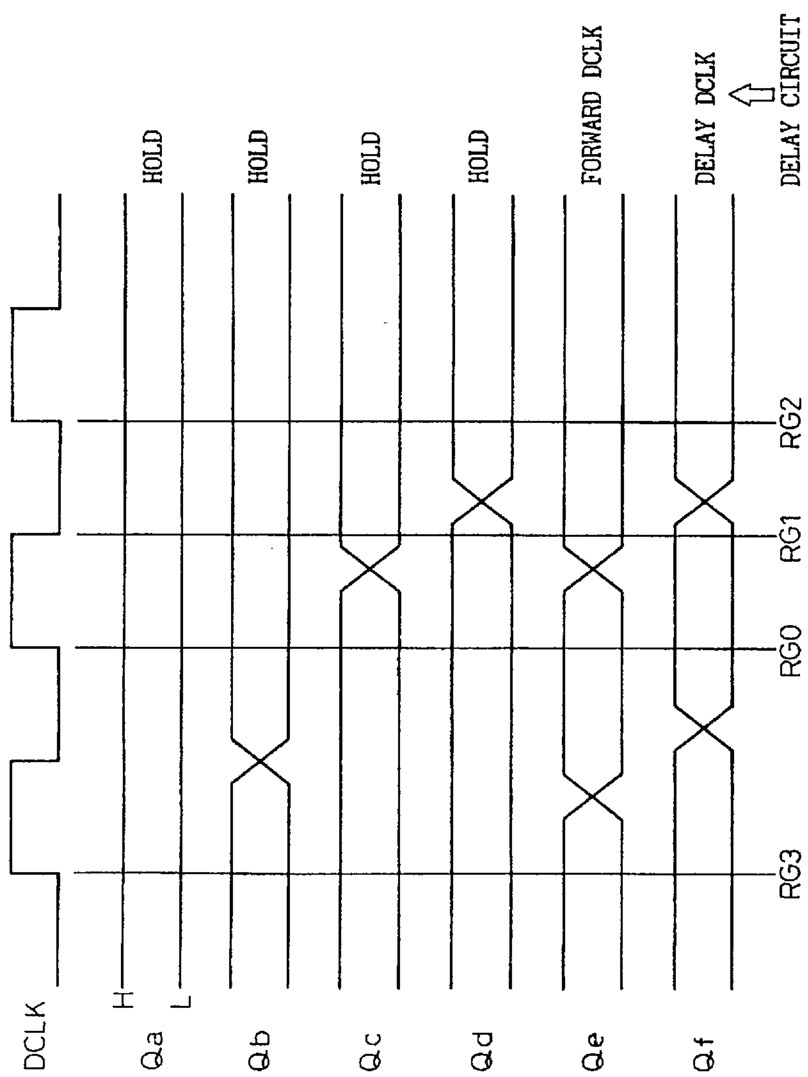


Fig.37

Fig.38

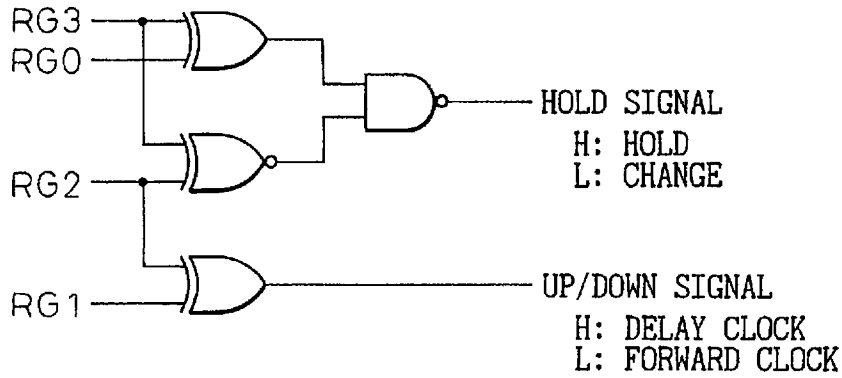


Fig.39

CONDITION	REGISTER				OPERATION
	RG3	RG0	RG1	RG2	
Qa-1	H	H	H	H	HOLD
Qa-2	L	L	L	L	
Qb-1	H	L	L	L	
Qb-2	L	H	H	H	
Qc-1	H	H	L	L	
Qc-2	L	L	H	H	
Qd-1	H	H	H	L	
Qd-2	L	L	L	H	
Qe-1	H	L	H	H	FORWARD CLOCK
Qe-2	L	H	L	L	
Qf-1	H	L	L	H	DELAY CLOCK
Qf-2	L	H	H	L	

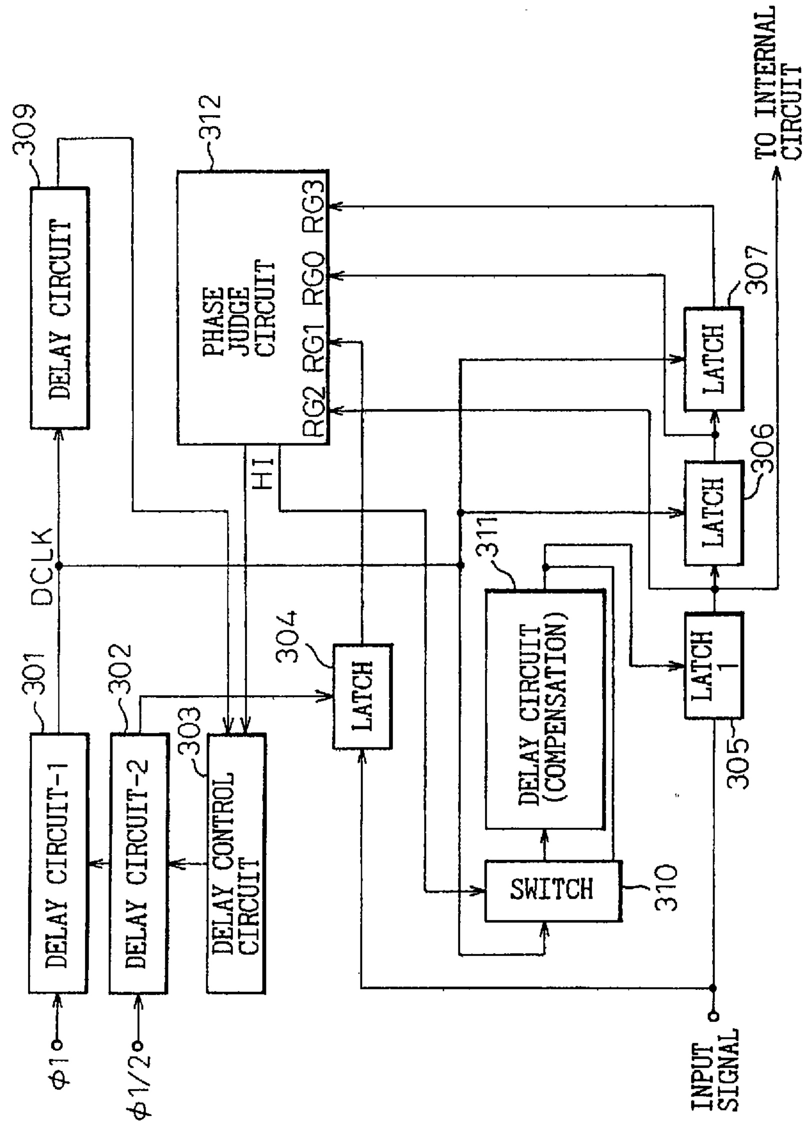


Fig.40
DELAY CIRCUIT-1
DELAY CIRCUIT-2
DELAY CONTROL CIRCUIT
DELAY CIRCUIT
PHASE JUDGE CIRCUIT
RG2 RG1 RG0 RG3
HI
DCLK
LATCH
SWITCH
DELAY CIRCUIT (COMPENSATION)
LATCH 1
TO INTERNAL CIRCUIT
INPUT SIGNAL
φ1
φ1/2
301
302
303
304
305
306
307
309
310
311
312

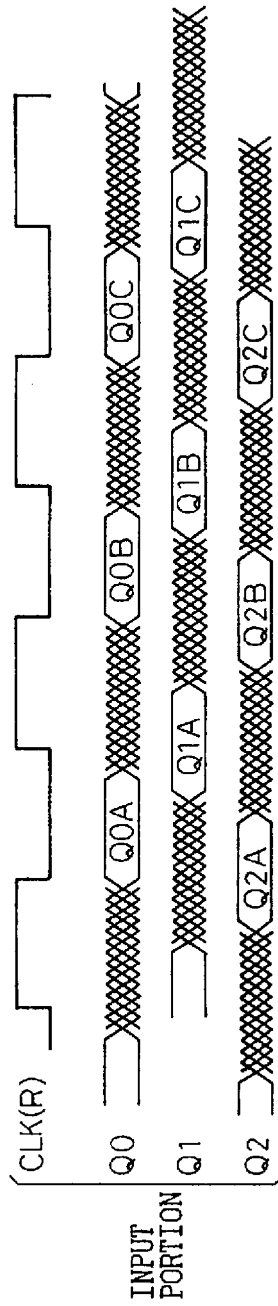
Fig.41

Fig.42

Fig.43

<table>
<tr><th rowspan="2">CONDITION</th><th colspan="4">REGISTER</th><th rowspan="2">OPERATION</th><th rowspan="2">COMPENSATION CONTROL SIGNAL (H1)</th></tr>
<tr><th>RG3</th><th>RG0</th><th>RG1</th><th>RG2</th></tr>
<tr><td>Qa−1</td><td>H</td><td>H</td><td>H</td><td>H</td><td rowspan="8">HOLD</td><td rowspan="2">ADD (H)</td></tr>
<tr><td>Qa−2</td><td>L</td><td>L</td><td>L</td><td>L</td></tr>
<tr><td>Qb−1</td><td>H</td><td>L</td><td>L</td><td>L</td><td rowspan="2">NOT ADD (L)</td></tr>
<tr><td>Qb−2</td><td>L</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>Qc−1</td><td>H</td><td>H</td><td>L</td><td>L</td><td rowspan="4">ADD (H)</td></tr>
<tr><td>Qc−2</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>Qd−1</td><td>H</td><td>H</td><td>H</td><td>L</td></tr>
<tr><td>Qd−2</td><td>L</td><td>L</td><td>L</td><td>H</td></tr>
<tr><td>Qe−1</td><td>H</td><td>L</td><td>H</td><td>H</td><td rowspan="2">FORWARD CLOCK</td><td rowspan="4">NOT ADD (L)</td></tr>
<tr><td>Qe−2</td><td>L</td><td>H</td><td>L</td><td>L</td></tr>
<tr><td>Qf−1</td><td>H</td><td>L</td><td>L</td><td>H</td><td rowspan="2">DELAY CLOCK</td></tr>
<tr><td>Qf−2</td><td>L</td><td>H</td><td>H</td><td>L</td></tr>
</table>

Fig. 44



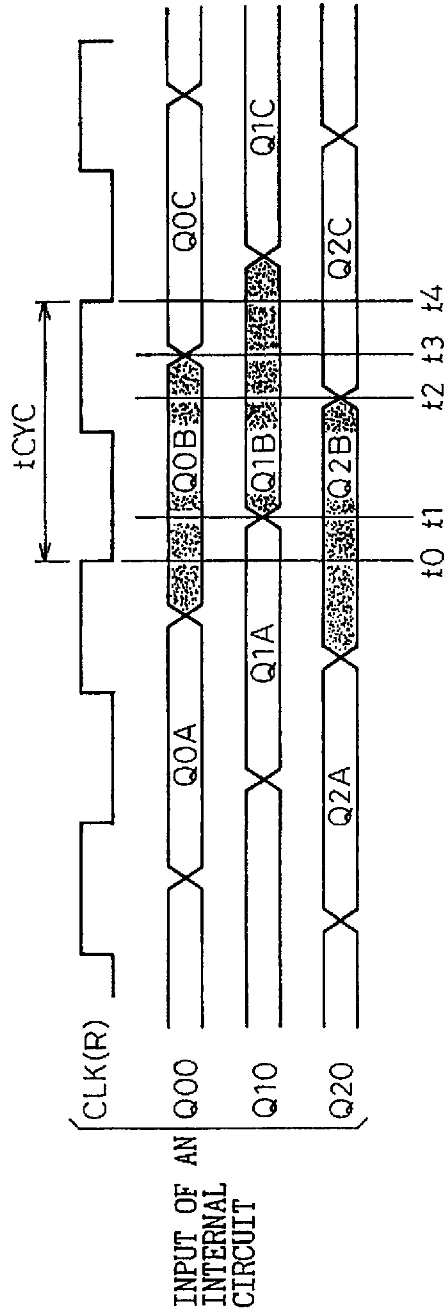
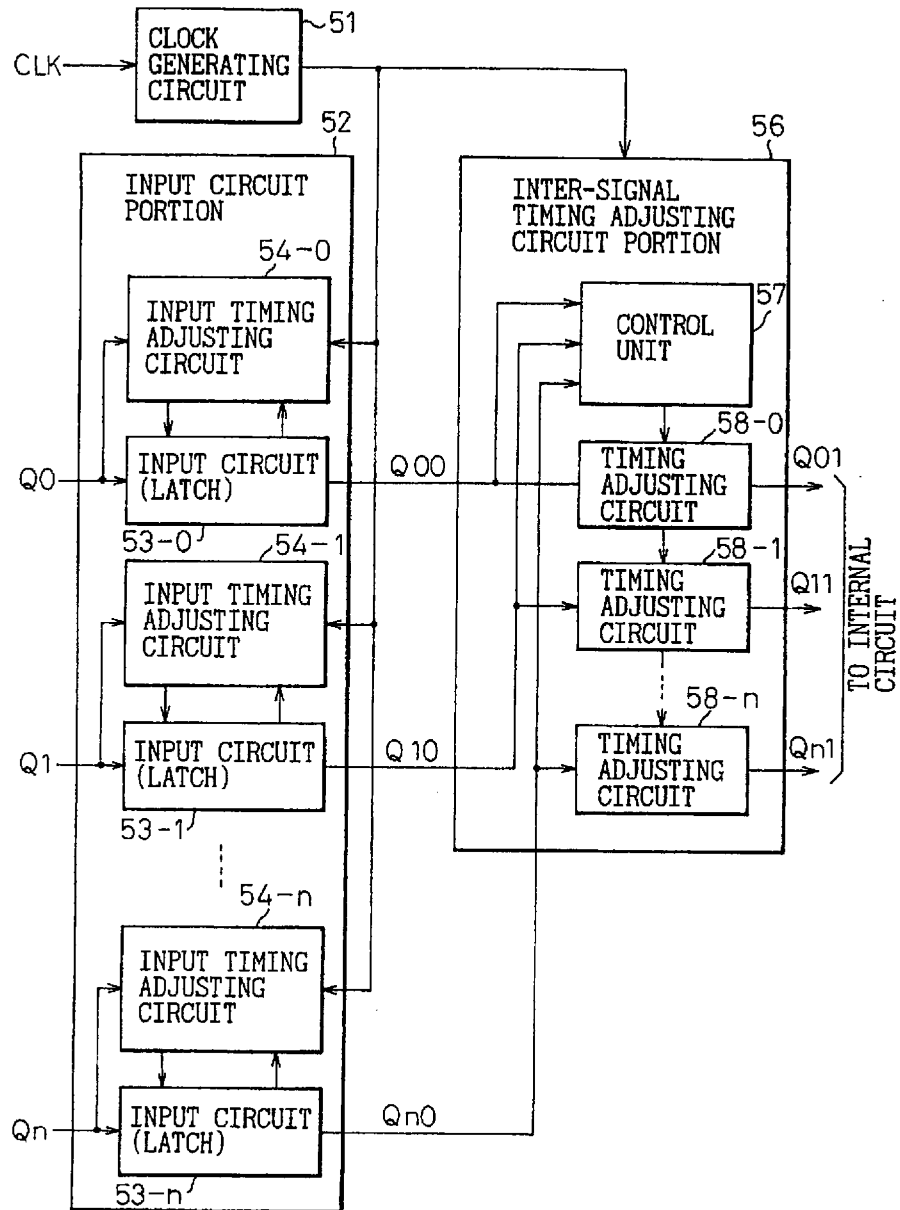


Fig.45

	t_0-t_1	t_1-t_2	t_2-t_3	t_3-t_4	
Q0	Q0B	Q0B	Q0B	Q0C	
Q1	Q1A	Q1B	Q1B	Q1B	
Q2	Q2B	Q2B	Q2C	Q2C	

Fig.46



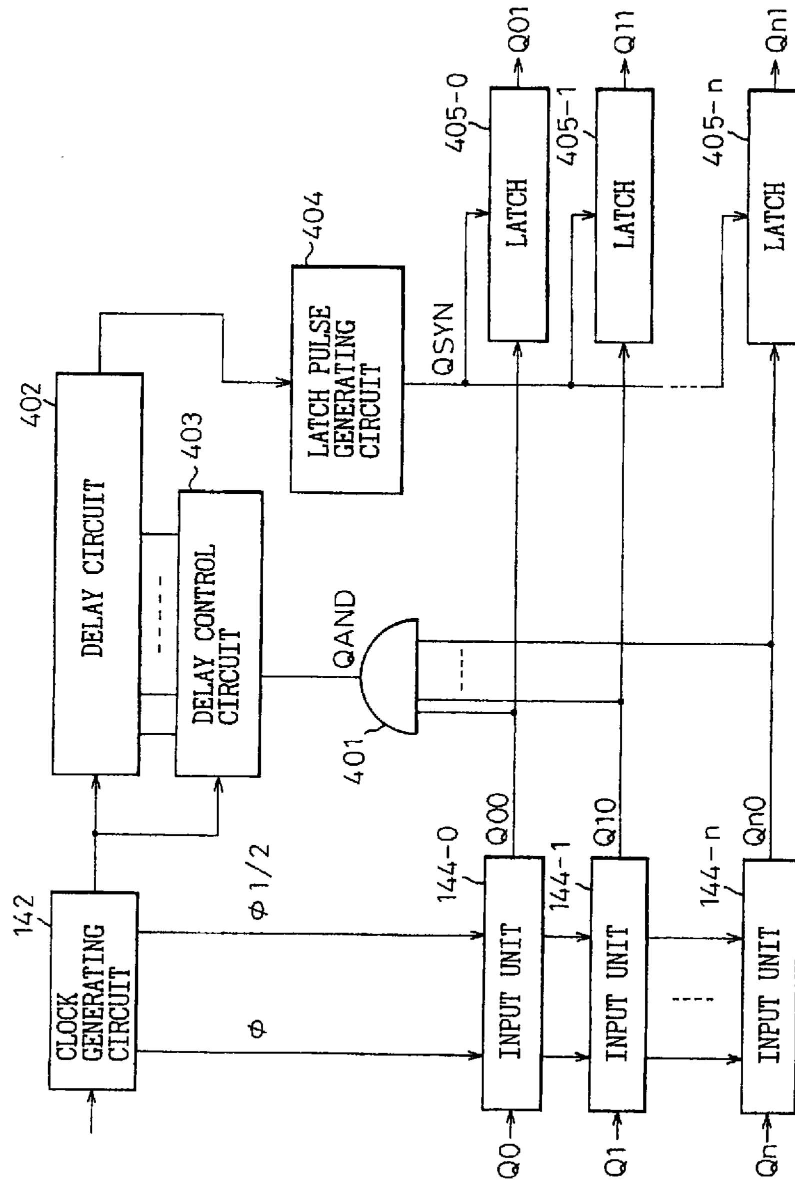


Fig.47
142
CLOCK GENERATING CIRCUIT
φ1/2
φ
402
DELAY CIRCUIT
403
DELAY CONTROL CIRCUIT
404
LATCH PULSE GENERATING CIRCUIT
QSYN
QAND
401
144-0
144-1
144-n
INPUT UNIT
INPUT UNIT
INPUT UNIT
Q0
Q1
Qn
Q00
Q10
Qn0
405-0
405-1
405-n
LATCH
LATCH
LATCH
Q01
Q11
Qn1

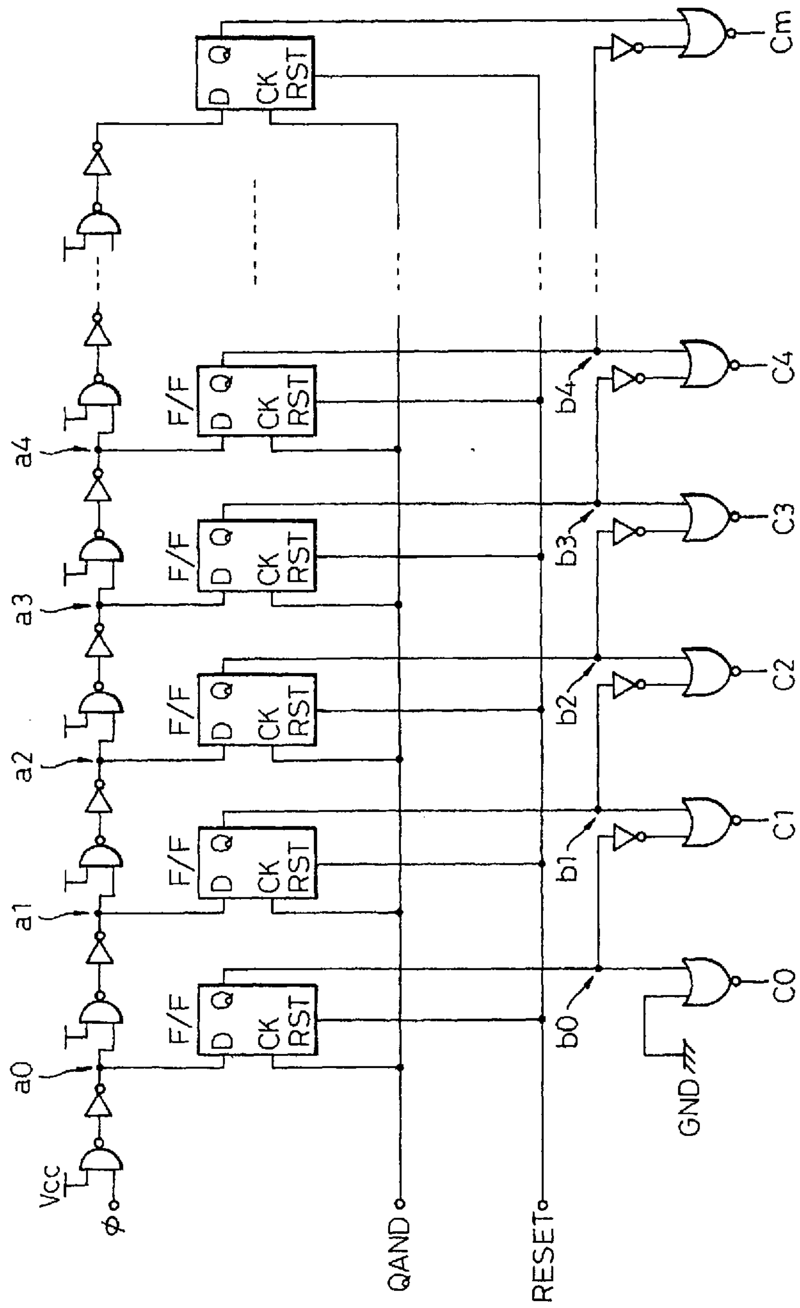


Fig. 48

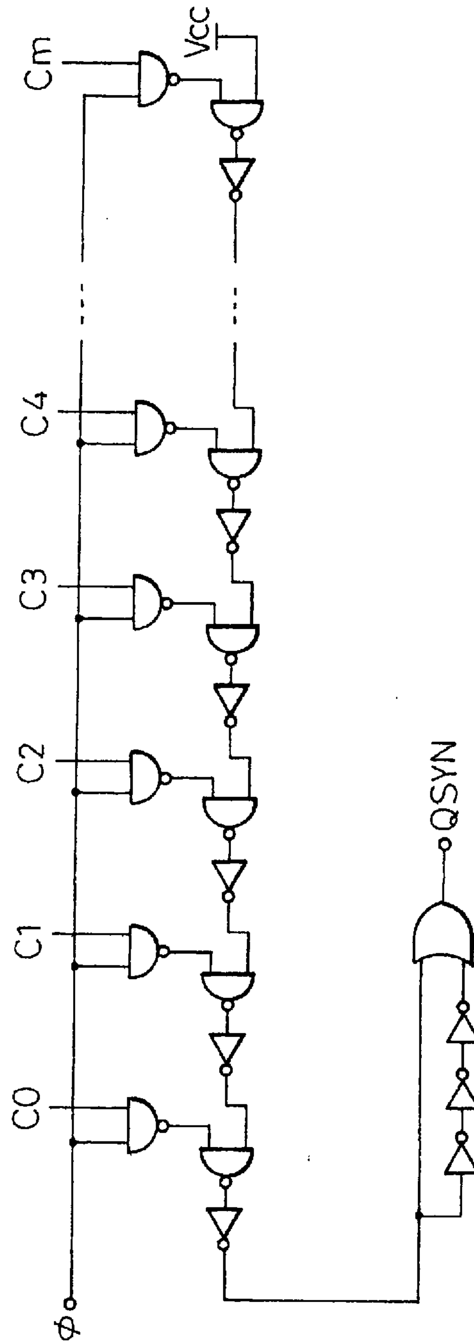


Fig.49

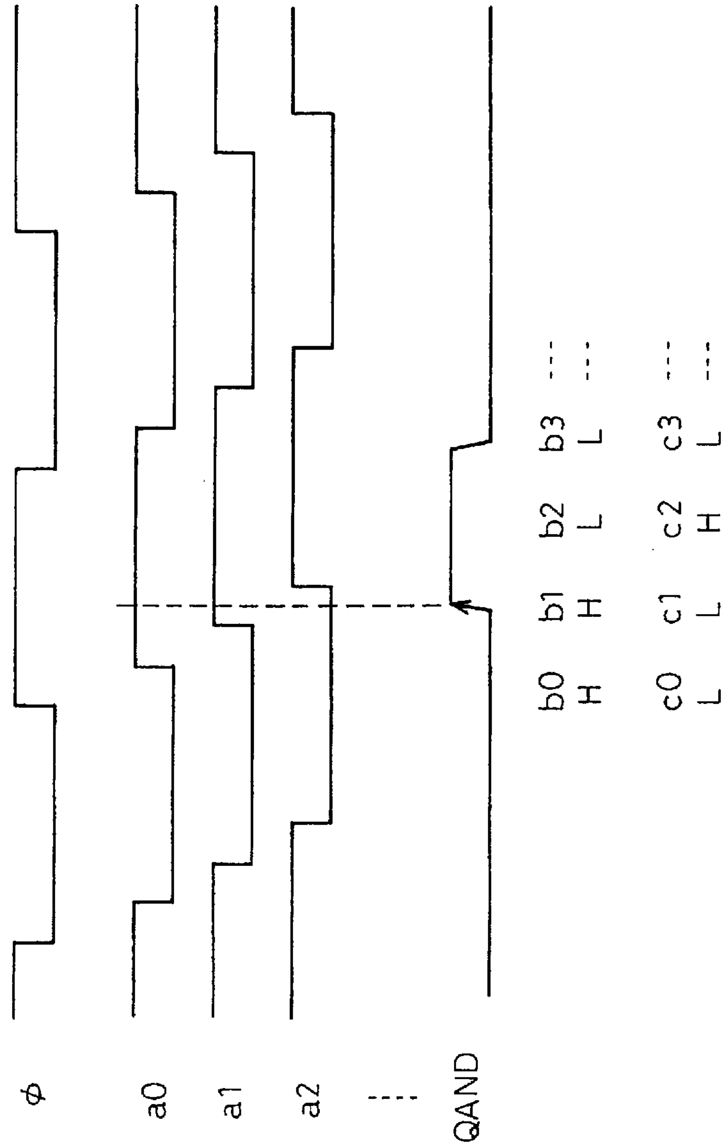


Fig.50
φ
a0
a1
a2
QAND
b0 H
b1 H
b2 L
b3 L
c0 L
c1 L
c2 H
c3 L

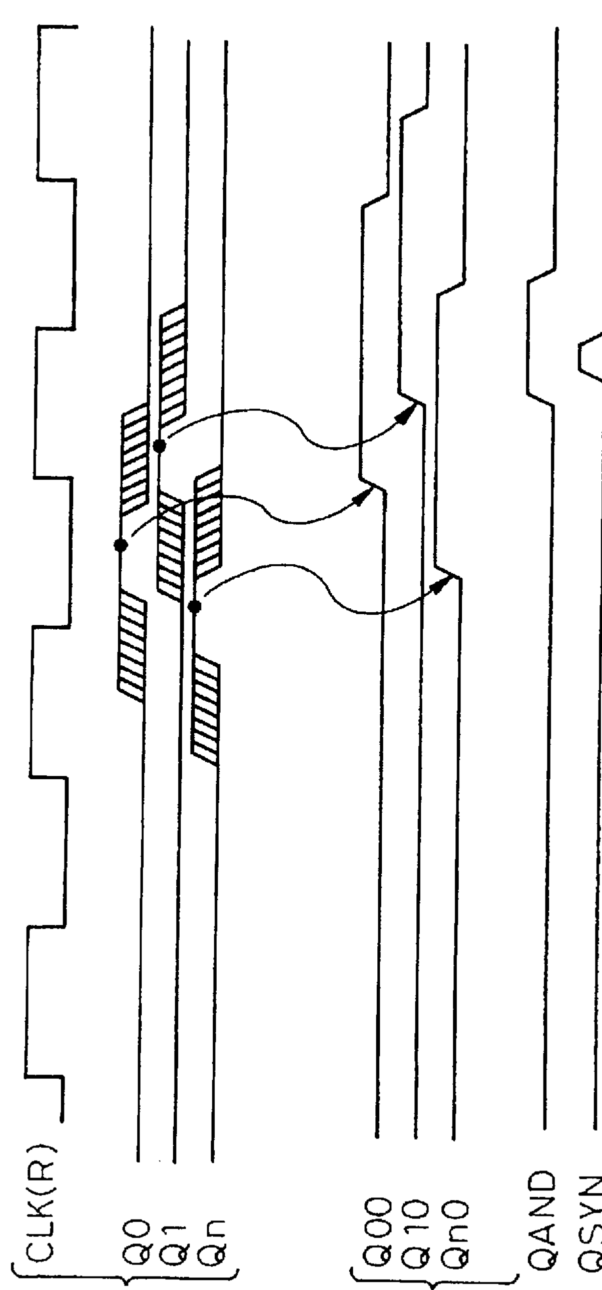


Fig.51

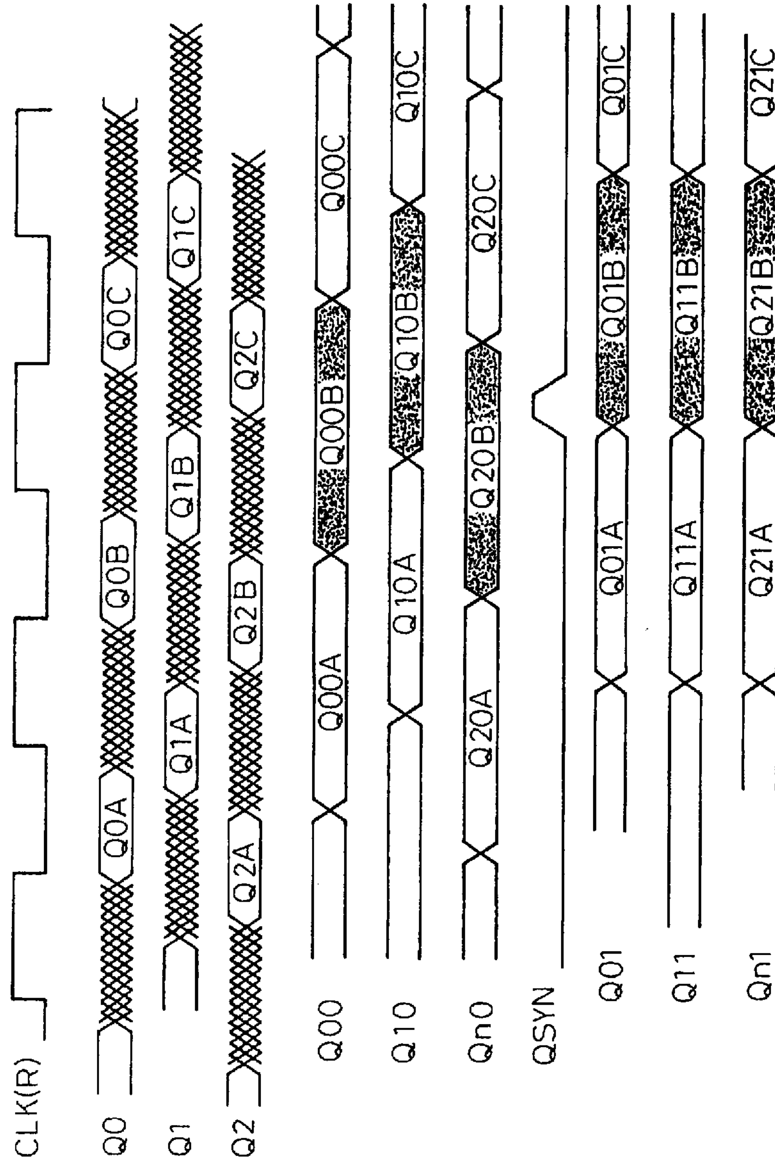


Fig.52
CLK(R)
Q0
Q0A
Q0B
Q0C
Q1
Q1A
Q1B
Q1C
Q2
Q2A
Q2B
Q2C
Q00
Q00A
Q00B
Q00C
Q10
Q10A
Q10B
Q10C
Qn0
Q20A
Q20B
Q20C
QSYN
Q01
Q01A
Q01B
Q01C
Q11
Q11A
Q11B
Qn1
Q21A
Q21B
Q21C

Fig.53

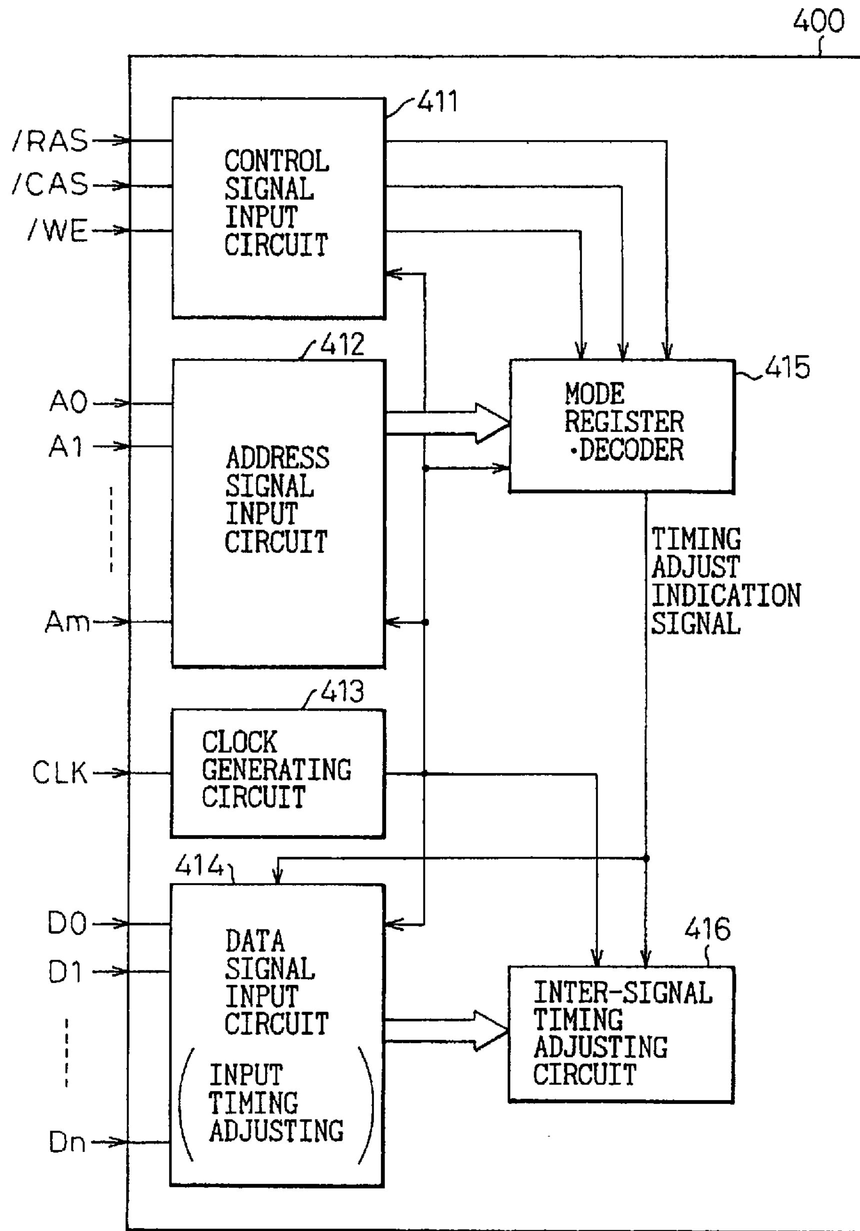


Fig.54

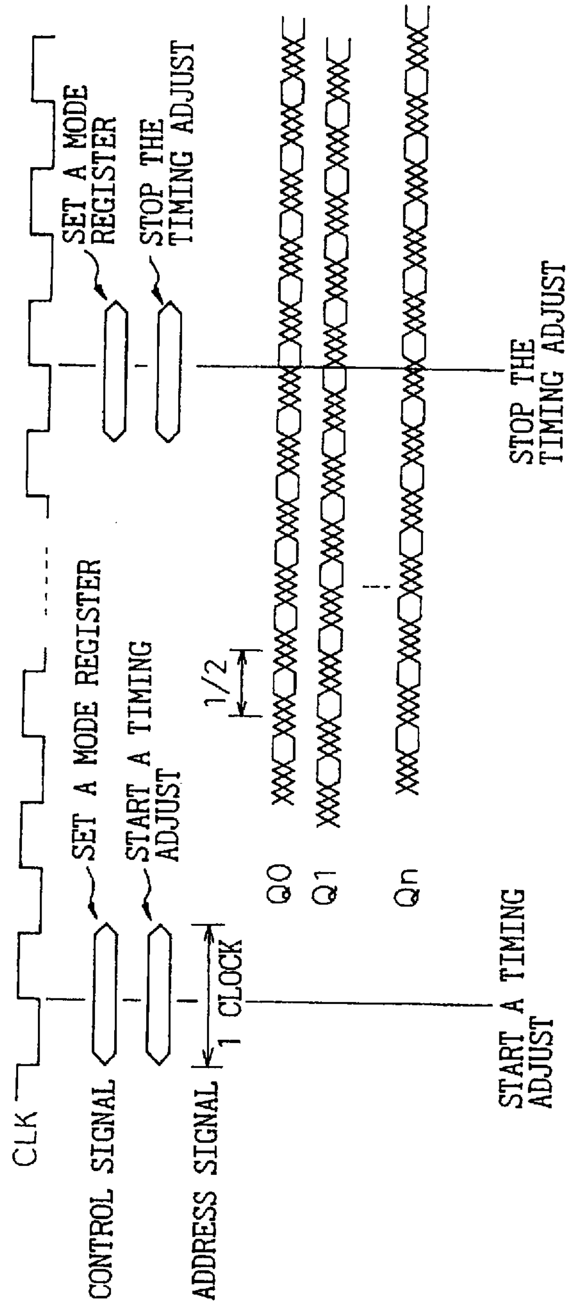
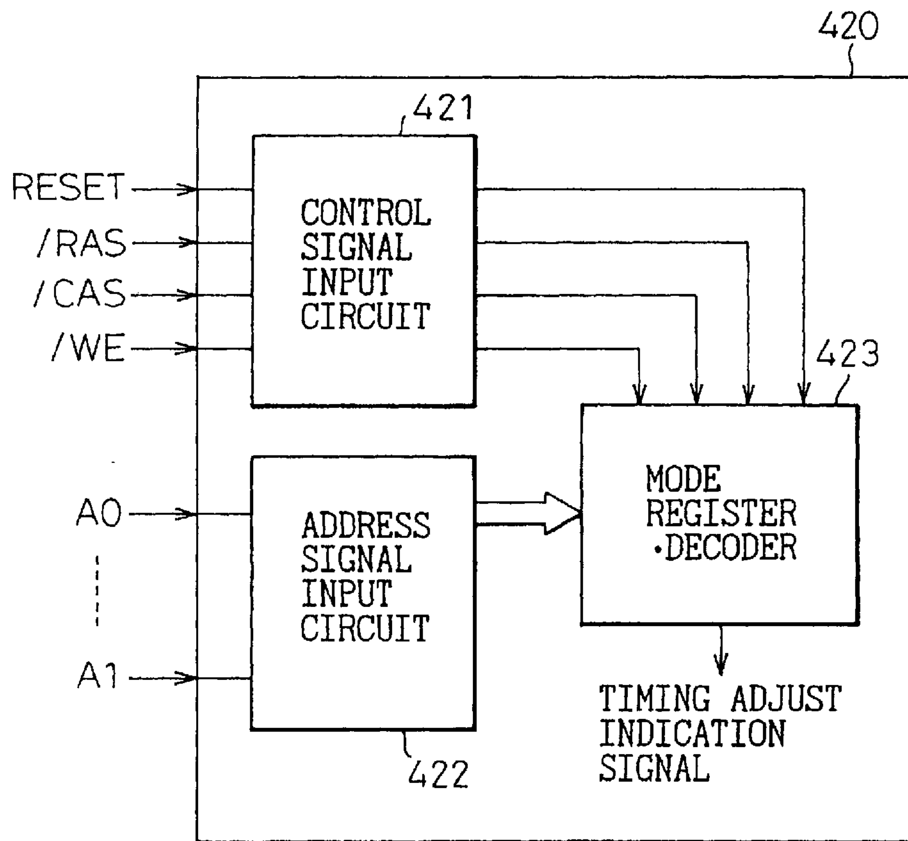


Fig.55



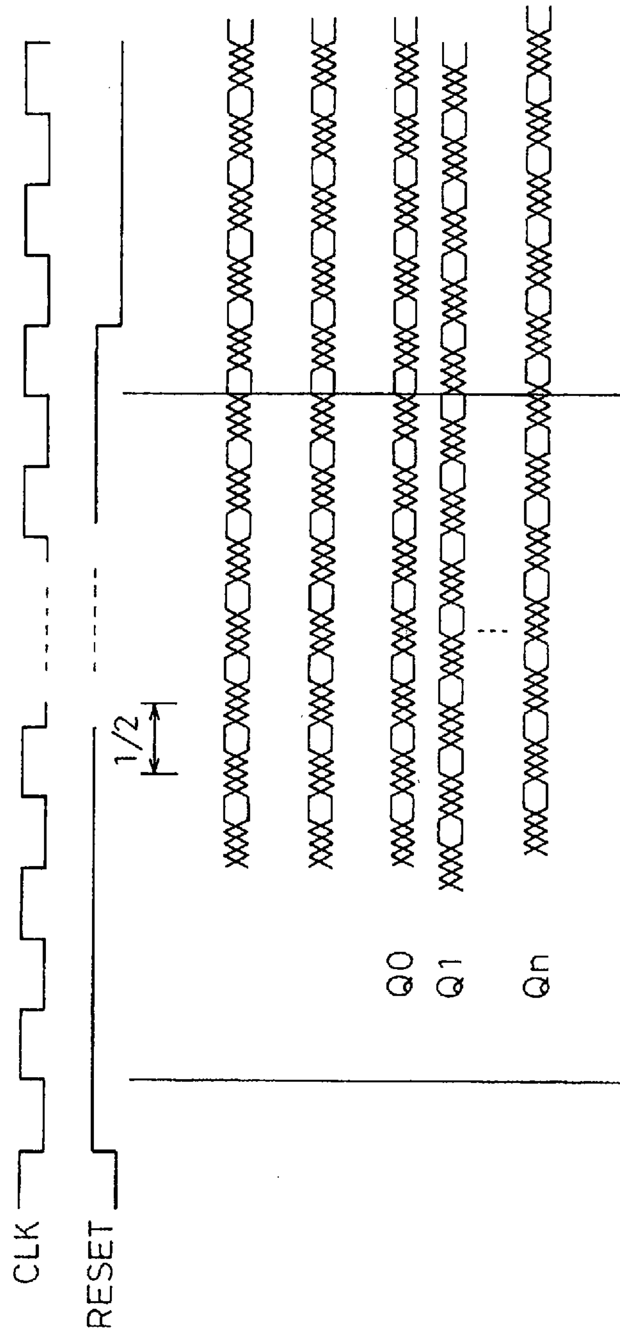


Fig.56
CLK
RESET
1/2
Q0
Q1
Qn

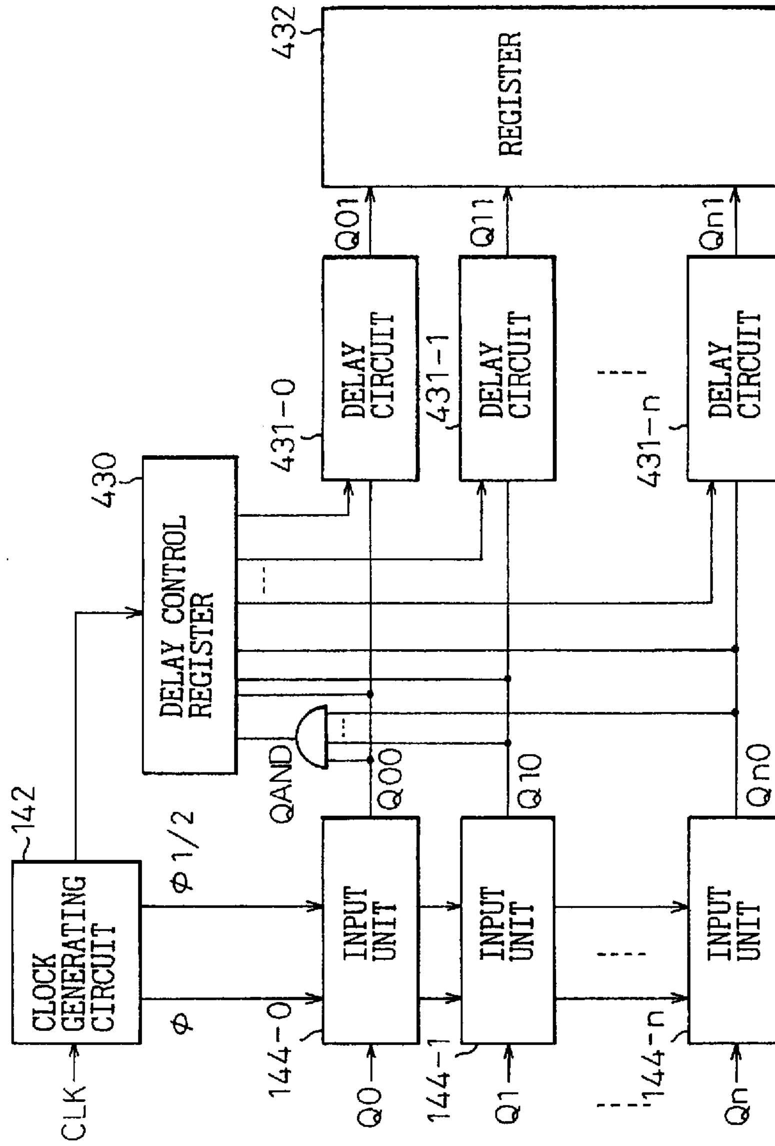
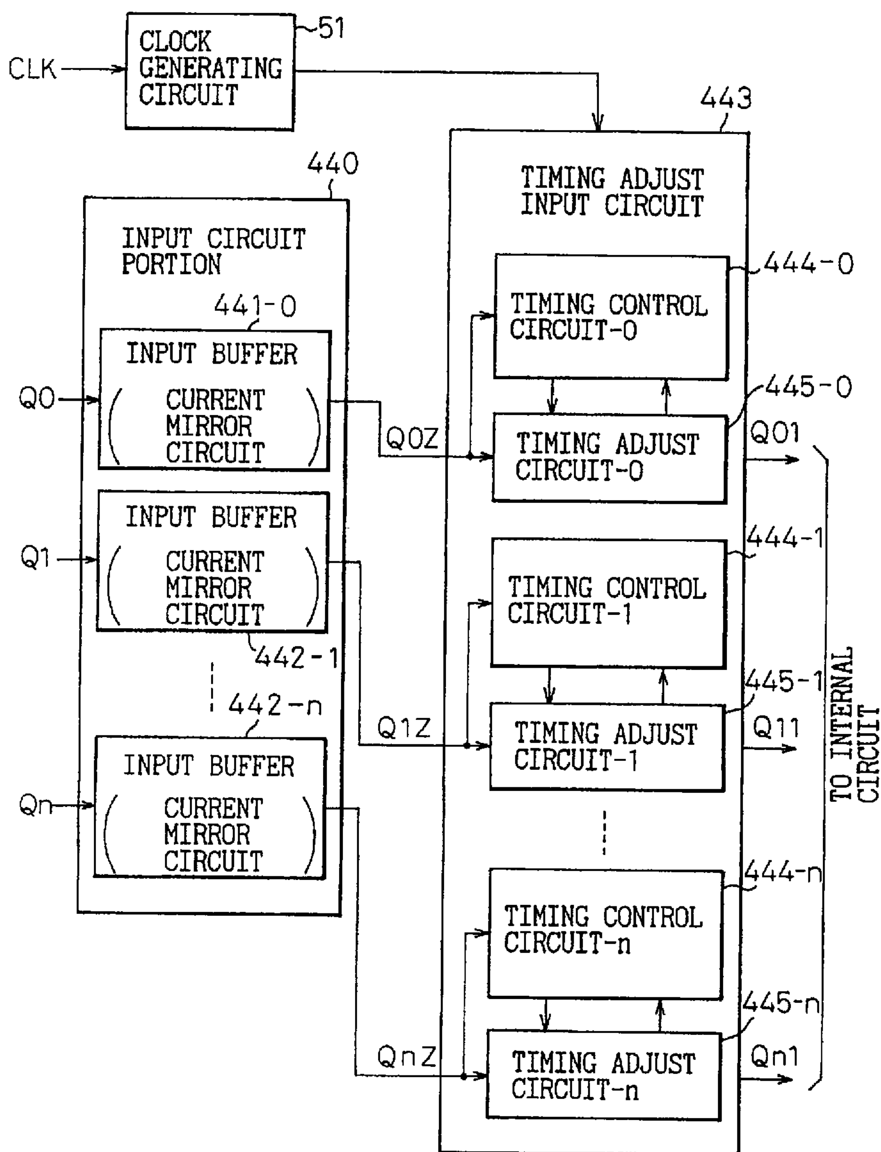


Fig.57
432
REGISTER
Q01
Q11
Qn1
431-0
DELAY CIRCUIT
431-1
DELAY CIRCUIT
431-n
DELAY CIRCUIT
430
DELAY CONTROL REGISTER
142
CLOCK GENERATING CIRCUIT
CLK
φ 1/2
φ
QAND
Q00
Q10
Qn0
INPUT UNIT
INPUT UNIT
INPUT UNIT
144-0
144-1
144-n
Q0
Q1
Qn

Fig.58



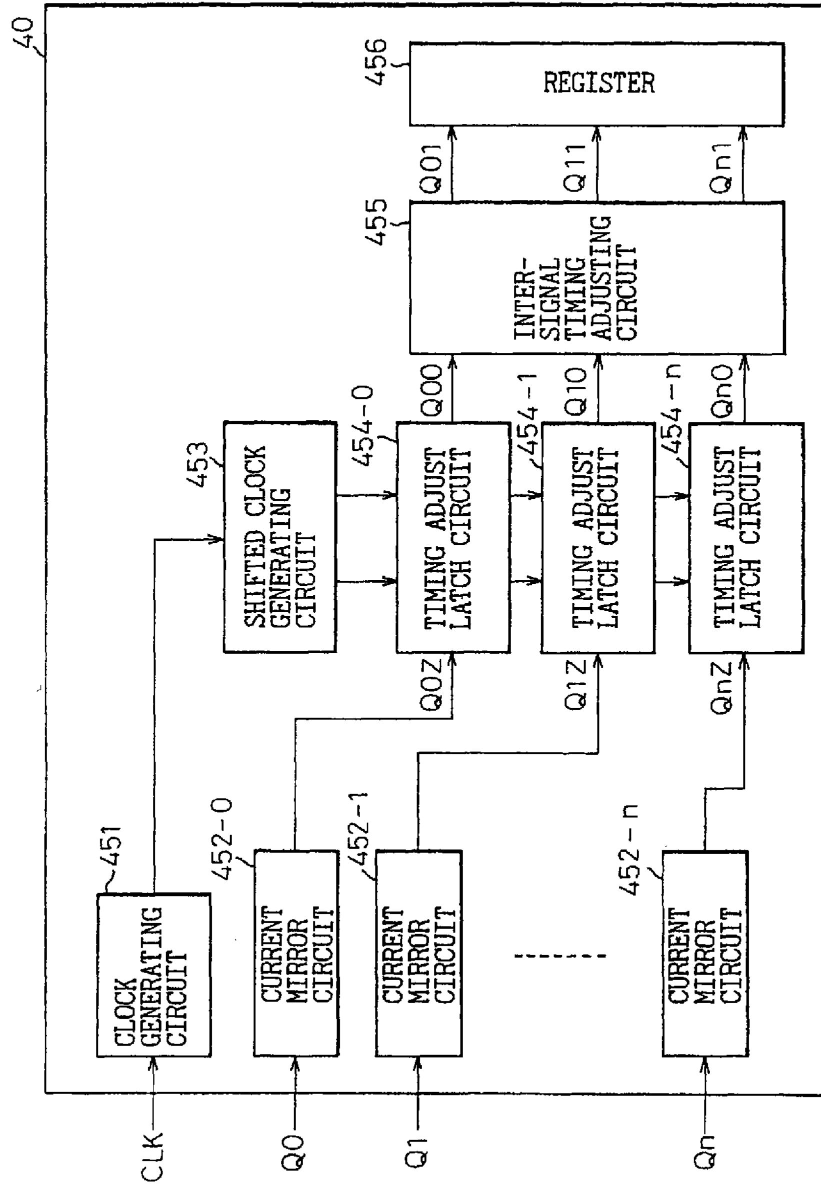


Fig.59
40
CLOCK GENERATING CIRCUIT
451
CURRENT MIRROR CIRCUIT
452-0
CURRENT MIRROR CIRCUIT
452-1
CURRENT MIRROR CIRCUIT
452-n
SHIFTED CLOCK GENERATING CIRCUIT
453
TIMING ADJUST LATCH CIRCUIT
454-0
TIMING ADJUST LATCH CIRCUIT
454-1
TIMING ADJUST LATCH CIRCUIT
454-n
INTER-SIGNAL TIMING ADJUSTING CIRCUIT
455
REGISTER
456
CLK
Q0
Q1
Qn
Q0Z
Q1Z
QnZ
Q00
Q10
Qn0
Q01
Q11
Qn1

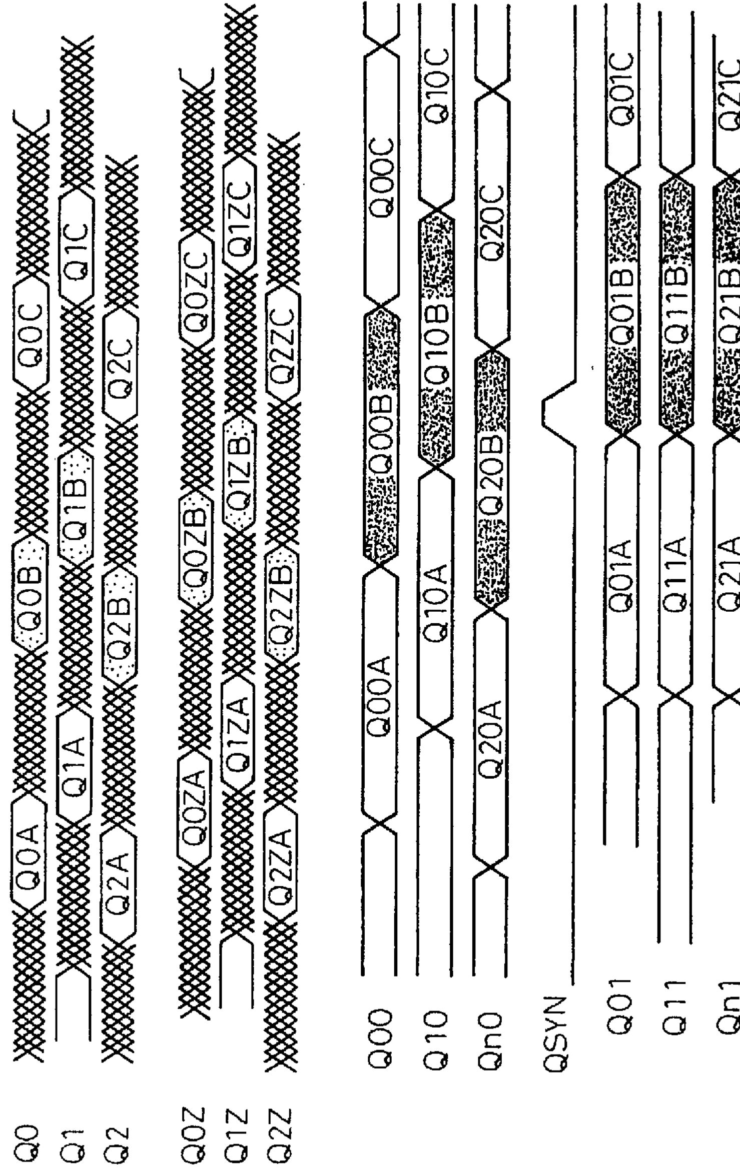


Fig.60
Q0
Q1
Q2
Q0Z
Q1Z
Q2Z
Q00
Q10
Qn0
QSYN
Q01
Q11
Qn1
Q0A
Q0B
Q0C
Q1A
Q1B
Q1C
Q2A
Q2B
Q2C
Q0ZA
Q0ZB
Q0ZC
Q1ZA
Q1ZB
Q1ZC
Q2ZA
Q2ZB
Q2ZC
Q00A
Q00B
Q00C
Q10A
Q10B
Q10C
Q20A
Q20B
Q20C
Q01A
Q01B
Q01C
Q11A
Q11B
Q21A
Q21B
Q21C

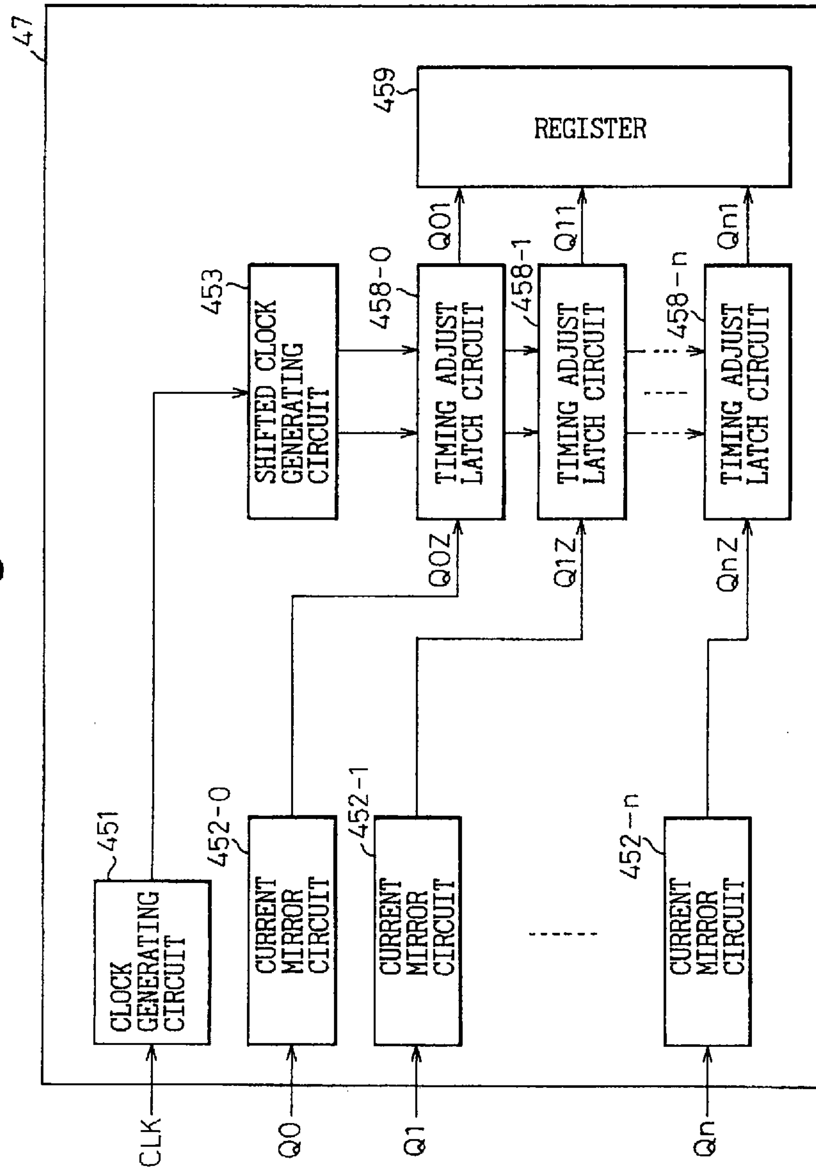


Fig.61
47
451
CLOCK GENERATING CIRCUIT
452-0
CURRENT MIRROR CIRCUIT
452-1
CURRENT MIRROR CIRCUIT
452-n
CURRENT MIRROR CIRCUIT
453
SHIFTED CLOCK GENERATING CIRCUIT
458-0
TIMING ADJUST LATCH CIRCUIT
458-1
TIMING ADJUST LATCH CIRCUIT
458-n
TIMING ADJUST LATCH CIRCUIT
459
REGISTER
CLK
Q0
Q1
Qn
Q0Z
Q1Z
QnZ
Q01
Q11
Qn1

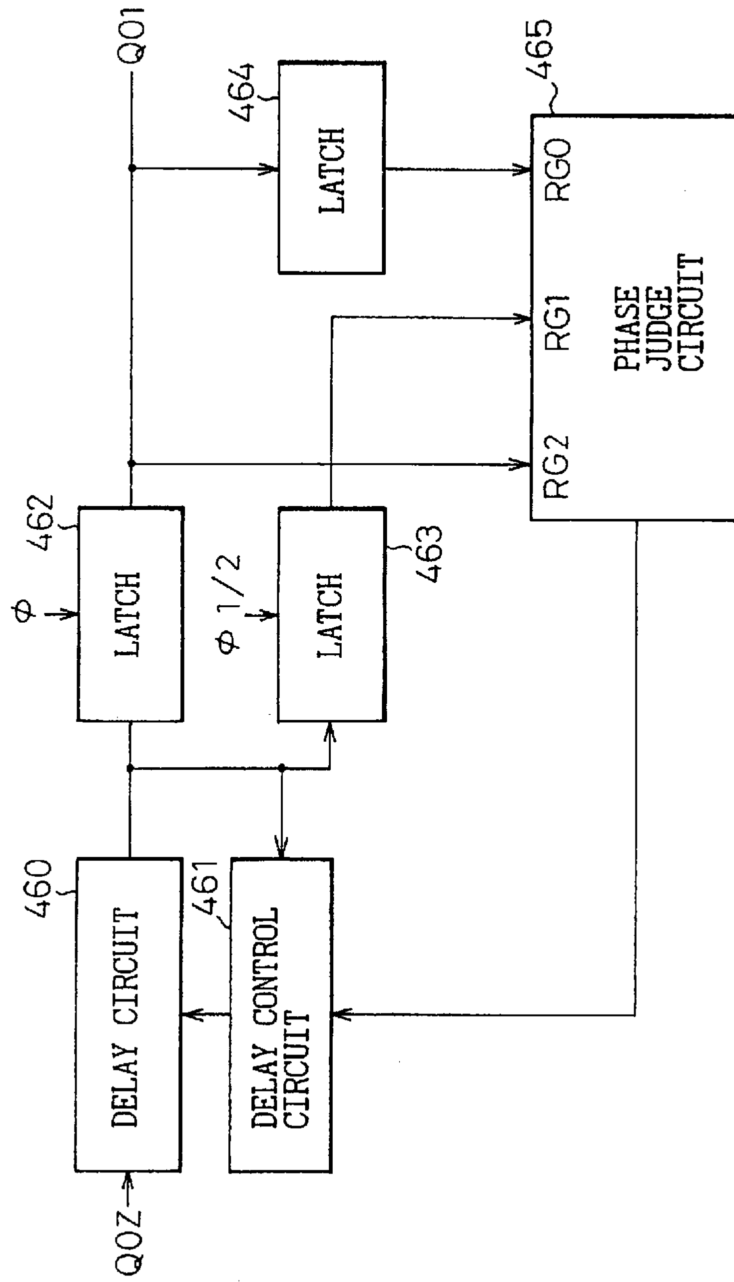


Fig.62
Q01
464
LATCH
465
RG0
RG1
RG2
PHASE
JUDGE
CIRCUIT
462
φ
LATCH
φ 1/2
LATCH
463
460
DELAY CIRCUIT
461
DELAY CONTROL
CIRCUIT
Q0Z

Fig.63

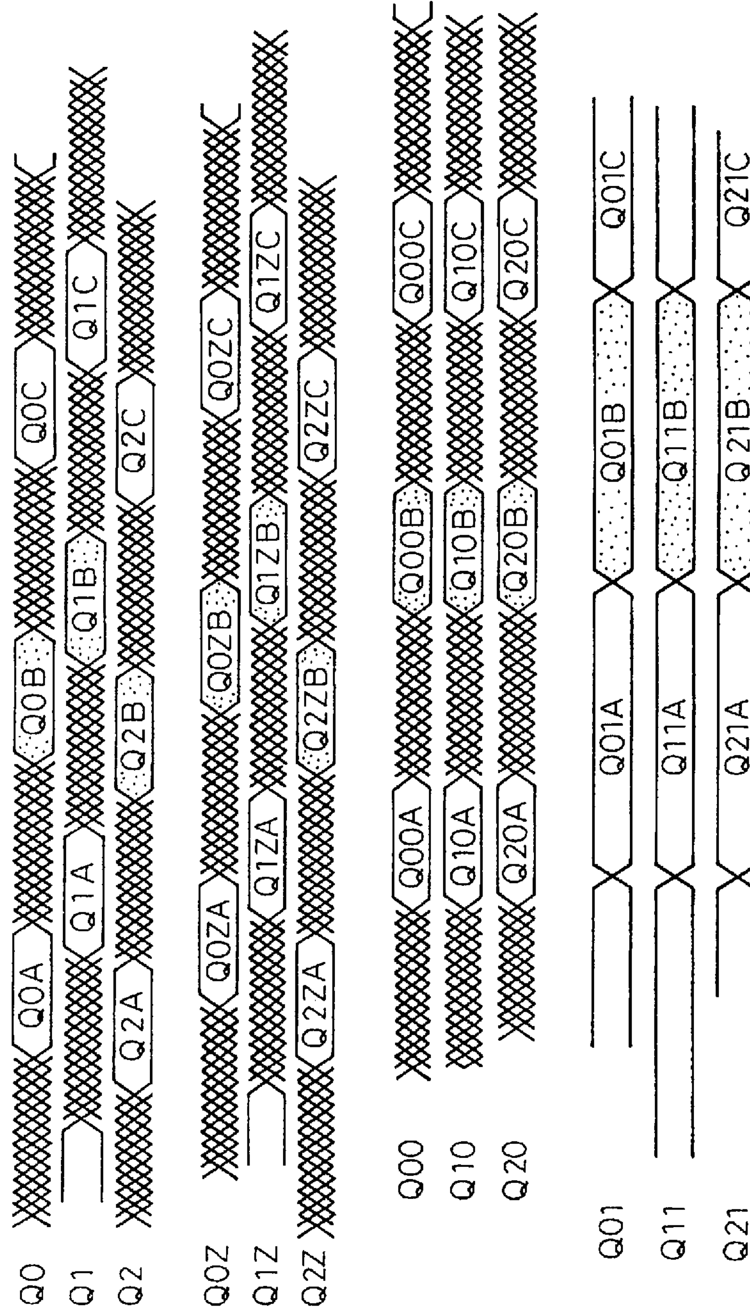
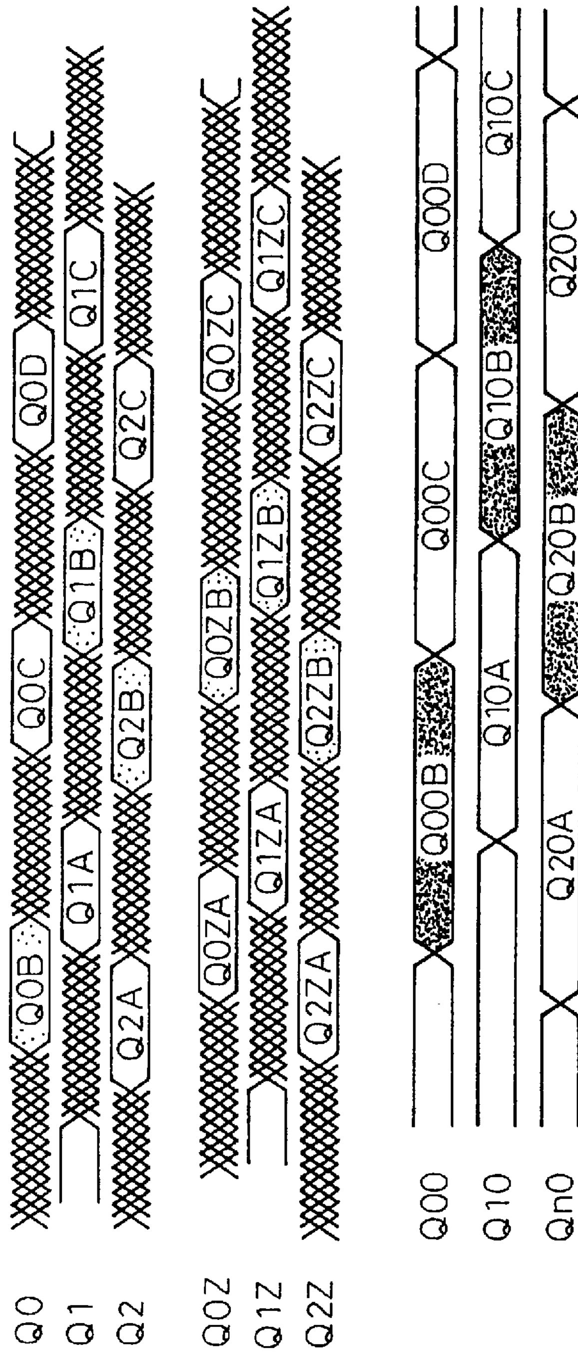


Fig.64



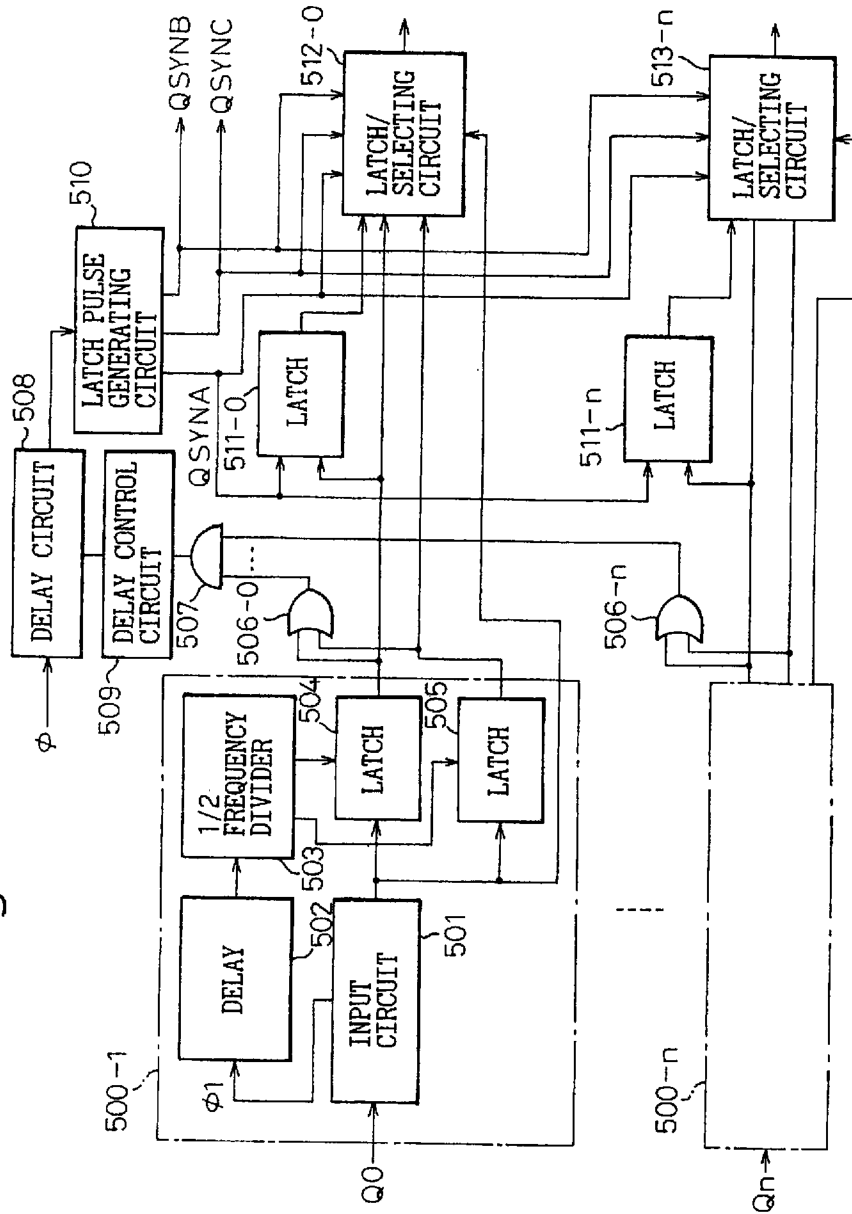


Fig.65
DELAY CIRCUIT
508
DELAY CONTROL CIRCUIT
509
LATCH PULSE GENERATING CIRCUIT
510
QSYNA
QSYNB
QSYNC
LATCH
511-0
511-n
LATCH/ SELECTING CIRCUIT
512-0
513-n
507
506-0
506-n
1/2 FREQUENCY DIVIDER
503
LATCH
504
505
DELAY
502
INPUT CIRCUIT
501
500-1
500-n
φ
φ1
Q0
Qn

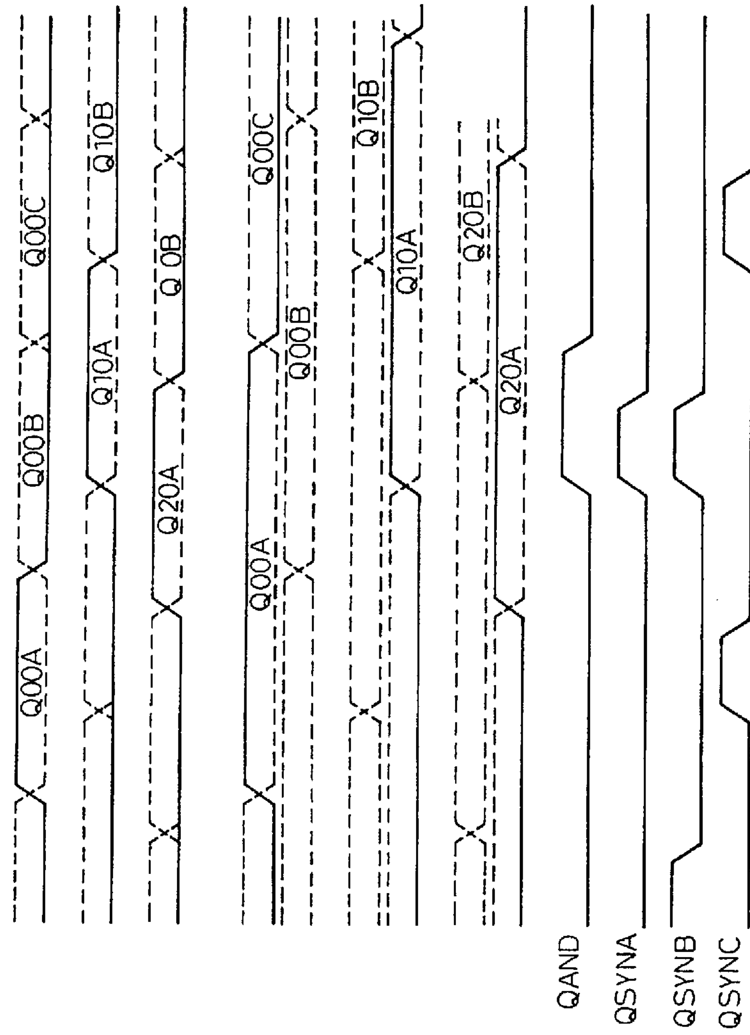


Fig.66
Q00A
Q00B
Q00C
Q10A
Q10B
Q20A
Q 0B
Q00A
Q00B
Q00C
Q10A
Q10B
Q20A
Q20B
QAND
QSYNA
QSYNB
QSYNC

Fig.67

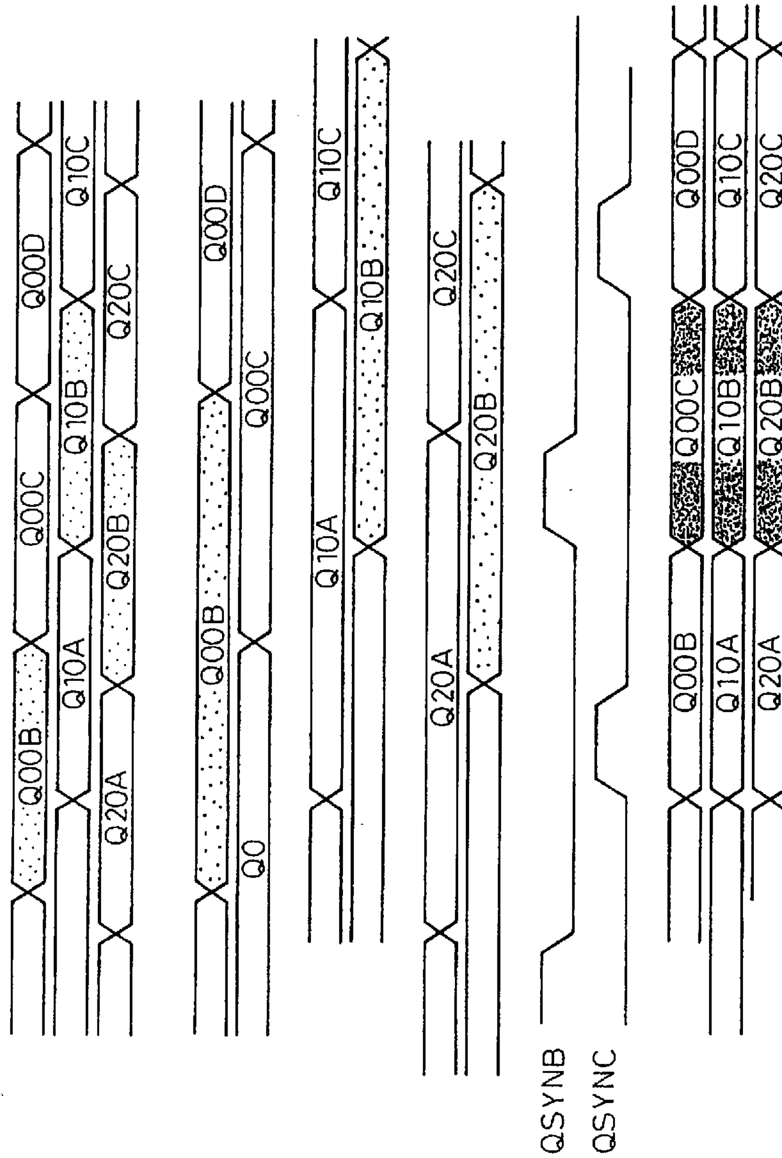
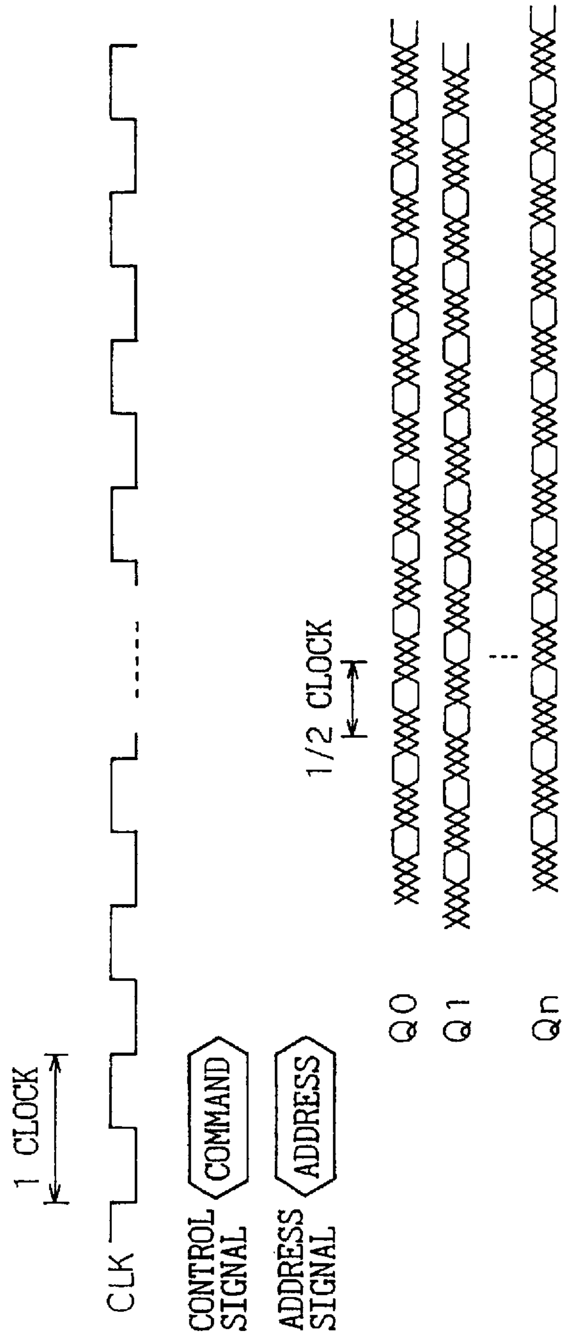


Fig.68



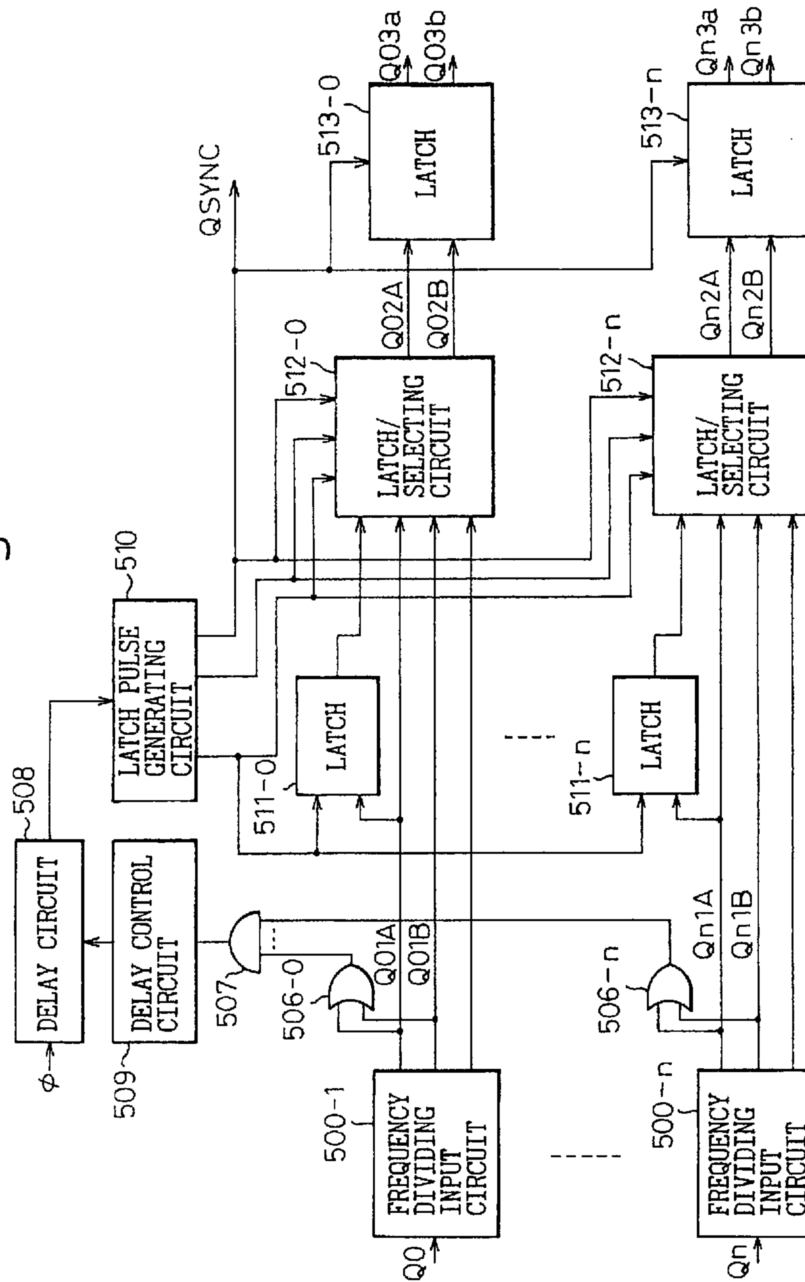


Fig.69
DELAY CIRCUIT
DELAY CONTROL CIRCUIT
LATCH PULSE GENERATING CIRCUIT
LATCH
LATCH/ SELECTING CIRCUIT
FREQUENCY DIVIDING INPUT CIRCUIT
QSYNC
Q03a
Q03b
Qn3a
Qn3b
Q02A
Q02B
Qn2A
Qn2B
Q01A
Q01B
Qn1A
Qn1B
Q0
Qn
φ
500-1
500-n
506-0
506-n
507
508
509
510
511-0
511-n
512-0
512-n
513-0
513-n

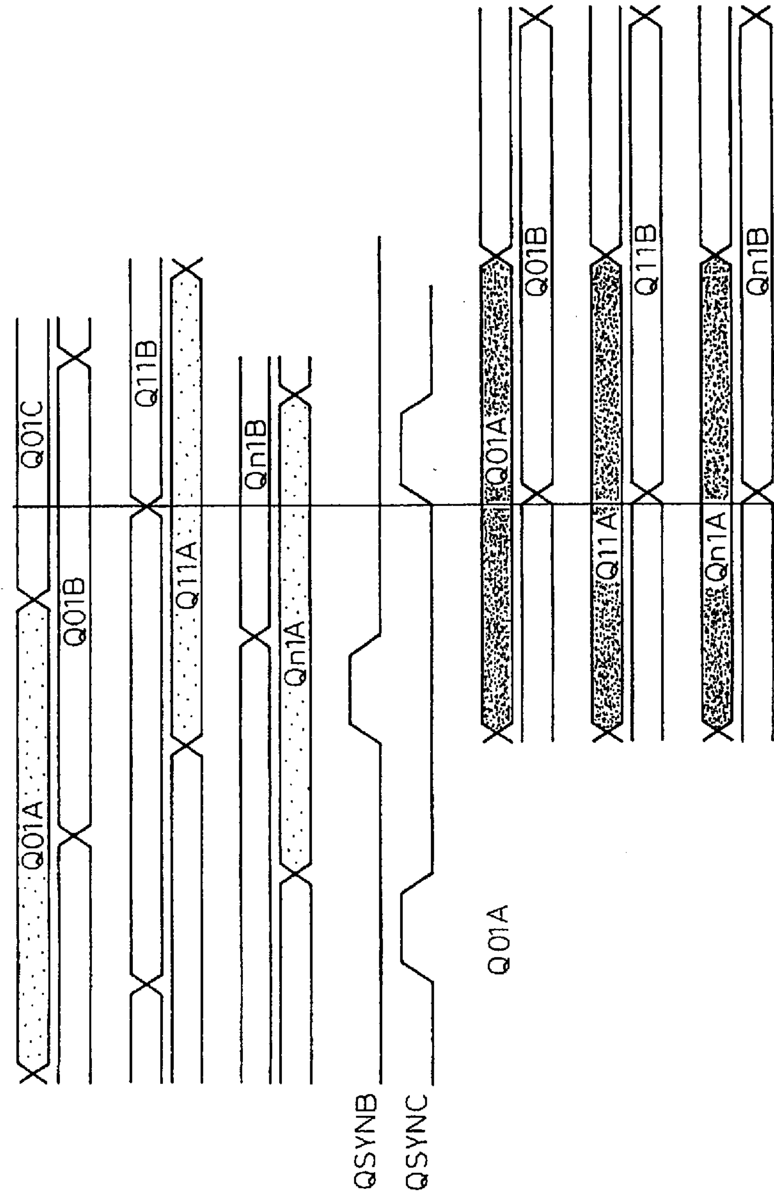


Fig.70
Q01A
Q01C
Q01B
Q11B
Q11A
Qn1B
Qn1A
QSYNB
QSYNC
Q01A
Q01B
Q11A
Q11B
Qn1A
Qn1B

Fig.71

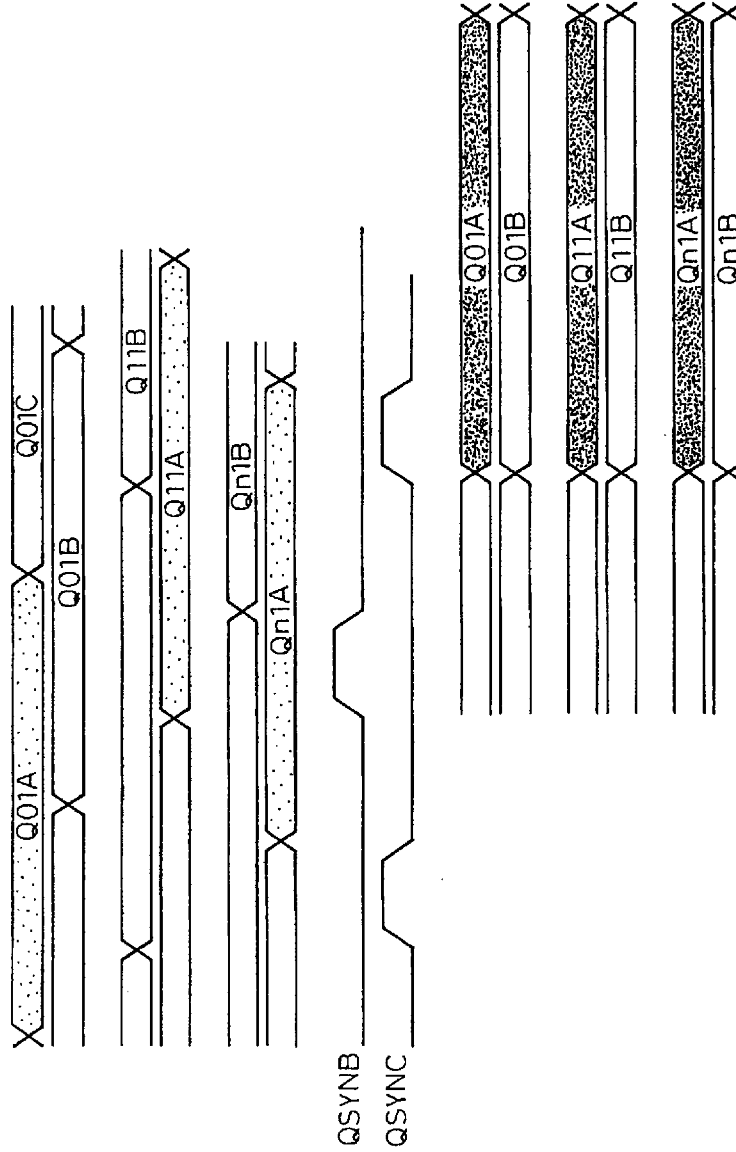
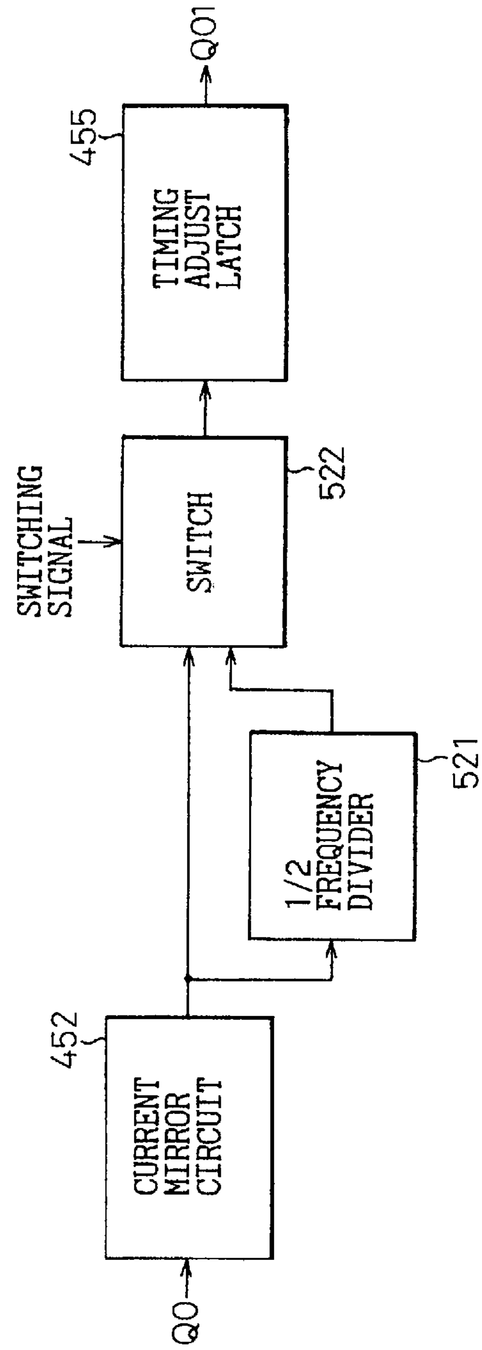


Fig.72



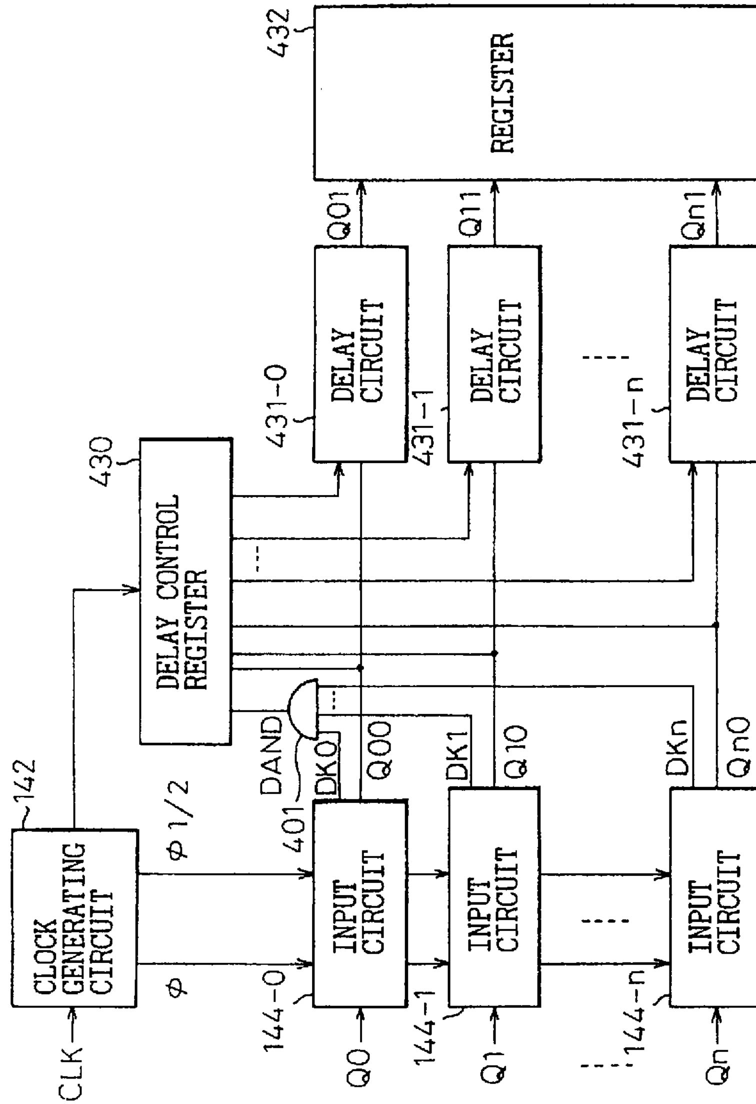


Fig.73

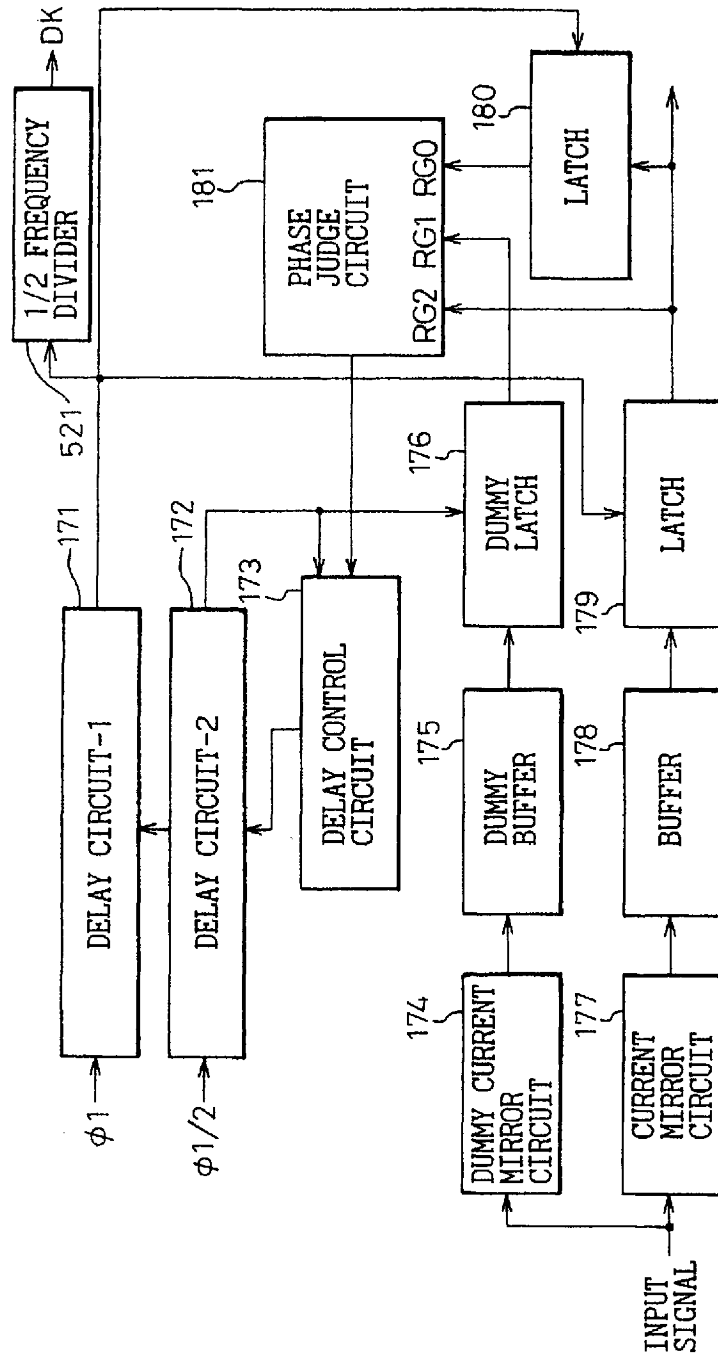


Fig.74
DK
1/2 FREQUENCY DIVIDER
521
PHASE JUDGE CIRCUIT
181
RG2
RG1
RG0
LATCH
180
171
172
173
DUMMY LATCH
176
LATCH
179
DELAY CIRCUIT-1
DELAY CIRCUIT-2
DELAY CONTROL CIRCUIT
DUMMY BUFFER
175
BUFFER
178
DUMMY CURRENT MIRROR CIRCUIT
174
CURRENT MIRROR CIRCUIT
177
φ1
φ1/2
INPUT SIGNAL

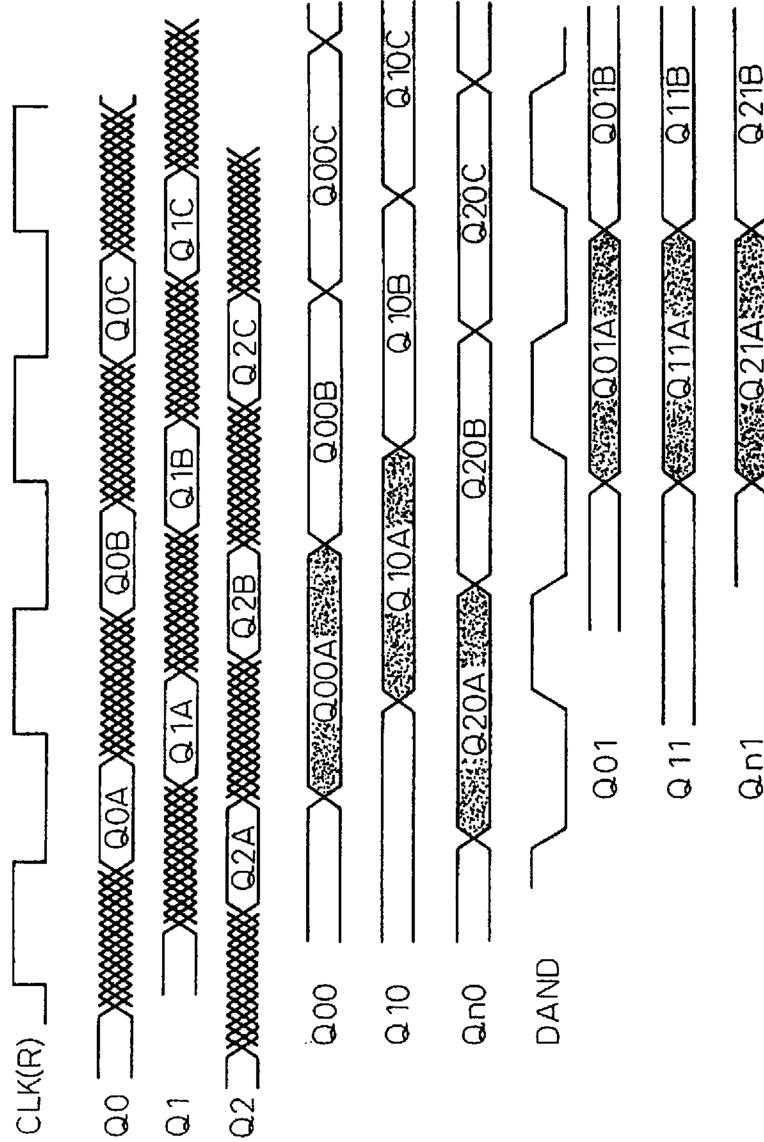


Fig.75

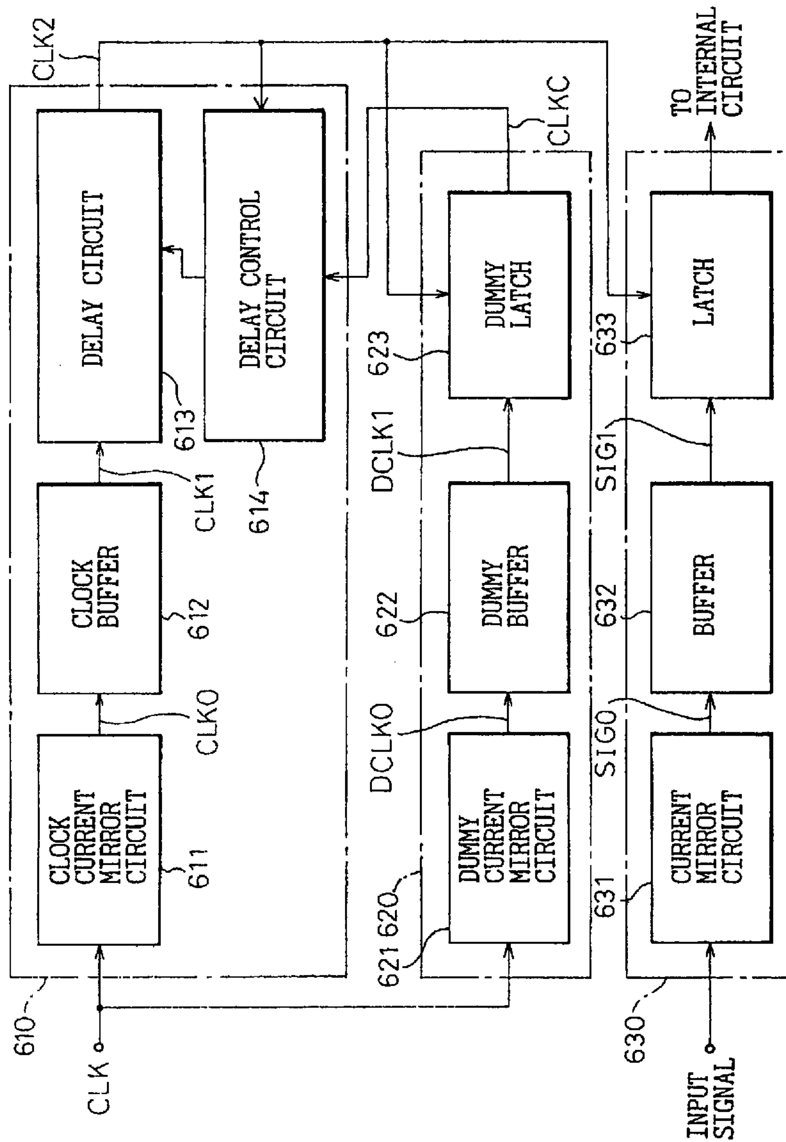
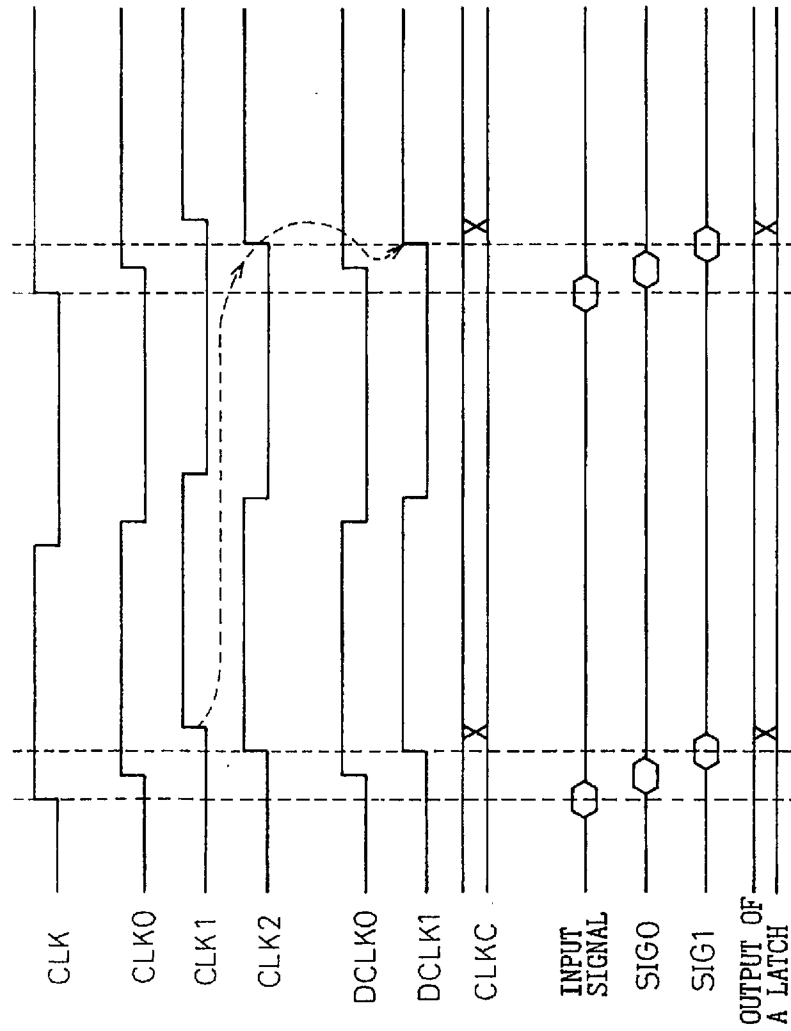


Fig.76
CLK
610
CLOCK CURRENT MIRROR CIRCUIT
611
CLK0
CLOCK BUFFER
612
CLK1
DELAY CIRCUIT
613
DELAY CONTROL CIRCUIT
614
CLK2
CLKC
620
621
DUMMY CURRENT MIRROR CIRCUIT
DCLK0
DUMMY BUFFER
622
DCLK1
DUMMY LATCH
623
630
INPUT SIGNAL
CURRENT MIRROR CIRCUIT
631
SIG0
BUFFER
632
SIG1
LATCH
633
TO INTERNAL CIRCUIT

Fig.77



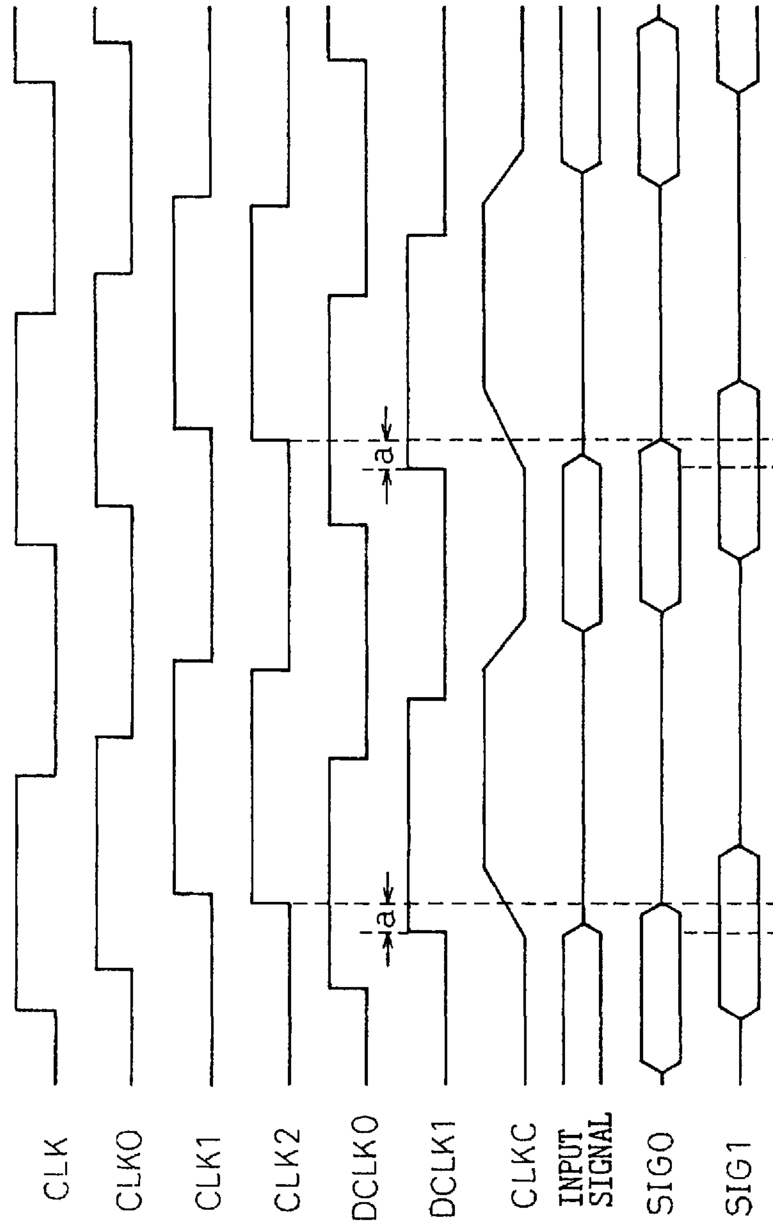


Fig.78

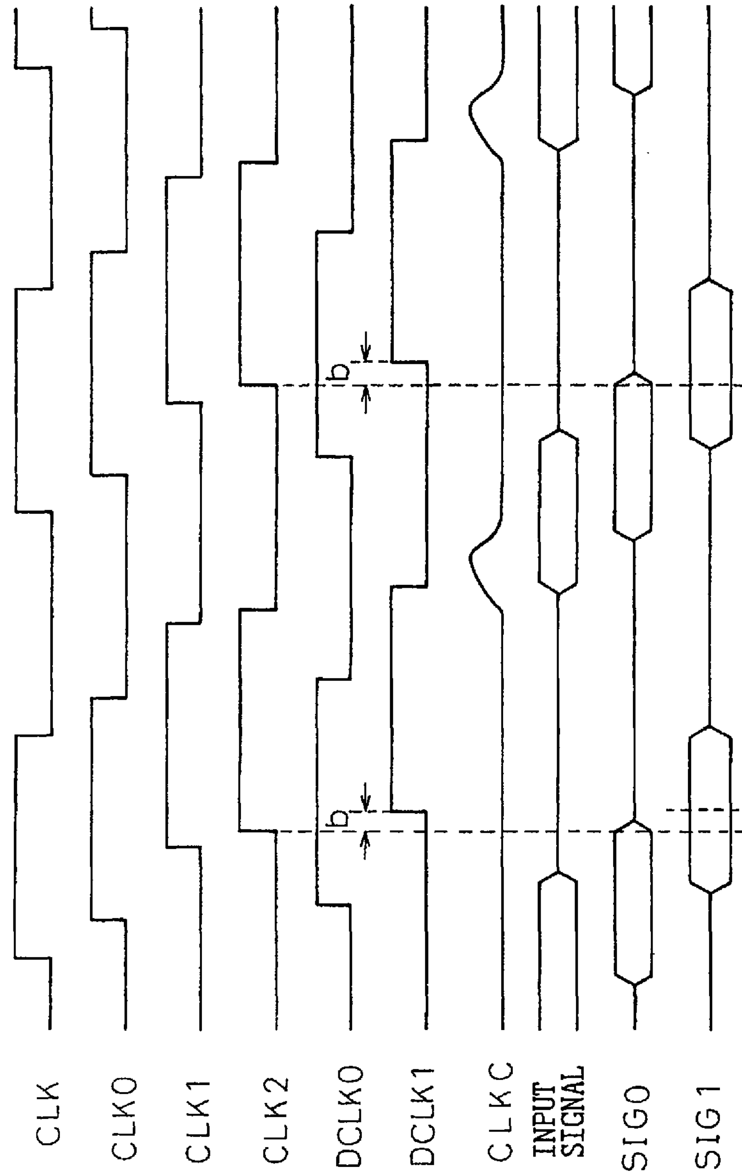


Fig.79
CLK
CLK0
CLK1
CLK2
DCLK0
DCLK1
CLKC
INPUT SIGNAL
SIG0
SIG1
b
b

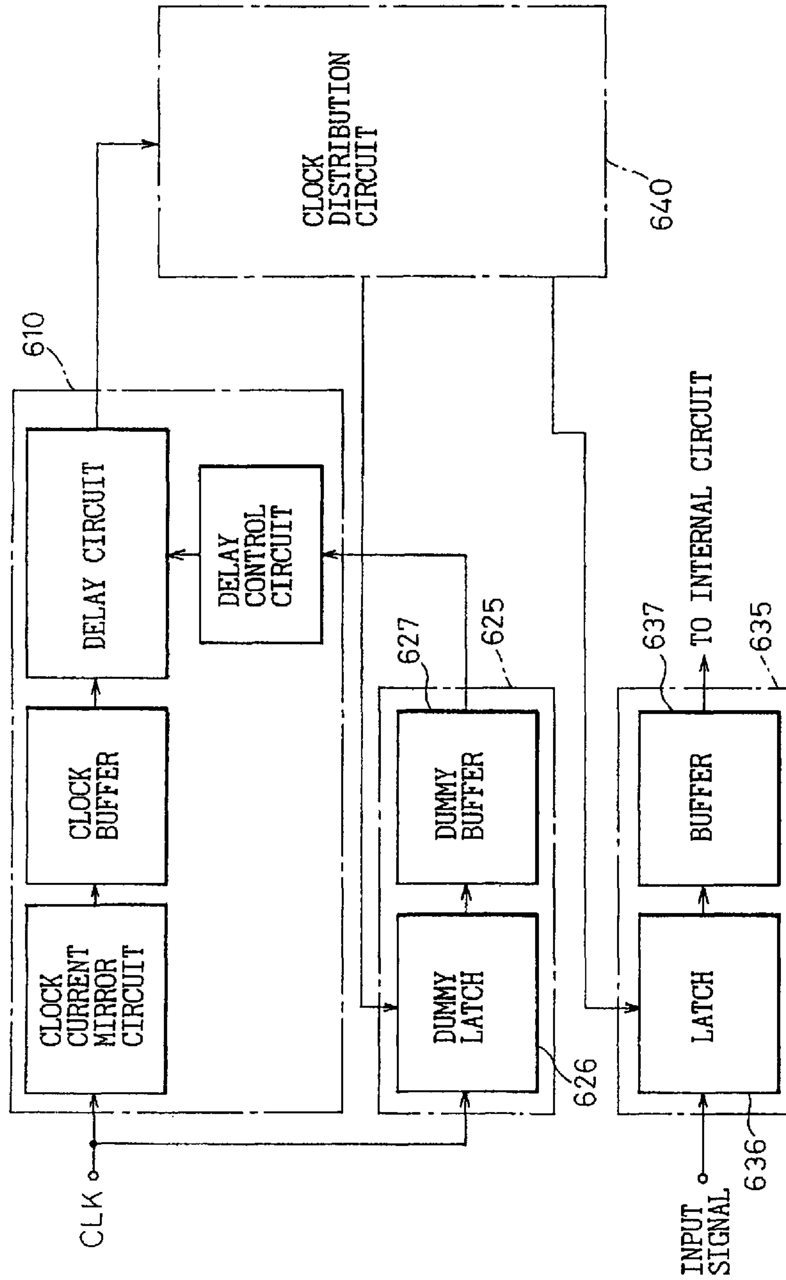


Fig.80
CLK
CLOCK CURRENT MIRROR CIRCUIT
CLOCK BUFFER
DELAY CIRCUIT
DELAY CONTROL CIRCUIT
610
CLOCK DISTRIBUTION CIRCUIT
640
DUMMY LATCH
DUMMY BUFFER
625
626
627
INPUT SIGNAL
LATCH
BUFFER
TO INTERNAL CIRCUIT
635
636
637

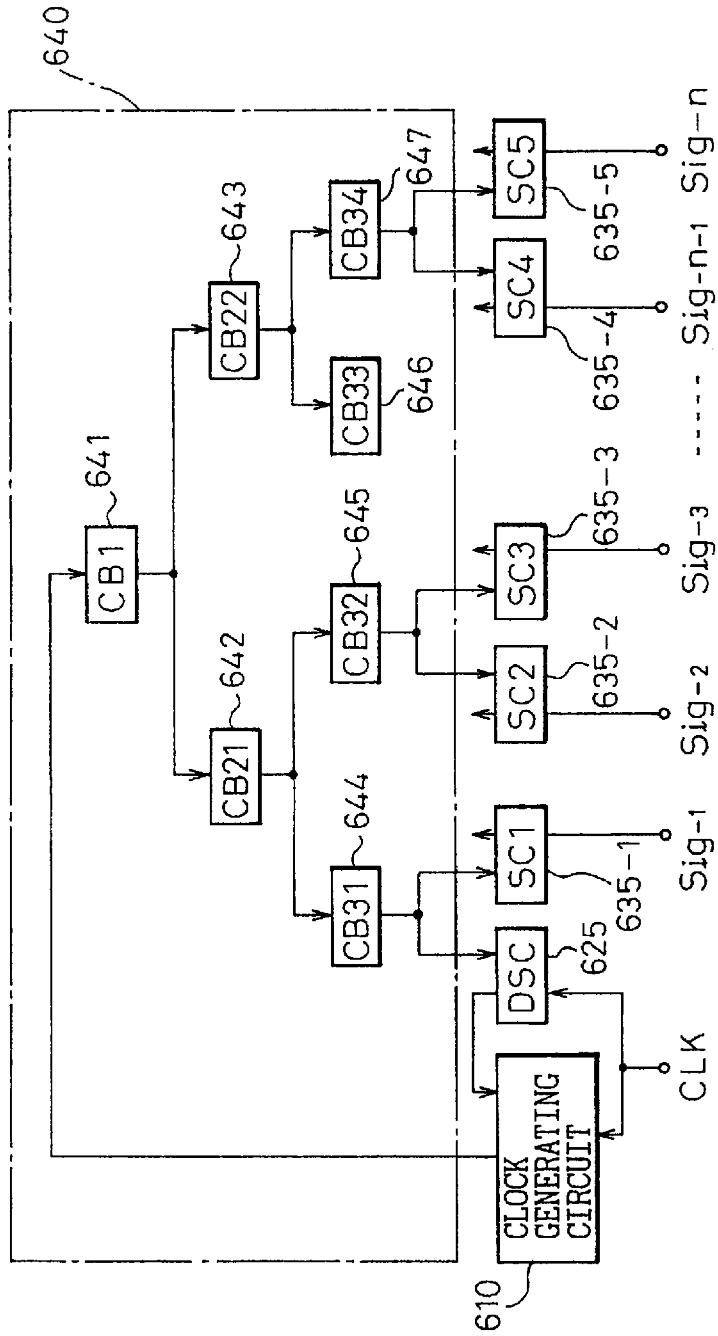


Fig.81
640
CB1
641
CB21
642
CB22
643
CB31
644
CB32
645
CB33
646
CB34
647
DSC
625
SC1
SC2
SC3
SC4
SC5
635-1
635-2
635-3
635-4
635-5
Sig-1
Sig-2
Sig-3
Sig-n-1
Sig-n
CLK
CLOCK GENERATING CIRCUIT
610

Fig.82

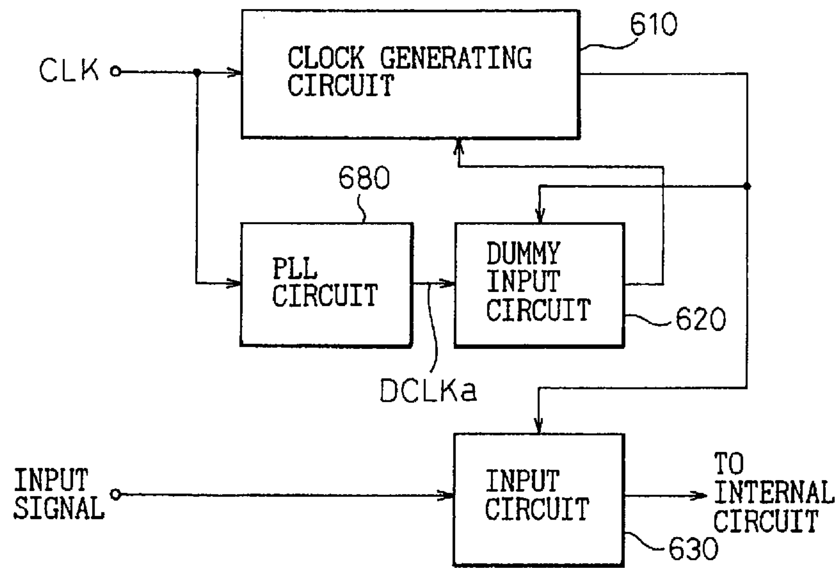
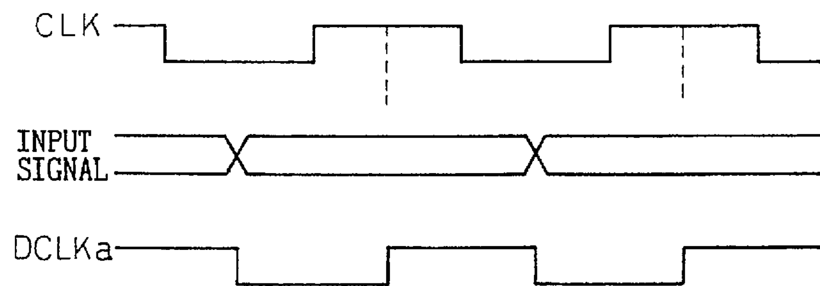


Fig.83



SYSTEM CONFIGURED OF SYNCHRONOUS SEMICONDUCTOR DEVICE FOR ADJUSTING TIMING OF EACH INPUT AND SEMICONDUCTOR DEVICE USED THEREFOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a system using a semiconductor device for retrieving an input signal effectively synchronous with an external clock in synchronism with an internal clock generated from the external clock, and a semiconductor device used for the system, or more in particular to a semiconductor device system adapted to retrieve an input signal at a predetermined timing by adjusting the timing of the internal clock in the case where a skew exists between signals or the ambient temperature or the source voltage undergoes a fluctuation, and a semiconductor device used for the system.

2. Description of the Related Art

A large-scale semiconductor device system including a computer using a semiconductor device is configured in such a manner that each portion of the system is synchronized with a clock, and the input/output operation of signals including data signals and address signals are executed in synchronism with the clock signal. A memory operated in accordance with a clock supplied from an external source is called the synchronous type, and a DRAM (dynamic random access memory) of synchronous type is called the SDRAM. The present invention primarily relates to the SDRAM, which will be mainly referred to in the description that follows. Nevertheless, the present invention is not confined to the SDRAM.

In recent years, the increased speed of clocks for CPUs or the increased processing speed of various other electronic circuits have given rise to a demand for increasing the speed of interfaces connecting semiconductor devices. The SDRAM is a semiconductor device meeting this demand for higher speed, and continuous addresses therein can be accessed very quickly. Signals on a data bus undergo a change with a very short period, and therefore it is necessary to retrieve the signals from the data bus at high speed.

In the case where a semiconductor device retrieves an input signal, a period is defined during which the input signal is required to be established before and after the timing of retrieval. The period during which the input signal is required to be established before the retrieval timing is called a set-up time, and the period during which the input signal is required to be established after the retrieval timing is called a hold time.

With the ever increasing speed of CPU clocks in computer systems and various electronic circuits in recent years, an increased speed of the interfaces connecting semiconductor devices is urgently required. In a high-speed system using such high-speed semiconductor devices, the input establishment time for each semiconductor device to retrieve the input signal defines the system speed. The input establishment time of the semiconductor devices should therefore be reduced.

In a low-speed system, the period before a signal is established is relatively small as compared with the clock period, and poses no problem. Such a period poses a very serious problem, however, for a high-speed system with a very short clock period. For this reason, in high-speed systems measure are taken to equalize the length of the clock signal line and the lengths of other signal lines as far as possible. In spite of this, it is difficult to equalize the wiring lengths and loads exactly, and some phase difference is unavoidable, thereby posing a barrier to an increased speed.

Another problem is that of the phase difference for the semiconductor device at the receiving end. The clock input circuit has a configuration equivalent to the input circuits for other input signals, so that an arrangement is made to assure the same delay of the clock period and the input signal applied to the semiconductor device before being transmitted to a latch circuit. Actually, however, it is impossible to design the circuits to be completely identical to each other. For this reason, although the delay amounts are set as close to each other as possible, somewhat different circuits and wirings are unavoidable. Taking into consideration the variations in the production process and the temperature dependency and the source voltage dependency of the delay amount, the delay amount is differentiated even in the case where the clock input circuit is equivalent to the signal input circuit. Due to the difference in delay amount, the input establishment time required by the circuit operation varies somewhat from the rising edge of the clock CLK. The input establishment time is required to be included in the effective signal period, and in the case where this condition fails to be met, a normal input signal retrieval is impossible. Conventionally, however, the input establishment time, i.e., the set-up time and the hold time required for the circuit operation are defined taking these variations into consideration.

With the recent increase in the CPU clock speed and the processing speed of various electronic circuits in the computer systems, there is an ever increasing demand for a higher speed of the interfaces connecting the semiconductor devices. In a high-speed system using such high-speed semiconductor devices, the input establishment time for each semiconductor device to retrieve the input signal defines the system speed, and it is necessary to reduce the input establishment time of the semiconductor devices.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a system capable of increasing the speed of data transfer even in the case where the clock and a signal are out of phase with each other at the receiving end or even in the case where a phase difference develops between the clock input circuit and the other signal input circuits in the semiconductor device at the receiving end, and to provide a semiconductor device used for such a system.

In order to achieve the above-mentioned object, according to the present invention, there is provided a semiconductor device system comprising an input timing adjusting circuit in the semiconductor device at the receiving end for adjusting the phase of the clock supplied to the input circuit to allow the input circuit to retrieve the input signal in an effective, safe manner. The input timing adjusting circuit is preferably provided for each input circuit. In the case where the skew between input signals is smaller than the skew between the input signals and the clock, however, an input timing adjusting circuit can be shared by a plurality of input circuits.

In a semiconductor device system according to this invention, the skew which may develop between the clock and the input signal is reduced substantially to zero as a result of the adjustment made to attain the optimum timing. Therefore, the input signal can remain effective for a longer time in the input circuit.

The input timing adjusting circuit includes a delay circuit with a selectable delay amount for delaying the internal clock generated on the basis of a received clock and producing it as an input timing clock, a signal input circuit for retrieving the input signal in synchronism with the input timing clock, a phase comparator for comparing the phase of the input timing cock with that of the input signal, and a delay control circuit for changing the amount of delay of the delay circuit in such a manner as to attain a predetermined phase of the input timing clock with respect to the input signal on the basis of the decision of the phase comparator.

In the case where the input timing adjusting circuit includes such a feedback circuit, some time is required before the control value of the feedback circuit converges. In the case where such a semiconductor device system is started, therefore, a predetermined time adjust mode is always necessary. In this adjust mode, a signal suitable for feedback of the input timing adjusting circuit can be applied as an input. Even after this adjust mode, the feedback control is continued or the control value as of the time point at the end of the adjust mode is stored and maintained. In the case where the feedback control is continued even after the adjust mode, any phase change that may occur after the adjust mode can be handled. Since a signal associated with normal operation is input after the adjust mode, however, it is necessary that the feedback control can be carried out with such a signal for normal operation. In the case where the control value as of the time point at the end of the adjust mode is stored and maintained, on the other hand, the configuration is simpler than in the case where the feedback control is continued after the adjust mode, but any phase change that may occur after the adjust mode cannot be handled appropriately. For this reason, an adjust mode is preferably inserted at regular intervals of time.

In the case where two signal phases are compared, it is generally determined whether the changing edge of one signal is advanced of that of the other signal by comparing the temporal relation between the two signals. As for an input circuit, however, the input timing clock is a signal changing with the input signal in a stable state, and therefore the phases thereof cannot be compared. As a result, it is necessary that the phase of the input timing clock is displaced by a predetermined amount to generate a shift clock changing in phase with the input signal, so that the phase of the shift clock is compared with that of the input signal, or that the input signal phase is displaced by a predetermined amount to compare the phase of the input timing clock with that of the shift input signal thus displaced. In the case where a shift clock or a displaced input signal is generated at the receiving end, the input signal can be retrieved by the input timing clock while comparing the phases thereof and therefore it is possible to continue the feedback control after completion of the adjust mode. In the case where a signal with a phase displaced by a predetermined amount is generated at the driving end, however, the signal displaced by a predetermined amount of phase different from the signal for normal operation is required to be transmitted to the receiving end. Such a signal, however, cannot be transmitted in a normal mode. A signal displaced by a predetermined amount of phase can be generated at the driving end, therefore, only in the case where the feedback control is not carried out after the adjust mode. In the case where an input signal displaced by a predetermined amount of phase is generated at the receiving end, on the other hand, the input signals received by a current mirror circuit and a buffer circuit are required to be used directly for comparison without latching the input signals. Under such a condition, however, pulse quality of the input signals are deteriorated and therefore satisfactory comparison is impossible. In the case where a signal displaced by a predetermined amount of phase is generated at the receiving end, therefore, a shift clock is desirably generated. An alternative is to generate a shift clock at the driving end and transmit it in the adjust mode. In view of the fact that the clock constitutes a reference for synchronous operation, however, different clock phases are not desirable even in the adjust mode. In the case where a signal displaced by a predetermined amount of phase is generated and transmitted at the driving end, therefore, it is desirable to produce such a signal in synchronism with the shift clock in the adjust mode and produce it in synchronism with the clock at the time of normal operation.

In phase comparison, the phase of the input signal before being latched can be compared with that of the timing signal or the shift clock. The problem, however, is that the deteriorated input signal as described above makes satisfactory phase comparison difficult. In view of this, according to this invention, phase comparison is done taking advantage of the fact that in the case where an input signal changing in one direction is latched by a timing signal in the neighborhood of the changing edge thereof, the latched value is different depending on whether the phase is advanced or delayed.

In the presence of a receiving timing adjust mode, the signal retrieved by a signal input circuit can be used always as a signal changing in predetermined periods. As a result, in the case where a signal is involved which changes a predetermined time before the timing of retrieving the signal value to be decided, i.e., in the case where a signal changing each period is involved, for example, it can be decided whether the signal changes from "low" to "high" or from "high" to "low" by determining a signal value one-half period before. In the case where a decision is made in normal mode, in contrast, the signal retrieved by the signal input circuit is a normal signal and therefore the manner in which it changes cannot be determined. In such a case, the signal values before and after the timing of retrieving the signal value to be determined are handled to determine whether the input signal has changed and, if so, the direction in which it may have changed.

At higher speeds, the value of the input signal which may change for each clock cycle may change to the next value before a full change to a value. In view of the fact that the input signal has changed sufficiently to a value in the case where the same values succeed, however, the waveform changing to the next value is different, thereby generating a phase difference. In the case where the input timing is adjusted, therefore, it is necessary to take the previous state of the input signal into consideration. In a semiconductor device system according to this invention, the receiving end thereof includes a minimum period change detection circuit for detecting any continuous change of the input signal during the immediately preceding two clock cycles, wherein the delay control circuit carries out the feedback control to change the amount of delay of the delay circuit only when the input signal changes continuously during the immediately preceding two clock cycles but carries out no feedback control on other occasions. This control leads to the adjustment to attain the optimum timing in the case where the input signal value changes at each clock cycle. When the input signal value continues to remain the same, therefore, the input timing signal is desirably corrected by a corresponding amount. In view of this, the receiving end of the semiconductor device system according to this invention includes a timing correction circuit for selecting whether the timing of retrieval at the signal input circuit should be

delayed by a predetermined amount or not and an immediately preceding change detection circuit for detecting any change of the input signal which may occur during the immediately preceding clock cycle. Thus, in the case where the input signal fails to change during the immediately preceding clock cycle, the timing of retrieval at the signal input circuit is delayed a predetermined amount by the timing correction circuit. As a result, regardless of whether the input signal value changes for each clock cycle or continues to assume the same value, the input signal can be retrieved at appropriate timings.

Further, since the input timing is adjusted by an input timing adjusting circuit included in each input circuit, each input circuit can retrieve an input signal at optimum timing. In spite of this, the outputs of the input circuits are out of phase and fail to be in phase. This out-of-phase condition is not desirable in view of the fact that the operation of the internal circuits is performed in synchronism with the clock, and the signals applied to the internal circuits are desirably in phase. For this reason, the receiving end of the semiconductor device system according to this invention further includes an inter-signal timing adjusting circuit for detecting the phase difference between the output signals of the input circuits and regulating the signals into phase.

The inter-signal timing adjusting circuit includes, for example, a common effective period detection circuit for detecting the period during which all the outputs of a plurality of input circuits are in the same cycle and for producing a common effective signal during the same period, and a plurality of latch circuits for latching the outputs of the plurality of the input circuits during the common effective signal period. As an alternative, the inter-signal timing adjusting circuit includes a signal delay circuit for delaying the outputs of the plurality of the input circuits and a delay control register for detecting a signal most delayed among the outputs of the input circuits and controlling the amount of delay of the signal delay circuit in such a manner as to meet the need of the most delayed signal. For this adjustment to be carried out, it is necessary to change all the input signals in the same pattern and also to provide an adjust mode for this purpose. The phase difference between the outputs of the input circuits can also be detected by the control value of the input timing adjusting circuit inserted in each input circuit. In such a case, the inter-signal timing adjusting circuit can detect the phase difference between the output signals of the signal input circuits on the basis of the control value of the delay control circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the description as set below with reference to the accompanying drawings, wherein:

FIG. 1 is a diagram showing an example configuration of a semiconductor device system;

FIG. 2 is a diagram showing a basic configuration of a transmission system of a signal synchronous with a clock;

FIG. 3 is a diagram showing a configuration for clock synchronous transmission in a semiconductor device system;

FIG. 4 is a diagram showing an example of a conventional input circuit of a semiconductor device;

FIG. 5 is a diagram showing an example of correlation between a clock and other signals in a semiconductor device system;

FIG. 6 is a diagram showing an effective period attributable to the correlation between a clock and other signals in a semiconductor device system;

FIG. 7 is a diagram for explaining the problem points of a conventional semiconductor device system;

FIG. 8 is a diagram showing a basic configuration of the present invention;

FIG. 9 is a diagram for explaining the principle of phase judgement for the input signal retrieved according to the invention;

FIG. 10 is a diagram showing a basic configuration of a semiconductor device system according to a first aspect of the invention;

FIG. 11 is a diagram showing a basic configuration at the receiving end according to the first aspect;

FIG. 12 is a diagram showing a basic operation according to the first aspect;

FIG. 13 is a diagram showing a basic configuration of a semiconductor device at the receiving end according to a second aspect of the invention;

FIG. 14 is a diagram showing a basic configuration of a semiconductor device at the receiving end according to a third aspect of the invention;

FIG. 15 is a diagram showing a configuration of a clock generating circuit and an output timing adjusting section of a semiconductor device at the driving end according to a first embodiment of the invention;

FIG. 16 is a diagram showing a basic configuration of a shift clock generating circuit according to the first embodiment of the invention;

FIG. 17 is a diagram showing a configuration of a shift clock generating circuit according to the first embodiment;

FIG. 18 is a diagram showing a configuration of a clock generating circuit and an input circuit of a semiconductor device at the receiving end according to the first embodiment;

FIG. 19 is a diagram showing an example configuration of a delay circuit and a delay control circuit of a semiconductor device at the receiving end according to the first embodiment;

FIG. 20 is a diagram showing an example configuration of a latch circuit;

FIG. 21 is a time chart for explaining the operation of the first embodiment;

FIG. 22 is a diagram showing a configuration of an input section of a semiconductor device at the receiving end according to a second embodiment;

FIG. 23 is a diagram showing a configuration of a clock generating circuit according to the second embodiment;

FIG. 24 is a diagram showing a configuration of an input circuit according to the second embodiment;

FIG. 25 is a diagram showing a configuration of a phase judge circuit;

FIG. 26 is a diagram for explaining the phase judging operation according to the second embodiment;

FIG. 27 is a diagram for explaining the phase judging operation according to the second embodiment;

FIG. 28 is a diagram for explaining the phase judging operation according to the second embodiment;

FIG. 29 is a truth table for the phase judging operation according to the second embodiment;

FIG. 30 is a diagram showing an example configuration of a delay circuit and a delay control circuit of a semiconductor device at the receiving end according to the second embodiment;

FIG. 31 is a diagram showing a configuration of a clock generating circuit according to a third embodiment;

FIG. 32 is a diagram showing a configuration of an input circuit according to the third embodiment;

FIG. 33 is a diagram showing a configuration of an input circuit according to a fourth embodiment;

FIG. 34 is a diagram showing the operation modes according to a fourth embodiment;

FIG. 35 is a diagram showing the difference of the optimum timing due to the pattern of an input signal;

FIG. 36 is a diagram showing a configuration of an input circuit according to a fifth embodiment;

FIG. 37 is a diagram for explaining the phase judging operation according to the fifth embodiment;

FIG. 38 is a diagram showing a configuration of a phase judge circuit according to the fifth embodiment;

FIG. 39 is a diagram showing a truth table for a phase judge circuit according to the fifth embodiment;

FIG. 40 is a diagram showing a configuration of an input circuit according to a sixth embodiment;

FIG. 41 is a diagram showing a configuration of a timing correction circuit according to the sixth embodiment;

FIG. 42 is a diagram showing a configuration of a phase judge circuit according to the sixth embodiment;

FIG. 43 is a diagram showing a truth table for a phase judge circuit according to the sixth embodiment;

FIG. 44 is a diagram for explaining the problem points of the input circuit according to the invention shown in FIG. 8;

FIG. 45 is a diagram showing a change in the signal value within a clock cycle of the output of the input circuit according to the invention shown in FIG. 8;

FIG. 46 is a diagram showing a basic configuration according to a seventh embodiment of the invention;

FIG. 47 is a diagram showing a configuration of a semiconductor device at the receiving end according to the seventh embodiment of the invention;

FIG. 48 is a diagram showing an example configuration of a delay control circuit according to the seventh embodiment;

FIG. 49 is a diagram showing a configuration of a delay circuit and a latch pulse generating circuit according to the seventh embodiment;

FIG. 50 is a diagram for explaining the operation of the delay control circuit according to the seventh embodiment;

FIG. 51 is a diagram for explaining the principle of the input timing adjustment according to the seventh embodiment;

FIG. 52 is a diagram showing the operation of the input timing adjustment according to the seventh embodiment;

FIG. 53 is a diagram showing a general configuration of a semiconductor device according to the seventh embodiment;

FIG. 54 is a diagram showing the switching of the operation mode according to the seventh embodiment;

FIG. 55 is a diagram showing a modification comprising a signal terminal for indicating the timing adjustment;

FIG. 56 is a diagram showing the switching of the operation mode according to a modification;

FIG. 57 is a diagram showing a configuration of a semiconductor device at the receiving end according to an eighth embodiment of the invention;

FIG. 58 is a diagram showing a basic configuration of a semiconductor device at the receiving end according to a ninth embodiment of the invention;

FIG. 59 is a diagram showing a configuration of a semiconductor device at the receiving end according to the ninth embodiment;

FIG. 60 is a diagram showing the operation of input timing adjustment according to the ninth embodiment;

FIG. 61 is a diagram showing a configuration of a semiconductor device at the receiving end according to a tenth embodiment of the invention;

FIG. 62 is a diagram showing a configuration of a timing adjustment delay circuit according to the tenth embodiment of the invention;

FIG. 63 is a diagram showing the operation of input timing adjustment according to the tenth embodiment;

FIG. 64 is a diagram for explaining the problem points of a skew as long as not less than one clock cycle;

FIG. 65 is a diagram showing a configuration of a semiconductor device at the receiving end according to an 11th embodiment of the invention;

FIG. 66 is a diagram showing the operation of input timing adjustment according to the 11th embodiment;

FIG. 67 is a diagram showing the operation of input timing adjustment according to the 11th embodiment;

FIG. 68 is a diagram showing an input signal according to a 12th embodiment of the invention;

FIG. 69 is a diagram showing a configuration of a semiconductor device at the receiving end according to the 12th embodiment of the invention;

FIG. 70 is a diagram showing the operation of input timing adjustment according to the 12th embodiment;

FIG. 71 is a diagram showing the operation of input timing adjustment according to the 12th embodiment;

FIG. 72 is a diagram showing a configuration of a semiconductor device at the receiving end according to a 13th embodiment of the invention;

FIG. 73 is a diagram showing a configuration of a semiconductor device at the receiving end according to a 14th embodiment of the invention;

FIG. 74 is a diagram showing a configuration of an input circuit according to the 14th embodiment;

FIG. 75 is a diagram showing the operation of input timing adjustment according to the 14th embodiment;

FIG. 76 is a diagram showing a configuration of an input section of a semiconductor device according to a 15th embodiment of the invention;

FIG. 77 is a time chart showing the operation of the 15th embodiment;

FIG. 78 is a time chart for explaining the operation of the 15th embodiment;

FIG. 79 is a time chart for explaining the operation of the 15th embodiment;

FIG. 80 is a diagram showing a configuration of an input section of a semiconductor device according to a 16th embodiment;

FIG. 81 is a diagram showing a configuration of a clock distribution circuit, and an arrangement of a clock generating circuit, a signal input circuit and a dummy input circuit according to the 16th embodiment;

FIG. 82 is a diagram showing a configuration according to a 17th embodiment of the invention; and

FIG. 83 is a diagram showing the operation of the 17th embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Prior to the description of the preferred embodiments of the present invention, input timing in a synchronous DRAM

of a prior art will be described for a better understanding of the difference between the present invention and the prior art. The embodiments in which the present invention is adapted to a synchronous DRAM will be described later. As mentioned previously, the present invention is not limited to the synchronous DRAM but can apply to any semiconductor integrated circuit for receiving an input signal synchronously with an externally-input signal.

FIG. 1 is a diagram showing an example configuration of a typical conventional semiconductor device system. The system shown in FIG. 1 is for controlling the data input/output to and from a plurality of memories **12-0, 12-1, 12-2** by a controller **11**, and especially represents a configuration for writing data into the memories. As shown in FIG. 1, a clock signal line **12**, a control signal bus **14**, an address signal bus **15** and a write data bus **16** extending from the controller **11** are arranged in parallel. The memories **12-0, 12-1, 12-2** are arranged along these signal lines. Each of the terminals of the memories **12-0, 12-1, 12-2** is connected to a corresponding wire. In FIG. 1, the memories **12-0, 12-1, 12-2** are shown to be arranged above the signal lines and buses. Actually, however, the wiring is arranged to pass between the terminals of the memories **12-0, 12-1, 12-2**. A signal is output from the controller **11** to the clock signal line **13**, the control signal bus **14**, the address signal bus **15** and the write data bus **16**. Each memory retrieves the clock, generates an internal clock, retrieves the signals from the control signal bus **14**, the address signal bus **15** and the write data bus **16** on the basis of the internal clock thus generated, and after the required processing, stores the data output on the write data bus. The memories **12-0, 12-1, 12-2** are SDRAMs operating in accordance with the clock supplied from an external source.

FIG. 2 is a diagram showing an example of a most basic configuration of such a semiconductor device system as described above. As shown in FIG. 2, this system includes a semiconductor device **11** at the driving end for sending out a signal and a semiconductor device **12** at the receiving end for receiving the signal. Output signals D0 to Dn are output in synchronism with a clock signal CLK as well as the clock signal CLK from the semiconductor device **11** at the driving end. The signals sent from the semiconductor device **11** at the driving side in synchronism with the received clock CLK are retrieved as input signals Q0 to Qn by the semiconductor device **12** at the receiving end. The semiconductor devices making up the semiconductor device system transmit and receive signals to and from other semiconductor devices, and can therefore operate either at the driving end or at the receiving end depending on the operation involved.

FIG. 3 is a diagram showing in detail a route of signal transmission and receiving for the semiconductor devices at the driving and receiving ends. As shown in FIG. 3, the driving-end semiconductor device **11** outputs a clock signal CLK(D) from a clock output circuit **21**. Output signals D0, D1, . . . , Dn generated by a register **23** are output through output circuits **22-0, 22-1**, . . . , **22**-n, respectively. The receiving-end semiconductor **12**, on the other hand, includes a clock generating circuit **31** for generating an internal clock in response to the clock signal CLK, input circuits **32-0, 32-1**, . . . , **32**-n for retrieving input signals Q0, Q1, . . . , Qn corresponding to the output signals D0, D1, . . . , Dn, respectively, and a register **33** arranged for receiving these signals in an internal circuit for processing the outputs of the input circuits **32-0, 32-1**, . . . , **32**-n.

FIG. 4 is a diagram showing a conventional input circuit of a semiconductor device at the receiving end.

As shown in FIG. 4, an input circuit **32** has a clock current mirror circuit **41** supplied with a clock CLK input from an external source. The output of this circuit is transmitted as an internal clock to each part of the semiconductor device from a clock buffer circuit. In similar fashion, the input signal, after being input to the current mirror circuit **43**, is applied through an input signal buffer circuit **44** to a latch circuit **45**. The latch circuit **45** latches the input signal produced from the input signal buffer circuit **44** in synchronism with the rising edge of the internal clock from the clock buffer circuit **42**. The input signal thus is retrieved into the semiconductor device. The input signal thus latched at the latch circuit **45** is transmitted to each part of the internal circuit. The current mirror circuit is used for accurately receiving the signals input from an external source. In FIG. 4, only one input signal and only one input circuit are shown. Actually, however, a plurality of input signals are available, and there are as many input circuits as there are input signals, each input circuit including the current mirror circuit **43**, the input signal buffer circuit **44** and the latch circuit **45**.

In the circuit of FIG. 4, the clock input circuit and the input circuits for other input signals have an equivalent circuit configuration. The delay of the clock input to the semiconductor device and transmitted to the latch circuit **45** is set to the same as the delay amount of the input signal. The timing relation between the clock input to the clock input terminal of the semiconductor device and the other input signals can also be maintained by a latch circuit **135**.

FIG. 5 is a diagram showing a clock CLK and a signal on a bus in a semiconductor device system. The driving-end semiconductor device **11** changes the signal output to the control signal bus **14**, the address signal bus **15** and the write data bus **16** in synchronism with the rising edge of the clock CLK. In response to this, the receiving-end semiconductor device **12** retrieves the output signal of the driving-end semiconductor device **11** in synchronism with the rising edge of the clock CLK as an input signal. This specification describes a case in which the output signal is changed in synchronism with the falling edge of the clock CLK and retrieved as an input signal in synchronism with the rising edge of the clock CLK. Nevertheless, the input signal may be changed out of phase with the rising edge or the falling edge of the clock CLK and may be retrieved by the semiconductor device in an out-of-phase state.

In the case where a semiconductor device retrieves an input signal, a certain period is defined where the input signal is required to be established before and after the timing of retrieval. As shown in FIG. 5, the period during which the input signal is required to be established before the retrieval timing is called a setup time tS, and the time during which the input signal is required to be established after the retrieval timing is called a hold time tH.

FIG. 6 is a diagram showing a clock CLK and signals on the bus of a semiconductor device system of FIG. 2. The upper part of the drawing shows the clock CLK (D) and the output signals D0 to Dn produced from the driving end, and the lower part the state of these signals retrieved at the receiving end as the clock CLK (R) and the output signals Q0 to Qn. The driving-end semiconductor device **11** changes the output signals D0 to Dn in synchronism with the falling edge of the clock (D). The receiving-end semiconductor device **12** retrieves the output signals D0 to Dn as the input signals Q0 to Qn in synchronism with the rising edge of the clock signal retrieved.

In FIGS. 5 and 6, it is assumed that the output signals are changed at the falling edge of the clock CLK and are retrieved as input signals in synchronism with the falling edge of the clock CLK. Nevertheless, the input signals may

change and may be retrieved into the semiconductor device out of phase with the falling edge or the rising edge of the clock CLK. In the description that follows, however, it is assumed, for the simplicity of explanation, that the input signals are changed in synchronism with the falling edge of the clock CLK and the input signals are retrieved in synchronism with the rising edge of the clock CLK. The present invention, however, is not limited to such functions.

In the semiconductor device system shown in FIG. 2, the time of signal transmission from the driving-end semiconductor device **11** to the receiving-end semiconductor device **12** is defined by the length of the signal line on the one hand and is subject to change by the load of the signal line on the other hand. The length and the load cannot be exactly the same for different signals lines. As shown in FIG. **6**, therefore, even when an output signal is output from the driving end in such a manner as to change in synchronism with the falling edge of the clock, therefore, a phase difference occurs between the signals at the time point when the signals are input to the input terminal of the receiving-end semiconductor **12**. In FIG. **6**, time tD is required for the clock to be transmitted from the driving end to the receiving end. Specifically, the clock CLK (R) received is delayed by tD from the clock CLK (D) output from the driving-end semiconductor device **11**. The output signal D0 output from the driving-end semiconductor device **11** is transmitted with a smaller delay than the clock, and therefore the input signal Q0 changes more rapidly than the falling edge of the clock CLK (R). In a similar fashion, the change in the input signal Qn is delayed from the falling edge of the clock CLK (R). Assume that Q0 is most advanced, and that Qn is most delayed. During the period from the change of Q0 to the change of Qn shown in FIG. **6** represents the state where incorrect signal is input. During this period, therefore, the signal is not established. As a result, the period when the signal is effective is the period excluding the signal change, i.e., constitutes one clock period less the period during which the signal is not established.

FIG. **7** is a diagram for explaining the time required for signal establishment for the receiving-end semiconductor device. In the circuit of FIG. **4**, the latch circuit **45** naturally has a set-up time tS and a hold time tH required for the operation thereof. FIG. **7** shows such times as input establishment times required for circuit operation. As described above, the circuit of FIG. **4** includes the clock input circuit having a circuit configuration equivalent to the input circuit for the input signal so as to assure the same delay for the clock and the input signal from the time when they are input to the semiconductor device until they reach the latch circuit **45**. Actually, however, it is impossible to design exactly the same circuit, and therefore circuits and lines having some difference in delay amount are unavoidable in spite of efforts to equalize the delay amount as much as possible. Considering the variations in the fabrication process, the dependence of the delay amount on the temperature and the source voltage, therefore, there occurs a difference in delay even in the case where the clock input circuit is made equivalent to the input circuits for other input signals as shown in FIG. **4**. This difference in delay amount causes some variations in the time required for input establishment with respect to the rising edge of the clock CLK between conditions **1** and **2** as shown in FIG. **4**. Consequently, the input establishment time of FIG. **7** is required to be included in the effective signal time of FIG. **6**. In the case where this condition is not met, normal signal retrieval is impossible. In the prior art, the input establishment time, i.e., the set-up time tS and the hold time tH required by the circuit operation are defined taking these variations into consideration.

FIG. **8** is a diagram showing a basic configuration of a semiconductor device used at the receiving end according to this invention. The semiconductor device according to this invention, in order to achieve the above-mentioned object, comprises input timing adjusting circuits **54-0**, **54-1**, . . . **54-n** for adjusting the phase of the clock supplied to the input circuit to enable the input circuits **53-0**, **53-1**, . . . , **53-n** to retrieve the input signals in effective and stable state. In FIG. **8**, reference numeral **1** designates a clock input circuit, and numeral **5** designates an internal circuit supplied with the clock and the input signals retrieved by the input circuits **53-0**, **53-1**, . . . , **53-n**.

FIG. **9** is a diagram for explaining the principle of phase comparison for input signal retrieval. When the phases of two signals are compared, the temporal relation between a specific changing edge of one signal and that of the other signal are usually determined thereby to determine whether one signal is advanced or retarded with respect to the other signal. In the case of the input circuit, however, the input timing clock DCLK is a signal changing while the input signal is stable as shown in the drawing. The input signal is required to be stable before the set-up time tS when the input timing clock rises, and remains stable during the period from the rising edge of the input timing clock through the hold time tH. For this reason, the input signal is desirably changed $tP \times tS/(tS+tH)$ before the rising edge of the input timing clock, where tP represents one clock cycle. This input signal and the input timing clock DCLK cannot be compared in phase with each other at the changing edges thereof. In view of this, it is necessary that the input timing clock is displaced by a predetermined amount of phase to generate a shift clock SCLK changing in phase with the input signal, and the phase of this shift clock is compared with that of the input signal, or the input signal phase is displaced by a predetermined amount so that the phase of the input timing clock is required to be compared with that of the shift input signal. In the case where the shift clock SCLK or the displaced input signal are generated at the receiving end, the input signal can be retrieved by the input timing clock DCLK while comparing the phases thereof. Thus the feedback control can be continued after completion of the adjust mode. In the case where a signal displaced by a predetermined amount of phase is generated at the driving end, in contrast, a signal displaced by a predetermined amount of phase and having an operation different from a normal operation is required to be transmitted to the receiving end. In normal mode, such a signal cannot be transmitted. A signal displaced by a predetermined amount of phase can be generated at the driving end, therefore, only when the feedback control is not carried out after the adjust mode. In the case where an input signal displaced by a predetermined amount of phase is generated at the receiving end, the input signals received by a current mirror circuit and a buffer circuit are required to be used directly without being latched. A satisfactory comparison is impossible, however, because the input signal is dulled. When generating a signal displaced by a predetermined amount of phase at the receiving end, therefore, it is desirable to generate a shift clock. A possible alternative is to generate a shift clock at the driving end and transmit it in the adjust mode. However, the clock provides a reference for synchronous operation and different clock phases are not desirable even in the adjust mode. In the case where a signal displaced by a predetermined amount of phase is generated at the driving end, therefore, it is desirable to produce an output in synchronism with the shift clock in the adjust mode and to produce an output in synchronism with the clock in normal operation.

Now, an explanation will be given of a basic configuration of the present invention based on the foregoing description. First, in adjust mode, assume a configuration in which an output signal displaced by a predetermined amount of phase as compared with the signal in normal operation mode is output from the driving end.

FIG. 10 is a diagram showing a basic configuration of a semiconductor device system according to a first aspect of the invention. The semiconductor device at the driving end of this system includes a clock generating circuit for generating and selectively producing a clock and a shift clock displaced by a predetermined amount of phase from the first clock, and signal output circuits **88-0**, **88-1**, . . . , **88**-n for producing an output signal in synchronism with the clock or the shift clock generated by the clock generating circuit. This system can be selectively set either in normal mode for producing an output signal in synchronism with a clock, or in receiving-end timing adjust mode for receiving an output signal in synchronism with the shift clock. In FIG. **10**, the clock generating circuit includes a clock source **81** for generating a basic clock, a shift clock generating circuit **82**, and a switch **87** for selecting the basic clock or the shift clock among the clocks applied from the shift clock generating circuit **82** to the output circuits **88-0**, **88-1**, . . . , **88**-n. The system further comprises a dummy output circuit **84** for producing a signal in adjust mode suitable for adjusting the input timing adjusting circuit, and a switch **85** for selecting the output of the internal circuit **83** or the output from the dummy output circuit **84**. With this configuration, an output signal changing at the rising edge of the clock is produced in adjust mode, and an output signal changing with a predetermined amount of phase displaced from the rising edge of the clock is produced in a normal mode.

The shift clock generating circuit **82** includes a plurality of shift delay circuits having the same delay in each stage as a selectable amount, with the output of each stage being applied to the following stage, and with the first stage thereof supplied with the basic clock, a clock phase comparator for comparing the phase of the output in the last stage of the shift delay circuits with that of the basic clock, and a delay control circuit for controlling the delay amount of the plurality of shift delay circuits having a plurality of stages in such a manner that the phase of the output of the last stage coincides with that of the basic clock on the basis of the result of comparison at the clock phase comparator.

At the receiving end of the semiconductor device system according to the first aspect, the phase of the received clock is compared with that of the received input signal and the timing of retrieving the input signal is adjusted in adjust mode, while when entering the normal mode after the adjust mode, the control value at the end of the adjust mode is stored and continues to be held. The input signal sent from the driving end in the adjust mode is adapted to change at the rising edge of the clock and can be compared directly. Therefore, this signal can be used for determining the value retrieved by latching in the input circuit.

FIG. 11 is a diagram showing a basic configuration at the receiving end of the semiconductor device system according to the first aspect. As shown in FIG. 11, a phase comparator **70** includes a change information detection circuit **68** and a phase judge circuit **69**. The phase judge circuit **69** compares the phase of the value latched at the input latch **62** with the phase of the input signal detected by the change information detecting circuit **68** according to whether the input signal has changed, or, if changed, according to the direction of the changing edge involved. Especially, in the case where the input signal sent from the driving end in adjust mode changes per clock cycle, the change information detecting circuit **68** is not required to detect whether or not the input signal has undergone a change but only the direction of the changing edge.

FIG. **12** is a diagram showing an example of an output signal and a clock CLK produced from the driving end in normal mode and in the receiving time adjust mode (calibration mode) for the semiconductor device system according to the first aspect. The particular diagram shows the case in which the output signal changes per clock cycle in the adjust mode. As shown in FIG. **12**, the clock CLK is a signal remaining the same and continuous over both the calibration mode and the normal mode. The output signal is adapted to change for each rising edge of the clock in calibration mode. The output signal may change, but not always, in normal mode at the falling edge of the clock.

Now, a configuration will be explained in which the input timing adjusting circuit is controlled by feedback even after the adjust mode. In this case, the driving-end semiconductor device has the same configuration as the conventional device.

FIG. **13** is a diagram showing a basic configuration of a receiving-end semiconductor device according to the second aspect of the invention. As shown in FIG. **13**, this semiconductor device includes a clock generating circuit **51** supplied with an external clock ECLK for generating an internal clock CLK, an input circuit **53** having an input buffer **61** and an input lath **62**, and an input timing adjusting circuit **54** for adjusting the phase of the internal clock CLK supplied to the input latch **62** in such a manner that the input circuit may retrieve the input signal in effective and stable way. The input timing adjusting circuit **54** includes a delay circuit **64** with the delay amount thereof selectable for delaying the received internal clock CLK and producing it as an input timing clock DCLK, a phase comparator **66** for determining the phase of the input timing clock and the input signal, a delay control circuit **65** for changing the amount of delay of the delay circuit in such a manner that the input timing clock has a predetermined phase relationship with the input signal on the basis of the result of comparison at the phase comparator, and a shift clock generating circuit **70** for shifting the input timing clock by a predetermined amount of phase and generating a shift clock changing in phase with the input signal. The phase comparator **66** includes a dummy latch **67** for latching the input signal in synchronism with the shift clock, a change information detecting circuit **68** for detecting whether the input signal has undergone a change, and if so, the direction of such a change, and a phase judge circuit **69** for determining the phase on the basis of the result of detection at the change information detecting circuit **68** and the value latched at the dummy latch **67**.

The shift clock is a signal displaced by a predetermined amount of phase from the input timing signal, and in the case where the phase of the input timing signal is adjusted and changed, it must be changed accordingly. For this purpose, according to the second aspect, a shift clock is generated from the input timing signal output from the delay circuit of the input timing adjusting circuit. The shift clock generating circuit **70** can have the same configuration as the shift clock generating circuit **82** of FIG. **10**.

In a semiconductor device of clock synchronous type, on the other hand, a clock of a phase opposite to the internal clock is often used within the device and an internal clock exactly 180% out of phase is generated in many cases. In the case where the input signal changes 180% out of phase with the rising edge of the clock, i.e., in the case where the input

signal changes at the falling edge of the clock, then a clock of an opposite phase can be used as a shift clock. FIG. 14 is a diagram showing a basic configuration of a receiving-end semiconductor device according to a third aspect of the invention which is applicable in such a case. As shown in FIG. 14, this semiconductor device, unlike the device according to the second aspect, includes a shift clock generating circuit 71 for generating an opposite-phase clock /CLK exactly 180% out of phase with the internal clock CLK and comprises a delay circuit including two delay circuits, -1 and -2, for delaying CLK and /CLK by the same amount.

According to the second and third aspects described above, a shift clock with the input timing signal displaced by a predetermined amount of phase is generated at the receiving end, and the input signal, being the one in a normal mode, can be controlled by being fed back in a normal operation mode. The semiconductor devices according to the second and third aspects are applicable also in the case where the control value at the end of adjust mode is maintained after the adjust mode. In such a case, a signal suitable for operation of the input timing adjusting circuit is desirably output at the driving end.

Embodiments of the present invention will be described below. A first embodiment is associated with a semiconductor device system according to the first aspect shown in FIG. 10.

FIG. 15 is a diagram showing a configuration of a portion of the signal output circuit and the clock generating circuit of a driving-end semiconductor device of a semiconductor device system according to the first embodiment of the invention. The first embodiment, as shown in FIG. 12, can switch between both the normal mode and the receiving timing adjust mode. In starting the system, first, the timing is adjusted by setting to the receiving timing adjust mode, and then the normal mode is entered. Also, the normal mode is interrupted to transfer to the receiving timing adjust mode as required, in which case the normal mode can be restored again after the timing adjustment.

As shown in FIG. 15, the driving-end semiconductor device according to the first embodiment includes a clock source 81 for generating and supplying a clock CLK to each part of the device, a shift clock generating circuit 82 for generating and outputting a selected one of a basic clock providing the base of the output timing from the input clock CLK and a ½ shift clock shifted a one-half cycle from the basic clock, a delay adjusting circuit 83 for adjusting the delay amount of the clock produced from the shift clock generating circuit 82 and adjusting and outputting the output timing clock in such a manner that the output signal is synchronized with the clock produced to an external unit, a clock distribution circuit 87 with equidistant wirings for distributing the output timing clock among the output circuits, output circuits 88-1 to 88-n for producing a signal output from the output signal generating circuit 90 in synchronism with the output timing clock from the clock distribution circuit 87, the output signal generating circuit having a dummy signal generating circuit 91, a dummy current mirror circuit 62 for receiving the output signal input from the output circuit 88-0, and a dummy buffer circuit 93 for receiving the output of the dummy current mirror circuit 92 and applying it to the delay adjusting circuit 83. The delay adjusting circuit 83 includes a delay circuit 84 capable of adjusting the delay amount, a phase comparator 85 and a delay control circuit 86. The phase of the output signal input through the dummy current mirror circuit 92 and the dummy buffer circuit 93 is compared with that of the output timing clock produced from the shift clock phase shift circuit 82. The delay control circuit 86 adjusts the delay amount of the delay circuit 84 based on the result of comparison in such a manner that the phase of the output signal coincides with that of the output timing clock. As a result, regardless of the difference between the internal circuits, the output signal is produced in phase with the clock as shown in FIG. 9. The feature of the driving-end semiconductor device according to the first embodiment exists in the shift clock generating circuit 82, therefore, the remaining circuit components are not described.

Prior to the shift clock generating circuit 82 according to the first embodiment, an explanation will be given about a circuit for generating a clock displaced exactly by a predetermined amount of phase. FIG. 16 is a diagram showing a circuit configuration for generating a shift clock displaced by $2\pi i/N$ from the phase of the clock CLK. As shown in FIG. 16, a combination of a delay circuit A 101 and a buffer 102, a combination of a delay circuit B 103 and a buffer 104, . . . , a combination of a delay circuit N 105 and a buffer 106 having the same configuration are connected in N stages in series in such a manner that the output of the first stage is applied to the next stage. Each delay circuit is supplied with the same control value by the delay control circuit 108 and therefore the delay amount is changed at the same time, so that each delay circuit has the same delay amount. The phase comparator 107 compares the phase of the output of the buffer 106 in the last stage with that of the clock CLK. Based on the result of this comparison, the delay control circuit 106 changes the delay amount of the delay circuit in such a manner that the phase of the output at the last stage coincides with that of the clock CLK. In the case where the phase of the output at the last stage coincides with the phase of the clock CLK, the output at each stage is a signal having a phase shifted exactly 1/N of a cycle. Consequently it suffices if the output at any one of the stages is a clock displaced by a predetermined amount of phase, and the number of stages that causes such a phase displacement is determined. As described above, for the present purpose, the set-up time and the hold time are equal to each other. In a normal mode, therefore, the output signal changes in synchronism with the falling edge of the clock. Since the input circuit retrieves the input signal in synchronism with the rising edge of the clock, a shift clock 180% out of phase, i.e., a signal displaced by one half clock cycle serves the purpose, which can be realized by constructing two stages.

FIG. 17 is a diagram showing a configuration of the shift clock generating circuit 82 according to the first embodiment. A shown in FIG. 17, the shift clock generating circuit 82 includes first and second ½φ delay circuits 110 and 116 having the same configuration, an input stage 122, a phase comparator 125, a delay control circuit 126 and a mode selecting circuit 127. The first and second ½ delay circuits 110 and 116 each include input stages 111 and 117, respectively, identical to the input stage 122, delay circuits 114 and 120, respectively, adjustable in delay amount, and buffer circuits 115 and 121, respectively. The input stages 111, 117, 122 have current mirror circuits (CM) 112, 118, 123 and buffer circuits 113, 119, 124, respectively. The current mirror circuit is for retrieving the change in the input signal accurately.

The clock produced from the input stage 111 is delayed in the delay circuit A 114, then applied to the delay circuit B 120 through the buffer circuit 115 and the input stage 117, and thus delayed by the same amount as the delay circuit A 114. The resulting signal is applied to the phase comparator 125 through the buffer circuit 125 and the input stage 122.

value of the CLKC. The decoder 157 sets one of the outputs to H level and the other output to L level in accordance with the output of the up-down counter 156. In the case where the up-down counter 156 counts up, the output position associated with H level is shifted rightward, while the output position associated with H level is shifted to the left when the up-down counter 156 counts down. The output of the decoder 157 is connected to the remaining input terminal of each of the AND gates 152-1, 152-2, . . . , 152-n in that order, so that only the AND gate supplied with H signal from the decoder 157 is activated. Among the output signals of the inverter string, the signal applied to the activated AND gate is output as an internal clock DCLK. The number of stages of the inverter string affected is varied depending on the particular AND gate activated. In this way, the delay amount of the internal clock can be selected. The unit of adjustment for delay amount control is thus represented by each two inverters. By the way, the configuration shown in FIG. 19 can be used for the delay circuit and the delay control circuit shown in FIGS. 15 and 16.

FIG. 20 is a diagram showing a circuit configuration of the latch circuit 142. The dummy latch circuit 139 also has the same circuit configuration. This circuit configuration is widely known and will not be described.

FIG. 21 is a time chart for explaining the operation of the system according to the first embodiment. In the receiving timing adjust mode, the driving-end semiconductor device 11 outputs an output signal CD changing for every period in synchronism with the rising edge of the clock CLK (D). The left portion of the drawing shows the case in which such a signal is transmitted to the receiving-end semiconductor device 12 when the input signal CQ is delayed behind the clock CLK (R), and the right portion of the drawing shows the case in which the input signal CQ is transmitted earlier than the clock CLK (R).

Now, assume that the delay amount in the delay circuit 134 is equal to one clock period. The basic clock DCLK output from the delay circuit 134 is identical to the clock CLK (R) delayed by the delay amount of the clock input circuit 131. The current mirror circuit 140 and the buffer circuit 141 are identical to the clock current mirror circuit 132 and the clock buffer circuit 133 of the clock input circuit 131, respectively. The delay amount of the input signal CQ before being applied to the latch circuit 142, therefore, is the same as that for the clock input circuit 131. The phase relation therefore is the same as when the input signal CQ is retrieved at the rising edge of the clock CLK (R). For a similar reason, the dummy latch circuit 139 retrieves the input signal in synchronism with the falling edge of the clock CLK (R).

As shown in FIG. 21, the output signal CD changes for each period in synchronism with the rising edge of the clock CLK (D). Once it is known whether or not the input signal rises or falls, therefore, it is possible to judge whether the rising edge of the clock CLK (R) is advanced or retarded with respect to the changing edge of the input signal CQ by judging the signal value retrieved by the latch circuit 142 in synchronism with the rising edge of the clock CLK (R). When the input signal CQ rises, for example, the phase is delayed if the signal value is L, while it is advanced if the signal value is H. The relation is opposite when the input signal CQ falls. Since the input signal CQ changes for each period, judgement of the signal value one half period before can determine the manner in which the signal changes next. According to the first embodiment, this judgement is effected from the signal value DLD of the dummy latch circuit 139.

The outputs DLD and LD of the dummy latch circuit 139 and the latch circuit 142, respectively, undergo a change as shown in the drawing, so that the exclusive-OR CLKC of the DLD and LD changes in the manner shown in the drawing. Therefore, the judgement as to whether the count-up or the count-down is involved is required to be made after DCLK rises and LD changes before DCL rises and DLD changes. According to the first embodiment, as shown in FIG. 19, the counting operation of the up-down counter 156 is performed in accordance with the value of CLKC when the clock ϕ½D rises. Specifically, judgement is made at the timings indicated by arrows at the portion of CLKC in FIG. 21. In the case where the input signal CQ on the left side is delayed from the clock CLK (R), therefore, the CLKC is "L". Since the basic clock CLK2 is advanced, the up-down counter 156 is counted up and the delay amount in the delay circuit 134 is increased. In the case where the input signal CQ on the right side is advanced of the clock CLK (R), on the other hand, CLKC is "H", so that the up-down counter 156 is counted down thereby to reduce the delay amount in the delay circuit 134. The count-up and the count-down operations are repeated until the out-of-phase condition is eliminated, and then the count-up and the count-down are repeated. When the mode select signal is switched to normal mode under this condition, the application of the clock to the up-down counter 156 is interrupted by the AND gate of FIG. 19. Thus the up-down counter 156 holds the count. The condition is the one in which the rising edge of the delay clock DCLK coincides with the changing edge of the input signal.

In a normal mode, the output signal CD output from the driving-end semiconductor device 11 is switched to change in synchronism with the falling edge of the clock CLK (D). As explained with reference to FIGS. 16 and 17, it is possible to displace it by exactly one half period. The rising edge of the clock CLK (D), therefore, is located in the middle of the changing edge of the output signal CD. In the receiving-end semiconductor 12, the rising edge of the DCLK is adjusted in the manner described above. When the input signal is displaced by one half period, therefore, the rising edge of DCLK is situated in the middle of the changing edge of the input signal CQ. As a consequence, the period during which the input signal is required to be stable is the sum of the time lengths required for the latch circuit 142 to set up and hold. Thus the period during which the input signal is required to be stable can be minimized. As a result, the clock frequency can be increased until the clock period is equal to this time, thereby making it possible to increase the operation speed.

The first embodiment refers to the case including the receiving timing adjust mode. Now, explanation will be made about the second embodiment, in which the receiving timing adjust mode is not provided but the receiving timing is constantly adjusted in normal mode. In the second embodiment, therefore, the driving-end semiconductor device can produce an output signal in synchronism with the clock and can have a configuration shown in FIG. 15 lacking the shift clock generating circuit 82.

FIG. 22 is a diagram showing a configuration of the receiving section of the receiving-end semiconductor device according to the second embodiment. The second embodiment corresponds to the third aspect of the invention shown in FIG. 14.

The receiving-end semiconductor device according to the second embodiment includes a clock generating circuit 202 for retrieving the clock ECLK input to the terminal 201 from the driving-end semiconductor device and generating an

internal clock $\phi 1$ and a ½ shift clock ϕ½ displaced by one half period from the internal clock $\phi 1$, and input sections **204-0**, **204-1**, . . . , **204**-n for retrieving the input signals D0 to Dn synchronous with the clock ECLK input to the terminals **203-0** to **203**-n, respectively.

FIG. **23** is a diagram showing a configuration of the clock generating circuit **202**. In FIG. **23**, reference numerals **210**, **216**, **222** designate input circuits **1**, **2**, **3**, respectively, having the same configuration, numerals **213**, **219** delay circuits A, A1, respectively, having the same configuration, numerals **214**, **220** auxiliary delay circuits B, B1, respectively, having the same configuration, numerals **215**, **221** buffer circuits having the same configuration, numeral **225** a phase comparator, and numeral **226** a delay control circuit. As is clear from the diagram, the clock generating circuit **202** has substantially the same configuration as the shift clock generating circuit shown in FIG. **17**, except that the select circuit **127** is lacking, that both $\phi 1$ and ϕ½ are produced, that the buffers **115**, **121** are replaced by the auxiliary delay circuits **214**, **220**, respectively, and that the outputs of the delay circuits **213**, **219** are output through the buffers **215**, **221**, respectively. The clock generating circuit shown in FIG. **23** can also produce a clock signal exactly one half period out of phase like the shift clock generating circuit shown in FIG. **17**.

FIG. **24** is a diagram showing a configuration of each input section of the second embodiment. As shown, the input section has a configuration similar to that of the corresponding configuration shown in FIG. **18**. The difference lies, however, in that separate delay circuits **231** and **232** are provided in order to adjust the phases of the clocks $\phi 1$ and ϕ½ and in that the EXOR gate **143** is replaced by a latch circuit **240** and a phase judge circuit **241**.

In the input circuit according to the second embodiment, the input signal is normally retrieved in synchronism with the clock $\phi 1$, while the input signal for judging the out-of-phase condition is retrieved by a dummy input circuit in synchronism with the clock **100** ½. Consequently, the clock $\phi 1$ and the clock ϕ½ supplied to the latch circuit are required to be out of phase with each other by one half period exactly. For this purpose, the delay circuits **231** and **232** are controlled in common by the delay control circuit **233** to have the same delay amount, so that the clocks output from the delay circuits **231** and **232** maintain relative phases exactly one half period out of phase with each other. As a result, the signal value retrieved by the dummy input circuit can be judged in synchronism with the clock ϕ½ to thereby judge the out-of-phase condition.

The input signal is a normal signal. It changes at every rising edge as in the first embodiment, but it may or may not change so in the second embodiment. As a result, according to the second embodiment, a signal value one half period displaced is detected before and after the rising edge of the clock ϕ½, and by judging the three signal values, it is judged whether the input signal has changed or not, and if it has changed, the direction in which it has changed and the direction of phase shift. The signal value at the time point one half period displaced before and after the rising edge of the clock ϕ½ represents an input signal normally retrieved and therefore utilizes the output of the latch circuit **239**. The signal value retrieved at the time point one half period displaced in a forward direction in the first half period undesirably undergoes a change if an input signal is retrieved at the time point one half period displaced backward in the last half period. It is therefore necessary to store the signal value before the change and hold it for one period. The latch circuit **240** has this function. It stores the signal value immediately before the output change of the latch **239** in synchronism with the rising edge of $\phi 1$, and holds it for one period before the next rising edge of $\phi 1$. The phase judging circuit **241** is a circuit for judging whether the input signal has changed or not, and if changed, the direction of change and the direction of phase shift, from the three signal values including the rising edge of the clock ϕ½ and the two time points one half period displaced before and after it. The signal value at the time point one half period displaced in forward direction is RG0, the signal value at the rising edge of the clock ϕ½ is RG1, and the signal value at the time point one half period displaced backward is RG2.

FIG. **25** is a circuit diagram showing a configuration of a phase judging circuit **241**. The operation of the phase judging circuit **241** will be explained with reference to FIGS. **26** to **29**.

As long as there is no out-of-phase condition, the input signal changes at the falling edge of $\phi 1$. The state 1 represents the time point when the input signal remains unchanged at "H". Under this condition, RG0, RG1, RG2 are all "H", and the out-of-phase condition cannot be judged, so that no counting operation is performed. In similar fashion, the state 2 represents the time when the input signal remains unchanged at "L", when all of RG0, RG1, RG2 are "L". The out-of-phase condition cannot be judged also in this case, and therefore no counting operation is performed.

The states 3 and 4 shown in FIG. **24** represent the case in which the input signal changes from "H" to "L". In the case where the changing edge of the input signal is delayed behind the rising edge of ϕ½ as in the state 3, RG0, RG1, RG2 assume "H", "H" and "L", respectively. In such a case, the delay amount of the delay circuits **231** and **232** is increased. In the case where the changing edge of the input signal is advanced of the rising edge of ϕ½ as in state 4, on the other hand, RG0, RG1, RG2 assume "H", "L", "L", respectively. In this case, the delay amount of the delay circuits **231** and **232** is reduced.

The states 5 and 6 shown in FIG. **28** represent the case in which the input signal changes from "L" to "H". In the case where the changing edge of the input signal is delayed behind the rising edge of ϕ½ as in state 5, RG0, RG1, RG2 assume "L", "L", "H", respectively. In such a case, the delay amount of the delay circuits **231** and **232** is increased. In the case where the changing edge of the input signal is in advance of the rising edge of ϕ½ as in state 6, on the other hand, RG0, RG1, RG2 assume "L", "H", "H", respectively. In such a case, the delay amount of the delay circuits **231** and **232** is reduced.

FIG. **29** is a table showing each of the abovementioned states, the associated values of RG0, RG1, RG2 and the required operation.

The phase judging circuit of FIG. **25** outputs a "L" signal as a hold signal and a "H" signal as an up/down signal in states 1 and 2, and a "H" signal as a hold signal in states 3 to 6. In addition, it outputs a "H" signal for indicating the count-up as an up/down signal in states 3 and 5, and a "L" signal for indicating the count-down as an up/down signal in states 4 and 6.

FIG. **30** is a diagram showing a configuration of the delay circuit **231** and the delay control circuit **233** according to the second embodiment. As shown in FIG. **24**, these circuits have the same configuration as the delay circuit **231**. A delay circuit **232**, though not shown, has the same configuration as the delay circuit **231** and is controlled by the same control value as the delay control circuit **233**. As shown in FIG. **30**, this configuration is similar to that of FIG. **19**, the difference

being that an up/down signal is applied as a CLKC, a hold signal is input in place of the mode select signal, and the clock ϕ½ output from the delay circuit **2** and frequency-divided by the frequency divider **159** is input in place of ϕ½D. Some time is required before the delay amount in the delay circuit **134** is changed by the arithmetic operation in the phase judge circuit **241** and the operation of changing the control value at the decoder **157** and the up/down counter **156** based on the result of calculation in the phase judge circuit **241**. In the case where this time is longer than the one-half period, the delay amount based on the judgement is actually changed after the next judgement, thereby causing a time delay of feedback operation. This time delay of feedback would cause a periodical fluctuation of the delay amount in the time range corresponding to the two stages of the delay circuit where the phases almost coincide with each other. According to this embodiment, the clock ϕ**1** is applied after being frequency-divided in the frequency divider **159** in order to obviate this problem. As a result, only one feedback is executed for each group of clocks, and no problem occurs.

The input circuit of a semiconductor device according to the second embodiment constantly performs the operation of adjusting the out-of-phase condition during the operation of the semiconductor device. During the operation of the semiconductor, the out-of-phase condition is thus always adjusted. Even in the case where there occurs any difference in delay amount due to temperature changes or the like, therefore, the adjustment for preventing the out-of-phase condition is automatically carried out. The input circuit of the semiconductor device according to the second embodiment requires no process of switching the mode. In view of the possibility of a large displacement occurring immediately after starting the system, however, it is necessary to provide an appropriate initialization period corresponding to an appropriate number of clocks for calibration. According to the second embodiment, therefore, an initialization time is set which is longer than the number of clocks required for convergence from the maximum displacement, and a dummy signal generating circuit is inserted in the driving-end semiconductor device, so that a periodically-changing dummy signal suitable for the adjustment of the receiving timing is output during the initialization period. The receiving-end semiconductor device adjusts the input timing adjusting circuit based on this dummy signal during the initialization period, and adjusts the input timing adjusting circuit by a normal input signal after the initialization period.

FIG. **31** is a diagram showing a clock generating circuit of the receiving-end semiconductor device according to a third embodiment, and FIG. **32** is a diagram showing a configuration of the input section of the receiving-end semiconductor device according to the third embodiment. The third embodiment represents the case in which the input circuit and the clock generating circuit according to the second embodiment are partially modified, and has the same basic configuration as the second embodiment.

As shown in FIG. **31**, the clock generating circuit according to the third embodiment is similar to the clock generating circuit according to the second embodiment shown in FIG. **23** lacking the input circuits **216** and **222**. Since the two input circuits **216** and **222** are removed at the same time, the route leading from the delay circuit **253** to the delay circuit **256** is identical to the route leading from the delay circuit **256** to the phase comparator **259**, so that the clock ϕ**1** and the clock ϕ½ displaced from the clock ϕ**1** by exactly one half period are output. The current mirror circuit is used for retrieving the signal with accurate timing. The present invention in which the phase is adjusted, however, is relatively free of this restriction and can be done without the current mirror circuit.

As shown in FIG. **32**, the input section according to the third embodiment (including the input circuit and the input timing adjusting circuit) constitutes a circuit lacking the current mirror circuit **237**, the buffer circuit **238**, the dummy current mirror circuit **234** and the dummy buffer circuit **235** included in the input section of the second embodiment shown in FIG. **24**. Instead, it includes a ϕ delay circuit **276** in place of the latch circuit and also a delay circuit **278** for adjusting the timing of the counting operation in accordance with the result of judgement at the delay control circuit **273**.

As described above, the current mirror circuit is used for retrieving the signal with accurate timing. According to the present invention, in contrast, the phase is adjusted, and therefore the need of the current mirror circuit is reduced and therefore eliminated. The current mirror circuit in which current constantly flows consumes a large power. The elimination of the current mirror circuit, therefore, can reduce the power consumption.

The second embodiment is such that the clock ϕ**1** is frequency-divided by a frequency divider circuit to prevent the problem which otherwise might be posed by the feedback delay. According to the third embodiment, in contrast, an appropriate timing signal is generated by the delay circuit **278**, and this timing signal is used to perform the up/down counting operation. Therefore, the feedback delay is reduced and no such problem as described above occurs.

In the second and third embodiments, the clock generating circuit generates an internal clock and a shift clock just one half period displaced from the internal clock, and the input timing adjusting circuit includes two delay circuits for delaying the two clocks, respectively. It is also possible to generate a shift clock just one half period displaced from the output of the delay circuit for adjusting the input timing as according to the second aspect of the invention shown in FIG. **13**. The fourth embodiment is such an example.

FIG. **33** is a diagram showing a configuration of an input circuit and an input timing adjusting circuit according to the fourth embodiment. The input circuit and the input timing adjusting circuit according to the fourth embodiment, as shown, have a configuration similar to the corresponding circuits of the second embodiment shown in FIG. **24**. The difference, however, lies in that the present embodiment has only one delay circuit and includes a shift clock generating circuit **289** for generating a shift clock from the output of the delay circuit, that the dummy latch **284** is supplied with the output of the buffer circuit **287** of the input circuit without the dummy current mirror circuit and the dummy buffer circuit, and that a control value monitor circuit **290** is provided for monitoring whether or not the control value of the delay control circuit **282** has ceased to change or not. The same shift clock generating circuit **289** as the described above is used. The input circuit and the input timing adjusting circuit according to the fourth embodiment operate substantially the same way as the corresponding circuits of the second embodiment except for the above-mentioned points.

As described above, in the circuit according to the second embodiment, a sufficiently long initialization period is inserted after starting the system so that the control value may converge within the initialization period from the state which may be displaced to a maximum. According to the fourth embodiment, the control value monitor circuit **290** checks for the fluctuations of the control value of the delay

control circuit 282. In the case where the input timing signal is set in optimum state, the control value of the delay control circuit 282 is considered to cease to change. If the continuation of the same control value is detected by the control value monitor circuit 290, therefore, it is judged that the input timing signal is set in optimum state.

FIG. 34 is a diagram showing an operation mode according to the fourth embodiment. With the start of the system, a power-on reset signal is produced to thereby start the initialization mode (calibration mode). In the calibration mode, the driving-end semiconductor device produces a signal of a value changing in predetermined cycles. The receiving-end semiconductor device, upon receipt of this signal, changes the control value of the input timing adjusting circuit gradually to an optimum timing. Once the input timing is optimized, as described above, the control value of the delay control circuit 282 ceases to change. The control value monitor circuit 190 thus detects that the same control value is generated continuously and turns on the control value monitor signal. In response to this, the system switches the mode signal to normal mode for starting the normal operation. The input timing adjusting circuit of the receiving-end semiconductor device, even after entering the normal mode, compares the phase of the input signal and on the basis of the comparison result, continues the feedback control.

In the first to fourth embodiments described above, the phases of the input signal and the input timing signal are compared by judging the value of the input signal actually retrieved to attain the optimum timing. In the case where the clock period has become very short, however, the optimum input timing develops a difference between when the input signal changes every clock cycle and when the same value is continued.

FIG. 35 is a diagram for explaining this problem. The solid lines represent the level change of the input signal with the input signal undergoing a change in every clock cycle, and the dashed lines the level change of the input signal with the same value continued. As shown, when the input signal changes every clock cycle, the input signal begins to change to the next level before reaching to a sufficient level. Specifically, the input signal changes only up to midway of the level, resulting in a small amplitude. In the case where the input signal continues with the same value, on the other hand, the input signal reaches a sufficient level. In the case where a signal that has reached a sufficient level assuming the same value undergoes a change, the amplitude changes greater than in the case where the input signal changes in the immediately preceding two cycles and reaches only up to midway of the level. Thus the time before changing while passing the intermediate level is delayed. Consequently, the phase comparison at the falling edge of the clock CLK develops a difference by the amount of the delay between when the input signal value changes and when the input signal value remains the same in the immediately preceding two cycles. As a result, a displacement occurs by the amount of the delay as shown depending on the type of the input signal pattern for which the input timing is adjusted. Also, as shown, the optimum timing for retrieving the changing input signal is different when the input signal value changes in the immediately preceding two cycles than when the input signal value remains the same during the same period.

According to a fifth embodiment, the problem of the difference in the input timing adjustment due to the input signal pattern is solved by comparing the phases and correcting the result of comparison by feedback only when the input signal value changes in the immediately preceding two cycles.

FIG. 36 is a diagram showing a configuration of the input circuit and the input timing adjusting circuit of the receiving-end semiconductor device according to the fifth embodiment. As shown in FIG. 36, the input circuit and the input timing adjusting circuit according to the fifth embodiment, which are similar to the input section of the second embodiment shown in FIG. 24, includes a latch 307 for further latching the output of the latch 306, and the output of the latch 307 is applied as RG3 to the phase judge circuit 308. The latch 307, like the latch 306, retrieves the output of the latch 306 in synchronism with the input timing signal output by the delay circuit 1. The latch 307 thus displays the function of holding the output of the latch 306 for another one clock cycle. Also, the output signal of the delay circuit 301 delayed by the delay circuit 309 is applied as a timing signal for changing the control value of the delay control circuit 303 in a manner similar to the input section according to the third embodiment shown in FIG. 32.

FIG. 37 is a diagram for explaining the relation between the input signal pattern, the values retrieved by each latch and the phase judgement according to the fifth embodiment. The latches 305, 306, 307 retrieve the input signal and the output of the preceding stage, respectively, in synchronism with an input timing signal and output them as RG2, RG0, RG3, respectively. The latch 304 retrieves the input signal at a timing just one half period displaced from the input timing signal and outputs it as RG1. The relations, therefore, between RG0, RG1, RG2, RG3, are as shown. Character Qa designates an input signal that remains unchanged at "high" (H) or "low" (L), and character Qb an input signal that has changed in the immediately preceding cycle but one but has remained unchanged in the immediately preceding cycle. Characters Qc and Qd, on the other hand, designate input signals that have not changed in the immediately preceding cycle but have changed in the immediately preceding cycle. Character Qc represents the case in which the phase of the input timing signal DCLK is advanced, while Qd the case in which the phase of the input timing signal DCLK is delayed. Characters Qe and Qf represent the case in which the input signal has changed successively in the immediately preceding two cycles, Qe the case in which the phase of the input timing signal DCLK is advanced, and Qf the case in which the phase of the input timing signal DCLK is delayed. As described above, according to the fifth embodiment, the phase comparison and the feedback correction are carried out only when the input signal value changes in the immediately preceding two cycles. As for the input signal Qe, therefore, the control value of the delay control circuit 303 is changed in such a manner as to delay the input timing signal DCLK, and as for the input signal Qf, the control value of the delay control circuit 303 is changed in such a manner as to advance the input timing signal DCLK. As for other input signals, the control value of the delay control circuit 303 is held.

FIG. 38 is a circuit diagram showing a phase judging circuit 308, and FIG. 39 a truth table therefor. The truth table of FIG. 39 is derived from the circuit of FIG. 38. Only in the case where the input signal is Qe or Qf in FIG. 37, therefore, the hold signal assumes a "low" (L) level, so that the control value of the delay control circuit 303 is changed in accordance with the up/down signal. In the case where the input signal assumes any one of Qa to Qd, on the other hand, the hold signal turns "high" (H) thereby to hold the control value of the delay control circuit 303.

As described above, the optimum timing for retrieving the changing input signal is differentiated between when the input signal value changes in the immediately preceding two

cycles and when the input signal remains the same value in the same two cycles. According to a sixth embodiment, as in the fifth embodiment, the input timing is adjusted, and if the input signal assumes different values in the immediately preceding two cycles, the input signal is retrieved in synchronism with the particular input timing signal. In the case where the input signal remains the same during the immediately two preceding cycles, in contrast, the next input timing signal is retrieved by delaying it by a predetermined amount.

FIG. **40** is a diagram showing a configuration of an input circuit according to a sixth embodiment. The difference of this embodiment from the fifth embodiment shown in FIG. **36** resides in that the present embodiment further includes a switch **310** and a correction delay circuit **311**, and that the input timing signal DCLK supplied to the latch **305** can be selectively delayed by a predetermined amount in accordance with a compensation control signal H1. FIG. **41** is a diagram showing a configuration of the switch **310** and the compensation delay circuit **311** according to the sixth embodiment. Transfer gates **321**, **322** and an inverter **323** make up the switch **310**, and two inverters **324** and **325** constitute the compensation delay circuit **311**. The compensation control signal H1 output from the phase judge circuit **308** assumes a L level when the input signal value has changed in the immediately preceding two cycles, and a H level when it remains the same value. When the correction control signal H1 is at L level, the transfer gate **322** opens, so that the input timing signal DCLK is applied to the latch **305** directly without being delayed. In the case where the compensation control signal H1 is at H level, on the other hand, the transfer gate **321** opens and therefore the input timing signal DCLK is input to the latch **305** after being delayed by the amount corresponding to the two inverters **324** and **325**.

FIG. **42** is a diagram showing a configuration of the phase judge circuit **312** according to the sixth embodiment. FIG. **43** is a truth table of this circuit. Comparison between FIGS. **38** and **39** shows that the phase judge circuit **308** of the fifth embodiment has an added function of judging whether or not the input signal value is different in the immediately two preceding cycles. As to Qa, Qc and Qd for which the input signal value is different in the immediately preceding two cycles, the correction control signal H1 assumes a H level, while in the case of Qb, Qe and Qf for which the input signal value remains the same in the immediately preceding two cycles, on the other hand, the compensation control signal H1 assumes a L level.

In the first to sixth embodiments described above, the receiving-end semiconductor device has a basic configuration shown in FIG. **8**, and includes an input timing adjusting circuit for each input circuit, by which each input signal can be retrieved at optimum timing. This in turn poses the problem of different phases of the signals output from the input circuits. FIG. **44** is a diagram for explaining this problem. In FIG. **44**, input signals as applied to input circuits **53-0**, **53-1**, . . . , **53**-n are assumed to be Q0, Q1, Q2, and output signals of the respective input circuits as applied to the internal circuit **55** are assumed to be Q00, Q10, Q20, respectively. When the phases of the input signals Q0, Q1, Q2 are displaced as shown, the input timing adjusting circuits **54-0**, **54-1**, . . . , **54**-n adjust the phase of the internal clock in such a manner that the input circuits **53-0**, **53-1**, . . . , **53**-n retrieve the input signals Q0, Q1, . . . , Qn at a most appropriate timing. The phase of the signals Q00, Q10, Q20 diagram showing the cycles taken by the signals **Q00**, **Q10**, **Q20** in one clock cycle. Characters t0 to t4 designate the timing shown in FIG. **44**. As shown in FIG. **45**, during the period of t0 to t1, Q00 and Q20 take the forms of Q0B and Q2B, respectively, having the same cycle, while Q10 assumes the form Q1A of the previous cycle. In similar fashion, during the period of t2 to t3, Q00 and Q10 assume the form of signals Q0B and Q1B having the same cycle, while Q20 is a signal Q2C in the next cycle. If the internal circuit **55** executes the process based on the signals between t0 and t1 or between t2 and t4, different sets of signals would be processed, leading to the problem of a processing error.

The embodiment explained below solves this problem. Specifically, even when the clock is out of phase with the signal at the receiving end, or even when a phase difference develops between the clock input circuit and an input circuit for other signals in the semiconductor device at the receiving end, fast delivery of signals becomes possible.

FIG. **46** is a diagram showing a basic configuration of a semiconductor device according to a seventh embodiment of the invention. As shown in FIG. **46**, the semiconductor device according to the seventh embodiment includes, in addition to the basic configuration of the invention shown in FIG. **8**, an inter-signal timing adjusting circuit for detecting the phase difference between output signals of the input circuits and adjusting them to be in phase with each other. The semiconductor device system according to the seventh embodiment is assumed to take the form as shown in FIG. **3**.

FIG. **47** is a diagram showing a configuration of a clock input circuit, input sections and an inter-signal timing adjusting circuit of the receiving-end semiconductor device according to the seventh embodiment.

As shown in FIG. **47**, the receiving-end semiconductor device according to the seventh embodiment includes a clock input circuit **142** supplied with a clock transmitted from the driving-end semiconductor device for generating internal clocks ϕ and ϕ½, input sections **144-0**, **144-1**, . . . , **144**-n for retrieving as an input signal thereto the signal transmitted from the driving-end semiconductor device, an AND gate **401** for calculating the logic product of the outputs of the input sections, a delay circuit **402**, a delay control circuit **403**, a latch pulse generating circuit **404**, and latch circuits **405-0**, **405-1**, . . . , **405**-n for latching the outputs of the input sections **144-0**, **144-1**, . . . , **144**-n in accordance with the latch pulse QSYN output from the latch pulse generating circuit **404**. The clock input circuit **142** and the input sections **144-0**, **144-1**, . . . , **144**-n are identical to the corresponding ones of the second embodiment. The clock input circuit **142** has a configuration as shown in FIG. **23**, and each input section has a configuration as shown in FIG. 24. As a result, the input circuit of the semiconductor device according to the seventh embodiment can constantly adjust the out-of-phase condition during the operation of the semiconductor device. In the seventh embodiment, however, the adjusting operation is performed only when the mode signal is input and indicates the input timing adjust mode.

FIG. **48** is a diagram showing a configuration of the delay control circuit **403** shown in FIG. **47**. FIG. **49** is a diagram showing a configuration of the delay circuit **402** and the latch pulse generating circuit **404**. FIG. **50** is a time chart showing the operation of the delay control circuit **403**. As shown in FIG. **47**, the output QAND of the AND gate **401** assumes a H level when all the outputs Q00, Q10, . . . , Qn1

changes in such a pattern that it assumes a H level only in specific cycles with successive L levels. If all the outputs **Q00**, **Q10**, . . . , **Qn1** assume a H level in the cycle portion when the input signal is at H level, the output pulse QAND assume a H level. The rising edge of this output QAND represents the timing when the most delayed input signal rises. The period when QAND remains H represents a period during which the outputs **Q00**, **Q10**, . . . , **Qn1** are all signals of the same cycle. Once the outputs of the input sections **144-0**, **144-1**, . . . , **144**-n are latched by the latch circuits **405-0**, **405-1**, . . . , **405**-n, respectively, during this period, therefore, it follows that all the outputs become uniform. The signals a**0**, a**1**, . . . , am shown in FIG. **48** are progressively delayed and undergo a change as shown in FIG. **50**. With the rise of the output QAND, a flip-flop F/F latches the signals a**0**, a**1**, . . . , am. The values latched so, however, are different depending on the timing when the output QAND rises. Among the signals b**0**, b**1**, . . . , bm in FIG. **48**, for example, those up to b**1** are H, while subsequent signals assume a L level. Upon application of these signals to the NOR gate

a mode register/decoder **415**, and an inter-signal timing adjusting circuit **416**. The corresponding circuits according to the first embodiment described above are applied to the data signal input circuit section **414** and the inter-signal timing adjusting circuit **416**. As described earlier, the SDRAM is required to process the input and output of data signals at high speed, while the control signals and address signals are not required to be processed at such a high speed but at a lower speed, compared with the data signals. Thus, the mode indication signal is made of a combination of signals applied at signal terminals at comparatively low speed, i.e., a combination of a control signal and an address signal. The mode register/decoder **415** judges whether or not the control signal has instructed a mode register to be set, followed by judging a specific process from the value of the address signal.

FIG. **54** is a diagram for explaining the judgement of the operation mode and the input timing adjust mode according to the seventh embodiment. As shown in FIG. **54**, the mode

different logic value only during a specific one of the cycles when the logic value remains the same.

The data signal is required to be input to and output from the SDRAM at high speed, while the other signals including control signals and address signals can be input or output with a lower speed than the data signals. In view of this, a mode indication signal can be produced by combining the signals input to signal terminals at comparatively low speed, i.e., by combining the values of the input signals having a long period. Also, a dedicated input signal terminal may be provided for applying the mode indication signal. The mode indication signal can be a reset signal, for example. An arrangement can thus be made in which upon receipt of a reset signal, the adjust mode is entered automatically for a predetermined length of time. In such a case, the input signal of a predetermined signal pattern desirably continues to be applied during a predetermined length of time after an instruction is given to terminate the receiving timing adjust mode.

FIG. **58** is a diagram showing a basic configuration of a semiconductor device according to a ninth embodiment of the invention. As shown in FIG. **58**, the semiconductor device according to the ninth embodiment of the invention includes an input circuit section having a plurality of input buffers **441-0**, **441-1**, . . . , **441-n** such as current mirror circuits, and also a timing adjust input circuit **443** for retrieving the output of each input buffer with the delay amount thereof adjusted in such a manner as to enable the output of each input buffer to retrieve a predetermined internal clock optimally. The timing adjust input circuit **443** includes each of timing adjusting circuits **445-0**, **445-1**, . . . , **445-n** for adjusting the input signal timing, and each of timing control circuits **444-0**, **444-1**, . . . , **444-n** as a combination, respectively, for each input signal. This combination specifically includes a delay circuit with a selectable delay amount for delaying the outputs of the input buffer circuits **441-0**, **441-1**, . . . , **441-n**, a signal input circuit for retrieving the outputs of the input buffer circuits in synchronism with an internal clock, a phase judge circuit for judging the phase of the outputs of the input buffer circuits mirror circuits **452-0**, **452-1**, . . . , **442-n** are arranged in the vicinity of signal terminals, and the timing latch circuits **454-0**, **454-1**, . . . , **454-n** are arranged in the vicinity of the inter-signal timing adjusting circuit **455**. Accordingly, the shift clock generating circuit **453** is also desirably arranged in the vicinity of the timing latch circuits **454-0**, **454-1**, . . . , **454-n**.

FIG. **60** is a diagram for explaining the input timing adjustment according to the ninth embodiment. The operation of this embodiment is different from that of the seventh embodiment shown in FIG. **52** only in that the input signals are sent to the internal timing latch circuits **454-0**, **454-1**, . . . , **454-n** in an unstable state.

FIG. **61** is a diagram showing a configuration of a semiconductor device according to a tenth embodiment. According to this embodiment, as in the ninth embodiment, current mirror circuits **452-0**, **452-1**, . . . , **452-n** are arranged in the vicinity of the input signal terminals, but the timing adjusting latch circuits **454-0**, **454-1**, . . . , **454-n** and the inter-signal timing adjusting circuit **455** are replaced by timing adjusting latch circuits **458-0**, **458-1**, . . . , **458-n**.

FIG. **62** is a diagram showing a configuration of the timing adjusting latch circuits **458-0**, **458-1**, . . . , **458-n**. These timing adjusting latch circuits are not for delaying the clock but are adapted to adjusting the delay amount of the input signal to match the phase of the input signals Q0Z, Q1Z, . . . , Q2Z with the phase of the clock ϕ and the clock ϕ½ produced from the shift clock generating circuit **453**. The delay circuit **460**, the delay control circuit **461**, the latch circuits **462**, **463**, **464** and the phase judge circuit **465** are similar to those shown in FIG. **32**, respectively, and will not be described in more detail.

FIG. **63** is a diagram showing the timing adjusting operation according to the tenth embodiment. Characters Q0, Q1, Q2 designate input signals applied to current mirror circuits **452-0**, **452-1**, . . . , **452-n**, respectively, characters Q0Z, Q1Z, Q2Z input signals to the timing adjusting latch circuits **454-0**, **454-1**, . . . , **454-n**, respectively, characters Q00, Q10, Q20 the signals set in phase in the timing adjusting latch

further includes a delay circuit **502**, a ½ frequency divider circuit **503** and latch circuits **504**, **505**, and in that outputs QSYNA, QSYNB, QSYNC are produced from the latch pulse generating circuit **510**.

FIGS. **66** and **67** are diagrams for explaining the operation of the semiconductor device according to an 11th embodiment. The operation of the 11th embodiment will be explained with reference to these diagrams.

The ½ frequency divider circuit **503** outputs a ½ frequency-divided clock of opposite phase having a half frequency of the clock. In accordance with the ½ frequency-divided clock of opposite phase, the latch circuits **504**, **505** latch the output of the input circuit **501**. The latch circuit **504** thus latches Q00A, and the latch circuit **505** Q00B. The same can be said of the other input signals. After an OR gate **506-0** produces a logic sum of the outputs of the latch circuits **504** and **505**, a signal is output which indicates the period during which the signals Q00A and Q00B are at H level. In other words, an input signal widened to three clock cycles is produced. Consequently, when this signal is input the input timing even in the case where the input signal is out of phase by one clock cycle or more in the tenth embodiment. As shown in FIG. **72**, the present embodiment includes a ½frequency divider circuit **521** for dividing the frequency of the output signal of the current mirror circuit **452** by one half, and a switching circuit **522** for switching the signal applied to the timing adjusting latch circuit **455** between the output of the current mirror circuit **42** and the output of the ½ frequency divider circuit **521**. In this case, in the initial stage of the receiving timing adjust mode, the output of the ½ frequency divider circuit is switched and applied to the timing adjusting latch circuit **455** by the switching operation. After that, the output of the current mirror circuit **452** is switched to the timing adjusting latch circuit **455**. In such a case, in the receiving timing adjust mode, an input signal is applied having a pattern changing at intervals of four clock cycles or more.

In the seventh to 13th embodiments described above, an input signal changing with a predetermined pattern is required for resynchronizing the input signal retrieved with

result, by applying the signals DK0, . . . , DKn to the AND gate **401**, the resynchronization is made possible as in the seventh embodiment.

In the case where the input signal retrieved by the input circuit is applied to the internal circuit, an inter-signal timing adjusting circuit is preferably arranged in the vicinity of the internal circuit. Further, the input section is preferably realized by an input buffer such as a current mirror circuit, and the latch circuit and the input timing adjusting circuit can be arranged in the vicinity of the internal circuit.

A plurality of the input timing adjusting circuits are desirably arranged in a cluster to share a delay circuit for adjusting the phase of the clock. As a result, the circuit can be reduced in scale.

In the case where the input signal is out of phase by one clock cycle or more, all the outputs of a plurality of the input circuits are not overlaid one on another, and therefore the logic product thereof is absent. In such a case, therefore, a parallel conversion circuit is provided in the input circuit for

internal clock generated from the received clock, and therefore the internal clock is required to be distributed among various internal portions. Further, since each such portion operates in synchronism with the internal clock, it is necessary that the distributed internal clocks should have a small phase difference. In the case where the internal clocks are distributed among many internal units, the wiring from the internal clock generating circuit to clock destinations is lengthened and the need arises for a multiplicity of clock buffers midway. The internal clocks thus distributed, therefore, are delayed considerably behind the input clock. In the case where the input circuit retrieves the input signal in synchronism with the internal clock thus delayed, a skew, no matter how small it is between the clock and the input signal at the input terminal, often leads to a large phase difference between the internal clock used by the input circuit to retrieve the input signal, i.e., the input timing signal and the input signal. In such a case, as described above, an input timing adjusting circuit is provided for one representative input signal, and the input signal is retrieved

latch circuit **633**. The signal input circuit **630** is generally arranged in the vicinity of the signal input terminal, and is according to the present embodiment. The dummy input circuit **620** has a configuration equivalent to the signal input circuit **630**, and includes a current mirror circuit **631** supplied with an external clock CLK, an input buffer circuit **632**, a dummy current mirror circuit **621** corresponding to the latch circuit **633**, a dummy input buffer circuit **622**, and a dummy latch circuit **623**. The dummy input circuit **620** is also arranged in the vicinity of the clock input terminal supplied with the external clock CLK. Each current mirror circuit, each buffer circuit and each latch circuit are identical to the conventional ones, respectively. The description of the current mirror circuit and the buffer circuit, therefore, will be omitted herein. The latch circuit has a configuration as shown in FIG. **20**, and the delay circuit **613** and the delay control circuit **614** a configuration as shown in FIG. **19**.

FIG. **77** is a time chart showing the operation of the configuration of FIG. **76**.

As shown in FIG. **77**, the input signal is applied in such a manner as to be effective before and after the rising edge of the external clock CLK. The output CLK0 of the clock current mirror circuit **611** and the output CLK1 of the clock buffer circuit **612** assume the form as shown due to the delay in the respective circuits. As shown by dashed arrow, the CLK1 is delayed by the delay circuit **613** and output behind the clock by about one cycle. The output SIG0 of the current mirror circuit **631** and the output SIG1 of the input signal buffer circuit **632** have an effective period as shown due to the delay of the input signals caused in the respective circuits. The dummy current circuit **621** is supplied with the external clock CLK. The dummy current circuit **621** and the dummy buffer circuit **622**, however, produce outputs DCLK0 and DCLK1 as shown, respectively, due to the same delay caused as in the current mirror circuit **631** and the input signal buffer circuit **632**. Specifically, DCLK1 rises at an optimum timing with respect to the effective period of SIG1. Consequently, the amount of delay in the delay circuit **613** is adjusted in such a manner that the internal clock CLK2 rises at the same timing as DCLK1. The dummy latch circuit **623** latches DCLK1 in accordance with the internal clock CLK2. Depending on whether DCLK1 rises before or after the internal clock CLK2, the CLKC of the dummy latch circuit **623** produces different outputs. In accordance with CLKC, therefore, the up/down counter of the delay control circuit **614** is counted up or down, and the delay amount in the delay circuit **613** is adjusted by feedback in such a manner that the internal clock CLK2 rises at the same timing as DCLK1.

Conversely, in the case where DCLK1 is delayed by b behind the internal clock CLK2, CLKC remains L substantially over the entire period as shown. The delay control circuit **614** increases the delay amount in the delay circuit **613** at the falling edge of the internal clock CLK2 with CLKC at L level. The result is that the internal clock CLK2 changes in such a manner that the rising edge thereof coincides with that of DCLK1.

As described above, according to the 15th embodiment, as compared with the case in which an external clock is applied to a dummy input circuit equivalent to the signal input circuit and latched by the internal clock, the direction in which the signal is latched by the internal clock through the signal input circuit is detected. On the basis of the result of this detection, an optimum timing is attained by adjustment. Regardless of the temperature conditions or the source voltage, therefore, the input signal can be retrieved at an always optimum timing.

FIG. **80** is a diagram showing a configuration of the clock generating circuit and the signal input circuit of a semiconductor device according to a 16th embodiment. The difference of this embodiment from the 15th embodiment lies in a clock distribution circuit **640** provided for distributing the internal clock generated from the clock generating circuit among the various parts in the semiconductor device. The difference, therefore, is that the internal clock distributed from the clock distribution circuit **640** is applied to the dummy input circuit **625** and the signal input circuit **635**, and that the dummy input circuit **625** and the signal input circuit **635** are of a latch type in which the external clock CLK or the input signal is applied directly to the latch circuit.

As described already, the use of a current mirror circuit at the portion receiving an external signal is for the purpose of accurately retrieving the signal change. The signal retrieval error directly constitutes a timing error, and therefore, a current mirror circuit capable of accurately retrieving the signal change has been conventionally used. The current mirror circuit, in spite of its capability of retrieving the signal change accurately, has a problem of large power consumption as current constantly flows therethrough. An application of the invention, on the other hand, makes it possible to adjust the input signal to be retrieved at an appropriate timing in the semiconductor device. Even without using the current mirror circuit, therefore, no timing error occurs at the time of signal retrieval. Consequently, as shown in the diagram, the signal input circuit **35** can be configured of the input signal latch circuit **636** and the buffer circuit **637** without using the current mirror circuit. The

FIG. **81**, the internal clocks applied to the signal input circuits **635-1**, **635-2**, . . . , **635**-n and the dummy input circuit **625** are all in phase with each other. If the dummy input circuit **625** judges the extent to which the phase of the internal clock is advanced of that of the external clock and the delay amount in the clock generating circuit **610** is adjusted on the basis of the judgement, then, all the signal input circuits **635-1**, **635-2**, . . . , **635**-n can retrieve the input signals Sig-**1**, Sig-**2**, . . . , Sig-n at an appropriate timing.

FIG. **82** is a diagram showing a configuration of the clock generating circuit and the signal input circuit of a semiconductor device according to a 17th embodiment. FIG. **83** is a time chart showing the operation of the 17th embodiment. A clock generating circuit **610**, a dummy input circuit **620** and an input circuit **630** are identical to the corresponding circuits in the 15th embodiment. The difference of this embodiment from the 15th embodiment resides in the provision of a PLL circuit **680**. According to the first embodiment, the input signal is effective for a predetermined length of time before and after the rising edge of the external clock. In spite of this, the input signal may remain effective for a predetermined length of time about the phase displaced with respect to the leading or falling edge of the external clock. As shown in FIG. **83**, in the 17th embodiment, the input signal is switched at the time point when CLK is at L level just intermediate between the leading and falling edges of the external clock CLK and is shown to be retrieved at an exactly intermediate point between the leading and falling edges of CLK at H level. For the dummy input circuit to judge the timing, a signal changing at a point just intermediate between the leading and falling edges of the CLK at H level in phase with the input signal is required to be input to the dummy input circuit. Such a signal may be generated by delaying the external clock CLK. In such a case, however, the problem is caused by an error occurring in the circuit for delaying the CLK, which makes an accurate judgement impossible. For this reason, as shown in FIG. **82**, the external clock CLK is delayed by one-fourth of the clock

- a phase comparator circuit for judging the phase of said input timing clock and said input signal; and
- a delay control circuit for changing the delay amount of said delay circuit in such a manner that said input timing clock assumes a predetermined phase relation with respect to said input signal on the basis of the judgement of said phase comparator circuit.

3. A semiconductor device system according to claim **2**, wherein:

- said receiving-end semiconductor device includes a shift clock generating circuit for displacing said input timing clock by said predetermined phase and generating a shift clock changing in phase with said input signal; and
- said phase comparator circuit compares the phase of said shift clock with that of said input signal.

4. A semiconductor device system according to claim **2**, wherein:

- said receiving-end semiconductor device includes a shift clock generating circuit for generating from said internal clock two original shift clocks displaced by a predetermined amount of phase from each other;
- said delay circuit outputs said two original shift clocks delayed by the same amount, one shift clock as said input timing clock and the other shift clock as an output to said phase comparator circuit; and
- said phase comparator circuit compares the phase of said shift clocks with that of said input signal.

5. A semiconductor device system according to claim **2**, wherein:

- said phase comparator circuit includes a change information detection circuit for detecting whether said input signal has changed and, if changed, the direction of change, and means for judging the phase on the basis of the result of detection by said change information

of input timing adjusting circuits each of which corresponds to said input timing adjusting circuit,

and each input timing adjusting circuit is provided for each input circuit.

9. A semiconductor device system according to claim 8, wherein:

said receiving-end semiconductor device further includes an inter-signal timing adjusting circuit for detecting the phase difference between the output signals of said plurality of input circuits and adjusting said output signals in phase with each other.

10. A semiconductor device system according to claim 9, wherein:

said inter-signal timing adjusting circuit detects the phase difference between the output signals of said plurality of signal input circuits on the basis of the control value of delay control circuit.

11. A semiconductor device system according to claim 1, wherein:

a predetermined period after starting said semiconductor device system is set as a receiving timing adjust mode for adjusting said input timing adjusting circuit, followed by a normal operation mode, said input timing adjusting circuit being adjusted also in said normal operation mode.

12. A semiconductor device system according to claim 1, wherein:

said semiconductor device system has a normal mode and a receiving timing adjust mode for adjusting the timing of receiving said input signal in said receiving-end semiconductor device; and

said input timing adjusting circuit changes the phase of said internal clock supplied to said input circuit in said receiving timing adjust mode and holds said phase of said clock supplied to said input circuit in said normal mode.

13. A semiconductor device system according to claim 2, wherein:

the modes of operation of said semiconductor device system include a normal mode and a receiving timing adjust mode for adjusting the timing of receiving said input signal in said receiving-end semiconductor device; and said delay control circuit changes the delay amount on the basis of the result of comparison of said phase comparator circuit in said receiving timing adjust mode, and holds the delay amount in said normal mode.

14. A semiconductor device system according to claim 13, wherein:

said driving-end semiconductor device issues a mode indication signal for indicating the receiving timing adjust mode for the input signal; and

said receiving-end semiconductor device includes a mode register/decoder for recognizing said mode indication signal.

15. A semiconductor device system according to claim 13, wherein:

said driving-end semiconductor device outputs an adjust output signal changing at a predetermined period in said receiving timing adjust mode at a timing displaced by a predetermined amount of phase from the timing for said normal mode.

16. A semiconductor device system according to claim 13, wherein:

said driving-end semiconductor device includes an output timing adjusting circuit for comparing the phase of said output signal produced from said driving-end semiconductor device with that of said clock and adjusting the phase of said output signal with respect to said clock.

17. A semiconductor device system according to claim 13, wherein:

said receiving-end semiconductor device receiving a plurality of input signals including said input signal,

said receiving-end semiconductor device includes a plurality of input circuits including said input circuit for receiving said plurality of input signals and a plurality of input timing adjusting circuits each of which corresponds to said input timing adjusting circuit, and each input timing adjusting circuit is provided for each input circuit.

18. A semiconductor device system according to claim 17, wherein:

said receiving-end semiconductor device includes an inter-signal timing adjusting circuit for detecting the phase difference between the output signals of said plurality of input circuits and adjusting said output signals into the same phase.

19. A semiconductor device system according to claim 18, wherein:

said inter-signal timing adjusting circuit performs the adjusting operation on the basis of a combination of said input signals having a predetermined signal pattern input during said receiving timing adjust mode, and maintains the adjusted value after completion of said receiving timing adjust mode.

20. A semiconductor device system according to claim 19, wherein:

a predetermined signal pattern of said input signals input during said receiving timing adjust mode assumes a different logical value only during a specific one of the cycles where the same logical value continues.

21. A semiconductor device system according to claim 13, wherein:

said receiving-end semiconductor device receives a plurality of input signals including said input signal, some of said input signals having a long period and other of said input signals having a short period, and

said mode indication signal is a combination of the values of said input signals of a long period.

22. A semiconductor device system according to claim 19, wherein:

said input signal having said predetermined signal pattern is input for a predetermined length of time even after indication of the end of said receiving timing adjust mode.

23. A semiconductor device system according to claim 18, wherein:

said input signal includes a combination of a plurality of signals in continuous cycles;

said input circuit includes a parallel conversion circuit for retrieving said input signals and converting said plurality of signals of continuous cycles into parallel signals; and

said inter-signal timing adjusting circuit adjusts said combination of outputs of said parallel conversion circuits into the same phase.

24. A semiconductor device system according to claim 23, wherein:

a plurality of said input signals are input during one cycle of said clock.

25. A semiconductor device, comprising:

an input circuit for receiving an input signal and latching said input signal in synchronism with an internal clock; and

an input timing adjusting circuit receiving a clock and outputting said internal clock for adjusting a phase of said internal clock,

wherein said input timing adjusting circuit includes a feedback circuit receiving said internal clock and generating a timing control signal, said adjusting of the phase of said internal clock is carried out in response to the timing control signal.

26. A semiconductor device according to claim 25, wherein said input timing adjusting circuit includes:

a delay circuit for delaying said clock to produce said internal clock;

a phase comparator circuit for comparing the phase of said internal clock and the phase of said input signal; and

a delay control circuit for controlling a delay amount of said delay circuit in response to a comparison result of said phase comparator circuit in such a manner that said internal clock has a predetermined phase relation with respect to said input signal.

27. A semiconductor device according to claim 26, further comprising:

a shift clock generating circuit for generating a shift clock changing in phase with said input signal by displacing said input timing clock by a predetermined amount of phase;

wherein said phase comparator circuit compares the phase of said shift clock with the phase of said input signal.

28. A semiconductor device according to claim 27, further comprising a shift clock generating circuit for generating two original shift clocks displaced by said predetermined phase relation from each other from said internal clock;

wherein said delay circuit delays each of said two original shift clocks by the same amount, one of said original shift clocks being output as said input timing clock, the other of said original shift clocks being output to said phase comparator circuit as a shift clock; and

wherein said phase comparator circuit compares the phase of said shift clock with the phase of said input signal.

29. A semiconductor device according to claim 27, wherein said shift clock generating circuit includes:

a plurality of stages of shift delay circuits with the same selectable delay amount, the output of a preceding stage being applied to the following stage, said input timing clock being applied to the initial stage;

a clock phase comparator circuit for comparing the phase of the output in the last stage of said shift delay circuits with the phase of said input timing clock; and

a delay control circuit for controlling the delay amount of said plurality of stages of said shift delay circuits in such a manner that the phase of

the output from said last stage coincides with the phase of said input timing clock on the basis of the result of comparison at said clock phase comparator circuit; and

the output from a predetermined stage of said shift delay circuits is output as said shift clock.

30. A semiconductor device according to claim 28, wherein said shift clock generating circuit includes:

a plurality of stages of shift delay circuits with the same selectable delay amount, the output of a preceding stage being applied to the following stage, said internal clock being applied to the initial stage;

a clock phase comparator circuit for comparing the phase of the output in the last stage of said shift delay circuits with the phase of said input timing clock; and

a delay control circuit for controlling the delay amount of said plurality of stages of said shift delay circuits in such a manner that the phase of the output from said last stage coincides with the phase of said input timing clock on the basis of the result of comparison at said clock phase comparator circuit; and

the output from a predetermined stage of said shift delay circuits and said internal clock or the output from the last stage are output as said two original shift clocks.

31. A semiconductor device according to claim 27, wherein said phase comparator circuit includes:

a dummy latch for receiving said input signal in synchronism with said shift clock;

a change information detection circuit for detecting whether the change of said input signal in the vicinity of an area where said dummy latch receives said input signal is a rising edge or a falling edge; and

a phase judge circuit for judging the direction in which the phase of said shift clock is changed with respect to the phase of said input signal only when said input signal is changed, on the basis of the value received by said dummy latch and the result of detection at said change information detection circuit.

32. A semiconductor device according to claim 31, wherein said change information detection circuit includes:

a latch for receiving said input signal before said dummy latch receives said input signal; and

a holding circuit for holding the value received by said latch for a predetermined length of time after said latch receives the next input signal;

wherein said phase judge circuit detects whether said input signal has changed and, if changed, the direction of said change, from the value of said latch and said holding circuit.

33. A semiconductor device according to claim 32, wherein said holding circuit is a delay latch for receiving the output of said latch at the same timing as said latch.

34. A semiconductor device according to claim 32, wherein said holding circuit is a delay circuit for delaying the output of said latch.

35. A semiconductor device according to claim 32, wherein said latch constitutes said input circuit for retrieving said input signal.

36. A semiconductor device according to claim 26, further comprising a minimum period change detection circuit for detecting that said input signal has changed continuously in the immediately preceding two clock cycles;

wherein said delay control circuit changes the delay amount of said delay circuit only when said input signal has changed continuously in the immediately preceding two clock cycles.

37. A semiconductor device according to claim 36, wherein said minimum period change detection circuit includes:

a first delay latch for receiving the output of a latch of said input circuit for receiving said input signal, at the same timing as said latch;

a second delay latch for receiving the output of said first delay latch at the same timing as said latch; and

a minimum period change judging circuit for judging that said input signal has continuously changed in the immediately preceding two clock cycles when all the

outputs of said latch, said first delay latch and said second delay latch undergo a change.

38. A semiconductor device according to claim 32, further comprising a minimum period change detection circuit for detecting that said input signal has continuously changed in the immediately preceding two clock cycles;

wherein said delay control circuit changes the delay amount of said delay circuit only when said input signal changes continuously in the immediately preceding two clock cycles; and

wherein said change information detection circuit and said minimum period change detection circuit partially share each other.

39. A semiconductor device according to claim 25, further comprising:

a timing correction circuit for selecting whether or not the timing of retrieval at said input circuit is to be delayed by a predetermined amount; and

an input signal change detection circuit for detecting that said input signal has changed in the immediately preceding clock cycle;

wherein in the case where said input signal fails to change in the immediately preceding clock cycle, the timing of retrieval at said signal input circuit is delayed by a predetermined amount by said timing correction circuit.

40. A semiconductor device according to claim 39, wherein said input signal change detection circuit includes:

a delay latch for receiving the output of a latch of said input circuit for receiving said input signal, at the same timing as said latch; and

a circuit for judging that said input signal fails to change in the immediately preceding clock cycle when the output of said latch is identical to the output of said delay latch.

41. A semiconductor device according to claim 38, further comprising:

a timing correction circuit for selecting whether or not the retrieval timing at said signal input circuit is to be delayed by a predetermined amount; and

an input signal change detection circuit for detecting that said input signal has changed in the immediately preceding clock cycle;

wherein in the case where said input signal fails to change in the immediately preceding clock cycle, said timing correction circuit delays the retrieval timing of said signal input circuit by a predetermined amount; and

wherein said change information detection circuit, said minimum period change detection circuit and said input signal change detection circuit partially share circuitry.

42. A semiconductor device according to claim 25, wherein said semiconductor device receives a plurality of input signals including said input signal,

said semiconductor device comprises a plurality of input circuits including said input circuit for receiving said plurality of input signals,

said input timing adjusting circuit is provided for each of said input circuits; and

said semiconductor device further comprises an inter-timing adjusting circuit for detecting the phase difference between the output signals of said signal input circuits and adjusting said output signals into the same phase.

43. A semiconductor device according to claim 42, wherein said input timing adjusting circuit includes:

a delay circuit with a selectable delay amount for receiving the internal clock generated based on the clock received and producing said internal clock as an input timing clock;

a phase comparator circuit for judging the phase of the input timing clock and the phase of said input signal; and

a delay control circuit for changing the delay amount of said delay circuit in such a manner that said input timing clock has a predetermined phase relation with respect to said input signal on the basis of the result of the comparison at said phase comparator circuit;

said inter-signal timing adjusting circuit detects the phase difference between the output signals of said signal input circuits on the basis of a control value of said delay control circuit.

44. A semiconductor device according to claim 25, wherein a predetermined period after activating said semiconductor device constitutes a receiving timing adjust mode for adjusting said input timing adjusting circuit, the subsequent period constituting a normal operation mode, and the adjustment by said input timing adjusting circuit is carried out also in said normal operation mode.

45. A semiconductor device according to claim 26,

wherein said semiconductor device has a normal mode and a receiving timing adjust mode for adjusting the retrieval timing of said input signal; and

wherein said delay control circuit changes the delay amount on the basis of the result of comparison of said phase comparator circuit in the receiving timing adjust mode and holds the delay amount in said normal mode.

46. A semiconductor device according to claim 45, further comprising a mode register/decoder for recognizing a mode indication signal indicating said receiving timing adjust mode.

47. A semiconductor device according to claim 45, further comprising a clock generating circuit for generating the internal clock and a shift clock for shifting said internal clock by a predetermined amount of phase on the basis of said received clock, and applying selected one of said internal clock and said shift clock to said delay circuit;

wherein said clock generating circuit selectively outputs said internal clock in said normal mode and outputs said shift clock in said receiving timing adjust mode.

48. A semiconductor device according to claim 47, wherein said phase comparator circuit includes:

a dummy latch for receiving said input signal in synchronism with said shift clock;

a change information detection circuit for detecting whether the change of said input signal in the vicinity of a point of retrieval of said input signal by said dummy latch is a rising edge or a falling edge; and

a phase judge circuit for judging the direction in which the phase of said shift clock is changed with respect to the phase of said input signal only when said input signal has changed, on the basis of the value retrieved by said dummy latch and the result of detection at said change information detection circuit.

49. A semiconductor device according to claim 48, wherein said change information detection circuit includes:

a latch for receiving said input signal before or after said dummy latch retrieves said input signal;

a holding circuit for holding the value received by said latch for a predetermined length of time after said latch receives the next input signal;

wherein said phase judge circuit detects whether said input signal has changed and, if changed, the direction of said change, from the value of said latch and said holding circuit.

50. A semiconductor device according to claim **49**, wherein said input latch constitutes said input circuit for retrieving said input signal.

51. A semiconductor device according to claim **45**, wherein said semiconductor device receives a plurality of input signals including said input signal,

said semiconductor device comprises a plurality of input circuits including said input circuit for receiving said plurality of input signals,

said input timing adjusting circuit is provided for each of said input circuits;

said semiconductor device further comprises an inter-signal timing adjusting circuit for detecting the phase difference between the output signals of said input circuits and adjusting said output signals of said plurality of input circuits into the same phase.

52. A semiconductor device according to claim **51**, wherein said inter-signal timing adjusting circuit includes: a common effective period detection circuit for detecting a period during which all the output signals of said input circuits have the same cycle; and

a plurality of latch circuits for latching the output signal of said input circuits during said common effective signal period.

53. A semiconductor device according to claim **51**, wherein said inter-signal timing adjusting circuit includes: a signal delay circuit for delaying the output signals of said input circuits; and

a delay control register for detecting the most delayed signal among the output signals of said input circuits and controlling the delay amount of said signal delay circuit in conformance with said most delayed signal.

54. A semiconductor device according to claim **51**, further comprising a mode register/decoder for recognizing a mode indication signal supplied from an external source for indicating the receiving timing adjust mode for the input signal;

wherein said input timing adjusting circuit performs the adjustment on the basis of a combination of said input signals having a predetermined signal pattern input during said receiving timing adjust mode, and maintains an adjusted value after said receiving timing adjust mode.

55. A semiconductor device according to claim **52**, further comprising a mode register/decoder for recognizing a mode indication signal supplied from an external source for indicating the receiving timing adjust mode for the input signal;

wherein said input timing adjusting circuit and said inter-signal timing adjusting circuit perform the adjustment on the basis of a combination of said input signals having a predetermined signal pattern input during said receiving timing adjust mode, and maintains an adjusted value after said receiving timing adjust mode.

56. A semiconductor device according to claim **55**,

wherein the predetermined signal pattern of said input signal input during said receiving timing adjust mode assumes a different logic value only in a specific one of the cycles in which the same logic value continues; and

wherein said common effective period detection circuit includes a gate for calculating the logic product of the output signals of said input circuits, and detects the period during which all the output signals of the input circuits have the same cycle, on the basis of the output of said gate.

57. A semiconductor device according to claim **53**, further comprising a mode register/decoder for recognizing a mode indication signal supplied from an external source for indicating the receiving timing adjust mode for the input signal;

wherein said input timing adjusting circuit and said inter-signal timing adjusting circuit perform the adjustment on the basis of a combination of said input signals having a predetermined signal pattern input during said receiving timing adjust mode, and maintains an adjusted value after said receiving timing adjust mode.

58. A semiconductor device according to claim **56**, wherein said input signals include at least one of two kinds of signals of a short period and a long period, and wherein said mode indication signal is a combination of the values of said input signals of a long period.

59. A semiconductor device according to claim **56**, wherein said mode indication signal is applied by way of a dedicated input signal terminal.

60. A semiconductor device according to claim **58 59**, wherein said input signal having said predetermined signal pattern is applied during a predetermined length of time after the end of said receiving timing adjust mode is indicated.

61. A semiconductor device according to claim **51**, further comprising an internal circuit supplied with output signals from said input circuits;

wherein said inter-signal timing adjusting circuit is arranged in the vicinity of said internal circuit.

62. A semiconductor device according to claim **61**, wherein said input timing adjusting circuit is arranged in the vicinity of said internal circuit.

63. A semiconductor device according to claim **51**, wherein a plurality of said input timing adjusting circuits are arranged in a cluster.

64. A semiconductor device according to claim **63**,

wherein said input timing adjusting circuit includes a delay circuit for adjusting the phase of said clock; and

wherein said plurality of said input timing adjusting circuits arranged in a cluster share a part of said delay circuit.

65. A semiconductor device according to claim **51**,

wherein said input circuit includes a parallel conversion circuit for converting two continuous said input signals into parallel signals after retrieving said input signals; and

wherein said inter-signal timing adjusting circuit adjusts the of output signals said parallel conversion circuit in such a manner that the signals of the same cycle are in phase with each other.

66. A semiconductor device according to claim **51**,

wherein said input signals constitute signal sets each having a plurality of cycles;

wherein said input circuit includes at least one parallel conversion circuit for converting said signals having said plurality of continuous cycles into parallel signals after retrieving said input signals; and

wherein said inter-signal timing adjusting circuit adjust the outputs of said at least one parallel conversion circuit into the same phase.

67. A semiconductor device according to claim **66**, wherein said plurality of said input signals are applied during one cycle of said clock.

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Rogers et al.

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(45) **Date of Patent:** Sep. 11, 2001

(54) **CACHED SYNCHRONOUS DRAM ARCHITECTURE HAVING A MODE REGISTER PROGRAMMABLE CACHE POLICY**

(75) Inventors: **Jim L. Rogers**, Milton; **Steven W. Tomashot**, Williston, both of VT (US); **David W. Bondurant**, Colorado Springs, CO (US); **Oscar Frederick Jones, Jr.**, Colorado Springs, CO (US); **Kenneth J. Mobley**, Colorado Springs, CO (US)

(73) Assignee: **International Business Machines Corp.**, Armonk, NY (US)

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(51) Int. Cl.[7] **G06F 12/06**

(52) U.S. Cl. **711/105**; 711/118

(58) Field of Search 711/3, 105, 118, 711/133, 134, 154, 167, 168

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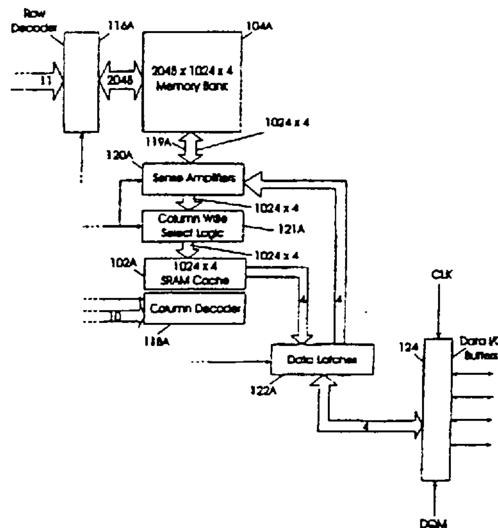
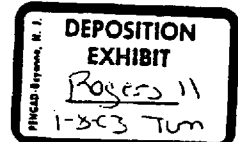
Primary Examiner—Tuan V. Thai
Assistant Examiner—Christian P. Chace
(74) *Attorney, Agent, or Firm*—Francis J. Thornton; Robert A. Walsh

(57) **ABSTRACT**

A cached synchronous dynamic random access memory (cached SDRAM) device having a multi-bank architecture and a programmable caching policy includes a synchronous dynamic random access memory (SDRAM) bank, a synchronous static randomly addressable row register, a select logic gating circuit, and mode register for programming of the cached SDRAM to operate in a Write Transfer mode corresponding to a Normal Operation mode of a standard SDRAM during a Write cycle, and to operate in a No Write Transfer mode according to an alternate operation mode during a Write cycle, thereby operating under a first and a second caching policy, respectively. The SDRAM includes a row decoder for selecting a row of data in a memory bank array, sense amplifiers for latching the row of data selected by the row decoder, and a synchronous column selector for selecting a desired column of the row of data. The row register stores a row of data latched by the sense amplifiers and the select logic gating circuit, disposed between the sense amplifiers and the row register, selectively gates the row of data present on the bit lines to the row register in accordance to particular synchronous memory operations being performed.

19 Claims, 13 Drawing Sheets





DEPOSITION EXHIBIT
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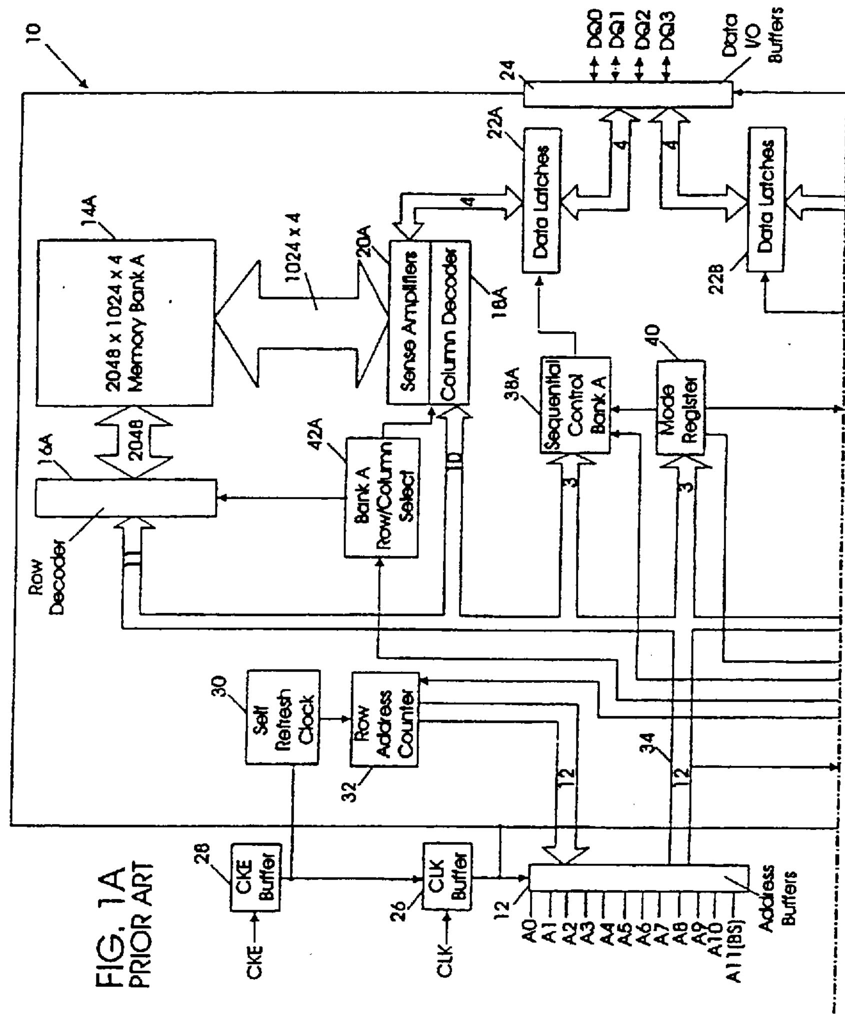


FIG. 1A
PRIOR ART

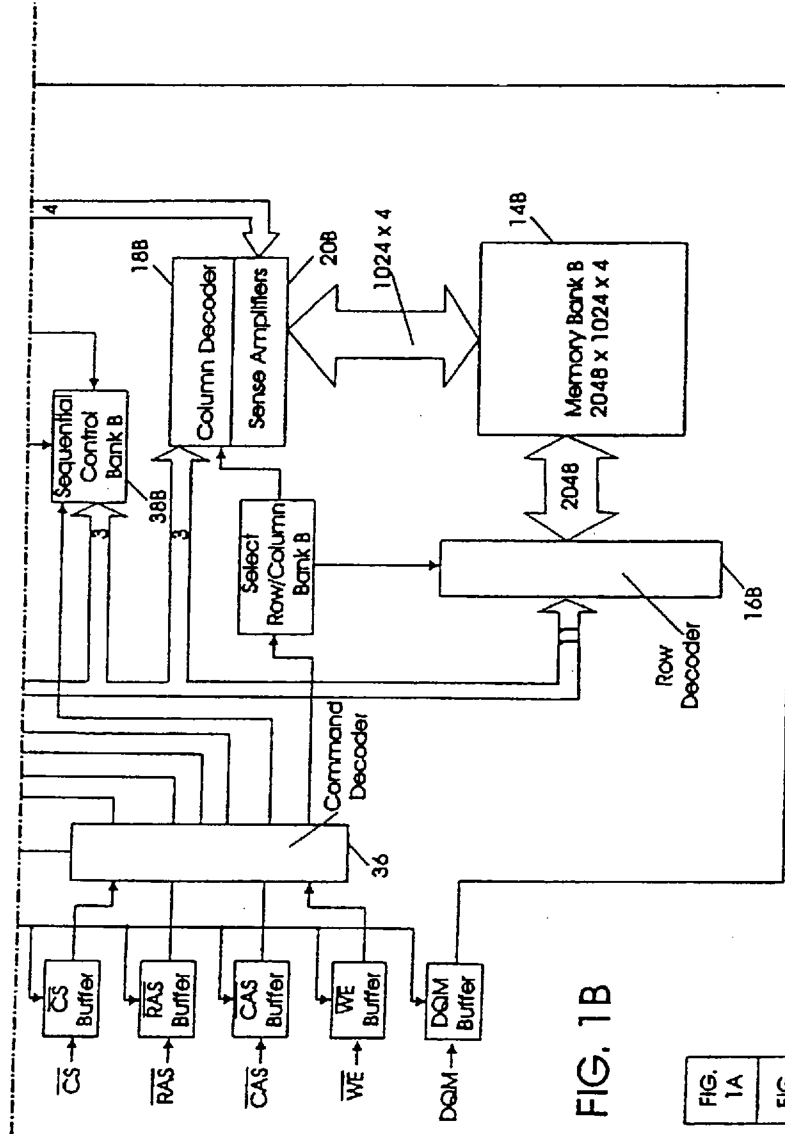
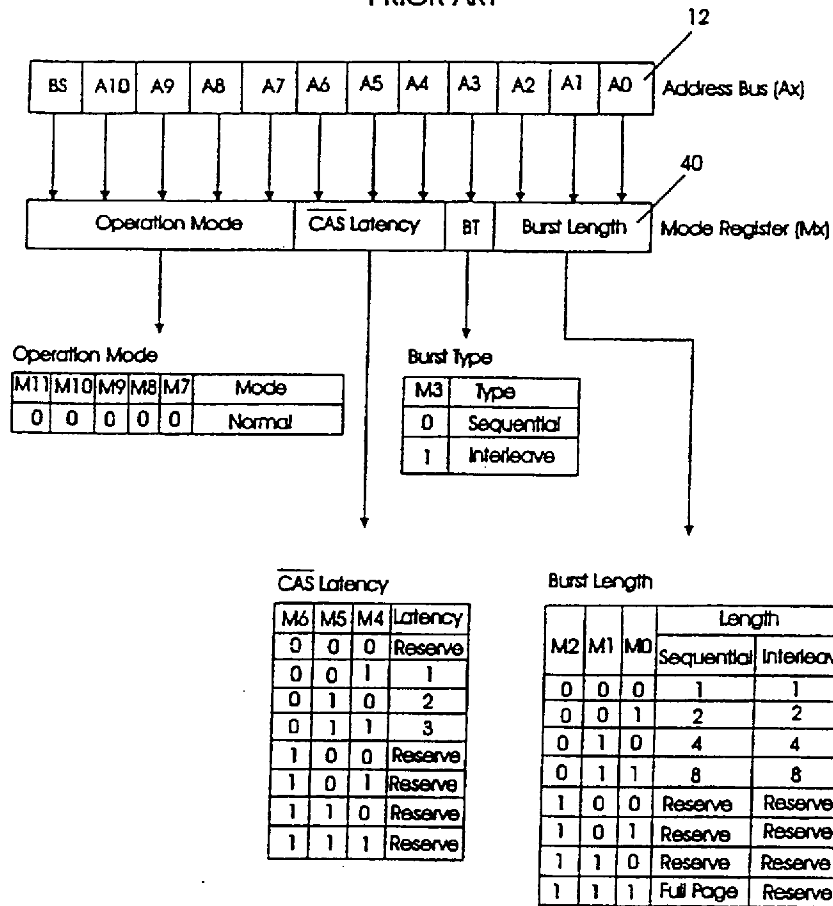


FIG. 1B

FIG. 1

FIG. 2
PRIOR ART



Operation Mode

M11	M10	M9	M8	M7	Mode
0	0	0	0	0	Normal

Burst Type

M3	Type
0	Sequential
1	Interleave

CAS Latency

M6	M5	M4	Latency
0	0	0	Reserve
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserve
1	0	1	Reserve
1	1	0	Reserve
1	1	1	Reserve

Burst Length

M2	M1	M0	Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Full Page	Reserve

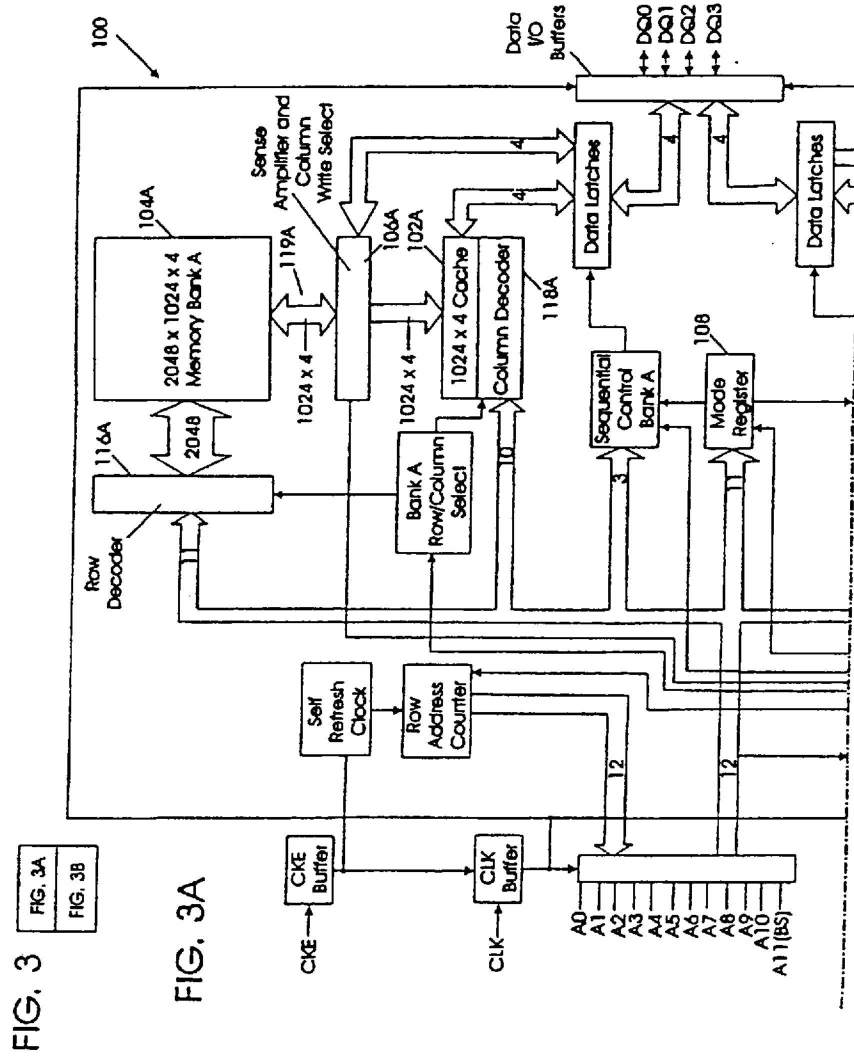


FIG. 3
FIG. 3A
FIG. 3B
FIG. 3A
100
104A
2048 x 1024 x 4 Memory Bank A
119A
1024 x 4
Sense Amplifier and Column Write Select
106A
102A
1024 x 4 Cache
Column Decoder
118A
Data Latches
Data I/O Buffers
DQ0
DQ1
DQ2
DQ3
4
Sequential Control Bank A
3
108
Mode Register
Data Latches
116A
2048
Row Decoder
Bank A Row/Column Select
10
Self Refresh Clock
Row Address Counter
12
CKE Buffer
CLK Buffer
CKE
CLK
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11(BS)

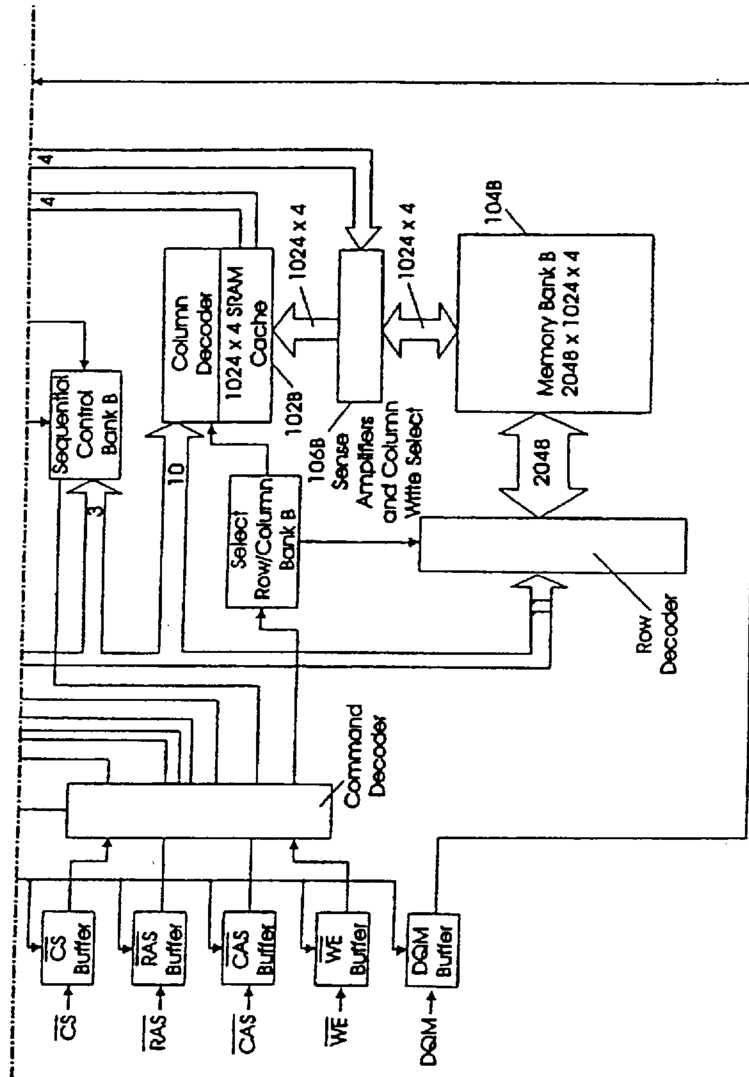
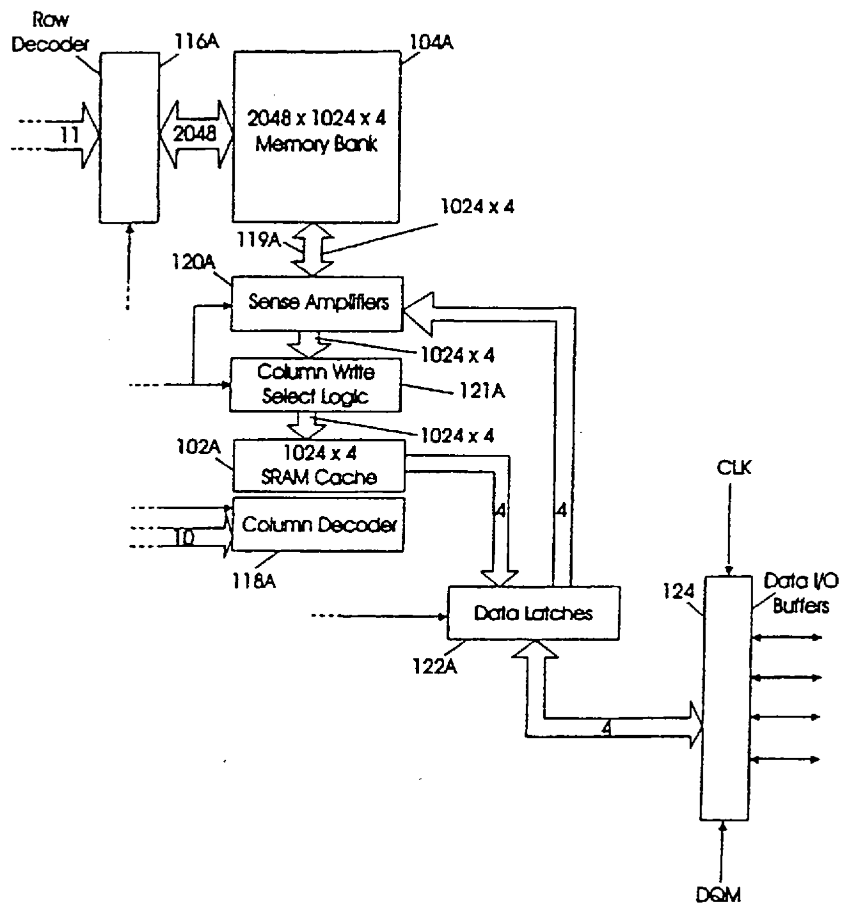


FIG. 3B

FIG. 4



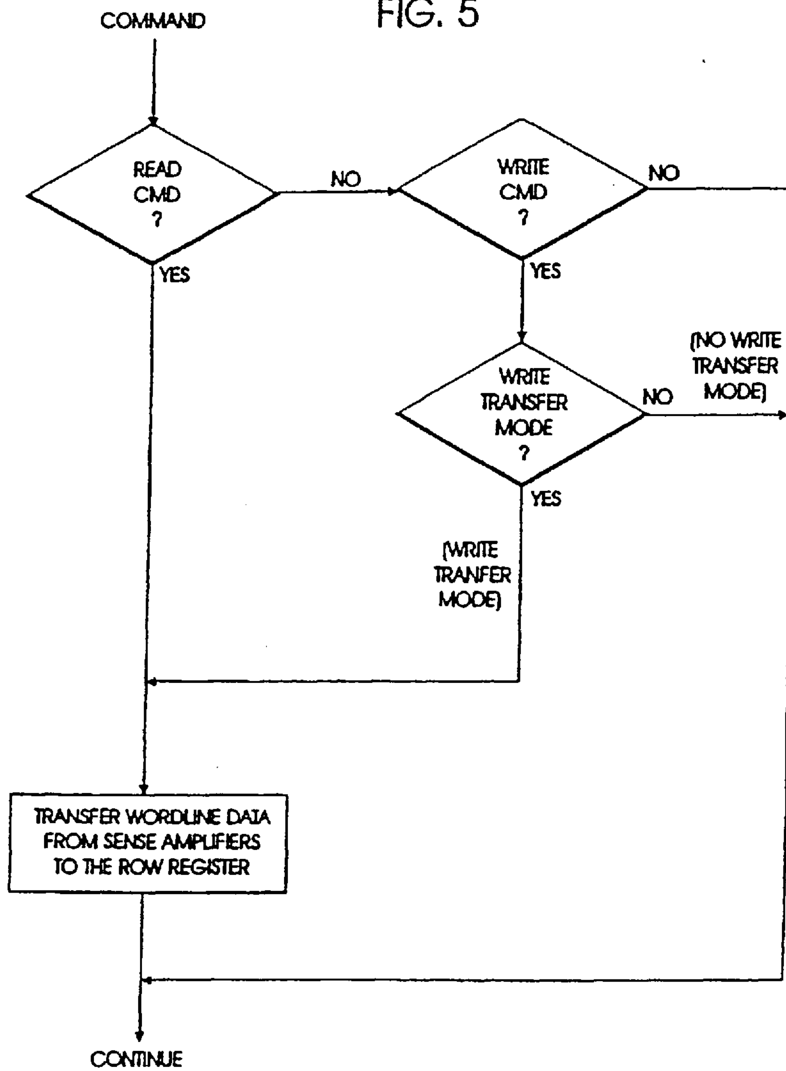
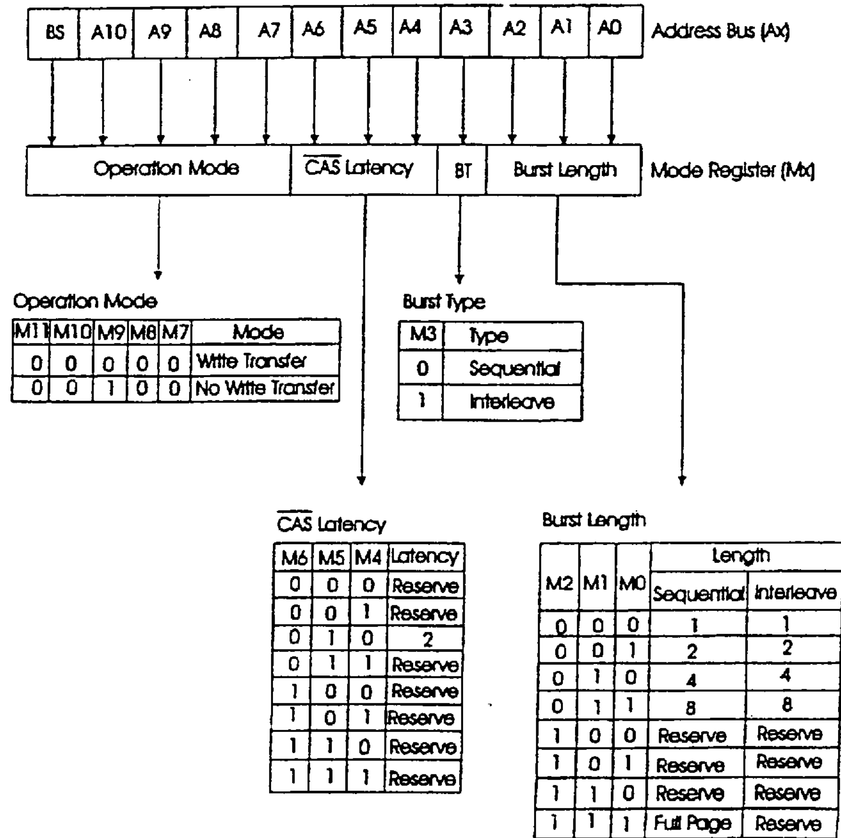


FIG. 5
COMMAND
READ CMD ?
NO
YES
WRITE CMD ?
NO
YES
WRITE TRANSFER MODE ?
NO
(NO WRITE TRANSFER MODE)
YES
(WRITE TRANFER MODE)
TRANSFER WORDLINE DATA FROM SENSE AMPLIFIERS TO THE ROW REGISTER
CONTINUE

FIG. 6



Operation Mode

M11	M10	M9	M8	M7	Mode
0	0	0	0	0	Write Transfer
0	0	1	0	0	No Write Transfer

Burst Type

M3	Type
0	Sequential
1	Interleave

CAS Latency

M6	M5	M4	Latency
0	0	0	Reserve
0	0	1	Reserve
0	1	0	2
0	1	1	Reserve
1	0	0	Reserve
1	0	1	Reserve
1	1	0	Reserve
1	1	1	Reserve

Burst Length

M2	M1	M0	Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Full Page	Reserve

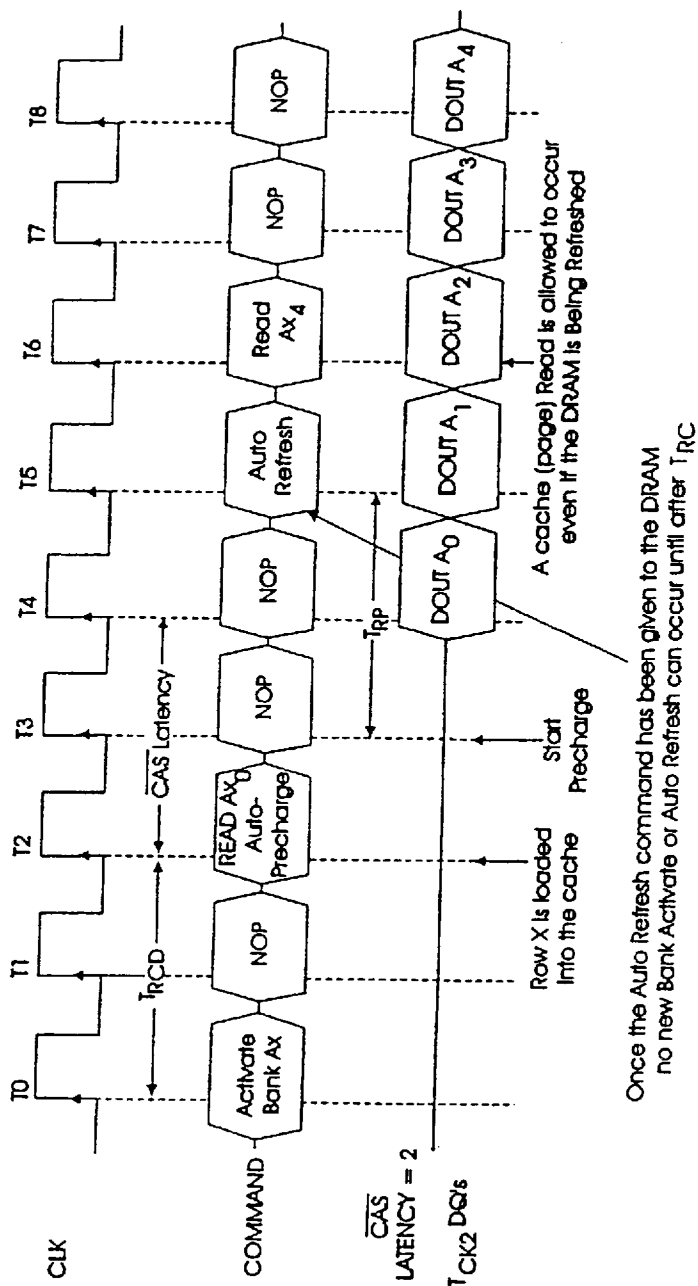


FIG. 7

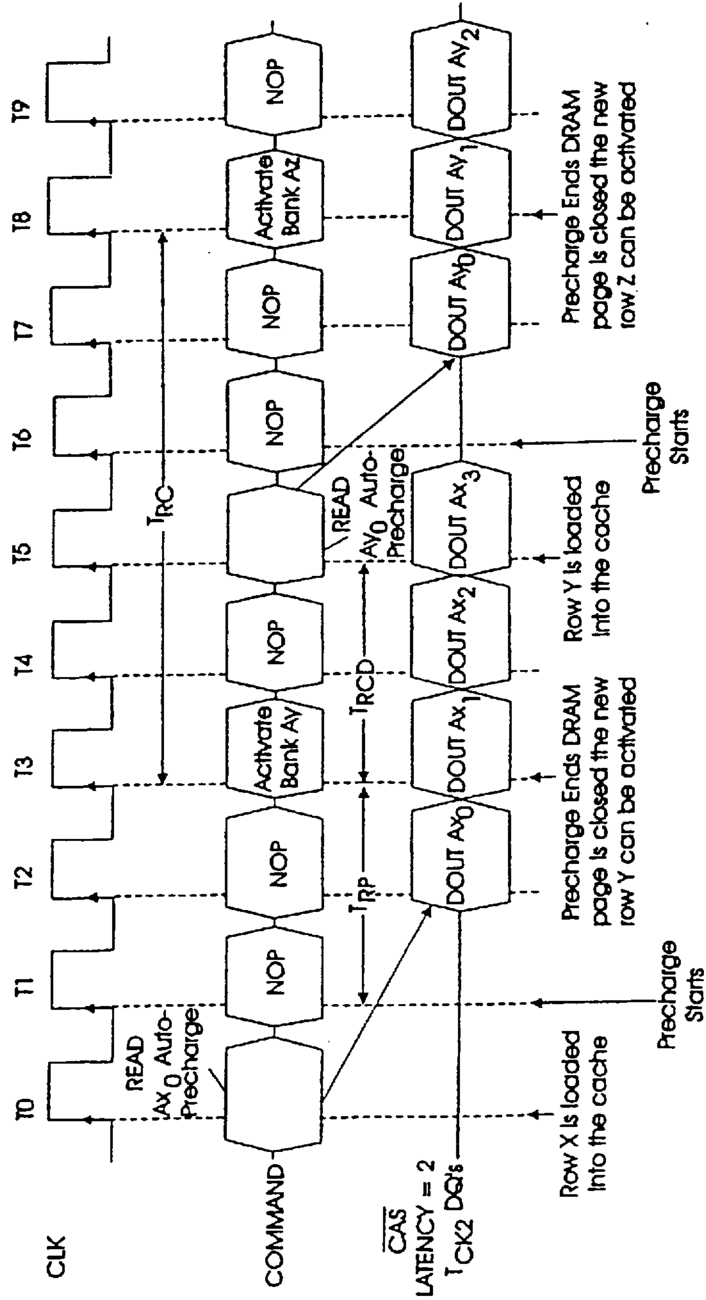


FIG. 8
CLK
COMMAND
$\overline{CAS}$ LATENCY = 2
T_{CK2} DQ's
T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
READ Ax0 Auto-Precharge
NOP
NOP
Activate Bank Ay
NOP
READ Ay0 Auto-Precharge
NOP
NOP
Activate Bank Az
NOP
T_{RP}
T_{RCD}
T_{RC}
DOUT Ax0
DOUT Ax1
DOUT Ax2
DOUT Ax3
DOUT Ay0
DOUT Ay1
DOUT Ay2
Row X is loaded into the cache
Precharge Starts
Precharge Ends DRAM page is closed the new row Y can be activated
Row Y is loaded into the cache
Precharge Starts
Precharge Ends DRAM page is closed the new row Z can be activated

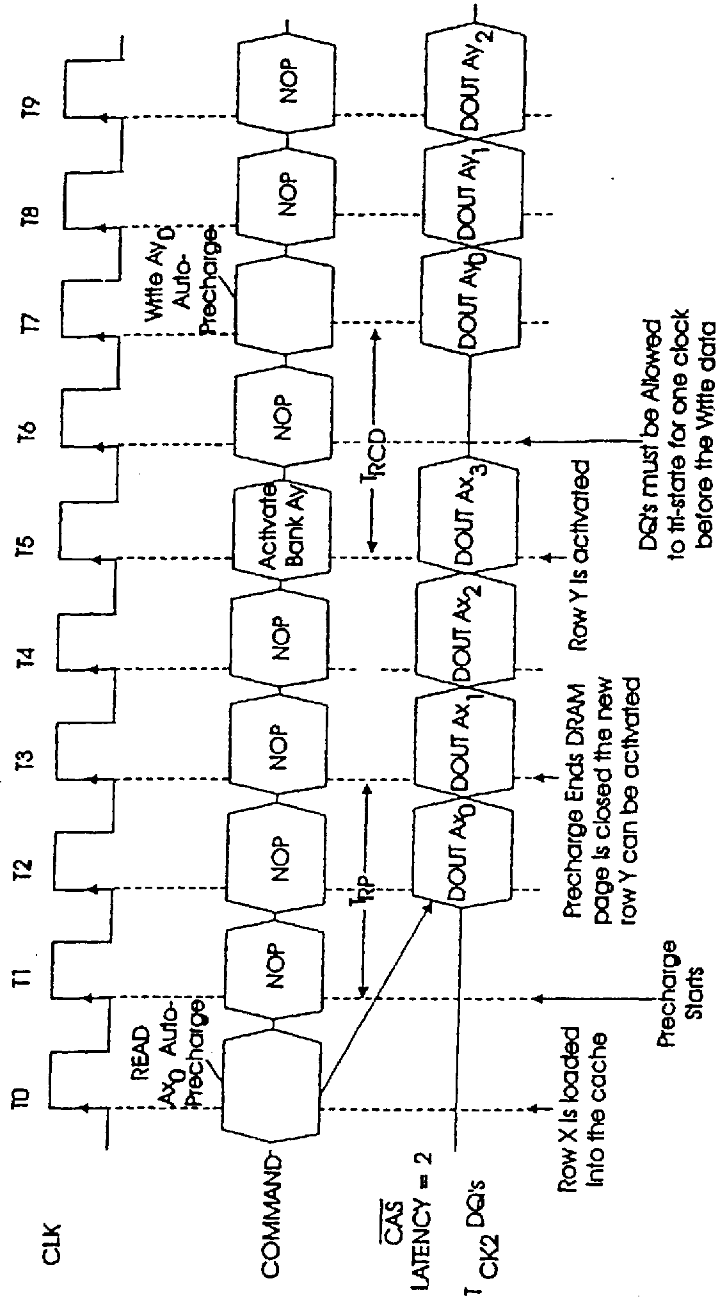


FIG. 9

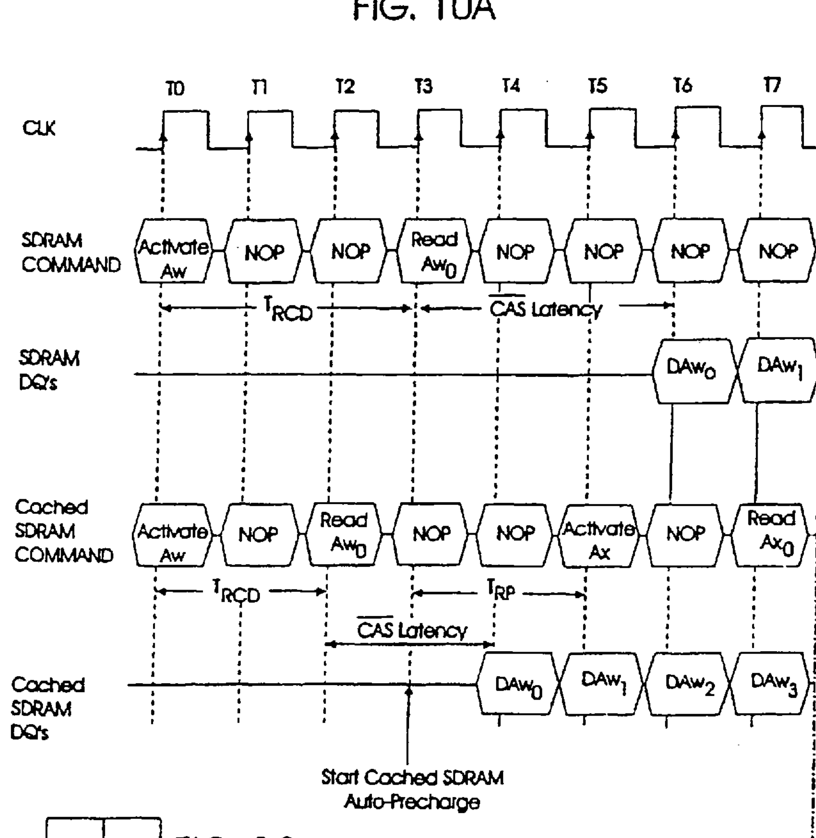
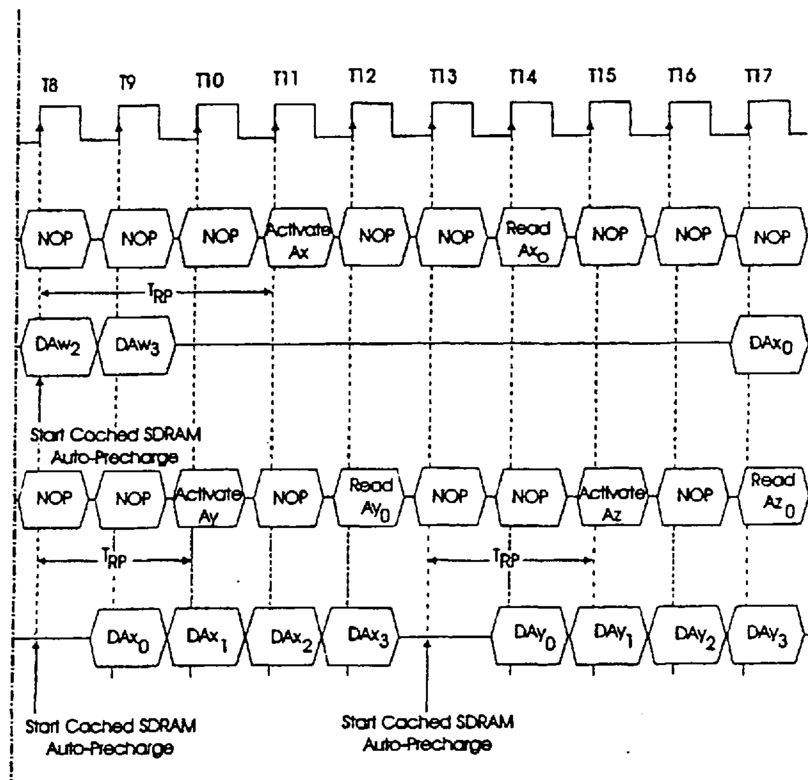


FIG. 10A
T0
T1
T2
T3
T4
T5
T6
T7
CLK
SDRAM COMMAND
Activate Aw
NOP
NOP
Read Aw0
NOP
NOP
NOP
NOP
TRCD
CAS Latency
SDRAM DQ's
DAw0
DAw1
Cached SDRAM COMMAND
Activate Aw
NOP
Read Aw0
NOP
NOP
Activate Ax
NOP
Read Ax0
TRCD
TRP
CAS Latency
Cached SDRAM DQ's
DAw0
DAw1
DAw2
DAw3
Start Cached SDRAM Auto-Precharge
FIG. 10A
FIG. 10B
FIG. 10

FIG. 10B



CACHED SYNCHRONOUS DRAM ARCHITECTURE HAVING A MODE REGISTER PROGRAMMABLE CACHE POLICY

This application is a continuation of application Ser. No. 83/733,841, filed Oct. 18, 1996, now abandoned.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to synchronous dynamic random access memory (SDRAM) device and, more particularly, to a cached SDRAM and a caching policy thereof.

2. Discussion of the Related Art

Turning now to FIG. 1, a block diagram of a standard SDRAM is shown, in particular, a 2Mbit×4 I/O×2 Bank SDRAM. Other configurations of SDRAMs are also known (e.g., 1Mbit×8 I/O×2 Bank, 512Mbit×16 I/O×2 Bank, etc.). The typical SDRAM **10** includes an address buffer **12**, first and second memory banks (**14A**, **14B**) and corresponding row decoders (**16A**, **16B**), column decoders (**18A**, **18B**), sense amplifiers (**20A**, **20B**), and data latches (**22A**, **22B**). Data input/output buffers **24** receive data to be written into a memory array (i.e., either array **14A** or **14B**) and output data read from a memory array (i.e., either array **14A** or **14B**).

An externally supplied system clock (CLK) signal is input to a clock buffer **26** (CLK Buffer), the CLK signal for providing system timing for the various function blocks of the SDRAM **10**. SDRAM **10** inputs are sampled on the rising edge of the CLK signal. An externally supplied clock enable signal (CKE) is input to a clock enable buffer **28** (CKE Buffer). The CKE buffer **28** provides an enable output to the CLK Buffer **26** and to a Self Refresh Clock **30**. CKE activates the CLK signal when in a high state and deactivates the CLK signal when low. By deactivating the clock CKE low initiates a Power Down mode, Suspend mode, or a Self Refresh mode. The Self Refresh Clock **30** and a Row Address Counter **32** operate in a standard manner for implementing the Self Refresh mode.

Address buffer **12** receives address inputs, A0–A11, and outputs information via address data lines **34** to the command decoder **36**, row decoders (**16A**, **16B**), column decoders (**18A**, **18B**), sequential controls (**38A**, **38B**) and mode register **40**. The data input/output buffer **24** provides input/outputs, corresponding to DQ0–DQ3.

The command decoder **36** outputs approximate command signals for executing a desired operation of the SDRAM **10**, in accordance with input signals which it receives. Examples of typical SDRAM operations include a Read operation and a Write operation. During a Read operation, upon the receipt of a Read command, the SDRAM **10** reads data from a particular memory location specified by the address received on the address lines. Similarly, during a Write operation, the SDRAM writes data received on the data input/output (I/O) lines DQ0–DQ3 into a particular memory location specified by the address received on the address lines. In conjunction with the carrying out of SDRAM operations, the command decoder **36** receives buffered inputs including a chip select (CS), row address strobe $\overline{RAS}$, column address strobe $\overline{CAS}$, write enable WE, and a bank select (BS) input. In accordance with a first operation, the command decoder **36** provides a command signal to the row address counter **32** for performing a self refresh operation. In accordance with other operations, the command decoder **36** provides command

signals to a mode register **40**, row/column select blocks (**16A**, **16B**) for each memory bank (**14A**, **14B**), and sequential control blocks (**38A**, **38B**) for each memory bank, as appropriate for carrying out the desired synchronous memory operation wherein the synchronous memory operation corresponds to a standard SDRAM command decoded by the command decoder on a rising or falling clock edge. The mode register **40**, for instance, provides a control signal to a respective sequential control (**38A**, **38B**) of each memory bank (**14A**, **14B**). The sequential control for each memory bank controls respective data latches associated with the respective memory bank. The Mode Register **40** receives input data via address buffer **12** for programming the operating mode, $\overline{CAS}$Latency, burst type ($\overline{BT}$), and burst length as shown in FIG. 2. The row/column select (**42A**, **42B**) for each memory bank (**14A**, **14B**) controls respective row decoders (**16A**, **16B**) and column decoders (**18A**, **18B**) associated with the respective memory bank (**14A**, **14B**). A buffered data mask input (DWM) is connected to the data input/output buffers **24** for selectively masking all or none of the data inputs or data outputs of the SDRAM chip **10**. Specific implementations for Read, Write, Refresh, and other typical operations of the SDRAM, as shown in FIG. 1, are known in the art and not further discussed herein.

As discussed above, synchronous DRAM products are generally known in the art. Industry standards for SDRAMs have been established, i.e., electrical and mechanical. Included in the standards for 16Mbit synchronous DRAM products, for example, is a requirement that all of the control, address and data input/output circuits are synchronized with the positive edge of an externally supplied clock. Additionally, prior to any access operation, the CAS latency, burst length, and burst sequence must be programmed into the device by address inputs A0–A9 during a Mode Register Set cycle.

While standard synchronous DRAMS are designed to be flexible through programmability and to provide higher burst rates not achievable with asynchronous DRAMs, unfortunately, a standard SDRAM does not improve the initial latency of a page hit or miss. A page hit occurs during a read cycle when the row being accessed is already being sensed by the sense amplifiers and the memory array or bank is open. A page miss occurs during a read cycle when the row being accessed is not currently being sensed by the sense amplifiers, wherein the memory bank must first be closed, reactivated, refreshed, and reopened. Furthermore, the standard SDRAM does not reduce the penalties caused by the DRAM cycle time (t_{RC}) and the DRAM precharge time (t_{RP}). With multiple memory banks, a standard SDRAM does allow the user to perform simultaneous operations on both memory banks in order to hide some of the precharge and cycle time delays. However, this feature is only useful if the data being stored is orderly and can be organized such that the SDRAM can ping-pong between the two open banks uninterrupted. With today's multi-tasking computer operating systems, this is a formidable task. Standard SDRAMs thus suffer some performance limitations including, for instance, an inability to fully utilize the memory bandwidth and further having undesirable system wait states for all memory accesses.

SUMMARY OF THE INVENTION

An object of the present invention to solve performance issues of standard SDRAMs by reducing the latency of the memory and allowing simultaneous operations to occur on the same memory bank, that is, using a single memory bank of a multi-bank device.

Another object of the present invention is to enable a full utilization of memory bandwidth and to eliminate system wait states for all memory accesses.

According to the present invention, a cached synchronous dynamic random access memory (cached SDRAM) device having a multi-bank architecture and a programmable caching policy includes a synchronous dynamic random access memory (SDRAM) bank, the SDRAM bank including a row decoder coupled to a memory bank array for selecting a row of data in the memory bank array. Sense amplifiers are coupled to the memory bank array via bit lines for latching the row of data selected by the row decoder. A synchronous column selected means is provided for selecting a desired column of the row of data. A randomly addressable row register stores a row of data latched by the sense amplifiers. A select logic gating means is disposed between the sense amplifiers and the row register for selectively gating the row of data present on the bit lines to the row register in accordance to particular synchronous memory operations of the cached SDRAM being performed. Data to be input into cached SDRAM during a Write operation is received by the same amplifiers and written into the memory bank array. Data to be output from the cached SDRAM during a Read operation is read out only from the SSRAM, the row of data contained in the row register first having been read from the memory bank array to the sense amplifiers and then selectively gated to the row register in accordance with the particular synchronous memory operations. A means is provided for programming of the cached SDRAM to operate in a Write Transfer mode (i.e., Write Allocate mode) corresponding to a Normal Operation mode of a standard SDRAM during a Write cycle, and to operate in a No Write Transfer mode (i.e., a No Write Allocate mode) according to an alternate operation mode during a Write cycle, thereby operating under a first and a second caching policy, respectively.

Alternatively, in accordance with the present invention, a method of implementing a programmable caching policy on a cached synchronous dynamic random access memory (cached SDRAM) device having a multi-bank architecture includes the steps of:

providing a synchronous dynamic random access memory (SDRAM) bank including a row decoder coupled to a memory bank array for selecting a row of data in the memory bank array, sense amplifiers coupled to the memory bank array via bit lines for a latching the row of data selected by the row decoder, and a synchronous column select means for selecting a desired column of the row of data;

providing a randomly addressable row register for storing a row of data latched by the sense amplifiers;

providing a select logic gating means, disposed between the sense amplifiers and the row register, for selectively gating the row of data present on the bit lines to the row register in accordance to particular synchronous memory operations of the cached SDRAM being performed, wherein data to be input into the cached SDRAM during a Write operation is received by the sense amplifiers and written into the memory bank array and wherein data to be output from the cached SDRAM during a Read operation is read out only from the row register, the row of the data contained in the row register first having been read from the memory bank array to the sense amplifiers and then selectively gated to the row register in accordance with the particular synchronous memory operation; and

programming of the cached SDRAM to operate in a Write Transfer mode corresponding to a Normal Operation mode of a standard SDRAM during a Write cycle, and to operate in a No Write Transfer mode according to an alternate operation mode during a Write cycle, thereby operating under a first and a second caching policy, respectively.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other teachings and advantages and advantages of the present invention will become more apparent upon a detailed description of the best mode for carrying out the invention as rendered below. In the description to follow, reference will be made to the accompanying drawings, where like reference numerals are used to identify like parts in the various views and in which:

FIG. 1 shows a block-diagram of a known (2Mbit×4 I/O×2 Bank) synchronous dynamic random access memory device;

FIG. 2 is exemplary of address inputs used in conjunction with a programming of a mode register of a known SDRAM;

FIG. 3 shows a block diagram of a cached (2Mbit×4 I/O ×2 Bank) synchronous dynamic random access memory device according to the present invention;

FIG. 4 illustrates a portion of the cached SDRAM according to the present invention as shown in the block diagram of FIG. 3 in greater detail;

FIG. 5 illustrates a flow diagram for explanation of a portion of the programmable caching policy in accordance with the present invention;

FIG. 6 is exemplary of address inputs used in conjunction with a programming of a mode register of a cached SDRAM in accordance with the present invention;

FIG. 7 shows an example of an Auto Refresh command during cache (page) reads (burst length=4, $\overline{CAS}$ latency=2);

FIG. 8 shows an example of a Read followed by a Read miss (burst length=4, $\overline{CAS}$ latency=2);

FIG. 9 shows an example of a Read miss followed by a Write miss (burst length=4, $\overline{CAS}$ latency=2), and

FIG. 10 is illustrative of a comparison of timing diagrams of a standard SDRAM versus a cached SDRAM according to the present invention for random row reads to the same bank;

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

Because dynamic random access memories (DRAMs), and more particularly, synchronous DRAMs are known in the art, the present invention shall be described in particular to elements forming part of, or cooperating directly with, the invention. It is to be understood, however, that other elements not specifically shown or described may take various forms known to persons of ordinary skill in the semiconductor memory art. In addition, for clarity purposes, the present invention shall be described with respect to a 16Mbit SDRAM (2Mbit×4 I/O×2 Bank). Other SDRAM densities, organizations, and bank quantities are possible.

Referring now to FIG. 3, a block diagram of a cached SDRAM 100 according to the present invention is shown. An 8K bit integrated cache on the SDRAM 100 comprises a 4Kbit integrated static random access memory (row register) (102A, 102B) for each SDRAM bank (104A, 104B). As used in the following, the terms "cache," "integrated row register," and "static random access memory" are used interchangeably and shall be interpreted to mean a static random access memory. Furthermore, the discussion to follow shall refer to Bank A (104A) and the associated

integrated row register 102A, however, the discussion is equally applicable to Bank B (104B) and the associated integrated row register 102B. Still further, the following detailed description of the present invention includes the use of the terms "hit" and "miss," which shall hereafter refer to a page of data contained in a row register (to be discussed further herein below). A "hit" occurs when the row being accessed is already in the row register, thus a new row of a memory bank array does not need to be accessed. A "miss" occurs when the row being accessed is not the one currently in the row register. A "miss" on a Write command may not affect the row register, while on the other hand a "miss" on a Read command causes the new row to be loaded into the row register. The content of the row register is always equal to the last row Read from the SDRAM array as modified by any Writes that may have occurred in an interim period.

When a row of the SDRAM Bank A is activated, the row data is latched by the associated sense amplifiers 106A, but does not get directly transferred into the cache 102A. This allows the SDRAM array 104A to be refreshed or a new row access to be initiated without modifying the current contents of the cache 102A. However, when a Read command occurs after a new row has been activated, the entire row is automatically transferred into the cache 102 where it is then read from the chip 100 within the specific $\overline{CAS}$ Latency. In accordance with the invention, all Read commands synchronously retrieve data from the SDRAM array (104A, 104B) and through the SRAM cache (102A, 102B) and do not directly access the SDRAM array (104A, 104B), as will be discussed further herein below with reference to a "Write Transfer" mode and a "No Write Transfer" mode.

In accordance with the one aspect of the present invention, the cached SDRAM architecture improves systems performance by reducing the latency of the memory, in addition to allowing the system to perform concurrent operations on a same bank of DRAM memory. Since Reads always access the cache according to the present invention, and Write data is buffered, the cached SDRAM is able to perform random column access at SRAM speeds.

Using the row register (102A, 102B), the cache SDRAM of the present invention is able to perform concurrent operations to the same bank (104A, 104B, respectively). This ability to perform concurrent operations provides a significant increase in the performance of the memory, in some instances, effectively doubling a memory's bandwidth over that of a standard SDRAM (See FIG. 10).

Referring now to FIGS. 3 and 4, a cached synchronous dynamic random access memory (cached SDRAM) device 100 having a multi-bank architecture includes a synchronous dynamic random access memory (SDRAM) bank including a row decoder 116A coupled to a memory bank array 104A for selecting a row of data in the memory bank array. Sense amplifiers 120A are coupled to the memory bank array 104A via bit lines 119A for latching the row of data selected by the row decoder 116A. A column decoder 118A is provided for selecting a desired column of the row of data. A row register 102A is provided for storing a row of data latched by the sense amplifiers 120A. The column decoder 118A of the SDRAM is further for selecting a desired column of the row of data stored by the row register 102A.

FIG. 4 shows in detail a select logic gating means 121, disposed between the sense amplifiers 120A and the row register 102A is provided for selectively gating the row of data present in the sense amplifier 121A to said row register 102A in accordance a particular memory operation of the cached SDRAM 100 being performed. Select logic gating means 121A includes appropriate logic circuitry for performing a desired gating of a row of data from the sense amplifiers 120A to the row register 102A. Data to be input into cached SDRAM 100 during a Write operation is received by the sense amplifiers 120A and written into the memory bank array 104A. In addition, data to be output from cached SDRAM 100 during a Read operation is read out only from the row register 102A, the row of data contained in the row register 102A first having been read from the memory bank array 104A to the sense amplifiers 120A and then selectively gated to the row register 102A in accordance with the particular synchronous memory operation. For instance, subsequent to a Read operation in which a row of data selected by the row decoder is gated into the row register 102A and upon an occurrence of a additional subsequent memory operation affecting the same row of data in the memory bank array (such as a Write operation), the select logic gating means 121A can gate the affected row of data present can the bit lines to the row register 102A, thereby maintaining a row data coherency.

In addition to the above, the cached SDRAM 100 of the present invention further includes data input/output (I/O) buffers 124 having nput lines for receiving the data to be input into and output from the cached SDRAM 100. Data latches 122A are coupled between the data I/O bufers 124 and the row register 102A for latching data output from the row register 102A onto the data I/O buffers 124. The data latches 122A further are coupled between the data I/O bufers 124 and the sense amplifiers 120A for latching from cached SDRAM 100, and more particularly now register 120A, is synchronous data synchronized with the external clock signal being applied to cached SDRAM 100.

A control means (not shown), such as a microprocessor or memory controller, can be used for controlling the cached SDRAM 100 for enabling concurrent memory operations to occur on the row register 102A and on a corresponding memory bank array of a same ban 104A of the multi-bank architecture. The control means can control the cached SDRAM 100 for enabling of Burst Read operation on the row register 102A and a bank Precharge operation on the memory bank array 104A of the same bank of the multi-bank architecture to occur concurrently. Alternatively, the control means can control the cached SDRAM 100 for enabling a Burst read operation on row register 102A and a bank activate operation on the corresponding memory bank array 104A of the same bank of the multi-bank architecture to occur concurrently. The control means may further control the cached SDRAM 100 for enabling a burst read operation on the row register 102A and a bank refresh operation on the corresponding memory bank array 104A of the same bank of the multi-bank architecture to occur concurrently.

The cached SDRAM 100 of the present invention further includes a second synchronous dynamic random access memory (SDRAM) bank including a second row decoder coupled to a second memory bank array for selecting a second row of data in the second memory bank array, a second sense amplifiers coupled to the second memory bank array via second bit lines for latching the row of data selected by the second row decoder, and a second column decoder for selecting a desired column of the row of data. A second randomly addressable row register stores a row of data latched by the second sense amplifiers. A second select logic gating means, integrated with the sense amplifiers, as 106B, is disposed between the second sense amplifiers and the second row register 102B, for selectively gating the row of data present on the second bit lines to the row register 102B in accordance to particular memory operations of the

cached SDRAM being performed. Data to be input into the second bank of the cached SDRAM 100 during a Write operation is received by the second sense amplifiers 106B and written into the second memory bank array 104B. Data to be output from the second bank of the cached SDRAM during a Read operation is read out only from the second row register 102B, the row of data contained in the second row register 102B first having been read from the second memory bank array 104B to the second sense amplifiers and then selectively gated to the second row register 102B in accordance with the particular synchronous memory operations.

With reference to FIGS. 7, 8 and 9, the following is a discussion on which concurrent operations are allowed and how they can be used to maximize memory performance and minimize system watts states.

Referring now to FIG. 7 (in conjunction with FIGS. 3, 4 and 5) when a Bank Activate command is given to the cached SDRAM, the row is selected in memory and the data is latched by the sense amplifiers 106A. At this point the contents of the cache 102A remain unchanged. When a Read command is issued, the entire selected row is transferred into the cache 102A within one clock cycle and the first Read data appears on the outputs within two clock cycles. On the clock cycle following the Read command, the row data is latched in both the cache 102A and the sense amplifiers 106A. Since all Reads retrieve data from the cache 102A and do not access the array 104A, the DRAM array 104A no longer needs to be held open. As a result, the DRAM array 104A can be precharged on the clock cycle following the Read command using the auto-precharge function (Read with Auto-Precharge). The manual Precharge command cannot be used at this time because it would terminate the burst Read. Note that Manual Precharge termination of a burst is implemented with the cached SDRAM of the present invention in order to maintain a backward compatibility with standard SDRAMs. To allow the burst to complete, the Manual Precharge Command can be given two clock cycles before the end of the Read burst. Once the SDRAM array 104A has been precharged, the system (not shown) can issue the Auto Refresh command (Time T5 of FIG. 7) and/or another Bank Activate command to the same or different Bank during cache (i.e., page) Read accesses.

The ability of the cached SDRAM to perform a Bank Activate during a cache (page) Read gives the system the option to pipeline memory accesses to the same bank. This is accomplished by a controller closing the open page and then starting a new row access (to the same page) while bursting out Read data from the previous row held in the cache (FIG. 8). Using pipelining, the precharge time and the t_{RCD} of a page miss can be completely hidden during a Read burst as well as a portion of the $\overline{CAS}$ Latency. This is a very powerful feature of the cached SDRAM 100, and in the case of random row Reads, pipelining can more than double the bandwidth of the memory (FIG. 10). The row cache can also be used to hide some of the latency of a Write miss cycle following a Read cycle as shown in FIG. 9.

Combining the reduced latency of the cached SDRAM with the capability of overlapping memory access cycles gives the cached SDRAM a significant performance advantage over standard SDRAM (see FIG. 10). That is, the cached SDRAM can reduce the latency of a Read page miss to that of a Read page hit, thereby more than doubling the performance of the memory over a SDRAM operating at the same clock frequency. It should be noted that Write bursts cannot be pipelined due to the fact that a DRAM must be held open and cannot be precharged during a Write cycle until the last bit of input data is properly stored in the memory cell.

Turning once again to FIGS. 3–6, the row data from the DRAM sense amplifiers (106A, 106B) is transferred into the cache (102A, 102B) only on a first Read or Write command (and with respect to the Write command, only in the instance of the chip being in the Write Transfer Mode) occuring after a Bank Activate command. Any subsequent Read or Write commands to the same row do not load the cache (102A, 102B) and the cache contents remain unchanged. In other words, multiple reads to a same row does not cause reloading of the cache each time.

In accordance with another embodiment of the present invention, the cached synchronous dynamic random access memory (cached SDRAM) device 100 having a multi-bank architecture and a programmable caching policy includes a synchronous dynamic random access memory (SDRAM) bank including a row decoder 116A coupled to a memory bank array 104A for selecting a row of data in the memory bank array 104A, sense amplifiers 120A coupled to the memory bank array 104A via bit lines 119A for latching the row of data selected by the row decoder 116A, and a column decoder 118A for selecting a desired column of the row of data. A randomly addressable row register 102A stores a row of data latched by the same amplifiers 120A. A select logic gating means 121A is disposed between the sense amplifiers 120A and the row register 102A for selectively gating the row of data present in the sense amplifier 120A to row register 102A in accordance a particular synchronous memory operation of the cached SRAM 100 being performed. Data to be input into cached SDRAM 100 during a Write operation is received by the sense amplifiers 120A and written into the memory bank array 104A. Data to be output from cached SDRAM 100 during a Read operation in read out only from the row register 102A, the row of data contained in row register 102A first having been read from the memory bank array 104A to the sense amplifiers 120A and then selectively gated to the row register 102A in accordance with the particular memory operation. The column decoder 118A and of the SDRAM is further provided for selecting a desired column of the row of data stored by the row register 102A. Subsequent to a Read operation in which a row of data selected by the row decoder is gated into row register 102A, and upon an occurrence of a additional subsequent memory operation affecting the same row of data in the memory bank array, select logic gating means 121A gates the affected row of data present on the bit lines to the row register 102A, thereby maintaining a row data coherency.

A means 108 is provided for programming of the cached SDRAM 100 to operate in a Write Transfer mode (i.e., Write Allocate mode) corresponding to a Normal Operation mode of an industry standard SDRAM during a Write cycle, and to operate in a No Write Transfer mode (i.e., a No Write Allocate mode) according to an alternate operation mode during a Write cycle, thereby operating under a first and a second caching policy, respectively. Preferably, the programming means includes the mode register 108, as shall be discussed further herein below with reference to FIGS. 5 and 6. Alternatively, the programming may also be accomplished through other means such as a wirebond or metal mask option.

Select logic gating means 121A is responsive to a control signal from programming means 108A, wherein during the Write Transfer mode and upon an occurrence of a Write command, the caching policy is such that select logic gating means 121A automatically loads a previously activated row from the SDRAM array 104A in the row register 102A. Furthermore, during the No Write Transfer mode and upon

an occurrence of a Write command, the caching policy is such that the select logic gating means 121A does not transfer a previously activated row to the row register 102A, where in the latter instance, the row register 102A functions as an independent cache Read bank and the SDRAM array 104A functions as a semi-independent DRAM Write bank.

The cached SDRAM 100 can further include a second synchronous dynamic random access memory (SDRAM) bank including a second row decoder coupled to a second memory bank array for selecting a second row of data in the second memory bank array, second sense amplifiers coupled to the second memory bank array via second bit lines for latching the row of data selected by the second row decoder, and a second column decoder for selecting a desired column of the row of data. A second randomly addressable row register is provided for storing a row of data latched by the second sense amplifiers. Furthermore, a second select logic gating means, disposed between the second sense amplifiers and the second row register, is provided for selectively gating the row of data present on the second bit lines to said row register in accordance a particular memory operation being performed. Data to be input into the second SDRAM during a Write operation is received by the second sense amplifiers and written into the second memory bank array. Data to be output from the second SDRAM during a Read operation is read out only from the second row register, the row of data contained in the second row register first having been read from the second memory bank array to the second sense amplifiers and then selectively gated to the second row register in accordance with the particular memory operation.

In accordance with another aspect according to the present invention, a method of implementing a programmable caching policy on a cached synchronous dynamic random access memory (cached SDRAM) device having a multi-bank architecture includes the steps of:

providing a synchronous dynamic random access memory (SDRAM) bank including a row decoder coupled to a memory bank array for selecting a row of data in the memory bank array, sense amplifiers coupled to the memory bank array via bit lines for latching the row of data selected by the row decoder, and a column decoder for selecting a desired column of the row of data;

providing a randomly addressable row register (ROW REGISTER) for storing a row of data latched by the sense amplifiers;

providing a select logic gating means, disposed between the sense amplifiers and said row register, for selectively gating the row of data present on the bit lines to the row register in accordance a particular synchronous memory operation of the cached SDRAM being performed, wherein data to be input into the cached SDRAM during a Write operation is received by the sense amplifiers and written into the memory bank array and wherein data to be output from the cached SDRAM during a Read operation is read out only from the row register, the row of data contained in the row register first having been read from the memory bank array to the sense amplifiers and then selectively gated to the row register in accordance with the particular synchronous memory operation; and

programming of the cached SDRAM to operate in a Write Transfer mode corresponding to a Normal Operation mode of an industry standard SDRAM during a Write cycle, and to operate in a No Write Transfer mode during a Write cycle thereby operating under a first an a second caching policy, respectively.

In addition, the method further includes providing the select logic gating means for being responsive to a control signal from the programming means, wherein during the Write Transfer mode and upon an occurrence of a Write command, the caching policy is such that the select logic gating means automatically loads a previously activated row from the SDRAM array into the row register. Furthermore, during the No Write Transfer mode and upon an occurrence of a Write command, the caching policy is such that the select logic gating means does not transfer a previously activated row to the row register, where in the latter instance, the row register functions as an independent cache Read bank and the SDRAM array functions as a semi-independent DRAM Write bank. Still further, the method includes a step wherein subsequent to a Read operation in which a row of data selected by the row decoder is gated into the row register, and upon an occurrence of a additional subsequent memory operation affecting the same row of data in the memory bank array, the select logic gating means gates the affected row of data present on the bit lines to the row register, thereby maintaining a row data coherency.

The programmable caching policy method in accordance with the present invention can further comprise providing a second synchronous dynamic random access memory (SDRAM) bank including a second row decoder coupled to a second memory bank array for selecting a second row of data in the second memory bank array, second sense amplifiers coupled to the second memory bank array via second bit lines for latching the row of data selected by the second row decoder, and a second column decoder for selecting a desired column of the row of data. A second randomly addressable row register is provided for storing a row of data latched by the second sense amplifiers. A second select logic gating means, disposed between the second sense amplifiers and the second row register, is provided for selectively gating the row of data present on the second bit lines to the row register in accordance a particular synchronous memory operation being performed. Data to be input into the second SDRAM during a Write operation is received by the second sense amplifiers and written into the second memory bank array. Alternatively, data to be output from the second SDRAM during a Read operation is read out only from the second row register, the row of data contained in the second row register first having been read from the second memory bank array to the second sense amplifiers and then selectively gated to the second row register in accordance with the particular synchronous memory operation.

In further discussion of the Write Transfer mode and the No Write Transfer mode of operation, the present invention incorporates a programmable caching policy for providing a maximum device flexibility. This feature allows an cached SDRAM user to optimize the cached SDRAM's cache for a particular application, resulting in obtaining an optimal memory performance and compatibility. With respect to the present invention, the mode register 108, as shown in FIGS. 3 and 6, is preferably used for selecting whether the Write Transfer mode or the No Write Transfer mode of operation shall be used in a particular application. During a Mode Register Set cycle, the Normal/Write Allocate (Write Transfer) mode or the No Write Allocate (No Write Transfer) mode is selected based upon the content of address lines A7–A11/BS as shown in FIG. 6.

If a Write command occurs after a new row activate, the Mode Register 108 is queried to determine whether or not the data from the sense amplifiers (106A, 106B) are to be loaded into the cache (102A, 102B) i.e., whether or not to transfer wordline data from the sense amplifiers to the cache.

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If the Mode Register 108 indicates that the cached SDRAM 100 chip is in a Write Transfer mode, a Write command causes the sense amplifier data to be loaded from the SDRAM array (104A, 104B) into the cache (102A, 102B). If the mode register 108 indicates that the cached SDRAM 100 chip is in a No Write Transfer mode, a Write command does not cause an automatic transfer of the sense amplifier data into the cache (102A, 102B). If a Write hit occurs (i.e., the Write page is already in the cache), the cached SDRAM 100 will automatically update the cache, as the data is written to the DRAM array (104A, 104B). (See FIGS. 5 and 6).

In an instance in which the cached SDRAM is used in the Write Transfer (Normal) mode, a Write miss will cause a new row of data to be activated and transferred from the SDRAM array (104A, 104B) into the cache (102A, 102B) overwriting any previous information stored in the cache (102A, 102B). Since Read operations always load the cache (102A, 102B), the row data in the SDRAM sense amplifiers (106A, 106B) will always equal the cache data after a Read or a Write command is given. Therefore, in Write Transfer mode, only one DRAM cache row per bank (104A, 104B) is available for reading or writing (See FIG. 5).

Referring again to FIG. 7, a more detailed discussion of the Write Transfer mode shall be given. When a Read miss occurs, a Bank activate command must be issued for a new row. After a time t_{RCD}, a Read command or a Read with Auto Precharge command can be given to the cached SDRAM in order to access data from the new row. When the Read command is issued at time T0, data from row X is transferred from the SDRAM bank into the cache on a same clock cycle. If the Auto Precharge function is invoked, the DRAM precharge is started on the clock cycle following the Read command. Two clock cycles later, the SDRAM bank is closed or precharged and a new row Y from the same bank can be activated (clock time T3). When a Write command is issued a time T5, the cached SDRAM transfers sense amplifier data (row Y) into the cache. At this point, both the SDRAM sense amplifiers and the cache are holding the same information (row Y). Any subsequent Read command will read row Y column data from the cache (see times T7–T9 of FIG. 7). Similarly, any subsequent Write command will simultaneously write data to row Y being held in the sense amplifiers and also update row Y in the cache.

Since the SDRAM sense amplifiers 102A and the cache 106A will always hold the same row after a Read or Write command is issued, a memory controller (not shown) would require only one page tag per bank of the cached SDRAM. This is the same number of page tags per bank required for an industry standard SDRAM. In addition, the control of the SDRAM/cache bank (104A, 102A) would be identical to the control of a standard SDRAM's DRAM bank. For further compatibility with a standard SDRAM, the binary code of the Write Transfer mode corresponds to the code for the Normal Operation mode of an industry standard SDRAM (See FIG. 6). These features help make the cached SDRAM 100% (one hundred percent) compatible with a SDRAM, allowing the cached SDRAM to replace a standard SDRAM without making any modifications to an existing memory controller and system (not shown).

When the cached SDRAM is placed in the No Write Transfer mode, a Write miss will not transfer a new row into the cache (See FIG. 5). Instead, the new row is updated in the DRAM sense amplifiers, thereby, leaving the cache contents unaffected. This advantageously allows the cached SDRAM to have a Read page and a Write page open simultaneously in the same DRAM bank.

Referring again to FIG. 8, the No Write Transfer mode shall be further discussed. When a Read miss occurs, a Bank Activate command must be issued to activate a new row. After a time t_{RCD}, a Read command can be given to the cached SDRAM in order to access data from the new row. When the Read command is issued at time T0, data from row X is transferred from the SDRAM into the cache on the same clock cycle. If the Auto Precharge function is invoked, the SDRAM precharge is started on the clock cycle following the Read command. Two clock cycles later, the SDRAM bank is closed and the new row Y can be activated. When a Write command is issued a time T5, the cached SDRAM does not load the row Y into the cache. Instead, the Write data is used to update the SDRAM sense amplifiers 106A and the cache 102A remains unaffected. At this point, there are two rows (row X and row Y) open in the bank from which column Reads/Writes can occur. Any subsequent Read command will read column data from row X in the cache (see time T7–T9 in FIG. 8). Similarly, any subsequent Write command will write data to row Y in the SDRAM. Data cannot be read from the row Y unless the SDRAM is precharged and row Y is reactivated, followed by a Read command. Similarly, data cannot be written to row X unless the SDRAM is precharged and row X is reactivated, followed by a Write command.

The above discussed No Write Transfer mode setup is ideal for a system (not shown) that reads data from one page of memory, processes the data, and then writes the results back to a different page of the memory. In this case, the cached SDRAM can have both the Read page and the Write page open simultaneously in the same bank. Additionally, any application in which data copy or data move operations occur frequently could advantageously encounter a performance benefit using the No Write Transfer mode of the cached SDRAM according to the present invention.

The cached SDRAM 100 thus represents an evolutionary improvement to a SDRAM. For instance, the design of the cached SDRAM 100 has been implemented in such a way as to maintain a backward compatibility with industry standard SDRAMs (e.g. 16 Mbit SDRAM). The cached SDRAM 100 of the present invention maintains a backwards compatibility with SDRAM by: (i) supporting the SDRAM command, address and data setup/hold times; (ii) using the same pin out and packages as industry standard 16 Mbit SDRAMs; (iii) using the same commands definitions, command sequence, and truth table as an SDRAM; and, (iv) providing support for $\overline{CAS}$ Latency of 3 operation at all frequencies of operation. To elaborate briefly on point (iv), the cached SDRAM can operate with frequencies ranging from 83 MHz to 133 MHz with a $\overline{CAS}$ Latency of 2. Standard SDRAMs require a $\overline{CAS}$ Latency of 3 to operate at all of these frequencies. As a result, a given cached SDRAM will support both a $\overline{CAS}$ Latency of 2 and 3 operation at its operation frequency. For example, a 100 MHz CAS Latency cached SDRAM part will operate with 100 MHz CAS Latency 3 SDRAM controls. However, the performance of the cached SDRAM will be the same as an SDRAM in this situation if the SCRAM control does not take advantage of any of the performance improvements of the cached SDRAM.

From a functionality point of view, the cached SDRAM according to the present invention can be made plug-compatible with a standard SDRAM. Furthermore, it can be programmed as indicated herein for operating like a standard SDRAM when given SDRAM control signals.

As discussed herein, the cached SDRAM advantageously solves performance limitations of a standard SDRAM. For example, the cached SDRAM reduces the column latency of

a standard SDRAM by having all Read operations occur from the row register. In addition, the cached SDRAM increases memory performance by supporting concurrent operations on the same bank. Thus a user is allowed to pipeline accesses and overlap commands in order to hide the latency of the SDRAM. These changes can lead to more than twice the memory performance over standard SDRAM at the same clock frequency (ad exemplified in FIG. 10). Again, the design of the cached SDRAM represents an evolutionary change that enables the user to fully utilize memory bandwidth and eliminate system wait states for all memory accesses.

While the invention has been particularly shown and described with reference to specific embodiments thereof, it will be understood by those skilled in the art that various changes in form an detail may be made thereto, and that other embodiments of the present invention beyond embodiments specifically described herein may be made or practiced without departing from the spirit and scope of the invention as claimed.

What is claimed is:

1. A cached synchronous dynamic random access memory (cached SDRAM) device having a multi-bank architecture and a programmable caching policy, said cached SDRAM comprising:

- a synchronous dynamic random access memory (SDRAM) bank including a row decoder coupled to a memory bank array for selecting a row of data in the memory bank array, sense amplifiers coupled to the memory bank array via bit lines for latching the row of data selected by the row decoder, and a synchronous column select means for selecting a desired column of the row of data;
- a randomly addressable row register for storing a row of data latched by the sense amplifiers;
- a select logic gating means, disposed between the sense amplifiers and said row register, for selectively gating the row of data present on the bit lines to said row register in accordance to particular synchronous memory operations of said cached SDRAM being performed, wherein data to be input into said cached SDRAM during a Write operation is received by the sense amplifiers and written into the memory bank array and wherein data to be output from said cached SDRAM during a Read operation is read out only from said row register, the row of data contained in said row register first having been read from the memory bank array to the sense amplifiers and then selectively gated to said row register in accordance with the particular synchronous memory operations; and
- means for programming said cached SDRAM to operate in a Write Transfer mode corresponding to a Normal Operation mode of a standard SDRAM during a Write cycle, and to operate in a No Write Transfer mode according to an alternate operation mode during a Write cycle, thereby operating under a first and a second caching policy, respectively.

2. The cached SDRAM device of claim 1, further wherein said select logic gating means is responsive to a control signal from said programming means, wherein during the Write Transfer mode and upon an occurrence of a Write command, the caching policy is such that said select logic gating means automatically loads a previously activated row from the sense amplifiers into said row register, and further wherein during the No Write Transfer mode and upon an occurrence of a Write command, the caching policy is such that said select logic gating means does not transfer a

previously activated row to said row register, where in the latter instance, said row register functions as an independent cache Read bank and the SDRAM array functions as a semi-independent DRAM Write bank.

3. The cached SDRAM device of claim 1, wherein the synchronous column select means of said SDRAM is further for selecting a desired column of the row of data stored by said row register.

4. The cached SDRAM device of claim 1, wherein subsequent to a Read operation in which a row of data selected by the row decoder is gated into said row register, and upon an occurrence of a additional subsequent synchronous memory operation affecting the same row of data in the memory bank array, said select logic gating means gates the affected row of data present on the bit lines to said row register, thereby maintaining a row data coherency.

5. The cached SDRAM device of claim 1, further comprising:

- a second synchronous dynamic random access memory (SDRAM) bank including a second row decoder coupled to a second memory bank array for selecting a second row of data in the second memory bank array, second sense amplifiers coupled to the second memory bank array via second bit lines for latching the row of data selected by the second row decoder, and a second synchronous column select means for selecting a desired column of the row of data;
- a second randomly addressable row register for storing a row of data latched by the second sense amplifiers; and
- a second select logic gating means, disposed between the second sense amplifiers and said second row register, for selectively gating the row of data present on the second bit lines to said row register in accordance to particular synchronous memory operations of said cached SDRAM being performed, wherein data to be input into the said second SDRAM of said cached SDRAM during a Write operation is received by the second sense amplifiers and written into the second memory bank array and wherein data to be output from said second SDRAM of said cached SDRAM during a Read operation is read out only from said second row register, the row of data contained in said second row register first having been read from the second memory bank array to the second sense amplifiers and then selectively gated to the second row register in accordance with the particular synchronous memory operations.

6. The cached SDRAM device of claim 1, wherein said programming means includes a mode register.

7. The cached SDRAM device of claim 1, wherein said programming means includes a wirebond programming option.

8. The cached SDRAM device of claim 1, wherein said programming means includes a metal mask programming option.

9. A method of implementing a programmable caching policy on a cached synchronous dynamic random access memory (cached SDRAM) device having a multi-bank architecture, said method comprising the steps of:

- providing a synchronous dynamic random access memory (SDRAM) bank including a row decoder coupled to a memory bank array for selecting a row of data in the memory bank array, sense amplifiers coupled to the memory bank array via bit lines for latching the row of data selected by the row decoder, and a synchronous column means for selecting a desired column of the row of data;

providing a randomly addressable row register for storing a row of data latched by the sense amplifiers;

providing a select logic gating means, disposed between the sense amplifiers and the row registers, for selectively gating the row of data present on the bit lines to the row register in accordance to particular synchronous memory operations of the cached SDRAM being performed, wherein data to be input into the cached SDRAM during a Write operation is received by the sense amplifiers and written into the memory bank array and wherein data to be output from the cached SDRAM during a Read operation is read out only from the row register, the row of data contained in the row register first having been read from the memory bank array to the sense amplifiers and then selectively gated to the row register in accordance with the particular synchronous memory operations; and

programming of the cached SDRAM to operate in a Write Transfer mode corresponding to a Normal Operation mode of a standard SDRAM during a Write cycle, and to operate in a No Write Transfer mode according to an alternate operation mode during a Write cycle, thereby operating under a first and a second caching policy, respectively.

10. The method of claim 9, further wherein providing the select logic gating means further includes the selective logic gating means being responsive to a control signal from the programming means, wherein during the Write Transfer mode and upon an occurrence of a Write command, the caching policy is such that the select logic gating means automatically loads a previously activated row from the sense amplifiers into the row register, and further wherein during the No Write Transfer mode and upon an occurrence of a Write command, the caching policy is such that the select logic gating means does not transfer a previously activated row to the row register, where in the latter instance, the row register functions as an independent cache Read bank and the SDRAM array functions as a semi-independent DRAM Write bank.

11. The method of claim 9, wherein subsequent to a Read operation in which a row of data selected by the row decoder is gated into the row register, and upon an occurrence of a additional subsequent synchronous memory operation affecting the same row of data in the memory bank array, the select logic gating means gates the affected row of data present on the bit lines to the row register, thereby maintaining a row data coherency.

12. The method of claim 9, further comprising:

providing a second synchronous dynamic random access memory (SDRAM) bank including a second row decoder coupled to a second memory bank array for selecting a second row of data in the second memory bank array, second sense amplifiers coupled to the second memory bank array via second bit lines for latching the row of data selected by the second row decoder, and a second synchronous column select means for selecting a desired column of the row of data;

providing a second randomly addressable row register for storing a row of data latched by the second sense amplifiers; and

providing a second select logic gating means, disposed between the second sense amplifiers and the second row register, for selectively gating the row of data present on the second bit lines to the second row register in accordance to particular synchronous memory operations of the cached SDRAM being performed, wherein data to be input into the second SDRAM of the cached SDRAM during a Write operation is received by the second sense amplifiers and written into the second memory bank array and wherein data to be output from the second SDRAM of the cached SDRAM during a Read operation is read out only from the second row register, the row of data contained in the second row register first having been read from the second memory bank array to the second sense amplifiers and then selectively gated to the second row register in accordance with the particular synchronous memory operations.

13. The method of claim 9, wherein programming of the cached SDRAM includes utilizing a mode register.

14. The method of claim 9, wherein programming of the cached SDRAM includes utilizing a wirebond option.

15. The method of claim 9, wherein programming of the cached SDRAM includes utilizing a metal mask option.

16. A cached synchronous dynamic random access memory device comprising:

external clock means coupled to said memory device;

first and second synchronous dynamic random access memory banks;

a first row decoder coupled to the first memory bank array for selecting a row of data in the first memory bank array;

a first set of sense amplifiers coupled to the first memory bank array for latching the row of data selected by the first row decoder;

a first row register coupled to the first set of sense amplifiers for storing a row of data latched by the first set of sense amplifiers;

a first column decoder coupled to the first row register for selecting a desired column of the row of data selected by the first row decoder and stored in the first row register;

a first column write select logic means, disposed between said first set of sense amplifiers and the first row register for gating a row of data from the first set of sense amplifiers to the firs row register;

first data latches coupled between data I/O buffers an the first row register for latching data output, from the first row register to the I/O buffers and from the I/O buffers to the first set of sense amplifiers wherein data to be input into the cached synchronous dynamic random access memory device during a Write operation is received by the first sense amplifiers and written into the first memory bank array and data to be output from the cached synchronous dynamic random access memory device during a Read operation is read out only from the first row register, the row of data contained in the first row register having been read from the first memory bank array to the first sense amplifiers and then selectively gated to the first row register in accordance with a selected synchronous memory operation;

a second row decoder coupled to the second memory bank array for selecting a row of data in the second memory bank array;

a second set of sense amplifiers coupled to the second memory bank array for latching the row of data selected by the second row decoder;

a second row register coupled to the second set of sense amplifiers for storing a row of data latched by the second set of sense amplifiers;

a second column decoder coupled to the second row register for selecting a desired column of the row of data selected by the second row decoder and stored by the second row register;

a second column write select logic means, disposed between said second set of sense amplifiers and the second row register for gating a row of data from the second set of sense amplifiers to the second row register;

second data latches coupled between the data I/O buffers and the second row register for latching data output from the second row register to the data I/O buffers and from the data I/O buffers to the second set of sense amplifiers wherein data to be input into the cached synchronous dynamic random access memory device during a Write operation is received by the second set of sense amplifiers and written into the second memory bank array and data to be output from the cached synchronous dynamic random access memory device during a Read operation is read out only from the second row register, the row of data contained in the second row register having been read from the second memory bank array to the second sense amplifiers and then selectively gated to the second row register in accordance with a selected synchronous memory operation;

the data output from the cached synchronous dynamic random access memory device, and from the first and second row registers, being synchronized with the output signals from said external clock; and

control means for enabling concurrent memory operations to occur on said first and second row registers and the respective first and second memory bank arrays coupled thereto.

17. The cached synchronous dynamic random access memory device of claim 16 wherein the concurrent memory operations are a Burst Read operation on a selected row register and a bank Precharge operation on the memory bank array coupled to the selected row register.

18. The cached synchronous dynamic random access memory device of claim 16 wherein the concurrent memory operations are a Burst read operation on a selected one of said first and second row register and bank activate operation on the memory bank array 104A coupled to the selected row register.

19. The cached synchronous dynamic random access memory device of claim 16 wherein the concurrent memory operations are a Burst read operation on a selected for register 102A and a bank refresh operation on the memory bank array 104A coupled to the selected row register.

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(54) **SEMICONDUCTOR MEMORY DEVICE**

(75) Inventors: **Katsumi Dosaka; Masaki Kumanoya; Yasuhiro Konishi; Katsumitsu Himukashi; Kouji Hayano; Akira Yamazaki; Hisashi Iwamoto; Hideaki Abe; Yasuhiro Ishizuka; Tsukasa Saika**, all of Hyogo-ken (JP)

(73) Assignees: **Mitsubishi Denki Kabushiki Kaisha; Mitsubishi Electric Engineering Co., Ltd.**, both of Tokyo (JP)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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Related U.S. Application Data

(60) Continuation of application No. 08/865,310, filed on May 29, 1997, now Pat. No. 6,026,029, which is a division of application No. 08/625,578, filed on Mar. 28, 1996, now Pat. No. 5,848,004, which is a continuation of application No. 08/464,033, filed on Jun. 5, 1995, now abandoned, which is a division of application No. 07/869,917, filed on Apr. 15, 1992, now Pat. No. 5,652,723.

(30) **Foreign Application Priority Data**

Apr. 18, 1991	(JP)	3-85625
Aug. 23, 1991	(JP)	3-212140
Sep. 24, 1991	(JP)	3-242286
Feb. 3, 1992	(JP)	4-17809

(51) **Int. Cl.**[7] **G11C 11/00**
(52) **U.S. Cl.** **365/189.01**; 365/189.05
(58) **Field of Search** 365/189.01, 189.05, 365/185.09

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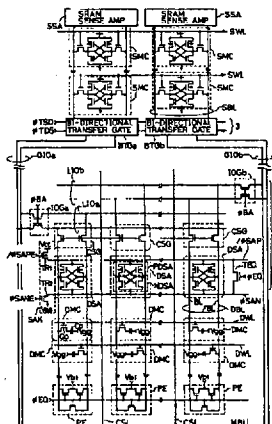
(List continued on next page.)

Primary Examiner—Terrell W. Fears
(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

(57) **ABSTRACT**

A semiconductor memory device includes a DRAM, an SRAM and a bi-direction transfer gate circuit provided between SRAM and DRAM. SRAM array includes a plurality of sets of word lines. Each set is provided in each row of SRAM array and each word line in each set is connected to a different group of memory cells of an associated row. An address signal for the SRAM and an address signal for the DRAM are separately applied to an address buffer. The semiconductor memory device further includes an additional function control circuit for realizing a burst mode and a sleep mode. A data transfer path from DRAM to the SRAM and a data transfer path from the SRAM to the DRAM are separately provided in the bi-directional transfer gate circuit. Data writing paths and data reading paths are separately provided in the DRAM array. By the above described structure, operation of the buffer circuit is stopped in the sleep mode, reducing power consumption. Since data writing path and data reading path are separately provided in the DRAM array, addresses to the DRAM array can be applied in non-multiplexed manner, so that data can be transferred at high speed from the DRAM array to the SRAM array, enabling high speed operation even at a cache miss.

5 Claims, 199 Drawing Sheets



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JP	1-128294	5/1989
JP	1-134517	5/1989
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"A Circuit Design of Intelligent Cache DRAM with Automatic Write–Back Capability", by K. Arimoto et al., IEEE Journal of Solid–State Circuits, vol. 26, No. 4, pp. 561–565.

* cited by examiner

FIG.1 PRIOR ART

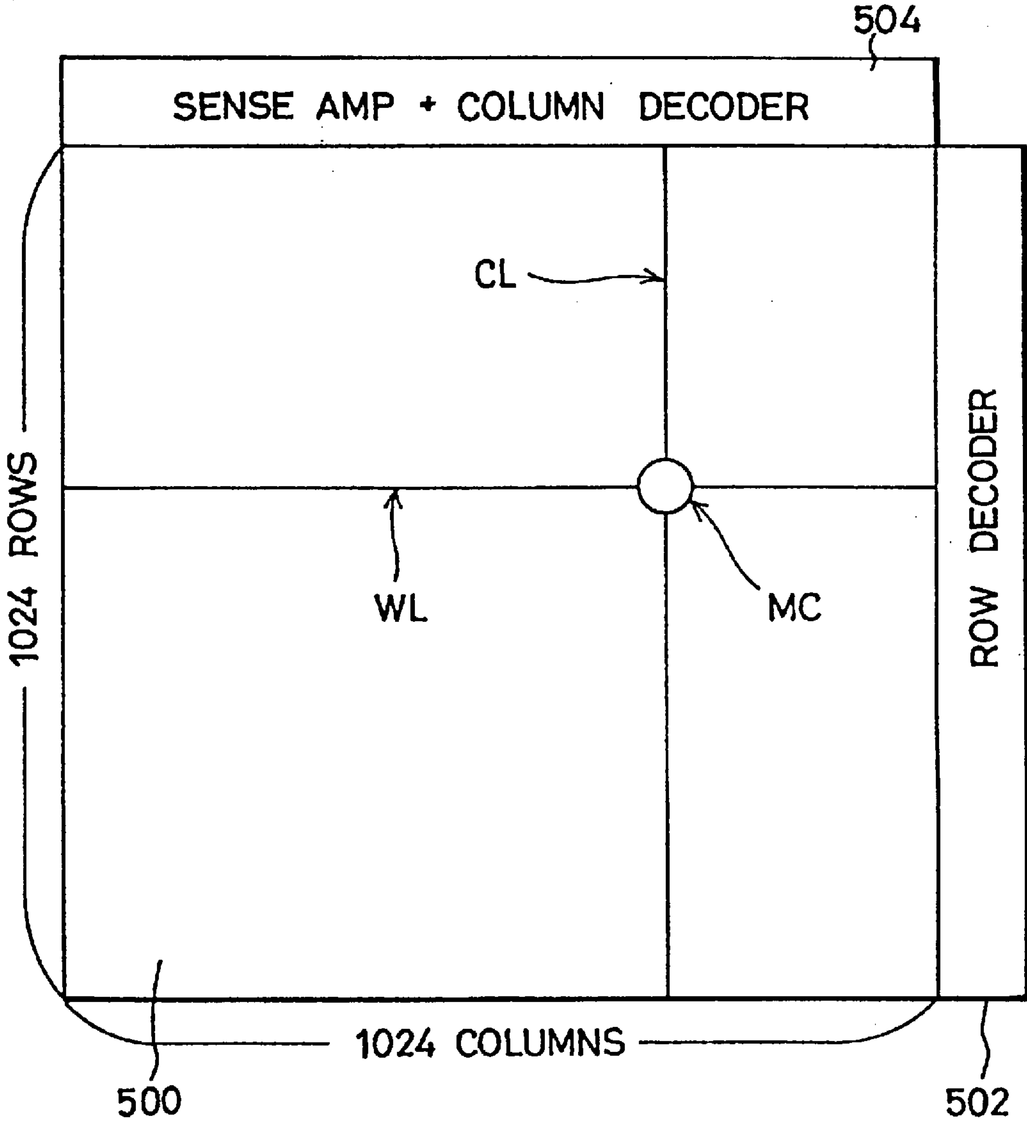


FIG. 2 PRIOR ART

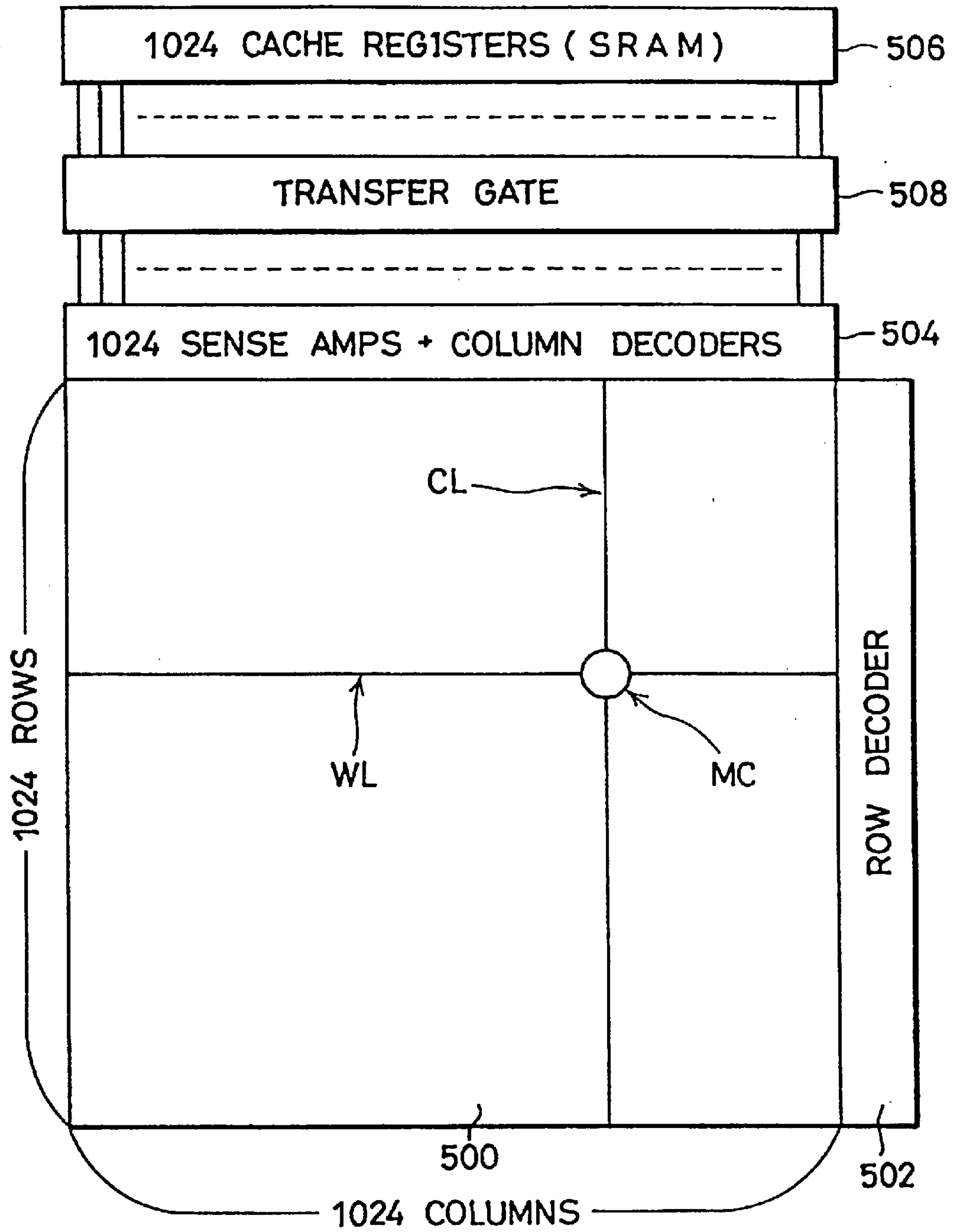


FIG.3 PRIOR ART

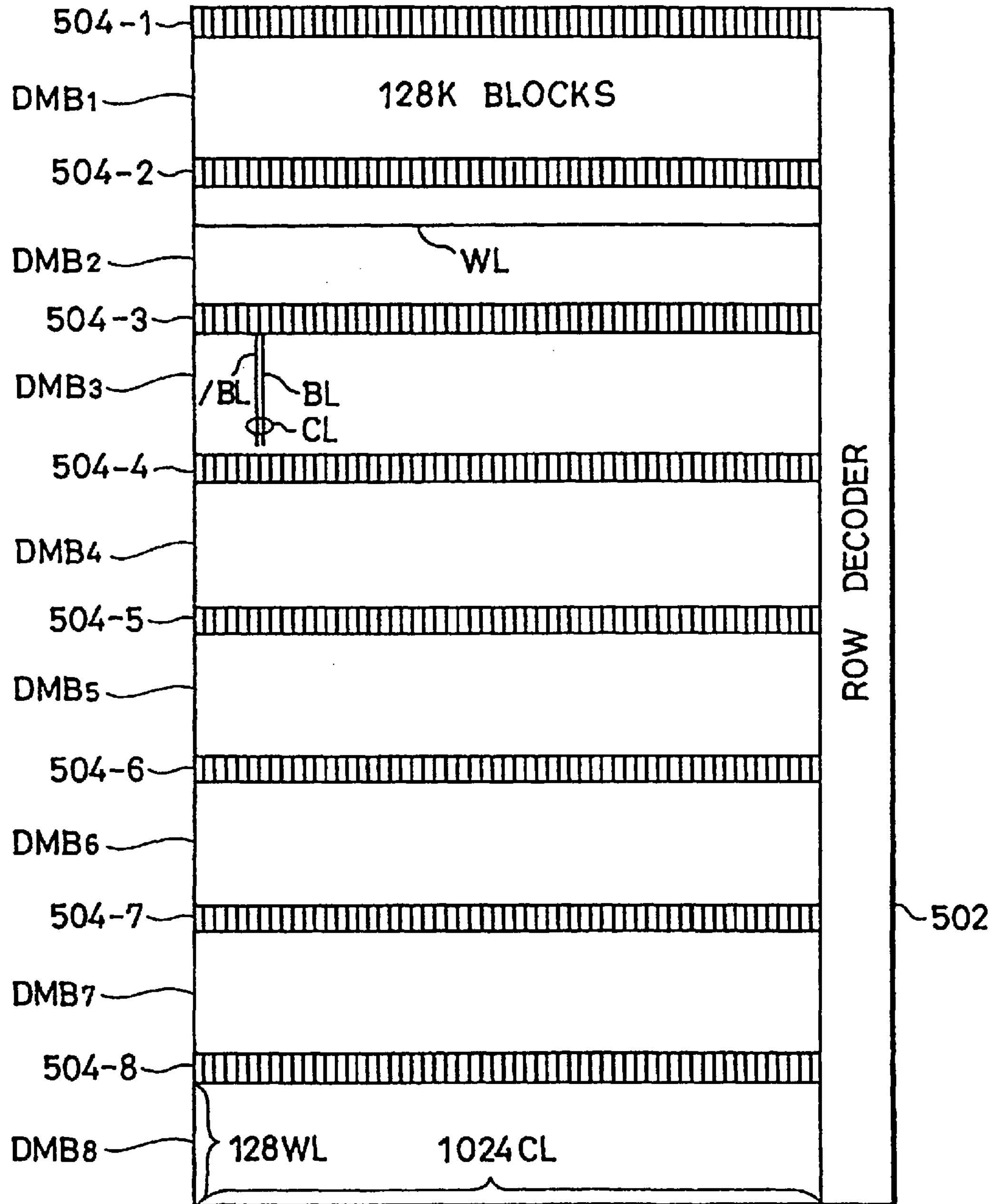
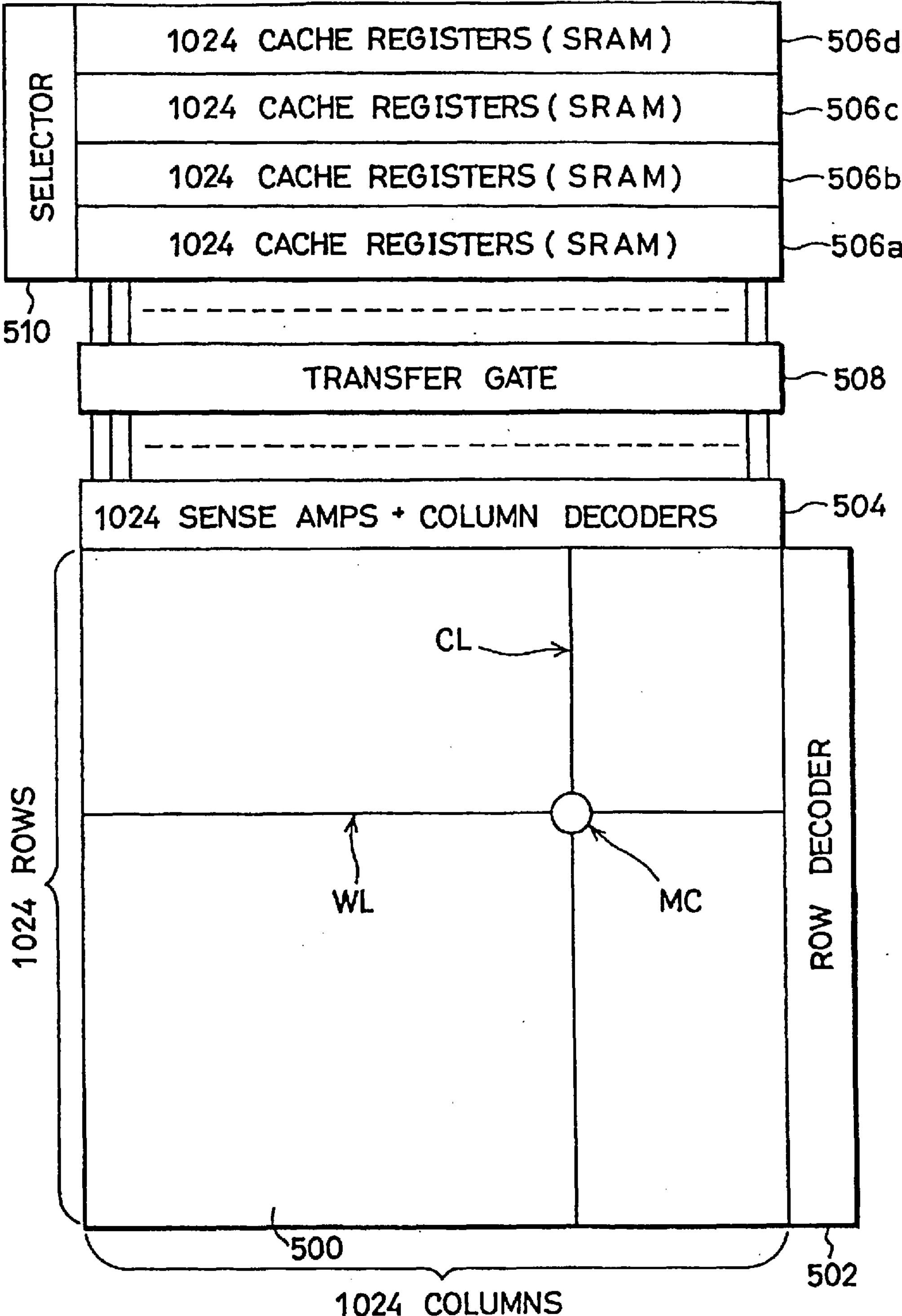
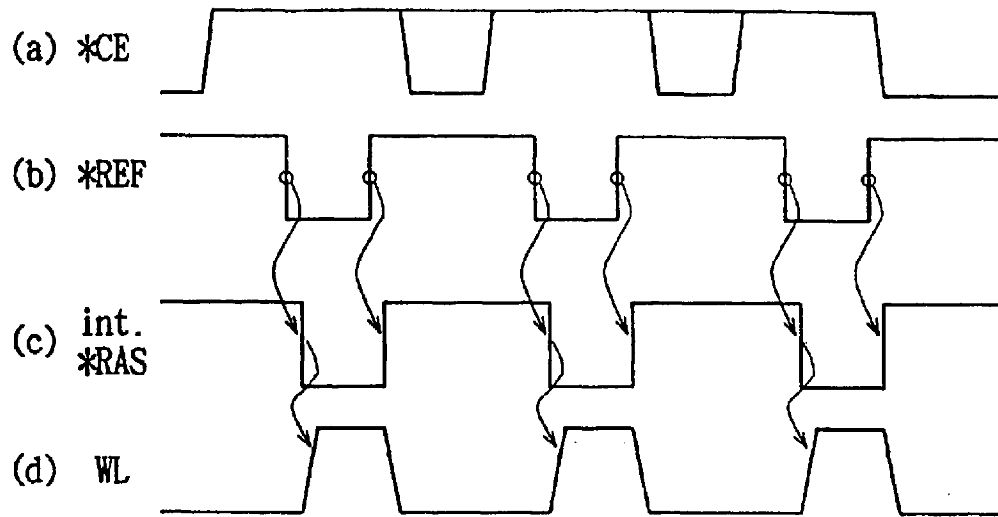


FIG. 4 PRIOR ART

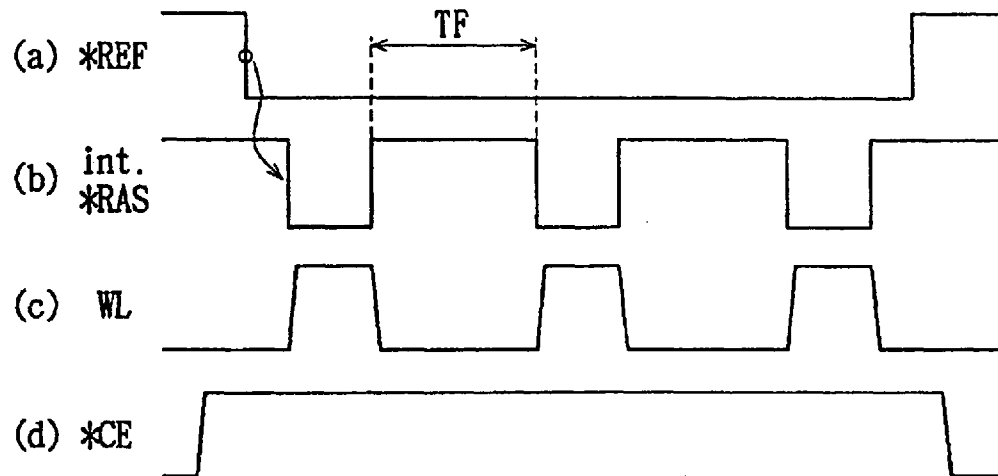


F I G. 5 PRIOR ART

AUTO REFRESH

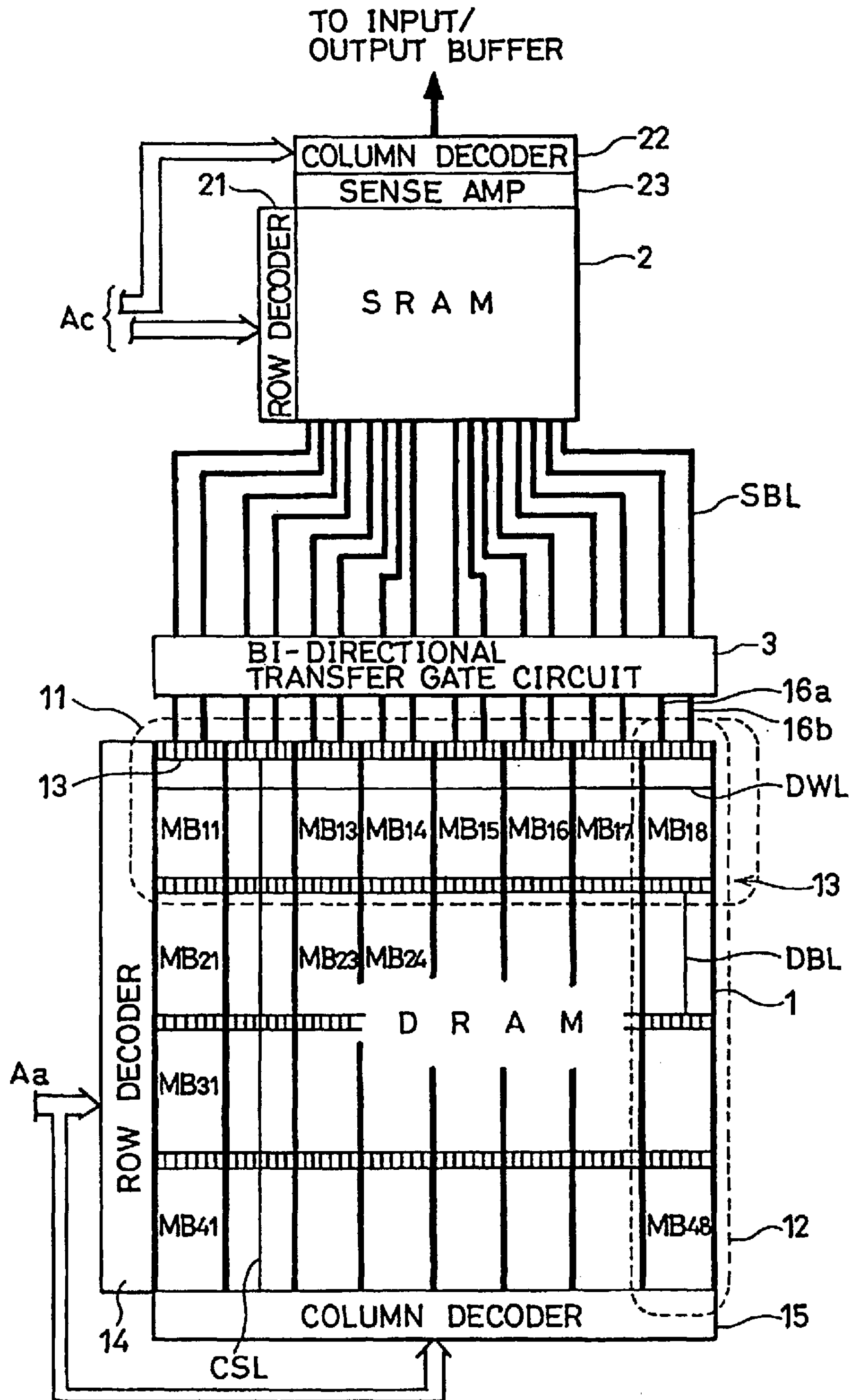


F I G. 6 PRIOR ART



SELF REFRESH

FIG. 7



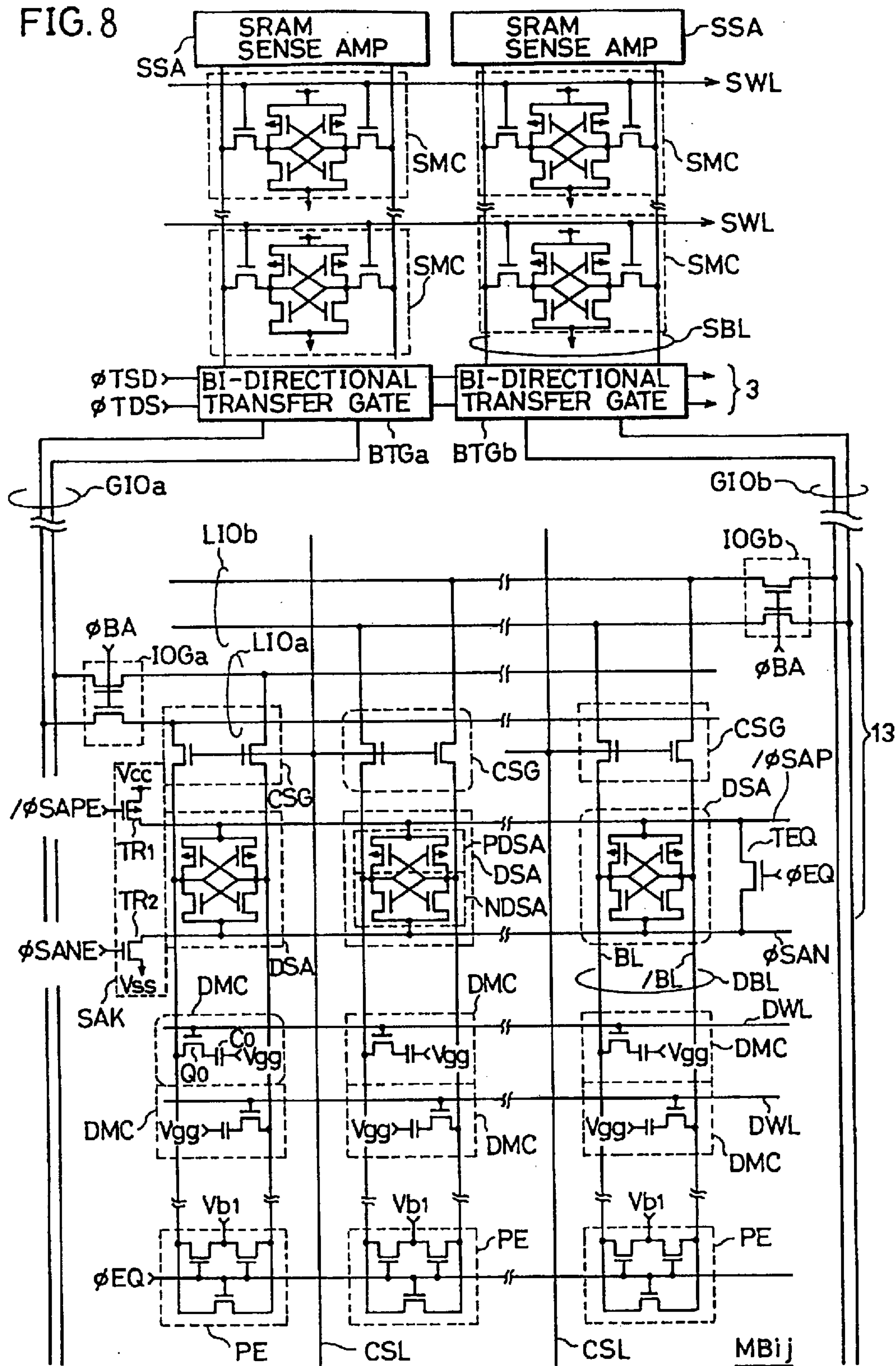


FIG. 8
SRAM SENSE AMP
SRAM SENSE AMP
SSA
SSA
SWL
SWL
SMC
SMC
SMC
SMC
SBL
φTSD
φTDS
BI-DIRECTIONAL TRANSFER GATE
BI-DIRECTIONAL TRANSFER GATE
3
BTGa
BTGb
GIOa
GIOb
LIOb
IOGb
φBA
IOGa
LIOa
φBA
CSG
CSG
CSG
/φSAP
DSA
Vcc
/φSAPE
TR1
TR2
φSANE
Vss
SAK
PDSA
DSA
NDSA
TEQ
φEQ
13
DSA
BL
/BL
DBL
φSAN
DMC
DMC
DWL
C0
Q0
Vgg
DMC
DMC
DMC
DWL
DMC
Vb1
PE
PE
φEQ
PE
CSL
CSL
MBij

F I G. 9

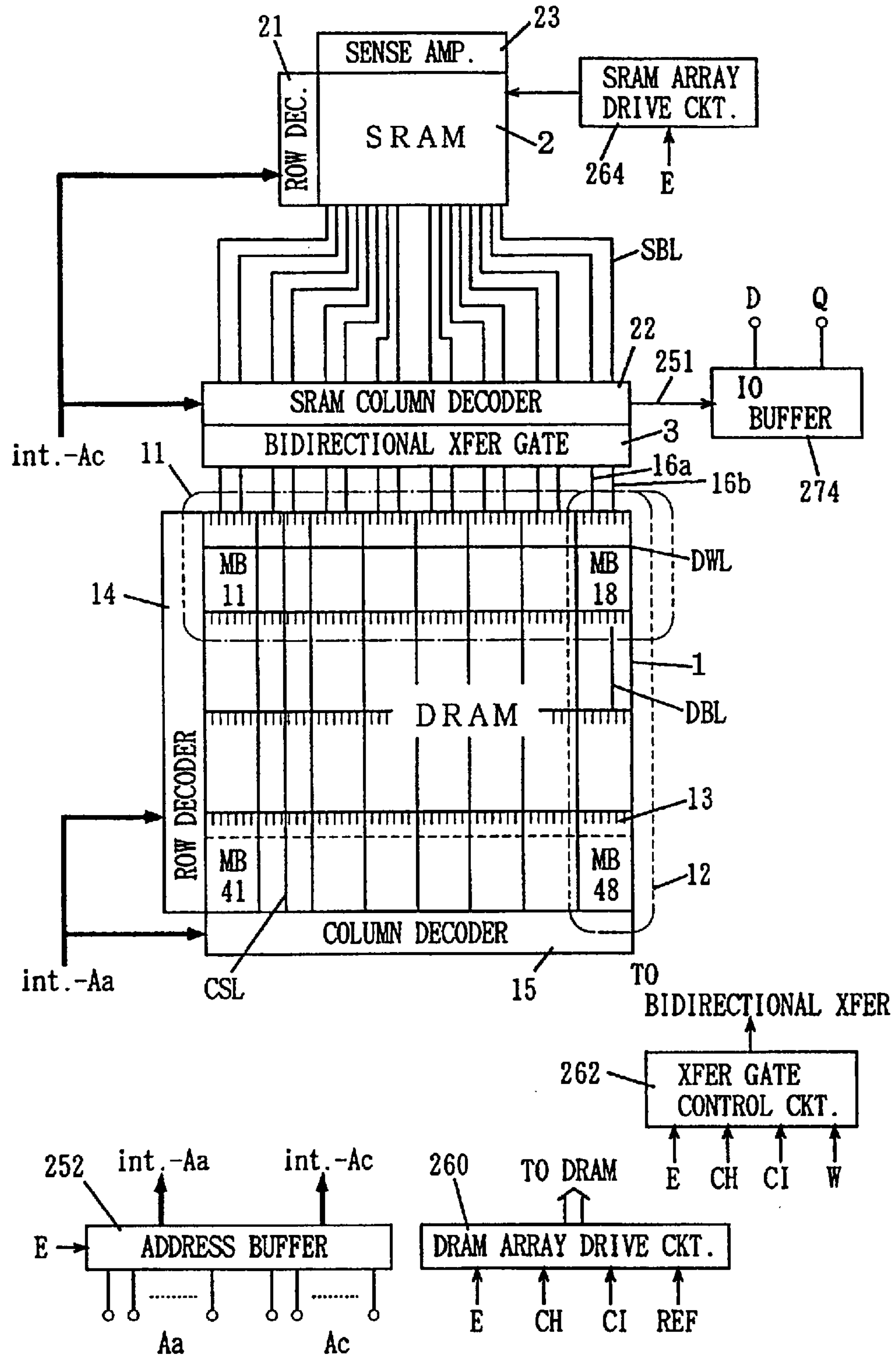


FIG.10

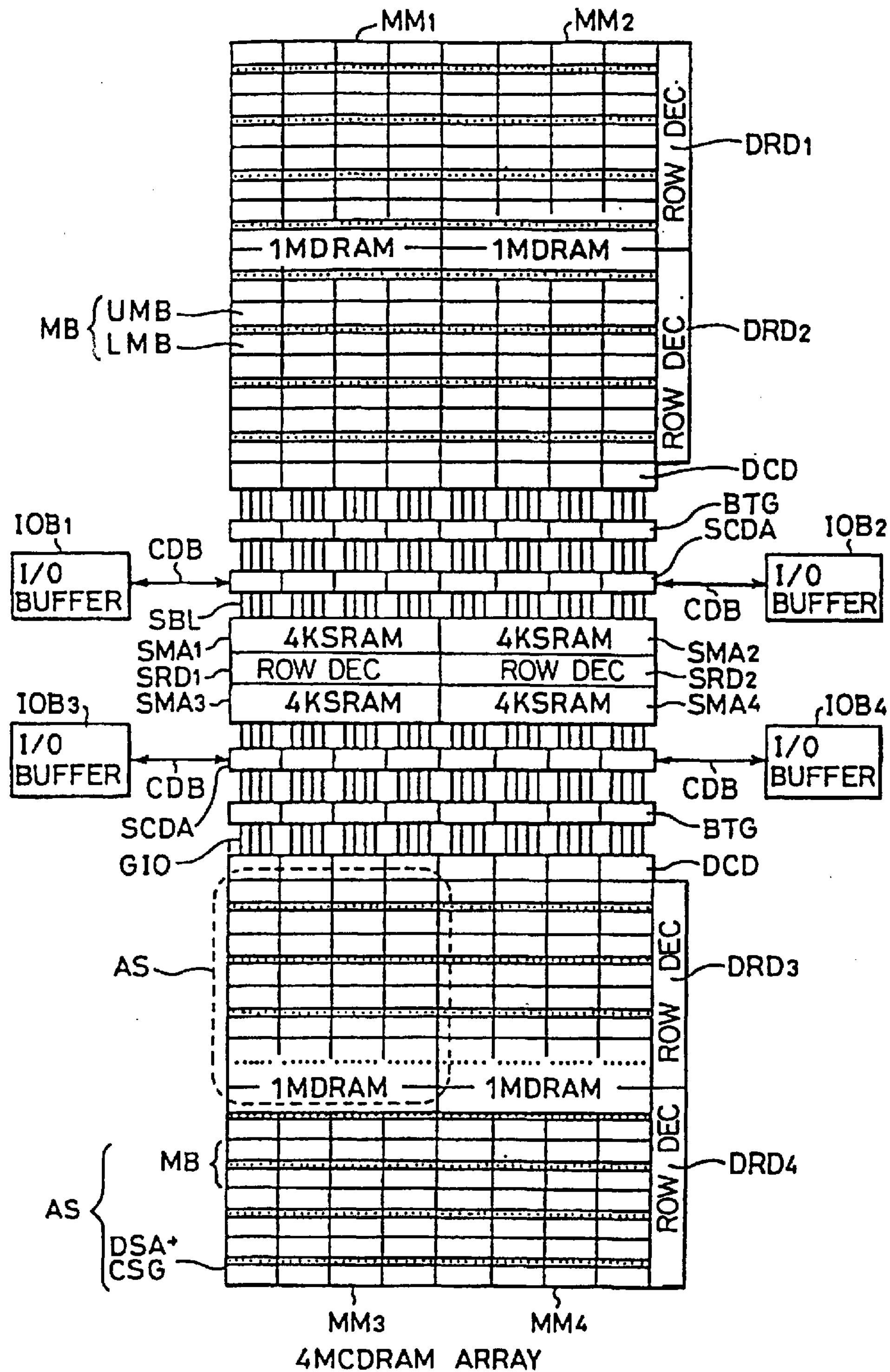


FIG.11

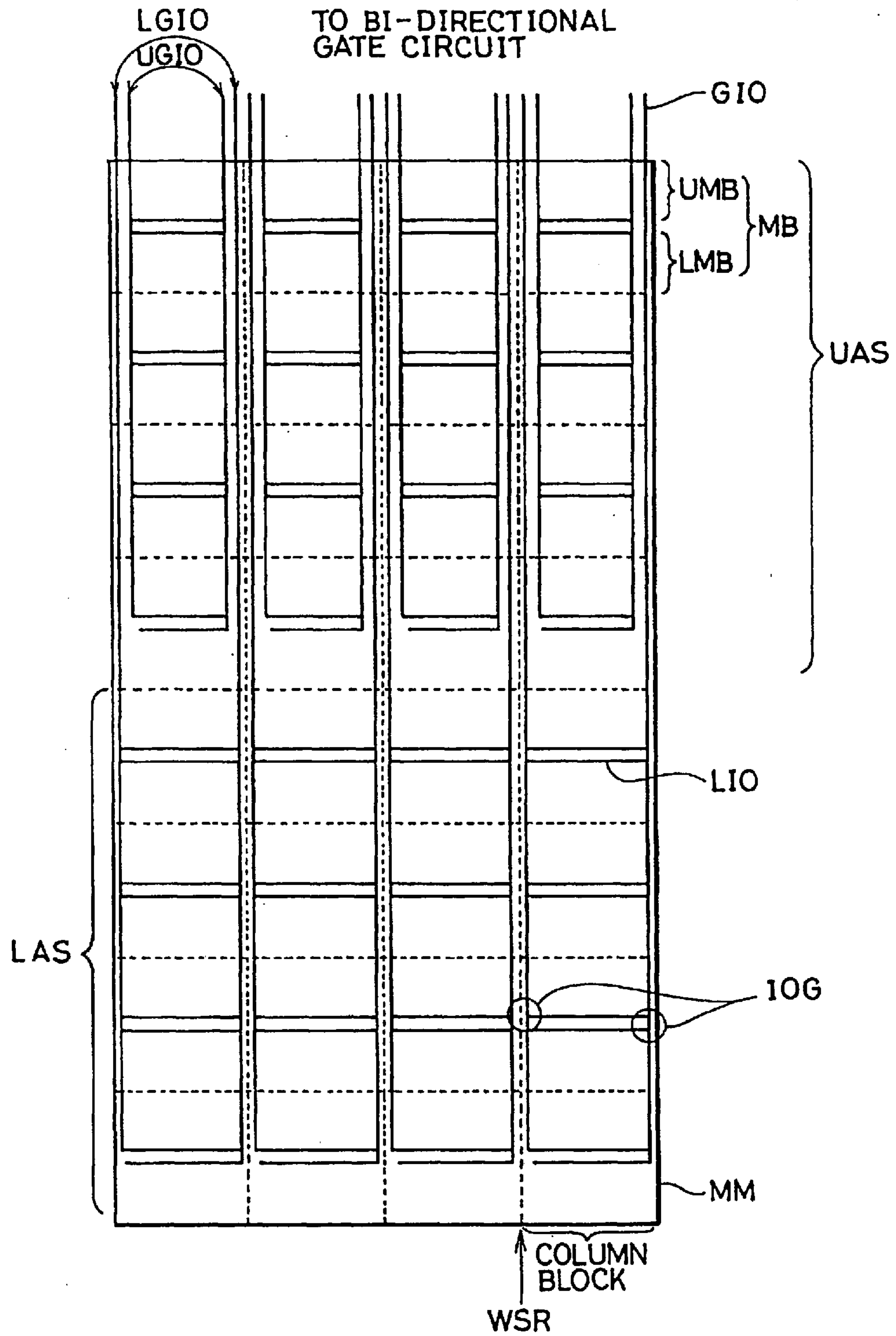


FIG.12

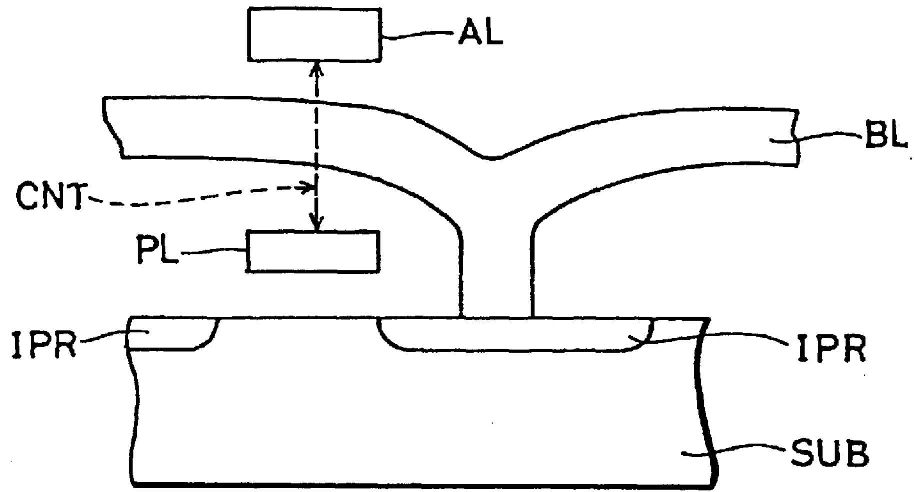


FIG.13

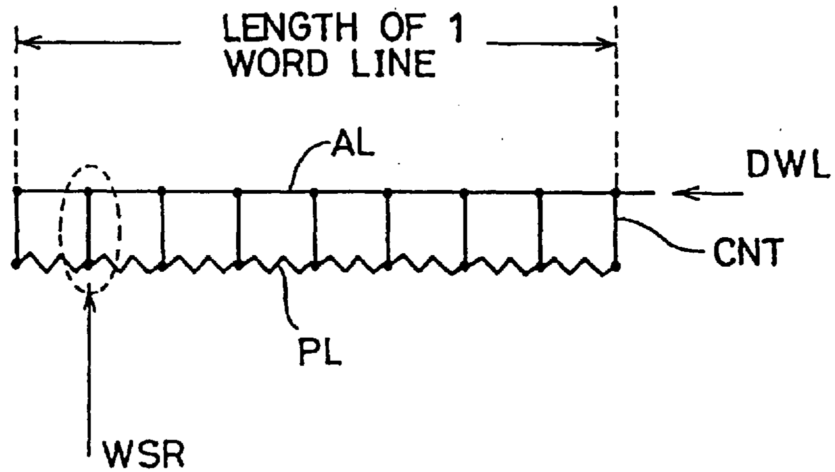


FIG.14

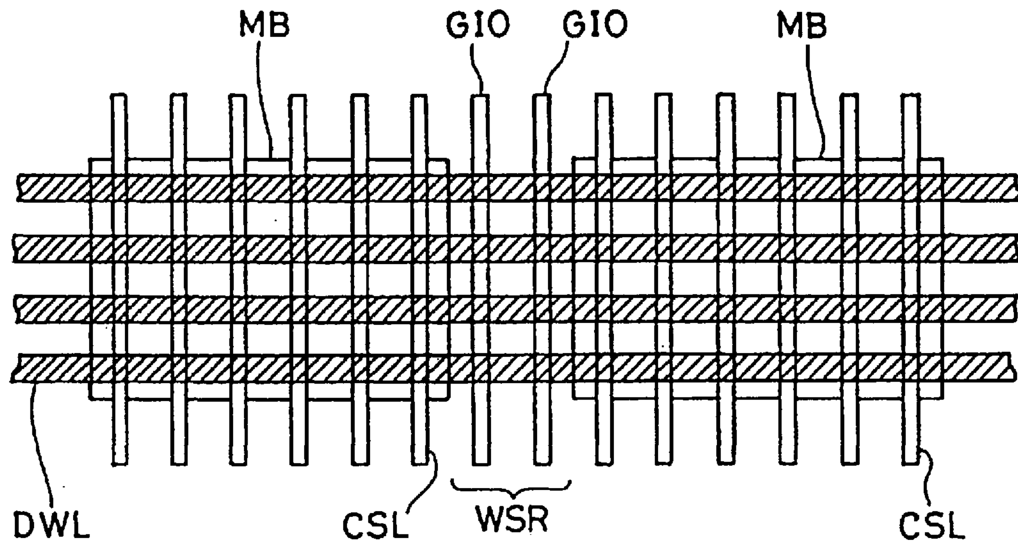


FIG.15

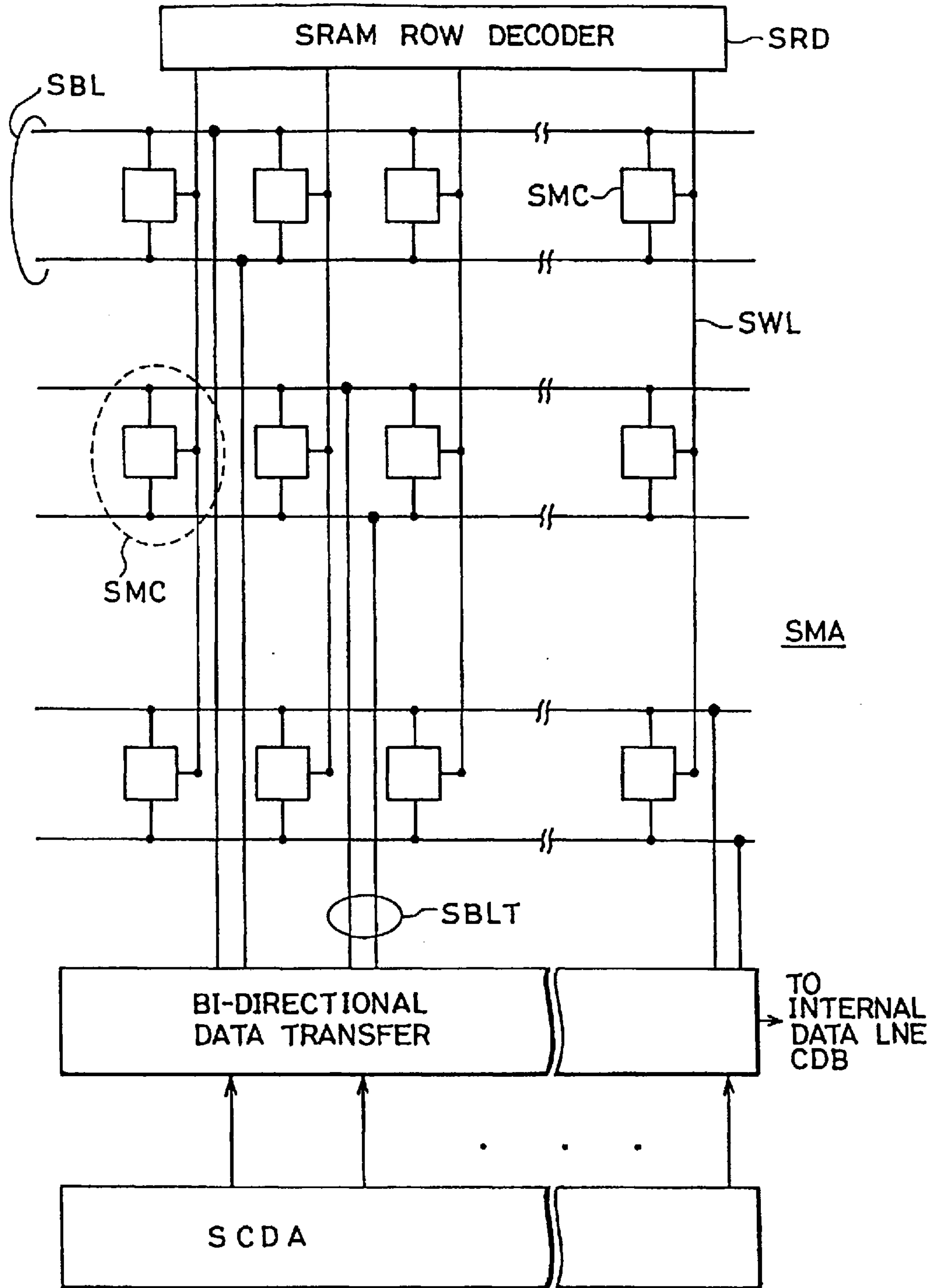
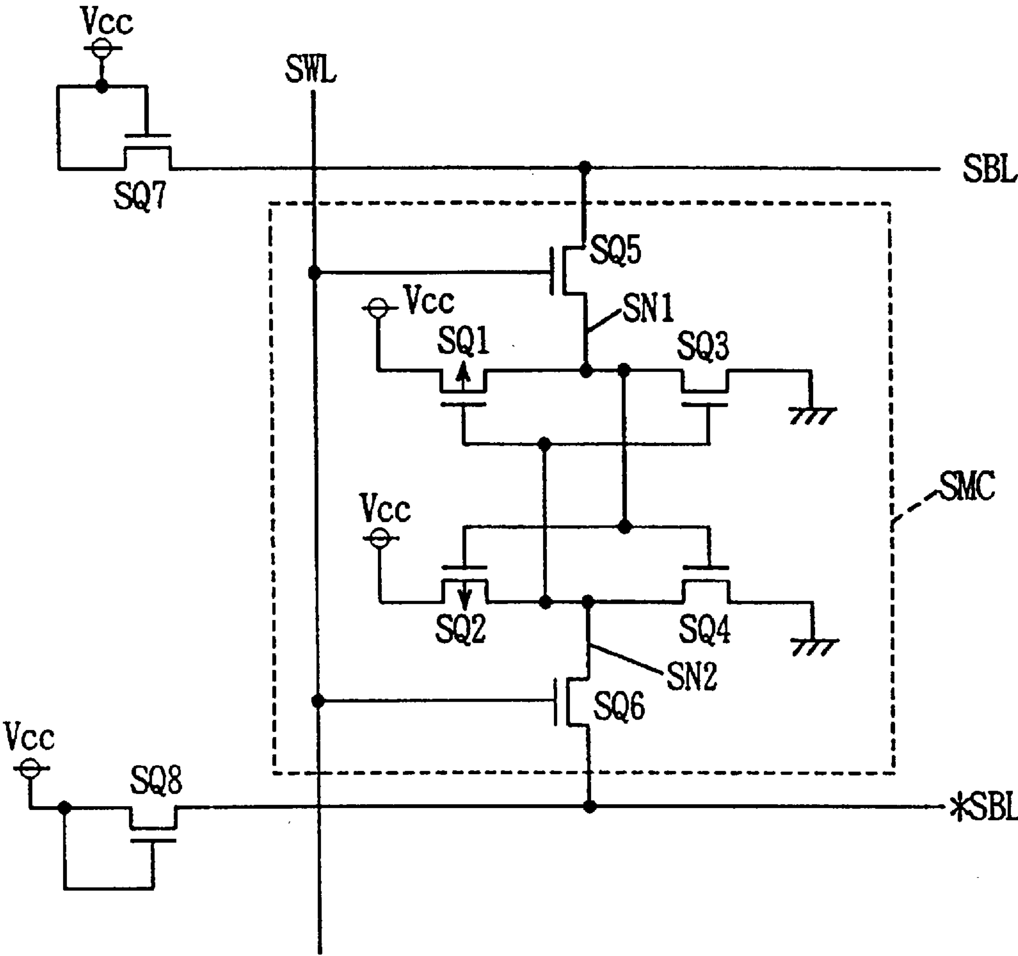


FIG. 16 PRIOR ART



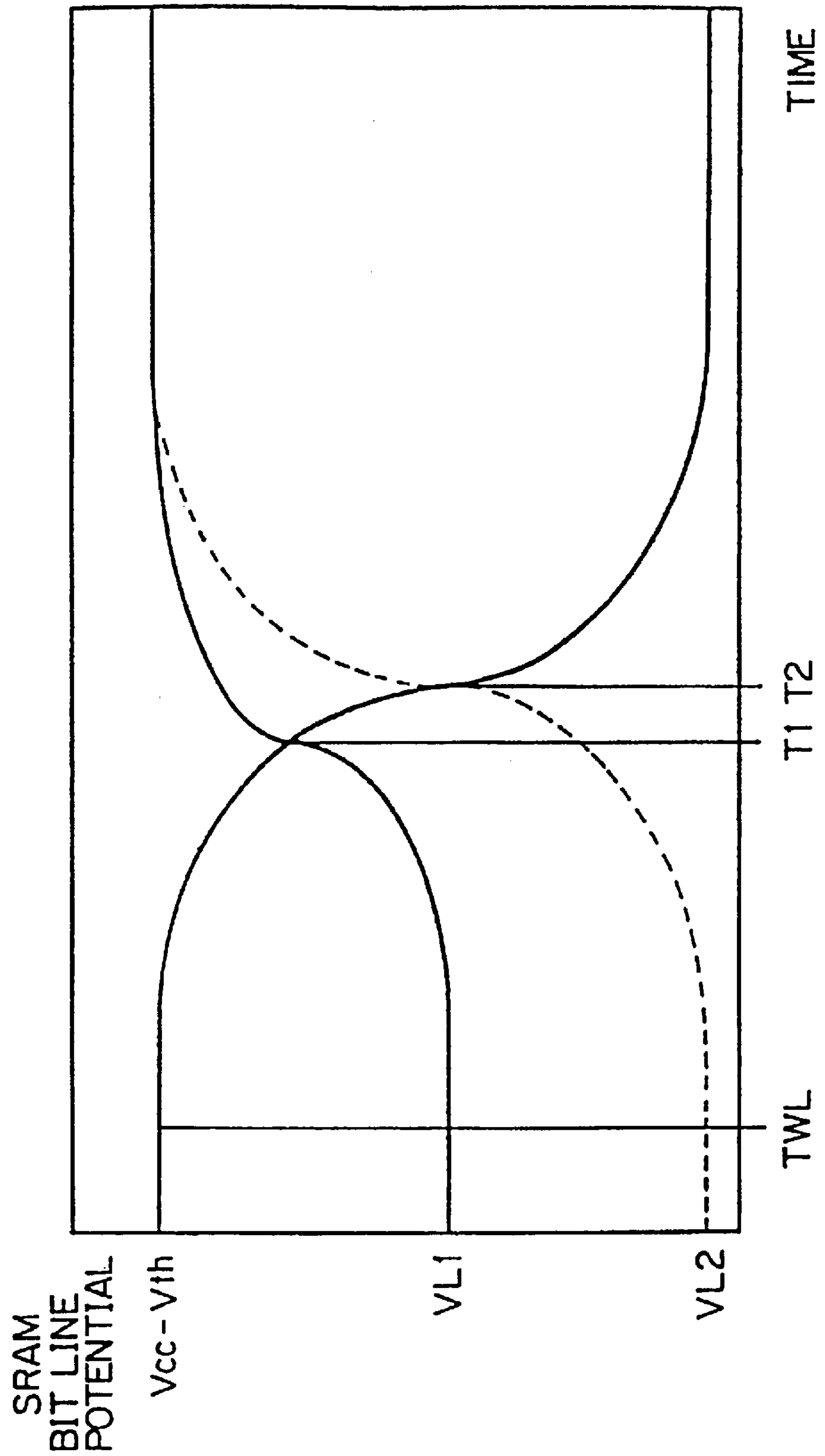


FIG.17 PRIOR ART

FIG. 18

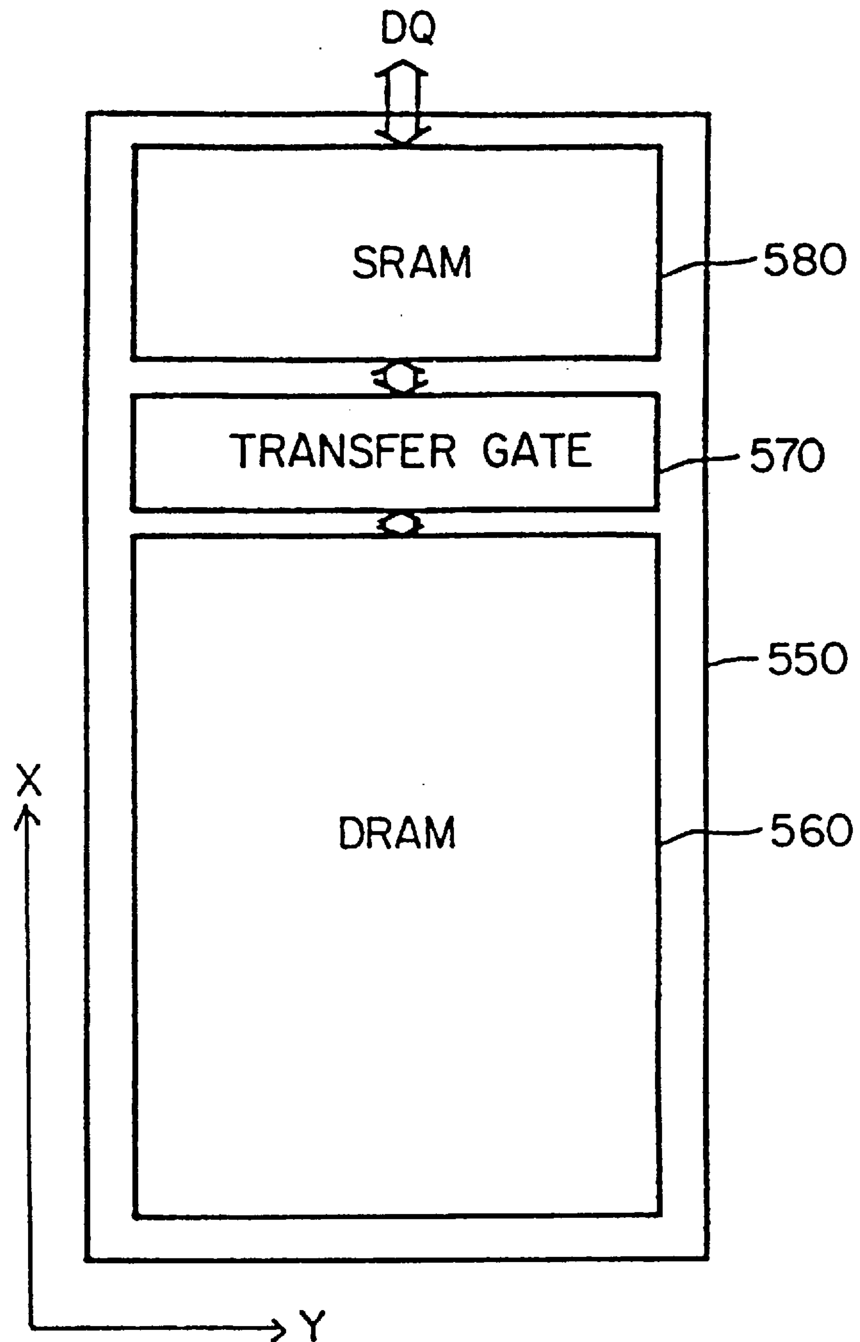
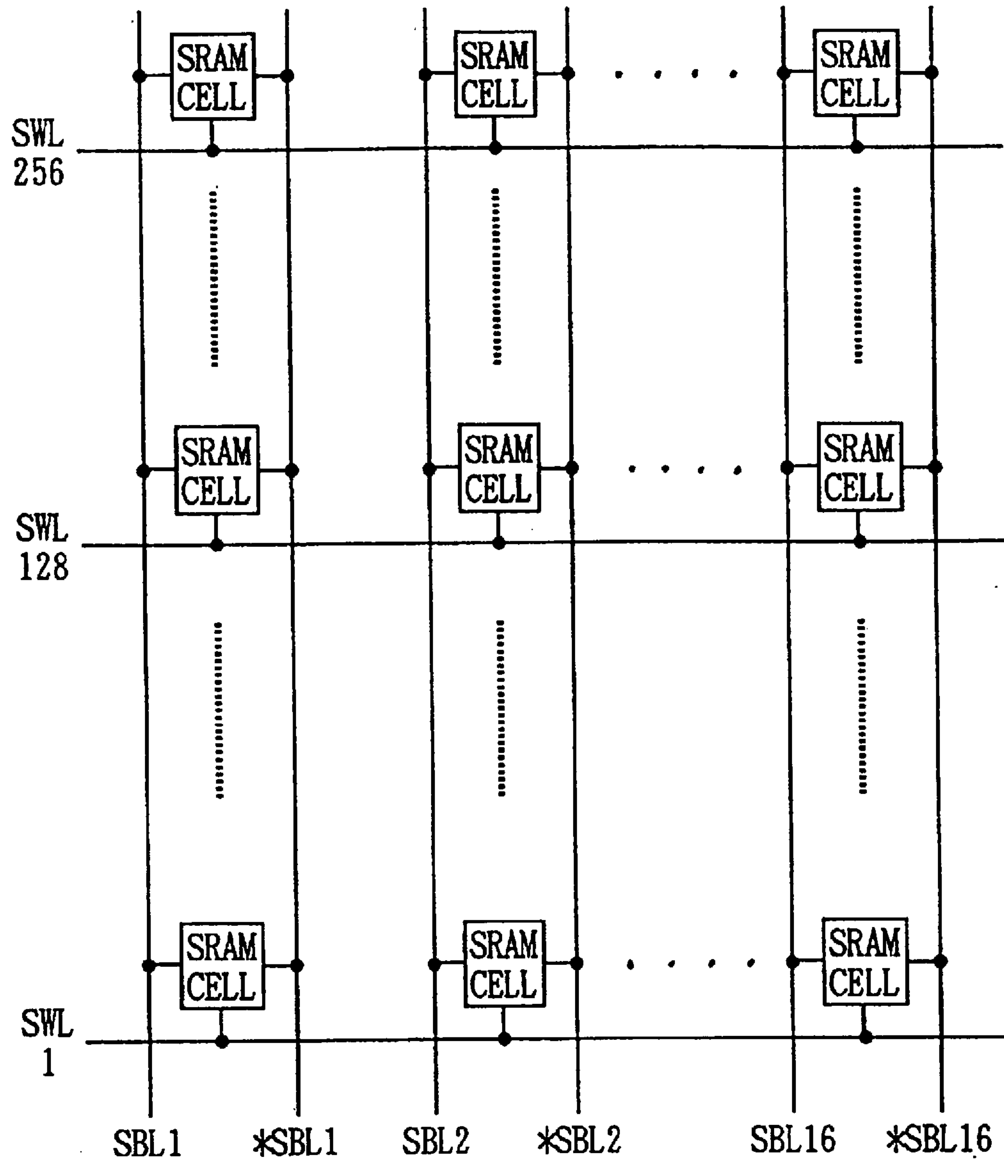


FIG. 19



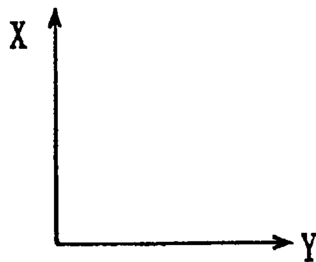


FIG. 20

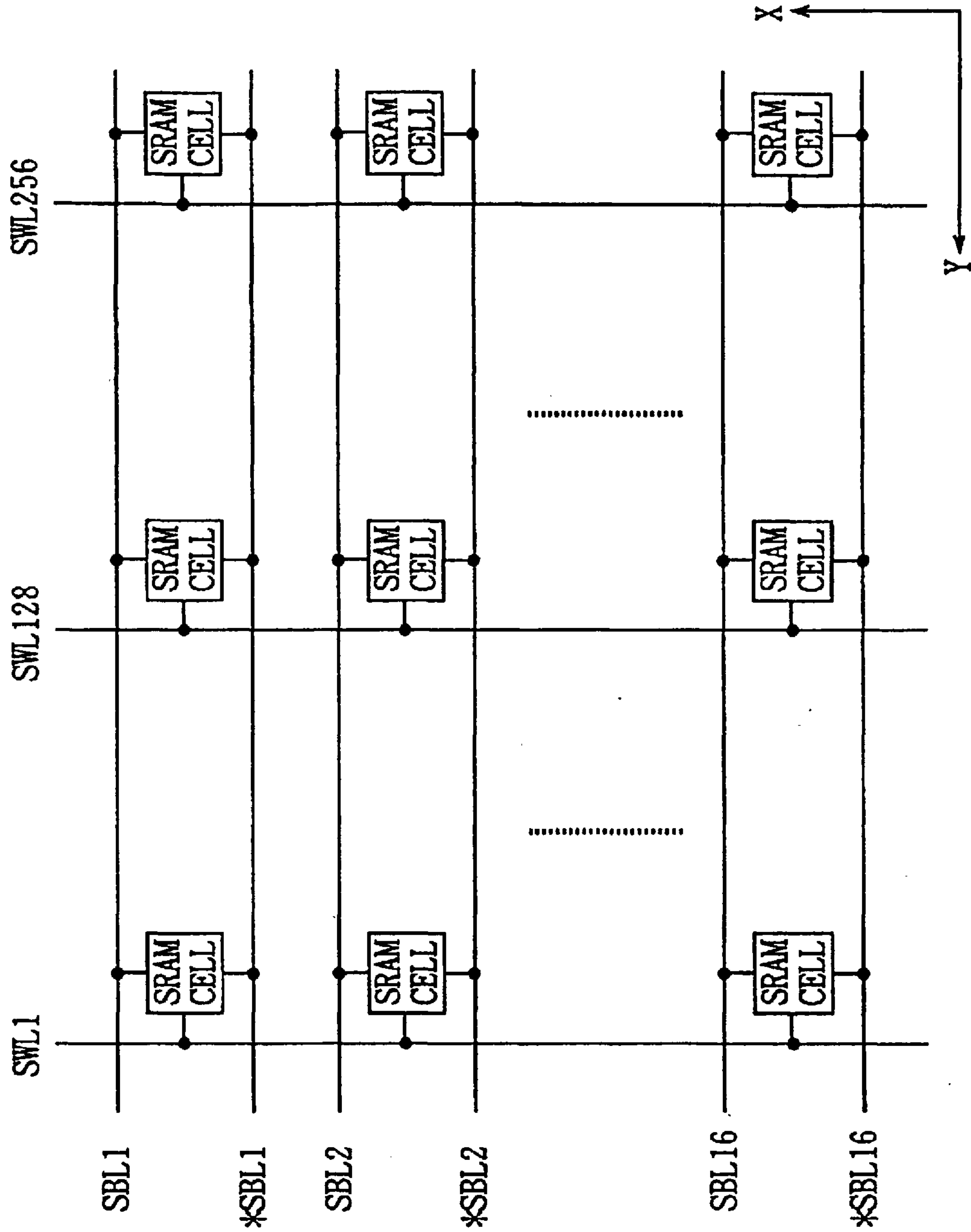
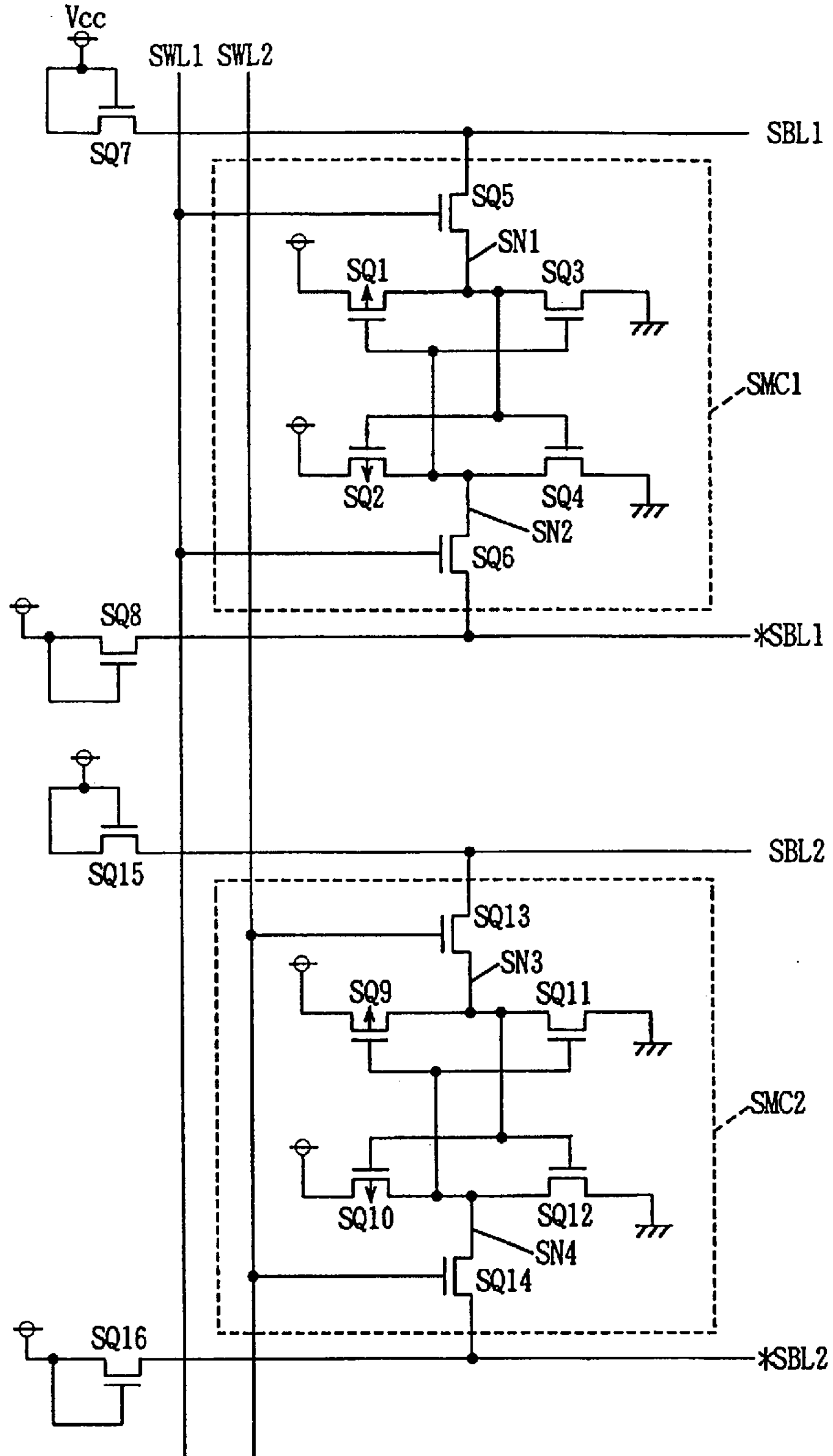
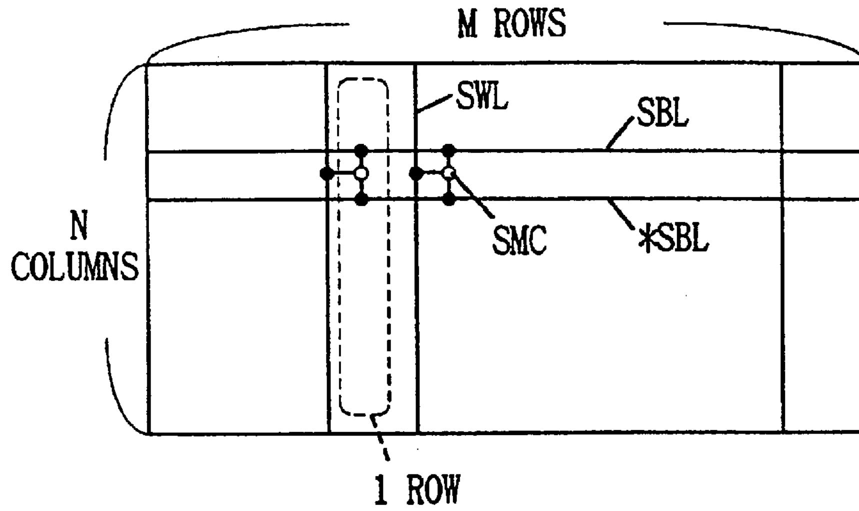


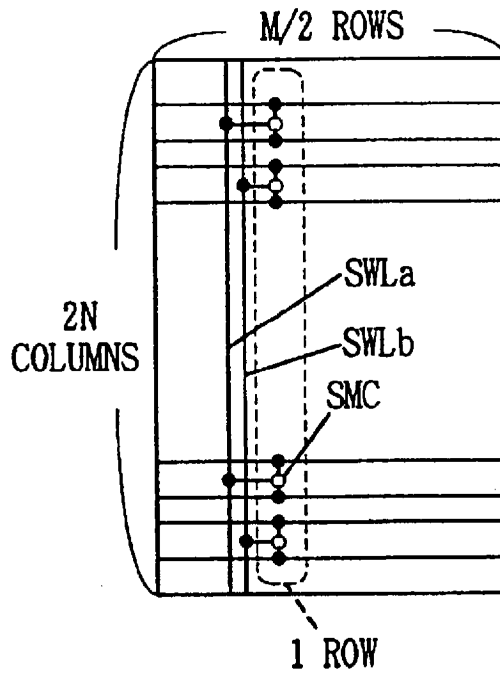
FIG. 21



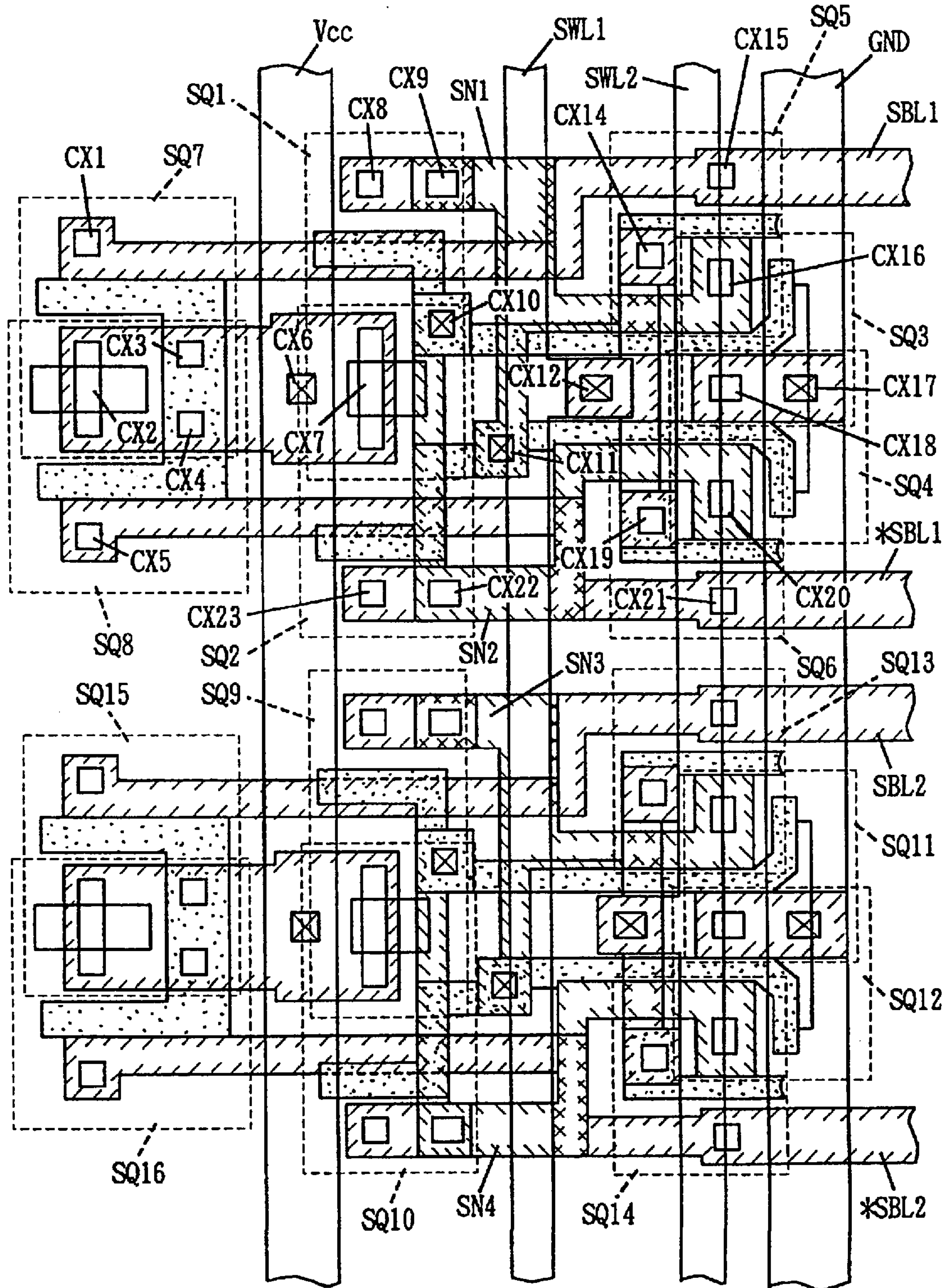
F I G. 2 2 A



F I G. 2 2 B



F I G. 2 3



F I G. 2 4

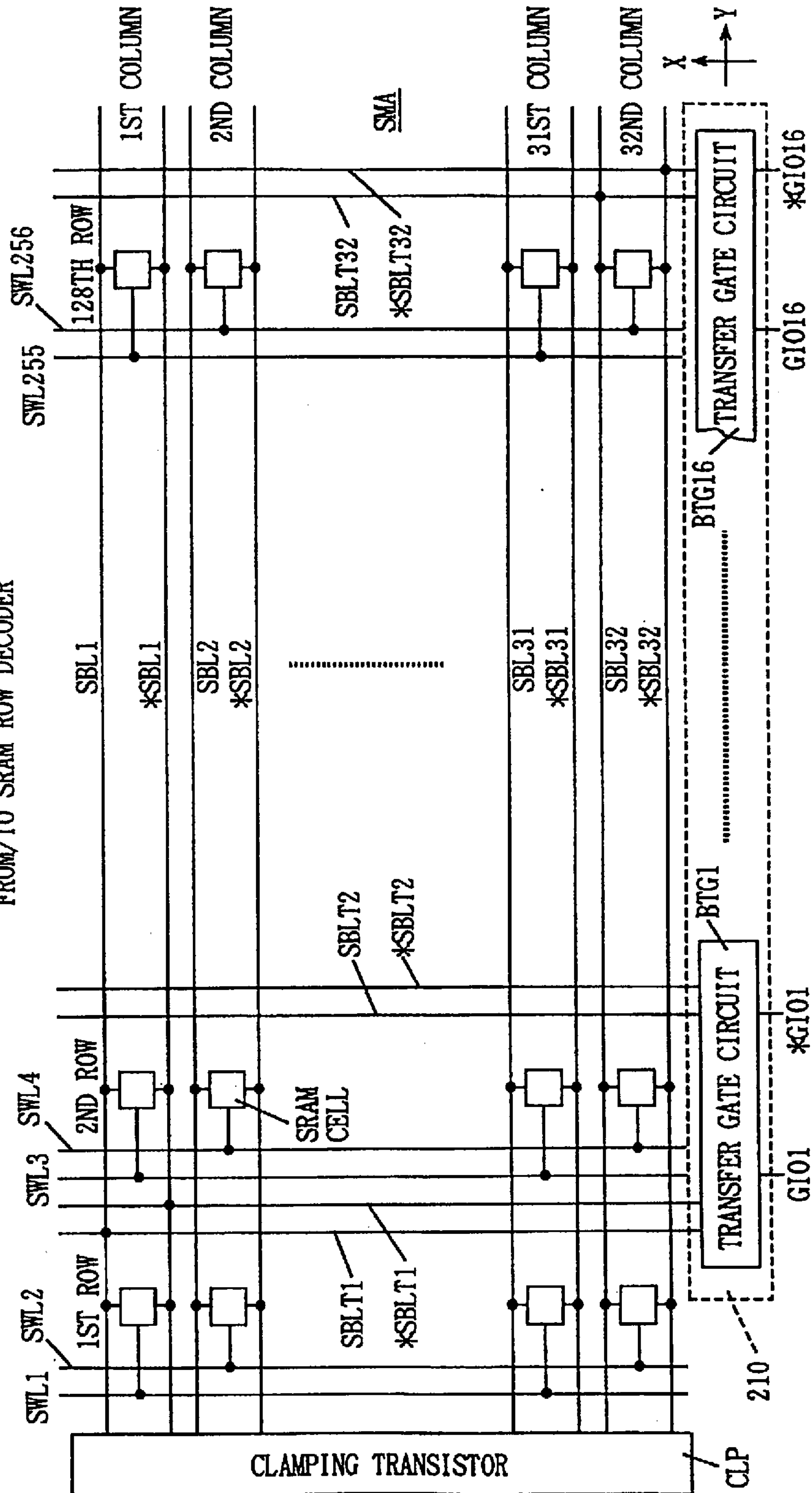


FIG. 25

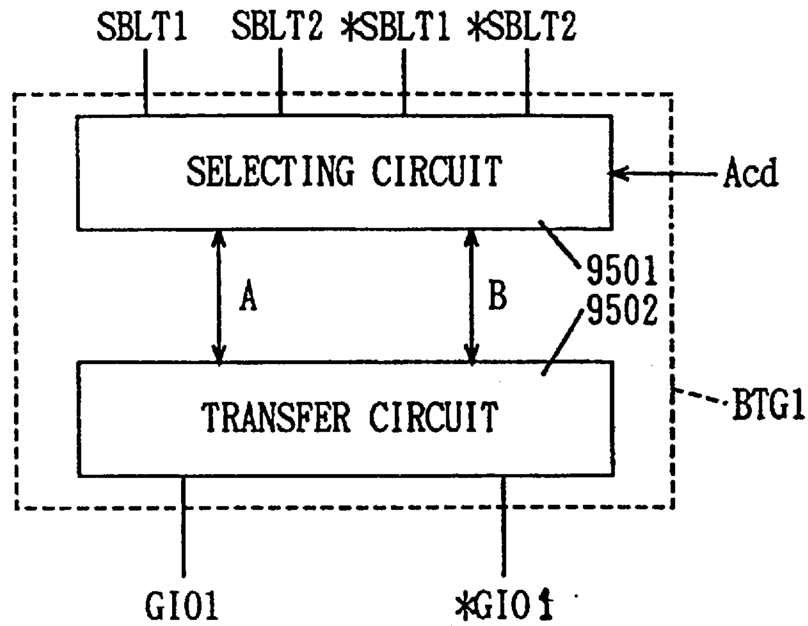
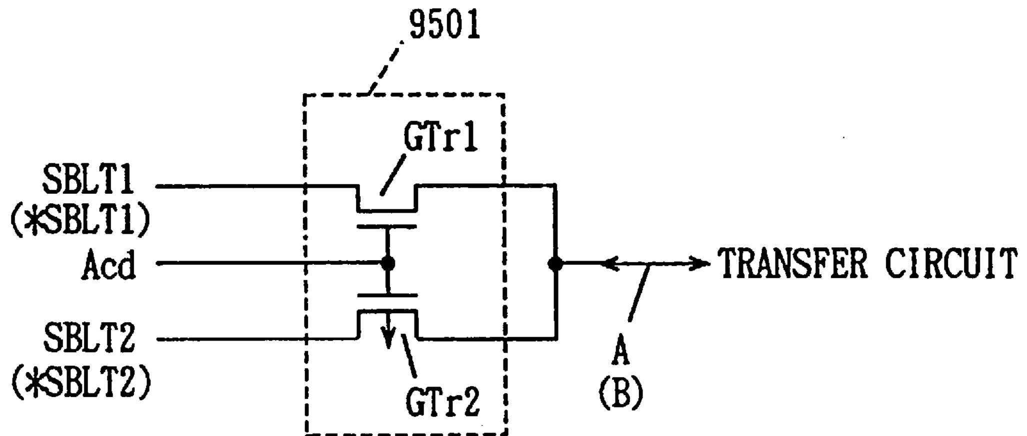


FIG. 26



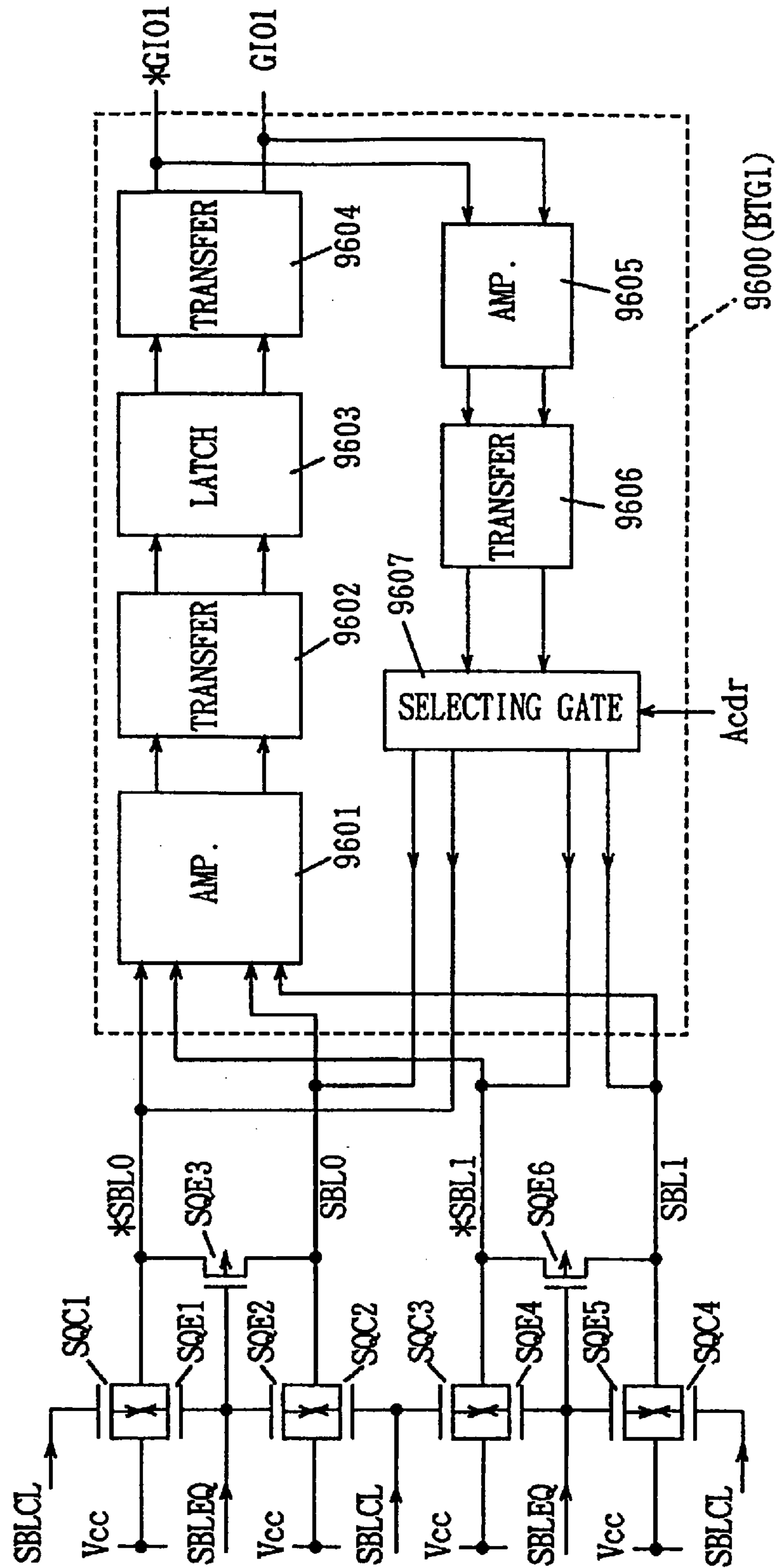
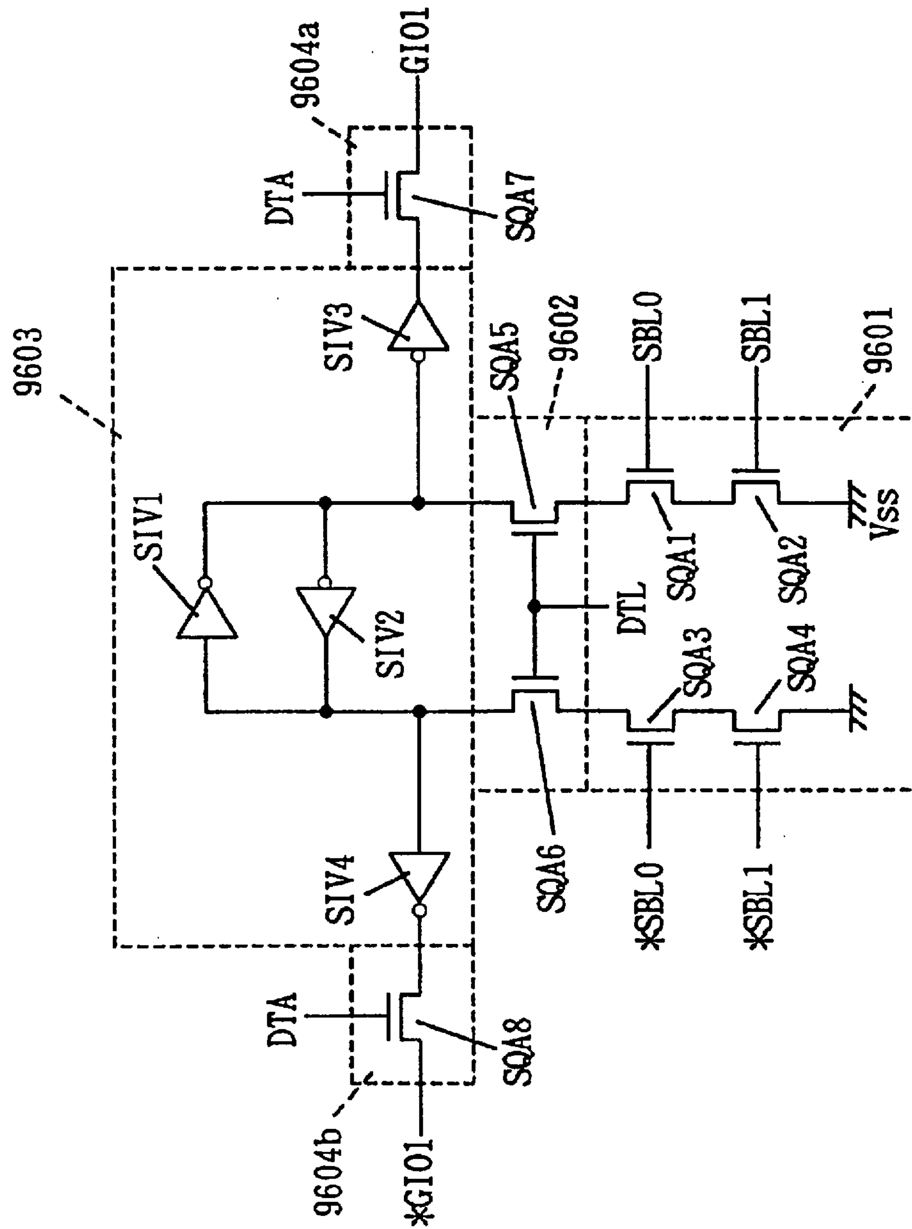
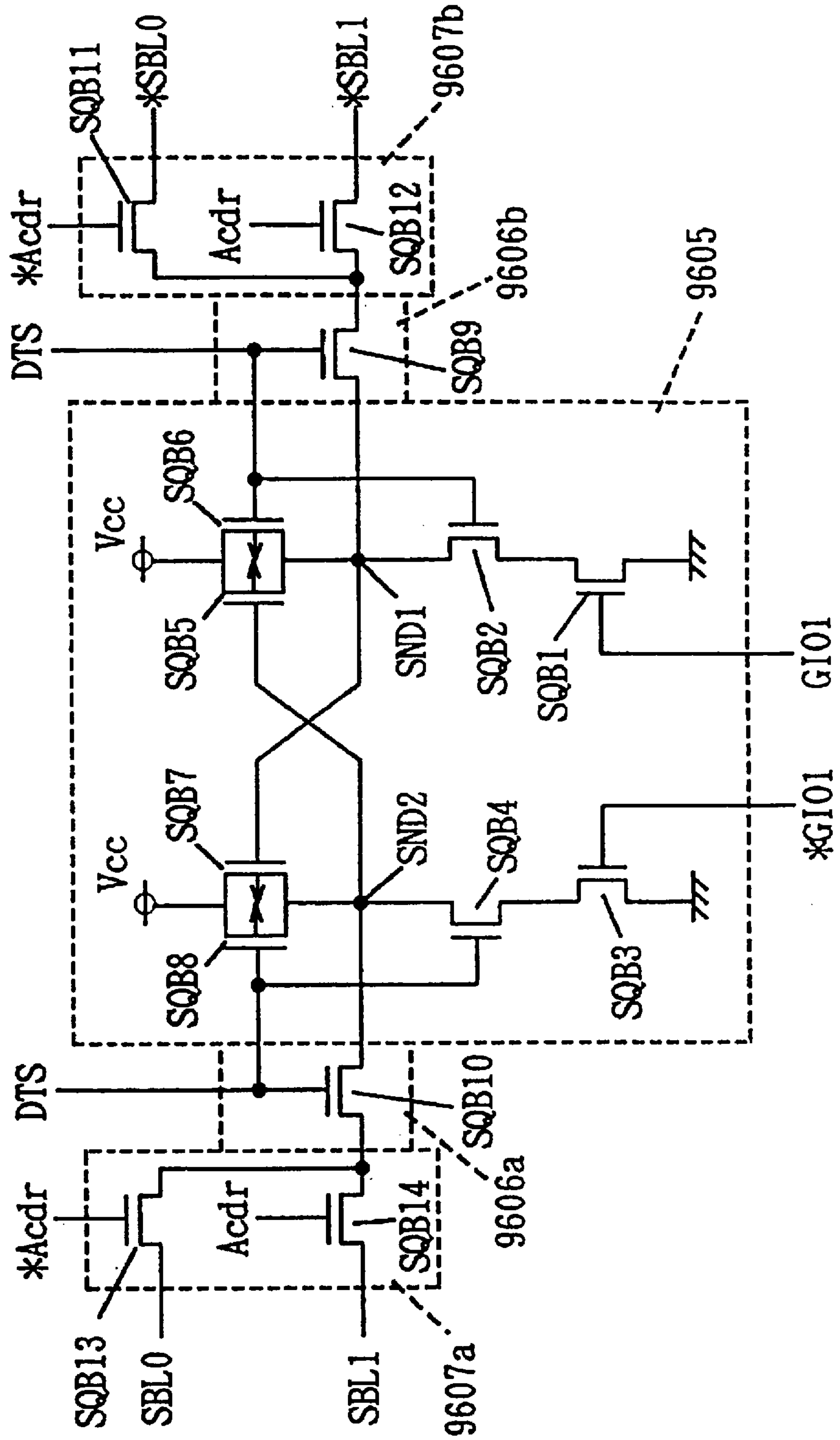


FIG. 27



F I G. 28



F I G. 29
*Acdr
SQB11
*SBL0
*SBL1
9607b
Acdr
SQB12
9606b
9605
DTS
SQB9
Vcc
SQB6
SQB5
SND1
SQB2
SQB1
GIO1
SQB7
SQB8
SND2
SQB4
SQB3
*GIO1
DTS
SQB10
9606a
*Acdr
Acdr
SQB14
SQB13
SBL0
SBL1
9607a

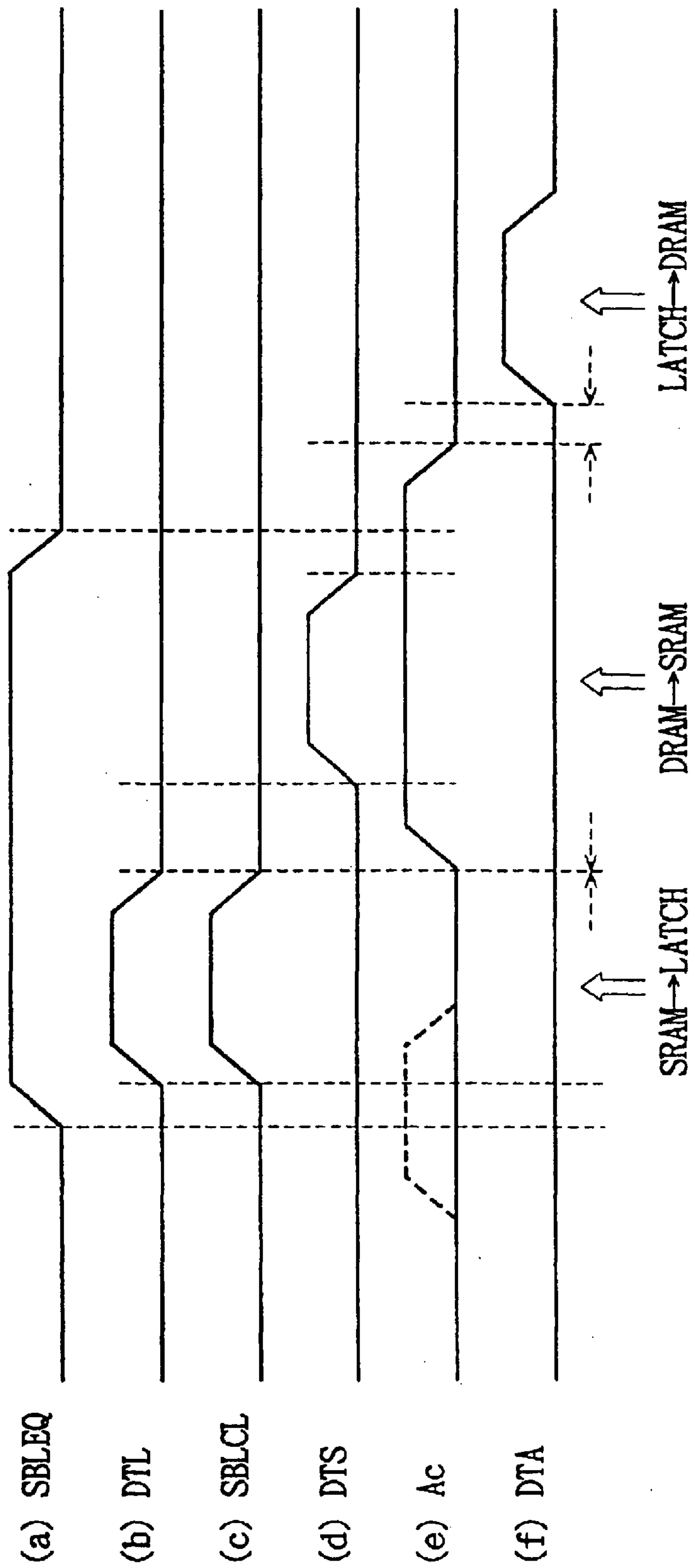


FIG. 30

FIG. 31

MASKED WRITE	D/Q SEPARATION	Pin		Pin	D/Q SEPARATION	MASKED WRITE
	FOR DRAM−Vcc	1		44	REF#(REFRESH)	
	Aa0/Ar0	2		43	Aa9	
	Aa1/Ar1	3		42	Aa8	
	CI#(CACHE INHIBITION)	4		41	K(CLOCK)	
	W#(WRITE ENABLE)	5		40	G#(OUTPUT ENABLE)	
	Ac0	6		39	Ac11	
	Ac1	7		38	Ac10	
	Ac2	8		37	Ac9	
M0	D0	9		36	D3	M3
DQ0	Q0	10	300 mil	35	Q3	DQ3
	FOR SRAM Vcc	11	TSOP	34	Gnd FOR SRAM	
	FOR SRAM Gnd	12	Type 11	33	Vcc FOR SRAM	
DQ1	Q1	13	(18.4mm)	32	Q2	DQ2
M1	D1	14		31	D2	M2
	Ac3	15		30	Ac8	
	Ac4	16		29	Ac7	
	Ac5	17		28	Ac6	
	E#(CHIP SELECT)	18		27	CH#(CACHE HIT)	
	Aa2	19		26	Aa7	
	Aa3	20		25	Aa6	
	Aa4	21		24	Aa5	
	Gnd (FOR DRAM)	22		23	CR#(COMMAND REGISTER)	

FIG. 32

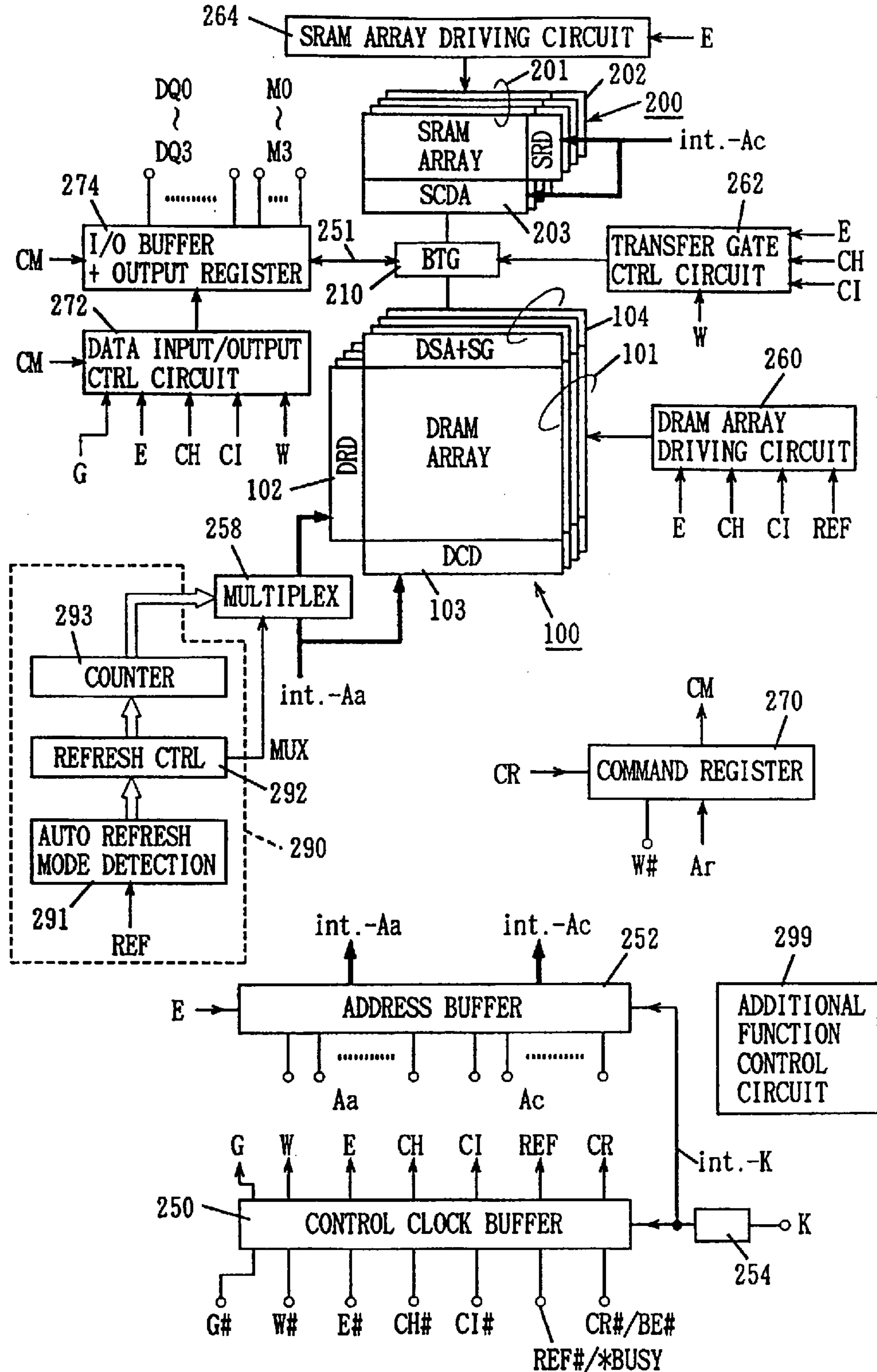


FIG. 33

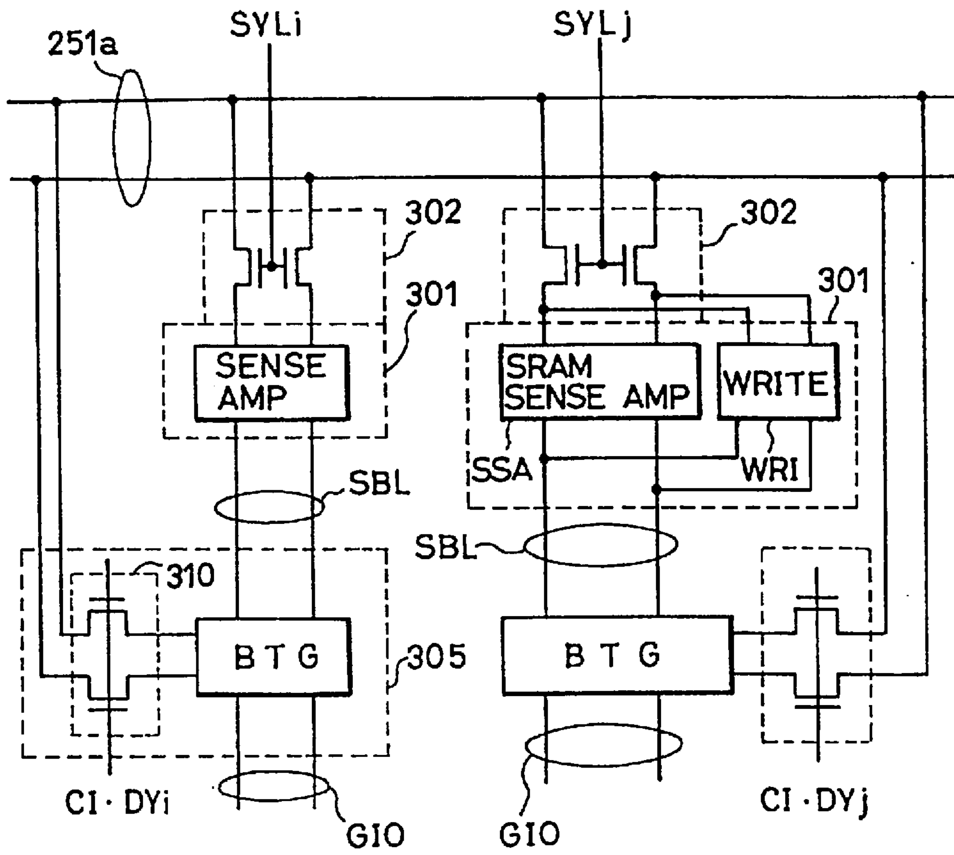


FIG. 34

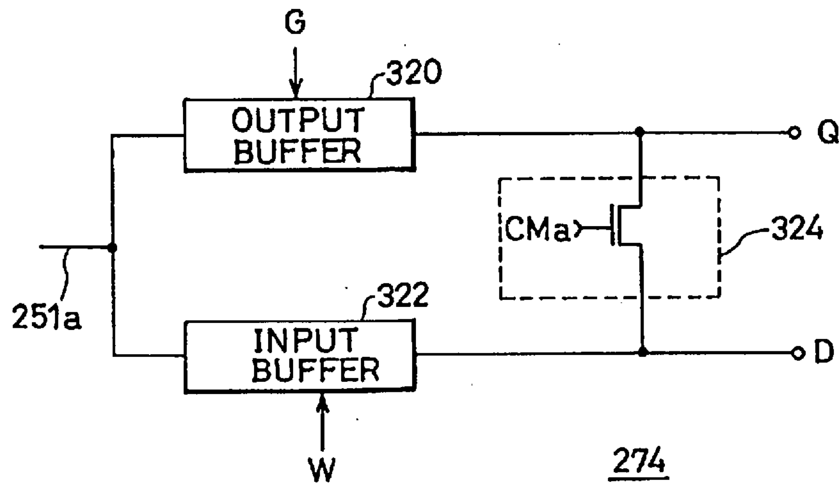


FIG. 35

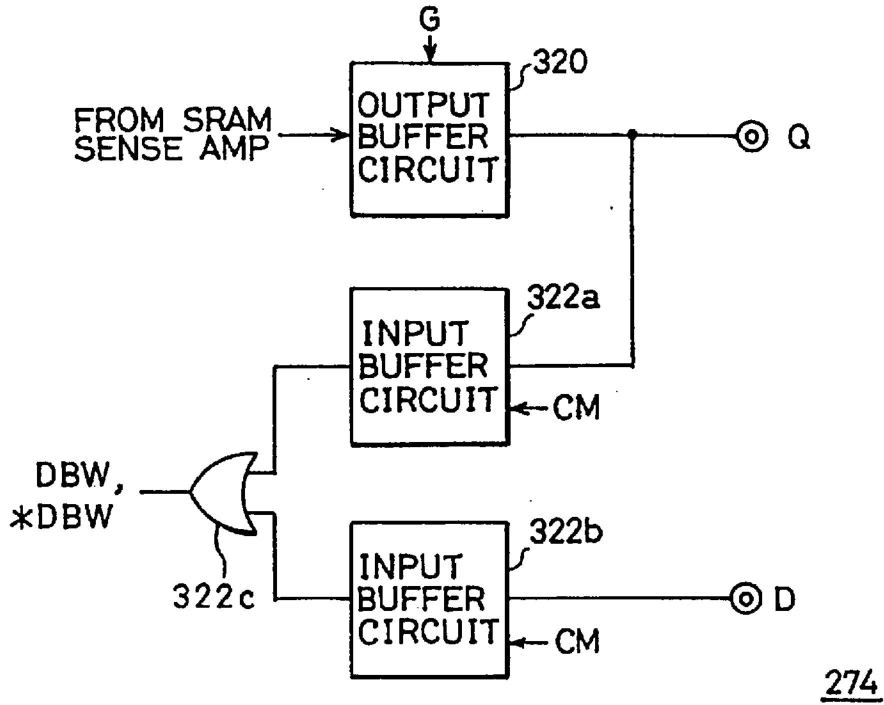
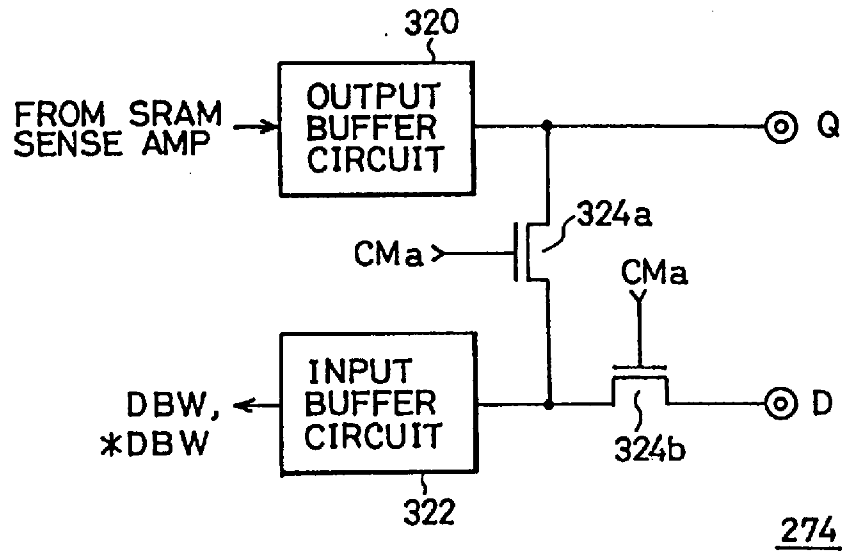


FIG. 36



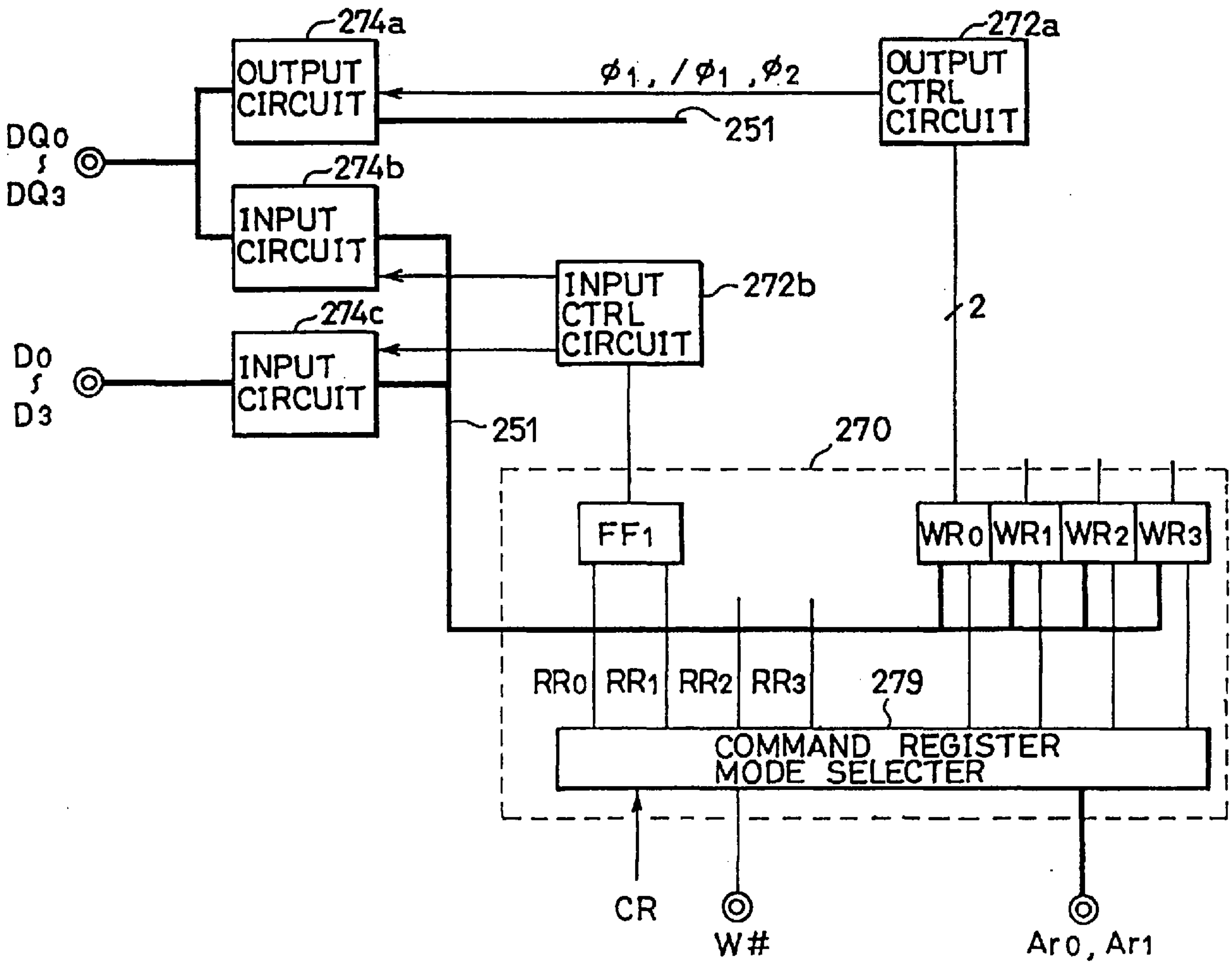


FIG. 37
274a
OUTPUT CIRCUIT
φ1, /φ1, φ2
251
272a
OUTPUT CTRL CIRCUIT
DQ0 ~ DQ3
274b
INPUT CIRCUIT
INPUT CTRL CIRCUIT
272b
2
274c
D0 ~ D3
INPUT CIRCUIT
251
270
FF1
WR0
WR1
WR2
WR3
RR0
RR1
RR2
RR3
279
COMMAND REGISTER MODE SELECTER
CR
W#
Ar0, Ar1

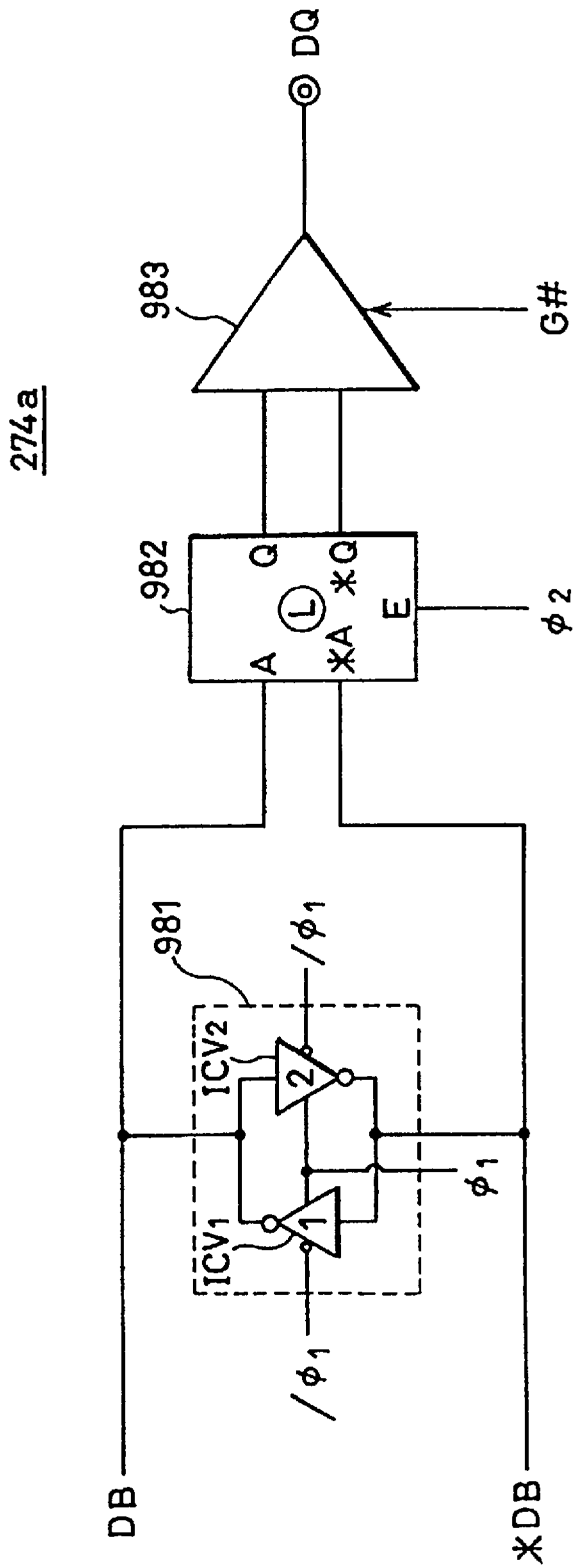


FIG. 38

FIG. 39

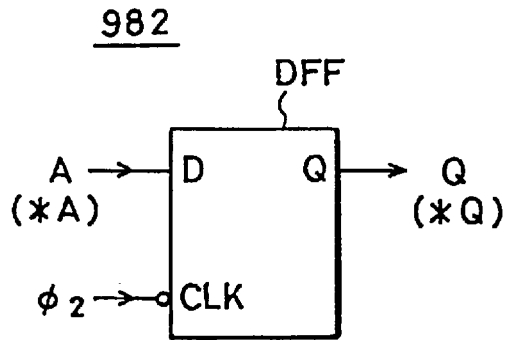


FIG. 40

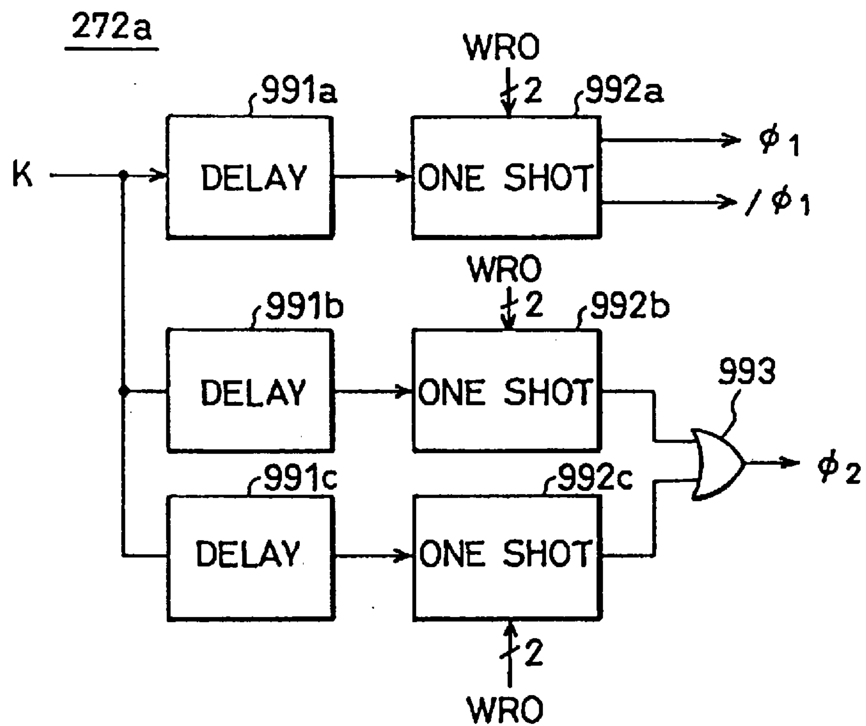


FIG. 41

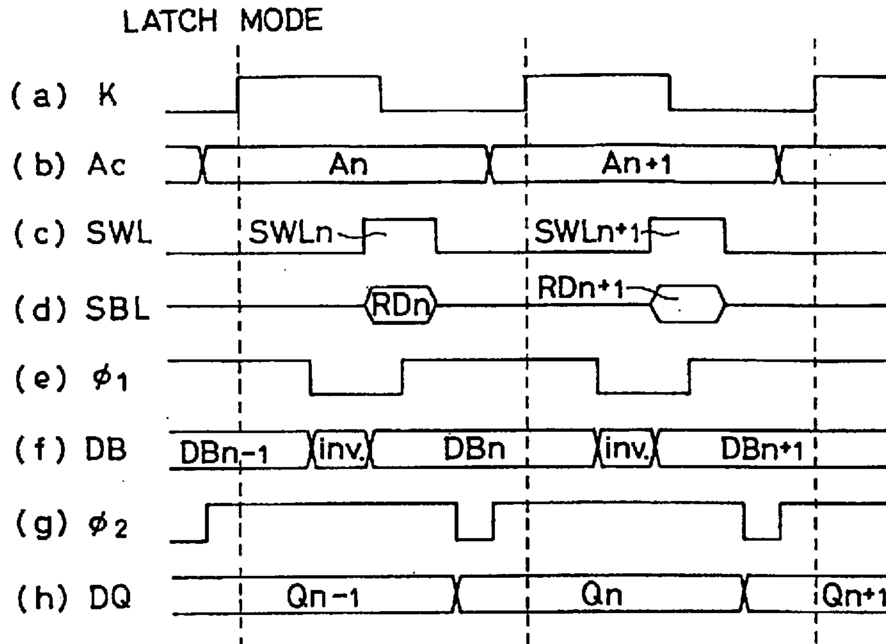


FIG. 42

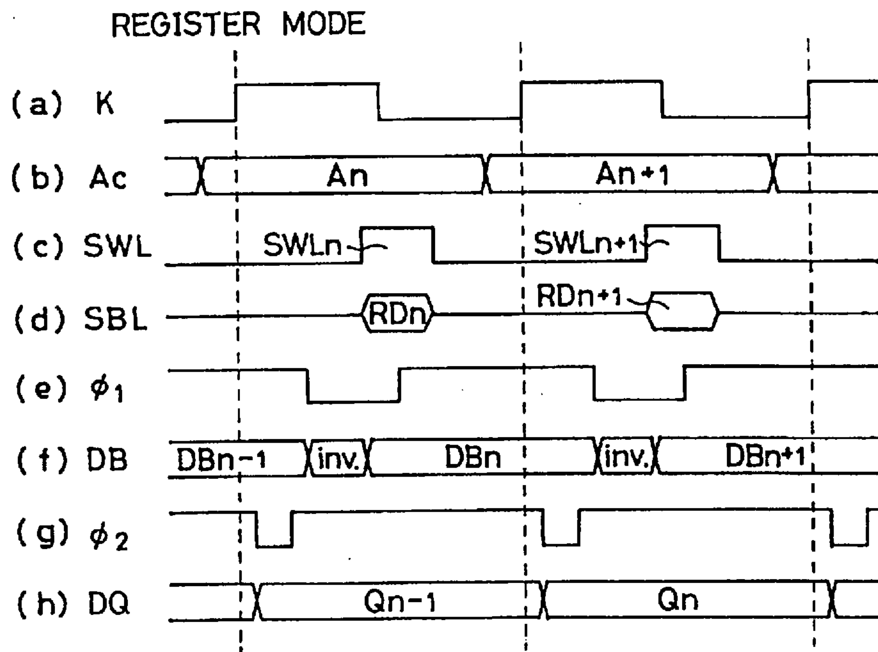


FIG. 43A

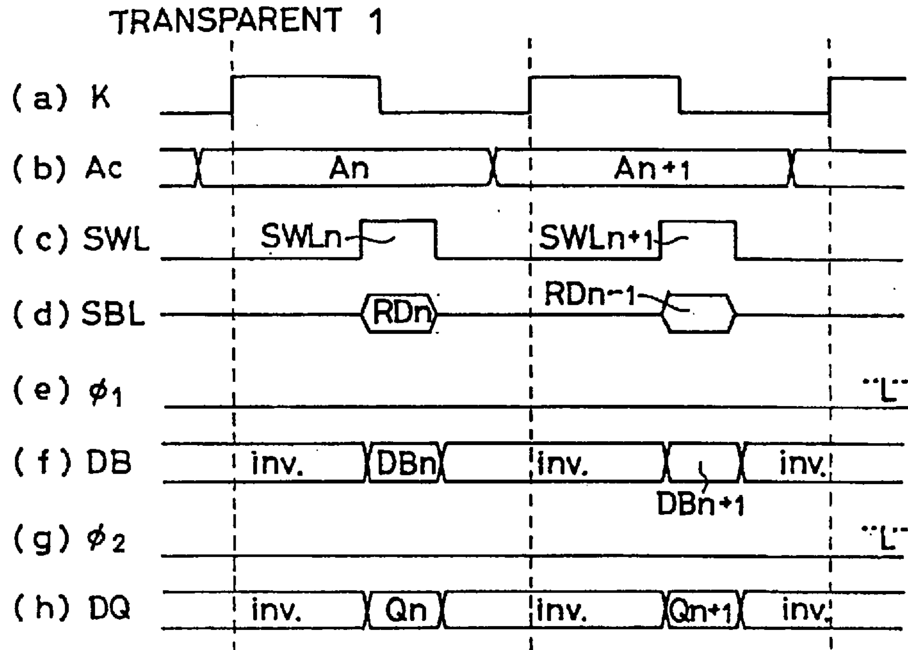


FIG. 43B

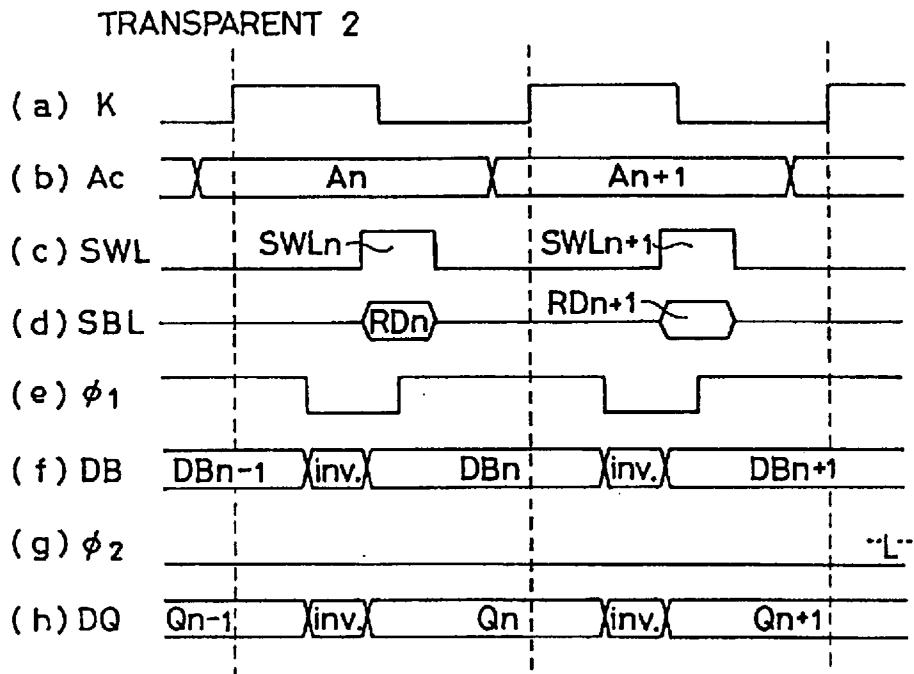


FIG. 44

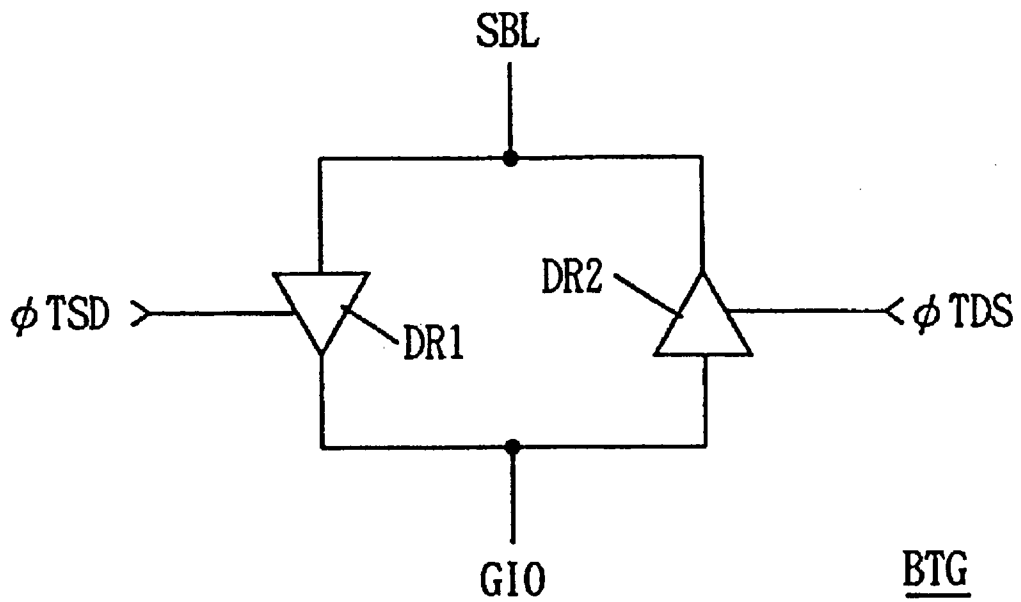


FIG. 45

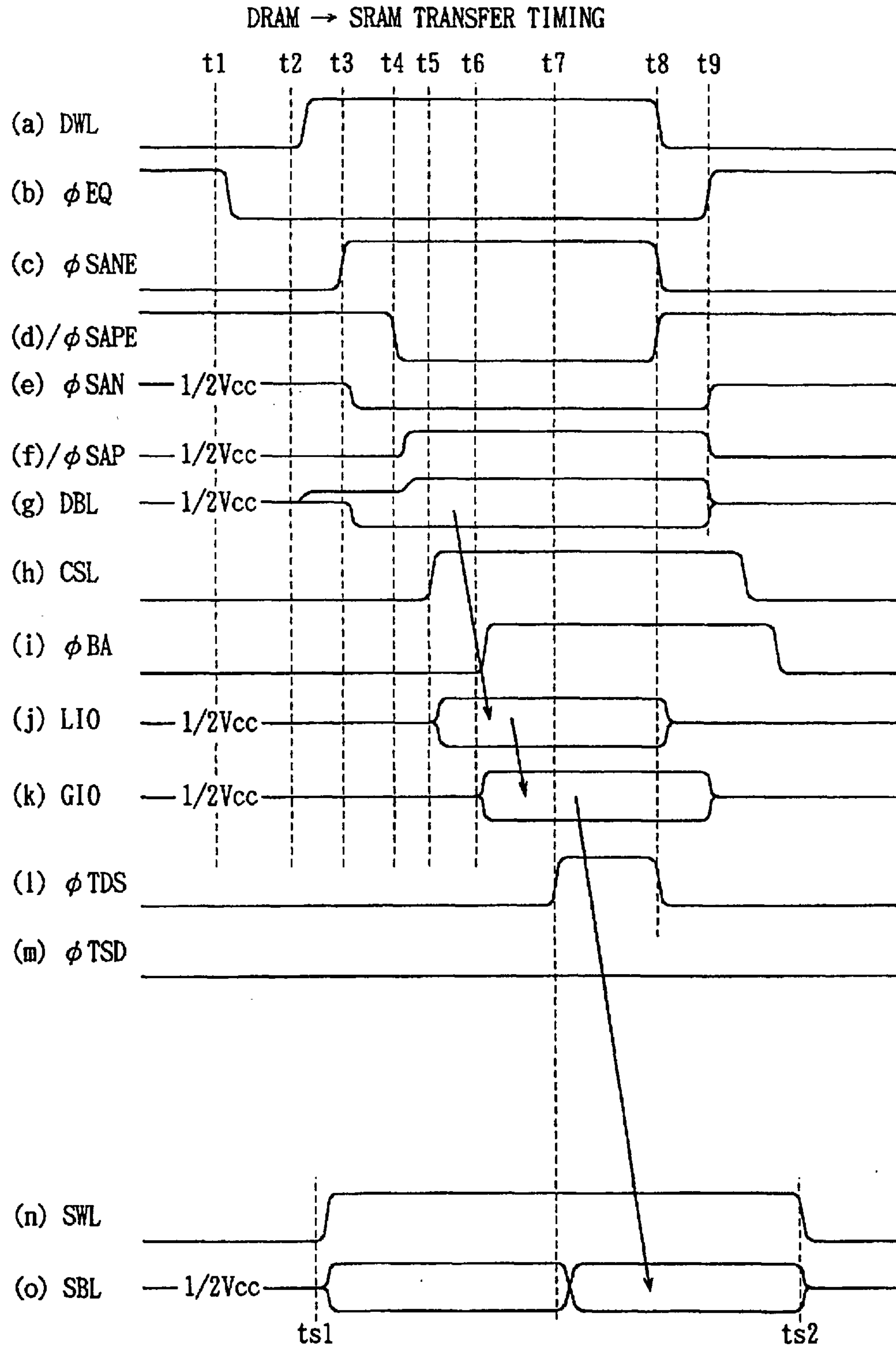


FIG. 46

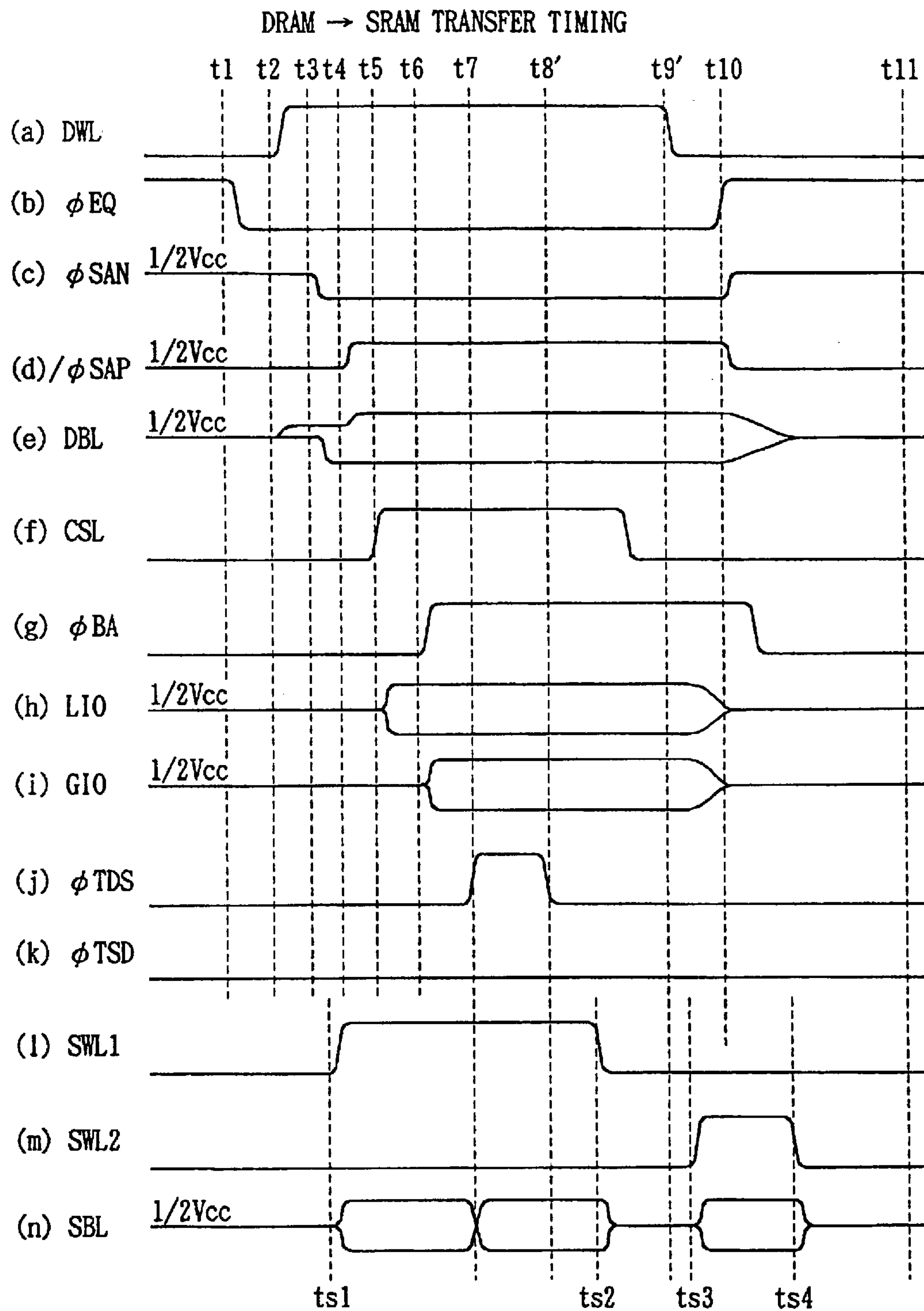


FIG. 47

SRAM → DRAM TRANSFER TIMING

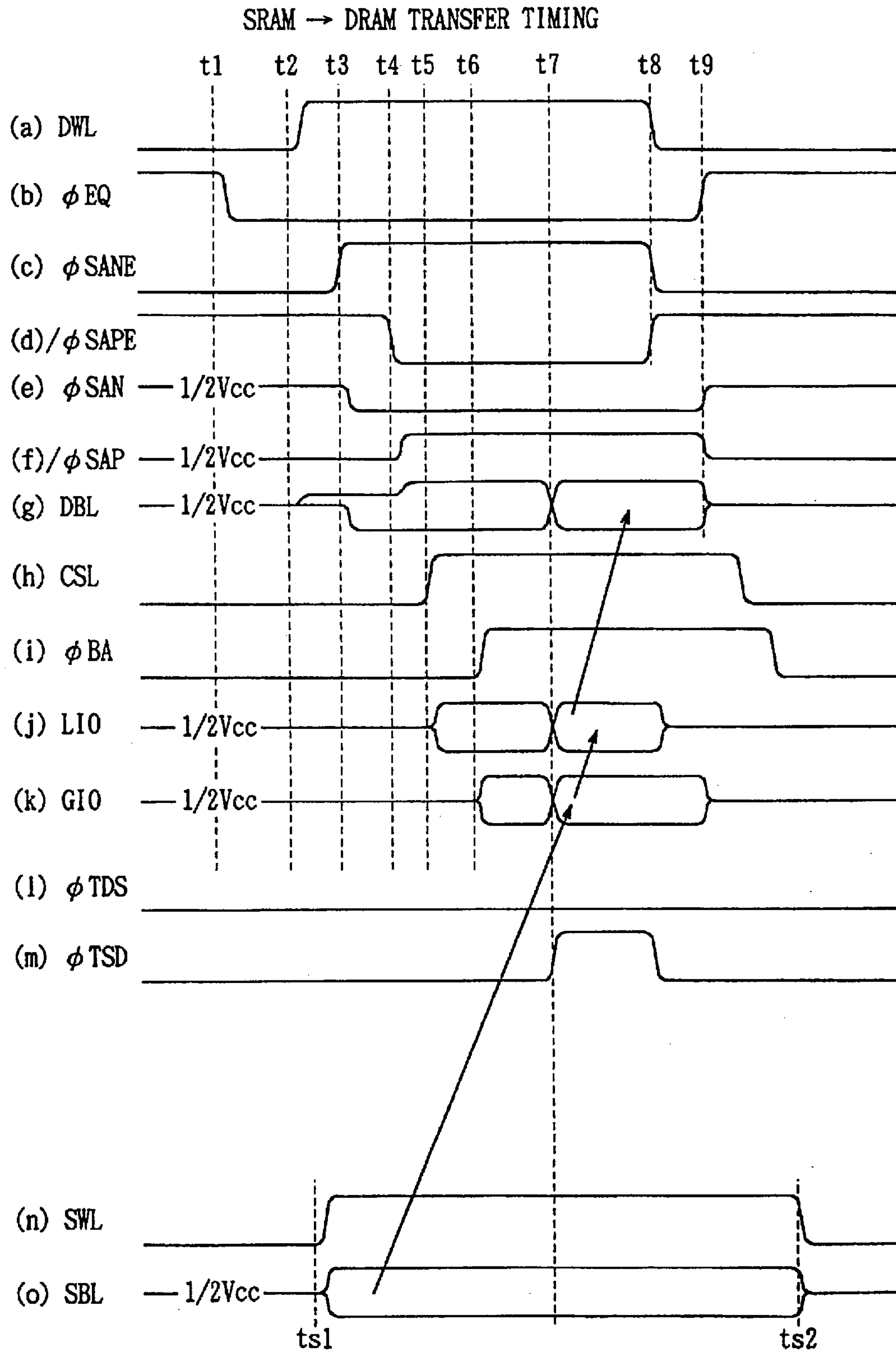


FIG. 48 A

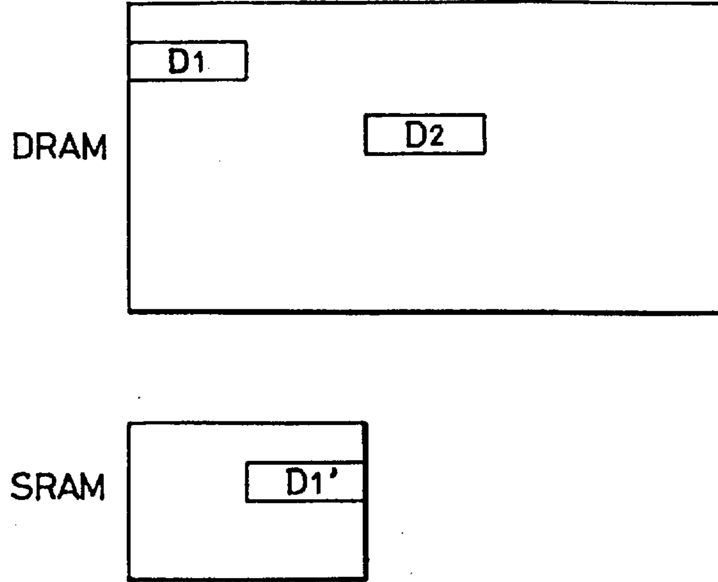


FIG. 48 B

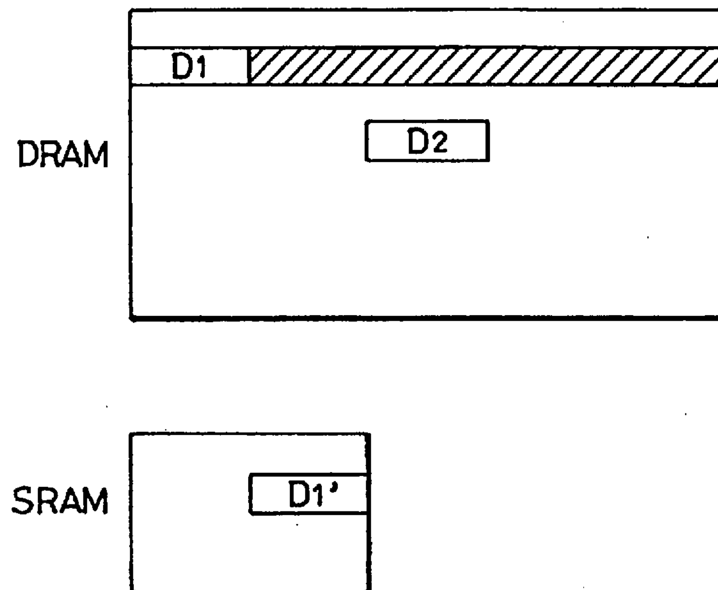


FIG. 48C

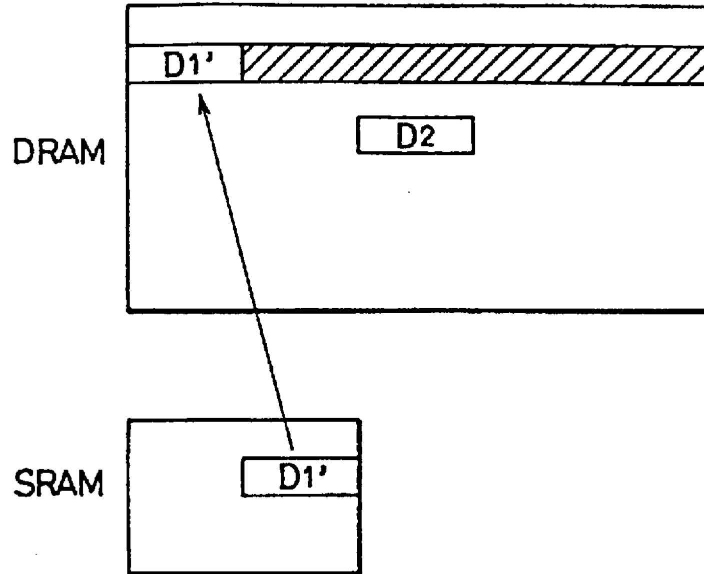


FIG. 48D

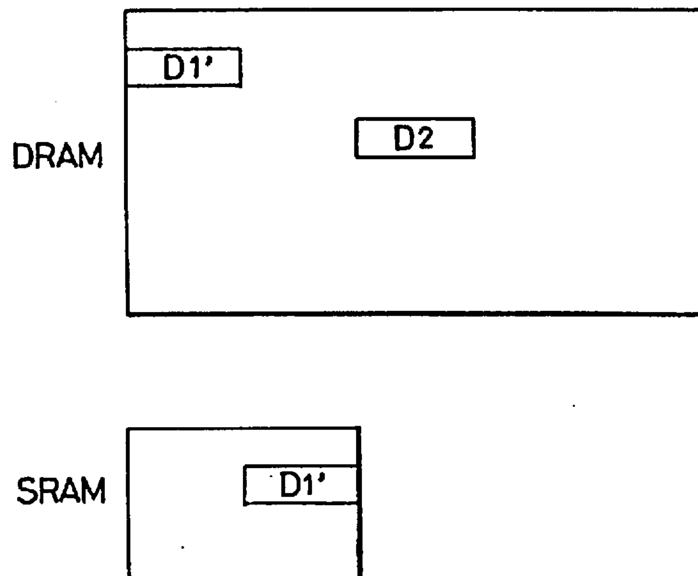


FIG.48E

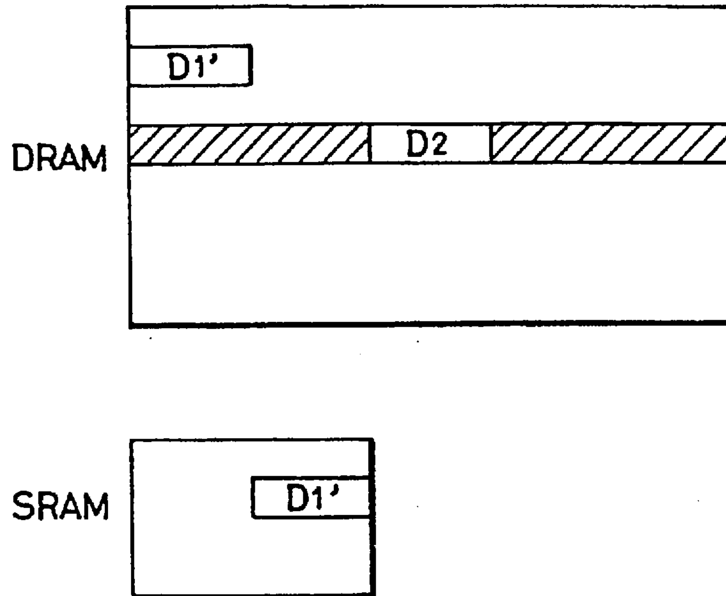
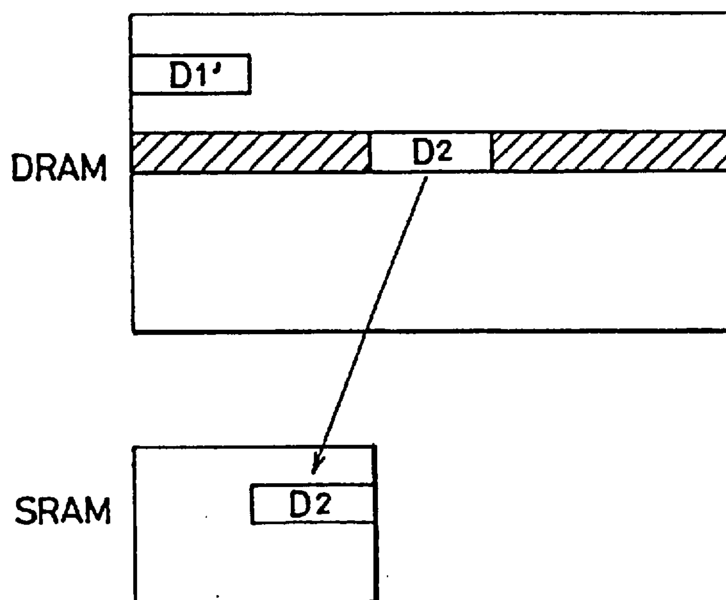


FIG.48F



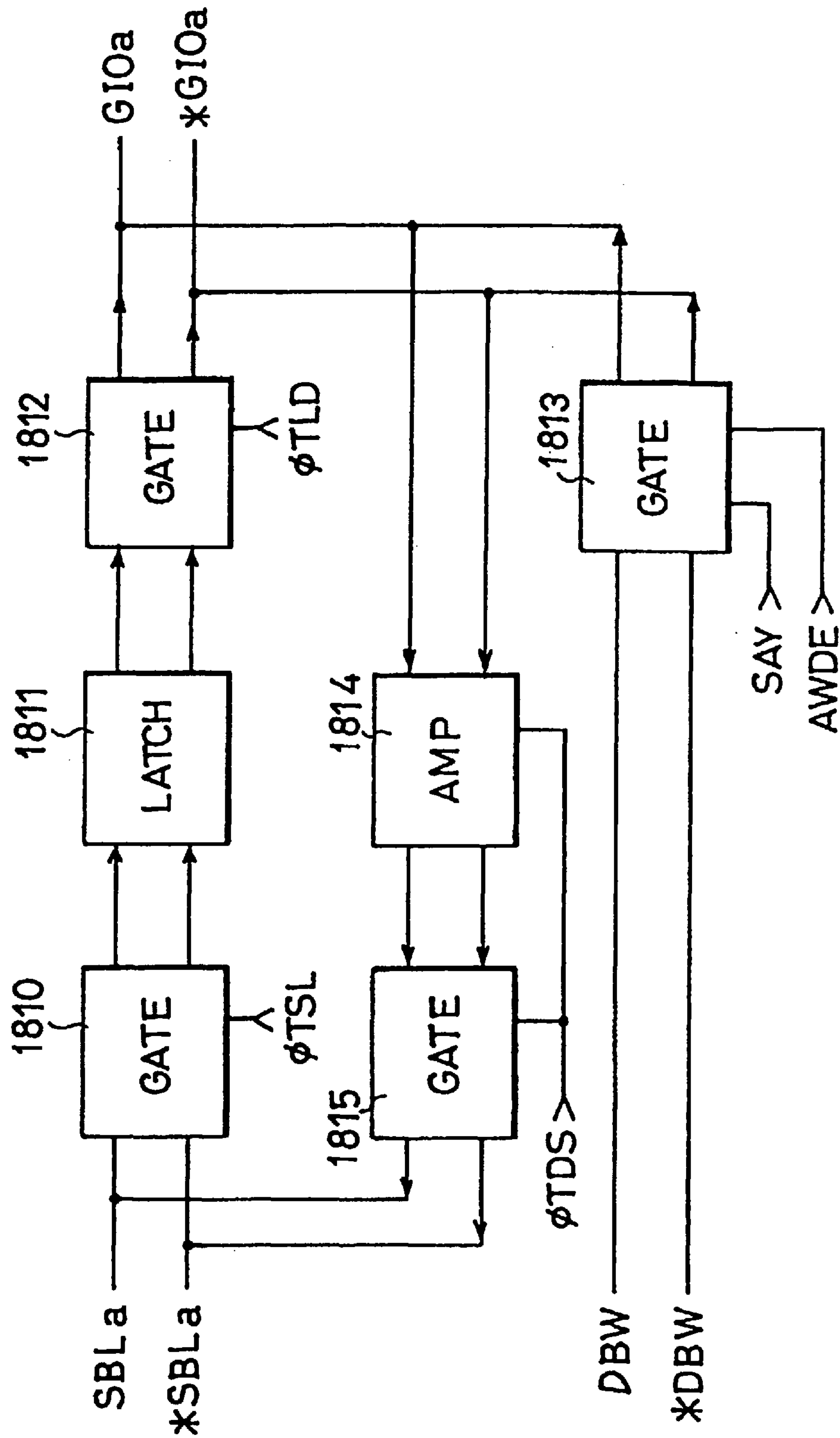


FIG. 49

FIG. 50

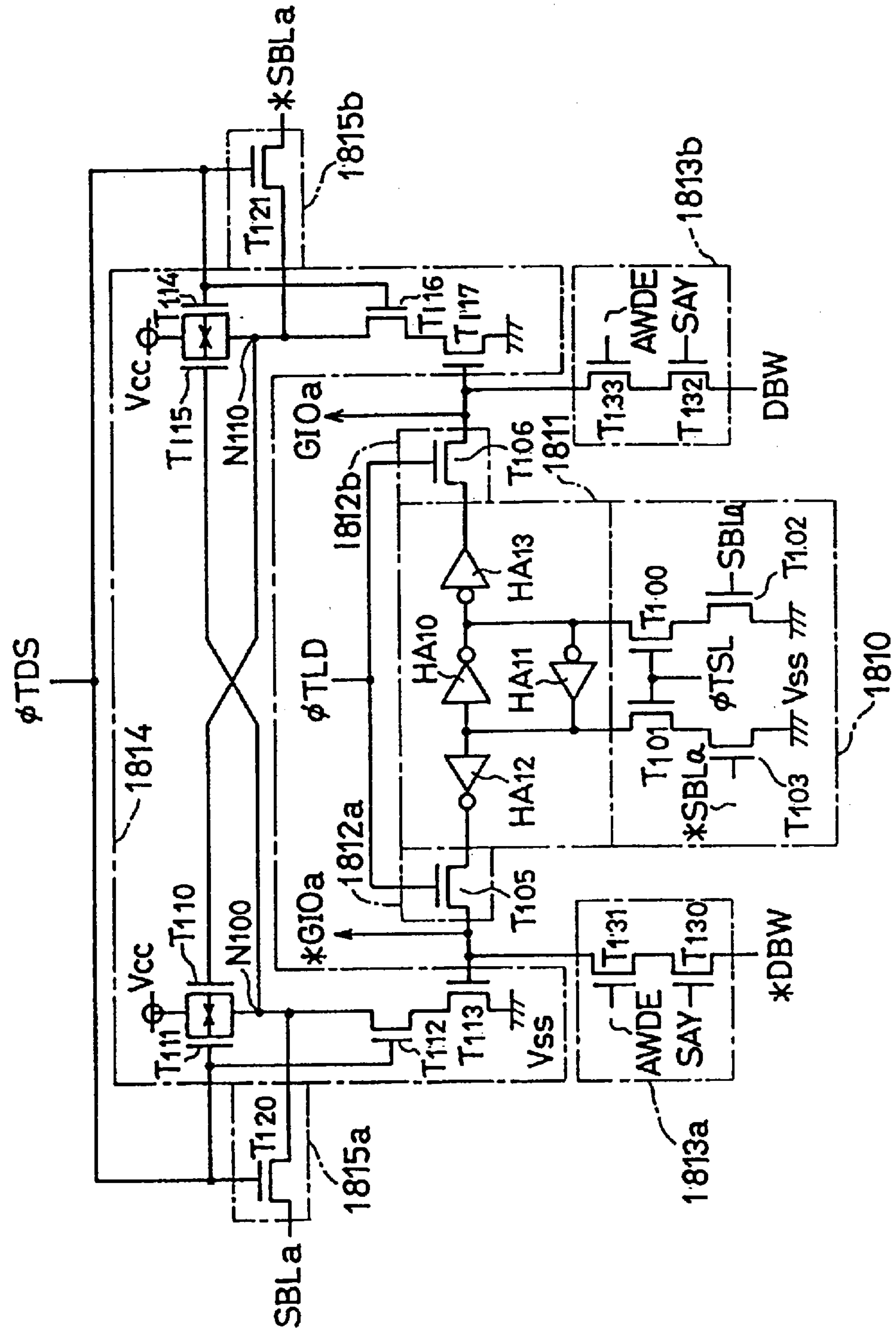


FIG. 51

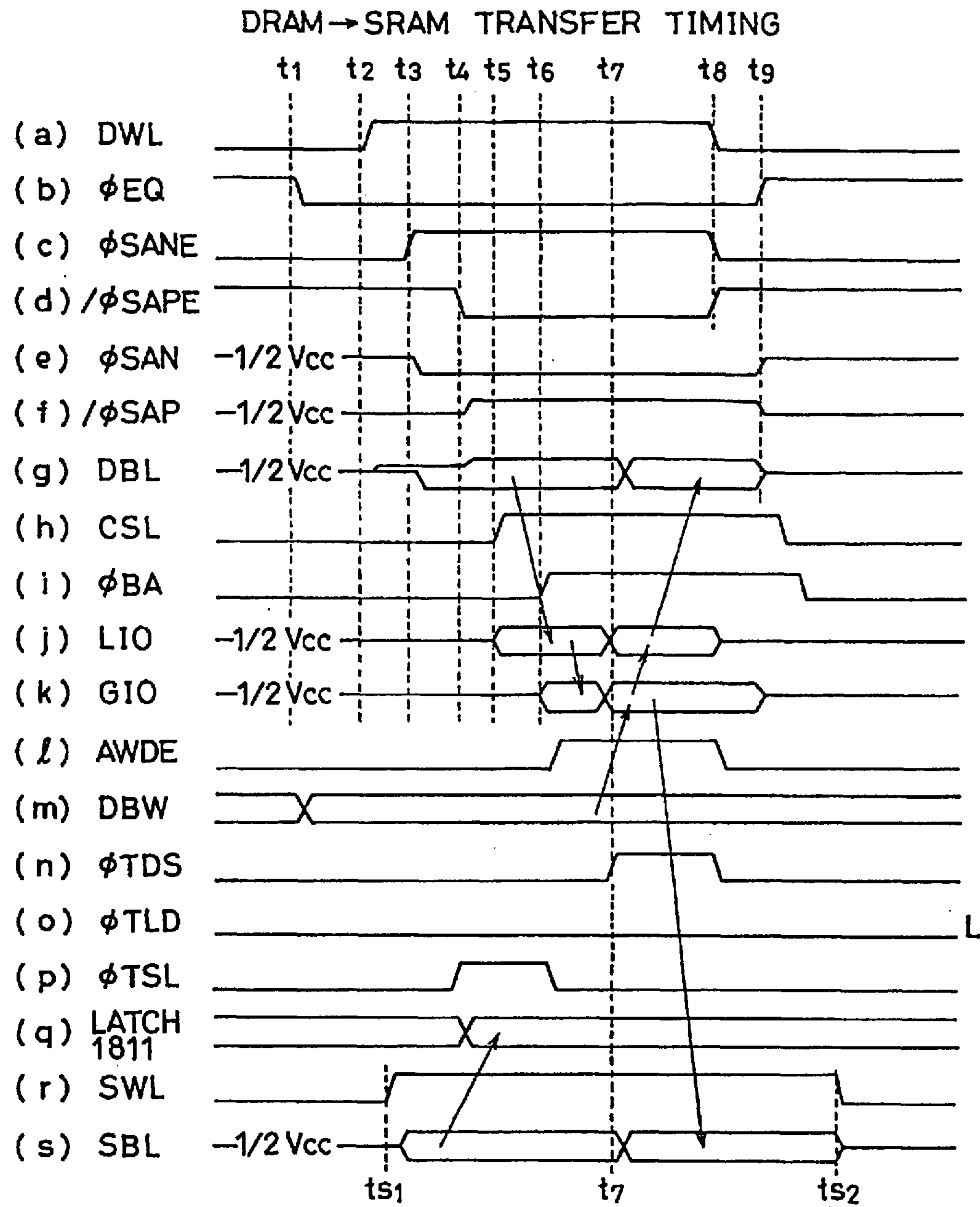


FIG. 52A

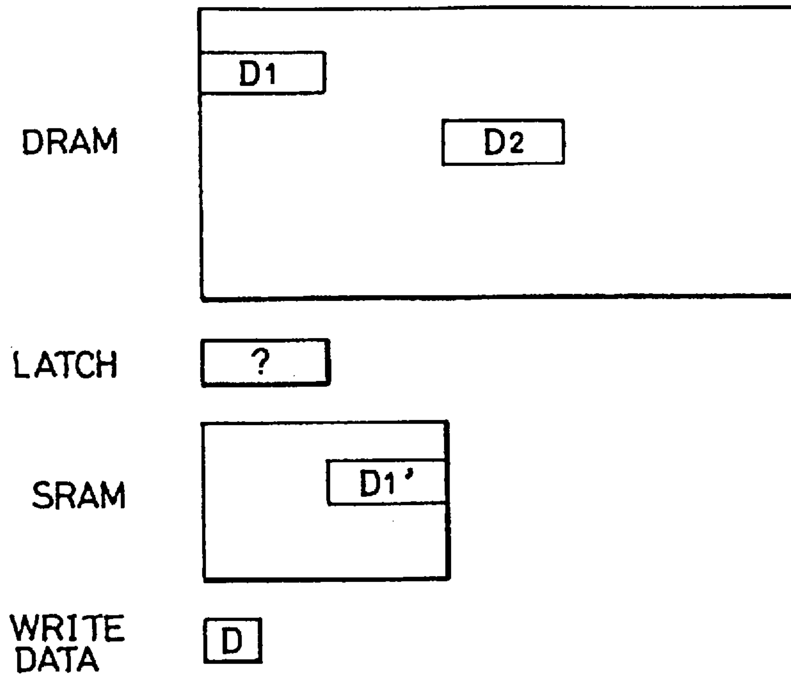


FIG. 52B

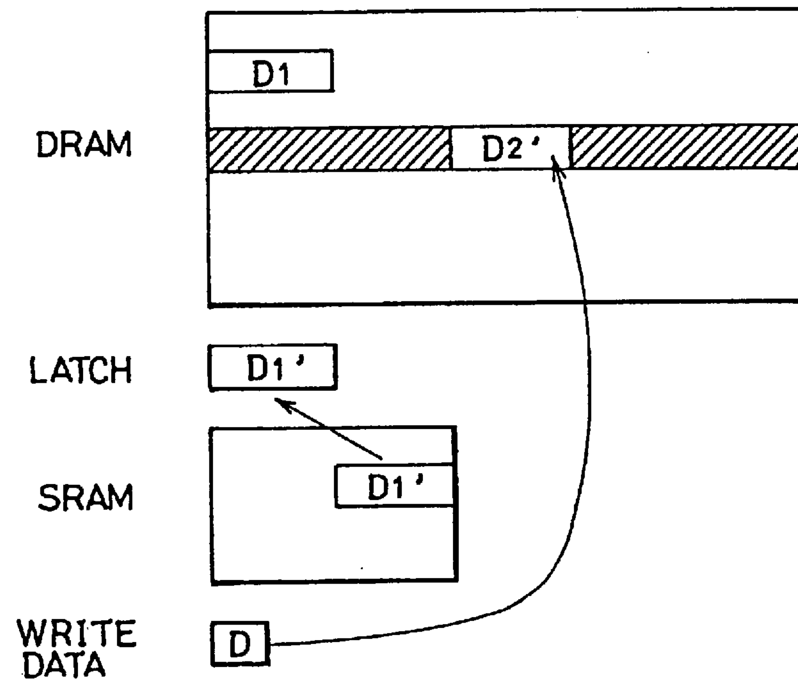


FIG. 52C

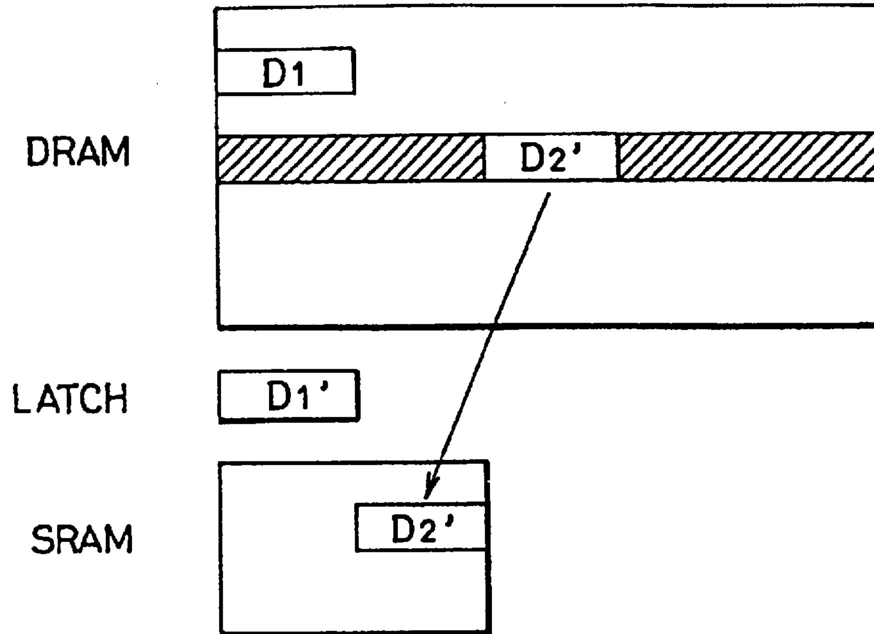


FIG. 52D

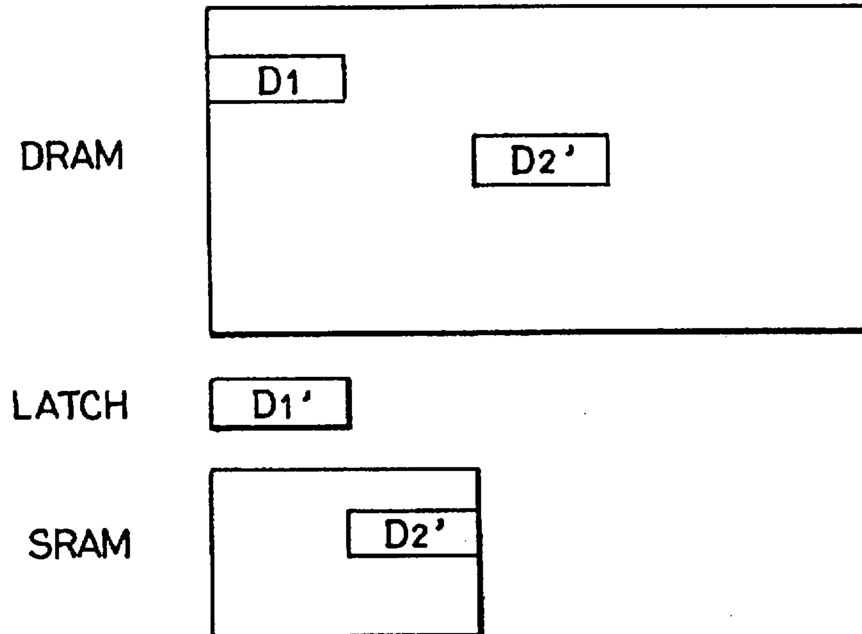


FIG. 53

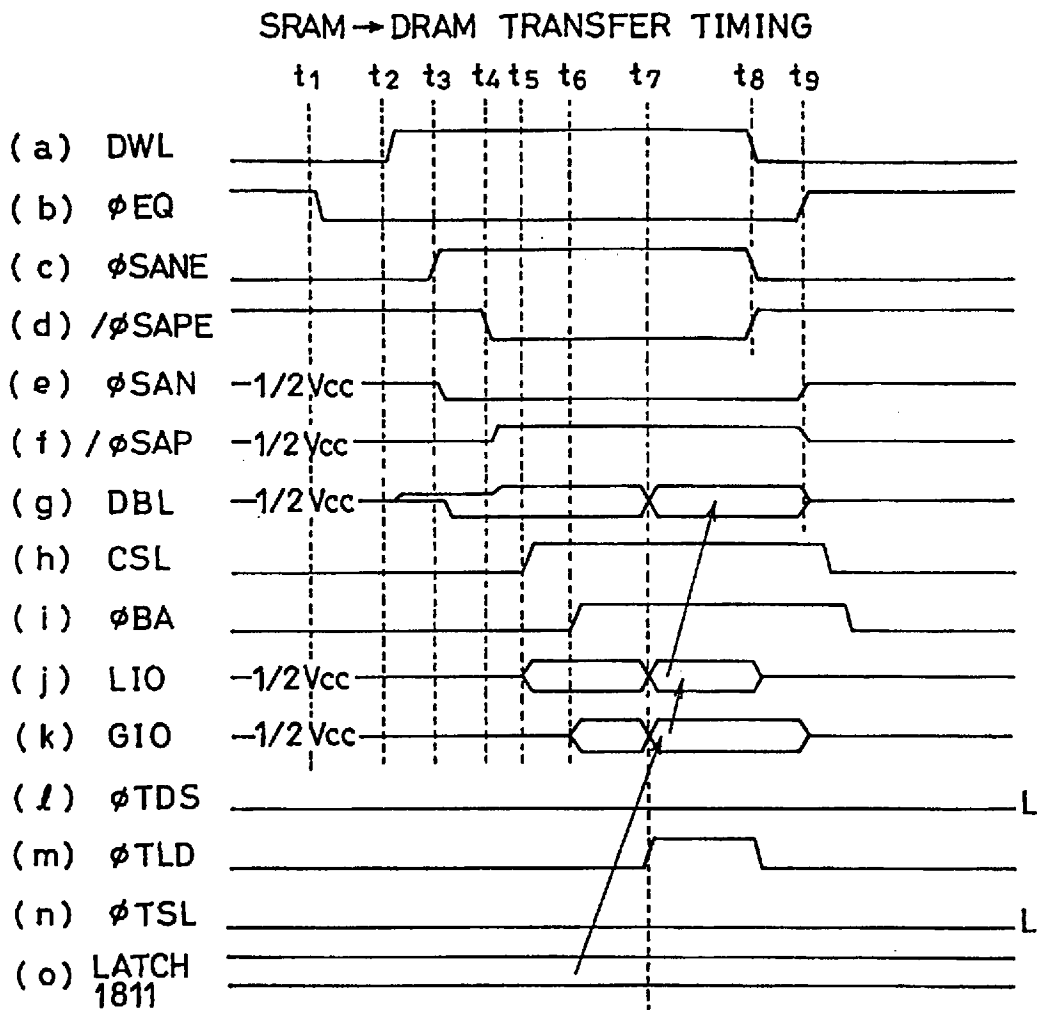


FIG. 54A

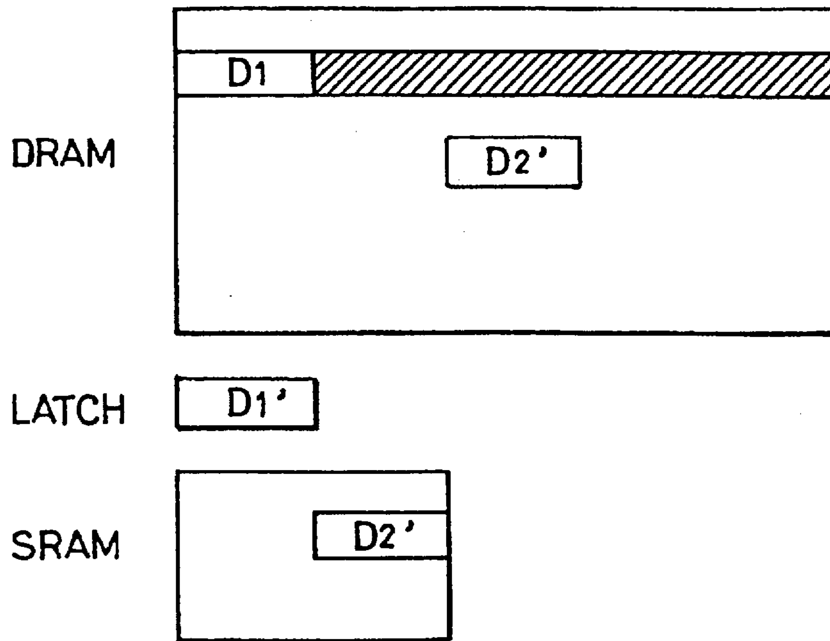


FIG. 54B

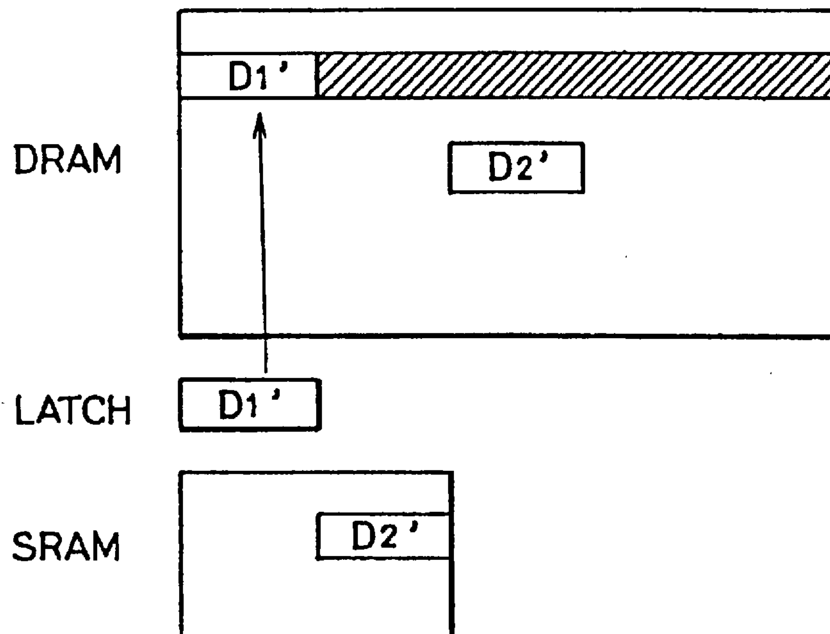


FIG. 55

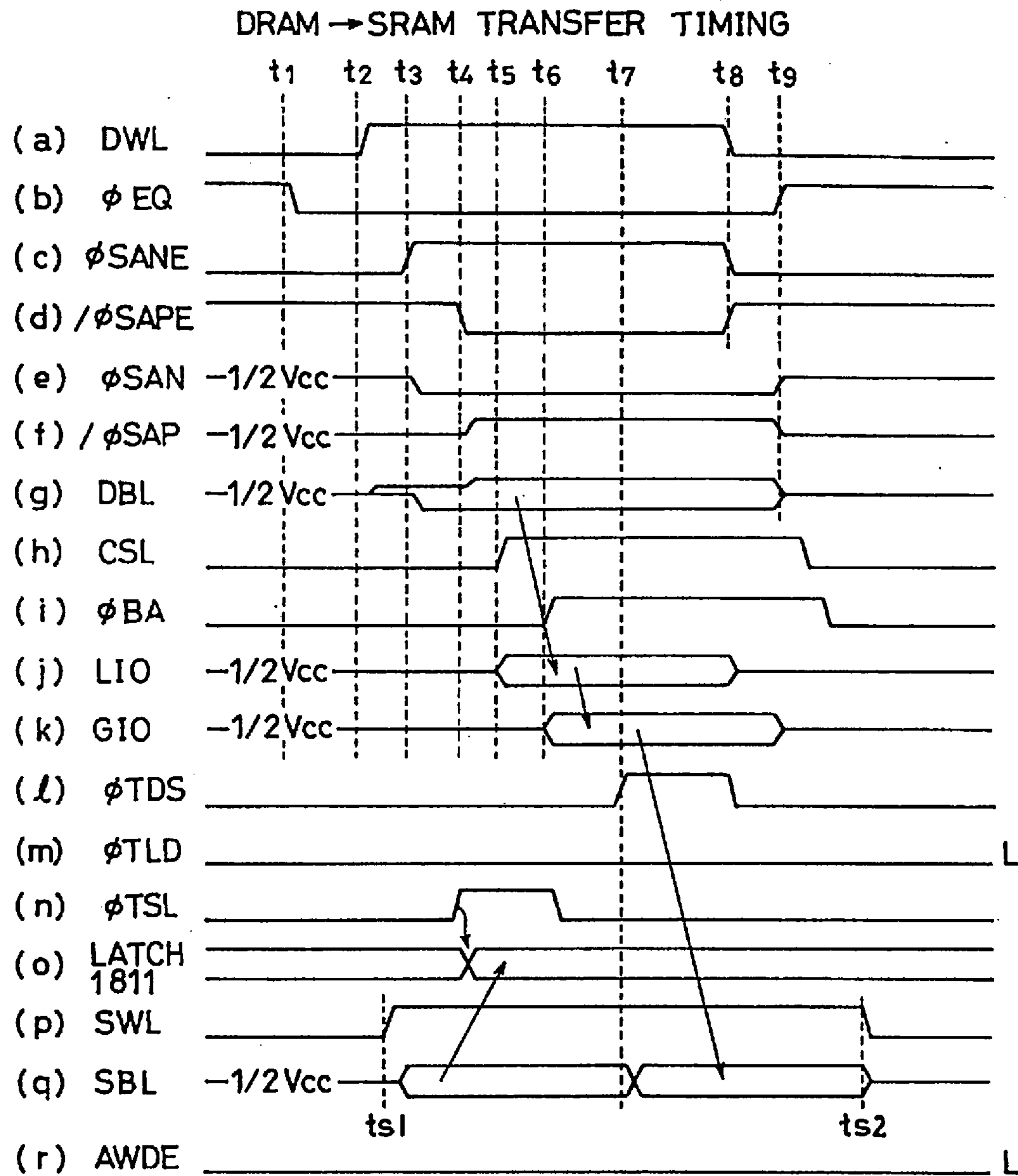


FIG. 56A

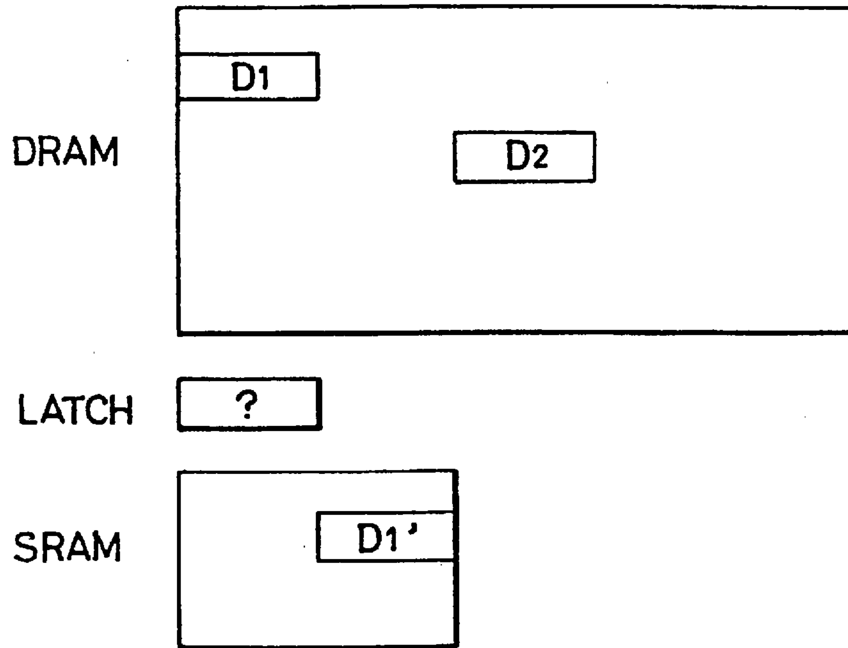


FIG. 56B

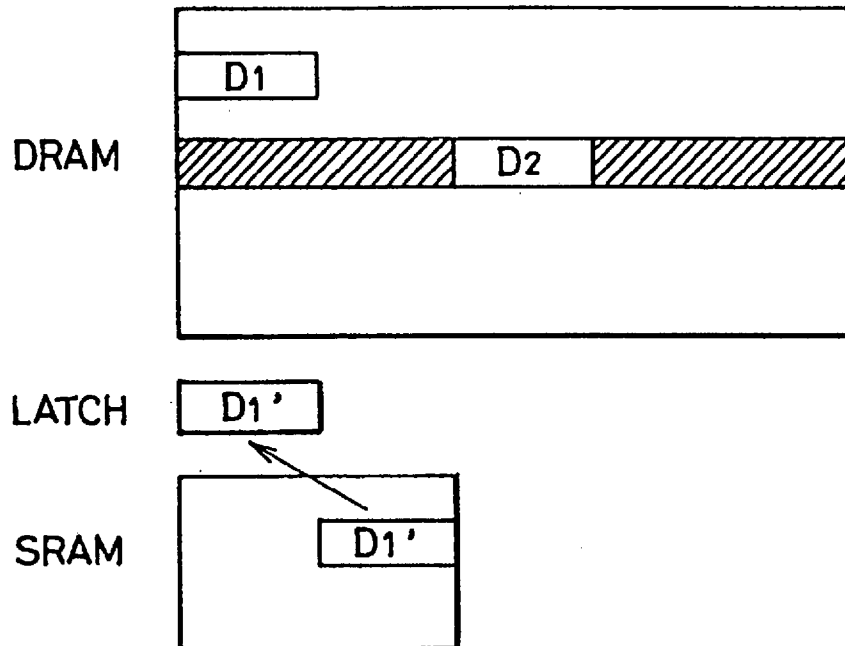


FIG. 56C

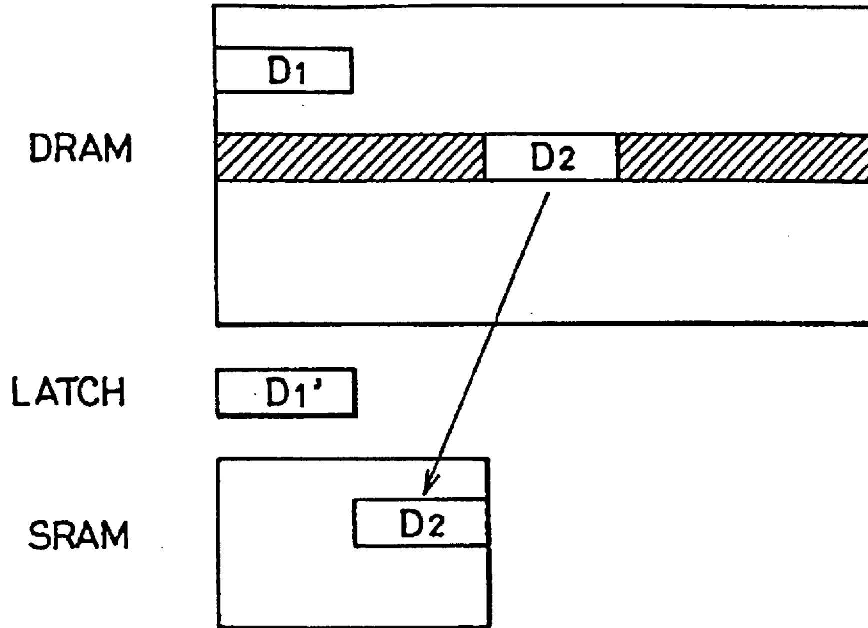


FIG. 56D

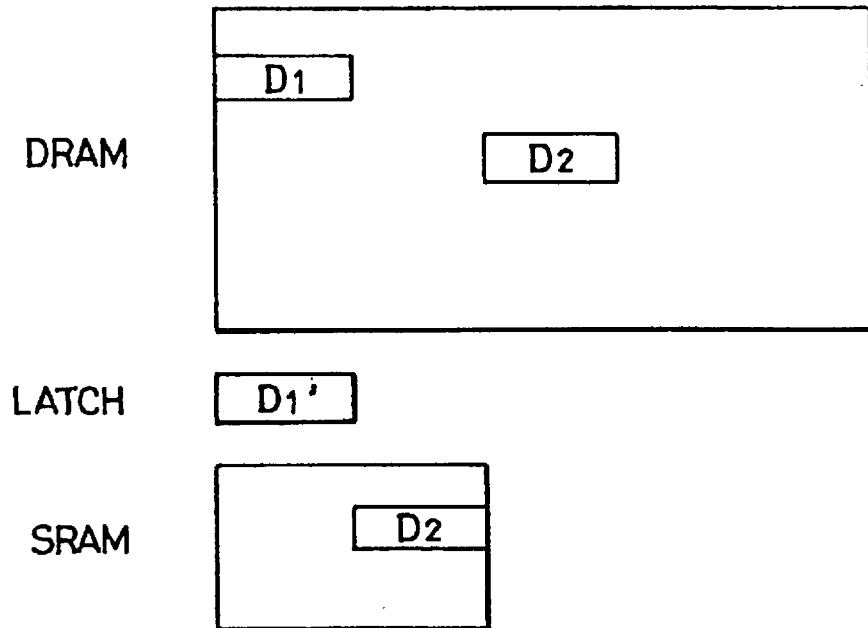


FIG. 56E

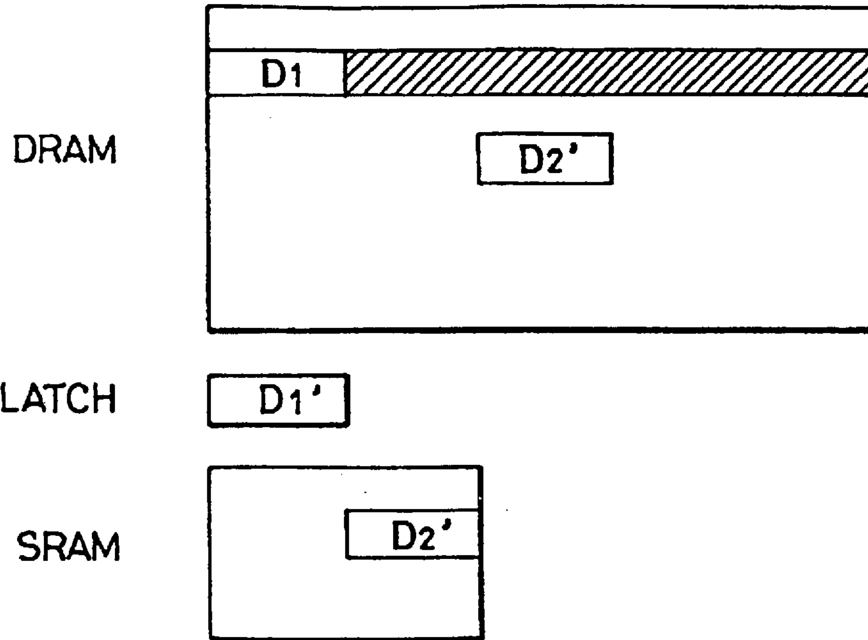
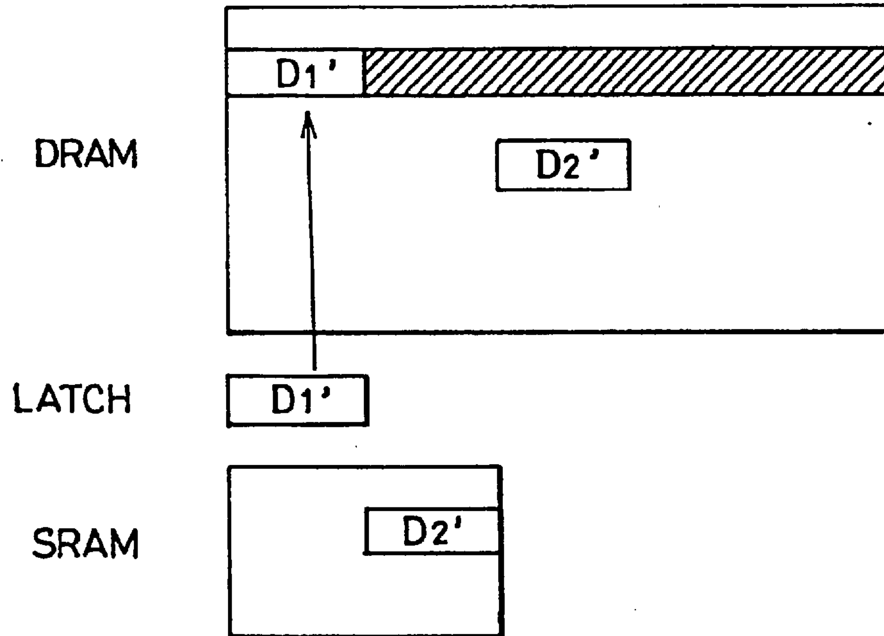


FIG. 56F



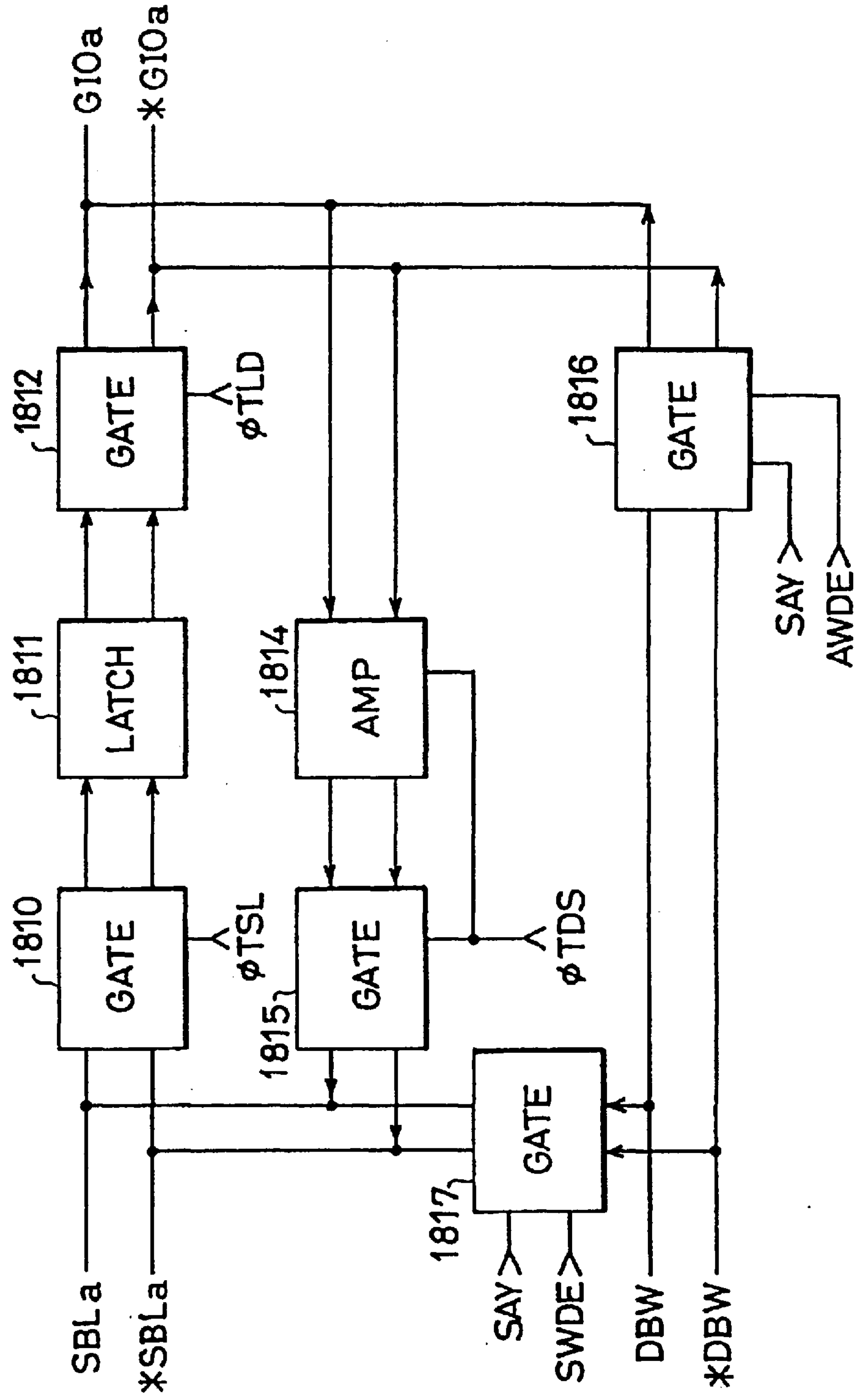


FIG. 57

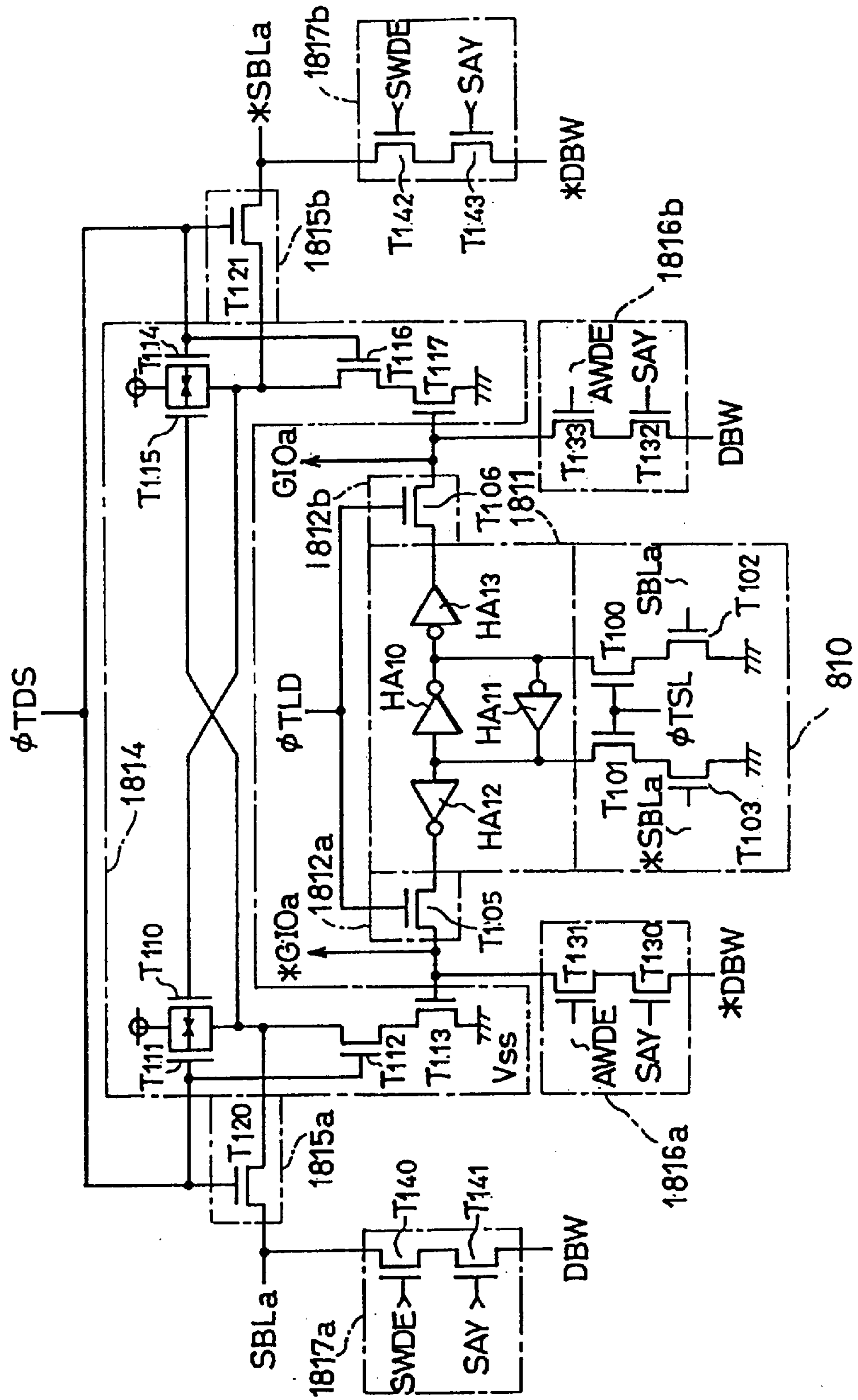


FIG. 58

FIG. 59

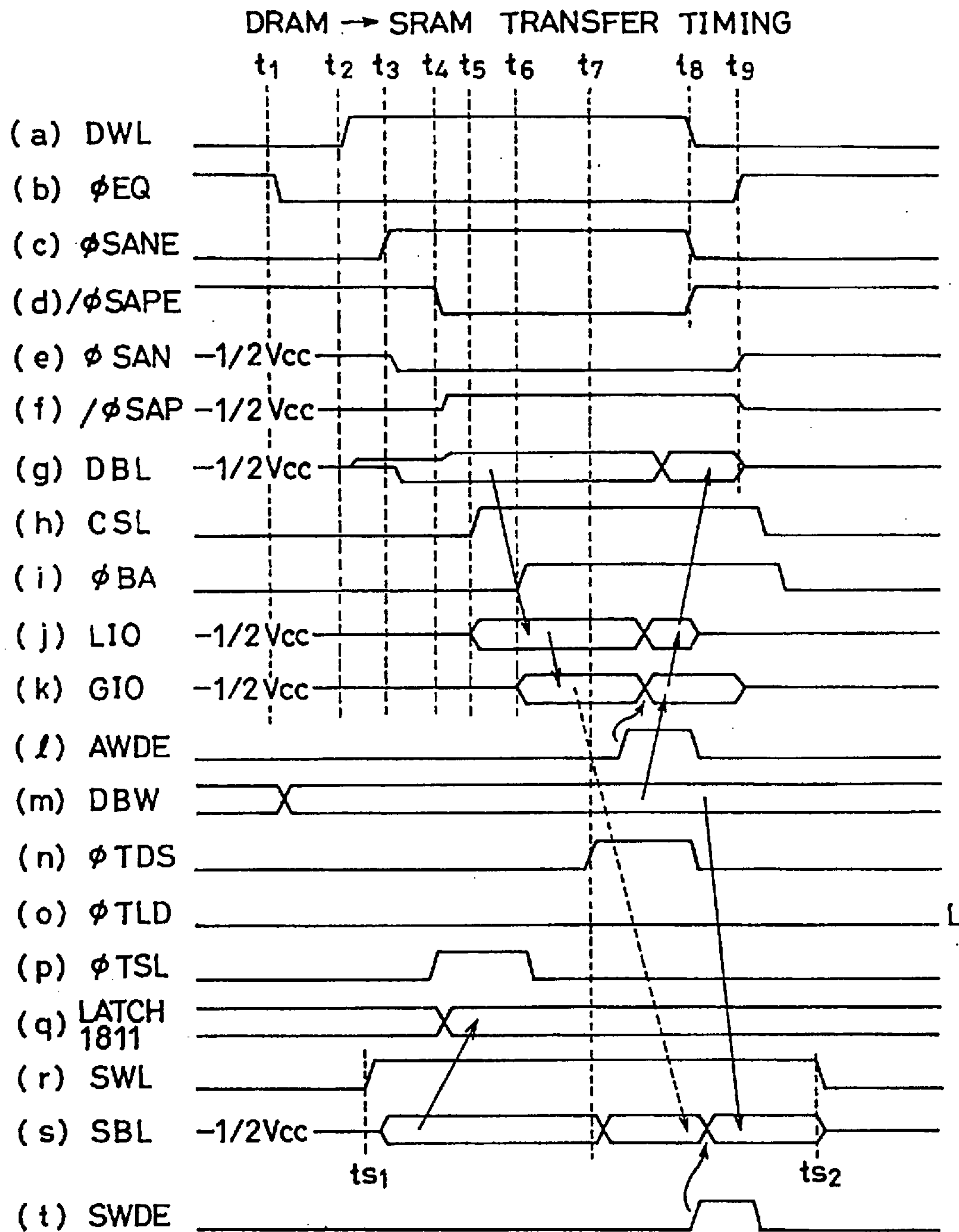


FIG. 60A

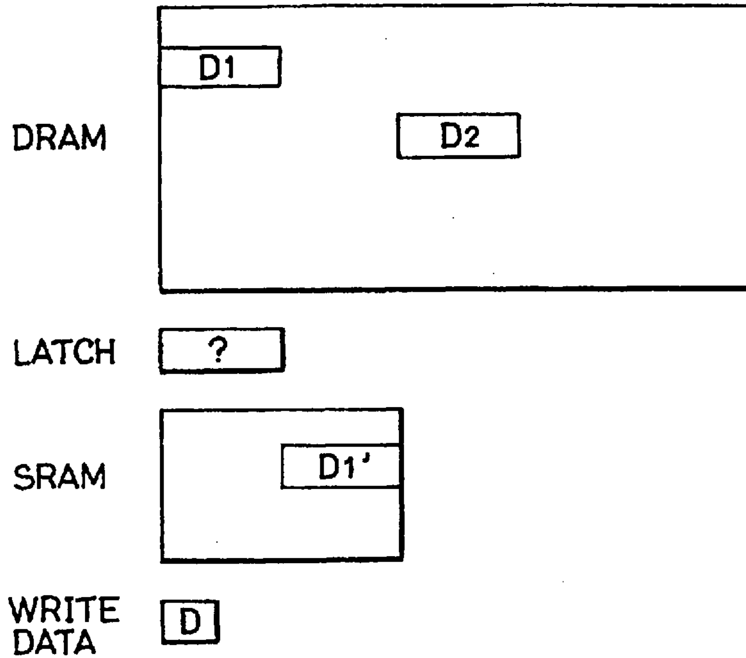


FIG. 60B

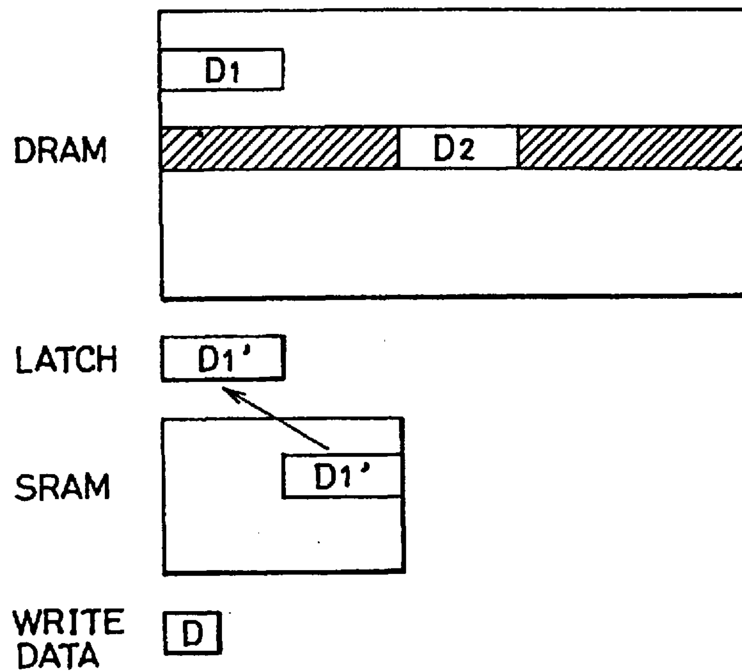


FIG. 60C

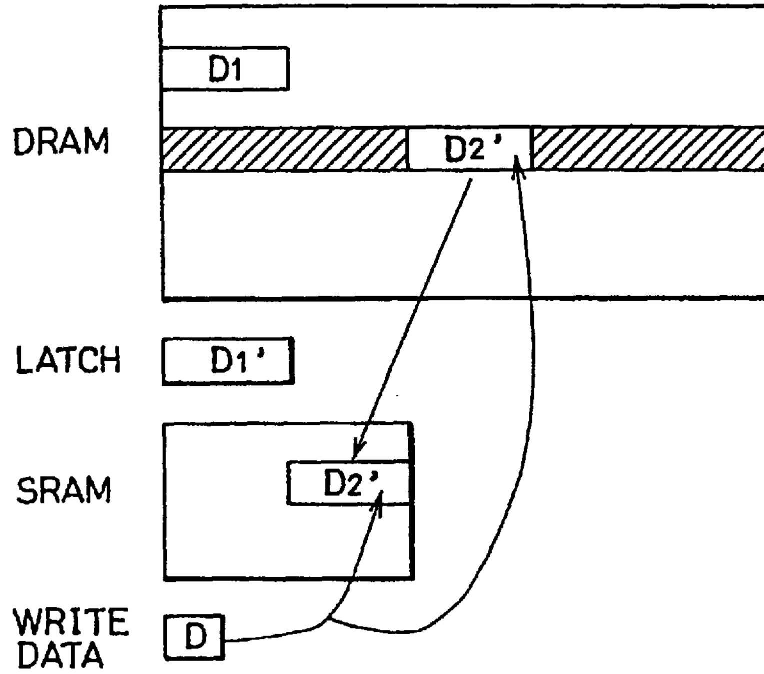


FIG. 60D

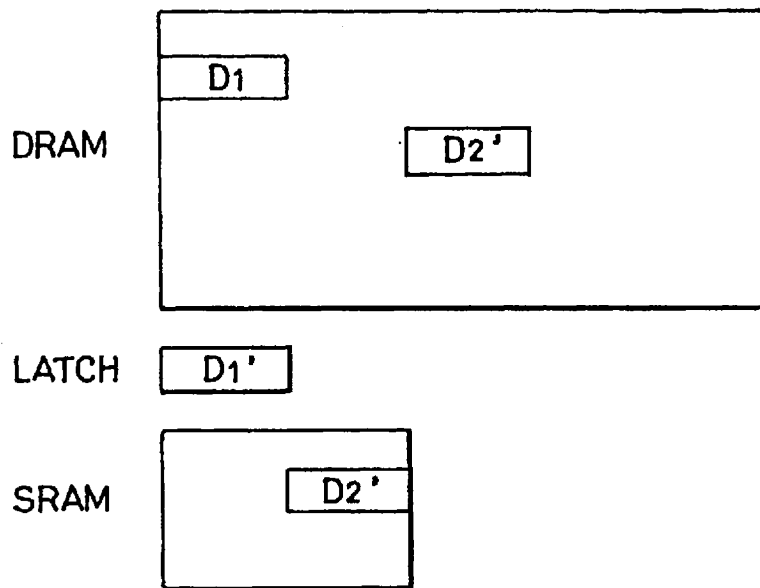


FIG. 61

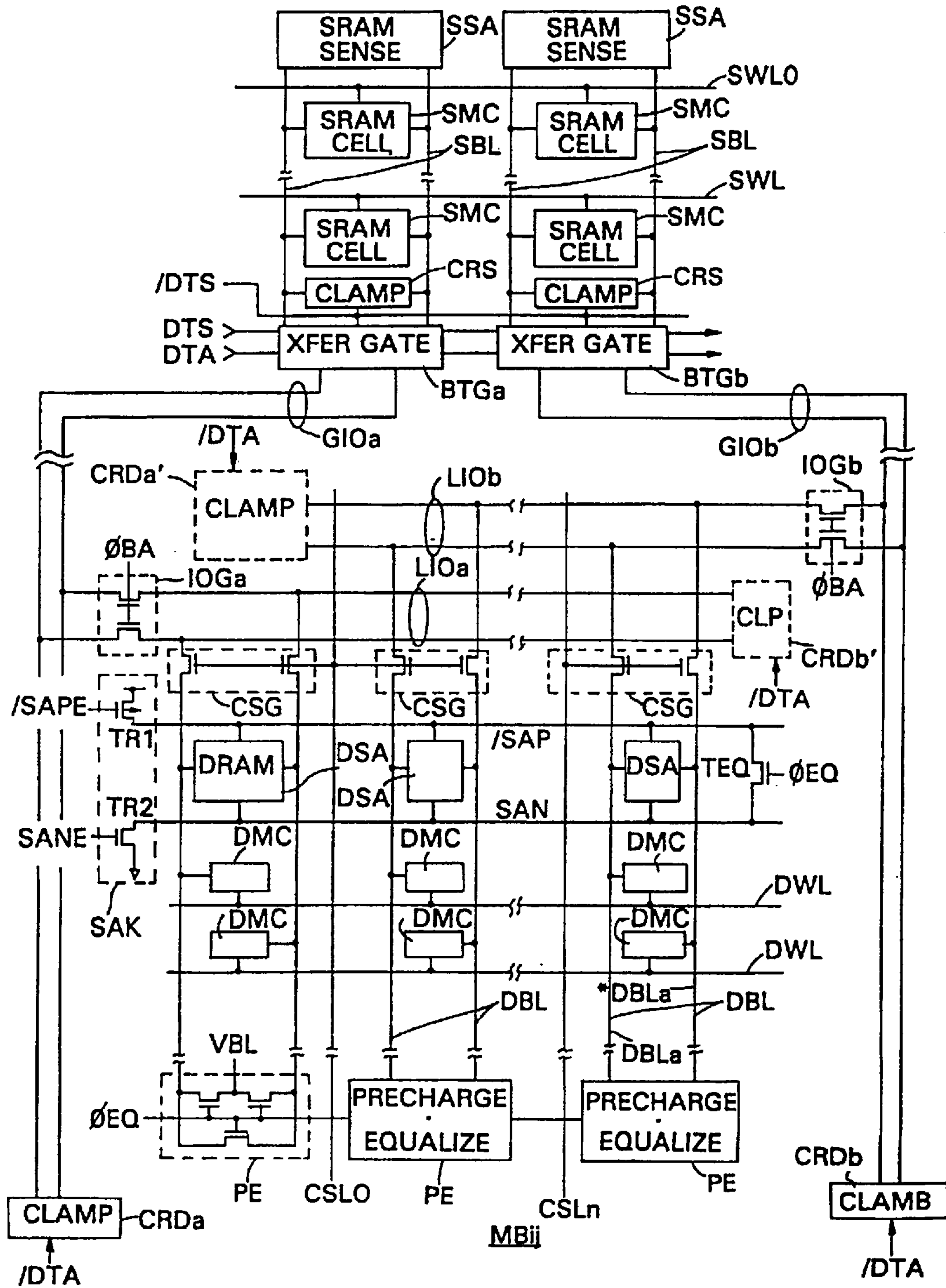


FIG. 62

Vcc
Vcc
CRS
SQ80
SQ70
/DTS
/DTS
SSA
SRAM SENSE
SMC
SRAM CELL
SMC
SRAM CELL
SBLa
*SBLa
SWL0
SBL
SWLm
BTG
XFER GATE
DTS
DTA
Vcc
DQ80
DQ70
/DTA
/DTA
CRD
DIO
*DIOa
DIOa
SG0
CSL0
CSLn
SGn
DMC
DRAM CELL
DWL0
DMC
DRAM CELL
DWLp
DBL
SAN
DSA
DRAM SENSE
/SAP
DBLa0
*DBLa0
DBLan
*DBLan
DSA

FIG. 63

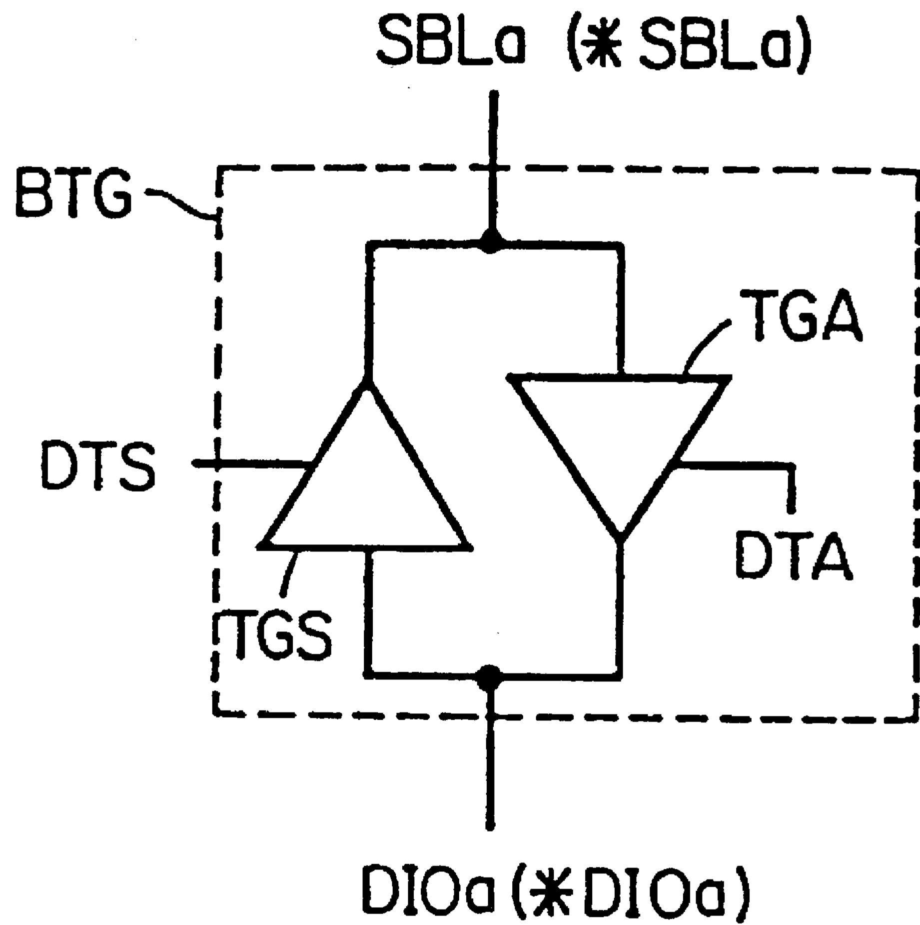


FIG. 64

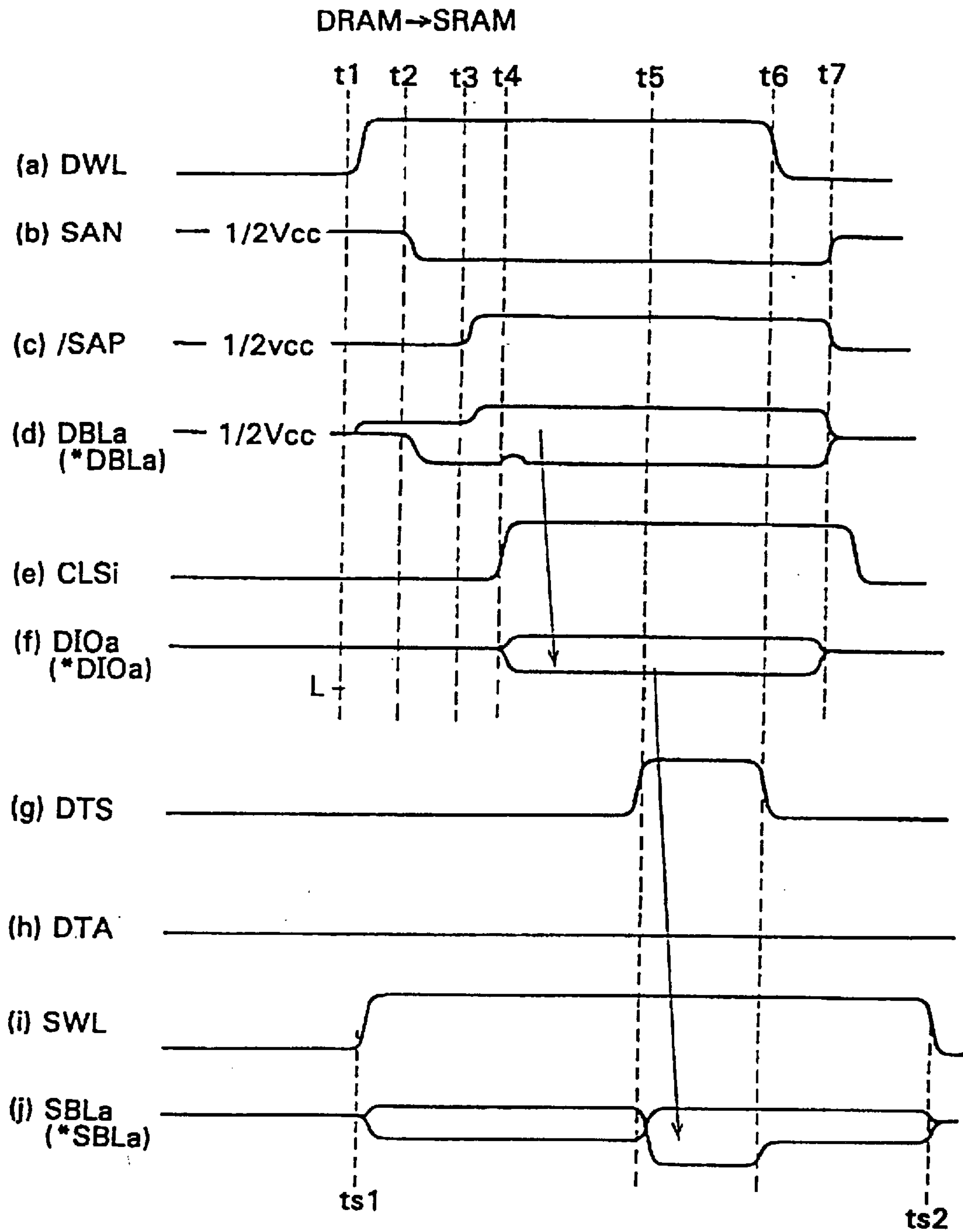


FIG. 65

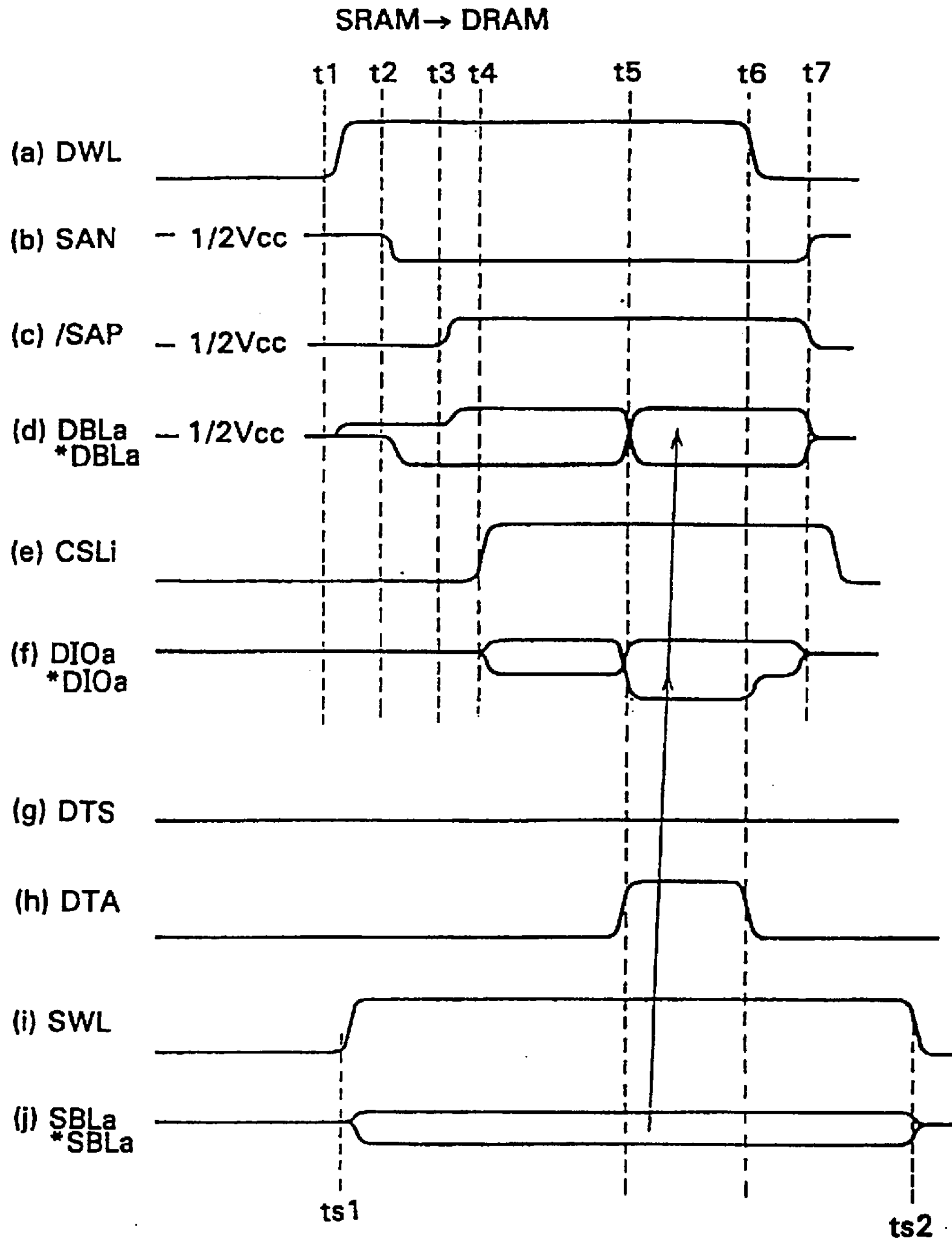


FIG.66

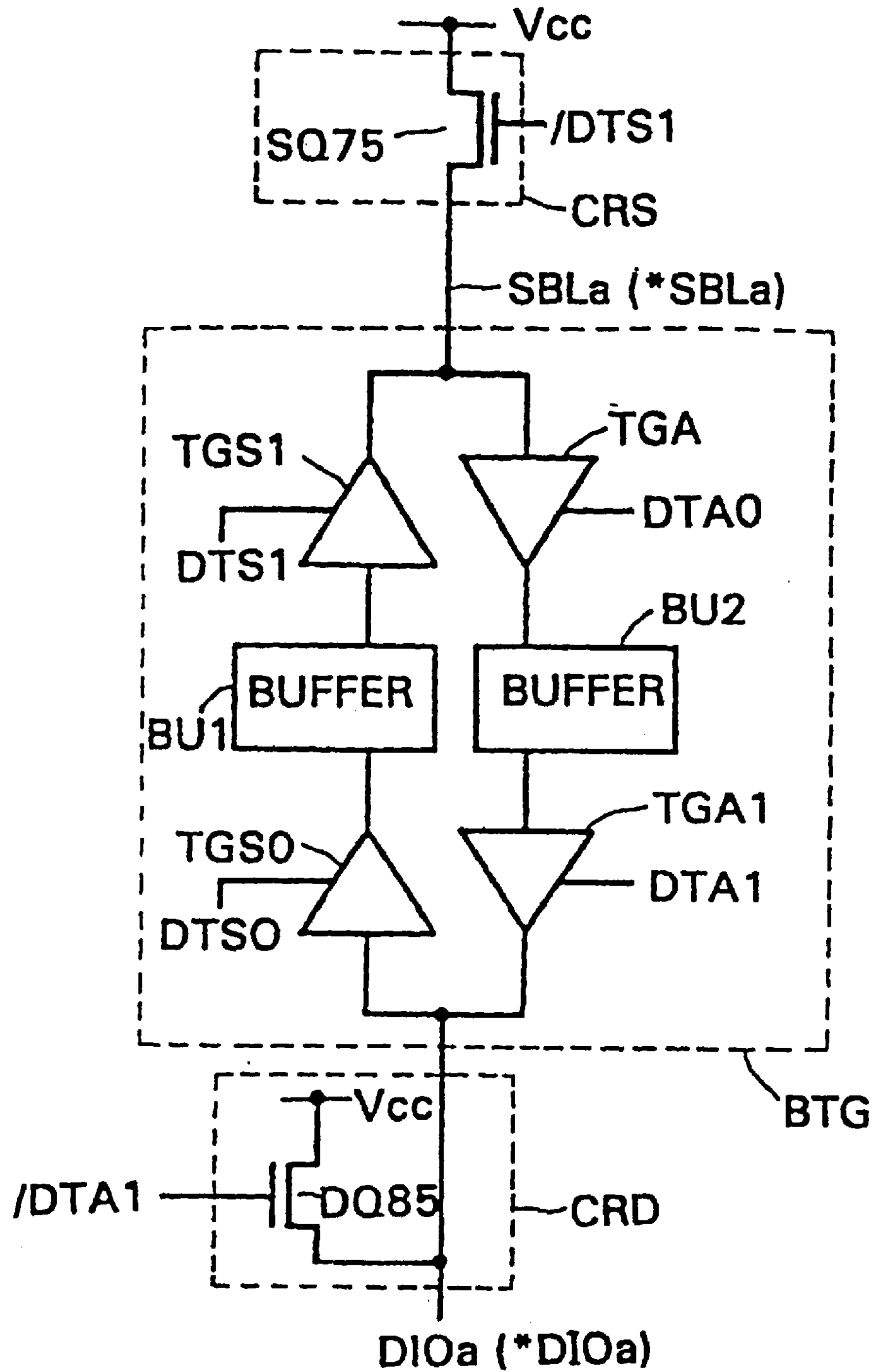


FIG. 67A

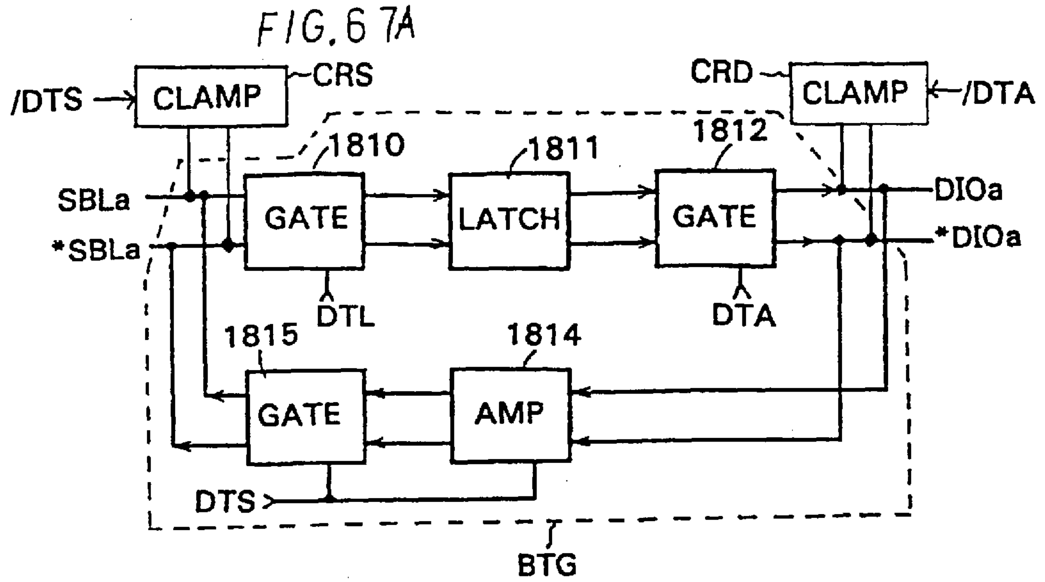


FIG. 67B

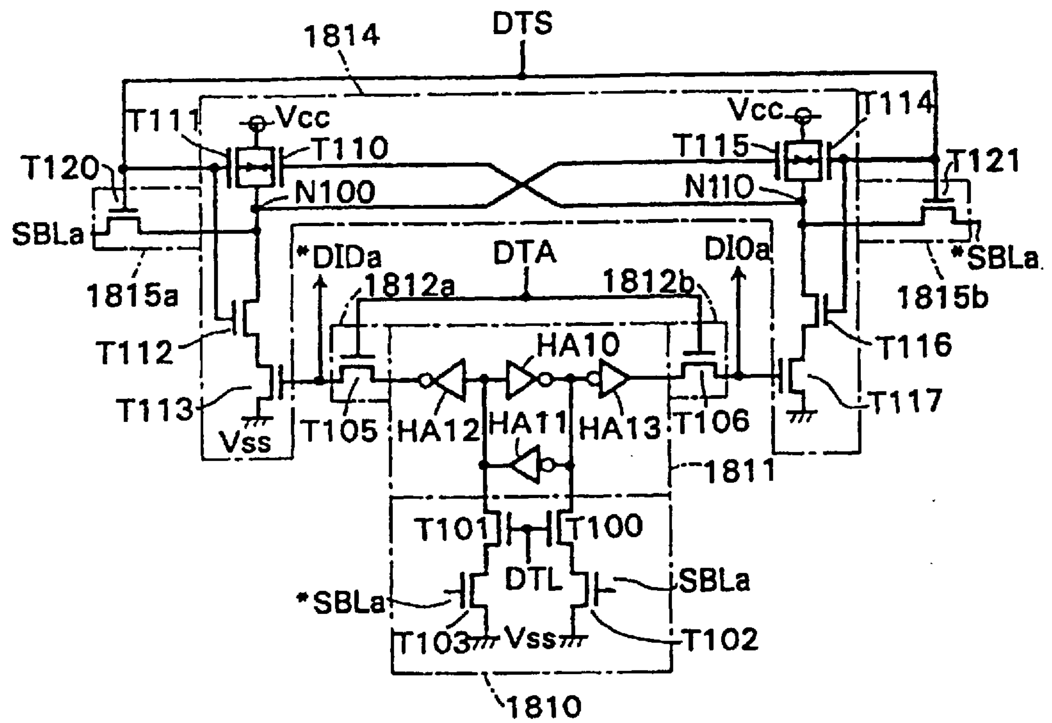


FIG.68

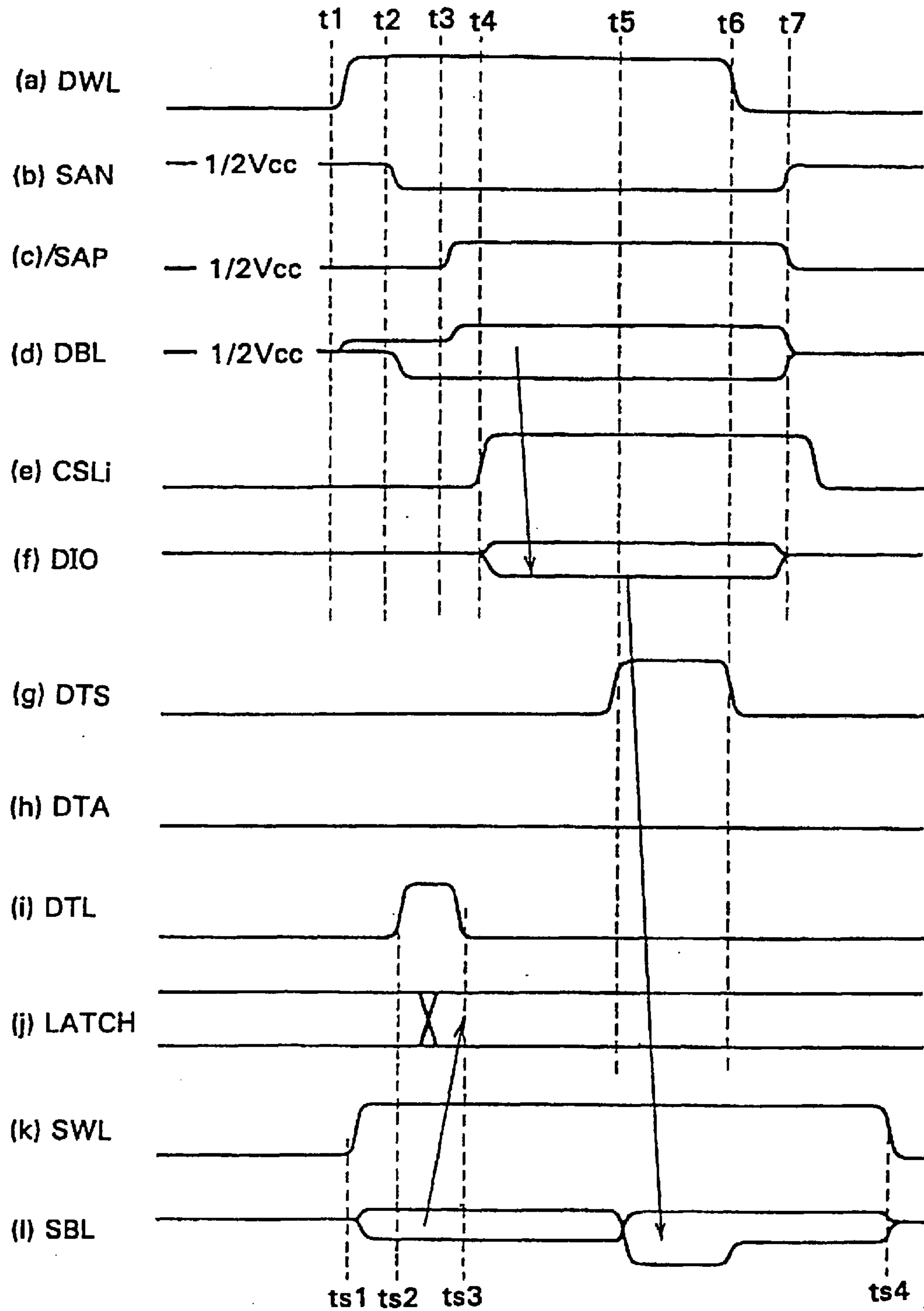


FIG. 69

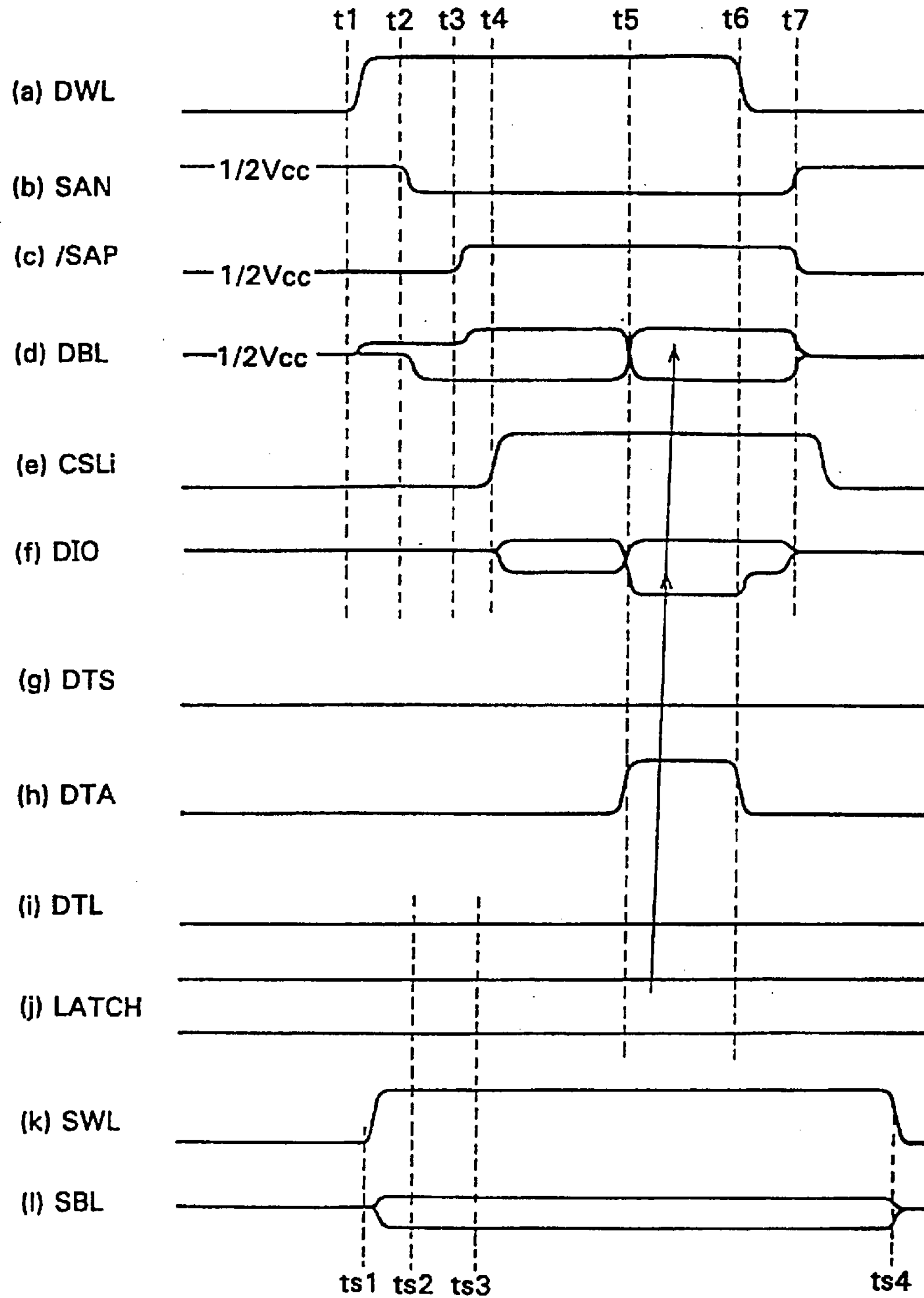


FIG. 70

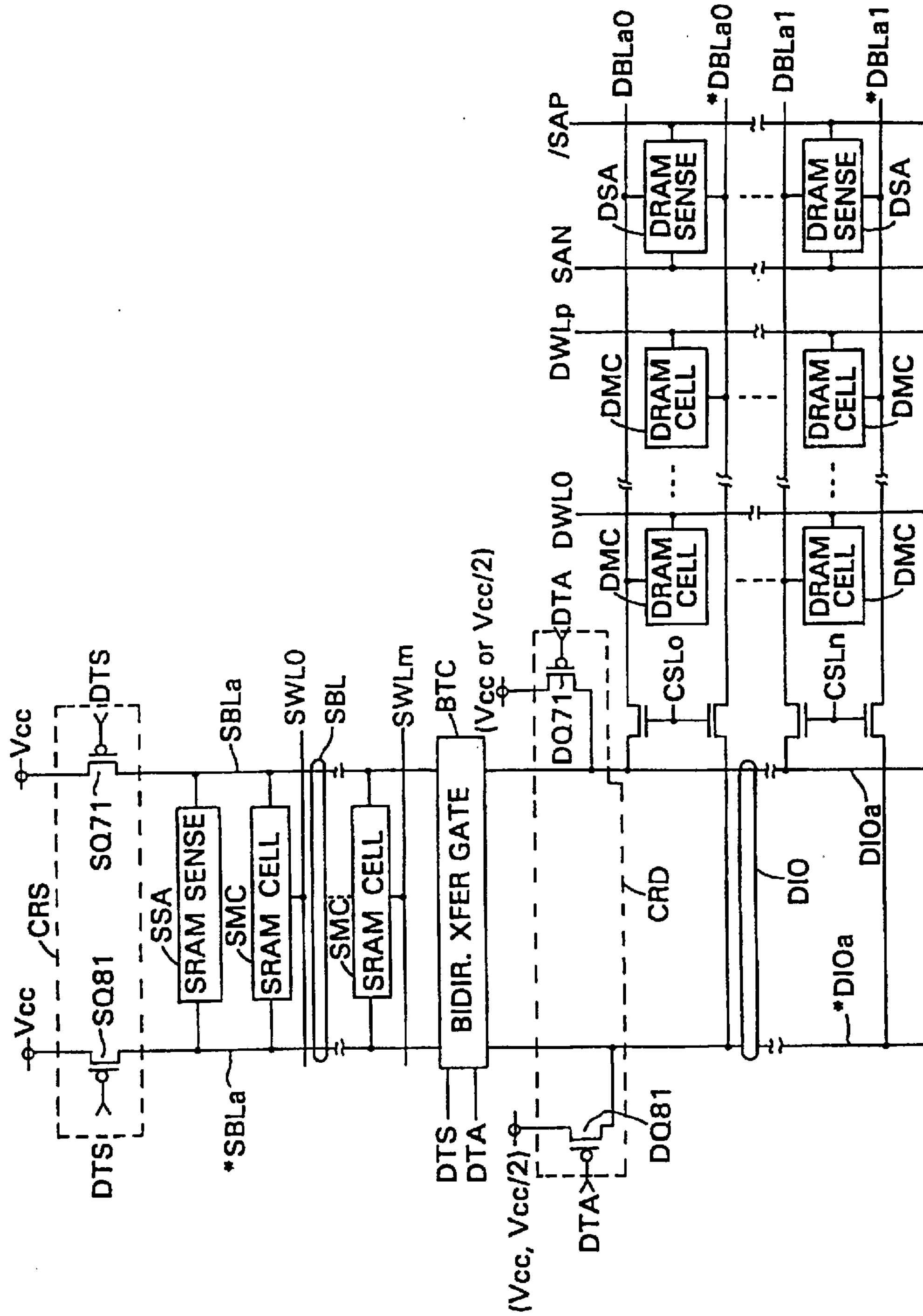


FIG. 71

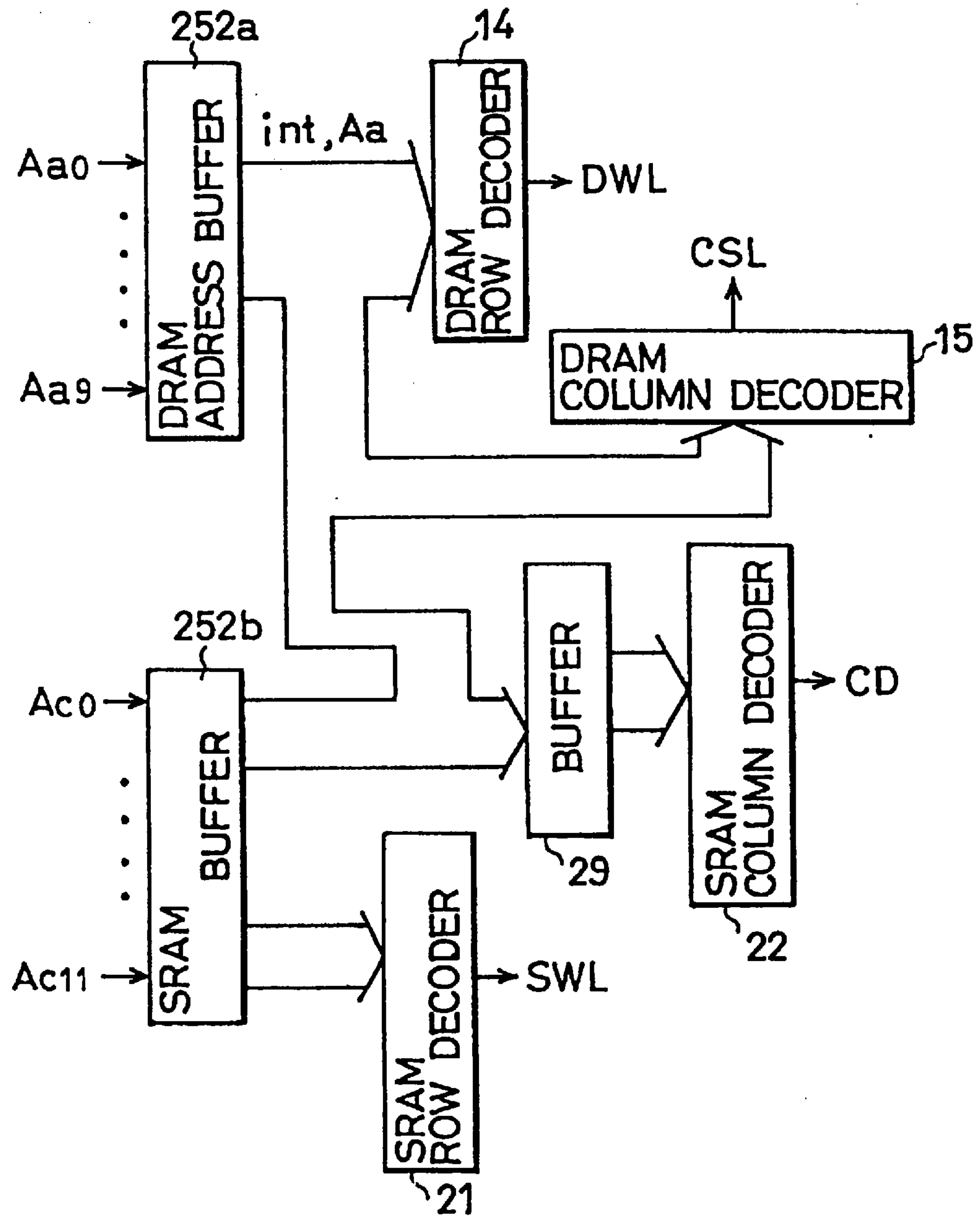


FIG. 72

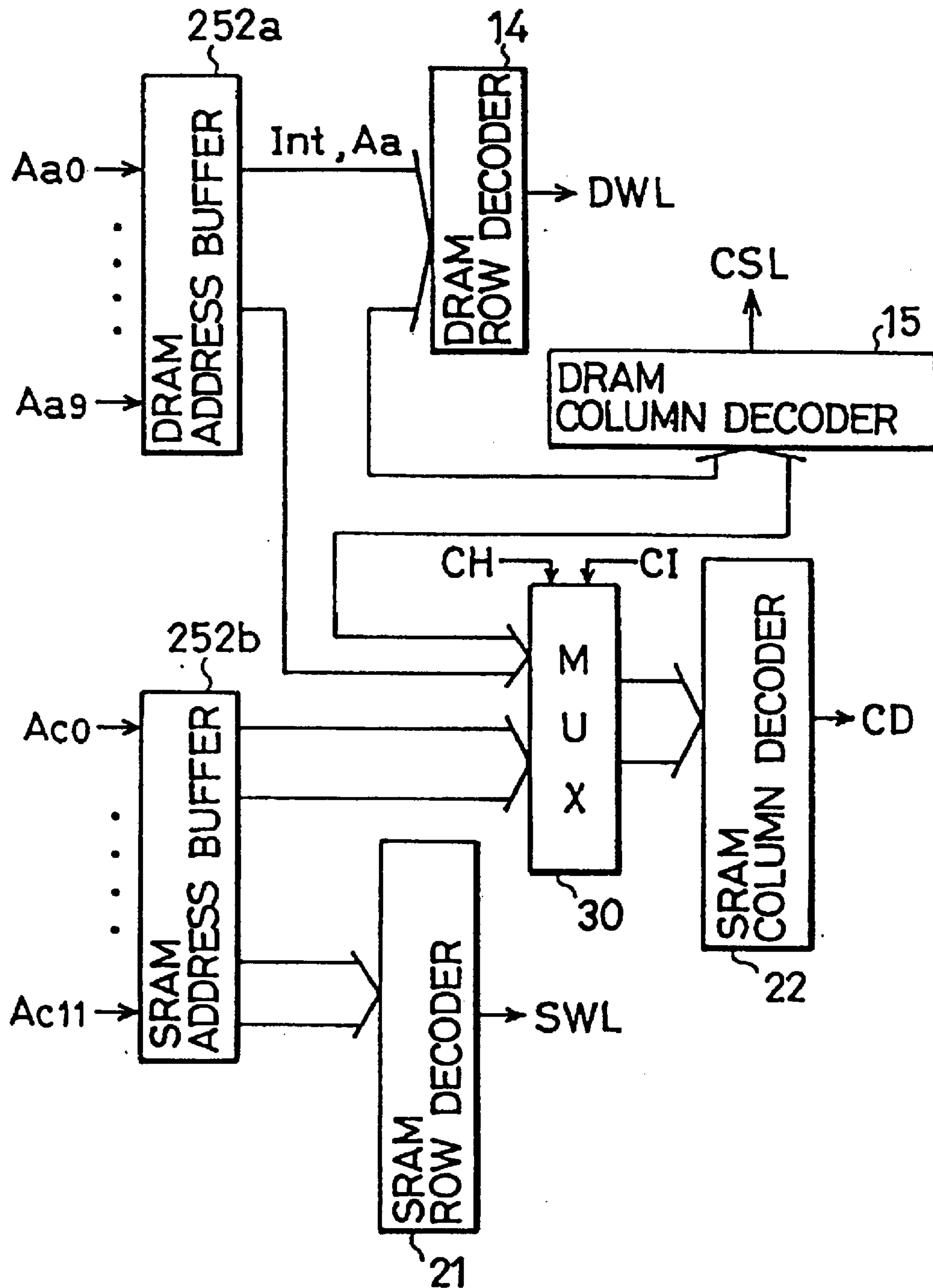


FIG. 73

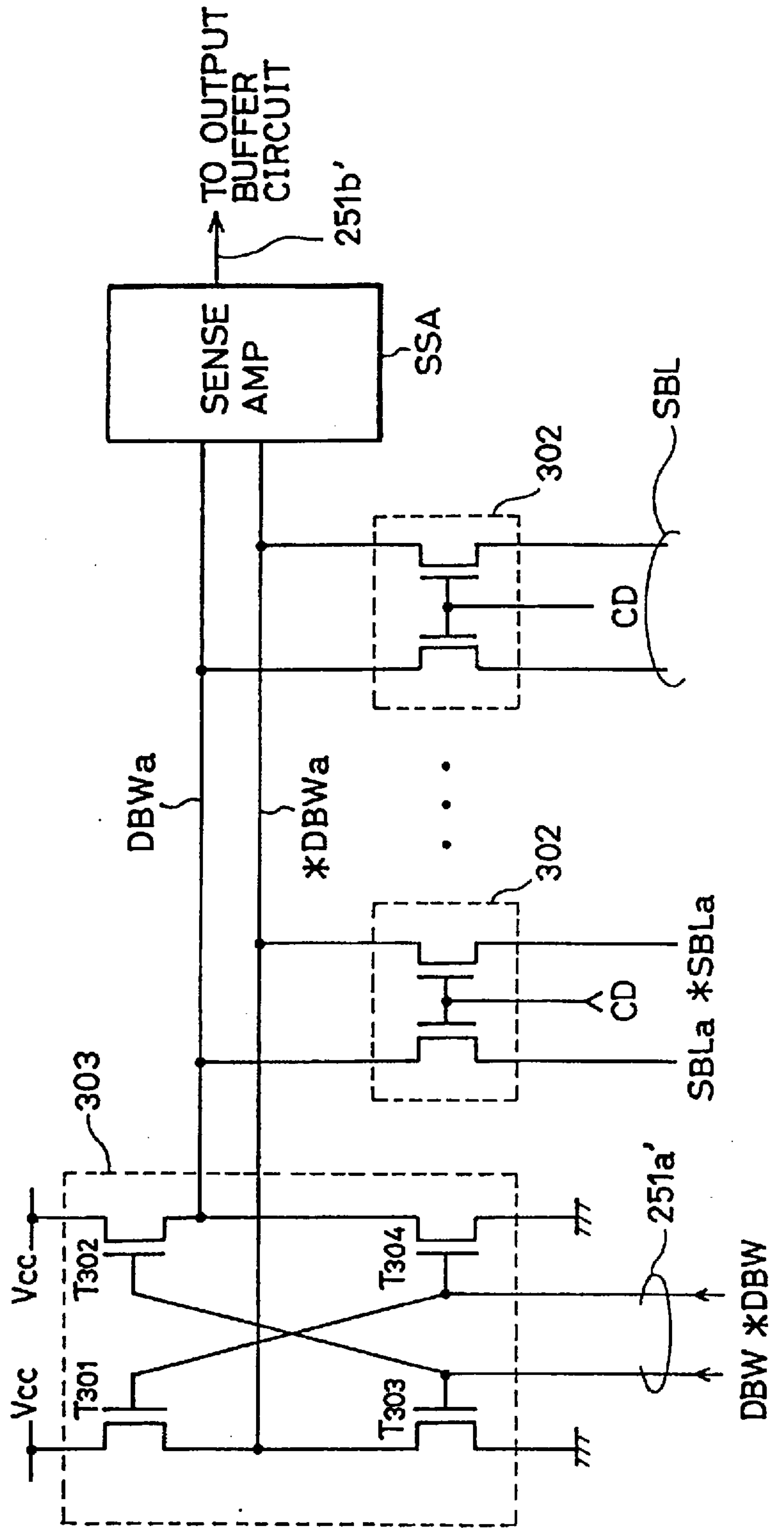


FIG. 74

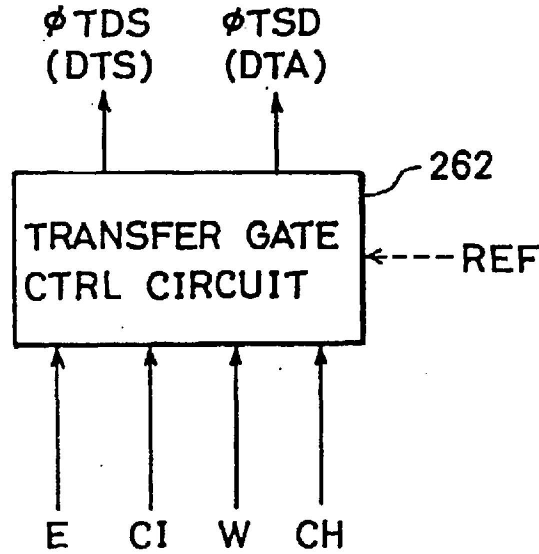


FIG. 75

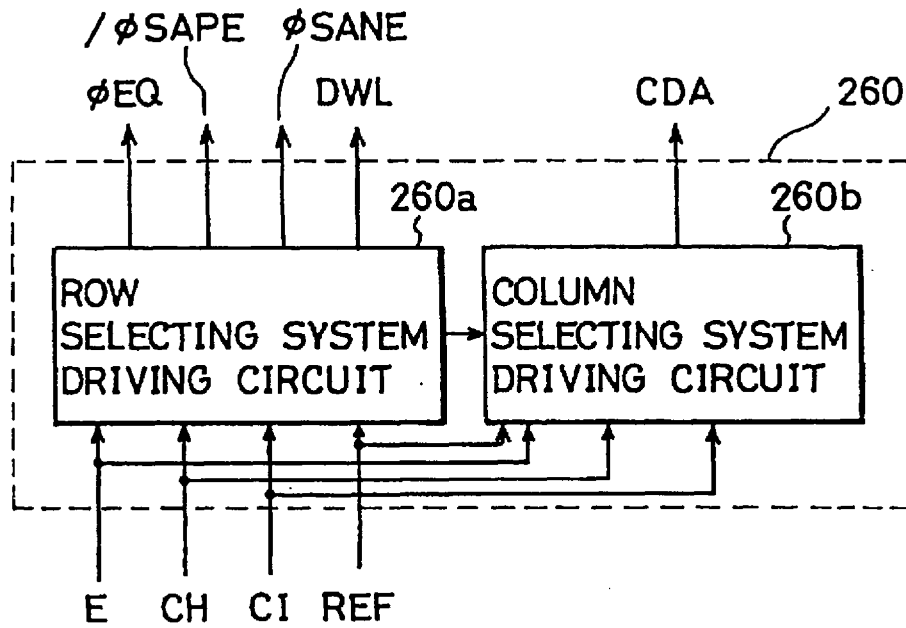


FIG. 76

OPERATION MODE	E#	CH#	CI#	CR#	W#	REF#
STAND-BY	H	X	X	X	X	H
ARRAY REFRESH	H	X	X	X	X	L
CPU ← CACHE	L	L	H	H	H	H
CPU → CACHE	L	L	H	H	L	H
CPU ← CACHE & ARRAY REFRESH	L	L	H	H	H	L
CPU → CACHE & ARRAY REFRESH	L	L	H	H	L	L
CPU ← ARRAY	L	X	L	H	H	H
CPU → ARRAY	L	X	L	H	L	H
CACHE ← ARRAY	L	H	H	H	H	H
CACHE → ARRAY	L	H	H	H	L	H
CPU ↔ COMMAND REGISTER	L	H	H	L	H/L	H
CPU ↔ COMMAND REGISTER & ARRAY REFRESH	L	H	H	L	H/L	L

FIG. 77

COMMAND REGISTER

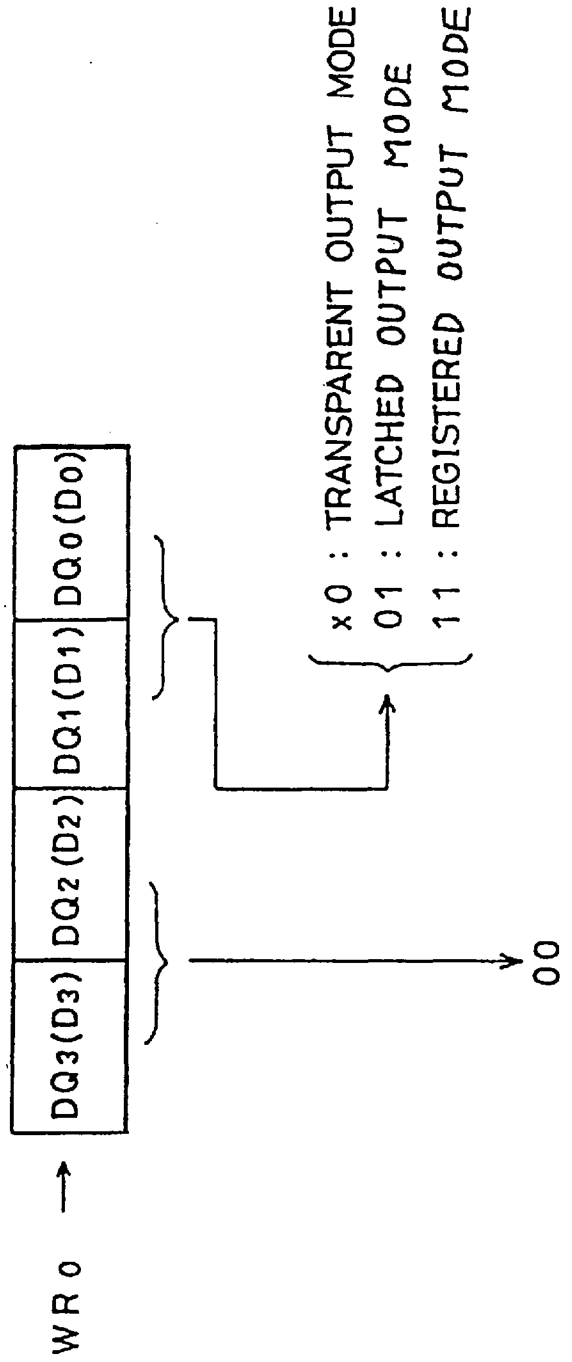
	Ar_0	Ar_1	W#
RR_0	0	0	H
RR_1	1	0	H
RR_2	0	1	H
RR_3	1	1	H
WR_0	0	0	L
WR_1	1	0	L
WR_2	0	1	L
WR_3	1	1	L

FIG. 78

RR_0 → MASKED WRITE MODE (DEFAULT)

RR_1 → D/Q SEPARATION MODE

WR_0 →



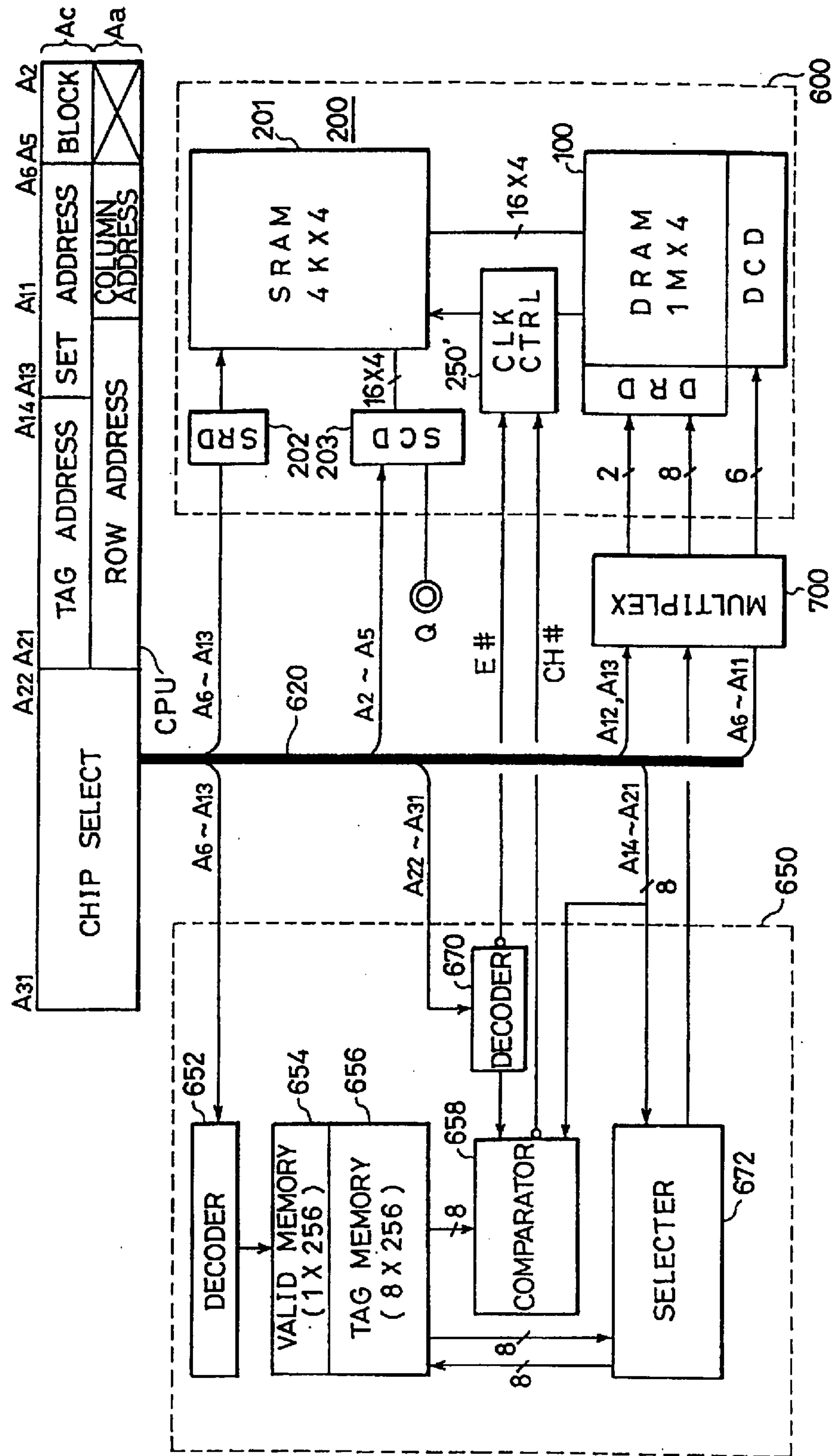


FIG. 79
CHIP SELECT
TAG ADDRESS
SET
ADDRESS
BLOCK
ROW ADDRESS
COLUMN ADDRESS
A31
A22 A21
A14 A13
A11
A6 A5
A2
Ac
Aa
CPU
620
A6 ~ A13
A2 ~ A5
Q
E #
CH #
A12, A13
A6 ~ A11
A22 ~ A31
A14 ~ A21
SRAM 4KX4
201
200
SRD
202
SCD
203
16X4
250'
CLK CTRL
DRAM 1MX4
100
DCD
DRD
600
MULTIPLEX
700
DECODER
652
VALID MEMORY (1 X 256)
654
TAG MEMORY (8 X 256)
656
COMPARATOR
658
670
SELECTER
672
650

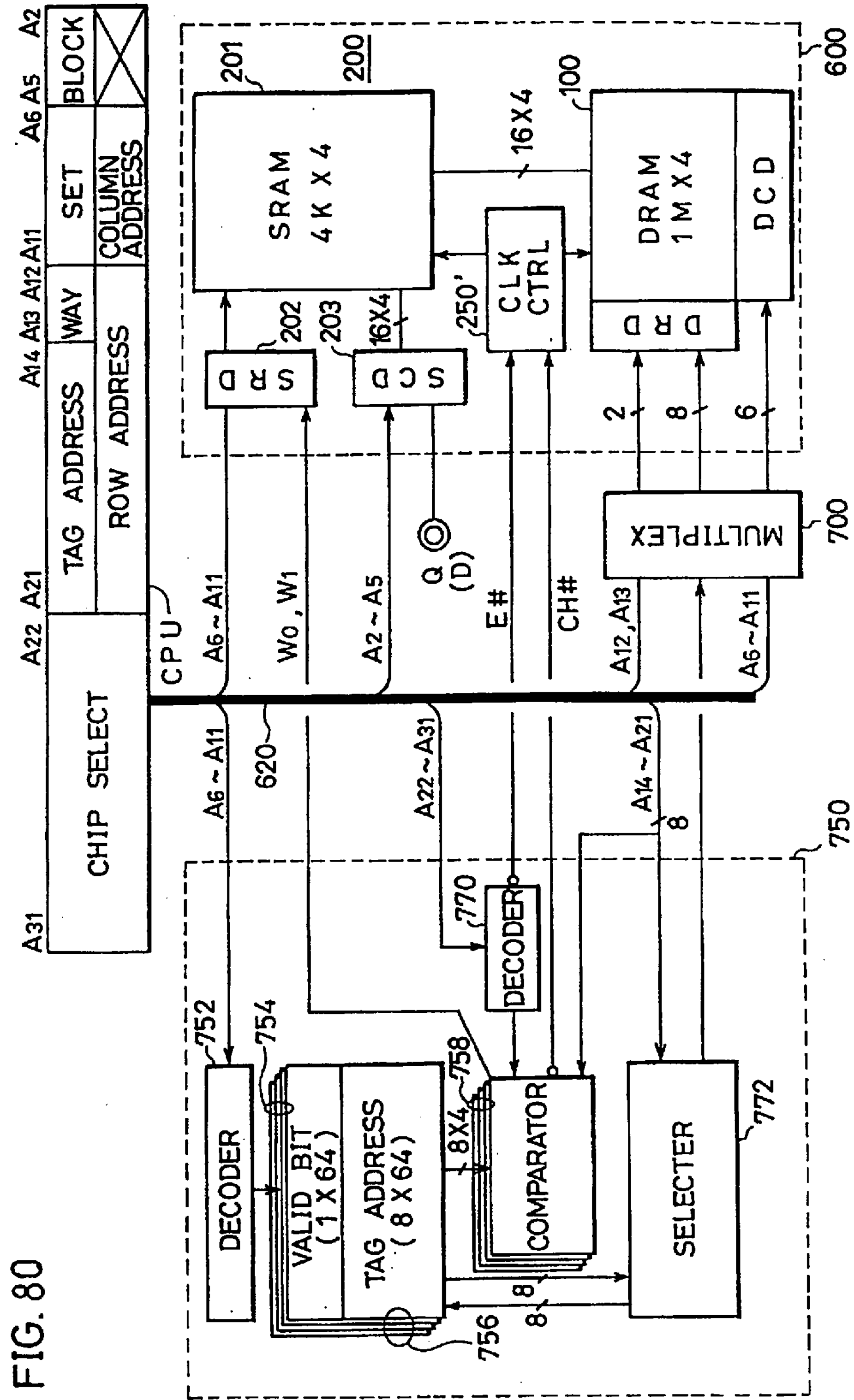


FIG. 80
A31
A22
A21
A14 A13 A12 A11
A6 A5
A2
CHIP SELECT
TAG ADDRESS
ROW ADDRESS
WAY
SET
COLUMN ADDRESS
BLOCK
CPU
A6~A11
W0, W1
A2~A5
Q (D)
E#
CH#
A12, A13
A6~A11
620
A22~A31
A14~A21
8
600
200
201
SRAM 4 K X 4
16X4
100
DRAM 1 M X 4
DCD
CLK CTRL
250'
202
203
16X4
SRD
SCD
DRD
2
8
6
MULTIPLEX
700
750
770
DECODER
752
754
DECODER
VALID BIT (1 X 64)
TAG ADDRESS (8 X 64)
758
8X4
COMPARATOR
SELECTER
772
756
8
8

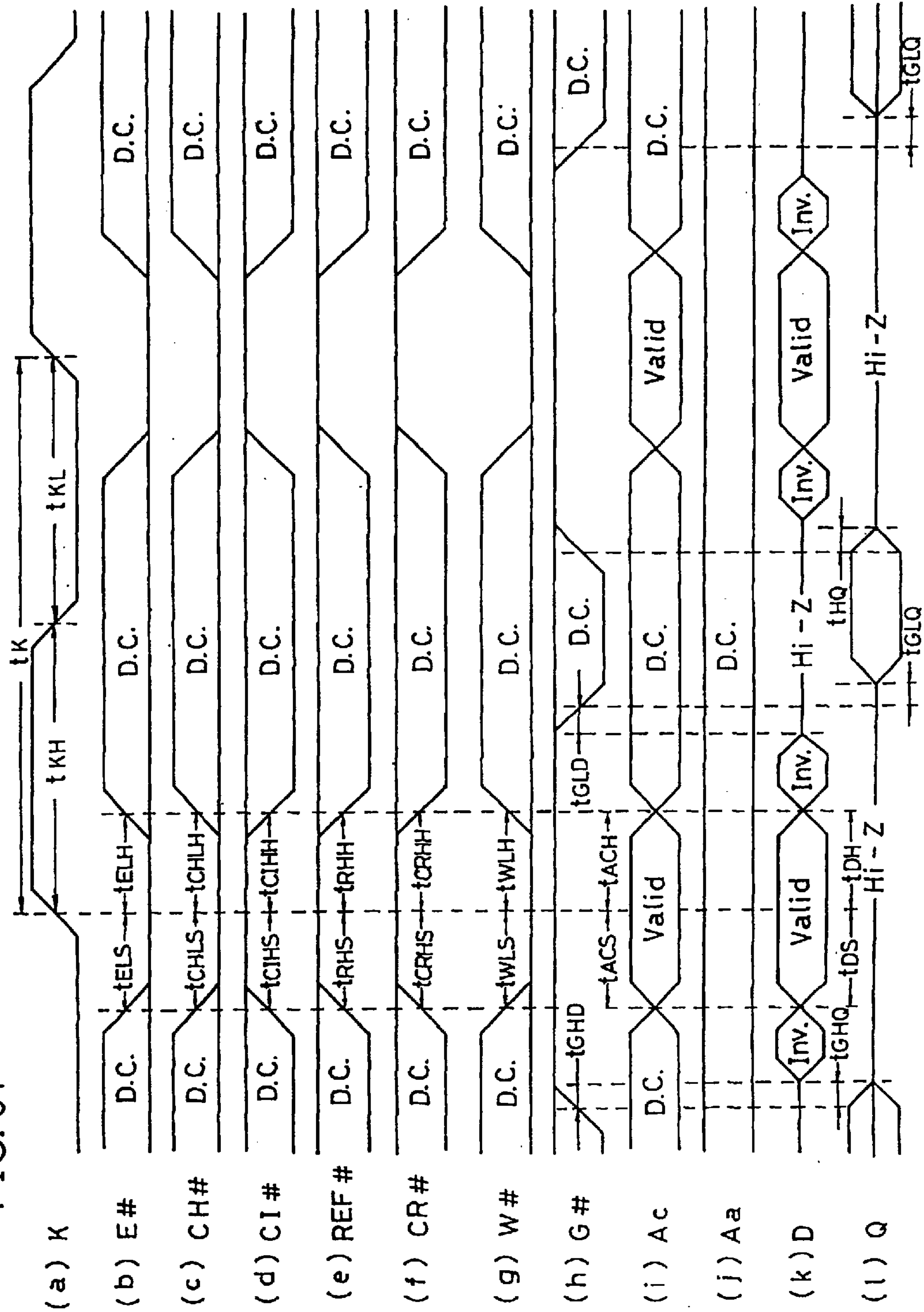


FIG. 81
CACHE HIT WRITE
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
tK
tKH
tKL
tELS
tELH
tCHLS
tCHLH
tCIHS
tCIHH
tRHS
tRHH
tCRHS
tCRHH
tWLS
tWLH
tGHD
tGLD
tACS
tACH
tGHQ
tDS
tDH
tHQ
tGLQ
D.C.
Valid
Inv.
Hi-Z

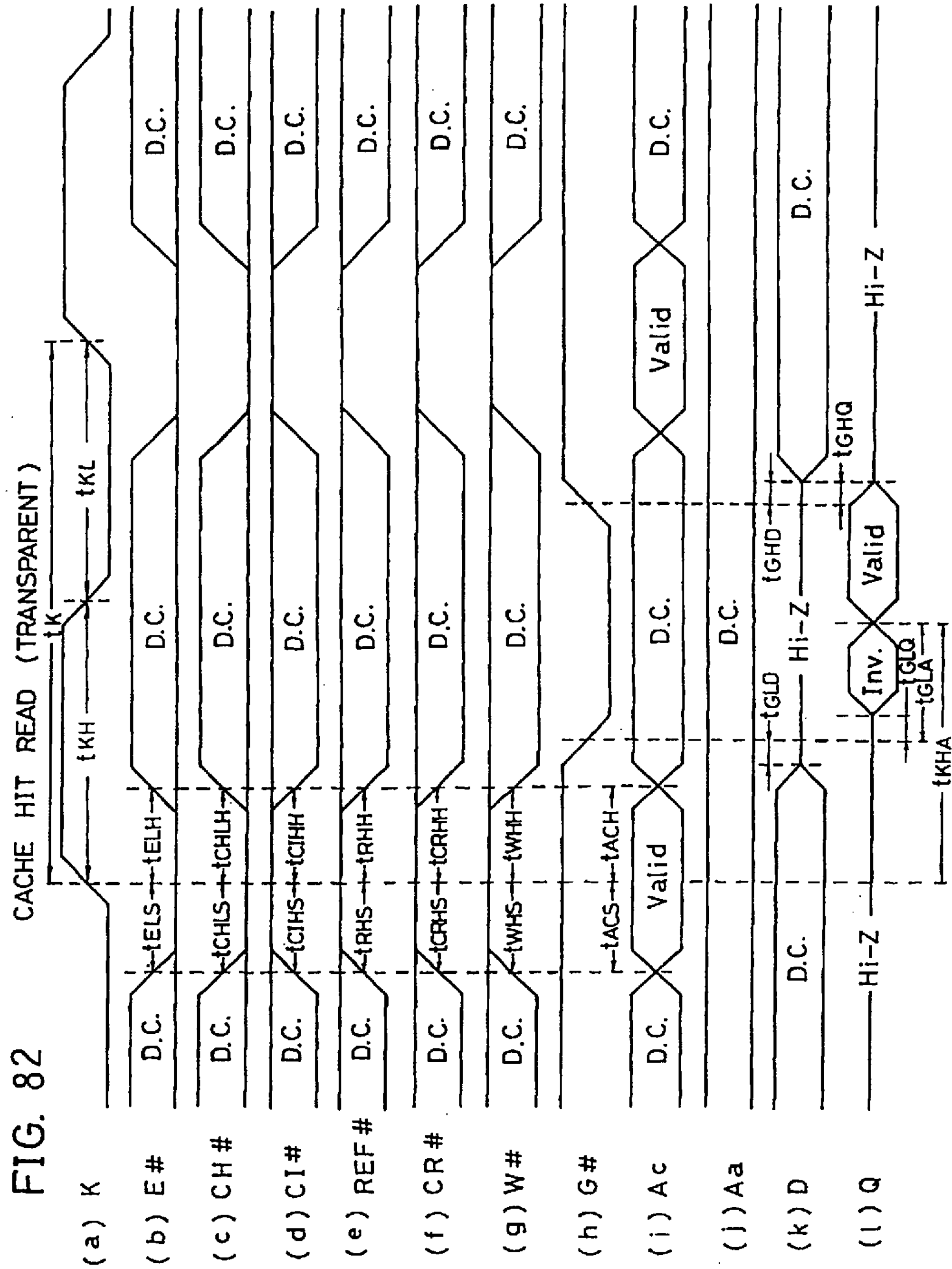


FIG. 82
CACHE HIT READ (TRANSPARENT)
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
tK
tKH
tKL
tELS
tELH
tCHLS
tCHLH
tCIHS
tCIHH
tRHS
tRHH
tCRHS
tCRHH
tWHS
tWHH
tACS
tACH
tGLD
tGHD
tGHQ
tGLQ
tGLA
tKHA
D.C.
Valid
Hi-Z
Inv.

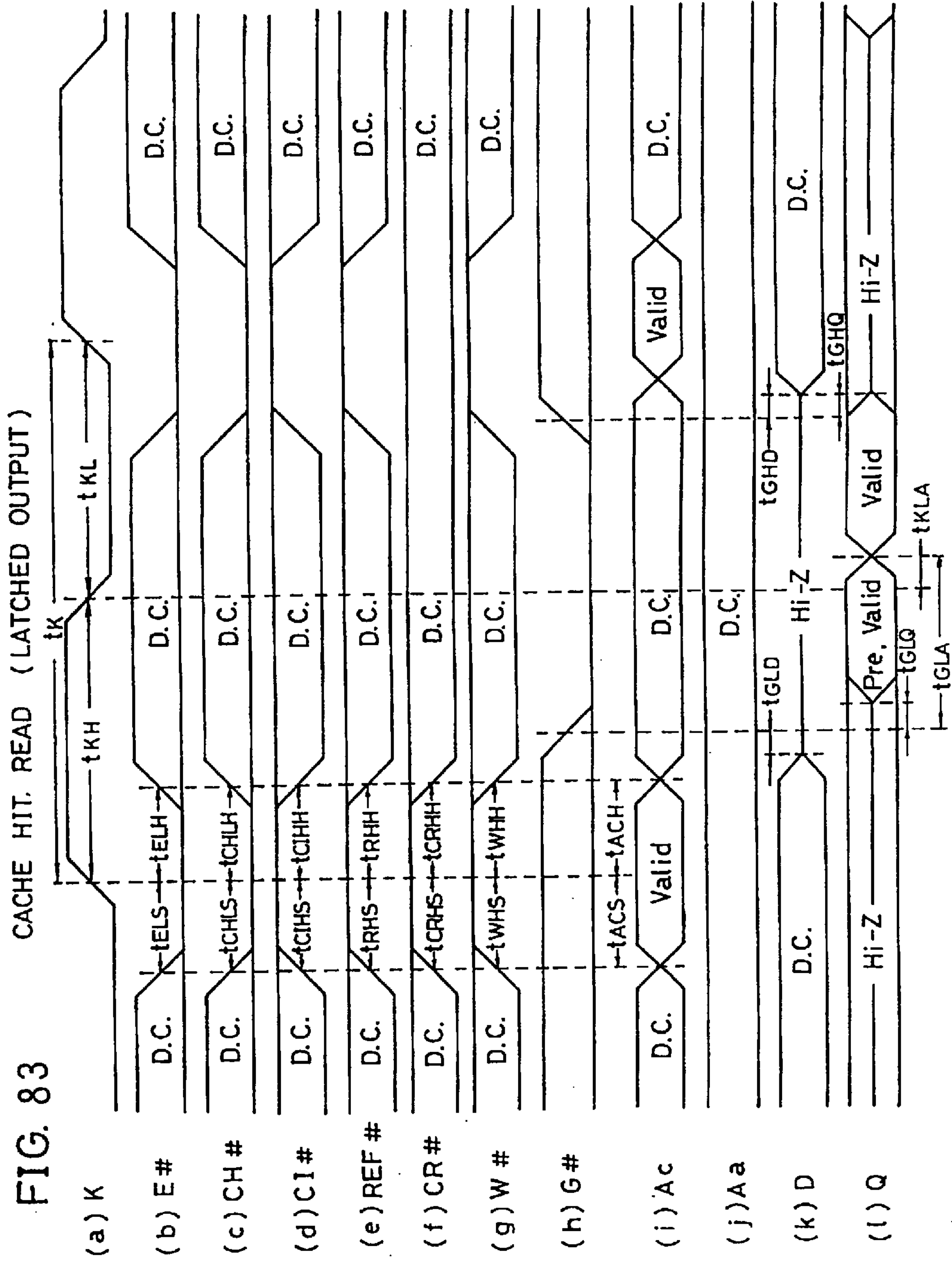


FIG. 83
CACHE HIT. READ (LATCHED OUTPUT)
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
tK
tKH
tKL
tELS
tELH
tCHLS
tCHLH
tCIHS
tCIHH
tRHS
tRHH
tCRHS
tCRHH
tWHS
tWHH
tACS
tACH
tGLD
tGHD
tGHQ
tGLQ
tKLA
tGLA
D.C.
Valid
Hi-Z
Pre. Valid

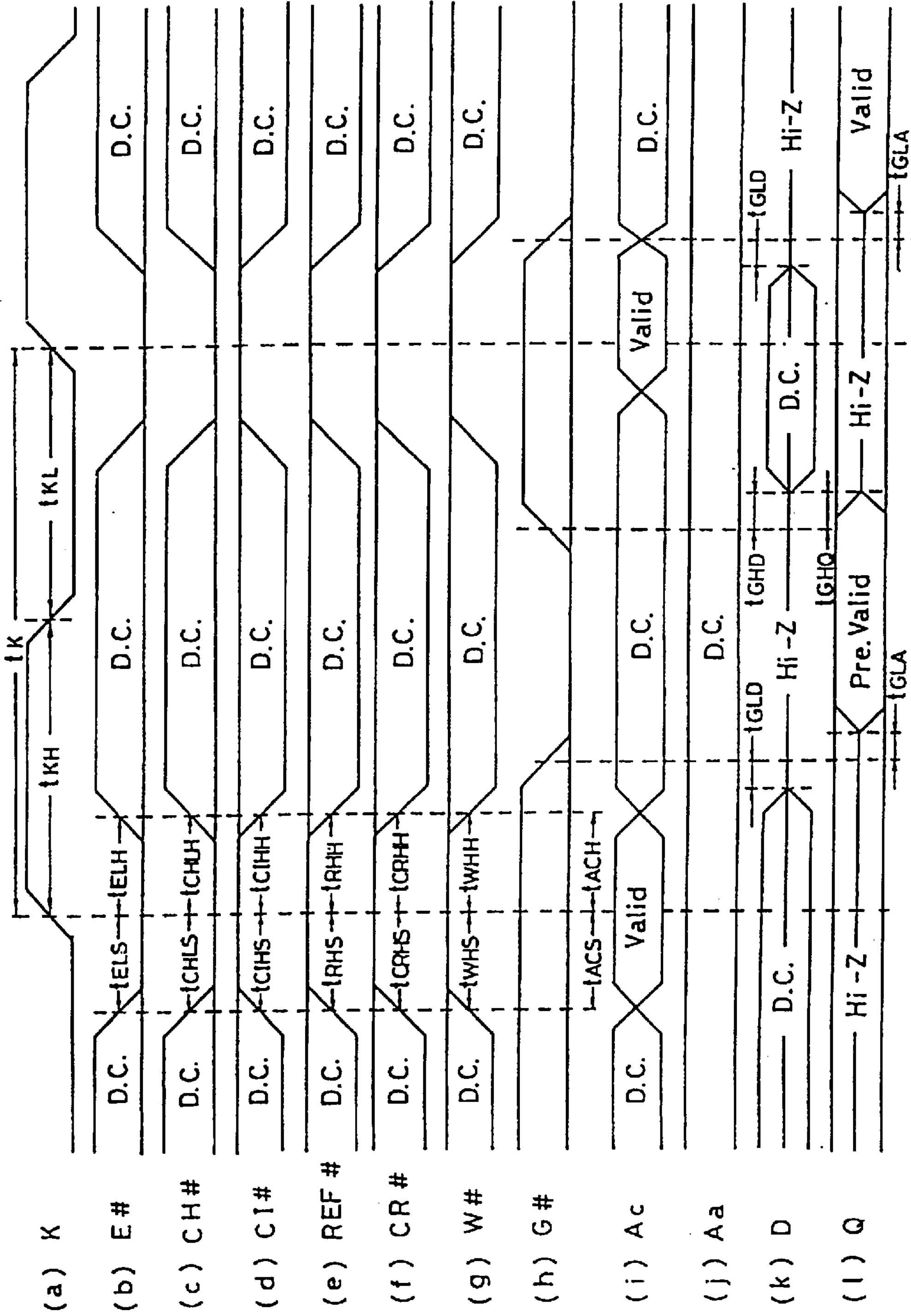


FIG. 84
CACHE HIT READ (REGISTERED OUTPUT)
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
tK
tKH
tKL
tELS
tELH
tCHLS
tCHLH
tCIHS
tCIHH
tRHS
tRHH
tCRHS
tCRHH
tWHS
tWHH
tACS
tACH
tGLD
tGHD
tGHQ
tGLA
D.C.
Valid
Hi-Z
Pre. Valid

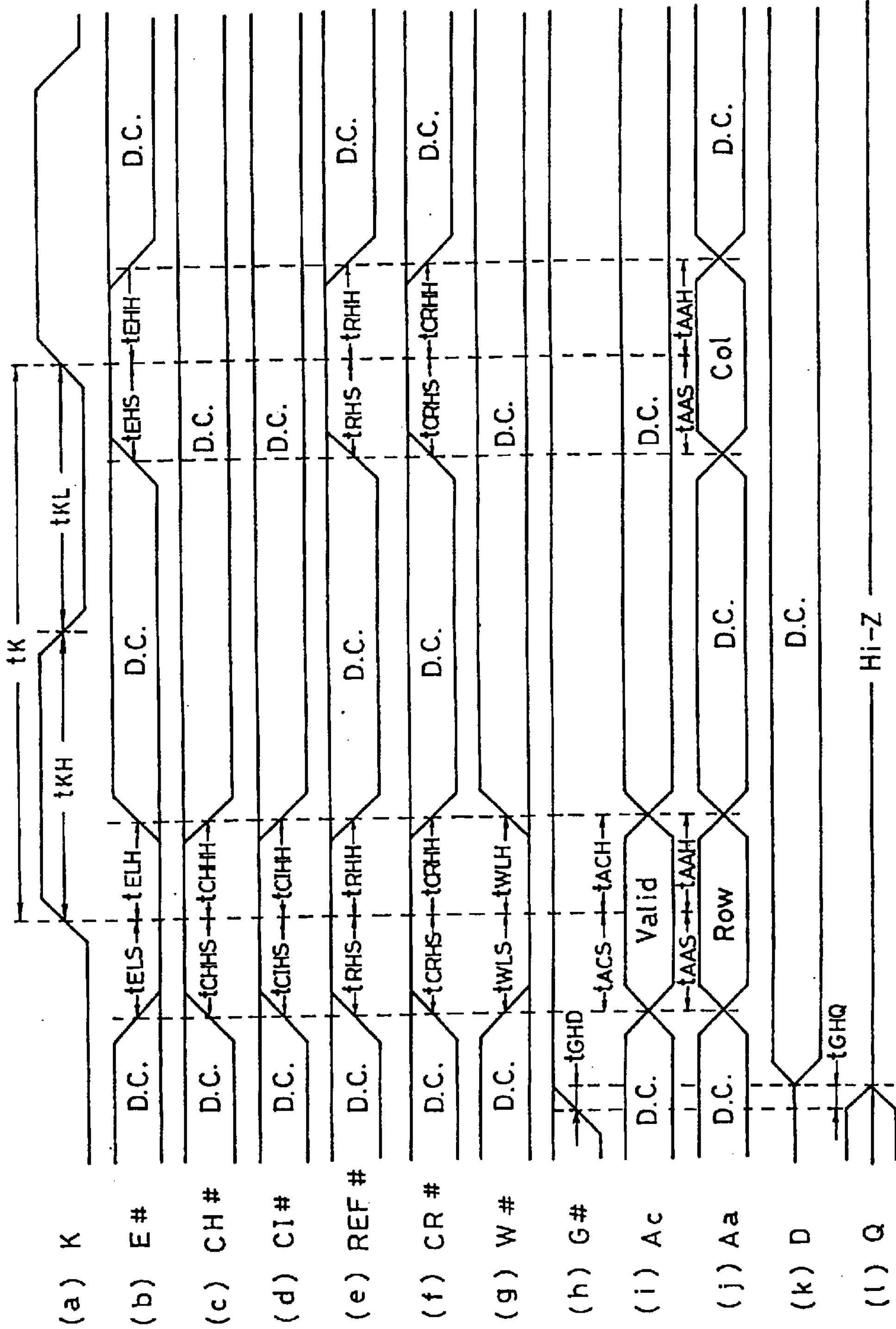


FIG. 85
COPY BACK (SRAM TO DRAM)
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
tK
tKH
tKL
tELS
tELH
tEHS
tEHH
tCHHS
tCHHH
tCIHS
tCIHH
tRHS
tRHH
tCRHS
tCRHH
tWLS
tWLH
tGHD
tACS
tACH
tAAS
tAAH
tGHQ
D.C.
Valid
Row
Col
Hi-Z

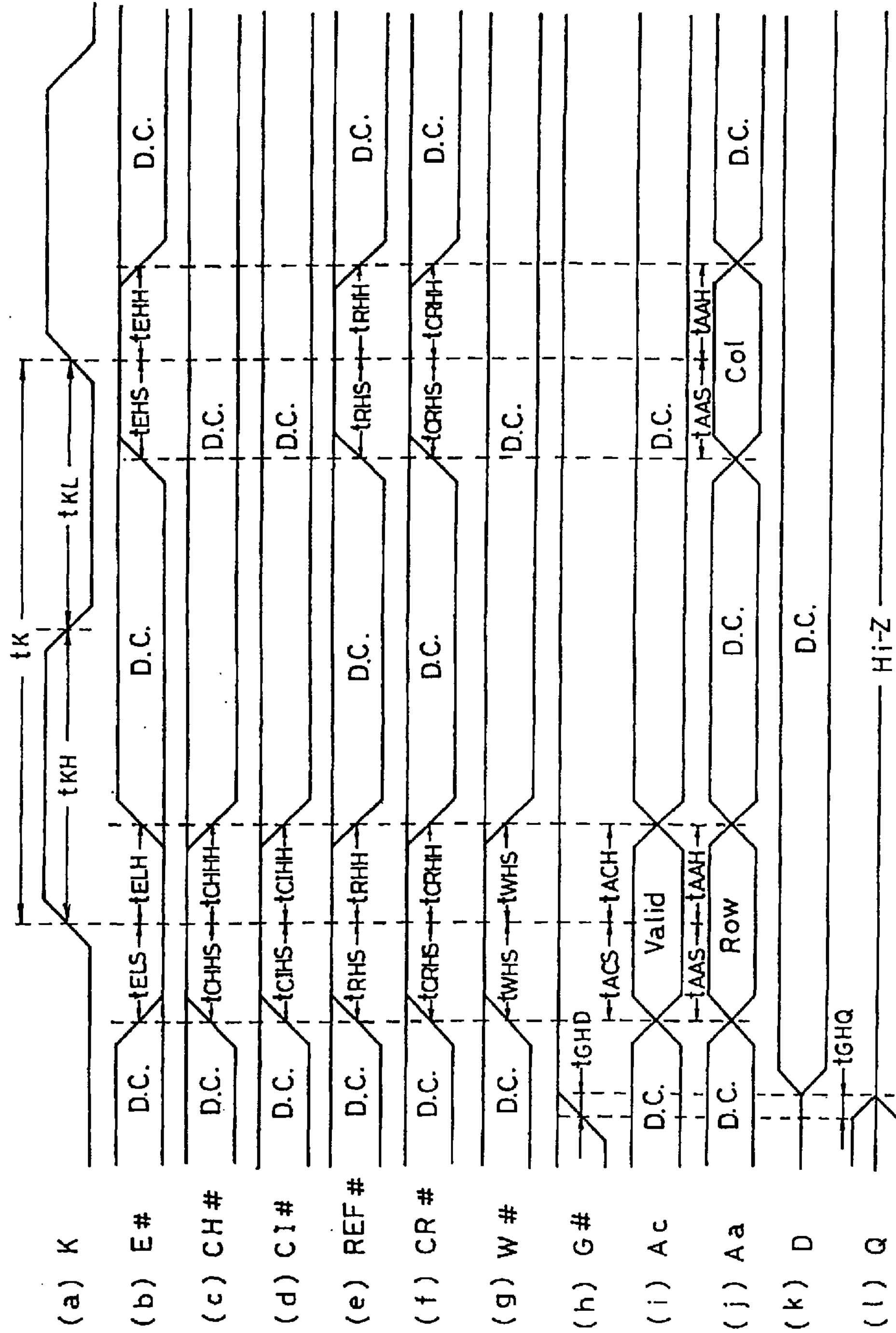


FIG. 86
BLOCK TRANSFER (DRAM TO SRAM)
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
tK
tKH
tKL
tELS
tELH
tEHS
tEHH
tCHHS
tCHHH
tCIHS
tCIHH
tRHS
tRHH
tCRHS
tCRHH
tWHS
tGHD
tACS
tACH
tAAS
tAAH
tGHQ
D.C.
Valid
Row
Col
Hi-Z

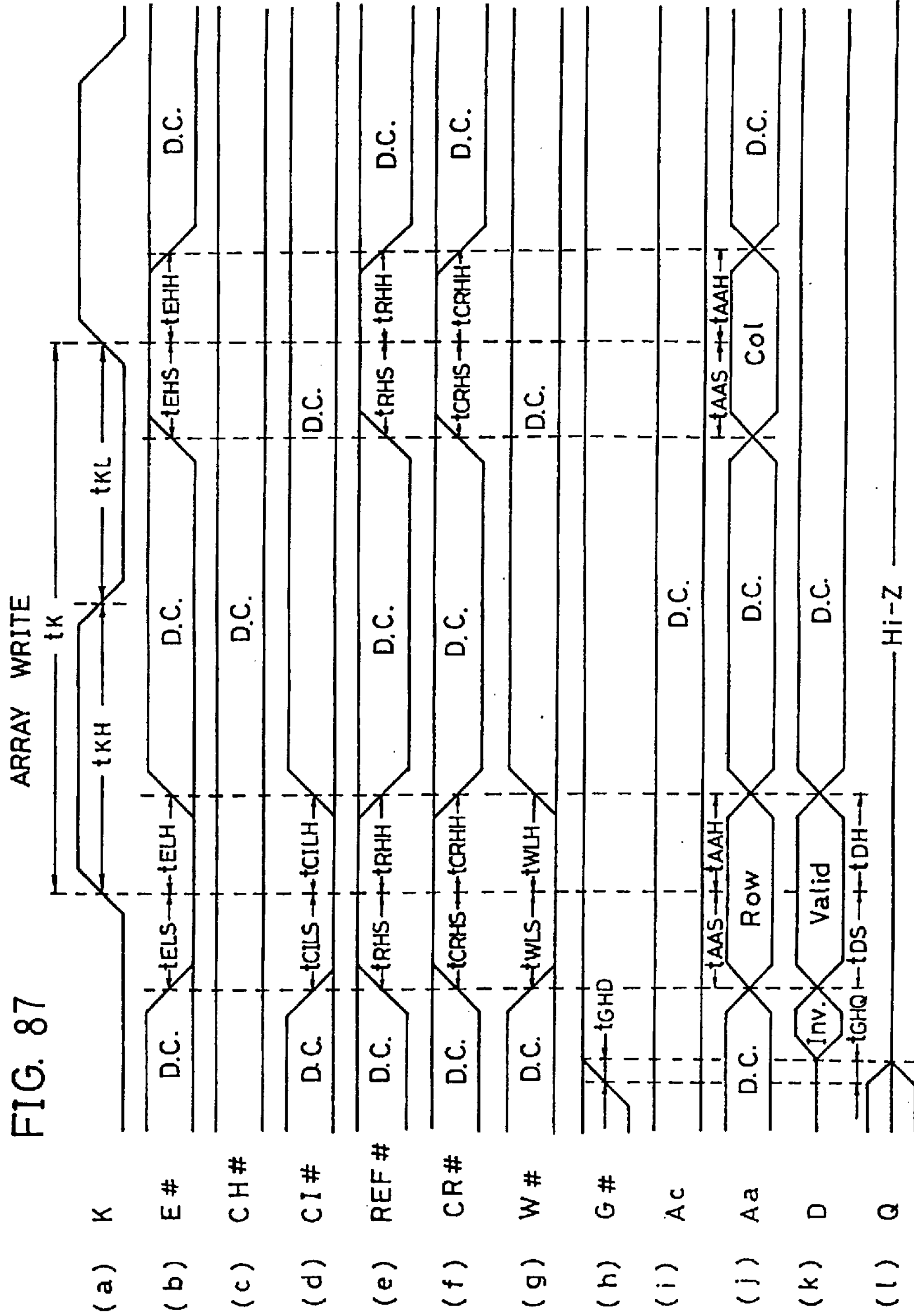


FIG. 87
ARRAY WRITE
tK
tKH
tKL
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
D.C.
tELS
tELH
tEHS
tEHH
tCILS
tCILH
tRHS
tRHH
tCRHS
tCRHH
tWLS
tWLH
tGHD
tAAS
tAAH
Row
Col
Inv.
Valid
tGHQ
tDS
tDH
Hi-Z

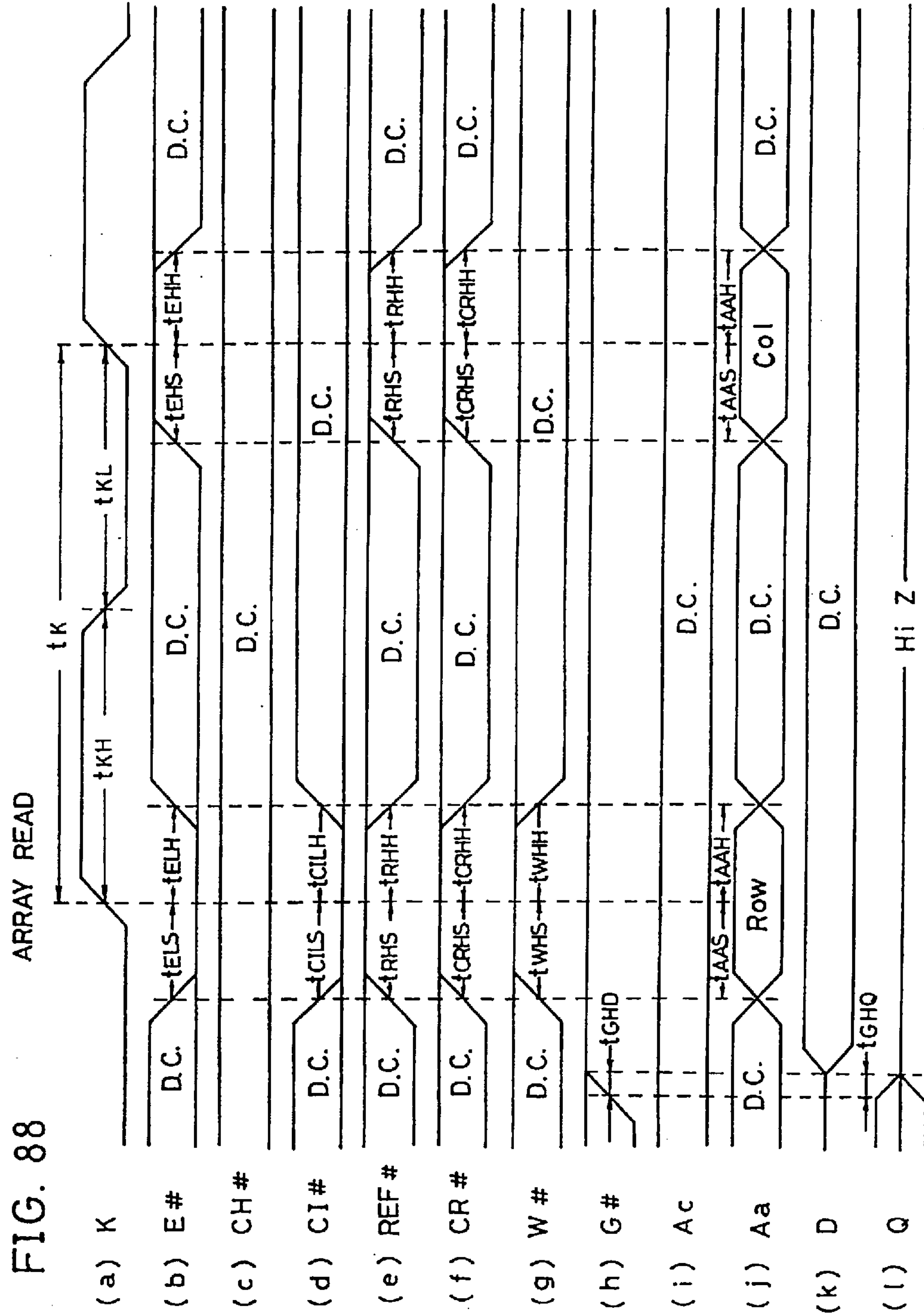


FIG. 88
ARRAY READ
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
tK
tKH
tKL
tELS
tELH
tEHS
tEHH
tCILS
tCILH
tRHS
tRHH
tCRHS
tCRHH
tWHS
tWHH
tGHD
tAAS
tAAH
Row
Col
tGHQ
D.C.
Hi Z

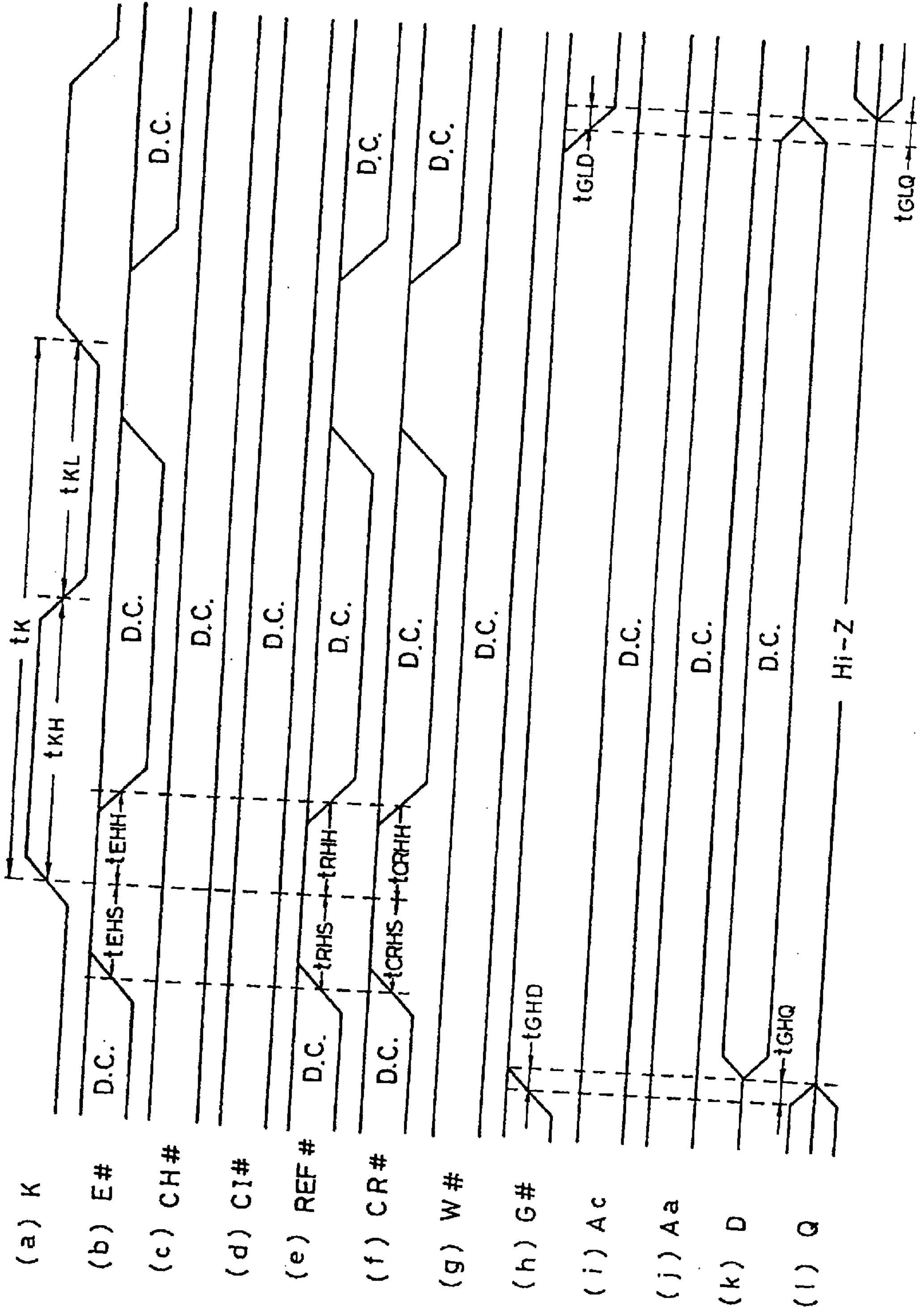


FIG. 89
ARRAY ACTIVE CYCLE
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
tK
tKH
tKL
tEHS
tEHH
tRHS
tRHH
tCRHS
tCRHH
tGHD
tGHQ
tGLD
tGLQ
D.C.
Hi-Z

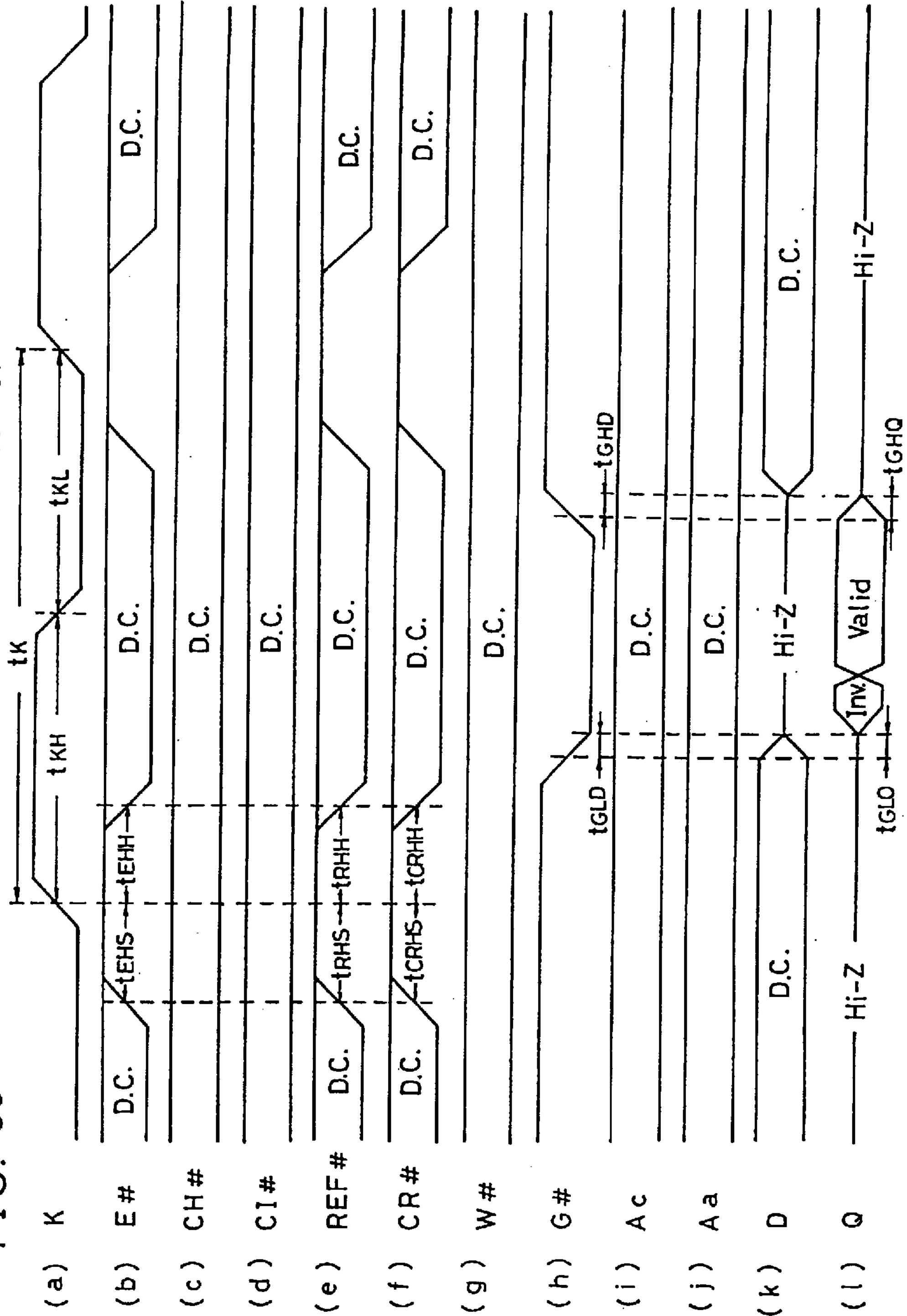


FIG. 90
ARRAY ACTIVE WITH TRANSPARENT OUTPUT
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
tK
tKH
tKL
tEHS
tEHH
tRHS
tRHH
tCRHS
tCRHH
tGLD
tGHD
tGLQ
tGHQ
D.C.
Hi-Z
Inv.
Valid

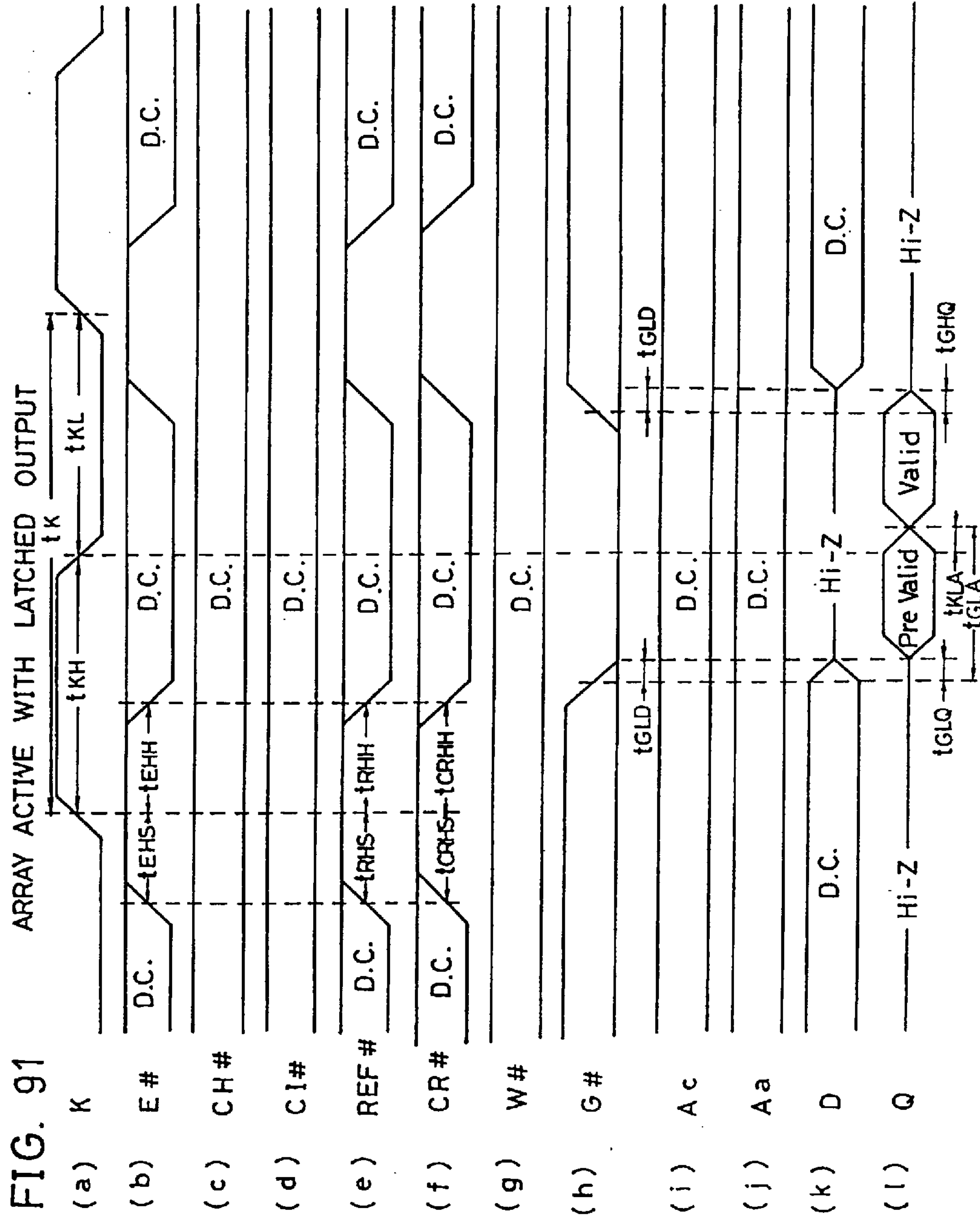


FIG. 91
ARRAY ACTIVE WITH LATCHED OUTPUT
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
tK
tKH
tKL
tEHS
tEHH
tRHS
tRHH
tCRHS
tCRHH
tGLD
tGLQ
tKLA
tGLA
tGHQ
D.C.
Hi-Z
Pre Valid
Valid

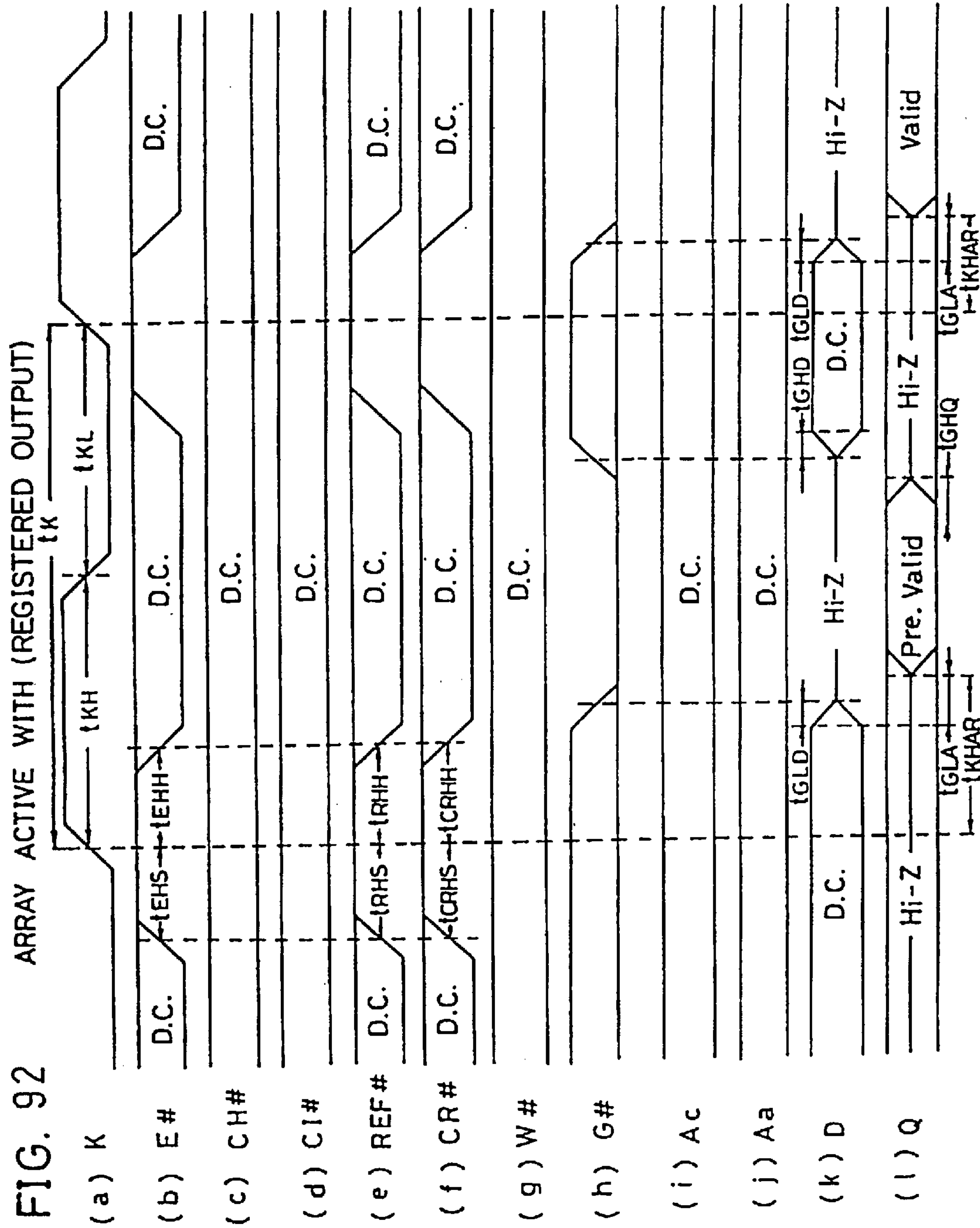


FIG. 92
ARRAY ACTIVE WITH (REGISTERED OUTPUT)
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
tK
tKH
tKL
tEHS
tEHH
tRHS
tRHH
tCRHS
tCRHH
tGLD
tGHD
tGHQ
tGLA
tKHAR
D.C.
Hi-Z
Pre. Valid
Valid

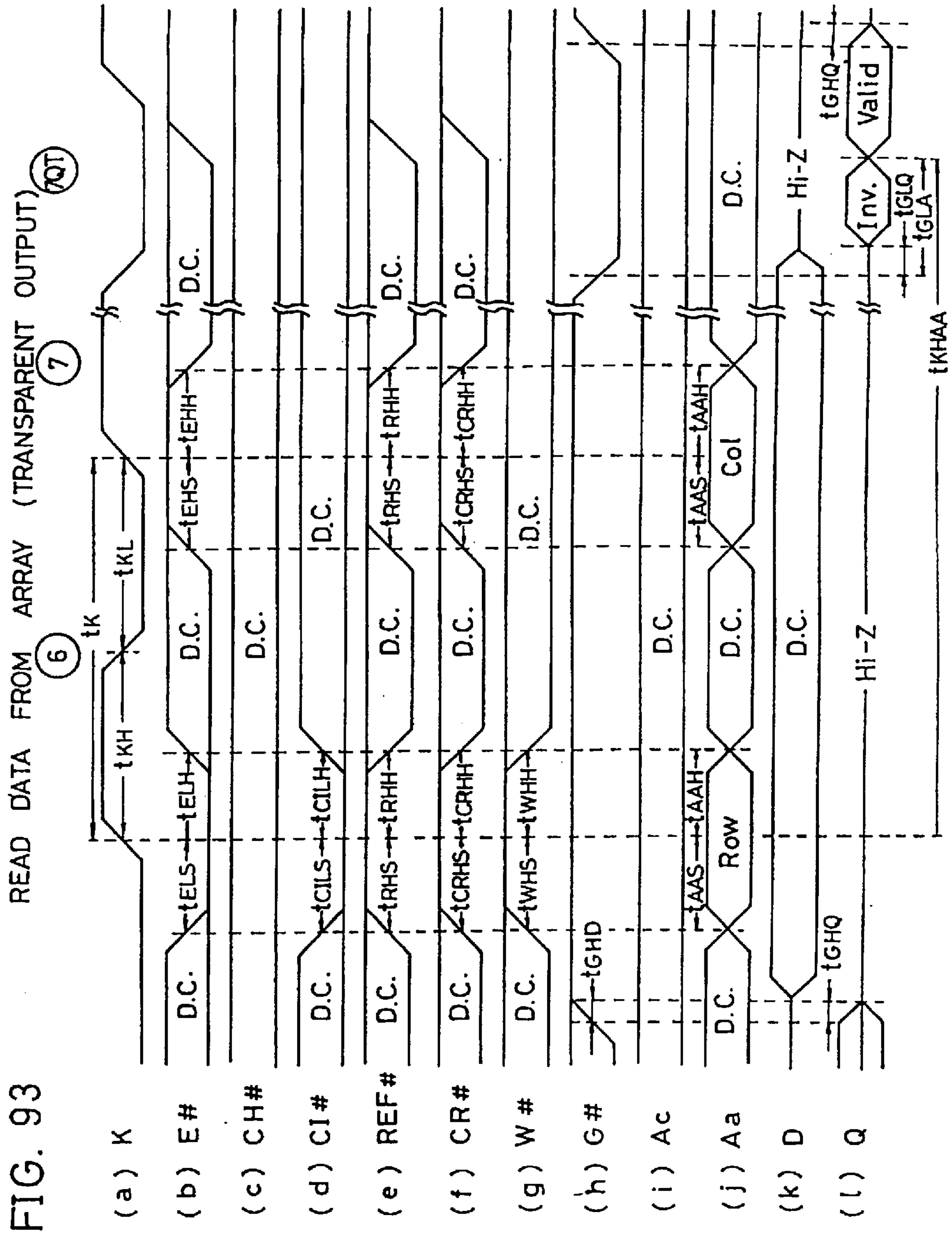


FIG. 93
READ DATA FROM ARRAY (TRANSPARENT OUTPUT)
6
7
7QT
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
tK
tKH
tKL
tELS
tELH
tEHS
tEHH
tCILS
tCILH
tRHS
tRHH
tCRHS
tCRHH
tWHS
tWHH
tGHD
tAAS
tAAH
tGHQ
tGLQ
tGLA
tKHAA
D.C.
Row
Col
Hi-Z
Inv.
Valid

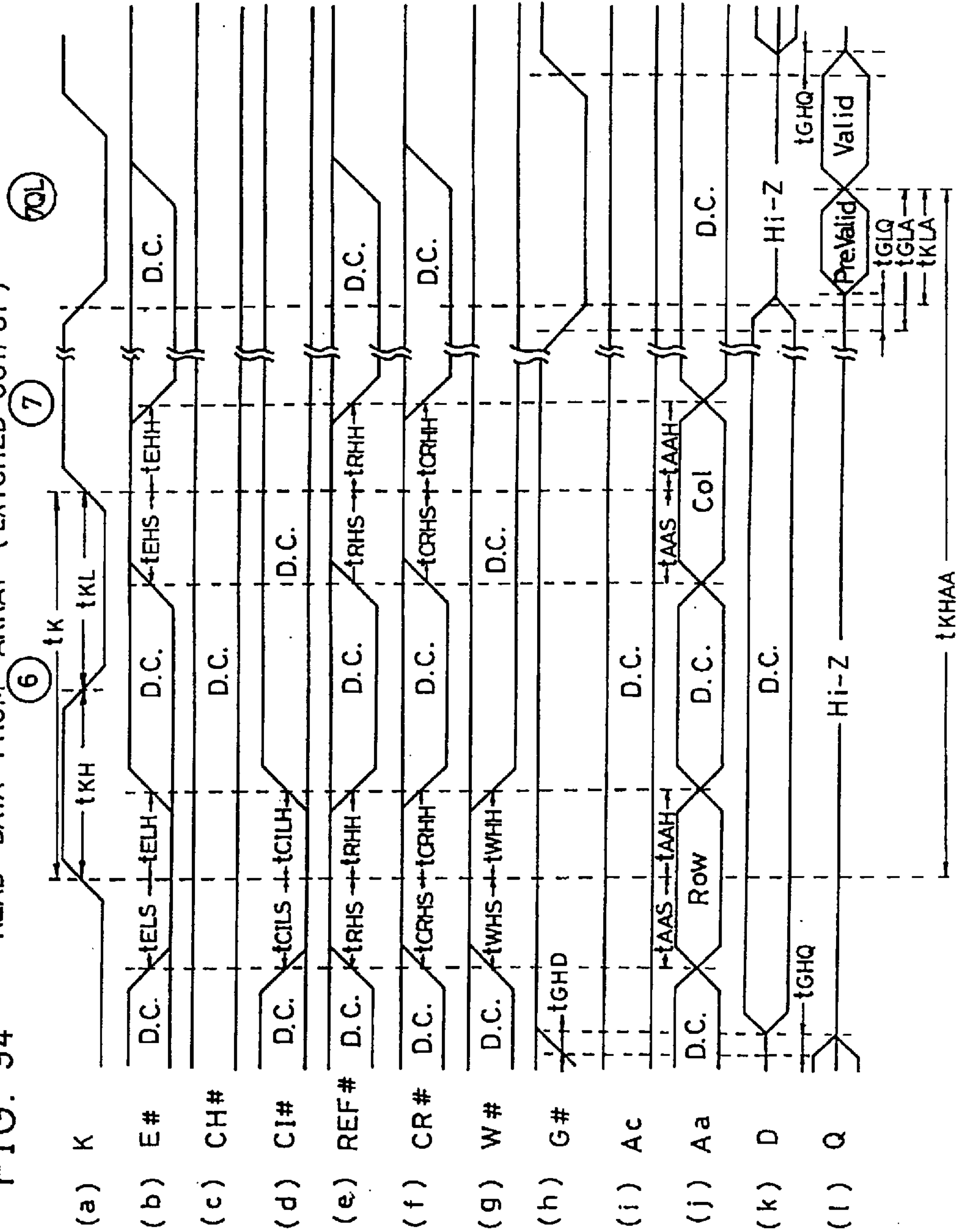


FIG. 94
READ DATA FROM ARRAY (LATCHED OUTPUT)
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
6
7
7QL
tK
tKH
tKL
tELS
tELH
tEHS
tEHH
tCILS
tCILH
tRHS
tRHH
tCRHS
tCRHH
tWHS
tWHH
tGHD
tAAS
tAAH
Row
Col
D.C.
Hi-Z
Pre.Valid
Valid
tGHQ
tGLQ
tGLA
tKLA
tKHAA

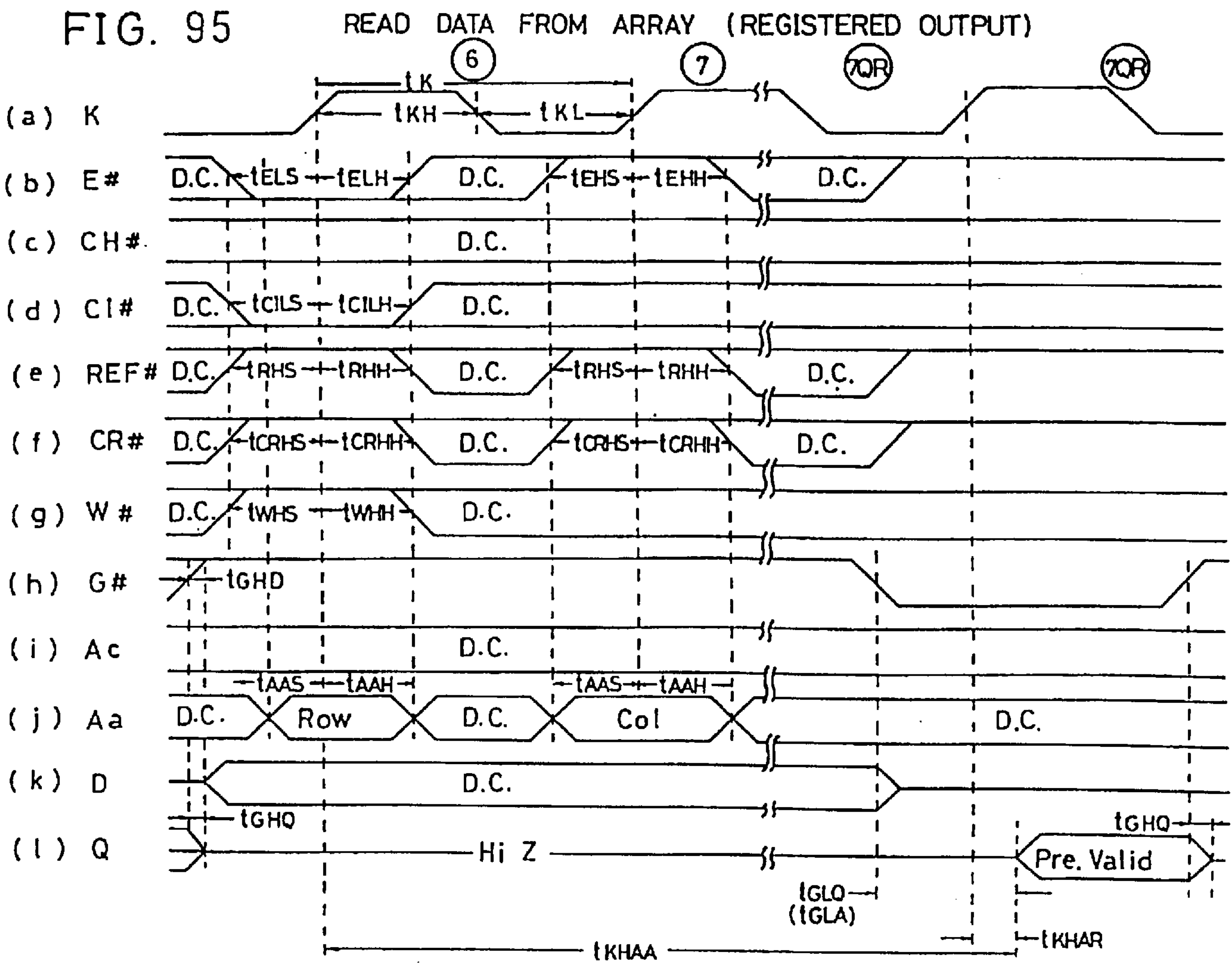


FIG. 95
READ DATA FROM ARRAY (REGISTERED OUTPUT)
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
6
7
7QR
tK
tKH
tKL
tELS
tELH
tEHS
tEHH
tCILS
tCILH
tRHS
tRHH
tCRHS
tCRHH
tWHS
tWHH
tGHD
tAAS
tAAH
tGHQ
tGLQ
(tGLA)
tKHAA
tKHAR
D.C.
Row
Col
Hi Z
Pre. Valid

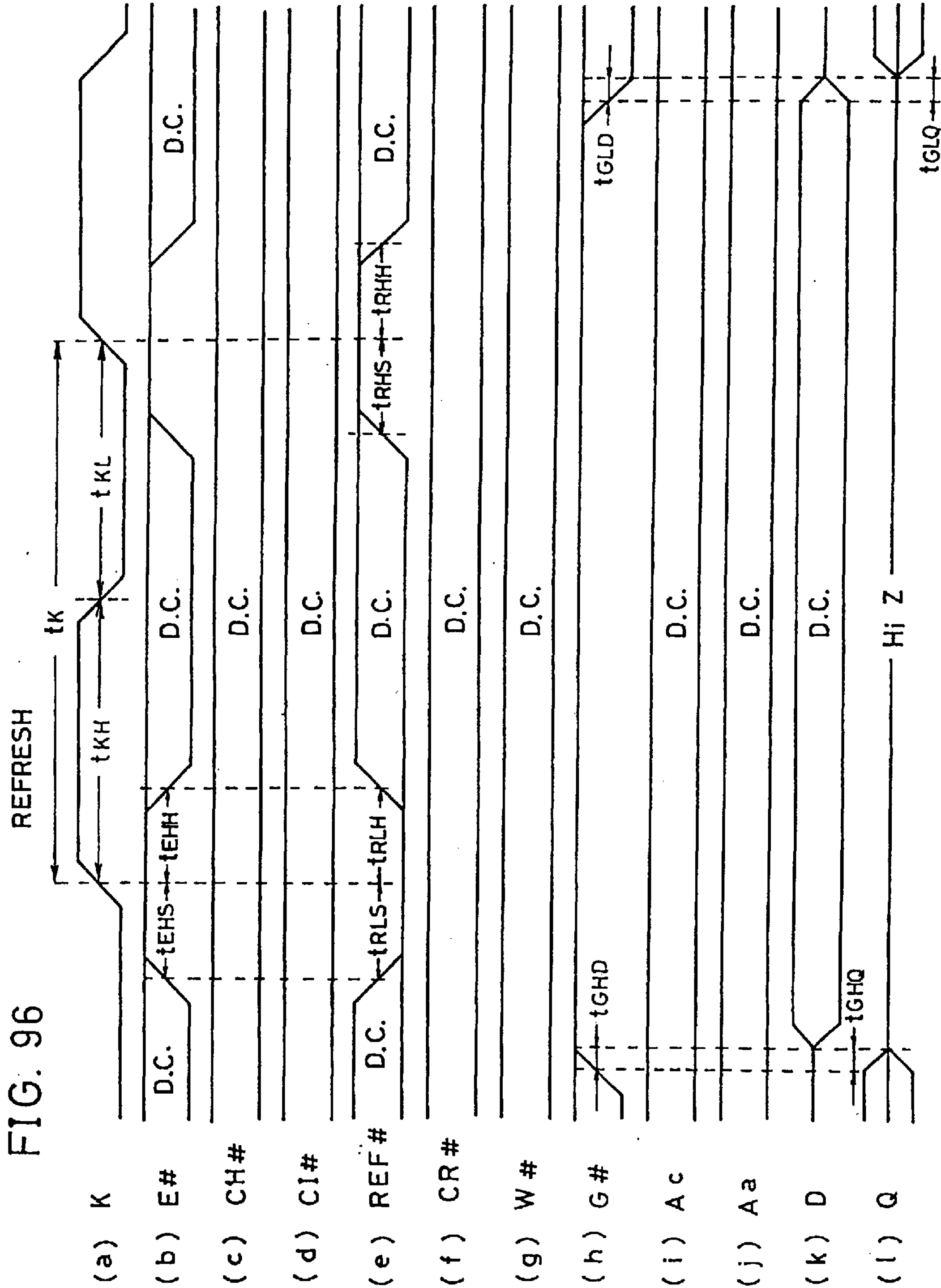


FIG. 96
REFRESH
tK
tKH
tKL
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
D.C.
tEHS
tEHH
tRLS
tRLH
tRHS
tRHH
tGHD
tGLD
tGHQ
tGLQ
Hi Z

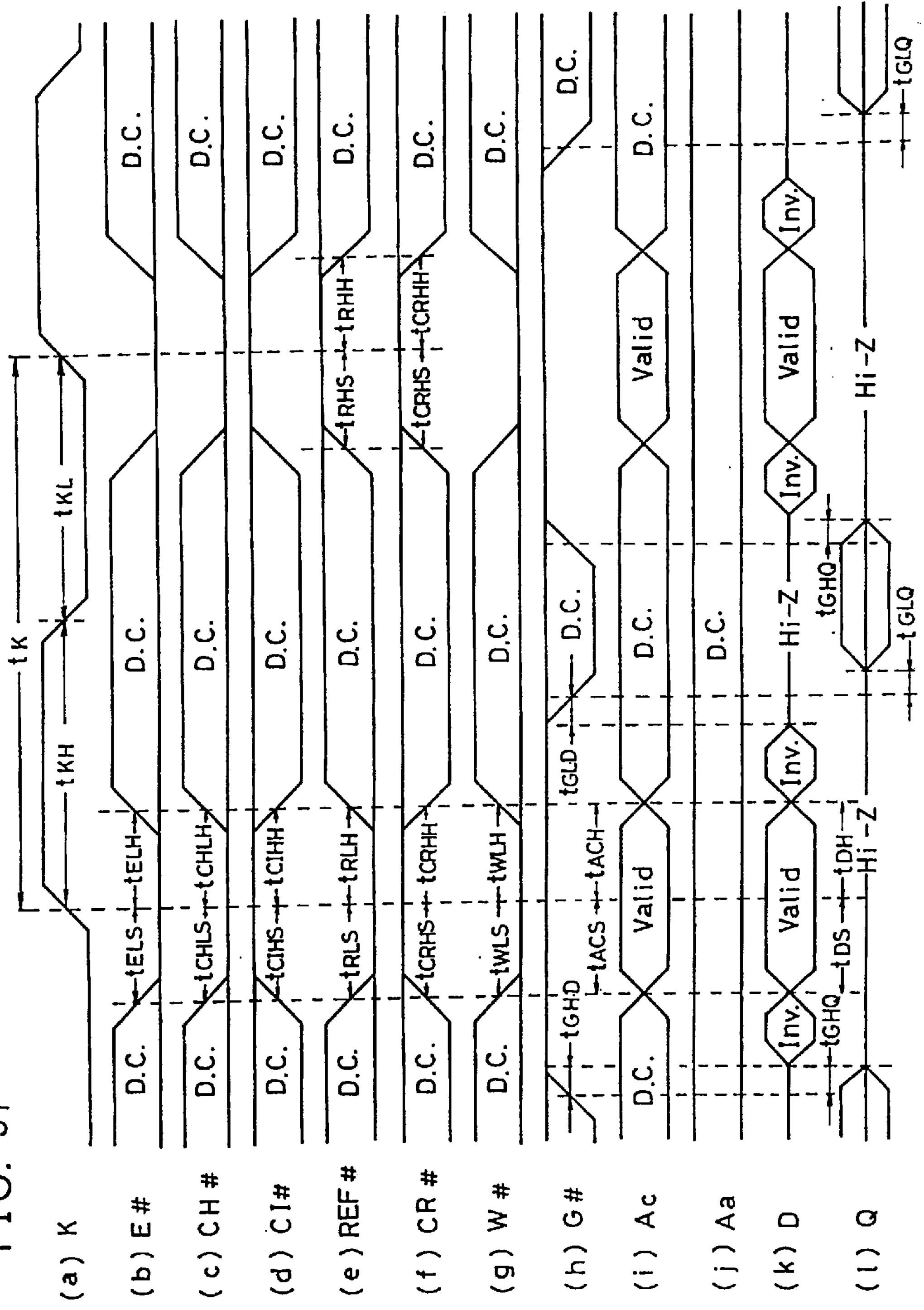


FIG. 97
REFRESH WITH CACHE HIT WRITE
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
tK
tKH
tKL
tELS
tELH
tCHLS
tCHLH
tCIHS
tCIHH
tRLS
tRLH
tCRHS
tCRHH
tRHS
tRHH
tWLS
tWLH
tGHD
tGLD
tACS
tACH
tGHQ
tDS
tDH
tGLQ
D.C.
Valid
Inv.
Hi-Z

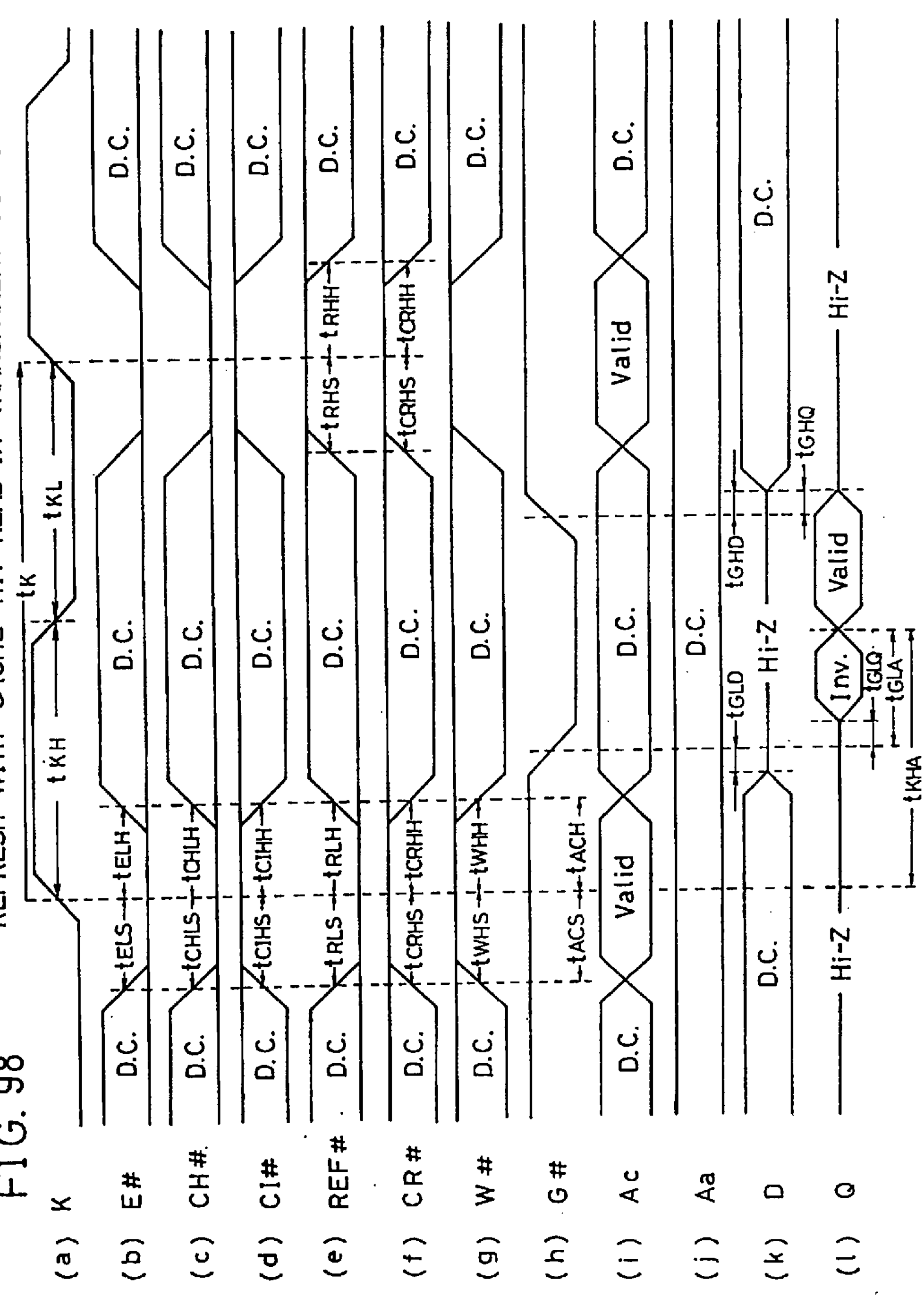


FIG. 98
REFRESH WITH CACHE HIT READ IN TRANSPARENT OUTPUT
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
tK
tKH
tKL
tELS
tELH
tCHLS
tCHLH
tCIHS
tCIHH
tRLS
tRLH
tCRHS
tCRHH
tWHS
tWHH
tACS
tACH
tRHS
tRHH
tCRHS
tCRHH
tGLD
tGHD
tGHQ
tGLQ
tGLA
tKHA
D.C.
Valid
Inv.
Hi-Z

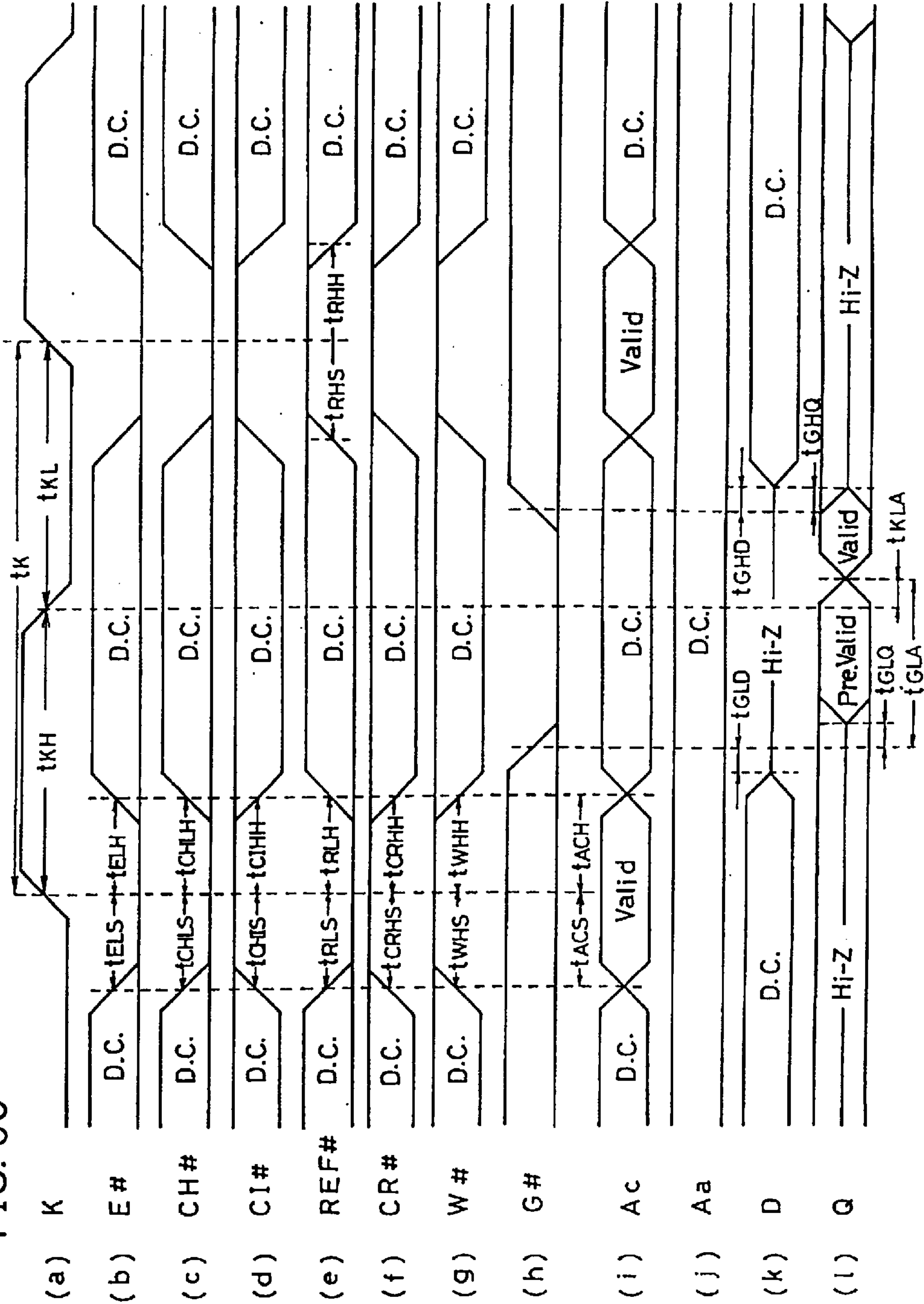


FIG. 99
REFRSH WITH CACHE HIT READ IN LATCHED OUTPUT
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
tK
tKH
tKL
tELS
tELH
tCHLS
tCHLH
tCIHS
tCIHH
tRLS
tRLH
tRHS
tRHH
tCRHS
tCRHH
tWHS
tWHH
tACS
tACH
tGLD
tGHD
tGHQ
tGLQ
tGLA
tKLA
D.C.
Valid
Hi-Z
Pre.Valid

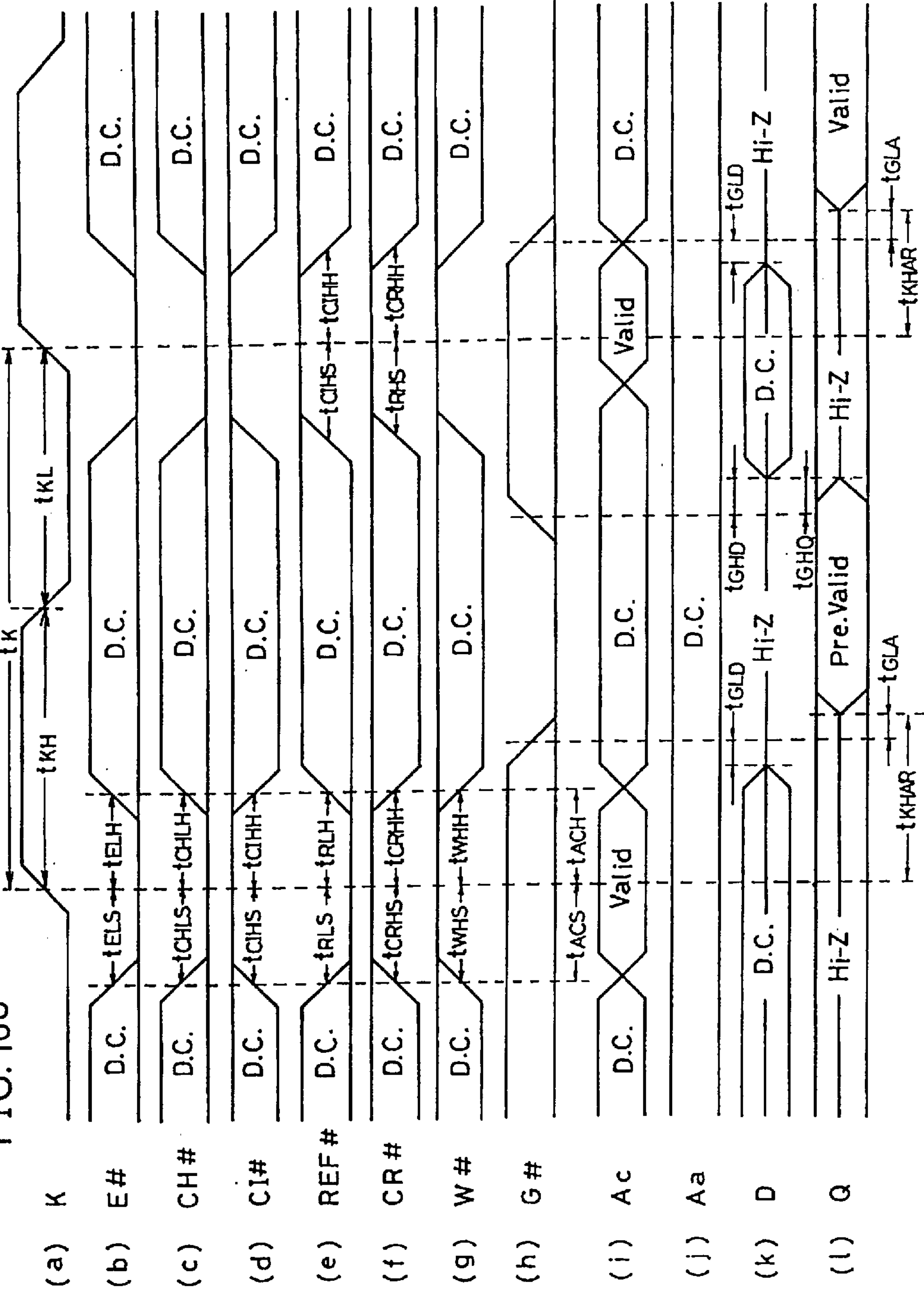


FIG. 100
REFRESH WITH CACHE HIT READ IN REGISTERED OUTPUT
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Aa
(k) D
(l) Q
tK
tKH
tKL
tELS
tELH
tCHLS
tCHLH
tCIHS
tCIHH
tRLS
tRLH
tCRHS
tCRHH
tWHS
tWHH
tACS
tACH
tRHS
tGLD
tGHD
tGHQ
tGLA
tKHAR
D.C.
Valid
Hi-Z
Pre.Valid

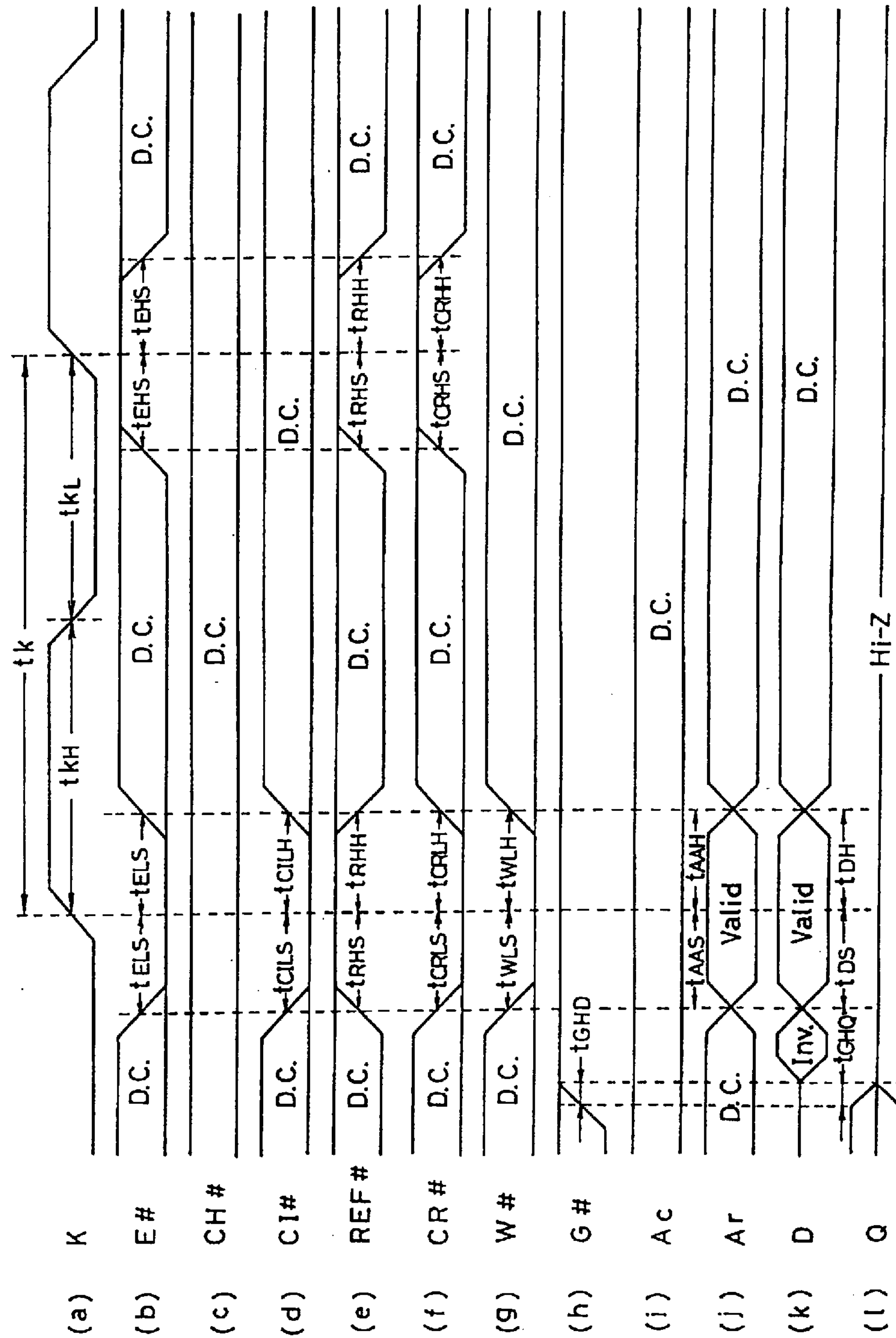


FIG.101
COMMAND REGISTER SET
(a) K
(b) E#
(c) CH#
(d) CI#
(e) REF#
(f) CR#
(g) W#
(h) G#
(i) Ac
(j) Ar
(k) D
(l) Q
tk
tkH
tkL
tELS
tEHS
tCILS
tCILH
tRHS
tRHH
tCRLS
tCRLH
tCRHS
tCRHH
tWLS
tWLH
tGHD
tAAS
tAAH
tDS
tDH
tGHQ
D.C.
Valid
Inv.
Hi-Z

FIG. 102A

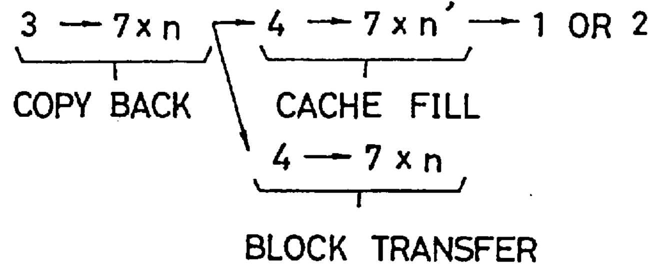
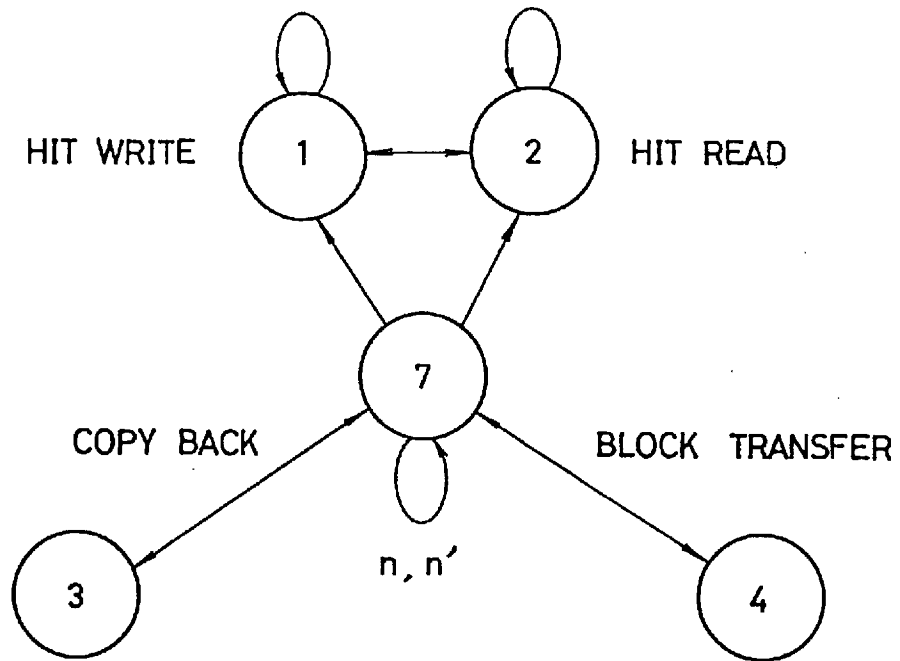


FIG. 102B



$n = (ta / tk) - 1$

$n' = (ta / 2tk) - 1$

FIG. 103A

ARRAY ACCESS

(i) ARRAY WRITE :	5 ⟶ 7 × n
(ii) ARRAY READ :	6 ⟶ 7 × n' ⟶ 7 Q × (n'+1)

FIG. 103B

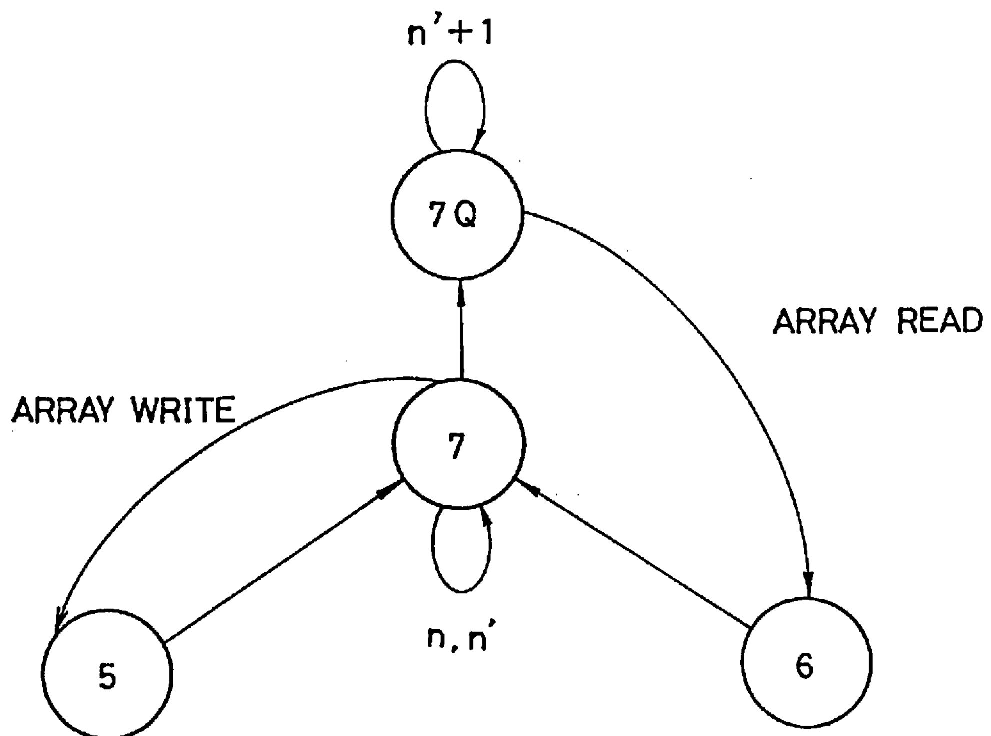
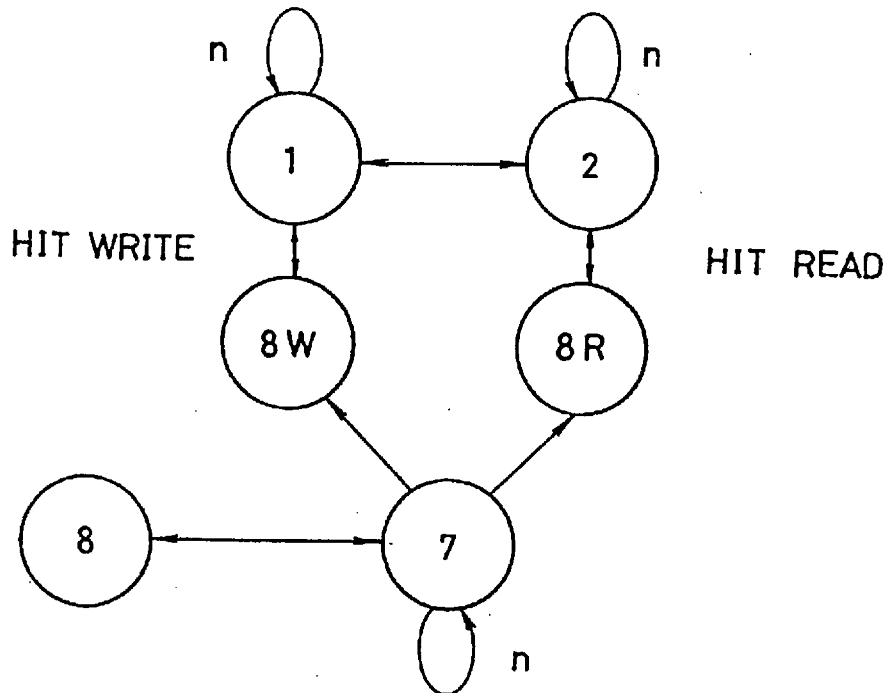


FIG. 104A

REFRESH

(i) NORMAL REFRESH	8 ⟶ 7 x n
(ii) REFRESH WITH HIT WRITE	8W ⟶ 1 X n
(iii) REFESH WITH HIT READ	8R ⟶ 2 X n

FIG. 104B



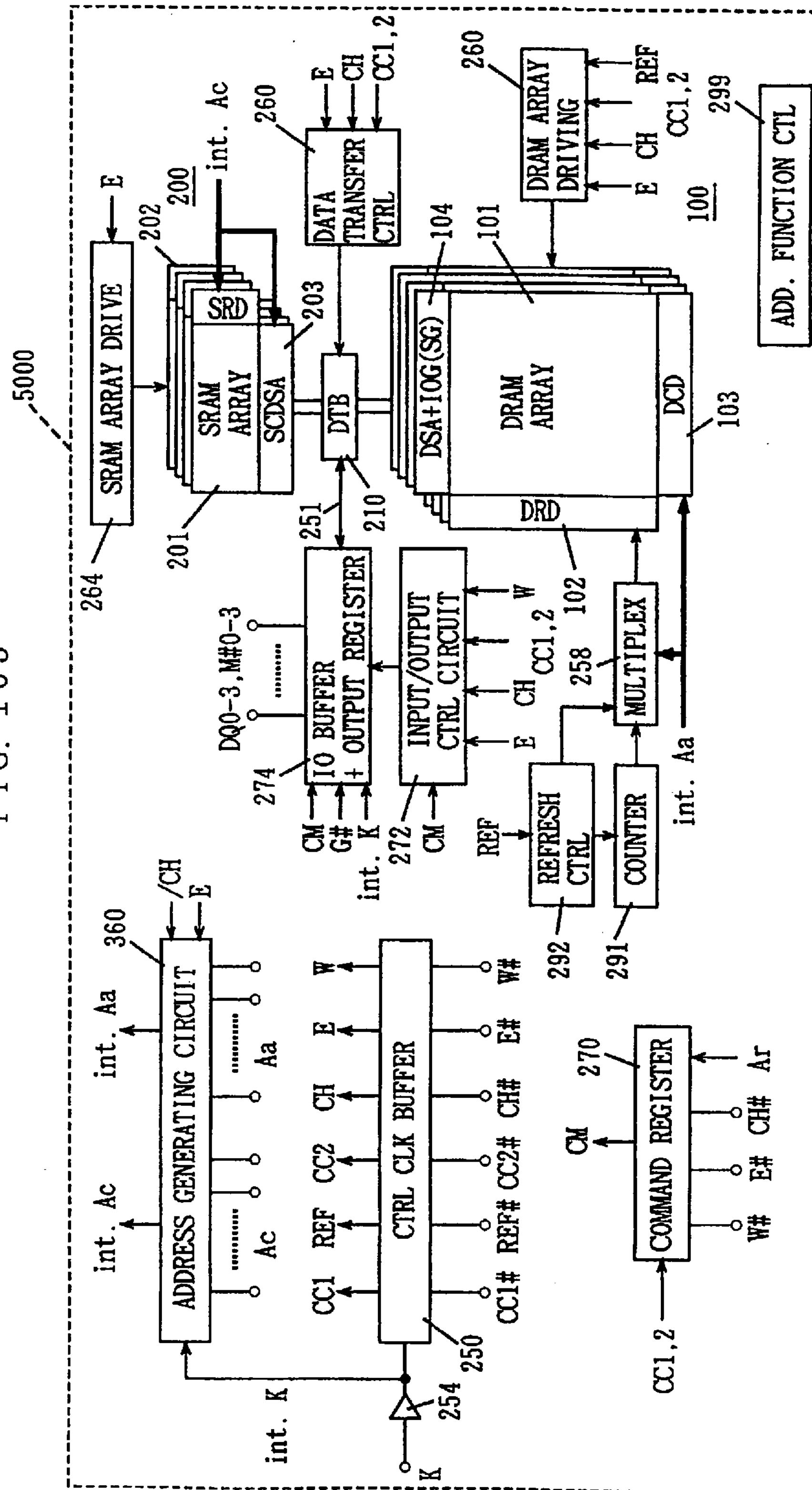


FIG. 105

FIG. 106

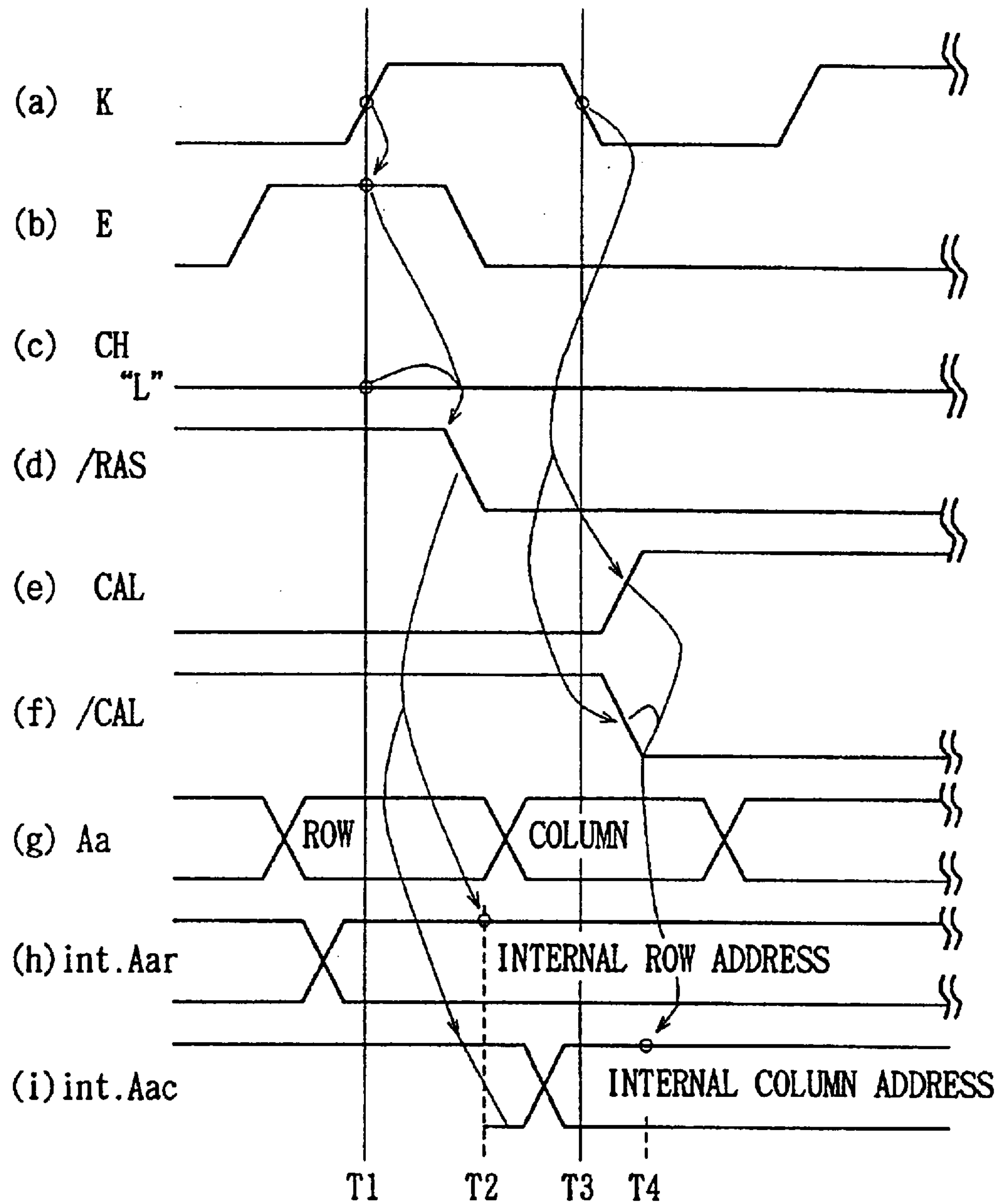
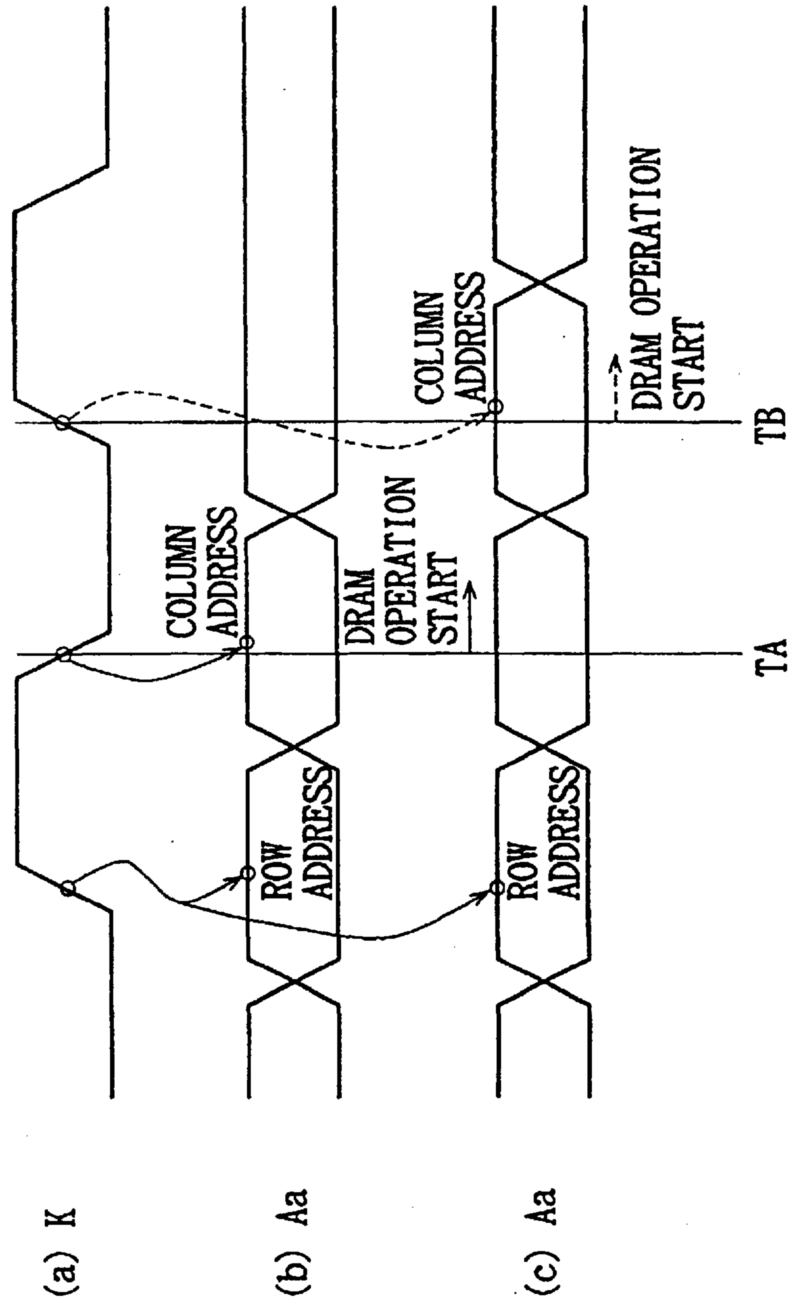
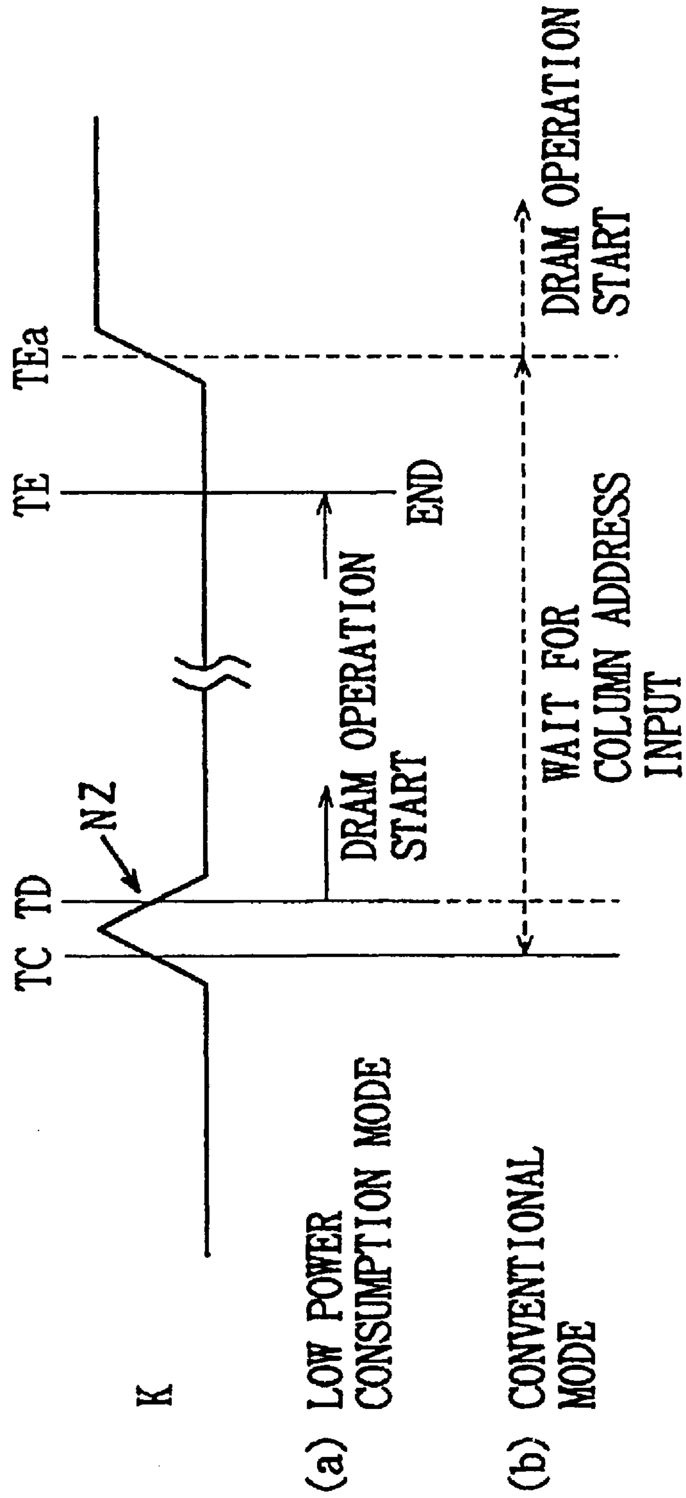


FIG. 107



F I G. 1 0 8



F I G. 1 0 9

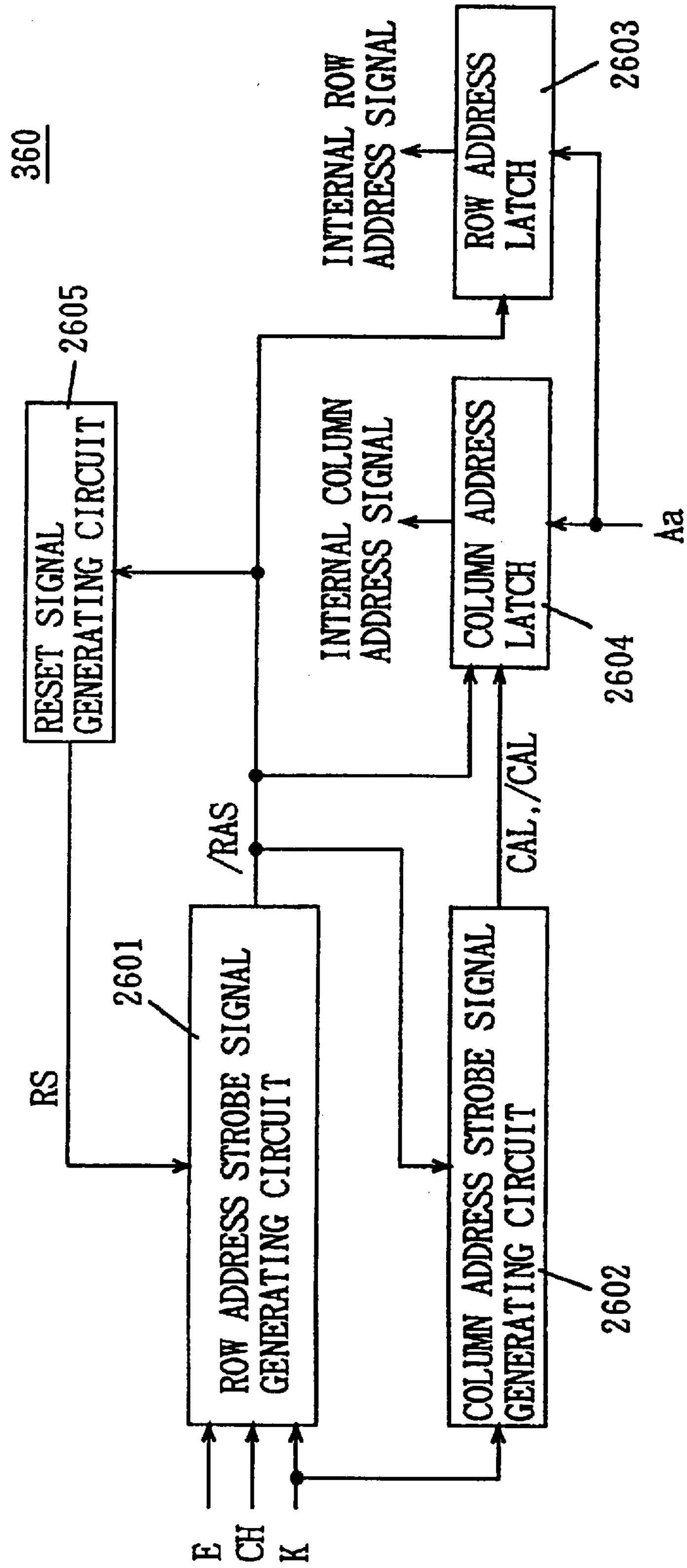


FIG. 110

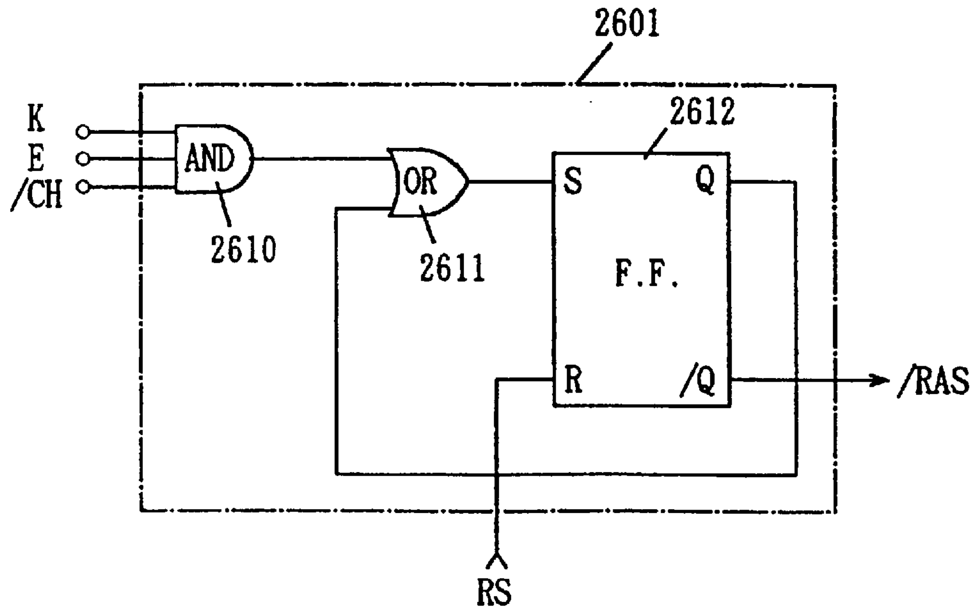


FIG. 111

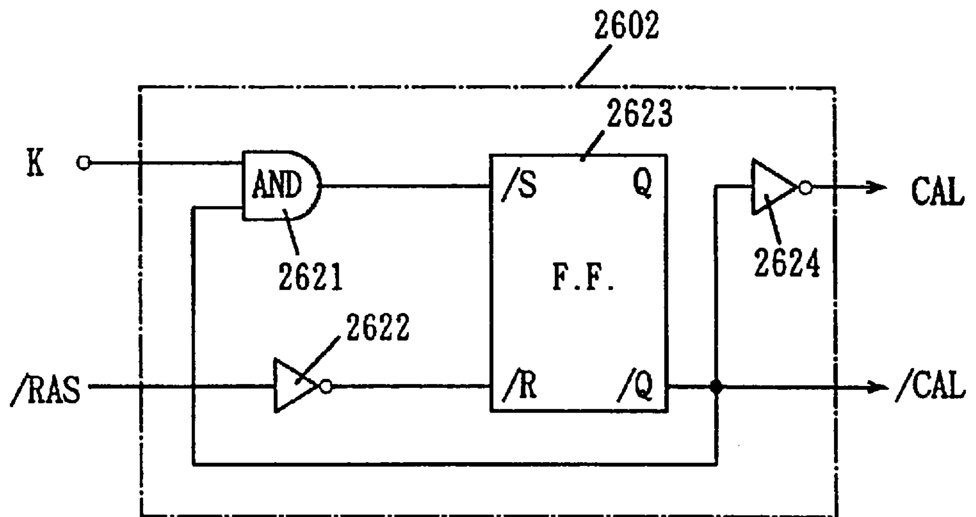


FIG. 112

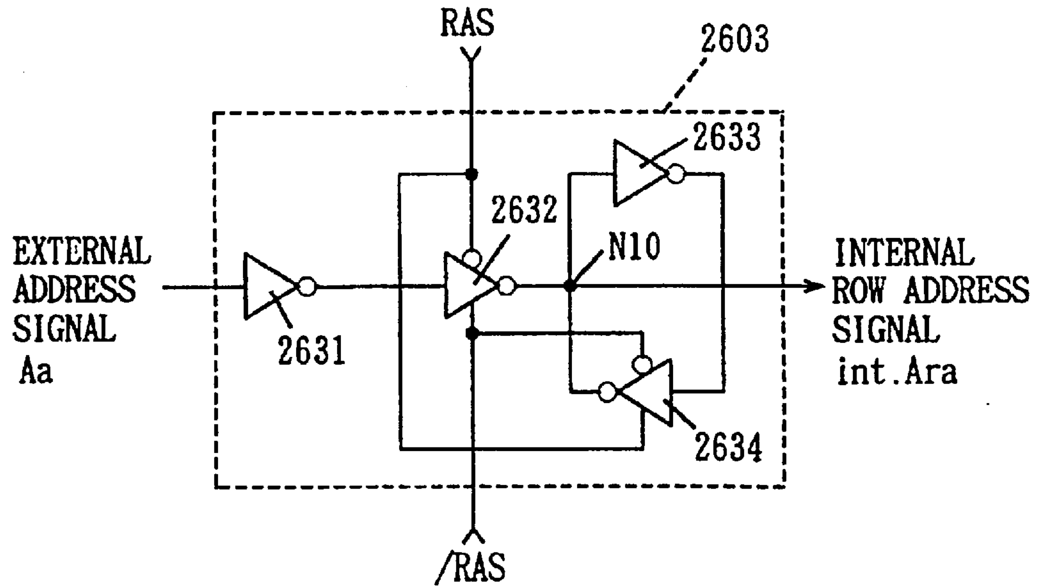
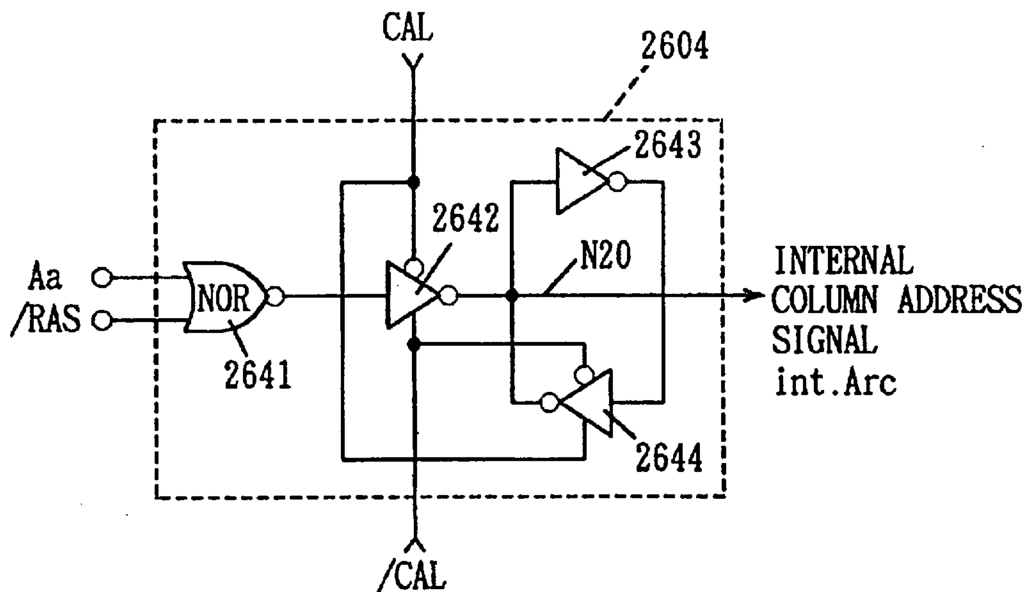
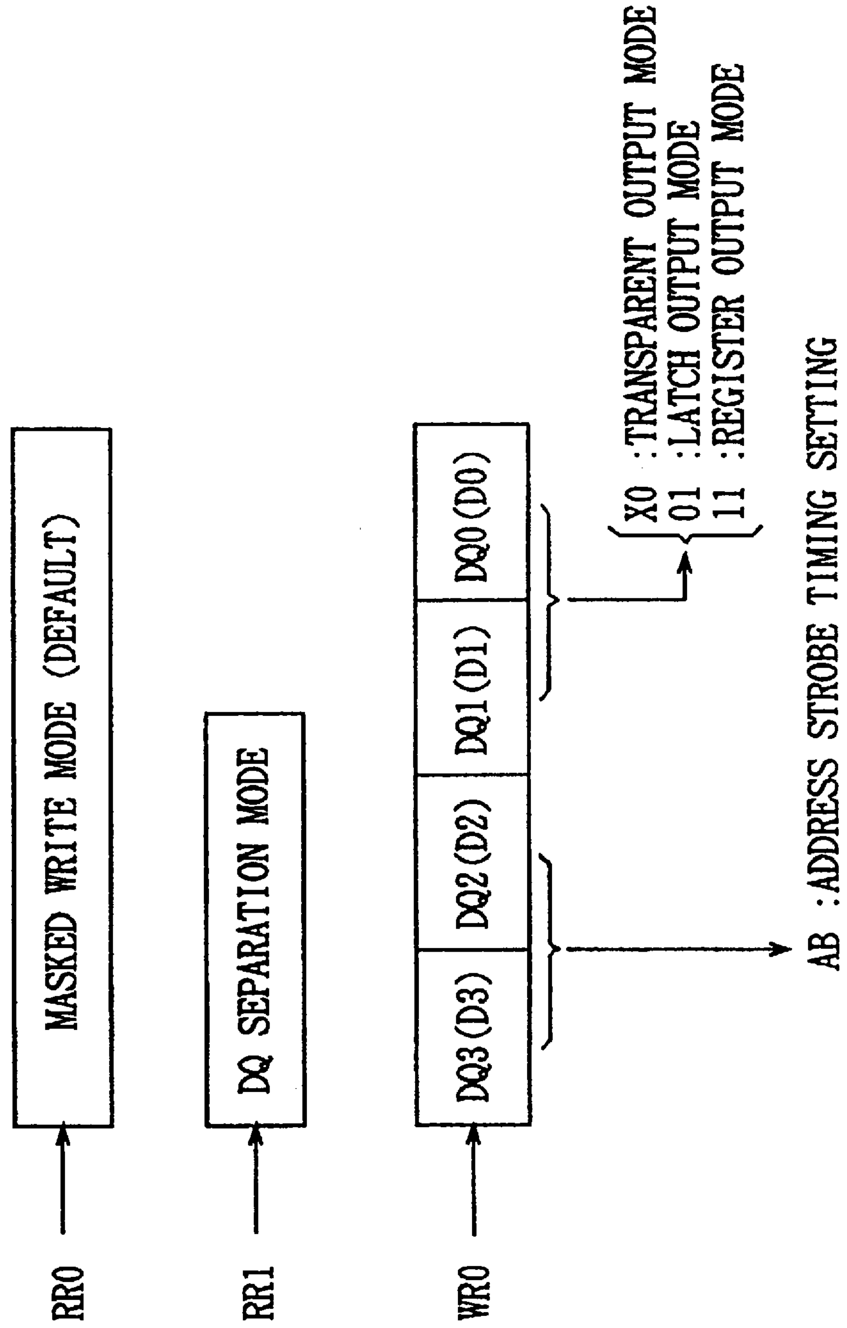
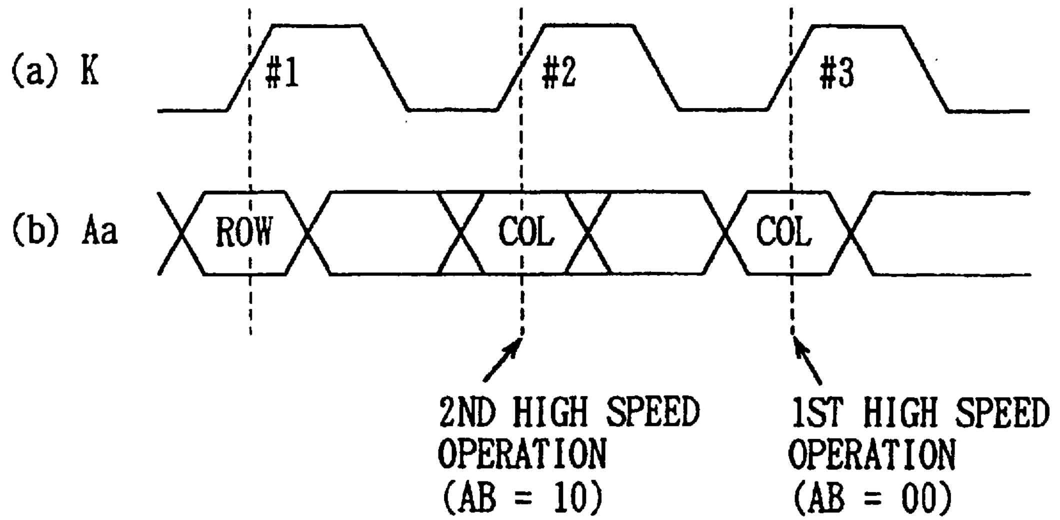


FIG. 113

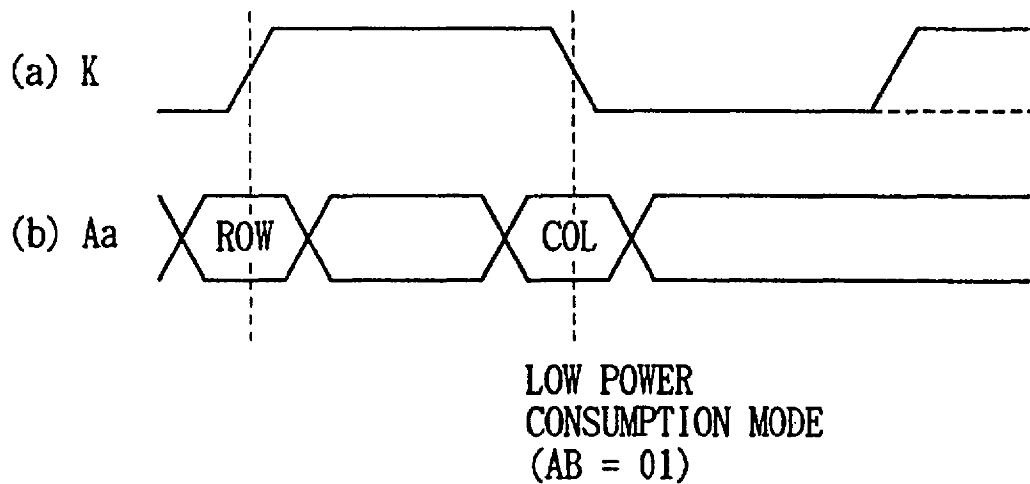



F I G. 1 1 4
MASKED WRITE MODE (DEFAULT)
DQ SEPARATION MODE
RR0
RR1
WR0
DQ3 (D3)
DQ2 (D2)
DQ1 (D1)
DQ0 (D0)
X0 :TRANSPARENT OUTPUT MODE
01 :LATCH OUTPUT MODE
11 :REGISTER OUTPUT MODE
AB :ADDRESS STROBE TIMING SETTING

F I G. 1 1 5



F I G. 1 1 6



F I G. 1 1 7

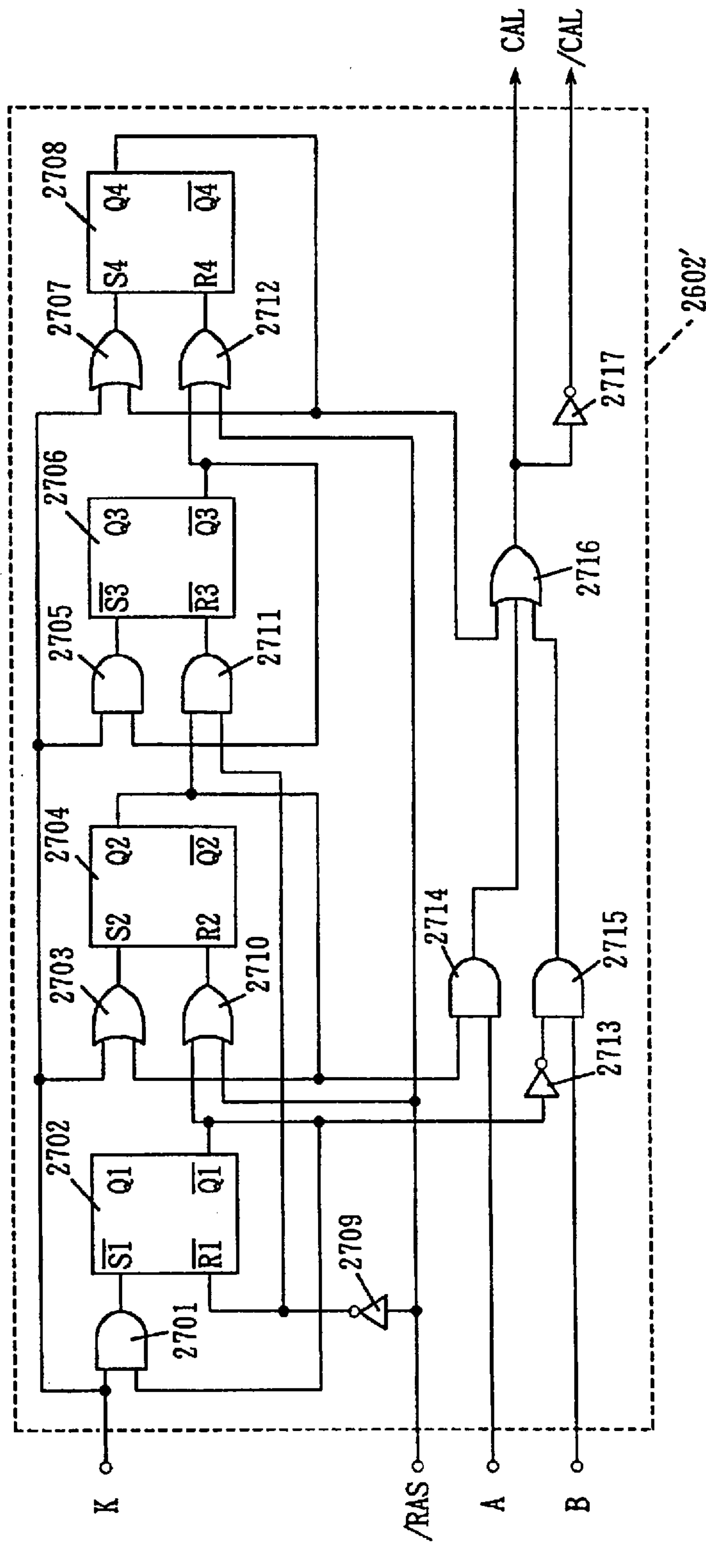


FIG. 118

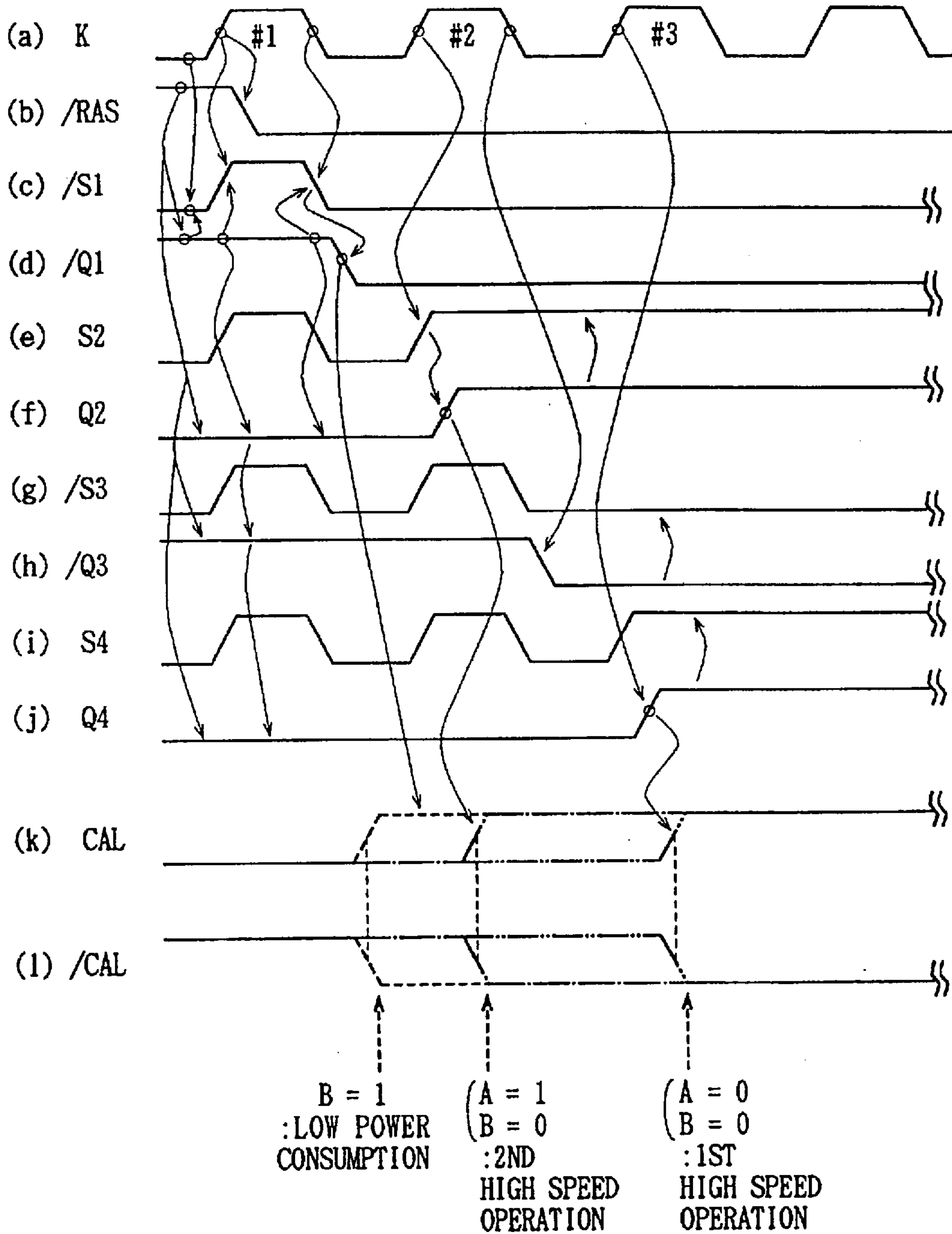
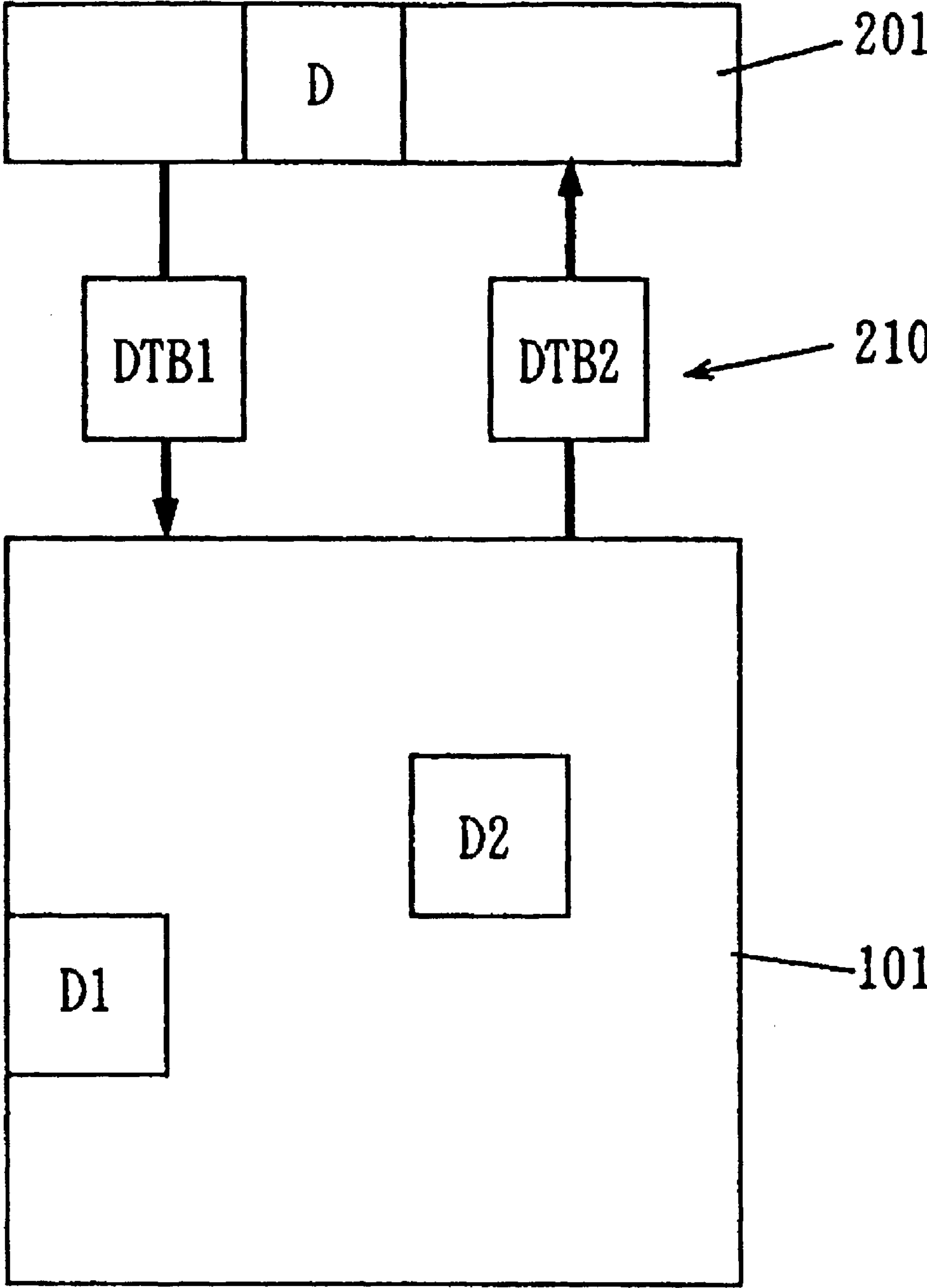
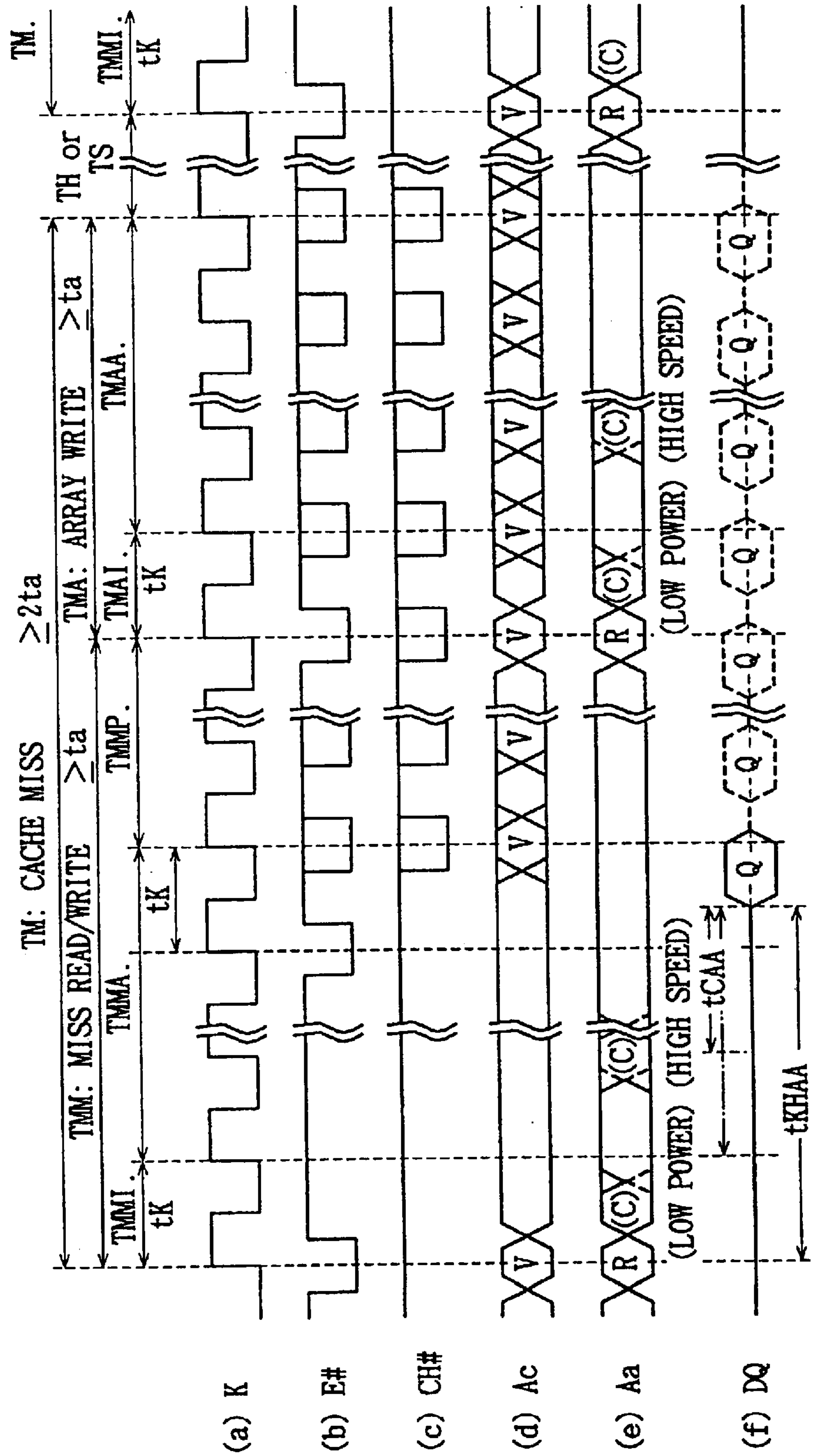


FIG. 119

OPERATION			E#	CH#	CC1#	CC2#	W#	REF#
TH. (CACHE)			L	L	H/L	H	H/L	H
TG. (COMMAND REGISTER SET)			L	H	L	L	H/L	H/L
TS. (STANDBY)			H	×	×	×	×	H
TM. (CACHE MISS)	TMM. (MISS READ/ WRITE)	TMMI. INITIATE	L	H	H	H	H/L	H
		TMMA. ARRAY ACTIVE	H	H	H	H	H	H
		TMMP. PRECHARGE *	H L	H L	H	H	H/L	H
	TMA. (ARRAY WRITE)	TMAL. INITIATE *	L	H L	H L	L H	H/L	H
		TMAA. ARRAY ACTIVE + PRECHARGE *	H L	H L	H	H	H/L	H
TD. (DIRECT ARRAY ACCESS)		TDL. INITIATE	L	H	L	H	H/L	H
		TDA. ARRAY ACTIVE + PRECHARGE	H	H	H	H	H	H
TR. (REFRESH)		TRI. INITIATE *	H L	H L	H	H	H/L	L
		TRA. ARRAY ACTIVE + PRECHARGE *	H L	H L	H	H	H/L	H
TC. (COUNTER CHECK)		TCI. INITIATE	L	H	L	H	H/L	L
		TCA. ARRAY ACTIVE + PRECHARGE	H	H	H	H	H	H

FIG. 120




F I G. 1 2 1
TM: CACHE MISS ≥2ta
TMM: MISS READ/WRITE ≥ta
TMA: ARRAY WRITE ≥ta
TH or TS
TM.
TMMI.
tK
TMMA.
TMMP.
TMAI.
TMAA.
(LOW POWER) (HIGH SPEED)
tCAA
tKHAA
(a) K
(b) E#
(c) CH#
(d) Ac
(e) Aa
(f) DQ
V
R
(C)
Q

F I G. 122

LTHR:CACHE HIT READ OPERATION (LOW POWER CONSUMPTION) (TRANSPARENT OUTPUT)

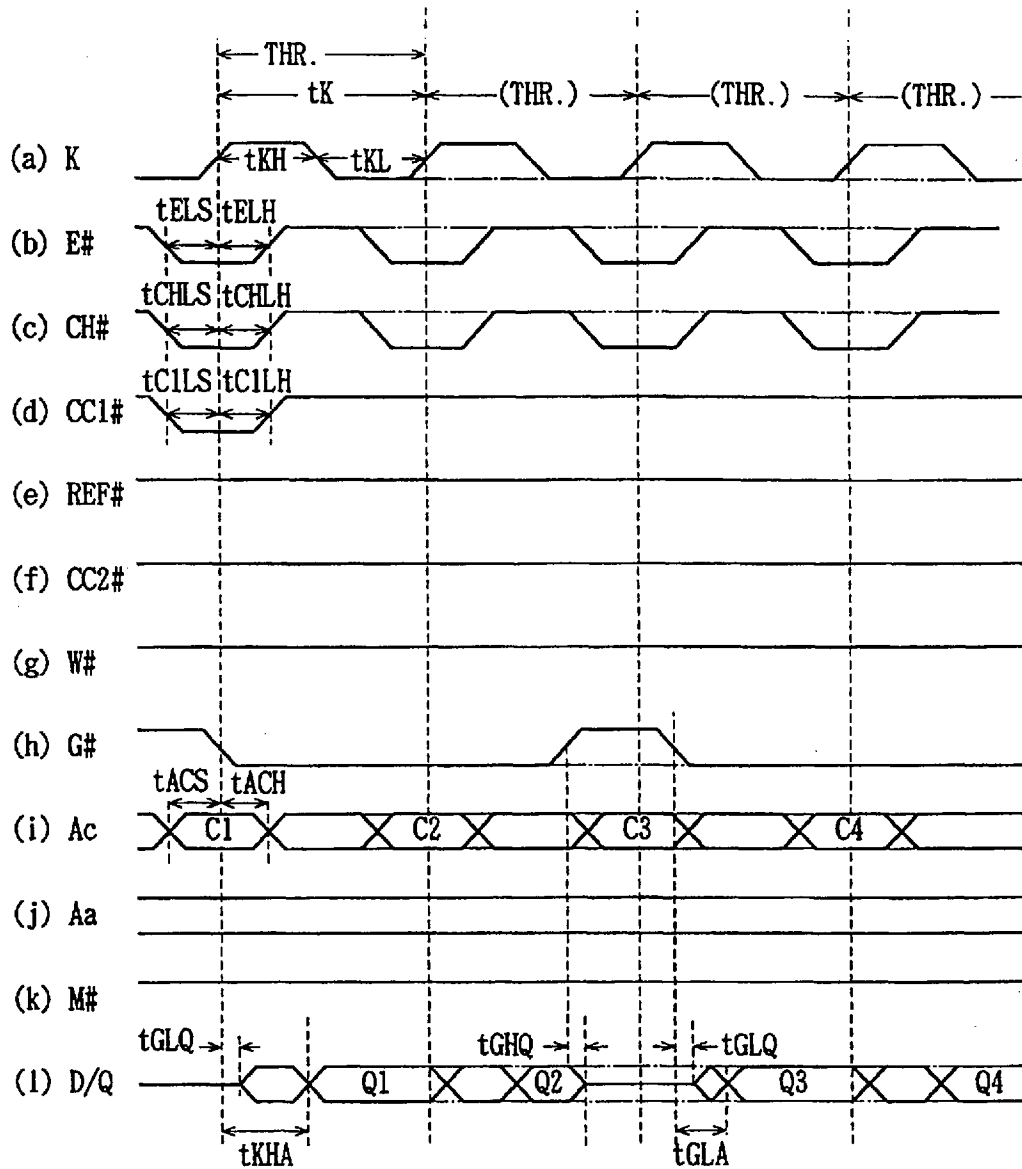


FIG. 123

LTHW:CACHE HIT WRITE (LOW POWER CONSUMPTION)

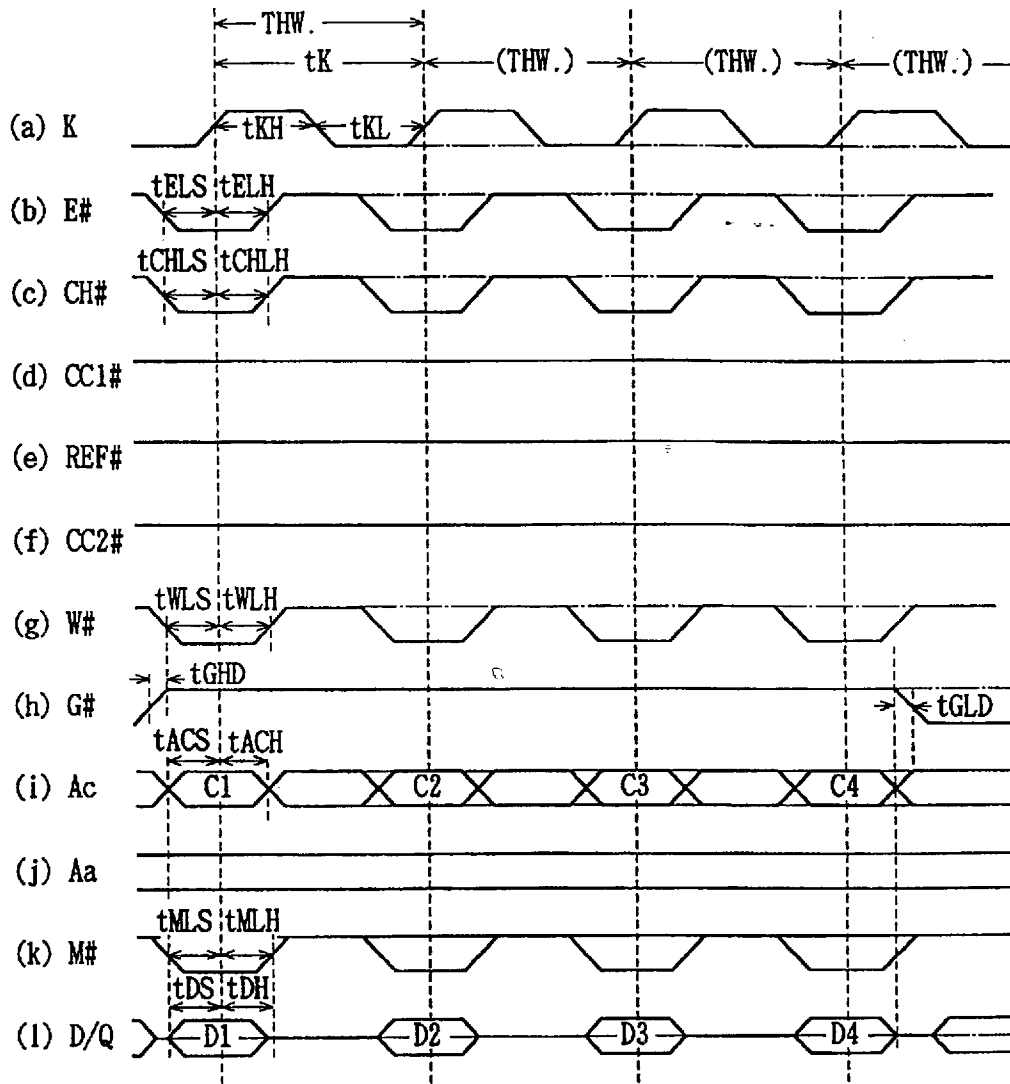


FIG. 124

LTMMR:CACHE MISS READ OPERATION (LOW POWER CONSUMPTION)

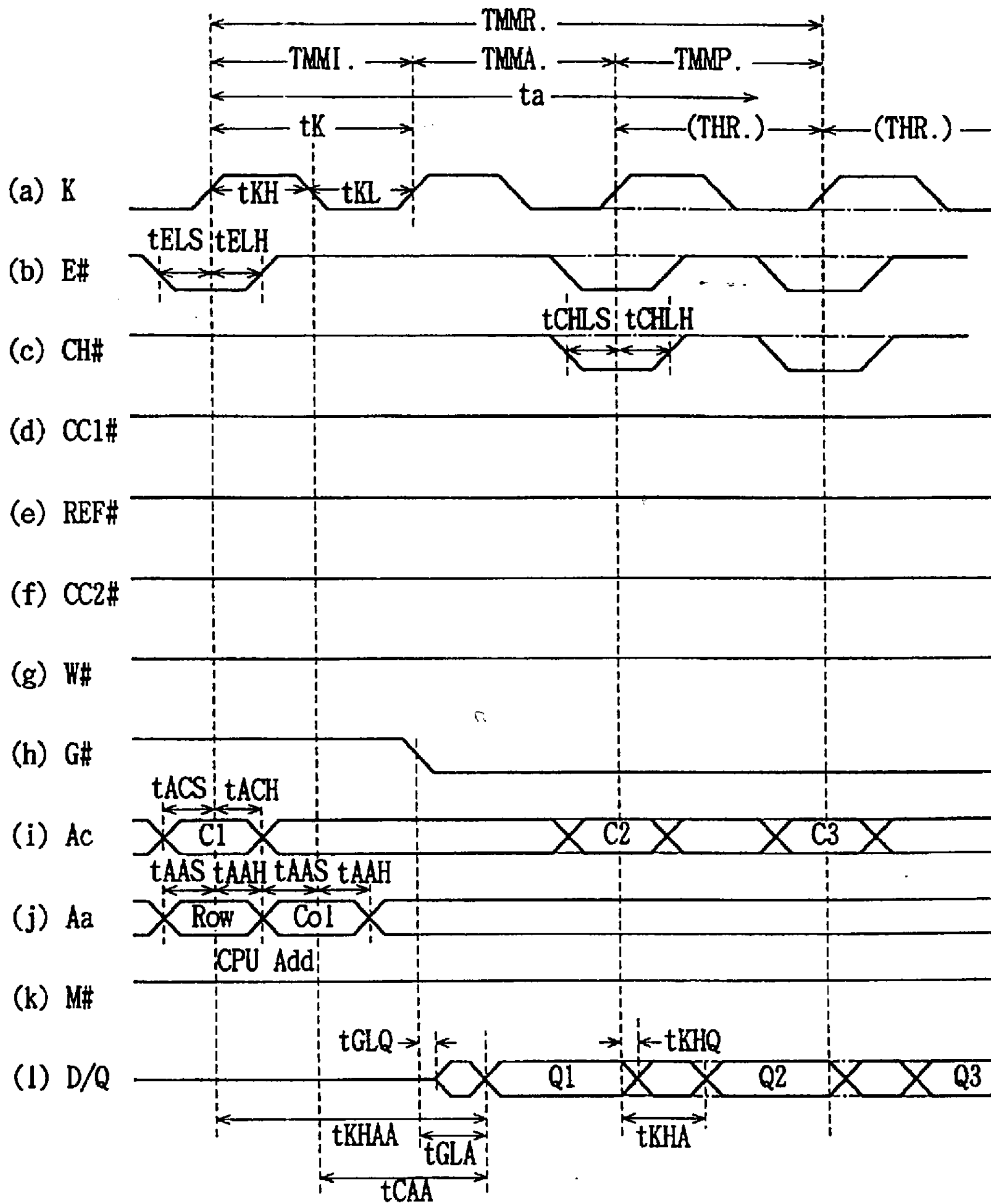


FIG. 125

LTMMW:CACHE MISS WRITE OPERATION (LOW POWER CONSUMPTION)

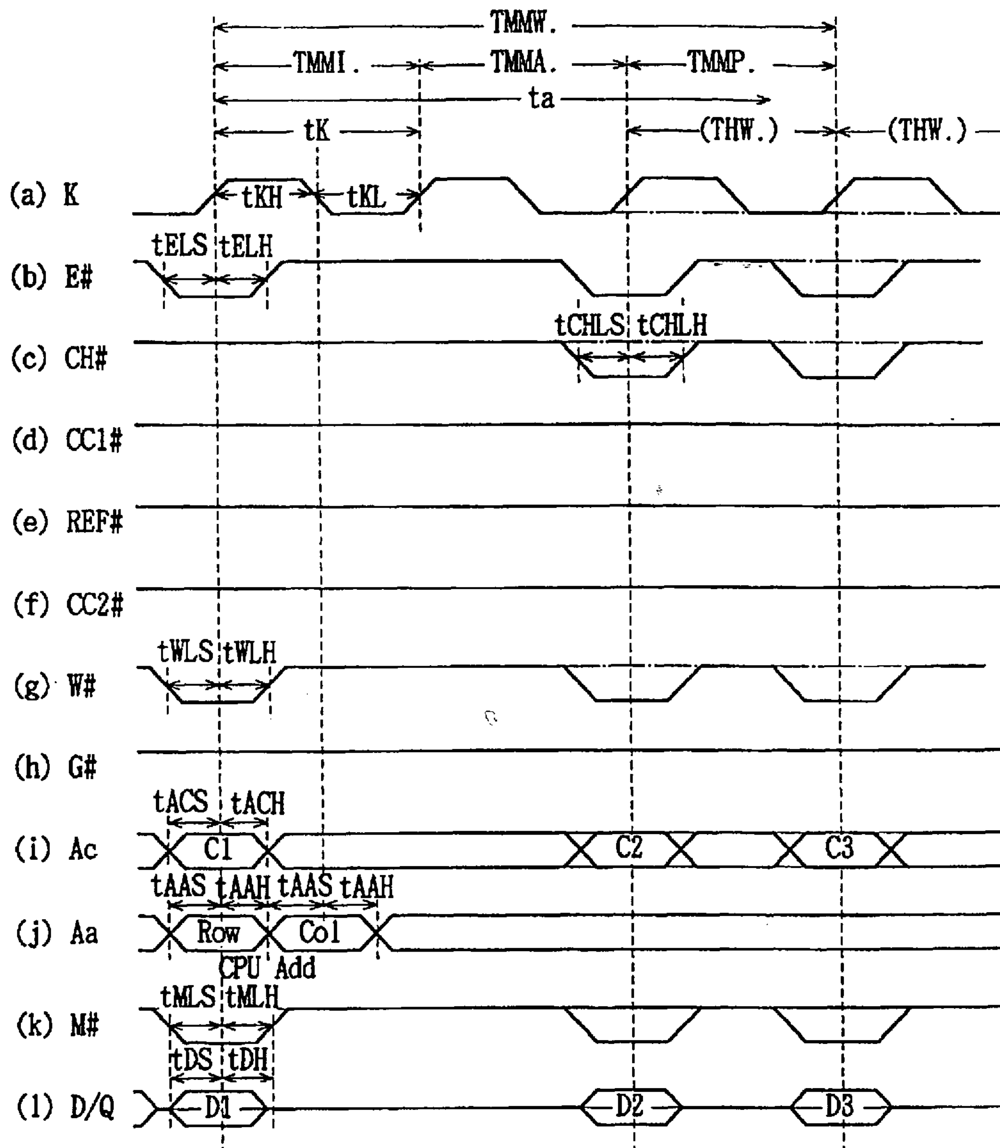


FIG. 126

LTMA.:ARRAY WRITE OPERATION (LOW POWER CONSUMPTION)
(DTB → ARRAY)

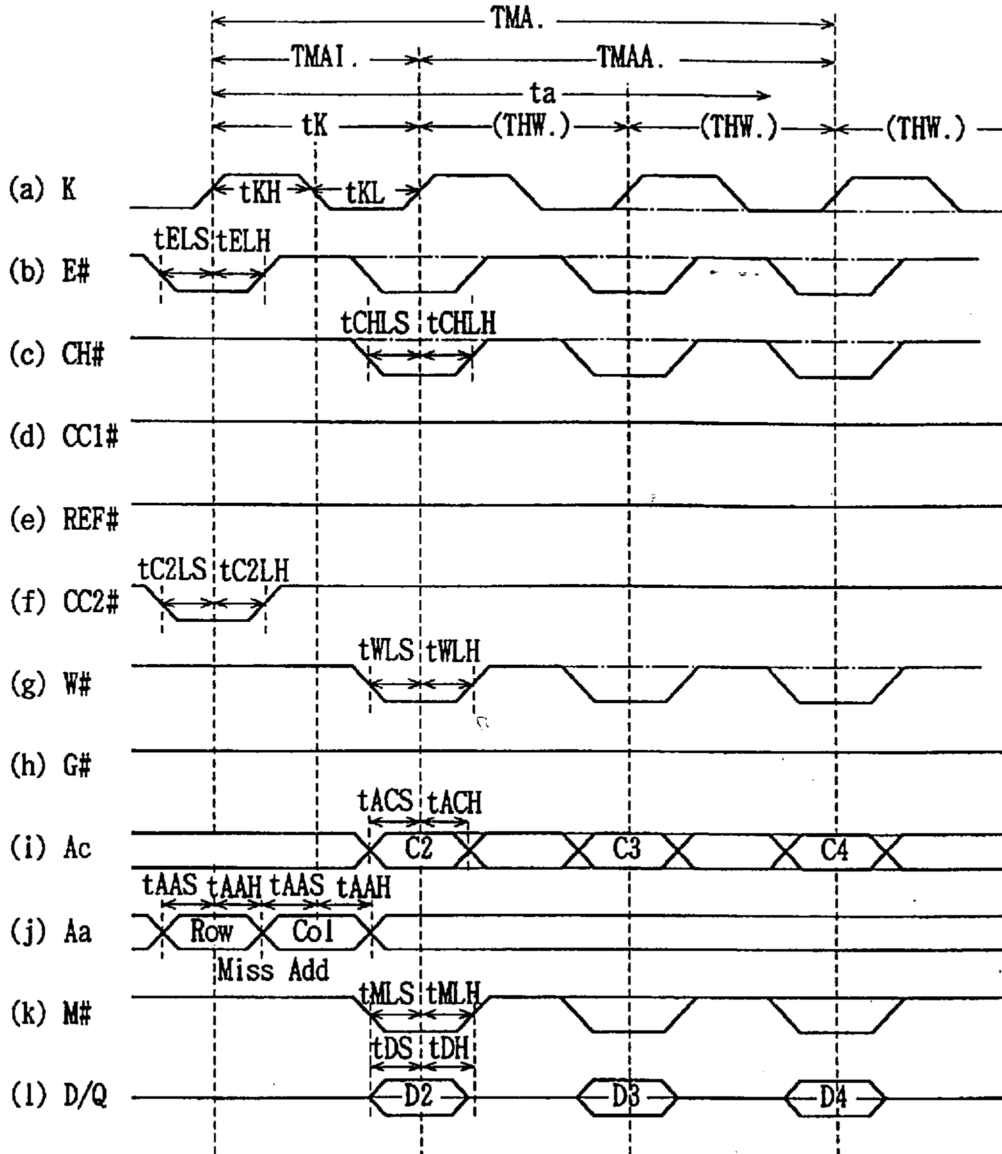


FIG. 127

LTMAR:ARRAY WRITE OPERATION WITH CACHE HIT READ (LOW POWER CONSUMPTION)

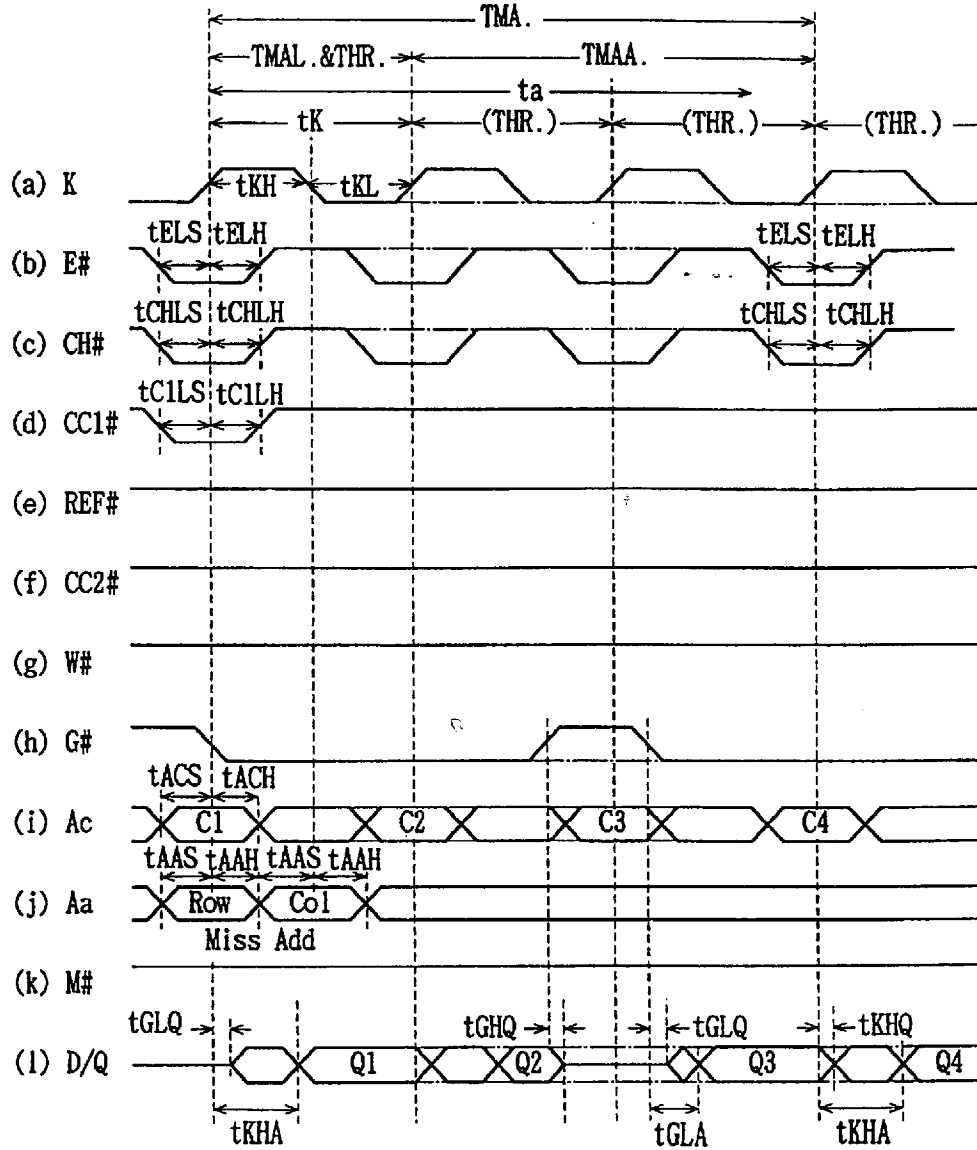


FIG. 128

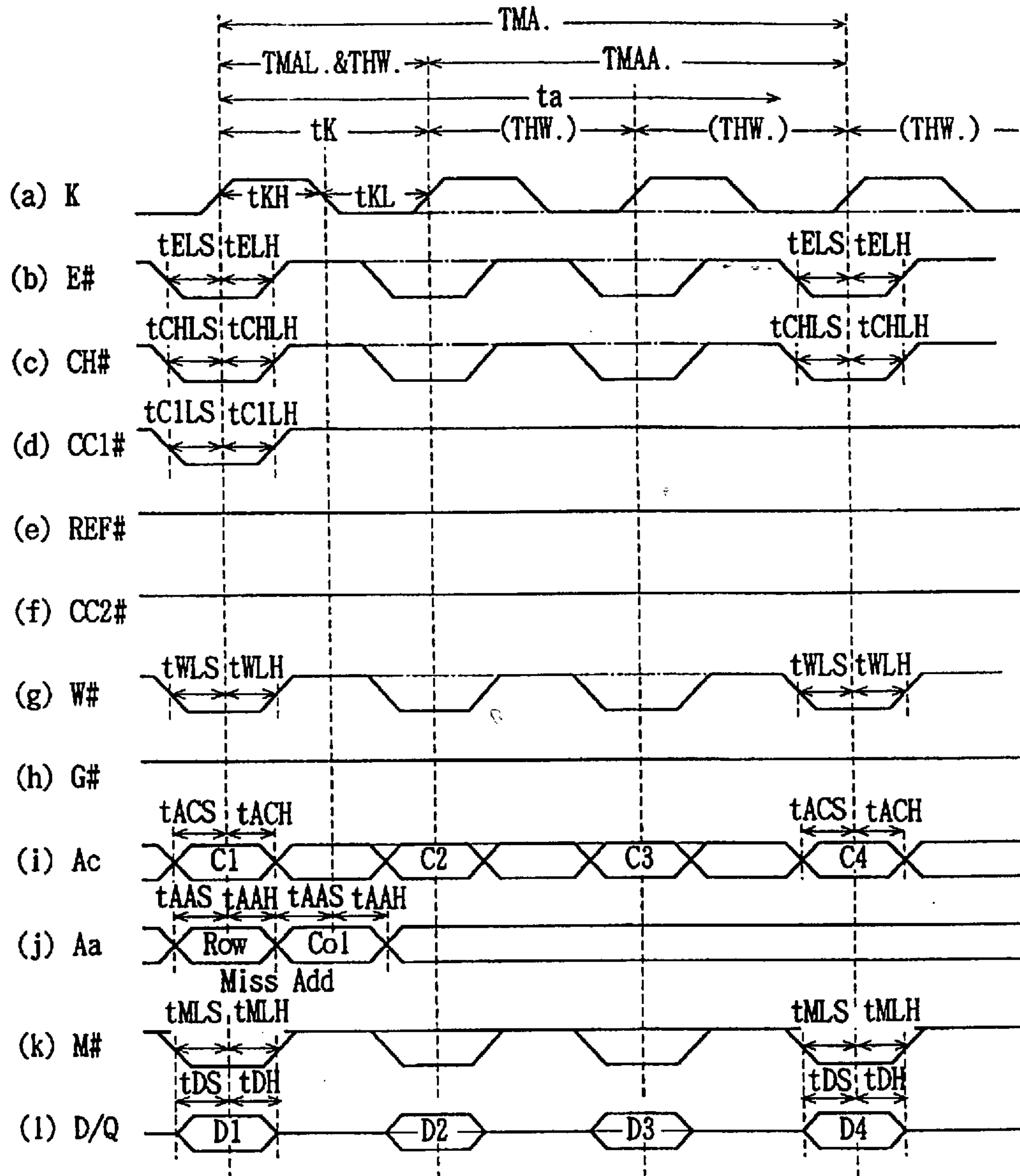


FIG. 129

LTDR:DIRECT ARRAY READ OPERATION (LOW POWER CONSUMPTION)

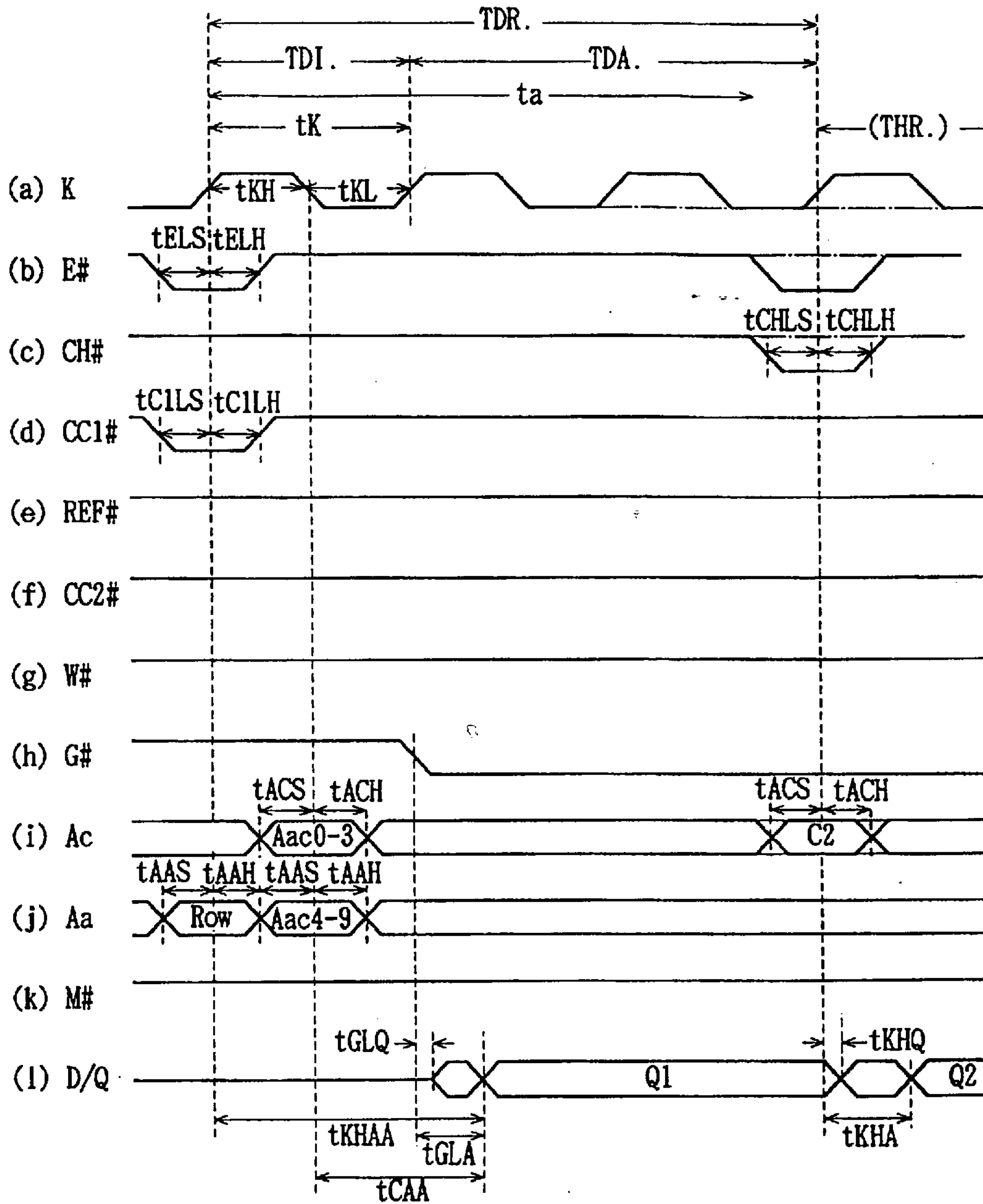


FIG. 130

LTDW:DIRECT ARRAY WRITE OPERATION (LOW POWER CONSUMPTION)

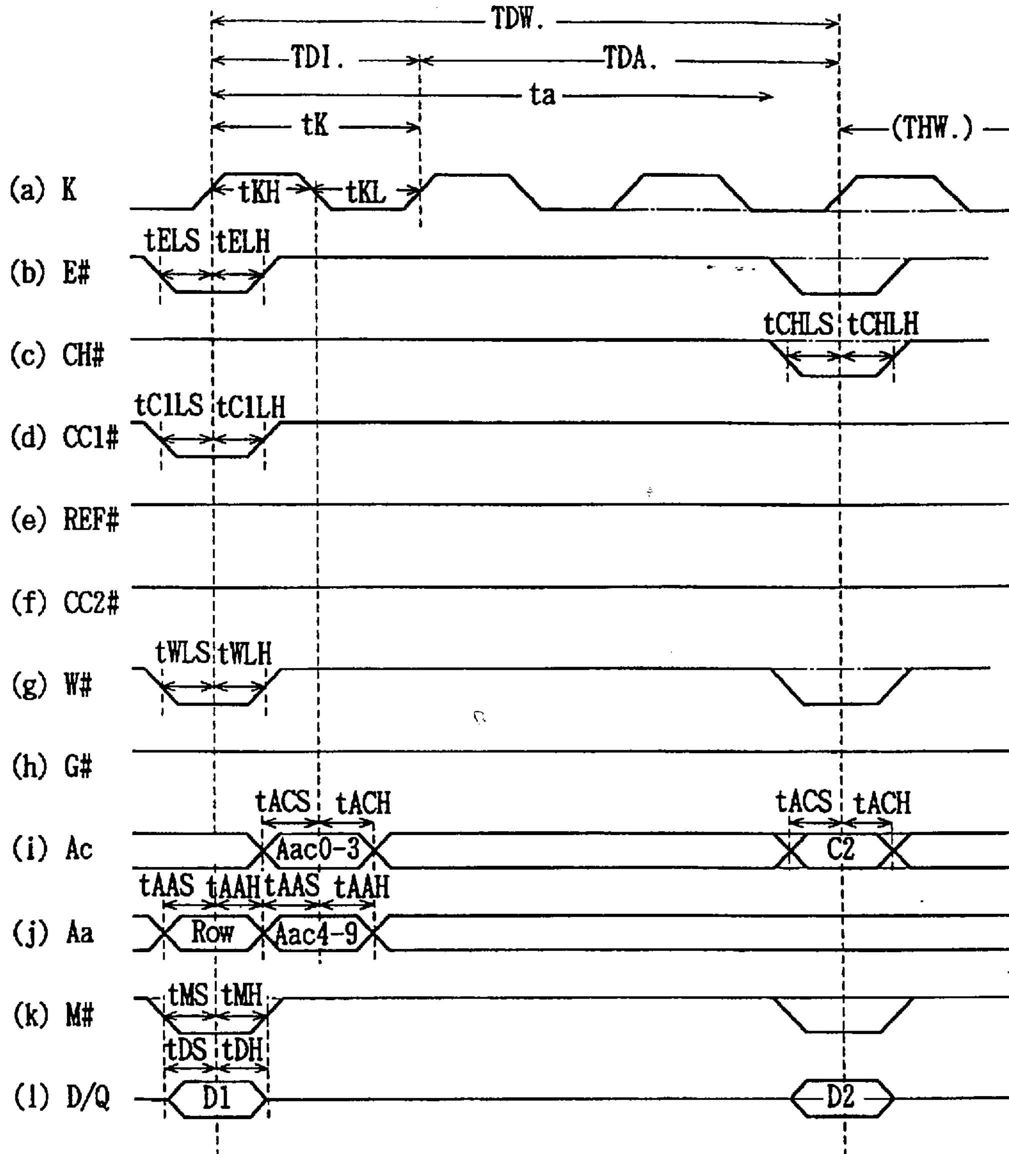
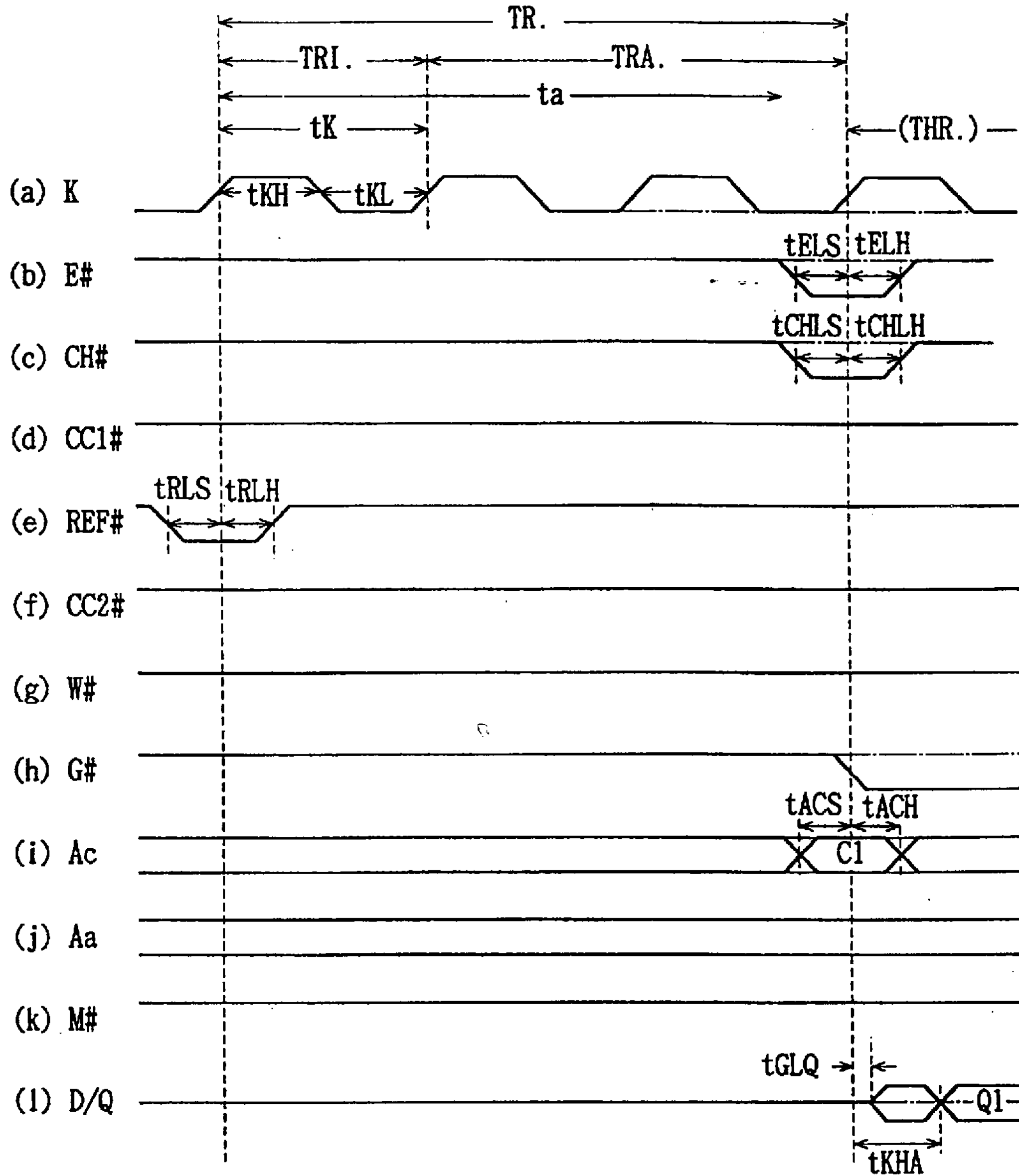


FIG. 131

LTR:REFRESH ARRAY OPERATION (LOW POWER CONSUMPTION)



F I G. 1 3 2

LTRR:REFRESH ARRAY OPERATION WITH CACHE HIT READ (LOW POWER CONSUMPTION)

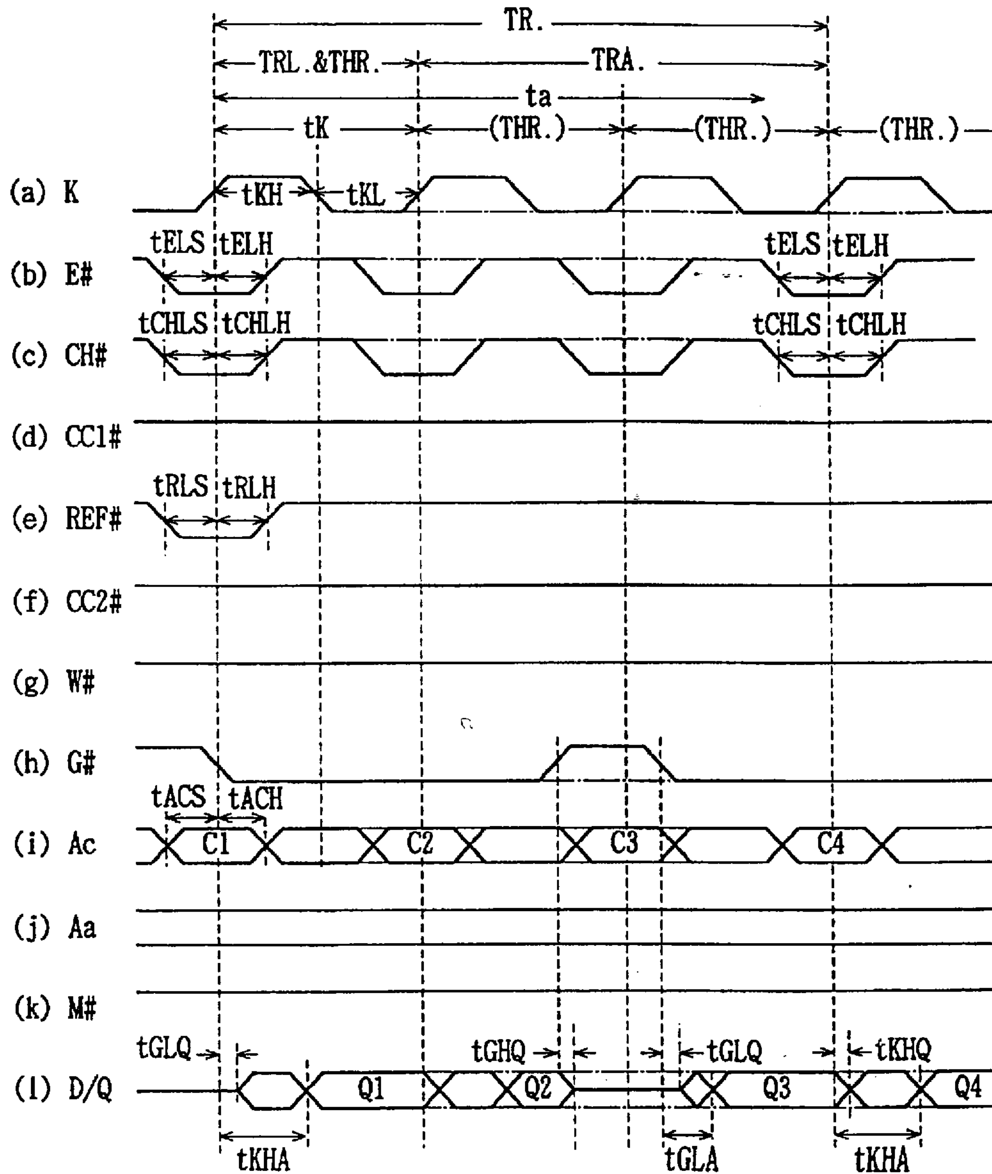


FIG. 133

LTRW:REFRESH ARRAY OPERATION WITH CACHE HIT WRITE (LOW POWER CONSUMPTION)

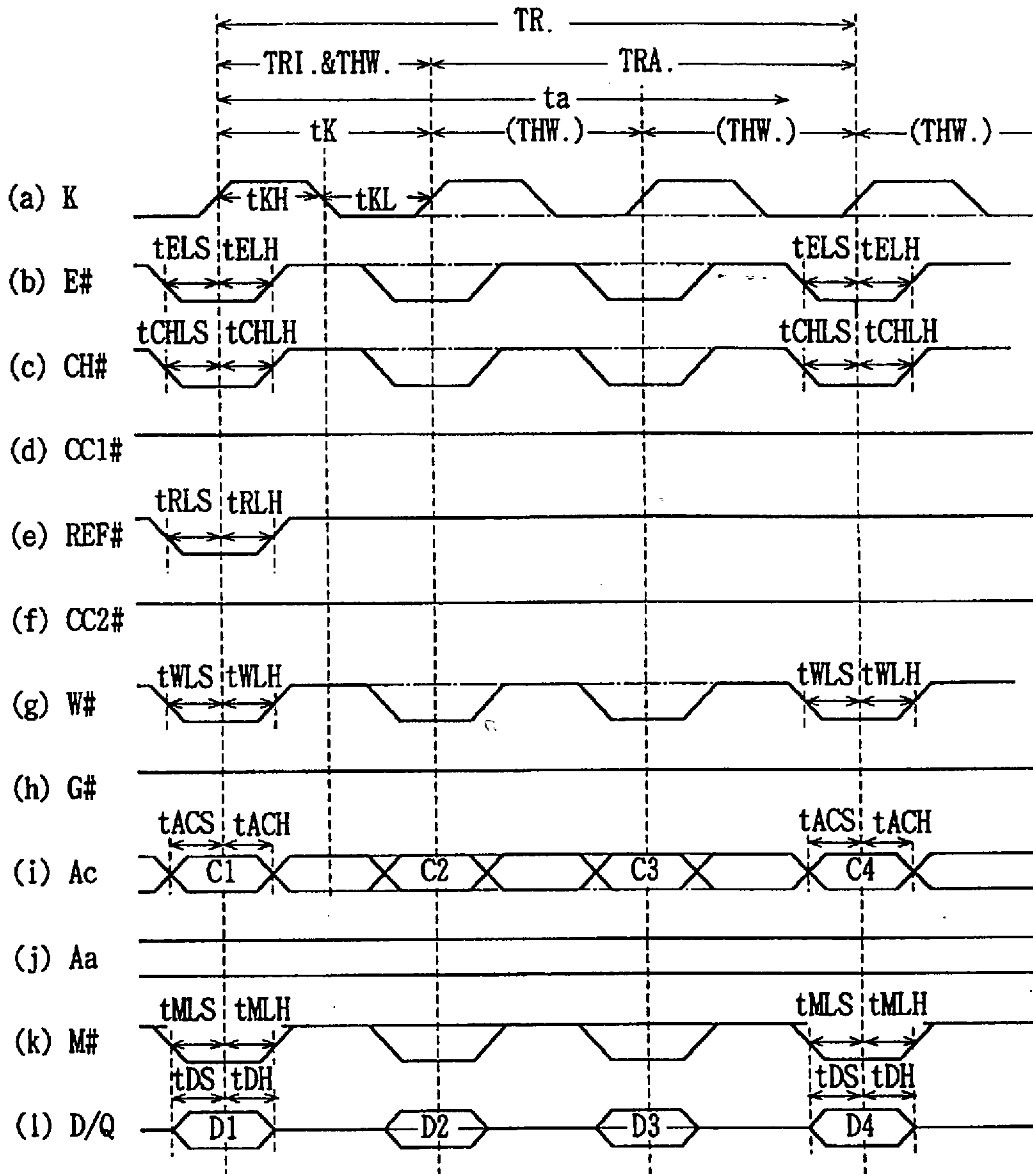


FIG. 134

LTCR:COUNTER CHECK READ OPERATION (LOW POWER CONSUMPTION)

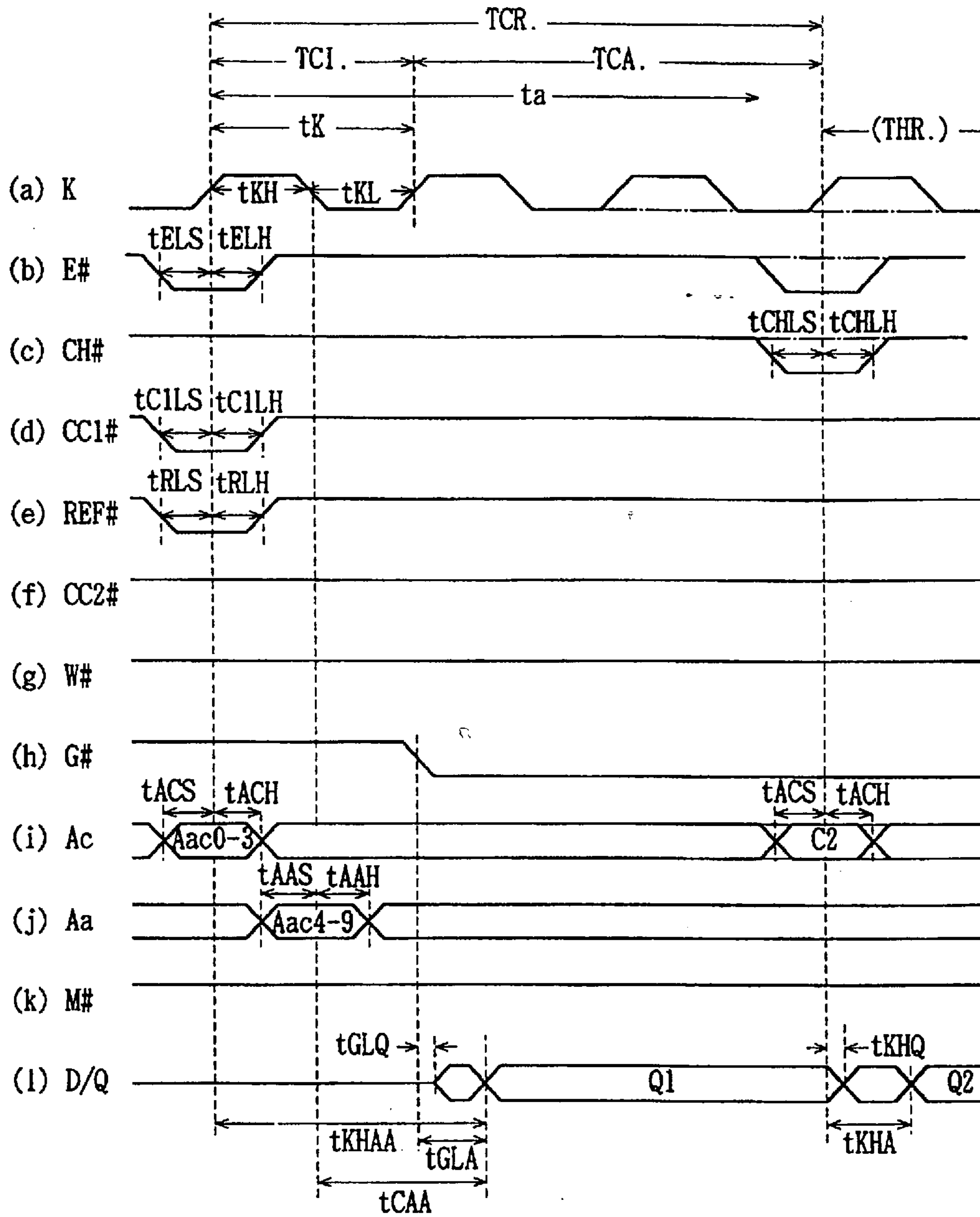


FIG. 135

LTCW:COUNTER CHECK WRITE OPERATION (LOW POWER CONSUMPTION)

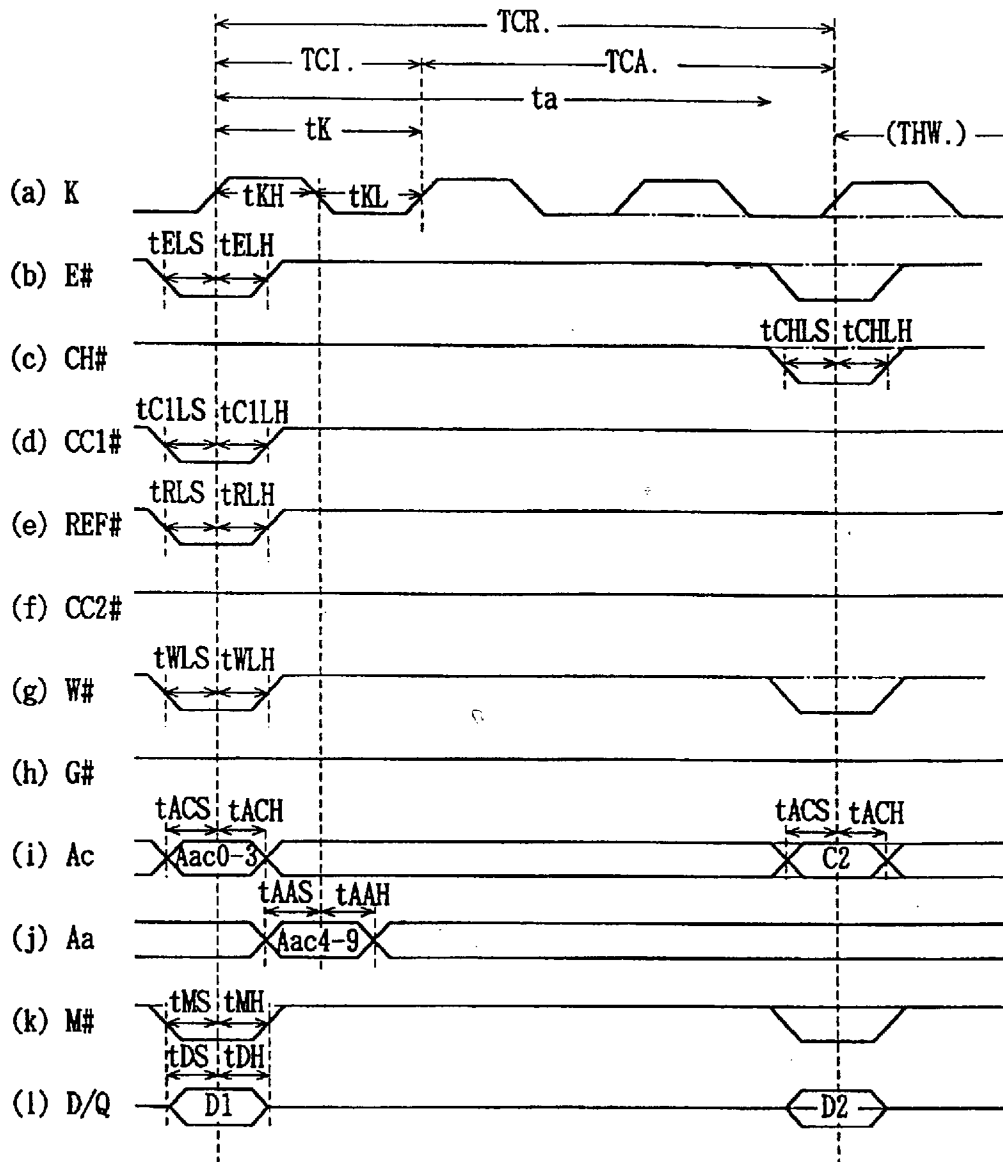


FIG. 136

LTG:COMMAND REGISTER SETTING OPERATION (LOW·POWER CONSUMPTION)

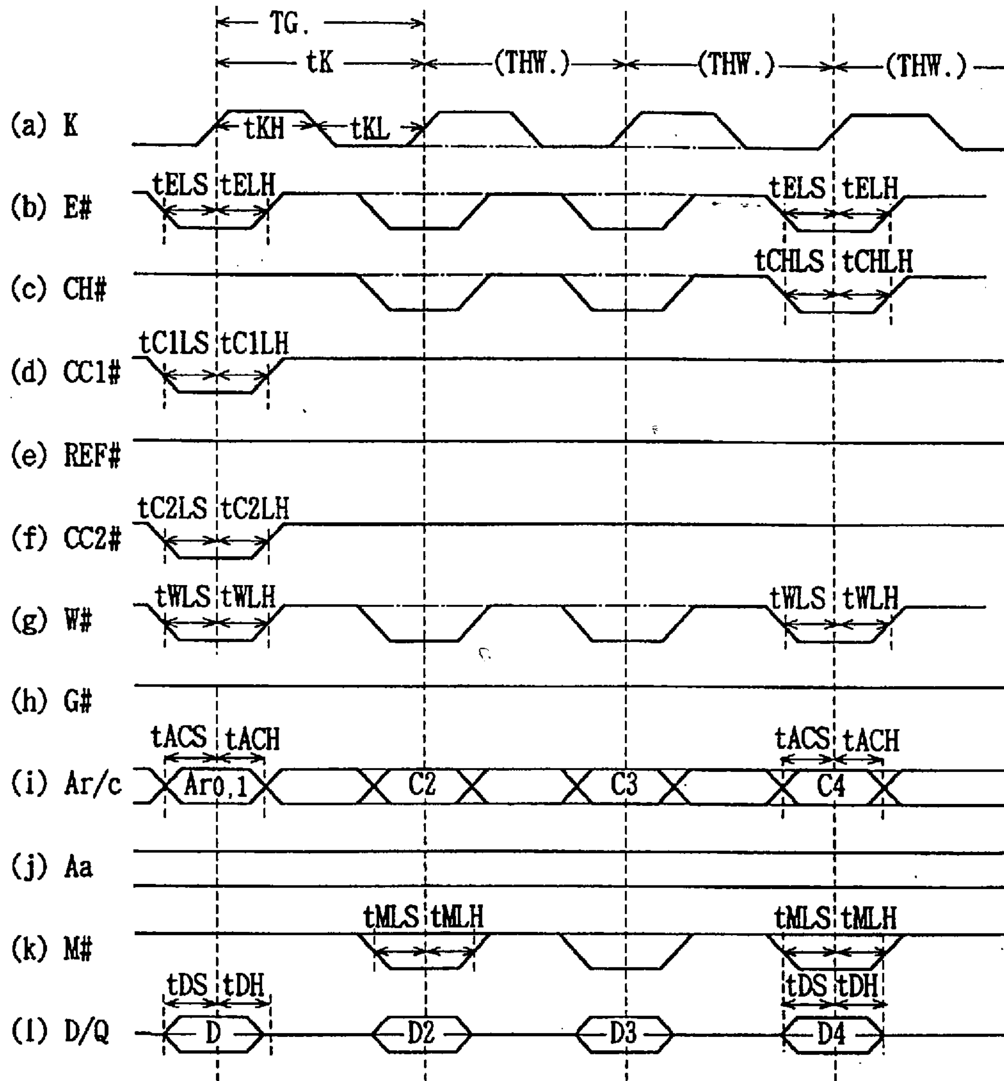


FIG. 137

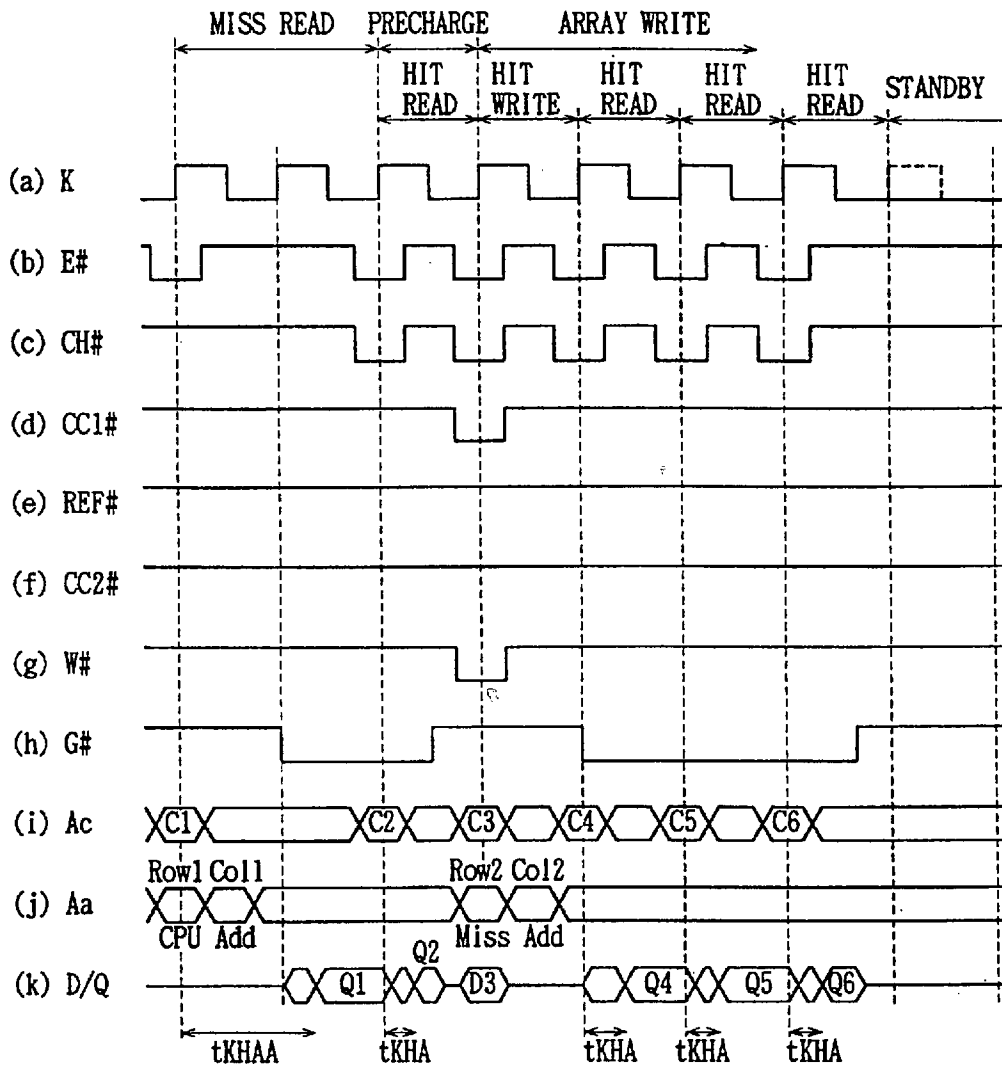


FIG. 138

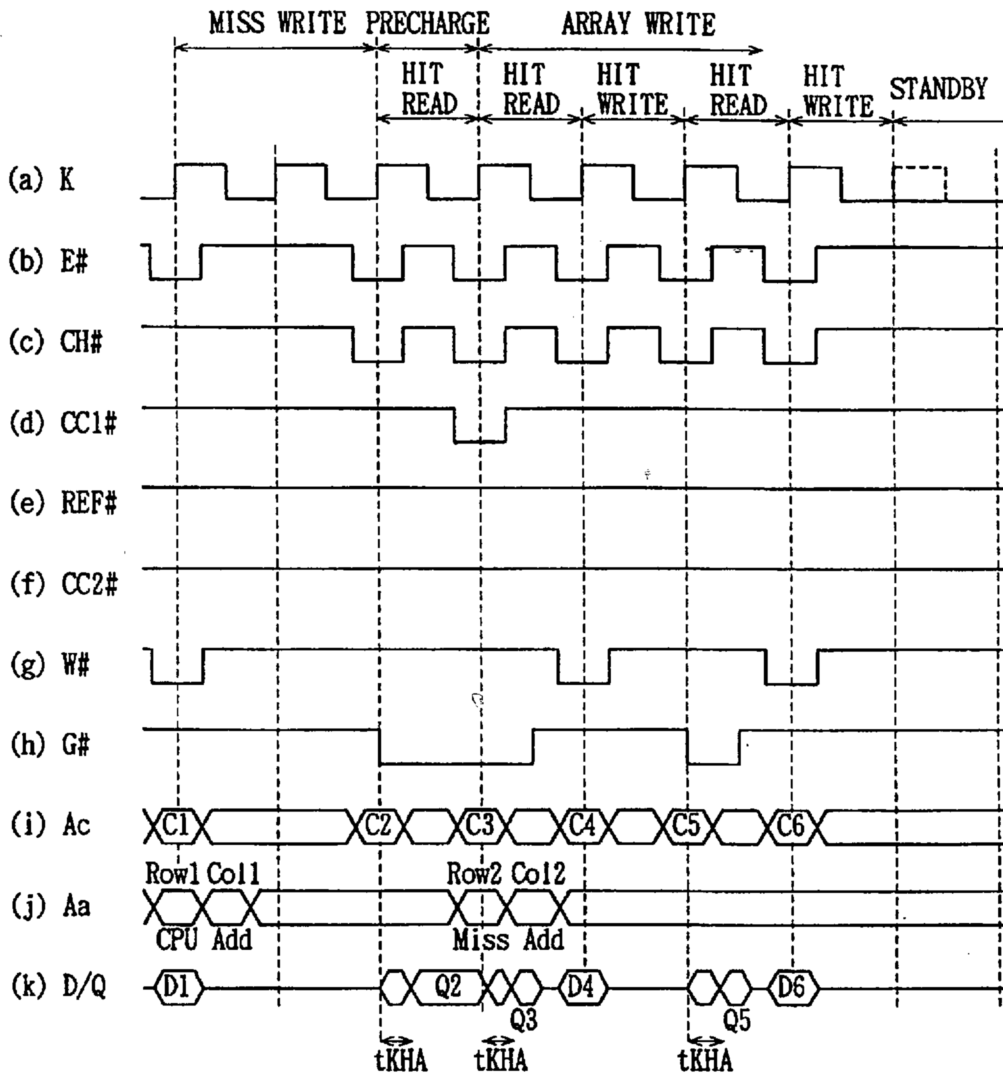


FIG. 139

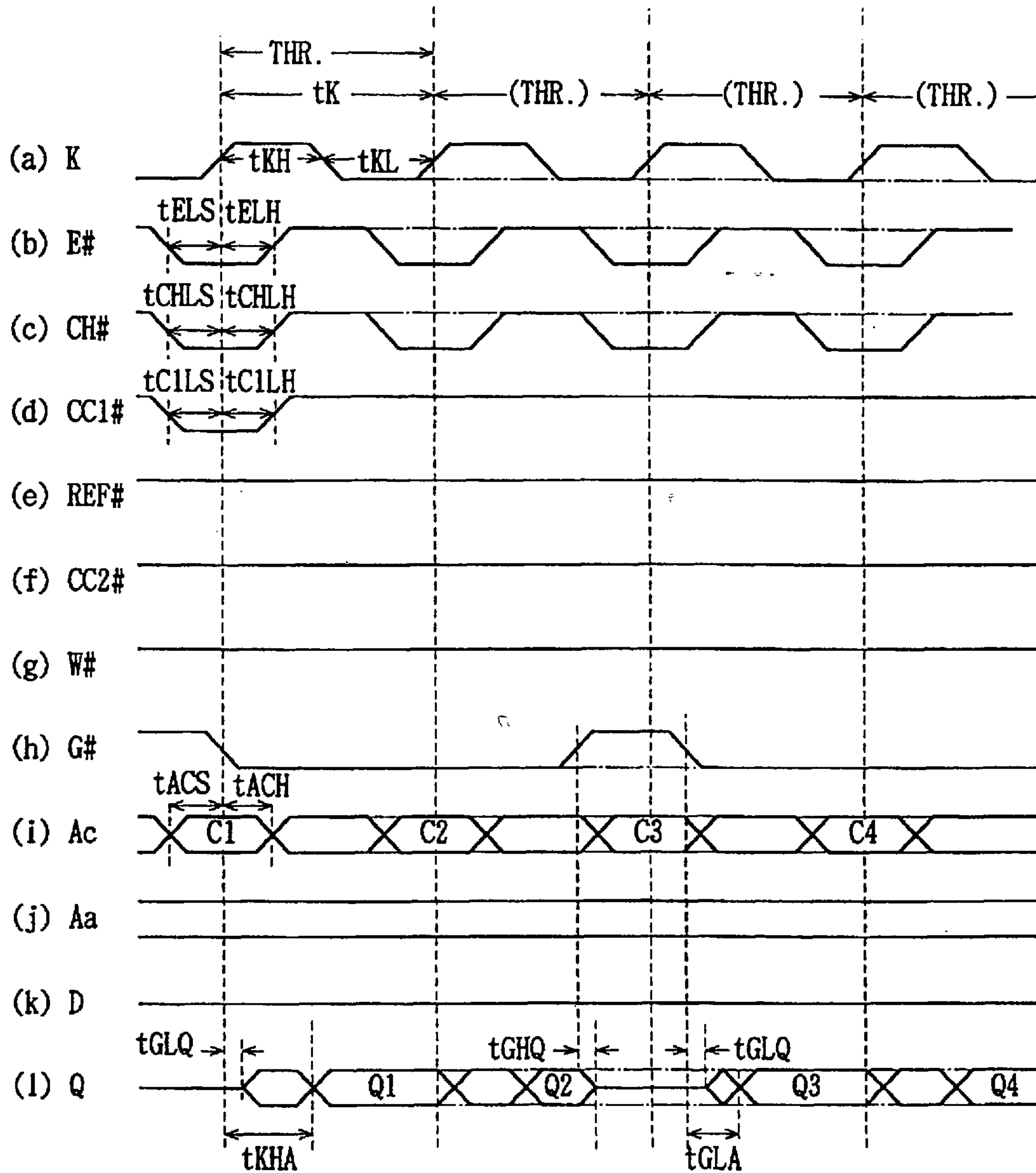


FIG. 140

THRL:CACHE HIT READ OPERATION (HIGH SPEED OPERATION)
(LATCH OUTPUT)

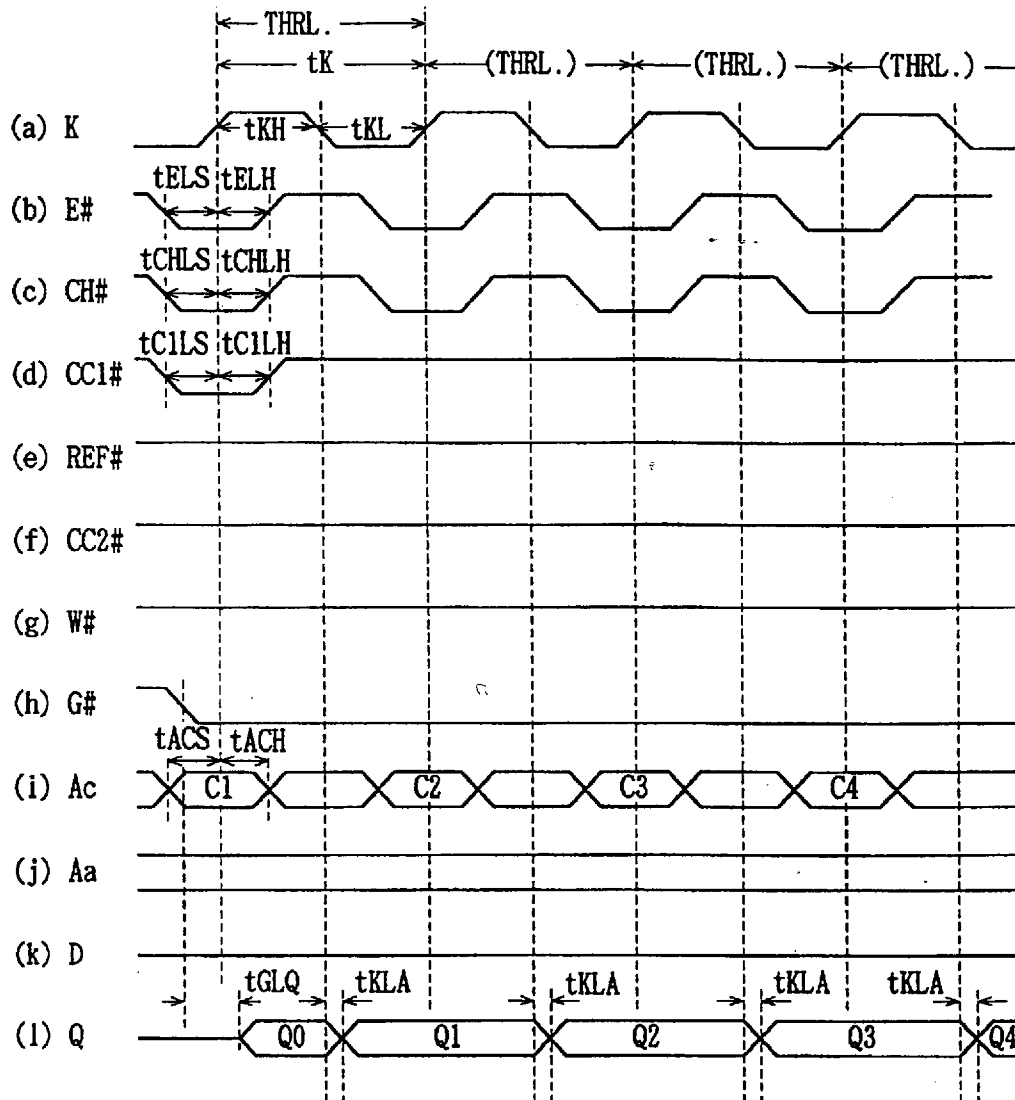


FIG. 141

THRR:CACHE HIT READ OPERATION (HIGH SPEED OPERATION)
(REGISTER OUTPUT)

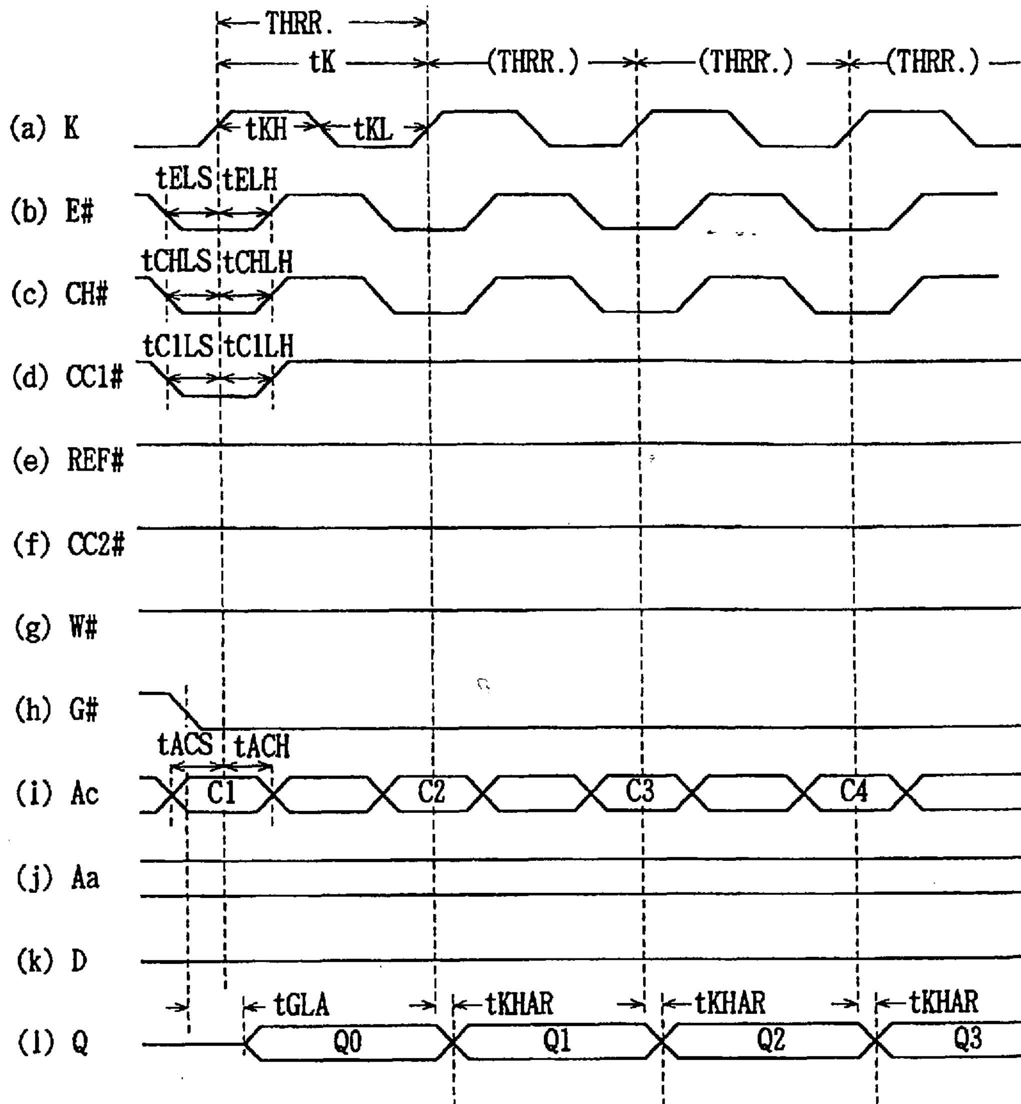


FIG. 142

THW:CACHE HIT WRITE OPERATION (HIGH SPEED OPERATION)

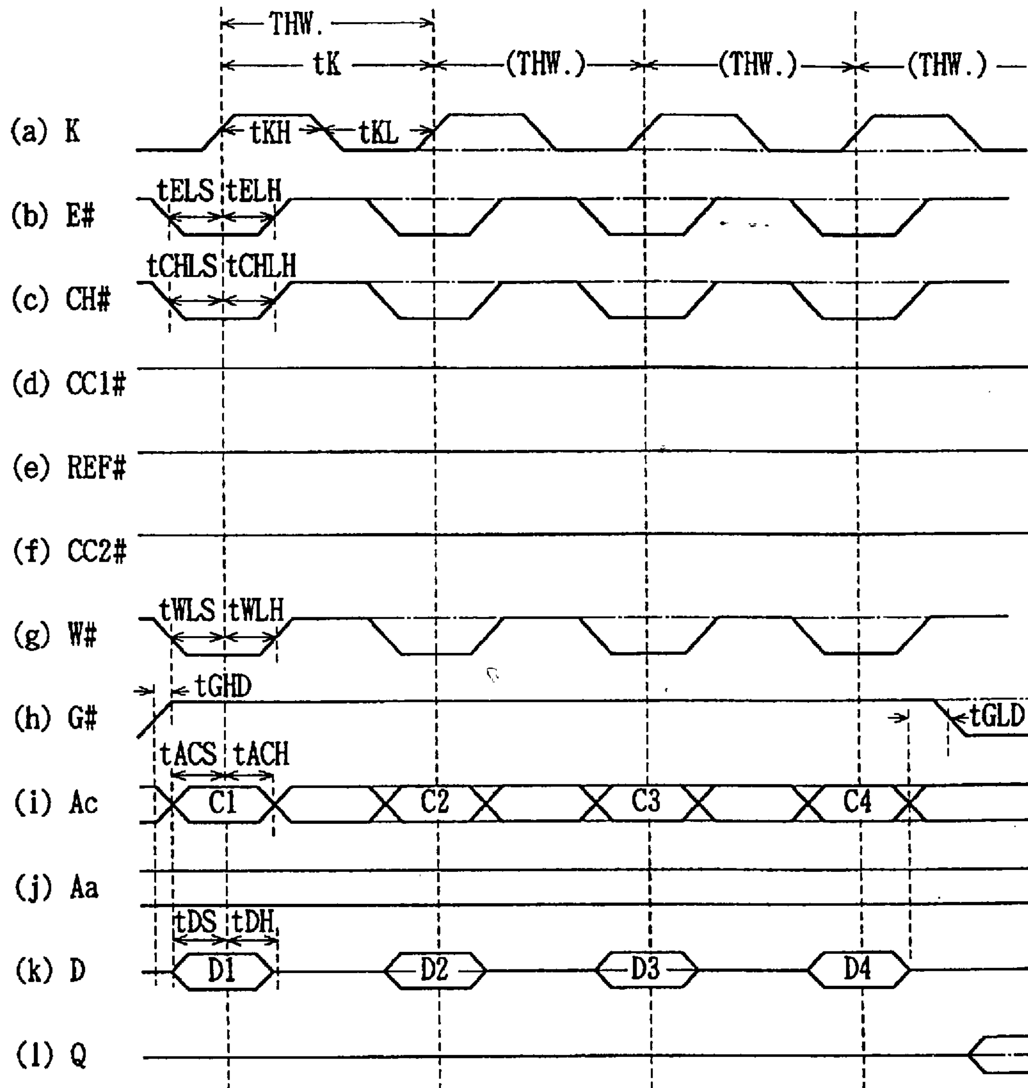


FIG. 143

TMMR:CACHE MISS READ OPERATION (HIGH SPEED OPERATION)

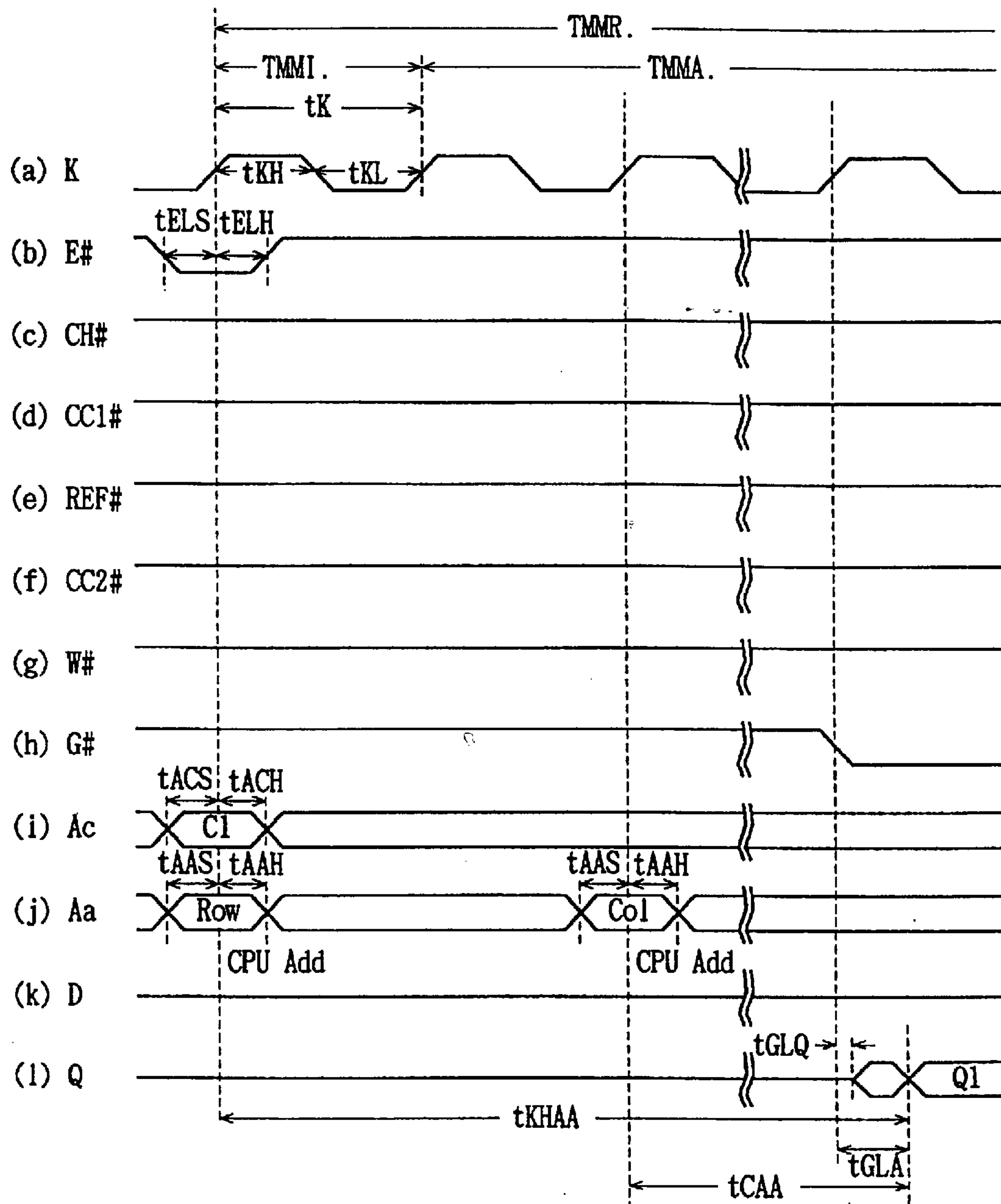


FIG. 144

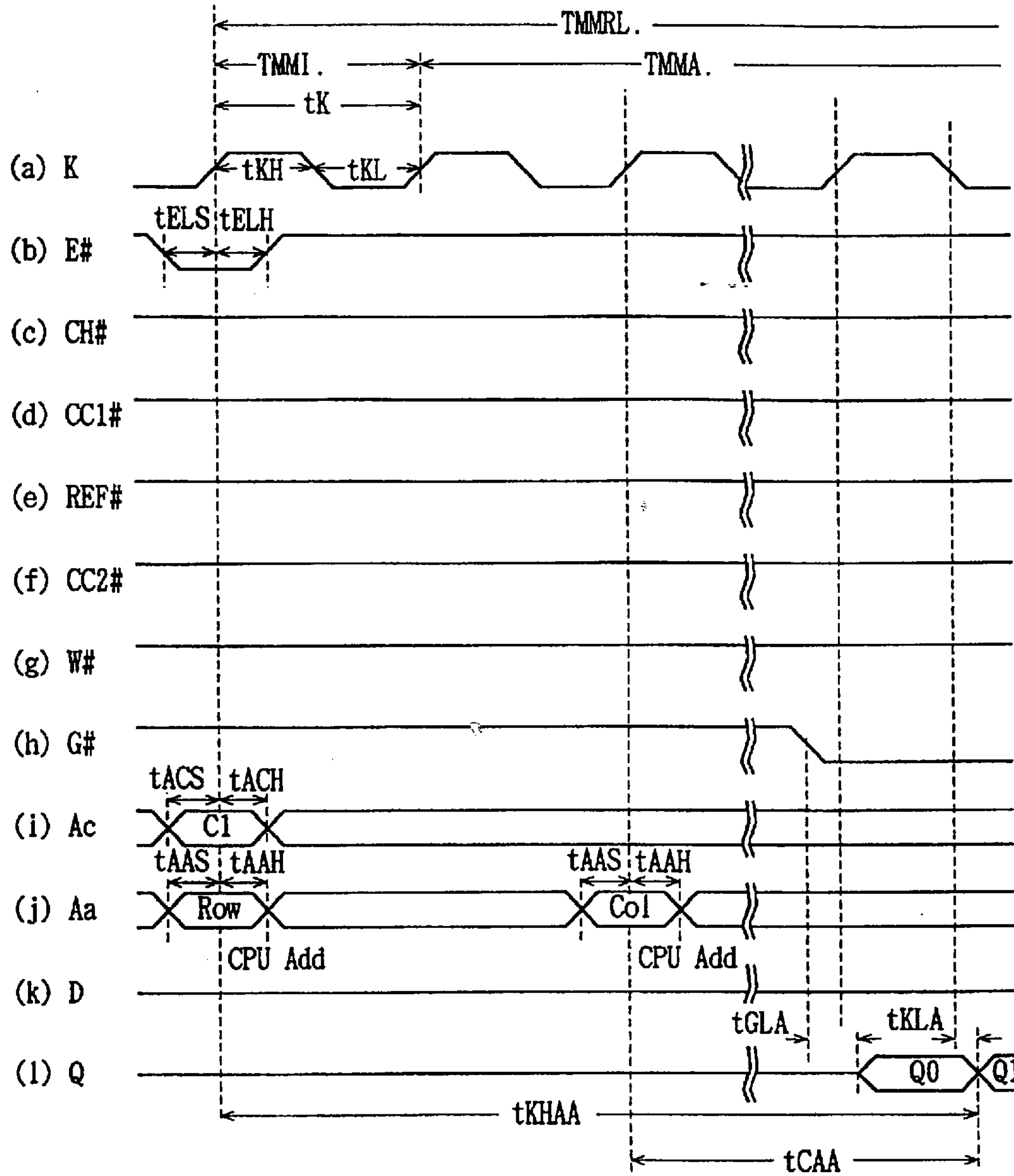


FIG. 145

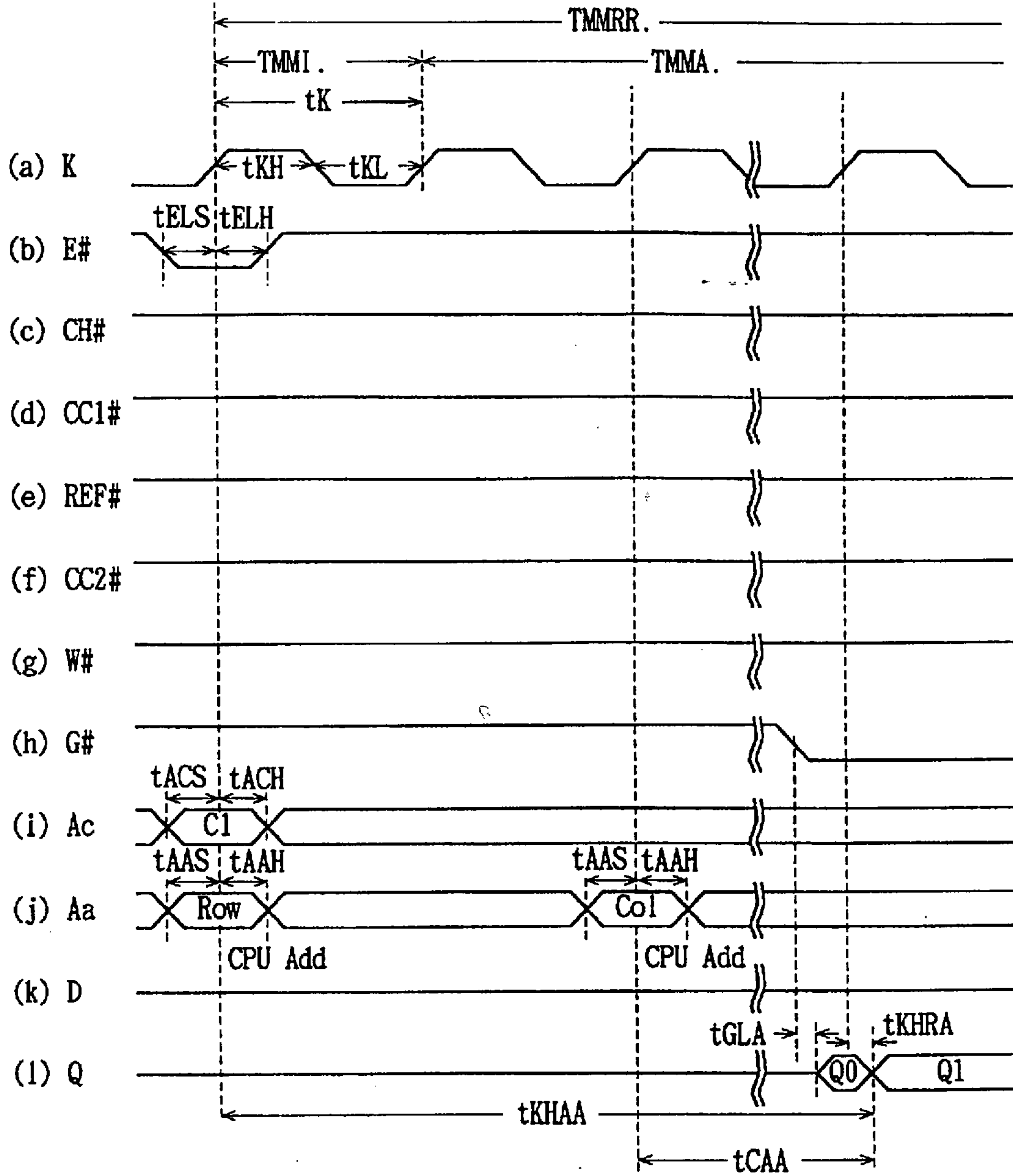
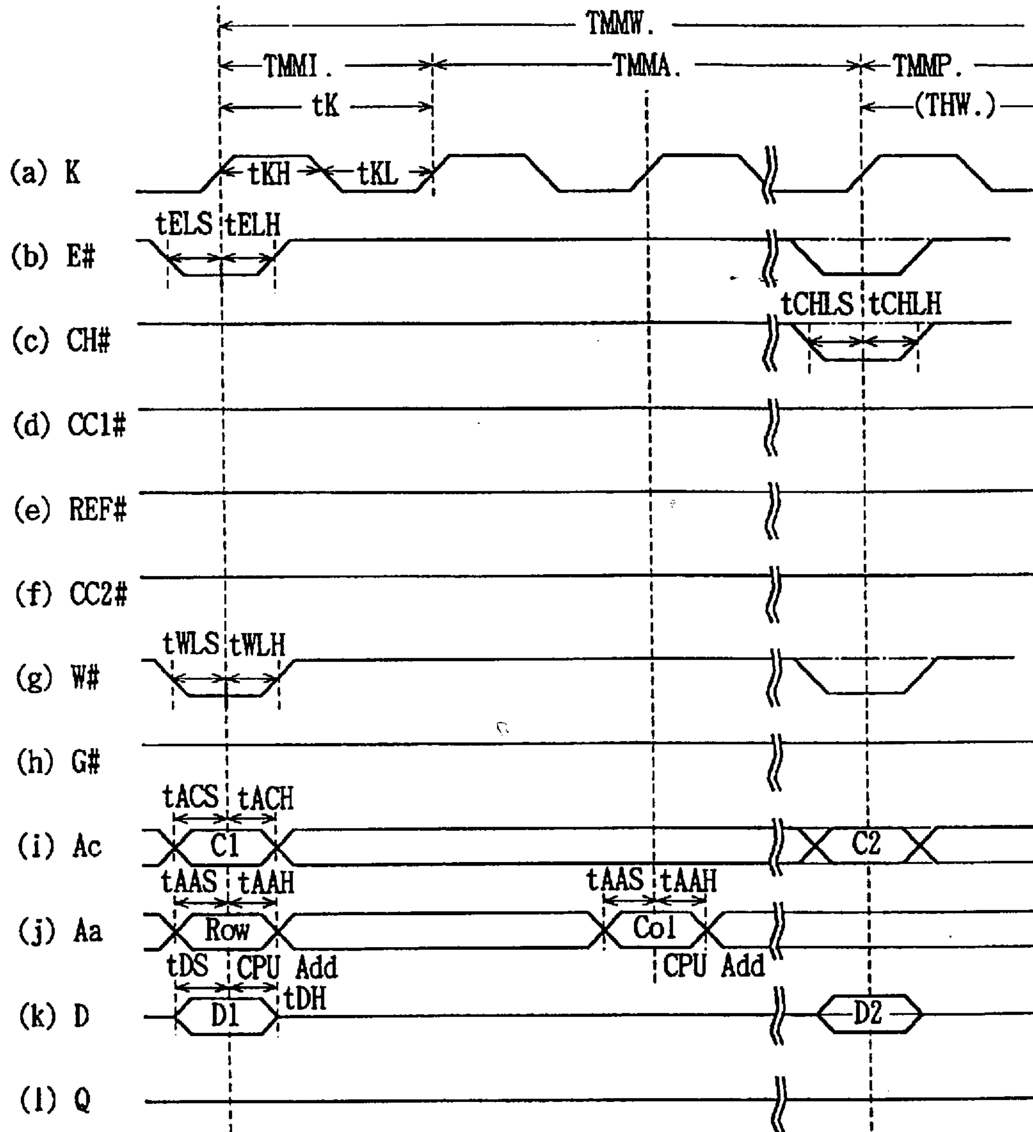


FIG. 146

TMMW:CACHE MISS WRITE OPERATION (HIGH SPEED OPERATION)



F I G. 1 4 7

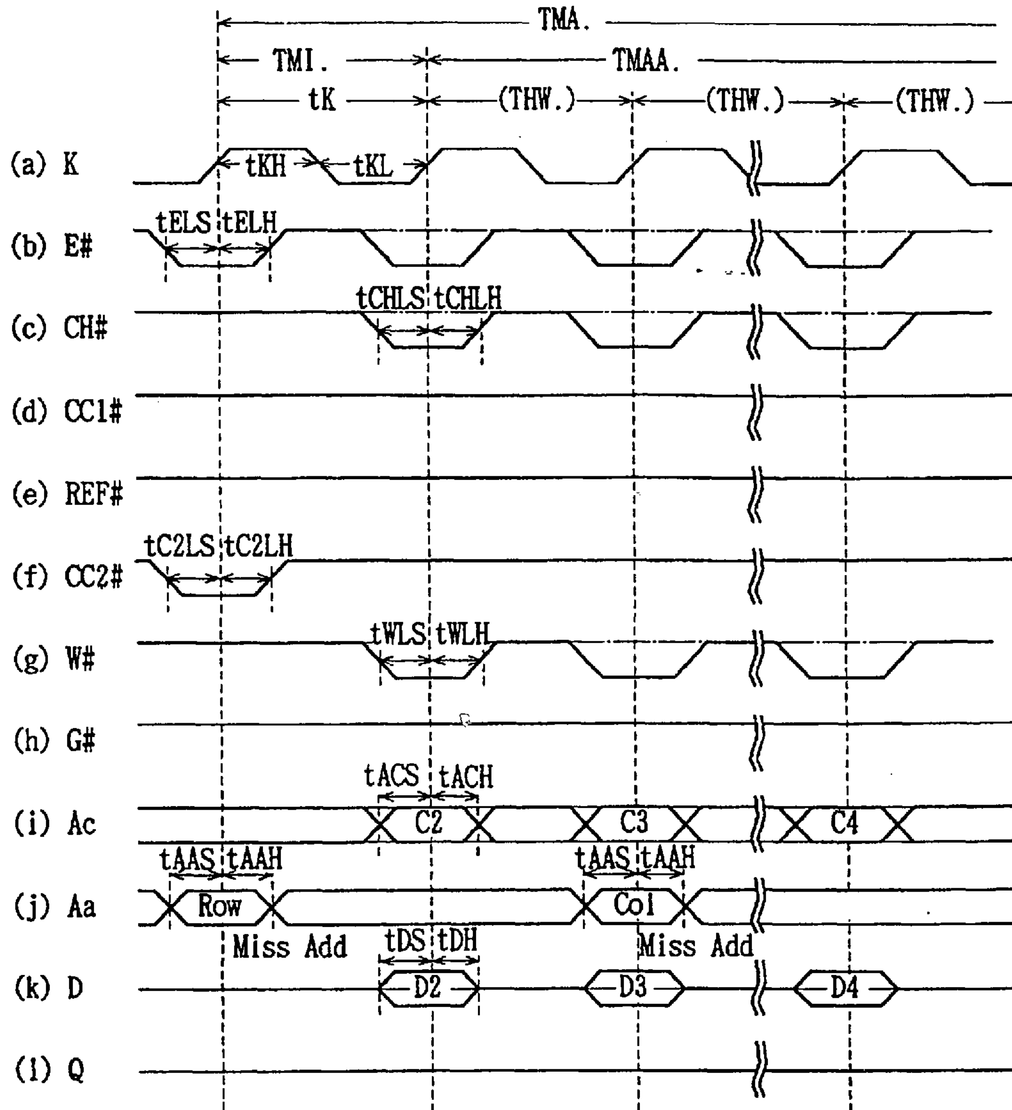


FIG. 148

TMAR:ARRAY WRITE OPERATION WITH CACHE HIT READ (HIGH SPEED OPERATION)

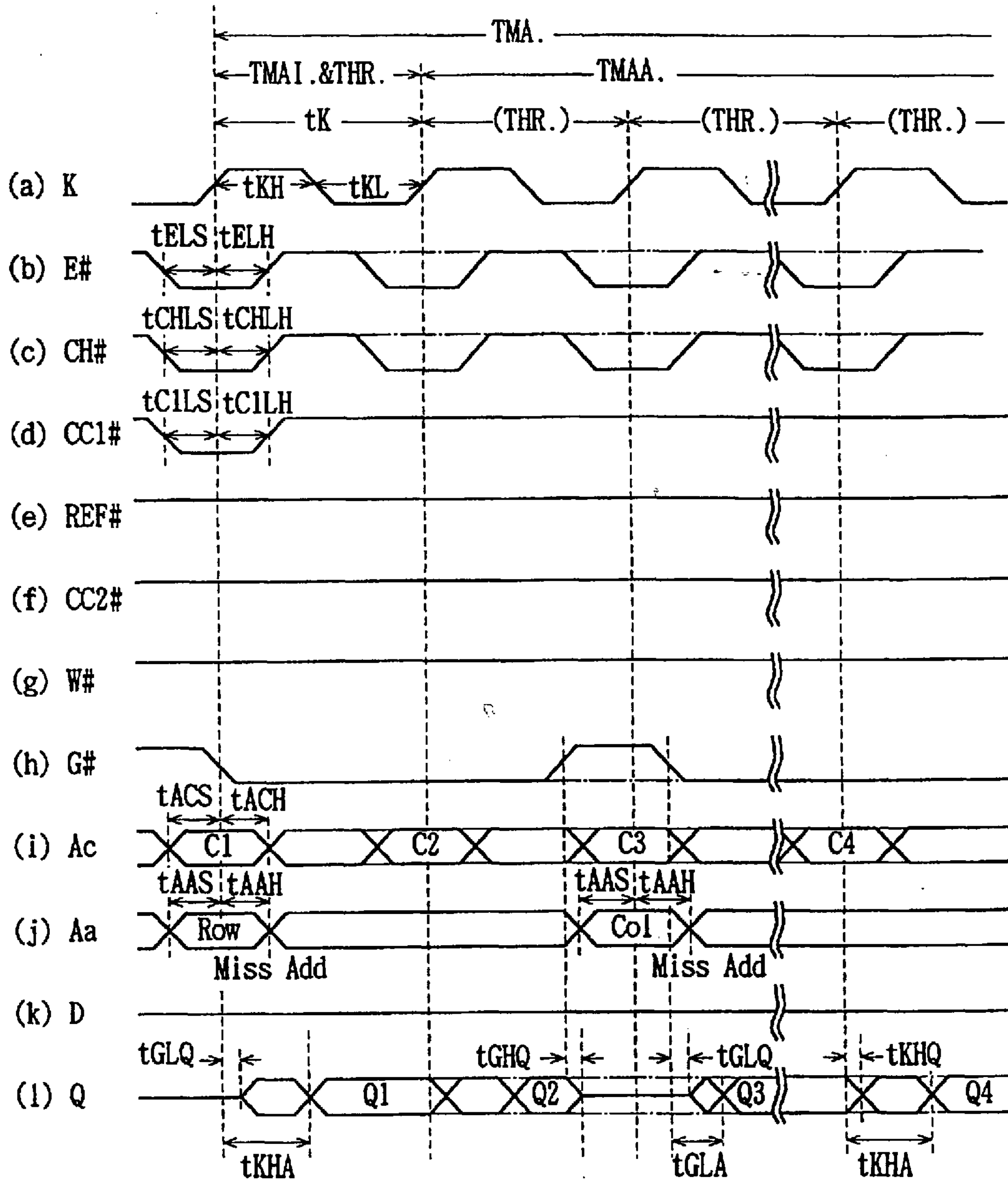


FIG. 149

TMARL:ARRAY WRITE OPERATION WITH CACHE HIT READ (HIGH SPEED OPERATION) (LATCH OUTPUT)

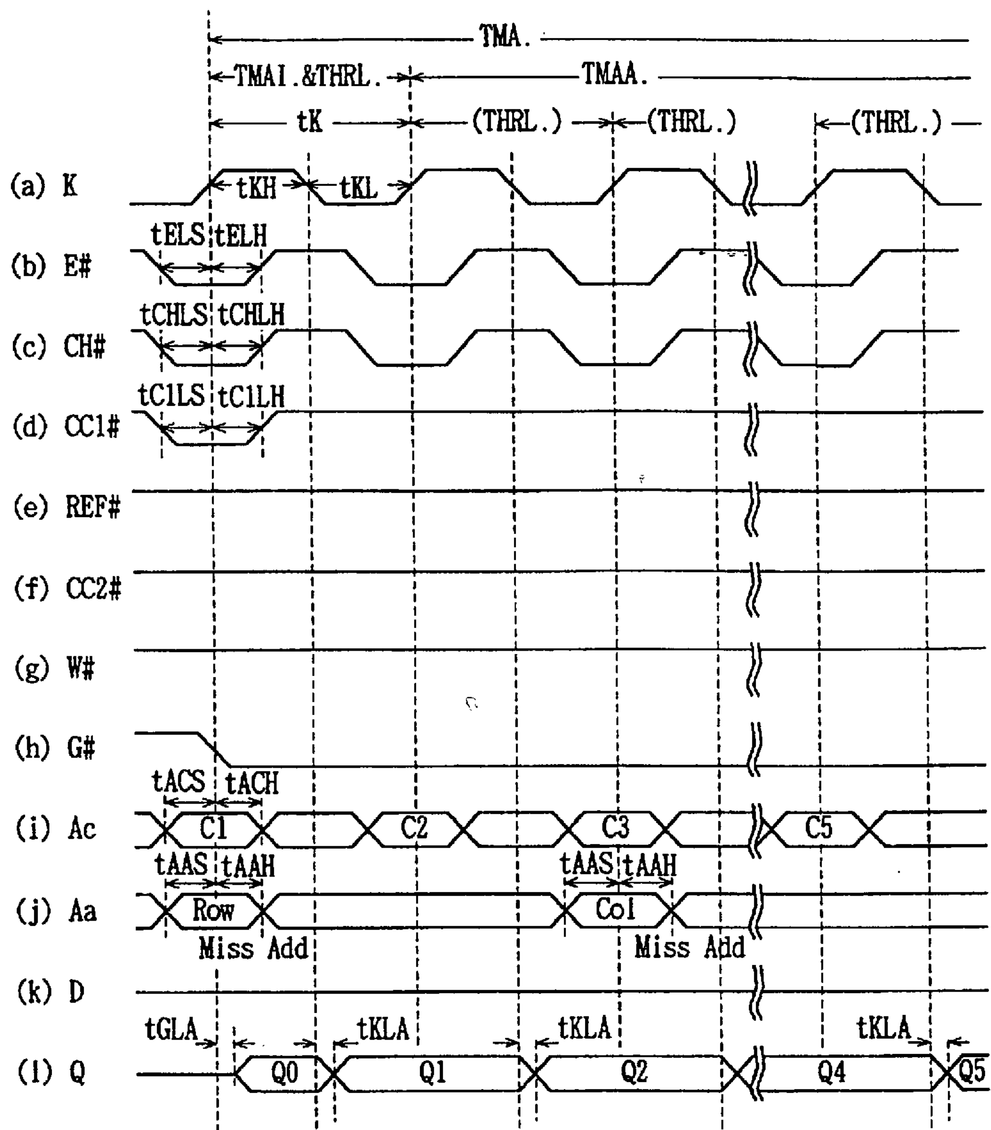


FIG. 150

TMARR:ARRAY WRITE OPERATION WITH CACHE HIT READ (HIGH SPEED OPERATION)
(REGISTER OUTPUT)

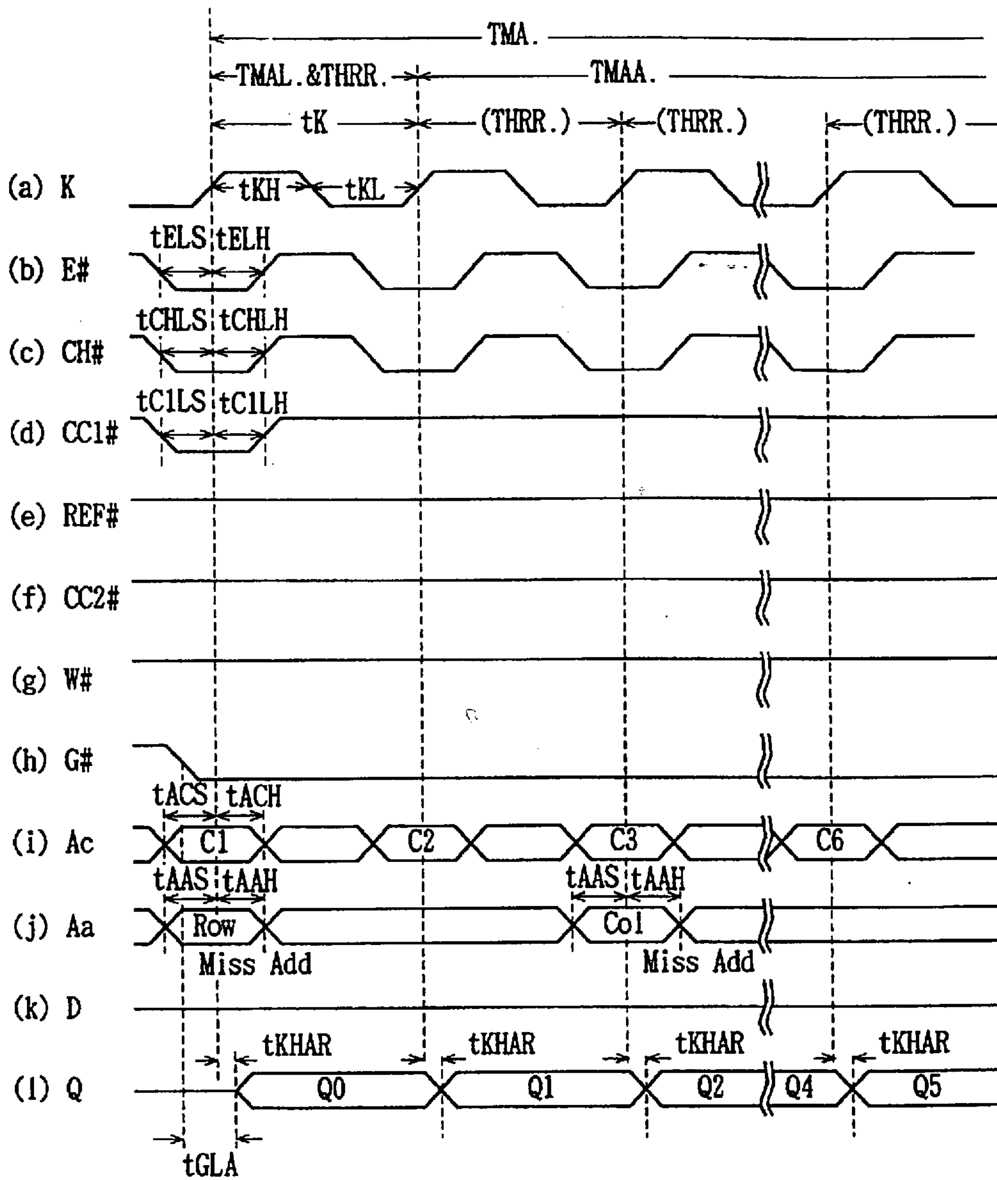


FIG. 151

TMAW:ARRAY WRITE OPERATION WITH CACHE HIT WRITE (HIGH SPEED OPERATION)

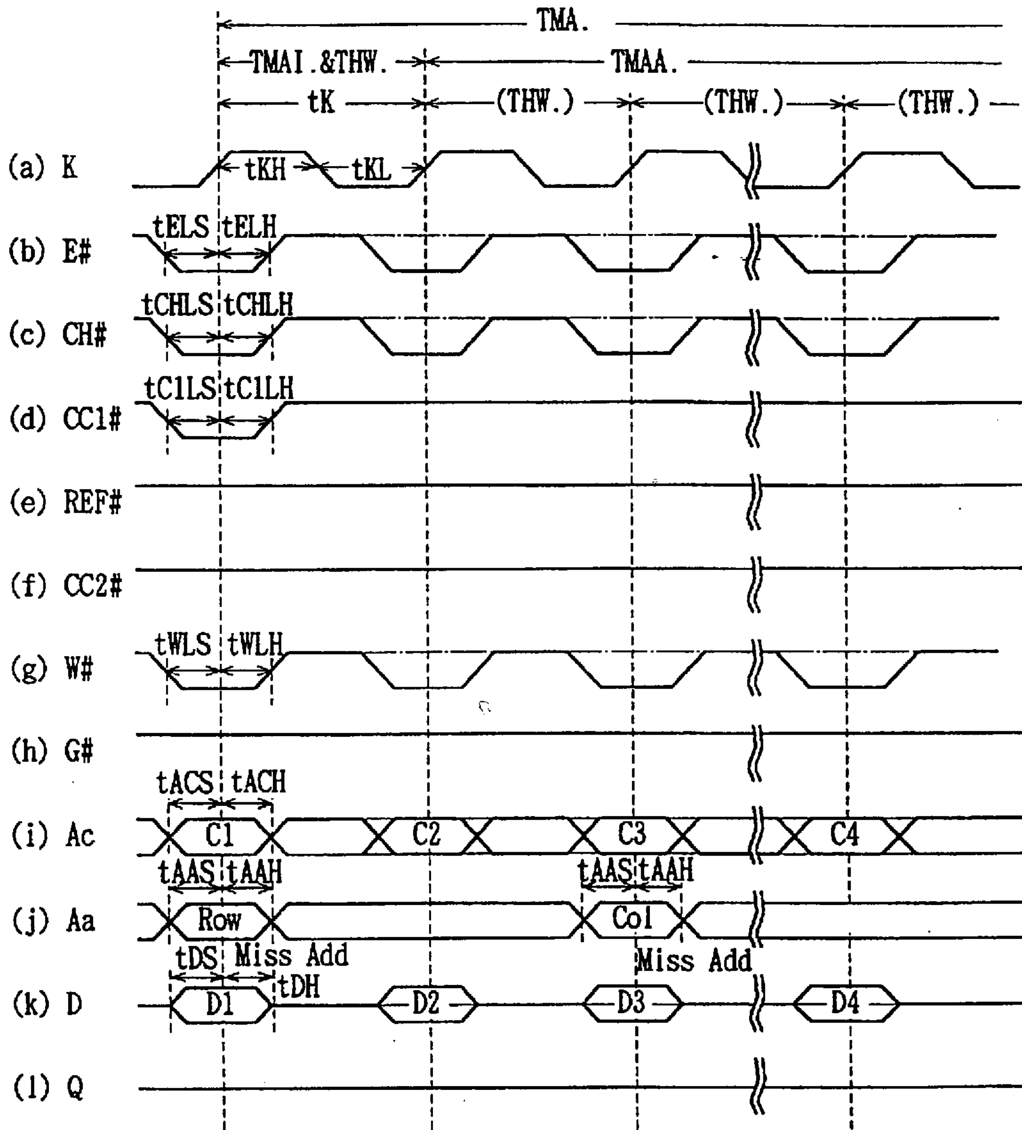


FIG. 152

TDR:DIRECT ARRAY READ OPERATION (HIGH SPEED OPERATION)

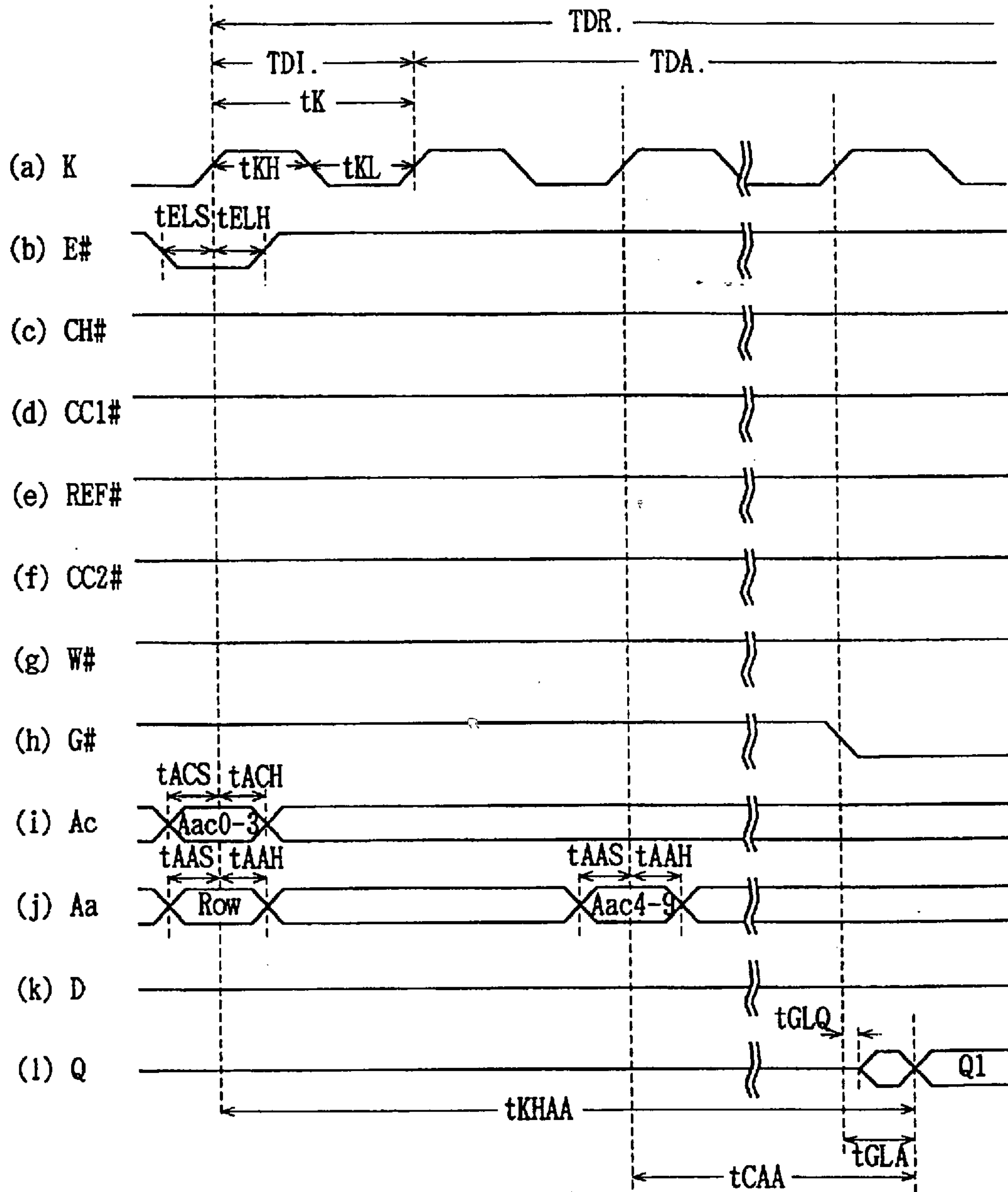


FIG. 153

TDW:DIRECT ARRAY WRITE OPERATION (HIGH SPEED OPERATION)

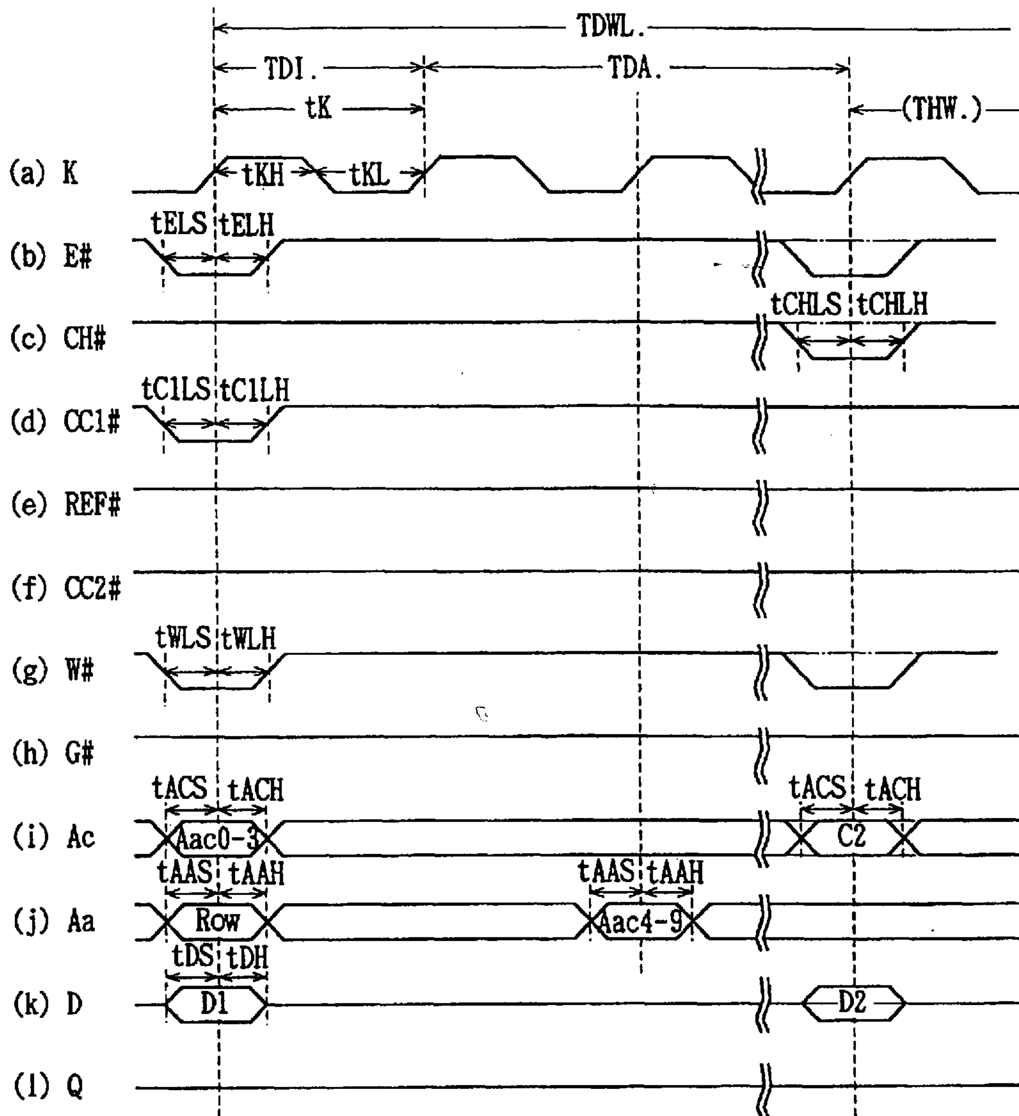


FIG. 154

TR:REFRESH ARRAY OPERATION (HIGH SPEED OPERATION)

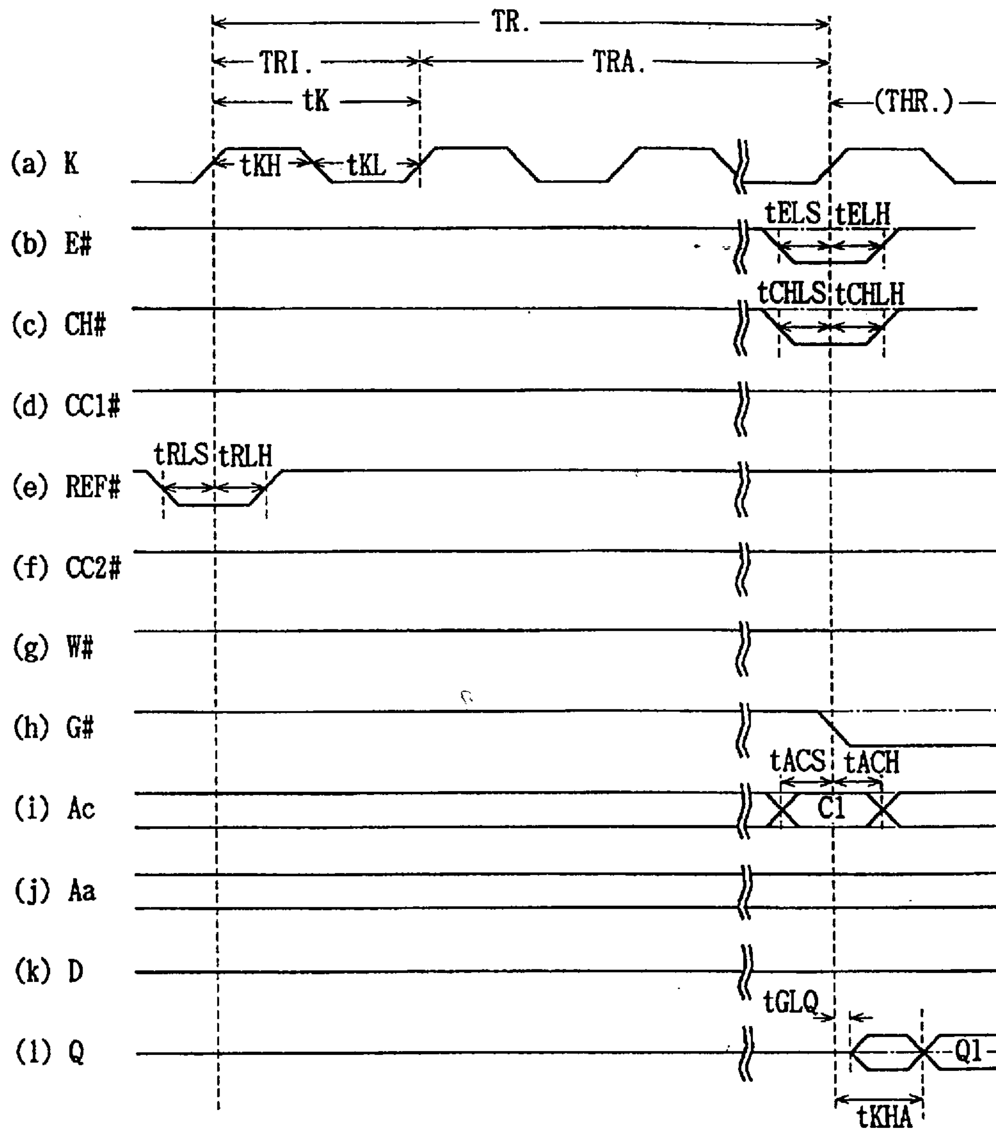


FIG. 155

TRR:REFRESH OPERATION WITH CACHE HIT READ (HIGH SPEED OPERATION)

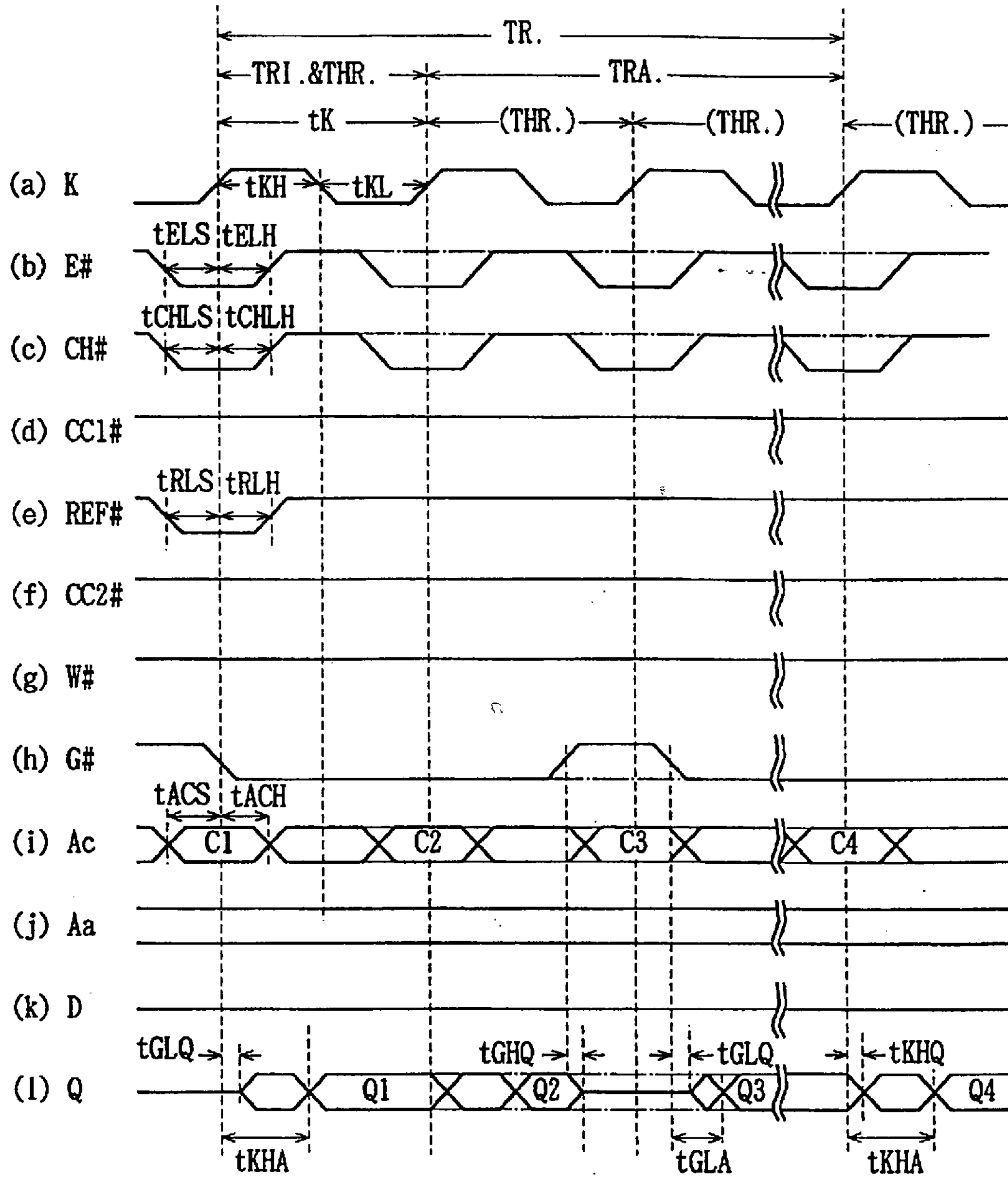


FIG. 156

TRW:REFRESH ARRAY OPERATION WITH CACHE WRITE (HIGH SPEED OPERATION)

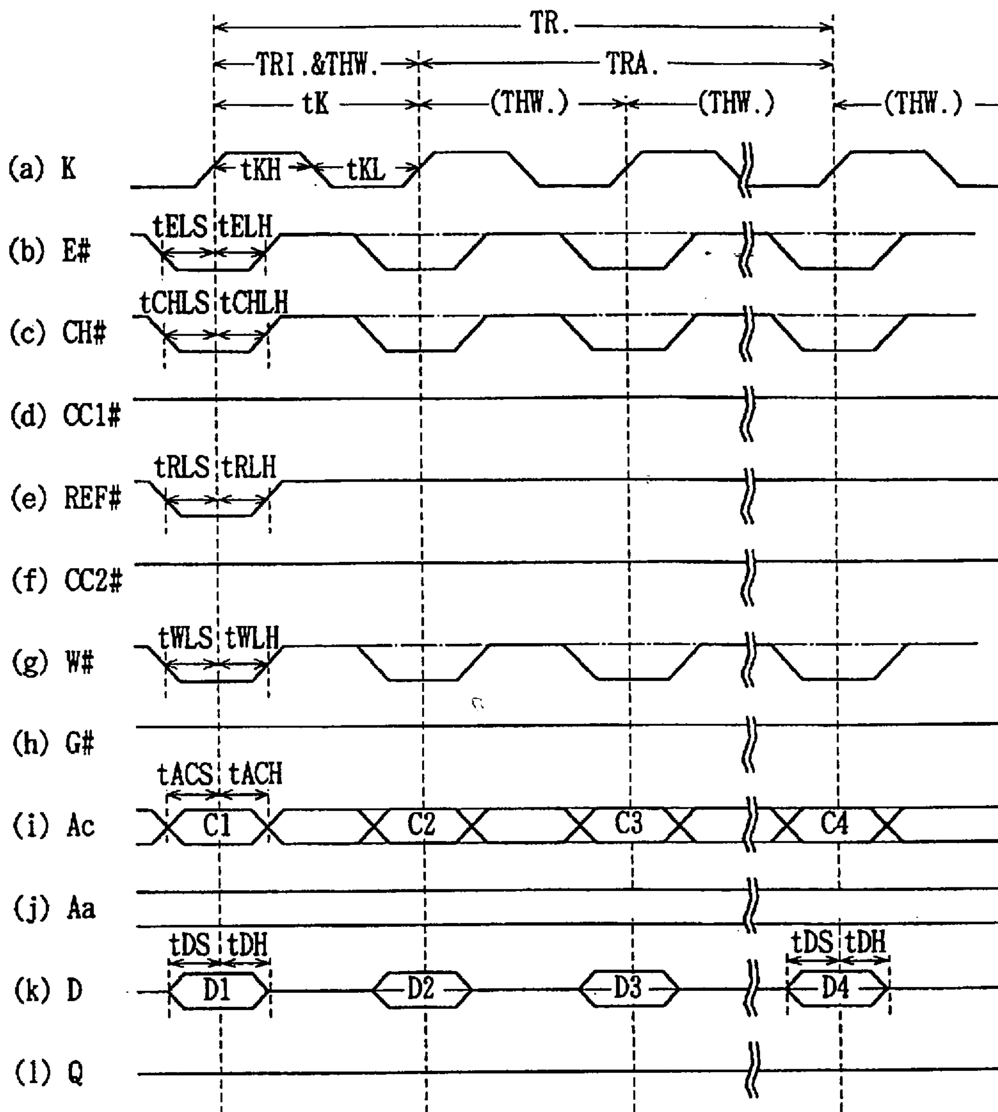


FIG. 157

TCR:COUNTER CHECK OPERATION (HIGH SPEED OPERATION)

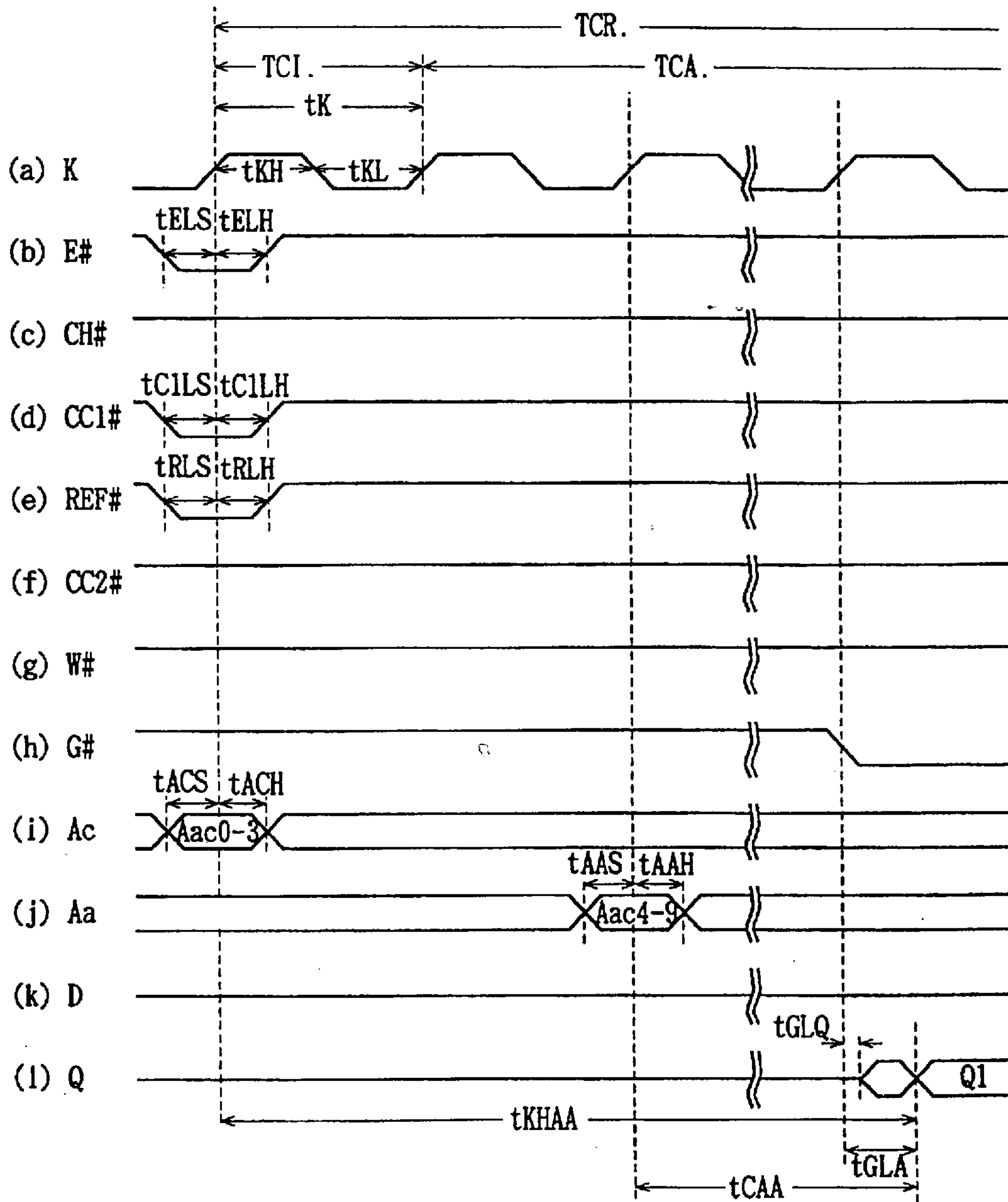


FIG. 158

TCW:COUNTER CHECK WRITE OPERATION (HIGH SPEED OPERATION)

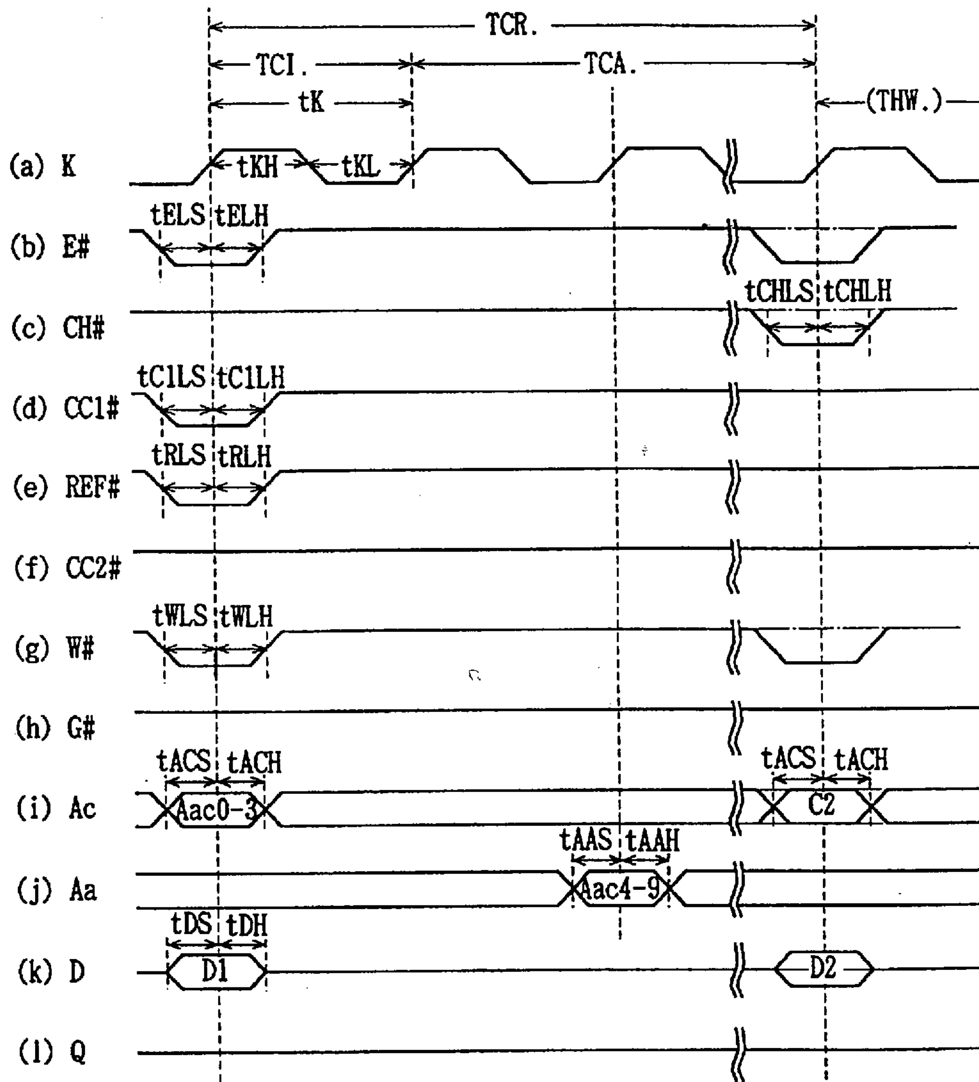


FIG. 159

TG:COMMAND REGISTER SETTING OPERATION (HIGH SPEED OPERATION)

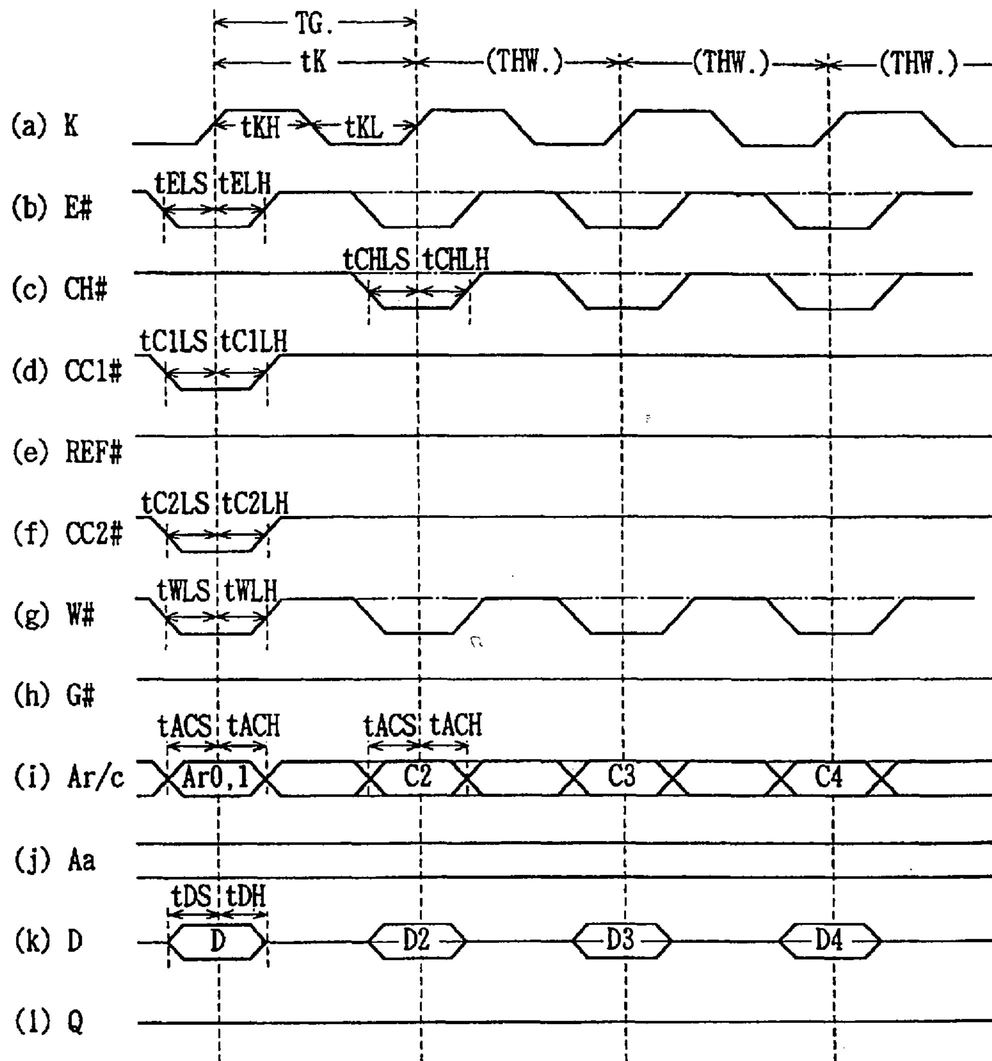


FIG. 160

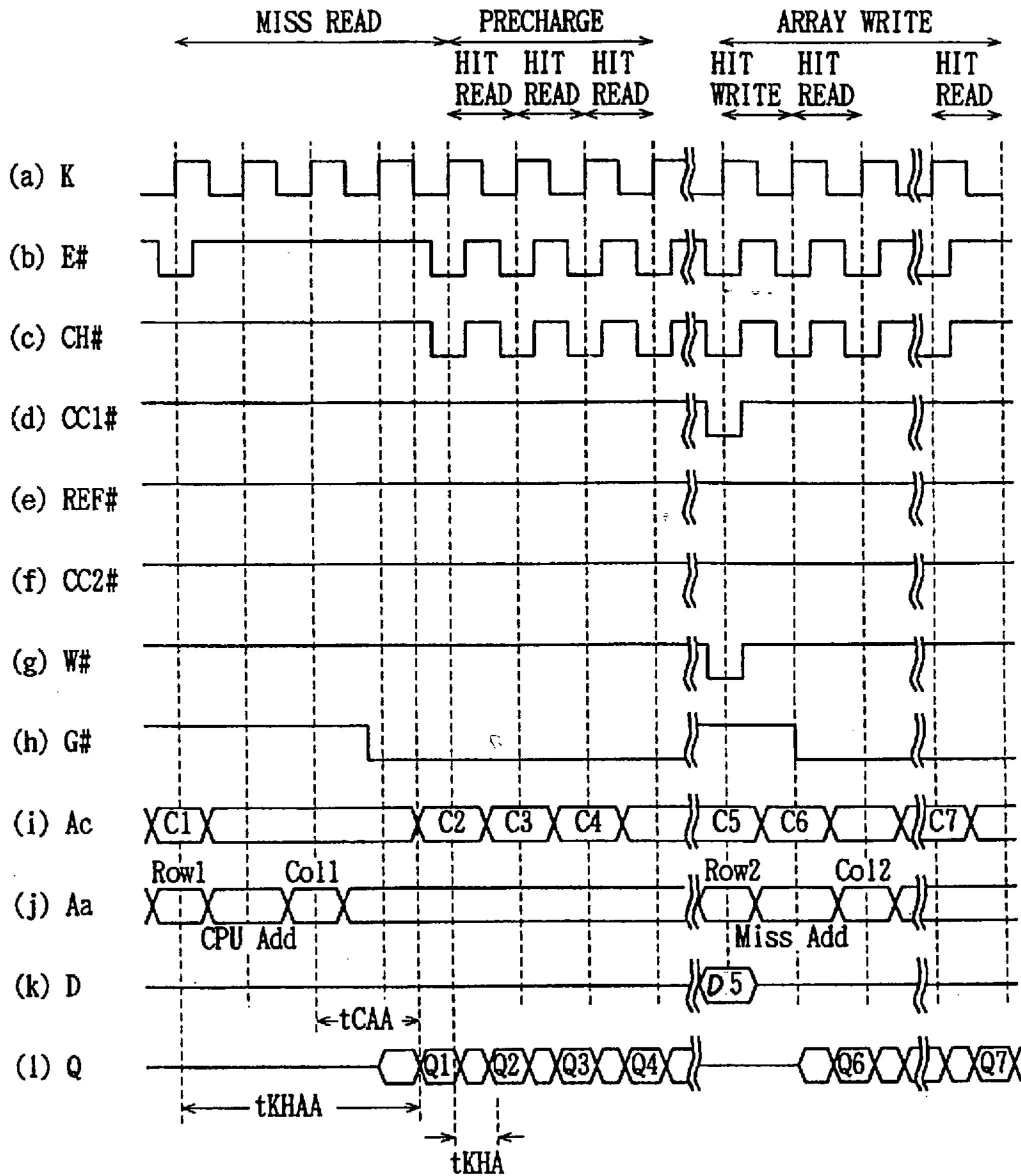
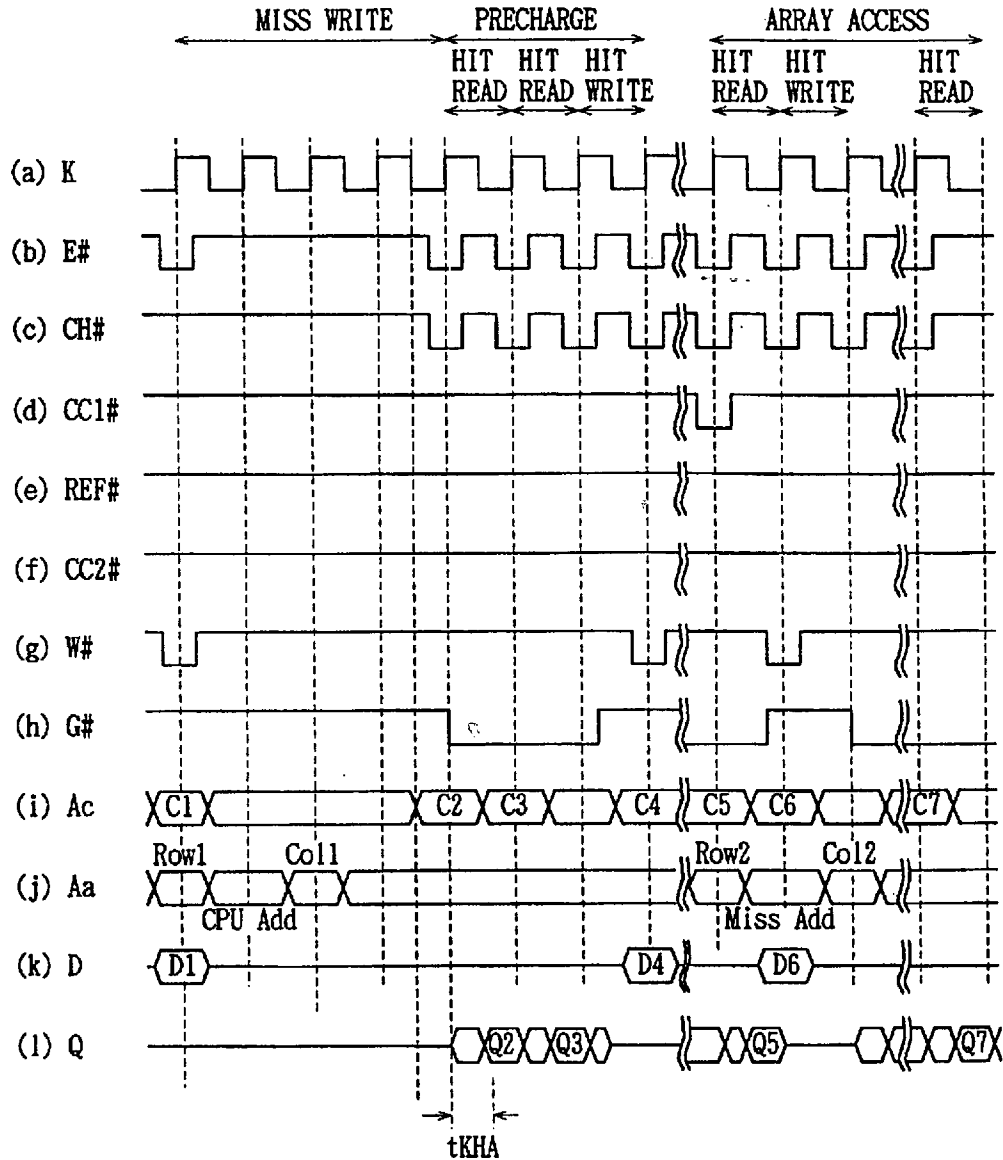


FIG. 161



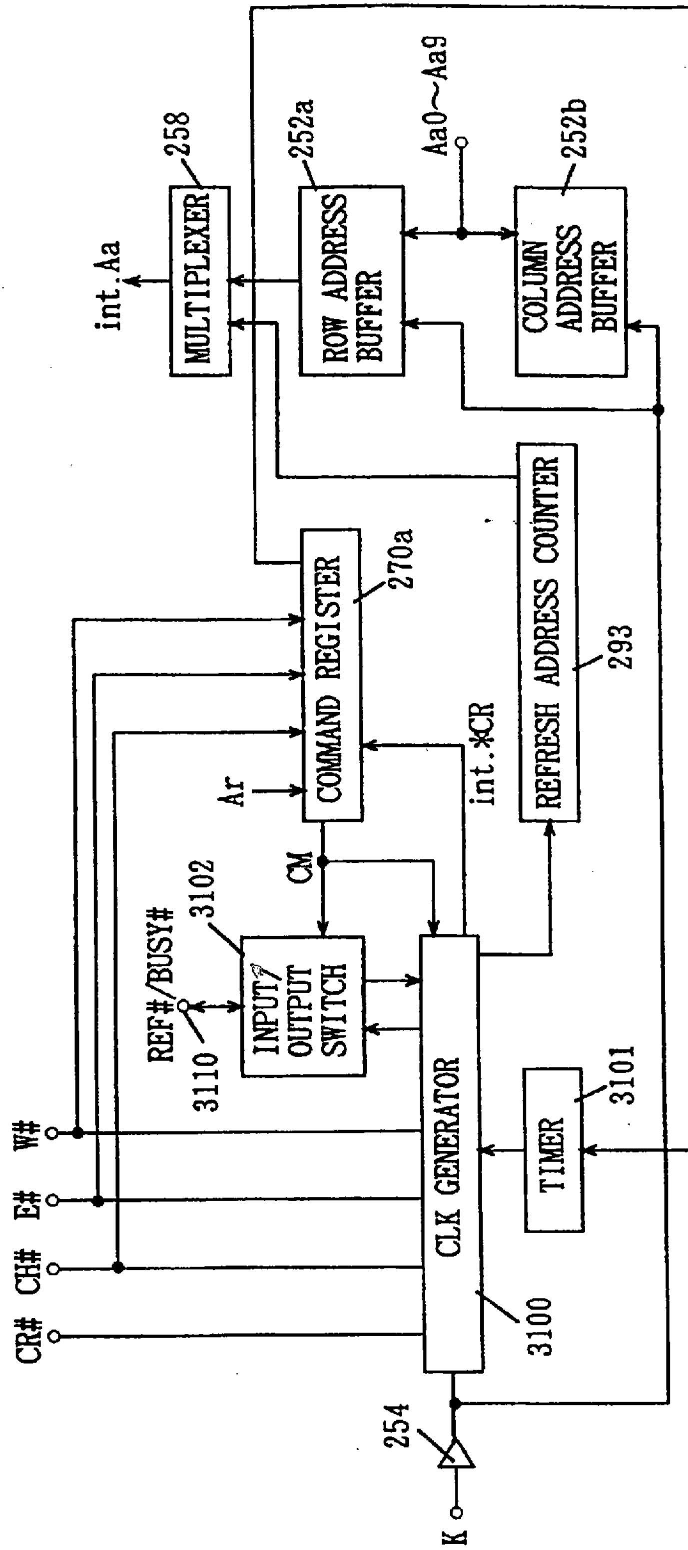

F I G. 1 6 2
int. Aa
MULTIPLEXER
258
ROW ADDRESS BUFFER
252a
Aa0~Aa9
COLUMN ADDRESS BUFFER
252b
COMMAND REGISTER
270a
REFRESH ADDRESS COUNTER
293
Ar
int.*CR
CM
REF#/BUSY#
3102
3110
INPUT/ OUTPUT SWITCH
CLK GENERATOR
3100
TIMER
3101
W#
E#
CH#
CR#
254
K

FIG. 163

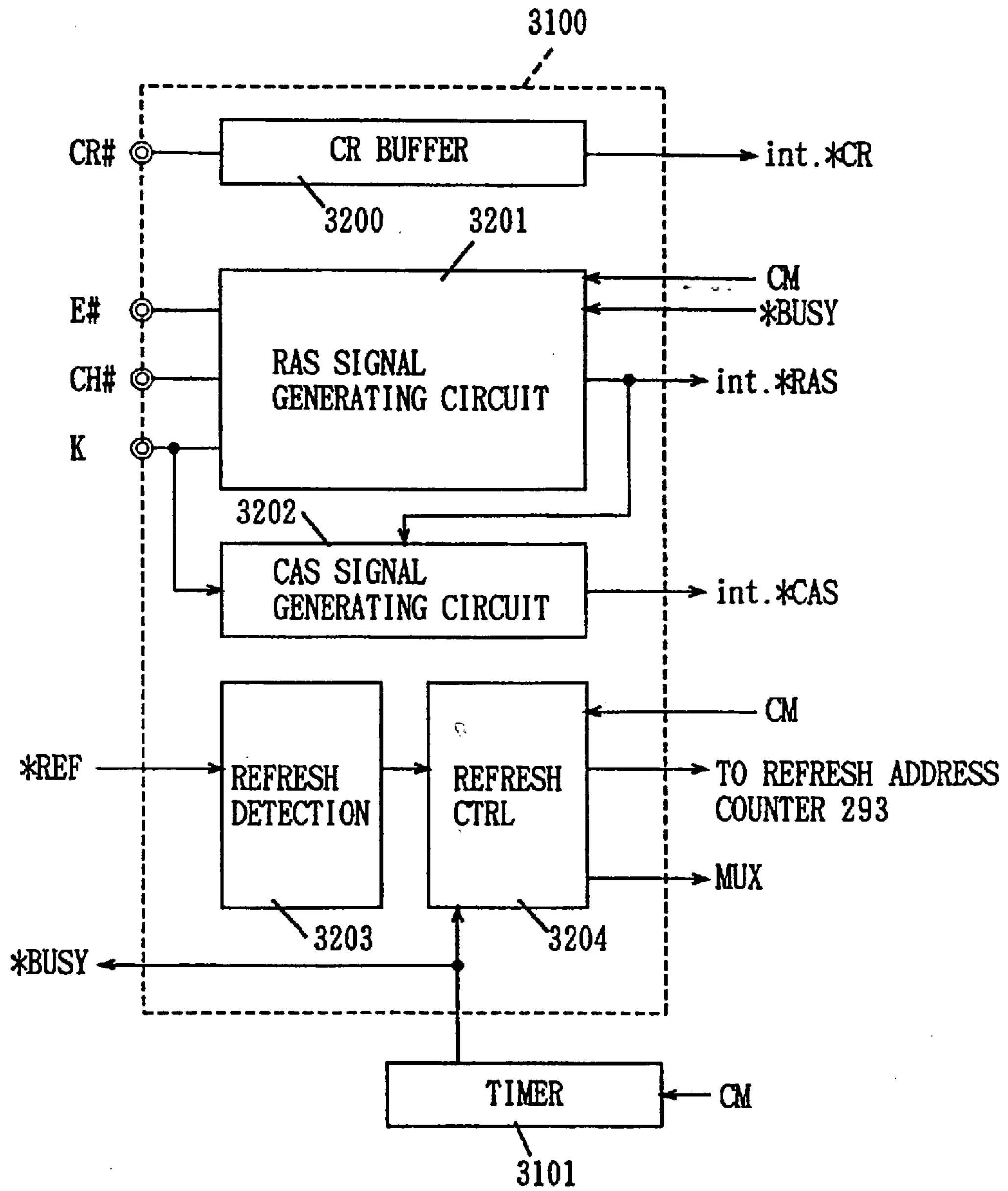
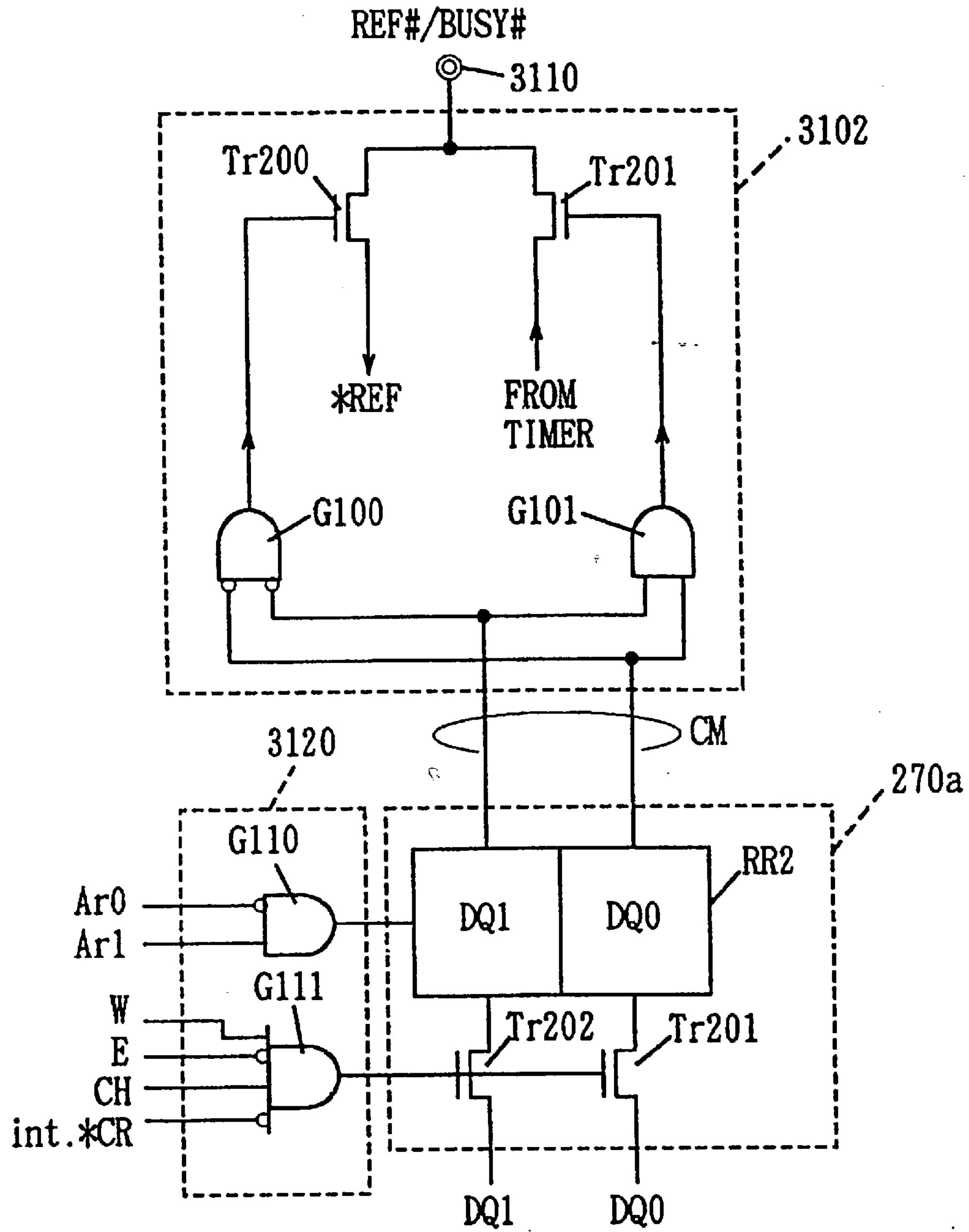
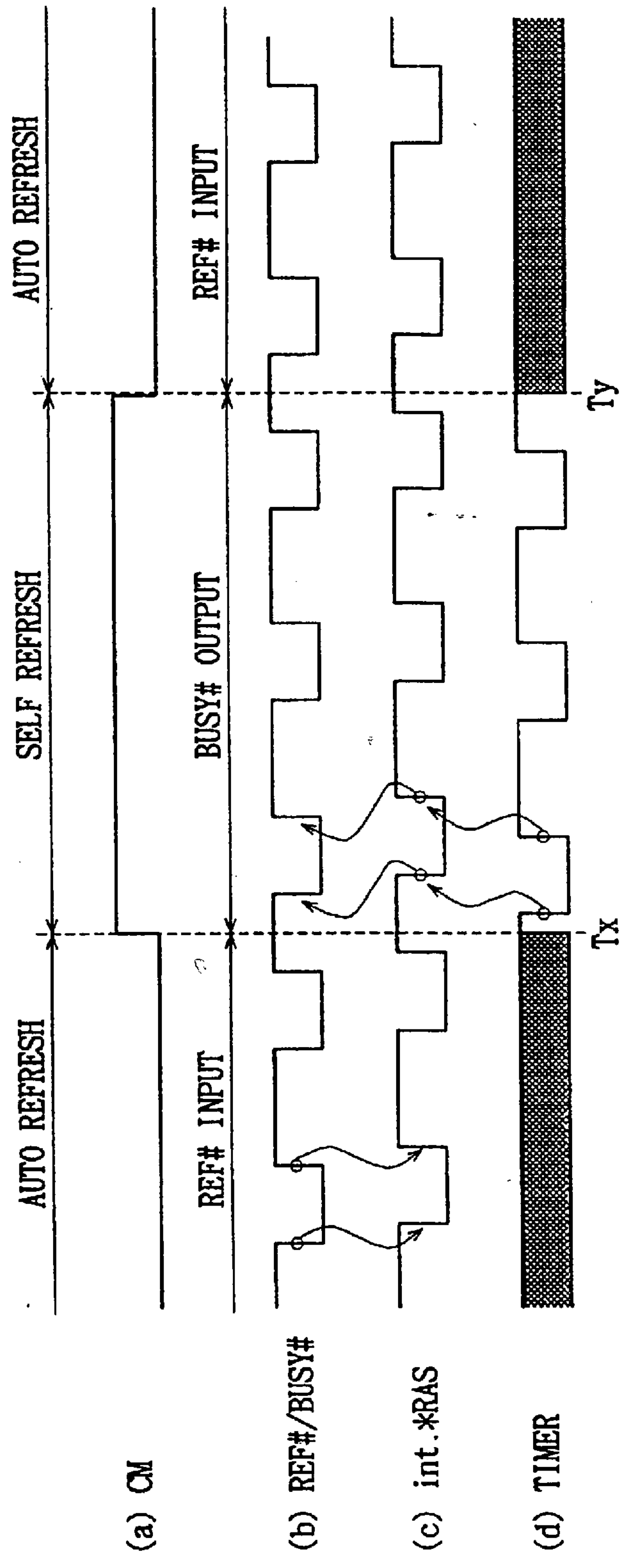
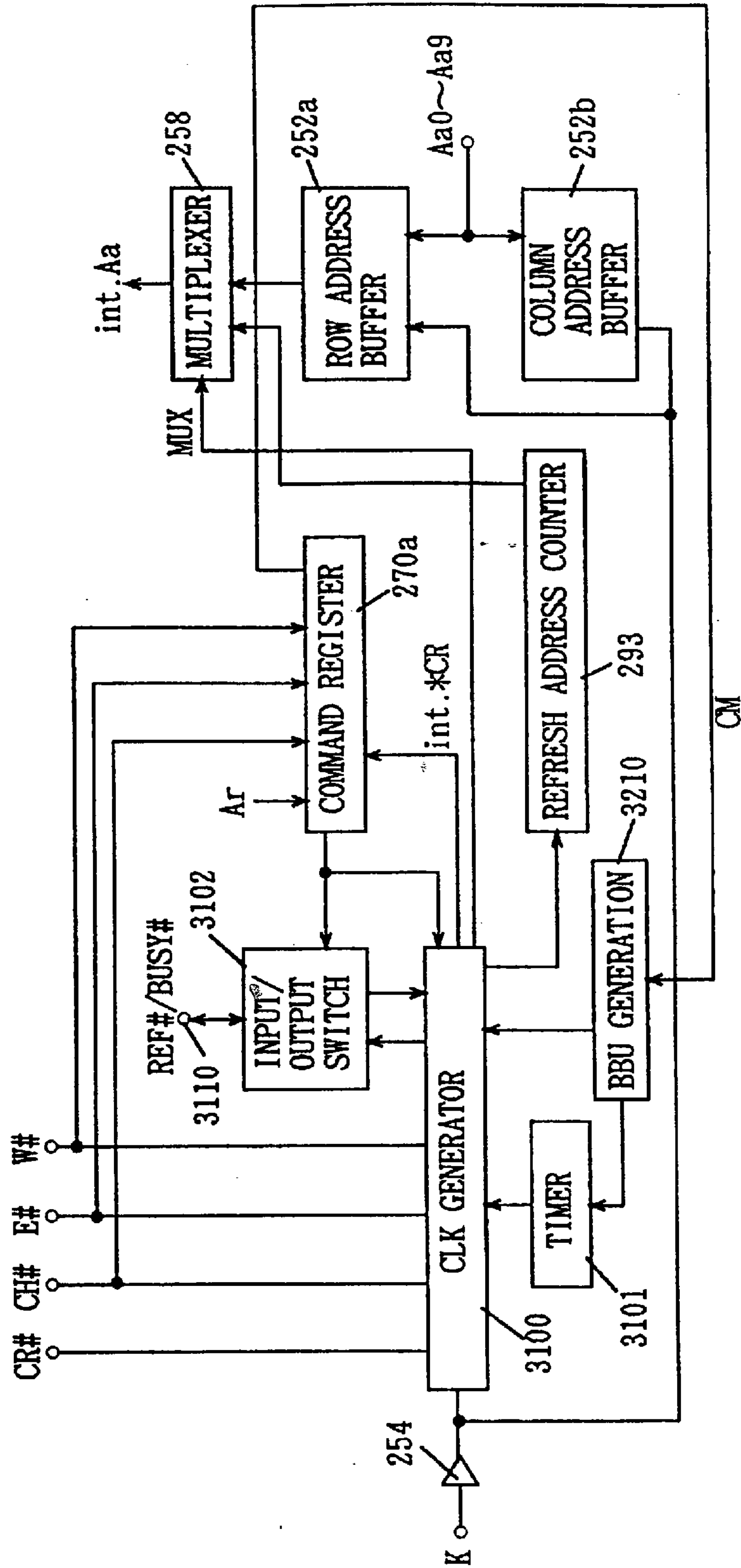


FIG. 164




F I G. 1 6 5
AUTO REFRESH
SELF REFRESH
AUTO REFRESH
REF# INPUT
BUSY# OUTPUT
REF# INPUT
(a) CM
(b) REF#/BUSY#
(c) int.*RAS
(d) TIMER
Tx
Ty

F I G. 1 6 6



F I G. 1 6 7

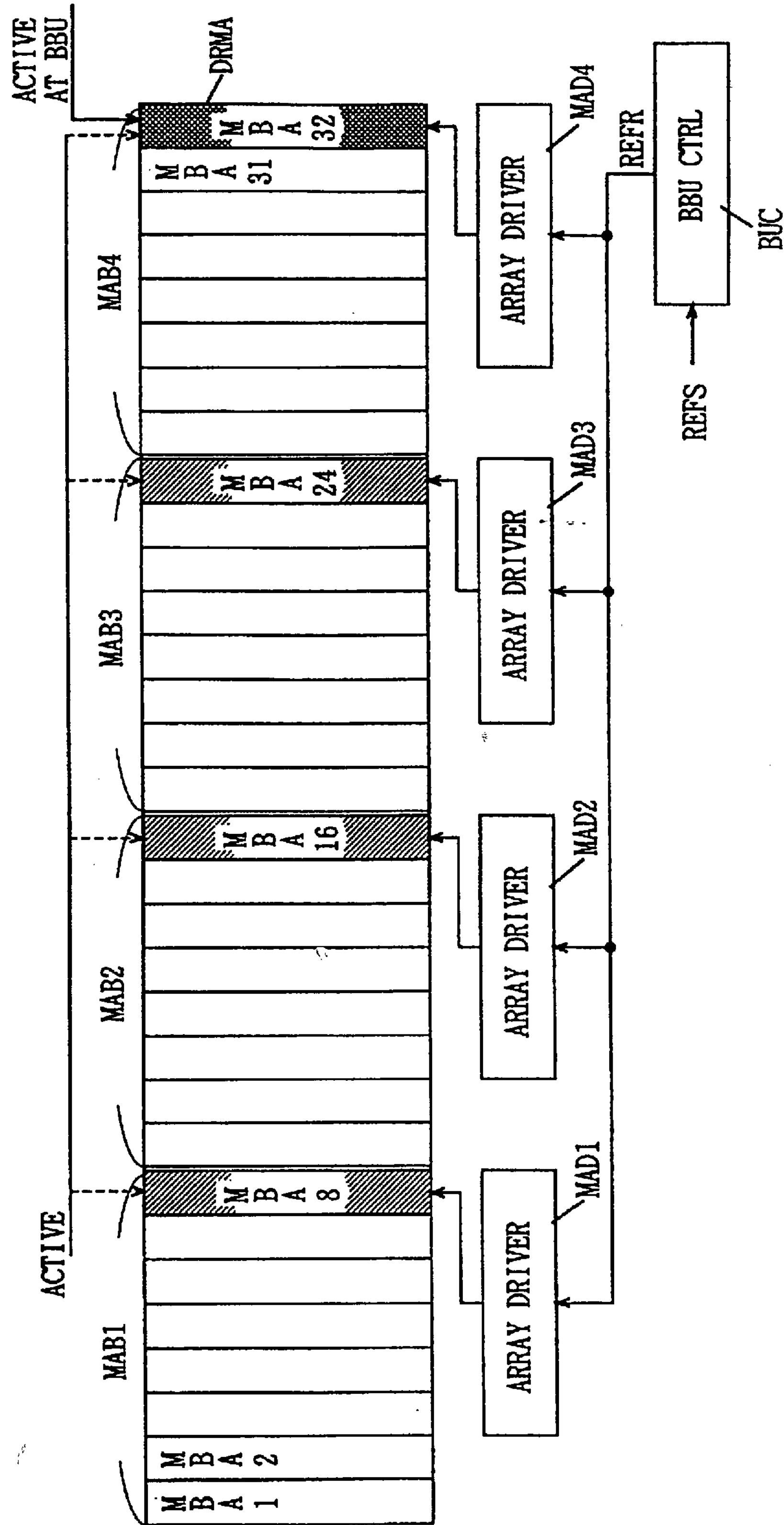


FIG. 168

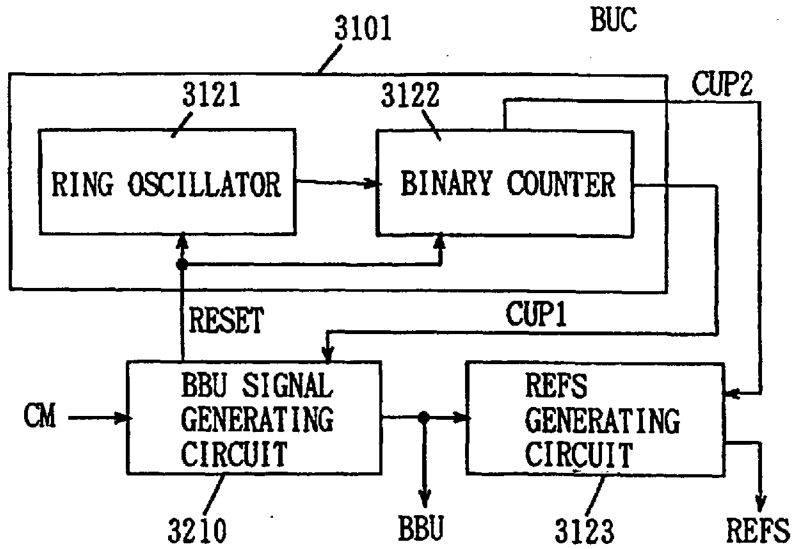


FIG. 169

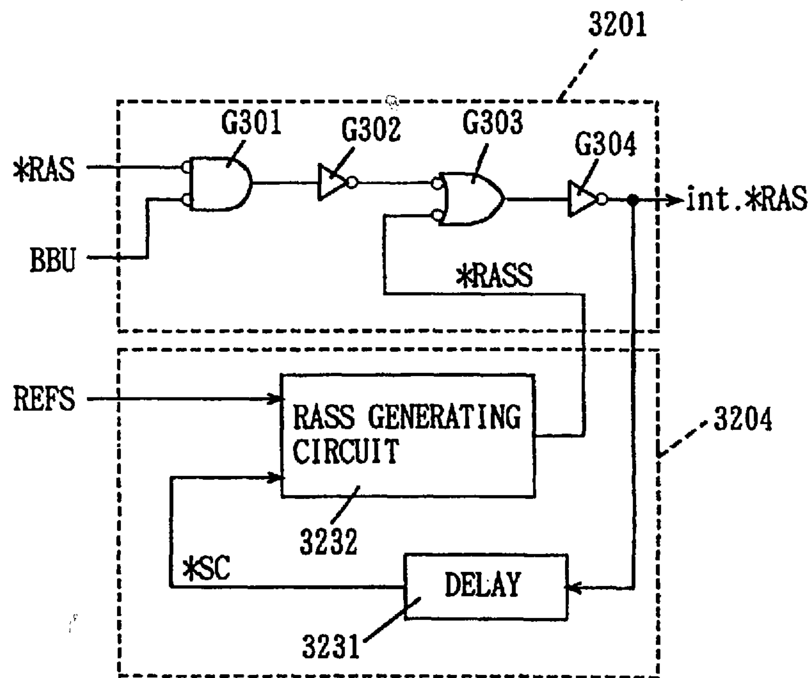


FIG. 170

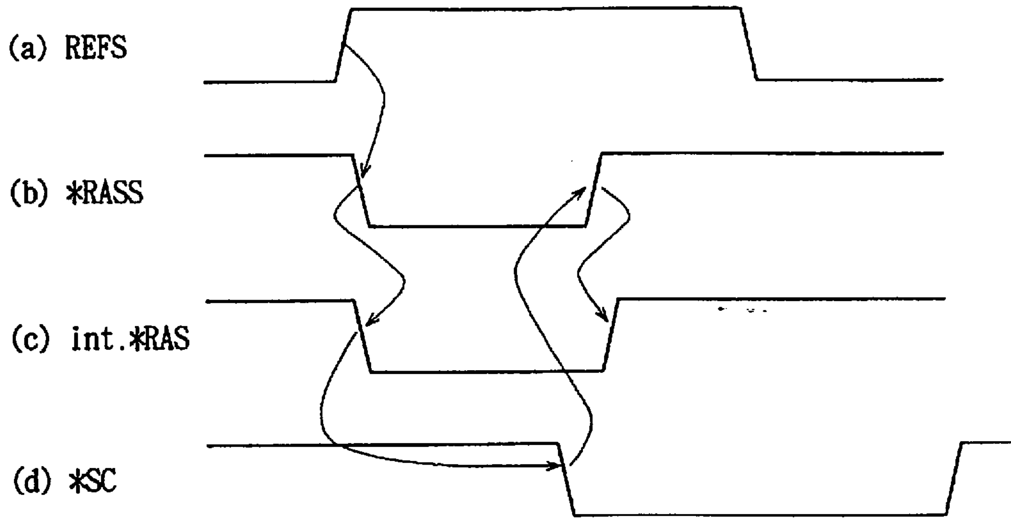
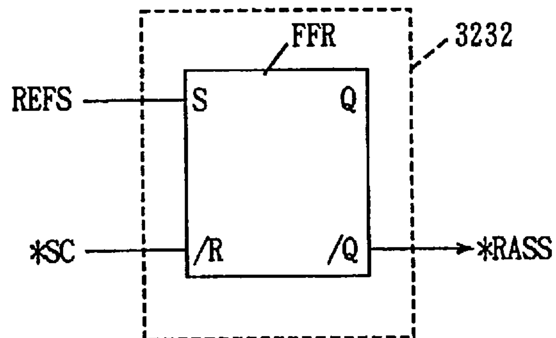


FIG. 171



F I G. 1 7 2

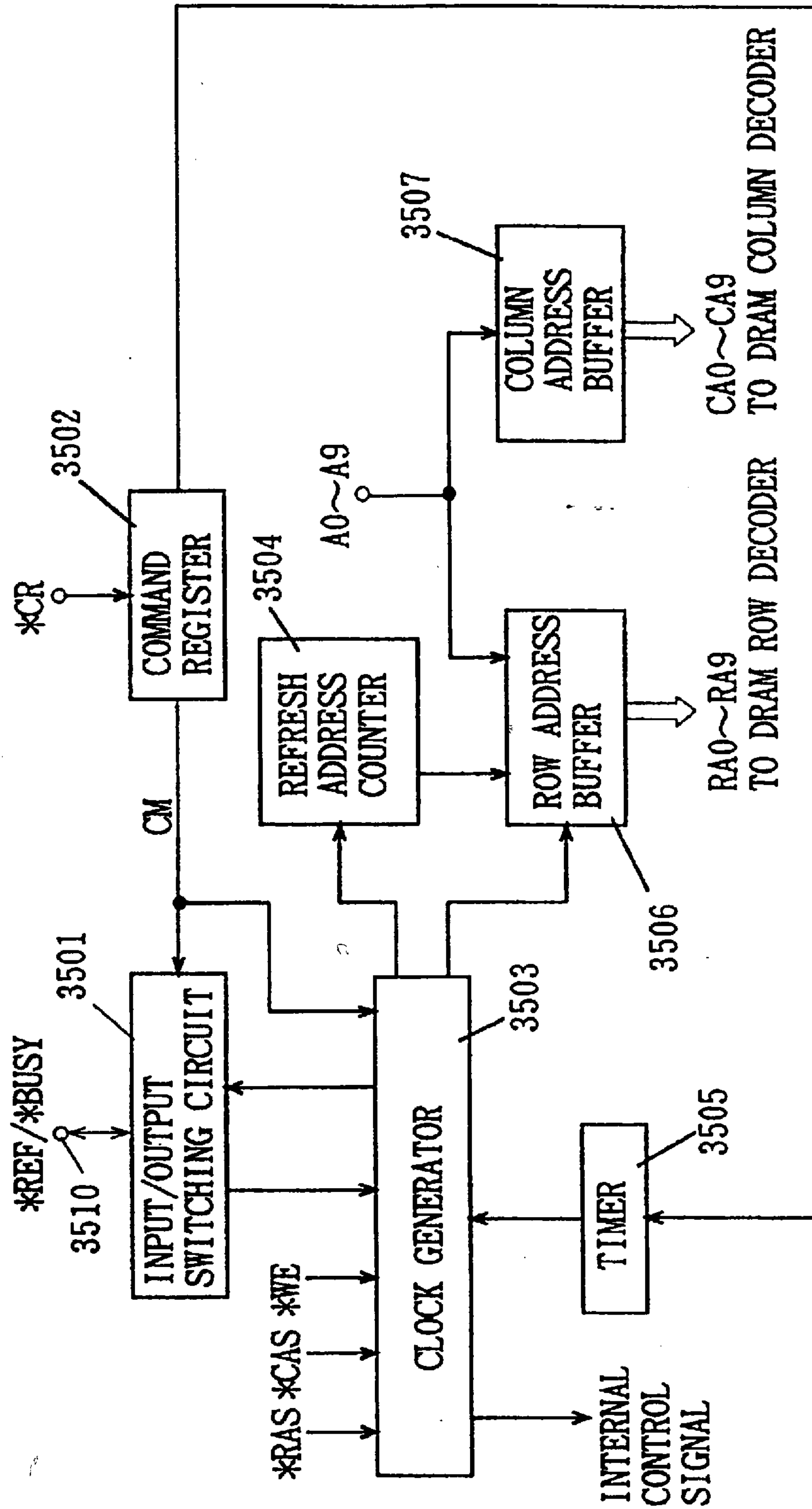


FIG. 173

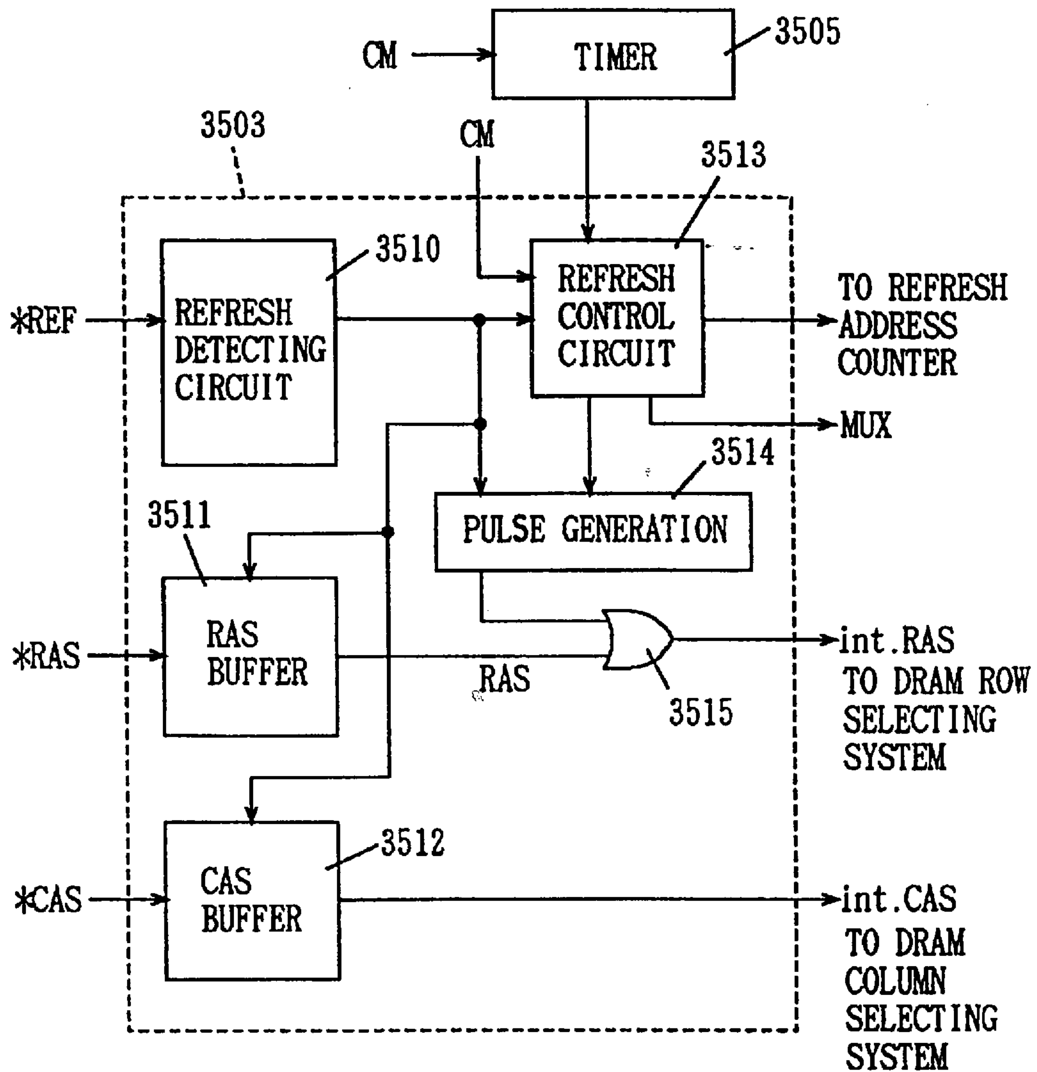


FIG. 174

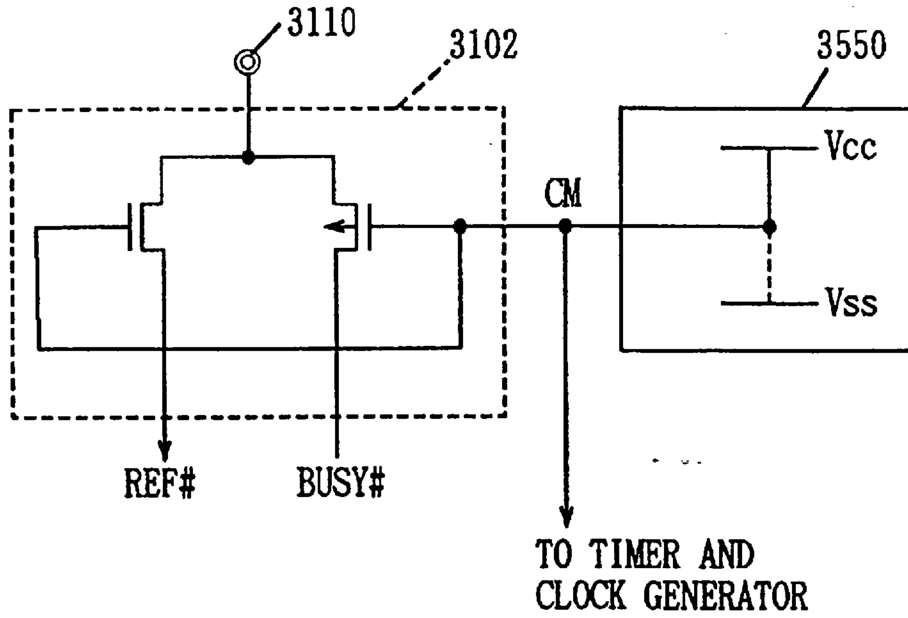


FIG. 175

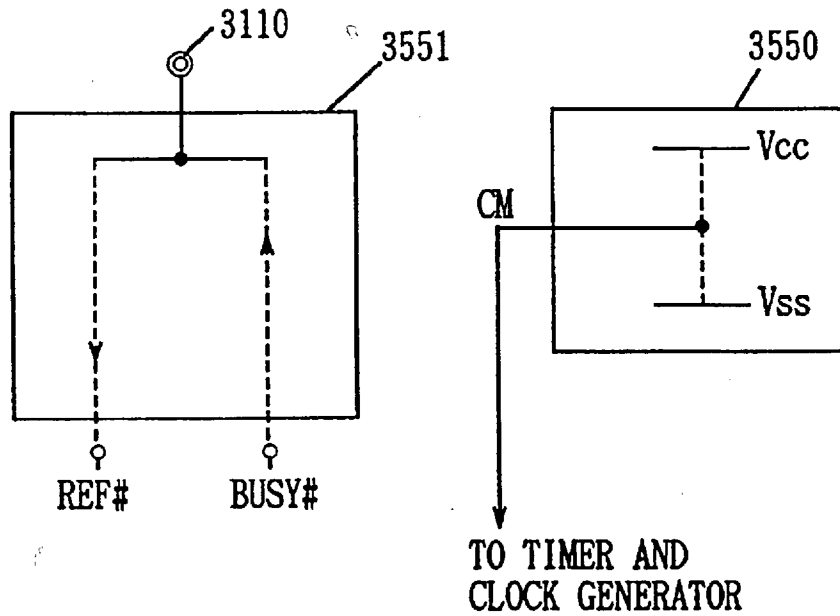


FIG. 176

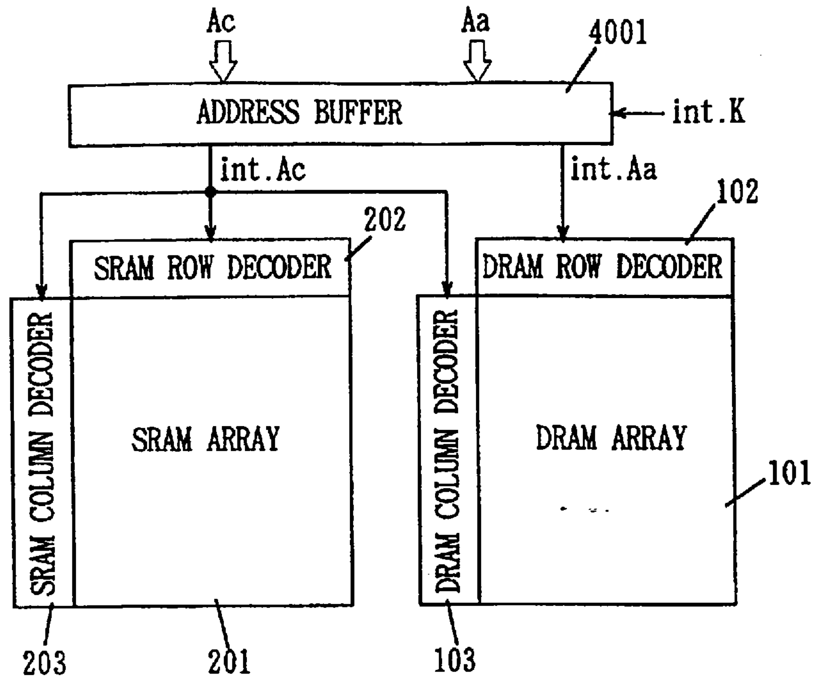


FIG. 177

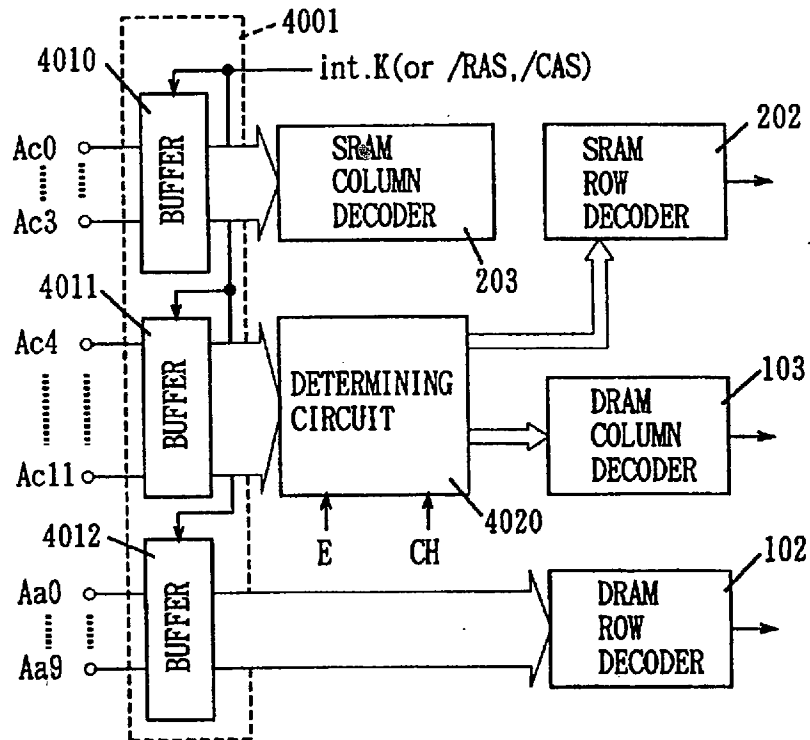


FIG. 178

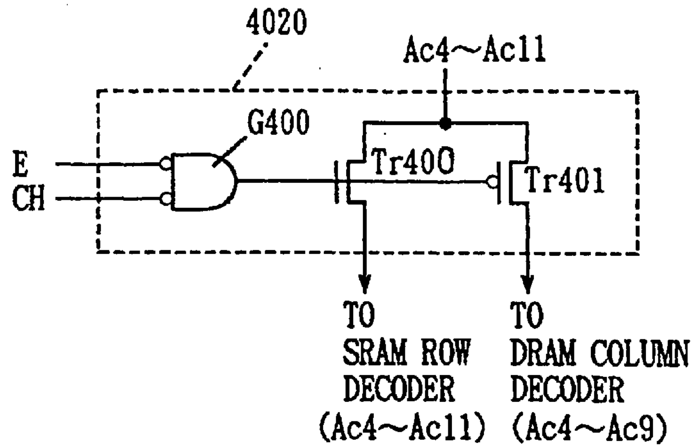


FIG. 179

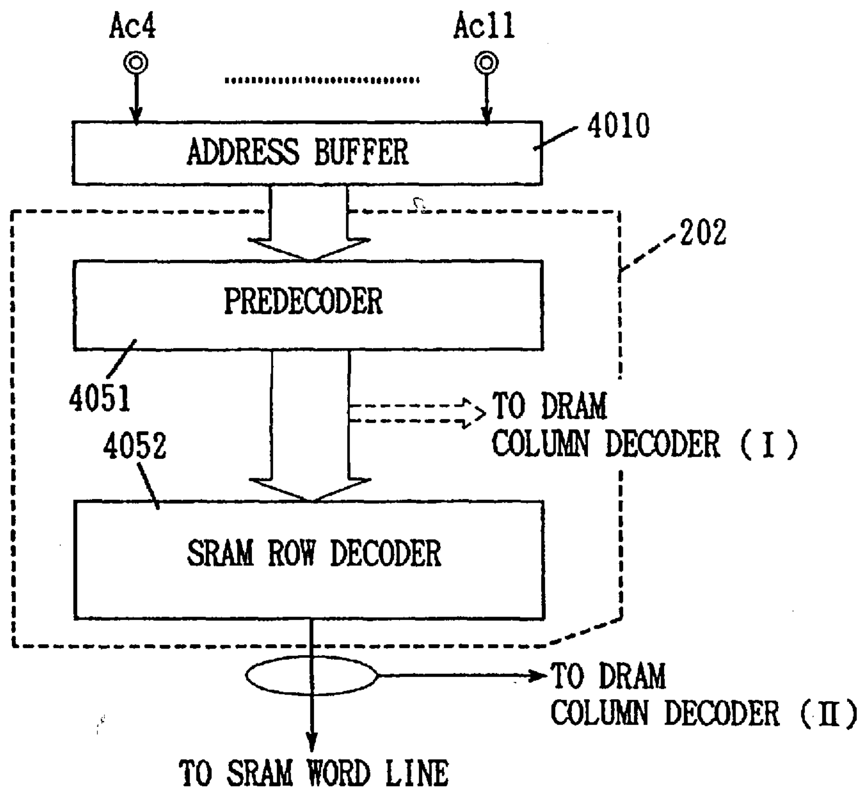
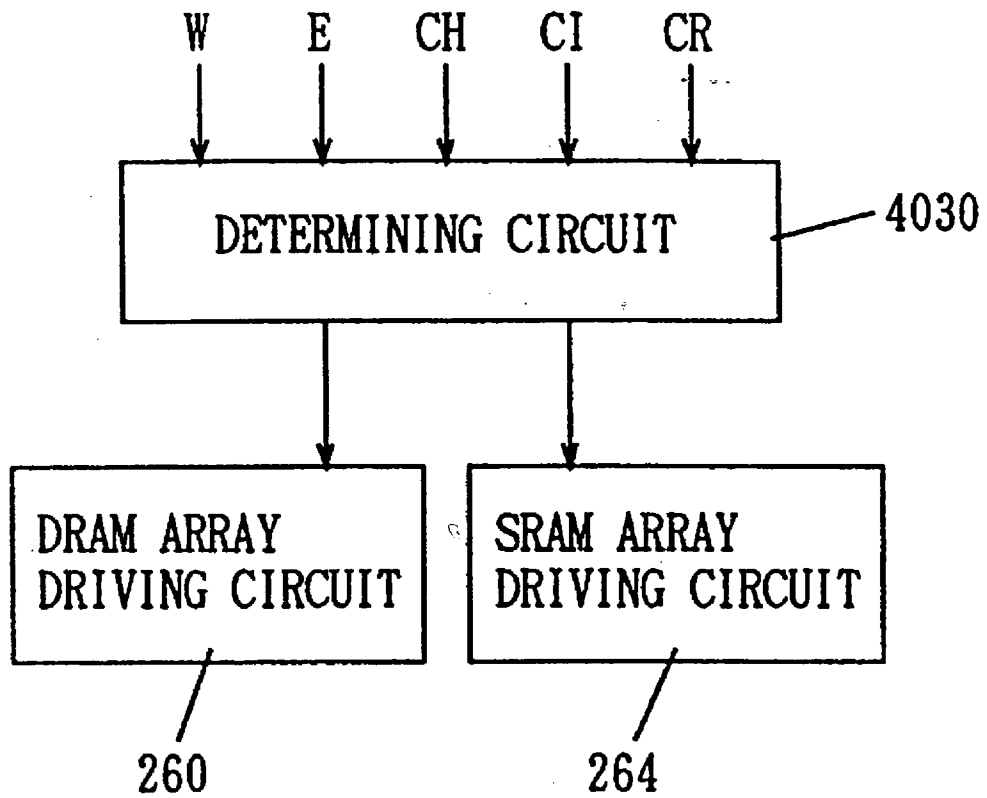


FIG. 180



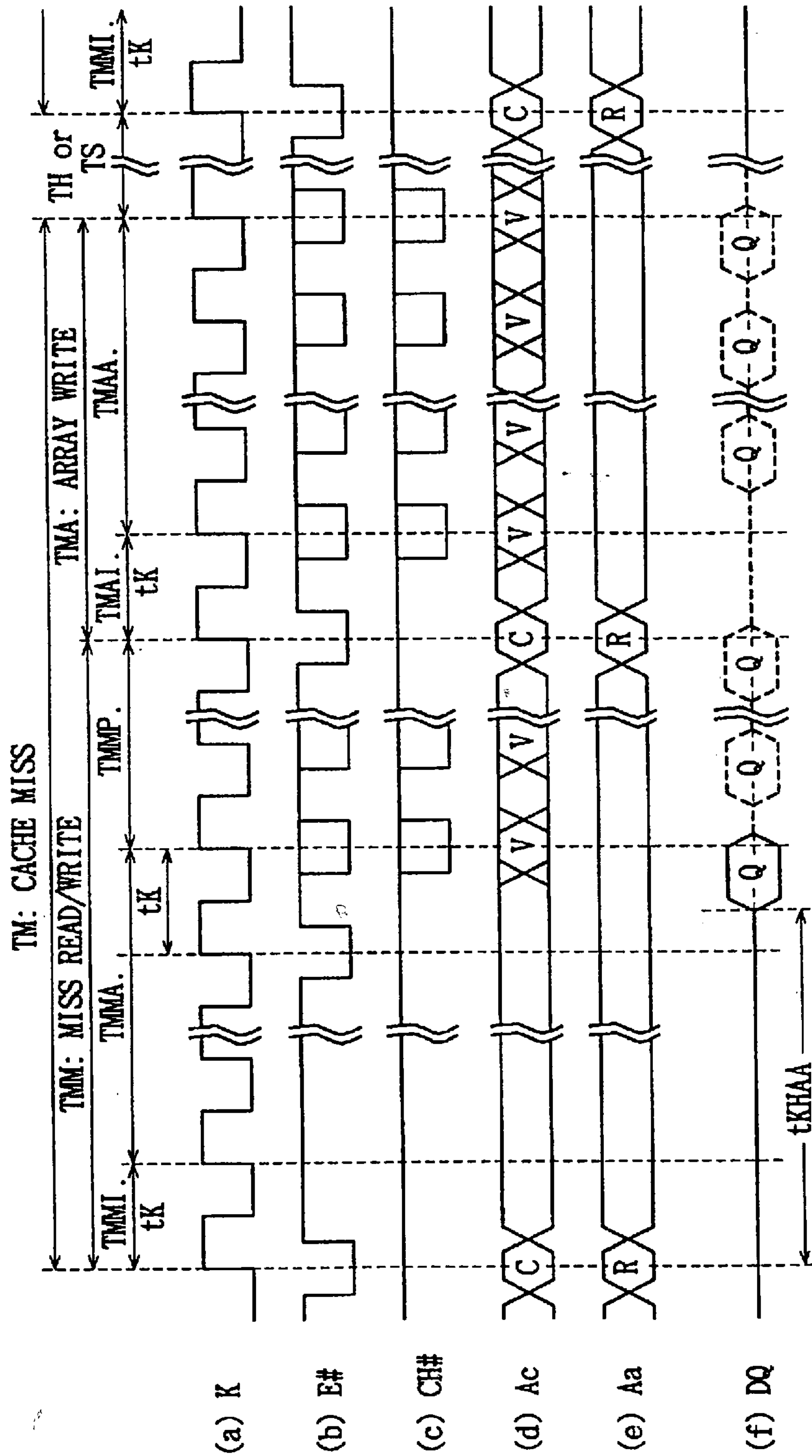


FIG. 181

FIG. 182

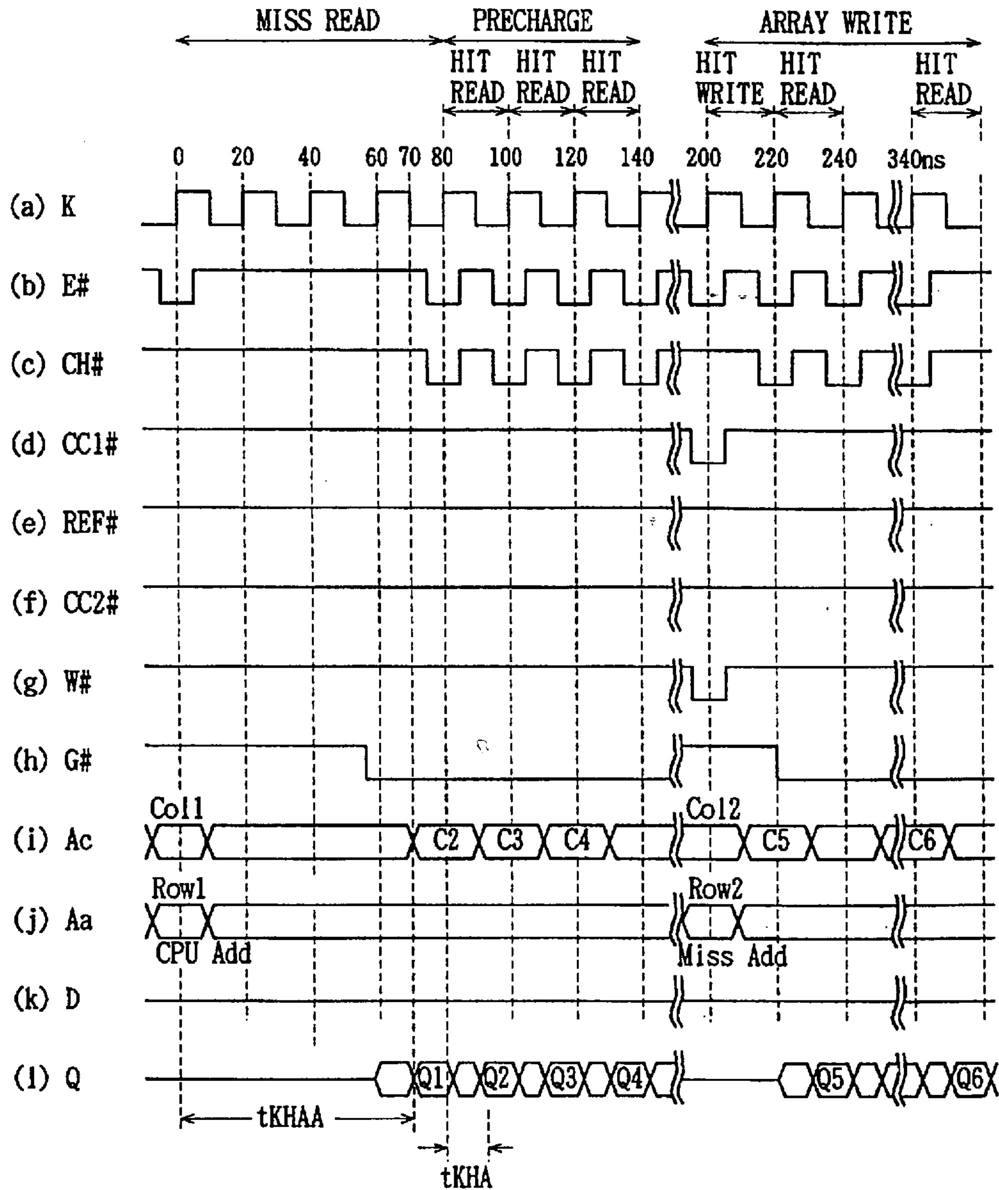
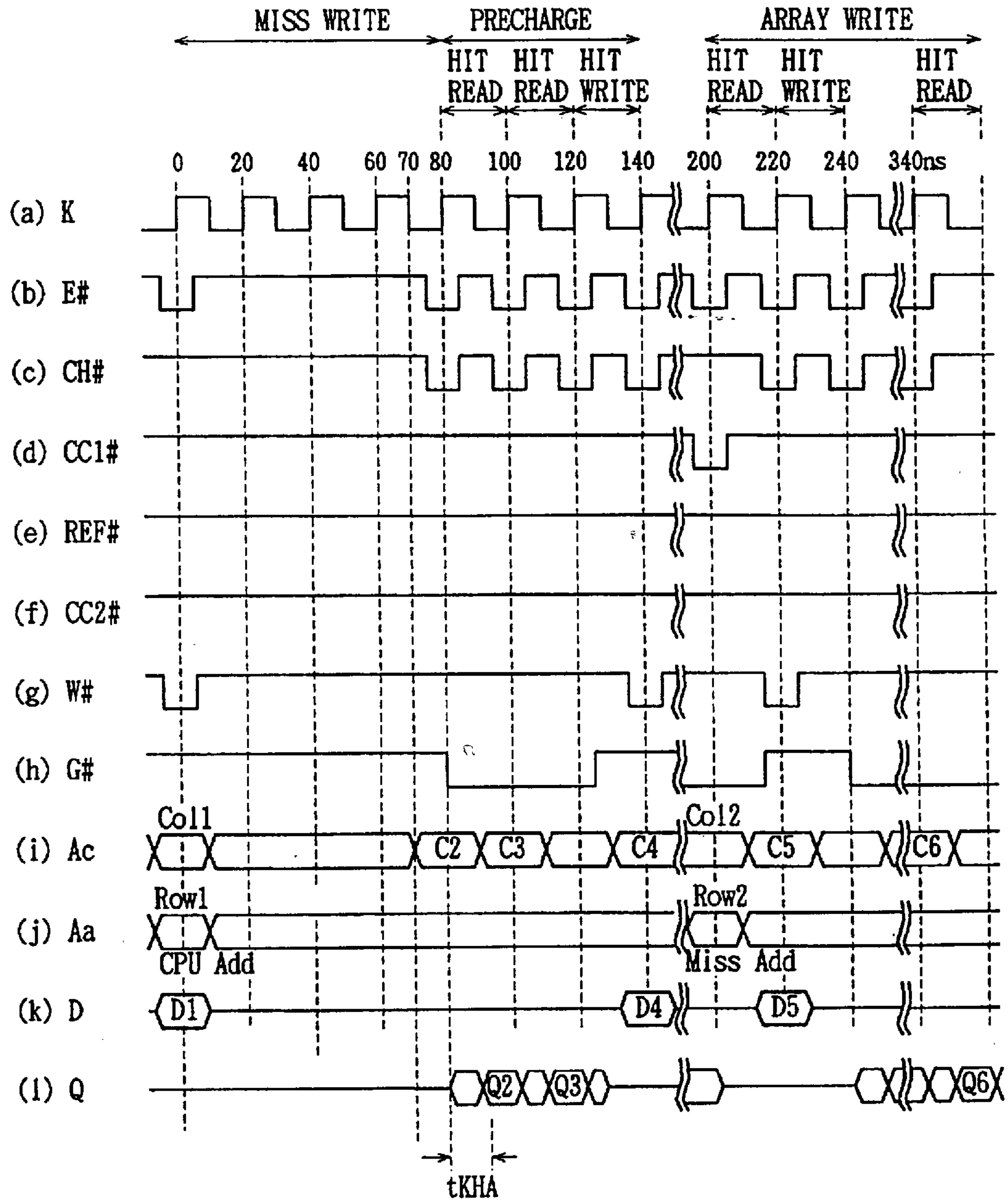
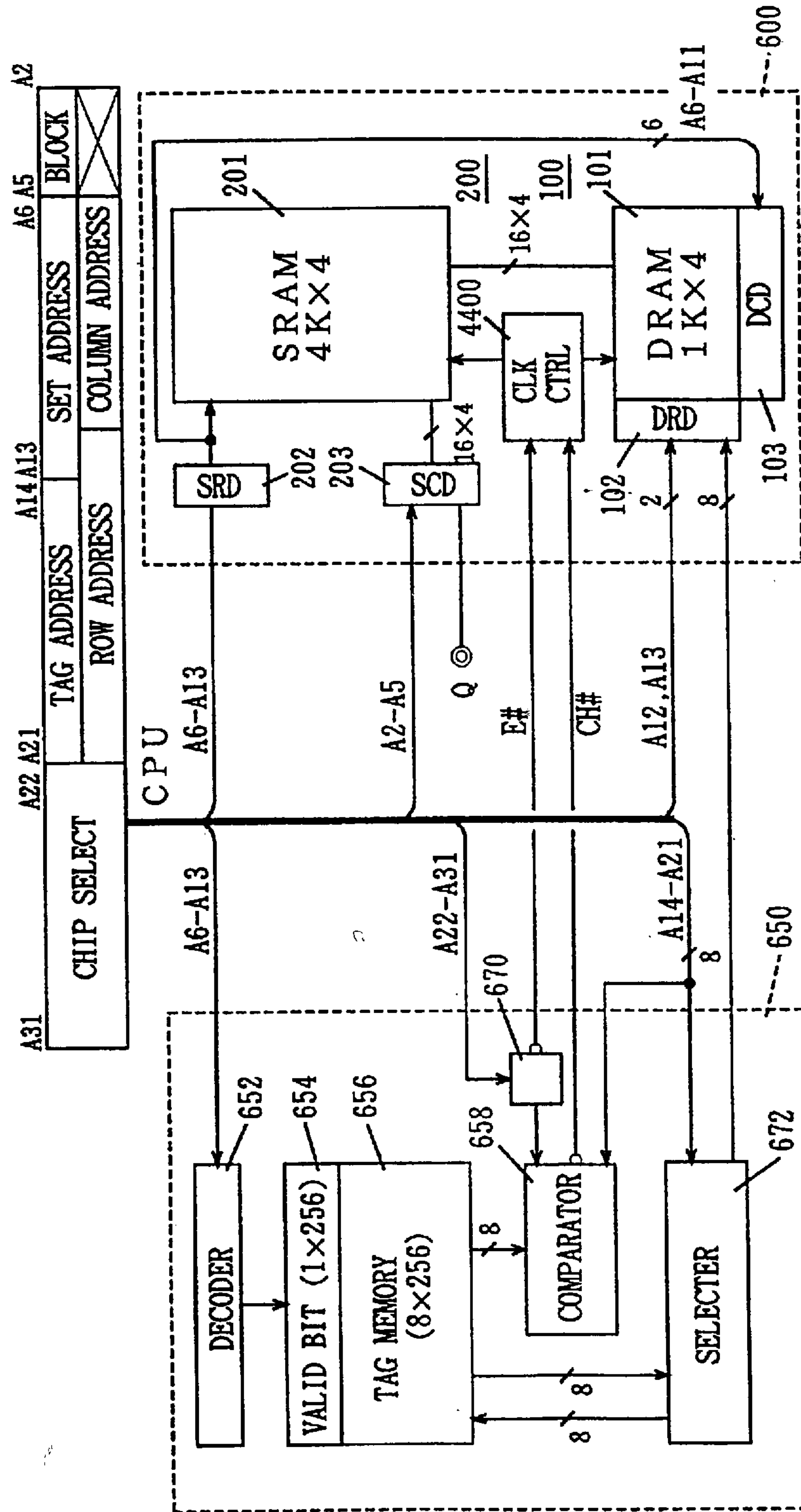


FIG. 183




F I G. 1 8 4
A31
A22 A21
A14 A13
A6 A5
A2
CHIP SELECT
TAG ADDRESS
ROW ADDRESS
SET ADDRESS
COLUMN ADDRESS
BLOCK
CPU
A6-A13
A2-A5
Q
E#
CH#
A12, A13
600
A6-A11
6
201
200
100
101
SRAM
4K×4
16×4
4400
CLK
CTRL
DRAM
1K×4
DCD
DRD
16×4
SRD
202
203
SCD
102
2
8
103
A6-A13
A22-A31
A14-A21
8
650
670
652
654
656
658
672
DECODER
VALID BIT (1×256)
TAG MEMORY
(8×256)
8
COMPARATOR
8
8
SELECTER

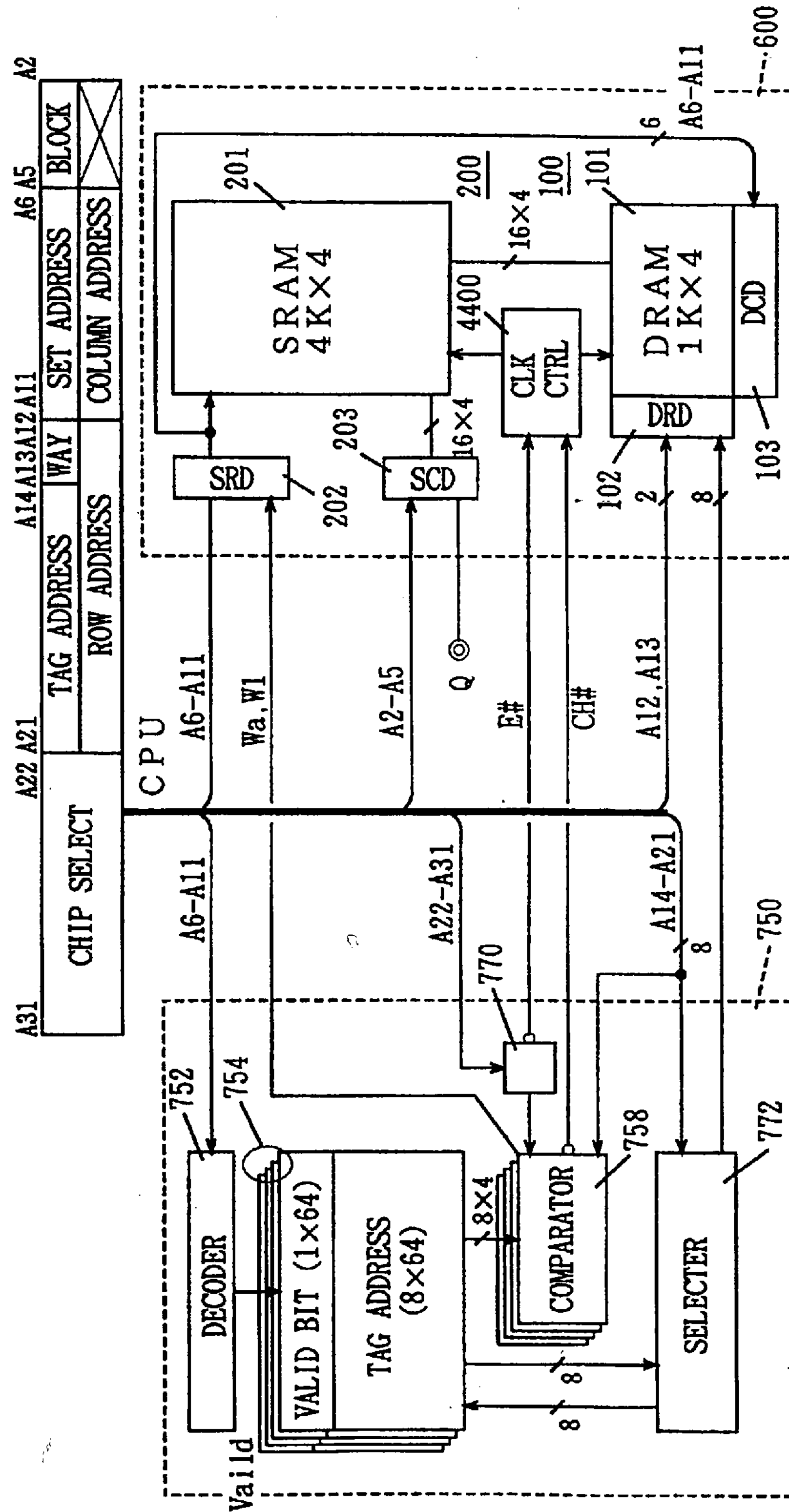
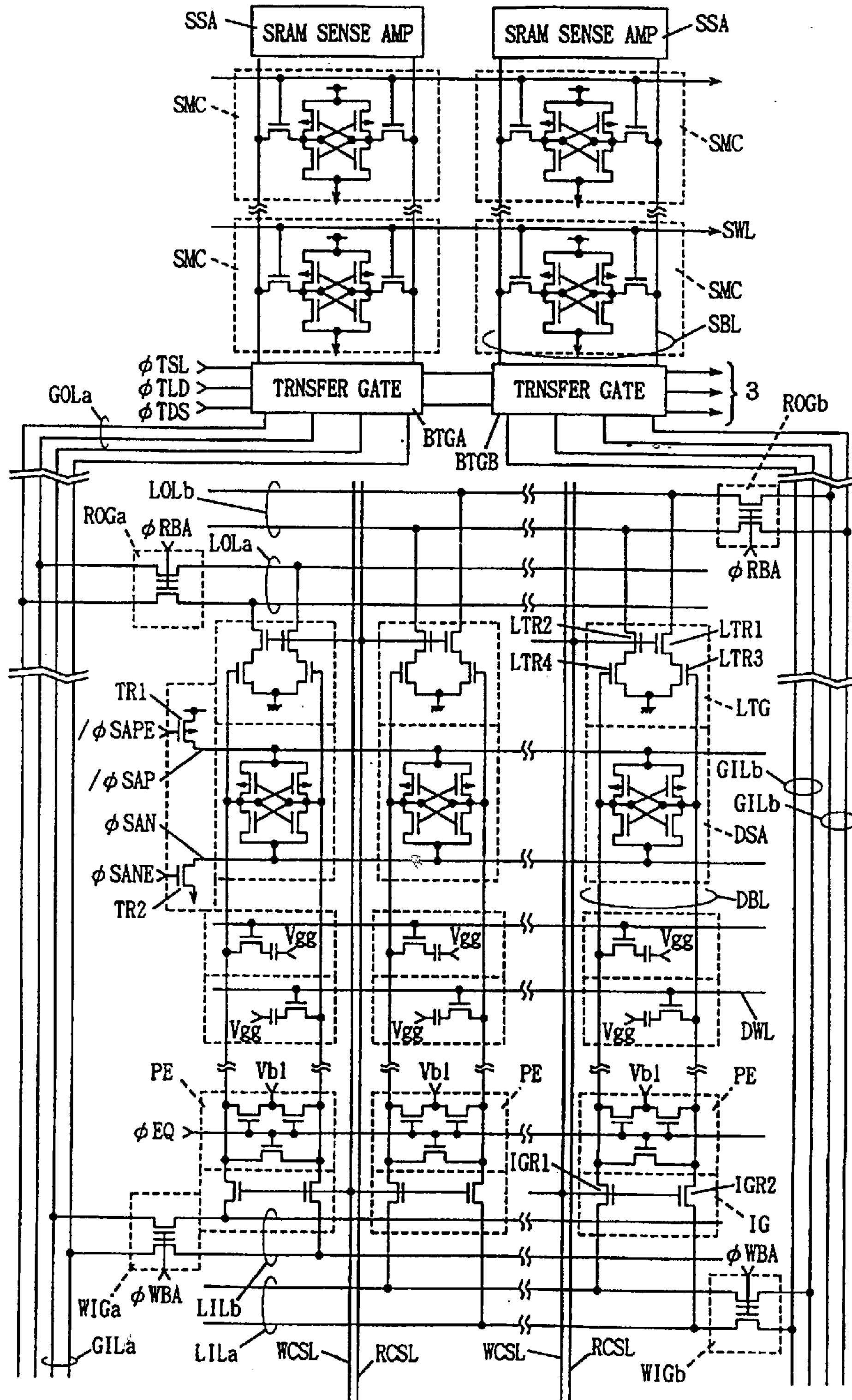

F I G. 1 8 5
A31
A22 A21
A14 A13 A12 A11
A6 A5
A2
CHIP SELECT
TAG ADDRESS
ROW ADDRESS
WAY
SET ADDRESS
COLUMN ADDRESS
BLOCK
CPU
A6-A11
Wa, W1
A2-A5
Q
E#
CH#
A12, A13
A22-A31
A14-A21
600
200
100
101
201
SRAM
4K×4
DRAM
1K×4
DCD
DRD
CLK
CTRL
4400
16×4
SRD
SCD
202
203
102
103
6
2
8
750
770
752
754
758
772
DECODER
VALID BIT (1×64)
TAG ADDRESS
(8×64)
8×4
COMPARATOR
SELECTER
Vaild

FIG. 186



F I G. 1 8 7

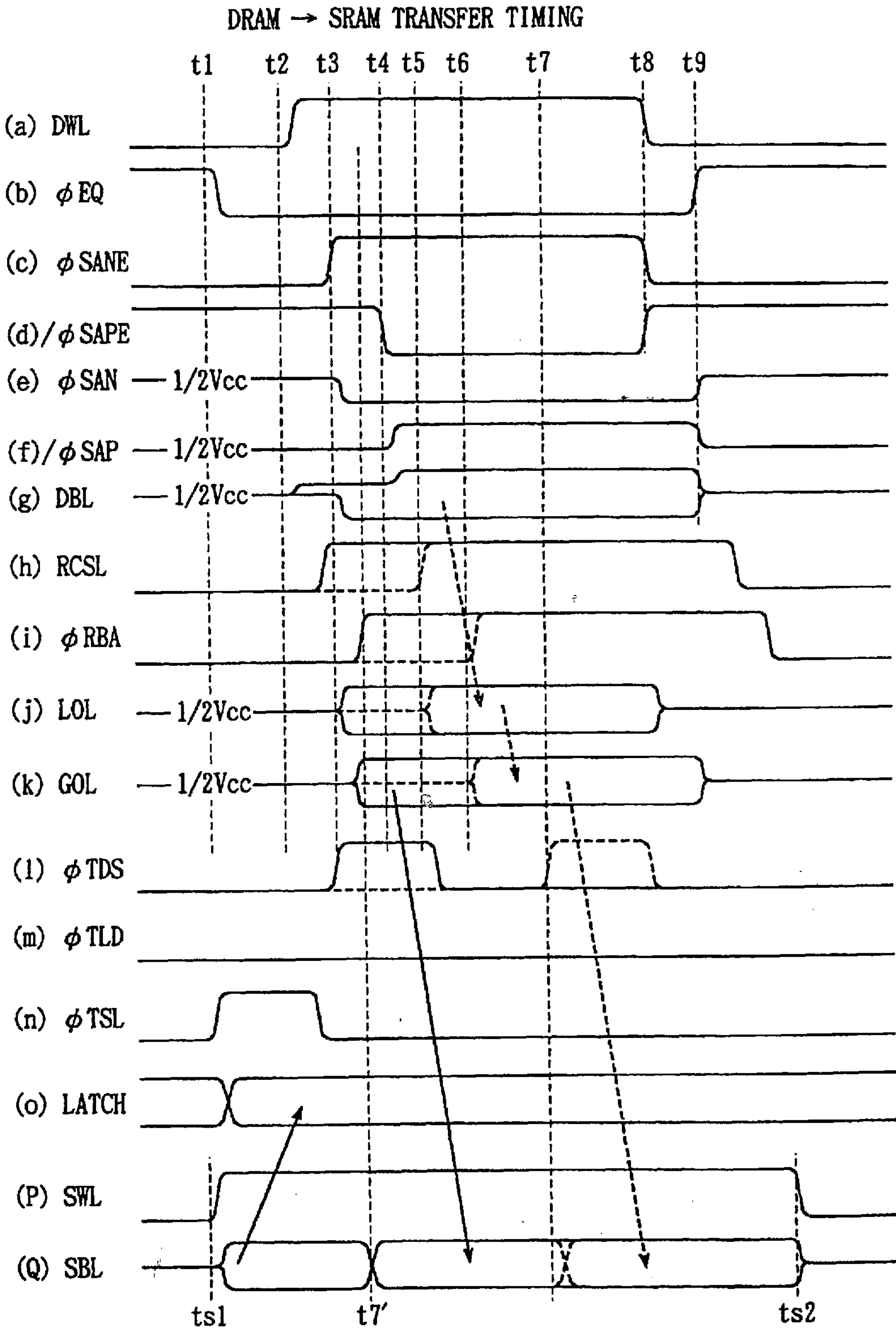
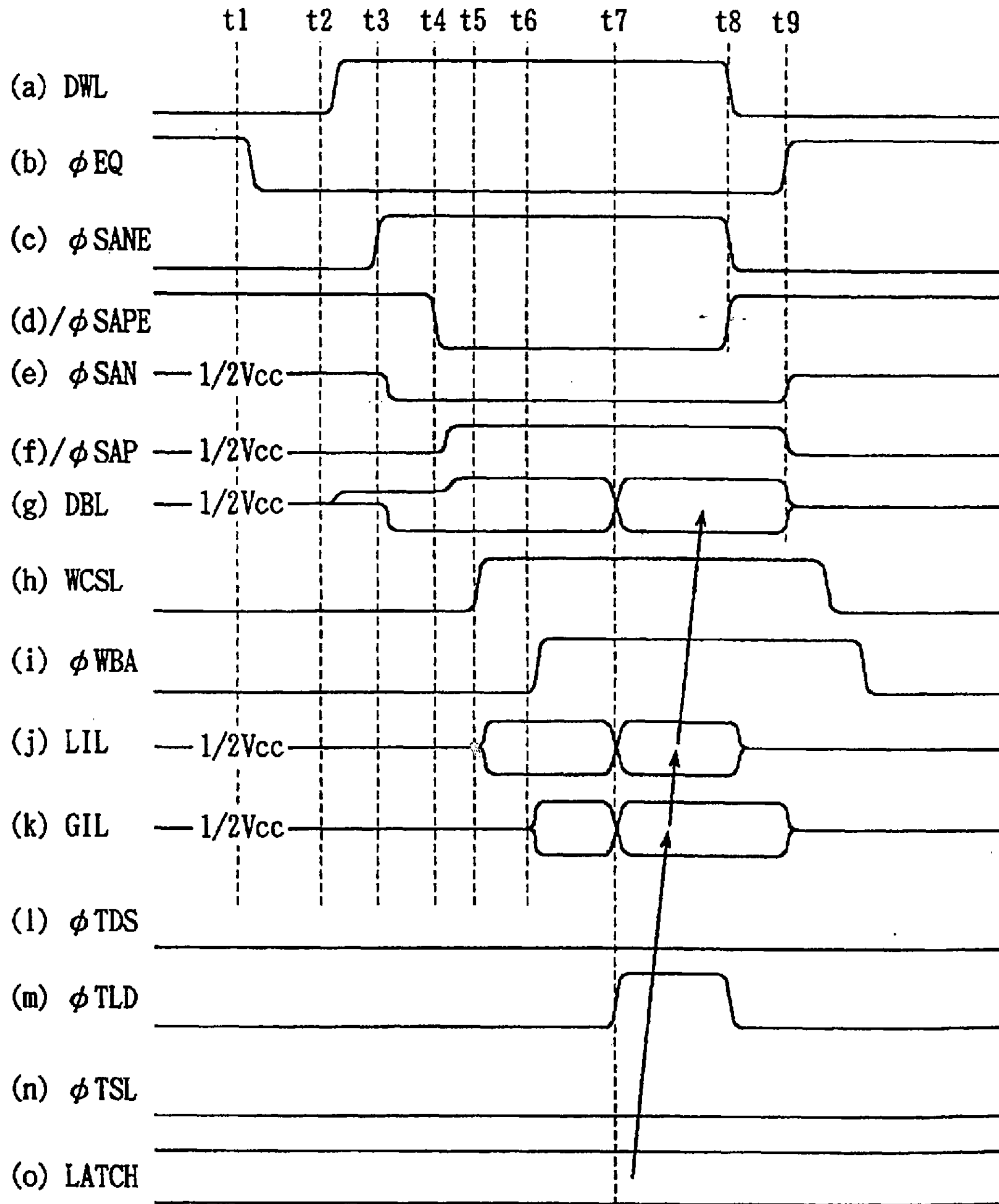


FIG. 188



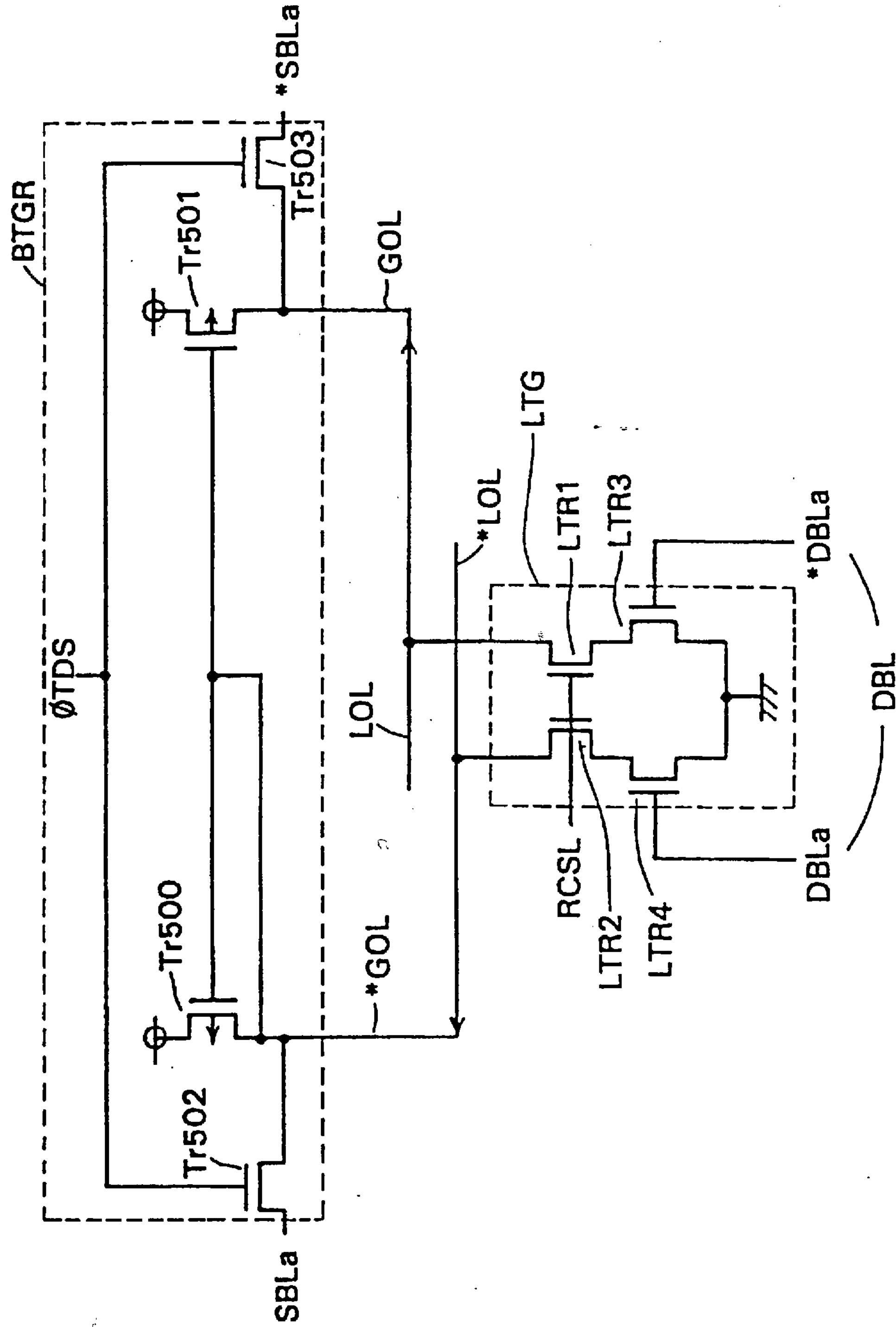


FIG.189

FIG. 190

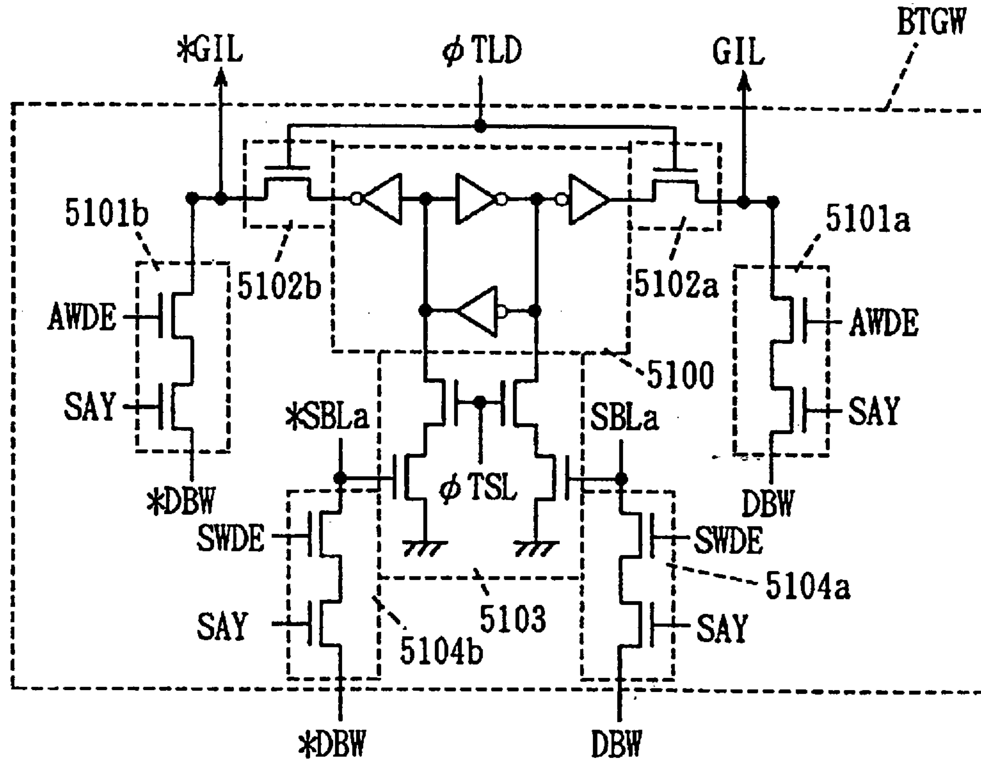


FIG. 191

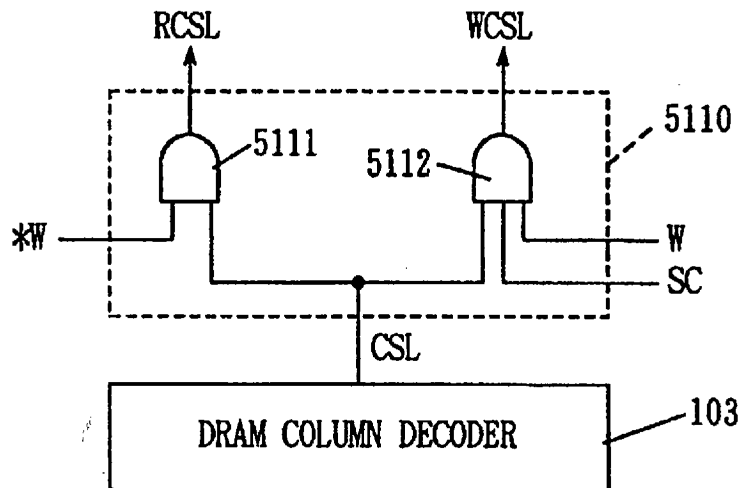


FIG. 192

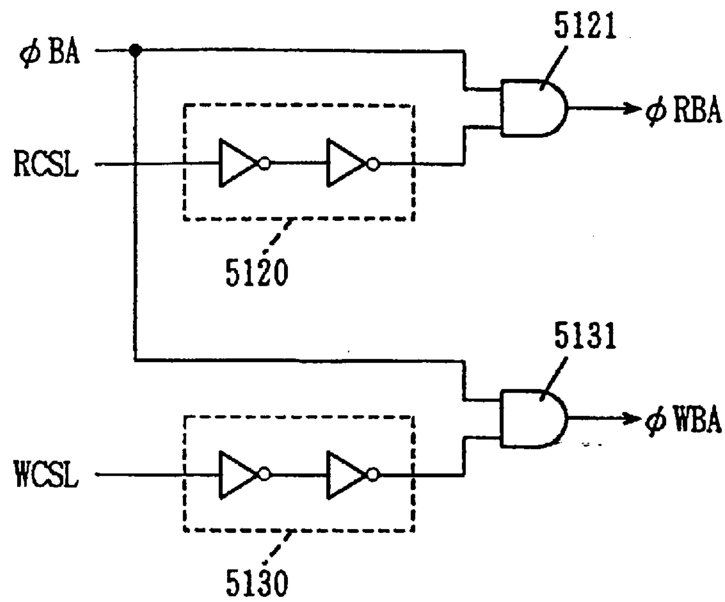


FIG. 193

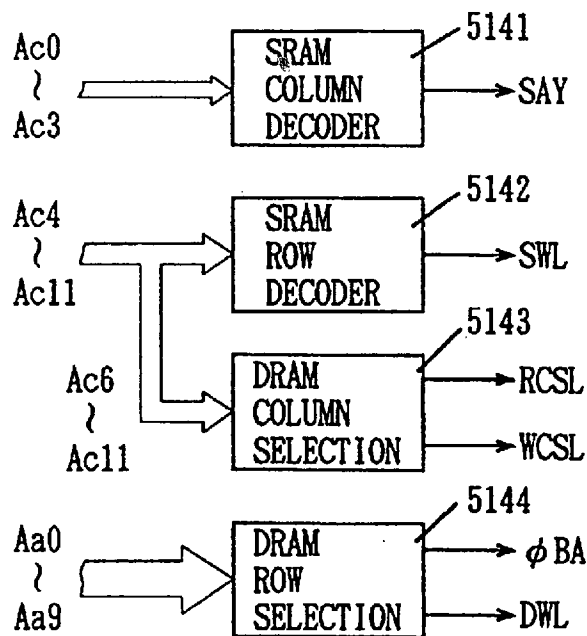


FIG. 194

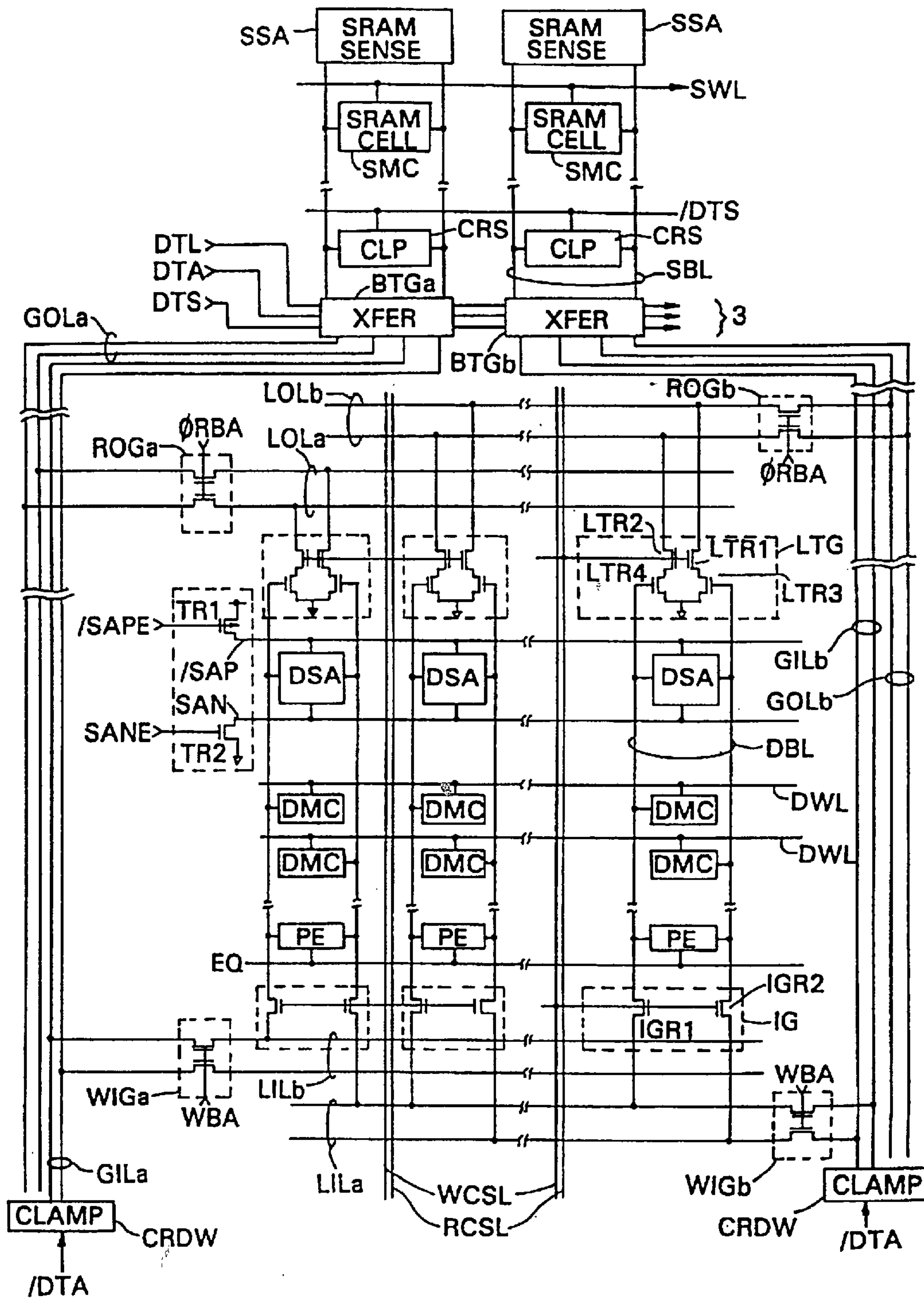


FIG. 195

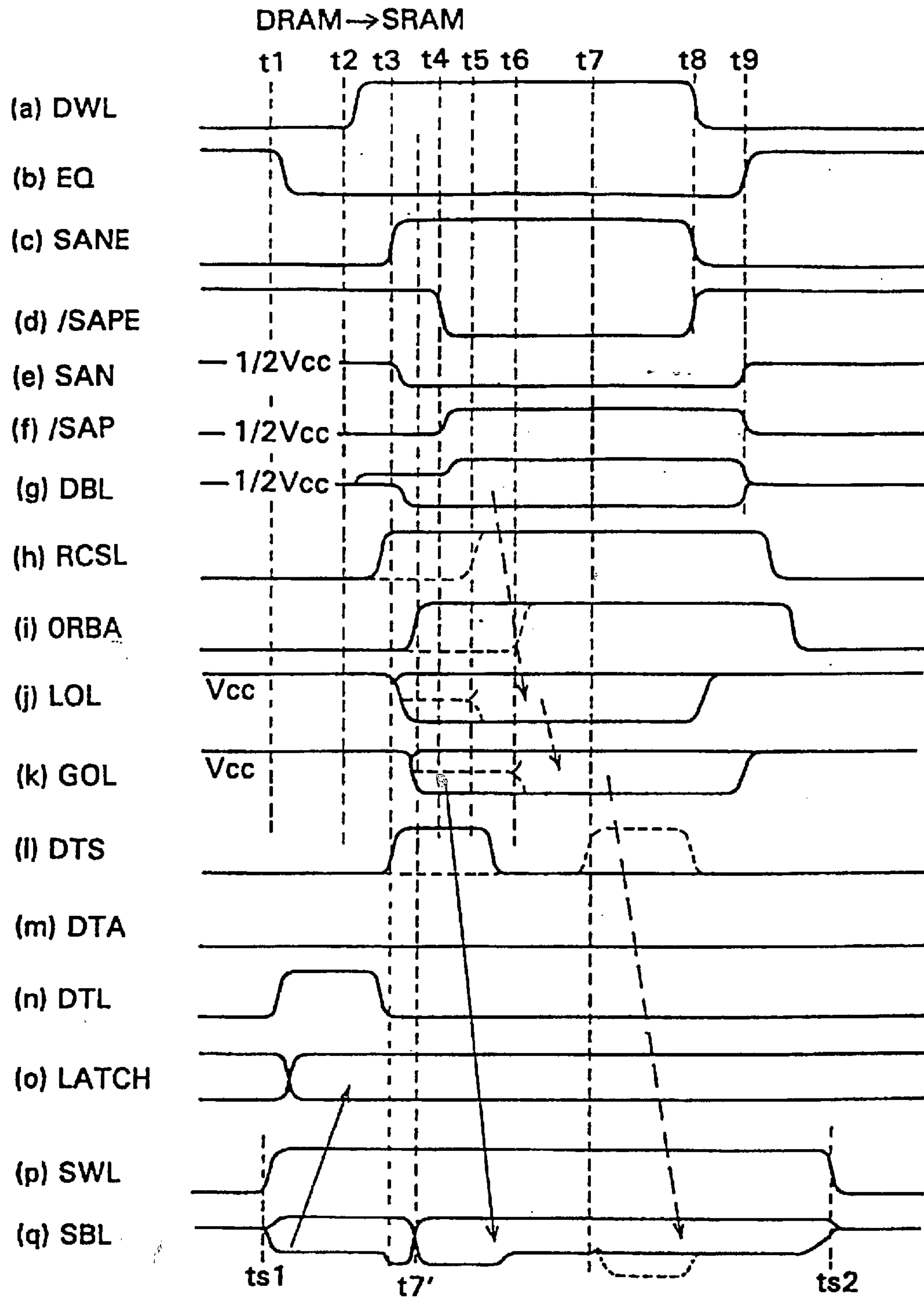


FIG.196

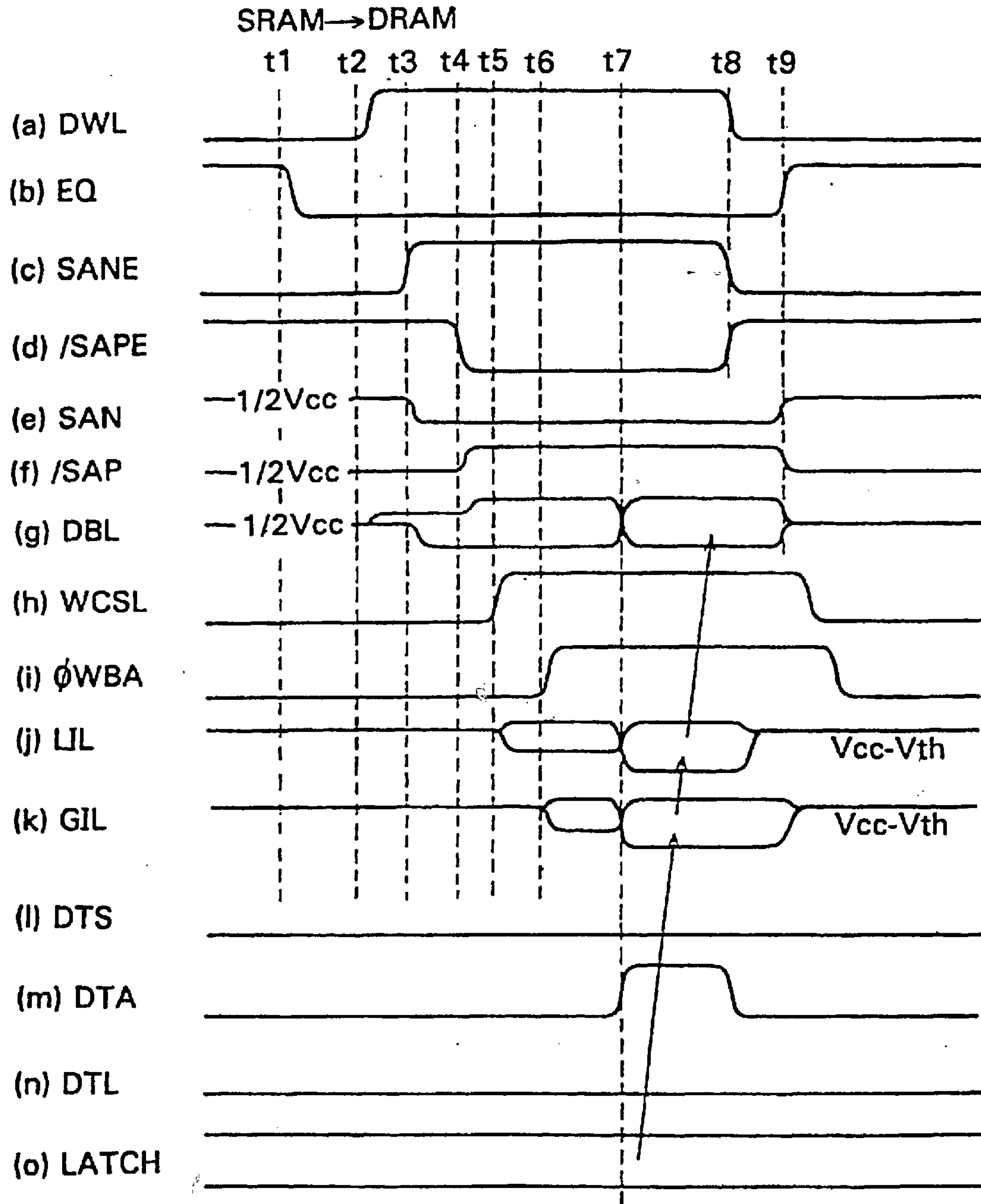
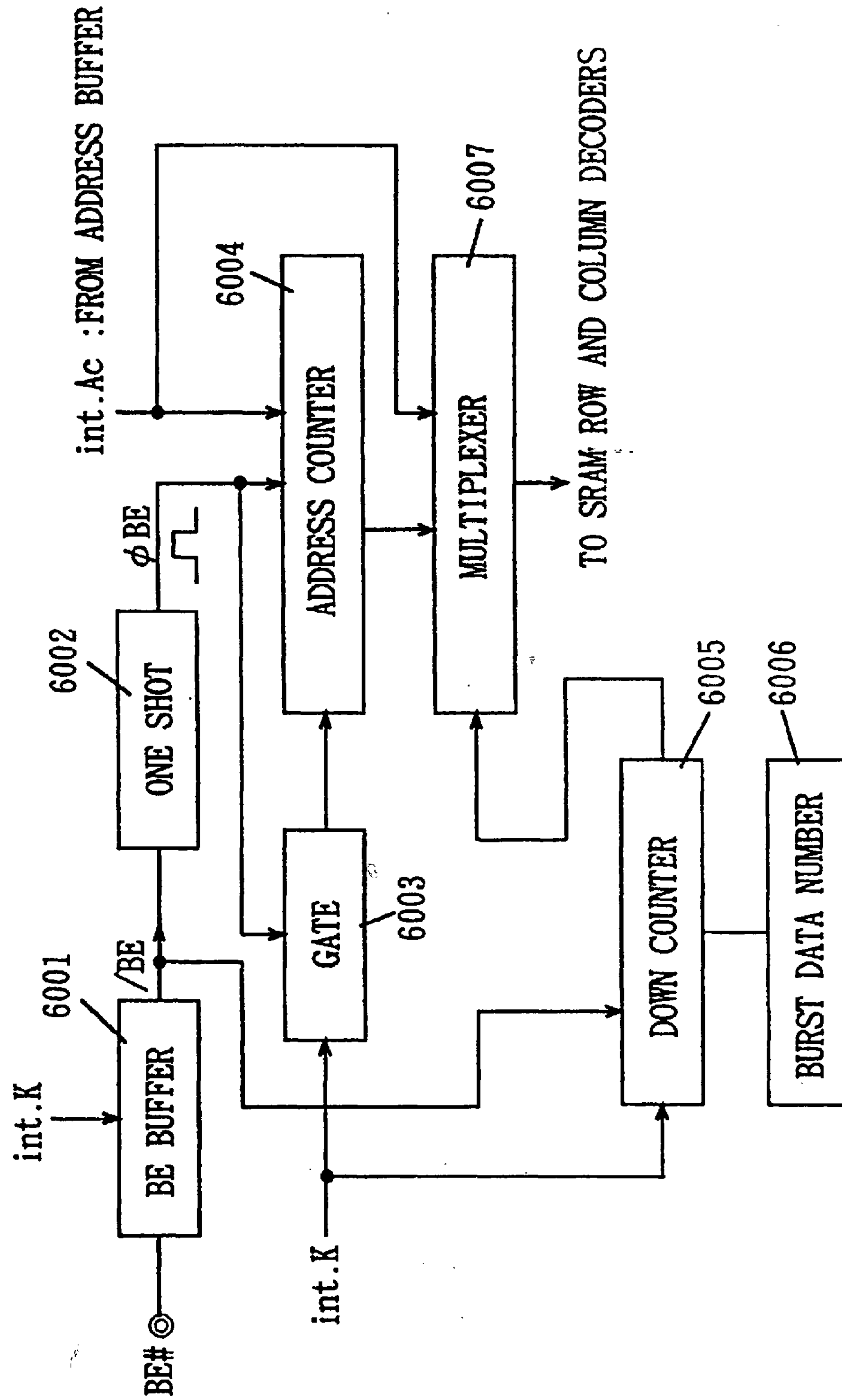


FIG. 197



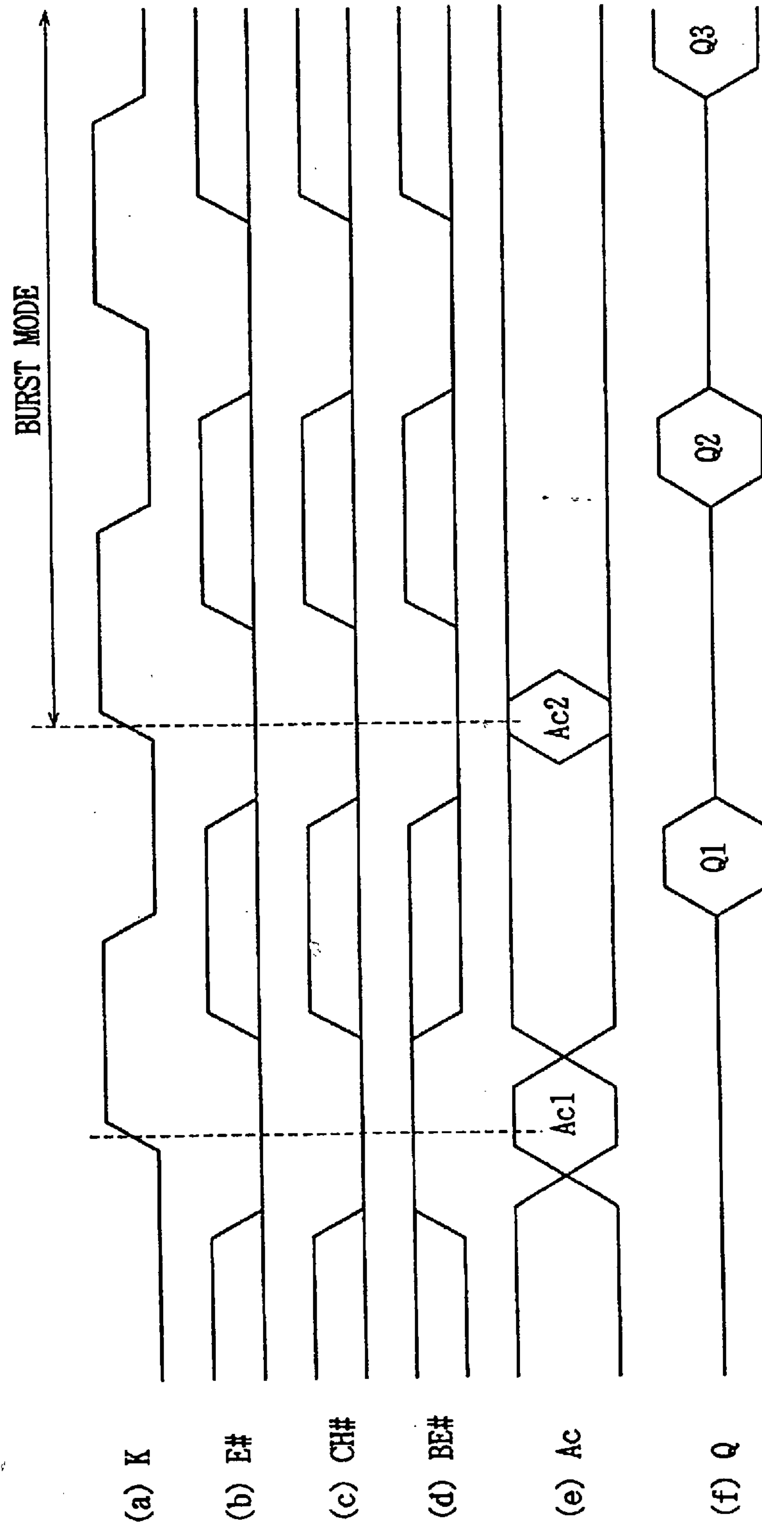


FIG. 198

F I G. 1 9 9

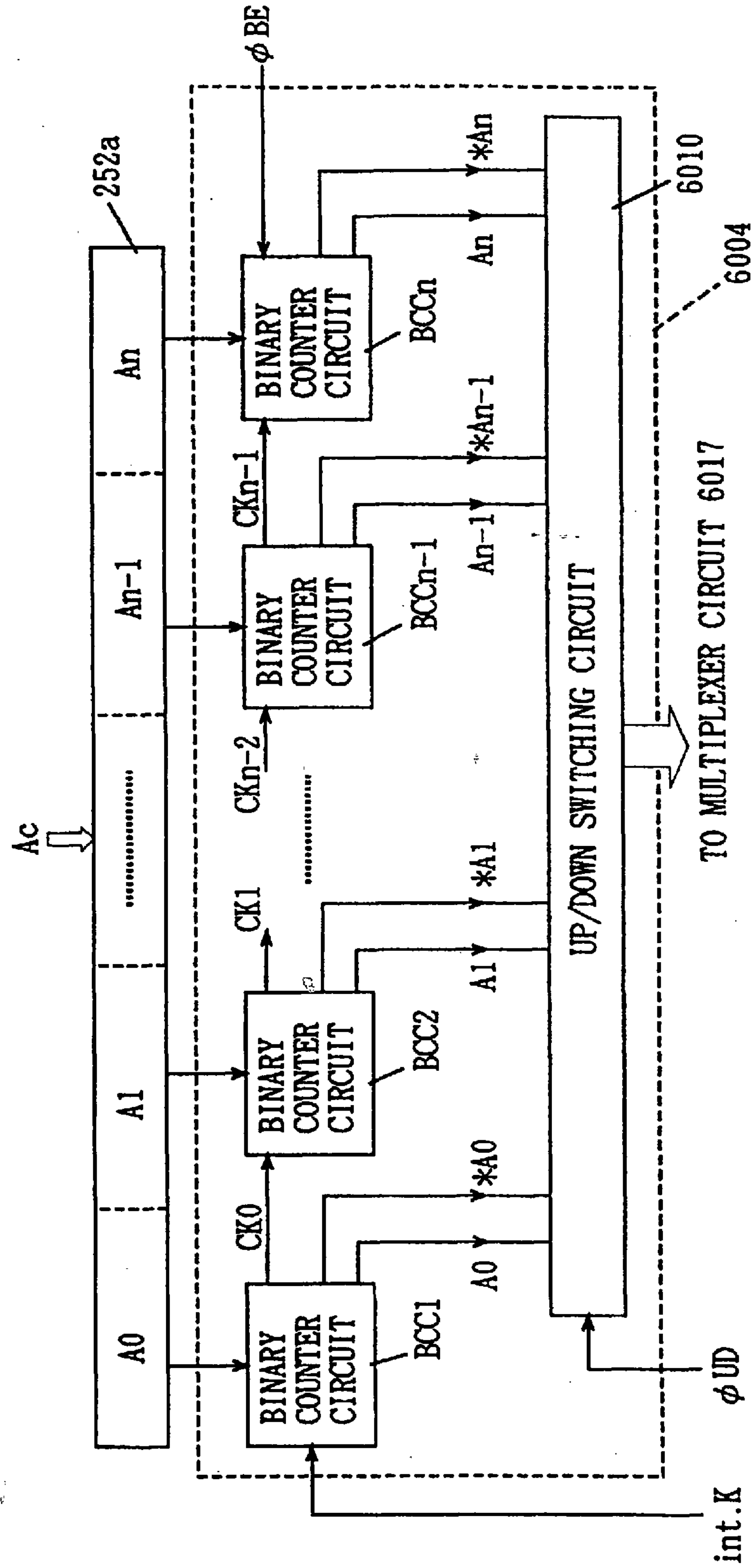


FIG. 200

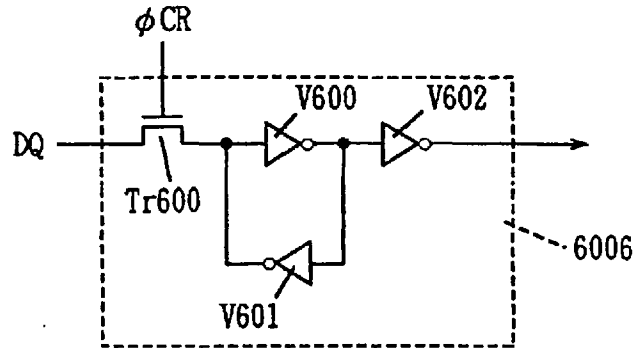


FIG. 201

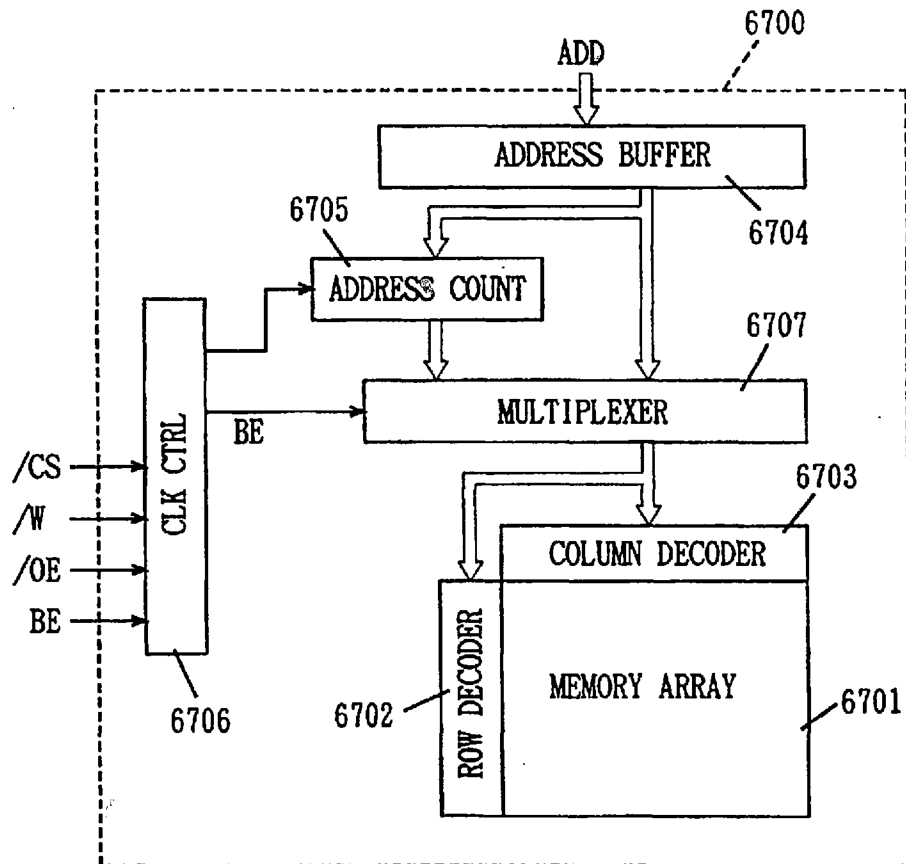


FIG. 202

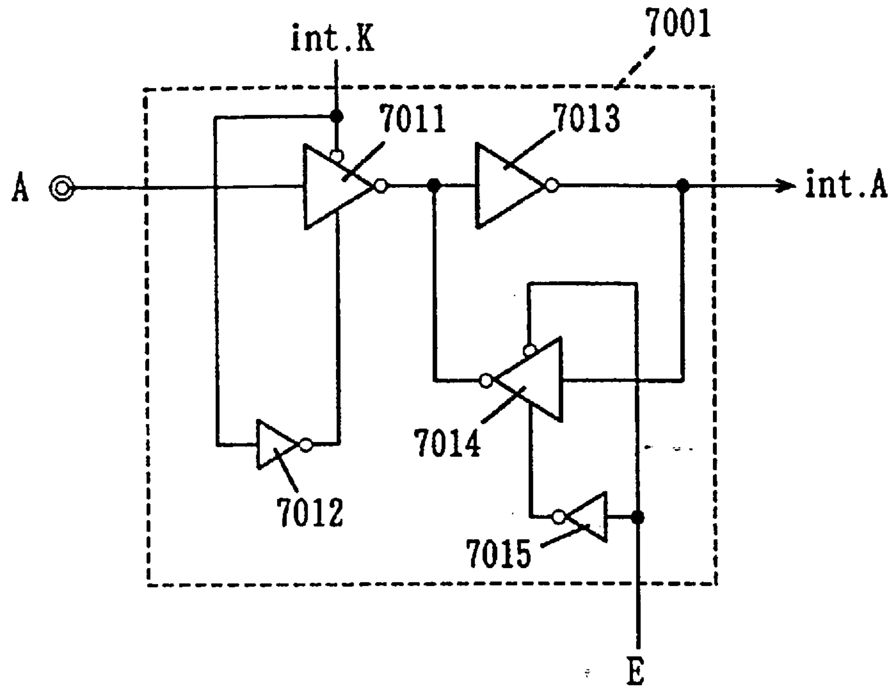
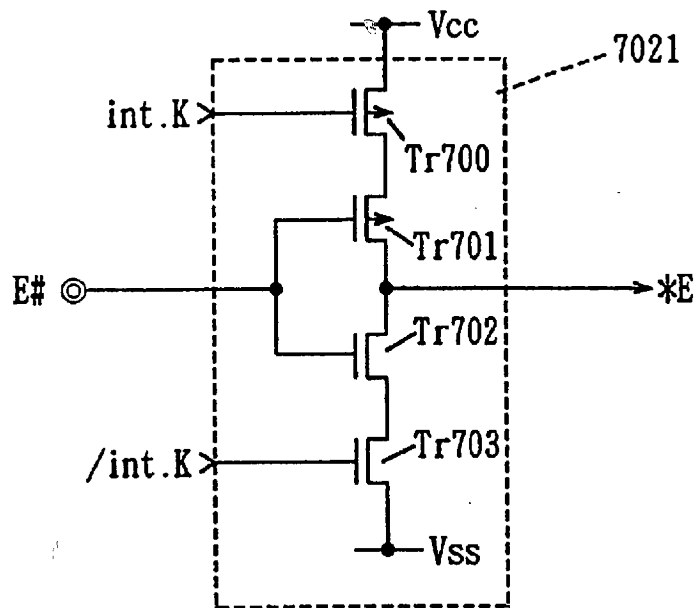


FIG. 203



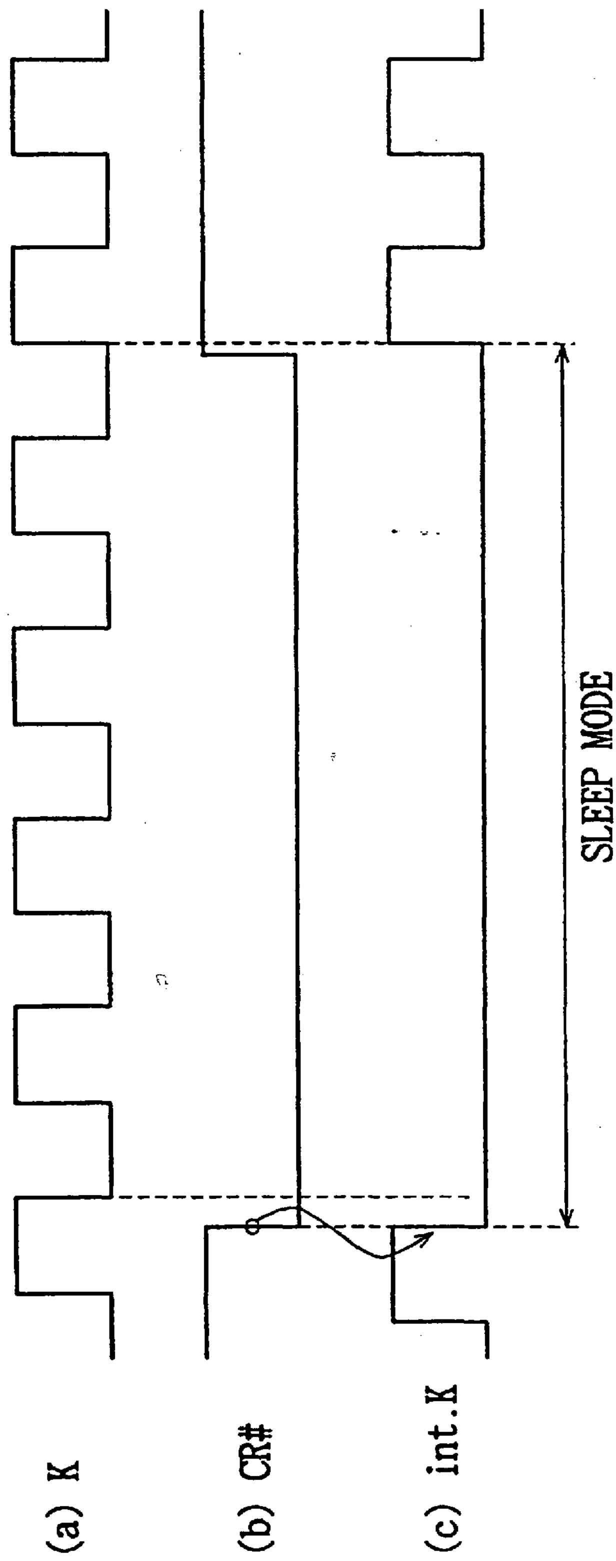


FIG. 204

FIG. 205

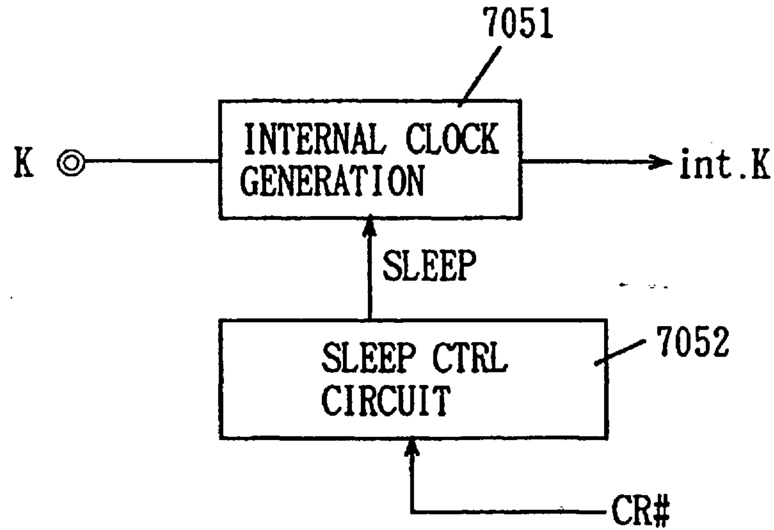
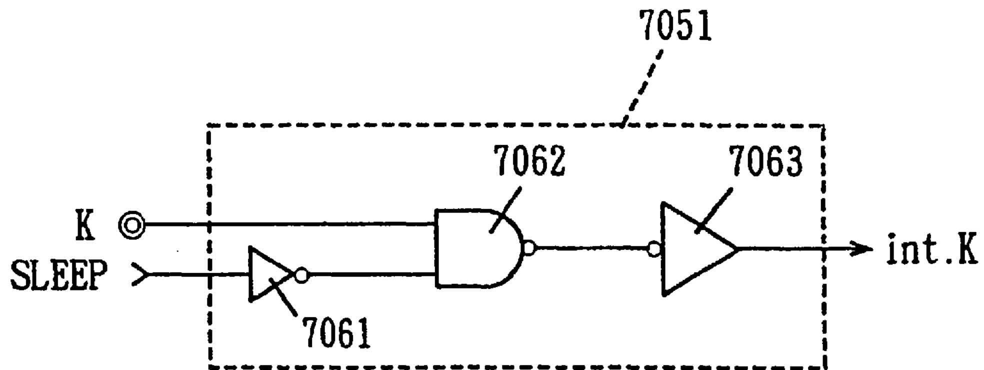


FIG. 206



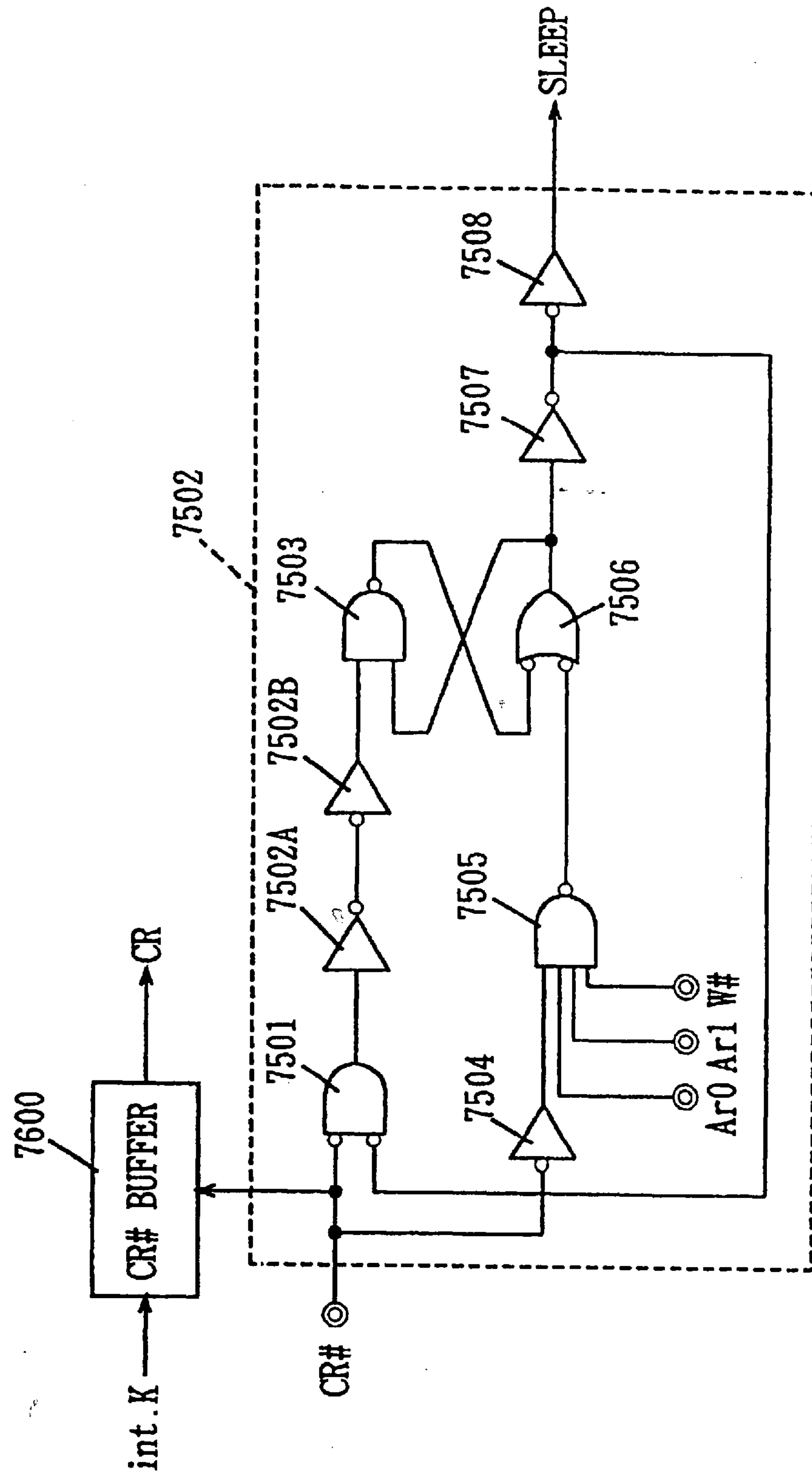


FIG. 207

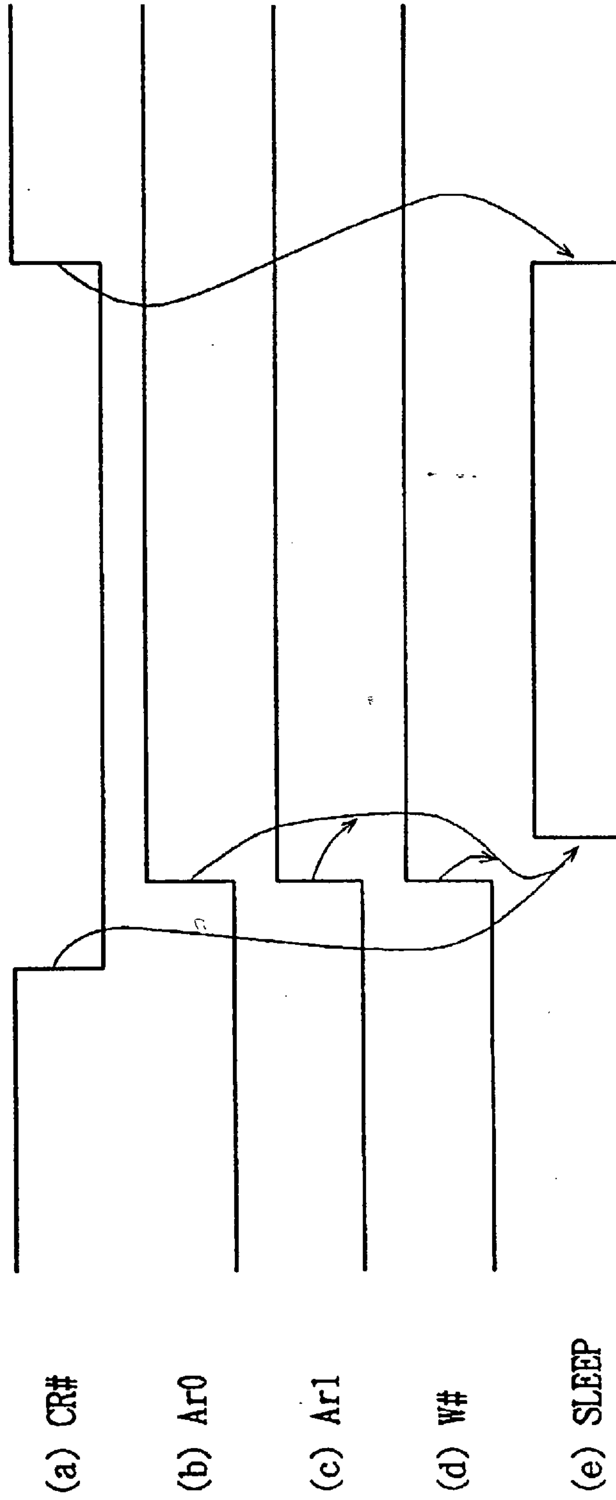


FIG. 208

FIG. 209

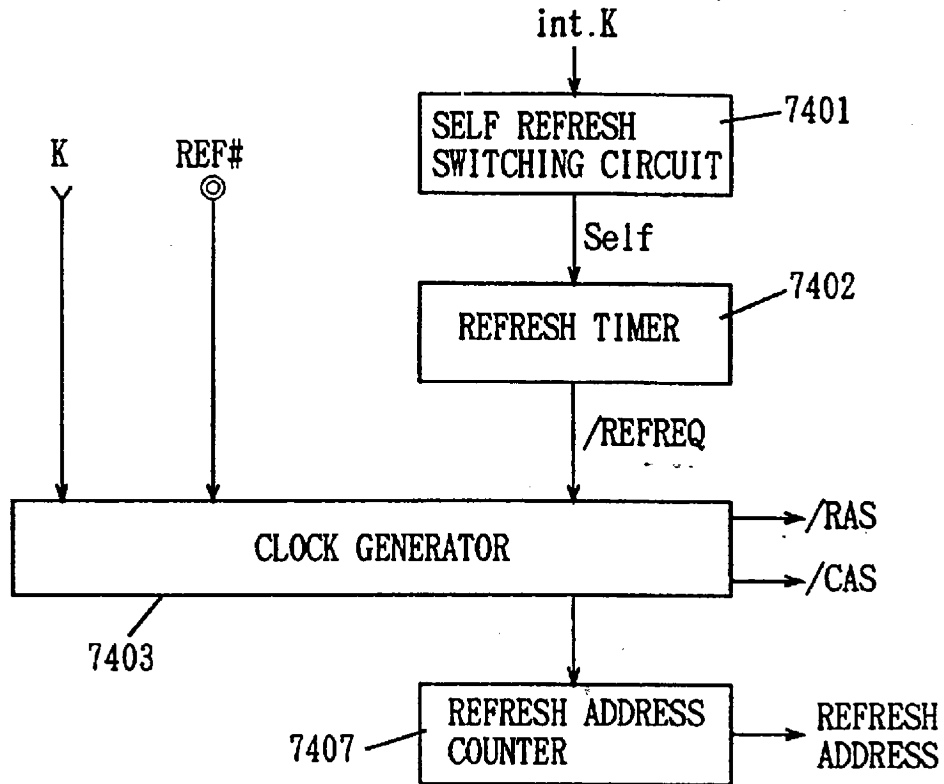


FIG. 210

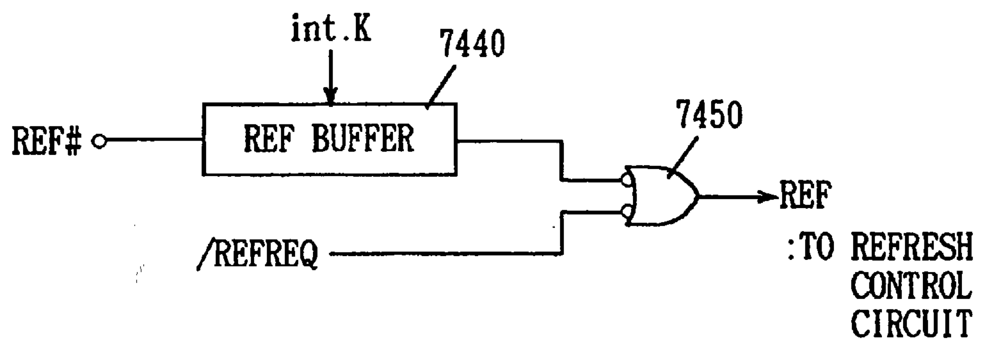


FIG. 211

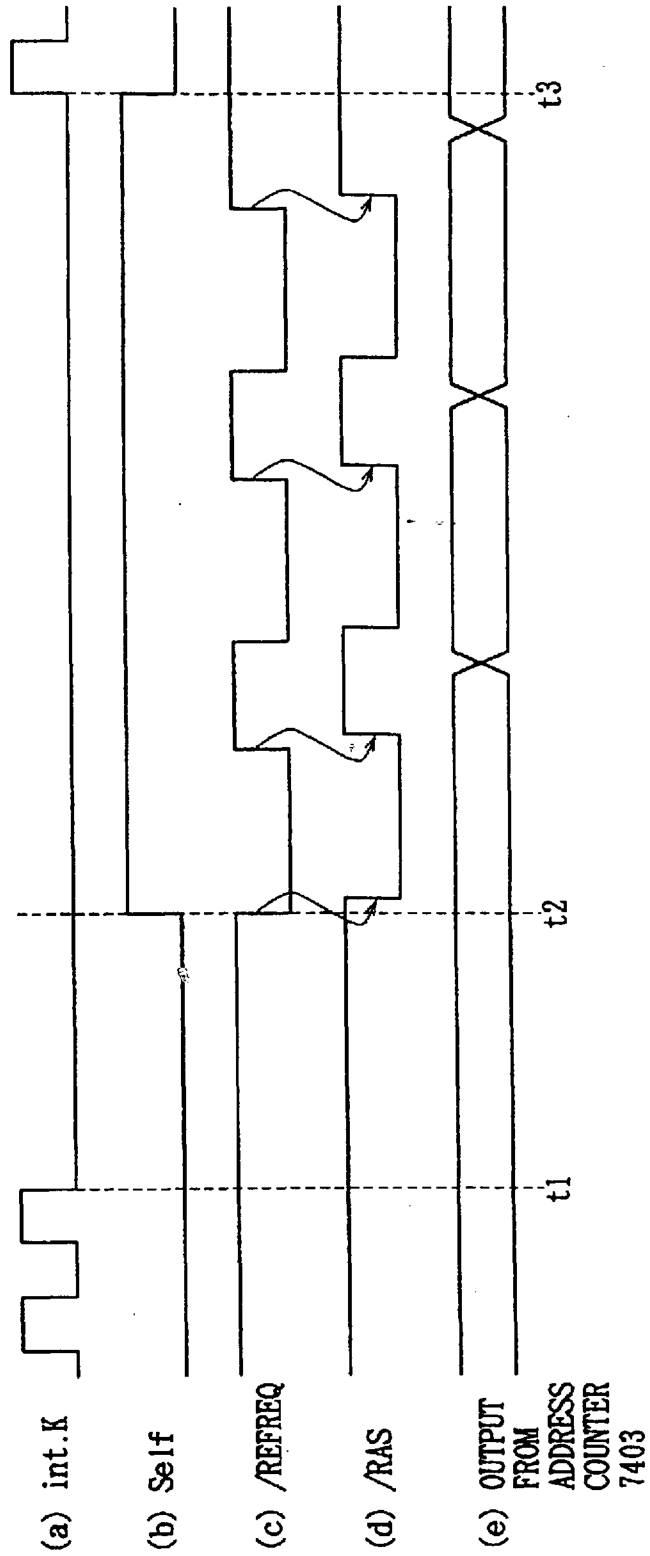
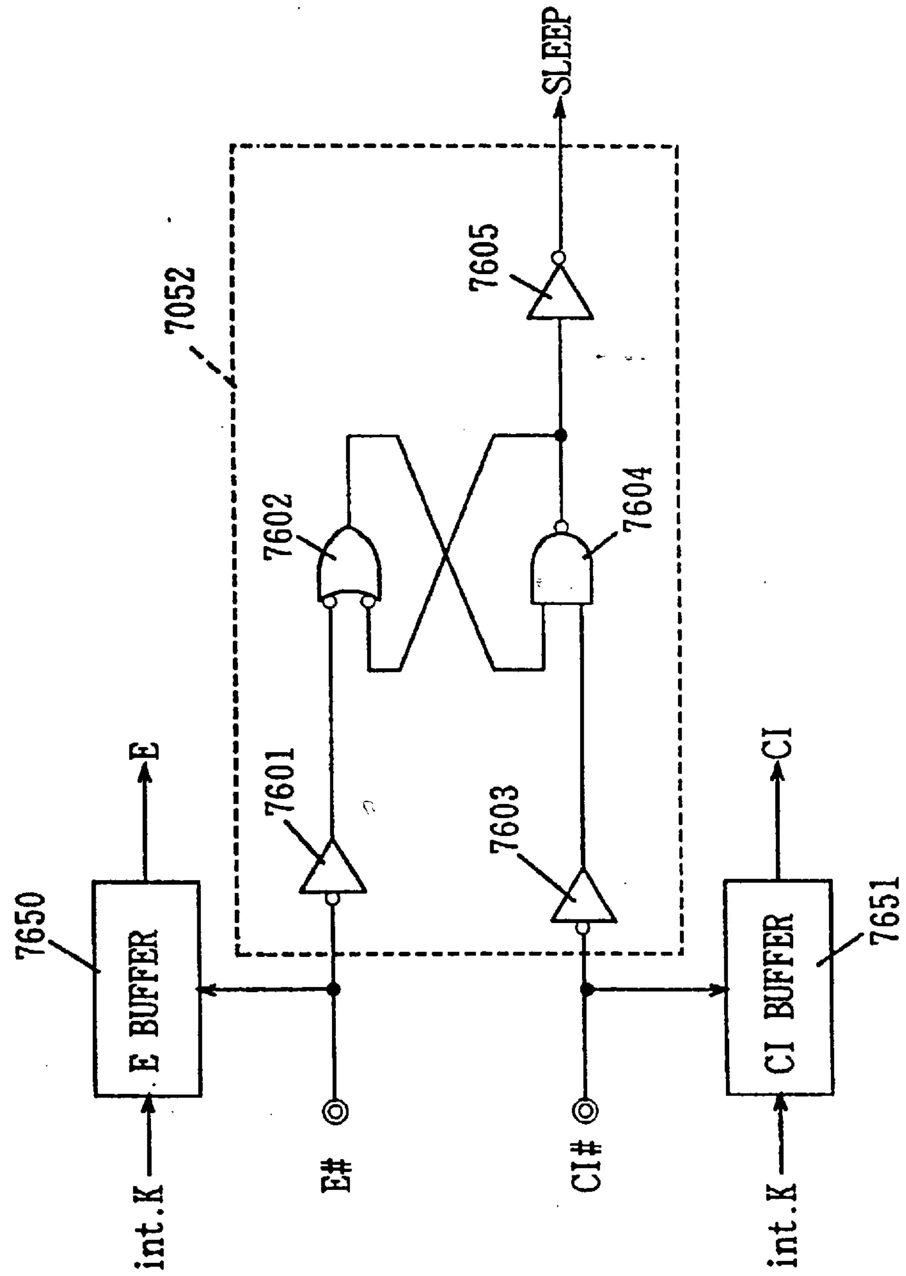


FIG. 212



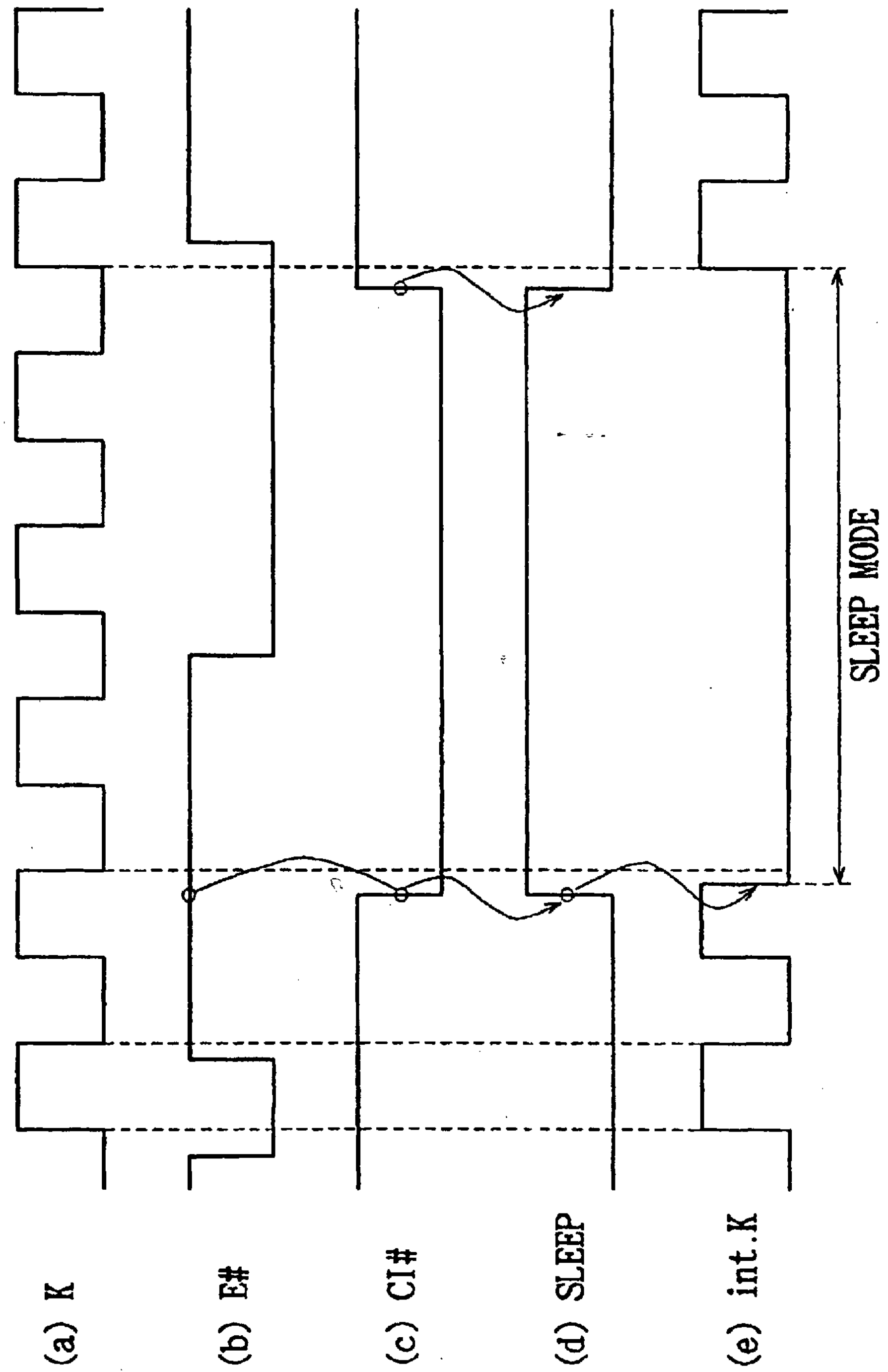

F I G. 2 1 3
(a) K
(b) E#
(c) CI#
(d) SLEEP
(e) int.K
SLEEP MODE

FIG. 214

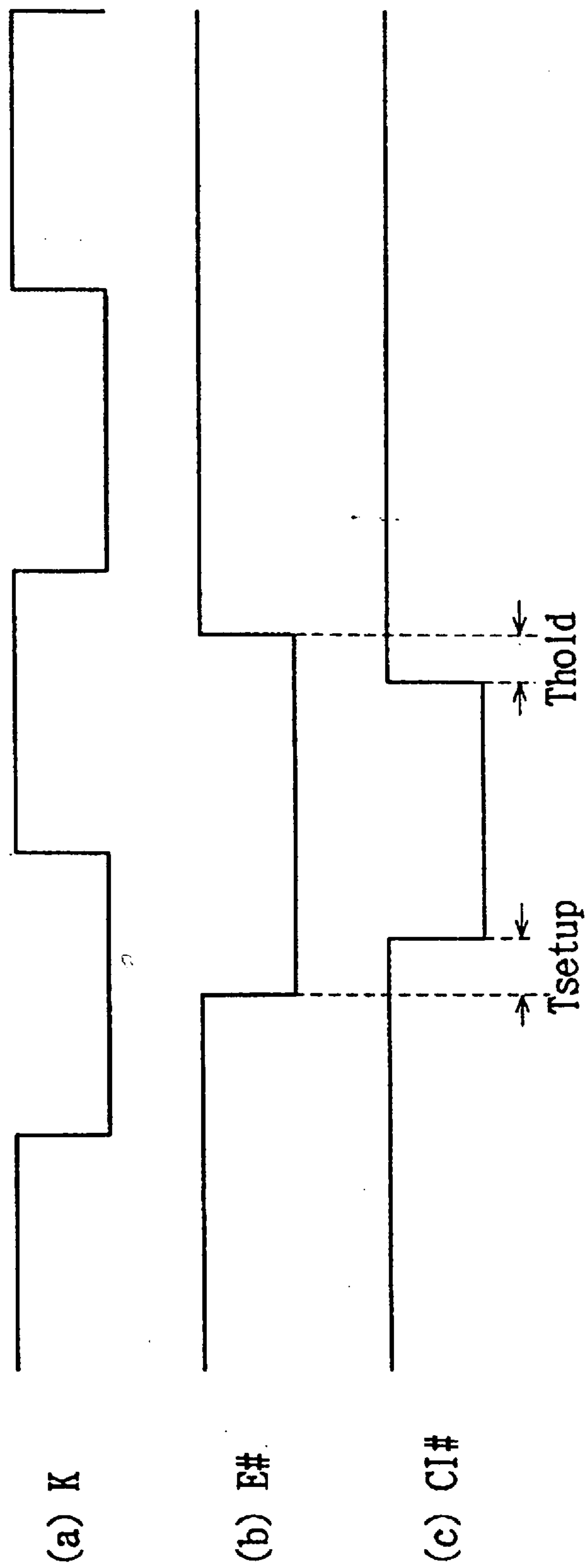


FIG. 215

	E#	CH#	CC1# (CI#)	CC2# (CR#)	W#	REF#	
STAND BY	H	×	×	×	×	H	
REFRESH	H	×	×	×	×	L	
HIT READ	L	L	H	H	H	H/L	
HIT WRITE	L	L	H	H	L	H/L	
HIT READ BURST	L	L	H	L	H	H/L	
HIT WRITE BURST	L	L	H	L	L	H/L	
HIT READ(& ARRAY WRITE)	L	L	L	H	H	H	CHCHE→CPU,LATCH→ARRAY
HIT WRITE(& ARRAY WRITE)	L	L	L	H	L	H	CACHE←CPU,LATCH→ARRAY
HIT READ BURST(·ARRAY WRITE)	L	L	L	L	H	H	
HIT WRITE BURST(·ARRAY WRITE)	L	L	L	L	L	H	
MISS READ	L	H	H	H	H	H	CACHE→LATCH,ARRAY→CACHE→CPU
MISS WRITE	L	H	H	H	L	H	CACHE→LATCH,ARRAY→CACHE←CPU
ARRAY WRITE(LATCH→ARRAY)	L	H	H	L	H	H	FOR HIGH SPEED COPY BACK
ARRAY WRITE(CACHE→ARRAY)	L	H	H	L	L	H	ARRAY INITIALIZATION
ARRAY DIRECT ACCESS	L	H	L	H	H/L	H/L	ARRAY INITIALIZATION
COMMAND REGISTER	L	H	L	L	H/L	H/L	

SEMICONDUCTOR MEMORY DEVICE

This application is a Continuation of application Ser. No. 08/865,310 filed May 29, 1997, now U.S. Pat. No. 6,026, 029, which is a Divisional of application Ser. No. 08/625, 578 filed Mar. 28, 1996, now U.S. Pat. No. 5,848,004, which is a Continuation of application Ser. No. 08/464,033 filed Jun. 5, 1995, now abandoned, which is a Divisional of application Ser. No. 07/869,917 filed Apr. 15, 1992, now U.S. Pat. No. 5,652,723.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to semiconductor memory devices and, specifically, to a clock synchronized type semiconductor memory device which operates in synchronization with externally applied clock signals. More specifically, the present invention relates to a structure of a semiconductor memory device containing a cache, in which a dynamic random access memory (DRAM) having a large storage capacity serving as a main memory, and a static random access memory (SRAM) having small storage capacity serving as a cache memory are integrated on the same semiconductor chip.

2. Description of the Background Art

Historical Review on Memory Environment in a Conventional Data Processing System

(i) Usage of Standard DRAM as a Main Memory

Operation speed of recent 16-bit or 32-bit microprocessing unit (MPU) has been so much increased as to have operation clock frequency as high as 25 MHz or higher. In a data processing system, a standard DRAM (Dynamic Random Access Memory) is often used as a main memory having large storage capacity, since cost per bit is low. Although access time in the standard DRAM has been reduced, the speed of operation of the MPU has been increased much faster than that of the standard DRAM. Consequently, in a data processing system using the standard DRAM as a main memory, increase of wait state is inevitable. The gap in speed of operation between MPU and the standard DRAM is inevitable because the standard DRAM has the following characteristics.

(1) A row address and a column address are time divisionally multiplexed and applied to the same address pin terminals. The row address is taken in the device at a falling edge of a row address strobe signal/RAS. The column address is taken in the device at a falling edge of a column address strobe signal/CAS. The row address strobe signal/RAS defines start of a memory cycle and activates row selecting circuitry. The column address strobe signal/CAS activates column selecting circuitry. Since a prescribed time period called "RAS-CAS delay time (tRCD)" is necessary from the time the signal/RAS is set to an active state to the time the signal/CAS is set to the active state, there is a limit in reducing the access time, namely, there is a limit derived from address multiplexing.

(2) When the row address strobe signal/RAS is once raised to set the DRAM to a standby state, the row address strobe signal/RAS cannot fall to "L" again until a time period called a RAS precharge time (tRP) has lapsed. The RAS precharge time is necessary for surely precharging various signal lines in the DRAM to predetermined potentials. Due to the RAS precharge time TRP, the cycle time of DRAM cannot be reduced. In addition, when the cycle time of the DRAM is reduced, the number of charging/discharging of signal lines in the DRAM is increased, which increases current consumption.

(3) The higher speed of operation of the DRAM can be realized by circuit technique such as improvement of layout, increase of degree of integration of circuits, development in process technique and by applicational improvement such as improvement in the method of driving. However, the speed of operation of the MPU is increased at much faster rate than DRAM. The speed of operation of semiconductor memories is hierarchical. For example, there are high speed bipolar RAMs using bipolar transistors such as ECLRAMs (Emitter Coupled RAM) and Static RAM, and relatively low speed DRAMs using MOS transistors (insulated gate type field effect transistors). It is very difficult to expect the operation speed (cycle time) as fast as several tens ns (nano seconds) in a standard DRAM formed of MOS transistors.

There have been various applicational improvements to stop the gap between speed of operations of the MPU and the standard DRAM. Such improvements mainly comprise the following two approaches. (1) Use of high speed mode of the DRAM and interleave method (2) External provision of a high speed cache memory (SRAM).

The first approach (1) includes a method of using a high speed mode such as a static column mode or a page mode, and a method of combining the high speed mode and the interleave method. in the static column mode, one word line (one row) is selected, and thereafter only the column address is changed successively, to successively access memory cells of this row. In the page mode, one word line is selected, and then column addresses are successively taken by toggling the signal/CAS to successively access memory cells connected to the selected one word line. In either of these modes, memory cells can be accessed without toggling the signal/RAS, enabling higher speed accessing than the normal access using the signals/RAS and/CAS.

In the interleave method, a plurality of memories are provided in parallel to a data bus, and by alternately or successively accessing the plurality of memories, the access time is reduced in effect. The use of high speed mode of the DRAM and combination of the high speed mode and the interleave method have been known as a method of using the standard DRAM as a high speed DRAM in a simple and relatively effective manner.

The second approach (2) has been widely used in a main frame art. A high speed cache memory is expensive. However, in the field of personal computers in which high performance as well as low cost are desired, this approach is employed in some parts of the field with a sacrifice of cost. There are three possible ways to provide the high speed cache memory. Namely,

(a) the high speed cache memory is contained in the MPU itself;

(b) the high speed cache memory is provided outside the MPU; and

(c) the high speed cache memory is not separately provided but the high speed mode contained in the standard DRAM is used as a cache (the high speed mode is used as a pseudo cache memory). When a cache hit occurs, the standard DRAM is accessed in the high speed mode, and at the time of a cache miss, the standard DRAM is accessed in the normal mode.

The above mentioned three ways (a) to (c) have been employed in the data processing systems in some way or other. In most MPU systems, the memories are organized in a bank structure and interleaving is carried out on bank by bank basis in order to conceal the RAS precharge time (TRP) which is inevitable in the DRAM, in view of cost. By this method, the cycle time of the DRAM can be substantially one half that of the specification value.

The method of interleave is effective only when memories are sequentially accessed. When the same memory bank is to be continuously accessed, it is ineffective. Further, substantial improvement of the access time of the DRAM itself cannot be realized. The minimum unit of the memory must be at least 2 banks.

When the high speed mode such as the page mode or the static column mode is used, the access time can be reduced effectively only when the MPU successively accesses a certain page (data of a designated one row). This method is effective to some extent when the number of banks is comparatively large, for example 2 to 4, since different rows can be accessed in different banks. When the data of the memory requested by the MPU does not exist in the given page, it is called a "miss hit" (cache miss). Normally, a group of data are stored in adjacent addresses or sequential addresses. In the high speed mode, a row address, which is one half of the addresses, has been already designated, and therefore possibility of "miss hit" is high.

When the number of banks becomes as large as 30 to 40, data of different pages can be stored in different banks, and therefore the "miss hit" rate is remarkably reduced. However, it is not practical to provide 30 to 40 banks in a data processing system. In addition, if a "miss hit" occurs, the signal/RAS is raised and the DRAM must be returned to the precharge cycle in order to re-select the row address, which sacrifices the characteristic of the bank structure.

In the above described second method (2), a high speed cache memory is provided between the MPU and the standard DRAM. In this case, the standard DRAM may have relatively low speed of operation. Standard DRAMs having storage capacities as large as 4M bits or 16M bits have come to be used. In a small system such as a personal computer, the main memory thereof can be formed by one or several chips of standard DRAMs. External provision of the high speed cache memory is not so effective in such a small system in which the main memory can be formed of one standard DRAM. If the standard DRAM is used as the main memory, the data transfer speed between the high speed cache memory and the main memory is limited by the number of data input/output terminals of the standard DRAM, which constitutes a bottleneck in increasing the speed of the system.

When the high speed mode is used as a pseudo cache memory, the speed of operation thereof is slower than the high speed cache memory, and it is difficult to realize the desired system performance.

(ii) Consideration on a Conventional Cache Containing DRAM

Provision of the high speed cache memory (SRAM) in the DRAM is proposed as a method of forming a relatively inexpensive and small system, which can solve the problem of sacrifice of system performance when the interleave method or the high speed operation mode is used. More specifically, a single chip memory having a hierarchical structure of a DRAM serving as a main memory and a SRAM serving as a cache memory has been conceived. The one-chip memory having such a hierarchical structure is called a cache DRAM (CDRAM). The CDRAM will be described with reference to FIGS. 1 through 4.

FIG. **1** shows a structure of a main portion of a conventional standard 1 megabit DRAM. As shown in FIG. **1**, the DRAM comprises a memory cell array **500** including a plurality of memory cells MC arranged in a matrix of rows and columns. A row of memory cells are connected to one word line WL. A column of memory cells MC are connected to one column line CL. Normally, the column line CL is formed by a pair of bit lines. A memory cell MC is positioned at a crossing of one of the pair of bit lines and one word line WL. In a 1M DRAM, the memory cells MC are arranged in a matrix of 1024 rows×1024 columns. Namely, the memory cell array **500** includes 1024 word lines WLs and 1024 column lines CLs (1024 pairs of bit lines).

The DRAM further comprises a row decoder **502** which decodes an externally applied row address (not shown) for selecting a corresponding row of the memory cell array **500**; a sense amplifier which detects and amplifies data of the memory cell connected to the word line selected by the row decoder **502**; and a column decoder which decodes an externally applied column address (not shown) for selecting a corresponding column of the memory cell array **502**. In FIG. **1**, the sense amplifier and the column decoder are denoted by one block **504**. If the DRAM has a×1 bit structure in which input/output of data is effected bit by bit, one column line CL (a bit line pair) is selected by the column decoder.

If the DRAM has a×4 bit structure in which input/output of data is effected 4 bits by 4 bits, 4 column lines CL are selected by the column decoder. One sense amplifier is provided for each column line (bit line pair) CL in the block **504**.

In memory access for writing data to or reading data from the memory cell MC in the DRAM, the following operation is carried out. First, a row address is applied to the row decoder **502**. The row decoder **502** decodes the row address and raises the potential of one word line WL in the memory cell array **500** to "H". Data of the 1024 bits of memory cells MC connected to the selected word line WL are transmitted to corresponding column lines CL. The data on the column lines CL are amplified by sense amplifiers included in the block **504**. Selection of a memory cell to which the data is written or from which the data is read out of the memory cells connected to the selected word line WL is carried out by a column selection signal from the column decoder included in the block **504**. The column decoder decodes column address signals (more accurately, internal column address signals), and generates a column selecting signal for selecting the corresponding column in the memory cell array **500**.

In the above described high speed mode, column addresses are successively applied to the column decoder included in the block **504**. In the static column mode operation, column addresses applied at predetermined time intervals are decoded as new column addresses by the column decoder, and the corresponding memory cell out of the memory cells connected to the selected word line WL is selected by the column line CL. In the page mode, new column address is applied at every toggling of the signal /CAS, and the column decoder decodes the column address to select the corresponding column line. In this manner, one row of memory cells MC connected to the selected word line WL can be accessed at high speed by setting one word line WL at a selected state and by changing the column addresses only.

FIG. **2** shows a general structure of a conventional **1**M bit CDRAM. Referring to FIG. **2**, the conventional CDRAM comprises, in addition to the components of the standard DRAM shown in FIG. **1**, SRAM **506** and a transfer gate **508** for transferring data between one row of the memory cell array **500** of the DRAM and the SRAM **506**. The SRAM includes a cache register provided corresponding to each column line CL of the memory cell array **500** so as to enable simultaneous storage of data of one row of the DRAM memory cell array **500**. Therefore, 1024 cache registers are

provided. The cache register is formed by a static memory cell (SRAM cell).

In the structure of the CDRAM shown in FIG. 2, when a signal representing a cache hit is externally applied, the SRAM 506 is accessed, enabling access to the memory at high speed. At the time of a cache miss (miss hit), the DRAM portion is accessed.

A CDRAM as described above having a DRAM of a large storage capacity and a high speed SRAM integrated on the same chip is disclosed in, for example, Japanese Patent Laying-Open Nos. 60-7690 and 62-38590.

In the above described conventional CDRAM structure, column lines (bit line pairs) CL of the DRAM memory cell array 500 and column lines (bit line pairs) of the SRAM (cache memory) 506 are connected in one to one correspondence through a transfer gate 508. More specifically, in the above described conventional CDRAM structure, data of the memory cells connected to one word line WL in the DRAM memory cell array 500 and the data of the same number of SRAM cells as memory cells of one row of the memory cell array 500 are transferred bi-directionally and simultaneously, through the transfer gate 508. In this structure, the SRAM 506 is used as a cache memory and the DRAM is used as a main memory.

The so called block size of the cache is considered to be the number of bits (memory cells) the contents of which are rewritten in one data transfer in SRAM 506. Therefore, the block size is the same as the number of memory cells which are physically coupled to one word line WL of DRAM memory cell array 500. As shown in FIGS. 1 and 2, when 1024 memory cells are physically connected to one word line WL, the block size is 1024.

Generally, when the block size becomes larger, the hit rate is increased. However, if the cache memory has the same size, the number of sets is reduced in inverse proportion to the block size, and therefore the hit rate is decreased. For example, when the cache size is 4K bits and the block size 1024, the number of sets is 4. However, if the block size is 32, the number of sets is 128. Therefore, in the conventional CDRAM structure, the block size is made too large, and the cache hit rate cannot be very much improved.

A structure enabling reduction in block size is disclosed in, for example, Japanese Patent Laying-Open No. 1-146187. In this prior art, column lines (bit line pairs) of the DRAM array and the SRAM array are arranged in one to one correspondence, but they are divided into a plurality of blocks in the column direction. Selection of the block is carried out by a block decoder. At the time of a cache miss (miss hit), one block is selected by the block decoder. Data are transferred only between the selected DRAM block and the associated SRAM block. By this structure, the block size of the cache memory can be reduced to an appropriate size. However, there remains the following problem unsolved.

FIG. 3 shows a standard array structure of a 1M bit DRAM array. In FIG. 3, the DRAM array is divided into 8 memory blocks DMB1 to DMB8. A row decoder 502 is commonly provided for the memory blocks DMB1 to DMB8 on one side in the longitudinal direction of the memory array. For each of the memory blocks DMB1 to DMB8, (sense amplifier+column decoder) blocks 504-1 to 504-8 are provided.

Each of the memory blocks DMB1 to DMB8 has the capacity of 128K bits. In FIG. 3, one memory block DMB is shown to have 128 rows and 1024 columns, as an example. One column line CL includes a pair of bit lines BL, /BL.

As shown in FIG. 3, when the DRAM memory cell array is divided into a plurality of blocks, one bit line BL (and/BL) becomes shorter. In data reading, charges stored in a capacitor (memory cell capacitor) in the memory cell are transmitted to a corresponding bit line BL (or/BL). At this time the amount of potential change generated on the bit line BL (or/BL) is proportional to the ratio Cs/Cb of the capacitance Cs of the memory cell capacitor to the capacitance Cb of the bit line BL (or/BL). If the bit line BL (or/BL) is made shorter, the bit line capacitance Cb can be reduced. Therefore, the amount of potential change generated on the bit line can be increased.

In operation, sensing operation in the memory block (memory block DMB2 in FIG. 3) including the word line WL selected by the row decoder 502 is carried out only, and other blocks are kept in a standby state. Consequently, power consumption associated with charging/discharging of the bit lines during sensing operation can be reduced.

When the above described partial activation type CDRAM is applied to the DRAM shown in FIG. 3, a SRAM register and a block decoder must be provided for each of the memory blocks DMB1 to DMB8, which significantly increases the chip area.

In this structure, only SRAM cache registers corresponding to the selected block operate, and therefore, efficiency in using the SRAM cache registers is low.

Further, the bit lines of the DRAM array and of the SRAM array are in one to one correspondence, as described above. When direct mapping method is employed as the method of mapping memories between the main memory and the cache memory, then the SRAM 506 is formed by 1024 cache registers arranged in one row, as shown in FIG. 2. In this case, the capacity of the SRAM cache is 1K bits.

When 4 way set associative method is employed as the mapping method, the SRAM array 506 includes 4 rows of cache registers 506a to 506d as shown in FIG. 4. One of the 4 rows of cache registers 506a to 506d is selected by the selector 510 in accordance with a way address. In this case, the capacity of the SRAM cache is 4K bits.

As described above, the method of memory cell mapping between the DRAM array and the cache memory is determined dependent on the internal structure on the chip. When the mapping method is to be changed, the cache size also must be changed.

In both of the CDRAM structures described above, the bit lines of the DRAM array and the SRAM array are in one to one correspondence. Therefore, the column address of the DRAM array is inevitably the same as the column address of the SRAM array. Therefore, full associative method in which memory cells of the DRAM array are mapped to an arbitrary position of the SRAM array is impossible in principle.

Another structure of a semiconductor memory device in which the DRAM and the SRAM are integrated on the same chip is disclosed in Japanese Patent Laying-Open No. 2-87392. In this prior art, the DRAM array and the SRAM array are connected through an internal common data bus. The internal common data bus is connected to an input/output buffer for inputting/outputting data to and from the outside of the device. Selected memory cells of the DRAM array and the SRAM array can be designated by separate addresses.

However, in this structure of the prior art, data transfer between the DRAM array and the SRM array is carried out by an internal common data bus, and therefore the number of bits which can be transferred at one time is limited by the number of internal data bus lines, which prevents high speed rewriting of the contents of the cache memory. Therefore, as in the above described structure in which the SRAM cache

is provided outside the standard DRAM, the speed of data transfer between the DRAM array and the SRAM array becomes a bottleneck, preventing provision of a high speed cache memory system.

(iii) Consideration on a General Clock Synchronized Type Semiconductor Device For the Problems of Which the Present Invention Includes the Solution

A semiconductor memory device of an application specific IC (ASIC) or for pipe line usage operates in synchronization with an external clock signal such as a system clock. Operation mode of a semiconductor memory device is determined dependent on states of external control signals at rising or falling edge of the external clock signal. The external clock signal is applied to the semiconductor memory device no matter whether the semiconductor memory device is being accessed or not. In this structure, in response to the external clock signal, input buffers or the like receiving the external control signals, address signals and data operate. In view of power consumption, it is preferred not to apply the external clock signal to the semiconductor memory device when the semiconductor memory device is not accessed, or to elongate period of the external clock signal.

Generally, a row address signal and the column address signal are applied multiplexed time divisionally to the DRAM. The row address signal and the column address signal are taken in the device in synchronization with the external clock signal. Therefore, when the conventional DRAM is operated in synchronization with the external clock signal, it takes long time to take the row address signal and the column address signal. Therefore, if low power consumption is given priority, the DRAM can not be operated at high speed.

If the conventional semiconductor memory device is operated in synchronization with the external clock signal, the speed of operation is determined solely by the external clock signal. If the semiconductor memory device is to be used where low power consumption is given priority over the high speed operation with the speed defined by the external clock signal, the conventional clock synchronized type semiconductor memory device can not be used for such application.

In a clock synchronized type semiconductor memory device, control signals and address signals are taken inside in synchronization with the clock signal. The control signals and address signals are taken inside by buffer circuits. Each buffer circuit is activated in sychronization with the clock signal and generates an internal signal corresponding to the applied external signal. In a standby state or the like, valid control signals and valid address signals are not applied. However, external clock signals are continuously applied, causing unnecessary operations of the buffer circuits. This prevents reduction in power consumption during standby state. If the cycle period of the external clock signal becomes shorter, the number of operations of the buffer circuits is increased, causing increase of power consumption during standby period. This is a serious problem in realizing low power consumption.

(iv) Consideration on the Problems in Refreshing Operation in a Conventional RAM

If the semiconductor memory device includes dynamic memory cells (DRAM cells), the DRAM cells must be periodically refreshed. The refresh mode of a DRAM generally includes an auto refresh mode and a self refresh mode, as shown in FIGS. 5 and 6.

FIG. 5 shows waveforms in the auto refresh operation. In the auto refresh mode, a chip select signal *CE is set to "H" and an external refresh designating signal *REF is set to "L". In response to a fall of the external refresh designating signal *REF, an internal control signal int. *RAS for driving row selecting circuitry falls to "L". In response to the internal control signal int. *RAS, a word line is selected in accordance with a refresh address generated from a built-in address counter, and memory cells connected to the selected word line are refreshed. In the auto refresh mode, the timing of refreshing the semiconductor memory device is determined by the externally applied refresh designating signal *REF. Therefore, whether or not refreshing is being carried out in the semiconductor memory device can be known outside the memory device.

FIG. 6 shows waveforms in the self refresh operation. In the self refresh mode, the chip select signal *CE is set to "H" and the external refresh designating signal *REF is set to "L". When the external refresh designating signal *REF falls to "L", the external control signal int. *RAS is generated, and a word line is selected in accordance with the refresh address from the built-in address counter. Thereafter, sensing operation and rewriting of the memory cells connected to the selected word line are carried out, and the memory cells connected to the word line WL are refreshed.

The first cycle of self refreshing is the same as that of auto refreshing. When the chip select signal *CE is at "H" and the refresh designating signal *REF is kept at "L" for a predetermined time period TF or longer, a refresh request signal is generated from a built-in timer. In response, the internal control signal int. *RAS is generated, the word line is selected and the memory cells connected to the selected word line are refreshed. This operation is repeated while the refresh designating signal *REF is at "L". In the refreshing operation in the self refresh mode, the timings of refreshing are determined by a timer contained in the semiconductor memory device. Therefore, timings of refreshing can not be known from the outside. Normally, data can not be externally accessed in the self refresh mode. Therefore, in the normal mode, sell refreshing is not carried out. The self refresh mode is generally carried out at a standby for retaining the data.

Different semiconductor chips have different upper limits of refresh period necessary for retaining data (see NIKKEI ELECTRONICS, Apr. 6, 1987, p. 170, for example). Generally, a guaranteed value for retaining data is measured by testing the semiconductor memory device, and period of a timer defining the self refresh cycle is programmed in accordance with the guaranteed value, for carrying out self refreshing. When auto refresh mode and self refresh mode are selectively used, the guaranteed value for retaining data must be measured in order to determine the self refresh cycle. As shown in FIG. 6, in the self refresh mode, an operation similar to that in the auto refreshing is carried out in response to the external refresh designating signal *REF, and then refreshing operation in accordance with the timer is carried out. Therefore, in an accurate sense, the self refresh cycle means a cycle carried out after a lapse of a prescribed time period TF successive to the auto refreshing. In the self refresh cycle, the refresh timing is determined by the contained timer, as described above, and the timings of refreshing can not be known from the outside. Therefore, the self refresh cycle can not be used as a method of hidden refreshing, for example, in a normal operation mode.

(v) Consideration on Array Arrangement in CDRAM and Data Transfer Between CDRAM and MPU (Burst Mode)

In a semiconductor memory device containing a DRAM array and a SRAM array, it is preferred to transfer data at high speed from the DRAM array to the SRAM array, so as

to enable high speed operation. When data are transferred from the DRAM array to the SRAM array, a row (word line) is selected, data of the memory cells connected to the selected word line are detected and amplified, and then a column is selected in the DRAM array.

Generally, a row address signal and a column address signal are applied multiplexed to the DRAM. Therefore, increase of the speed of data transfer from the DRAM array to the SRAM array is limited by this address multiplexing. In this case, it is possible to apply the row address and the column address simply in accordance with a non-multiplex method to the DRAM. However, in that case, the number of terminals for inputting DRAM addresses are increased significantly. When the number of terminals is increased, the chip size and the package size are increased, which is not preferable.

In addition, data transfer from the DRAM array to the SRAM array must be done after detection and amplification of the memory cell data by the sense amplifiers. Therefore, data transfer from the DRAM array to the SRAM array can not be carried out at high speed.

Further, some external operational processing units such as a CPU (Central Processing Unit) include a data transfer mode called a burst mode for carrying out data transfer at high speed. In the burst mode, a group of data blocks are transferred successively. A block of data is stored at successively adjacent address positions. Since the burst mode is a high speed data transfer mode, the data blocks are stored in the cache memory in the semiconductor memory device containing a cache. A semiconductor memory device containing a cache which can be easily connected to an operational processing unit having burst mode function has not yet been provided.

In order to implement a CDRAM, DRAM array and SRAM array are integrated on the same semiconductor chip. The semiconductor chip is housed in a package. The layout of DRAM array and SRAM array as well as the geometrical figures thereof on the chip are determined by the geometrical figure and the physical dimensions of the housing package.

DRAM array and its associated circuitry occupy a major area of a chip in CDRAM because DRAM is employed as a large storage capacity memory. Thus, the size and figure of DRAM array are substantially determined by the size and shape of the housing package.

In order to efficiently use the chip area, SRAM array should be arranged or laid out on the chip efficiently. However, no consideration has made on the configuration of SRAM array for implementing efficient chip area utilization and for housing CDRAM in a package of an arbitrary shape and size.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a novel CDRAM with various operational functions and efficient chip layout.

Another object of the present invention is to provide a semiconductor memory device in which self refreshing can be carried out in the normal mode.

A further object of the present invention is to provide a semiconductor memory device allowing data transfer between DRAM array and a SRAM array at a high speed and with less power consumption.

A further another object of the present invention is to provide a clock synchronized type semiconductor memory device in which power consumption at standby mode can be significantly reduced.

A still further object of the present invention is to provide a semiconductor memory device which can be accessed at high speed even at a cache miss (miss hit).

A still further object of the present invention is to provide a semiconductor memory device containing a cache which can be easily connected to an arithmetic operation unit having burst mode function.

A still further object of the present invention is to provide a semiconductor memory device which operates at high speed even if the period of external clock signals is made longer.

A still further object of the present invention is to provide a clock synchronized type semiconductor memory device which surely operates even if the period of the external clock signal is made longer or even if the external clock signal is generated intermittently.

A still further object of the present invention is to provide a semiconductor memory device containing a cache which operates at high speed without malfunction with low power consumption.

A still further object of the present invention is to provide a semiconductor memory device containing a cache which operates in synchronization with clocks, and operates at high speed without malfunction under low power consumption.

A still further object of the present invention is to provide a semiconductor memory device which can be readily applied to use where high speed operation is given priority and to use where low power consumption is given priority.

A still further object of the present invention is to provide a semiconductor memory device containing a cache which easily realizes high speed operation and low power consumption dependent on the intended use.

A still further object of the present invention is to provide a semiconductor memory device containing a cache operating in synchronization with clocks which easily realizes both high speed operation and low power consumption dependent on intended use.

A still further another object of the present invention is to provide an array arrangement which allows effective use of chip area.

Yet another object of the present invention is to provide an SRAM array arrangement having a flexible array structure which can easily correspond to an arbitrary shape of the DRAM array.

A yet further object of the present invention is to provide a semiconductor memory device containing a cache having an array arrangement having high density and suitable for high degree of integration.

The present invention includes various aspects each of which is recited independently of others in the following.

A semiconductor memory device in accordance with a first aspect of the present invention includes a DRAM array having dynamic memory cells; means for generating a refresh address; an automatic refresh means for refreshing the DRAM array in response to an external refresh designation; timer means measuring time for outputting a refresh request every prescribed timing; refresh means for refreshing the DRAM array in response to the refresh request from the timer means; refresh mode setting means for setting the refresh mode to either the auto refresh or self refresh mode; and input/output switching means for setting one pin terminal to a refresh designating input terminal or to a self refresh execution designating output terminal, in accordance with the refresh mode set by refresh mode setting means. The timer means is activated when self refresh mode is set by the refresh mode setting means.

In accordance with a second aspect of the present invention, the semiconductor memory device comprises first and second memory cell arrays each including a plurality of memory cells arranged in rows and columns; a first row address input terminal for receiving a first row address for designating a row of the first memory cell array; a first column address input terminal for receiving a first column address for designating a column of the first memory cell array; a second row address input terminal for receiving a second row address for designating a row of the second memory cell array; and a second column address input terminal for receiving a second column address for designating a column of the second memory cell array. The first row address input terminal and the first column address input terminal include input terminals different from each other. The second row address input terminal and the second column address input terminal include input terminals which are different from each other. The first column address input terminal includes a pin arrangement which is shared with at least one of the second row address input terminal and the second column address input terminal.

In accordance with the third aspect of the present invention, the semiconductor memory device includes first and second memory cell arrays each including a plurality of memory cells arranged in rows and columns; first address means for generating a first internal row address signal and a first internal column address signal for designating a row and a column of the first memory cell array in accordance with an external address; and second address means for generating a second internal row address and a second internal column address for designating a row and a column of the second memory cell array in accordance with the external address. The first and second address means are activated in synchronization with an external clock signal, and simultaneously generates the first internal row address signal, the first internal column address signal, the second internal row address signal and the second internal column address signal in accordance with the timing determined by the clock signal.

The semiconductor memory device in accordance with the fourth aspect of the present invention includes a DRAM array including a plurality of dynamic memory cells arranged in rows and columns; an SRAM array including a plurality of static memory cells arranged in rows and columns; data transfer means provided separate from an internal data transmitting line for transferring data between the DRAM array and the SRAM array; sense amplifier means for detecting and amplifying information of the selected memory cells of the DRAM array; and control means responsive to a transfer designation from the DRAM array to the SRAM array for activating the transferring means at a timing earlier than the timing of activating the sense amplifier means. Bit line data of the DRAM array are transmitted directly to the transfer means, not through the internal data line.

The semiconductor memory device in accordance with the fifth aspect of the present invention includes a DRAM array including a plurality of dynamic memory cells arranged in rows and columns; an SRAM array including a plurality of static memory cells arranged in rows and columns; amplifying means provided for each column of the DRAM array for amplifying signals on the corresponding column; sense amplifier means for amplifying and latching signals on the corresponding column; data transfer means provided separate from an internal data transmitting line for transferring data between the DRAM array and the SRAM array; means responsive to an address signal for selectively transmitting outputs from the amplifying means to the data transferring means; and control means responsive to a data transfer designation for activating the data transferring means before the activation of the sense amplifier means. The transfer mean includes means for forming a current mirror amplifying means by supplying current to the amplifying means.

In accordance with a sixth aspect of the present invention, the semiconductor memory device includes address input means for receiving address signals; address generating means responsive to a burst mode designation for successively generating address signals at prescribed timings; address selecting means receiving an output from address input means and an output from address generating means, responsive to the burst mode designation for selectively passing the output of the address generating means; and memory cell selecting means for selecting a corresponding memory cell out of a plurality of memory cells in accordance with the output from the address selecting means.

In accordance with a seventh aspect of the present invention, the semiconductor memory device includes address input means for receiving addresses applied from an external arithmetic processing unit; address generating means responsive to a burst mode designation from the external arithmetic processing unit for generating addresses in synchronization with external clock signals; address selecting means for selectively passing an output from address input means or an output from address generating means; and memory cell selecting means for selecting a corresponding memory cell from the memory cell array in accordance with the output from the address selecting means. The address selecting means selectively passes the output from the address generating means in response to the burst mode designation.

In accordance with the eighth aspect of the present invention, the memory device includes internal clock generating means responsive to an external clock signal for generating an internal clock signal, and setting means for setting the internal clock generating means to operation inhibited state in response to a standby state designating signal. The externally applied signal is taken in response to the internal clock signal generated from the internal clock generating means.

In accordance with a ninth aspect of the present invention, the semiconductor device includes, in addition to those provided in the eighth aspect, refreshing means responsive to the inhibition of the internal clock generation by the setting means for refreshing dynamic memory cells.

A semiconductor memory device in accordance with a tenth aspect of the present invention includes a memory cell array having a plurality of memory cells arranged in rows and columns, and internal address generating means receiving an external address signal for generating an internal address signal. The external address signal includes an external row address signal for designating a row of the memory cell array, and an external column address signal for designating a column of the memory cell array. The internal address generating means generates internal row address signal and internal column address signal corresponding to the external row address signal and the external column address signal, respectively.

The internal address generating means of the semiconductor memory device in accordance with the tenth aspect of the present invention includes first address generating means which takes one of the above mentioned external row address signal and the external column address signal at a

first timing of an externally applied clock signal for generating a first internal address signal corresponding to the taken external address signal, and second address generating means which takes the other one of the external row address signal and the external column address signal at a second timing of the externally applied clock signal for generating a second internal address corresponding to the taken external address signal.

The first timing is determined by one of the rise and fall of the externally applied clock signal, and the second timing is determined by the other one of the rise and fall of the externally applied clock signal.

The semiconductor memory device in accordance with an eleventh aspect of the present invention includes a memory cell array including a plurality of memory cells, and address generating means receiving externally applied external address signal for generating an internal address signal corresponding to the received external address signal. The external address signal designates a memory cell in the memory cell array.

The semiconductor memory device in accordance with the eleventh aspect of the present invention further includes setting means responsive to an externally applied timing designating signal for taking an address for setting the timing for the address generating means to take the externally applied address signal.

The address generating means takes the applied external address signal in accordance with the timing set by the setting means and generates the internal address signal.

The semiconductor memory device in accordance with the twelfth aspect of the present invention includes a DRAM array including a plurality of dynamic memory cells arranged in rows and columns, an SRAM array including a plurality of static memory cells arranged in a matrix of rows and columns, and data transferring means provided between the DRAM array and the SRAM array for transferring data between a selected memory cell of the DRAM array and a selected memory cell in the SRAM array.

Each row of the matrix of the SRAM array includes memory cells divided into n groups. The SRAM array further includes a plurality of word lines each connected to memory cells of different group, n word lines being arranged for each row in parallel to the row direction of the matrix.

A semiconductor memory device in accordance with a thirteenth aspect of the invention includes a high speed memory array having a plurality of static type memory cells, a large storage capacity memory array having a plurality of memory cells, and data transfer means for transferring data between a selected static type memory cell and a selected dynamic type memory cell.

The semiconductor memory device of the thirteenth aspect further includes a data transfer bus for coupling the selected memory cell of the large storage capacity memory array with the data transfer means, clamping means for clamping the potential on the data transfer bus, and control means responsive to an indication of data transfer from the high speed memory array to the large storage capacity memory array for inhibiting a clamping operation of the clamping means.

A semiconductor memory device in accordance with a fourteenth aspect of the invention includes a high speed memory array having a plurality of static type memory cells arranged in rows and columns, a large storage capacity memory array having a plurality of dynamic type memory cells, and data transfer means for transfer data between a selected static type and a selected dynamic type memory cell.

The semiconductor memory device in accordance with the fourteenth aspect further includes clamping means provided for each column of the high speed memory array for clamping the potential of an associated column, and control means responsive to an indication of data transfer from the large storage capacity memory array to the high speed memory array for inhibiting a clamping operation by the clamping means.

According to the first aspect of the present invention, setting of the self refresh mode or the auto refresh mode is done by refresh mode setting means and one terminal is switched by the input/output switching means to be a refresh designating input terminal in the auto refresh mode, and the self refresh execution designating output terminal in the self refresh mode. Therefore, even in the self refresh mode, refresh timing can be known from the outside of the memory device, and self refresh mode can be utilized even in the normal mode.

In accordance with the second aspect of the present invention, since the row and column designating input terminals of the first and second memory cell array are provided separately for inputting the row address signals and the column address signals, the row address signals and the column address signals to the first and second memory cell arrays can be applied in the non-multiplexed manner. Part of the address signals to the first memory cell array and address signals to the second memory cell array is applied to the same input terminal. Therefore, address non-multiplex method can be realized without increasing the number of input terminals.

According to the third aspect of the present invention, the first and second address means generate internal address signals by simultaneously taking address signals in synchronization with the external clock signal, and therefore the clock synchronized type semiconductor memory device can be operated at high speed employing address non-multiplex method.

According to the fourth aspect of the present invention, data transfer means is activated at an earlier timing than the activation of the sense amplifier in the DRAM array, and therefore data can be transferred from the DRAM array to the SRAM array at high speed.

According to the fifth aspect of the present invention, an output from a current mirror type amplifier is transmitted through the data transfer means, and therefore the data transfer means can be activated without waiting for the activation of the latch type sense amplifier, which enables high speed data transfer from the DRAM array to the SRAM array.

According to the sixth aspect of the present invention, an internal counter is activated in response to a burst mode designation from an external arithmetic processing unit, an output from the address counter is selected by a multiplexer to be utilized as an address signal, and the multiplexer selects external address signals in a mode other than the burst mode. Therefore, a semiconductor memory device which can be easily connected to an external arithmetic processing unit having burst mode function can be provided.

According to the seventh aspect of the present invention, a counter as a built-in address generator effects counting operation in synchronization with the external clock signal, the output from the counter is used as an address in the burst mode, and external address signals are taken and utilized in synchronization with an external clock signal in operation modes other than the burst mode, therefore, a clock synchronized type semiconductor memory device which can be

easily connected to an external operational processing unit having burst mode function can be realized.

According to the eighth aspect of the present invention, when generation of the internal clock signal is stopped at the standby state of the clock synchronized type semiconductor memory device, operations of external signal input buffer and the like are stopped, so that power consumption in the standby state can be reduced.

According to the ninth aspect of the present invention, self refresh mode is activated when generation of the internal clock signal is stopped in the invention in accordance with the eighth aspect, and therefore data of the DRAM array can be surely retained in the standby state.

According to the tenth aspect of the present invention, since the external row address signals and the external column address signals are taken at timings determined by the rise and fall of the external clock signals, the external row address signal and the external column address signal can be taken by a single pulse of the external clock signal. Therefore, compared with a structure in which the external row address signal and the external column address signal are taken time divisionally at timings determined by the rise of the external clock signal, the external row address signal and the external column address signal can be taken sooner. Generally, operation of a clock synchronized type semiconductor memory device starts after the external address signals are taken. Therefore, the semiconductor memory device can be operated at higher speed.

According to the eleventh aspect of the present invention, the timing for taking the external address signals is determined by timing information set by setting means. Therefore, time required for taking the external address signals can be set to an optimal value dependent on the period of the external clock signals, and therefore higher speed of operation and lower power consumption can be flexibly realized.

In the SRAM array according to the twelfth aspect memory cells arranged in one row is divided into a plurality of groups. Memory cells of each group is connected to a word line provided corresponding to each group. Therefore, memory cells of one row of the SRAM array are connected to a plurality of word lines. By adjusting the number n of the groups of the memory cells of one row, an SRAM array having an arbitrary shape can be provided without changing the number of memory cells connected to one word line.

In the semiconductor memory device according to the thirteenth and fourteenth aspects, the control means is operable to inhibit the clamping operation of the clamping means provided at the data receiving side. Consequently, a current flow is prevented from flowing into the data transfer means from the clamping means, resulting in reduced current consumption.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

This application includes a large number of the drawing figures, and we first classify the figures according to the embodiments for the reader's convenience.

FIGS. 1 through 6 are related to a conventional memory device.

FIGS. 7 through 31 represent an array arrangement of CDRAM of the present invention.

FIGS. 32 represents an overall view of a functional construction of the CDRAM.

FIGS. 33 through 43B represent data outputting operation of the CDRAM.

FIGS. 44 through 60D represents data transfer between DRAM array and SRAM array.

FIGS. 61 through 70 represent modified data transfer arrangement with clamping circuitry.

FIGS. 71 through 75 represent peripheral circuitry of the CDRAM.

FIGS. 76 to 80 represent the usage of CDRAM in a system.

FIGS. 81 through 104B represent specific operation modes of the CDRAM.

FIG. 105 shows an overall construction of another CDRAM according to the present invention.

FIGS. 106 through 118 are related to high speed and low power operation modes.

FIGS. 119 through 161 represent specific operations of another CDRAM.

FIGS. 162 through 175 represent selective usage of the auto-refreshing and self refreshing.

FIGS. 176 through 185 represent common usage of DRAM column address and SRAM row address.

FIGS. 186 through 193 represent separated I/O structure type DRAM array of another CDRAM.

FIGS. 194 through 196 represent modified separated IO array architecture CDRAM for fast data transfer by means of clamping circuitry.

FIGS. 197 through 201 represent burst mode operation in CDRAM's of the present invention.

FIGS. 202 through 214 represent sleep mode operation in CDRAMs of the present invention.

FIG. 215 summarizes the internal operations of another CDRAM.

Now, respective figures are described in the following.

FIG. 1 shows a structure of a memory array in a conventional dynamic semiconductor memory device.

FIG. 2 shows a structure of an array portion in a conventional semiconductor memory device containing a cache.

FIG. 3 shows, as an example, a layout of the cache and the DRAM array in the conventional semiconductor memory device containing a cache.

FIG. 4 shows a structure of a cache when 4 way set associative method is realized by the conventional semiconductor memory device containing a cache.

FIG. 5 is a diagram of signal waveforms showing the operation in the automatic refreshing in the conventional semiconductor memory device.

FIG. 6 is a diagram of signal waveforms showing self refreshing operation in the conventional semiconductor memory device.

FIG. 7 schematically shows a structure of a memory array portion of the semiconductor memory device according to an embodiment of the invention.

FIG. 8 shows detailed structure of the memory array shown in FIG. 7.

FIG. 9 shows another example of the structure of the array arrangement in the semiconductor memory device according to an embodiment of the invention.

FIG. 10 shows array arrangement of a semiconductor memory device containing a 4M bit DRAM and a 16K bit SRAM.

FIG. 11 shows layout of DRAM array signal lines in one memory block of the semiconductor memory device shown in FIG. 10.

FIG. 12 schematically shows structures of a bit line and a word line related to a memory cell of the DRAM shown in FIG. 10.

FIG. 13 schematically shows a structure of a word line in the semiconductor memory device of FIG. 10.

FIG. 14 shows layout of signal lines in the semiconductor memory device shown in FIG. 10.

FIG. 15 shows a structure of an SRAM array of the semiconductor memory device shown in FIG. 5.

FIG. 16 shows a structure of a conventional SRAM cell.

FIG. 17 is a diagram of signal waveforms showing the operation of the SRAM cell shown in FIG. 16.

FIG. 18 shows an example of a shape of a package for a semiconductor memory device containing a cache, and SRAM array and DRAM array arrangements contained therein.

FIG. 19 shows problems of the general SRAM array.

FIG. 20 is a diagram showing problems of the general SRAM array arrangement.

FIG. 21 shows a principle of the SRAM array arrangement of the present invention.

FIG. 22 shows, in comparison, the arrangement of the SRAM array of the present invention and the prior art arrangement.

FIG. 23 shows a pattern layout of the SRAM cell shown in FIG. 21.

FIG. 24 shows an SRAM array structure of the semiconductor memory device containing a cache in accordance with one embodiment of the present invention.

FIG. 25 shows an example of a transfer gate circuit structure shown in FIG. 24.

FIG. 26 shows an example of a specific structure of the selecting circuit shown in FIG. 25.

FIG. 27 shows a structure of the SRAM array arrangement and a structure of a transfer gate circuit employed for that SRAM arrangement.

FIG. 28 shows a specific structure of a transfer path from the SRAM array to the DRAM array of the transfer gate circuit shown in FIG. 27.

FIG. 29 shows a detailed structure of the data transfer path from the DRAM array to the SRAM array of the transfer gate circuit shown in FIG. 27.

FIG. 30 is a diagram of signal waveforms showing the operation of the transfer gate circuit shown in FIGS. 27 to 29.

FIG. 31 shows a pin arrangement and a package for containing the semiconductor memory device shown in FIG. 5.

FIG. 32 shows functionally the whole structure of a semiconductor memory device containing a cache in accordance with one embodiment of the present invention.

FIG. 33 shows manner of connections of the bit lines in the DRAM array and bit lines in the SRAM array with internal data line in the semiconductor memory device shown in FIG. 32.

FIG. 34 shows an example of a structure of a data input/output circuit of the semiconductor memory device shown in FIG. 32.

FIG. 35 shows another example of the data input/output circuit of the semiconductor memory device shown in FIG. 32.

FIG. 36 shows a further example of the data input/output circuit of the semiconductor memory device shown in FIG. 32.

FIG. 37 shows a circuit structure for setting data output mode of the semiconductor memory device shown in FIG. 32.

FIG. 38 shows a structure of an output circuit shown in FIG. 36.

FIG. 39 shows an example of a specific structure of a latch circuit shown in FIG. 37.

FIG. 40 is a block diagram showing a structure of an output control circuit shown in FIG. 36.

FIG. 41 shows timings of operations in latch output mode of the circuit shown in FIG. 37.

FIG. 42 shows timings of operations in register output mode of the circuit shown in FIG. 37.

FIG. 43 shows timing of operations in transparent output mode of the circuit shown in FIG. 37.

FIG. 44 shows an example of a specific structure of a data transfer circuit in the semiconductor memory device shown in FIG. 32.

FIG. 45 is a diagram of signal waveforms showing data transfer operation from the DRAM array to the SRAM array when the transfer gate circuit shown in FIG. 44 is employed.

FIG. 46 is a diagram of signal waveforms showing data transfer operation from the SRAM array to the DRAM array.

FIG. 47 is another diagram of signal waveforms showing data transfer operation from the DRAM array to the SRAM array when the bi-directional data transfer circuit shown in FIG. 44 is employed.

FIGS. 48A through 48F show, as an example, data transfer operation at a cache miss in the semiconductor memory device shown in FIG. 32.

FIG. 49 shows another example of the structure of the bi-directional transfer gate circuit.

FIG. 50 shows specific structure of the circuit shown in FIG. 49.

FIG. 51 shows data transfer operation from the DRAM array to the SRAM array by the circuit shown in FIGS. 49 and 50.

FIGS. 52A through 52D show, as an example, data transfer operation shown in FIG. 51.

FIG. 53 is a diagram of signal waveforms showing data transfer operation from the SRAM array to the DRAM array when the data transfer circuit shown in FIGS. 49 and 50 is employed.

FIG. 54 shows, as an example, data transfer operation shown in FIG. 53.

FIG. 55 is a diagram of signal waveforms showing data transfer operation from the DRAM array to the SRAM array at a cache miss reading, when the transfer gate circuit shown in FIGS. 49 and 50 is employed.

FIGS. 56A through 56F show, as an example, data transfer operation shown in FIG. 55.

FIG. 57 shows another example of the structure of the bi-directional data transfer gate.

FIG. 58 shows detailed structure of the circuit shown in FIG. 57.

FIG. 59 is a diagram of signal waveforms showing data transfer operation from the DRAM array to the SRAM array when the circuit of FIG. 57 is employed.

FIGS. 60A through 60D show, as an example, data transfer operation shown in FIG. 59.

FIG. 61 shows a modified array arrangement of CDRAM with clamping circuitry.

FIG. 62 shows an equivalent arrangement to the arrangement of FIG. 61.

FIG. 63 shows a specific construction of the bidirectional transfer gate of FIG. 62.

FIG. 64 is a waveform diagram showing data transfer from DRAM to SRAM with the transfer gate of FIG. 63.

FIG. 65 is a waveform diagram showing data transfer from SRAM to DRAM with the transfer gate of FIG. 63.

FIG. 66 shows another construction of the bidirectional transfer gate of FIG. 63.

FIG. 67 shows further another construction of the bidirectional transfer gate of FIG. 62.

FIG. 68 is a waveform diagram showing data transfer from DRAM to SRAM with the transfer gate of FIG. 67.

FIG. 69 is a waveform diagram showing data transfer from the latch circuit to DRAM with the transfer gate of FIG. 67.

FIG. 70 shows another construction of the clamping circuit.

FIG. 71 shows an example of the manner of allottance of DRAM addresses and SRAM addresses in the semiconductor memory device shown in FIG. 32.

FIG. 72 shows another structure for allotting DRAM addresses and SRAM addresses in the semiconductor memory device shown in FIG. 32.

FIG. 73 shows a manner of connection between internal data lines and SRAM bit line pairs when addresses are allotted in the manner shown in FIG. 72.

FIG. 74 functionally shows the structure of the transfer gate control circuit shown in FIG. 32.

FIG. 75 shows functional structure of a DRAM driving circuit shown in FIG. 32.

FIG. 76 is a table showing combinations of control signals for effecting various operations realized by the semiconductor memory device shown in FIG. 10.

FIG. 77 shows combinations of command registers of the semiconductor memory device shown in FIG. 32 and control signals for selecting the command registers.

FIG. 78 shows, as an example, a function realized by the command register shown in FIG. 77.

FIG. 79 shows one example of a manner of connection between the semiconductor memory device shown in FIG. 10 and an external CPU.

FIG. 80 shows another example of the manner of connection between the semiconductor memory device containing a cache shown in FIG. 10 and an external CPU.

FIG. 81 shows timings of cache hit writing operation in the semiconductor memory device shown in FIG. 10.

FIG. 82 shows timings showing cache hit reading operation in transparent output mode of the semiconductor memory device shown in FIG. 10.

FIG. 83 shows timings showing cache hit reading operation in latch output mode in the semiconductor memory device shown in FIG. 10.

FIG. 84 shows timings of cache hit reading operation in a register output mode in the semiconductor memory device shown in FIG. 10.

FIG. 85 shows timings for setting a copy back operation in the semiconductor memory device shown in FIG. 5.

FIG. 86 shows timings for setting a block transfer operation in the semiconductor memory device shown in FIG. 10.

FIG. 87 shows timings for setting an array writing operation in the semiconductor memory device shown in FIG. 10.

FIG. 88 shows timings of control signals for setting an array reading operation in the semiconductor memory device shown in FIG. 10.

FIG. 89 shows timings for setting an array active cycle in the semiconductor memory device shown in FIG. 10.

FIG. 90 shows timings of control signals for setting an array active operation accompanying a transparent output mode in the semiconductor memory device shown in FIG. 10.

FIG. 91 shows timings of control signals for setting an array active cycle accompanied with a latched output mode in the semiconductor memory device shown in FIG. 10.

FIG. 92 shows timings of control signals for setting an array active operation accompanied with the registered output mode in the semiconductor memory device shown in FIG. 10.

FIG. 93 shows timings of an array read cycle in the transparent output mode in the semiconductor memory device shown in FIG. 10.

FIG. 94 shows timings of array read cycle accompanied with the latched output mode in the semiconductor memory device shown in FIG. 10.

FIG. 95 shows timings of array read cycle operation in the register output mode in the semiconductor memory device shown in FIG. 10.

FIG. 96 shows timings of control signals for setting the refreshing operation in the semiconductor memory device shown in FIG. 10.

FIG. 97 shows timings of various control signals for simultaneously carrying out the cache hit writing operation and refreshing in the semiconductor memory device shown in FIG. 10.

FIG. 98 shows timings of control signals for setting refreshing operation with cache hit reading in the transparent output mode of the semiconductor memory device shown in FIG. 10.

FIG. 99 shows timings of control signals for setting refreshing operation with cache reading in the latch output mode of the semiconductor memory device shown in FIG. 10.

FIG. 100 shows timings of control signals for setting refreshing accompanied with cache hit reading operation in the registered output mode of the semiconductor memory device shown in FIG. 10.

FIG. 101 shows timings of control signals for setting a command register setting cycle of the semiconductor memory device according to FIG. 10.

FIG. 102 illustrates state transitions showing the operation at a cache miss of the semiconductor memory device shown in FIG. 10.

FIG. 103 illustrates state transitions showing the array access operation in the semiconductor memory device shown in FIG. 10.

FIG. 104 shows state transitions during refreshing operation of the semiconductor memory device shown in FIG. 10.

FIG. 105 functionally shows a structure of a semiconductor memory device in accordance with a second embodiment of the present invention.

FIG. 106 is a diagram of waveforms showing timings for taking DRAM addresses of the semiconductor memory device shown in FIG. 105.

FIG. 107 shows effects provided by an address generating circuit included in the semiconductor memory device shown in FIG. 105.

FIG. 108 shows another effect of the address generating circuit shown in FIG. 105.

FIG. 109 shows a specific structure of the address generating circuit shown in FIG. 105.

FIG. 110 shows a specific structure of a row address strobe signal generating circuit shown in FIG. 109.

FIG. 111 shows a specific structure of a column address strobe signal generating circuit shown in FIG. 109.

FIG. 112 shows a specific structure of a row address latch shown in FIG. 109.

FIG. 113 shows a specific structure of a column address latch shown in FIG. 109.

FIG. 114 shows a structure for setting timings for taking addresses of the circuit shown in FIG. 109.

FIG. 115 illustrates high speed operation of the address generating circuit shown in FIG. 109.

FIG. 116 illustrates an operation at a low power consumption mode of the address generating circuit shown in FIG. 109.

FIG. 117 shows another structure of the column address strobe signal generating circuit shown in FIG. 109.

FIG. 118 is a diagram of signal waveforms showing the operation of the circuit shown in FIG. 117.

FIG. 119 is a table showing operations realized by the semiconductor memory device shown in FIG. 105 and combinations of control signal states for realizing these operations.

FIG. 120 shows manner of data transfer between the SRAM array and the DRAM array of the semiconductor memory device shown in FIG. 105.

FIG. 121 is a diagram of signal waveforms showing an operation at a cache miss of the semiconductor memory device shown in FIG. 105.

FIG. 122 shows timings at a cache hit reading operation of the semiconductor memory device shown FIG. 105.

FIG. 123 is a diagram of waveforms showing a cache hit writing operation at a low power consumption mode of the semiconductor memory device shown in FIG. 105.

FIG. 124 is a diagram of signal waveforms showing a cache hit reading operation at a low power consumption mode of the semiconductor memory device shown in FIG. 105.

FIG. 125 is a diagram of signal waveforms showing a cache miss writing operation at a low power consumption mode of the semiconductor memory device shown in FIG. 105.

FIG. 126 is a diagram of signal waveforms showing a array writing operation at a low power consumption mode of the semiconductor memory device shown in FIG. 105.

FIG. 127 is a diagram of signal waveforms showing an array writing operation accompanied with cache hit reading at a low power consumption mode of the semiconductor memory device shown in FIG. 105.

FIG. 128 is a diagram of signal waveforms showing an array writing operation accompanied with cache hit writing at a low power consumption mode of the semiconductor memory device shown in FIG. 105.

FIG. 129 is a diagram of signal waveforms showing a direct array reading operation at a low power consumption mode of the semiconductor memory device shown in FIG. 105.

FIG. 130 is a diagram of signal waveforms showing a direct array writing operation at a low power consumption mode of the semiconductor memory device shown in FIG. 105.

FIG. 131 is a diagram of signal waveforms showing a refresh array operation at a low power consumption mode of the semiconductor memory device shown in FIG. 105.

FIG. 132 is a diagram of signal waveforms showing a refresh array operation accompanied with cache hit reading at a low power consumption mode of the semiconductor memory device shown in FIG. 105.

FIG. 134 is a diagram of signal waveforms showing a refresh array operation accompanied with cache hit writing at a low power consumption mode of the semiconductor memory device shown in FIG. 105.

FIG. 134 is a diagram of signal waveforms showing a counter check reading operation at a low power consumption mode of the semiconductor memory device shown in FIG. 105.

FIG. 135 is a diagram of signal waveforms showing a counter check writing operation at the low power consumption mode of the semiconductor memory device shown in FIG. 105.

FIG. 136 is a diagram of signal waveforms showing a command register setting operation at the low power consumption mode of the semiconductor memory device shown in FIG. 105.

FIG. 137 shows an example of a specific operation sequence at the low power consumption mode of the semiconductor memory device shown in FIG. 105.

FIG. 138 shows another example of the specific operation sequence at the low power consumption mode of the semiconductor memory device shown in FIG. 105.

FIG. 139 is a diagram of signal waveforms showing a cache hit reading operation in the transparent output mode in high speed operation mode realized by the semiconductor memory device shown in FIG. 105.

FIG. 140 is a diagram of signal waveforms showing the cache hit reading operation in the latched output mode of the high speed operation mode realized by the semiconductor memory device shown in FIG. 105.

FIG. 141 is a diagram of signal waveforms showing a cache hit reading operation in the registered output mode in the high speed operation mode realized by the semiconductor memory device shown in FIG. 105.

FIG. 142 is a diagram of signal waveforms showing the cache hit writing operation in the high speed operation mode realized by the semiconductor memory device shown in FIG. 105.

FIG. 143 is a diagram of signal waveforms showing the cache miss reading operation in the high speed operation mode realized by the semiconductor memory device shown in FIG. 105.

FIG. 144 is a diagram of signal waveforms showing the cache miss reading operation accompanied with the latched output mode in the high speed operation mode realized by the semiconductor memory device shown in FIG. 105.

FIG. 145 is a diagram of signal waveforms showing the cache miss reading operation in the registered output mode in the high speed operation mode realized by the semiconductor memory device shown in FIG. 105.

FIG. 146 is a diagram of signal waveforms showing the cache miss writing operation in the high speed operation mode realized by the semiconductor memory device shown in FIG. 105.

FIG. 147 is a diagram of signal waveforms showing the array writing operation in the high speed operation mode realized by the semiconductor memory device shown in FIG. 105.

FIG. **148** is a diagram of signal waveforms showing the array writing operation accompanied with the cache hit reading in the high speed operation mode realized by the semiconductor memory device shown in FIG. **105**.

FIG. **149** is a diagram of signal waveforms showing the array writing operation accompanied with the cache hit reading in the latched output mode in the high speed operation mode realized by the semiconductor memory device shown in FIG. **105**.

FIG. **150** is a diagram of signal waveforms showing the array writing operation accompanied with the cache hit reading in accordance with the registered output mode in the high speed operation mode realized by the semiconductor memory device shown in FIG. **105**.

FIG. **151** is a diagram of signal waveforms showing the array writing operation accompanied with the cache hit writing in the high speed operation mode in the semiconductor memory device shown in FIG. **105**.

FIG. **152** is a diagram of signal waveforms showing a direct array reading operation in the high speed operation mode realized by the semiconductor memory device shown in FIG. **105**.

FIG. **153** is a diagram of signal waveforms showing a direct array writing operation in the high speed operation mode realized by the semiconductor memory device shown in FIG. **105**.

FIG. **154** is a diagram of signal waveforms showing the refresh array operation in the high speed operation mode realized by the semiconductor memory device shown in FIG. **105**.

FIG. **155** is a diagram of signal waveforms showing the refreshing operation accompanied with cache hit reading in the high speed operation mode realized by the semiconductor memory device shown in FIG. **105**.

FIG. **156** is a diagram of signal waveforms showing the refresh array operation accompanied with cache hit writing in the high speed operation mode realized by the semiconductor memory device shown in FIG. **105**.

FIG. **157** is a diagram of signal waveforms showing the counter check operation in the high speed operation mode realized by the semiconductor memory device shown in FIG. **105**.

FIG. **158** is a diagram of signal waveforms showing the counter check writing operation in the high speed operation mode realized by the semiconductor memory device shown in FIG. **105**.

FIG. **159** is a diagram of signal waveforms showing the command register setting operation in the high speed operation mode realized by the semiconductor memory device shown in FIG. **105**.

FIG. **160** is a diagram of signal waveforms showing an example of an operation sequence-carried out in the high speed operation mode by the semiconductor memory device shown in FIG. **105**.

FIG. **161** shows another example of the operation sequence realized in the high speed operation mode by the semiconductor memory device shown in FIG. **105**.

FIG. **162** shows a structure which can selectively effect self refreshing and auto-refreshing in the semiconductor memory device shown in FIG. **32** or FIG. **105**.

FIG. **163** is a block diagram showing a specific structure of the clock generator shown in FIG. **162**.

FIG. **164** shows an example of a specific structure of the input/output switching circuit and a command register shown in FIG. **162**.

FIG. **165** is a diagram of signal waveforms showing the operation of the circuit shown in FIG. **162**.

FIG. **166** shows another example of the structure of the circuit shown in FIG. **162**.

FIG. **167** illustrates battery backup mode.

FIG. **168** is a block diagram showing a specific structure of a BBU control shown in FIG. **166**.

FIG. **169** shows a structure of the clock generator shown in FIG. **166** when the battery backup mode is employed.

FIG. **170** is a diagram of signal waveforms showing the operation of the circuit shown in FIG. **169**.

FIG. **171** shows an example of a specific structure of a RASS generating circuit shown in FIG. **169**.

FIG. **172** shows a structure when the structure of FIG. **162** is applied to a general DRAM.

FIG. **173** shows an example of a specific structure of the clock generator shown in FIG. **172**.

FIG. **174** shows another example of the structures of the input/output switching circuit and the command register shown in FIG. **162**.

FIG. **175** shows another example of the structures of the input/output switching circuit and the command register shown in FIG. **162**.

FIG. **176** shows another example of the manner of allotting addresses in the semiconductor memory device shown in FIG. **32** or FIG. **105**.

FIG. **177** shows connection between the address buffer circuit and the address decoder in accordance with the array allotting method shown in FIG. **176**.

FIG. **178** shows an example of a specific structure of a determining circuit shown in FIG. **177**.

FIG. **179** shows, as an example, positions of dividing address signal lines in accordance with the address allotting method shown in FIG. **176**.

FIG. **180** shows another example of the structure for realizing the address allotting method shown in FIG. **176**.

FIG. **181** is a diagram of signal waveforms showing the operation of the semiconductor memory device in accordance with the address allotting method shown in FIG. **176**.

FIG. **182** shows timings of operations of the semiconductor memory device in accordance with the address allottance shown in FIG. **176**.

FIG. **183** shows, as an example, an operation of the semiconductor memory device in accordance with the address allotting method shown in FIG. **176**.

FIG. **184** shows, as an example, the manner of connection between an external CPU and the semiconductor memory device shown in FIG. **176**.

FIG. **185** shows, as an example, the manner of connection between an external CPU and the semiconductor memory device in accordance with the address allotting method shown in FIG. **176**.

FIG. **186** shows another example of the structure of the DRAM array.

FIG. **187** is a diagram of signal waveforms showing data transfer operation from the DRAM array to the SRAM array in the memory array and transfer gate structure shown in FIG. **186**.

FIG. **188** is a diagram of signal waveforms showing data transfer operation from the SRAM array to the DRAM array in the structure shown in FIG. **186**.

FIG. **189** shows data transferring portion from the DRAM array to the SRAM array of the transfer gate shown in FIG. **186**.

FIG. **190** shows a circuit structure for transferring data from the SRAM array to the DRAM array of the transfer gate shown in FIG. **186**.

FIG. **191** shows a circuit structure for generating a signal for driving a column selecting line in FIG. **186**.

FIG. **192** shows a circuit structure for generating a block selecting signal shown in FIG. **186**.

FIG. **193** shows, as an example, an array allotting method for effectively driving the array structure shown in FIG. **186**.

FIG. **194** shows a modified separated IO DRAM array arrangement of CDRAM with clamping circuitry.

FIG. **195** is a waveform diagram showing data transfer from DRAM to SRAM in CDRAM of FIG. **194**.

FIG. **196** is a waveform diagram showing data transfer from SRAM (or the latch) to DRAM in CDRAM of FIG. **194**.

FIG. **197** shows a circuit structure for realizing data transfer in the burst mode.

FIG. **198** is a diagram of signal waveforms showing the operation of the circuit shown in FIG. **197**.

FIG. **199** shows an example of a specific structure of the address counter shown in FIG. **197**.

FIG. **200** shows an example of a specific structure of a burst data number storing circuit shown in FIG. **197**.

FIG. **201** shows a structure for driving a common semiconductor memory device in the burst mode.

FIG. **202** shows a specific structure of the address buffer of the semiconductor memory device shown in FIG. **32** or FIG. **105**.

FIG. **203** shows an example of a specific structure of the control clock buffer shown in FIG. **32** or FIG. **105**.

FIG. **204** is a diagram of signal waveforms showing an operation in a sleep mode.

FIG. **205** is a block diagram showing a circuit structure for realizing the sleep mode.

FIG. **206** shows an example of a specific structure of the internal clock generating circuit shown in FIG. **205**.

FIG. **207** shows an example of a specific structure of the sleep control circuit shown in FIG. **205**.

FIG. **208** is a diagram of signal waveforms showing the operation of the circuit shown in FIG. **207**.

FIG. **209** shows a circuit structure for realizing self refreshing in the sleep mode.

FIG. **210** shows a structure of portions related to a refresh requesting signal of the clock generator shown in FIG. **209**.

FIG. **211** is a diagram of signal waveforms showing the operation of the circuit shown in FIG. **209**.

FIG. **212** shows another example of a structure of the sleep control circuit shown in FIG. **205**.

FIG. **213** is a diagram of signal waveforms showing the operation of the circuit shown in FIG. **212**.

FIG. **214** shows, as an example, required conditions of the control signals E# and CI# for surely setting the sleep mode.

FIG. **215** is a table showing operations realized by the semiconductor memory device shown in FIG. **105** in combination with the states of control signals.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Array arrangement of DRAM and SRAM arrays in CDRAM are described with reference to FIGS. **7** through **23**. In the arrangement, DRAM array includes a plurality of blocks to implement partial activation type operation. DRAM array includes local IO lines provided for respective blocks, and global IO lines each provided for blocks arranged in a row direction. SRAM array includes a plurality of SRAM cells arranged in a matrix. Data transfer of a plurality of bits between DRAM array and SRAM array is made through bidirectional transfer gate circuit and global IO lines. DRAM address and SRAM address can be set independently of each other. This arrangement allows first data transfer in any mapping scheme between DRAM array and SRAM array, as the blocks arranged in a column direction are simultaneously activated to communicate data with corresponding global IO lines through local IO lines. Now, detailed explanation will be made on specific DRAM and SRAM array arrangements.

[Array Arrangement 1]

FIG. **7** schematically shows a structure of a memory array portion of the semiconductor memory device in accordance with one embodiment of the present invention. Referring to FIG. **7**, the semiconductor memory device comprises a DRAM array **1** including dynamic memory cells arranged in a matrix of rows and columns, a SRAM array **2** including static memory cells arranged in a matrix of rows and columns, and a bi-directional transfer gate circuit **3** for transferring data between DRAM array **1** and SRAM array **2**.

DRAM array **1** includes, assuming that it has storage capacity of 1 M bit, 1024 word lines WL and 1024 pairs of bit lines BL and/BL. In FIG. **7**, the DRAM bit line pair is denoted by DBL. DRAM array **1** is divided into a plurality of blocks along the row and column directions. In FIG. **7**, DRAM array **1** is divided into 8 blocks MBi**1** to MBi**8** (i=1 to 4) along the column direction and divided into 4 blocks MB**1**j to MB**4**j (j=1 to 8) along the row direction, namely, it is divided into a total of 32 memory blocks as an example.

8 blocks Mbi**1** to Mbi**8** divided in the column direction constitute a row block **11**. 4 blocks MB**1**j MB**4**j divided in the row direction constitute a column block **12**. The memory blocks Mbi**1** to Mbi**8** included in one row block **11** share the same word line WL. The memory blocks MB**1**j to MB**4**j included in the same column block **12** shares a column selecting line CSL. A sense amplifier +IO block **13** is provided for each of the memory blocks MB**11** to MB**18**. The structure of sense amplifier +IO block **13** will be described later. Column selecting line CSL simultaneously selects two columns (two pairs of bit lines).

The semiconductor memory device further comprises a row decoder **14** responsive to an address for selecting a corresponding one row from DRAM array **1**, and a column decoder **15** responsive to an applied column address for selecting one column selecting line CSL. Column blocks **12** are connected to the bi-directional transfer gate circuit **13** through two pairs of I/O lines **16**a and **16**b which are independent and separate from each other.

SRAM array **2** includes **16** pairs of bit lines SBL which are connected to **16** pairs of I/O lines through the bi-directional transfer gates circuit **3**, respectively. If SRAM array **2** has the capacity of 4K bit, it includes 16 pairs of bit lines and 256 word lines. Namely, in SRAM array **2**, one row is comprised of 16 bits. SRAM array **2** is associated with a SRAM row decoder **21** for decoding a row address applied to the SRAM for selecting one row of SRAM array **2**, a SRAM column decoder **22** for decoding an applied column address and for selecting a corresponding column in SRAM array **2**, and a sense amplifier circuit **23** for amplifying and outputting data of the memory cell selected by SRAM row decoder **21** and SRAM column decoder **22** in data reading.

The SRAM bit line pair SBL selected by SRAM column decoder **22** is connected to a common data bus, and input/output of data with the outside of the device is effected through an input/output buffer (not shown). Addresses applied to DRAM row decoder **14** and DRAM column decoder **15** are independent of addresses applied to SRAM row decoder **21** and SRAM column decoder **22**, and are applied to mutually different address pin terminals from those for SRAM addresses. Data transfer operation of the semiconductor memory device shown in FIG. **7** will be briefly described.

The operation of the DRAM portion will be described. First, in accordance with an externally applied row address, row decoder **14** carries out a row selecting operation and raises potential of one word line DWL to "H". Data are read to corresponding 1024 bit lines BT (or/BL) from memory cells connected to the selected one word line DWL.

Then, sense amplifiers (included in the block **13**) of row block **11** including the selected word line DWL are activated at one time, and differentially amplify potential difference between each bit line pair. Only one of the four row blocks **11** is activated to reduce power consumption associated with charging/discharging of the bit lines during the sensing operation. (This operation, in which only the row block including the selected row is activated, is called partial activation method.)

In accordance with an externally applied column address, DRAM column decoder **15** carries out a column selecting operation and one column selecting line CSL is set to the selected state in each column block **12**. The column selecting line CSL selects two pairs of bit lines, and the two pairs of bit lines are connected to two pairs of I/O lines **16***a* and **16***b* provided corresponding to the block. Consequently, a plurality of bits (16 bits in this embodiment) of data are read to the plurality of I/O line pairs **16***a* and **16***b* from DRAM array **1**.

Operation of the SRAM portion will be described. In accordance with an externally applied row address, SRAM row decoder **21** carries out row selecting operation and selects one word line from SRAM array **2**. As described above, 16 bits of memory cells are connected to one SRAM word line. Therefore, by the selection of one word line, 16 static memory cells (SRAM cells) are connected to 16 pairs of bit lines SBL.

After 16 bit data have been transmitted to I/O line pairs **16***a* and **16***b* for DRAM array **1**, bi-directional transfer gate circuit **3** is turned ON, and 16 pairs of I/O lines **16***a* and **16***b* are connected to 16 pairs of bit lines SBL of the SRAM. Consequently, data which have been transmitted to **16** pairs of I/O lines **16***a* and **16***b* are written to the 16 bits of memory cells which have been selected in SRAM array **2**.

A sense amplifier circuit **23** and column decoder **22** provided in the SRAM are used to transfer data between the memory cells in SRAM array **2** and an input/output buffer for inputting/outputting external data.

It is possible to set addresses for selecting SRAM cells in SRAM array **2** completely independent from addresses for selecting dynamic memory cells (DRAM cells) in DRAM array **1**. Therefore, it is possible for the 16 bits of memory cells selected in DRAM array **1** to exchange data with memory cells at an arbitrary position (row) of SRAM array **2**. Therefore, all of the direct mapping method, set associative method and full associative method can be realized without changing the structure, or the array arrangement.

The principle of simultaneous transfer of 16 bits of data from the DRAM to the SRAM has been described. Simultaneous transfer of 16 bits of data from SRAM array **2** to DRAM array **1** is carried out in the same manner, except that the direction of data flow through the bi-directional transfer gate circuit **3** is reversed. The structure and operation of the semiconductor memory device containing a cache in accordance with the present invention will be described in detail.

FIG. **8** shows a specific structure of a main portion of the semiconductor memory device shown in FIG. **7**. FIG. **8** shows, as a representative, a portion related to data transfer of one memory block MBij of DRAM array. Referring to FIG. **8**, DRAM memory block MBij includes a plurality of DRAM cells DMCs arranged in rows and columns. DRAM cell DMC includes one transistor **Q0** and one capacitor **C0**. A constant potential Vgg is applied to one electrode (cell plate) of memory capacitor **C0**.

The memory block MBij further includes DRAM word lines DWL to each of which one row of DRAM cells DMCs are connected, and DRAM bit line pairs DBL to each of which a column of DRAM cells DMCs are connected. The DRAM bit line pair DBL includes two bit lines BL and/BL. Signals complementary to each other are transmitted to bit lines BL and/BL. A DRAM cell DMC is arranged at a crossing of a DRAM word line DWL and a DRAM bit line pair DBL.

A DRAM sense amplifier DSA for detecting and amplifying potential difference on a corresponding bit line pair is provided for each of the DRAM bit line pairs DBL. Operation of DRAM sense amplifier DSA is controlled by a sense amplifier activating circuit SAK which generates sense amplifier driving signals ϕSAN and/ϕSAP in response to sense amplifier activating signals ϕSANE and/ϕSAPE. DRAM sense amplifier DSA includes a first sense amplifier portion having p channel MOS transistors cross coupled for raising a bit line potential which is higher in a bit line pair to operational supply potential Vcc level in response to the signal /ϕSAP, and a second sense amplifier portion having n channel MOS transistors cross coupled for discharging potential of a bit line in the pair which is at lower potential to, for example, the potential Vss of the ground potential level, in response to the signal ϕSAN.

The sense amplifier activating circuit SAK includes a sense amplifier activating transistor TR1 which is turned on in response to sense amplifier activating signal/ϕSAPE for activating the first sense amplifier portion of DRAM sense amplifier DSA, and a sense amplifier activating transistor **TR2** which is turned on in response to sense amplifier activating signal ϕSANE for activating the second sense amplifier portion of DRAM sense amplifier DSA. Transistor TR1 is formed by a P channel MOS transistor, while the transistor **TR2** is formed by an n channel MOS transistor. When turned on, transistor **TR1** transmits a driving signal/ϕSAP of the operational supply potential Vcc level to one supply node of each sense amplifier DSA. When turned on, transistor TR2 transmits a signal ϕSAN of the potential Vss level to the other supply node of DRAM sense amplifier DSA.

Between a signal line/ϕSAP and the signal line ϕSAN to which signals /ϕSAP and ϕSAN are output from sense amplifier activating circuit SAK, an equalize transistor TEQ is provided for equalizing both signal lines in response to an equalize designating signal ϕEQ. Therefore, in the standby state, sense amplifier driving signal lines /ϕSAP and ϕSAN are precharged to an intermediate potential of (Vcc+Vss)/2. Signal lines and signals transmitted thereto are represented by the same reference characters.

For each of the DRAM bit line pairs DBL, a precharge/equalize circuit PE which is activated in response to a precharge equalize signal ϕEQ for precharging and equal-

izing bit lines of the corresponding bit line pair to a predetermined precharge potential Vb1 is provided.

DRAM memory block MBij further comprises a column selecting gate CSG provided for each of the DRAM bit line pairs DBL and turned on in response to a signal potential on column selecting line CSL for connecting the corresponding DRAM bit line pair DBL to a local I/O line pair LIO. A column selecting line CSL is commonly provided for two pairs of DRAM bit lines, and therefore, two DRAM bit line pairs DBL are selected simultaneously. In order to receive data from the simultaneously selected two pairs of DRAM bit lines, two pairs of local I/O lines, that is, LIOa and LIOb are provided.

Memory block MBij further comprises IO gates IOGa and IOGb responsive to a block activating signal ϕBA for connecting the local I/O line pairs LIOa and LIOb to global I/O line pairs GIOa and GIOb, respectively. Column selecting line CSL extends in the row direction over one column block shown in FIG. 7, and global I/O line pair GIOa and GIOb also extend in the row direction over one column block. Local I/O line pair LIOa and LIOb extend only in the column direction in one memory block.

I/O lines 16*a* and 16*b* in FIG. 7 correspond to local I/O line pair LIOa and LIOb, IO gates IOGa and IOGb, and global I/O line pairs GIOa and GIOb, respectively.

SRAM comprises SRAM word lines SWL to each of which one row of SRAM cells SMCs are connected, SRAM bit line pairs SBL to each of which a column of SRAM cells SMCs are connected, and SRAM sense amplifiers SSA provided corresponding to the SRAM bit line pairs SBL for detecting and amplifying potential difference between the corresponding bit line pair.

Bi-directional transfer gate circuit 3 comprises bi-directional transfer gates BTGa and BTGb provided between SRAM bit line pair SBL and global I/O line pair GIO. Both of bi-directional transfer gates BTGa and BTGb transfer data between SRAM bit line pair S3L and global I/O line pairs GIOa and GIOb in response to data transfer designating signals ϕTSD and ϕTDS. Data transfer designating signal ϕTSD designates data transfer from SRAM portion to DRAM portion, while data transfer designating signal ϕTDS designates data transfer from DRAM portion to SRAM portion.

[Array Arrangement 2]

FIG. 9 shows another example of the structure of the array arrangement. In the array arrangement of FIG. 9, an SRAM column decoder 22 is provided between DRAM array 1 and SRAM array 2. An input/output buffer 274 is connected to a column selected by SRAM column decoder 22 through an internal data line 251. In the structure shown in FIG. 9, the column selected by DRAM array 1 is connected to internal data line 251 through the bi-directional transfer gate. The connection between DRAM array 1 and internal data line 251 through bi-directional transfer gate circuit 3 may be effected by the column selecting gate provided in the bi-directional transfer gate by a column selecting signal from column decoder 15 of the DRAM. The connection between DRAM array 1 and internal data line 251 and connection between SRAM array 2 and internal data line 251 will be described in detail later.

An address buffer 252 takes an address signal Aa applied externally in response to a chip enable signal E and generates an internal row•column address signal int-Aa for designating a row•column of DRAM array 1. Address buffer 252 takes an externally applied address signal Ac in response to chip enable signal E and generates an internal row•column address signal int-Ac for designating a row and a column of SRAM array 2. External address signal Aa for DRAM array and address signal Ac for SRAM array are applied to address buffer 252 through separate terminals.

In this structure shown in FIG. 9, internal address int-Ac applied to the row decoder 21 and column decoder 22 of SRAM and internal address int-Aa applied to row decoder 14 and column decoder 15 of DRAM are applied through independent paths. Therefore, by this structure, addresses of memory cells in SRAM array 2 and DRAM array 1 can be independently designated.

In the structure shown in FIG. 9, a SRAM column decoder 22 is provided between bi-directional transfer gate circuit 3 and SRAM array 2. SRAM column decoder 22 may be provided between bi-directional transfer gate circuit 3 and DRAM array 1. Alternatively, a corresponding I/O line pair of DRAM array may be selected from I/O line pairs 16*a*, 16*b* of DRAM array 1 by an output from DRAM column decoder 15 to connect the same to internal common data bus 251, and SRAM bit line pair SBL may be connected to internal data transmitting line 251 by SRAM column decoder 22.

[Array Arrangement 3]

FIG. 10 shows a layout of an array in a semiconductor memory device in accordance with another embodiment of the present invention. A CDRAM shown in FIG. 10 includes a 4M bit DRAM array and a 16K bit SRAM array. More specifically, the CDRAM of FIG. 10 includes 4 CDRAMs shown in FIG. 7 or 9. Referring to FIG. 10, the CDRAM includes four memory mats MM1, MM2, MM3 and MM4 each having the storage capacity of 1M bit. Each of the DRAM memory mats MM1 to MM4 includes a memory cell arrangement of 1024 rows (word lines) by 512 columns (bit line pairs). Each of the DRAM memory mats MM1 to MM4 is divided into 32 memory blocks MBs each having a structure of 128 columns (bit line pairs)×256 rows (word lines).

One memory mat MM is divided into 4 memory blocks in the row direction, and into 8 blocks in the column direction. As shown in FIG. 10, a 1M bit memory mat is divided into 8 blocks in the column direction and 4 blocks in the row direction, different from the arrangement of the DRAM of FIG. 7, in order to house the device in a rectangular package, as will be described later.

Sense amplifiers DSA for DRAMs and column selecting gates CSG are arranged corresponding to respective bit line pairs DBL at the central portion in the column direction of the respective memory blocks MB. A memory block MB is divided into an upper memory block UMB and a lower memory block LMB with the sense amplifier DSA and column selecting gate CSG positioned at the center. In operation, either the upper memory block UMB or the lower memory block LMB is connected to the sense amplifier DSA and to the column selecting gate CSG. Whether the upper memory block UMB or lower memory block LMB is to be connected to sense amplifier DSA and column selecting gate CSG is determined by an address. Such a structure in which one memory block MB is divided into upper and lower two memory blocks UMB and LMB and one of the two blocks is connected to sense amplifier DSA and to column selecting gate CSG is commonly used in DRAM s having shared sense amplifier structure having the storage capacity equal to or larger than 4M bit.

One memory mat MM includes two activation sections AS. One word line is selected in one activation section. Different from the structure shown in FIG. 7, one word line is divided into two portions and allotted to respective activation sections in the structure of FIG. 10. Namely, selection of one word line in one memory mat MM is equivalent to selection of one word line in each activation section AS.

The semiconductor device (CDRAM) further comprises 4 DRAM row decoders DRD1, DRD2, DRD3 and DRD4 for selecting one word line from each of four DRAM memory mats MM1 to MM4. Therefore, in the CDRAM shown in FIG. 10, 4 word lines are selected at one time. DRAM row decoder DRD1 selects one row from corresponding activation sections AS of the memory mats MM1 and MM2. DRAM row decoder DRD2 selects one row from lower activation sections AS of memory mats MM1 and MM2. DRAM row decoders DRD3 and DRD4 select one row from upper activation sections AS of DRAM memory mats MM3 and MM4 and from lower activation sections AS of this memory mat, respectively.

The CDRAM further comprises DRAM column decoders DCD for selecting two columns (bit line pairs) from each of the column blocks of memory mats MM1 to MM4 of the DRAM. Column selection signal from the DARM column decoder DCD is transmitted to a column selection line CSL shown in FIG. 8. A column selection line CSL extends to be shared by the upper and lower activation sections AS. Therefore, in the structure shown in FIG. 10, 4 columns are selected from one column block (in FIG. 10, a block including 8 memory blocks MBs divided in the column direction), by the column selection signal from DRAM column decoder DCD.

Columns selected by column decoder DCD are connected to corresponding global I/O line pairs GIO. Two pairs of global I/O lines GIO extend in the column direction in each column block in one activation section. Connection between the global I/O line pair GIO and local I/O line pair LIO in each column block will be described in detail later.

CDRAM shown in FIG. 10 further includes SRAM array blocks SMA1 to SMA4 each formed of SRAM cells having the capacity of 4K bit. Row decoders SRD1 and SRD2 for SRAM are provided at a middle portion between 2 SRAM array blocks to be shared by two SRAM array blocks. SRAM row decoder SRD1 is commonly used by SRAM array blocks SMA1 and SMA3. SRAM row decoder SRD2 is commonly used by SRAM array blocks SMA2 and SMA4. Details of the structure of SRAM array block SMA will be descrbed in detail later.

The CDRAM includes 4 input/output buffer circuits IOB1, IOB2, IOB3 and IOB4 for carrying out input/output of data 4 bits by 4 bits. Input/output buffer circuits IOB1 to IOB4 are connected to blocks SCDA of sense amplifiers and column decoders for SRAM, through common data buses (internal data buses), respectively. In the structure shown in FIG. 10, input/output of data are shown to be carried out through the sense amplifier and column decoder block SCDA for the SRAM. However, input/output of data may be carried out through the portion of bi-directional transfer gates BTG.

In operation, one word line is selected in each activation section AS. Only the row block including the selected word line is activated. Other row blocks are maintained at the precharge state. In the selected row block, only a small block UMB (or LMB) including the selected word line is connected to the sense amplifier DSA and column selecting gate CSG for DRAM, and the other small memory block LMB (or UMB) in the selected block is separated from sense amplifier DSA and column selecting gate CSG for DRAM. Therefore, as a whole, activation (charge/discharge) of 1/8 of bit lines is effected. By this partial activation, power consumption in charging/discharging of the bit lines can be reduced. In addition, by dividing one memory block MB into an upper memory block UMB and a lower memory block LMB and by arranging a sense amplifier DSA at the center therebetween, the bit line can be made shorter, the ratio Cb/Cs of bit line capacitance Cb to memory capacitor capacitance Cs can be reduced, and sufficient reading voltage can be obtained at high speed.

In each activation section AS, sensing operation in 4 small blocks UMB (or LMB) in the row direction is carried out. In each activation section AS, two pairs of bit lines are selected in one column block by a column selection signal from DRAM column decoder DCD. Global I/O line pair GIO extends in the column direction to be shared by column blocks in each activation section AS. Two pairs of bit lines are selected from each column block in each activation section AS and connected to corresponding two pairs of global I/O lines GIO. 4 pairs of global I/O lines GIO are connected to one bi-directional transfer gate BTG. 4 bi-directional transfer gates BTG are provided for one memory mat MM. Therefore, 16 pairs of global I/O lines GIO can be connected to SRAM bit line pairs SBL of the corresponding SRAM array from one memory mat MM. Layout of the global I/O lines will be described.

FIG. 11 shows arrangement of global I/O lines for one memory mat. Referring to FIG. 11, the global I/O line pair GIC includes an upper global I/O line pair UGIO provided for an upper activation section UAS and a lower global I/O line pair LGIO provided for a lower activation section LAS. The upper global I/O line pair UGIO and the lower global I/O line pair LGIO are arranged in parallel. Lower global I/O line pair GIO passes through upper activation section UAS but is not connected to local I/O line pair LIO in the upper activation section UAS. Global I/O line pair GIO and local I/O line pair LIO are connected through an IO gate IOG which is a block selecting switch. Only an IO gate IOG provided in the row block including the selected word line is turned on by a block selecting signal ϕBA and connects the corresponding local I/O line pair LIO to the corresponding global I/O line pair GIO.

Since DRAM sense amplifier DSA and column selecting gate CSG are arranged at the central portion in the column direction of the memory block MB, local I/O line pair LIO is arranged along the row direction at the central portion in the column direction of memory block MB.

A word line shunt region WSR is provided in the column direction between adjacent column blocks. A word line shunt region WSR is used to provide a contact between a word line formed of polysilicon having relatively high resistance and an aluminum interconnection having low resistance. The word line shunt region will be described briefly.

FIG. 12 schematically shows a cross sectional structure of a selecting transistor Q0 (see FIG. 11) included in a DRAM cell. Referring to FIG. 12, the selecting transistor Q0 includes impurity regions IPR formed at a surface of a semiconductor substrate SUB, a bit line BL connected to one impurity region IPR, and a polysilicon layer PL formed on the surface of the semiconductor substrate between the two impurity regions IPR. When a word line driving signal DWL (the signal line and the signal transmitted thereon are represented by the same reference character) is transmitted to the polysilicon layer PL, a channel is formed at the surface of the semiconductor substrate between the impurity regions IPR, and the selecting transistor Q0 is turned on. Polysilicon has relatively high resistance. If word line DWL has high resistance, a signal delay is generated due to the resistance of polysilicon. In order to lower the resistance of the word line DWL, an aluminum interconnection AL having low resistance is provided in parallel to the polysilicon layer PL. By periodically connecting the aluminum interconnection

AL and the polysilicon layer PL at predetermined intervals, the resistance of the word line DWL can be reduced. Aluminum interconnection AL is formed above the bit line BL. Therefore, a region for providing contact between polysilicon layer PL and aluminum interconnection AL must be provided at a region where there is no bit line BL (/BL), that is, a region where memory cell is not arranged. For this purpose, a word line shunt region is provided between column blocks. The manner of connection is shown in FIG. 13.

Referring to FIG. 13, aluminum interconnection AL having low resistance is provided in parallel to polysilicon layer PL having relatively high resistance serving as a word line. Word line driving signal DWL is transmitted to aluminum interconnection AL. Aluminum interconnection AL and polysilicon layer PL are periodically connected to each other by a contact layer CNT in word line shunt region WSR. By periodically providing contacts between aluminum interconnection AL and polysilicon layer PL through contact region CNT, the resistance of polysilicon layer PL can be effectively reduced. Therefore, even if a word line is very long, the word line driving signal WL can be transmitted to the terminal end of the word line at high speed.

FIG. 14 schematically shows a layout of global I/O lines and column selecting lines CSL. In FIG. 14, layout of these lines for two memory blocks MB only is shown. In FIG. 14, global I/O line pair GIO is arranged in word line shunt region WSR. DRAM word lines DWL are arranged in a direction orthogonally crossing the global I/O line pair GIO. In FIG. 14, aluminum interconnection AL and polysilicon layer are arranged in parallel to each other, and in this plan view, they are overlapped with each other. Therefore, they are shown as the same word lines DWL. Column selecting lines CSL for transmitting column selection signal from DRAM column decoder are arranged in a direction orthogonally crossing DRAM word lines DWL.

Although the bit line pairs DBL of DRAM are not shown in this layout, the bit line pairs are arranged in parallel to column selecting lines CSL. Aluminum interconnection AL (see FIG. 12) for DRAM word lines DWL is formed by a first layer aluminum interconnection. Column selecting lines CSL are formed by a second layer aluminum interconnection. Global I/O lines are formed by the same aluminum interconnection as the column selecting lines CSL. By providing global I/O line pair GIO in word line shunt region WSR, chip area is not increased even if I/O lines for connecting DRAM array and bi-directional transfer gates are adapted to have hierarchical structure of local I/O lines and global I/O lines.

FIG. 15 schematically shows a structure of SRAM array block SMA shown in FIG. 10. Referring to FIG. 15, a SRAM array block SMA includes 16 pairs of bit lines SBL and 256 SRAM word lines SWL. SRAM cells SMC are arranged at crossings of SRAM bit line pairs SBL and SRAM word lines SWL. As shown in FIG. 10, in order to have the SRAM array block SMA accordant with a rectangular chip layout, SRAM bit line pairs SBL are arranged in the row direction of DRAM array and SRAM word lines SWL are arranged in column direction of DRAM array. SRAM word lines SWL are connected to SRAM row decoder SRD.

SRAM bit line pairs SBL must be connected to global I/O line pair GIO through bi-directional transfer gate BTG. Therefore, SRAM bit line pairs SBL must be connected to bi-directional transfer gate BTG on the lower side as viewed in FIG. 15 (or upper side of FIG. 15: determined by the arrangement of the memory array). For this purpose, in the structure shown in FIG. 15, SRAM bit line taking lines SBLT are arranged in parallel to SRAM word lines SWL.

The number of SRAM bit line taking lines SBLT is the same as the number of bit line pairs SBL of the SRAM array block SMA, and the taking lines are connected to corresponding SRAM bit line pairs SBL. If SRAM bit line taking lines SBLT are formed by the same interconnection layer as SRAM word lines SWL, SRAM bit line taking lines SBLT can be implemented easily without additionally providing interconnection layers formed by additional step of manufacturing.

The SRAM row decoder SRD decodes a row address for SRAM to select one of the 256 SRAM word lines SWL. 16 bits of SRAM cells SMC connected to the selected SRAM word line SWL are connected to corresponding SRAM bit line pair SBL and to SRAM bit line taking line SBLT. In data transfer, the bit line taking lines SBLT are connected to global I/O line pair GIO through bi-directional transfer gate BTG.

By employing such a layout as shown in FIGS. 11 and 15, a structure as shown in FIG. 10 can be realized, in which DRAM arrays are arranged divided into upper and lower portions as viewed in the figure, SRAM arrays are collectively arranged between the upper and lower DRAM array blocks, and input/output buffer circuits IOB1 to IOB4 are provided near SRAM arrays formed at the central portion of the semiconductor memory device (chip). Such structure having SRAM arrays collectively formed at the central portion of the chip and input/output of data are effected near the central portion of the chip is advantageous for CDRAM as will be described in the following.

High speed access to a cache register is the first and most important characteristic of CDRAM. Arrangement of the SRAM array serving as the cache register near the input/output buffer for inputting/outputting data to and from the outside of the device results in shorter signal lines, which enables high speed input/output of data, and thus meets the demand of high speed accessing.

By collectively arranging SRAM arrays at the central portion, address lines for selecting SRAM cells can be made shorter. If an address line is made shorter, interconnection resistance and parasitic resistance of the address line can be reduced, SRAM cells can be selected at high speed, and therefore it is suitable for high speed accessing to the cache register.

In the architecture shown in FIG. 10, interconnections connecting the DRAM array and SRAM array may be longer, lowering the speed of data transfer between the DRAM array and SRAM array. However, data transfer is carried out between DRAM array and SRAM array only when a cache miss (miss hit) occurs. In that case, access speed as low as that of the standard DRAM is sufficient, and it is not very much desired to increase this access speed. Therefore, this is not a problem in practical use. In this case also, writing/reading of data can be carried out at high speed by using the data transfer apparatus which will be described later.

[Another Arrangement of SRAM Array]

In this section, reference is made on FIGS. 16 to 30. SRAM array is arranged to implement any shape with storage capacity fixed. Each row of SRAM array has a plurality of word lines associated therewith. One of word lines is selected. One row corresponds effectively to a plurality of rows. Data transfer between DRAM array and SRAM array of multiplicate word line arrangement be also described.

FIG. 16 shows a structure of the SRAM cell. Referring to FIG. 16, the SRAM cell SMC includes MOS (insulated gate

type) transistors SQ1, SQ2, SQ3 and SQ4 constituting an inverter latch. P channel MOS transistor SQ1 and n channel MOS transistor SQ3 are complementary connected between operational supply potential Vcc and the other supply potential (ground potential), forming one inverter circuit.

P channel MOS transistor SQ2 and n channel MOS transistor SQ4 are complementary connected between the operational supply potential Vcc and the ground potential, forming the other inverter circuit. Transistors SQ1 and SQ3 have their gates connected to an node SN1, and transistors SQ2 and SQ4 have their gates connected to an node SN2. Node SN1 is an output node of one inverter circuit (transistors SQ1 and SQ3), and node SN2 is an output node of the other inverter circuit (transistors SQ2 and SQ4).

SRAM cell SMC further includes n channel MOS transistors SQ5 and SQ6 rendered conductive in response to a signal on SRAM word line SWL for connecting nodes SN1 and SN2 to bit lines SBL and *SBL. Diode connected n channel MOS transistors SQ7 and SQB are provided on bit lines SBL and *SBL. MOS transistors SQ7 and SQ8 clamp the potential of "H" on bit lines SBL and *SBL at a potential Vcc-Vth and "L" thereon at VL1 (described later). The character Vth represents the threshold voltage of the transistors SQ7 and SQ8.

Data writing and reading operations of the SRAM cell will be briefly described.

In data writing, data complementary to each other are transmitted to bit line SBL and complementary bit line *SBL. Assume that a potential at "H" is transmitted to bit line SBL and a potential at "L" is transmitted to complementary bit line *SBL. Potential on word line SWL is at "H" and nodes SN1 and SN2 are connected to bit lines SBL and *SBL through conductive transistors SQ5 and SQ6, respectively. The potential of node SN1 is applied to the gates of transistors SQ2 and SQ4, so that transistor SQ4 is rendered conductive and transistor SQ2 is rendered non-conductive. The potential at "L" on node SN2 is applied to the gates of transistors SQ1 and SQ3, so that transistor SQ1 is rendered conductive, and transistor SQ3 is rendered non-conductive. Consequently, the potential at node SN1 is set to "H", the potential on node SN2 is set to "L" and these potentials are latched by the inverter latch circuits formed of transistors SQ1 to SQ4. By the fall of the potential on SRAM word line SWL to "L", writing of data is completed.

In data reading, the potential of the SRAM word line SWL rises to "H" and transistors SQ5 and SQ6 are rendered conductive. The stored data (potential) which has been latched at nodes SN1 and SN2 are transmitted to bit lines SBL and *SBL, respectively. Complementary data of "H" and "L" are transmitted to bit lines SBL and *SBL. The signal potentials on bit lines SBL and *SBL are amplified by a sense amplifier, not shown, and thus data is read out.

FIG. 17 is a diagram for illustrating the functions of transistors SQ7 and SQ8 shown in FIG. 16. The operation of the transistors SQ7 and SQ8 will be described with reference to FIGS. 16 and 17.

Transistors SQ7 and SQ8 are diode connected, and clamp the potentials on bit lines SBL and *SBL to Vcc-Vth. More specifically, the "H" potential level of the potential amplitude of bit lines SBL and *SBL is set to Vcc-Vth. The data of "H" latched in node SN1 has the potential at Vcc level. When the latched data of "H" is transmitted to bit line SBL, the level of this data Vcc-Vth, because of signal loss by transistor SQ5.

The "L" level potential VL1 of the potential amplitude of bit line SBL (or *SBL) is determined by resistive division of transistors SQ4, SQ6 and SQ8 (or SQ3, SQ5 and SQ7). The potential VL1 of "L" level of the bit line potential amplitude is higher than the ground potential Vss.

Namely, transistors SQ7 and SQ8 have also a function of raising potential of "L" of bit lines SBL and *SBL.

Assume that transistors SQ7 and SQ8 are not provided. In that case, the "L" level potential VL2 of bit lines SBL and *SBL are discharged by transistors SQ6 and SQ4 (or SQ5 and SQ3) to the ground potential Vss to be approximately at the ground potential level. The "H" level potential of bit line SBL (or *SBL) is provided as Vcc-Vth even when transistors SQ7 and SQ8 are not provided. In this case, it is assumed that the "H" level applied to word line SWL is at the level of operational supply voltage Vcc, and that there is a loss of the threshold voltage Vth of transistor SQ5 or SQ6 in transistor SQ5 (or SQ6).

Assume that the potential on SRAM word line SWL rises to "H" at time TWL in FIG. 17. When transistors SQ7 and SQ8 are provided, data stored in SRAM cell SMC is transmitted to bit lines SBL and *SBL, and potentials "H" and "L" on bit lines SBL and *SBL cross at time T1.

When transistors SQ7 and SQ8 are not provided, the potentials "H" and "L" of bit lines SBL and *SBL cross at time T2.

Data on respective bit lines SBL and *SBL are established after the time of crossing of potentials "H" and "L" on bit lines SBL and *SBL. Therefore, by the provision of transistors SQ7 and SQ8, logic amplitude of bit lines SBL and *SBL can be made smaller and the access time can be made shorter.

Different from the DRAM, the SRAM does not need SRA precharge time, and therefore it can be accessed at high speed. However, in SRAM array, one memory cell always exists at a crossing of an SRAM word line and a bit line. One memory cell is connected to bit line SBL and complementary bit line *SBL. A SRAM cell includes 6 transistors as shown in FIG. 16, and therefore compared with a DRAM cell including one transistor and on e capacitor, it occupies larger area. Therefore, to provide a CDRAM which is highly integrated with high density, SRAM array should be effectively arranged in as small an area as possible.

Assume that the CDRAM is to be housed in a rectangular package 550 as shown in FIG. 18. Package 550 has a longer side direction represented by X and a shorter side direction represented by Y in FIG. 18. For packaging in such a rectangular package, a DRAM array 560 having large storage capacity is arranged in a rectangular so as to match with the shape of package (or chip) 550. Here, it should be noted that the chip having DRAM array and CDRAM array integrated thereon has the same shape as the package. Data are transferred bi-directionally through transfer gate 570 between DRAM array 560 and SRAM array 580. In such arrangement, the SRAM array 580 should have the same length as the shorter side length of the DRAM array, in view of effective chip area occupation or array layout.

Assume that DRAM array 560 and SRAM array 580 can transfer data of 16 bits at one time, as shown in FIG. 19 and described previously. In this case, cache size is 16 bit. 16 pairs of SRAM bit lines SBL and *SBL are arranged for one SRAM word line SWL. SRAM array 580 has a structure of 256 rows×16 columns. When 256 SRAM word lines SWL1 to SWL256 are arranged along the longer side of package 550 as shown in FIG. 19, SRAM array 580 becomes long in the long side direction (X direction). If so, it can not be arranged in the area allotted to SRAM array 580 of package 550.

If SRAM word lines SWL1 to SWL256 are arranged in the short side direction (Y direction) of package 550 as

shown in FIG. 20, the length in the long side direction (X direction) in FIG. 18 can be reduced, but it becomes longer in the short side direction (Y direction). Therefore, in this case also, it can not be arranged in the area allotted to SRAM array in package 550.

The size of SRAM array is determined uniquely when the number of bit line pairs and the number of SRAM word lines are determined. Therefore, the shape of SRAM array can not be flexibly changed.

In SRAM array, when a memory cell is selected, current always flows through the selected memory cell. Therefore, in view of current consumption, the number of memory cells connected to one word line should preferably be as small as possible. If the number of word lines are increased to reduce the number of memory cells connected to one word line, the bit line becomes longer. This in turn causes a problem that parasitic capacitance of the bit line is increased and access time is increased.

The shape of the DRAM array can be changed to be suited for the package relatively easily, by employing block divided arrangement, shared sense amplifier structure and the like. Therefore, it is preferred to provide a semiconductor memory device containing a cache occupying small area to realize an SRAM array structure whose shape can be flexibly changed corresponding to the shape of the DRAM array.

The arrangement of the DRAM array and the SRAM array in the rectangular area as described previously is required to house a 4M CDRAM in a rectangular package. The SRAM array SMA is arranged between DRAM arrays MMs as shown in FIG. 10. SRAM array SMA is arranged in a rectangular region which is short in the long side direction (X direction) of the chip and long in the short side direction (Y direction) of the chip.

SRAM array SMA has a storage capacity of 4K bits, and transfers 16 bits of data at one time to and from the corresponding DRAM array MM through a bi-directional transfer gate circuit BTG.

In this embodiment, SRAM array SMA includes 256 word lines and 16 pairs of bit lines. The SRAM array structure for effectively arranging SRAM array in the rectangular area will be described.

FIG. 21 shows in principle the structure of the SRAM array in accordance with an embodiment of the present invention. FIG. 21 shows two SRAM word lines SWL1 and SWL2 and two pairs of bit lines SBL1, *SBL1, SBL2 and *SBL2, as representatives. SRAM cells SMC1 and SMC2 are arranged in one row. SRAM word lines SWL1 and SWL2 are commonly provided for the row in which SMC1 and SMC2 are arranged. Word line SWL1 is connected to memory cell SMC1. Word line SWL2 is connected to memory cell SMC2. SRAM memory cell SMC1 is connected to bit line pair SBL1, *SBL1. Memory cell SMC2 is connected to bit line pair SBL2, *SBL2.

Clamping transistors SQ7, SQ8, SQ15 and SQ16 are provided for clamping "H" and "L" level potential of the bit line potential for bit lines SBL1, *SBL1, SBL2 and *SBL2. Memory cells SMC1 and SMC2 have the same structure as the SRAM cell SMC shown in FIG. 16 and has a structure of a latch type storing element. SRAM cell SMC1 includes p channel MOS transistors SQ1 and SQ2 and n channel MOS transistors SQ3, SQ4, SQ5 and SQ6. Transistors SQ5 and SQ6 are rendered conductive in response to a signal potential on word line SWL1 and connect nodes SN1 and SN2 to bit lines SBL1 and *SBL1, respectively. Transistors SQ1, SQ2, SQ3 and SQ4 constitute an inverter type latch circuit.

SRAM cell SMC2 includes p channel MOS transistors SQ9 and SQ10 and n channel MOS transistors SQ11, SQ12, SQ13 and SQ14. Transistors SQ13 and SQ14 are rendered conductive in response to a signal potential on SRAM word line SWL2, and connect nodes SN3 and SN4 to bit lines SBL2 and *SBL2. Transistor SQ9, SQ10, SQ11 and SQ12 constitute an inverter type latch circuit.

In the array arrangement shown in FIG. 21, memory cells existing on even numbered columns (SMC2 and the like) of memory cells arranged in one row are connected to word line SWL2, while memory cells existing on odd numbered columns (SMC1 and the like) are connected to word line SWL1. The number of memory cells connected to word line SWL1 is the same as the number of memory cells connected to the word line SWL2. In this structure, an SRAM array having an arbitrary shape can be easily realized, as will be made clear later.

FIGS. 22A and 22B shows a comparison between the conventional SRAM array arrangement and the SRAM array arrangement of the present invention. Referring to FIG. 22A, one word line SWL is arranged for one row of memory cells. In this case, memory cells SMCs are arranged in M rows×N columns.

Meanwhile, as shown in FIG. 22B, two word lines SWLa and SWLb are provided for one row of memory cells SMC, and one row of memory cells SMCs are connected alternately to word lines SWLa and SWLb. In this case, memory cells SMCs are arranged in M/2 rows×2N columns. In both array arrangements shown in FIGS. 22A and 22B, N memory cells SMCs are connected to one word line. In the structure of FIG. 22B, when three or more word lines are arranged for one row of memory cells and memory cells are connected alternatively to respective word lines, an SRAM array having an arbitrary shape can be provided. This increases degree of freedom in designing the structure and arrangement of the SRAM array in chip lay out.

FIG. 23 shows a pattern of memory cell arrangement shown in FIG. 21. The structure of the memory cell will be described briefly with reference to FIG. 23. Supply line Vcc, SRAM word lines SWL1 and SW2 and a ground line GND are arranged in parallel and formed by a second layer aluminum interconnection (second aluminum interconnection). Bit lines SBL1, *SBL1, SBL2 and *SBL2 are formed by a first layer aluminum interconnection (first aluminum interconnection). Gates of transistors SQ1 to SQ16 are formed by a first layer polysilicon interconnection (first poly interconnection). The respective transistors are connected by a fourth layer polysilicon interconnection (fourth poly interconnection), and word lines are connected to the gates of the transistors by the first layer aluminum interconnection. Memory cells SMC1 and SMC2 have the same pattern layout. In the following, connection of memory cell SMC1 will be described.

Clamping transistor SQ7 has its drain connected to bit line SBL1 through a contact hole CX1, its gate and source connected to the first layer aluminum interconnection through contact holes CX3 and CX2, and this first aluminum interconnection is connected to supply line Vcc through a contact hole CX6. Transistor SQ8 has its drain connected to bit line *SBL1 formed of the first layer aluminum interconnection through a contact hole CX5, and its gate and source connected to the first layer aluminum interconnection layer through contact holes CX4 and CX2, and this first layer aluminum interconnection layer is connected to supply line Vcc through contact hole Cx6.

Transistor SQ1 has its drain connected to the first layer aluminum interconnection through a contact hole CX8, and this first layer aluminum interconnection is connected to the fourth layer polysilicon interconnection through a contact

hole CX9. This fourth layer polysilicon interconnection connected to contact hole CX9 provides node SN1. Node SN1 is connected to gate electrodes of transistors SQ2 and SQ4 through the fourth layer polysilicon interconnection and contact hole CX11. This fourth layer polysilicon interconnection of node SN1 is connected to the drain of transistor SQ3 and to one conduction terminal of transistor SQ5 through contact hole CX16.

Transistor SQ1 has its gate connected to node SN2 through contact hole CX10 and through the fourth layer polysilicon interconnection. Transistor SQ1 has its source connected to supply line Vcc through contact hole CX7, the first layer aluminum interconnection and contact hole CX6.

Transistor SQ2 has its drain connected to the first layer aluminum interconnection through a contact hole CX23, and this first layer aluminum interconnection is connected to the fourth layer polysilicon interconnection through a contact hole CX22. The fourth layer polysilicon interconnection connected to contact hole CX22 provides node SN2. Transistor SQ1 has its gate connected to the fourth layer polysilicon interconnection providing node SN1, through contact hole CX11.

Transistor SQ3 has its drain connected to the fourth layer polysilicon interconnection through contact hole CX16 and connected to node SN1. Transistor SQ3 has its gate connected to the fourth polysilicon interconnection layer through contact hole CX10 and to node SN2. Transistor SQ3 has its source connected to the first layer aluminum interconnection through contact hole CX18, and the first layer aluminum interconnection is connected to the ground line GND through contact hole CX17.

Transistor SQ4 has its source connected to ground line GND through contact hole CX18, the first layer aluminum interconnection and contact hole CX17. Transistor SQ4 has its gate connected to node SN1 through contact hole CX11 and the fourth layer polysilicon interconnection. Transistor SQ4 has its drain connected to node SN2 through contact hole CX20 and the fourth layer polysilicon interconnection.

Transistor SQ5 has its gate connected to the first layer aluminum interconnection through contact hole CX14, and this first aluminum interconnection is connected to word line SWL1 through contact hole CX12.

Transistor SQ6 has its gate connected to the first layer aluminum interconnection through contact hole CX19, and to word line SWL1 through contract hole SX12. One conduction terminal of transistor SQ6 is connected to bit line SBL1 through contact hole CX21. The other conduction terminal of transistor SQ6 is connected to node SN2 through contact hole CX20 and the fourth layer polysilicon interconnection.

As shown in FIG. 23, memory cells are arranged in one row, two word lines SWL1 and SWL2 can be arranged for the one row, and multiplicate word line arrangement in which a plurality of word lines are provided for memory cells arranged in one row can be easily realized.

FIG. 24 shows an SRAM. array arrangement in accordance with one embodiment of the present invention. The SRAM array arrangement shown in FIG. 24 is applied to the 4K bit SRAM array shown in FIG. 10. Referring to FIG. 24, the SRAM array SMA includes static memory cells (SRAM cells) arranged in 128 rows and 32 columns. Two SRAM word lines SWL are provided for SRAM cells arranged in one row. For example, two SRAM word lines SWL1 and SWL2 are provided for the first row of SRAM cells. SRAM word lines SWL3 and SWL4 are provided for the second row of memory cells.

SRAM cells of the odd numbered columns are connected to odd numbered SRAM word lines (SWL1, SWL3, . . .) while SRAM cells of the even numbered columns are connected to even numbered SRAM word lines (SWL2, SWL4, . . .). Every other SRAM cells of the respective rows of SRAM cells are connected to corresponding SRAM word lines SWL1 to SWL256. Namely, 16 bits of SRAM cells are connected to each of SRAM word lines SWL1 to SWL256.

In accessing SRAM cell, a column should be selected. The arrangement of FIG. 24 includes effectively 16 columns. In column selection, SRAM column address and word line group designating signal (a least significant SRAM row address bit, for example) are combined to generate a SRAM column select signal to connect a selected SRAM column to internal data bus.

As shown in FIG. 10, an SRAM row decoder for selecting the SRAM word lines is arranged in a direction orthogonally crossing the word lines SWL1 to SWL256. Data is transferred between the DRAM array and a SRAM cell through a transfer gate circuit BTG. Data must be transferred through SRAM bit lines SBL and *SBL. Therefore, as in the case of FIG. 15, bit line taking line SBLT is provided for each bit line pair SBL and *SBL. The bit line taking lines SBLT and *SBLT are formed by the second layer aluminum interconnection.

One bi-directional transfer gate circuit BTG is provided for two pairs of bit lines SBL and *SBL, that is, two pairs of SRAM bit line taking lines SBLT and *SBLT. Bi-directional transfer gate circuit BTG is connected to corresponding global I/O lines GIO and *GIO. 16 bits of data are transferred at one time between DRAM array and SRAM array through bi-directional transfer gate 210. In accordance with the structure, one transfer gate circuit can be arranged for two pairs of SRAM bit line taking lines SBLT and *SBLT in the SRAM array. Consequently, pitch condition in the Y direction for transfer gate circuit BTG can be released, and therefore even a transfer gate circuit having a complicated structure can be formed with sufficient margin.

Although memory cells are arranged in 128 rows and 32 columns in the arrangement of SRAM array shown in FIG. 24, the structure is substantially equivalent with the SRAM array of 256 rows×16 columns. In this case, the dimension in Y direction can be reduced to approximately one half of the SRAM array arrangement of 256 rows×16 columns, and therefore SRAM cells can be arranged in the rectangular SRAM array area shown in FIG. 10 or 18. In the SRAM array arrangement shown in FIG. 24, only one half of memory cells of one row of memory cells are selected, which realizes substantial block dividing operation or partial activation, and thus the SRAM can be driven with low current consumption.

Now, data transfer between DRAM array of FIG. 8 and SRAM array of FIG. 24 will be described with reference to FIGS. 25 through 30.

FIG. 25 shows an example of the structure of the transfer gate circuit BTG shown in FIG. 24. FIG. 25 shows, as a representative, a transfer gate circuit BTG1 provided for SRAM bit line pairs SBL1, *SBL1 and SBL2 and *SBL2, that is, for SRAM bit line taking lines SBLT1, *SBLT1, SBLT2 and *SBLT2. Transfer gate circuit BTG includes a selecting circuit 9501 for selecting a pair of bit lines out of two pairs of bit lines in response to an address signal Acd for the SRAM; and a transfer circuit 9502 for connecting global I/O lines GIO1 and *GIO1 to internal nodes A and B for transferring data between nodes A and B and global I/O lines GIO1 and *GIO1.

The least significant bit of the row address for the SRAM is used as the selection control signal applied to the selecting

circuit **9501**. When selected SRAM word line is an even numbered word line, selecting circuit **9501** selects SRAM bit line taking lines SBLT1 and *SBLT1 corresponding to the even numbered column, and otherwise it selects SRAM bit line taking lines SBLT2 and *SBLT2 corresponding to the odd numbered column.

The details of the structure of transfer circuit **9502** will be described later. Any circuit having the function of bi-directional data transfer may be used.

FIG. **26** shows an example of a specific structure of selecting circuit **9501** shown in FIG. **25**. Referring to FIG. **26**, selecting circuit **9501** includes an n channel MOS transistor GTr1 responsive to a selection control signal Acd for selecting SRAM bit line taking line SBLT1 (or *SBLT1), and a p channel MOS transistor GTr2 responsive to the selection control signal Acd for selecting SRAM bit line taking line SBLT2 (or *SBLT2). The other terminal of each of the transistors GTr1 and GTr2 is connected to node A (or B).

In the structure shown in FIG. **26**, when selection control signal Acd is 1 ("H" level), transistor GTr1 is rendered conductive, and SRAM bit line taking line SBLT1 (or *SBLT1) is selected and connected to node A (or B). When selection control signal Acd is 0 ("L" level), SRAM bit line taking line SBLT2 (or *SBLT2) is selected and connected to node A (or B).

In the structure shown in FIG. **24**, clamp transistors (indicated by the block CLP) for raising "L" level of potential amplitude are provided for the SRAM bit line pair SBL and *SBL. Therefore, the non-selected bit line pairs are maintained at the "H" clamp potential, and potential of each bit line changes only for the selected columns.

In the SRAM array structure shown in FIG. **24**, the clamp transistor (represented by block CLP in FIG. **24**) provided for each SRAM bit line pair SBL, *SBL are always kept conductive. A structure in which function of the clamp transistor is stopped during the SRAM word line selecting operation may be used.

FIG. **27** shows another structure of the SRAM array and a structure of the bi-directional transfer gate circuit used associatively. FIG. **27** shows, as representatives, SRAM bit line pairs SBL**0**, *SBL**0**, SBL1 and *SBL1. The SRAM cells are omitted for simplicity of the drawing. Accurately, SRAM bit line taking lines SBLT and *SBLT are connected to the transfer gate circuit (BTG1). However, in FIG. **27**, the SRAM bit lines SBL and *SBL are shown to be directly connected to the transfer gate circuit.

Referring to FIG. **27**, for SRAM bit line pair SBL**0** and *SBL**0**, p channel MOS transistors SQE1, SQE2 and SQE3 responsive to a SRAM bit line equalizing signal SBLEQ for precharging and equalizing SRAM bit lines SBL**0** and *SBL**0** to a predetermined potential, and p channel MOS transistors SQC1 and SQC2 responsive to a SRAM bit line clamping signal SBLCL for clamping potentials on SRAM bit lines *SBL**0** and SBL**0** are provided. Transistors SQE1 and SQE2 precharge SRAM bit lines *SBL**0** and SBL**0** to a predetermined potential (Vcc) in response to SRAM bit line equalizing signal SBLEQ. Transistor SQE3 equalizes potential on SRAM bit lines SBL**0** and *SBL**0** in response to SRAM bit line equalizing signal SBLEQ.

Transistors SQC1 and SQC2 clamp potentials on SRAM bit lines *SBL**0** and SBL**0** in response to SRAM bit line clamping signal SBLCL. Transistors SQC1 and SQC2 also function as load transistors. SRAM bit line equalizing signal SBLEQ is generated at a standby of the SRAM, and SRAM bit line clamping signal SBLCL is set to the inactive state of "H" when a word line is selected in the SRAM array.

For SRAM bit lines *SBL1 and SBL1, p channel MOS transistors SQE4, SQE5 and SQE6 which are rendered conductive in response to SRAM bit line equalizing signal SBLEQ, and p channel MOS transistors SQC3 and SQC4 which are rendered conductive in response to SRAM bit line clamping signal SBLCL are provided. Transistors SQE4 and SQE5 precharge SRAM bit.lines *SBL1 and SBL1 at the time of standby. Transistor SQE6 equalizes potentials on bit lines *SBL1 and SBL1 at the standby of the SRAM. Transistors SQC3 and SQC4 clamp potentials on SRAM bit lines *SBL1 and SBL1.

In the SRAM array arrangement shown in FIG. **27**, each of the bit lines SBL and *SBL is precharged to the "H" level at the standby of the SRAM, the clamping transistor is rendered non-conductive only when the word line is being selected, and SRAM bit lines are set to the floating state. In this state, when SRAM bit lines SBL**0** and *SBL**0** are selected, potential change corresponding to the data stored in the selected memory cell appears on the bit lines. Meanwhile, non-selected bit line pair SBL1 and *SBL1 is maintained at "H" level of the potential having been clamped by the clamping transistors SQC3 and SQC4. In such a structure in which potentials of one pair of bit lines out of two pairs of-bit-lines connected to one transfer gate circuit is at the clamp potential and potential change corresponding to the stored data of the memory cell (SRAM cell) appears only on the other bit line pair, selecting circuit for selecting an SRAM bit line pair is not necessary when data is transferred from the SRAM array to the DRAM array.

The structure shown in FIG. **27** utilizes the fact that the potential of one bit line pair is clamped at "H". Referring to FIG. **27**, the transfer gate circuit **9600** (BTG1) includes an amplifier **9601** receiving signal potentials on SRAM bit line pairs SBL**0**, *SBL**0** and SBL1, *SBL1 for amplifying potential of the SRAM bit lines on which potential change is generated; a first transfer circuit **9602** for transferring a signal from amplifier **9601**; a latch circuit **9603** for latching signal data transferred from first transfer circuit **9602**; and a second transfer circuit **9604** for transferring data latched in latch circuit **9603** to DRAM array (global IO line). Amplifier **9601**, first transfer circuit **9602**, latch **9603** and second transfer circuit **9604** are used for data transfer from SRAM array to DRAM array.

Bi-directional transfer gate circuit **9600** further includes an amplifier **9605** for amplifying data from global IO lines GIO1 and *GIO1 from the DRAM array; a third transfer circuit **9606** for transferring data amplified by amplifier **9605**; and selecting gate **9607** for transmitting data from transfer circuit **9606** by selecting corresponding SRAM bit line pair in accordance with the least significant bit Acdr of the SRAM row address. Amplifier **9605**, third transfer circuit **9606** and selecting gate **9607** are used for data transfer from the DRAM array to the SRAM array.

FIG. **28** shows a specific structure of the data transfer path from the SRAM array to the DRAM array. Referring to FIG. **28**, amplifier circuit **9601** includes n channel MOS transistors SQAL and SQA2 having their gates connected to SRAM bit lines SBL**0** and SBL1, respectively; and n channel MOS transistors SQA3 and SQA4 having their gate connected to respective complementary SRAM bit lines *SBL**0** and *SBL1. Transistors SQA1 and SQA2 are connected in series, and the other conduction terminal of transistor SQA2 is connected to ground potential Vss. Transistors SQA3 and SQA4 are connected in series, and the other conduction terminal of transistor SQA4 is connected to ground potential Vss.

First transfer circuit **9602** includes n channel MOS transistors SQA**5** and SQA**6** which are rendered conductive in

response to data transfer designating signal DTL. Transistor SQA5 is connected in series with transistor SQA1, and transistor SQA6 is connected in series with transistor SQA3.

Latch circuit **9603** includes inverter circuits SIV1 and SIV2 connected in anti-parallel, and inverter circuits SIV3 and SIV4 for inverting data transferred from transfer circuit **9602**.

Second data transfer circuit **9604** includes a transfer gate **9604***a* for transmitting an output from latch circuit **9603** to global I/O line GIO1 and a transfer gate **9604***b* for transferring data latched in latch circuit **9603** to global I/O line *GIO1. Transfer gates **9604***a* and **9604***b* includes n channel MOS transistors SQA7 and SQA8 which are rendered conductive in response to data transfer designating signal DTA, respectively.

FIG. **29** shows an example of the specific structures of the amplifier, the third transfer circuit and the selecting gate shown in FIG. **27**. Referring to FIG. **29**, amplifying circuit **9605** includes an n channel MOS transistor SQB1 having its gate connected to the global I/O line GIO1, an n channel MOS transistor SQB3 having its gate connected to the complementary global I/O line *GIC1, n channel MOS transistors SQB2 and SQB4 which are rendered conductive in response to data transfer designating signal DTS for transmitting signal potential amplified by transistors SQB1 and SQB3, and p channel MOS transistors SQB5, SQB6, SQB7 and SQB8 for amplifying and maintaining the signal potential transmitted from the transistors SQB2 and SQB4. Transistors SQB5 and SQB6 are connected in parallel between supply potential Vcc and node SND1. Data transfer designating signal DTS is applied to the gate of transistor SQB6. The transistor SQB5 has its gate connected to node SND2. Transistors SQB7 and SQB8 are connected in parallel between supply potential Vcc and node SND2. Transistor SQB7 has its gate connected to node SND1. Data transfer designating signal DTS is applied to the gate of transistor SQB8.

Third transfer circuit **9606** includes two transfer gates **9606***b* and **9606***a*. Transfer gate **9606***a* includes an n channel MOS transistor SQB10 which is rendered conductive in response to data transfer designating signal DTS for transmitting data amplified by amplifier circuit **9605**. Transfer gate **9606** includes an n channel MOS transistor SQB9 which is rendered conductive in response to data transfer designating signal DTS for transmitting signal potential at node SND1 of amplifier circuit **9605**.

Selecting gate **9607** includes two selecting gates **9607***a* and **9607***b*. Selecting gate **9607***a* includes an n channel MOS transistor SQB14 which is rendered conductive in response to SRAM address Acdr, and an n channel MOS transistor SQB13 which is rendered conductive in response to SRAM address *Acdr. The least significant bit (Ac4) of the row address of the SRAM array is used to generate the SRAM addresses Acdr and *Acdr.

Selecting gate **9607***b* includes an n channel MOS transistor SQB12 which is rendered conductive in response to address signal Acdr for transmitting data from transfer gate **9606**, and an n channel MOS transistor SQB11 which is rendered conductive in response to complementary address signal *Acdr for transmitting data from transfer gate transistor SQB9. When address signal Acdr is at "H", transistors SQB12 and SQB14 are rendered conductive and bit line pair SBL1 and *SBL1 is selected. When address signal Acdr is at "L", transistors SQB11 and SQB13 are rendered conductive and bit line pair SBL0 and *SBL0 is selected.

Prior to the data transfer operation, the operation of the amplifier circuit **9605** will be briefly described. Assume that global I/O line GIO1 is at "H" and global I/O line *GIC1 is at "L". In this case, if the signal DTS is at "H", transistor SQB1 is conductive and transistor SQB3 is rendered non-conductive. Potential at node SND1 is discharged to ground potential Vss, while there is no discharging path for the potential at node SND2. In this case, transistor SQB7 is rendered conductive, and potential of node SND2 is charged by transistor SQB7. Therefore, the potential at node SND2 is set to "H" and potential at node SND1 is set to "L". When data transfer is to be designated, data transfer designating signal DTS rises to "H". Therefore, in data transfer, transistors SQB6 and SQB8 are rendered non-conductive, and potentials at nodes SND1 and SND2 are rapidly set at potentials corresponding to the data which is to be transferred. Normally, the signal DTS is at "L", and nodes SND1 and SND2 are maintained at "H" level by transistors SQB6 and SQB8. The data transfer operation of the transfer circuit shown in FIG. **27** will be described with reference to FIG. **30**, which is a diagram of signal waveforms.

In data transfer operation of transfer circuit **9600** shown in FIG. **27**, data is transferred from the SRAM array to latch circuit **9603**, while data is transferred from the DRAM array to the SRAM array. Thereafter, data which has been latched in latch circuit **9603** is transferred to DRAM array. The data transfer operation of transfer circuit will be described in detail later.

When SRAM bit line equalizing signal SBLEQ rises to "H", SRAM enters the memory cycle. In response, precharge and equalizing transistors SQE1 to SQE6 provided for each bit line pair SBL, *SBL are rendered non-conductive. At this time, SRAM bit line clamping signal SBLCL is still at "L", and each bit line SBL, *SBL is maintained at "H" level through the clamping transistors (SQC1, SQC2, SQC3 and SQC4).

Thereafter, word line selecting operation is executed in the SRAM array, and the SRAM word line rises. Approximately at the same time, the SRAM bit line clamping signal SBLCL rises to "H". Timing of rising of clamping signal SBLCL may be set earlier than the word line selecting timing in the SRM array. Consequently, data of half of the memory cells of one row are read. Assume that word line SWL1 is selected. In this case, referring to FIG. **27**, SRAM bit line pair SBL0 and *SBL0 maintain "H" level as in the standby state. Meanwhile, potentials of SRAM bit line pair SBL1 and *SBL attain the levels corresponding to the data stored in the memory cells connected thereto. In this case, referring to FIG. **28**, transistors SQA1 and SQA3 are rendered conductive. Conduction/non conduction of transistors SQA2 and SQA4 is determined dependent on the data of the selected memory cell at that time.

Responsive to the rise of data transfer designating signal DTL to "H", signal potentials on SRAM bit lines SBL1 and *SBL1 are latched by latch circuit **9603**.

In parallel to the latching operation, data transfer from the DRAM array to the SRAM array is executed. In the SRAM array, the word line is kept at the selected state. When signal potentials on global I/O lines GIO1 and *GIO1 are established, conduction/non conduction of transistors SQB1 and SQB3 is determined (see FIG. **29**). Thereafter, when data transfer designating signal DTS is generated, transistors SQB2 and SQB4 are rendered conductive, data on global I/O lines GIO1 and *GIO1 are inverted and amplified to be maintained at nodes SND1 and SND2.

The data at nodes SND1 and SND2 are transmitted to selecting gates **9607***b* and **9607***a* through transfer gates SQB9 and SQB10 which are already conductive in response to the signal DTS. Now, since word line SWL1 is selected

and address signal Acdr is at "H", transistors SQB14 and SQB12 are rendered conductive, and data on transfer gates **9606***b* and **9606***a* are transmitted to SRAM bit line pair *SBL1 and SBL1. Consequently, data are transferred to the corresponding SRAM memory cells. In FIG. **30**, the reference character Ac represents the SRAM address in data transfer from the DRAM array to the SRAM array.

Then, after the data transfer from the DRAM array to the SRAM array, the DRAM is once returned to the standby state. When the DRAM array is rendered active, the data which has been latched in latch circuit **9603** is transmitted to the DRAM array (global I/O lines GIO1 and *GIO1). In this case, data transfer designating signal DTA attains "H", transfer gates **9604***a* and **9604***b* are rendered conductive, and data which has been latched in latch circuit **9603** is transmitted to global IO lines GIO1 and *GIO1. During data transfer from the latch circuit **9603** to the DRAM array, the SRAM array can be independently accessed.

When the SRAM word line is selected, the SRAM bit line clamping signal SBLCL is set to "H" in order to surely set the amplifying transistor included in the amplifier circuit **9601** to conductive/non-conductive state during data transfer. In this case, a structure may be used in which clamping function is set to non-operative state only during data transfer, and the clamp signal SBLCL is always kept active when the SRAM array is accessed with data transfer not being carried out. A structure for block division or partial activation in which SRAM bit line pair is selected dependent on the even/odd row address may be used for writing/reading of data of the SRAM array.

Data transfer operation between DRAM array and SRAM array will be discussed in more detail later.

As described above, since one row of SRAM cells are divided into a plurality of groups and a plurality of word lines are arranged corresponding to respective groups for each row, an SRAM array which can have an arbitrary shape without changing memory structure of rows and columns can be provided.

Since the shape of the SRAM array can be arbitrary selected, the degree of freedom in designing the SRAM array arrangement is improved. Therefore, an SRAM array having optimal shape for the DRAM array can be arranged, and therefore a semiconductor memory device containing a cache having high density and high degree of integration effectively utilizing chip area can be provided.

Since the shape of the SRAM array can be changed without changing the memory structure, a semiconductor memory device which can be contained easily in a package having an arbitrary shape can be provided.

[Pin Arrangement]

FIG. **31** shows an example of a pin arrangement of a package housing the CDRAM having the array arrangement [Array Arrangement 3] shown in FIG. **10**. As shown in FIG. **10**, the CDRAM contained in the package of FIG. **31** includes a 4M bit DRAM and a 16K bit SRAM integrated on one chip. The CDRAM is housed in a 300 mil TSOP (Thin Small Outline Package) of type II with lead pitch of 0.8 mm, chip length of 18.4 mm and 44 pins.

The CDRAM has two data input/output modes, that is, D/Q separation and masked write. D/Q separation is a mode of inputting/outputting write data D and output data Q through separate pins. Masked writing is an operation mode in which write data D and read data Q are output through the same pin terminal, and writing of external data can be masked.

In order to effectively supply the supply voltage to CDRAM and to facilitate layout of power supply interconnection, three pins are provided for each of the supply potential Vcc and Gnd. More specifically, external supply potential vcc is supplied to pins of the pin numbers **1**, **11** and **33**. The supply potential Vcc supplied to the pins **1**, **11** and **33** may have the same voltage values as the operational supply potential Vcc. Alternatively, the external supply potential Vcc supplied to the pins **1**, **11** and **33** may be lowered in the device to supply the operational supply potential. The ground potential GND is supplied to the pins of the numbers **12**, **22** and **34**. Pins of the numbers **11**, **12**, **33** and **34** at the center provide operational power supply for SRAM, while pins of the numbers **1** and **22** provide power supply for DRAM.

A cache inhibiting signal CI# indicating cache access inhibition is applied to a pin terminal of the number **4**. When the cache inhibition signal CI# is set to "L", access to the SRAM array is inhibited, and direct access (array access) to the DRAM array is allowed.

A write enable signal W# indicating data writing mode is applied to the pin of the number **5**. A chip select signal ER indicating that this chip is selected, is applied to a pin of the number **18**.

A command register designating signal CR# for designating the special mode is applied to a pin of the pin number **23**. When the command register designating signal CR# is "L", command addresses Ar0 and Ar1 applied to the pins of the numbers **2** and **3** are rendered valid, enabling setting of the special mode (selection of a register).

A cache hit signal CH# indicating a cache hit is applied to a pin of the pin number **27**. If the cache hit signal CH# is "L", access to the cache (SRAM) is possible. An output enable signal G# indicating an output mode is applied to a pin of the number **40**. A clock signal K is applied to the pin of the number **41**.

A refresh designating signal REF# designating refreshing of the DRAM array is applied to a pin of the number **44**. When the refresh designating signal REF# attains to "L", automatic refreshing of the DRAM array inside is carried out in the cycle.

When self refreshing is designated, the pin terminal of the pin number **44** is switched to an output terminal. When self refreshing is effected, a signal BUSY# indicating execution of self refreshing is output from the pin terminal of the pin number **44**. It becomes possible to know the timing of the self refreshing outside the CDRAM by this signal BUSY#, and therefore self refreshing can be utilized in a normal cycle.

Different data are applied to the pins of the numbers **9**, **10**, **13**, **14**, **31**, **32**, **35** and **36** dependent on the two different operation modes, that is, D/Q separation and masked write. The operation modes of D/Q separation and masked write are set by a command register (which will be described later).

In masked write mode, pins of the numbers **10**, **13**, **32** and **35** are used as common data input and output terminals for commonly carrying out data input/output. Pins of the numbers **9**, **14**, **31**, **35** and **36** receive masked write designating data M0, M1, M2 and M3 for indicating which data applied to which input/output pins should be masked, respectively.

In D/Q separation mode, pins of the numbers **9**, **14**, **31** and **36** are used as pins for inputting write data D0, D1, D2 and D3. Pins of the numbers **10**, **13**, **32** and **35** are used as data output pins for outputting read data Q0, Q1, Q2 and Q3.

SRAM addresses Ac0 to Ac11 and DRAM addresses (array addresses) Aa0 to Aa9 are applied through separate pin terminals and independent from each other. In the pin arrangement shown in FIG. **31**, external operation control

signals generally used in a standard DRAM, that is, row address strobe signal/RAS and column address strobe signal/CAS are not used. In the CDRAM contained in the package of FIG. 31 (see FIG. 10), data and control signals are input in response to a rising edge of an external clock signal K.

[Internal Function]

In this section, internal functions of CDRAM are briefly described.

(i) FIG. 32 is a block diagram showing internal structure of the CDRAM chip housed in a package of FIG. 31. The block arrangement shown in FIG. 31 is for the purpose of functionally showing the internal structure of the CDRAM, and it should be noted that the structure shown in this figure is not the same as the actual layout.

Referring to FIG. 32, a CDRAM includes a DRAM 100 and a SRAM 200. DRAM 100 comprises a 4M bit DRAM array 101; a DRAM row decoder block 102 for decoding an applied internal row address for the DRAM and for selecting 4 rows from DRAM array 101; a DRAM column decoder block 103 for decoding applied internal column address for DRAM and for selecting one column from each of the selected 4 rows in a normal operation mode (array access); and a block 104 including DRAM sense amplifiers DSA for detecting and amplifying data of the memory cells connected to the selected rows, and selecting gates SG responsive to a column selecting signal from block 103 for selecting 16 bits of DRAM array 101 in a data transfer mode and for selecting 4 bits of memory cells in an array access mode.

SRAM 200 comprises an SRAM array 201 having the capacity of 16K bits; a SRAM row decoder block 202 for decoding an internal row address for the SRAM and for selecting 4 rows from SRAM array 201; and a column decoder/sense amplifier block 203 including SRAM column decoders and SRAM sense amplifiers for decoding the internal column address for the SRAM, selecting 1 bit from each of the selected 4 rows and connect the same to an internal data bus 251, and for detecting and amplifying information of the selected SRAM cells in data reading. A bi-directional transfer gate circuit 210 is provided between DRAM 100 and SRAM 200. Referring to FIG. 32, the gate circuit 210 may be connected to an output (input) of the column decoder/sense amplifier block 203, as in the arrangement of FIG. 10. However, in FIG. 32, data input/output to and from DRAM 100 are carried out through the common data bus 251 in the array access mode, and therefore the common data bus 251 is shown as coupled to bi-directional transfer gate circuit 210.

The CDRAM in accordance with the present invention further comprises a control clock buffer 250 receiving externally applied control signals G#, W#, E#, CH#, CI#, REF# and CR# to generate internal control signals G, W, E, CH, CI, REF and CR; an address buffer 252 for generating an internal address int-Aa for the DRAM and an internal address int-Ac for the SRAM; and a clock buffer 254 for buffering an externally applied clock signal K. Control clock buffer 250 takes an applied control signal and generates an internal control signal in response to a rise of an internal clock from clock buffer 254. An output from clock buffer 254 is also applied to address buffer 252. Address buffer 252 takes an externally applied addresses Aa and Ac which are applied when the internal chip enable signal E is active at a rising edge of the clock K from the clock buffer 254 and generates internal addresses int-Aa and int-Ac.

The CDRAM includes a refresh circuit 290 for refreshing memory cells in DRAM array 100. Refresh circuit 290 includes a counter circuit 293 which is activated in response to internal refresh designating signal REF for generating a refresh address of the DRAM array; and an address multiplex circuit 258 for applying either a refresh address from counter circuit 256 or an internal row address from address buffer 252 to DRAM row decoder block 102 in response to a switching signal MUX from a refresh control circuit 292. Refresh control circuit 292 is driven in response to a refresh request from an automatic refresh mode detecting circuit 291. The refresh operation will be described later.

The CDRAM further comprises a DRAM array driving circuit 260 responsive to the internal control signals E, CH, CI and REF for generating various control signals for driving DRAM 100; a transfer gate controlling circuit 262 responsive to the internal control signals E, CH and CI for generating signals for controlling transfer operation of bi-directional transfer gate 210; and a SRAM array driving circuit 264 responsive to internal chip select signal E for generating various control signals for driving SRAM 200.

The CDRAM in accordance with the present invention further comprises a command register 270 which is activated in response to an internal control signal CR for generating a command CM for designating operation mode of the CDRAM in response to external write enable signal Wr and to command addresses Ar (Ar0 and Ar1); a data input/output control circuit 272 for controlling data input/output in accordance with the internal control signals G, E, CH, CI and W and to the special mode command CM; an input/output circuit 274 formed of an input/output buffer and an output register for inputting/outputting data between common data bus 251 and the outside of the device. An output register is provided in the input/output circuit 274 for realizing a latched output mode and a registered output mode, which are the special modes of the CDRAM. Data input/output control circuit 272 sets input/output timing of data in accordance with the mode designated by the special mode command CM as well as the manner of input/output of data. In FIG. 32, manners of data input/output pins in masked write mode is shown as an example.

The CDRAM further includes an additional function control circuit 299 for realizing various functions. Functions realized by additional function control circuit 299 will be described in detail later. The function includes prohibition of generation of internal clocks at the time of standby, switching between autorefresh/self refresh, switching of address generating source in burst mode, and the like. Structures of various circuits will be described in the following.

[Input/Output Circuit]

(Connection Between DRAM Array, SRAM Array and Internal Data Line)

FIG. 33 shows one example of manner of connection of bi-directional transfer gate circuit (BTG) and internal common data line 251 shown in FIG. 32. Referring to FIG. 33, a SRAM input/output gate 301 comprises SRAM sense amplifier SSA and write circuit WRI which is activated in data writing to SRAM array for transmitting data on internal data line 251*a* to a corresponding SRAM bit line pair SBL. SRAM bit line pair SBL is connected through SRAM sense amplifier SSA and SRAM column selecting gate 302 to internal data line 251*a*. A SRAM column selecting signal SYL from SRAM column decoder block 203 is applied to SRAM selecting gate 302. Consequently, a pair of SRAM column bit line pair SBL only is connected to internal data line 251*a*. Internal data line 251 shown in FIG. 32 transfers 4 bits of data, and only an internal data line corresponding to 1 bit is shown in FIG. 33.

Referring to FIG. 33, the CDRAM further comprises an access switching circuit 310 responsive to a logical product signal on cache inhibiting signal CI and DRAM column

selecting signal DY for connecting global I/O line pair GIO to internal data line **251***a* for enabling array access. Access switching circuit **310** and bi-directional transfer gate BTG are included in transfer gate circuit block **305**.

The column selecting signal DYi of DRAM is generated by decoding, for example, lower 4 bits of a column address. More specifically, 16 pairs of global I/O lines GIO are provided for one DRAM memory mat (having the capacity of 1M bits). For array accessing, only one pair must be selected therefrom. Therefore, column selecting signal DYi is generated by decoding lower 4 bits of column address for DRAM.

The access switching circuit **310** simply connects global I/O line pair GIO to internal data line **251***a*, and connection to corresponding signal lines are carried out in bi-directional transfer gate BTG. A structure in which global I/O line pair GIO is connected to internal data line **251***a* through SRAM sense amplifier SSA may be used to realize array accessing, without providing such an access switching circuit **310**. At this time, column selecting signal applied to SRAM selecting gate **302** is a selecting signal based on column address to the DRAM. This is realized by a circuit multiplexing the column selecting signal by the signal CI. Such a multiplex circuit applies column selecting signal for DRAM to SRAM selecting gate, when the signal CI is active.

In the SRAM, a SRAM sense amplifier SSA is provided for each SRAM bit line pair SBL. However, one SRAM sense amplifier may be provided for the SRAM bit line pairs of 1 block, as in a normal SRAM. However, when the SRAM sense amplifier is provided for each SRAM bit line SBL, output of data can be more surely carried out at high speed. If the SRAM sense amplifier SSA has the same structure as the DRAM sense amplifier, it is not necessary to provide writing circuit WRI.

[Data Input/Output Circuitry with Reference to FIGS. **34** to **36**: Separated DQ and D/Q Common structure]

FIG. **34** shows a structure for realizing D/Q separation in input/output circuit **274**. Referring to FIG. **34**, input/output circuit **274** comprises an output buffer **320** which is activated in response to an internal output enable signal G for generating output data Q from data on internal data line **251***a*; an input buffer **322** which is activated in response to an internal write designating signal W for generating internal write data from external write data D and transmitting the same to internal data line **251**; and a switch circuit **324** responsive to a D/Q separation designating bit CMa from command register **270** (see FIG. **32**) for short-circuiting an output from output buffer **320** and an input of input buffer **322**. D/Q separation designating bit CMa is included in a special mode designating command CM generated from command register **270**. If the switch circuit **324** is rendered conductive, input/output of data are carried out through the same pin. If the switch circuit **324** is off, input/output of data are carried out through separate pins. Structure related to data input/output of 1 bit only is shown in FIG. **34** as a representative.

FIG. **35** shows connection between data input/output circuit and other portions. Referring to FIG. **35**, output buffer circuit **320** receives data from selected memory cell data of DRAM array or SRAM sense amplifier to transmit the same to an external output pin Q. A first input buffer circuit **322***a* is connected to external pin terminal Q, and a second input buffer circuit **320***b* is connected to an external data input pin terminal D. Outputs of the first and second input buffer circuits **322***a* and **322***b* are transmitted through an OR circuit **322***c* to internal data buses DBW, *DEW (**251***a*). Enabling/disabling of the first and second input buffer circuits **322***a* and **322***b* are carried out in response to designation bit CM from command register (see FIG. **32**). If the command register designates D/Q separation mode, the first input buffer circuit **322***a* is disabled, and input buffer circuit **322***b* is enabled. If the designation bit CM designates masked write mode common to D/Q, the first input buffer circuit **322***a* is enabled and the second input buffer circuit **322***b* is disabled.

In the structure shown in FIG. **35**, data from SRAM sense amplifier are transmitted to output buffer circuit **320**, since this figure shows a case in which data of selected memory cells of the DRAM array are transmitted to internal data bus through column lines (bit lines) of SRAM array and through sense amplifiers of the SRAM. More specifically, this figure shows an example of the structure of FIG. **33** without the gate **310**, in which column selecting signals SYLi and SYLj applied to gate **302** are commonly used as the DRAM column decoder outputs DYi and DYj. This structure will be described later.

FIG. **36** shows a further structure of the input/output circuit. Referring to FIG. **36**, a transistor **324***a* which is turned on in response to the designation bit CMa is provided between output buffer circuit **320** and input buffer circuit **322**. A transistor gate **324***b* which is turned on in response to a complementary designation bit/CMa is provided between input buffer circuit **322** and a data input pin terminal D. In this structure, when designation bit CMa designates D/Q separation mode, the transistor gate **324***a* is turned off, and the transistor gate **324***b* is turned on. Conversely, if the designation bit CMa designates masked write mode with common D/Q pin, the transistor gate **324***a* is turned on and the transistor gate **324***b* is turned off.

By this structure, input buffer circuit **322** can be selectively connected to data output pin terminal Q or to data input pin terminal D, whereby D/Q separation mode and D/Q common mode can be selectively set.

[Data Output Modes of Transparent, Latched and Registered Modes With Reference to FIGS. **37** Through **43B**]

A circuit structure for setting a data output mode of the input/output circuit will be described. The data output mode is set by a command register.

The data output mode is set to transparent mode, latch mode or register mode in accordance with the set data set in the command register.

FIG. **37** shows a circuit structure related to setting of data output mode. Referring to FIG. **37**, command register **270** includes a command register mode selector **279** responsive to a command register mode detecting signal (internal command register signal) CR for decoding write enable signal W# and command data **Ar0** and **Ar1**, registers **WR0–WR3**, and a flipflop **FF1**. Command register includes 8 registers **RR0–RR3** and **WR0–WR3**, as will be described later. However, in FIG. **37**, registers **RR2** and **RR3** are not shown. Each of the registers **WR0–WR3** is a 4-bit register. Registers **RR0** and **RR1** share one flipflop **FF1**. When register **RR0** is selected, flipflop **FF1** is set to masked write mode. When register **RR1** is selected, flipflop **FF1** is set to D/Q separation mode in which D pins and Q pins are separated. An input control circuit **272***b* selects either an input circuit **274***b* or **274***c* dependent on the data set in the flipflop **FF1**.

By decoding command data **Ar0** and **Ar1**, it is determined to which register **WR0–WR3** the data is to be set. When write enable signal W# is active, 4 bits of data **D0–D3** (or **DQ0–DQ3**) are set to a corresponding register, through the input circuit **274***b* or **274***c* selected by input control circuit **272***b*. Since register **WR0** is related to data output mode, setting of data output mode will be described. Output control

circuit 272a is set in a transparent, latched or registered output mode in accordance with lower 2 bits of data of the register WR0, and it outputs control signals ϕ1, /ϕ1 and ϕ2 for selectively activating output circuit 274a, dependent on the set output mode.

FIG. 38 shows an example of a specific structure of the output circuit 274a. Referring to FIG. 38, output circuit 274a includes a first output latch 981 responsive to control signals ϕ1 and /ϕ1 for latching data on read data buses DB and *DB, a second output latch 982 responsive to a clock signal ϕ2 for passing data latched in output latch 1 or data on data buses DB and *DB, and an output buffer 983 receiving data from output latch 982 for transmitting the same as output data to an external pin terminal DQ in response to control signal G#.

First output latch 981 includes clocked inverters ICV1 and ICV2 which are activated in response to clock signals ϕ1 and /ϕ1. An input and an output of clocked inverter ICV1 are connected to an output and an input of clocked inverter ICV2, respectively. Output latch 981 is set to a latched state when clock signal ϕ1 is "H". Namely, clocked inverters ICV1 and ICV2 are activated when clock signal ϕ1 is "H" and serve as an inverter. When clock signal ϕ1 is "L", clocked inverters ICV1 and ICV2 are disabled, and latch 981 does not carry out latching operation.

Second output latch 982 latches data applied to inputs A and *A and outputs the data from outputs Q and *Q, when clock signal ϕ2 is at "L". Output latch 982 outputs data latched when clock signal ϕ2 is at "L" from outputs Q and *Q regardless of the signal state at inputs A and *A, when clock signal ϕ2 is "H". Clock signals ϕ1, /ϕ1 and ϕ2 controlling the latching operation are synchronous with external clock K, and timings of generation thereof are made different from each other by output control circuit.272a.

Output buffer 983 is activated when output enable signal G# is made active, and transmits output data from output latch 982 to a terminal DQ.

FIG. 39 shows an example of a specific structure of second output latch 982. Referring to FIG. 39, second output latch 982 includes a D flipflop DFF receiving an input A (*A) at a D input thereof and receiving clock signal ϕ2 at its clock input CLK. An output Q (*Q) of output latch 982 is provided from output Q of the flipflop DFF. The D flipflop DFF is of a down edge trigger type. It takes an input A at a timing of a fall of the clock signal ϕ2 to L, and outputs input A as received while clock signal ϕ2 is "L". When clock signal ϕ2 is at "H", it outputs previously latched data, regardless of the state of the input A applied to input terminal D. Thus, an output latch 982 realizing desired function is provided. D type flipflop DFF is provided for each of the inputs A and *A. The output latch 982 may have other structure. Any circuit structure capable of realizing latched state and through state in response to clock signal ϕ2 may be used.

FIG. 40 shows an example of a specific structure of the output control circuit 271a. Output control circuit 272a includes delay circuits 981a, 981b and 981c for providing a predetermined time delay to the external clock; a one shot pulse generating circuit 992a for generating a one shot pulse signal having a predetermined pulse width in response to an output from delay circuit 991a; a one shot pulse generating circuit 992b for generating a one shot pulse signal having a predetermined pulse width in response to an output from delay circuit 991b; and a one shot pulse generating circuit 992c for generating a one shot pulse signal having a predetermined pulse width in response to an output from delay circuit 991c. Clock signals ϕ1 and/ϕ1 are generated from one shot pulse generating circuit 992a.

Outputs from one shot pulse generating circuits 992b and 992c are applied to an OR circuit 993. Clock signal ϕ2 is generated from OR circuit 993. Delay time provided by the delay circuit 991b is shorter than the delay time provided by the delay circuit 991c. Enable/disable of one shot pulse generating circuits 992a to 992c is set by 2 bits of command data WR0. When 2 bits of command data WR0 represents latch mode, one shot pulse generating circuits 992a and 992c are enabled, and one shot pulse generating circuit 992b is disabled. Operation of the command register and the data output circuit shown in FIGS. 37 to 40 will be described.

First, latch operation will be described with reference to FIG. 41, which is a diagram of signal waveforms. Latched output mode as the data output mode is set by setting lower 2 bits of command data register WR0 to (01). At this time, one shot pulse generating circuits 992a and 992c are enabled. Let us assume that output enable signal G# is at an active state of "L", indicating data output. At this time, an external address An is taken into an address buffer at a rising edge of the clock K, a corresponding SRAM word line SWLn is selected, and data RDn appears on the SRAM bit line SBL. At this time, one shot pulse generating circuit 992a generates a one shot pulse at a predetermined timing in response to the rise of external clock K, and is kept at "L" for a predetermined time period. When the clock signal ϕ1 falls to "L", latch operation of output latch 981 is prohibited. At this time, clock signal ϕ2 is at "H" maintaining the latch state, latches and outputs data Qn−1 which has been read in the previous cycle. 4 bits of data selected in accordance with an external address out of 64 bits of data RDn on the SRAM bit line pair SBL which has been selected by the external address are transmitted to internal output data buses DB and *DB. With the data DBn on data buses DB and *DB being established, the clock signal ϕ1 rises to "H". Consequently, output latch 981 carries out latching operation to latch the established data DBn.

Thereafter, a one shot pulse is generated from one shot pulse generating circuit 992c and signal ϕ2 falls to "L". Consequently, output latch 982 newly takes the latched data DBn and transmits the same to output terminal DQ through an output buffer 983. The clock signal ϕ2 is generated in synchronization with a fall of the clock K, and in response to a fall of the external clock K, data DBn selected in this cycle is output as output data Qn. Clock signal ϕ2 rises to "H" by the time the external clock K rises again. Consequently, output latch 982 continuously output established data DBn regardless of the data on internal output data buses DB and *DB.

Thereafter, clock signal ϕ1 is set to "L" and latch state of output latch 981 is released, so as to be ready for the next cycle, that is, latching operation of the next established data. Consequently, in response to a rise of the external clock K, data read in the previous cycle are output successively as established data.

Register mode will be described with reference to FIG. 42. Setting of the register mode is done by setting lower 2 bits of command data WR0 to (11). In registered output mode, one shot pulse generating circuit 992b is enabled, and one shot pulse generating circuit 992c is disabled. At this time, in response to a rise of the external clock K, a one shot pulse which falls to "L" is generated from one shot pulse generating circuit 992b. Since clock signal ϕ1 is at "H" at this time, data DBn−1 which has been read in the previous cycle is latched by output latch 982.

In registered output mode, timing of falling of clock signal ϕ2 to "L" is determined in response to a rise of external clock K. In this case, in response to (n+1) th cycle

of the external clock K, data DBn read in nth clock cycle is output as output data Qn at output pin terminal DQ. Namely, only the timing of generation of the clock signal φ2, that is, timing of falling thereof to "L" is different between latched output mode and registered output mode. Consequently, latched output mode in which data of previous cycle is output and data read in the present cycle is output continuously, and registered output mode in which data read in nth cycle is output at (n+1) th cycle are realized.

Transparent mode will be described with reference to FIGS. **43**A and 43B. A first transparent output mode will be described with reference to FIG. **43**. As described above, transparent output mode is realized by setting lower 2 bits of the register **WR0** to (X0). The first transparent output mode or a second transparent output mode is selected by setting the bit value of X to 0 or 1. Either first transparent output mode or second transparent output mode may be selected arbitrarily corresponding to either of the values of X. In first transparent output mode, clock signals **φ1** and **φ2** are both maintained at "L". At this time, latch operation in output latch **981** is released, and output latch **982** is in a through state. Therefore, in this case, data DBn transmitted to internal data buses DB, *DB are directly output as output data Qn. If data on the SRAM bit line pair SBL or global I/O line pair GIO is invalid data (INVALID DATA), invalid data INV appears on output pin DQ in response.

In second transparent output mode shown in FIG. **43**, clock signal **φ1** is generated. First output latch **981** carries out latching operation while clock signal **φ1** is at "H". Therefore, even if data RDn on SRAM bit line pair SBL is set to an invalid state, data on data buses DB and *DB are latched as valid data by latch circuit **891** and output for a predetermined time period (while the clock signal **φ1** is at "H"). Therefore, a period in which invalid data INV is output can be made shorter. In second transparent output mode, clock signal **φ2** is also kept at "L".

Although a D flipflop of a down edge trigger type has been used as second output latch **982** in the above described structure, an up edge trigger type latch circuit may be used to provide the same effect, by changing polarity of the clock signal **φ2**. The structure of output latch **981** can also be implemented by other latch circuits.

The characteristics of the output modes set by the common register are as follows.

(1) Transparent output mode: In this mode, data on internal data buses DB, *DB are directly transmitted to an output buffer. In this mode, valid data as output data DQ (Q) appears after a time lapse of tKHA (array access time) from a rising edge of external clock K or after a lapse of a time period tGLA (access time from the signal G# has reached "L" to an output of a valid data) from a falling edge of output enable signal G#, which is later. If output enable signal G# falls before the time tKHA, invalid data (INV) is kept continuously output to tKHA, since valid data has not yet appeared on internal data buses DB and *DB, if output enable signal G# falls at an earlier timing. Therefore, in this mode, a period in which output data is valid is limited to a period in which valid data is appearing on the internal bus.

(2) Latched output mode: In this mode, an output latch circuit is provided between the internal data buses DB and *DB and the output buffer. In the latched output mode, data is latched by an output latch circuit while external clock K is at "H". Therefore, when output enable signal G# falls before the time tKHA, data read in the previous cycle is output. Therefore, even if invalid data has appeared on internal data buses DB and *DB, invalid data is not output externally. Namely, this mode provides an advantage that sufficient time period for the CPU to take output data in can be provided.

(3) Registered output mode: In this mode, an output register is provided between the internal data bus and the output buffer. In the registered output mode, valid data of the previous cycle is output as output data after a lapse of tKHAR from a rising edge of external clock K or after a lapse of tGLA from a falling edge of output enable signal G#, which is later. From the same reason as in the latch mode, invalid data is not output in register mode. When data are to be output continuously in register mode, it seems that data are output at very high speed in view of the rise of the external clock K. Such operation is generally called a pipeline operation, in which an apparent access time can be further reduced from the cycle time.

Since the above described output modes can be set by command registers, a user can select an output mode suitable for a system.

[Data Transfer Between DRAM and SRAM]

Now, the data transfer between DRAM array and SRAM will be described in detail with reference to FIGS. **44** through **60D**. Transfer mode includes (a) block transfer mode from DRAM to SRAM, (b) copy back mode from SRAM to DRAM and (c) fast copy back mode with block transfer and copy back-modes in parallel. In the following description, no multiple word line scheme in SRAM array is assumed. However, the data transfer method in the following is also applicable to multiple SRAM word line structure.

FIG. **44** shows one example of a structure of bi-directional transfer gate BTG. Referring to FIG. **44**, bi-directional transfer gate BTG (BTGa or BTGb) comprises a drive circuit DR1 which is activated in response to data transfer designating signal φTSD for transmitting data on SRAM bit line pair SBL to global I/O line pair GIO, and a drive circuit DR2 which is activated in response to data transfer designating signal φTDS for transmitting data on global I/O line pair GIO to SRAM bit line pair SBL. Drive circuits DR1 and DR2 are set to an output high impedance state when data transfer designating signals φTSD and φTDS are inactive.

(a) FIG. 45 is a diagram of signal waveforms showing operation when data are transferred from DRAM array to SRAM array. Data transfer operation from DRAM array to SRAM array will be described with reference to FIGS. **78** and **44**.

While precharge designating signal φEQ is at an active state "H" before time t1, sense amplifier driving signal lines φSAN, /φSAP, local I/O line pair LIO and global I/O line pair GIO are maintained at a precharge potential of Vcc/2. At this time, precharge equalize circuit PE is activated to precharge DRAM bit line pair DBL to the precharge potential of Vcc/2 (=Vb1) and equalizes potentials of the bit lines BL, /BL.

When precharge designating signal φEQ falls at **t1**, precharge equalize circuit PE and equalize transistor TEQ are rendered inactive. Consequently, equalizing operation of the sense amplifier driving signal lines φSAN and/φSAP is completed, equalize/precharge operation of DRAM bit line pair DBL is stopped, and DRAM bit line pair DBL and sense amplifier driving signal lines φSAN and/φSAP are set to a floating state at the intermediate potential vcc/2 (where Vss=0V).

Thereafter, in accordance with an externally applied address, row selecting operation is effected by row decoder **14** (see FIG. **7**), one word line DWL is selected in DRAM array **1** (see FIG. **7**) at **t2**, and potential of the selected word line DWL rises to "H". One row of memory cells connected to the selected word line DWL are connected to corresponding DRAM bit line pair DBL (DRAM bit line BL or /BL), and potential of respective DRAM bit lines changes depen-

dent on data of the memory cell connected thereto. FIG. 45 shows potential change of a DRAM bit line pair DBL when a memory cell storing the potential "H" is selected.

At time t3, sense amplifier activating signal φSANE rises from ground potential Vss to the operational supply potential Vcc level, and transistor TR2 in sense amplifier activating circuit SAK is turned on. Consequently, the second sense amplifier portion in DRAM sense amplifier DSA is activated, and a bit line of lower potential in the DRAM bit line pair DBL is discharged to the level of the ground potential GND.

At time t4, sense amplifier activating signal/φSAPE falls from the potential Vcc to the ground potential GND level, and transistor TR1 in sense amplifier activating circuit SAK is turned on. Consequently, the first sense amplifier portion of DRAM sense amplifier DSA is activated, and the bit line of higher potential in the DRAM bit line pair DBL is charged to the level of the operational supply potential Vcc.

At time t5, in accordance with a column selecting signal from DRAM column decoder 15 (see FIG. 7), one column selecting line CSL is selected, and potential of the selected column selecting line CSL rises to "H". Consequently, two pairs of DRAM bit line pairs DBL are connected to local I/O line pairs (LIOa and LIOb) through the column selecting gate CSG. Consequently, potential on the selected DRAM bit line pair DBL is transmitted to local I/O line pair LIO, and potential of local I/O line pair changes from the precharge potential Vcc/2.

At time t6, block activating signal φBA rises to "H" only for the selected row block, and I/O gate IOG is turned on. Consequently, signal potential on local I/O line pair LIO is transmitted to global I/O line pair GIO. "Selected row block" means a row block including the selected word line DWL. Designation of the selected row block is effected by decoding, for example, upper 2 bits of the row address used for selecting the DRAM word line. By such block dividing operation, current consumption can be reduced.

In SRAM, row selecting operation is done by SRAM row decoder 21 (see FIG. 7) at time ts1, one SRAM word line SWL is selected in SRAM array, and potential of the selected SRAM word line SWL rises to "H". Row selecting operation in DRAM and row selecting operation in SRAM are carried out in an asynchronous manner. Data of SRAM cells connected to the SRAM word line SWL are transmitted to corresponding SRAM bit line pair SBL. Consequently, potential of SRAM bit line pair SBL changes from the precharge potential Vcc/2 to potential corresponding to the information stored in the corresponding SRAM cell.

At time t7, data transfer designating signal φTDS attains to and is maintained at "H" for a predetermined time period. Before t7, data of DRAM cell has been already transmitted to the global I/O line pair GIO, and SRAM cells have been connected to SRAM bit line pair SBL. In response to data transfer designating signal φTDS, bi-directional transfer gate BTG is activated and it transmits signal potential on global I/O line pair GIO to the corresponding SRAM bit line pair SBL. Consequently, data are transmitted from DRAM cells to SRAM cells.

Time relation between ts1, t1 and t6 is arbitrary, provided that the time t7 at which data transfer designating signal φTDS is activated is after t6 at which block activating signal φBA rises and after ts1 at which SRAM word line SWL is selected. In this cycle, data transfer designating signal φTSD designating transfer from SRAM to DRAM is kept at inactive state, that is, "L".

At time t8, potential of the selected DRAM word line DWL falls to "L", at time ts2, potential of the selected SRAM word line SWL falls to "L", and various signals are returned to the initial state. Thus, the data transfer cycle from DRAM to SRAM is completed.

As described above, DRAM column decoder 15 (see FIG. 7) selects one column selecting line CSL in each column block 12. One column selecting line CSL selects two pairs of DRAM bit lines DBL. Data transfer from DRAM to SRAM is carried out column block by column block in parallel. Therefore, in the embodiment shown in the figure, 16 bits of data are transferred simultaneously. This relation is realized in a structure having 8 column blocks and in which two pairs of DRAM bit lines are selected in each column block. The number of bits of the data transferred at one time changes dependent on the number of DRAM bit line pairs selected at one time or dependent on the number of column blocks. Therefore, appropriate block size can be set.

(a) Another Transfer Timing From DRAM to SRAM

As shown in FIG. 45, when DRAM word line driving signal DWL falls to "L" of the inactive state approximately at the time t8, data transfer designating signal φTDS falls to "L" in response. At this time t8, local I/O line pair LIO is disconnected from SRAM bit line pair SBL, and DRAM array and SRAM are electrically separated. After the time t8, DRAM portion and SRAM portion can operate independent from each other. Therefore, as shown in FIG. 46, when data transfer designating signal φTDS is made inactive at time t8', the word line driving signal DWL in DRAM array is still maintained at the active state, that is, "H". At this time, the DRAM cannot be newly accessed externally, but SRAM array portion can be externally accessed.

More specifically, as shown in FIG. 46, when data transfer designating signal φTDS falls to "L" at time t8' and even if DRAM array is active at that time, SRAM array can be newly accessed after the lapse of a predetermined time period from time ts2 at which it is set to the standby state. Therefore, after the time t8', SRAM portion can be accessed regardless of the state of DRAM. For example, at time t8', data at a cache miss can be read from SRAM array.

Further, before the DRAM is returned to the standby state, SRAM can be accessed by newly setting an external address. The reason for this is that RAS precharging operation necessary for a DRAM is not necessary for the SRAM and the SRAM can be accessed at high speed after the return to the standby state.

Referring to FIG. 46, DRAM word line driving signal DWL falls to "L" at time t9'. When equalize signal φEQ is activated at time t10, equalize and precharge operations of DRAM bit line pair DBL is started. At this time, equalizing operation of sense amplifier driving signal lines φSAN and/φSAP is also carried out. DRAM together with peripheral circuits thereof are returned to the standby state at a time t11 after several tens nsec from time t9'. The DRAM array cannot be accessed until a predetermined RAS precharge time period has lapsed. However, in SRAM array, at time ts3 after several nsec from time ts2 at which the SRAM word line SWL1 is set to the non-selected state, it is possible to select a different SRAM word line SWL2 in accordance with an external address and to access (read data from or write data to) memory cells connected to the selected SRAM word line SWL2.

Time interval between ts2 at which data transfer designating signal φTDS falls to the inactive state "L" and ts3 at which SRAM word line SWL2 can be activated is set at an appropriate value by external specification. Since access to the SRAM is made possible before DRAM is returned to the standby state, a semiconductor memory device especially a

semiconductor memory device containing a cache which operates at high speed, can be provided.

Since it is not necessary in SRAM to carry out column selecting operation after the sensing and latch operation of the sense amplifier as in the DRAM, a very short time period is enough for the selecting period of the word line SWL2 in SRAM. At time ts4, access to the SRAM is completed. In a normal SRAM, the time period from ts3 to ts4 is about 10 nsec at the most. Access to the SRAM is completed during the standby state of the DRAM. The structure enabling access to the SRAM before the DRAM array is returned to the standby state is realized by the semiconductor memory device of the present invention in which SRAM and DRAM can be accessed by designating addresses, which addresses are independent from each other.

(b) Data Transfer From SRAM to DRAM

FIG. **47** is a diagram of signal waveforms showing operations in data transfer from SRAM to DRAM. The data transfer operation from SRAM to DRAM will be described with reference to FIGS. **7**, **8** and **47**. The operation in the DRAM portion from t1 to t6 is the same as that in data transfer from the DRAM to SRAM shown in FIG. **45**. As to the operation of the SRAM portion, potential of SRAM word line SWL rises to "H" at time ts1, as in the signal waveform of FIG. **45**.

After the time ts1 and t6, that is, after DRAM bit line pair DBL is connected to global I/O line pair GIO and SRAM cells (SMCS) are connected to SRAM bit line pair SBL, data transfer designating signal φTSD is activated and rises to "H" for a predetermined time period after t7. In response, bi-directional transfer gate BTG is activated and transmits signals on SRAM bit line pair SBL to DRAM bit line pair DBL through global I/O line pair GIO (GIOa, GIOb) and through local I/O line pair LIO (LIOa, LIOb). Consequently, data of the DRAM cells connected to the selected DRAM bit line pair DBL are rewritten. Namely, data in the SRAM cells are transferred to the DRAM cells. In the data transfer cycle from SRAM array to DRAM array, data transfer designating signal φTDS is maintained at inactive state, that is, "L".

The data transfer operation shown in FIGS. **45** to **47** is effected when a cache miss occurs with the SRAM array used as a cache. More specifically, when data to which access is requested by a CPU, which is an external processing unit, is not stored in the SRAM array, necessary data is transferred from DRAM array to SRAM array. At a cache miss, a copy back operation for transferring data from SRAM array to DRAM array as well as block transfer for transferring desired data from DRAM array to SRAM array are carried out. Copy back operation and block transfer operation will be described in the following.

Referring to FIG. **48**A, let us assume that data D2 to which access is requested by the CPU is not stored at a corresponding position of the SRAM. Data D1' is stored at the corresponding position of the SRAM, that is, the cache. When the cache miss of the SRAM occurs, the DRAM is still at a precharge state.

Referring to FIG. **48**B, in response to a cache miss designating signal, a word line (shown by hatched portion) including the region to which data D1' is to be stored is selected in the DRAM. This is an array active state. In the SRAM, the region of the data D1' has been selected.

Referring to FIG. **48**C, transfer designating signal φTSD is generated, and data D1' of the SRAM is transmitted to the corresponding region of the selected word line of the DRAM. Consequently, data D1' is stored in the data region D1 of the DRAM.

Referring to FIG. **48**D, after the completion of transfer of data D' to the data region D1 of the DRAM, the DRAM array is returned to the precharge state.

Referring to FIG. **48**E, a word line (shown by a hatching) including data D2 to which access is requested by CPU is selected in the DRAM.

Referring to FIG. **48**F, data D2 included in the selected word line is transmitted to the corresponding region of the SRAM array in response to data transfer designating signal φTDS. Consequently, data D1 of the SRAM array is rewritten by data D2. The copy back operation corresponds to the FIGS. **48**A to **48**D, and the block transfer mode corresponds to FIG. **48**D to FIG. **48**F. The step shown in FIG. **48**D is included in both cycles, since the precharge period of the DRAM is considered to be included in both cycles, when these two operations are carried out successively.

(c) Fast Copy Back Mode Operation

In this above method of data transfer, a precharging period of the DRAM array is interposed, and direction of data transfer is always one way. Therefore, data transfer between SRAM array and DRAM array can not be carried out at high speed. Data transfer operation carried out at a higher speed by overlapping data transfer to and from DRAM array and SRAM array will be described in the following.

FIG. **49** is a block diagram schematically showing another structure of a data transfer device. A circuit portion for transferring data of 1 bit between SRAM array and DRAM array in the data transfer device is shown in FIG. **49**. The data transfer device includes 16×4 of the bi-directional transfer gate circuits shown in FIG. **49**. In the following, the data transfer device shown in FIG. **49** is referred to as a bi-directional transfer gate circuit for transferring data of 1 bit.

Referring to FIG. **49**, the bi-directional transfer gate circuit includes a gate circuit **1810** responsive to transfer control signal φTSL for connecting SRAM bit line pair SBLa and *SBLa to a latch circuit **1811**; a gate circuit **1812** responsive to transfer control signal φTLD for transmitting data latched in latch circuit **1811** to global I/O lines GIOa and *GIOa; and a gate circuit **1813** responsive to DRAM write enable signal AWDE and to SRAM column decoder output SAY for transferring data on write data bus lines DBW and *DBW to global I/O lines GIOa and *GIOa. An output SAY of SRAM column decoder selects 1 bit out of 16 bits which has been simultaneously selected in DRAM array block. Therefore, a structure in which lower 4 bits of a column address signal for DRAM array are applied to SRAM column decoder is shown as an example.

The bi-directional transfer gate circuit further includes an amplifier circuit **1814** which is activated in response to transfer control signal φTDS for activating data on global I/O lines GIOa and *GIOa; and a gate circuit **1815** responsive to transfer control signal φTDS for transferring data amplified by the amplifier circuit **1814** to SRAM bit line pair SBLa and *SBLa.

Gate circuit **1810** and latch circuit **1811** constitute first transfer means, gate circuit **1815** and amplifier circuit **1814** constitute second transfer means, and gate circuit **1812** and gate circuit **1813** constitute a third transfer means.

SRAM write enable signal AWDE is generated upon occurrence of a cache miss in an array access cycle when CPU requests data writing. More specifically, it is generated from a transfer gate control circuit **262**, which will be described later, when a chip select signal E# attains "L", cache hit signal CH# is "H" and write enable signal W# is "L" at a rising edge of a clock signal K.

When data is to be written to DRAM array by gate circuit **1813**, write data can be directly transmitted to global I/O lines GIOa and *GIOa, not through SRAM bit line pair SBLa and *SBLa. Consequently, data can be written at a

higher speed. Gate circuit **1812** is used for adjusting timing, when 64 bits (in the case of 4 MCDRAM) of data are to be simultaneously transferred from SRAM array to DRAM array in response to transfer control signal φTLD. Similarly, gate circuit **1815** is used for adjusting timing when 64 bits of data are to be simultaneously transferred from DRAM array to SRAM array.

FIG. **50** shows an example of a specific structure of the bi-directional transfer gate circuit shown in FIG. **49**.

Gate circuit **1810** includes n channel MOS transistors **T102** and **T103** for amplifying signal potential on SRAM bit line pair SBLa and *SBLa, and n channel MOS transistors **T100** and **T101** which are rendered conductive in response to transfer control signal φTSL for transmitting data amplified by transistors **T102** and **T103** to a latch circuit **1811**. Transistor **T102** has its gate connected to SRAM bit line SBLa, one conduction terminal connected to the ground potential Vss and the other conduction terminal connected to one conduction terminal of transistor **T100**. Transistor **T103** has its gate connected to SRAM bit line *SBLa, one conduction terminal connected to the ground potential Vss and the other conduction terminal connected to one conduction terminal of transistor **T101**.

Latch circuit **1811** includes inverter circuits **HA10** and **HA11** having their inputs connected to the outputs of each other. Inverter circuits **HA10** and **HA11** constitute an inverter latch. Latch circuit **1811** further includes inverter circuits **HA12** and **HA13** for inverting latched data of the inverter latch (inverter circuits **HA10** and **HA11**).

Gate circuit **1812** includes a gate circuit **1812*b*** for transmitting data to global I/O line GIOa, and a gate circuit **1812*a*** for transmitting data to global I/O line *GIOa. Gate circuit **1812*a*** is formed by an n channel MOS transistor **T105** and gate circuit **1812*b*** is formed by an n channel MOS transistor **T106**. Transfer control signal φTLD is applied to the gates of the transistors **T105** and **T106**.

Amplifier circuit **1816** includes an n channel MOS transistor **T113** for amplifying potential on global I/O line *GIOa, an n channel MOS transistor **T112** which is turned on in response to transfer control signal φTDS for transmitting data amplified by transistor **T113** to node **N100**, a p channel MOS transistor **T111** responsive to transfer control signal TDS for precharging node **N110** to a supply potential Vcc, and a p channel MOS transistor **T110** which is connected in parallel to transistor **T211** between power supply Vcc and a node **N100**.

Amplifier circuit **1814** further includes an n channel MOS transistor **T117** for amplifying signal potential on global I/O line GIOa, an n channel MOS transistor **T116** which is turned on in response to transfer control signal φTDS for transmitting signal potential on global I/O line GIOa amplified by transistor **T117** to node **N110**, a p channel MOS transistor **T114** responsive to transfer control signal φTDS for precharging node **N110** to supply potential Vcc, and a p channel MOS transistor **T115** which is connected in parallel to transistor **T214** between power supply Vcc and node **N110**.

Transistor **T110** has its gate connected to node **N110**, and transistor **T115** has its gate connected to node **N100**. Transistors **T110** and **T115** constitute a differential amplifying circuit.

Gate circuit **1815** includes a gate circuit **1815*a*** for transferring data to SRAM bit line SBLa, and a gate circuit **1815*b*** for transferring data to SRAM bit line *SBLa. Gate circuit **1815*a*** includes an n channel MOS transistor **T120** which is turned on in response to transfer control signal φTDS for transmitting signal potential on node **N100** to SRAM bit line SBLa. Gate circuit **1815*b*** includes an n channel MOS transistor **T111** which is turned on in response to a transfer control signal φTDS for transmitting signal potential on node **N110** to SRAM bit line *SBLa.

Gate circuit **1813** includes a gate circuit **1813*a*** for transmitting signal potential on internal data bus line *DBW to global I/O line *GIOa and a gate circuit **1813*b*** for transmitting signal potential on internal data bus line DBW to global I/O line GIOa. Gate circuit **1813*a*** includes an n channel MOS transistor **T130** which is turned on in response to an output SAY from SRAM column decoder, and an n channel MOS transistor **T131** which is turned on in response to DRAM write enable signal AWDE. Transistors **T131** and **T130** are connected in series between internal write data bus line *DBW and global I/O line *GIOa.

Gate circuit **1813*b*** includes an n channel MOS transistor **T132** which is turned on in response to output SAY of SRAM column decoder, and an n channel MOS transistor **T133** which is turned on in response to SRAM write enable signal AWDE. Transistors **T132** and **T133** are connected in series between internal data bus line DBW and global I/O line GIOa. The operation of the bi-directional transfer gate circuit will be described in the following.

Referring to FIG. **51**, data transfer operation in a cache miss writing operation will be described. In a cache miss writing, chip select signal E# and write enable signal W# both attain to "L" and cache hit signal CH# attains to "H" at a rising edge of clock signal K (as will be described in detail later). In response, DRAM and SRAM are both activated. An address applied to SRAM and DRAM at this time is applied from CPU.

At time **t1**, precharge cycle is completed in DRAM, and a memory cycle is started. In response, equalize signal #EQ rises to an inactive state "L". By the time a DRAM word line DWL is set to a selected state in DRAM, signal potential on internal data bus line DBW has been established to a value corresponding to write data. When a DRAM word line DWL is selected and signal potential on DRAM bit line pair DBL is changed at time **t2**, sense amplifier activating signals φSAN and/φSAP are activated at times **t3** and **t4**, and signal potential on each DRAM bit line pair attains to a value corresponding to the read memory cell data.

In SRAM, a SRAM word line SWL is selected at time **ts1**. Data of memory cells connected to the selected word line SWL are transmitted to a corresponding SRAM bit line SBLa (*SBLa). When signal potential on SRAM bit line SBLa (*SBLa) is established, transfer control signal φTSL rises to "H", gate circuit **1810** is opened, and signal potential on SRAM bit lines SBLa and *SBLa are transmitted to latch circuit **1811**. More specifically, in the circuit structure shown in FIG. **50**, transistors **T100** and **T101** are turned on, one of transistors **T102** and **T103** is turned on and the other thereof is turned off, and the potential "L" is transmitted through the transistor (**T102** or **T103**) which is on to latch circuit **1811**. Latch circuit **1811** latches the applied signal potential "L" at a corresponding node.

In DRAM, in parallel to the data latch operation of the latch circuit **1811**, column selecting line CSL is selected (time **t5**), and in response, potential on local I/O line pair LIO is established. Then, by the block selecting signal φBA, potential on local I/O line pair LIO is transmitted to global I/O line pair GIO (**t6**).

When signal potential on global I/O line pair GIO is established, DRAM write enable signal AWDE rises to "H". At this time, output signal SAY from SRAM column decoder is set to an active state, and gate circuit **1813** provided for one global I/O line out of 16 bits is opened.

Consequently, write data appeared on data bus lines DBW and *DBW are transmitted to global I/O lines GIOa and *GIOa through gate circuits 1813*b* and 1813*a*.

When signal potential on global I/O line pair GIO has reached a value corresponding to write data at time t7, transfer control signal φTDS rises to "H" at time t7'. In response, transistors T111 and T114 are turned off, precharging of nodes N100 and N110 is stopped, and transistors T110 and T115 differentially amplify signal potential on global I/O lines GIOa and *GIOa which have been transmitted through transistors T112 and T116. Consequently, signal potential on nodes N100 and N110 attains to the potential which is the inversion of the signal potential on global I/O lines *GIOa and GIOa.

For example, let us assume that signal potential on global I/O line GIOa is "H" and that the signal potential on global I/O line *GIOa is "L". At this time, transistor T117 is turned on, and transistor T113 is turned off, potential at node N110 attains to "L" and potential at node N100 attains to "H". The potential "L" at node N110 turns transistor T110 on, and potential "H" at node N100 turns transistor T115 off. By the transistors T110 and T115, signal potentials on nodes N100 and N110 are differentially amplified and latched.

In parallel to the amplifying operation in amplifying circuit 1814, gate circuits 1815*a* and 1815*b* are rendered conductive in response to a rise to "H" of transfer control signal φTDS, signal potential on node N100 is transmitted to SRAM bit line SBLA, and signal potential on node N110 is transmitted to SRAM bit line *SBLa. At this time, since transfer control signal φTLD is fixed at "L", gate circuits 1812*a* and 1812*b* are closed, and data latched in latch circuit 1811 is not transmitted to global I/O lines GIOa and *GIOa.

In DRAM array, write data transmitted to global I/O line pair GIO is transmitted to DRAM bit line pair DBL through local I/O line pair LIO.

At time t8, memory cycle of DRAM is completed, and precharge period is started. At time t9, a standby state for waiting the next cycle is started.

In SRAM, potential on SRAM word line SWL falls to "L" at time ts2, and thus one cycle is finished.

As described above, in a cache miss writing operation, by writing write data to a corresponding memory cell of the DRAM array and by transmitting the data changed by the external write data to the SRAM array, writing of data to the memory cell in SRAM is completed when one data transfer cycle is completed, and therefore even at a cache miss, data can be written at a high speed.

The above described data transfer operation (hereinafter referred to as a high speed copy back mode) is schematically shown in FIGS. 52A through 52D. Data transfer operation in high speed copy back mode at a cache miss writing operation will be described with reference to FIGS. 52A through 52D.

Let us assume that CPU generates a request for rewriting data D2 by D. At this time, at that region of the SRAM to which access is requested by the CPU, data D1' has been stored, and data D2 is stored in DRAM array (FIG. 52A).

When such a cache miss writing occurs, first, in SRAM, data D1' is transferred to a latch (latch circuit 1811). In parallel to this transferring operation, in DRAM, a word line (hatched portion) including data D2 is selected in accordance with an access from CPU, and write data D is transmitted to the region storing data D2 connected to the selected word line (FIG. 52B). Consequently, data D2 in DRAM is replaced by D2'.

Thereafter, data D2' rewritten by the external write data D is transferred to that region of the SRAM to which access is requested by the CPU. Therefore, the region of the SRAM which has stored data D1' is rewritten by data D2' (FIG. 52C). Therefore, data rewritten by data D2 is stored in that region of the SRAM to which access is requested by the CPU. After the completion of this transfer, DRAM is set to the precharge state. At this state, SRAM can be accessed (see FIG. 52D).

Thereafter, transfer of data D1 stored in the latch to region D1 of DRAM is carried out. Transfer operation of the data D1' latched in latch 1811 to DRAM array will be described.

FIG. 53 is a diagram of signal waveforms showing data transfer operation from SRAM to DRAM. Referring to FIG. 53, at time t1, an array access request is made, and an address for designating a region in which data D1' is to be stored is applied (for example, output from a tag memory). From t1 to t6, selection of a DRAM word line DWL, detection and amplification of memory cell data connected to the selected word line are carried out in the same manner as shown in FIG. 51, and data on local I/O lines and on global I/O lines are established.

At time t7, transfer control signal φTLD is generated, and gate circuit 1812 shown in FIG. 49 is opened. Namely, referring to FIG. 50, transistors T105 and T106 are turned on, and data latched in latch circuit 1811 is transmitted to global I/O line GIOa and *GIOa. Data transmitted to global I/O line GIOa (*GIOa) is transmitted to DRAM bit line DBL (*DBL) selected by a column selecting line CSL through a local I/O line LIOa (*LIOa). The transfer operation of data D1 from SRAM to DRAM is completed.

During transfer operation of data latched in latch circuit 1811 to DRAM (copy back operation), SRAM can be arbitrarily accessed. More specifically, the address applied to DRAM at this time is independent from the address applied to SRAM. (Since simultaneous transfer of 16 bits×4 bits of data is carried out in DRAM at the copy back transfer), selecting operation can be done by SRAM column decoder in accordance with a SRAM address signal Ac. At this time, since transfer control signal φTDS is at "L" and transfer control signal φTSL is also at "L", gate circuits 1815 and 1810 are both closed, and therefore, DRAM array is separated from SRAM array. SRAM array can be independently accessed without any influence of data transfer operation to the DRAM array.

FIG. 54 schematically shows data transfer operation from latch circuit to DRAM. Referring to FIG. 54A, data D1' is stored in the latch. In the DRAM, a word line (hatched portion) including a region for storing data D1 is selected in accordance with an external address (applied from a tag memory or the like).

Thereafter, data D1' latched in the latch is transferred to the region D1 included in the selected word line, and data in this region is changed to D1' (FIG. 54B). Consequently, data transfer from the latch to the DRAM is completed.

The operation at a cache miss reading will be described. The operation in the cache miss reading is the same as the operation of the cache miss writing described above, except that the DRAM write enable signal AWDE is at "L" and the gate circuit 1813 is closed. In this operation, as shown in the diagram of waveforms of FIG. 55, word lines SWL and DWL are selected in the SRAM array and the DRAM array. Data of the SRAM array is latched by latch circuit 1811, and data from the DRAM array is transmitted to SRAM bit line SBLa (*SBLa) at time t7. After the data transfer to SRAM at t7, precharging operation is not necessary in SRAM. Therefore, the transferred data can be immediately read. Namely, at a time of a cache miss, data writing operation and data reading operation can be executed in the same cycle

time. Data transfer operation from latch circuit **1811** to DRAM is the same as the operation at the time of cache miss writing described above (see FIGS. **53** and **54**).

Let us assume that data D1' is stored in that region of the SRAM array which is designated by an address from the CPU, and that CPU requests data D2. At this time, DRAM and SRAM are at the standby state (FIG. **56**A).

If such a cache miss occurs, first a SRAM word line is selected in SRAM, and data D1' is transferred to the latch (latch circuit **1811**). In parallel to the latching operation, a word line (hatched portion) including data D2 is selected in the DRAM in accordance with an address from the CPU (FIG. **56**B).

Thereafter, data D2 included in the selected word line of the DRAM is transferred to the region of the SRAM in which the data D1' has been stored, through amplifier circuit **1814** and gate circuit **1815**. The latch circuit **1811** keeps the data D1' latched. In the SRAM, data D2 which has been transferred from DRAM can be immediately read (FIG. **56**C).

After the data transfer from DRAM to SRAM, the DRAM is temporarily set to a precharge state, so as to replace data D1 by data D1'. The region storing the data D1 is that region in which the data D1' which has been stored in the SRAM is to be stored (FIG. **56**D).

After the completion of precharging in the DRAM, a word line (hatched portion) including data D1 is selected (FIG. **56**E). In the word line selecting cycle (array active cycle), the SRAM can be externally accessed.

To the region storing data D1 included in the selected word line of the DRAM, the data D1' which has been latched in the latch (latch circuit **1811**) is transferred. Consequently, data D1 in the DRAM is rewritten by the data D1' which has been stored in the SRAM (FIG. **56**F).

The externally applied address means, in the DRAM, an address from the CPU when a word line is selected in data transfer to SRAM. It means an address from, for example, an external tag memory, when a word line is selected for receiving data from the latch circuit.

FIG. **57** schematically shows a further structure of a bi-directional data transfer device. FIG. **57** shows a bi-directional transfer gate circuit related to transfer of 1 bit of data in the bi-directional data transfer device, as does FIG. **49**. In FIG. **57**, the same or corresponding portions are denoted by the same reference numerals as in FIG. **49**.

Referring to FIG. **57**, the bi-directional transfer gate circuit includes, in addition to the structure of the bi-directional data transfer circuit shown in FIG. **49**, a gate circuit **1817** which is provided between SRAM bit line pair SBLa, *SBLa and internal write data transmitting lines DBW, *DBW. Gate circuit **1817** is opened in response to an output SAY of SRAM column decoder and to SRAM write enable signal SWDE. SRAM write enable signal SWDE is generated at data writing to SRAM, and it is generated when the write enable signal W# is at an active state, that is, "L", either at a cache hit or at a cache miss.

FIG. **58** shows an example of a specific structure of the bi-directional transfer gate circuit shown in FIG. **57**. Referring to FIG. **58**, gate circuit **1817** includes a gate circuit **1817***a* for transmitting write data on internal write data bus line DBW to SRAM bit line SBLa, and a gate circuit **1817***b* for transmitting write data on write data bus line *DBW to SRAM bit line *SBLa. Gate circuit **1817***a* includes an n channel MOS transistor **T141** which is turned on in response to the output SAY from SRAM column decoder, and an n channel MOS transistor **T140** which is turned on in response to SRAM write enable signal SWDE.

Gate circuit **1817***b* includes an n channel MOS transistor **T143** which is turned on in response to the output SAY of SRAM column decoder, and an n channel MOS transistor **T142** which is turned on in response to SRAM write enable signal SWDE. Both of the gate circuits **1817***a* and **1817***b* transmit data on internal data bus lines DBW and *DBW to SRAM bit lines SBLa and *SBLa when the SRAM column decoder output SAY and SRAM write enable signal SWDE are at the active state, that is, "H". Other structures are the same as those shown in FIG. **50**. Data transfer from DRAM to SRAM in cache miss writing will be described with reference to FIG. **59**, which is a diagram of signal waveforms.

The operation up to the time t7 is the same as that of the bi-directional transfer gate circuit shown in FIGS. **49** and **50**. Data from the SRAM has been latched in the latch circuit **1811**, and memory cell data from the DRAM array has been transmitted to global I/O line GIOa (*GIOa).

When transfer control signal φTDS rises to "H" at time t7, amplifier circuit **1814** and gate circuit **1815** operate to amplify signal potentials on the global I/O lines GIOa and *GIOa and transmit the same to SRAM bit line pair SBLa and *SBLa. In parallel to this transfer operation, DRAM write enable signal AWDE rises to "H", gate circuit **1816** is opened, and write data on write data lines DBW and *DBW are transmitted to global I/O lines GIOa and *GIOa. Consequently, write data is written to the memory cell selected in the DRAM array.

In parallel to the data transfer operation from the DRAM to the SRAM in response to transfer control signal φTDS, SRAM write enable signal SWDE rises to "H", gate circuit **1817** (**1817***a*, **1817***b*) is opened, and write data on the write data bus lines DBW and *DBW are transmitted to SRAM bit lines SBLa and *SBLa. Consequently, signal potentials on the SRAM bit lines SBLa and *SBLa are established at signal potentials corresponding to the value of the write data.

The DRAM write enable signal AWDE and SRAM write enable signal SWDE may be generated at any time after the generation of transfer control signal φTDS and after the start of data transfer operation from DRAM to SRAM.

In the structure of the bi-directional transfer gate circuit shown in FIGS. **57** and **58**, write data on the internal write data bus line is directly transmitted to SRAM bit lines SBLa and *SBLa through the gate circuit **1817**. Therefore, when writing to data in the SRAM is effected by transferring write data from internal data bus lines DBW and *DBW to DRAM, and then transmitting write data from DRAM to the SRAM, and if the access time of DRAM is relatively short, there is a possibility that data rewritten by the write data cannot be surely transmitted to the SRAM, since there is not always sufficient time for transmitting write data through such path. In that case, a structure in which data is directly transmitted from internal write data bus lines DBW and *DBW to the SRAM bit lines SBLa and *SBLa through gate circuit **1817** enables transmission of data which is surely rewritten by the write data to the SRAM.

FIGS. **60**A through **60**D schematically show data transfer operation from the DRAM to the SRAM by the bi-directional transfer gate circuit shown in FIGS. **57** and **58**. The data transfer operation will be briefly described with reference to FIGS. **60**A through **60**D.

As in FIG. **60**A, let us assume that CPU requests rewriting of data D2. DRAM and SRAM are both at the precharge state (FIG. **60**A).

Referring to FIG. **60**B, a word line (hatched portion) including data D2 is selected in the DRAM, while in the SRAM, data of the region including data D1' are transmitted

to the latch. The data D1' is not to be rewritten but it should be transferred to that region of the DRAM in which the data D1 is to be stored.

Referring to FIG. 60C, while data D2 of the DRAM is being transferred to a corresponding memory cell of the SRAM, write data D is transferred to the region of the DRAM to which data D2 is to be stored, and also to that region of the SRAM to which data D1 is to be stored. Consequently, data D2 in the DRAM and in the SRAM are changed to data D2' which has been rewritten by the write data D. Namely, in parallel to data transfer from the DRAM to SRAM, write data D is written to SRAM, and data writing is carried out in DRAM.

Referring to FIG. 60D, the DRAM is returned to a precharge state, so as to transfer the latched data D1' to the region for storing the data D1 in the DRAM. In this state, CPU can access SRAM.

Transfer operation of the data D1' latched in the latch (latch circuit 1811) to data D1 storing region of the DRAM is the same as that described with reference to FIG. 54. Therefore, it is not repeated.

In the bi-directional data transfer circuit shown in FIGS. 57 and 58, gate circuits 1816 and 1817 are both opened in cache miss writing. Therefore, the same operation as the data transfer operation described with reference to the bi-directional transfer gate circuit shown in FIGS. 49 and 50 is carried out, namely, only the data transfer operation schematically shown in FIGS. 56A to 56F is carried out. Therefore, the description thereof is not repeated.

By providing such a gate circuit 1817 as described above, even if there is not a sufficient time for rewriting data in the DRAM by write data D and then transmitting the rewritten data to the SRAM, data in the SRAM can be surely rewritten by the write data D.

A so-called "write through mode" is available in the above described bi-directional data transfer device. In the "write through mode", data written to the SRAM is also written to the corresponding memory cell of the DRAM at that time during cache access. Namely, if the above described cache miss writing operation is executed at a cache hit when data exists in the SRAM, the write through is enabled. In cache miss writing operation when data does not exist in the cache, the above described cache miss writing operation may be done without modification for directly writing data to the DRAM array.

When the DRAM is to be directly accessed, data can be directly written to the DRAM by activating only the DRAM write enable signal AWDE. When data is to be written only to the SRAM at a time of a cache hit and it is not necessary to execute the write through mode operation, only the SRAM write enable signal SWDE is set to the active state.

When data transfer is carried out by using the data transfer device shown in FIGS. 49 and 50 or FIGS. 57 and 58, only one precharge period is necessary in the DRAM for receiving the latched data, and therefore data transfer can be carried out at a high speed between the SRAM and the DRAM. In the conventional copy back and block transfer mode cycles, the SRAM cannot be accessed before the completion of block transfer. However, by using the high speed copy back mode, data transfer from the DRAM to the SHAM is carried out in the first data transfer cycle, namely, the conventional block transfer is carried out at first, so that after the data transfer to the SRAM, the SRAM can be directly accessed. Therefore, a semiconductor memory device containing a cache having higher speed of operation can be realized.

In the bi-directional data transfer device, rewriting of data to SRAM is carried out in parallel to data transfer. Therefore, operations in cache miss reading and cache miss writing can be executed in the same cycle time.

In the foregoing, the high speed copy back mode is applied to data transfer between SRAM array and DRAM array at a cache miss in a semiconductor memory device containing a cache, as an example. However, high speed exchange of data is also made possible when data are transferred between two memory cells such as a normal SRAM array and a DRAM array, and efficiency in data transfer can be significantly improved. Namely, the bi-directional data transfer device can be applied not only to a semiconductor memory device containing a cache such as shown in FIG. 32 but also to a semiconductor memory device having a general high speed memory and a memory of large capacity, as a data transfer device between the high speed memory and large capacity memory.

(c) Data Transfer Between DRAM Array and SRAM Array With Reduced Current Consumption

(i) In the arrangement with clamping transistors as shown in FIGS. 24 and 30, data can be transferred between DRAM array and SRAM array because of the reduced logical swing of the potentials of SRAM bit lines. This clamping transistor arrangement can be expanded more generally to achieve high speed data transfer operation with less current consumption. Now, data transfer operation with modified clamping transistor arrangement will be described with reference to FIGS. 61 through 70.

FIG. 61 shows an array structure for fast data transfer with reduced current consumption. The arrangement of FIG. 61 is the same as that of FIG. 8 except that clamping circuits CRS are provided for respective SRAM bit line pairs SBL, and clamping circuits CRD for clamping DRAM IO lines are provided. The SRAM clamping circuit has the same construction as that of FIG. 21, that is, diode-connected transistors provided for each SRAM bit line.

DRAM clamping circuits CRD includes a clamp circuit CRDa provided for the global IO line pair GIOa and a clamping circuit CRDb provided for the global IO line pair GIOb. Clamping circuits may be provided for the local IO line pairs LIOa and LIOb. The clamping circuits may be provided both for the global IO line pairs GIOa and GIOb and for the local IO line pairs LIOa and LIOb.

The SRAM array of FIG. 61 is shown having one word line per one row of SRAM cells, but it may have the multiplicate word line arrangement of a plurality of word lines per one row of SRAM cells as shown in FIG. 24.

The bidirectional data transfer gate circuit 3 includes bidirectional transfer gates BIGa and BIGb provided between SRAM bit line pairs SBL and the global IO line pairs GIOa and GIOb. The bidirectional transfer gates BIGa and BIGb carry out data transfer between SRAM bit line pairs and the global IO lines GIOa and GIOb in response to data transfer instructing signals DIS and DIA. The signal DIS instructs data transfer from DRAM array to SRAM array. The signal DIA instructs data transfer from SRAM array to DRAM array.

SRAM clamping circuit CRS is enabled and disabled in response to a signal/DTS which is an inversion signal of the signal DTS. DRAM clamping circuits CRD is enabled and disabled in response to a signal/DTA which is an inversion signal of the signal DTA.

In data transfer from DRAM array to SRAM array, the transfer instructing signal DTS is activated to be "M" to disable the SRAM clamping circuit CRS to inhibit the bit line clamping in SRAM array. In data transfer from SRAM array to DRAM array, the transfer instructing signal DTA is activated to be "H" to disable the clamping circuits CRDa and CRDb (and/or CRDa' and CRDb').

FIG. 62 shows a construction related to a data transfer gate of FIG. 61. In FIG. 62, the global IO line pair LIO and the global IO line pair GIO are shown combinedly as DRAMIO line pair DIO. The global IO line pair is provided only for one memory block while the global IO line pair is provided commonly for the memory blocks in a column block (see FIGS. 7 and 8). Therefore, the clamping circuit CRD is preferably provided at least for the global IO line pair GIO. The arrangement of FIG. 60 includes the block selection gates IOGa and IOGb. However, the global IO line pair GIO and the local IO line pair LIO are combinedly shown as DRAMIO line pair DIO. Accordingly, block selection gate IOG and column selection gate CSG of FIG. 60 is combinedly shown as a selection gate SG.

Only the DRAMIO line pair DIO connected to one bidirectional transfer gate BIG is shown in FIG. 62, and therefore the column selection signal CSL transferred on the column selecting line CSL is shown selecting one selection gate SG in FIG. 62.

DRAM bit line pair DBL includes bit lines DBL and *DBLa, and SRAM bit line pair SBL includes bit lines SBLa and *SBLa. DRAM bit lines DBLa and *DBLa representatively show pairs of bit lines DBLaO, *DBLaO through DBLan, *DBLan. SRAM array also includes word lines SWLo through SWLn, and DRAM array includes word lines DWLo through DWLp.

SRAM clamping circuit CRS includes n channel MOS transistor SQ70 for the SRAM bit line SBLa and n channel MOS transistor SQ80 for the SRAM bit line *SBLa. The transistors SQ70 and SQ80 receive the inversion signal/DIS at their gates.

DRAM clamping circuit CRD includes n channel MOS transistor DQ70 for DRAMIO line DIOa and n channel MOS transistor SQ80 for DRAMIO line *DIOa. The inversion signal/DTA is applied to the gates of the transistors DQ70 and DQ80.

(ii) Various constructions can be applied for the data transfer gate. First, the bidirectional transfer gate as shown in FIG. 63 is considered. The gate of FIG. 63 is the same as the gate of FIG. 44 except for the naming of the components and the signal. Therefore, no detailed explanation is described of the gate of FIG. 63. Now, an operation in transferring data from DRAM array to SRAM array with reference to FIG. 63 showing the operating waveform diagram therefor. Data transfer from DRAM array to SRAM array is effected in the cache miss where the signal CI is active at "H".

Before time t1, the precharge instructing signal ϕEQ is active at "H", and therefore, the equalizing transistors TEQ equalize the sense amplifier driving signal lines SAN and /SAP to the precharge potential of Vcc/2. The DRAM bit line pair DBL (bit lines DBLa, *DBLa) are precharged to the intermediate potential of Vcc/2 by the precharge/equalize circuit DE.

DRAMIO lines DIOa and *DIOa are precharged to "H" at the potential level of Vcc-Vth by the clamping circuit CRD. SRAM bit liens SBLa and *SBLa are precharged to "H" at the potential level of Vcc-Vth by the clamping circuit CRS.

At time t1, the precharge instructing signal ϕEQ falls to "L" to disable the equalizing transistors TEQ and precharge/equalize circuit DE, which completes the precharging of the sense amplifier driving signal lines SAN and /SAP, and the DRAM bit lines DBLa and *DBLa. DRAM bit lines DBLa and *DBLa, and the sense amplifier driving signal lines SAN and /SAP are brought into a floating state at the intermediate potential Vcc/2.

Then, row decoder 14 (see FIG. 9) carries out a row selection operation in accordance with an externally applied address.

After a certain time has elapsed from the time t1, one word line DWL is selected in DRAM array, and the potential of the selected word line DWL (one of the word lines DWLo to DWLp) rises to "H". DRAM memory cells DMC connected to the selected word line DWL are connected to associated DRAM bit lines DBLa (or *DBLa) whose potentials are changed in accordance with data of the associated memory cells.

FIG. 64 shows the DRAM bit line potential change when a memory cell storing "H" data is selected.

At time t2, a sense amplifier activating signal SANE rises from the ground potential to the operating power supply Vcc, to turn on the transistor TR2 in the sense amplifier activating circuit SAK. Consequently, the sense amplifier driving signal SAN falls from the intermediate potential level Vcc/2 to the ground potential, to activate the N sense amplifier part in the DRAM sense amplifier DS. Potential of the bit line of a lower potential in a DRAM bit line pair is discharged to the ground potential level Vss.

At time t3, the sense amplifier activating signal/SAPE falls from the Vcc level to Vss level, to turn the transistor TR1 in the sense amplifier activating circuit SAK. Responsively, the sense amplifier driving signal/SAP rises from the intermediate potential Vcc/2 to the supply potential Vcc. Then, D sense amplifier part in DRAM sense amplifier DSA is activated to boost the potential of a bit line of a higher potential in the pair to the supply potential level Vcc.

At time t4, the column selection signal CSL is generated by the decoding in the column decoder 15 (see FIG. 9). Then, a selected gate SGi is make conductive to connect and associated DRAM bit line pair (DBLia, *DBLia) to DRAMIO line pair DIO (DIOa, *DIOa). DRAM sense amplifier DSA has a larger driving ability than the current supplying ability of the clamping circuit CRD. Consequently, the potentials of DRAMIO line pair correspond to the potential levels of "H" and "L" amplified by the sense amplifier DSA.

In this operation, "L" level of DRAMIO line pair DIO is slightly higher than the ground potential because the clamping circuit CRD supplies current flow to implement the pull-up function. The "L" level potential is determined by the current driving abilities of the clamping transistors SQ70 and SQ80, the transistor of the selection gate SGi and the discharging transistors (n channel MOS transistors; see FIG. 8) in DRAM sense amplifier DSA. The selection gate SGi has a relatively high resistance, and the logical swing of the DRAMIO line DIOa (*DIOa) is determined by the ratio of on resistances of the clamping transistor DQ70 (or DQ80) and the transistor of the selection gate SGi. DRAM bit line has substantially a full logical swing of Vcc level by DRAM sense amplifier DSA.

DRAMIO line DIOa (or DIOa) has a greater capacitance than DRAM bit line DBLa (or *DBLa). Thus, although "L" level potential of DRAM bit line DBLa (or *DBLa) rises slightly when the column selection signal CSLi rises, DRAM bit line is ensurely discharged to the ground level by DRAM sense amplifier DSA driving the small capacitance of DRAM bit line. This situation is analogous to the data reading out operation in an ordinary DRAM in which internal data transmitting lines are precharged to "H" level. Therefore, even if the clamping transistors DQ70 and DQ80 are in an on-state, the current flow from the clamping transistors DQ70 and DQ80 cannot destruct data in a DRAM memory cell.

In SRAM array, SRAM row decoder 21 (see FIG. 9) carries out row selection operation at time ts1 to select a

SRAM word line SWL (one of SRAM word lines SWLO to SWLm), and raises the potential of the selected SRAM word line SWL.

Row selection in DRAM and row selection in SRAM are carried out asynchronously with each other. Data of SRAM cells connected to the selected SRAM word line SWL are transferred to associated SRAm bit line pair SBL. Consequently, the potentials of SRAM bit lines SBLa and *SBLa change from the clamping potential of Vcc-Vth to the potentials corresponding to the transferred data.

At time **t5**, the data transfer instructing signal DTS instructing data transfer from DRAM array to SRAM array rises to "H". Before the time **t5**, data of selected DRAM cell has been transferred onto DRAMIO lines DIOa and *DIOa, and SRAM cell has been connected to SRAM bit line pair SBL. Then, the transfer circuit TGS shown in FIG. **63** is activated to transfer data on DRAMIO lines DIOa and *DIOa to SRAM bit lines SBLa and *SBLa in response to the signal DIS.

In this operation, the clamping transistors SQ**70** and SQ**80** are made being turned off. Thus, "H" and "L" levels of SRAM bit lines SBLa and *SBLa correspond to the potential levels supplied by the transfer gate TGS.

The relationship between the time **ts1** and the times **t1** through **t5** is arbitrary as far as the time **t5** at which the signal DIS is activated is alter than both the time when the column selection signal CSLi is generated and the potentials of DRAMIO line pair DIO are asserted and the time **ts1** when selection of SRAM word line SWL is carried out. The signal DIA instructing data transfer from SRAM array to DRAM array is maintained at "L" during this data transfer operation.

At time **t6**, the selected DRAM word line DWL has its potential fallen to "L", and the transfer instructing signal DIS falls to "L". Responsively, the clamping circuit CRS, for SRAM bit line pair SBL is activated again to raise the "L" potential level of SRAM bit line SBLa (or *SBLa).

At time **t7**, the sense amplifier driving signals SAN and /SAP both return to the intermediate potential level Vcc to release the latching by DRAM sense amplifier DSA. Then, DRAMIO lines DIOa and *DIOa have the potential returned to "H" of Vcc-Vth by means of DRAM clamping circuit CRD for DRAMIO line pair DIO. Thereafter, the column selection signal CSLi falls to "L" to isolate DRAM bit line pair from DRAMIO line pair.

In SRAM, the potential of SRAM word line SWL falls to "L" at the time **ts2**, to complete the data transfer cycle for transferring data from DRAM array to SRAM array.

Clamping circuits CRD and *CRS operate to reduce the logical swing of associated signal lines to establish the signal potentials thereon at high speed, resulting in fast data transfer.

If clamping circuits CRS and CRD are maintained active during the data transfer operation, a current flow flows from the clamping transistor SQ**70** (or SQ**80**) for SRAM bit line through an output driving transistor included in the transfer circuit TGS into the ground level, resulting in increased current consumption. Data transfer is made on a unit of plural bits such as 16 bits in the CDRAM of the invention, and therefore the penetrating current flow from the clamping transistors provides a significant value to degrade the low current consumption performance. Inhibition of the clamping by the clamping circuit CRS for SRAM bit line pair receiving the transferred data reduces significantly the penetrating current flow.

In DRAM transferring data, clamping circuit CRD is maintained operating. The clamping circuit CRD implements pull-up function. The current supply abilities of the clamping transistors DQ**70** and DQ**80** is small. The on-resistance of the selection gate SGi is relatively large. The current flow from the clamping transistor DQ**70** or DQ**80** is discharged by DRAM sense amplifier DSA. DRAM bit line potentials are made at Vcc and Vss levels by DRAM sense amplifier DSA while "L" level of DRAMIO line DIOa or *DIOa is slightly raised to a level determined by the ration of on-resistance of the clamping transistor DQ**70** (or DQ**80**) to on-resistance of the selection gate SGi and the discharging transistor in DRAM sense amplifier DSA.

Bidirectional transfer gate BTG has sufficiently larger current driving ability than the discharging ability (or latching ability) of the transistor in SRAm memory cell. Therefore, when the bidirectional transfer gate BTG operates, large current flow is caused from the clamping transistor SQ**70** or SQ**80** into a driving transistor in the transfer gate BTG. The current flow becomes large when a block of data is transferred simultaneously. This large current flow is saved by deactivation of SRAM clamping circuit CRS.

In the data transfer from DRAM to SRAM as described above, the clamping circuit CRS for SRAM bit line pair SBL is inhibited from clamping the potential in synchronization with the data transfer instructing signal DTS. However, there is a possibility that a column current which flows from the clamping transistor SQ**70** or SQ**80** into SRAM memory cell transistor may be caused when SRAM word line SWL has the potential risen to "H" and SRAM bit lines are subjected to the potential clamping. In order to reduce this column current, the clamping operation of the SRAM clamping circuit CRS is inhibited in synchronization with the selection of an SRAM word line. This construction can be implemented by applying a logical product signal of the data transfer instructing signal for data transfer from DRAM to SRAM and an SRAM word line driving signal SWL. Data transfer from DRAM to SRAM is carried out in a cache miss, and the data transfer instructing signal DTS can be asserted prior to the selection of an SRAM word line.

Now, data transfer from SRAM to DRAM will be described with reference to FIG. **65** showing operation waveforms therefor.

In DRAM, the same operation as that of DRAM to SRAM data transfer described with reference to FIG. **64** is carried out from the time **t1** till the time **t4**. In SRAM, similarly, SRAM word line SWL is selected to have the potential risen at the time **ts1**.

After the times **t4** and **ts1**, the transfer instructing signal DTA allowing data transfer from SRAM to DRAM is activated for a predetermined period from the time **t5**. The transfer circuit TG as shown in FIG. **63** is activated to transfer the signal potentials appearing on SRAM bit lines SBLa and *SBLa to DRAMIO lines DIOa and *DIOa in response to the transfer instructing signal DTA. DRAMIO lines DIOa and *DIOa have the potentials of "H" at Vcc level and "L" at Vss (ground) level by the large driving ability of the transfer circuit TGA. The signal potentials on DRAMIO lines DIOa and *DIOa are transferred onto the selected DRAM bit lines DBLa and *DBLA through the selected selection gate SGi. The transfer circuit TGA has a driving ability much larger than the latching ability of DRAM sense amplifier DSA, and therefore DRAM bit lines DRAM bit lines DBLa and *DBLa have the signal potentials corresponding to the data transferred from the selected SRAM memory cell.

DRAM clamping circuit CRD has its clamping operation inhibited at the time **t5** in response to the signal DTA, and

the transistors DQ70 and DQ80 are turned off. Consequently, no current flows from the clamping transistors DQ70 and DQ80 into a driving transistor in the transfer circuit TGA, reducing the current consumption.

At the time t6, the data transfer instructing signal DTA falls to "L", and at substantially the same timing, DRAM word line DWL has the potential fallen to "L". The falling of DRAM word line potential completes the data writing for a selected DRAM cell.

The clamping circuit CRD is activated again to raise the low level potential of DRAMIO line DIOa or *DIOa by the clamping operation. The active DRAM sense amplifier DSA maintains "H" and "L" levels of DRAM bit lines DBLa and *DBLa.

At time t7, the sense amplifier driving signals SAN and/SAP are deactivated, and the column selection signal CSLi rises, and DRAM returns to the precharge state.

In SRAM, SRAM word line SWL has the potential fallen to "L" at the time ts2 to isolate SRAM memory cell from SRAM bit line pair.

The SRAM bit lines SBLa and *SBLa have the "H" potential level determined by the clamping transistors SQ70 and SQ80.

As described above, inhibition of the clamping operation of DRAM clamping circuit CRD during data transfer from SRAM to DRAM prevents the generation of discharging current flow (penetrating current flow) through the driving transistor included in the transfer circuit TGA having a large driving ability, resulting in reduced current consumption.

(iii) Second data transfer arrangement with reduced current consumption at a high speed.

FIG. 66 shows another construction of the bidirectional transfer gate circuit BTG. By use of the construction of FIG. 66, data transfer from SRAM to DRAM can be carried out in parallel with the data transfer from DRAM. to SRAM.

In FIG. 66, the bidirectional transfer gate BTG includes a drive circuit TGAO for transferring data on SRAM bit line SBLa (or *SBLa) in response to a data transfer allowing signal DTAO, a buffer BU2 for buffering an output of the drive circuit TGAO, and a drive circuit TGA1 for transferring are output of the buffer BU2 onto DRAMIO line DIOa (or *DIOa) in response to a data transfer allowing signal DTAI.

The data transfer allowing signals DTAO and DTAI are generated at different timings from each other.

The transfer gate BTG further includes a drive circuit TGSO responsive to a data transfer allowing signal DISO for transferring data on the DRAMIO line DIOa (or *DIOa), a buffer BU1 for buffering an output of the drive circuit TGSO, and a drive circuit TGSI for transferring an output of the buffer BU1 onto the SRAM bit line SBLa (or *SBLa) in response to a data transfer allowing signal DTSI. Transfer allowing signals DTAO and DTSO are generated at substantially the same timing and the transfer allowing signals DTAI and DTSI are generated at substantially the same timing, if data transfer from SRAM to DRAM as well as data transfer from DRAM to DRAM are carried out.

In the construction of FIG. 66, the transfer allowing signals DTAO and DISO are first generated. Prior to the generation of these signals DTAO and DISO, the name operation as shown in FIGS. 64 and 65 is carried out. When the transfer allowing signals DISO and DTAO are generated, data of a selected SRAM memory cell is transferred to the buffer BU2 to be buffered therein. Data of a selected DRAM memory cell is transferred to the buffer BU1 to be buffered thereat. After the outputs of the buffers BU1 and BU2 are settled, the data transfer allowing signals DTAI and DISI are made active. Responsively, the output data of the buffer BU1 is transferred to SRAM bit line SBLa (or *SBLa) through the drive circuit TGSI.

The output data of the buffer BU2 is transferred to dram bit line DBLa (or *DBLa) through the drive circuit TGAI and DRAMIO line DIOa (or *DIOa). The transfer allowing signals DTAO and DTAI, and DISO and DISI can be considered as two shot pulsed signals DIA, and DIS respectively, in FIGS. 64 and 65. According to this construction, data transfer from SRAM to DRAM and data transfer from DRAM to SRAM can be carried out in parallel with each other, resulting in efficient data transfer.

The timings for generating the signals DTAO, DTAI, DISO and DISI may be determined such that data transfer from SRAM to DRAM and data transfer from DRAM to SRAM are carried out in a partially overlapped manner.

SRAM bit line SBLa (or *SBLa) is provided with a clamping transistor SQ75 and DRAMIO line DIOa (or *DIOa) is provided with a clamping transistor DQ85 in order to implement fast data transfer with less current consumption. The transistor SQ75 provides the SRAM clamping circuit CRS, and the clamping transistor DQ75 provides the DRAM clamping circuit CRD.

In this construction, the clamping circuit CRS has the clamping operation inhibited by a signal /DTSI of an inversion of the signal DTSI in order to prevent current from flowing into a driving transistor in the drive circuit TGSI from the clamping transistor SQ75 when SRAM bit line SBLa (or *SBLa) receives data transferred from DRAM. The transistor SQ75 receives the signal /DTSI at the gate. Likewisely, DRAM clamping circuit CRD has the clamping operation inhibited by the signal /DTAI of an inversion of the signal DTAI. The transistor DQ85 receives the signal /DTAI at the gate. (iii) Third embodiment for first data with less current consumption.

FIG. 67A shows a further another construction of the bidirectional data transfer gate, and FIG. 67B shows a detailed construction of the transfer gate of FIG. 67A. The construction of the bidirectional data transfer gate is the same as that shown in FIGS. 49 and 50. In FIGS. 67A and 67B, like components have like reference numerals allotted thereto, and detailed explanation on the construction of FIGS. 67A and 67B is omitted.

The signal DTS corresponds to the signal ϕTDS, and the signal DTA corresponds to the signal ϕTLD, and the signal DTL corresponds to the signal ϕTSL.

SRAM bit line pair SBL is provided with the SRAM clamping circuit CRS operable in response to the signal /DTS, and DRAMIO line pair DIO is provided with the DRAM clamping circuit CRD operable in response to the signal /DTA. Now, the operation of the gate of FIGS. 67A and 67B will be described with reference to FIGS. 68 and 69 showing the operating waveforms thereof.

First, data transfer from DRAM array to SRAM array will be described with reference to FIG. 68. In this data transfer operation, substantially the same operation as that shown in FIG. 55 except for the control of the clamping circuits CRD and CRS. Thus, only the control on the clamping circuits CRD and CRS will be described.

At time t5, the data transfer control signal DIS rises to "H" to inhibit the clamping operation of the clamping circuit CRS. The SRAM bit lines SBLa and *SBLa are released from the clamping by the clamping circuit CRS, and have the potentials corresponding to the potential levels supplied from the amplifier circuit 1814. Due to the deactivation of the clamping circuit CRS,a current flowing path from the clamping circuit CRS through the transistors T120, T112

and T113 or through the transistors T121, T116 and T117 of FIG. 67B is cut off.

At zime t6, DRAM word line DWL has the potential fallen to "L", and the transfer control signal DIS falls to "L" substantially at the same timing. Responsively, SRAM clamping circuit CRS is activated to clamp the potentials of SRAM bit lines SBLa and *SBLa or to raise "L" level potential of SRAM bit line pair SBL. In this state, the transistors T120 and T121 of the gate 1815 are turned off in response to the falling of the signal DTS, and current from the clamping circuit CRS does not flow into the bidirectional gate circuit BTG to the ground.

After the time t6 at which the transfer control signal DIS falls to "L", DRAM array and SRAM array are isolated from each other, and SRAM array can be accessed externally so that data transferred from DRAM array can be read out at a high speed.

Now, the operation of data transfer from the latch circuit 1811 to DRAM array will be described with reference to FIG. 70. Data transfer operation per se is the same as that shown in FIG. 53. Thus, the operation of the clamping circuit CRD will be described.

At the time t5, the transfer control signal DTA rises to "H". In this data transfer cycle, the signals DTS and DTL both are maintained at "L". In response to the transfer control signal DTA, the gate circuit 1812 of FIG. 67A or the transistors T105 and T106 turn on to transfer the data latched in the latch circuit 1811 to DRAMIO line pair DIO. DRAM clamping circuit CRD is deactivated to have its clamping operation inhibited. DRAMIO lines DIOa and *DIOa have the potentials of "H" and "L" corresponding to the data latched in the latch circuit 1811.

Because of the transfer control signal DTA at "H", the clamping transistors DQ70 and DQ80 (see FIG. 62) are turned off, to cut off the clamping current flowing path through DRAMIO line DIOa, the transistor T106 and the inverter circuit HA13 or through DRAMIO line *DIOa, the transistor T105 and the inverter circuit HA12.

At the time t6, DRAM word line DWL has the potential fallen, and the transfer control signal DTA falls to "L" substantially at the same timing. DRAM clamping circuit CRD is activated again to raise "L" level potential of DRAMIO line pair DIO.

At the time t7, the memory cycle of DRAM is completed, and successively the column selection signal CSLi falls to "L". DRAMIO line pair DIO has the potential levels determined by the DRAM clamping circuit CRD.

In this data transfer cycle, the transfer control signals DIS and DIL both are maintained at "L". DRAM array is isolated from SRAM array. DRAM address and SRAM address can be designated independently of each other. Thus, in the data transfer to DRAM array from the latch circuit 1811 SRAM can be accessed externally to have an SRAM memory selected independently of the data transfer operation. More specifically, in SRAM, a word line SWL is selected according to an external access at the time t1. SRAM bit line pair SBL has the potential levels changed from the "H" potential levels clamped by SRAM clamping to the levels corresponding to data of a selected SRAM cell, and an access to the selected SRAM cell is carried out.

At the time ts4, SRAM word line SWL has the potential fallen to "L", and SRAM bit lines SBLa and *SBLa have the potentials clamped by SRAM clamping circuit CRS.

As described above, inhibition of clamping operation of DRAM clamping circuit CRD in the data transfer to DRAM array to the latch circuit 1811 prevents the clamping current of the clamping circuit CRD from flowing into a drive transistor (discharging transistors of the inverter circuits HA12 and HA13 of FIG. 67B) to reduce current consumption in data transfer operation.

(iv) Modification of Clamping Circuit

FIG. 70 shows a modification of the clamping circuit. In FIG. 70, SRAM clamping circuit CRS includes p channel MOS transistor SQ71 having a gate receiving the transfer control signal DIS for clamping the potential of SRAM bit line SBLa, and p channel MOS transistor SQ81 having a gate receiving the signal DTS for clamping the potential of SRAM bit line *SBLa.

DRAM clamping circuit CRD includes p channel MOS transistor DQ71 having a gate receiving the transfer control signal DTA for clamping the potential of DRAMIO line DIOa, and p channel MOS transistor DQ81 having a gate receiving the signal DTA for clamping the potential of DRAM IO line *DIOa. The transistors DQ71 and DQ81 may have their one conduction terminals coupled to receive Vcc potential level or Vcc/2 potential level.

The operation of the clamping circuits of FIG. 70 is the same as that of the clamping circuit of FIG. 62. The clamping circuits of p channel MOS transistors provides the same effect as that of the clamping circuits of n channel MOS transistors.

[Address Allottance]

In the CDRAM, DRAM address and SRAM address are set independently of each other. DRAM column decoder selects 16 column select lines in DRAM array, while SRAM column decoder selects 1 column out of 16 columns. SRAM column decoder eventually selects a DRAM column in array access. Address allottance is described with reference to FIGS. 61 to 63.

FIG. 71 shows one example of connection of addresses to DRAM and SRAM. In the structure shown in FIG. 71, access to the DRAM array is carried out through bi-directional transfer gate circuit or SRAM bit line pairs SBL of the SRAM array. In this structure, column selection signal CD from SRAM column decoder 22 is commonly used as a column selecting signal for the DRAM array and the column selecting signal for the SRAM array.

In FIG. 71, DRAM address buffer 252*a* receives external DRAM addresses Aa0 to Aa9 and generates internal address int.Aa. DRAM row decoder 14 decodes internal row address from internal address int.Aa, and generates a word line driving signal DWL for selecting a word line from DRAM array. DRAM column decoder 15 receives a portion of internal column address from DRAM address buffer 252*a*, and generates a signal CSL for selecting a column selecting line from DRAM array. The remaining internal column address from DRAM address buffer 252*a* is applied to a buffer 29. Buffer 29 receives internal column address from SRAM buffer 252*b* and transmits the same to SRAM column decoder 22. When DRAM array is accessed, internal column address is not generated from SRAM buffer 252*b*, as will be described in detail later. At that time, the buffer 29 receives internal column address from DRAM address buffer 252*a* and transmits the same to SRAM column decoder 22.

SRAM row decoder 21 receives internal row address from SRAM buffer 252*b*, and generates a SRAM word line driving signal SWL for selecting one row from SRAM array. In accordance with the structure shown in FIG. 71, in the data input/output structure of FIG. 33, the column selecting signals DYi and DYj are equivalent to SRAM column selecting signals SYLi and SYLj.

FIG. 72 shows another example of a structure of address input/output portion. In the structure shown in FIG. 72,

instead of the buffer **29**, a multiplexer **30** responsive to a cache hit designating signal CH and to a DRAM access designating signal CI for passing either an internal column address from DRAM address buffer **252*a*** or an internal column address from SRAM address buffer **252*b*** is provided. The cache signal CH and the DRAM array access designating signal CI will be described in detail later. Only an outline will be described. When a cache hit designating signal CH is generated, access to SRAM array is permitted, and writing/reading of data by accessing to DRAM is inhibited. When DRAM array access designating signal (cache access inhibiting signal) CI is generated, writing/reading of data by access to memory cells in DRAM array is permitted.

Therefore, when the signal CH is generated, multiplexer **30** selects the internal column address from SRAM address buffer **252*b*** and transmits the same to SRAM column decoder **22**. When DRAM array access designating signal CI is generated, multiplexer **30** selects the internal column address from DRAM address buffer **252*a*** to transmit the same to SRAM column decoder **22**. In the structure shown in FIG. **72** also, SRAM column decoder **22** is used for both column selections on DRAM array and on SRAM array.

The structure for allotting addresses shown in FIGS. **71** and **72** are mere examples. Structures for independently decoding internal column address for DRAM array and decoding internal column address for SRAM array may be employed.

FIG. **73** shows a further example of the connection between SRAM array and internal data transmitting line pair. In the structure shown in FIG. **33**, a SRAM sense amplifier SSA is provided for each SRAM bit line pair SBL. In the structure shown in FIG. **73**, one SRAM sense amplifier SSA is provided for a plurality of SRAM bit line pairs SBL. A selecting gate circuit **302** is provided for each SRAM bit line pair SBLa, *SBLa. A column selecting signal CD is supplied to selecting gate circuit **302**. The column selecting signal CD is generated from SRAM column decoder shown in FIGS. **71** and **72**. Internal data line pair includes an internal write data line **251*a*'** for transmitting write data, and a read data transmitting line **251*b*'** for transmitting read data to an output buffer circuit. The internal write data transmitting line **251*a*'** includes a complementary data line pair DBW, *DBW. Complementary data from an input buffer circuit are transmitted to internal data lines DBW and *DBW. The internal write data line **251*a*'** is connected to a write circuit **303**.

The write circuit **303** includes cross coupled n channel MOS transistors **T301**, **T302**, **T303** and **T304**. Gates of transistors T302 and T303 are connected to the internal data line DBW. Gates of transistors T301 and T304 are connected to internal data line *DBW. Complementary write data from write circuit **303** are transmitted to respective transmitting gate circuits **302** through data lines DBWa, *DBWa. Transistors T301 and T302 transmit a supply potential Vcc when they are on. Transistors T303 and T304 transmit ground potential Vss when they are on.

For example, let us assume that data "H" are transmitted to internal data line DBW. At this time, "L" data are transmitted to internal data line *DBW. At this time, the transistors T302 and T303 are turned on. Consequently, "H" data are transmitted to internal data line DBWa through transistor T302 from writing circuit **303**, and "L" data are transmitted to the other internal data line *DBWa through transistor T303.

In data reading, "L" data are transmitted to both of the internal write data lines DBW and *DBW from the input buffer circuit, and accordingly, an output from the write circuit **303** is set to a high impedance state. At this time, sense amplifier SSA is activated, and data transmitted to internal data lines DBWa and *DBWa through a selected selecting gate circuit **302** are amplified by the sense amplifier SSA and transmitted to an output buffer circuit through internal read data transmitting line **251*b*'**.

As shown in FIG. **73**, by separately providing write data transmitting line **251*a*'** and read data transmitting line **251*b*'** as the internal data line **251**, design of input/output circuit layout is made easier than a structure in which writing/reading of data are carried out through a common internal data bus.

[Refreshing Operation]

The DRAM array includes dynamic memory cells as components. Therefore, data stored therein must be refreshed periodically, or in a predetermined time period. Refreshing operation of the semiconductor memory device containing a cache will be described in the following.

Returning to FIG. **32**, an external refresh designating signal REF# is supplied. Automatic refreshing (Auto-refreshing) is carried out in the semiconductor memory device when the external refresh designating signal REF# is set to an active state of "L" at a rise of an internal clock K.

Referring to FIG. **32**, circuit structure for refreshing includes an auto refresh mode detecting circuit **291** responsive to an internal refresh designating signal REF from a control clock buffer **250** detecting designation of auto-refresh; and a refresh control circuit **292** responsive to a refresh request from auto refresh mode detecting circuit **291** for generating various control signals and applying these signals to a counter **293** and to a multiplexer circuit **258**. Counter circuit **293** applies a count value stored therein to multiplexer circuit **258** as a refresh row address indicating a row to be refreshed, in response to refresh designating signal from refresh control circuit **292**.

Multiplexer circuit **258** selects the refresh row address from counter circuit **293** and applies the same to DRAM row decoder **102**, in response to a switch control signal MUX from refresh control circuit **292**. The internal refresh designating signal REF is also applied to a DRAM array driving circuit **260**. DRAM array driving circuit **260** is rendered active when internal refresh designating signal REF is applied and carries out operations related to row selection in DRAM array **101**.

Refresh control circuit **292** increments by one the count value in counter circuit **293** at the completion of refreshing, every time refresh designating signal REF is applied. Refresh control circuit **292** sets switch control signal MUX to inactive state at the completion of refreshing, and in response, multiplexer circuit **258** selects an internal address int-Aa for internal DRAM from address buffer circuit **252** and transmits the same to DRAM row decoder **102**.

FIG. **74** functionally shows a transfer gate controlling circuit **262**. The transfer gate controlling circuit **262** generates the signals ϕTDS and ϕTSD for controlling transfer operation of the bi-directional transfer gate circuit **210** (3, BTG), in response to internal control signals E, CI, W and CH. When cache hit signal CH is active, the transfer gate controlling circuit **262** does not generate the transfer control signals ϕTDS and ϕTSD. However, if array access designation (cache inhibition) signal CI is set to an active state, it successively generates control signals ϕTDS and ϕTSD in accordance with the state of the write enable signal W at that time.

Transfer gate controlling circuit **262** also receives an internal refresh designating signal REF. The transfer gate

controlling circuit **262** may be adapted to be set to the inactive state when internal refresh designating signal REF is applied. However, since a refresh designating signal REF# is applied externally, it is not necessary for transfer gate controlling circuit **262** to receive especially refresh designating signal REF, when generation of the array access designating signal CI is prevented by an external specification. When refreshing is being carried out in the DRAM, SRAM array must be surely separated electrically from the DRAM array. If a structure is provided in which the transfer gate controlling circuit **262** is disabled in response to internal refresh designating signal REF, the SRAM array can be surely separated electrically from the DRAM array during refreshing operation, and external access to SRAM array is made possible.

Transfer gate controlling circuit **262** may have a structure in which transfer gate control circuit **262** is disabled when either cache hit signal CH or refresh signal REF is made active. More preferably, a gate circuit which sets the transfer gate control circuit **262** to a disabled state when either cache hit signal CH or refresh designating signal RF is active should be provided. Except that time, transfer control signals ϕTDS and ϕTSD are generated at predetermined timings in accordance with the control signals CI and W.

FIG. **75** shows functional structure of DRAM array driving circuit **260** shown in FIG. **32**. DRAM array driving circuit **260** includes a row selecting circuitry driving circuit **260***a* for driving circuits related to row selection of DRAM array, and a column selecting circuitry driving circuit **260***b* for driving circuits related to column selection in DRAM array **1**. Row selection circuitry driving circuit **260***b* generates various control signals ϕEQ, /ϕSAPE, ϕSANE and DWL at predetermined timings, respectively, in response to internal control signals E, CH, CI and REF. Column selecting circuitry driving circuit **260***b* generates a signal CDA (which corresponds to internal control signal int. *CAS) for driving DRAM column decoder **15** at a predetermined timing in response to control signals E, CH, CI and REF.

Column selecting circuitry driving circuit **260***b* generates a column decoder activating signal CDA at a predetermined timing when refresh designating signal REF is inactive and the row selecting circuitry driving circuit **260***a* is made active. When refresh designating signal REF is made active, column selecting circuitry driving circuit **260***b* is disabled. Consequently, column selecting operation in the DRAM is prohibited.

By this structure, when refresh designating signal REF is made active, refreshing operation in the DRAM array can be carried out independent from the operation of the SRAM array.

Auto refresh mode detecting circuit **291**, refresh control circuit **292** and counter circuit **293** shown in FIG. **32** operate in response to refresh designating signal REF, and their operations are set independent from the operation of a command register **270**. Therefore, refreshing of DRAM array **101** can be carried out in parallel to command mode setting of the command register **270**. More specifically, command register **270** simply generates a command data CM and applies the data to a data input/output control circuit **272** and to an input/output buffer+output register block **274**. Data maintained therein has no influence to memory cell selecting operation in the DRAM array **101**.

Setting of data in command register **270** is completed in 1 cycle of external clock signal K, as will be described in detail later with reference to a timing diagram. Refreshing operation in DRAM array needs n cycles. This is because the speed of operation of the DRAM **100** is lower than that of the clock K. Therefore, in this case, in short, 1 clock cycle is saved in effect. However, if the period of external clock K is made slower in accordance with the operation mode and the period is similar to 1 memory cycle of the DRAM **100**, setting of data to the command register **270** can be carried out in parallel to the refreshing operation of the DRAM array **101**. The change of the period of the external clock K enables reduction in current consumption corresponding to lowering of the speed of operation of CDRAM. More specifically, when the DRAM is in the standby state or when low power consumption is desired more rather than higher speed of operation of the memory device, the speed of operation of the semiconductor memory device is lowered and the power consumption is reduced by elongating the period of the clock. The period of the external clock K may be made longer only when access to the DRAM only is being carried out.

By the above described structure, a CDRAM having the following characteristics can be provided.

(1) The CDRAM in accordance with the present invention has a DRAM memory array serving as a main memory and an SRAM array serving as a cache memory integrated on one chip, and these memories are coupled to each other by an internal bus used only for data transfer, which is different from an internal common data bus. Consequently, block transfer between the DRAM array and the SRAM array (cache) can be completed in 1 clock cycle. In the following description, the term "array" refers to the DRAM array. Compared with a conventional cache memory system employing a standard DRAM and a standard SRAM, system performance can be significantly improved.

(2) The DRAM memory array and the SRAM array can be accessed by separate and independent addresses. Therefore, various mapping methods, for example direct mapping method, set associative method and full associative method can be implemented.

(3) The CDRAM operates in synchronization with an external clock K. Compared with a method in which internal clock signals are generated by using an address change detecting circuit, delay of a cycle time derived from address skew or the like can be prevented, realizing accurate control.

(4) Externally applied signals (or data) such as array addresses (addresses for the DRAM) Aa**0** to Aa**9**, cache addresses (addresses for SRAM) Ac**0** to Ac**11**, data input/output D**0** to D3 or DQ**0** to DQ3, a write enable signal W#, a cache hit signal CH#, a chip select signal E#, a refresh signal REF#, a cache inhibition signal CI# and a command register signal CR# are all taken at a rising edge of the external clock K.

(5) Since array addresses are taken in accordance with a multiplexing method, the number of pins for array addresses can be reduced, increasing packaging density of the CDRAM.

(6) Addresses of the array and of the cache are independent from each other. At a time of a cache hit, access to the cache only is carried out, enabling high speed cache hit accessing.

(7) Data can be read at an arbitrary timing by an output enable signal G# regardless of the timing of the external clock K, so that asynchronous bus control can be done in the system.

(8) By using the command register **270**, output specification (transparent, latch, register) and I/O structure (input/output pin separation, masked write) can be arbitrarily designated by a user. When a registered output method is used, output data of an address designated in the previous cycle appears at a rising edge of the external clock K. Such data output mode is suitable for pipeline application.

In a latched output method, output data of an address designated in the previous cycle is continuously output at the timing at which invalid data were to be output otherwise. Therefore, invalid data is not output at all, and valid output data only is provided. By this latched output mode, sufficient period of time for the CPU to take output data can be provided.

(9) Data writing operation is started at a rising edge of the external clock K. However, writing is automatically terminated by an internal timer or the like. Therefore, it is not necessary to set completion of writing operation by, for example, an external write enable signal W#, and therefore setting of timings in the system is facilitated.

(10) A refresh designating signal REF# for designating auto-refreshing can be externally applied. Therefore, the DRAM array can be automatically refreshed easily at a desired timing.

(11) As described above, the CDRAM of the present invention can be housed in 300 mil, TSOP package, type II having 44 pins. The TSOP package type II is a very thin rectangular package, which realizes a system having high packaging density.

(12) SRAM array has a multiplicate word line arrangement in which a plurality of ward lines are provided for one row of SRAM memory cells. Thus, SRAM array with high density and desired physical dimensions corresponding to the shape of DRAM array is easily obtained to provide efficient layout of SRAM array and DRAM array on a chip, resulting in CDRAM with high density and high integration.

(13) Clamping circuits are provided for SRAM bit line pair and DRAMIO line pair.

In data transfer, the clamping circuit at a data receiving side has the clamping operation inhibited. This arhitecture provide fast data transfer between SRAM and DRAM with less current consumption.

FIG. **76** shows, in a table, operation modes of the CDRAM of the present invention and states of control signals for designating respective operation modes. An operation mode of CDRAM is set by a combination of the states of external control signals E#, CH#, CI#, CR#, W# and REF#. Referring to FIG. **76**, "H" represents a high level signal potential, "L" represents a low level signal potential, and "X" represents an arbitrary state (don't care D.C). As shown in FIG. **76**, operation modes of the CDRAM includes a standby mode in which the CDRAM is set in a standby state; an array refresh for automatically refreshing the DRAM array, data transfer between a CPU (Central Processing Unit) and a cache (SRAM); data transfer between CPU and array; data block transfer between a cache and an array; and setting of special mode in the command register. Timings and combinations of the states of the signals for setting respective operation modes will be described in detail later with reference to a diagram of signal waveforms. In FIG. **76**, write enable signal W# is indicated as "H/L" at data transfer between the CPU and the command register. It means that write enable signal W# is set to "H" or "L" in this operation mode, and either "H" or "L" state is used for designating a certain special mode.

[Command Register]

Various operation modes can be set internally by the command register.

FIGS. **77** and **78** shows the contents in the command register **270** shown in FIG. **32** and a method of selecting the contents. Command register **270** includes 8 registers **RR0–RR3** and **WR0–WR3**. Combination of write enable signal W# and 2 bits of command addresses **AR0** and **AR1** is used for selecting a register. By setting the external write enable signal W# to "H" at a rising edge of external clock K. one of the registers **RR0–RR3** is selected. Register **RR0** is selected by setting command addresses **Ar0** and **Ar1** to "0". Register **RR1** is selected by setting command address bit **Ar0** to "1" and command address bit **Ar1** "0". Selection of register **RR0** means setting of a masked write mode (this masked write mode is also a default). Selection of the register **RR1** means setting of D/Q separation mode.

When write enable signal W# is set to "L" at a rising edge of external clock K and setting command addresses **Ar0** and **Ar1** both to "0", then register **WR0** is selected. As shown in FIG. **37** or **78** this register **WR0** sets the output mode to transparent, latch or register mode, dependent on the combination of data at data input terminals **DQ0** (**D0**) to **DQ3** (**D3**) at that time. Details of the respective output modes has been described previously. When register **WR0** is selected, input data **D2** and **D3** (**DQ2** and **DQ3**) are both set to "0". When input data **D0** is set to "0" and input data **D1** is set to an arbitrary value in this state, transparent output mode is set. When input data **D0** is set to "1" and input data **D1** is set to "0", latched output mode is selected. When input data **D0** and **D1** are both set to "1", registered output mode is selected. Other registers are used for arbitrary extended functions.

[Connection Between CPU & DRAM]

CDRAM is employed with CPU in a data processing system. The CDRAM provides various mapping scheme. System structure such as bus connection is varied depending on the mapping scheme of CDRAM. Specific system implementation using CDRAM is described with reference FIGS. **79** and **80**.

FIG. **79** is a block diagram showing a structure of a system when a cache system is formed by a direct mapping method using the CDRAM **600** in accordance with the present invention. Referring to FIG. **79**, the cache system comprises, in addition to CDRAM **600**, a controller **650** for controlling access to the CDRAM **600**, and a CPU for carrying desired data processing by inputting/outputting data to and from the CDRAM **600**. FIG. **79** shows only an address structure output from the CPU when cache access is required. The CPU is assumed to have 32 bits. The cache system further includes an address multiplex circuit **700** for multiplexing and applying row and column addresses to the CDRAM **600**. Portions only related to cache access to the CDRAM **600** are shown as representatives.

Controller **650** includes a decoder **652** for decoding set addresses A6 to A13 from the CPU, valid bit memory **654** indicating which set is valid in response to an output from decoder **652**, and a tag memory **656** for storing tag addresses of data stored in SRAM **200**. SRAM **200** has a structure of 4K×4 bits, and there are 256 tags. Therefore, tag memory **656** includes 8 bits×256 structure. Valid bit memory **654** has a structure of 1 bit×256 for indicating which of the 256 sets is valid. Decoder **652** decodes set addresses A6 to A13 and makes valid one of the valid bit memory **654**.

Controller **650** further includes a decoder **670** receiving addresses A22 to A31 from the CPU as a chip selecting signal for determining whether or not a corresponding CDRAM **600** is designated, a comparator **658** which is activated in response to an output from decoder **670**, comparing a tag address from tag memory **656** with tag addresses A14 to A21 from CPU for determining a cache hit or miss, and a selector **672** in response to a cache hit/miss for selecting either the tag address from tag memory **656** or tag addresses A14 to A21 from CPU for applying thus selected one to the multiplex circuit **700**. At a time of a cache miss, selector **672** stores tag address applied from the CPU to a corresponding position of the tag memory **656**.

The operation will be briefly described in the following. When access to the CDRAM. **600** is requested by the CPU, addresses A2 to A31 are generated on the data bus **620**. Addresses A20 to A31 out of **30** bits of addresses on common data bus **620** are used as a chip select signal and applied to decoder **670** in controller **650**. Decoder **670** decodes addresses A22 to A31 as the chip select signal, and determines whether or not an access to the corresponding CDRAM is requested. If it is determined that an access to the CDRAM **600** is requested, chip select signal E# is generated from decoder **670** and applied to CDRAM **600**. A comparator **658** is activated by the chip select signal from decoder **670**.

Decoder **652** included in controller **650** takes and decodes addresses A6 to A13 out of addresses transmitted from CPU to address bus **620** as the set address. Decoder **652**, which has decoded 8 bits of the set address, sets corresponding bits of the valid bit memory **654** for selecting one set out of 256 sets. An address of 8 bits indicating a tag corresponding to the valid bit of the valid bit memory **654** is read from tag memory **656** and applied to comparator **658**. Comparator **658** compares tag address from tag memory **656** with the tag address of A14 to A21 output from CPU. When they match with each other, comparator **658** makes cache hit signal CH# fall to "L" and applies the same to CDRAM **600** so as to indicate a cache hit. If they do not match with each other, comparator **658** generates a cache hit signal CH# of "H" to indicate a cache miss (miss hit).

At a time of a cache hit, the following operation is carried out in the CDRAM **600**. The control of operation at this time is carried out by control signals from a control clock buffer **250** and by SRAM array driving circuit **264** (see FIG. **32**). SRAM row decoder **202** selects one of 256 sets in response to the set address of A6 to A13 from the CPU. Namely, one row (one in each SRAM array block, 4 rows in total) is selected. Consequently, 16 bits of SRAM cells are selected in each SRAM array block of the SRAM **200**. SRAM column decoder SCD **203** decodes the block address of A2 to AS from CPU, selects 1 bit out of 16 bits of memory cells, and connects the selected one to data input/output terminal. FIG. **79** shows an output data Q at the time of a hit reading.

Operation at a miss hit will be described. At this time, data to which access is requested by the CPU is not stored in the SRAM **200**. In controller **650**, selector **672** applies a corresponding tag address stored in tag memory **656** to multiplex circuit **700** in response to a miss hit designating signal from comparator **658**. At this time, selector **672** has the 8 bits of tag address A14 to A21 applied from CPU as a new tag address stored at corresponding positions in tag memory **656**.

In CDRAM **600**, a copy back, that is, simultaneous transfer of 16 bits from SRAM **200** to DRAM **100** is carried out in this cycle. Data of 16 bits×4 selected by SRAM row decoder SRD **202** in accordance with the set address of A6 to A13 from the CPU in SRAM **200** are stored at corresponding positions of DRAM cells of 16 bits×4 which have been selected by row and column selecting operation in the DRAM **100** in accordance with 8 bits of tag address output from selector **672** and in accordance with the address A6 to A13 output from the CPU.

In the next operation cycle, CDRAM **600** selects 16 bits×4 DRAM cells in DRAM **100** in accordance with the address A6 to A21 output from the CPU, and writes the data of 16 bits×4 to corresponding 16 bits×4 memory cells of SRAM **200** which have been selected by SRAM row decoder SRD in accordance with address A6 to A13 from CPU. This data transfer may be carried out in accordance with the high speed transfer mode.

As described above, for the SRAM, address bits A2 to A5 are used as a block address, address bits A6 to A13 are used as a set address, address bits A14 to A21 are used as a tag address. For the DRAM, address bits A6 to A11 are used as a column address, and address bits A12 to A21 are used as a row address. Consequently, a direct mapping method can be realized between DRAM **100** and SRAM **200**.

FIG. **80** is a block diagram showing a system structure of 4 way set associative method using the CDRAM of the present invention. CDRAM **600** has the same structure as that shown in FIG. **79**, which includes SRAM **200**, DRAM **100** and a clock control circuit **256'**. Clock control circuit **256'** includes control clock buffer **250**, SRAM array driving circuit **264** and DRAM array driving circuit **260** shown in FIG. **32**. For simplicity, circuit structures for controlling data input/output are omitted.

Controller **750** includes a decoder **752**, a valid bit memory **754**, a tag address memory **756**, a comparator **758**, a decoder **770** and a selector **772**. For correspondence to 4 ways, valid bit memory **754** includes 4 memory frames each having 1 bit×64 structure. Tag address memory **756** also has 4 memory frames each having 8 bits×64 structure. Similarly, 4 comparators **758** are provided for selecting one of 4 ways, that is, one comparator is provided for each memory frame of the tag address memory **756**. In 4 way set associative method, 256 rows of SRAM **200** are divided into 4 ways, and therefore the number of sets is 64.

Addresses having the following structures are transmitted from CPU to address bus **620**. Address of A22 to A31 is an address for selecting a chip, address of A14 to A21 is a tag address, address of A12 and A13 is a way address, address of A6 to A11 is a set address, and address of A2 to A5 is a block address. Address of A6 to A11 and address A12 to A21 are used as a column address and a row address for the DRAM **100**, respectively. Multirlex circuit **700** is provided for DRAM **100** of CDRAM **600** for multiplexing the row and column addresses. The operation will be described.

Address A6 to A11 from CPU is applied as a set address to decoder **752**. Address of A22 to A31 is applied as a chip select address to decoder **770**. Decoder **752** decodes the set address of A6 to A11 and sets the valid bit related to a corresponding set to valid state, in valid bit memory **754**. Consequently, 1 set (4 ways) is selected. Decoder **770** decodes chip select address of A22 to A31 to determine whether or not there is an access request to CDRAM **600**. If an access to CDRAM **600** is requested, decoder **770** sets chip select signal E# to an active state, that is, "L", and activates comparator **758**. Comparator **758** reads corresponding 4 way tag addresses from tag address memory **756** referring to valid bits in valid bit memory **754**, and compares the read tag addresses with the address of A14 to A21 from the CPU. If a matching is found, comparator **758** outputs a way address of **W0** and **W1** indicating the way in which the matching is found, and makes cache hit signal CH# fall to "L" so as to indicate a cache hit. if there is not a match in comparator **758**, cache hit signal CH# is set to "H"to indicate a miss hit.

When a cache hit occurs, way address of **W0** and **W1** from controller **750** and address of A6 to A11 from the CPU are applied as a row address to SRAM row decoder **202**, and 16 bits×4 SRAM cells are selected in SRAM array **201**. Block address A2 to A5 as a column address are decoded by SRAM column decoder **203**. Out of selected 26 bits×4 SRAM cells, 1 bit×4 are selected to be connected to data output terminals Q (or data input terminals D).

In case of a miss hit, selector **772** selects one of the 4 way tag address to select a region in which tag address is to be

rewritten in accordance with LRU (Least-Recently Used) logic. The tag address selected by selector **772** is applied as an array address to DRAM row decoder DRD in DRAM **100** through multiplex circuit **700**. Selector **772** replaces the tag address which is to be rewritten by address of **A14** to **A21** applied from the CPU.

In CDRAM **600**, the first cycle is a copy back mode. In copy back mode, way address of **W0** and **W1** indicating the way to be rewritten, is output under the control of selector **772**. In SRAM **200**, address of **A6** to **A11** from CPU and way address of **W0** and **W1** from controller **750** are decoded, and 16 bits×4 SRAM cells are selected. In DRAM **100**, 16 bits×4 DRAM cells are selected in accordance with 8 bits of tag address output from selector **772** and to address A6 to **A13** output from the CPU. Thereafter, data are transferred from selected 16 bits×4 SRAM cells to selected 16 bits×4 DRAM cells.

In the next operation cycle, 16 bits×4 DRAM cells are selected in DRAM **100** in accordance with address **A6** to **A21** from the CPU. Data of the newly selected 16 bits×4 DRAM cells are simultaneously transferred to 16 bits×4 SRAM cells which have been selected in accordance with address **A6** to **A11** and way address **W0** and **W1**. The data transfer may be carried out in accordance with the high speed transfer mode.

By the above described structure, either direct mapping method or set associative method can be realized without changing internal structure of CDRAM **600**. Although not shown, full associative mapping method is also possible. In that case, in controller **750**, a tag address memory for storing SRAM cache address and a corresponding address of the DRAM **100** is necessary. Relation between signal timings in various operation cycles and state transitions in CDRAM will be described.

CDRAM operates synchronized with a clock K, to latch external control signal, write in data and address signal. Operation cycle of CDRAM is determined by combined states of external control signals at the rising edge of the clock. However, internal operation of CDRAM is advanced asynchronously with the clock K. Specific operation cycles are described with reference to FIGS. **81** to 104B.

As described above, control signals except output enable signal G# and addresses Aa and Ac are latched at a rising edge of external clock signal K. The states of respective signals are arbitrarily (D.C) except that set up time and hold time are necessary before and after a rising edge of the external clock K. In accordance with the external clock synchronizing method, it is not necessary to take cycle time margin derived from skew of address signals and the like into consideration, and the cycle time can be reduced. Thus, a CDRAM operating at high speed can be provided.

Output enable signal G# controls the states of outputs from output buffer and output register included in input/output circuit **274** shown in FIG. **37**. When output enable signal G# is at "H", output data is in a high impedance state (Hi-Z). When output enable signal G# attains to active state, that is, "L", data is output.

[Specific Operation Cycles & Timings]

The operation modes of CDRAM are as shown in a table of FIG. **76**. The respective operation modes together with the timings thereof will be described, referring to FIGS. **81** to **104B**.

In the standby state, chip select signal E# and refresh designating signal REFO are both set to "H" at a rising edge of external clock signal K, and remaining control signals CH#, CI#, CR# and W# are at arbitrary states. In the standby state, memory operation is not carried out at all in CDRAM.

No. 1: Cache Hit Write Cycle

FIG. **81** shows timings of various signals in cache hit write cycle. External clock signal K has a cycle time tk Cycle time tk includes an H pulse width tKH at which external clock signal K is at "H", and a L pulse width tKL at which external clock signal K is at "L". A cache hit write cycle is a cycle for writing data to SRAM cache. When this state is selected, chip select signal E# is set to "L", cache hit signal CH# is set to "L", cache hit inhibition signal CI# is set to "H", command register signal CR# is set to "H", write enable signal W# is set to "L" and output enable signal G# is set to "H" at a rising edge of external clock signal K.

At this state, an address for SRAM **200** is latched as valid, and access to SRAM is carried out in accordance with the address Ac for the SRAM. At this time, an address Aa for the DRAM is arbitrary (D.C). At a rising edge of the external clock signal K, input data D is assumed valid, and valid write data is written to SRAM cell selected by the SRAM address Ac. Since access to the cache memory SRAM is at high speed, writing is completed in 1 clock cycle of external clock signal K as shown in FIG. **81**. Namely, the time required for a cache hit writing is the clock cycle time tK.

Although output-data-Q changes in response to an arbitrary state (D.C.) of output enable signal G# in FIG. **81**, this means that output data appears corresponding to the "H" and "L" levels of the output enable signal G#. FIG. **81** shows set up times and hold times of respective control signals and address signals. The set up time is necessary for setting surely the control signal or addresses at an established state by the time of the rising edge of external clock signal K. The hold time is necessary for ensuring operation by holding the signal for a constant time period from a rising edge of the external clock signal K. The set up time and the hold time will be described briefly.

Chip select signal E# includes a set up time tELS which is necessary when it is set to "L", a set up time tEHS which is necessary when it is set to "H", a hold time tELH necessary when it changes to "L", and a hold time tEHH which is necessary when it changes to "H".

To the cache hit signal CH#, a set up time tCHLS which is necessary when it change to "L", a set up time tCHS which is necessary when it is changed to "H", a hold time tCHLH which is necessary when it is changed to "L" and a hold time tCHHH which is necessary when it is changed to "H" are set.

Cache inhibition signal CI# includes set up times tCILS and tCIHS which are necessary when it is changed to "L" and to "H", respectively, and hold times tCILH and tCIHH which are necessary when it is changed to "L" and to "H", respectively.

The command register signal CR# includes set up times tCRLS and tCRHIS which are necessary when it is changed to "L" and to "H", respectively , and hold times tCRLH and tCRHH which are necessary when it is changed to "L" and "H", respectively.

Refresh signal RE# includes set up times tRLS and tRHS which are necessary when it is changed to "L" and to "H", respectively, and hold times tRLH and tRHH which are necessary when it is changed to "L" and to "H", respectively.

Write enable signal W# includes set up times tWLS and tWHS which are necessary when it is changed to "L" and "H", respectively, and hold times TWLH and tWHH which are necessary when it is changed to "L" and "H", respectively. The address Ac for SRAM includes a set up time tACS which is necessary for determining the state thereof as valid, and a hold time tACH which is necessary when it is valid.

The address Aa for DRAM includes a set up time tAAS which is necessary to a rising edge of external clock signal K at which it is determined valid, and a hold time tAAH which is necessary after it is determined to be valid.

As to write data D, a set up time tDS required for valid data, and a hold time tDH required for valid data are necessary.

As to output enable signal G#, time tGHD necessary from the time at which output is disabled to the time when data input pin is activated, a delay time tGLD which is necessary from the time at which data input pin is set to the high impedance state to the time when signal G# is changed to "L", time tGLQ which is necessary from the time when it is changed to "L" to the time when the output pin is activated, and time tGHQ which is necessary from the time when it is changed to "H" to the time when the output pin is set to the high impedance state are set.

As to access time, an access time tGLA from the time when output enable signal G# attains to "L" to an output of valid data, access time tKLA from the time when external clock signal K attains to "L" to an output of valid data, an access time tKHA from the time when external clock signal K attains to "H" to the output of valid data, an access time tKHAR from the time when external clock signal K attains to "H" in registered output mode to the output of valid data, and an array access time tKHAA necessary from the time when external clock signal K attains to "H" to the time when TRAM is accessed and valid data are output are set.

Referring to FIG. **81**, after a lapse of tGHD from a rising edge of output enable signal G#, the write data D is regarded as invalid.

The cycle time of the CDRAM of the present invention is set to 10 nS to 20 nS, as an example. Array access time tKHAA is set to 70 to 80 ns. Various set up times and hold times are set to several nano seconds.

No. 2T: Cache Hit Read Cycle (Transparent Output Mode)

FIG. **82** shows timings of cache hit read cycle in the transparent output mode. As described above, the output mode includes transparent output mode, latched output mode and registered output mode. Designation of the output mode is carried out by the command register. Referring to FIG. **82**, when a cache hit read cycle is set, chip select signal E# and cache designating signal CH# are both set to "L" at a rising edge of the external clock signal K, and cache hit inhibition signal CI#, refresh designating signal REF#, command register signal CR# and write enable signal W# are set to "H".

In this state, an address Ac for the SRAM is made valid at the rising edge of the external clock signal k, and a SRAM cell is selected in accordance with this valid address Ac. In transparent output mode, data of the SRAM cell designated by the valid address Ac is output in this clock cycle. In transparent output mode, valid output data Q is output after a lapse of tKHA from the rising edge of the external clock K or after a lapse of time tGLA from a falling edge of output enable signal G#, which ever is later.

When output enable signal G# falls to "L" before the time tKHA, invalid data is continuously output until the time tKHA has lapsed. In the cache hit read cycle, write data is set to high impedance state (Hi-Z), and the address Aa from the DRAM may be set to any state, since it is not used.

No. 2L: Cache Hit Read Cycle (Latch Output Mode)

FIG. **83** shows timings in cache hit read cycle of latched output mode. The difference between latched output mode and transparent output mode is that when output enable signal G# falls to "L" before the access time tKHA, data of the SRAM cell which has been selected in the previous cycle (Pre.Valid) is output at first. Other signal timings are the same as those in transparent output mode shown in FIG. **82**. In the latch output mode, invalid data (INV) is not output. Valid data only are output.

No. 2R: Cache Hit Read Cycle (Register Output Mode)

FIG. **84** is a timing diagram of the cache hit read cycle in registered output mode. Timings of external control signals in the cache hit read cycle of the registered output mode are the same as those in the transparent output mode and in the latched output mode shown in FIGS. **82** and **83**. In the registered output mode, valid data of the previous cycle (Pre.Valid) is output after the lapse of tKHAR from the rising edge of external clock signal K or after a lapse of time tGLA from a falling edge of output enable signal G#, which is later. In registered output mode, invalid data is not output. Register output mode is suitable for pipeline operation.

Switching of the above described output modes is realized by controlling the operation of an output register included in input/output circuit **274** shown in FIGS. **32** and **37** (particularly see FIG. **37**).

No. 3: Copy Back Cycle

FIG. **85** shows timings of various signals in copy back cycle. The copy back cycle is a cycle for transferring data from cache (SRAM) to array (DRAM), and it is carried out as a first cycle at a time of a miss hit. In the copy back cycle, chip select signal E# and write enable signal W# are both set to "L", and cache hit signal CH#, cache inhibition signal CI#, refresh designating signal REF#, command register signal CR# and output enable signal G# are set to "H" at a rising edge of external clock signal K. In the copy back cycle, an array address Aa must be input to DRAM for selecting the memory cells. A row address (Row) and the column address (Col) are multiplexed and applied as the array address Aa. An array row address is latched at a first rising edge of external clock signal K, and an array column address is latched at a second rising edge of external clock signal K. At the second rising edge of external clock signal K, cache hit designating signal CH#, cache inhibition signal CI#, write enable signal W# and cache address (address to SRAM) Ac may be at arbitrary states.

Write enable signal W#has been set to "L" at the first rising edge of external clock signal K, and external input data D changes from high impedance state to an arbitrary state. External output data Q is set to high impedance state, since output enable signal G# is at "H".

No. 4: Block Transfer Cycle

In block transfer cycle shown in FIG. **86**, a data block is transferred at one time from the array to the cache (SRAM) before, after or simultaneously with a copy back operation. Timing conditions which are the same as in the copy back cycle shown in FIG. **85** are satisfied in the block transfer cycle, except that write enable signal W# is set to "H" at a first rising edge of the external clock signal K.

More specifically, when write enable signal W# is set to "L" at the first rising edge of external clock signal K at a cache miss (miss hit), the copy cycle is started. If write enable signal W# is set to "H", block transfer cycle from the array to the cache is set.

Whether a high speed copy back is to be carried out or normal copy back and block transfer is to be carried out, or whether write through operation is to be carried out is determined by setting of command data to the command registers.

No. 5: Array Write Cycle

The array write cycle shown in FIG. **87** is a cycle for setting a mode in which CPU directly accesses to the array

for writing data. A DRAM cell in the array is selected by array address Aa. At this time, data may be written through access switching circuit **310** of bi-directional transfer gate circuit **305** as shown in FIG. **33**. Alternatively, data may be written through SRAM bit line pair SBL, the bi-directional transfer gate BTG and global I/O line pair GIO as shown in FIGS. **49** and **57**, without providing access switching circuit **310**. If the structure is adapted to write data through SRAM bit line pair SBL in SRAM array, lower bits of array address Aa may be applied to column decoder SCD of SRAM as a block address. A column selecting signal may be applied from DRAM column decoder to SRAM selecting gate.

Array write cycle is designated by setting chip select signal E#, cache inhibition signal CI# and write enable signal W# to "L" and by setting refresh designating signal REF#and output enable signal G# to "H" at the first rising edge of external clock signal K, as shown in FIG. **87**. Cache designating signal CH# may be at an arbitrary state. In array write cycle, array address Aa is latched as a row address (row) at the first rising edge of external clock signal K, and array address Aa is latched as a column address (Col) at the second rising edge of external clock signal K. Since the cache is not accessed at this time, address Ac for the cache may be at an arbitrary state. External write data D is latched at the first rising edge of external clock signal K. External output data Q is set to high impedance state.

In the cache system shown in FIGS. **79** and **80**, only 16 bits of an address are applied to DRAM **100**, and column selecting operation in blocks is carried out in accordance with the block address in SRAM. FIGS. **79** and **80** show a structure for a cache system and those figures do not show the structure of the array access. However, the structure may use 4 bits of a block address as column selecting address for DRAM **100**, when cache inhibition signal CI# attains to "L" at array accessing.

No. **6**: Array Read Cycle

Array read cycle shown in FIG. **88** is a cycle for setting a mode in which CPU directly accesses to array for reading data. Array read cycle is designated by setting chip select signal E# and cache inhibition signal CI# to "L" and by setting refresh designating signal REF#, command register signal CR#, write enable signal W# and output enable signal G# to "H" at the first rising edge of external clock signal K. At the second rising edge of external clock signal K, chip select signal E#, refresh designating signal REF# and command register signal CR# are set to "H", and cache inhibition signal CI# and write enable signal W# may be at an arbitrary state. The cache hit designating signal CH# may be at an arbitrary state in array read cycle. Output enable signal G# is maintained at "H". Array address Aa is latched as a row address at the first rising edge of external clock signal K, and array address Aa is latched as a column address at the second rising edge of the external clock signal K. External input data D may be at an arbitrary state, and external output data Q is set to high impedance state.

Array access cycles (array write cycle and array read cycle) are set by setting cache signal CI# to "L" at the first rising edge of the external clock signal K. The array access cycles are cycles for setting modes in which CPU directly accesses the array. Data reading/writing are not actually carried out in the array write cycle and array read cycle.

In operations such as copy back operation, block transfer operation and array access operation which require reading/writing of data in the array, selection of a word line in the DRAM array, detection and amplification of data in the selected cells by sense amplifiers, restore operation of data, and RAS precharge are necessary. Therefore, these operations requiring reading/writing of data in the array takes several clock cycles. When we represent the cycle time of the DRAM by tA and the cycle time of the external clock signal K as tK, external clock cycles of m=ta/tK is necessary for the array access. m cycles correspond to a wait time for the CPU. Timings when the CPU is kept in a waiting state in reading/writing data while memory cells are selected in the array will be described.

No. **7**: Array Active Cycle

In array active cycle shown in FIG. **89**, row selecting operation, column selecting operation and data writing/reading are carried out in accordance with the applied array address Aa. In array active cycle, chip select signal E#, refresh designating signal REF# and command register signal CR# are set to "H" at a rising edge of external clocks signal K, and output enable signal G# is fixed at "H" for this cycle. Cache hit signal CH#, cache inhibition signal CI# and write enable signal W# may be at an arbitrary state. External input data D may be at an arbitrary state and external output data Q is set at high impedance state in the array active cycle.

No. 7QT: Array Active Cycle Accompanied With Transparent Output Mode

Control signals E#, CH#, CI4, REF#, CR# and W# are set in the same manner as in the array active cycle shown in FIG. **89** for designating the array active cycle in the transparent output mode shown in FIG. **90**. In the array active cycle in transparent output mode, when the output enable signal G# is set to "L", an output buffer is activated and valid data are output. In array active cycle of the transparent output mode, data of the DRAM cells corresponding to the array address Aa set in array read cycle shown in FIG. **88** are output.

No. 7QL: Array Active Cycle in Latched Output Mode

Timings of control signals in array active cycle of the latched output mode shown in FIG. **91** are the same as those shown in FIG. **89**. Data (latched in an output register) read in the previous access cycle (either a cache access cycle or array access cycle) is output at first, then data read in the current array access cycle is output.

No. 7QR: Array Active Cycle in Registered Output Mode

States of control signals in the array active cycle in registered output mode shown in FIG. **92** are the same as those shown in FIGS. **90** and **91**. In the array active cycle of the registered output mode, when output enable signal G# which has been maintained at "H" is set to "L", external write data D is set to the high impedance state, and data read in the previous access cycle is output in the current cycle. In the registered output mode array access cycle, when output enable signal G# falls from "H" to "L" at the next clock cycle, data read in the current array access cycle is output.

By combining cycles shown in FIGS. **88** to **92**, output data Q in accordance with an external address can be provided from the array.

FIG. **93** shows the cycles executed when data are read from the array in transparent output mode. In FIG. **93**, numerals in circles at the upper portion of the timing diagram correspond to numbers allotted to the above description of respective cycles.

In array reading operation in the transparent output mode, the array read cycle (No. **6**) shown in FIG. **88** is executed. In this cycle No. **6**, the array address Aa is successively taken as the row address and the column address at the rising edges of the external clock signal K. Thereafter, the array active cycle shown in FIG. **89** is carried out for a prescribed number of times, for selecting rows and columns in the DRAM array. Finally, the cycle No. **7** shown in FIG. **90** is

executed, and by making output enable signal G# fall to "L", invalid data is output, and then valid data is output. In this case, access time tKHAA is approximately the same as the access time in a normal DRAM.

FIG. 94 shows the cycles carried out when data are read from the array in the latched output mode. In the array reading operation in the latched output mode also, at first the array read cycle (No. 6) shown in FIG. 88 is executed, as in the array reading operation in the transparent output mode shown in FIG. 93, and mode for reading data from the array is set. After the array address Aa has been latched by this array read cycle (cycle No. 6), array active cycle shown in FIG. 89 (cycle No. 7) is carried out for a predetermined number of times. After the array active cycle (cycle No. 7), an array active cycle in the latched output mode (cycle No. 7QL) shown in FIG. 90 is executed. When output enable signal G# which has been set at "H" falls to "L" in this cycle No. 7QL, data read by the previous access is output, and then data of the memory cell to which access is requested in the present array read cycle is output. The access time tKHAA at this time corresponds to the time required from the first rising edge of the external clock signal K to the output of memory cell data (valid) to which access is requested in the present array access cycle.

FIG. 95 shows cycles carried out when data are read from the array in registered output mode. Referring to FIG. 95, first the cycle No. 6 is executed and array read mode is set. At a rising edge of external clock signal K, the array address Aa is time divisionally latched as the row address and the column address. Thereafter, the array active cycle of cycle No. 7 is carried out for a predetermined number of times, and then the array active cycle of cycle No. 7QR is executed. In this cycle No. 7QR, after a time lapse of tQHA or tGLA which is later after the rise of the external clock signal K and after the fall of the output enable signal G# to "L", data read in the previous cycle is output as the output data Q. The access time tKHAA is the time from the first rising edge of the external clock signal K to the output of valid data in cycle No. 6.

The DRAM cells must be refreshed periodically. Setting of the refresh operation is done by an external refresh designating signal REF#. In the refreshing operation, a refresh address is generated from a refresh address counter (see counter circuit 293 of FIG. 32) in response to refresh designating signal REF# in the CDRAM, and DRAM cells are automatically refreshed in accordance with the refresh address. DRAMs having such auto-refreshing function have been known in the field of DRAMs. Timings of signals for refreshing will be described.

No. 8: Refresh Cycle

FIG. 96 shows signal timings of the refresh cycle. As shown in FIG. 86, refresh mode of the DRAM is set by setting chip select signal E# and refresh designating signal REF# to "H" and "L", respectively, at a rising edge of external clock signal K as shown in FIG. 96. When chip select signal E# is set to "H" and refresh designating signal REF# is set to "H" at a rising edge of the external clock signal K, refreshing of the DRAM is stopped. In the refresh cycle, other control signals CH#, CI#, CR# and W# may be at arbitrary states, and the output enable signal G# is set to "H". Therefore, the cache address Ac and array address Aa may be at arbitrary states. External input data D also may be set at an arbitrary state. External output data Q is set to a high impedance state.

Refreshing operation is effected only to the DRAM. Refreshing is not necessary in the SRAM. Therefore, cache (SRAM) can be accessed during the refreshing operation.

Timings where refreshing operation and access to the cache are simultaneously carried out will be described in the following.

No. 8W: Refresh Cycle With Cache Hit Writing

In cycle No. 8W, in parallel to refreshing of the DRAM, writing of data to a corresponding SRAM cell is carried out when a cache hit occurs. Setting of the refresh cycle with the cache hit writing is set by setting chip select signal E#, cache hit signal CH#, refresh designating signal REF# and write enable signal W# to "L" and by setting cache inhibition signal CI# and output enable signal GT to "H" at a rising edge of external clock signal K as shown in FIG. 97. Thus a cache hit write cycle is set and refresh cycle is set.

In the cache (SRAM), external write data D is taken and then written to a corresponding SRAM cell at a rising edge of external clock signal K, in response to active states of the cache hit designating signal CH# and write enable signal W#. In the DRAM, an internal refresh address counter is started by the refresh designating signal REF#, and refreshing operation is carried out in accordance with a refresh address from the counter.

When refresh designating signal REF# is set to "H" at a rising edge of external-clock signal K, the cache hit write cycle (cycle No. 1) shown in FIG. 81 only is carried out, and refreshing operation of the DRAM is stopped.

No. 8RT: Refresh Cycle With Cache Hit Reading in Transparent Output Mode

In cycle No. 8RT, cache hit reading is carried out in accordance with the transparent output mode, and DRAM is automatically refreshed. The cycle No. 8 is set by setting the chip select signal E#, cache hit signal CH# and refresh designating signal REF# to "L" at a rising edge of external clock signal K, and by setting cache inhibition signal CI#, command register signal CR# and write enable signal W# to "H" as shown in FIG. 98. In SRAM cache, cache address Ac at a rising edge of external clock signal K is taken and a corresponding SRAM cell is selected in response to the designation of cache hit reading. When output enable signal G# falls to "L", valid output data Q is output after a lapse of a predetermined time period.

In the DRAM, auto-refreshing is carried out in response to refresh designating signal REF#. When refresh designating signal REF# is set to "H" at a rising edge of external clock signal K in refresh cycle with cache hit reading, automatic refreshing carried out in response to refresh designating signal REF# is stopped. Therefore, in this case, cache hit read cycle in the transparent output mode which is the same as the cycle No. 2T is carried out.

No. 8RL: Refresh Cycle With Cache Hit Read in Latch Output Mode

In cycle No. 8RL shown in FIG. 89, cache hit reading in latched output mode is carried out together with auto-refreshing of the DRAM. Timing conditions of various control signals are the same as those shown in FIGS. 87 and 88. In the latched output mode, when a cache hit occurs, output enable signal G# falls to "L", then data accessed in the previous cycle is output, and successively data accessed in the present cycle is output.

No. 8RR: Refresh Cycle With Cache Hit Read Cycle in Register Output Mode

In cycle No. 8RR shown in FIG. 100, data reading is carried out in accordance with the cache hit read cycle in the registered output mode, and the DRAM is automatically refreshed. Timing conditions of various control signals are the same as those shown in FIGS. 97 and 98, and hit reading and auto-refreshing are carried out. in this cycle No. 8RR, when output enable signal G# falls to "L", output data

selected in the previous cycle is output. Thereafter, output enable signal G# is once raised to "H", and thereafter output enable signal G# is set to "L", in the next clock cycle, and then data of the SRAM cell selected in the present cycle is output.

The transparent output mode, latched output mode, registered output mode, masked write mode and D/Q separation mode of the CDRAM can be realized by setting commands for setting desired special function in the command register. Operation cycle for setting commands in the command register will be described in the following.

No. **9**: Command Register Set Cycle

FIG. **101** shows timings of various signals in command register set cycle (cycle No. **9**). The command registers set cycle is realized by setting chip select signal E#, cache inhibition signal CI#, command register signal CR# and write enable signal W# to "L" at a rising edge of external clock signal K. At this time, any one of four registers **WR0** to **WR3** of the command register is selected as shown in FIG. **77**. Command register **WR0** is selected in setting the output mode, and the kind of the output mode is selected dependent on the combination of the input data D at that time. Therefore, at a rising edge of the external clock signal K, a command address Ar and an external write data D are regarded as valid and latched. When 2 bits **Ar0** and **Ar1** of the command address AR are both 0 ("L"), the command register **WR0** is selected. When upper 2 bits **D2** (**DQ2**) and **D3** (**DQ3**) of 4 bits of external write data D are "0" ("L") and the least significant bit **D0** (**DQ0**) is "0" of 4 bits of external write data D, the transparent output mode is set.

The latched output mode is selected by setting external write data **D0** and **D1** to "1" ("H") and "0", respectively and by setting remaining 2 bits of external write data **D2** and **D3** to "0" at a rising edge of external clock signal K. The registered output mode is selected by setting command address **Ar0** and **Ar1** to "0", setting external write data **D0** and **D1** (**DQ0** and **DQ1**) both to "1" and by setting external write data **D2** and **D3** (**DQ2** and **DQ3**) both "0" at a rising edge of external clock signal K.

In the structure of the command registers shown in FIG. **77**, 8 registers are provided, enabling setting of 8 different special modes. The command register **RR0** for setting the masked write mode, and the register **RR1** for setting D/Q separation mode are selected by setting write enable signal W# to "H" at the timing shown in FIG. **91**. Dependent on the value of the command address Ar at this time, a desired mode can be selected.

FIGS. **102A** and **102B** show state transition of the CDRAM at a time of a cache miss (miss hit). FIG. **102A** shows a flow of state transition, and FIG. **102B** shows state transition between respective cycles. In FIG. **102** the cycles are denoted by cycle numbers.

Referring to FIG. **102A**, when a cache miss occurs, a copy back cycle (cycle No. **3**) shown in FIG. **85** is carried out at first. Consequently, data transfer mode from the SRAM to DRAM is set. Thereafter, array access cycle (cycle No. **7**) shown in FIG. **89** is repeated for n (n=(ta/tk)−1) times. The character ta represents cycle time of the DRAM, and tk represents cycle time of the external clock K. By repeating cycle No. **7** for n times, collective transfer of data blocks from SRAM to DRAM is completed. Thereafter, block transfer cycle (cycle No. **4**) shown in FIG. **86** is carried out. Consequently, data transfer mode from DRAM to SRAM is set. By repeating cycle No. **7** for n times successive to the cycle No. **4**, transfer of data blocks from DRAM to SRAM is carried out. Thereafter, the DRAM is ready for receiving next access. This state is referred to as a block transfer mode. From this time on, the CPU can access to SRAM or DRAM.

When array active cycle (cycle No. **7**) is repeated for n'(n'=(ta/2·tK)−1) times successive to the cycle No. **4**, restore operation to the memory cell and RS precharging are not yet completed in the DRAM, and therefore it cannot be accessed. However, in the SRAM, block data has been already transferred from the DRAM in this state, restore is not necessary, and data on the SRAM bit line pair has been established. Therefore, the CPU can access to the SRAM at this state. This state is referred to as a cache fill state. In the cache fill state, the CPU can access only to the SRAM. Either the cache hit write cycle (cycle No. **1**) shown in FIG. **81** or cache hit read cycle (cycle No. **2**) shown in FIGS. **82** to **84** is carried out after cache fill. The cache hit read cycle (cycle No. **2**) may be carried out in transparent output mode, latched output mode or registered output mode. Hit writing can be successively carried out at every clock cycle, and hit read cycle can be successively carried out at every clock cycle. The operation may be switched from the hit read cycle to the hit write cycle. Data transfer may be carried out in accordance with the high speed transfer mode (fast copy back) in which "copy back" and "block transfer" are carried out parallel to each other.

FIGS. **103A** and **103B** shows state transition at a time of array accessing. FIG. **103A** (A) shows a flow of state transition in array access, and FIG. **103B** (B) shows state transition between respective cycles. Array access includes array writing to write data to the array, and array read for reading data from the array. In array writing, array write cycle (cycle No. **5**) shown in FIG. **83** is carried out. Successive to the cycle No. **5**, the array active cycle of cycle No. **7** is repeated for n times to write data to the DRAM array.

In array reading, the array read cycle (cycle No. **6**) shown in FIG. **88** is carried out, and access to the DRAM is enabled. After the array read cycle (cycle No. **6**), the array active cycle shown in FIG. **89** (cycle No. **7**) is repeated for n' times. At this state, data cannot be read from DRAM. Subsequent to the cycle No. **7**, the array active cycle for data output (cycle No. **7Q**) shown in FIGS. **90** to **92** is repeated for n'+1 times. The cycle No. **7Q** may be the array active cycle for transparent output, array active cycle with latch output, or array active cycle with registered output.

By setting output enable signal G3 to "L" at the last cycle of the cycle No. **7Q**, data can be read from the array. The cycle times of the array writing and array reading seem to be different from each other. However, n=n'+1, and therefore reading and writing of data from and to the array can be carried out in the same clock cycles. After the array writing operation or array reading operation, array writing or array reading can be successively carried out.

FIGS. **104A** and **104B** show the state transition at a time of refreshing. FIG. **104A** is a flow of state transition of the refreshing operation, and FIG. **89B** shows state transition between respective cycles at the time of refreshing.

In normal refreshing in which auto-refreshing of DRAM only is carried out and access to SRAM is not carried out, first the refresh cycle (cycle No. **8**) shown in FIG. **96** is carried out. Thereafter, the array active cycle (cycle No. **7**) shown in FIG. **84** is repeated for n times. Consequently, one auto-refreshing operation in accordance with the refresh address from the refresh counter contained in the CDRAM is completed.

In refreshing with hit writing, the refresh cycle with cache hit writing shown in FIG. **97** (cycle No. **8W**) is carried out at first. Then, auto-refreshing of the DRAM is carried out for the n successive clock cycles. During this period, the cache hit write cycle shown in FIG. **81** can be executed by the CPU for n times.

In refresh cycle with hit reading, the refresh cycle with cache hit reading shown in FIGS. **98** to **100** (cycle No. **8**R) is carried out. Consequently, auto-refreshing of the DRAM is started, and auto-refreshing is carried out for n clock cycles in the DRAM. CPU can execute hit reading during the n clock cycles. The output mode of the cycle No. **8**R may be transparent output mode, latched output mode or registered output mode.

[Second Embodiment]

Basic constructions, arrangements and operations of CDRAM of the present invention have been described. Various modifications and additional functions can be considered, which will be described as a second embodiment in the following.

In the second embodiment, control signal CI# (cache access inhibiting signal) and a command set/burst enable signal CR#/BE# applied to the pin number **4** are defined as control signals CC1 and CC2. These signals have the same function as in the first embodiment described above, and only the names of the signals are changed. [Low Power and High Speed Operations Modes]

It is desirable to change the clock frequency according to the situation of accessing to CDRAM in terms of power consumption. For example, when only DRAM in CDRAM is successively accessed, no fast clock is needed as its operating speed is slow. So, a low clock is preferable in such situation in terms of low power consumption. If SRAM cache is successively accessed, a fast clock should be applied in terms of fast operationability. CDRAM should operate as fast as possible with least power consumption regardless of clock frequency. In order to implement such operating characteristics, DRAM address strobing timing is varied according to the clock frequency. More specifically, CDRAM is adapted to include two operation modes, i.e. low power consumption mode in which DRAM row address is latched at a leading edge of the clock K while DRAM column address is latched at the following trailing edge of the clock K, and high speed mode in which DRAM row address is latched at a leading edge of the clock K while DRAM column address is latched at another leading edge of the clock K. In the following, structure for implementing such changing of address strobe timing is described with reference to FIGS. **105** through **118**.

FIG. **105** is a block diagram showing functionally the whole structure of the CDRAM in accordance with the second embodiment. In the CDRAM shown in FIG. **105**, an address generating circuit **360** which takes external address signals Ac and Aa and generates internal addresses int-Ac and int-Aa in accordance with internal chip enable signal E, internal cache hit designating signal /CH and an internal clock signal int-K from clock buffer **254** is provided in place of address buffer **260** shown in FIG. **32**. By adjusting timings of taking addresses Ac and Aa in address generating circuit **360**, the CDRAM **5000** can be set to either one of low power consumption mode and high speed operation mode.

A row address signal and a column address signal are externally applied time divisionally to provide the DRAM internal address signal int-Aa applied to DRAM row decoder **102** and DRAM column decoder **103**. By adjusting timings for taking these address signals, the speed of operation of DRAM can be adjusted. Address generating circuit **360** generates an internal row address signal and an internal column address signal while adjusting the timing for taking the external DRAM address signal Aa in accordance with an internal control signal K (int-K) and internal control signals E and /CH.

FIG. **106** is a diagram of signal waveforms showing the operation of circuitry related to the portion generating the internal address signal int-Aa for the DRAM of this address generating circuit **360**. The operation of address generating circuit **360** will be described with reference to FIG. **106**.

An operation mode in which high speed operation is carried out with low power consumption (hereinafter referred to as a low power consumption mode) is set by setting, at time T1, the internal control signals E and CH to "H" and "L", respectively, at a rising edge of the clock signal K. At this time, address generating circuit **360** takes external address signal Aa as an internal row address signal int·Aar in response to the rising edge of the clock signal K. Then, it takes external address signal Aa in response to a falling edge of the clock K and generates an internal column address signal int·Aac. The details of this operation is as follows.

At time T1, the external address signal Aa has been already applied to address generating circuit **360** at the rising edge of the external clock signal K. At this time, in accordance with the combination of the states of the signals E and CH, an internal row address strobe signal /RAS for taking a row address signal is generated and set to an active state of "L". Since internal row address strobe signal /RAS is a signal of active "L" address generating circuit **360** latches external address signal Aa and thereafter continuously generates internal row address signal int·Aar and applies the same to DRAM row decoder **102** (time T2).

When internal row address strobe signal /RAS is at "L" at a falling edge of the external clock signal K at time T3, internal column address strobe signals CAL and /CAL are generated. In response, address generating circuit **360** takes and latches the external address signal Aa as an internal column address signal (time T4), and applies the same to DRAM column decoder **103**.

The scheme shown in FIG. **106** which DRAM row address signal int·Aar and DRAM column address signal int·Aac are taken by a single pulse of clock signal K enables faster operation of the DRAM compared with the structure of a common clock synchronized type semiconductor memory device such as shown in FIG. **107** in which operation is effected only at the rising edge of the external clock signal.

Namely, as shown in FIG. **107**, in the low power consumption mode, the row address signal and the column address signal for the DRAM are taken at time TA, at which the operation for the DRAM is started.

If all operations are determined at the same timing (rising edge) of the clock signal K as in the conventional clock synchronized type semiconductor memory device, the column address signal for the DRAM is taken at the rising edge of the next clock signal K (time TB), and from this point of taking the column address signal, the DRAM starts its operation. Therefore, even when power consumption is given priority than the speed of operation of the CDRAM and the period of the clock signal K is made longer or the clock signal K is generated intermittently in order to reduce power consumption of the CDRAM, the start point of operation of the DRAM can be made earlier by the time period (TB-TA) between TB and TA, compared with the structure of the conventional clock synchronized type semiconductor memory device. Namely, a clock synchronized type semiconductor memory device which can be operated at high speed even in the low power consumption mode can be provided.

As shown in FIG. **105**, internal operations of CDRAM are all controlled by the external control signals. Internal row address strobe signal /RAS and internal column address strobe signals CAL and /CAL shown in FIG. **106** are control signals which simply determines the timing of taking DRAM addresses in address generating circuit **360**.

Assume that the external clock signal K is generated intermittently in order to further reduce power consumption, while period of the external clock signal K is made longer so as to meet the demand of low power consumption. In this case also, by resetting the taking operation of address generating circuit **360** by utilizing internal row address strobe signal /RAS, a CDRAM which can minimize an influence of possible noise generated in such intermittent operation can be provided. Here, the intermittent operation mode corresponds to a mode in which period of the clock signal K is made longer temporarily, or a mode in which period of the external clock signal K is variable. A margin for noise pulses generated when the period of the external clock signal is long will be described.

FIG. **108** is a diagram for comparison between the conventional operation mode and the low power consumption mode. In the low power consumption mode, if a noise pulse NZ is generated in the external clock signal K, external address signal Aa is taken in the CDRAM at time TC, then external address signal Aa is taken as an internal column address signal at time TD, and the DRAM starts its operation from time TD. However, if the structure is adapted to reset address generating circuit **360** after the lapse of a prescribed time period, the operation of the DRAM terminates automatically at time TE, and malfunction caused by the noise pulse NZ can be prevented. More specifically, when external clock signal K rises at time TEa, the operation of the DRAM has been already completed and it is returned to the precharge state. Accordingly, operations in accordance with the combinations of the states of various control signals at the rising edge of the external clock signal K can be carried out, and therefore a CDRAM having sufficient margin for the malfunction of the noise pulse NZ can be provided.

When the row address signal and the column address signal are to be taken only at the rising edge of the external clock signal K as in the normal mode, and if the row address signal is erroneously taken in response to a rising edge of the noise pulse NZ at time TC, the CDRAM is kept in a waiting state for the input of the column address signal until the next rising point TEa of the external clock signal K. At this time, the CDRAM takes address signal Aa, at time TEa when the accurate external clock signal K rises, as a column address signal and starts its operation. Therefore, when an accurate external clock signal K is applied, an erroneous operation is effected. Namely, because of the longer period of the external clock signal K to reduce power consumption, margin for the noise is lost in the conventional operating mode.

As described above, by resetting the DRAM after the lapse of a predetermined time period (for example, time required till completion of the sensing operation in the DRAM array) from taking of the DRAM column address signal in address generating circuit **360**, sufficient margin for the noise can be provided even if the external clock signal K is applied intermittently.

FIG. **109** shows an example of a specific structure of address generating circuit **360** shown in FIG. **105**. Referring to FIG. **109**, address generating circuit **360** includes a row address strobe signal generating circuit **2601** responsive to control signals E and CH and to external clock signal K for generating an internal row address strobe signal /RAS; a column address strobe signal generating circuit **2602** responsive to internal row address strobe signal /RAS from row address strobe signal generating circuit **2601** and to clock signal K for generating internal column address strobe signals CAL, /CAL; a row address latch **2603** responsive to internal row address strobe signal /RAS for taking external address signal Aa to generate an internal row address signal; a column address latch **2604** responsive to internal row address strobe signal /RAS and internal column address strobe signals CAL and /CAL for taking external address signal Aa to generate an internal column address signal; and a reset signal generating circuit **2605** responsive to internal row address strobe signal /PAS for generating a reset signal after a lapse of a predetermined time period (for example, period of active state of the DRAM) to apply the same to row address strobe signal generating circuit **2601**. Here, external clock signal K and internal clock signal int-K are substantially the same signal, and in the following, internal clock signal is simply referred to as K.

The row address strobe signal generating circuit **2601** generates internal row address strobe signal /RAS when control signal E is at "H" and control signal CH is at "L" at a rising edge of (internal) clock signal K. Column address strobe signal generating circuit **2602** generates internal column address strobe signals CAL, /CAL in response to a falling edge of clock signal K. Column address strobe signal generating circuit **2602** is reset when internal row address strobe signal /RAS rises to inactive "H".

Row address latch **2603** is set to a latch state when internal row address strobe signal /RAS attains "L" and outputs continuously the latched signal as internal row address signal regardless of the state of external address signal Aa.

Column address latch **2604** takes external address Aa in response to internal row address strobe signal /RAS, and outputs applied address signal continuously as internal column address signal in response to column address strobe signals CAL, /CAL. The address generating circuit shown in FIG. **109** is related to DRAM addresses. At a time of cache hit in which SRAM array is accessed, the row address signal and the column address signal are simultaneously applied to SRAM address generating circuit (not shown). Therefore, the row address signal and the column address signal for SRAM are taken at the same timing of the external clock signal. The operation of the address signal generating circuit shown in FIG. **109** is the same as that described with reference to the diagram of signal waveforms of FIG. **106**, and therefore description thereof is not repeated. Specific structure of respective circuits in FIG. **109** will be described.

FIG. **110** shows a specific structure of row address strobe signal generating circuit **2601** shown in FIG. **109**. Referring to FIG. **100**, row address strobe signal generating circuit **2601** includes an AND circuit **2610** receiving the clock signal K, control signal E and control signal /CH (inverted signal of CH); and an OR circuit **2611** receiving at one input, the output from AND circuit **2610**, and receiving at the other input, a Q output of a flipflop (FF) **2612**. Flipflop **2612** includes a set input S receiving an output from OR circuit **2611**, a reset input R receiving a reset signal RS from reset signal generating circuit **2605** shown in FIG. **109**, a Q output and /Q output. Q output and /Q output provide signals complementary to each other.

Internal row address strobe signal /RAS is generated from /Q output from flipflop **2612**. Generally, flipflop **2612** has a circuit structure including two NOR circuits cross coupled to each other. The flipflop **2612** is set when "H" signal is applied to set input S, and outputs a signal at "L" from /Q output. When a signal at "H" is applied to reset input R, it is reset and signal output from /Q attains "H". Operation of row address strobe signal generating circuit **2601** shown in FIG. **110** will be described with reference to the diagram of waveforms of is FIG. **106**.

When control signal E is at "H" and control signal C is at "L" when clock signal K rises to "H", then the output from

AND circuit **2610** attains to "H". Consequently, the output from OR circuit **2611** rises to "H" and flipflop **2612** is set. Then, internal row address strobe signal /RAS provided as an output from /Q output of flipflop **2612** falls to "L". At this time, Q output of flipflop **2612** attains "H" and output from OR circuit **2611** attains "H". After a lapse of a predetermined time period from the generation of internal row address strobe signal /PAS, a reset signal is generated from reset signal generating circuit **2605** (see FIG. **109**), flipflop **2612** is reset and row address strobe signal /RAS rises to "H". Therefore, the row address generating circuit **360** is ready to receive the next address.

When a reset signal of "H" is applied while "H" signal being applied to set input S of flipflop **2612** having NOR gates cross coupled to each other, Q output and /Q output may both attain "L". At this time, since Q output of flipflop **2612** is applied to one input of OR circuit **2611**, the output of OR circuit **2611** attains "L". If reset signal RS has an appropriate pulse width, flipflop **2612** is kept at a stable reset state. In order to ensure operation of flipflop **2612** at this time, a one shot pulse signal may be generated when Q output of flipflop **2612** attains to "H" to apply the one shot pulse signal to OR circuit **2611** in place of Q output of flipflop **2612**. Alternatively, a circuit generating a one shot pulse having an appropriate pulse width in response to an output from AND circuit **2610** may be provided to apply the pulse from this one shot pulse generating circuit to the set input of flipflop **2612**.

FIG. **111** shows an example of a specific structure of column address strobe signal generating circuit **2602** shown in FIG. **109**. Referring to FIG. **111**, the column address strobe signal generating circuit **2602** includes an AND circuit **2621** receiving at its one input clock signal K; an inverter circuit **2622** receiving internal row address strobe signal /RAS; and a flipflop **2623** having a set input IS receiving an output from AND circuit **2621**, a reset input /R receiving an output from inverter circuit **2622**, a Q output and /Q output. /Q output of flipflop **2623** is applied to the other input of AND circuit **2621**. Column address strobe signal /CAL is generated from /Q output of flipflop **2623**, and column address strobe signal CAL is generated from the inverter circuit **2624** receiving /Q output of flipflop **2623**.

Flipflop **2623** includes two NAND circuits cross coupled to each other, for example. It is set when a signal at "L" is applied to set input /S, and it is reset when a signal at "L" is applied to reset input /R. The operation will be described.

Assume that flipflop **2623** is reset. At this time, /Q output of flipflop **2623** is at "H", and output from AND circuit **2621** is at "H" in response to the rise of clock signal K. When clock signal K falls to "L", the output from AND circuit **2621** falls to "L", flipflop **2623** is set, column address strobe signal /CAL from /Q output thereof attains "L" and column address strobe signal CAL from inverter circuit **624** attains "H". Row address strobe signal /RAS attains to "L" in response to the rise of clock signal K, and output of inverter circuit **2622** attains "H".

After a lapse of a predetermined time period, internal row address strobe signal /RAS rises from "L" to "H", and the output from inverter circuit **2622** falls to "L". Consequently, flipflop **2623** is reset, column address strobe signal /CAL attains "H" and column address strobe signal CAL attains "L".

At this time, signals to set input /S and reset input /R of flipflop **2623** may be both "L". However, such state can be prevented by providing a structure for resetting /Q output of flipflop **2623**. A circuit structure for setting Q output of flipflop **2623** as well may be provided.

Alternatively, a structure for generating a one shot pulse signal having a predetermined pulse width in response to a fall of clock signal K to provide the same to set input /S of flipflop **2623** may be used as a simple method. At this time, the generated one shot pulse signal falls from "H" to "L" upon generation.

FIG. **112** shows an example of a specific structure of row address latch **2603** shown in FIG. **109**. Referring to FIG. **102**, row address latch **2603** includes an inverter circuit **2631** receiving external address signal Aa; a clocked inverter **2632** receiving an output from inverter circuit **2631**; an inverter circuit **2633** receiving an output from clocked inverter **2632**; and a clocked inverter **2634** receiving an output from inverter circuit **2633**.

Operation of clocked inverter **2632** is controlled by internal row address strobe signals RAS and /RAS. When internal row address strobe signal RAS is at "H" and internal row address strobe signal /RAS is at "L", clocked inverter **2632** is set to an output high impedance state, which is an inactive state. When internal row address strobe signal RAS is at "L" and internal row address strobe signal /RAS is at "H", clocked inverter **2632** is rendered active, and it inverts an output from inverter circuit **2631** and transmits the same to a node **N10**.

Clocked inverter **2634** is rendered active when internal row address strobe signal /RAS is at "L" and internal row address strobe signal RAS is at "H" and it functions as an inverter. When internal row address strobe signal RAS is at "L" and internal row address strobe signal /RAS is at "H", clocked inverter **2634** is set to an output high impedance state, which is an inactive state. Therefore, when clocked inverter **2634** is active, inverter circuit **2633** and clocked inverter **2634** constitute a latch circuit, and continuously outputs signal potential appearing on the node **N10**. Internal row address signal int·Ara is generated from node **N10**. The operation will be described in the following.

When internal row address strobe signal /RAS is at inactive "H", clocked inverter **2632** functions as an inverter. At this time, clocked inverter **2634** is at the output high impedance state. Therefore, at this time, external address signal Aa is transmitted to node **N10**. When clocked inverter **2632** is set to the output high impedance state, and clocked inverter **2634** is rendered active to function as an inverter. At this state, signal potential appearing at node **N10** when the internal row address strobe signal /RAS has been "H" is latched by inverter circuit **2633** and clocked inverter **2634**, and it is continuously output as internal row address signal int·Ara.

FIG. **113** shows an example of a specific structure of column address latch **2604** shown in FIG. **109**. Referring to FIG. **103**, column address latch **2604** includes an NOR circuit **2641** receiving at one input external address signal Aa and at the other input internal row address strobe signal /RAS; a clocked inverter **2642** receiving an output from NOR circuit **2641**; an inverter circuit **2643** receiving an output from clocked inverter **2642**; and a clocked inverter **2644** receiving an output from inverter **2643**

Clocked inverter **2642** is rendered active and serves as an inverter when internal column address strobe signal CAL is at "L" and internal column address strobe signal /CAL is at "H". When internal column address strobe signal CAL is at "H" and internal column address strobe signal /CAL is at "H", clocked inverter **2642** is rendered inactive and set to the output high impedance state. Clocked inverter **2644** is rendered active and serves as an inverter when internal column address strobe signal /CAL is at "L" and internal column address strobe signal CAL is at "H". When internal

column address strobe signal CAL is at "L" and internal column address strobe signal /CAL is "H", clocked inverter 2644 is rendered inactive and set to the output high impedance state. When clocked inverter 2644 is active, inverter circuit 2643 and clocked Inverter 2644 constitute a latch circuit, which latches a signal potential appearing at node N20. An internal column address signal int·Arc is generated from node N20. The operation will be described.

When internal row address strobe signal /RAS is at "H", an output from NOR circuit 2641 is at "L". Since internal column address strobe signals CAL and /CAL have not yet been generated at this time, clocked inverter 2642 serves as an inverter and transmits a signal at "H" to node N20.

When internal row address strobe signal /RAS falls to "L", NOR circuit 2641 functions as an inverter. At this time, NOR circuit 2641 outputs an inverted signal of external address signal Aa. After a predetermined time period from a fall of the internal row address strobe signal /RAS to "L", internal column address strobe signals CAL and /CAL are generated, clocked inverter 2642 is set to the output high impedance state, and clocked inverter 2644 is rendered active and functions as an inverter. Consequently, signal potential appearing at node N20 when internal column address strobe signals CAL and /CAL are generated is continuously output as internal column address signal int·Arc.

The structures shown in FIGS. 112 and 113 correspond to portions related to 1 bit of external address signal Aa. The circuit shown in FIGS. 112 and 113 are provided for each bit of each external address signal Aa.

Reset signal generating circuit 2605 shown in FIG. 109 may have any circuit structure provided that reset pulse RS is generated after a predetermined time period from detection of a fall of internal row address strobe signal /RAS to "L". The reset signal generating circuit can be readily realized by a circuit structure including a circuit for providing a delay in row address strobe signal /RAS and a circuit for generating a one shot pulse signal in response to the output from the delay circuit.

The reset signal generating circuit 2605 may have a structure that the reset signal is generated from DRAM array driving circuit 260 shown in FIG. 105. At this time, DRAM array driving circuit 260 generates a signal for activating circuitry of a portion related to row selecting operation of the DRAM array, and the reset pulse may be generated at a time point when the operation of the circuitry related to row selection is completed. For example, a structure generating reset pulse RS after a predetermined time period from the generation of a sense amplifier activating signal for sensing operation in DRAM array 101 may be employed.

A structure for setting CDRAM to operation modes dependent on intended use, that is, high speed operation mode or low power consumption mode, will be described. Command registers are used for setting such modes.

As shown in FIG. 114, operation mode of the CDRAM is set dependent on data values of data input pins DQ3 (D3) and DQ2 (D2) when a register WR0 is selected.

When DQ3 (D3) and DQ2 (D2) are both set to "0", a first high speed mode is designated. By setting DQ3 (D3) and DQ2 (D2) to "0" and "1", respectively, a low power consumption mode is designated. When DQ3 (D3) and DQ2 (D2) are set to "1" and "0", respectively, a second high speed operation mode is designated. The input terminal is represented as DQ (D) when register WR0 is set, since pin function differs dependent on whether DQ separation mode is designated by a register RR1 or masked write mode is selected by a register RR0. Operation modes realized by data AB applied to data DQ3 (D3) and DQ2 (D2) of register WR0 will be described.

FIG. 115 shows a high speed operation mode of the CDRAM. The first high speed operation mode is selected by setting upper 2 bits of data AB of register WR0 both to "0". In this state, a row address signal (ROW) is taken at first at a rising edge of the first clock signal K (#1) of the clock signal K, and then, a column address signal (COL) is taken at a rise of a third clock signal K (43). The operation of the CDRAM is started from a falling edge of the third clock signal #3.

The second high speed operation mode is selected by setting the upper 2 bits of data AB of the command register WR0 to "1" and "0". In the second high speed operation mode, row address signal (ROW) is taken at a rising edge of the first clock signal K (#1), and column address signal (COL) is taken at a rising edge of the successively applied second clock signal K1 (#2).

Therefore, when the DRAM array is to be accessed at a cache miss of the CDRAM or the like, speed of operation can be set at an optimal value dependent on the intended use. Since time required for accessing the DRAM array can be set at an optimal value dependent on the object of processing, flexible system structure is enabled.

FIG. 116 is a diagram of signal waveforms showing an operation in which CDRAM operates in the low power consumption mode. The low power consumption mode is designated by setting upper 2 bits of AB of command register WR0 shown in FIG. 114 to "0" and "1", respectively. in the low power consumption mode, row address signal (ROW) is taken at a rising edge of clock signal K, and column address signal (COL) is taken at a falling edge of clock signal K. in this case, row and column address signals are taken responsive to a single pulse. Even if the clock signal K is generated intermittently or the period of the clock signal K is made longer temporarily and therefore the period of the clock is made longer, row and column address signals can be taken by a single clock signal. Since DRAM starts its operation immediately after the column address signal is taken, a CDRAM which operates at high speed with low power consumption can be provided.

FIG. 117 shows a circuit structure for setting a timing for taking external address signal Aa dependent on the operation mode. The circuit structure shown in FIG. 107 is used as column address strobe signal generating circuit 2602 shown in FIG. 109. More specifically, the column address strobe signal generating circuit shown in FIG. 117 is used instead of column address strobe signal generating circuit shown in FIG. 111. The above described respective circuits may be used for other circuit structures. Referring to FIG. 117, column address strobe signal generating circuit 2602' includes an AND circuit 2701 receiving, at its one input, clock signal K; and a flipflop 2702 receiving an output from AND circuit 2701 at its set input /S1 and internal column address strobe signal /RAS at its reset input /R1 through an inverter circuit 2709. An output /Q1 of flipflop 2702 is applied to the other input of AND circuit 2701. Flipflop 2702 is set or reset when a signal at "L" is applied to input /S1 or /R1.

Circuit 2602' further includes an OR circuit 2703 receiving at one input the clock signal K, an OR circuit 2270 receiving output /Q1 of flipflop 2702 and internal row address strobe signal /RAS; and a flipflop 2704 having a set input S2 receiving an output from OR circuit 2703 and a reset input R2 receiving an output from OR circuit 2710. An output Q2 of flipflop 2704 is applied to the other input of OR circuit 2703. Flipflop 2704 is set when an output from OR

circuit **2703** rises to "H", and it is reset when an output from OR circuit **2710** rises to "H".

Circuit **2602'** further includes an AND circuit **2705** receiving, at one input, clock signal K; an AND circuit **2711** receiving an output Q2 of flipflop **2704** and internal row address strobe signal RAS from inverter circuit **2709**; and a flipflop **2706** receiving at a set input /S3 an output from AND circuit **2705** and at a reset input /R3 an output from AND circuit **2711**. An output Q3 of flip flop **2706** is applied to the other input of AND circuit **2705**. Flipflop **2706** is set in response to a fall of a signal applied to set input /S3, and it is reset in response to a fall of a signal applied to reset input /R3.

Circuit **2602'** further includes an OR circuit **2707** receiving, at one input, clock signal K; an OR circuit **2712** receiving an output /Q3 of flipflop **2706** and internal row address strobe signal /RAS; and a flipflop **2708** receiving at a set input S4 an output from OR circuit **2707** and at a reset input R4 an output from OR circuit **2712**. An output Q4 of flipflop **2708** is applied to the other input of OR circuit **2707**. Flipflop **2708** is set in response to a rise of a signal applied to set input S4, and it is reset in response to a rise of a signal applied to reset input R4.

Column address strobe signal generating circuit **2602'** further includes an AND circuit **2715** receiving an Q2 output from flipflop **2704** and data B (corresponding to DQ2 shown in FIG. **114**) set in register **WR0**; an inverter circuit **2713** receiving an output /Q1 from flipflop **2702**; an AND circuit **2714** receiving an output from inverter **2713** and data A (corresponding to data DQ3 shown in FIG. **104**) set in register **WR0**; an OR circuit **2716** receiving an output from AND circuit **1714**, an output from AND circuit **2715** and an output Q4 of flipflop **2708**; and an inverter circuit **2717** receiving an output from OR circuit **2716**. Column address strobe signal CAL is generated from OR circuit **2716**, and column address strobe signal /CAL is generated from inverter circuit **2717**. The operation will be described with reference to the diagram of signal waveforms of FIG. **118**.

The operation when low power consumption mode is set will be described. At this time, data A is "0" ("L"), and data B is "1" ("H"). In this state, an output from AND circuit **2714** is "L". Flipflops **2702**, **2704**, **2706** and **2708** are at reset state. When external clock signal K rises for the first time, an output from AND circuit **2701** attains "H". At this time, in flipflop **2702**, only a signal applied to set input /S1 rises from "L" to "H", and therefore it is kept at the reset state. In response to a rise of clock signal K; internal row address strobe signal /RAS falls to "L". At this time, since flipflop **2702** is kept at the reset state, output /Q1 of flipflop **2702** is at "H", and therefore output from OR circuit **2710** is also at "L".

Even when output from OR circuit **2703** rises to "H" in response to a rise of clock signal K, flipflop **2704** is set by the output from OR circuit **2710**, so that the output Q2 attains "H". At this time, the output from AND circuit **2711** is at "L", and the output from OR circuit **2712** is at "H" (the output /Q3 of flipflop **2703** is at "H"), so that flipflops **2706** and **2708** are also maintained at the same state as the reset state. Therefore, in this state, an output from AND circuit **2715** is at "L" and the output from OR circuit **2716** is also at "L".

When clock signal K falls to "L", the output from AND circuit **2701** falls to "L", flipflop **2702** is set, and output /Q1 of flipflop **2702** falls from "H" to "L". In response, the output from inverter circuit **2713** rises to "H". Since data B is at "H" potential level, the output from AND circuit **2715** rises to "H" in response to the fall of output /Q1 of flipflop **2702** to "L". Consequently, the output from OR circuit **2716** rises, internal column address strobe signal CAL attains "H" and internal column address strobe signal /CAL falls to "L". Consequently, low power consumption mode in which row address signal and column address signal are taken at the rising and falling edges of one pulse (**#1**) of clock signal K can be realized.

A second high speed operation mode in which a row address signal and a column address signal are taken at rising edges of respective clock signals will be described. At this time, data A is set to 1 ("H") and data B is set to 0 ("L"). At this time, the output from AND circuit **2715** is fixed at "L". The output from AND circuit **2714** attains "H" when output Q2 of flipflop **2704** rises to "H". Output Q2 of flipflop **2704** rises to "H" when flipflop **2704** is released from the reset state and the output from OR circuit **2703** rises to "H". More specifically, flipflop **2704** is set when the output of OR circuit **2703** attains "H" in response to a rise of clock signal K (**#2**) which is applied after flipflop **2702** is set and /Q1 output thereof attains "L". Therefore, in the second high speed operation mode, column address strobe signal CAL is set to "H" and internal column address strobe signal /CAL is set to "L" at a rising edge of the second clock signal K (**#2**). Thus the second high speed operation mode is realized.

A first high speed operation mode in which column address is taken at a rising edge of the third clock signal K (**#3**) will be described. In this case, data A and B are both set to "0". In this state, outputs from AND circuits **2714** and **2715** are both "L". Output Q2 of flipflop **2704** rises to "H" in response to the second rise (**#2**) of the clock signal K. Consequently, the output from AND circuit **2711** attains "H" and flipflop **2706** is released from the reset state. In response to the second fall (**#2**) of the clock signal K, the output from AND circuit **2705** falls to "L", flipflop **2706** is set, and output Q3 of flipflop **2706** falls to "L". Since output /Q3 of flipflop **2706** falls to "L", the output from OR circuit **2712** attains "L", and flipflop **2708** is released from the reset state. When the output from OR circuit **2707** rises to "H" at a third rise (**#3**) of the clock signal K, the flipflop **2708** is set, and the potential of output Q4 thereof rises to "H". Consequently, the output of OR circuit **2716** attains "H". Thus the first high speed operation mode in which row address signal is taken at the rise of the first clock signal K and column address signal is taken at a rise of the third clock signal K is realized.

In any of the above described operation cycle modes, when internal row address strobe signal /RAS rises to "H" after a lapse of a predetermined time period, flipflops **2702**, **2704**, **2706** and **2708** are all reset. Flipflops **2702**, **2704**, **2706** and **2708** have the same structure as flipflops **2612** and **2623** shown in FIGS. **110** and **111**.

As described above, since the CDRAM operates in synchronization with external clock signal K, delay of cycle time derived from skews of addresses and the like can be prevented, and accurate control can be effected, compared with a method in which internal clock signals are generated by using an address transition detecting circuit.

In addition, by arbitrarily setting timings for taking the column address of the DRAM, a CDRAM which can flexibly corresponds to applications in which low power consumption is given priority and to applications in which high speed operation is given priority can be provided.

The structure for changing timings for taking the column address is not limited to apply the CDRAM and any semiconductor memory device of address multiplexing type which operates in synchronization with clock signals can be used to provide the same effect. A structure in which a row

address signal and a column address signal are applied to separate pin terminals may be used.

[Specific Operation Cycles]

CDRAM with a low power and a high speed operation modes can provide various operation cycles similar to those shown in FIGS. **81** through **84**B. The relationship between operation cycles and external control signals is summarized in a table of FIG. **119** and respective operating cycles for the low power consumption mode and the high speed operation mode are described with reference to FIGS. **120** through **161**.

FIG. **119** is a table showing operation modes of the CDRAM in accordance with the second embodiment of the present invention and states of control signals for designating respective operation modes. The operation modes of the CDRAM are set by various combinations of external control signals, that is, a chip select signal E#, a cache hit signal CH#, a write enable signal W#, a refresh designating signal REF# and control signals CC1# and CC2#. Referring to FIG. **119**, the character "H" represents a high level signal potential, and "L" represents a low level signal potential. As shown in FIG. **119**, operation modes of the CDRAM include a cache mode TH for accessing the SRAM cache; a command register set mode TG for setting command data in command registers; a standby mode TS for setting the CDRAM to a standby state; a cache miss mode DM for carrying out operation at a cache miss (miss hit); a direct array access mode TD for directly accessing the DRAM array; a refresh mode TR for refreshing the DRAM array; and a counter check mode TC for checking a counter generating row addresses for refreshing the DRAM array. Combinations of signal states and timings for setting the respective operation modes will be described in detail later with reference to diagrams of signal waveforms. The operation at a cache miss will be briefly described.

At a time of cache miss, or a miss hit, data requested by the CPU is not stored in the SRAM cache. Therefore, the requested data must be transferred from the DRAM array to the SRAM cache. This transfer is done through bi-directional transfer gate circuit (DTB) **210** shown in FIG. **105**. Data transfer operation will be described with reference to FIG. **120**. Bi-directional transfer gate **210** includes a transfer gate DTB **2** for transferring data in DRAM array **101** to SRAM array **201**, and a transfer gate DTB **1** for latching data from SRAM array **201** and for transferring the same to DRAM array **101** (see structure of data transfer gate shown in FIGS. **49** and **57**.

Assume that data D2 is stored in a region D of SRAM array **201**, and CPU requests data D1 in this region D. This is a cache miss. At this time, in accordance with the address output from the CPU, data D1 is selected from DRAM array **101** and it is transmitted to transfer gate DTB **2**. In parallel, data D2 stored in SRAM array **201** is latched in transfer gate DTB **1**. Then, data D1 which has been transferred to transfer gate DTB2 is transferred to a corresponding region D of SRAM array **201**. Data D2 is latched in transfer gate DTB **1**. After data D1 has been transferred to SRAM array **201**, CPU can access SRAM array **201**. DRAM array **101** is once set to a precharge state to receive data D2 from transfer gate DTD **1**. Then an address indicating an address in which data D2 is to be stored is applied from, for example a tag memory to DRAM array **101**, and row selection operation is effected in accordance with this address (hereinafter referred to as a miss address). After the row selecting operation, data D2 stored in transfer gate DTB **1** is transferred to the corresponding region.

Since data transfer is done in two directions in parallel as described above, even at a cache miss, CPU can access SRAM array **201** for reading/writing desired data immediately after data transfer from DRAM array **101** to SRAM array **201**, without waiting for the DRAM array **101** returning to the precharge state. Operations in respective operation modes (high speed mode, low power consumption mode) du ring data transfer will be described in detail with reference to FIG. **121**, which is a diagram of signal waveforms.

First, by setting chip select signal E# to "L" and cache hit signal CH# to "H" at a rising edge of clock signal K, an initiate cycle "H" for cache miss cycle TM is effected. In cache miss initiate cycle TMMI, an SRAM address Ac is taken as valid in the device at a rising edge of clock signal K, and a row address signal (R) out of DRAM address Aa is taken in the device. In low power consumption mode, a column address signal (C) of DRAM address Aa is taken successively at a falling edge of the clock K. In the second high speed operation mode, the column address signal (C) is taken at a rising edge of a third c lock signal K.

Then array active cycle TMMA is started at a second rise of clock signal K. In array active cycle TMMA, memory cell selecting operation is done in the DRAM array in accordance with the CPU address, and selected memory cell data is transferred to the SRAM array. After the data transfer from the DRAM array to the SRAM array, memory cells is selected in the SRAM array in accordance with the SRAM address taken in advance, and selected data Q is output. At this time, the data which has been transferred from SRAM array to the transfer gate is kept latched in the transfer gate DTB **1**. By this state, array active cycle TMMA is completed. It takes time tKHAA from the first rise of clock signal K to the output of data Q requested by the CPU, and it takes time tCAA from taking of the DRAM column address to the output of the requested data Q.

After the completion of the array active cycle TMMA a precharge cycle TMMP for precharging the DRAM is effected. During this precharge period, SRAM cache can be independently accessed. Chip select signal E# and cache hit signal CH# are set to "H" or "L" dependent on whether the SRAM is accessed or not, and data is output dependent on the accessing state at this time. Meanwhile, internal precharging operation is effected in the DRAM array, and various signal lines are precharged to desired potentials. After the completion of precharging of the DRAM array, an array write cycle TMA for writing data which has been transferred from the SRAM array to the transfer gate DTB **1** to corresponding memory locations of the DRAM array is carried out.

Array write cycle TMA is started with an initiate cycle TMAI. This initiate cycle is started by setting chip select signal E# to "L" at a rising edge of clock signal K. Consequently, a miss address applied from a tag memory, for example, is applied to the DRAM, and in the DRAM array, the applied miss address is taken as the row address signal (R) and column address signal (C) dependent on the operation mode. After the row and column address signals are taken, an array write-array active cycle for actually writing the latched data to the DRAM array and the precharge cycle TMAA are carried out.

In array active-precharge cycle TMAA, a corresponding memory cell is selected from the DRAM array in accordance with the applied miss address, and data which has been latched in bi-directional transfer gate DTBI is written to the selected memory cell and then DRAM array is subject to precharging. In parallel to the data writing cycle in the DRAM array, the CPU can independently access the SRAM array.

Cycle time of clock signal K is tK, and array cycle time of the DRAM (necessary for reading desired data by directly

accessing the DRAM array) is represented as TA. The cycle time necessary for the miss read/write cycle TMM at a cache miss must be not shorter than array cycle time ta. Similarly, cycle time of the array write cycle TMA must be not shorter than array cycle time ta.

FIG. **122** is a diagram of signal waveforms showing a cache hit reading operation in the low power consumption mode. FIG. **122** shows the cache hit reading operation (LTHR) in the transparent output mode. The cache hit reading operation is effected by setting chip select signal E# to "L", cache hit signal CH# to "L", control signal CC1# to "L", refresh designating signal REF#, control signal CC2# and write enable signal W# to "H" at a rising edge of clock signal K. At this time, SRAM address (CPU address) Ac is taken at the rising edge of the clock signal K and the SRAM cache is accessed. By making output enable signal G# fall from "H" to "L", data Q1 corresponding to the taken SRAM address C1 is output after the lapse of time tKHA from the rising edge of the clock signal K.

In the hit read cycle THR at a cache hit, only the SRAM cache is accessed, and data is output in the same clock cycle of the clock signal K. Control signal CC1# is set to "L" only in the first hit read cycle, in order to execute a data transfer array write cycle in the DRAM array. A plurality of cycles are necessary as the DRAM array cycle time, and from this time on, array write cycle is effected in the DRAM, and therefore, control signal CC1# is kept at "H" in the subsequent hit read cycle. When output enable signal G# is at "L", an output from the data input/output circuit shown in FIG. **105** (see also FIG. **37**) is transmitted to the data output pin. Therefore, in the second hit read cycle, data Q2 corresponding to the address C2 is output after the SRAM address C2 is taken and after the output of invalid data. When output enable signal G# is at "H", the output data pin D/Q is set to the high impedance state. In the following description, the CDRAM is in the masked write mode, and arrangement of a pin M# for receiving masked data and a DQ pin for commonly carrying out data input/output is shown as an example.

FIG. **123** is a diagram of signal waveforms showing the cache hit writing operation in low power consumption. The cache hit mode THW is effected by setting chip select signal E#, cache hit signal CH# and write enable signal W# to "L" and setting control signals CC1#, CC2# and refresh designating signal REF# to "H" at a rising edge of clock signal K. At this time, output enable signal G# is set to "H". In this state, SRAM address signal C1 is taken at a rising edge of the clock signal K, and data D1 which has been applied to data input/output pin DQ is taken. If it is in the masked write mode, the data which is to be written at this time can be masked by setting the signal potential applied to data pin M# to "H" or "L". Since access to the SRAM array only is done in the cache hit write mode THW in the cache hit writing operation, the cycle time of the hit write mode THW is the same as the cycle time tK of clock signal K.

FIG. **124** is a diagram of signal waveforms showing a cache miss reading operation in the low power consumption mode. The cache miss reading operation is started with a miss initiate cycle TMMI. This initiate cycle TMMI is started by setting chip select signal E# to "L" and other control signals CH#, CC1#, REF#, CC2#, W# and G# to "H" at a rising edge of clock signal K. In the initiate cycle TMMI, first an SRAM address Ac1 is taken for designating an address of the SRAM array, and, at the same time, the same address is taken as the DRAM array address signal Aa. At this time, 16 bits (16 bits×4) of data are simultaneously transferred for one memory cycle. Since the output data includes 4 bits, the necessary address bits except the lower address bits out of the address (CPU Add) applied from the CPU, are applied as the DRAM address signal Aa.

For the operation with low power consumption, the DRAM address signal Aa is taken as the row address (ROW) at a rising edge of clock signal K, and a column address signal COL is taken at the falling edge of this clock signal K. At this state, memory cell selecting operation is effected in the SRAM array and the DRAM array, and corresponding memory cell data are transferred from the DRAM to the SRAM array. Data selecting operation in the DRAM array is carried out by setting the array active cycle TMMA. The array active cycle TMMA is designated by setting all control signals to "H" at a rising edge of clock signal K.

By making the output enable signal G' fall to "L" in array active cycle TMMA, data Q1 selected in accordance with the address signal C1 in the SRAM array is output after a lapse of a predetermined time period. After the completion of the array active cycle in the DRAM array, the operation must be once changed to the precharge cycle for writing data which has been read from the SRAM array and latched in the bi-directional transfer gate circuit to the DRAM array. For setting the precharge cycle TMMP at a miss read, the same combination of signals as to designate standby or cache hit operation TK is used at a rising edge of clock signal K. When chip select signal E# is set to "L" while setting cache hit signal CH# to "L" at this time, data can be read from the SRAM array while the DRM array is in the precharge cycle.

FIG. **125** is a diagram of signal waveforms showing a cache miss writing operation in the low power consumption mode. The cache miss writing operation is realized by setting the chip select signal E# and write enable signal W# to "L" at a rising edge of clock signal K. At this time, initiate cycle TMMI for cache miss writing operation is effected at first. The cache miss writing operation is the same as the cache miss reading operation shown in FIG. **124** except that the direction of data flow is different. After corresponding data are transferred from the DRAM array, or simultaneously with the data transfer, writing of data D1 to the corresponding memory cell in accordance with the address signal C1 for the SRAM array is carried out. The only difference between cache miss writing and cache miss reading is that the write enable signal W# is at "L" or not.

FIG. **126** is a diagram of signal waveforms showing an array writing operation. In the array writing operation; data which has been transferred from the SRAM array to the bi-directional transfer gate circuit to be latched therein is written to the corresponding memory cell of the DRAM array. The array writing operation cycle LTMA includes initiate cycle TMAI and array active cycle TMAA. The initiate cycle TMAI is set by setting chip select signal E# and control signal CC2# to "L" and control signal CH#, CC1# to "H" at a rising edge of clock signal K. In this initiate cycle TMAI of the array writing operation cycle LTMA in the low power consumption mode, an address signal (MissAdd) applied from an external device such as a tag memory is taken corresponding to the rising and falling edges of the clock signal K, and internal row address and column address signals are generated responsively. Successive to the initiate cycle TMAI, chip select signal E# and cache hit signal CH# are set to "L" and control signal CC1# is set to "H" at a rising edge of the clock signal K. Thus array active cycle TMMAA as well as cache hit operation are set. At this time, when write enable signal W# is set to "L", the SRAM address signal Ac is taken, and data is written to the SRAM cell corresponding to the taken address C2. At this time, masked data M#, may be applied. In the array active cycle

TMAA in the array writing operation, DRAM memory cell is selected in accordance with the taken address, and data which has been latched in the bi-directional transfer gate is written to the selected DRAM memory cell.

FIG. **127** is a diagram of signal waveforms showing array writing operation accompanied with cache hit reading operation. Array writing operation accompanied with cache hit reading in the low power consumption mode is shown, and in this cycle LTMAR, reading of data from the SRAM cache is carried out in parallel with data transfer from the bi-directional transfer gate to the DRAM array.

This operation cycle LTMAR is set by setting chip select signal E#, control signal CC1# and cache hit signal CH# to "L" and by setting control signal CC2# and write enable signal W# to "H" at a rising edge of clock signal K. Since refreshing is not carried out, the refresh designating signal REF# is at "H". By the setting of these signals, the initiate cycle TMAI of the array writing operation is effected together with the cache read cycle THR. More specifically, in this operation mode, the SRAM address signal Ac is taken at first at the rising edge of the clock signal K, and corresponding data Q1 is output.

The DRAM address signal Aa is taken as the row address signal and the column address signal at the rising edge and the falling edge of the clock signal K, respectively. An address signal (MissAdd) from an externally provided tag memory, for example, is applied as the DRAM address signal Aa for selecting a memory cell to which the data which has been latched in the bi-directional transfer gate is to be written. In this manner, data transfer operation to the DRAM array is carried out in parallel with the cache reading operation of the SRAM array.

The array write cycle is carried out by setting the array active and precharge cycle DMAA. The array active/precharging operation in the array writing operation accompanied with cache hit reading is set by setting chip select signal E# to "L", cache hit signal CH# to "L" and control signals CC1# and CC2# both to "H".

FIG. **128** is a diagram of signal waveforms showing an array write operation cycle LTMAW accompanied with cache hit writing in the low power consumption mode. The array write operation cycle LTMAW accompanied with cache hit writing is set by setting chip select signal E#, cache hit signal CH# and control signal CC1# to "L" and setting control signal CC2# and refresh designating signal REFR to "H" at a rising edge of clock signal K. By setting the signals to such states, the array write initiate cycle TMAI and hit writing cycle THW are set. In response, the SRAM address signal Ac for selecting the SRAM array is taken at the rising edge of clock signal K, and the DRAM address signal Aa is taken at a rising edge of clock signal K.

The DRAM address signal Aa is also taken at a falling edge of the clock signal K and an internal column address signal is generated. Since it is an array writing operation, the DRAM address signal Aa is not the address applied by the CPU for writing data which caused cache miss but the address MissAdd applied by an external device such as a tag memory. The array write operation cycle LTMAW accompanied with cache hit writing is the same as the array write operation cycle LTMAR accompanied with cache hit reading shown in FIG. **127** except that the state of the write enable signal W# is different. Namely, data is written to the SRAM array in accordance with the CPU address in parallel with transfer of data which has been latched in the bi-directional transfer gate to the DRAM array.

FIG. **129** is a diagram of signal waveforms showing a direct array read operation cycle LTDR in the low power consumption mode. In the direct array read operation cycle LTDR, the DRAM array can be directly accessed to read the corresponding memory cell data of the DRAM. The direct array read operation cycle LTDR is started by setting chip select signal E# and control signal CC1 to "L" and setting control signal CC2# to "H", cache hit signal C1#, write enable signal Wr and refresh desianatina signal REF# to "H" at a rising edge of the clock signal K. By setting these signals to such states, an initiate cycle TDI of the direct read array cycle LTDR is set.

In the initiate cycle TDI, DRAM address signal Aa is taken as the row address signal (ROW) at a rising edge of clock signal K, and successively, 4 bits of address signals Aac **0** to Aac **3** applied to the SRAM address terminal and the DRAM address signal Aa are taken at a falling edge of the clock signal K. The SRAM address signal is also used in the direct array read operation from the following reason.

Generally, in array accessing, 16 bits of data are transferred simultaneously per 1 memory block. In case of a 4M bit DRAM, 16 bits×4 data are transferred. Therefore, a total of 16 bits of row address signals and column address signals only are applied generally. Therefore, in direct array read operation, SRAM address signals Aac **0** to Aac **3** are -taken as lower address signals for further selecting 4 bits from 16×4 bits of memory cells. A structure for selecting 4 bits of data from the SRAM column decoder in accordance with the taken 4 bits of SRAM address signals Aac **0** to Aac **3** may be used. In that case, the data selected in the DRAM is transmitted and selected through a SRAM bit line. Other structure may be used.

Thereafter, the array active/precharge cycle TDA is executed in which the memory selecting operation and the data reading operation in the DRAM array are carried out. For setting the array active/precharge cycle TDA in the direct array read operation, all control signals are set to "H". The output timing of the output data Q1 is determined by output enable signal G#. Consequently, the direct array read operation cycle LTDR in which the DRAM array is directly accessed to read memory cell data therefrom is completed.

After the completion of the direct array read operation cycle LTDR, by setting chip select signal E# and cache hit signal CH# to "L" at a rising edge of clock signal K, memory cell reading operation in accordance with the SRAM address signal Ac is effected.

FIG. **130** is a diagram of signal waveforms showing a direct array write operation cycle LTDW in the low power consumption mode. In the direct array write operation cycle LTDW shown in FIG. **130**, data is directly written to the DRAM array in accordance with an external address signal. The direct array write operation cycle LTDW is set by setting chip select signal E#, control signal CCI# and write enable signal W# to "L" and by setting cache hit signal CH#, refresh designating signal REF#, control signal CC2# and output enable signal G# to "H" at a rising edge of clock signal K. The direct array write operation cycle LTDW is the same as the direct array read operation cycle LTDR shown in FIG. **129** except that write enable signal W# is set to "L" at a rising edge of clock signal K. At this time, the data T1 applied at the rising edge of the clock signal K is written to the DRAM memory cell selected in accordance with the DRAM address signal Aa and 4 bits of SRAM address signals Aac **0** to Aac **3**.

The direct array write operation cycle LTDW includes an initiate cycle TDI and the array active/precharge cycle TDA for actually activating the DRAM array. The array active/precharge cycle TDA is the same as the array active cycle TDA shown in FIG. **129**. After the lapse of the DRAM access cycle time ta, the SRAM cache can be externally accessed.

FIG. 131 shows the refresh array operation. In the refresh array operation mode LTR, the DRAM array is refreshed under control of refresh control circuit 292 and counter 291 shown in FIG. 105. In this case, a refresh row address indicating a row to be refreshed is generated from counter 291 shown in FIG. 105. The refresh cycle is designated by setting refresh designating signal REF# to "L" at a rising edge of clock signal K.

Consequently, a refresh initiate cycle TRI is set; and from the next rise of the clock signal K, the array active cycle TRA for actually refreshing the DRAM array is executed. In the array active cycle TRA in the refresh array operation mode LTR, all control signals are set to "H". FIG. 131 shows an example in which cache hit reading operation is carried out after the completion of refreshing.

FIG. 137 is a diagram of signal waveforms showing the refresh array operation mode accompanied with cache hit reading in the low power consumption operation. The refresh array operation is carried out only for the DRAM array, and refreshing of the SRAM array is not necessary. Therefore, in parallel with the refresh array operation, the SRAM array can be accessed for reading data. In the refresh array operation mode LTRR accompanied with the cache hit reading is started by setting chip select signal E, cache hit signal CH# and refresh designating signal REF# to "L" and by setting control signals CC1#, CC2# and write enable signal W# to "H" at a rising edge of clock signal K.

By the refresh designating signal REF#, refreshing of the DRAM array is designated, and by chip select signal E# and cache hit signal C1#, the cache hit operation is designated. At this time, auto-refreshing operation is carried out in the DRAM array in accordance with an output from a built-in address counter. Successive to the refresh initiate cycle TRI, the DRAM array is refreshed in the array active cycle TRA in accordance with the refresh row address. In the SRAM array, data is read in accordance with an externally applied address signal Ac.

FIG. 133 is a diagram of signal waveforms showing a refresh operation mode with cache hit reading in low power consumption mode. The refresh operation mode LTRW accompanied with cache hit writing shown in FIG. 133 is the same as the refresh array operation accompanied with the cache hit read ing shown in FIG. 132 except that write enable signal W# falls to "L". In this case, data is written in the SRAM array in accordance with the address signal Ac, and DRAM array is refreshed in accordance with the refresh address in the DRAM array.

FIG. 134 is a diagram of signal waveforms showing a counter check reading operation in the low power consumption mode. The counter check read operation mode LTCR is an operation mode for testing whether or not the address counter generating the refresh row address for refreshing the DRAM array functions properly. The counter check read operation mode LTCR is started by setting chip enable signal E#, control signal CC1# and refresh designating signal REF# to "L" and control signal CC1# and write enable signal W# to "H" at a rising edge of clock signal K. In the counter check read operation mode LTCR, lower 4 bits Aac 0 to Aac 3 of the SRAM address signal Ac are taken as the lower 4 bits of the column address signal of the DRAM array at a rising edge of clock signal K in initiate cycle TCI thereof.

Thereafter, DRAM address signal Aa is taken as a column address signal (upper column address bits) at a falling edge of the clock signal K. In case of a 4M bit DRAM array, 10 bits of column address signal are necessary for selecting 4 bits of memory cells. At that time, only 6 bits are applied as the column address in the DRAM as described above. Therefore, the remaining 4 bits are taken from the SRAM address signal pins. Then, by setting the respective control signals to "H" at a rising edge of the clock signal K, memory cell selecting operation is carried out in the DRAM array in accordance with the taken column addresses, and selected memory cell data are read. By comparing the read data with predetermined data or written data, it can be determined whether or not the refresh row address counter functions properly.

FIG. 135 is a diagram of signal waveforms showing the counter check writing operation in the low power consumption mode. To start the counter check write operation mode LTCW, chip select signal E#, control signal CC1#, refresh designating signal REF# and write enable signal W# are set to "L" and cache hit signal CH# and control signal CC2# are set to "H" at a rising edge of clock signal K. At this time, the states of control signals in this mode are the same as those in the counter check read operation mode LTCR shown in FIG. 134 except that the write enable signal W# is set to "L". After counter check writing operation is set in the initiate cycle TCI, an array active cycle CTA for actually accessing the DRAM array is executed. In the array active cycle, an address from the refresh row address counter is taken as the row address, external addresses Aac 4 to Aac 9 and Aac 0 to Aac 3 are taken as the column address signal to carry out row and column selecting operations, and externally applied data are written to the selected DRAM memory cells.

FIG. 136 is a diagram of signal waveforms showing a command register setting operation in the low power consumption mode. The command register setting operation mode LTG shown in FIG. 136 is an operation mode for writing desired data to the command register 270 shown in FIG. 105. By utilizing the command register setting operation mode LTG, the CDRAM can be set to the low power consumption mode, the first high speed operation mode, the second high speed operation mode, the masked write mode, DQ separation mode and the like. The command resister setting cycle LTG is designated by setting chip select signal E#, control signals CC1# and CC2# and write enable signal W# to "L" (or "H"), and setting refresh designating signal REF# to "H" at a rising edge of clock signal K. By this setting of the operation mode, a command address signal Ar is taken and a corresponding command register is selected. If write enable signal W# is at "L" at this time, data is written to the register WR0 for designating write mode/output mode, for example. If write enable signal W# is at "H", any of the registers RR0 to RR3 included in the command register is selected in accordance with the command address bits Ar0 and Ar1. FIG. 136 shows writing of data to any of the command registers WR0 to WR3, as an example. The command register setting operation mode LTG has its set cycle T1 completed in 1 cycle of the clock signal K.

FIG. 137 shows an example of an operation sequence in the CDRAM in the low power consumption mode. In the operation sequence of FIG. 137, an operation at a cache miss is shown as an example. When a cache miss reading occurs, only the chip select signal E# is set to "L" at a rising edge of clock signal K. Consequently, the initiate cycle TMMI of cache miss reading is carried out, the SRAM address signal C1 and address signal Aa (CPU address) for the DRAM array are taken, and thereafter, the array active cycle TMMA for the time of miss read is effected. In the array active cycle and the time of a miss read, memory cell data selected in the DRAM array are transmitted to the memory cells of the SRAM array, and memory cell data corresponding to the SRAM address signal C1 applied at the cache miss is read as the output data Q1 at the last cycle of miss reading.

In the DRAM array, the remaining precharge cycle TMMP of the miss read operation cycle TMMR is carried out. In this precharge cycle, the SRAM array can be accessed by the CPU. In FIG. 137, hit read operation is set simultaneously with the setting of the precharge cycle, and data Q2 is read in accordance with address signal C2.

Successive to the precharge cycle, an array write cycle for writing in DRAM array data which has been transferred from the SRAM array to the bi-directional transfer gate and has been latched therein is effected. If a hit write cycle is being carried out in parallel, the array write cycle is set by setting chip select signal E#, cache hit signal CH#, control signal CC1# and write enable signal W# to "L" at a rising edge of clock signal K. Consequently, the DRAM enters the array access cycle TMAA, memory cell selecting operation is carried out in accordance with an address MissAdd from a tag memory, for example, and data is transferred from the bi-directional transfer gate to the selected DRAM memory cell.

In the SRAM array, data D3 is written to the memory cell selected in accordance with SRAM address signal C3. In the array write cycle in the DRAM array, hit read cycles are continuously carried out in parallel, and output data Q4, Q5 and Q6 corresponding to SRAM address signals C4, C5 and C6 are output. After the hit reading, generation of clock signal K is stopped to reduce power consumption. This state is shown as a standby state in FIG. 137.

FIG. 138 shows another example of the operation sequence in the low power consumption mode. FIG. 138 shows a cache miss writing operation and successive cache hit operation. When a cache miss writing occurs, an initiate cycle TMMI of the cache miss write cycle is effected. At this time, chip select signal E# and write enable signal W# are set to "L". Consequently, address signals for selecting memory cells in the SRAM array and the DRAM array are taken. Thereafter, the array active cycle is effected, and data are transferred from the DRAM array to the SRAM array.

After the completion of data transfer or in parallel with data transfer, data D1 which have caused cache miss writing is written to the corresponding location in the SRAM array. After the completion of the array active cycle, precharge cycle of the DRAM array is carried out. At this time, hit read operation THR is effected for the After the precharging operation, an array write cycle for writing, to the DRAM array, data which has been transferred from the SRAM array to the bi-directional transfer gate is carried out.

In the initiate cycle TMAI in the array write cycle, cache hit cycle TH is also carried out simultaneously, and therefore control signal CC1# is set to "L". After the completion of the initiate cycle TMI in array writing, the array active and precharge cycle is carried out. In parallel with this array write cycle, hit writing operation, hit read operation and hit writing operation are carried out. If the CDRAM is not accessed after a lapse of a predetermined time period, the cycle of the clock signal K is made longer, or clock signal K is generated intermittently.

As shown in FIGS. 137 and 138, 2 cycles of clocks signal K are taken for the DRAM array write cycle. Meanwhile, only 1 clock is necessary for accessing the SRAM array. Therefore, the CDRAM operates at a relatively low speed, and low power consumption is given priority to high speed operation.

FIG. 139 is a diagram of signal waveforms showing cache hit reading operation in the high speed operation mode. FIG. 139 shows data output in the transparent output mode for the cache hit read operation mode THR under the high speed operation mode. The cache hit reading operation mode THR in the high speed operation mode has signal waveforms the same as those in the cache hit reading operation mode LTHR in the low power consumption mode shown in FIG. 122, and therefore detailed description thereof is not repeated. FIG. 139 shows data input/output terminals in the DQ separation mode. More specifically, input data D and output data Q are input and output through separate pin terminals.

FIG. 140 shows a diagram of signal waveforms showing cache hit reading operation in which data is output in latched output mode. The cache hit read operation mode THRL shown in FIG. 140 is carried out in the high speed operation mode. The combinations of control signals for setting this operation mode are the same as those shown in FIG. 139. The cache hit read operation mode THR shown in FIG. 139 differs from cache hit read operation mode THRL in the latched output mode in that timings of output data are different. More specifically, in the latched output mode, data read in the last cycle is output in an invalid data period of the waveform of the output data Q shown in FIG. 139. Namely, the data read in the last cycle is continuously output until valid data is output in the next cycle. In the latched output mode, invalid data is not output, and therefore stable data processing operation is possible

FIG. 141 is a diagram of signal waveforms showing a cache hit read operation mode in registered output mode in high speed operation made. The cache hit read operation mode THRR in the registered output mode is realized by the same combination of signal states as that for the operation modes THR and THRL shown in FIGS. 139 and 140. Different from the transparent output mode (see FIG. 139) and latched output mode (see FIG. 140), memory cell data selected in the previous cycle is output in synchronization with clock signal K in the registered output mode. in the register output mode, data read in the last cycle is output in synchronization with the clock signal, and therefore it is suitable for pipe line application.

FIG. 142 is a diagram of signal waveforms showing cache hit writing operation in the high speed operation mode. The cache hit write operation mode THW shown in FIG. 142 is realized by the same combination of signal states as in the cache write operation LTHW in low power consumption mode shown in FIG. 123, and therefore, description thereof is not repeated.

FIG. 143 is a diagram of signal waveforms showing cache miss reading operation in the high speed operation mode. In the cache miss read operation mode TMMR in the high speed operation mode, the initiate cycle TMMI is completed in 1 clock cycle. However, in the high speed operation mode, the column address is taken at a rising edge of a third clock signal K. This is the difference from the cache miss read operation mode LTMMR in the low power consumption mode shown in FIG. 124.

FIG. 144 is a diagram of signal waveforms showing cache miss reading operation in latched output mode in the high speed operation mode. The cache miss read operation mode TMMRL shown in FIG. 144 is the same as the cache miss read operation mode TMMR shown in FIG. 144 except that data Q0 read in the last cycle is output in a period of the output data Q in which invalid data were otherwise to be output. Except this point, the operation is the same as FIG. 143.

FIG. 145 is a diagram of signal waveforms showing cache miss reading operation in the registered output mode in the high speed operation mode. The cache miss read operation mode TMMRR shown in FIG. 145 is the same as operation modes TMMR and TMMRL shown in FIGS. 143 and 144, except the timing of output of the output data Q. Namely, in

the latched output mode, data read in the last cycle is kept continuously output in the period at which invalid data were otherwise to be output, and after a lapse of a prescribed time period from the fall of clock signal K, the signal read in the present cycle is output.

In the registered output mode, data is output in synchronization with clack signal K. If clock signal K rises in a short period of time from the fall of output enable signal G#, data read in the last cycle is output in response to the rise of clock signal K. Except this point, the operation is the same as those in FIGS. **143** and **144**.

FIG. **146** is a diagram of signal waveforms showing cache miss writing operation in high speed operation mode. The cache miss write operation mode TMMW shown in FIG. **146** is the same as the cache miss write operation mode LTMMW shown in FIG. **125** except the timing for taking the DRAM address signal Aa as a column address signal. In this case also, the array active cycle TMMA is effected after the completion of the initiate cycle TMMI. After the completion of the array active cycle TMMA, the precharge cycle TMMP is carried out.

FIG. **147** is a diagram of signal waveforms showing array write operation in the high speed operation mode. The array write operation mode TMA shown in FIG. **147** is the same as the array write operation mode LTMA in the low power consumption mode shown in FIG. **126** except the timing for taking the column address signal (COL) of the DRAM address signal. In the array write operation mode TMA in the high speed operation mode, cache hit write operation is effected prior to column selection in the DRAM. The fact that array write operation is carried out means that data transfer to the SRAM has already been completed. Therefore, the SRAM cache can be accessed at this time.

FIG. **148** is a diagram of signal waveforms showing array write operation accompanied with cache hit reading in the high speed operation mode.

The combination of states of control signals in the array write operation mode TMAR accompanied with cache hit reading shown in FIG. **148** is the same as that in the array write operation mode LTMAR in the low power consumption mode shown in FIG. **126** except the timings for taking the column address signal for accessing the DRAM array.

FIG. **149** is a diagram of signal waveforms showing array write operation accompanied with cache hit reading in the latched output mode in the high speed operation mode. Signal states in the array write operation mode TMARL accompanied with cache hit reading in the latched output mode are the same as those in the array write operation mode TMAR accompanied with cache hit reading shown in FIG. **148** except the timing of appearance of the output data Q. Namely. in the latched output mode, in place of the output data Q shown in FIG. **148**, data read in the last cycle are continuously output in the period in which invalid data were to be output. Except this point, the operations are the same.

FIG. **150** is a diagram of signal waveforms showing array write operation accompanied with cache hit reading in registered output in high speed operation mode. The array write operation mode TMARR accompanied with cache hit reading shown in FIG. **150** is the same as the array write operation modes TMAR and TMARL shown in FIGS. **148** and **149** except the output timing of data. In the registered output mode, data read in the last cycle is output in response to a rise of clock signal K.

FIG. **151** is a diagram of signal waveforms showing array write operation accompanied with cache hit writing in the high speed operation mode. The combination of the states of control signals in the array write operation mode TMAW accompanied with cache hit writing shown in FIG. **151** is the same as that of array write operation mode LTMAW shown in FIG. **128**, except the timing of taking the column address signal as an address for accessing the DRAM array.

FIG. **152** is a diagram of signal waveforms showing direct array read operation in the high speed operation mode. The combination of states of control signals in the direct array read operation mode TDR shown in FIG. **152** is the same as that of the direct array read operation mode LTDR shown in FIG. **129** except the timing of taking the column address signal out of the DRAM address signals. Therefore, the description thereof is not repeated.

FIG. **153** is a diagram of signal waveforms showing direct array write operation in the high speed operation mode. The combination of states of control signals in the direct array write operation mode TDW shown in FIG. **153** is the same as that of the direct array write operation mode LTDW in the low power consumption mode shown in FIG. **130** except the timing of taking a column address signal for accessing the DRAM array. Therefore, the description thereof is not repeated.

FIG. **154** is a diagram of signal waveforms showing refresh array operation in the high speed operation mode. The refresh array operation mode TR shown in FIG. **154** is completely the same as the refresh array operation mode LTR in the low power consumption mode shown in FIG. **131**, and therefore the description thereof is not repeated.

FIG. **155** is a diagram of signal waveforms showing refresh operation accompanied with cache hit reading in the high speed mode. The refresh operation mode TRR accompanied with cache hit reading shown in FIG. **155** is completely the same as the refresh array operation mode LTRR accompanied with cache hit reading showing in FIG. **132**. Therefore, the detailed description thereof is not repeated.

FIG. **156** is a diagram of signal waveforms showing refresh operation accompanied with cache writing in the high speed operation mode. The combination of states of control signals in the refresh operation mode TRW accompanied with cache writing shown in FIG. **156** is the same as that of refresh operation mode accompanied with cache hit writing shown in FIG. **133**. Therefore, the description is not repeated.

FIG. **157** is a diagram of signal waveforms showing counter check operation in the high speed operation mode. The counter check operation mode TCR shown in FIG. **157** is the same as the counter check read operation mode LTCR in the low power consumption mode shown in FIG. **134** except the timings for taking column address signal bits Aac **4** to Aac **9**. Therefore, description thereof is not repeated.

FIG. **158** is a diagram of signal waveforms showing counter check writing operation in the high speed operation mode. The counter check write operation mode TCW shown in FIG. **158** is the same as the counter check write operation mode LTCW shown in FIG. **135** except the timings for taking the column address signal bits Aac **4** to Aac **9**, and the combination of the states of control signals is the same.

FIG. **159** is a diagram of signal waveforms showing command register setting operation in the high speed operation mode. The combination of the states of control signals in the command register setting operation mode TG shown in FIG. **159** is the same as that of the command register setting operation mode LTG shown in FIG. **136**.

As described above, in the high speed operation mode, only the timings for taking column address signals for accessing the DRAM array are different when access to the DRAM array is necessary, and various operations can be readily realized by the same combinations of the control

signals for the respective operation modes in the low power consumption mode.

FIG. 160 shows an example of an operation sequence of the CDRAM in the high speed operation mode. In the operation sequence shown in FIG. 160, access to the cache (SRAM) is effected in parallel with miss read operation, when a miss read occurs, as an example. At a time of miss read, the SRAM array and the DRAM array are both accessed as in the case of FIG. 137. At this time, different from the low power consumption mode shown in FIG. 137, the column address signal COL 1 for accessing the DRAM array is taken at a third rising edge of the clock signal. When data transfer from the DRAM array to the SRAM array is completed according to the miss read operation mode TMM, the precharge cycle starts in the DRAM array. Before the start of the precharging, reading of data Q1 in accordance with the address signal C1 is completed. Hit read operation is effected in parallel with the precharge cycle.

The hit read operation is shown carried out three times in the precharge cycle. In the high speed operation mode, the clock signal is applied three times in the precharge cycle, and signals C2, C3 and C4 are applied as the SRAM array address signals Ac in the respective clock cycles, so that output data Q2, Q3 and Q4 are output. After the completion of the precharging operation, the array write operation is carried out. In parallel with the array writing operation, hit write operation, hit read operation and hit read operation are shown carried out in the SRAM array.

Therefore, in the high speed operation mode shown in FIG. 160, the period of the clock signal K is short, and data can be read at high speed by accessing the SRAM array while the DRAM array is being accessed.

FIG. 161 shows another example of the operation sequence in the high speed operation mode. An operation at a time of miss writing is shown as an example. In the operation sequence shown in FIG. 161, the miss writing operation is effected instead of the miss reading operation shown in FIG. 160, and the operation sequence is similar. The hit read cycle, hit read cycle and hit write cycle are shown carried out during precharging after the completion of array access, and in the array access cycle after the completion of the precharging, the hit read cycle, the write cycle and hit read cycle are shown carried out again.

Each operation cycle includes a command register cycle and an array active precharge cycle, and each cycle is determined by the execution of the initiate cycle.

[Other Example of Refresh Structure]

(Auto refresh/Self refresh Architecture)

In the CDRAM described above, refreshing is externally designated by the signal REF#. In other words, CDRAM carries out auto-refreshing. There is another refreshing scheme called self-refreshing in which refresh timing is internally set. In general, an external device is not signaled of refreshing timing in the self-refreshing operation. In the following, a construction by which refresh timing can be known externally even in self refreshing is described with reference to FIGS. 162 through 175. In the described construction, a pin terminal is selectively set to an input terminal pin for receiving a signal REF# or to an output pin terminal for supplying a signal BUSYT indicating refreshing operation. If the pin serves as the input terminals, auto-refreshing is carried out. If the pin serves as the output terminal, self-refreshing is carried out. Such a compatible auto-refreshing/self refreshing architecture can also apply to a DRAM.

FIG. 162 shows another example of the refresh method of the CDRAM in accordance with the present invention. Portions corresponding to the circuit structure shown in FIG. 32 are denoted by the same reference characters in FIG. 162. In the CDRAM structures shown in FIGS. 32 and 105, refreshing is carried out in accordance with an externally applied refresh designating signal REF#. Namely, only auto-refresh can be done in the CDRAM shown in FIGS. 32 and 105. A structure allowing self refreshing in the normal mode will be described.

Referring to FIG. 162, the CDRAM includes a clock generator 3100 taking external control signals CR#, CH#, EH# and W# in response to an internal clock int-K from clock buffer 254 for generating various control signals; a command register 270a for setting the refresh mode of the CDRAM to auto-refresh or self refresh; and an input/output switching circuit 3102 in response to a command signal CM from command register 270a for setting a pin terminal 3110 to an input terminal or an output terminal. The pin terminal 3110 corresponds to the pin terminal of pin number 44 shown in FIG. 31. Pin terminal 3110 receives external refresh designating signal REF# when it is set as an input terminal. If it is set as an output terminal, pin terminal 3110 outputs a signal BUSY# indicating that self refreshing is being carried out in the CDRAM.

The CDRAM further includes a timer 3101 which is activated in response to a command from command register 270a for outputting a refresh request at a predetermined time interval. Clock generator 3100 corresponds to the control clock buffer 250 and DRAM array driving circuit 260 shown in FIG. 32 or FIG. 105.

FIG. 163 shows a specific structure of clock generator 3100 shown in FIG. 162. Referring to FIG. 163, clock generator 3100 includes an CR buffer 3200 receiving an externally applied command register set signal CR# for generating an internal control signal int. *CR; a RAS signal generating circuit 3201 receiving externally applied control signals CH# and E# and clock signal K for generating an internal control signal int. *RAS; and a CAS signal generating circuit 3202 responsive to internal control signal int. *RAS from RAS signal generating circuit 3201 and to external clock signal K for generating an internal control signal int. *CAS.

Internal control signal int. *RAS from RAS signal generating circuit 3201 defines operation of the circuitry related to row selecting operation of the DRAM array. In response to internal control signal int. *RAS, row selecting operation and sensing operation are carried out in the DRAM array. Internal control signal int. *CAS from CAS signal generating circuit 3202 determines operation of the circuitry related to column selection in the DRAM. An example of the circuit related to the column selecting operation in the DRAM array is the DRAM column decoder.

RAS signal generating circuit 3201 contains a circuit for generating internal control signal int. *RkS in response to the refresh requesting signal *BUSY (internal signal) from timer 3101 and to a command signal CM from the command register 270a. In this case, external control signals E# and CH# are neglected. A circuit structure for generating internal control signal int. *RAS and neglecting external control signals, in response to the refresh request (signal *BUSY) from timer 3101 is shown in, for example, "64K bit MOS dynamic RAM containing auto/self refresh function", Journal of Institute of Electronics and Communication Engineers, January 1983, volume J66-C, No. 1.

Internal control signal int. *RAS generated from RAS signal generating circuit 3201 and internal control signal int. *CAS generated from CAS signal generating circuit 3202 may be generated from row address strobe signal generating

circuit **2601** and column address strobe signal generating circuit **2602** shown in FIG. **109** of the second embodiment.

Clock generator **3100** further includes a refresh detecting circuit **3203** in response to an externally applied refresh designating signal *REF (this represents internal signal) for detecting designation of refreshing; and a refresh control circuit **3204** responsive to a refresh request from refresh detecting circuit **3203** for controlling count value of the refresh address counter **293** and for generating a switching signal MUX for switching connection of multiplexer **258**.

Refresh control circuit **3204** also carries out an operation similar to that executed in accordance with a refresh designation from refresh designating circuit **3203** in response to refresh requesting signal (*BUSY) applied from timer **3101**, and controls operation of refresh address counter **293** and of multiplexer **258**. Timer **3101** is activated in response to the command signal CM and generates the refresh request signal at predetermined time intervals.

In the structure of FIG. **163**, instead of applying command signal CM and refresh requesting signal *BUSY to RAS signal generating circuit **3201**, a control signal from refresh control circuit **3204** may be applied to RAS signal generating circuit **3201**. In that case, RAS signal generating circuit **3201** neglects external control signals in response to the refresh designating signal from refresh control circuit, and generates internal control signal int. *RAS for a predetermined time period. After the completion of one refresh cycle, refresh control circuit **3204** increments the count value of refresh address counter **293** by 1.

FIG. **164** shows an example of a specific structure of input/output switching circuit **3202** and command register **270*a*** shown in FIG. **162**. Referring to FIG. **164**, command register **270*a*** includes a command register RR2 formed of a 2 bit data register. Command register RR2 takes and stores data applied to data input pins DQ0 and DQ1, when it is selected. The command register RR2 is selected by setting control signals Ar0 and Ar1 to "1" and "0", respectively, and by setting external control signal W# to "H" in the command register setting mode (see FIGS. **101**, **136** and **159**), as shown in FIG. **77**. A structure of the data input/output pin when masked write mode is selected and input and output of data are carried out through the same pin terminal is shown as an example.

Command register **270*a*** further includes transfer gate transistors Tr **201** and Tr **202** for connecting the command register RR2 to data input pins DQ0 and DQ1. A register selecting circuit **3120** for selecting command register RR2 for setting a desired command includes a gate circuit G110 receiving register selecting signals Ar0 and Ar1, and a gate circuit G111 receiving internal control signals W, E, CH and int. *CR. Register selecting circuit **3120** corresponds to command register mode selector **279** shown in FIG. **37**.

When command selecting signal Ar is at "L" and control signal Ar1 is at "H", gate circuit G110 outputs a signal at "H". The command register RR2 is activated when the output from gate circuit G110 attains "H", so as to latch the applied data.

When internal control signal int. *CR and internal chip select signal E are both at "L" and internal control signals W and CH are at "H", gate circuit G110 outputs a signal of "H". Therefore, in the command register mode, when gate circuit G111 is selected and output signal therefrom attains "H", command register RR2 is connected to data input/output terminals DQ0 and DQ1 and latches the applied data.

Instead of command register RR2, a command register formed of 1 bit flipflop (for example, RR1 and RR2), in which structure auto refresh/self refresh is set by setting of one flipflop in accordance with combination of the signals Ar0 and Ar1 in the command register setting mode.

Input/output switching circuit **3102** includes an NOR circuit G100 and an AND circuit G101 receiving 2 bits of command signals CM from command register RR2; a switching transistor Tr200 receiving at its gate an output from NOR circuit G100 and passing a signal applied to data input/output pin **3110**; and a switching transistor Tr201 responsive to an output from AND circuit G101 for transmitting refresh requesting signal *BUSY from timer **3101** (see FIG. **162**) to a terminal **3110**.

A signal from switching transistor Tr200 is transmitted to an input buffer circuit for the refresh signal for latching a signal in response to external clock signal K. It is transmitted to transistor Tr201 after the output from timer **3101** is buffered. Switching transistors Tr200 and Tr201 may be an input buffer and an output buffer, respectively. When switching transistor Tr200 is replaced by an input buffer, the input buffer receives not only the output from gate circuit G100 but also a signal applied in response to a rise of the clock signal K.

In the structure of the input/output switching circuit **3102** shown in FIG. **164**, NOR circuit G100 outputs a signal at "H" when 2 bits of data from command register RR2 are both at "L". AND circuit G101 outputs a signal at "H" when 2 bits of command signals CM are both "1". Therefore, when 2 bits of data DQ0 and DQ1 are both at "0", refresh mode of the semiconductor memory device is set to the auto refresh mode, and when 2 bits of data DQ0 and DQ1 are both "1", the semiconductor memory device is set to the self refresh mode.

Other logics may be used for the gate circuits G100 and G101 shown in the input/output switching circuit **3102**. Combinations of values of the bits DQ0 and DQ1 of the command signal CM for designating auto refresh and self refresh may be varied.

A 1 bit command signal may be used as a signal bit for designating auto refresh/self refresh.

FIG. **165** is a diagram of signal waveforms showing the operation of the circuit shown in FIGS. **162** to **164**. The operation will be described with reference to FIGS. **162** to **165**.

Assume that data "0" (00) indicating auto refresh is set in accordance with the command register setting mode, in the command register RR2 of command register **270*a***. In this case, an output from gate circuit G100 attains "H" and an output from AND circuit G101 attains "L". Consequently, input/output switching circuit **3102** switches pin terminal **3110** as a signal input terminal. Pin terminal **3110** receives and passes an externally applied refresh designating signal REF#. In the auto refresh mode, an output from timer **3101** is neglected or timer **3101** is reset. In this state, a refresh address and an internal control signal int. *RAS are generated under control of refresh detecting circuit **3203** and refresh control circuit **3204** in accordance with externally applied refresh designating signal REF#, and the DRAM array is refreshed in accordance with the generated refresh address.

The command register setting mode is started at time Tx and when "1" (11) is set in register RR2 of command register **270*a***, an output from gate circuit G101 attains "H" and an output from gate circuit G100 attains "L". Consequently, input terminal **3110** is switched to data output terminal, by the function of the input/output switching circuit **3102**. Refresh requesting signal *BUSY is transmitted from timer **3101** to pin terminal **3110**, which is used as a signal representing that self refreshing is being carried out in the semiconductor memory device to the outside of the device.

Timer **3101** is activated in response to the setting of the self refresh mode in command register **270*a***, and applies a refresh request to refresh control circuit **3204**. Refresh control circuit **3204** sets multiplexer **258** to a state in which output from refresh address counter **293** is selected, and controls generation of internal control signal int. *RAS from RAS signal generating circuit **3201** in response to the refresh request from timer **3101**. When the refresh request is applied from refresh control circuit **3204**, RAS signal generating circuit **3201** generates internal control signal int. *RAS at a predetermined timing.

In accordance with internal control signal int. *RAS, row selecting operation and sensing operation are carried out in the DRAM, and refreshing operation for the row designated by the refresh address from refresh address counter **293** is carried out. After a lapse of a predetermined time period, an output from timer **3101** rises to "H". Consequently, the refresh period is completed. Refresh control circuit **3204** increments address count value of refresh address counter **293** by 1, and stops generation of internal control signal int. *RAS from RAS signal generating circuit **3201**.

The period in which the output from timer **3101** is maintained at "L" is set previously. The period in which the output of timer **3101** is kept at "L" is approximately the same as the memory cycle in a common DRAM. After the lapse of this period, timer **3101** resumes its operation, and after a lapse of a prescribed time period, generates a refresh request again and applies the same to refresh control circuit **3204**. The DRAM array is refreshed under control of the refresh control circuit **3204** and RAS signal generating circuit **3201** in accordance with the refresh request.

The operation of timer **3101** is continued during designation of self refresh by command signal CM. The interval of refreshing of timer **3101** may be fixedly set in advance, or it may be programmed in accordance with the guaranteed time of data retainment of the semiconductor chip. As described above, the semiconductor memory device can be set to the auto refresh or self refresh mode in accordance with command signal CM set in the command register. When refresh designating signal REF# is at "H", the DRAM can be accessed. While refresh designating signal REF# is at "L", timer **3101** does not operate. Refresh operation is controlled externally. During the refreshing period, the DRAM array can not be externally accessed.

In self refreshing, refresh execution designating signal BUSY# is output from pin terminal **3110** during refreshing operation in the DRAM array. Therefore, by monitoring refresh execution designating signal BUSY# by an external device, the external device can determine as to whether the DRAM can be accessed, and self refreshing can be carried out in the normal mode.

The operation can be switched from self refresh to auto refresh by executing command register setting mode at a rise of clock signal K and by setting register RR2 of command register **270*a*** to the auto refresh mode (see time Ty of FIG. **165**). By so doing, the operation of the timer is inhibited, and auto refresh mode is set in the CDRAM.

By the above described structure, a CDRAM capable of executing auto refresh and self refresh in one chip can be provided. In addition, since execution timing of self refreshing can be known during the normal operation mode, self refresh can be utilized in the normal operation cycle.

[Modification of Self Refresh/Auto Refresh]

FIG. **166** shows a modification of the refresh circuit shown in FIG. **152**. In the structure shown in FIG. **166**, a BBU generating circuit **3210** is provided, and command signal CM from command register **270*a*** is transmitted to BBU generating circuit **3210**.

BBU generating circuit **3210** has a circuit structure for executing a battery backup mode. The BBU mode is described in, for example, "Battery Backup (BBU) Mode for Reducing Data Retaining Current in a Standard DRAM", Dosaka et al., Journal of Institute of Electronics, Information and Communication Engineers, 1990, No. 103, ED90-78, pp. 35 to 40, and in "38 ns 4M bit DRAM Having BBU Mode", Konishi et al., IEEE International Solid States Circuits Conference, 1990 Digest of Technical Papers, pp. 230 to 231 and p. 303. In the BBU mode, the number of arrays operating in the normal mode is reduced to ¼ in the battery backup mode of a standard DRAM so as to enable refreshing with low current to retain data.

Self refreshing is executed in the BBU mode. The BBU mode will be briefly described.

FIG. **167** is a diagram for illustrating the BBU mode. A DRAM array DRMA includes 32 small blocks MBA **1** to MBA **32**. The DRAM array DRMA is further divided into memory block groups MAB **1** to MAB **4** by 8 small blocks. One small block is driven or activated in one group. This structure corresponds to the structure of FIG. **10**. Array drivers MAD **1** to MAD **4** for driving the DRAM array are provided for the memory array block groups MAB **1** to MAB **4**, respectively. A BBU control circuit BUC is provided for driving array drivers MAD **1** to MAD **4**.

BBU control circuit BUC transmits a refresh requesting signal to one of array drivers MAD **1** to MAD **4** when a control signal REFS is applied. The refresh requesting signal REFR is successively transmitted to array drivers MAD **1** to MAD **4** from BBU control circuit BUC. Array drivers MAD **1** to MAD **4** drive one block in corresponding memory array groups MAB **1** to MAB **4**, respectively. A row address signal (for example, RAB) applied from a path, not shown, determines which block is to be selected. In the normal mode, one block is selected from each of the memory array groups MAB **1** to MAB **4**. Namely, four blocks (in the figure, memory blocks MBA **8**, MBA **16**, MBA **24** and MBA **32**) are driven.

In the BBU mode, only one memory array group is driven and only one memory block is driven (in the shown example, memory array block MBA **32**). Compared with the normal mode, the number of driven blocks is reduced to ¼, and thus current consumption in refreshing can be considerably reduced. The structure shown in FIG. **166** utilizes the BBU generating circuit (included in BBU control BUC).

FIG. **168** shows an example of a specific structure of the BBU control circuit BUC. Referring to FIG. **168**, timer **3101** includes a ring oscillator **3121** oscillating at prescribed intervals, and a binary counter **3122** counting pulse signals from ring oscillator **3121** for generating a signal every prescribed period. Binary counter **3122** generates signals for determining refresh timing (for example, every 64 μs in self refreshing) and maximum counter value for example, 16 ms; specification value of the refresh cycle).

BBU control circuit BUC further includes a BBU signal generating circuit **3210** which start its operation in response to command signal CM and is activated in response to count up signal CUP **1** from binary counter **3122** for generating a battery backup mode designating signal BBU; and a REFS generating circuit **3123** responsive to the signal BBU from BBU signal generating circuit **3210** and to a refresh cycle defining circuit CPU **2** from binary counter **3122** for generating a refresh requesting signal REFS.

BBU signal generating circuit **3210** is activated in response to self refresh designation of command signal CM and waits for application of count up signal CUP **1** from binary counter **3122**. BBU signal generating circuit **3210** is

rendered inactive when command signal CM designates the normal mode or the auto refresh mode, and it resets refresh timer 3101.

Upon reception of count up signal CUP 1, BBU signal generating circuit 3210 generates the signal BBU. The signal BBU indicates that the CDRAM is switched to the battery backup mode. REFS generating circuit 3123 is activated in response to the signal BBU, and generates refresh requesting signal REFS every time refresh cycle defining signal CUP 2 is applied from binary counter 3122.

FIG. 169 shows a circuit structure for generating internal control signal int. *RAS. In the structure of FIG. 169, only the circuit structure for generating internal control signal int. *RAS out of RAS signal generating circuit 3201 and refresh control circuit 3204 shown in FIG. 163 is shown. RAS signal generating circuit 3201 includes a gate circuit (NOR circuit) G301 receiving the signals *RAS and BBU; an inverter circuit G302 receiving an output from gate circuit G301; and a gate circuit G303 receiving an output from inverter circuit G302 and refresh requesting signal RASS from refresh control circuit 3204. Gate circuit G301 generates a signal at "H" when signals applied to both input thereof are at "L". Gate circuit G303 generates a signal at "H" when one input thereof is at "L".

The signal *RAS denotes an array access designating signal which is determined by signals E and CH which are taken in the device at a rising edge of clock signal K in the CDRAM to which the present invention is applied. This signal may be generated from the row address strobe signal generating circuit shown in FIG. 109.

Refresh control circuit 3204 includes a delay circuit 3231 for providing a prescribed delay to internal control signal int. *RAS; and a RASS generating circuit 3232 responsive to refresh requesting signal REFS from REFS generating circuit 3123 and to an output signal *SC of delay circuit 3231 for generating refresh designating signal RASS. The signal *SC from delay circuit 3231 represents completion of sensing, which is generated when sensing operation in the DRAM is completed and data of the memory cell to be refreshed is surely latched by the sense amplifier. RASS generating circuit 3232 renders active the internal control signal int. *RAS in response to refresh requesting signal REFS, and renders internal control signal int. *RAS in response to the generation of sense completion signal *SC.

The operation of the circuit shown in FIGS. 168 and 169 will be described with reference to FIG. 170 which is a diagram of signal waveforms.

The signal *RASS plays the role of *RAS in the BBU mode. when refresh requesting signal REFS is generated from REFS generating circuit 3123, signal *RASS from RASS generating circuit 3232 rises to "L" and is activated. In response, internal control signal output from gate circuit G303 rises to "H", and internal control signal int. *RAS output from inverter circuit G304 attains active "L".

Row selecting operation and sensing operation are carried out in the DRAM in accordance with internal control signal int. *RAS. After the completion of sensing operation, sense completion signal *SC from delay circuit 3231 falls to active "L".

In response to the fall of the sense completion signal *SC, RASS generating circuit 3232 raises output signal *RASS. In response, internal control signal int.RAS attains active "H", and thus refresh cycle in the DRAM is completed.

More specifically, in the BBU mode, a rise (transition to the active state) of refresh requesting signal REFS from REFS generating circuit 3123 is used as a trigger for carrying out a self-timed refreshing. By applying the signal BBU to gate circuit G301, array access is requested in the BBU mode, and even if *RAS is rendered active "L", the output from gate circuit G301 is kept at "L", whereby entrance to the array active cycle in the BBU mode is prevented. Although active level of the signal BBU is not shown, the signal BBU attains "H" when the BBU mode is designated.

FIG. 171 shows an example of a specific structure of RASS generating circuit 3232 shown in FIG. 169. RASS generating circuit 3232 is formed by a set•reset type flipflop. The flipflop receives refresh requesting signal REFS at its set input, and receives a sense completion signal *SC at its reset input /R. Signal *RASS is generated from /Q output thereof. Flipflop FFR is set in response to a rise of a signal applied to the set input S, and its /Q output becomes "0". It is reset in response to a fall of a signal applied to its reset input /R and its /Q output becomes "H".

[Application to Other Structures]

The above described structure shows an application to the CDRAM. However, this structure can be applied to a general dynamic type semiconductor memory device containing the DRAM array only. A common dynamic semiconductor memory device receives a row address strobe signal *RAS, a column address strobe signal *CAS and a write enable signal WE as external control signals. Switching between auto refresh and self refresh can be done in the dynamic semiconductor memory device receiving external control signals *RAS, *CAS and *WE.

FIG. 172 shows a circuit portion related to refresh mode setting circuit in a common dynamic semiconductor memory device. Referring to FIG. 172, the circuitry related to refreshing includes a command register 3502 receiving and latching an externally applied refresh mode designating signal *CR; an input/output switching circuit 3501 responsive to a command signal (refresh mode setting signal) CM set in command register 3502 for setting a terminal 3510 to an input terminal or an output terminal; and a clock generator 3503 receiving external control signals *RAS, *CAS, *WE and a refresh designating signal *REF when terminal 3510 is used as an input terminal, and receiving command signal CM from command register 3502 for generating various internal control signals of the semiconductor memory device and for controlling refreshing operation.

The dynamic semiconductor memory further includes a refresh address counter 3504 responsive to a control signal from clock generator 3503 for generating a refresh address; a row address buffer 3506 for passing one of externally applied addresses A0 to A9 and the outputs of refresh address counter 3504 for generating internal row address signals RA0 to RA9; and a column address buffer 3507 receiving externally applied address signals A0 to A9 for generating internal column address signals CA0 to CA9. Timings for taking respective address signals at the row address buffer 3506 and column address buffer 3507 are determined by an internal control signal from clock generator 3503. The timing for taking external row address signals A0 to A9 at the row address buffer 3506 is determined by external control signal *RAS, and timings for taking external address signals A0 to A9 of column address buffer 3507 is provided by external control signal *CAS.

Row address buffer 3506 includes not only a simple buffer circuit but also a multiplex circuit, though not explicitly shown. The multiplex circuit may receive external row addresses A0 to A9 and an output from refresh address counter 3504 to selectively transmit one of these to the buffer circuit. The multiplex circuit may receive row addresses A0 to A9 after the external addresses are converted to internal row addresses.

FIG. 173 shows an example of a specific structure of clock generator 3503 shown in FIG. 172. Referring to FIG. 173, clock generator 3503 includes a refresh detecting circuit 3510 receiving refresh designating signal *REF for determining whether or not there is a refresh designation; a RAS buffer 3511 receiving external control signal *RAS for generating internal control signal int. RAS; and a CAS buffer 3512 receiving external control signal *CAS for generating internal control signal int. CAS. When refresh detecting circuit 3510 detects a refresh designation, RAS buffer 3511 and CAc buffer 3512 are rendered inactive. When timer 3505 outputs a refresh request, buffers 3511 and 3512 are set to a signal input prohibited state under the control of refresh control circuit 3513 (the signal path in this case is not shown).

Clock generator 3503 further includes a pulse generating circuit 3514 responsive to refresh designation from refresh detecting circuit 3510 and refresh control circuit 3513 for generating an internal pulse signal having a prescribed width; and a gate circuit 3515 receiving internal control signal RAS from RAS buffer 3511 and pulse generating circuit 3514. Internal control signal int. RAS is generated from gate circuit 3515. The active period of the pulse generated by pulse generating circuit 3514 is the period necessary for the completion of refreshing in the DRAM. When a refresh request is generated from timer 3505, refresh control circuit 3513 generates a switching signal MUX to multiplexer (included in row address buffer 3506) so as to select the output from refresh address counter, and activates pulse generating circuit 3514 for generating a pulse signals at a prescribed timing.

Timer 3505 starts its operation in response to command signal CM from command register 3502 as in the above described embodiment, and generates pulse signals (refresh request signals) at prescribed intervals.

When auto-refreshing is designated by command signal CM, refresh control signal 3513 neglects the output from timer 3505, and carries out necessary control for refreshing in response to the output from refresh detecting circuit 3510. When command signal CM designates self refreshing, refresh control circuit 3513 carries out necessary control operations for refreshing of DRAM in accordance with the refresh request from timer 3505.

Returning to FIG. 172, the structure of the command register 3502 and input/output switching circuit 3501 is the same as that shown in FIG. 164. In this case, it is not necessary for the command register 3502 to latch refresh mode setting signal *CR in synchronization with the clock signal K, and it latches control signals applied at arbitrary timing. The refresh mode setting signal *CR applied externally may be a 1 bit signal or 2 bit signal.

By the above described structure, auto refreshing and self refreshing are both available in a common DRAM. By the function of input/output switching circuit 3501, one pin terminal 3510 can be switched to input terminal or output terminal. When pin terminal 3510 is set to an output terminal, it represents that self refresh is being carried out in the semiconductor memory device. In the self refresh mode, refresh requesting signal from timer 3505 is output as refresh execution designating signal *BUSY. Therefore, by monitoring the signal *BUSY, the timing of refreshing can be known by an external device.

By the structure of FIG. 172, a dynamic semiconductor memory device allowing self refreshing in the normal mode can be provided, in a common DRAM.

Further, a BBU generating circuit may be further connected as shown in FIG. 166 to the structure of the dynamic semiconductor memory device shown in FIG. 172.

In the structures shown in FIGS. 162, 166 and 172, the self refresh mode and the auto refresh mode can be selectively executed. When the output from command register 3502 has its level fixed by wire bonding, for example, pin terminal 3510 is fixedly used as an input terminal or an output terminal. Therefore, a semiconductor memory device (dynamic type semiconductor memory device or CDRAM) capable of auto refreshing operation only or a semiconductor memory device (dynamic type semiconductor memory device or a CDRAM) capable of self refreshing only can be optionally provided. Namely, semiconductor memory devices which can accommodate self refresh mode and auto refresh can be provided by one common of the semiconductor chip.

Especially by the structure realizing the auto refresh and the self refresh mode on the same semiconductor chip, the guaranteed time of data retainment of the chip can be measured by using the auto refresh mode in the refresh interval program necessary when the self refresh is set, and therefore self refresh cycle period can be set exactly.

When the auto refresh or the self refresh is to be fixed, it is not necessary to independently and separately provide an input/output switching circuit, and the pin terminal (for example, terminal 3510 in FIG. 172) may be set as an input terminal or the output terminal by interconnections. This structure is shown in FIGS. 174 and 175. In the structure of FIG. 174, refresh mode designating command CM set by refresh mode setting circuit 3550 is set to the supply voltage Vcc or ground potential Vss by wiring. In this structure, input/output switching circuit 3102 is fixedly set to an input circuit or an output circuit.

In the structure shown in FIG. 175, refresh mode setting circuit 3550 is set to the auto refresh mode or the self refresh mode by wiring, as in the structure of FIG. 174. Input/output switching circuit 3551 is set to a signal input circuit or a signal output circuit by wiring, as shown by the dotted lines.

In the above described structures also, signal BUSY# is externally output in the self refresh mode, and therefore self refresh can be carried out in the normal mode.

[Another Embodiment of Address Allottance]

In the CDRAM, the row address and the column address are applied as DRAM address Aa time division multiplexedly, as described previously. However, even if the period of the external clock K is made longer (including intermittent generation), it is preferred to operate the CDRAM at a speed as high as possible. A structure for operating the CDRAM at high speed will be described. The following structure which will be described with reference to FIGS. 177 to 185 is another embodiment of address allotting method shown in FIGS. 71 and 72.

FIG. 176 shows a further embodiment of the address allotting method. In the structure shown in FIG. 176, an internal address int. Ac from an address buffer 4001 is also applied to DRAM column decoder 103. Namely, a part of the DRAM column address and the SRAM address are shared.

Address buffer 255 shown in FIG. 32 or address generating circuit 360 shown in FIG. 105 may be used as address buffer 4001. In the structure shown in FIG. 176, by applying a row address as an address Aa externally and by applying a column address as an address Ac, the DRAM address can be provided in non multiplexed manner without increasing the number of external pin terminals. Therefore, timings for taking column address of the DRAM can be made faster than in the multiplexing method, and the speed of operation of the DRAM can be increased. The structure for utilizing the SRAM address and the DRAM address will be described in detail.

FIG. 177 shows more specifically the structure in which SRAM address and DRAM address are commonly used. Referring to FIG. 177, address buffer 4001 includes a buffer circuit 4010 receiving external column address signals Ac0 to Ac3 for the SRAM for generating an internal column address signal; a buffer circuit 4011 receiving external address signals Ac4 to Ac11 for generating internal address signals; and a buffer circuit 4012 receiving external address signals Aa0 to Aa9 for generating internal row address signals for the DRAM. The buffer circuits 4010, 4011 and 4012 latches external addresses and generates internal address signals in response to internal clock signal int. K or strobe signals /RAS, /CAL.

An internal address signal from buffer circuit 4010 is applied to SRAM column decoder 203. An internal address signal from buffer circuit 4011 is applied to a determining circuit 4020. An internal address signal from buffer circuit 4012 is applied to DRAM row decoder 102.

Determining circuit 4020 determines whether the address signal from buffer circuit 4011 is to be applied to SRAM row decoder 202 or DRAM column decoder 103, in accordance with chip select signal E and cache hit designating signal CH (these signals may be internal signals or external signals).

When the SRAM array is accessed, determining circuit 4020 applies the internal address signal from buffer circuit 4011 to SRAM row decoder 202. When the DRAM array is accessed, determining circuit 4020 applies the address signal from buffer circuit 4011 to DRAM column decoder 103.

In the structure shown in FIG. 177, out of columns selected by DRAM column decoder 103 in the DRAM array, 4 bits (in case of 4M CDRAM) are further selected, by an output from SRAM column decoder 203.

In the structure shown in FIG. 177, address signals Aa0 to Aa9 are used as array row address signals for designating a row of the DRAM array. Address signals Ac0 to Ac3 are used as cache column address signals for designating a column in the SRAM array and as array column address signals in direct access to the DRAM array. Address signals Ac4 to Ac9 are used as cache row address signals for designating a row in the SRAM array, and an array column address signals for designating columns in the DRAM array.

By the structure in which address signals Ac0 to Ac11 and Aa0 to Aa9 can be independently applied and buffer circuits 4010, 4011 and 4012 simultaneously take applied address signals and generate internal address signals, as in the structure of FIG. 177, the row address signals and column address signals for the DRAM array can be simultaneously taken, and therefore access time in the DRAM array can be significantly reduced.

FIG. 178 shows an example of a specific structure of determining circuit 4020 shown in FIG. 177. Referring to FIG. 178, determining circuit 4020 includes a gate circuit G400 receiving internal chip select signal E and internal cache hit designating signal CH (which is generated from control clock buffer 250 shown in FIG. 32 or 105); and switching transistors Tr400 and Tr401 which are selectively turned on in response to an output from gate circuit G400. Switching transistor Tr400 transmits address signals from buffer circuit 4011 (see FIG. 177) to SRAM row decoder 202. Switching transistor Tr401 transmits internal address signals Ac4 to Ac11 to DRAM column decoder 103.

Gate circuit G400 generates a signal at "H" when both inputs thereof are at "L". The signals E and CH are both at "L" at a time of cache hit, that is, the time of accessing to the SRAM array. In that case, switching transistor Tr400 turns on, and internal address signals Ac4 to Ac11 are transmitted as SRAM row address signals to SRAM row decoder 202.

When the DRAM array is accessed, signal CH# attains to "H", and hence output of gate circuit G400 attains "L". Switching transistor Tr401 turns on and internal address signals Ac4 to Ac11 are transmitted to DRAM column decoder 103.

In the structure of determining circuit shown in FIG. 178, address signals can not be simultaneously transmitted to the DRAM and the SRAM in the block transfer mode and in the copy back mode. A structure in which switching transistors Tr400 and Tr401 are both turned on when the block transfer mode and the copy back mode are designated may be additionally provided in this case. Such a structure can be easily implemented by referring to the combination of the control signal s shown in FIG. 76 or 215.

In the structures shown in FIGS. 177 and 178, SRAM address signal lines Ac4 to Ac11 are branched into DRAM address signal lines and SRAM address signal lines. In this case, load capacitance associated with SRAM address signal lines connected to SRAM row decoder is increased. If the load capacitance associated with the SRAM address signal line is increased, signal delay occurs, an access time at a time of cache hit is increased. Therefore, load of the SRM address line must be as small as possible. A structure for preventing increase of load capacitance associated with the SRM address signal line is shown in FIG. 179.

Referring to FIG. 179, SRAM row decoder 202 includes a predecoder 4051 for pre-decoding internal address signals from address buffer 4010; and a SRAM row decoder 4052 for further decoding the pre-decoded signals from predecoder 4051 for selecting a word line in the SRAM array. The method of pre-decoding addresses described above is employed in common semiconductor memory devices in view of reduction in occupied area of the address signal lines and reduction of decoder circuit scale.

In such a structure as shown in FIG. 179, a pre-decoded signal from predecoder 4051 is transmitted to the DRAM column decoder as shown in (i) of FIG. 169. In this case (I), the length of SRAM address signal lines from address buffer 4010 can be made shorter, and delay in address signals can be reduced.

The SRAM word line selecting signal from SRAM row decoder 4052 may be applied to the DRAM column decoder (see case (II) of FIG. 179). When the SRAM word line selecting signal from SRAM row decoder 4052 is to be applied to the DRAM column decoder, the DRAM column decoder is simply comprised of a common buffer. In the case (II), since word line driving circuit are provided for respective SRAM word lines for driving the SRAM word lines, signal transmission delay is not generated on the SRAM word lines.

In the structure shown in FIG. 179, the influence of delay incidental to determining operation in determining circuit 4020 on the access time of SRAM array can be reduced. More specifically, determination as to whether DRAM array is accessed or SRAM array is accessed takes some time in the determining circuit 4020. In order to carry out cache hit operation at a high speed, the influence of time necessary for determining operation in determining circuit 4020 on the accessing to the SRAM array must be reduced.

Speed of operation in the DRAM array is not so high as in the SRAM. Therefore, the time for determination in the determining circuit 4020 does not affect the column selecting operation in the DRAM array. Therefore, by the structure shown in case (I) or (II) of FIG. 179 in which the SRAM address signal line and the DRAM column address signal lines are branched after the predecoder circuit 4051, any adverse influence to the access time for the SRAM array can be surely eliminated.

In the structure shown in FIG. 179, determining circuit shown in FIG. 178 may be provided at the branching point. Alternatively, signal lines successive to predecoder 4051 may be branched directly to SRAM signal lines and DRAM signal lines. In this case, address signals (pre-decoded signal or the SRAM word lines selecting signal) are directly transmitted to the DRAM column decoder. The operations of the DRAM row decoder, DRAM column decoder and the SRAM column decoder are controlled by determining circuit 4030 shown in FIG. 180. SRAM row decoder 202 is adapted to operate when the SRAM array is accessed and the DRAM array is accessed. In the SRAM row decoder 202, where address signal lines are branched at the output stage of predecoder 4051, the predecoder operates, and operation of SRAM row decoder 4052 is controlled by determining circuit 4030. Where signal lines are branched at the output stage of SRAM row decoder 4052, SRAM row decoder 4052 operates until determination by determining circuit 4030 is completed.

Even if the SRAM decoder is commonly used for selecting a column in the DRAM array and a column in the SRAM array, only the bit line pair in one of the arrays is connected to the internal data line, and therefore collision of data does not occur (see FIGS. 33, 49 and 57). A structure for controlling driving of the SRAM array and the DRAM array by the determining circuit is shown in FIG. 180.

Referring to FIG. 180, determining circuit 4030 receives internal control signals W, E, CH, CI and CR and controls operations of DRAM array driving circuit 260 and SRAM array driving circuit 264 in accordance with combinations of the control signals. Command register set signal CR is also applied to determining circuit 4030 because command register setting signal CR (CC2) is used when high speed copy back operation mode is set, as will be described later. By the structure of FIG. 180, row and column selecting operations in the DRAM array and the SRAM array can be carried out in parallel. Row and column selecting operations in the SRAM array and the DRAM array can be executed by taking addresses in parallel in the block transfer mode, the copy back mode and the like.

The operation in this method of commonly using addresses will be described.

FIG. 181 shows timings of operations at a cache miss. At a time of a cache miss, external control signal E# is set to "L" and cache hit designating signal CH# is set to "H" at a rising edge of clock K. Consequently, a cache miss is set. External address signals Aa and Ac applied at a rising edge of clock signal K are taken as a row address signal (R) and a column address signal (C) of the DRAM. Consequently, the initiate cycle TMMI is executed. Subsequent to the initiate cycle TMMI, array active cycle TMMA is carried out, and data selecting operation is carried out in the DRAM in accordance with the applied row address signal (R) and the column address signal (C). Block transfer or high speed copy back mode operation may be carried out in the array active cycle TMMA. By setting chip select signal E# to "L" at a rising edge of clock signal K in the last period of the array active cycle TMMA, data Q corresponding to the applied address signals R and C is output (When data reading operation is set).

In data writing, by setting chip select signal E# and write enable signal W# (not shown) to "L" in the initiate cycle TMMI, write data is written to the SRAM array as well as to the DRAM array.

When the array active cycle TMMA is completed, the precharge cycle TMMP is carried out and the DRAM array is set to the precharge state. In the precharge cycle TMMP, the SRAM array can be accessed. Internal address signal Ac is taken as the SRAM address signal at a rise of clock signal K and a corresponding memory cell in the SRAM array is accessed.

Thereafter, the array write cycle TMA is executed, and data is transferred from the SRAM array to the DRAM array (copy back; transfer of latched data to the DRAM array). The array write cycle TMA includes an initiate cycle TMI and an array active cycle TMMA. In the array active initiate cycle TMAI, chip select signal E# is set to "L" at a rising edge of clock signal K, and externally applied addresses Aa and Ac are taken as the row address signal (R) and column address signal (C). Thereafter, in the array write cycle TMA, corresponding data, of the SRAM array latched in a latch circuit is transferred to the DRAM array. Data transfer from the latch to the DRAM array is carried out in the array active cycle TMMA.

In the array write cycle TMA, data transfer from the latch circuit (see FIGS. 49 and 57) to the DRAM array is carried out, and therefore the SRAM array can be accessed. The access to the SRAM array in the array active cycle TMMA is shown in FIG. 181 as the address signal Ac being valid (V). Consequent to the cache miss cycle TM, a cache hit cycle TH or a standby cycle TS is carried out.

Specific reading operation and writing operation will be described. FIG. 182 shows timings of operations at a miss read. FIG. 182 shows a clock period of 20 ns as an example. In case of a miss read, only the chip select signal E# is set to "H" at a rising edge of clock signal K. At this time, addresses (ROW 1 and COL 1) applied from a CPU (external operational processing unit) are taken as the row address signal and the column address signal for the DRAM array. In this miss read operation, the DRAM array is accessed in accordance with the row address signal ROW 1 and COL1. Data transfer from the DRAM array to the SRAM array may be carried out during this operation. In this case, the same addresses are applied to the SRAM array and the DRAM array. In miss operations accompanied with data transfer from the DRAM array to the SRAM array, the structure of determining circuit 4030 shown in FIG. 180 is employed. If the structure of determining circuit 4020 shown in FIG. 177 is used, address signal Ac may be taken in accordance with the rising of the second clock signal K to carry out row selecting operation of the SRAM array. After a lapse of a prescribed time period, output enable signal G# is made to "L". When the output enable signal G# falls to "L", data Q1 corresponding to the applied addresses ROW1 and COL1 is output.

Thereafter, precharge cycle of the DRAM array is carried out. In the precharge cycle, SRAM array can be accessed. Simultaneously with the start of the precharge cycle, hit read operation starts in FIG. 182. In the hit read operation, chip select signal E# and cache hit designating signal CH# are both set to "L" at a rising edge of clock signal K. Accordingly, address signal Ac is taken as a signal for selecting a row and a column in the SRAM array and the corresponding memory cell data Q2 is output in that clock cycle. Referring to FIG. 182, a hit read and a hit read are continuously executed. In respective hit read cycles, output data Q3 and Q4 are output in accordance with addresses C3 and C4.

After the completion of the precharge cycle of the DRAM array, the array write cycle is carried out. In this array write cycle, corresponding data in the SRAM array has been already latched at the time of miss read, and the latched data is transferred to the DRAM array. The array write cycle is set by setting chip select signal E# to "L", cache hit designating

signal CH# to "H", control signal CC1# (corresponding to cache access inhibiting signal CI#) "L" and write enable signal W# to "L" at a rising edge of clock signal K.

In the array write cycle, externally applied address signals (miss addresses) Ac and Aa are both taken as the column address signal and the row address signal for the DRAM. In this state, the SRAM array can not be accessed. In the setting cycle of the array write cycle, execution of hit write cycle is inhibited even if a hit write occurs. Therefore, cache hit designating signal CH# is set to "H".

Subsequent to the setting cycle of the array write cycle, a hit read cycle is carried out. In the hit read cycle, chip select signal E# and cache hit designating signal CH# are set to "L", and output enable signal G# is set to "L". In this state, the SRAM array is accessed in accordance with the address signal Ac, and corresponding data Q5 is output. In the example of FIG. 182, cache read is again carried out in the last cycle of the array write cycle, and cache data Q6 in accordance with address C6 is output.

In the array write setting cycle, the address Aa is represented as a miss address (Miss Add). It means that the address necessary for transferring data from the SRAM array to the DRAM array is an address from an externally provided tag memory. FIG. 183 shows operation timings at a miss write. The miss writing is set by setting chip select signal E# to "L" and write enable signal W# to "L" at a rising edge of clock signal K. At this time, external addresses Ac and Aa are taken as the column address COL 1 and row address ROW 1 of the DRAM array, and externally applied write data D1 is taken. In this miss writing, the DRAM and SRAM arrays are accessed, and data D1 is written to a corresponding memory cell of the SRAM array. Writing of data to the SRAM and DRAM arrays may be carried out in accordance with any of the data transfer methods described above.

When the miss write cycle is completed, the DRAM array enters the precharge cycle. In the precharge cycle, the SRAM can be accessed. In the example of FIG. 183, hit read, hit read and hit write operations are carried out. In respective operation cycles, the address Ac is taken as SRAM array addresses C2, C3 and C4, respectively, output data Q2 and Q3 are output, and write data D4 is written.

Thereafter, the array write cycle is executed. The array write cycle is similar to that shown in FIG. 182. In the setting cycle of the array write cycle, control signal CC1# (corresponding to the array access designating signal (cache access inhibiting signal) CI#) is set to "L" and access to the SRAM array is inhibited. Therefore, even if a hit read occurs in the array write setting cycle, this hit reading is not carried out.

Successive to the setting cycle for the array write cycle, a hit write cycle is carried out. The hit write cycle is set by setting chip select signal E# to "L" at a rising edge of clock signal K. Since hit reading is designated, write enable signal W# is set to "H" and output enable signal G# is set to "L" in this state. In this state also, the array write cycle is set, external address (Miss Add) is simultaneously applied as addresses Ac and Aa, and these addresses are taken as the column address Col 2 and row address Row 2 of the DRAM array.

A hit write cycle is executed successive to the array write setting cycle, the address Ac is taken as an address CS for the SRAM, and data D5 applied at that time is written to the corresponding SRAM memory cell. A hit read cycle is executed in the last cycle of the array write cycle, address Ac is taken as a column address C6 of the SRAM array, and corresponding data Q6 is output.

FIGS. 184 and 185 show the manner of connection between a memory controller and the CDRAM in accordance with the method in which the addresses are commonly used.

FIG. 184 shows connection between an external control device and the CDRAM in accordance with direct mapping method. The manner of connection shown in FIG. 184 corresponds to the manner of connection shown in FIG. 79. In this manner of connection shown in FIG. 184, 8 bits of address signals A6 to A13 are applied to SRAM row decoder 202. 6 bits of address signals A6 to A11 of 8 bits of address signals A6 to A13 are applied to DRAM column decoder 103. Address signals A12 and A13 from the CPU and 8 bits of address signals A14 to A21 from a selector 672 are applied to row decoder 102 of DRAM 100. In this structure shown in FIG. 184, row address signals and column address signals of the DRAM are applied in non-multiplexed manner. Therefore, a multiplex circuit as shown in FIG. 79 is not externally provided. Chip select signal E# and cache hit designating signal CH# are applied to a clock control circuit 4400, and operations in accordance with accessing to the SRAM array and to the DRAM array are carried out. Clock control circuit 4400 includes control clock buffer 250, SRAM array driving circuit 264 and DRAM array driving circuit 260 shown in FIG. 32 or 105, and determining circuit 4030 shown in FIG. 180.

Referring to FIG. 184, address signals A6 to A11 are applied to column decoder 103 for the DRAM array from an output portion of SRAM. row decoder 202. Signals may be output from predecoder portion as shown in FIG. 179, or, alternatively, SRAM word line selecting signals may be applied. FIG. 184 simply shows that part of the row address signals of the SRAM array and part of column address signals of the DRAM are functionally used commonly. FIG. 184 does not exactly reflect the actual manner of connection.

The structure of external control circuit 650 is the same as that shown in FIG. 79. Compared with FIG. 79, in the structure of FIG. 184, multiplex circuit 705 for multiplexing the row address signals and the column address signals for the DRAM is not necessary, the system size can be reduced, and DRAM column addresses can be easily taken.

FIG. 185 shows a manner of connection of addresses when the CDRAM has a cache structure of 4 way set associative method. The structure shown in FIG. 185 corresponds to the address connecting structure shown in FIG. 170. In the structure of FIG. 185, address signals A6 to A11 from the CPU and way addresses W0 and W1 from a controller 750 are applied to SRAM column decoder 202. Out of address signals applied to SRAM row decoder 202, address signals A6 to A11 are applied to DRAM column decoder 103. Other structures are the same as those shown in FIG. 80 except that multiplex circuit 700 for multiplexing a row address and a column address of the DRAM array is not provided. The corresponding portions are denoted by the same reference characters.

In this structure also, even if address signals are commonly used by the SRAM and DRAM, the cache structure can be easily changed.

As described above, by using some of the SRAM address bits as DRAM address bits, address non-multiplexing method of the DRAM address can be realized without increasing the number of pin terminals, and column addresses for the DRAM array can be easily taken.

[A Further Embodiment of Data Transfer Method]

In a CDRAM, it is preferred to access at high speed even at a cache miss. A structure for transferring and reading data at high speed even at a cache miss will be described with reference to FIGS. 186 through 193.

Briefly stating, DRAM array have data reading path and data writing path provided separately from each other.

FIG. **186** shows a structure which carries out high speed data transfer, high speed data reading even at a cache miss, and increases speed of operation of data transfer such as high speed copy back mode. FIG. **186** shows structures of portions related to one memory block.

In a DRAM, a data reading path and a data writing path are provided separately. Accordingly, a global IO line includes global read line pairs GOLa and GOLb for transmitting data read from the DRAM array, and global write line pair GILa and GILb for transmitting write data to the DRAM array. The global read line pair GOLa and the global write line pair GILa are arranged parallel to each other, and global read line pair GOLb and the global write line pair GILb are arranged parallel to each other. The global read line pair GOL (generally represents global read line pairs) and the global write line pair GIL (generically represents global write line pairs) correspond to the global IO line pair GIL shown in FIG. **8**.

Local read line pair LOLa and LOLb are provided corresponding to the global read line pairs GOLa and GOLb. Local write line pairs LILa and LILb are provided corresponding to the global write line pairs GILa and GILb.

A read gate ROGa which turns on in response to a read block selecting signal φRBA is provided between the global read line pair GOLa and local read line pair LOLa. A read gate ROGb which turns on in response to a read block selecting signal φRBA is provided between global read line pair GOLb and local read line pair LOLb.

A write block selecting gate WIGa which turns on in response to a write block selecting signal φWBA is provided between global write line pair GILa and local write line pair LILb. A write block selecting gate WIGb which turns on in response to a write block selecting signal φWBA is provided between global write line pair GILb and local write line pair LITb.

A local transfer gate LTG for transmitting selected memory cell data to local read line pair LOL, and a write gate IG for connecting the selected memory cell to local write line pair LIL are provided for each bit line pair DBL.

A write column selecting line WCSL and a read column selecting line WCSL are provided for setting local transfer gate LTG and write gate IG to a selected state (conductive state). A write column selecting line WCSL and a read column selecting line RCSL constitute a pair and arranged in parallel. A write column selecting signal generated when data is to be written from DRAM column decoder is transmitted to write column selecting line WCSL. A read column selecting line generated when data is to be read from the DRAM array is transmitted to read column selecting line RCSL. The write column selecting line WCSL and read column selecting line RCSL are arranged to select two columns, respectively. This structure corresponds to the column selecting line CSL shown in FIG. **8** divided into a signal line for selecting a column for writing and a signal line for selecting a column for reading.

Local transfer gate LTG includes transistors LTR **3** and LTR **4** for differentially amplifying a signal on DRAM bit line pair DBL, and switching transistors LTR **1** and LTR **2** which turn on in response to a signal potential on read column selecting line RCSL for transmitting the signal amplified by the transistors LTR **3** and LTR **4** to local read line pair LOL. One terminal of each of the transistors LTR **3** and LTR **4** is connected to a fixed potential Vss, which is, for example, the ground potential. In this structure, local transfer gate LTG inverts the potential on DRAM bit line pair and transmits the same to local read line pair LOL. Transistors LTR **3** and LTR **4** are formed of MOS transistors (insulated gate type field effect transistors), with their gates connected to the DRAM bit line pair DBL. Therefore, local transfer gate LTG transmits the signal potential on the DRAM bit line pair DBL at high speed to local read line pair LOL without any adverse influence to the signal potential on the DRAM bit line pair DBL.

Write gate IG includes switching transistors IGR **1** and IGR **2** which turn on in response to the signal potential on write column selecting line WCSL for connecting the DRAM bit line pair to local write line pair LIL.

Other structures in the DRAM array are the same as those shown in FIG. **8**.

Transfer gates BTGA and BTGB are provided corresponding to two pairs of global write line pair GIL and global read line pairs GOL. Transfer gate BTG (generically represents transfer gates BTGA and BTGB) is connected to global read line pairs GOL and global write line pairs GIL. Structures of transfer gates BTGA and BTGB will be described in detail later. Transfer control signals φTSL, φTLD and φTDS are applied to transfer gates BTGA and BTGB.

Control signal φTDS is generated when data is to be transferred from the DRAM array to the SRAM array. Control signal φTSL is generated when data is to be transferred from the SRAM array to the latch in the transfer gate BTG. Control signal φTLD is generated when the latched data is to be written to the DRAM array. Transfer gates BTGA and BTGB, detailed structure of which will be described later, include latching means for latching data read from the SRAM array. Data transfer operation between the DRAM array and the SRAM array when the circuit of FIG. **186** is used will be described.

FIG. **187** is a diagram of signal waveforms showing data transfer operation from the DRAM to the SRAM in the array structure shown in FIG. **186**. The signal waveforms of data transfer operation shown in FIG. **187** correspond to the signal waveforms showing data transfer operation of FIG. **55**.

At time t**1**, equalizing signal φEQ falls to "L" and precharging state in the DRAM array ends. Then a DRAM word line DWL is selected at t**2**, and potential at the selected word line rises.

At time ts**1**, row selecting operation is being carried out in the SRAM array, potential of the selected SRAM word line SWL rises to "H", and memory cell data connected to the selected word line is transmitted to SRAM bit line pair SBL. The signal potential on SRAM bit line pair SBL is transferred to the latching means included in the transfer gate in response to transfer designating signal φTSL and latched therein.

In the DRAM, signal potential on the selected word line DWL rises to "H" at time t**2**, and when signal potential on DRAM bit line pair DBL attains sufficient magnitude, sense amplifier activating signal φSAN attains "L" at time t**3** and sense amplifier activating signal /φSAP rises to "H" at time t**4**. Consequently, signal potentials on DRAM bit line pair DBL are set to "H" and "L" corresponding to the read data, respectively.

Local transfer gate LTG directly receives signal potentials on the DRAM bit line pair DBL.

Before the rise of the sense amplifier activating signal /SAN at time t**3**, signal potential to read column selecting line RCSL rises to "H". Consequently, small change of the signal potential generated in DRAM bit line pair DBL is amplified at high speed at local transfer gate LTG and is transmitted to local read line pair LOL.

When signal potential on DRAM bit line pair DBL is transmitted to local read line pair LOL, read block selecting signal φRBA rises to "H" at time t7'. Consequently, local read line pair LOL is connected to global read line pair GOL, and the change in signal potential generated in the DRAM bit line pair DBL is transmitted through global read line pair GOL to transfer gate BTG.

Before the generation of change in signal potential of the global read line pair GOL at time t7', transfer control signal φTDS has been generated at time t3. The change in signal potential generated on global read line pair GOL is transmitted to a corresponding memory cell of the SRAM array at high speed through the transfer gate BTG.

Therefore, by the time the amplifying operation on DRAM bit line pair DBL by DRAM sense amplifier DSA is completed at time t5, data transfer to the SRAM array has already been completed.

By such a structure as described above in which a local transfer gate is provided and DRAM bit line pair DBL is connected to transfer gate BTG, data transfer can be carried out without waiting for completion of sense amplifying operation by DRAM sense amplifier DSA.

Arrows and signal waveforms shown by dotted lines in FIG. **187** show differences over data transfer operation shown in FIG. **55**. As is apparent from the comparison of the signal waveforms, transfer gate BTG can be activated (control signal φTDS can be generated) before activation of DRAM sense amplifier DSA, and accordingly data can be transferred at high speed in the structure shown in FIG. **187**.

The SRAM array can be accessed immediately after the data transfer from the DRAM array. Therefore, the SRAM array can be accessed at high speed even at a cache miss.

The data transfer operation from the SRAM array to the DRAM array will be described with reference to FIG. **188** showing operation timings thereof.

Data transfer from the SRAM array to the DRAM array is carried out through global write line pair GIL. In this case, global read line pair GOL and local read line pair LOL are not used.

At time t1, the precharge cycle of the DRAM array is completed. At time t2, a DRAM word line DWL is selected, and potential of the selected word line rises to "H". At t3 and t4, sense amplifier activating signals φSAN and /φSAP are rendered active, respectively, and signal potentials at DRAM bit line pair DBL attain to values corresponding to the data of the selected memory cell.

At time t5, a write column selecting line WCSL is selected and signal potential of the selected write column selecting line WCSL rises to "H". Consequently, a selected write gate IG turns on, and local write line pair LOL is connected to the selected DRAM bit line pair DBL.

At time t6, write block selecting signal φWBA rises to "H". Consequently, local write line pair LIL is connected to global write line pair GIL, and signal potential on global write line pair GIL attains to a value corresponding to the signal potential on local write line pair LIL.

At time t7, transfer control signal φTLD rises to "H", and data which has been latched in transfer gate BTG is transmitted to the selected DRAM bit line pair DBL through global write line pair GIL and local write line pair LIL.

FIG. **189** shows a structure of a portion carrying out data transfer from the DRAM array to the SRAM array, of the transfer gate BTG. Referring to FIG. **189**, transfer gate BTGR includes transistors **Tr500** and **Tr501** for differentially amplifying signal potentials on global read lines GOL and *GOL; and switching transistors **Tr503** and **Tr502** responsive to transfer control signal φTGS for transferring signal potentials on global read lines GOL and *GOL to SRAM bit lines SBLa and *SBLa. Transistor **Tr500** has its gate coupled to complementary global read line *GOL. Global read lines GOL and *GOL are coupled to local read lines LOL and *LOL, respectively. In the structure shown in FIG. **189**, the read block selecting gate is omitted for simplification.

In local transfer gate LTG, when the potential on DRAM bit line DBL is at "H", transistor LTR **4** is rendered deeper on, and transistor LTR **3** is rendered shallower on. Thus a large current flows through transistor LTR **4**. The signal potential on DRAM bit line DBL is inversely transmitted to global read line *GCL. The signal potential on DRAM bit line *DBL is inversely transmitted to local read line LOL. Transistors **Tr500** and **Tr501** receive the same potential at their gates, and they constitute a current mirror type current source to pass the same current flow to the transistors **LTR4** and **LTR3** through the global read lines *GOL and GOL. The current flowing through transistor **Tr500** is discharged through transistors LTR **2** and LTR **4**.

Since a current mirror circuit is formed, the same current as in transistor **Tr500** flows in the transistor **Tr501**. However, since transistor LTR **3** is at shallow on state or off state, the signal potential of global read line GOL is charged to "H" at high speed. After the signal potentials of global read lines GOL and *GOL are sufficiently amplified to "H" and "L", transfer control signal φTDS rises to "H", and signal potentials on global read lines GOL and *GOL are transmitted to SRAM bit lines SBL and *SBL, respectively.

In the structure of transfer gate BTGR, transistors **Tr500**, **Tr501**, LTR **1**, LTR **2**, LTR **3** and LTR **4** constitute a current mirror type amplifying circuit. Even if the signal potential transmitted to DRAM bit lines DBL and *DBL is small, it can be amplified at high speed, and signal potentials on global read lines GOL and *GOL attain to (inverted) values corresponding to DRAM bit lines *DBL and DBL. By this structure, the potentials on the DRAM bit lines are amplified by the current mirror type amplifying circuit having DRAM bit lines *DBL and DBL as direct inputs and are transmitted to SRAM bit line pair SBLa, *SBLa. Thus data can be transferred at high speed from the DRAM array to the SRAM array.

FIG. **190** shows a structure of the transfer gate shown in FIG. **186** for transferring data from the SRAM array to the DRAM array. The structure of data transfer gate BTGW shown in FIG. **190** corresponds to a structure of data transfer circuit shown in FIG. **51** with amplifying circuit portion omitted.

Referring to FIG. **190**, data transfer gate BTGW includes a transmission gate **5103** responsive to transfer control signal φTSL for inverting and transmitting data on SRAM bit lines SBLa and *SBLa; a latch circuit **5100** for latching data of SRAM bit lines SBLa and *SBLa which have been transmitted from transmission gate **5103**; and transmission gates **5102***a* an **5102***b* responsive to transfer control signal φTLD for transmitting data latched in latch circuit **5100** to global write lines GIL and *GIL, respectively.

Transfer gate BTGW further includes a gate circuit **5101***b* responsive to an array write designating signal AWDE and a DRAM column decoder output (which is also a SRAM column decoder output) SAY for connecting internal write data line *DBW to global write line *GIL; and a gate circuit **5101***a* responsive to the array write designating signal AWDE and column decoder output SAY for connecting internal write data line DBW to global write line GIL. When the DRAM array is directly accessed, write data is transmitted through gate circuits **5101***a* and **5101***b* to the DRAM array.

Transfer gate BTGW further includes gate circuits **5104***a* and **5104***b* responsive to a write designating signal SWDE to the SRAM and to SRAM column decoder output (which is also a column selecting signal of the DRAM array) SAY for connecting external write data lines DBW and *DBW to SRAM bit lines SBLa and *SBLa. The structure of transfer gate BTGW shown in FIG. **190** is the same as that of the portion for transferring data from SRAM array to the DRAM array in the transfer gate shown in FIG. **57**, and therefore detailed description thereof is not repeated.

FIG. **191** shows a circuit structure for driving write column selecting signal line WCSL and read column selecting signal line RCSL. Referring to FIG. **191**, a signal driving circuit **5110** is provided with respect to a column selecting line CSL from DRAM column decoder **103**. Signal line driving circuit **5110** includes a gate circuit **5111** receiving a column selecting signal CSL from DRAM column decoder **103** and an internal write enable signal *W, and a gate circuit **5112** receiving column selecting signal CSL, sense completion signal SC and internal write enable signal W. A signal for driving read column selecting line RCSL is output from gate circuit **5111**. A signal for driving write column selecting line WCSL is output from gate circuit **5112**.

Internal write enable signals *W and W may be taken inside in synchronization with clock K in response to an externally applied control signal W#. The internal write enable signal W may be generated at the same timing as the array write designating signal AWDE. Sense completion signal SC indicates completion of sensing operation of sense amplifier DSA in the DRAM array, which is generated by providing a prescribed delay to sense driving signal ϕSANE or ϕSAPE. In this manner, a structure in which read column selecting line RCSL is selected when data is to be written to the DRAM, and write column selecting line WCSL is selected when data is to be written from DRAM array can be provided.

FIG. **192** shows a structure for generating block selecting signals ϕRBA and ϕWBA. The circuit for generating read block selecting signal ϕRBA includes a delay circuit **5120** providing a prescribed time delay to read column selecting signal RCSL, and a gate circuit **5121** receiving an output from delay circuit **5120** and block selecting signal ϕBA (see FIG. **8**). Read block selecting signal ϕRBA is output from gate circuit **5121**.

The circuit for generating write block selecting signal ϕWBA includes a delay circuit **5130** for providing a prescribed delay to write column selecting signal WCSL, and a gate circuit **5131** receiving an output from delay circuit **5130** and block selecting signal ϕBA. Gate circuit **5131** generates write block selecting signal ϕWBA. Gate circuits **5121** and **5131** generate signals at "H" when both inputs thereof are at "H".

In the above described structure in which data writing path and reading path are separately provided in the DRAM array, data must be transferred from the DRAM array to the SRAM array as fast as possible. Therefore, it is preferred to drive block selecting signal ϕRBA and read column selecting line RCSL at a timing as fast as possible. The structure of FIGS. **176** and **177** in which address signals of the DRAM array and the SRAM array are commonly used is most effective for this structure. By this structure, the row address signal and the column address signal for the DRAM array can be applied in the non-multiplexed manner, read column selecting line RCSL can be generated immediately after the selection of the word line DWL in the DRAM array to render conductive the local transfer gate, and the DRAM bit line pair can be coupled at an earlier timing to the transfer gate BTG through local read line pair LOL and global read line pair GOL.

FIG. **193** shows a structure of a decoder circuit when the non-multiplexed address method structure is applied to the separated IO structure of the DRAM array. Referring to FIG. **193**, SRAM column decoder **5141** receives applied address signals Ac0 to Ac3, decodes the same and generate a column selecting signal SAY. Column selecting signal SAY is used as a column selecting signal of the SRAM array as well as a column selecting signal of the DRAM array.

SRAM row decoder **5142** receives address signals Ac4 to Ac11 and generates a signal for driving SRAM word line SWL. DRAM column selecting circuit **5143** receives address signals Ac6 to Ac11 out of applied address signals Ac4 to Ac11 and generates a signal for driving write column selecting line WCSL and read column selecting line RCSL. DRAM row selecting circuit **5144** receives address signals Aa0 to Aa9 and generates a block selecting signal ϕBA and DRAM word line driving signal DWL. In the structure shown in FIG. **193**, address signals Ac0 to Ac11 and Aa0 to Aa9 can be simultaneously applied, read column selecting line RCSL can be driven at high speed, and data can be transferred from the DRAM array to the SRAM array at higher speed more effectively.

In the structure shown in FIG. **186**, local read line pair LOL and local write line pair LIL are arranged on both ends of the bit line pair DBL. However, the local read line pair LOL and local write line pair LIL may be arranged on one side (for example a side near the transfer gate BTG) of the bit line pair DBL, or they may be arranged at the center of the bit line pair DBL.

By the above described structure, by utilizing high speed copy back method even at a cache miss, precharging and copy back operation of the DRAM array can be executed on the back ground of a cache hit, and therefore, the performance of the CDRAM can be significantly improved, by reducing access time at a cache miss.

By the structure for separating data reading path and data writing path of the DRAM array combined with the structure for applying addresses in non-multiplexed manner and with high speed copy back mode, remarkable effect can be obtained.

[Modification of Separated IO Array Architecture CDRAM]

In this section, a modification of the array arrangement shown in FIG. **186** is described, with reference to FIGS. **194** through **196**. The modified array arrangement can be considered as a combination of the clamping architecture shown in FIG. **61** and the separated IO DRAM array architecture shown in FIG. **186**. Clamping circuit is provided for global write line pair GIL.

FIG. **194** shows a main portion of another CDRAM which is a modification of CDRAM of FIG. **186**. In FIG. **194**, the components corresponding to those of FIG. **186** have like reference numerals, and characters, and no detailed explanation thereon is developed for saving duplicate description.

Referring to FIG. **194**, SRAM bit line pair SBL is provided with a clamping circuit CRS. The clamping circuit CRS has the same construction as that shown in FIG. **62** or FIG. **70**. SRAM clamping circuit CRS has the clamping operation inhibited by an inversion /DTS of the data transfer control signal DTS instructing data transfer from DRAM array to SRAM array.

Global write line pair GIL (GILa, GILb) is provided with a clamping circuit CRDW for clamping the potentials of the global write lines. DRAM clamping circuit CRDW has the clamping operation inhibited by an inversion /DTA of the data transfer control signal DTA instructing data transfer to DRAM array. DRAM clamping circuit CRDW may be provided for the local write line pair LIL, (LILa, LILb), and

may be provided for both the global write line pair GIL and the local write line pair LIL.

Bidirectional transfer gate BIG carries out data transfer between SRAM array and DRAM array in response to the data transfer control signals DTA, DTS and DTL. The transfer gate BTG has its same construction as that shown in FIGS. **189** and **190**. The signal DTA corresponds to the signal φTLD and allows data transfer from the latch circuit to DRAM array. The signal DTS corresponds to the signal φTDS and allows data transfer from DRAM array to SRAM array. The signal DTL corresponds to the signal φTSL and allows data transfer from SRAM array to the latch circuit.

Now, data transfer operation of the modified, separated IO configuration CDRAM will be described briefly with reference to FIGS. **189**, **190** and **194**. The operation of the bidirectional transfer gate is the same as that of the gate shown in FIGS. **189** and **190**.

With the real out gate of FIG. **189**, the signal potentials on a selected DRAM bit line pair DBL can be transferred to SRAM array at a high speed without adverse effect on the selected DRAM bit line DBL when a minute potential difference is produced in the DRAM bit line pair DBL. Consequently, data can be transferred from DRAM array to SRAM array at a high speed.

In this operation, if SRAM clamping circuit CRS is in an operating state for carrying out the clamping operation, the clamping current flows through the transistor Tr**502** or Tr**503** into the local transfer gate LTG, in which the current is discharged through the transistor LTR3 or LTR4 (see FIG. **189**). In order to prevent the current flow supplied from the clamping circuit CRS from flowing into the local read out gate LTG, the clamping operation of SRAM clamping circuit CRS is inhibited during the period when the transfer control signal DTS is active, to provide a reduced current consumption during data transfer to SRAM array.

Meanwhile, in data transfer to DRAM array, the clamping current from DRAM clamping circuit CRDW flows through the gate circuit **1812** and the discharging transistors in the inverter circuit of the latch circuit **1811** to the ground. Thus, in this data transfer operation, DRAM clamping circuit CRDW has the clamping operation inhibited in response to the signal DTA.

FIGS. **195** and **196** are operating waveform diagrams showing data transfer operations from DRAM to SRAM and from SRAM to DRAM, respectively. The operations shown in FIGS. **195** and **196** are the same as those shown in FIGS. **187** and **188** except the precharge level of global read line pair GOL, local read line pair GIL, global write line pair GIL, local write line pair LIL and SRAM bit line pair SBL. For precharging the global read line pair GIL and local read line pair LIL at "H", there may be additionally provided clamping transistors for clamping the potentials of these signal lines. For example, clamping transistors may be provided in parallel with the transistors Tr**500** and Tr**501** in the reading bidirectional transfer gate BTGR. In the following, only the operations related to inhibition of the clamping are described with reference to FIGS. **195** and **196**.

In FIG. **195**, the transfer control signal DTS is generated at the time t**3** prior to the time t7' at which the signal potential change is caused on the global read line pair GOL. The signal change on the global read line pair GOL is transferred to a selected SRAM memory cell at a high speed. If SPM clamping circuit CRS is operating, the clamping transistors SQ**70** and SQ**80** in the clamping circuit CRS supply a current flow charging the global read line pair and flowing into the local transfer gate LTG, before the global read line pair GOL has the signal potentials changed according to read out DRAM cell data. SRAM bit line clamping circuit CRS is inhibited from clamping SRAM bit lines in response to the transfer control signal DTS. Thus, SRAM bit line pair is charged and discharged by the current mirror circuit (transistors Tr**500** and Tr**501**) in the bidirectional transfer gate BTG, to have the potential levels corresponding to data read out from the selected DRAM cell.

As described above, inhibition of the clamping of SRAM clamping circuit CRS in response to the data transfer control signal DTS implements fast and reliable data transfer with less current consumption without adverse effect on the amplifying operation of local transfer gate LTG.

Now, in FIG. **196**, local write line pair LIL and global read line pair GOL are shown precharged or pulled up to "H" of Vcc-Vth by DRAM clamping circuit CRDW. Data transfer operation from SRAM to DRAM or from the latch circuit to DRAM will be described. In this description, only the operations to the clamping are described because of the similarity of the operation to that of FIG. **188**.

At the time t**5**, a write column selection line WCSL is selected, and the potential thereof rises to "H". Responsively, a write gate IG turns on to connect the local write line pair LIL to the selected DRAM bit line pair DBL. The write gate IG has a relatively large resistance. Thus, DRAM bit line pair has the potentials of full swing to "H" of Vcc and "L" of Vss, while the local write line pair LIL has "L" level potential raised from Vss due to the clamping of DRAM clamping circuit CRDW.

At the time t**6**, the write block selection signal φWBA rises to "H". Consequently, the local write line pair LIL is connected with the global write line pair GIL to have the potentials corresponding to the signal potential levels of the local write line pair LIL. If the gate WIG has a sufficiently larger resistance than the gate IG has, the global write line pair GIL has "L" level potential higher than "L" level potential of the local write line pair LIL (in the case where a clamping circuit is provided only for the global write line pair).

At the time t**7**, the transfer control signal DTA rises to "H", and data latched in the bidirectional transfer gate BTG is transferred to the selected DRAM bit line pair DBL through the global write line pair GIL and local write line pair LIL.

The clamping circuit CRDW for the write line pair GIL (and LIL as necessary) has the clamping operation inhibited. Consequently, the path of current flow from the clamping circuit CRDW into the discharging transistor in the inverter circuit of the bidirectional transfer gate is cut off to reduce the current consumption in this data transfer operation. The local write line pair LIL and the global write line pair GIL have the potential levels of "H" and "L" corresponding to the signal potentials latched in the latch circuit **1811**.

As described above, the clamping circuit provided at data receiving side bus has the clamping operation inhibited or deactivated, and therefore no penetrating current flows into a discharging transistor in the bidirectional transfer gate BTG to significantly reduce the current consumption even in the separated IO DRAM array type CDRAM.

The global write line pair GIL and the local write line pair LIL may be precharged to an intermediate potential of Vcc/2 by a clamping circuit.

The controlled clamping operation can be applied to a semiconductor memory device other than CDRAM of the invention as far as the semiconductor memory device includes SRAM array, DRAM array and a data transfer gate for data transfer between DRAM array and SRAM array.

[Other Function: Burst Mode]

Connection with external operational processing unit (CPU) having burst mode function will be described with reference to FIGS. **197** through **201**.

In the burst mode, a first address is set in an address counter, and subsequent address are generated sequentially from the counter during the burst mode operation or by a predetermined number of times.

As described previously, burst mode is an operation mode in which a data block are transferred at one time from the CPU. Control of the burst mode function is supported by a circuit portion of the additional function control circuit **299** shown in FIG. **32**.

FIG. **197** shows a circuit portion for realizing burst mode operation. Referring to FIG. **197**, burst mode control system includes a BE buffer circuit **6001** taking an externally applied burst enable signal BE# in response to internal clock signal int. K for generating an internal burst enable signal /BE; a one shot pulse generating circuit **6002** responsive to the first internal burst enable signal /BE from BE buffer circuit **6001** for generating a one shot pulse signal ϕBE having a prescribed pulse width; and a gate circuit **6003** responsive to the one shot pulse signal ϕBE having a prescribed pulse width; and a gate circuit **6003** responsive to one shot pulse signal ϕBE for gating the internal clock int. K. When one shot pulse signal ϕBE is generated, gate circuit **6003** inhibits passage of internal clock int. K. One shot pulse generating circuit **6002** does not respond to the second and the following /BE signals. When burst transfer operation is completed, the circuit **6003** is reset. This resetting is realized by providing a timer and by prohibiting generation of pulses while the timer is operating.

Burst enable control circuitry further includes an address counter **6004** for counting internal clock signals int. K applied from gate circuit **6003** with the initial value thereof set at internal address signal int. Ac applied from an address buffer (see FIG. **32**); and a multiplexer circuit **6007** for selectively passing either the count value of address counter **6004** or internal address signal int. Ac. An output from multiplexer circuit **6007** is transmitted to the SRAM row decoder and the column decoder. Address counter **6004** and multiplexer circuit **6007** are different from the address counter for generating refresh addresses for the refreshing operation and the multiplexer circuit for switching the refresh address and the DRAM address.

The burst enable control circuitry further includes a burst data number storing circuit **6006** for storing the number of data to be transferred in the burst mode and a down counter **6005** for counting down the internal clock signals int. K with the initial count value being the burst data number stored in burst data number storing circuit **6006**. Down counter **6005** starts its counting operation when internal burst enable signal /BE is generated from BE buffer **6001**. Down counter **6005** switches connection path of multiplexer circuit **6007** in accordance with the count value at that time.

Down counter **6005** is reset when internal burst enable signal /BE is inactive at a rising edge of internal clock signal int. K. When internal burst enable signal I3E is active (at "L" level) at a rising edge of internal clock signal int. K, it carries out counting operation. Down counter **6005** controls connection path of multiplexer circuit **6007** such that an output from address counter **6004** is selected during counting operation. Down counter **6005** is reset when the number of burst data stored in the burst data number storing circuit **6006** is counted and switches connection path of multiplexer circuit **6007** such that internal address signal int. Ac from the address buffer is selected. The operation of the structure shown in FIG. **197** will be described with reference to FIG. **198** which is a diagram of signal waveforms.

In normal accessing to SRAM array, chip select signal E# is set "L" and burst enable signal BE# is set to "H" at a rising edge of external clock signal K.

In this state, internal burst enable signal /BE is also at "H", and pulse signal is not generated from one shot pulse generating circuit **6002**. Down counter circuit **6005** is also kept at the reset state. In this state, multiplexer circuit **6007** selects internal address signal int. Ac (cache address) applied from the address buffer and transmits the same to the SRAM row decoder and the column decoder. A part of the address signal may be applied to the DRAM column decoder.

Consequently, the SRAM array is accessed in accordance with the address Ac1 for the SRAM applied at the rising edge of external clock signal K, and data Q1 corresponding to this address Ac1 is output.

When chip select signal E#, cache hit designating signal CH# and burst enable signal BE# are set to "L" at a rising edge of external clock signal K, the burst mode is effected. In this state, a one shot pulse signal ϕBE is generated in response to a rise of internal burst enable signal /BE from one shot pulse generating circuit **6002**. In response to one shot pulse signal ϕBE, address counter **6004** takes internal address signal int. Ac (Ac2) applied from the address buffer as a count initial value, and applies the initial value to multiplexer circuit **6007**. When the one shot pulse signal ϕBE is generated, gate circuit **6003** inhibits transmission of internal clock signal int. K. Therefore, in this clock cycle, the address signal Ac applied at a rising edge of clock signal K is applied from address counter **6004** to multiplexer circuit **6007**.

Down counter **6005** is activated in response to an active state ("L") of internal burst enable signal /BE, and carries out counting-down operation starting at the value stored in burst data number storing circuit **6006**. During the counting operation, down counter **6005** generates a signal indicating that the operation is in the burst mode to multiplexer circuit **6007**. Multiplexer circuit **6007** selects an output from address counter **6004** in response to the burst mode designating signal from down counter **6005**, and applies the output to the SRAM row decoder and the SRAM column decoder. The SRAM array is accessed in accordance with this address Ac2, and corresponding data Q2 is output.

Thereafter, when chip select signal E#, cache hit signal CH# and burst enable signal BE# are set to "L" at a rising edge of external clock signal K, externally applied address signal Ac is neglected, and access to the SRAM array is carried out in accordance with address counter **6004**. Namely, internal clock signal int. K is applied to address counter **6004** through gate circuit **6003**. Address counter **6004** carries out counting operation in accordance with the internal clock signal (count up or count down), and applies the count value to multiplexer circuit **6007**.

Multiplexer circuit **6007** selects the count value of address counter **6004** in accordance with a control signal from down counter **6005** and applies the count to the SRAM row decoder and the SRAM column decoder. Therefore, in the burst mode, access in accordance with the count value from address counter **6004** is effected, and corresponding data Q3, . . . are output every clock cycle. The burst mode operation ends when burst mode enable signal BE# is set to "H" at a rising edge of external clock signal K, or when counting down operation of down counter **6005** is completed.

The burst data number information stored in the burst data number storing circuit **6006** may be fixedly programmed in advance, or it may be stored in a command register or the like at each burst transfer mode.

In the structure shown in FIG. **197**, gate circuit **6003** inhibits transmission of internal clock signal int. K in

accordance with one shot pulse signal φBE. Alternatively, a structure in which address counter **6004** sets internal address int. Ac as a count initial value when internal clock signal int. K and one shot pulse signal φBE are applied may be used, without using gate circuit **6003**.

FIG. **199** shows one example of a specific structure of the address counter circuit. Referring to FIG. **199**, address counter **6004** includes n cascade connected in array counter circuits BCC **1** to BCC n. Binary counter circuits BCC **1** to BCC n are asynchronous type counter circuits and internal clock signal int. K is applied only to the least significant binary counter circuit BCC **1**. Each binary counter circuit effects binary counting operation, and output carrier signals CK**0** to CKn-**1** when count value reaches "1". The carry outputs CK**0** to CKn-**1** are applied to clock inputs of binary counter circuits BCC **2** to BCC n of the succeeding stages, respectively. Complementary count values AO, *A**0** to An and *An-**1** are generated from binary counter circuits BCC **1** to BCC n. Address counter **6004** further includes an up/down switching circuit **6010** for determining whether count up operation or count down operation is to be executed. Up/down switching circuit **6010** selectively passes either the outputs A**0** to An or complementary outputs *A**0** to An-**1** from counter circuits BCC **1** to BCC n in response to an up/down setting signal φUD. When count up operation is set, up/down switching circuit **6010** selects counter outputs A**0** to An. If count down operation is set, up/down switching circuit **6010** selects complementary outputs *A**0** to *An-**1**. Up/down setting signal φUD may be a control signal set in a command register, or it may be a control signal for setting one of the counting operation fixedly by wiring or the like.

The structure of the counter circuit is not limited to that of FIG. **199**. Any counter circuit having a function for setting an initial value may be used.

FIG. **200** shows an example of a specific structure of burst data number storing circuit **6006**. In the structure shown in FIG. **200**, a command register is used as burst data number storing circuit **6006**. Burst data number storing circuit **6006** includes a switching transistor Tr**600** responsive to a control signal φCR for transmitting data DQ applied to data input/output pin terminal; and inverter circuits V**600**, V**601** and V**602** for latching data applied through switching transistor Tr**600**. Inverter circuits V**600** and V**601** constitute a latch circuit.

Control signal φCR is a control signal generated in the command register setting mode. Combination of control signals (command register designating signals Ar, Ar1 and W#) is determined dependent on the command register used for storing the burst data number.

In the structure shown in FIG. **200**, the burst data number information is shown to be applied through data input/output terminal DQ. However, it may be applied through a data input terminal D.

The burst data number information may be stored in a register used for that purpose only, not in a command register.

[Application of Burst Mode Function to Other Memory Devices]

FIG. **201** shows a structure of another semiconductor memory having burst mode function. Referring to FIG. **201**, the semiconductor memory device **6700** includes a memory array **6701** including memory cells arranged in rows and columns, a row decoder **6702** for selecting a row of memory array **6701**, and a column decoder **6703** for selecting a column of memory array **6701**.

Semiconductor memory device **6700** further includes an address buffer circuit **6704** receiving an externally applied address ADD for generating an internal address; an address count circuit **6705** using an output from address buffer circuit **6704** as a count initial value for counting the clock signals from a clock control circuit **6706**; and a multiplexer circuit **6707** responsive to a control signal BE from clock control circuit **6706** for passing either an output from address count circuit **6705** or an output from address buffer circuit **6704**. Row and column address signals are applied from multiplexer circuit **6707** to row decoder **6702** and column decoder **6703**, respectively. Address count circuit **6705** includes the structure of address counter **6004**, down counter **6005** and burst data number storing circuit **6006** shown in FIG. **197**.

Clock control circuit **6706** receives externally applied chip select signal /CS, write enable signal /W, output enable signal /OE and burst mode requesting signal BE and generates respective internal control signals.

The semiconductor memory device **6700** is supposed to be a static type semiconductor memory device or a non-multiplexed address type memory device. However, a dynamic type semiconductor memory device having high speed operation mode such as static column mode or page mode may be used. The structures of address count circuit **6705** and multiplexer circuit **6707** are the same as those described above, and therefore the structures thereof are not shown.

As described above, by providing address count circuit **6705** for generating addresses in the burst mode, it becomes not necessary to externally connect an address generating circuit for the burst mode to the memory device, and therefore system size can be reduced. In addition, wires for connecting the burst mode address counter provided externally to the semiconductor memory device become unnecessary, signal delay in the signal lines for connection and current consumption associated with charging/discharging of the connecting wires can be reduced. In addition, since the address circuit for the burst mode is provided in the semiconductor memory device, connection to the CPU having burst mode function can be readily realized.

In the structure shown in FIG. **197**, an internal address from the address buffer is pre-set as the initial count value in the address counter **6004**. However, the initial count value of address counter **6004** may be set in the command register.

The semiconductor memory device shown in FIG. **201** may be replaced by other semiconductor memory device containing a cache.

[Other Function: Sleep Mode]

An operation mode for reducing current consumption in standby state, that is, a sleep mode will be described with reference to FIGS. **202** through **214**.

In sleep mode operation, internal clock K is inhibited from being generated. If no internal clock K is generated, self refreshing is responsively carried out. The function of the sleep mode is realized by the additional function control circuit **299** shown in FIG. **32**.

As described previously and repeatedly, the CDRAM of the present invention takes address signals, external control signals and write data in synchronization with the external clock signal K. Therefore, even in the standby mode, current is consumed in the buffer receiving these external signals.

FIG. **202** shows a structure of a portion related to **1** bit of the address buffer (**252*in***; FIG. **32**: FIG. **105**, **360**). Referring to FIG. **202**, address buffer **7001** includes a clocked inverter **7011** responsive to internal clock signal int. K for inverting and passing applied data; and inverters **7013** and **7014** for latching an output from clocked inverter **7011**. Clocked

inverter **7011** receives internal clock signal int. K through inverter **7012** at its positive control input, and receives internal clock signal int. K at its complementary control input.

Clocked inverter **7014** receives chip select signal E through inverter **7015** at its positive control input, and receives chip select signal E at its complementary control input.

Inverter **7013** and clocked inverter **7014** are connected in anti-parallel (or cross coupled) to form a latch circuit.

In the structure shown in FIG. **202**, clocked inverter **7011** is set to an output high impedance state in response to a rise of internal clock signal int. K. Clocked inverter **7014** functions as an inverter in response to a fall of chip select signal E. In this state, in response to the fall of chip select signal E, a latch circuit is provided by inverter **7013** and clocked inverter **7014**. Internal address signal int. A is generated from inverter **7013**.

More specifically, at a rising edge of external clock signal K, external address A which has been applied at that time is latched by the latch circuit formed of inverter **7013** and clocked inverter **7014**, and internal address int. A is generated.

As shown in FIG. **202**, even if the chip select signal E is at "H" and the chip is in the non-selected state, internal clock signal int. K is continuously applied. Therefore, in the standby state, clocked inverter **7011** operates and consumes current.

FIG. **203** shows a structure of a clock buffer circuit included in the control clock buffer. FIG. **203** shows a buffer related to chip select signal E# as an example. Referring to FIG. **203**, buffer circuit **7021** includes a p channel MOS transistor **Tr700** receiving internal clock signal int. K at its gate; a p channel MOS transistor **Tr701** receiving external chip select signal E# at its gate; an n channel MOS transistor **Tr702** receiving external chip select signal E# at its gate; and an n channel MOS transistor **Tr703** receiving an inverted signal /int. K of internal clock signal at its gate. Transistor **Tr700** to **Tr703** are connected in series between supply potential Vcc and the other supply potential (ground potential) Vss. In the structure shown in FIG. **203**, the buffer circuit **7021** is set to the output high impedance state at a rising edge of external clock signal int. K, and its output portion is set to a floating state at the signal potential which has been applied thereto. An inverter circuit or a latch circuit may be provided in the next stage of the buffer circuit having the above described structure.

As shown in FIG. **203**, also in the control clock buffer, information is transmitted to the output portion thereof in response to internal clock signal int. K, and consequently, current is consumed even in the standby mode. In view of the foregoing, a structure for reducing current consumption in the standby state will be described in the following.

FIG. **204** is a diagram of signal waveforms showing the sleep mode operation. The sleep mode is set not synchronized with the external clock signal K. The sleep mode is set by command register setting signal CR#. More specifically, when control signal CR# falls to "L", generation of internal clock signal int. K is stopped. Consequently, operations of respective buffer circuits are stopped in the standby state, for example. A circuit structure for realizing the sleep mode will be described.

FIG. **205** is a block diagram functionally showing the circuit structure for realizing the sleep mode. Referring to FIG. **205**, a sleep mode control system includes a sleep control circuit **7052** responsive to control signal CR# for generating a sleep mode control signal SLEEP; and an internal clock generating circuit **7051** responsive to sleep mode control signal SLEEP from sleep control circuit **7052** for controlling generation/stoppage of internal clock signal int. K. Internal clock generating circuit **7051** corresponds to clock buffer **254** shown in FIGS. **32** and **105**. Sleep control circuit **7052** may be included in additional function control circuit **299** shown in FIG. **32**, or a command register may be used.

FIG. **206** shows an example of a specific structure of internal clock generating circuit **7051** shown in FIG. **205**. Referring to FIG. **206**, internal clock generating circuit **7051** includes an inverter circuit **7061** receiving sleep mode control signal SLEEP; an NAND circuit **7062** receiving external clock signal K and an output from inverter circuit **7061**; and an inverter circuit **7063** receiving an output from NAND circuit **7062**. Sleep mode control signal SLEEP is set to "H" when sleep mode is set. The NAND circuit **7062** functions as an inverter when the output from inverter circuit **7061** is at "H". When the output from inverter circuit **7061** is at "L" level, the output of NAND circuit **7062** is fixed to the "H" level.

Therefore, in the structure shown in FIG. **206**, generation and stoppage of internal.clock signal K can be controlled by sleep mode control signal SLEEP.

FIG. **207** shows an example of a specific structure of sleep control circuit **7052** generating the sleep mode control signal.

Referring to FIG. **207**, sleep control circuit **7052** includes a gate circuit (NOR circuit) **7501** receiving external command register setting signal CR# and an output from inverter circuit **7507**; an inverter circuit **7502A** receiving an output from gate circuit **7501**; an inverter circuit **7502B** receiving an output from inverter circuit **7502A**; and a gate circuit (NAND circuit) **7503** receiving an output from inverter circuit **7502B** and an output from gate circuit (NAND circuit) **7506**.

Sleep control circuit **7052** further includes an inverter circuit **7504** receiving external command register setting signal CR#; a gate circuit (NAND circuit) **7505** receiving an output from inverter circuit **7504** and external control signals **Ar0**, Ar1 and W#; a gate circuit **7506** receiving both outputs from NAND circuits **7503** and **7505**; an inverter circuit **7507** receiving an output from gate circuit **7506**; and an inverter circuit **7508** receiving an output from inverter circuit **7507**. Sleep mode control signal SLEEP is generated from inverter circuit **7508**.

A CR# buffer **7600** is further shown in FIG. **207**. CR# buffer **7600** is included in the control clock buffer (see reference numeral **250** in FIG. **33**). CR# buffer **7600** takes the external command register setting signal CR# in response to internal clock signal int. K and generates internal control signal CR.

The operation of sleep control signal **7052** shown in FIG. **207** will be described with reference to FIG. **208** which is a diagram of signal waveforms.

Signals CR#, **Ar0**, Ar1 and W# shown in FIG. **207** are all external control signals. Therefore, sleep control circuit **7052** operates asynchronously with a clock signal K.

When external command register setting signal CR# is at "H", an output from gate circuit **7501** is "L". Therefore, an output from inverter circuit **7502B** is at "L". Meanwhile, an output from inverter circuit **7504** is "L". Therefore, an output from gate circuit **7505** attains **37** H" regardless of the states of control signals **Ar0**, **Ar1** and W#. Gate circuit **7506** receives signals at "H" at both inputs thereof. Consequently, an output from gate circuit **7506** attains "L", and sleep mode control signal SLEEP attains "L".

When sleep mode is to be set, external command register setting signal CR# is set to "L". Control signals Ar0, Ar1 and W# are also set to "H". In this state, gate circuit **7505** receives signals at "H" at its all inputs, and therefore it outputs a signal at "L". Since a signal at "L" is applied to one input of gate circuit **7506**, it outputs a signal at "H", and hence sleep mode control signal SLEEP rises to "H".

When sleep mode control signal SLEEP attains "H", an output from inverter circuit **7507** attains "L". Consequently, both inputs of gate circuit **7501** are at "L", providing an output of "H". Consequently, both inputs of gate circuit **7503** attain "H" level, providing an output of "L".

In this state, a signal at "L" is applied from gate circuit **7503** to one input of gate circuit **7506**, and therefore an output from gate circuit **7506** attains to "H" regardless of the states of external control signals Ar0, Ar1 and W#.

When external command register setting signal CR# rises to "H" at this state, sleep mode control signal SLEEP falls to "L", and thus sleep mode is canceled.

When generation of internal clock signal int. K is stopped by the sleep mode, external refresh designating signal REF# can not be taken at a rising edge of internal clock signal int. K. Therefore, auto-refreshing operation can not be executed. Therefore, in the sleep mode period, self refresh must be carried out instead of auto refresh. A circuit structure for carrying self refreshing in the sleep mode is shown in FIG. **209**.

Referring to FIG. **209**, in order to switch auto/self refresh modes dependent on execution of the sleep mode, a self refresh switching circuit **7401** is provided. Self refresh switching circuit **7401** monitors generation of internal clock signal int. K and when generation of internal clock int. K is stopped, it generates a self refresh switching signal Self.

A refresh timer **7402** is activated in response to self refresh switching signal Self, and generates a refresh requesting signal /REFREQ at a prescribed interval and applies the same to clock generator **7403**. Clock generator **7403** receives external clock signal K, external refresh designating signal REF# and refresh requesting signal /REFREQ from refresh timer **7402**, determines as to whether refreshing is to be executed, and generates various control signals necessary for executing refreshing. A structure shown in FIG. **163** may be used for the clock generator **7403**. Functions carried out by clock generator **7403** are the same as those shown in FIG. **163**. Function of switching input and output is not shown.

Self refresh switching circuit **7401** carries out counting operation in response to a rise of internal clock signal int. K and when internal clock signal int. K is not applied in a prescribed period (for example 1 clock cycle), its generates self refresh switching signal Self. Self refresh switching circuit **7401** is reset in response to a rise of internal clock signal int. K, and sets self refresh switching signal Self to auto refresh designating state. Refresh timer **7402** is the same as that shown in FIG. **162** which generates refresh requesting signal /REFREQ at a prescribed interval in response to self refresh switching signal Self.

Clock generator **7403** takes external refresh designating signal REF# at a rising edge of external clock signal K, and when either refresh designating signal REF# or refresh requesting signal /REFREQ is at active state, carries out necessary operations for refreshing. Internal control signals /RAS and /CAS generated from clock generator **7403** are control signals for controlling decoding operation and the like for the DRAM array.

Refresh address counter **7407** corresponds to refresh address counter shown in FIG. **32** and the like.

In correspondence with the structure shown in FIG. **32**, clock generator **7403** includes auto-refresh mode detecting circuit **291** and refresh control circuit **292**.

FIG. **210** shows a structure of a circuit generating refresh signal REF. The structure shown in FIG. **210** is included in clock generator **7403** shown in FIG. **209**. Referring to FIG. **210**, the circuit for generating refresh signal REF includes a REF buffer **7440** responsive to internal clock signal int. K for latching external refresh designating signal REF#; and a gate circuit **7450** receiving an output from REF buffer **7440** and refresh requesting signal /REFREQ from refresh timer **7402**. Gate circuit **7450** outputs a signal at "H" when one input thereof attains to "L". When refresh signal REF attains "H", refreshing is carried out.

FIG. **211** is a diagram of signal waveforms showing the operation of the circuit shown in FIG. **209**. Switching operation between auto refresh/self refresh in the sleep mode will be described with reference to FIGS. **209** to **211**.

At time t1, the sleep mode is set and generation of internal clock signal int. K is stopped. Self refresh switching circuit **7401** starts counting operation from time t1, and after a prescribed time period, generates self refresh switching signal Self at time t2 and applies the same to refresh timer **7402**. Refresh timer **7402** generates refresh requesting signal/REFREQ in response to self refresh switching signal Self and applies the same to clock generator **7403**.

Clock generator **7403** generates refresh signal REF in response to refresh requesting signal /REFREQ and generates internal control signal /RAS. At this time, generation of internal control signal /CAS is stopped. In response to internal control signal /RAS, row selecting operation and sensing operation are carried out in the DRAM array and self refreshing is effected.

Refresh timer **7402** generates refresh requesting signal /REFREQ every prescribed period. In response, internal control signal /RAS rises to "L" to effect refreshing. Refresh address of refresh address counter **7407** is incremented or decremented every refresh cycle.

When sleep mode is canceled at time t3, self refresh switching circuit **7401** is reset and generation of self refresh switching signal Self is stopped. Consequently, counting operation of refresh timer **7402** is reset and prohibited.

In the structure shown in FIG. **209**, self refresh switching circuit **7401** monitors internal clock signal int. K and generates self refresh switching signal Self. Self refresh switching circuit **7401** may include a structure for monitoring sleep mode control signal SLEEP. A structure in which refresh timer **7402** is activated in response to sleep mode control signal SLEEP may be used.

Further, refresh control system shown in FIG. **209** may be commonly used with auto refresh/self refresh switching circuit shown in FIG. **162**.

FIG. **212** shows another example of circuit structure for generating sleep mode control signal SLEEP. In the structure shown in FIG. **212**, sleep mode is set by external chip select signal E# and array access designating signal CI# (corresponding to CC1r). Referring to FIG. **212**, sleep mode control circuit **7052** includes an inverter circuit **7601** receiving internal chip select signal CE#; a gate circuit **7602** receiving an output from inverter circuit **7601** and an output from gate circuit **7604**; an inverter circuit **7603** receiving external array access designating signal CI#; a gate circuit **7604** receiving an output from gate circuit **7602** and an output from inverter circuit **7603**; and an inverter circuit **7605** receiving an output from gate circuit **7604**.

FIG. **212** also shows an E buffer **7650** and CI buffer **7651** included in the control clock buffer. E buffer **7650** and CI

buffer 7651 take external signals E# and CI# at a rising edge of internal clock signal int. K, respectively and generate internal control signals E and CI.

FIG. 213 is a diagram of signal waveforms showing the operation of the circuit shown in FIG. 212. Sleep mode setting operation will be described with reference to FIGS. 199 and 200.

In the circuit structure shown in FIG. 199, sleep mode is set by a combination of external control signals E# and CI#. When chip select signal E# is at "H" and cache access inhibiting signal CI# is at "L", the sleep mode is set. In this state, an output from gate circuit 7602 attains "H" and an output from inverter circuit 7603 attains "H". Since both inputs of gate circuit 7604 are at "H" level, the circuit 7604 outputs a signal at "L". Consequently, sleep mode control signal SLEEP from inverter circuit 7605 rises to "H".

When cache access inhibiting signal CI# rises to "H", an output from gate circuit 7604 rises to "H" and sleep mode control signal SLEEP falls to "L". In the structure shown in FIG. 212, length of the sleep mode period is determined by cache access inhibiting signal CI#.

Chip select signal E# and cache access inhibiting signal CI# are used as control signals when the DRAM array is to be directly accessed (namely, when chip select signal E# is at "L" and cache access inhibiting signal CI# is at "L" at a rising edge of clock signal K in FIG. 213, the DRAM array is directly accessed).

Therefore, in order to prevent setting of sleep mode when direct access cycle to the array is set, a setup time Tsetup and hold time Thold is set for chip select signal Et and cache access inhibiting signal CI#, as shown in FIG. 214. Namely, referring to FIG. 214, a setup time Tsetup from the fall of chip select signal E# to "L" until transition of cache access signal CI# to "L", and a hold time Thold from the time when access inhibition signal CI# attains "H" until the time when the chip select signal E# attains "H" are designated. When the array is accessed, cache access inhibition signal CI# changes to "L" after chip select signal E# has changed to "L". Consequently, a state in which cache access signal CI# falls to "L" when chip select signal E# is "H" in direct access to the array can be prevented, and therefore erroneous setting of the sleep mode can be prevented. In addition, the signal CI rises to "H" by at least the hold time T hold before the signal E# rises to "H" in an array access setting cycle. Thus, erroneous setting of the sleep mode is also prevented in this case.

[Summary of Internal Operation Cycle]

FIG. 215 is a table showing combinations of states of control signals for setting operation modes of the CDRAM. The operation modes of the CDRAM shown in FIG. 215 correspond to those shown in FIG. 51 but modified corresponding to 3 additional functions. In the structure shown in FIG. 215, burst mode operation, high speed copy back operation and data transfer using latches between DRAM and SRAM array are added.

The additional functions shown in FIG. 215 will be described briefly. The burst mode is set by setting control signals E#, CH# and CC2# (CR#) to "L" and control signal CC1# (CI#) to "H". The state of write enable signal W#determines whether data writing or data reading is to be carried out. If write enable signal W# is at "H", a hit read burst operation is carried out. If write enable signal W# is at "L", a hit write burst operation is carried out.

Cache hit operation as well as data transfer operation to the DRAM array are carried out when control signals E#, CH# and CC1# (CI#) are set to "L" and control signal CC2# (CR#) is set to "H". Namely, in this state, data writing/reading is carried out between tile cache (SRAM) and the CPU, and data which has been latched by latching means included in the transfer gate are transferred to the DRAM array. The state of write enable signal W# determines whether hit read operation or hit write operation is to be carried out.

In the state of a cache miss, data is transferred from the cache to the latching means included in the transfer gate and data is transferred from the DRAM array to the SRAM array (cache), and data writing/reading with the CPU is done through the cache (SRAM). This state is set by setting chip select signal E# to "L". The write enable signal W# determines whether the operation is a miss read or miss write.

The array write operation in which data transfer from the latch (included in the data transfer gate) to the DRAM array when high speed copy back mode operation is to be carried out, is set by setting control signals E# and CC2# (CR#) to "L" and control signals CH# and CC1# (CI#) to "H". In this state, data is transferred from the latch to the DRAM array in the high speed copy back mode. By setting control signals E#, CC2# and W# to "L" and control signals CH# and CC1# (CI#) to "H", data is transferred from the cache (SRAM array) to the DRAM array. Consequently, the DRAM array is initialized.

When control signals E# and CC1# (CI#) are set to "L" and control signals CH# and CC2# (CR#) to "H", the array can be directly accessed. Whether writing or reading of data is to be carried out is determined by write enable signal W#.

[Structure for Providing Optimal CDRAM]

A combination of functions effective in practice is a combination of: a structure allowing independent address designation of the DRAM and the SRAM; a structure for generating internal voltages by using continuously input clock signals; a structure of a data transfer path including two separated paths, that is, internal data transfer path and a data writing path; a structure for carrying out automatic refresh of the DRAM array while the SRAM array is being accessed; a structure for writing data to the DRAM array simultaneously with writing of data to the SRAM array at cache miss writing; a structure allowing selection of high speed operation mode and low power consumption mode; a structure facilitating connection to the CPU having burst mode function; a structure having the sleep mode for reducing standby current; and a structure for carrying out self refreshing even in the normal mode.

The structure for generating internal voltages by the clock K is a structure in which a charge pump is operated by the clock K to generate a desired internal voltage such as substrate bias voltage.

(2) A structure of the most effective CDRAM comprises the following functions: a structure allowing independent selection of a DRAM cell and a SRAM cell; a structure for generating internal voltages in accordance with external clock signals; a structure of data transfer path having two routes of internal transfer path and data writing path; high speed copy back mode function; a structure for carrying out automatic refreshing of the DRAM array while the SRAM array is being accessed; a structure for writing write data to the SRAM array at a cache miss writing; a structure in which SRAM addresses and DRAM column addresses are commonly used; a structure for switching methods of address generation dependent on the burst mode operation; sleep mode function; a structure for carrying out self refreshing even in the normal mode; and a structure for separating data writing path from the data reading path in the DRAM array.

[Effects of the Invention]

According to the first aspect of the present invention, switching between self refresh mode and auto refresh mode

is done by refresh mode setting means. In the auto refreshing mode, one terminal is used as a refresh designating input terminal, and in the self refresh mode, it is used as a self refresh execution designating output terminal. Therefore, even in the self refresh mode, refresh timing can be known outside the semiconductor memory device, and therefore self refresh mode can be utilized even in the normal mode.

According to the second aspect of the present invention, input terminals for designating rows and columns of the first and second memory arrays are separately provided for inputting row addresses and column addresses. Consequently, the row address signals and column address signals can be applied in a non-multiplexed manner to the first and second memory arrays. A part of the address signals for the first memory array and a part of address signals for the second memory array are applied to the same input terminal. Therefore, a structure in which addresses are applied to the first and second memory arrays in address non-multiplexed manner can be realized without increasing the number of input terminals.

According to a third aspect of the present invention, the first and second address signals are simultaneously taken in synchronization with external clock signals and internal address signals are generated. Therefore, a clock synchronized type semiconductor memory device can be operated at high speed.

According to a fourth aspect of the present invention, data transfer means is activated at an earlier timing than the activation timing of sense amplifiers of the DRAM array, and data can be transferred at high speed from the DRAM array to the SRAM array. Therefore, a CDRAM which can access at high speed even at a cache miss can be provided.

According to a fifth aspect of the present invention, a current mirror type amplifier constitutes data transfer means and also potential amplifier of the DRAM bit line, and therefore data transfer means can be activated without waiting for activation of the latch type sense amplifier of the DRAM. Consequently, data can be transferred at high speed from the DRAM array to the SRAM array.

According to a sixth aspect of the present invention, a counter starts its operation in response to a burst mode designation from an external operational processing unit, and outputs from the counter are used as address signals in the burst mode. Therefore, a semiconductor memory device which can be readily connected to an external operational processing unit having burst mode function can be provided.

According to the seventh aspect of the present invention, the counter executes counting operation in synchronization with external clock signals, and the counter outputs are used as addresses in the burst mode. Except the burst mode, externally applied address signals are used. Therefore, a clock synchronized type semiconductor memory device which can be readily connected to an external operational processing unit having burst mode function can be realized.

According to an eighth aspect of the present invention, generation of internal clock signals is stopped when the clock synchronized type semiconductor memory device is in the standby state. Consequently, operation of a circuit for taking signals in synchronization with internal clock signals, such as a control signal input buffer, can be stopped in the standby state, and accordingly current consumption in the standby state of the semiconductor memory device can be reduced.

According to a ninth aspect of the present invention, since self refresh mode is executed when generation of internal clock signals in the invention in accordance with the eighth aspect, and therefore data in the DRAM array can be surely retained even in the standby state.

According to a tenth aspect of the present invention, a row address signal and a column address signal are taken at the first and the second timings of the clock signal in a clock synchronized type semiconductor memory device, and therefore even if the clock signal has a long period or the clock signals are generated intermittently, a semiconductor memory device which can operate at high speed can be provided.

According to an eleventh aspect of the present invention, setting means for previously setting timings for taking addresses of the semiconductor memory device in accordance with an address timing designating signal is provided, and external addresses are taken in accordance with the address signal taking timings set in the setting means. Therefore, a semiconductor memory device which can flexibly correspond to applications in which high speed operation is given priority and applications in which low power consumption are given priority can be provided.

According to the twelfth aspect, SRAM array has a multiplicate word line architecture, and therefore SRAM array can be easily laid out in a desired physical dimensions to provide high density and high integration CDRAM.

According to the thirteenth and fourteenth aspects, the clamping circuit at a data receiving side has the clamping operation in data transfer between SRAM and DRAM, so that high speed data transfer with less current consumption can be implemented.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

What is claimed is:

1. A synchronous memory comprising:

a clock buffer for receiving a single clock signal;

an internal signal generator for taking an external signal in response to rising and falling edges of the single clock signal to generate an internal signal according to the external signal; and

a plurality of memory cells accessed in response to the internal signal.

2. The synchronous memory according to claim 1, wherein

said external signal includes an external address signal,

said internal signal includes an internal address signal, and

said internal signal generator includes an address generating circuit taking the external address signal as the internal address signal in response to the rising and falling edges of the single clock signal.

3. A synchronous semiconductor memory device, comprising:

a clock buffer for receiving an externally applied clock signal formed of a series of pulses each having a rising edge and a falling edge, and generating an internal clock signal corresponding to said externally applied clock signal;

internal signal generating circuitry responsive to the internal clock signal for taking in and latching an external signal to generate an integral signal according to the external signal, said internal signal generating circuitry taking in and latching successively applied external signals in response to rising and falling edges of a single pulse of the internal clock signal; and

a memory cell array having a plurality of memory cells arranged in rows and columns and accessed in response to the internal signal.

4. The semiconductor memory device according to claim 3, wherein

said external signal includes an external address signal designating an address of a memory cell in said memory cell array,

said internal signal includes an internal address signal, and

said internal signal generating circuitry includes an address generating circuit for taking in and latching the external address signal as the internal address signal in response to the rising and falling edges of the single pulse of the internal clock signal.

5. The semiconductor memory device according to claim 4, wherein

said external address signal includes an external row address signal designating a row of the memory cells in said memory cell array, and an external column address signal designating a column of the memory cells in said memory cell array,

said internal signal generating circuitry includes a row address circuit circuit for taking in and latching the external row address signal, in response to the rising edge of the single pulse, to generate an internal row address signal, and a column address circuitr for taking in the external address signal, in response to the falling edge of the single pulse, to generate an internal column address signal.

* * * * *

US006591353B1

(12) **United States Patent**
Barth et al.

(10) **Patent No.: US 6,591,353 B1**
(45) **Date of Patent: *Jul. 8, 2003**

(54) **PROTOCOL FOR COMMUNICATION WITH DYNAMIC MEMORY**

(75) Inventors: **Richard Maurice Barth**, Palo Alto, CA (US); **Frederick Abbot Ware**, Los Altos Hills, CA (US); **John Bradly Dillon**, Palo Alto, CA (US); **Donald Charles Stark**, Woodside, CA (US); **Craig Edward Hampel**, San Jose, CA (US); **Matthew Murdy Griffin**, Mountain View, CA (US)

(73) Assignee: **Rambus Inc.**, Los Altos, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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(51) **Int. Cl.**^{7} **G06F 12/00**
(52) **U.S. Cl.** **711/167**; 710/100; 710/107
(58) **Field of Search** 710/100–107; 711/167

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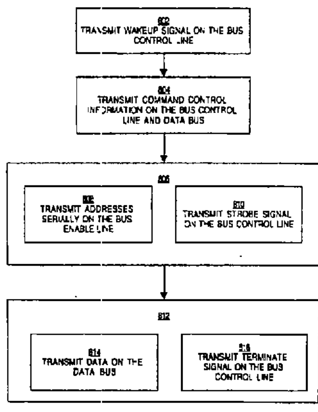
Primary Examiner—David Wiley
Assistant Examiner—George Neurauter

(57) **ABSTRACT**

A system and method for performing data transfers within a computer system is provided. The system includes a controller configured to dynamically adjust the interleave of the communications required to perform a series of data transfer operations to maximize utilization of the channel over which the communications are to be performed. The controller is able to vary the time interval between the transmission of control information that requests a data transfer and the performance of the data transfer by signaling the beginning of the data transfer with a strobe signal sent separate from the control information. The controller is able to defer the determination of how much data will be transferred in the operation by initiating the termination of a data transfer with a termination signal. The method provides a technique for distinguishing between identical control signals that are carried on the same line. The system includes a memory device with control circuitry that allows no more than one memory bank powered by any given power supply line to perform sense or precharge operations.

26 Claims, 21 Drawing Sheets



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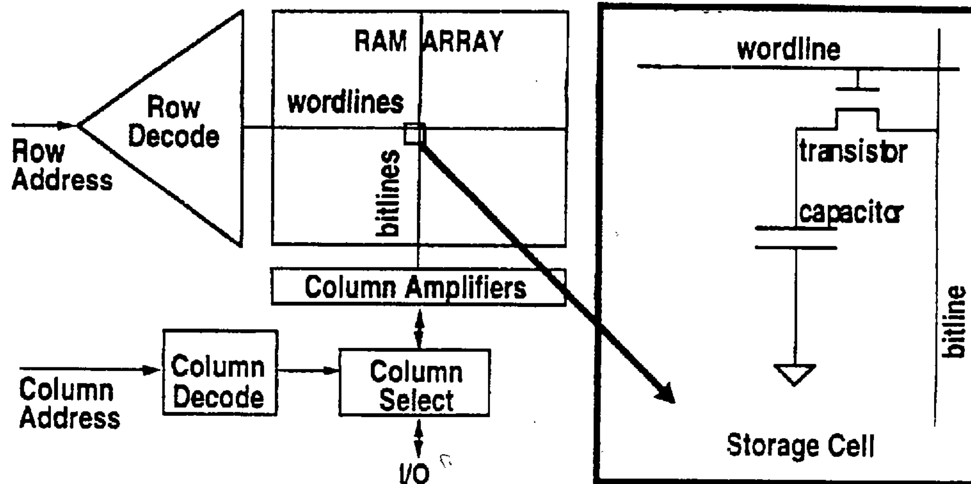

Figure 1A (Prior Art)

Figure 1B (Prior Art)

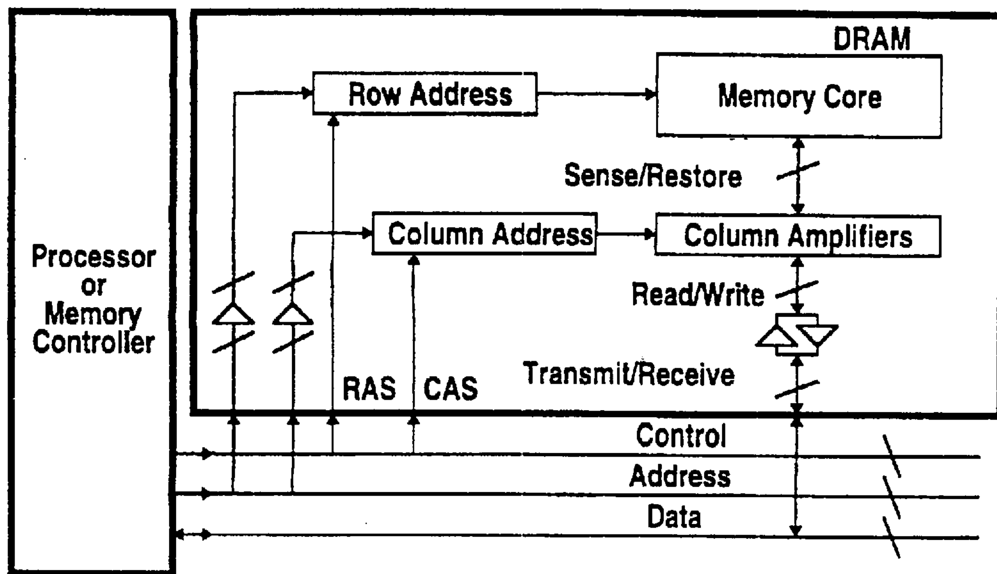

Figure 2
(Prior Art)

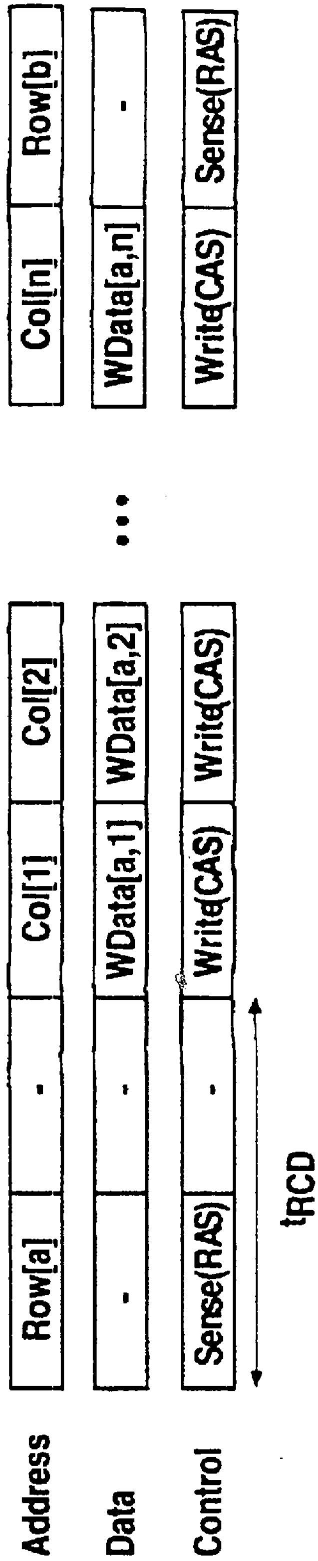

Figure 3A
(Prior Art)

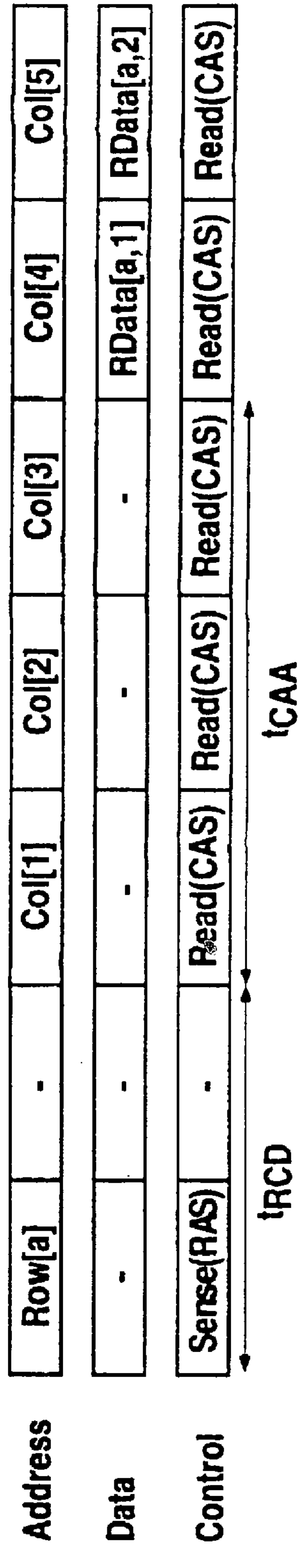

Figure 3B
(Prior Art)

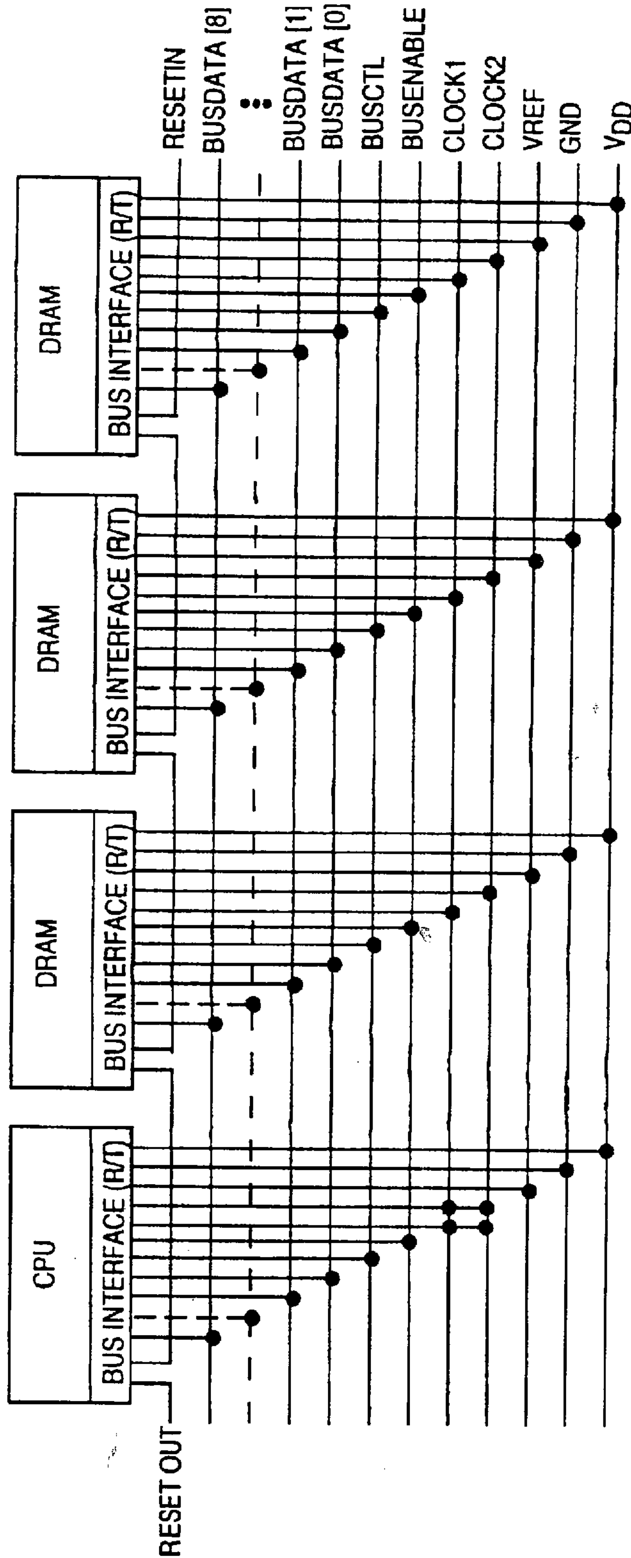

Figure 4
(Prior Art)

Clock Cycle	Bus-Enable	Bus-Ctrl	BusData								
			[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
OE	N	START	Op [0] 510	Adr [9:2] 502							
0O	N	Op 514	Op [3] 512	Adr [17:10] 504							
1E	N	OpX [1] 516	Adr [26:18] 506								
1O	N	Op [2] 518	Adr [35:27] 508								
2E	N	OpX [0] 520	U	U	Count [6,4,2] 522			U	U	U	U
2O	N	U	U	U	Count [7,5,3] 524			Count [1:0] 528		Adr [1:0] 501	

500

Figure 5
(Prior Art)

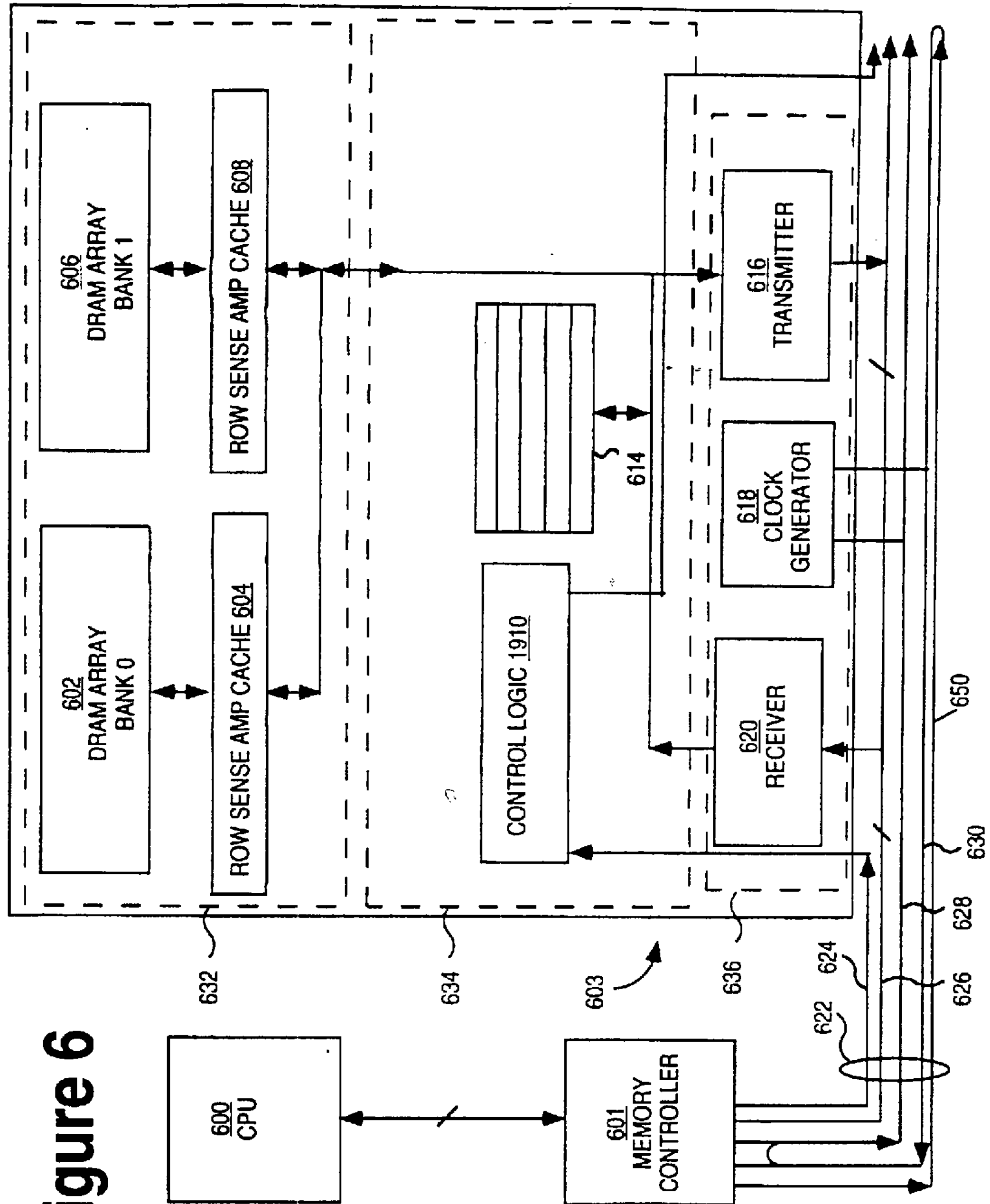
Figure 6
600 CPU
601 MEMORY CONTROLLER
602 DRAM ARRAY BANK 0
606 DRAM ARRAY BANK 1
ROW SENSE AMP CACHE 604
ROW SENSE AMP CACHE 608
CONTROL LOGIC 1910
614
616 TRANSMITTER
618 CLOCK GENERATOR
620 RECEIVER
603
622
624
626
628
630
632
634
636
650

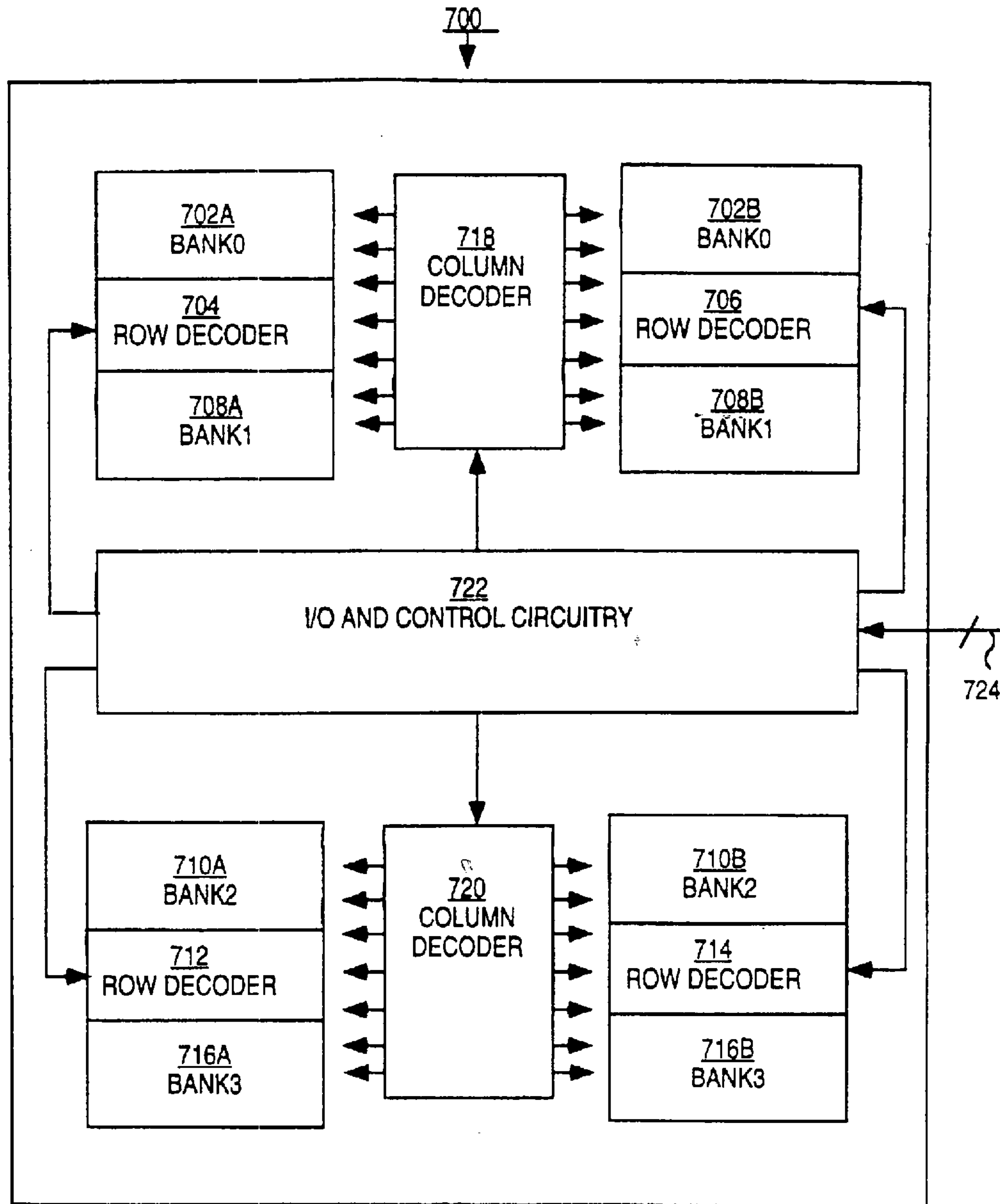

Figure 7

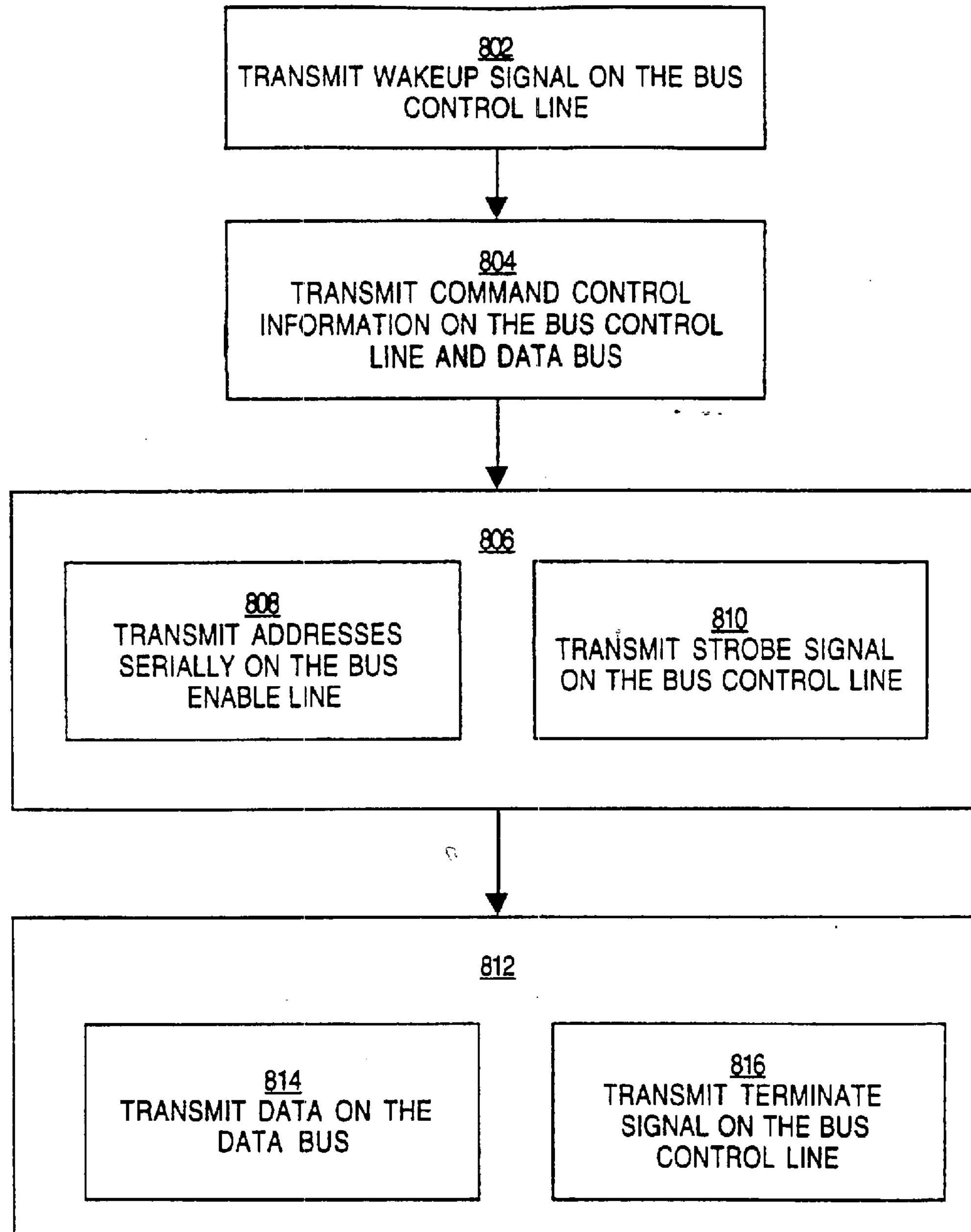

Figure 8

Clock Cycle	Bus-Enable	Bus-Ctrl	BusData								
			[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]:
OE	N	START 902	Op[0] 'Write' 906	Adr [9:2]							
0O	N	Op[1] 'Reg' 908	Op[3] 'Bcst' 912	Adr [17:10]							
1E	N	OpX[1]	Adr [26:18]								
1O	N	Op[2] 'NoByteM' 910	Adr [35:27]								
2E	N	OpX[0]	U	U	U	EvalCC	Open	Close	Pend [2:0]		
2O	N	U	U	Mask [7:0];							

904

Figure 9

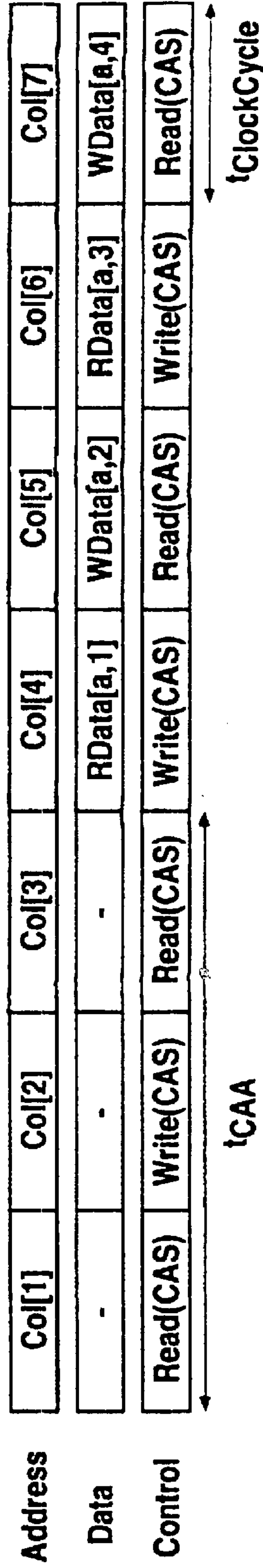

Figure 10
Prior Art

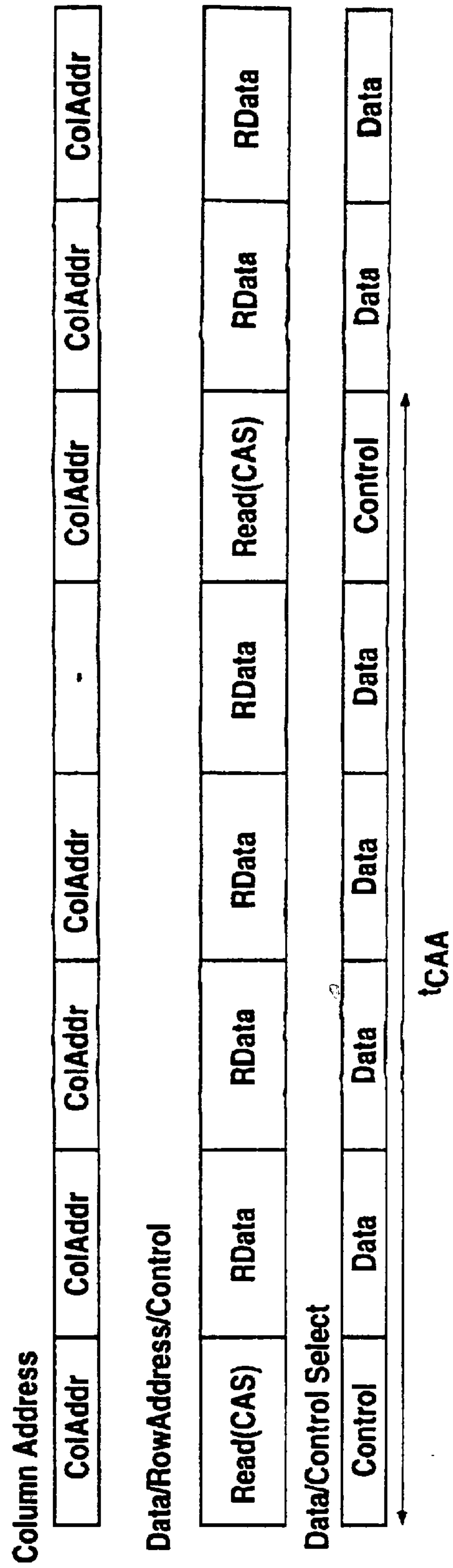

Figure 11
Prior Art

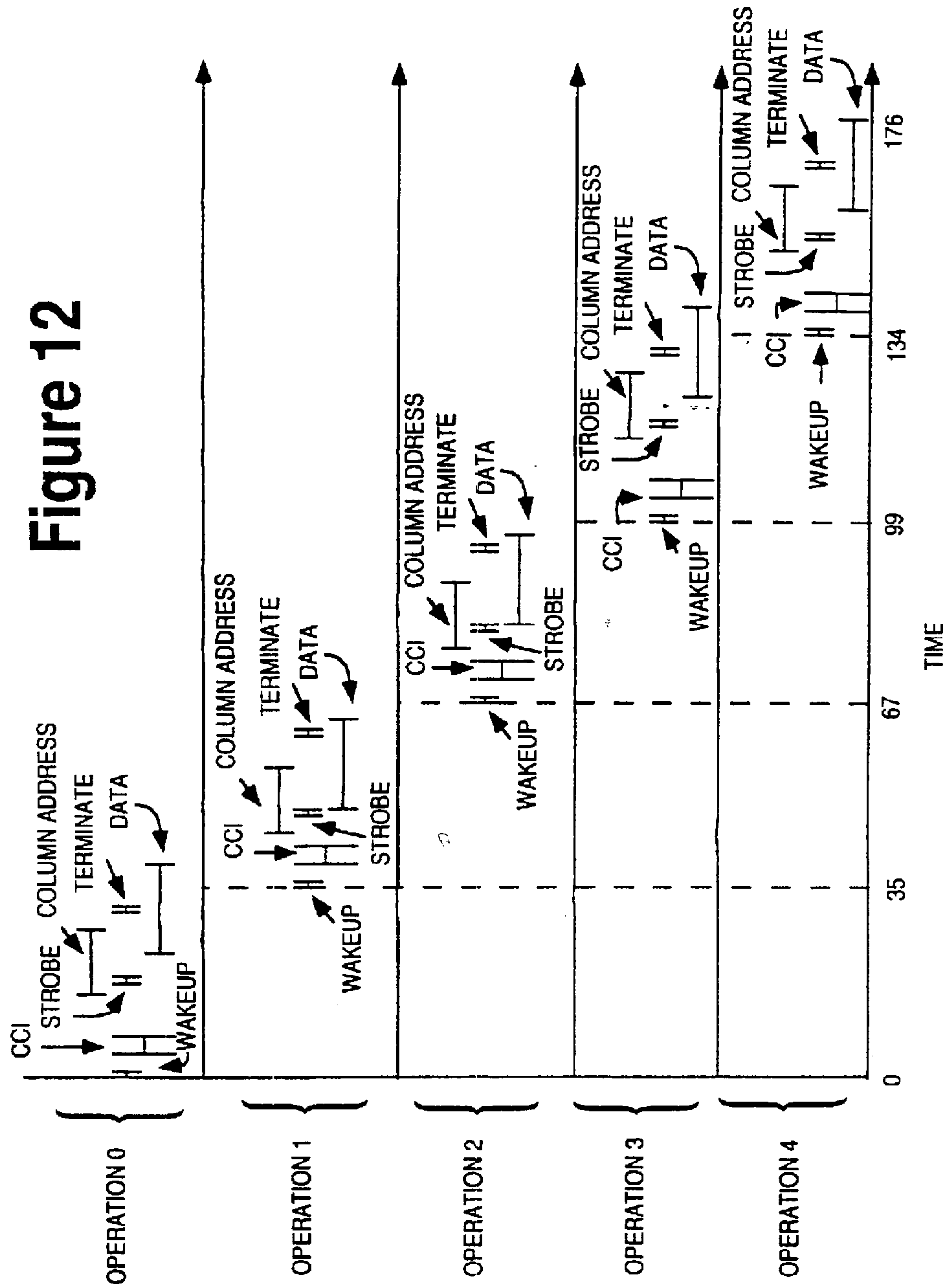

Figure 12

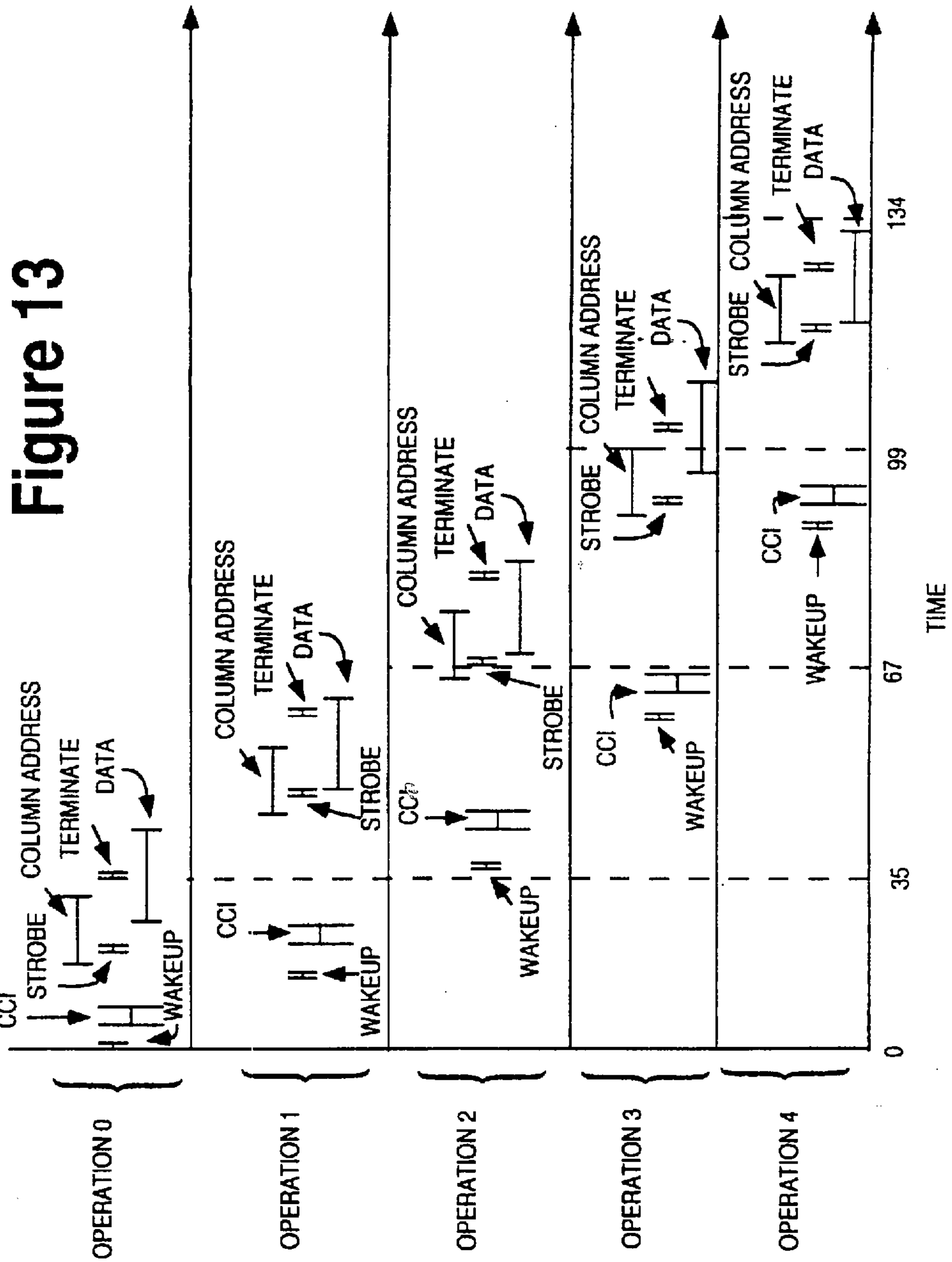
Figure 13
OPERATION 0
OPERATION 1
OPERATION 2
OPERATION 3
OPERATION 4
CCI
STROBE
COLUMN ADDRESS
TERMINATE
DATA
WAKEUP
0
35
67
99
134
TIME

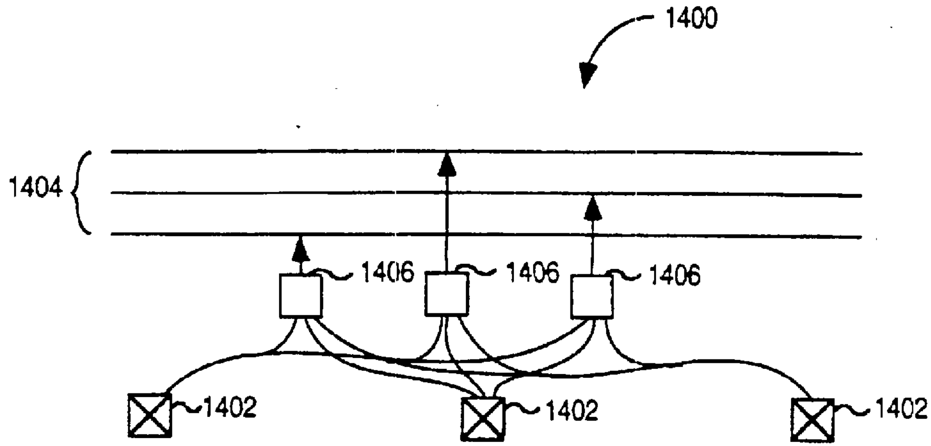

Figure 14
PRIOR ART

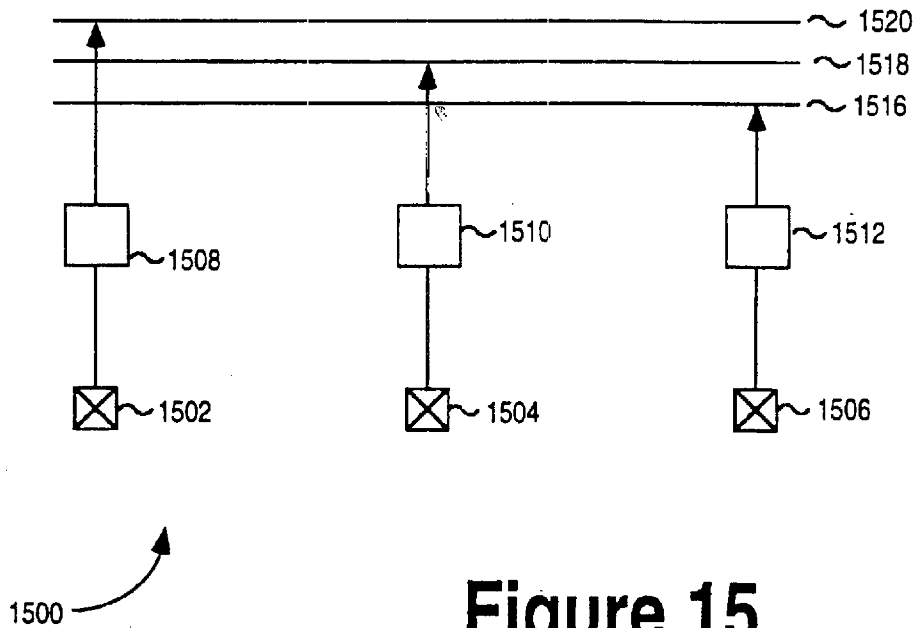

Figure 15

ACTION	Op[3] - Bcst	Op[2] - NoByte M	Op[1] - Reg	Op[0] - Write	ReadOp	WriteOp	RegOp	ReadRegOp	Rreg	WriteRegOp	Wreg	WregB
ILLEGAL	0	0	0	0		X						
MEMORY WRITE DIRECTED BYTE MASK	0	0	0	1								
ILLEGAL	0	0	1	0								
ILLEGAL	0	0	1	1								
MEMORY READ DIRECTED	0	1	0	0	X							
MEMORY WRITE DIRECTED	0	1	0	1		X						
REGISTER READ DIRECTED	0	1	1	0	X		X	X	X			
REGISTER WRITE DIRECTED	0	1	1	1		X	X			X	X	
ILLEGAL	1	0	0	0								
MEMORY WRITE BROADCAST BYTE MASK	1	0	0	1		X						
ILLEGAL	1	0	1	0								
ILLEGAL	1	0	1	1								
ILLEGAL	1	1	0	0								
MEMORY WRITE BROADCAST	1	1	0	1		X						
ILLEGAL	1	1	1	0								
REGISTER WRITE BROADCAST	1	1	1	1		X	X			X		X

Figure 16A

ACTION	MemOp	ReadMemOp	ReadMemDirectedOp	WriteMemOp	WriteMemNoByteMaskOp	WriteMemNoByteMaskDirectedOp	WriteMemNoByteMaskBradcastOp	WriteMemByteMaskOp	WriteMemByteMaskDirectedOp	WriteMemByteMaskBroadcastOp	RsrvOp	BroadcastOp
ILLEGAL											X	
MEMORY WRITE DIRECTED BYTE MASK	X			X				X	X			
ILLEGAL											X	
ILLEGAL											X	
MEMORY READ DIRECTED	X	X	X									
MEMORY WRITE DIRECTED	X			X	X	X						
REGISTER READ DIRECTED												
REGISTER WRITE DIRECTED												
ILLEGAL											X	
MEMORY WRITE BROADCAST BYTE MASK	X			X				X		X		X
ILLEGAL											X	
ILLEGAL											X	
ILLEGAL											X	
MEMORY WRITE BROADCAST	X			X	X		X					X
ILLEGAL											X	
REGISTER WRITE BROADCAST												X

Figure 16B

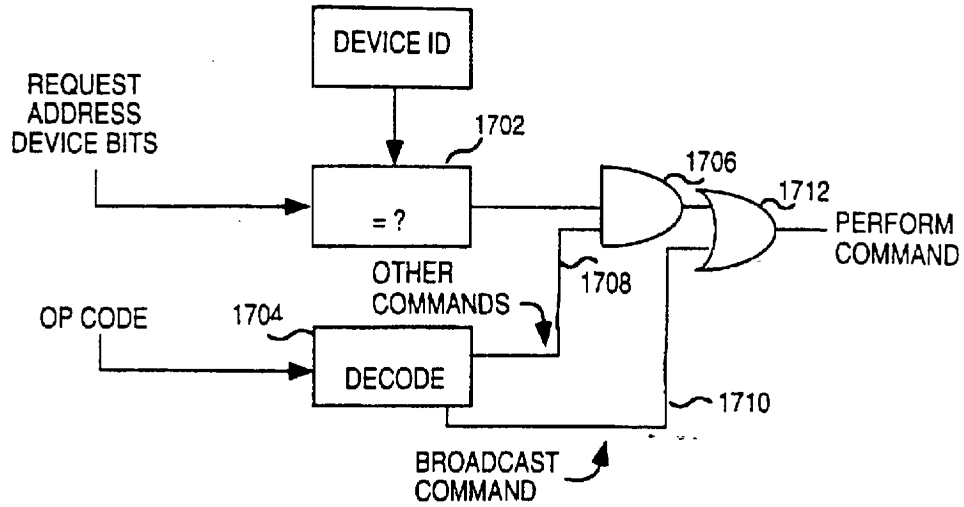

Figure 17

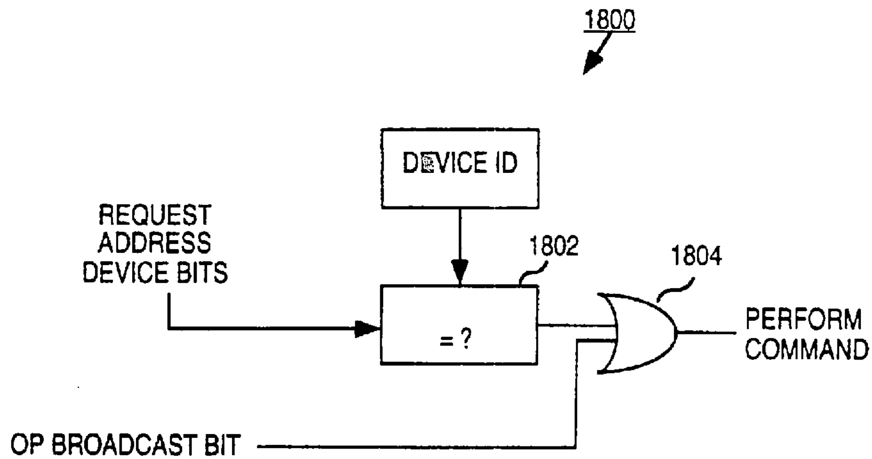

Figure 18

OPEN	CLOSE	Current BANK STATE	NEW BANK STATE	ACTION
0	0	CLOSED	CLOSED	ILLEGAL
0	1	CLOSED	CLOSED	NO ACTION
1	0	CLOSED	OPEN	SENSE-CARD
1	1	CLOSED	CLOSED	SENSE-COMMAND-PRECHARGE
0	0	OPEN	OPEN	COMMAND
0	1	OPEN	CLOSED	COMMAND-PRECHARGE
1	0	OPEN	OPEN	PRECHARGE-SENSE-COMMAND
1	1	OPEN	CLOSED	PRECHARGE-SENSE-COMMAND-PRECHARGE

Figure 19

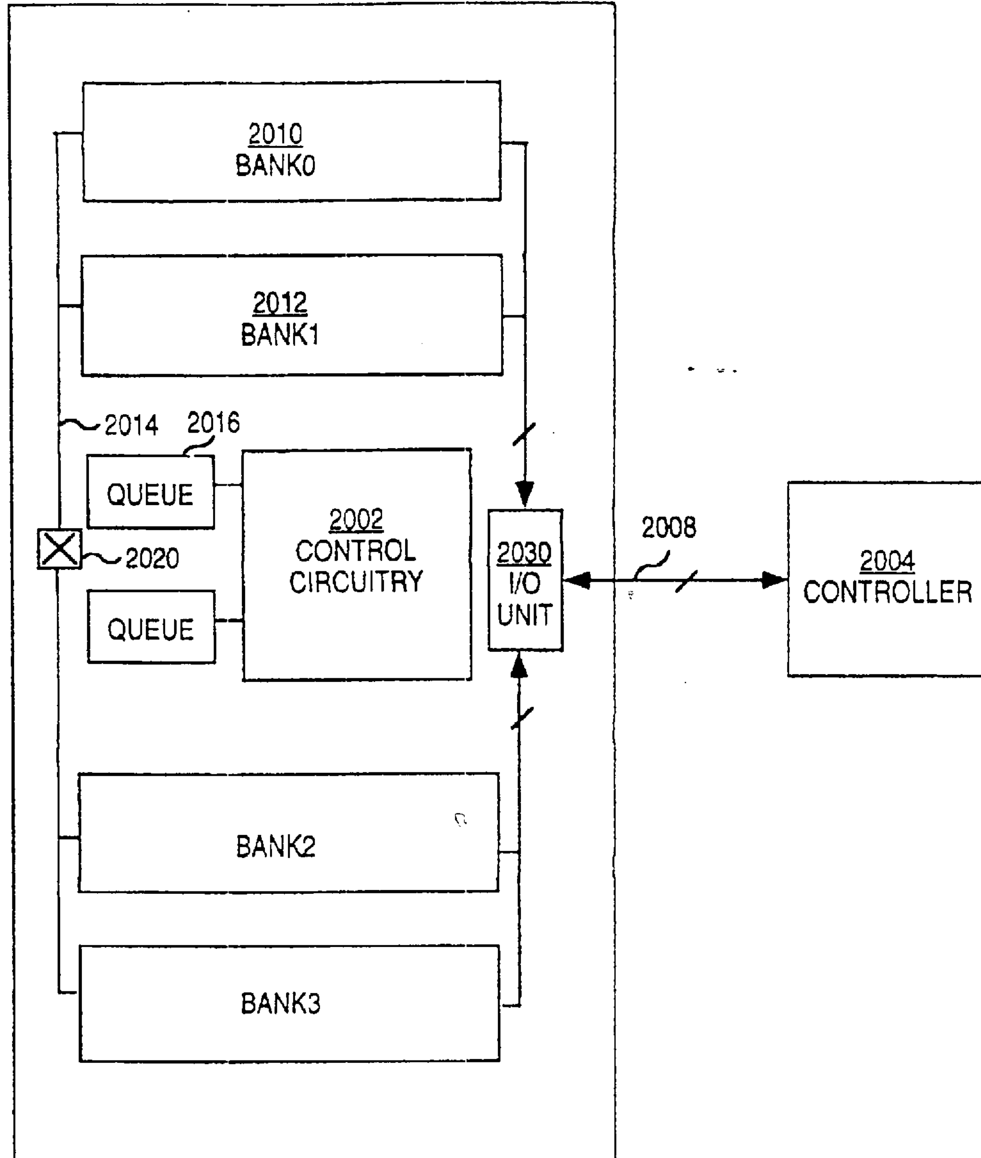

Figure 20A

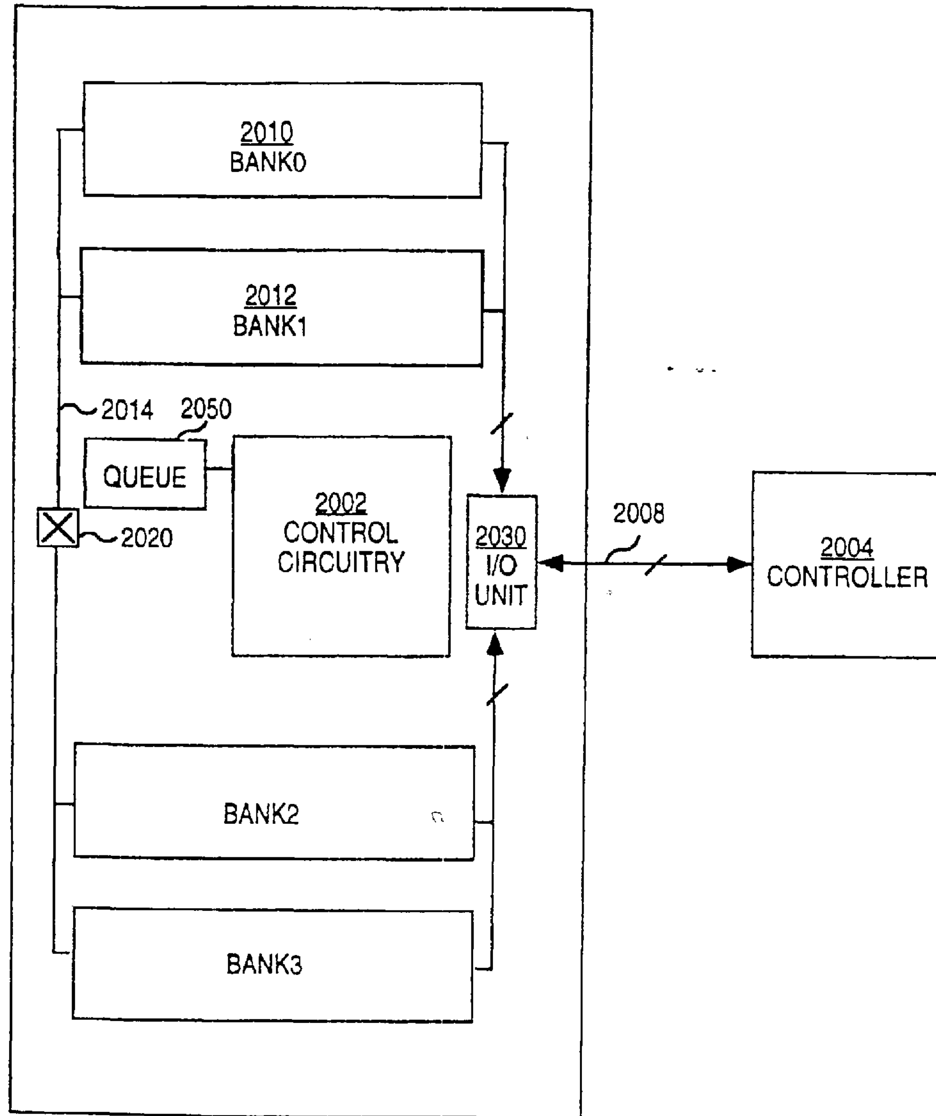

Figure 20B

PROTOCOL FOR COMMUNICATION WITH DYNAMIC MEMORY

This application is a continuation of application Ser. No. 09/480,767, filed on Jan. 10, 2000; which is a continuation of application Ser. No. 08/979,402, filed on Nov. 26, 1997; which is a division of application Ser. No. 08/545,292 filed on Oct. 19, 1995 (now U.S. Pat. No. 5,748,914).

FIELD OF THE INVENTION

The present invention relates to dynamic random access memory (DRAM), and more specifically, to a method and apparatus for controlling data transfers to and from a dynamic random access memory.

BACKGROUND OF THE INVENTION

Dynamic random access memory (DRAM) components, such as those illustrated in FIG. 1A, provide an inexpensive solid-state storage technology for today's computer systems. Digital information is maintained in the form of a charge stored on a two-dimensional array of capacitors. One such capacitor is illustrated in FIG. 1B.

FIG. 2 illustrates a prior art memory system including DRAM with the corresponding control, address and data wires which connect the DRAM to the processor or memory controller component. In synchronous DRAMs, a write access is initiated by transmitting a row address on the address wires and by transmitting row address strobe (RAS) signal. This causes the desired row to be sensed and loaded by the column amplifiers. The column address is transmitted on the address wires and the column address strobe (CAS) signal is transmitted along with the first word of the write data WData(a,1). The data word is then received by the DRAM and written into the column amplifiers at the specified column address. This step can be repeated "n" times in the currently loaded row before a new row is sensed and loaded. Before a new row is sensed, the old row must be restored back to the memory core and the bit lines of the DRAM precharged.

FIG. 3A illustrates synchronous write timing. In the figure, a, b . . . represent a row address; 1, 2 . . . n represent a column address, WData [row, col] represents the DRAM address of data words, the row address strobe (RAS) is a control signal for initiating a sense operation, and WRITE (CAS) initiates the write operation on the column amplifiers. In the present example, the row column address delay timing parameter is equal to two clock cycles. After the row address is asserted at the first clock cycle, column addresses and write data are asserted after the delay to write the data into the DRAM array.

FIG. 3B illustrates synchronous read timing. A processor initiates a read access by transmitting a row address on the address wires and by transmitting the row address strobe (RAS) signal. This causes the desired row to be sensed by the column amplifiers. The column address is then transmitted on the address wire and the column address strobe (CAS) signal is transmitted. The first word of the read data RData (a,1) is then transmitted by the DRAM and received by the processor. This step can be repeated "n" times in the currently loaded row before a new row is sensed and loaded. Before a new row is sensed, the old row must be restored back to the memory array.

Various attempts have been made to improve the performance of conventional DRAMs. Such attempts have resulted in DRAM architectures that deviate in varying degrees from conventional DRAM architectures. Various alternative DRAM architectures are described in detail in NEW DRAM TECHNOLOGIES, by Steven A. Przybylski, published by MicroDesign Resources, Sebastopol, Calif. (1994). Some of those architectures are generally described below.

Extended Data-Out DRAMS

The prior art includes Extended Data-Out (EDO) memory systems. In EDO DRAMs, the output buffer is controlled by signals applied to output enable (OE) and column address stobe (CAS) control lines. In general, data remains valid at the output of an EDO DRAM longer than it does for conventional DRAMs. Because the data remains valid longer, the transfer of the data to the latch in the memory controller can be overlapped with the next column precharge. As a result, burst transfers can be performed in fewer clock cycles.

Synchronous DRAMS

The prior art also includes Synchronous DRAM (SDRAM) memory systems. The interface of an SDRAM includes a multiplexed address bus and a high-speed clock. The high speed clock is used to synchronize the flow of addresses, data, and control on and off the DRAM, and to facilitate pipelining of operations. All address, data and control inputs are latched on the rising edge of the clock. Outputs change after the rising edge of the clock. SDRAMs typically contain a mode register. The mode register may be loaded with values which control certain operational parameters. For example, the mode register may contain a burst length value, a burst type value, and a latency mode value. The burst length value determines the length of the data bursts that the DRAM will perform. The burst type value determines the ordering of the data sent in the bursts. Typical burst orders include sequential and subblock ordered. The latency mode value determines the number of clock cycles between a column address and the data appearing on the data bus. The appropriate value for this time interval depends largely on the operating frequency of the SDRAM. Since the SDRAM cannot detect the operating frequency, the latency mode value is programmable by a user.

Request Oriented DRAM Systems

The prior art also includes memory systems in which data transfer operations are performed by DRAMs in response to transfer requests issued to the DRAMs by a controller. Referring to FIG. 4, it illustrates a memory system in which data transfers are made in response to transfer requests. The request packet format is designed for use on a high speed multiplexed bus for communicating between master devices, such as processors, and slave devices, such as memories. The bus carries substantially all address, data, and control information needed by the master devices for communication with the slave devices coupled to the bus. The bus architecture includes the following signal transmission lines: BusCtl, BusData [8:0], BusEnable, as well as clock signal lines and power and ground lines. These lines are connected in parallel to each device.

The processors communicate with the DRAMs to read and write data to the memory. The processors form request packets which are communicated to the DRAMs by transmitting the bits on predetermined transmission lines at a predetermined time sequence (i.e. at predetermined clock cycles). The bus interface of the DRAM receiver processes the information received to determine the type of memory request and the number of bytes of the operation. The

DRAMs then perform the memory operation indicated by the request packet.

FIG. **5** illustrates command control information **500** that is sent in a data transfer request according to a prior art protocol. In the illustrated example, the command control information **500** is sent over a BusCtl line and a nine-bit data bus (BusData[**8:0**]) in six clock cycles. The command control information **500** includes groups of bits **501, 502, 504, 506** and **508** that constitute an address, an operation code consisting of six bits **510, 512, 514, 516, 518** and **520**, and groups of bits **522, 524** and **528** that specify a count. The address identified in the command control information **500** specifies the target DRAM and the beginning location within the DRAM of the data on which the operation is to be performed. The count identified in the command control information **500** specifies the amount of information on which the operation is to be performed.

SUMMARY AND OBJECTS OF THE INVENTION

One object of the present invention is to provide a mechanism to decouple control timing from data timing.

Another object of the present invention is to provide mechanisms that use minimal bandwidth to determine data timing while minimizing the latency from signaling that the data transfer should terminate to the transmission of the final data packet.

Another object of the present invention is to provide mechanisms for arbitrarily long data transfers following a command. This may include simultaneous provision of a new column address for each data packet transferred.

Another object of the present invention is to provide a means to signal simultaneously with termination of the data transfer that a precharge operation should be performed.

Another object of the present invention is to provide mechanisms and methods for interleaving control and data information in such a fashion that pin utilization is maximized without placing latency requirements upon the DRAM core that are difficult or expensive to satisfy.

Another object of the present invention is to provide a mechanism for interleaving control and data information that minimizes bandwidth consumed for signaling the beginning and ending of data transfers.

Another object of the present invention is to provide for devices that do not always interpret the information presented at their pins. Each command provides sufficient information that all further control information related to the command can be easily determined even in the presence of control information related to previous command transfers.

Another object of the present invention is to provide a mechanism for optionally sequencing a series of core operations prior to data transmission and, optionally, a final core operation after data transmission is terminated.

Another object of the present invention is to provide a DRAM core which allows a single high current RAS operation at any one time in order to minimize the cost and complexity of the DRAM.

Another object of the present invention is to provide an encoding of the command such that decoding space and time is minimized and functionality is maximized.

The present invention provides a method and apparatus for performing data transfers within a computer system. The method includes causing a controller to transmit control information on a bus. The control information specifies a data transfer operation and a beginning location of data to be transferred. The controller determines, after transmitting the control information on the bus, a desired amount of data to be transferred in the data transfer operation. The controller transmits over the bus a terminate indication at a time that is based on the desired amount of data and a beginning time of the data transfer operation. A memory device reads the control information on the bus. The memory device performs the specified data transfer operation on data stored at the beginning location. The memory device continues to perform the specified data transfer operation until detecting the terminate indication on the bus. The memory device ceases to perform the data transfer operation at a time that is based on the time at which the terminate indication is detected.

Other objects, features, and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description that follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

FIG. **1A** is a block diagram of prior art dynamic random access memory (DRAM) component;

FIG. **1B** illustrates a storage cell of the DRAM shown in FIG. **1A**;

FIG. **2** is a block diagram illustrating a DRAM system and input/output pins and signal lines for accessing the DRAM;

FIG. **3A** is a timing diagram illustrating synchronous write timing;

FIG. **3B** is a prior art timing diagram illustrating synchronous read timing;

FIG. **4** is a prior art memory system in which a memory controller issues request packets to DRAM over a channel;

FIG. **5** illustrates command control information that is sent from a controller to a DRAM according to a prior art protocol;

FIG. **6** is a block diagram of a computing system that includes the present invention;

FIG. **7** is a block diagram the illustrates the control and decode circuitry of a DRAM according to one embodiment of the invention;

FIG. **8** is a flow chart illustrating the protocol employed by a controller to initiate data transfers according to an embodiment of the present invention;

FIG. **9** illustrates a request packet according to one embodiment of the present invention;

FIG. **10** is a timing diagram illustrating interleaved read/write transaction timing when the read latency equals the write latency according to a prior art protocol;

FIG. **11** is a timing diagram which illustrates synchronous interleaved read timing with multiplexed data/row/control information according to an alternative prior art protocol;

FIG. **12** illustrates the timing of five transactions performed in a non-interleaved embodiment of the present invention;

FIG. **13** illustrates the timing of five transactions performed in an interleaved embodiment of the present invention;

FIG. **14** illustrates circuitry for decoding operation codes according to the prior art;

FIG. **15** illustrates circuitry for decoding operation codes according to one embodiment of the present invention;

FIG. 16A illustrates an operation code encoding scheme according to an embodiment of the invention;

FIG. 16B is a continuation of the table illustrated in FIG. 16A;

FIG. 17 illustrates a prior art circuit for determining whether a particular DRAM should respond to an operation request; and

FIG. 18 illustrates a circuit for determining whether a particular DRAM should respond to an operation request according to an embodiment of the present invention;

FIG. 19 illustrates a mapping between Open and Close bits and the operations that are performed by a DRAM in response to the bits according to an embodiment of the invention;

FIG. 20A is a block diagram illustrating a DRAM configured to allow no more than one high current operation to be performed over each internal power supply line according to an embodiment of the invention; and

FIG. 20B is a block diagram illustrating a DRAM configured to allow no more than one high current operation to be performed within the DRAM at any given time according to an embodiment of the invention.

DETAILED DESCRIPTION

FIG. 6 is a block diagram of a computing system that includes the present invention. The data transport system includes a central processing unit 600, a memory controller 601 and a DRAM 603. The memory controller 601 connects the CPU 600 to a channel 622 to which DRAM 603 is connected. For the purposes of explanation, a single DRAM is shown on channel 622. However, the present invention is not limited to any particular number of DRAMs on the channel 622.

The CPU 600 may be, for example, a microprocessor. When the CPU 600 executes instructions that require a data transfer operation, the CPU 600 transmits control signals specifying the desired transfer operations to memory controller 601. Memory controller 601 may be, for example, an application specific integrated circuit (ASIC) memory controller configured to transmit request packets to DRAM 603 over channel 622 to specify the desired transfer operation.

According to one embodiment, channel 622 includes a line 624 for initializing daisy chain input, a "clock to end" line 650, a "clock from master" line 628; a "clock to master" line 630, and a plurality of lines 626 that includes a BusEnable line, a BusCtl line and a nine-bit data bus (BusData[8:0]). The "clock to end" line 650 carries a clock signal from memory controller 601 to the end of line 630. The "clock to master" line 630 routes the clock signal to the various devices on channel 622 and back to memory controller 601. The "clock from master" line 628 routes the clock signal from the "clock to master" line 630 back to the various devices on channel 622. The clock signal on the "clock from master" line 628 is aligned with request and write data packets transmitted by controller 601. The clock signal on the "clock to master" line 630 is aligned with read data packets transmitted by DRAM 603. The information communicated over lines 626 includes request packets, data transfer control signals, and data packets.

DRAM 603 is divided into three sections: an storage section 632, a control section 634, and a I/O section 636. The storage section 632 includes a DRAM core consisting of two independent memory banks 602 and 606. It should be noted that a two-bank DRAM shall be described simply for the purposes of explanation. The present invention is not limited to DRAMs with any particular number of memory banks.

Each of the memory banks 602 and 606 has a latching sense amplifier cache 604 and 608. The caches 604 and 608 hold the currently sensed row of their respective memory banks. The control section 634 includes control logic 610 and control registers 614. Control logic 610 performs initialization operations in response to control signals on line 624. Control registers 614 are read and written to using special register space commands. The contents of the control registers 614 determine how DRAM 603 operates. For example, the control registers 614 may store values that determine the output drive current used by DRAM 603, the base address of DRAM 603 and the configuration and size of DRAM 603.

The I/O section 636 includes a clock generator 618, a receiver 620, and a transmitter 616. The clock generator 618 uses the external-clock signals to create clock signals used internally by DRAM 603. The receiver 620 and transmitter 616 contain multiplexing and storage hardware to permit internal data paths to operate at a slower clock rate, but equivalent bandwidth, to lines 626.

FIG. 7 is a block diagram of a DRAM in which the present invention may be implemented according to one embodiment of the invention. Referring to FIG. 7, a DRAM 700 generally includes I/O and control circuitry 722, four banks of memory, a plurality of column decoders 718 and 720, and a plurality of row decoders 704, 706, 712 and 714. Each of the four banks are split into two memory blocks. Specifically, BANK0 is distributed over blocks 702A and 702B, BANK1 is distributed over blocks 708A and 708B, BANK2 is distributed over blocks 710A and 710B and BANK3 is distributed over blocks 716A and 716B.

I/O and control circuitry 722 receives request packets from a controller over a channel 724. The request packets include an address that corresponds to a storage location and an operation code that specifies the operation to be performed on the data stored in the specified storage location. To perform a read operation, I/O and control circuitry 722 transmits control signals to the row decoders 704, 706, 712 and 714 to cause the row that contains the specified data to be moved into a cache. Then the I/O and control circuitry 722 transmits control signals to the column decoders 718 and 720 to cause the data from a column of the row in the row cache to be transmitted out onto the channel 724. The column that is transmitted is the column that corresponds to the address contained in the request packet.

Controller Operation

Referring to FIG. 8, it is a flow chart that illustrates the protocol employed by a controller to initiate data transfers according to one embodiment of the invention. At step 802, the controller transmits a wakeup signal to the DRAM that will be involved in the data transfer operation (the "target DRAM"). At step 804, the controller transmits command control information to the target DRAM. The contents of the command control information according to one embodiment of the invention are illustrated in FIG. 9.

Referring to FIG. 9, the command control information is transmitted over the BusCtl line and BusData[8:0] lines over three clock cycles, where each clock cycle has even and odd phases. A start bit 902 is sent over the BusCtl line on the even phase of the first clock cycle. As shall be described in greater detail below, the start bit serves as a flag which allows the DRAM to identify the signals as command control information.

The command control information includes an address 904 that identifies the beginning memory location in the

target DRAM that will be involved in the specified data transfer operation. The command control information further includes an operation code, open and close bits, and a Pend value.

As shall be explained below, certain bits in the operation code directly correspond to control lines within the target DRAM. Specifically, the operation code includes a Write bit **906**, a Reg bit **908** and a NoByteM bit **910** that correspond to control lines in the target DRAM. Upon receipt of the command control information, the DRAM simply places the value stored in these bits on the respective control line. The operation code also contains a broadcast bit **912** to indicate whether the specified operation is a broadcast operation.

The Open, Close and Pend values serve functions described in greater detail below. In general, the Open and Close bits specify whether precharge and/or sense operations are to be performed before and/or after the operation specified in the operation code. The Pend value indicates how many odd phase bits will appear on the BusCtl line after the command control information and before the strobe signal that corresponds to the operation specified in the command control information (other than any odd phase bits in request packets for other transactions). The command control information also contains other values "EvalCC" and "Mask" that do not relate to the present invention.

Referring again to FIG. **8**, control passes from step **804** to step **806**. During step **806**, the controller transmits the strobe signal over the BusCtl line (step **810**). If the transaction involves more than one data packet, then the column address for data packets that are to be sent subsequent to the first data packet are transmitted serially over the BusEnable line (step **808**). Steps **808** and **810** are combined in step **806** to indicate that step **810** is performed concurrently with step **808**. In one embodiment, the transmission of the address for subsequent data packets begins at a sufficient interval prior to the time at which those data packets are to be sent to allow the second and subsequent data packets to be sent after the first data packet without interruption.

At step **814**, the data is transmitted over the data bus (BusData[**8:0**]). During this step, the data may be transmitted to or from the target DRAM, depending on whether the data transfer operation is write or read operation. At some fixed period of time prior to the transmission of the last data packet, the controller transmits the terminate signal on the BusCtl line,(step **816**). Steps **816** and **814** are shown as a single step **812** to indicate that step **816** is performed during the performance of step **814**.

As shall be explained below, one embodiment of the memory controller dynamically adjusts the interleave of data and control information to more fully utilize the channel. Interleave refers to the relative ordering of data, requests and control signals that are associated multiple transactions. To allow dynamic interleave adjustment, there is no fixed time period between the execution of steps **804** and **806**. Rather, the controller is free to adjust the timing of step **806** relative to the timing of step **804** as needed to provide the desired interleave (e.g., to provide time to transmit the command control information for other transactions between execution of steps **804** and **806**).

In one embodiment, the controller is configured to limit the number of requests that are targeted to any given DRAM. For example, if two data transfer operations have been requested for a given DRAM, the controller will refrain from issuing a third request until one of the outstanding requests has been serviced. By limiting the number of requests any DRAM must handle at any given time, the size of the command queue within the DRAM may be reduced, decreasing the complexity of the DRAM.

In one embodiment, the number of outstanding requests on the channel may be larger than the number of rests being processed by any single DRAM. Preferably, the number of outstanding requests is limited only by the size of the field which indicates the number of outstanding requests, and the aggregate number of requests which can be handled by all of the DRAMs on the channel.

Deferred Transfer Size Determination

In typical EDO and SDRAM components, only a finite number of data transfer sizes are supported. For each data transfer size, there is a fixed ratio between the amount of control information that must be sent to a DRAM and the amount of data to be transferred in the operation. Thus, the larger the amount of data to be transferred, the larger the amount of control information that must be sent to the DRAM. For example, with an SDRAM that only supports transfers of one or four data words, two four-word transfers must be performed to transfer eight data words. Thus, all of the control information that a controller must send to the DRAM for a four data word transfer, including an operation code and an address, must be sent twice.

In prior art request-oriented systems, a data transfer count is part of the command control information that a controller sends to a DRAM to initiate a data transfer operation. The amount of bits allocated in the control information for sending the data transfer count is fixed. Consequently, the size of data transfers that a system may perform in response to a single transfer request is limited to the number of data packets that can be specified in the available number of bits. The size limit thus placed on data transfers makes it necessary for transfers of large amounts of data to be performed using numerous requests for smaller data transfer operations. For example, if the data transfer count is only five bits long and data packets are eight bytes, then the maximum size of a data transfer is 256 bytes (32 data packets). For transfers larger than 256 bytes, more than one request packet must be used.

In one prior art request-oriented system, the controller is allowed to prematurely terminate a data transfer operation by transmitting a terminate control signal to the DRAM. Upon receipt of the terminate control signal during a particular data transfer operation, the DRAM ceases to process data for the operation, even if the amount of data that has been transferred is less than the amount of data that was specified in the data transfer count of the operation. This technique allows the controller to shorten data transfers after a particular transfer size has been specified, but does not overcome the limitations associated with having a maximum size limit per requested transaction.

According to one aspect of the present invention, the command control information within a request packet no longer contains size information. Rather, the DRAM is configured to start and end the transmission of data based on data transfer control information sent by the controller to the DRAM separate from and subsequent to the transmission of the command control information. According to one embodiment, the data transfer control information includes data transfer start information (a "strobe signal") sent from the controller to indicate when the DRAM is to begin sending data, and data transfer end information (a "terminate signal") to indicate when the DRAM is to stop sending data. The number of clock cycles that elapse between the transmission of the strobe signal and the terminate signal indicates the size of the data transfer.

If a data transfer operation involves more than one data packet, then the controller serially transmits column address information on the BusEnable line to specify the columns that contain the data to be sent in the second and subsequent data packets. Preferably, the controller begins to transmit the column address information at a time that allows the DRAM to have sufficient time to reconstruct the column addresses and prefetch the data from the specified columns in the DRAM core before the data packets that correspond to the column addresses are to be transmitted over the channel. Because the DRAM continuously receives column addresses over the BusEnable line during multi-packet transfers, the DRAM itself does not have to maintain a counter to determine from where to retrieve data for the next data packet.

By transmitting data transfer control information separate from the command control information, it is possible to specify a transfer operation for any amount of data. Thus, large transfers do not have to be broken up into multiple requests for smaller amounts of data. In one embodiment, the control circuitry within the DRAM is configured to begin retrieving requested data from the DRAM core as soon as possible after receipt of a request packet. The DRAM does not wait for the strobe signal to begin retrieving the data from the DRAM core. However, the DRAM does not transmit any data on the channel until the strobe signal is received. Because the initial data packet to be transmitted by the DRAM has been prefetched from the core, the data packet can be transmitted over the channel with minimal delay from when the strobe signal ultimately arrives.

There are numerous benefits to reducing the delay between the transmission of (1) a strobe signal for a transfer operation and (2) the first packet in the transfer operation. For example, the minimum latency between a transfer request and the beginning of the transfer can never be less than the strobe-to-data delay. Therefore, the strobe-to-data delay may determine the critical path for DRAMs that support fast core operations. In addition, the longer the strobe-to-data delay, the more complex the controller must be to accurately and efficiently pipeline the command control information and strobe signals.

The bandwidth required to indicate the start and end of a data transfer operation with single bit strobe and terminate signals is minimal. In one embodiment, a single line (the BusCtl line) is used to carry a variety of control signals, including the strobe and terminate signals. Further, the channel utilization employed to start and terminate a transfer operation does not vary with the size of the data to be transferred.

Due to intrinsic circuit delays, the DRAM does not instantly terminate data transmission upon the receipt of the terminate signal. Rather, the terminate signal causes the DRAM to initiate termination of the data transfer. Transmission of the last data packet in a transfer actually occurs on some clock cycle after the receipt of the terminate signal. When a terminate signal is used to specify the end of a transfer operation, it is important to minimize the latency between the transmission of the terminate signal for the transaction and the transmission of the last data packet of the transaction. By reducing the latency between the terminate signal for a transaction and the time at which the channel ceases to be used to send data for the transaction, the amount of time required for the controller to use the channel for another transaction is reduced. This is particularly important when there are multiple requesters that are contending for use of the same channel.

According to one embodiment, the terminate signal may be used to either end a transaction or suspend a transaction. The exact timing of the terminate signal may be used to indicate whether a transfer operation should be terminated or merely suspended. For example, if the terminate signal is sent at one modulus relative to the strobe signal, the DRAM is configured to terminate the data transfer operation. A modulus is the remainder obtained after dividing one integer by another integer. If the terminate signal is sent at a different modulus relative to the strobe signal, the DRAM is configured to suspend the transfer operation. The DRAM may be configured to continue transfer operations that have been suspended upon receipt of a continue control signal.

Decoupled Data Transfer Control Information

In prior art systems, the timing of a data transfer is dictated by the timing of the request for the data transfer. Thus, given that a transfer request arrived on a particular clock cycle, it was known that the data specified in the request would begin to appear on BusData[8:0] a predetermined number of clock cycles from the particular clock cycle. For example, the number of clock cycles that elapse between a request packet and the transfer of data specified in the request packet may be determined by a value stored in a register within the DRAM. This fact renders prior art systems inflexible with respect to how control and data signals may be interleaved to maximize the use of the channel.

As mentioned above, the data transfer control information which controls the timing of the data transfer associated with a request packet is sent separately from the command control information to which it corresponds. According to another aspect of the invention, the timing of the data transfer control information is variable relative to the timing of the corresponding request packet. That is, the number of clock cycles between the transmission of a request packet and the transmission of the strobe signal to begin the transfer specified in the request packet may vary from transaction to transaction.

According to an alternate embodiment of the invention, the amount of time that elapses between the transmission of a request packet and the transmission of the data specified in a request packet is varied without the use of strobe and terminate signals. In this embodiment, the request packet contains a delay value that indicates to the DRAM when the data specified in the request packet will begin to be sent relative to the time at which the request packet is sent. The DRAM would include a counter to count the clock cycles that elapse from the arrival of the request packet in order to send or receive the data specified in the request on the appropriate clock cycle. Because the controller may vary the latency between request packet and data transmission, the controller is able to dynamically adjust the operative interleave on the channel, as shall be described in greater detail below.

Dynamic Interleave Adjustment

As mentioned above, the fixed timing between requests and data transmissions renders prior art systems inflexible with respect to how control and data signals may be interleaved. For example, FIGS. 10 and 11 illustrate the timing of transactions for particular prior art protocol systems.

Referring to FIG. 10, it illustrates interleaved timing of read and write accesses. The interleave structure permits read accesses to a DRAM to be interleaved with write accesses to another DRAM. FIG. 11 illustrates synchronous interleaved read timing with multiplexed data/row/control information according to an alternative prior art protocol.

Both of these prior art interleave patterns increase utilization of the channel and the internal resources of the DRAM relative to non-interleaved protocols. However, the timing between requests and data transfers is fixed, so the interleave patterns are fixed. Consequently, controllers cannot make interleave adjustments to maximize usage of the channel and DRAM resources in response to changing conditions in the system.

The ability to vary the timing between the transmission of a request packet and the transmission of the data specified in the command control information makes it possible to interleave the information on BusData[**8**:**0**] in variations that were not previously possible. According to one embodiment of the invention, controllers dynamically adjust the interleave to maximize the use of the channel in the face of internal DRAM latencies that are long with respect to the transmission of control information or data.

Referring to Appendix A and FIG. **12**, they illustrate the timing of five non-interleaved data transfer operations. At clock cycle **0**, a wakeup signal associated with transaction **0** is transmitted from the controller to the DRAM on the BusCtl line "BC". At clock cycles **4** through **6** the command control information for transaction **0** is sent from the controller to the DRAM over the BusCtl line and nine bus data lines "BD8:0". At clock cycle **10** the DRAM begins sensing the row specified in the command control information of the bank specified in the command control information. At clock cycle **17** the controller sends the strobe signal associated with transaction **0** to the DRAM. At clock cycle **23** the DRAM begins transferring data beginning at the address specified in the command control information. At clock cycle **30** the controller sends a terminate signal associated with transaction **0** to the DRAM. At clock cycle **38**, the DRAM sends the last data associated with transaction **0**.

The wakeup signal for transaction **1** is transmitted at clock cycle **35**. At clock cycles **39** through **41** the command control information for transaction **1** is transmitted. The timing for transactions **1** through **4** proceeds as illustrated. This example clearly illustrates that there is mining timing overlap between transactions when signals for different transactions are not interleaved. Consequently, bandwidth that may be used to begin subsequent transactions goes unused.

Referring to Appendix B and FIG. **13**, they illustrate the timing of interleaved data transfer operations. In the illustrated example, the wakeup signal for transaction **1** is transmitted at clock cycle **20**, even before data has started to be sent for transaction **0**. By the time the terminate signal has been sent for transaction **0**, the wakeup signal and command control information have been sent to the DRAM for transaction **1**. The transmission of this information during the execution of transaction **0** does not result in any performance penalty because the bandwidth used to transfer the information was otherwise unused. Significantly, five transactions are completed by clock cycle **131** using the interleaved example shown in Appendix B, while completion of five transactions requires 172 clock cycles in the non-interleaved system shown in Appendix A.

The ability to dynamically adjust the interleave of control and data information allows controllers to increase the utilization of the channel. In addition, the controller can adapt the interleave to the changing demands being placed on the bus to minimize latency. For example, the controller can transition from a cold start, where the bus is idle, to an active state by issuing a series of requests back-to-back and then waiting for the data that will be sent in response to the requests. After start, the controller adjusts the interleave to shift from minimizing latency to maximizing utilization of the channel and internal resources of the DRAM. Therefore, after a steady state has been achieved, the controller avoids having too many back-to-back requests. Rather, the controller switches to a smoother interleave pattern, such as the pattern illustrated in Appendix B. An exemplary series of transactions that illustrate how a controller that employs the protocol of the present invention is able to dynamically change the interleave of transactions shall be discussed in greater detail below with reference to Appendix C.

Signal Overload

To help maximize utilization of the channel, the same control line may be used to carry numerous control signals. For example, in the protocol illustrated in Appendixes A and B, the BusCtl line is used to carry wakeup signals, strobe signals, portions of the command control information, and terminate signals. According to one embodiment of the invention, clock cycles are divided into even and odd phases. The command control information is preceded by a non-zero value "start bit" on the BusCtl line at an even phase of the clock cycle. Upon detection of a start bit, a DRAM knows that any signals on the BusCtl line during the three subsequent odd phases of the clock cycle are part of the command control information, and not strobe, wakeup or terminate signals. The strobe signals, wakeup signals and terminate signals are all indicated by non-zero values on the BusCtl line at an odd phase of the clock cycle. Consequently, the DRAM must have some mechanism for distinguishing between the signals.

In an embodiment of the invention that uses fixed interleaves, an operation begins at a fixed interval relative to the command control information that specifies the operation. Therefore, DRAMs simply use the arrival time of the command control information and the known interval to determine when to perform the operation. The terminate signal associated with a transaction is always the next odd-phased signal on the BusCtl line after its corresponding command control information. Therefore, if the command control information can be identified, the terminate signal can also be identified. Any signal on the BusCtl line during an odd phase of a clock cycle is a wakeup signal.

The method described above for distinguishing between identical control signals (i.e. control signals that use the same line and have the same characteristics) works well in an embodiment that employs fixed interleaves. However, where the timing interval between a request packet and its corresponding strobe signal is variable, a mechanism must be provided to indicate to the DRAMs when to look for the strobe signal that corresponds to a request packet that has been received.

In the example illustrated in Appendix B, the period between the transmission of the command control information for a transaction and the strobe signal for the transaction is not fixed. Consequently, the DRAM must have some other mechanism for determining that, of all the signals that arrive on the BusCtl line, the signal at clock cycle **47** is the strobe signal associated with the command control information for transaction 1.

According to one embodiment of the present invention, the DRAM is able to distinguish between identical signals on the BusCtl line based on knowledge of what information has previously appeared on the channel. To obtain information about data on the channel, the DRAM constantly monitors the channel. Because the DRAM constantly moni-

tors the channel, the controller does not have to transmit wakeup signals to the DRAM. Therefore, the only identical signals on the BusCtl line are the strobe signal and the terminate signal.

According to this embodiment, the order in which the controller sends strobe and terminate signals must match the order in which the controller sends request packets. For example, if the controller transmits request packets for transactions **0**, **1**, and **2**, in that order, then the controller must send strobe and terminate signals for transactions **0**, **1**, and **2**, in that order.

Under the constraints described above, the DRAM has the information it requires to correctly identify the strobe and terminate signals on the channel. Specifically, the first control signal on the BusCtl line will always be a strobe signal associated with the first transaction. The control signal that follows any strobe signal is always the terminate signal for the transaction that corresponds to the preceding strobe signal. The control signal that follows any terminate signal will always be a strobe signal for the transaction that immediately follows the transaction associated with the previous strobe signal.

While the approach described above allows a DRAM to accurately identify strobe and terminate signals, it has two obvious disadvantages. First, it requires that all DRAMs monitor the channel at all times. If any DRAM fails to monitor the line for any period, the DRAM will not be able to accurately identify the identical control signals. Because the DRAM has to constantly monitor the channel, the DRAM will not be able to conserve energy by entering a power-down mode. The expense associated with keeping all DRAMs powered up at all times is significant.

The second disadvantage is that the controller must send the control signals in exactly the same order as the command control information. As a result, the controller is limited with respect to the type of interleave patterns it may select. Specifically, the controller may not select any interleave patterns that retire a transaction out of order.

According to an alternate embodiment of the present invention, the controller is configured to transmit, as part of the command control information in a request packet, data which allows the DRAM to identify the strobe signal that corresponds to the command control information. For example, in one embodiment, the controller includes a "Pend" value in the command control information. The Pend value in a request packet indicates how many control signals that are identical to the strobe signal will occur between the end of the command control information for a transaction and the actual strobe signal for the transaction. Based on the Pend value, a DRAM is able to identify control signals without having to know what has transpired on the channel prior to the arrival of the command control information.

In the example illustrated in Appendix B, the command control information for transaction **1** is sent at clock cycle **24**, and the strobe signal for transaction **1** is sent at clock cycle **47**. Between the transmission of the command control information for transaction **1** and the transmission of the strobe signal for transaction **1**, a terminate signal for transaction **0**, a wakeup signal for transaction **2** and a request packet for transaction **2** are sent. (The DRAM knows to ignore the command control information for transaction **1** by detecting its start bit on an even phase of the clock cycle.).

The terminate signal for transaction **0** and the wakeup signal for transaction **2** both have identical characteristics to strobe signals. Therefore, the Pend value sent in the command control information for transaction **1** is two. By this Pend value, the DRAM is made aware that two strobe-like signals will appear on the BusCtl line prior to the actual strobe signal for transaction **1**. The DRAM monitors the channel after the receipt of the command control information for transaction **1**. Based on the Pend information in the command control information for transaction **1** and the signals that occur on the channel after receipt of the command control information for transaction **1**, the DRAM can identify the strobe for transaction **1**.

The Pend approach overcomes the disadvantages of the constant channel monitoring approach because the DRAM involved in a transaction does not need to know what transpired on the channel prior to the arrival of the command control information for the transaction. Consequently, a DRAM may assume a powered down mode until the arrival of a wakeup signal just prior to the transmission of a request packet. In addition, the Pend approach does not require transactions to be retired in the same order as the order in which they are requested. Therefore, a controller may specify interleave patterns in which some transactions are retired out of order.

Deferred Precharge Notification

At the time that a request packet is transmitted by a controller, the controller may not have enough information to determine whether a precharge operation should be performed after the completion of the transaction. Therefore, according to one embodiment of the invention, the command control information sent in request packets does not contain an indication of whether or not a precharge is to be performed after the transaction. Rather, the controller communicates to the DRAM whether a precharge is to be performed when the terminate signal that initiates the termination of a transfer operation is sent to the DRAM. Because the transmission of the terminate signal is deferred, the determination of whether or not a precharge operation is appropriate may be made by the controller based on information obtained between the transmission of the request packet and the transmission of the terminate signal.

For example, at the time that the request packet is sent, additional requests for data from different rows in the same DRAM may not have arrived. Therefore, it would appear that no post-operation precharge is required. However, prior to the transmission of the terminate signal, a request may arrive for an operation to be performed on a different row of the same bank within a DRAM. When the controller sends the terminate signal for the current operation, the controller can communicate to the DRAM that a precharge operation is to be performed. The DRAM can therefore begin a precharge operation for the bank containing the appropriate row while the current data transfer operation is being completed.

The technique used by the controller to communicate whether a precharge is to be performed after an operation preferably takes advantage of the fact that data is typically transferred as a series of one or more fixed-sized packets, where each packet contains more data than can be transmitted during a single clock cycle. Because the transmission of a single packet is performed over multiple clock cycles, the terminate signal may be sent during any one of a plurality of clock cycles to specify that a particular packet is the last packet. For example, assume that it takes four clock cycles to send a single packet of data, and that the DRAM is configured to send exactly one data packet after receipt of the terminate signal. As long as the terminate signal is sent at any one of the four clock cycles during which the

penultimate data packet is sent, the data transmission will terminate at the appropriate time.

According to one embodiment of the invention, the controller uses the exact timing of the terminate signal to indicate to the DRAM whether the DRAM is to perform a precharge operation. For example, assume that the controller can terminate a transfer at the appropriate time by sending the terminate signal during any one of four clock cycles, as described above. The controller can indicate to the DRAM that precharge is to be performed by transmitting the terminate signal in the first of the four possible clock cycles, and indicate that precharge is not to be performed by transmitting the terminate signal on the second of the four possible clock cycles. The DRAM decodes the precharge information by determining on which of the four possible clock cycles the terminate signal appeared. The DRAM may make this determination, for example, by determining the modulus of the clock cycle on which the terminate signal was received relative to the clock cycle on which the corresponding strobe was received.

According to an alternate embodiment, a particular precharge operation is associated with each of the four available clock cycles. For example, the DRAM may contain four banks of memory. The technique described above may be extended so that a terminate signal in the first possible clock cycle causes the DRAM to precharge the first memory bank, a terminate signal in the second possible clock cycle causes the DRAM to precharge the second memory bank, a terminate signal in the third possible clock cycle causes the DRAM to precharge the third memory bank, and a terminate signal in the fourth possible clock cycle causes the DRAM to precharge the fourth memory bank. Significantly, this embodiment allows the position of the terminate signal for an operation on one memory bank to indicate that a precharge operation is to be performed on a different memory bank. In this embodiment, the command control information may contain a bit for specifying that no precharge is to be performed, regardless of the timing of the terminate signal.

Optimized Operation Encoding

Typically, a controller indicates to a DRAM the operation it desires the DRAM to perform by transmitting to the DRAM a request packet that includes an operation code that corresponds to the desired operation. To determine how to respond to a request packet, each of the bits of the operation code must be wired from its point of reception on the DRAM and to a decoder prior to being globally transmitted through the interface in order to control functionality. The wiring and decoding process consumes space and power. A typical circuit for performing operation code decoding is illustrated in FIG. 14.

Referring to FIG. 14, a decoding circuit 1400 includes a plurality of pins 1402, a plurality of global control lines 1404, and a plurality of decode units 1406. Each decode unit 1406 corresponds to a particular global control line 1404. When a multiple-bit operation code is received at pins 1402, the entire operation code is routed to each of decode units 1406. Each of decode units 1406 decodes the operation code to determine the appropriate signal to apply to the control line 1404 to which it. corresponds.

Referring to FIG. 15, it illustrates a decode circuit 1500 according to an embodiment of the invention. Similar to decode circuit 1400, decode circuit 1500 includes a plurality of pins 1502, 1504 and 1506, a plurality of decode units 1508, 1510 and 1512, and a plurality of global control lines 1516, 1518 and 1520. Each of decode units 1508, 1510 and 1512 corresponds to one of the control lines 1516, 1518 and 1520. Unlike the prior art decode circuit 1400, each of decode units 1508, 1510 and 1512 receives only the signal from one pin. Based on the signal from the pin and state information stored in the decode unit, the decode unit applies the appropriate signal to the control line to which it corresponds.

The advantages of decode circuit 1500 over the prior art circuit shown in FIG. 14 include decreased wiring requirements, decreased power consumption and decreased circuit complexity. Specifically, only one line per pin is required to route the signals from pins 1502, 1504 and 1506 to decode units 1508, 1510 and 1512, respectively. Further, the complexity of decoders 1508, 1510 and 1512 is significantly reduced.

For decode circuit 1500 to work correctly, the operation codes transmitted by the controller must include bits that directly correspond to the signals carried on lines 1516, 1518 and 1520. Typically, the global control lines include a NoByteM line, a Reg line, and a Write line. The NoByteM line indicates whether a byte mask should be used on the data specified in the operation. The Reg line indicates whether the operation relates to a register or to memory. The Write line indicates whether the operation is a read operation or a write operation.

FIGS. 16A and 16B illustrates an operation code encoding scheme according to an embodiment of the invention. Referring to FIGS. 16A and 16B, they illustrate an operation-to-operation-code mapping in which bits in the operation code directly dictate the signals to be placed on each of the global control lines to perform the corresponding operation. Specifically, each operation code has a bit "OP[2]" that specifies whether a signal should be placed on the NoByteM control line, a bit "OP[1]" that specifies whether a signal should be placed on the Reg control line, and a bit "OP[0]" that specifies whether a signal should be placed on the Write control line. The operation code that corresponds to each possible type of operation has the various operation code bits set so as to cause the appropriate signals to be generated on the global control lines. For example, to perform a register read directed operation, a signal must be generated on the NoByteM and Reg control lines, but not on the Write control line. Therefore, in the operation code that corresponds to the register read directed operation, the bits that correspond to the NoByteM, Reg and Write control lines are respectively "1", "1" and "0".

Broadcast Operations

DRAMs respond to request packets if the operations specified in the request packets are specifically directed to the DRAM, or if the request packets specify broadcast operations. FIG. 17 illustrates a prior art circuit for determining whether a particular DRAM should respond to an operation request.

Referring to FIG. 17, a comparator 1702 compares the address bits in an request packet with the device ID of the DRAM. If the address bits in the request packet do not match the device ID, then a logical LOW is transmitted to one input of AND gate 1706. Consequently, the output of AND gate 1706 will be LOW. The operation code contained in the request is decoded by decode unit 1704. Decode unit 1704 decodes the operation code in the request packet and transmits signals over lines 1708 and 1710 based on the operation specified by the operation code. If the operation code represents a broadcast operation, then the decode unit 1704 applies a logical HIGH to line 1710. If the operation code

represents a non-broadcast operation, then the decode unit **1704** transmits a signal on line **1708** indicative of the command, and a logical LOW on line **1710**. Line **1710** and the output of AND gate **1706** are applied to an OR gate **1712**. The signal at output of OR gate **1712** determines whether the DRAM should process the specified operation. When the specified operation is a broadcast operation, the output of OR gate **1712** will be HIGH regardless of the output of AND gate **1706**.

Referring to FIG. **18**, it illustrates a circuit for determining whether a DRAM should respond to request packet, according to an embodiment of the present invention. Similar to the circuit shown in FIG. **17**, circuit **1800** includes a comparator **1802** for comparing the address bits in a request packet wit the device ID of the DRAM. However, circuit **1800** is configured for a protocol in which one bit in the operation code of a request indicates whether the request is for a broadcast operation. Referring again to FIGS. **16**A and **16**B, the operation codes employed in one embodiment include a bit "Op[3]" that indicates whether the operation specified by the operation code is a broadcast operation.

Because the operation code contains a bit which indicates whether the operation is a broadcast operation, it is not necessary to decode the operation code to determine whether the operation is a broadcast operation. Rather, the value of the broadcast bit is fed directly into one input of an OR gate **1804**. The other input of the OR gate **1804** receives a signal that indicates whether the address in the request matched the device ID of the DRAM. The output of the OR gate **1804** indicates whether the DRAM should respond to the request.

Because the operation code for every type of operation contains a bit that specifies whether the operation is a broadcast operation, the need to decode the operation codes to identify broadcast operations is avoided. Consequently, circuit **1800** is clearly simpler and more efficient that the circuit shown in FIG. **17**.

Controller-Specified State Changes

In typical DRAMs, data is not directly transmitted from the storage cells. Rather, data is temporarily copied to sense amplifiers prior to transmission. Typically, the sense amplifiers only store one row of data. If an operation is to be performed on a row of data other than the currently stored row, two operations must be performed. The first operation is referred to as a precharge operation, where pairs of bit lines within the memory are equalized to a midpoint voltage level. The second operation is referred to as a sense operation, where the row on which the operation is to be performed is copied onto the sense amplifiers. Between the precharge operation and the subsequent sense operation, the DRAM in question is said to be in a closed state. At all other times, the DRAM is said to be in an open state.

In the prior art, DRAMs are configured to determine whether precharge and sense operations have to be performed prior to servicing a data transfer request from a controller. Typically, the DRAM performs this determination by comparing the address contained in the request packet to the current address in the bank. If the addresses match, then the data is transmitted from the sense amplifiers and no precharge or sense operations are required. If the addresses do not match, then the DRAM performs a precharge and sense operation to load the sense amplifiers with data from the appropriate row, but does not service the data transfer request.

The overhead and complexity required for the DRAM to perform the address comparison results in a significant cost and performance penalty. Consequently, the present invention provides a controller that determines whether precharge and/or sense operations are required prior to making data transfer requests. Because the controller makes the determination, the complexity of the DRAM is reduced while the performance of the overall data transfer system is improved. The controller makes the determination of whether precharge and/or sense operations are required based on the address of the data in the operation, the current state of the bank that corresponds to the address and the address of the data that is currently stored in the bank. Typically, this information is already maintained by the controller for other purposes. Therefore, little additional overhead is required for the controller to make the determination.

Once the controller has made the determination for a particular data transfer operation, the controller must communicate the decision to the DRAM. Preferably, the controller communicates the determination to the DRAM through data sent with the command control information for the transaction. According to one embodiment of the invention, the command control information includes two bits ("Open" and "Close") that indicate to the DRAM what action to take with respect to the sensing and precharging the memory cells that correspond to the operation. Based on the current bank state and the value of the Open and Close bits, the DRAM determines what action to perform.

In general, the Close bit indicates whether to precharge the memory bank after performing the operation specified in the command control information, and the Open bit indicates whether some type of sense or precharge/sense operation must be performed before the operation. The actions performed in response to the Open and Close bits depends on the previous state of the bank in question. FIG. **19** illustrates how the combinations of values for the Open bit, Close bit, and previous bank state are mapped to actions to be performed according to one embodiment of the invention.

Referring to FIG. **19**, if the current bank state is closed and the Open and Close bits are "0" and "1", respectively, then the DRAM performs no action in response to the data transfer request. Since no action is performed, the state of the bank remains closed. If the current bank state is closed and the Open and Close bits are "1" and "0", respectively, then the DRAM senses the bank and then performs the operation specified in the command control information. After the operation is performed, the bank will be in the open state. If the current bank state is closed and the Open and Close bits are both "1", then the DRAM senses the bank, performs the specified operation, and precharges the bank. After these actions have been performed, the bank will be in the closed state. If the current bank state is closed, then both Open and Close bits cannot be "0".

If the current bank state is open and the Open and Close bits are both "0", then the DRAM simply performs the operation specified in the command control information. After the operation, the bank will still be in the open state. If the current bank state is open and the Open and Close bits are "0" and "1", respectively, then the DRAM performs the command and then precharges the memory bank. After the bank is precharged, it will be in the Closed state. If the current bank state is open and the Open and Close bits are "1" and "0", respectively, then the DRAM precharges the bank, senses the bank, and performs the specified operation. After the operation is performed, the bank will be in the open state. If the current bank state is open and the Open and Close bits are both "1", then the DRAM precharges the bank, senses the bank, performs the specified operation, then

precharges the bank. After these actions have been performed, the bank will be in the closed state.

In addition to giving the controller significantly more control over internal DRAM operation, the present invention establishes a one-to-many correspondence between request packets and specified operations. Specifically, a single request packet can cause a DRAM to perform (1) a plurality of DRAM core operations, (2) a DRAM core operation and a data transfer operation, or (3) a data transfer operation and a plurality of DRAM core operations. By increasing the number of operations performed by the DRAM in response to a request packet, the ratio of control information per operations performed is significantly reduced.

Line Noise Reduction

In typical DRAMs, multiple banks of memory receive power over the same power supply line. Every precharge or sense operation performed on a bank of memory generates some noise on the power supply line to which the bank is connected. In general, memory banks are not aware of operations that are concurrently being performed by other memory banks. Consequently, two or more memory banks that are powered over the same power supply line may concurrently perform precharge and/or sense operations. The increased noise that the power supply line experiences due to the concurrent execution of multiple noise-producing operations impairs the reliability of the DRAM in question or forces the power supply line to be larger, consuming precious die area.

To prevent these reliability problems, those prior art DRAMs must be exhaustively tested to ensure that all possible sense and precharge patterns can be performed without error. In the present invention, the DRAM includes a control circuit that is configured to allow no more than one bank on any given power supply line from performing precharge or sense operations at any given time. Because the DRAM does not allow more than one bank on a power supply line to be charged or sensed at a time, the DRAM is not susceptible to the noise problems that concurrent sense and precharge operations create. Further, the DRAM does not need to be tested for patterns that will never occur. In addition, the die size of the DRAM may be reduced because the power supply lines do not have to be able to handle current for more than one operation. The control circuit within the DRAM may enforce this restriction in a variety of ways.

In one embodiment, the control circuit includes a queue for each power supply line. Such an embodiment is illustrated in FIG. 20A. Referring to FIG. 20A, a DRAM **2000** includes control circuitry **2002** and four memory banks powered over two power supply lines that extend from a bond site **2020**. The control circuit **2002** receives request packets from the controller **2004** over the channel **2008** through an I/O unit **2030**. The request packets specify data transfer operations and the memory banks on which the operations are to be performed. The control circuit **2002** is configured to detect when the specified operations require precharge or sense operations. When a requested operation requires a precharge or a sense operation, the operation is placed on the queue associated with the power supply line to which the memory bank specified in the request packet is connected. For example, assume that control circuit **2002** receives a request packet that specifies an operation that requires bank **2010** to be precharged, and a request packet that specifies an operation that requires bank **2012** to be sensed. Banks **2010** and **2012** are powered by the same power supply line **2014**. Therefore, control circuitry **2002** will place both operations in the queue **2016** associated with power supply line **2014**.

The control circuit **2002** services the operations in any given queue one at a time. Thus, in the example given above, the control circuitry **2002** may cause the operation on bank **2010** to be performed, then cause the operation on bank **2012** to be performed. Because the operations are serviced sequentially, no more than one sense or precharge operation will be performed concurrently on banks connected to the same power supply line. Because the control circuitry **2002** maintains separate queues for each power supply line, precharge and sense operation may be perform concurrently on banks that are powered by different power supply lines within the same DRAM **2000**. In this embodiment, the controller **2004** is preferably configured to set the Open and Close bits in each request packet to prevent the queues associated with the power supply lines from overflowing.

In an alternate embodiment, control circuitry **2002** is configured to ignore request packets for operations that require a sense or precharge operation to be performed on a bank that is connected to the same power supply line as another bank on which a sense or precharge operation is currently being performed. In yet another embodiment, control circuitry **2002** does not process request packets that would violate the restriction, but transmits a message back to the controller **2004** to indicate that the request packet will not be serviced.

While a prohibition against concurrent sense and precharge operations by banks on the same power supply line limits the amount of concurrency that can take place between the memory banks, the overall architecture of the present invention is designed to maximize channel utilization without violating this restriction. Specifically, the controller adjusts the interleave of transactions in such a way as to maximize usage of the channel. No amount of concurrency within a DRAM will increase the throughput of a channel that is already fully utilized. Therefore, the enforcement of a prohibition against concurrent sense and precharge operations by banks on the same power supply line does not detrimentally affect the performance of the data transport system.

In an alternate embodiment illustrated in FIG. **20B**, the DRAM **2000** contains a single queue **2050**. All operations that require the DRAM **2000** of FIG. **20B** to perform a precharge or sense operation on any memory bank within DRAM **2000** of FIG. **20B** are placed in the queue **2050** by control circuitry **2002**. The control circuitry **2002** processes the operations stored in the queue **2050** sequentially, preventing more than one precharge or sense operation from being performed at the same time. While this embodiment does not allow the concurrency that is possible with the one-queue-per-power supply line embodiment, it requires less complex control circuitry.

In yet another embodiment, the control circuitry on the DRAM does not enforce the one core operation per power supply line restriction. Rather, control circuitry within the controller is configured to transmit request packets by selecting an order and timing that will not cause more than one core operation to be performed at the same time on banks connected to the same power supply line. In this embodiment, the DRAM may be manufactured with power supply lines designed to only support one core operation at a time, even though the DRAM itself does not enforce the restriction.

Example of Dynamically Adjusting Interleave

Referring to Appendix C, it illustrates a series of transactions in which a controller has dynamically adjusted the

interleave. The controller transmits the wakeup signal for the first transaction (transaction **0**) over the BusCtrl line at clock cycle **0**. The controller transmits the request packet for transaction **0** over the BusCtrl line and the BusData[**8**:**0**] lines from clock cycle **4** to clock cycle **6**. The controller transmits column address information over the BusEnable line from clock cycle **8** to clock cycle **10**. This column address information indicates the column address of the data for the second and subsequent data packets that will be involved in the transaction. The column address of the data for the first packet is included in the request packet. At clock cycle **10**, the controller transmits the strobe signal for transaction **0**. The timing of the strobe signal indicates to the DRAM when the DRAM is to begin retrieving and sending data for transaction **0**. In response to the strobe signal, the DRAM begins to retrieve data from the specified columns at clock cycle **10**, and begins sending the data over BusData [**8**:**0**] lines at clock cycle **16**. The DRAM first retrieves data from the column specified in the request packet, and then from the columns specified in the column address information that is sent over the BusEnable line. The controller transmits the terminate signal for transaction **0** over the BusCtrl line at clock cycle **15**. The timing of the terminate signal indicates to the DRAM when to stop sending data for tansaction **0**. In response to the terminate signal, the DRAM ceases to retrieve data after clock cycle **18**, and ceases to transfer data after clock cycle **23**. A total of two octbyte data packets are transmitted for transaction **0**.

The controller transmits the wakeup signal for the transaction **1** over the BusCtrl line at clock cycle **8**. The controller transmits the request packet for transaction **1** over the BusCtrl line and the BusData[**8**:**0**] lines from clock cycle **12** to clock cycle **14**. The controller transmits column address information over the BusEnable line from clock cycle **20** to clock cycle **31**. This column address information indicates the column address of the data for the second and subsequent data packets that will be involved in the transaction. The column address of the data for the first packet is included in the request packet. At clock cycle **22**, the controller transmits the strobe signal for transaction **1**. The timing of the strobe signal indicates to the DRAM when the DRAM is to begin retrieving and sending data for transaction **1**. In response to the strobe signal, the DRAM begins to retrieve data from the specified columns at clock cycle **23**, and begins sending the data over BusData[**8**:**0**] lines at clock cycle **28**. The DRAM first retrieves data from the column specified in the request packet, and then from the columns specified in the column address information that is sent over the BusEnable line. The controller transmits the terminate signal for transaction **1** over the BusCtrl line at clock cycle **35**. The timing of the terminate signal indicates to the DRAM when to stop sending data for transaction **1**. In response to the terminate signal, the DRAM ceases to retrieve data after clock cycle **38**, and ceases to transfer data after clock cycle **43**. A total of four octbyte data packets are transmitted for transaction **1**.

The controller transmits the wakeup signal for the transaction **2** over the BusCtrl line at clock cycle **20**. The controller transmits the request packet for transaction **2** over the BusCtrl line and the BusData[**8**:**0**] lines from clock cycle **24** to clock cycle **26**. The controller does not transmit column address information over the BusEnable line because transaction **1** involves only one octbyte data packet, the column address for which is included in the request packet. At clock cycle **50**, the controller transmits the strobe signal for transaction **2**. The timing of the strobe signal indicates to the DRAM when the DRAM is to begin retrieving and sending data for transaction **2**. In response to the strobe signal, the DRAM begins to retrieve data from the specified columns at clock cycle **51**, and begins sending the data over BusData[**8**:**0**] lines at clock cycle **56**. The controller transmits the terminate signal for transaction **2** over the BusCtrl line at clock cycle **51**. The timing of the terminate signal indicates to the DRAM when to stop sending data for transaction **2**. In response to the terminate signal, the DRAM ceases to retrieve data after clock cycle **54**, and ceases to transfer data after clock cycle **59**. A single octbyte data packet is transmitted for transaction **2**.

The controller transmits the wakeup signal for the transaction **3** over the BusCtrl line at clock cycle **40**. The controller transmits the request packet for transaction **3** over the BusCtrl line and the BusData[**8**:**0**] lines from clock cycle **44** to clock cycle **46**. The "open, no-close" parameters contained within the request packet indicates to the DRAM that the DRAM must perform a precharge and sense operation prior to performing the requested data transfer. Without waiting for the strobe signal for transaction **3**, the DRAM performs the precharge operation from clock cycle **50** to clock cycle **57**, and the sense operation from clock cycle **58** to clock cycle **65**. After the sense operation, a RAS operation is performed from clock cycle **66** to clock cycle **73**. The controller does not transmit column address information over the BusEnable line because transaction **3** involves only one octbyte data packet, the column address for which is included in the request packet. At clock cycle **66**, the controller transmits the strobe signal for transaction **3**. The timing of the strobe signal indicates to the DRAM when the DRAM is to begin retrieving and sending data for transaction **3**. In response to the strobe signal, the DRAM begins to retrieve data from the specified columns at clock cycle **66**, and begins sending the data over BusData[**8**:**0**] lines at clock cycle **72**. The controller transmits the terminate signal for transaction **3** over the BusCtrl line at clock cycle **67**. The timing of the terminate signal indicates to the DRAM when to stop sending data for transaction **3**. In response to the terminate signal, the DRAM ceases to retrieve data after clock cycle **70**, and ceases to transfer data after clock cycle **75**. A total of one octbyte data packet is transmitted for transaction **3**.

The controller transmits the wakeup signal for the transaction **4** over the BusCtrl line at clock cycle **48**. The controller transmits the request packet for transaction **4** over the BusCtrl line and the BusData[**8**:**0**] lines from clock cycle **52** to clock cycle **54**. The controller does not transmit column address information over the BusEnable line because transaction **1** involves only one octbyte data packet, the column address for which is included in the request packet. At clock cycle **58**, the controller transmits the strobe signal for transaction **4**. The timing of the strobe signal indicates to the DRAM when the DRAM is to begin retrieving and sending data for transaction **4**. In response to the strobe signal, the DRAM begins to retrieve data from the specified columns at clock cycle **59**, and begins sending the data over BusData[**8**:**0**] lines at clock cycle **64**. The controller transmits the terminate signal for transaction **4** over the BusCtrl line at clock cycle **59**. The timing of the terminate signal indicates to the DRAM when to stop sending data for transaction **4**. In response to the terminate signal, the DRAM ceases to retrieve data after clock cycle **62**, and ceases to transfer data after clock cycle **67**. A single octbyte data packet is transmitted for transaction **4**.

The transactions described above illustrate how the protocol employed by the present invention enables a controller to dynamically adjust numerous parameters relating to the timing and interleave of signals on the channel. For example, each of the transactions illustrates how the controller uses strobe and terminate signals to determine the

timing and size of data transfers. Thus, the size of the request packets for transaction **1** and transaction **3** are equal, but four times as much data is transmitted in transaction **1** as in transaction **3** because of the relative delay between the strobe and terminate signals for transaction **1**.

In addition, the controller can dynamically adjust the time between a request packet and the transmission of the data associated with the request. For example, three clock cycles elapse between the transmission of the request packet and the transmission of the strobe signal that dictates when the DRAM starts to send data for transaction **0**. In contrast, twenty-one clock cycles elapse between the transmission of the request packet for transaction **2** and the strobe signal that dictates when the DRAM starts to send data for transaction **2**.

Because the controller is able to adjust the time between the transmission of a request packet of a transaction and the transmission of data involved in the transaction, the controller can delay the transmission of data to allow the channel to be used for other purposes prior to the transmission of data. For example, the only signals sent over the BusCtrl and BusData[**8**:**0**] lines between the request packet for transaction **0** and the strobe for transaction **0** is a wakeup signal for transaction **1**. Therefore, the strobe signal for transaction **0** is sent three clock cycles after the request packet for transaction **0**. In contrast, the signals sent over the BusCtrl and BusData[**8**:**0**] lines between the request packet for transaction **2** and the strobe signal for transaction **2** include the data for transaction **1**, the terminate signal for transaction **1**, the wakeup signal for transaction **3**, the request packet for transaction **3** and the wakeup signal for transaction **4**. To allow all of this information to be sent before the data for transaction **3**, the strobe signal for transaction **3** is not sent until 24 clock cycles after the request packet for transaction **3**.

The transactions illustrated in Appendix C also illustrate that the protocol of the present invention enables a controller to alter the retirement order of transactions. In a typical DRAM system, transactions are serviced in the same order in which they are requested. However, the protocol of the present invention enables a controller to retire transactions out of order. In the example illustrated in Appendix C, the request packet for transaction **3** is transmitted at clock cycle **44** and the request packet for transaction **4** is transmitted **8** clock cycles later at clock cycle **52**. However, the strobe to start the data transfer for transaction **4** is transmitted at clock cycle **58**, while the strobe to start the data transfer for transaction **3** is not transmitted until clock cycle **66**. Consequently, transaction **4** is completely retired before the transmission of the data involved in transaction **3** even begins.

The transactions illustrated in Appendix C also illustrate that the protocol of the present invention enables a controller to adjust the interleave in a manner that causes the number of transactions outstanding on the channel to vary over time. For example, at clock cycle **15**, two transactions have been requested and none have been completed. Thus, two requests are outstanding. At clock cycle **55**, five transactions have been requested and two have been completed. Thus, three requests are outstanding.

As explained above, the protocol of the present invention enables a controller to dynamically adjust (1) the time at which data is sent relative to the time at which it is requested, (2) the retirement order of transactions, and (3) the number of outstanding requests. In addition, the protocol enables a controller to dictate the core operations to be performed by the DRAM, and the sequence in which the DRAM is to perform the core operations. The enhanced channel control bestowed by the protocol gives the controller the flexibility necessary to maximize the channel usage, allowing any given set of data transactions to be completed within a shorter period of time.

In the foregoing specification, the invention has been described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

APPENDIX A

Explanation of Transaction Templates

1.0 Introduction

This appendix contains a transaction template that shows the information that is communicated over a channel and the internal DRAM core states that occur during a series of transactions.

Timing information proceeds down the template, with each horizontal row representing a clock cycle or two bus samples. Each row represents 4 ns at 500 MHz or 3.75 ns at 533 MHz.

1.1 Clk Cyc Column.

The first column, labeled clock cycles, represents the time in clock cycles since the beginning of this template.

1.2 BE Column

The 2nd column labeled BE, is the state of the BusEnable pin during that clock cycle. BusEnable is only used to send serial addresses to the RDRAM.

1.3 BC Column

The 3rd column labeled BC, is the state of the BusCtrl pin during that clock cycle. BusCtrl is used to send request packets, strobe, terminate and wakeup information. During a request packet, this fields identifies the request number, so requests and data can be tracked, the request type, and the value of the Pend field for that transaction. For wakeup, strobes, and terminates it also indicates which transaction is being started, strobed and terminated, by the value carried with it, i.e. (strobe **0**)

1.4 BD[**8**:**0**] Column

The 4th column, labeled BD[**8**:**0**], is the state of the BusData wires during that clock cycle. During the data packet it indicates the transaction number and the octbyte being sent or received. During request packets it indicates the state of the control bits Open and Close. These bits are used to tell the RDRAM what core operations to perform. The state that is assumed for the bank being accessed and the addressed bank is also included in the last field of a request packet.

1.5 DRAM Internal State Columns

The 5th through 9th Columns represent the activity in an RDRAM labeled **0**, with the 5th column being it's CAS activity, and the next four being the activity or state of each of the 4 banks (Bank[**0**:**3**]). The 10th through 14th Columns represent the activity in any other RDRAM, labeled 1, with the 10th column being it's CAS activity, and the next four being the activity or state of each of the 4 banks (Bank[**0**:**3**]).

1.6 Column Encoding

The column encodings consist of two numbers. The first is the request number. The second is the octbyte number.

1.7 Bank[**0**:**3**] Encodings

These columns include a symbol that represents an operation and the number of the transaction that caused the operation. The meaning of the symbols is given in the table below.

Symbol	Name	Meaning	Length
p	Precharge	Precharge is the closing of a page (deassertion of RAS) and can be caused by closing at the end of a transaction, or opening a page that has not previously been precharged	8 Clocks
s	Sense	Sense is the operation of loading the sense amps to prepare for a CAS and is caused by a command with Open required	8 Clocks
r	RAS	RAS always follows the sense, and is needed to insure that the minimum RAS low time of the core is met.	8 Clocks

Non-interleaved precharged 4 oct 1 bank RWWRR

Clk				!0	Bank				!1	Bank			!
Cyc	BE	BC	BD [8:0]	!Col	0	1	2	3	!Col	0	1	2	3 !
0	----	wakeup 0	-------------	----	---	---	---	---	----	---	---	---	---
1	----	------------	-------------	----	---	---	---	---	----	---	---	---	---
2	----	------------	-------------	----	---	---	---	---	----	---	---	---	---
3	----	------------	-------------	----	---	---	---	---	----	---	---	---	---
4	----	req 0	open	----	---	---	---	---	----	---	---	---	---
5	----	read	close	----	---	---	---	---	----	---	---	---	---
6	----	pend 0	precharged 0	----	---	---	---	---	----	---	---	---	---
7	----	------------	-------------	----	---	---	---	---	----	---	---	---	---
8	----	------------	-------------	----	---	---	---	---	----	---	---	---	---
9	----	------------	-------------	----	---	---	---	---	----	---	---	---	---
10	----	------------	-------------	----	s0	---	---	---	----	---	---	---	---
11	----	------------	-------------	----	s0	---	---	---	----	---	---	---	---
12	----	------------	-------------	----	s0	---	---	---	----	---	---	---	---
13	----	------------	-------------	----	s0	---	---	---	----	---	---	---	---
14	----	------------	-------------	----	s0	---	---	---	----	---	---	---	---
15	0 1	------------	-------------	----	s0	---	---	---	----	---	---	---	---
16	0 1	------------	-------------	----	s0	---	---	---	----	---	---	---	---
17	0 1	strobe 0	-------------	----	s0	---	---	---	----	---	---	---	---
18	0 1	------------	-------------	0 0	r0	---	---	---	----	---	---	---	---
19	0 2	------------	-------------	0 0	r0	---	---	---	----	---	---	---	---
20	0 2	------------	-------------	0 0	r0	---	---	---	----	---	---	---	---
21	0 2	------------	-------------	0 0	r0	---	---	---	----	---	---	---	---
22	0 2	------------	turn	0 1	r0	---	---	---	----	---	---	---	---
23	0 3	------------	data 0 0	0 1	r0	---	---	---	----	---	---	---	---
24	0 3	------------	data 0 0	0 1	r0	---	---	---	----	---	---	---	---
25	0 3	------------	data 0 0	0 1	r0	---	---	---	----	---	---	---	---
26	0 3	------------	data 0 0	0 2	---	---	---	---	----	---	---	---	---
27	----	------------	data 0 1	0 2	---	---	---	---	----	---	---	---	---
28	----	------------	data 0 1	0 2	---	---	---	---	----	---	---	---	---
29	----	------------	data 0 1	0 2	---	---	---	---	----	---	---	---	---
30	----	term 0	data 0 1	0 3	---	---	---	---	----	---	---	---	---
31	----	------------	data 0 2	0 3	---	---	---	---	----	---	---	---	---
32	----	------------	data 0 2	0 3	---	---	---	---	----	---	---	---	---
33	----	------------	data 0 2	0 3	---	---	---	---	----	---	---	---	---
34	----	------------	data 0 2	----	---	---	---	---	----	---	---	---	---
35	----	wakeup 1	data 0 3	----	p0	---	---	---	----	---	---	---	---
36	----	------------	data 0 3	----	p0	---	---	---	----	---	---	---	---
37	----	------------	data 0 3	----	p0	---	---	---	----	---	---	---	---
38	----	------------	data 0 3	----	p0	---	---	---	----	---	---	---	---
39	----	req 1	open	----	p0	---	---	---	----	---	---	---	---
40	----	write	close	----	p0	---	---	---	----	---	---	---	---
41	----	pend 0	precharged 0	----	p0	---	---	---	----	---	---	---	---
42	----	------------	-------------	----	p0	---	---	---	----	---	---	---	---
43	----	------------	-------------	----	---	---	---	---	----	---	---	---	---
44	1 1	------------	-------------	----	---	---	---	---	----	---	---	---	---
45	1 1	------------	-------------	----	s1	---	---	---	----	---	---	---	---
46	1 1	------------	-------------	----	s1	---	---	---	----	---	---	---	---
47	1 1	strobe 1	-------------	----	s1	---	---	---	----	---	---	---	---
48	1 2	------------	data 1 0	----	s1	---	---	---	----	---	---	---	---
49	1 2	------------	data 1 0	----	s1	---	---	---	----	---	---	---	---
50	1 2	------------	data 1 0	----	s1	---	---	---	----	---	---	---	---
51	1 2	------------	data 1 0	----	s1	---	---	---	----	---	---	---	---
52	1 3	------------	data 1 1	----	s1	---	---	---	----	---	---	---	---
53	1 3	------------	data 1 1	1 0	r1	---	---	---	----	---	---	---	---
54	1 3	------------	data 1 1	1 0	r1	---	---	---	----	---	---	---	---
55	1 3	------------	data 1 1	1 0	r1	---	---	---	----	---	---	---	---
56	----	------------	data 1 2	1 0	r1	---	---	---	----	---	---	---	---
57	----	------------	data 1 2	1 1	r1	---	---	---	----	---	---	---	---
58	----	------------	data 1 2	1 1	r1	---	---	---	----	---	---	---	---
59	----	------------	data 1 2	1 1	r1	---	---	---	----	---	---	---	---
60	----	term 1	data 1 3	1 1	r1	---	---	---	----	---	---	---	---
61	----	------------	data 1 3	1 2	---	---	---	---	----	---	---	---	---
62	----	------------	data 1 3	1 2	---	---	---	---	----	---	---	---	---

-continued

63	----	-------------	data 1 3	1 2	---	---	---	---	----	---	---	---	---
64	----	-------------	-------------	1 2	---	---	---	---	----	---	---	---	---
65	----	-------------	-------------	1 3	---	---	---	---	----	---	---	---	---
66	----	-------------	-------------	1 3	---	---	---	---	----	---	---	---	---
67	----	wakeup 2	-------------	1 3	---	---	---	---	----	---	---	---	---
68	----	-------------	-------------	1 3	---	---	---	---	----	---	---	---	---
69	----	-------------	-------------	----	p1	---	---	---	----	---	---	---	---
70	----	-------------	-------------	----	p1	---	---	---	----	---	---	---	---
71	----	req 2	open	----	p1	---	---	---	----	---	---	---	---
72	----	write	close	----	p1	---	---	---	----	---	---	---	---
73	----	pend 0	precharged 0	----	p1	---	---	---	----	---	---	---	---
74	----	-------------	-------------	----	p1	---	---	---	----	---	---	---	---
75	----	-------------	-------------	----	p1	---	---	---	----	---	---	---	---
76	2 1	-------------	-------------	----	p1	---	---	---	----	---	---	---	---
77	2 1	-------------	-------------	----	s2	---	---	---	----	---	---	---	---
78	2 1	-------------	-------------	----	s2	---	---	---	----	---	---	---	---
79	2 1	strobe 2	-------------	----	s2	---	---	---	----	---	---	---	---
80	2 2	-------------	data 2 0	----	s2	---	---	---	----	---	---	---	---
81	2 2	-------------	data 2 0	----	s2	---	---	---	----	---	---	---	---
82	2 2	-------------	data 2 0	----	s2	---	---	---	----	---	---	---	---
83	2 2	-------------	data 2 0	----	s2	---	---	---	----	---	---	---	---
84	2 3	-------------	data 2 1	----	s2	---	---	---	----	---	---	---	---
85	2 3	-------------	data 2 1	2 0	r2	---	---	---	----	---	---	---	---
86	2 3	-------------	data 2 1	2 0	r2	---	---	---	----	---	---	---	---
87	2 3	-------------	data 2 1	2 0	r2	---	---	---	----	---	---	---	---
88	----	-------------	data 2 2	2 0	r2	---	---	---	----	---	---	---	---
89	----	-------------	data 2 2	2 1	r2	---	---	---	----	---	---	---	---
90	----	-------------	data 2 2	2 1	r2	---	---	---	----	---	---	---	---
91	----	-------------	data 2 2	2 1	r2	---	---	---	----	---	---	---	---
92	----	term 2	data 2 3	2 1	r2	---	---	---	----	---	---	---	---
93	----	-------------	data 2 3	2 2	---	---	---	---	----	---	---	---	---
94	----	-------------	data 2 3	2 2	---	---	---	---	----	---	---	---	---
95	----	-------------	data 2 3	2 2	---	---	---	---	----	---	---	---	---
96	----	-------------	-------------	2 2	---	---	---	---	----	---	---	---	---
97	----	-------------	-------------	2 3	---	---	---	---	----	---	---	---	---
98	----	-------------	-------------	2 3	---	---	---	---	----	---	---	---	---
99	----	wakeup 3	-------------	2 3	---	---	---	---	----	---	---	---	---
100	----	-------------	-------------	2 3	---	---	---	---	----	---	---	---	---
101	----	-------------	-------------	----	p2	---	---	---	----	---	---	---	---
102	----	-------------	-------------	----	p2	---	---	---	----	---	---	---	---
103	----	req 3	open	----	p2	---	---	---	----	---	---	---	---
104	----	read	close	----	p2	---	---	---	----	---	---	---	---
105	----	pend 0	precharged 0	----	p2	---	---	---	----	---	---	---	---
106	----	-------------	-------------	----	p2	---	---	---	----	---	---	---	---
107	----	-------------	-------------	----	p2	---	---	---	----	---	---	---	---
108	----	-------------	-------------	----	p2	---	---	---	----	---	---	---	---
109	----	-------------	-------------	----	s3	---	---	---	----	---	---	---	---
110	----	-------------	-------------	----	s3	---	---	---	----	---	---	---	---
111	----	-------------	-------------	----	s3	---	---	---	----	---	---	---	---
112	----	-------------	-------------	----	s3	---	---	---	----	---	---	---	---
113	----	-------------	-------------	----	s3	---	---	---	----	---	---	---	---
114	3 1	-------------	-------------	----	s3	---	---	---	----	---	---	---	---
115	3 1	-------------	-------------	----	s3	---	---	---	----	---	---	---	---
116	3 1	strobe 3	-------------	----	s3	---	---	---	----	---	---	---	---
117	3 1	-------------	-------------	3 0	r3	---	---	---	----	---	---	---	---
118	3 2	-------------	-------------	3 0	r3	---	---	---	----	---	---	---	---
119	3 2	-------------	-------------	3 0	r3	---	---	---	----	---	---	---	---
120	3 2	-------------	-------------	3 0	r3	---	---	---	----	---	---	---	---
121	3 2	-------------	turn	3 1	r3	---	---	---	----	---	---	---	---
122	3 3	-------------	data 3 0	3 1	r3	---	---	---	----	---	---	---	---
123	3 3	-------------	data 3 0	3 1	r3	---	---	---	----	---	---	---	---
124	3 3	-------------	data 3 0	3 1	r3	---	---	---	----	---	---	---	---
125	3 3	-------------	data 3 0	3 2	---	---	---	---	----	---	---	---	---
126	----	-------------	data 3 1	3 2	---	---	---	---	----	---	---	---	---
127	----	-------------	data 3 1	3 2	---	---	---	---	----	---	---	---	---
128	----	-------------	data 3 1	3 2	---	---	---	---	----	---	---	---	---
129	----	term 3	data 3 1	3 3	---	---	---	---	----	---	---	---	---
130	----	-------------	data 3 2	3 3	---	---	---	---	----	---	---	---	---
131	----	-------------	data 3 2	3 3	---	---	---	---	----	---	---	---	---
132	----	-------------	data 3 2	3 3	---	---	---	---	----	---	---	---	---
133	----	-------------	data 3 2	----	---	---	---	---	----	---	---	---	---
134	----	wakeup 4	data 3 3	----	p3	---	---	---	----	---	---	---	---
135	----	-------------	data 3 3	----	p3	---	---	---	----	---	---	---	---
136	----	-------------	data 3 3	----	p3	---	---	---	----	---	---	---	---
137	----	-------------	data 3 3	----	p3	---	---	---	----	---	---	---	---
138	----	req 4	open	----	p3	---	---	---	----	---	---	---	---
139	----	read	close	----	p3	---	---	---	----	---	---	---	---
140	----	pend 0	precharged 0	----	p3	---	---	---	----	---	---	---	---
141	----	-------------	-------------	----	p3	---	---	---	----	---	---	---	---

-continued

142	----	------------	------------	----	---	---	---	---	----	---	---	---	---
143	----	------------	------------	----	---	---	---	---	----	---	---	---	---
144	----	------------	------------	----	s4	---	---	---	----	---	---	---	---
145	----	------------	------------	----	s4	---	---	---	----	---	---	---	---
146	----	------------	------------	----	s4	---	---	---	----	---	---	---	---
147	----	------------	------------	----	s4	---	---	---	----	---	---	---	---
148	----	------------	------------	----	s4	---	---	---	----	---	---	---	---
149	4 1	------------	------------	----	s4	---	---	---	----	---	---	---	---
150	4 1	------------	------------	----	s4	---	---	---	----	---	---	---	---
151	4 1	strobe 4	------------	----	s4	---	---	---	----	---	---	---	---
152	4 1	------------	------------	4 0	r4	---	---	---	----	---	---	---	---
153	4 2	------------	------------	4 0	r4	---	---	---	----	---	---	---	---
154	4 2	------------	------------	4 0	r4	---	---	---	----	---	---	---	---
155	4 2	------------	------------	4 0	r4	---	---	---	----	---	---	---	---
156	4 2	------------	turn	4 1	r4	---	---	---	----	---	---	---	---
157	4 3	------------	data 4 0	4 1	r4	---	---	---	----	---	---	---	---
158	4 3	------------	data 4 0	4 1	r4	---	---	---	----	---	---	---	---
159	4 3	------------	data 4 0	4 1	r4	---	---	---	----	---	---	---	---
160	4 3	------------	data 4 0	4 2	---	---	---	---	----	---	---	---	---
161	----	------------	data 4 1	4 2	---	---	---	---	----	---	---	---	---
162	----	------------	data 4 1	4 2	---	---	---	---	----	---	---	---	---
163	----	------------	data 4 1	4 2	---	---	---	---	----	---	---	---	---
164	----	term 4	data 4 1	4 3	---	---	---	---	----	---	---	---	---
165	----	------------	data 4 2	4 3	---	---	---	---	----	---	---	---	---
166	----	------------	data 4 2	4 3	---	---	---	---	----	---	---	---	---
167	----	------------	data 4 2	4 3	---	---	---	---	----	---	---	---	---
168	----	------------	data 4 2	----	---	---	---	---	----	---	---	---	---
169	----	------------	data 4 3	----	p4	---	---	---	----	---	---	---	---
170	----	------------	data 4 3	----	p4	---	---	---	----	---	---	---	---
171	----	------------	data 4 3	----	p4	---	---	---	----	---	---	---	---
172	----	------------	data 4 3	----	p4	---	---	---	----	---	---	---	---
173	----	------------	------------	----	p4	---	---	---	----	---	---	---	---
174	----	------------	------------	----	p4	---	---	---	----	---	---	---	---
175	----	------------	------------	----	p4	---	---	---	----	---	---	---	---
176	----	------------	------------	----	p4	---	---	---	----	---	---	---	---

APPENDIX B

Explanation of Transaction Templates

1.0 Introduction

This appendix contains a transaction template that shows the information that is communicated over a channel and the internal DRAM core states that occur during a series of transactions.

Timing information proceeds down the template, with each horizontal row representing a clock cycle or two bus samples. Each row represents 4 ns at 500 MHz or 3.75 ns at 533 MHz.

1.1 Clk Cyc Column

The first column, labeled clock cycles, represents the time in clock cycles since the beginning of this template.

1.2 BE Column

The 2nd column labeled BE, is the state of the BusEnable pin during that clock cycle. BusEnable is only used to send serial addresses to the RDRAM.

1.3 BC Column

The 3rd column labeled BC, is the state of the BusCtrl pin during that clock cycle. BusCtrl is used to send request packets, strobe, terminate and wakeup information. During a request packet, this fields identifies the request number, so requests and data can be tracked, the request type, and the value of the Pend field for that transaction. For wakeup, strobes, and terminates it also indicates which transaction is being started, strobed and terminated, by the value carried with it, i.e. (strobe **0**)

1.4 BD[**8**:**0**] Column

The 4th column, labeled BD[**8**:**0**], is the state of the BusData wires during that clock cycle. During the data packet it indicates the transaction number and the octbyte being sent or received. During request packets it indicates the state of the control bits Open and Close. These bits are used to tell the RDRAM what core operations to perform. The state that is assumed for the bank being accessed and the addressed bank is also included in the last field of a request packet.

1.5 DRAM Internal State Columns

The 5th through 9th Columns represent the activity in an RDRAM labeled **0**, with the 5th column being it's CAS activity, and the next four being the activity or state of each of the 4 banks (Bank[**0**:**3**]). The 10th through 14th Columns represent the activity in any other RDRAM, labeled **1**, with the 10th column being it's CAS activity, and the next four being the activity or state of each of the 4 banks (Bank[**0**:**3**]).

1.6 Column Encoding

The column encodings consist of two numbers. The first is the request number. The second is the octbyte number.

1.7 Bank[**0**:**3**] Encodings

These columns include a symbol that represents an operation and the number of the transaction that caused the operation. The meaning of the symbols is given in the table below.

Symbol	Name	Meaning	Length
p	Precharge	Precharge is the closing of a page (deassertion of RAS) and can be caused by closing at the end of a transaction, or opening a page that has not previously been precharged	8 Clocks
s	Sense	Sense is the operation of loading the sense amps to prepare for a CAS and is caused by a command with Open required	8 Clocks
r	RAS	RAS always follows the sense, and is needed to insure that the minimum RAS low time of the core is met.	8 Clocks

Interleaved precharged 4 oct 2 bank RWWRWWRRR

Clk				!0	Bank				!1	Bank			!
Cyc	BE	BC	BD [8:0]	!Col	0	1	2	3	!Col	0	1	2	3 !
0	----	wakeup 0	-------------	----	---	---	---	---	----	---	---	---	---
1	----	-------------	-------------	----	---	---	---	---	----	---	---	---	---
2	----	-------------	-------------	----	---	---	---	---	----	---	---	---	---
3	----	-------------	-------------	----	---	---	---	---	----	---	---	---	---
4	----	req 0	open	----	---	---	---	---	----	---	---	---	---
5	----	read	close	----	---	---	---	---	----	---	---	---	---
6	----	pend 1	precharged 0	----	---	---	---	---	----	---	---	---	---
7	----	-------------	-------------	----	---	---	---	---	----	---	---	---	---
8	----	-------------	-------------	----	---	---	---	---	----	---	---	---	---
9	----	-------------	-------------	----	---	---	---	---	----	---	---	---	---
10	----	-------------	-------------	----	s0	---	---	---	----	---	---	---	---
11	----	-------------	-------------	----	s0	---	---	---	----	---	---	---	---
12	----	-------------	-------------	----	s0	---	---	---	----	---	---	---	---
13	----	-------------	-------------	----	s0	---	---	---	----	---	---	---	---
14	----	-------------	-------------	----	s0	---	---	---	----	---	---	---	---
15	----	-------------	-------------	----	s0	---	---	---	----	---	---	---	---
16	----	-------------	-------------	----	s0	---	---	---	----	---	---	---	---
17	----	-------------	-------------	----	s0	---	---	---	----	---	---	---	---
18	----	-------------	-------------	0 0	r0	---	---	---	----	---	---	---	---
19	----	-------------	-------------	0 0	r0	---	---	---	----	---	---	---	---
20	0 1	wakeup 1	-------------	0 0	r0	---	---	---	----	---	---	---	---
21	0 1	-------------	-------------	0 0	r0	---	---	---	----	---	---	---	---
22	0 1	strobe 0	-------------	0 0	r0	---	---	---	----	---	---	---	---
23	0 1	-------------	-------------	0 0	r0	---	---	---	----	---	---	---	---
24	0 2	req 1	open	0 0	r0	---	---	---	----	---	---	---	---
25	0 2	write	close	0 0	r0	---	---	---	----	---	---	---	---
26	0 2	pend 2	precharged 1	0 0	---	---	---	---	----	---	---	---	---
27	0 2	-------------	turn	0 1	---	---	---	---	----	---	---	---	---
26	0 3	-------------	data 0 0	0 1	---	---	---	---	----	---	---	---	---
29	0 3	-------------	data 0 0	0 1	---	---	---	---	----	---	---	---	---
30	0 3	-------------	data 0 0	0 1	---	s1	---	---	----	---	---	---	---
31	0 3	-------------	data 0 0	0 2	---	s1	---	---	----	---	---	---	---
32	----	-------------	data 0 1	0 2	---	s1	---	---	----	---	---	---	---
33	----	-------------	data 0 1	0 2	---	s1	---	---	----	---	---	---	---
34	----	-------------	data 0 1	0 2	---	s1	---	---	----	---	---	---	---
35	----	term 0	data 0 1	0 3	---	s1	---	---	----	---	---	---	---
36	----	-------------	data 0 2	0 3	---	s1	---	---	----	---	---	---	---
37	----	-------------	data 0 2	0 3	---	s1	---	---	----	---	---	---	---
38	----	-------------	data 0 2	0 3	---	r1	---	---	----	---	---	---	---
39	----	-------------	data 0 2	----	---	r1	---	---	----	---	---	---	---
40	----	wakeup 2	data 0 3	----	p0	r1	---	---	----	---	---	---	---
41	----	-------------	data 0 3	----	p0	r1	---	---	----	---	---	---	---
42	----	-------------	data 0 3	----	p0	r1	---	---	----	---	---	---	---
43	----	-------------	data 0 3	----	p0	r1	---	---	----	---	---	---	---
44	1 1	req 2	open	----	p0	r1	---	---	----	---	---	---	---
45	1 1	write	close	----	p0	r1	---	---	----	---	---	---	---
46	1 1	pend 2	precharged 0	----	p0	---	---	---	----	---	---	---	---
47	1 1	strobe 1	-------------	----	p0	---	---	---	----	---	---	---	---
46	1 2	-------------	data 1 0	----	---	---	---	---	----	---	---	---	---
49	1 2	-------------	data 1 0	----	---	---	---	---	----	---	---	---	---
50	1 2	-------------	data 1 0	----	s2	---	---	---	----	---	---	---	---
51	1 2	-------------	data 1 0	----	s2	---	---	---	----	---	---	---	---
52	1 3	-------------	data 1 1	----	s2	---	---	---	----	---	---	---	---
53	1 3	-------------	data 1 1	1 0	s2	---	---	---	----	---	---	---	---
54	1 3	-------------	data 1 1	1 0	s2	---	---	---	----	---	---	---	---
55	1 3	-------------	data 1 1	1 0	s2	---	---	---	----	---	---	---	---
56	----	-------------	data 1 2	1 0	s2	---	---	---	----	---	---	---	---
57	----	-------------	data 1 2	1 1	s2	---	---	---	----	---	---	---	---
58	----	-------------	data 1 2	1 1	r2	---	---	---	----	---	---	---	---
59	----	-------------	data 1 2	1 1	r2	---	---	---	----	---	---	---	---
60	----	term 1	data 1 3	1 1	r2	---	---	---	----	---	---	---	---
61	----	-------------	data 1 3	1 2	r2	---	---	---	----	---	---	---	---
62	----	-------------	data 1 3	1 2	r2	---	---	---	----	---	---	---	---

-continued

63	----	------------	data 1 3	1 2	r2	---	---	---	----	---	---	---	---
64	2 1	req 3	open	1 2	r2	---	---	---	----	---	---	---	---
65	2 1	read	close	1 3	r2	---	---	---	----	---	---	---	---
66	2 1	pend 3	precharged 1	1 3	---	---	---	---	----	---	---	---	---
67	2 1	strobe 2	------------	1 3	---	---	---	---	----	---	---	---	---
68	2 2	------------	data 2 0	1 3	---	---	---	---	----	---	---	---	---
69	2 2	------------	data 2 0	----	---	p1	---	---	----	---	---	---	---
70	2 2	------------	data 2 0	----	---	p1	---	---	----	---	---	---	---
71	2 2	------------	data 2 0	----	---	p1	---	---	----	---	---	---	---
72	2 3	------------	data 2 1	----	---	p1	---	---	----	---	---	---	---
73	2 3	------------	data 2 1	2 0	---	p1	---	---	----	---	---	---	---
74	2 3	------------	data 2 1	2 0	---	p1	---	---	----	---	---	---	---
75	2 3	------------	data 2 1	2 0	---	p1	---	---	----	---	---	---	---
76	----	------------	data 2 2	2 0	---	p1	---	---	----	---	---	---	---
77	----	------------	data 2 2	2 1	---	---	---	---	----	---	---	---	---
78	----	------------	data 2 2	2 1	---	s3	---	---	----	---	---	---	---
79	----	------------	data 2 2	2 1	---	s3	---	---	----	---	---	---	---
80	----	term 2	data 2 3	2 1	---	s3	---	---	----	---	---	---	---
81	----	------------	data 2 3	2 2	---	s3	---	---	----	---	---	---	---
82	----	------------	data 2 3	2 2	---	s3	---	---	----	---	---	---	---
83	----	------------	data 2 3	2 2	---	s3	---	---	----	---	---	---	---
84	----	------------	------------	2 2	---	s3	---	---	----	---	---	---	---
85	----	------------	------------	2 3	---	s3	---	---	----	---	---	---	---
86	----	------------	------------	2 3	---	r3	---	---	----	---	---	---	---
87	----	------------	------------	2 3	---	r3	---	---	----	---	---	---	---
88	3 1	wakeup 4	------------	2 3	---	r3	---	---	----	---	---	---	---
89	3 1	------------	------------	3 0	p2	r3	---	---	----	---	---	---	---
90	3 1	strobe 3	------------	3 0	p2	r3	---	---	----	---	---	---	---
91	3 1	------------	------------	3 0	p2	r3	---	---	----	---	---	---	---
92	3 2	req 4	open	3 0	p2	r3	---	---	----	---	---	---	---
93	3 2	write	close	3 0	p2	r3	---	---	----	---	---	---	---
94	3 2	pend 2	precharged 0	3 0	p2	---	---	---	----	---	---	---	---
95	3 2	------------	turn	3 1	p2	---	---	---	----	---	---	---	---
96	3 3	------------	data 3 0	3 1	p2	---	---	---	----	---	---	---	---
97	3 3	------------	data 3 0	3 1	---	---	---	---	----	---	---	---	---
98	3 3	------------	data 3 0	3 1	s4	---	---	---	----	---	---	---	---
99	3 3	------------	data 3 0	3 2	s4	---	---	---	----	---	---	---	---
100	----	------------	data 3 1	3 2	s4	---	---	---	----	---	---	---	---
101	----	------------	data 3 1	3 2	s4	---	---	---	----	---	---	---	---
102	----	------------	data 3 1	3 2	s4	---	---	---	----	---	---	---	---
103	----	term 3	data 3 1	3 3	s4	---	---	---	----	---	---	---	---
104	----	------------	data 3 2	3 3	s4	---	---	---	----	---	---	---	---
105	----	------------	data 3 2	3 3	s4	---	---	---	----	---	---	---	---
106	----	------------	data 3 2	3 3	r4	---	---	---	----	---	---	---	---
107	----	------------	data 3 2	----	r4	---	---	---	----	---	---	---	---
108	----	wakeup 5	data 3 3	----	r4	p3	---	---	----	---	---	---	---
109	----	------------	data 3 3	----	r4	p3	---	---	----	---	---	---	---
110	----	------------	data 3 3	----	r4	p3	---	---	----	---	---	---	---
111	----	------------	data 3 3	----	r4	p3	---	---	----	---	---	---	---
112	4 1	req 5	open	----	r4	p3	---	---	----	---	---	---	---
113	4 1	write	close	----	r4	p3	---	---	----	---	---	---	---
114	4 1	pend 2	precharged 1	----	---	p3	---	---	----	---	---	---	---
115	4 1	strobe 4	------------	----	---	p3	---	---	----	---	---	---	---
116	4 2	------------	data 4 0	----	---	---	---	---	----	---	---	---	---
117	4 2	------------	data 4 0	----	---	---	---	---	----	---	---	---	---
118	4 2	------------	data 4 0	----	---	s5	---	---	----	---	---	---	---
119	4 2	------------	data 4 0	----	---	s5	---	---	----	---	---	---	---
120	4 3	------------	data 4 1	----	---	s5	---	---	----	---	---	---	---
121	4 3	------------	data 4 1	4 0	---	s5	---	---	----	---	---	---	---
122	4 3	------------	data 4 1	4 0	---	s5	---	---	----	---	---	---	---
123	4 3	------------	data 4 1	4 0	---	s5	---	---	----	---	---	---	---
124	----	------------	data 4 2	4 0	---	s5	---	---	----	---	---	---	---
125	----	------------	data 4 2	4 1	---	s5	---	---	----	---	---	---	---
126	----	------------	data 4 2	4 1	---	r5	---	---	----	---	---	---	---
127	----	------------	data 4 2	4 1	---	r5	---	---	----	---	---	---	---
128	----	term 4	data 4 3	4 1	---	r5	---	---	----	---	---	---	---
129	----	------------	data 4 3	4 2	---	r5	---	---	----	---	---	---	---
130	----	------------	data 4 3	4 2	---	r5	---	---	----	---	---	---	---
131	----	------------	data 4 3	4 2	---	r5	---	---	----	---	---	---	---
132	5 1	req 6	open	4 2	---	r5	---	---	----	---	---	---	---
133	5 1	read	close	4 3	---	r5	---	---	----	---	---	---	---
134	5 1	pend 0	precharged 0	4 3	---	---	---	---	----	---	---	---	---
135	5 1	strobe 5	------------	4 3	---	---	---	---	----	---	---	---	---
136	5 2	------------	data 5 0	4 3	---	---	---	---	----	---	---	---	---
137	5 2	------------	data 5 0	----	p4	---	---	---	----	---	---	---	---
138	5 2	------------	data 5 0	----	p4	---	---	---	----	---	---	---	---
139	5 2	------------	data 5 0	----	p4	---	---	---	----	---	---	---	---
140	5 3	------------	data 5 1	----	p4	---	---	---	----	---	---	---	---
141	5 3	------------	data 5 1	5 0	p4	---	---	---	----	---	---	---	---

-continued

142	5 3	------------	data 5 1	5 0	p4	---	---	---	----	---	---	---	---
143	5 3	------------	data 5 1	5 0	p4	---	---	---	----	---	---	---	---
144	----	------------	data 5 2	5 0	p4	---	---	---	----	---	---	---	---
145	----	------------	data 5 2	5 1	---	---	---	---	----	---	---	---	---
146	----	------------	data 5 2	5 1	s6	---	---	---	----	---	---	---	---
147	----	------------	data 5 2	5 1	s6	---	---	---	----	---	---	---	---
148	----	term 5	data 5 3	5 1	s6	---	---	---	----	---	---	---	---
149	----	------------	data 5 3	5 2	s6	---	---	---	----	---	---	---	---
150	----	------------	data 5 3	5 2	s6	---	---	---	----	---	---	---	---
151	----	------------	data 5 3	5 2	s6	---	---	---	----	---	---	---	---
152	----	------------	-------------	5 2	s6	---	---	---	----	---	---	---	---
153	----	------------	-------------	5 3	s6	---	---	---	----	---	---	---	---
154	----	------------	-------------	5 3	r6	---	---	---	----	---	---	---	---
155	----	------------	-------------	5 3	r6	---	---	---	----	---	---	---	---
156	6 1	wakeup 7	-------------	5 3	r6	---	---	---	----	---	---	---	---
157	6 1	------------	-------------	6 0	r6	p5	---	---	----	---	---	---	---
158	6 1	strobe 6	-------------	6 0	r6	p5	---	---	----	---	---	---	---
159	6 1	------------	-------------	6 0	r6	p5	---	---	----	---	---	---	---
160	6 2	req 7	open	6 0	r6	p5	---	---	----	---	---	---	---
161	6 2	read	close	6 0	r6	p5	---	---	----	---	---	---	---
162	6 2	pend 2	precharged 1	6 0	---	p5	---	---	----	---	---	---	---
163	6 2	------------	turn	6 1	---	p5	---	---	----	---	---	---	---
164	6 3	------------	data 6 0	6 1	---	p5	---	---	----	---	---	---	---
165	6 3	------------	data 6 0	6 1	---	---	---	---	----	---	---	---	---
166	6 3	------------	data 6 0	6 1	---	s7	---	---	----	---	---	---	---
167	6 3	------------	data 6 0	6 2	---	s7	---	---	----	---	---	---	---
168	----	------------	data 6 1	6 2	---	s7	---	---	----	---	---	---	---
169	----	------------	data 6 1	6 2	---	s7	---	---	----	---	---	---	---
170	----	------------	data 6 1	6 2	---	s7	---	---	----	---	---	---	---
171	----	term 6	data 6 1	6 3	---	s7	---	---	----	---	---	---	---
172	----	------------	data 6 2	6 3	---	s7	---	---	----	---	---	---	---
173	----	------------	data 6 2	6 3	---	s7	---	---	----	---	---	---	---
174	----	------------	data 6 2	6 3	---	r7	---	---	----	---	---	---	---
175	----	------------	data 6 2	7 0	---	r7	---	---	----	---	---	---	---
176	----	------------	data 6 3	7 0	p6	r7	---	---	----	---	---	---	---
177	----	------------	data 6 3	7 0	p6	r7	---	---	----	---	---	---	---
178	----	------------	data 6 3	7 0	p6	r7	---	---	----	---	---	---	---
179	----	------------	data 6 3	7 0	p6	r7	---	---	----	---	---	---	---
180	----	------------	-------------	7 0	p6	r7	---	---	----	---	---	---	---
181	----	------------	-------------	7 0	p6	r7	---	---	----	---	---	---	---
182	----	------------	-------------	7 0	p6	---	---	---	----	---	---	---	---
183	----	------------	-------------	7 0	p6	---	---	---	----	---	---	---	---
184	7 1	wakeup 8	-------------	7 0	---	---	---	---	----	---	---	---	---
185	7 1	------------	-------------	7 0	---	---	---	---	----	---	---	---	---
186	7 1	strobe 7	-------------	7 0	---	---	---	---	----	---	---	---	---
187	7 1	------------	-------------	7 0	---	---	---	---	----	---	---	---	---
188	7 2	req 8	open	7 0	---	---	---	---	----	---	---	---	---
189	7 2	read	close	7 0	---	---	---	---	----	---	---	---	---
190	7 2	pend 2	precharged 0	7 0	---	---	---	---	----	---	---	---	---
191	7 2	------------	turn	7 1	---	---	---	---	----	---	---	---	---
192	7 3	------------	data 7 0	7 1	---	---	---	---	----	---	---	---	---
193	7 3	------------	data 7 0	7 1	---	---	---	---	----	---	---	---	---
194	7 3	------------	data 7 0	7 1	s8	---	---	---	----	---	---	---	---
195	7 3	------------	data 7 0	7 2	s8	---	---	---	----	---	---	---	---
196	----	------------	data 7 1	7 2	s8	---	---	---	----	---	---	---	---
197	----	------------	data 7 1	7 2	s8	---	---	---	----	---	---	---	---
198	----	------------	data 7 1	7 2	s8	---	---	---	----	---	---	---	---
199	----	term 8	data 7 1	7 3	s8	---	---	---	----	---	---	---	---
200	----	------------	data 7 2	7 3	s8	---	---	---	----	---	---	---	---
201	----	------------	data 7 2	7 3	s8	---	---	---	----	---	---	---	---
202	----	------------	data 7 2	7 3	r8	---	---	---	----	---	---	---	---
203	----	------------	data 7 2	8 0	r8	---	---	---	----	---	---	---	---
204	8 1	wakeup 9	data 7 3	8 0	r8	p7	---	---	----	---	---	---	---
205	8 1	------------	data 7 3	8 0	r8	p7	---	---	----	---	---	---	---
206	8 1	strobe 8	data 7 3	8 0	r8	p7	---	---	----	---	---	---	---
207	8 1	------------	data 7 3	8 0	r8	p7	---	---	----	---	---	---	---
208	8 2	------------	-------------	8 0	r8	p7	---	---	----	---	---	---	---
209	8 2	------------	-------------	8 0	r8	p7	---	---	----	---	---	---	---
210	8 2	------------	-------------	8 0	---	p7	---	---	----	---	---	---	---
211	8 2	------------	turn	8 1	---	p7	---	---	----	---	---	---	---
212	8 3	------------	data 8 0	8 1	---	---	---	---	----	---	---	---	---
213	8 3	------------	data 8 0	8 1	---	---	---	---	----	---	---	---	---
214	8 3	------------	data 8 0	8 1	---	---	---	---	----	---	---	---	---
215	8 3	------------	data 8 0	8 2	---	---	---	---	----	---	---	---	---
216	----	------------	data 8 1	8 2	---	---	---	---	----	---	---	---	---
217	----	------------	data 8 1	8 2	---	---	---	---	----	---	---	---	---
218	----	------------	data 8 1	8 2	---	---	---	---	----	---	---	---	---
219	----	term	data 8 1	8 3	---	---	---	---	----	---	---	---	---
220	----	------------	data 8 2	8 3	---	---	---	---	----	---	---	---	---

-continued

221	----	------------	data 8 2	8 3	---	---	---	---	----	---	---	---	---
222	----	------------	data 8 2	8 3	---	---	---	---	----	---	---	---	---
223	----	------------	data 8 2	----	---	---	---	---	----	---	---	---	---
224	----	------------	data 8 3	----	p8	---	---	---	----	---	---	---	---
225	----	------------	data 8 3	----	p8	---	---	---	----	---	---	---	---
226	----	------------	data 8 3	----	p8	---	---	---	----	---	---	---	---
227	----	------------	data 8 3	----	p8	---	---	---	----	---	---	---	---
228	----	------------	------------	----	p8	---	---	---	----	---	---	---	---
229	----	------------	------------	----	p8	---	---	---	----	---	---	---	---
230	----	------------	------------	----	p8	---	---	---	----	---	---	---	---
231	----	------------	------------	----	p8	---	---	---	----	---	---	---	---

APPENDIX C

Explanation of Transaction Templates

1.0 Introduction

This appendix contains a transaction template that shows the information that is communicated over a channel and the internal DRAM core states that occur during a series of transactions.

Timing information proceeds down the template, with each horizontal row representing a clock cycle or two bus samples. Each row represents 4 ns at 500 MHz or 3.75 ns at 533 MHz.

1.1 Clk Cyc Column

The first column, labeled clock cycles, represents the time in clock cycles since the beginning of this template.

1.2 BE Column

The 2nd column labeled BE, is the state of the BusEnable pin during that clock cycle. BusEnable is only used to send serial addresses to the RDRAM.

1.3 BC Column

The 3rd column labeled BC, is the state of the BusCtrl pin during that clock cycle. BusCtrl is used to send request packets, strobe, terminate and wakeup information. During a request packet, this fields identifies the request number, so requests and data can be tracked, the request type, and the value of the Pend field for that transaction. For wakeup, strobes, and terminates it also indicates which transaction is being started, strobed and terminated, by the value carried with it, i.e. (strobe **0**)

1.4 BD[**8**:**0**] Column

The 4th column, labeled BD[**8**:**0**], is the state of the BusData wires during that clock cycle. During the data packet it indicates the transaction number and the octbyte being sent or received. During request packets it indicates the state of the control bits Open and Close. These bits are used to tell the RDRAM what core operations to perform. The state that is assumed for the bank being accessed and the addressed bank is also included in the last field of a request packet.

1.5 DRAM Internal State Columns

The 5th through 9th Columns represent the activity in an RDRAM labeled **0**, with the 5th column being it's CAS activity, and the next four being the activity or state of each of the 4 banks (Bank[**0**:**3**]). The 10th through 14th Columns represent the activity in any other RDRAM, labeled **1**, with the 10th column being it's CAS activity, and the next four being the activity or state of each of the 4 banks (Bank[**0**:**3**]).

1.6 Column Encoding

The column encodings consist of two numbers. The first is the request number. The second is the octbyte number.

1.7 Bank[**0**:**3**] Encodings

These columns include a symbol that represents an operation and the number of the transaction that caused the operation. The meaning of the symbols is given in the table below.

Symbol	Name	Meaning	Length
p	Precharge	Precharge is the closing of a page (deassertion of RAS) and can be caused by closing at the end of a transaction, or opening a page that has not previously been precharged	8 Clocks
s	Sense	Sense is the operation of loading the sense amps to prepare for a CAS and is caused by a command with Open required	8 Clocks
r	RAS	RAS always follows the sense, and is needed to insure that the minimum RAS low time of the core is met.	8 Clocks

Vary data size, retirement order, outstandig requests, data time

Clk				!0	Bank				!1	Bank			!
Cyc	BE	BC	BD [8:0]	!Col	0	1	2	3	!Col	0	1	2	3 !
0	----	wakeup 0	------------	----	---	---	---	---	----	---	---	---	---
1	----	------------	------------	----	---	---	---	---	----	---	---	---	---
2	----	------------	------------	----	---	---	---	---	----	---	---	---	---
3	----	------------	------------	----	---	---	---	---	----	---	---	---	---
4	----	req 0	no-open	----	---	---	---	---	----	---	---	---	---
5	----	read	no-close	----	---	---	---	---	----	---	---	---	---
6	----	pend 1	sensed 0	----	---	---	---	---	----	---	---	---	---
7	----	------------	------------	----	---	---	---	---	----	---	---	---	---
8	0 1	wakeup 1	------------	----	---	---	---	---	----	---	---	---	---

-continued

9	0 1	-------------	-------------	----	---	---	---	---	----	---	---	---	---
10	0 1	strobe 0	-------------	----	---	---	---	---	----	---	---	---	---
11	0 1	-------------	-------------	0 0	---	---	---	---	----	---	---	---	---
12	----	req 1	no-open	0 0	---	---	---	---	----	---	---	---	---
13	----	read	no-close	0 0	---	---	---	---	----	---	---	---	---
14	----	pend 2	sensed 0	0 0	---	---	---	---	----	---	---	---	---
15	----	term 0	turn	0 1	---	---	---	---	----	---	---	---	---
16	----	-------------	data 0 0	0 1	---	---	---	---	----	---	---	---	---
17	----	-------------	data 0 0	0 1	---	---	---	---	----	---	---	---	---
18	----	-------------	data 0 0	0 1	---	---	---	---	----	---	---	---	---
19	----	-------------	data 0 0	----	---	---	---	---	----	---	---	---	---
20	1 1	wakeup 2	data 0 1	----	---	---	---	---	----	---	---	---	---
21	1 1	-------------	data 0 1	----	---	---	---	---	----	---	---	---	---
22	1 1	strobe 1	data 0 1	----	---	---	---	---	----	---	---	---	---
23	1 1	-------------	data 0 1	1 0	---	---	---	---	----	---	---	---	---
24	1 2	req 2	no-open	1 0	---	---	---	---	----	---	---	---	---
25	1 2	read	no-close	1 0	---	---	---	---	----	---	---	---	---
26	1 2	pend 3	sensed 0	1 0	---	---	---	---	----	---	---	---	---
27	1 2	-------------	turn	1 1	---	---	---	---	----	---	---	---	---
28	1 3	-------------	data 1 0	1 1	---	---	---	---	----	---	---	---	---
29	1 3	-------------	data 1 0	1 1	---	---	---	---	----	---	---	---	---
30	1 3	-------------	data 1 0	1 1	---	---	---	---	----	---	---	---	---
31	1 3	-------------	data 1 0	1 2	---	---	---	---	----	---	---	---	---
32	----	-------------	data 1 1	1 2	---	---	---	---	----	---	---	---	---
33	----	-------------	data 1 1	1 2	---	---	---	---	----	---	---	---	---
34	----	-------------	data 1 1	1 2	---	---	---	---	----	---	---	---	---
35	----	term 1	data 1 1	1 3	---	---	---	---	----	---	---	---	---
36	----	-------------	data 1 2	1 3	---	---	---	---	----	---	---	---	---
37	----	-------------	data 1 2	1 3	---	---	---	---	----	---	---	---	---
38	----	-------------	data 1 2	1 3	---	---	---	---	----	---	---	---	---
39	----	-------------	data 1 2	----	---	---	---	---	----	---	---	---	---
40	----	wakeup 3	data 1 3	----	---	---	---	---	----	---	---	---	---
41	----	-------------	data 1 3	----	---	---	---	---	----	---	---	---	---
42	----	-------------	data 1 3	----	---	---	---	---	----	---	---	---	---
43	----	-------------	data 1 3	----	---	---	---	---	----	---	---	---	---
44	----	req 3	open	----	---	---	---	---	----	---	---	---	---
45	----	read	no-close	----	---	---	---	---	----	---	---	---	---
46	----	pend 5	sensed 0	----	---	---	---	---	----	---	---	---	---
47	----	-------------	-------------	----	---	---	---	---	----	---	---	---	---
48	----	wakeup 4	-------------	----	---	---	---	---	----	---	---	---	---
49	----	-------------	-------------	----	---	---	---	---	----	---	---	---	---
50	----	strobe 2	-------------	----	p3	---	---	---	----	---	---	---	---
51	----	term 2	-------------	2 0	p3	---	---	---	----	---	---	---	---
52	----	req 4	no-open	2 0	p3	---	---	---	----	---	---	---	---
53	----	read	no-close	2 0	p3	---	---	---	----	---	---	---	---
54	----	pend 0	sensed 0	2 0	p3	---	---	---	----	---	---	---	---
55	----	-------------	turn	----	p3	---	---	---	----	---	---	---	---
56	----	-------------	data 2 0	----	p3	---	---	---	----	---	---	---	---
57	----	-------------	data 2 0	----	p3	---	---	---	----	---	---	---	---
58	----	strobe 4	data 2 0	----	s3	---	---	---	----	---	---	---	---
59	----	term 4	data 2 0	----	s3	---	---	---	4 0	---	---	---	---
60	----	-------------	-------------	----	s3	---	---	---	4 0	---	---	---	---
61	----	-------------	-------------	----	s3	---	---	---	4 0	---	---	---	---
62	----	-------------	-------------	----	s3	---	---	---	4 0	---	---	---	---
63	----	-------------	turn	----	s3	---	---	---	----	---	---	---	---
64	----	-------------	data 4 0	----	s3	---	---	---	----	---	---	---	---
65	----	-------------	data 4 0	----	s3	---	---	---	----	---	---	---	---
66	----	strobe 3	data 4 0	3 0	r3	---	---	---	----	---	---	---	---
67	----	term 3	data 4 0	3 0	r3	---	---	---	----	---	---	---	---
68	----	-------------	-------------	3 0	r3	---	---	---	----	---	---	---	---
69	----	-------------	-------------	3 0	r3	---	---	---	----	---	---	---	---
70	----	-------------	-------------	3 0	r3	---	---	---	----	---	---	---	---
71	----	-------------	turn	----	r3	---	---	---	----	---	---	---	---
72	----	-------------	data 3 0	----	r3	---	---	---	----	---	---	---	---
73	----	-------------	data 3 0	----	r3	---	---	---	----	---	---	---	---
74	----	-------------	data 3 0	----	---	---	---	---	----	---	---	---	---
75	----	-------------	data 3 0	----	---	---	---	---	----	---	---	---	---

What is claimed is:

1. A method of operation in a memory device that includes a plurality of memory cells, the method comprising:
 - receiving a command to sample data;
 - deferring sampling a first portion of the data until an external strobe signal is detected; and
 - sampling the first portion of the data from an external signal line in response to detecting the external strobe signal.

2. The method of claim 1, wherein the first portion of the data is sampled synchronously with respect to an external clock signal.

3. The method of claim 2, further comprising sampling a second portion of the data synchronously with respect to the external clock signal, wherein the first portion of the data is sampled during an odd phase of the external clock signal, and the second portion of the data is sampled during an even phase of the external clock signal.

4. The method of claim 3, wherein the first and second portions of the data are both sampled during a first clock cycle of the external clock signal.

5. The method of claim 1, further comprising:

detecting an external terminate signal; and

sampling additional portions of the data during a time interval between detection of the external strobe signal and detection of the external terminate signal.

6. The method of claim 1, wherein the external strobe signal is detected using an external clock signal.

7. The method of claim 1, wherein the command to sample data comprises a write operation code bit.

8. The method of claim 1, wherein the command to sample data is included in a write request packet.

9. The method of claim 1, wherein the command to sample data comprises:

precharge information that specifies whether to precharge sense amplifiers used in storing the first portion of the data in the plurality of memory cells; and

address information that specifies where to store the first portion of the data.

10. The method of claim 1, further comprising:

detecting an external terminate signal; and

sampling additional portions of the data during a plurality of clock cycles of an external clock signal that elapse between detection of the external strobe signal and detection of the external terminate signal.

11. A method of controlling a memory device that includes a plurality of memory cells, the method comprising:

issuing a first write command to the memory device, the memory device being configured to defer sampling data that corresponds to the first write command until a strobe signal is detected;

delaying for a first time period after issuing the write command; and

after delaying for the first time period, issuing the strobe signal to the memory device to initiate sampling of a first portion of the data by the memory device.

12. The method of claim 11, further comprising issuing the first portion of the data and a second portion of the data to the memory device, wherein the first portion of the data is sampled during an odd phase of an external clock signal, and the second portion of the data is sampled during an even phase of the external clock signal.

13. The method of claim 12, wherein the first and second portions of the data are both issued during a common clock cycle of the external clock signal.

14. The method of claim 11, further comprising:

issuing additional portions of the data to the memory device; and

issuing a terminate signal to the memory device to signal to the memory device to stop sampling data.

15. The method of claim 11, further comprising sampling data from another memory device during the first time period, wherein the data sampled from the other memory device corresponds to a read operation.

16. The method of claim 11, wherein the first write command is included in a write request packet.

17. The method of claim 11, further comprising:

issuing a terminate signal to the memory device; and

issuing additional portions of the data to the memory device during a plurality of clock cycles of an external clock signal that elapse between issuance of the strobe signal and issuance of the terminate signal.

18. The method of claim 11, further comprising issuing a second write command to another memory device during the first period.

19. A memory device having a plurality of memory cells, the memory device comprising:

a plurality of input receiver circuits to receive a write command and sample data that corresponds to the write command in response to detecting a strobe signal that is delayed relative to the write command by a first time period.

20. The memory device of claim 19, further comprising a clock generator circuit coupled to the plurality of input receiver circuits, the clock generator circuit receiving an external clock signal wherein the data is sampled synchronously with respect to the external clock signal.

21. The memory device of claim 19, wherein the plurality of input receiver circuits sample a first portion of the data and a second portion of the data, wherein the first portion of the data is sampled during an odd phase of an external clock signal, and the second portion of the data is sampled during an even phase of the external clock signal.

22. The memory device of claim 21, wherein the first and second portions of the data are both sampled during a first clock cycle of the external clock signal.

23. The memory device of claim 19, wherein the plurality of input receiver circuits receive additional portions of the data before detection of a terminate signal.

24. The memory device of claim 19, wherein the plurality of input receiver circuits further receive:

precharge information that specifies whether to precharge sense amplifiers used in storing the data that corresponds to the write command; and

address information to identify where to store the data.

25. The memory device of claim 19, wherein the strobe signal is detected synchronously with respect to an external clock signal.

26. The memory device of claim 19, wherein the first time period elapses during an interval spanning a plurality of clock cycles of an external clock signal.

* * * * *

UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

In the Matter of **RAMBUS INC.,** **a corporation.**	**Docket No. 9302**

CERTIFICATE OF SERVICE

I, James M. Berry, hereby certify that on July 28, 2003, I caused a true and correct copy of *Request for Official Notice of Various United States Patents; Order Granting Respondent Rambus Inc.'s Request For Official Notice Of Various United States Patents* to be served on the following persons by hand delivery:

Hon. Stephen J. McGuire Chief Administrative Law Judge Federal Trade Commission, Room H-112 600 Pennsylvania Avenue, N.W. Washington, D.C. 20580	M. Sean Royall, Esq. Deputy Director, Bureau of Competition Federal Trade Commission, Room H-372 600 Pennsylvania Avenue, N.W. Washington, D.C. 20580
Donald S. Clark, Secretary Federal Trade Commission, Room H-159 600 Pennsylvania Avenue, N.W. Washington, D.C. 20580	Malcolm L. Catt, Esq. Attorney Federal Trade Commission 601 New Jersey Avenue, N.W. Washington, D.C. 20001
Richard B. Dagen, Esq. Assistant Director, Bureau of Competition Federal Trade Commission 601 New Jersey Avenue, N.W. Washington, D.C. 20001	

James M. Berry

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