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WP2005-08
September 1, 2005

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In the mid-1990s, measured productivity growth for the semiconductor industry showed a pickup that coincided with an economy-wide acceleration in labor productivity growth. This pickup in semiconductor markets stems from an increase in the growth of real output that was, in turn, generated by what Dale Jorgenson (2001) called an “inflection point” in the price indexes for the semiconductor industry. Jorgenson further hypothesized that the inflection point reflected increases in the rate of product innovation made possible by an increase in Moore's Law, a stylized description of technology that currently states that the number of electrical components on a chip will double every eighteen months. Within semiconductors, microprocessors (MPUs) produced by Intel—the world's largest producer of the chips that serve as a computer's central processing unit—were the primary contributor to both the trend and inflection point in this price index in the 1990s.

Pricing and product cycles for Intel's chips also changed in the mid-1990s. As shown in the top panel of figure 1, price contours for Intel's chips became steeper around 1995. Because most price index formulae boil down to functions of weighted averages of price change, steeper price contours translate directly into more rapidly declining price indexes. Hence, the inflection point reflects the change in the contours seen beginning in 1995. At the same time, the product cycle for MPUs—the length of time chips are sold in the market—shortened and Intel began to introduce chips more frequently. This is

seen in the lower panel, where horizontal lines depict the lifespans for Intel's chips, plotted against the speed of the chip.

What caused these changes in pricing and product cycles? This paper provides a stylized model that shows a set of conditions under which an increase in Moore's Law is consistent with both of these stylized facts. In the model, an increase in Moore's Law raises the quality of future chips relative to today's chips. Under the assumption that consumers view these chips as substitutes, increases in the quality of tomorrow's chips push down the prices for today's chips and can, thus, generate an inflection point in the price index. With regard to product cycles, the model predicts that increases in the rate of product introductions and reductions in chips' market lives can simply be a monopolist's profit-maximizing response to an exogenous increase in Moore's Law.

Thus, the model provides support for the Moore's Law hypothesis. However, because substitution possibilities are the lever that generate these predictions, the model also suggests that changes in the attributes of *contemporaneous* substitutes can have the same effects. Thus, the model suggests that increases in the quality of competitor's chips can generate an inflection point through the same channel. This is an important possibility to consider because Intel came under increasing competition from AMD beginning in the mid-1990s, and the model suggests that this increase in competition could have contributed to the observed inflection point.

I. Price Contours and Inflection Points

A simple stylized model is developed to explore these possibilities. Quality is exogenously determined and evolves exponentially so that the quality of a chip

introduced at time t is $Q(t)=e^{qt}$. But, there are fixed costs incurred when a chip is introduced (I^c) so that chips are introduced only occasionally. For simplicity, it is assumed that the firm produces only one chip at a time and that all of its chips live for A periods, so that over some period of length M , $C=M/A$ chips are introduced. Under these assumptions, the quality level associated with chip $c=0,1,..C$ is $Q(c) = e^{q(Ac)}$, since (Ac) periods transpire between the introduction of chip $c=0$ and that of chip c .

The price that consumers are willing to pay for chip c aged a periods is given by:

$$(1) \quad P_{c,a} = P(Q) e^{-sa}$$

where $0 < s < 1$ is the slope of the (logged) price contour. Note that, in this context, a constant-quality price index declines at the rate s over time so that changes in prices that feed through $P(Q)$ only affect the level of the prices and do not affect the rate of price change. Therefore, in this context, an inflection point requires a change in the slope of the price contours. Thus, if the slope is specified as a function of the pace of quality change, $s=s(q)$, where increases in q make the contours steeper: $\partial s(q)/\partial q > 0$, then, an increase in q can generate an inflection point. Algebraically, this occurs because older chips experience sharper price declines than younger chips so that the price contours pivot when q changes: $\partial \ln P_{c,a} / \partial q = -(\partial s / \partial q)(a)$.

Consider two arguments to support the notion that changes in Moore's Law can generate inflection points. First, suppose that MPU markets are populated by heterogeneous buyers and that Intel engages in inter-temporal price discrimination—it sells first to those with a high willingness-to-pay, then sequentially lowers prices to sell to those with lower willingness to pay. As explained by Joel Dean (1969):

“Launching a new product with a high price is an efficient device for breaking the market up into segments that differ in price elasticity of demand. The initial high price serves to skim the cream of the market that is relatively insensitive to price. Subsequent price reductions tap successively more elastic sectors of the market. This pricing strategy is exemplified by the systematic succession of editions of a book, sometimes starting with a \$50 limited personal edition and ending up with a 25-cent pocket book.” (P. 174)

In this view, an increase in q causes price contours to pivot because buyers of older chips are more sensitive to the presence of substitutes than the early adopters.

The alternative argument—that does not require consumer heterogeneity—is that prices of older chips are more sensitive than those of new chips simply because older chips are “closer” to the available substitutes. So, for example, the inter-temporal substitution between today and tomorrow’s chips is more intense as the new chip’s arrival nears. This is, thus, one way to explain why prices for older chips—those closer in time to the arrival of the new chip—are lower than prices for newer chips. Moreover, it suggests that increases in q will cause price contours to pivot because substitution intensifies as the good gets “closer” to its substitutes.

II. A Simple Model

To assess conditions under which an increase in Moore’s Law can shorten product cycles and increase introduction rates, it is necessary to use the model to assess how increases in q affect the firm’s profit-maximizing choices for the length of market lives and the number of product introductions. To that end, assume that the rapidly declining

prices discussed above force the firm to produce at capacity. This is consistent with anecdotal evidence for this industry and has been used in previous models of the semiconductor industry (e.g., Ken Flamm (1989)). The other assumption is that capacity and, hence, output is fixed over time. This assumption is admittedly problematic because there are thought to be important learning economies for semiconductors, especially for devices sold in highly competitive markets (notably, memory chips). However, industry data suggests that learning effects are less important for MPUs (Aizcorbe(2002)).

The firm's problem is to choose the number of chips to introduce (and thus the length of each chip's market life) over the M periods so as to maximize profits over that period. To form an expression for profits over the M periods, note that the price contours above imply the following expression for revenues collected over the life of each chip c:

$$R_c = \int_a P(Q) \tilde{y} e^{-sa} = P(Q) \tilde{y} (1 - e^{-sA}) / s .$$

where \tilde{y} denotes the (fixed) per-period output level. Defining the effect of quality on each chip's price as $P(Q) = P_o e^{qAC}$, total revenues from all chips produced in the M periods may be written as:

$$\begin{aligned} R_M &= \int_c P_o e^{qAC} \tilde{y} (1 - e^{-sA}) / s \\ &= P_o \tilde{y} ((1 - e^{qAC}) / qA) (1 - e^{-sA}) / s \end{aligned}$$

The assumption that increasing the life of each chip necessarily involves reducing the number of chips introduced over the M periods is imposed by restating e^{-qAC} as e^{qM} so that total revenues is given by : $R_M = P_o \tilde{y} ((1 - e^{qM}) / qA) (1 - e^{-sA}) / s$. Finally, noting the per-chip introduction cost, I_c , and using $C=MA$ to restate the problem in terms of chip introductions, one obtains an expression for profits over the M periods:

$$\Pi_M = \{ P_o \tilde{y} ((1 - e^{qM}) / qM) (C) (1 - e^{-sM/C}) / s \} - I_c C .$$

The optimal C^* maximizes this expression. The first-order condition says that profits are maximized when the marginal revenue of adding an additional chip just equals the marginal cost of doing so: $MR(C)=MC(C)$. Algebraically, the first-order condition is:

$$(P_0 \tilde{y}(1-e^{qM})/qM)(1-e^{-sM/C})/s = (P_0 \tilde{y}(1-e^{qM})/qM)(Me^{-sM/C}/C) + I_c$$

The left-hand side measures marginal revenue: the new revenue obtained from producing an additional chip, measured, literally, as the average revenue per chip over all chips. It is readily shown that marginal revenue is a decreasing function of C (i.e., $\partial MR/\partial C < 0$). The right-hand side gives the attendant costs of increasing the number of chips to be introduced over M : the first term is the foregone revenue from not allowing chips to live as long and the second term is the introduction cost. It may be shown that marginal cost is increasing in C — $\partial MC/\partial C > 0$ —which ensures that the second-order conditions are met.

Surprisingly, the first order conditions do not include a term to measure changes in revenue that occur when introducing more chips alters the amount of time between introductions (AC) and, thus, changes the quality levels associated with each chip. This is because—through integration—the term that captures quality effects— $(1-e^{qM})/qM$ —is an average of the quality effect over all periods. Because the time period is fixed (at M), the average quality level does not change with changes in the number of introductions.

III. Effects of an Increase in Moore's Law

The model predicts that an increase in Moore's Law (q) will prompt a monopolist to increase the number of chips introduced over the period. Tracing through this effect, an increase in q steepens price contours and pushes down prices of all the chips. This

lowers the marginal revenue of adding more chip introductions because all chips now sell at a lower price ($\partial MR(C)/\partial q < 0$). However, the prices of older chips fall disproportionately more than those of younger chips, so that marginal cost falls more than marginal revenue ($\partial MC(C)/\partial q < \partial MR(C)/\partial q$). With marginal revenue exceeding marginal cost at the new q , the firm returns to equilibrium by increasing chip introductions until the first order condition is satisfied. In effect, the increase in q lowers the cost of product introductions and, thus increases the incentive for the firm to introduce more chips. The end result is a new equilibrium where more chips are introduced over the M periods and where each chip has a shorter market life.

Extending the model to allow for the possibility that “waiting” is a negative attribute of future chips yields similar results, except that the effect on the length of the product cycle is magnified. With waiting as an attribute, the slope of the price contours may be written: $s = s(q, W(a, A))$ and increases in q generate an inflection point through a second channel: the increase in q prompts the firm to increase the number of introductions and reduce the length in each chip’s market life, the reduction in A reduces the waiting time until new chips are introduced, $W(A)$, which, in turn, lowers the price that consumers are willing to pay for today’s chip.

IV. Increased Competition from AMD

In this simple framework, factors that change the slope of price contours can generate an inflection point. The lever that generates this result is the presence of the *inter-temporal* substitute: tomorrow’s chip. One might ask, then, whether changes in the attributes of *contemporaneous* substitutes can generate similar effects. If consumers view

the chips produced by competitors—like AMD—and Intel chips as substitutes, then the quality of the AMD chip becomes one of the determinants of the price contours for Intel's chips: $s=s(Q^{AMD},q,W(a,A))$. Following the logic used above, an increase in the quality of the AMD chip has both direct and indirect effects. First, the increase in Q^{AMD} directly pivots the price contours, as older chips are viewed as closer substitutes to the (lower quality) AMD chips so that those prices fall further in response to competition than prices for newer chips. This, in and of itself, would create an inflection point. Second, facing steeper price contours, the cost associated with introducing chips is lower and Intel responds by introducing more chips until the first-order condition is met. This increase in the number of chips to be introduced over M , implies shorter market lives for each chip which, in turn, implies shorter waiting time until new chips arrive in the market. If “waiting” treated as a negative attribute for tomorrow's chip, the reduction in waiting times further pivots Intel's price contours. The end result is the same as with an increase in Moore's Law: a new equilibrium where price contours are steeper, the price index has an inflection point, product introduction rates are higher and each chip's market life is shorter.

IV Conclusions

This paper constructs a stylized model that illustrates conditions under which an increase in Moore's Law can (i) generates an inflection point in the MPU price index and (ii) could have prompted Intel to increase the rate of product introduction and shorter each chips' product cycle. However, the assumptions required to generate this result suggest that an increase in competition can generate the same results. Because these competing explanations have different implications for the sustainability of the increase

in productivity growth, future work is needed to study these possibilities in a more rigorous fashion.

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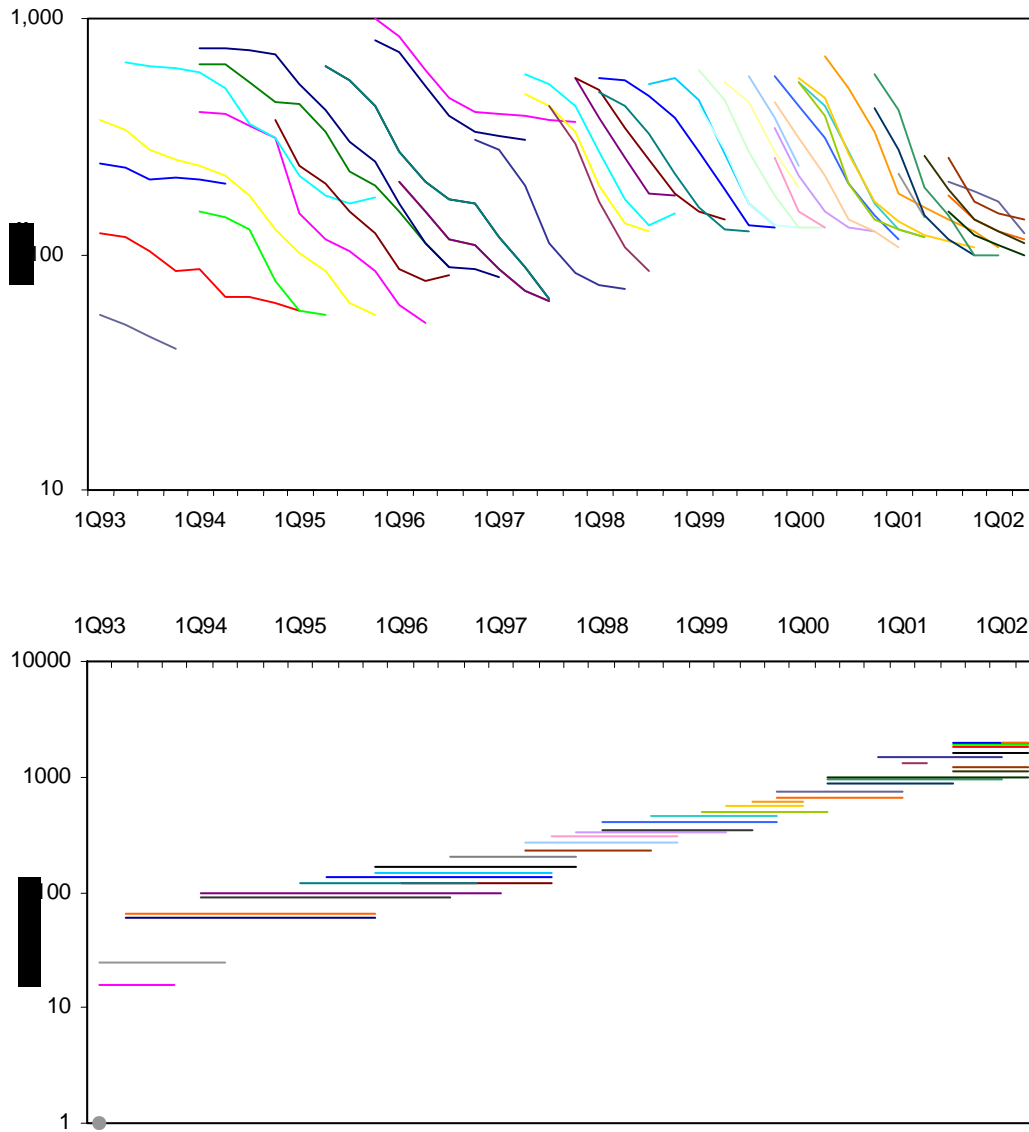
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Footnotes

¹ This is a shortened and revised version of Aizcorbe (2004). I wish to thank Sam Kortum for his comments as discussant at the NBER Productivity Workshop and from all that I have learned from our subsequent collaboration on these issues (Aizcorbe and Kortum (2004)). I also wish to thank Marshall Reinsdorf and seminar participants at the Bureau of Economic Analysis, the Brookings Institution and the New York Federal Reserve Bank for helpful comments.

Figure 1
Price Contours and Product Cycles for Intel Desktop MPUs, 1993-2002



Source: Aizcorbe (2004)