

Technology Profile Fact Sheet

Title: Low Cost Single Die-level Plating Process for Integrated Circuits

Aliases: None.

Technical Challenge: To develop a large volume single die-level plating process for the packaging of Integrated Circuits (IC) without the need for expensive electroplating equipment.

Description: Currently, the standard aluminum pads found on chips must be processed with an appropriate under bump metallization (UBM) to seal the pads from corrosion and prepare them for soldering. This new process demonstrates that large volume die-level and wafer-level plating can be done without the need for electroplating. During trial runs, a group of die (up to 50 at current capabilities) could be plated in less than one day as compared to a week and half for a wafer-level electroplating process. The aluminum bond pads can now receive solder without the need for wafers, masks, several lithography steps, sputtered metal deposition, or electroplating. Using this technology more than 1200 die have been successfully plated with a yield greater than 98%.

Demonstration Capability: A demonstration is not currently available.

Potential Commercial Application(s): The microelectronics packaging industry, national laboratories, and universities are potential places for commercial applications.

Patent Status: A patent application has been filed with the USPTO.

Reference Number: 1402