OSD RDT&E BUDGET ITEM JUSTIFICATION (R2 Exhibit)

Date: February 2006

APPROPRIATION/ BUDGET ACTIVITY	PE NUMBER AND TITLE
RDT&E/ Defense Wide BA# 1	**0601111D8Z - Government/Industry Co-sponsorship of University Research**

Cost ($ in Millions)		FY 2005	FY 2006	FY 2007	FY 2008	FY 2009	FY 2010	FY 2011
Total Program Element (PE) Cost		6.530	10.038	0.000	0.000	0.000	0.000	0.000
P111	Government/Industry Co-sponsorship of University Research	6.530	10.038	0.000	0.000	0.000	0.000	0.000

A. Mission Description and Budget Item Justification: (U) Program co-funds research efforts with DARPA's Focus Research Center Program in FY 2006 (FY 2006 funding reflects a Congressional increase for Focus Center Research Program).
(U) Program is a shared commitment between industry and Government to sponsor next generation semiconductor electronics research via the Government/Industry Co-sponsorship of University Research (GICUR) program. It capitalizes on university-based research, education and training in technologies of strategic importance to national defense and also to industry. It provides an emphasis on ground-breaking research with a long-term horizon, and education and training in selected research areas which are vital to advancement of technologies. The commitment is a jointly formed pool of funding (requiring an industry match of at least one-to-one) and a shared management structure for sponsoring this sort of long-term basic research at universities. This provides the military with early access to leading-edge technologies and concepts as well as reduces vulnerabilities of industries involved, increases long-term technical growth in these areas, and infuses new ideas and approaches, all of which are important for long-term national security. Industry and government share responsibility for research focus area selection and overall direction. Mechanisms have been established for personnel exchange and interactions to provide for continuing education of highly qualified researchers already working in leading edge and emerging S&T. One of the areas emphasizes basic concepts for DoD needs in high frequency applications such as component technologies for advanced radars, millimeter/microwave communications and radiometry, with special focus on high performance semiconductor technologies. The major areas of research are nanoscale electronic materials, new device structures, advanced interconnects, and robust circuit design approaches. The program supports both graduate and undergraduate research assistants; thereby assisting in the development of the future S&T workforce in these technical areas.

B. Program Change Summary	FY 2005	FY 2006	FY 2007
Previous President's Budget (FY 2006)	6.838	0.000	0.000
Current BES/President's Budget (FY 2007)	6.530	10.038	0.000
Total Adjustments	-0.308	10.038	0.000
Congressional Program Reductions			
Congressional Rescissions			
Congressional Increases		10.038	
Reprogrammings	-0.126		
SBIR/STTR Transfer	-0.168		
Other	-0.014		

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C. Other Program Funding Summary: Not Applicable.

D. Acquisition Strategy: Not Applicable.

E. Performance Metrics:

FY	Strategic Goals Supported	Existing Baseline	Planned Performance Improvement / Requirement Goal	Actual Performance Improvement	Planned Performance Metric / Methods of Measurement	Actual Performance Metric / Methods of Measurement
06						

Comment: Performance in the GICUR Program is monitored at several levels, individual level, focus center level, and overall program level. This research program is jointly funded between the Government and the Semiconductor industries. At the lowest level of the performer, efforts are tracked using project technical milestones that have been appropriately defined and agreed upon. In addition, published papers, conference presentations, and talks at industrial and government organizations are also used to gauge effectiveness of progress of individual efforts. Programmatic and technical milestones are also maintained at the Center level, and the interaction among the current five centers is tracked. Interactions between Centers and DoD labs and industrial organizations are also tracked. In addition, periodic technical and management reviews are conducted with the Centers to gauge progress and provide guidance. Industrial, government, and academic experts are invited to attend these reviews. At the program level, DARPA tracks major deliverables and examines the transition of technologies and ideas from the Center for development in other DARPA programs. DARPA looks at the numbers and impacts of GICUR core technologies that have moved from this program to other programs or to sponsorship by other organizations. Surveys with industry and government experts are used to understand impact and/or potential of individual technologies.

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Cost ($ in Millions)		FY 2005	FY 2006	FY 2007	FY 2008	FY 2009	FY 2010	FY 2011
P111	Government/Industry Co-sponsorship of University Research	6.530	10.038	0.000	0.000	0.000	0.000	0.000

A. Mission Description and Project Justification: (U) Program is a shared commitment between industry and Government to sponsor next generation semiconductor electronics research via the Government/Industry Co-sponsorship of University Research (GICUR) program. It capitalizes on university-based research, education and training in technologies of strategic importance to national defense and also to industry. It provides an emphasis on ground-breaking research with a long-term horizon, and education and training in selected research areas which are vital to advancement of technologies that are critically important to future defense platforms.

(U) Program co-funds efforts under DARPA's Focus Research Center Program (FY 2006 funding is a Congressional add for the Focus Center Research Program).

B. Accomplishments/Planned Program:

Accomplishment/Planned Program Title	FY 2005	FY 2006	FY 2007
Focus Center Program:	6.530	10.038	0.000

FY 2005 Accomplishments: The Focus Center Program has demonstrated new technologies that will provide new capabilities in the design and fabrication of semiconductor devices and integrated circuits. In the Gigascale Design Center, a design methodology for obtaining low power but high performance processors was developed using a robust checking circuit that corrects errors in a very low voltage core processor. A design roadmap was implemented to guide future technologies by enabling the accurate modeling and simulation of "what-if" experiments and scenarios on the complex semiconductor technology process. The concepts of platform-centric design were translated from the digital domain to the analog/mixed signal regime and work to formalize the approach was initiated. In the Interconnect Focus Center, the integration of optical materials with silicon were demonstrated. Optical links were developed and measurements of power consumption and bit-error rate were collected. Experiments with nanotubes were conducted, leading to the development and refinement of accurate models of transient performance, including parasitic reactances. In the Center for Circuits Solutions, robust design methodologies for enabling computation with unreliable or faulty components were investigated and interfaces were defined. In addition, applications of fin field effect transistors (finFETs) were investigated, including dynamic and dc properties. Under the Materials, Structures, and Devices Center, experiments with carbon nanotubes and the integration of nanotubes with silicon circuits were conducted. Measurements of mobility were performed and methods to form good contacts using metallics were developed. In addition, experiments were conducted to quantify how film strains and new materials will provide carrier mobility enhancements for very short channel transistors. In the Functional Electronic Nano-Architectures Center, advances in understanding the chemistry of certain polymeric materials enabled development of a process for creating a novel polymeric memory cell that would have significant low power and low fabrication cost and could be scaled to nano-scale dimensions.

FY 2006 Plan: The Gigascale Design Center, will continue to design methodologies for obtaining low power but high performance processors using a robust checking circuit that corrects errors in a very low voltage core processor. The design roadmap will continue to guide tuture technologies by enabling the accurate modeling and simulation of "what-if" experiments and senarious on the complex semiconductor technology process. The concepts of platform-centric design translated from the digital domain to the analog/mixed gignal regime and work to formalize the design approach will be continued. Design approaches for heterogeneous circuits operating under extreme conditions will also be developed. In the InterconnectFocus Center, the integration of optical materials with silicon will continue to be explored and demonstrated. Optical links will continue to be developed and measurements of power consuption and bit-error rate will continue to be collected. Experiments with nanotubes will continue, leading to the

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development and refinement of accurate models of transient performance, including parasitic reactances. In the Center of Circuits Solutions, robust design methodologies for enabling computation with unreliable or faulty components will continue to be investigated and interfaces will continue to be defined. In additiona, applications of fin field effect transistors (finFETs) will be investigated, including dynamic and dc properties and analog operation. Under the Materials, Structures, and Devices Center, experiments with carbon nanotubes and the integration of nanotubes with silicon circuits will continue to be conducted. Measurements of mobility will be performed and methods to form good contacts using metallics will continue to be developed. In addition, experiments will continue to be conducted to quantify how film strains and new materials will provide carrier mobility enhancements for very short channel transistors. In the functional Electronic Nano-Architectures Center, continued advances in understanding the chemistry and physics of nanoscale materials and devices will be coupled to computational architectures to better gauge metrics for new technologies.

C. Other Program Funding Summary: Not Applicable.

D. Acquisition Strategy: Not Applicable.

E. Major Performers

Category	Name	Location	Type of Work and Description	Award Date
Labs				
	DARPA	Arlington, VA	Provided for the Government/Industry Co-sponsorship of University Research in microelectronics.	17 DEC 2004