

SEMATECH

PROGRESS AND PROSPECTS

REPORT OF THE
ADVISORY COUNCIL ON
FEDERAL PARTICIPATION
IN SEMATECH

1989

SEMATECH

PROGRESS AND PROSPECTS

REPORT OF THE ADVISORY COUNCIL ON FEDERAL PARTICIPATION IN SEMATECH

CHAIRMAN

Dr. Robert B. Costello
Under Secretary for Acquisition
Department of Defense

REPORT DIRECTED BY

Robert Ortner
Under Secretary for
Economic Affairs
Department of Commerce

AUTHOR

Jeffrey L. Mayer
Director (Acting)
Office of Economic Policy
Department of Commerce

POLICY AND RESEARCH SUPPORT

Robert G. McKibben
Jane W. Molloy
Gerald Moody
K. Peter Wagner

Printed in the United States of America

3rd Printing 1989

Questions about this publication can be directed to the
U.S. Department of Commerce, Office of Economic Policy
at (202) 377-1727.

This report is submitted on behalf of the Advisory Council on Federal Participation in SEMATECH. As required by law, the report provides an assessment of the progress of SEMATECH in its first year of operation.

Established by the National Defense Authorization Act for Fiscal Years 1988 and 1989, and further directed by the Omnibus Trade and Competitiveness Act of 1988, the Advisory Council is charged with reviewing SEMATECH operations and assessing continued federal participation.

EXECUTIVE SUMMARY

SEMATECH

SEMATECH is a consortium of 14 U.S. semiconductor makers and the Department of Defense aimed at achieving global leadership in semiconductor manufacturing technology by 1993. The consortium will develop advanced manufacturing technology and transfer this technology to its members.

SEMATECH's members include both "merchant" and "captive" firms (i.e., firms that manufacture semiconductors mainly for sale and firms that manufacture mainly for their own use). Budgets are projected at roughly \$200 million a year for the period 1989-93, half to be provided by the member companies, and half by federal, state, and local government. DOD funding for SEMATECH totalled \$100 million in FY 1988 and a similar amount for FY 1989. Additional funding and in-kind benefits offered to the consortium as location incentives by the University of Texas, the State of Texas, and the City of Austin are valued at \$68 million over the life of the program.

SEMATECH is a non-profit corporation, barred by its charter from producing semiconductors for sale. The consortium's only product will be generic technology--i.e., new knowledge about how to make semiconductors rather than knowledge about specific chip designs. SEMATECH is the acronym for SEMiconductor MANufacturing TECHNOlogy.

Strategic Objectives

- o Developing and Disseminating Advanced Manufacturing Technology. SEMATECH's strategic plan calls for high-yield, factory-scale application of 0.35-micron production technology in SEMATECH's own fabricating facility ("fab") by 1993--an estimated six to twelve months ahead of leading foreign chipmakers, and three years ahead of most U.S. merchant firms (without SEMATECH).* The resulting commercial advantage for SEMATECH's members could be substantial.

* The number of circuits that can be traced on the surface of a semiconductor chip depends partly on the width of the circuit paths. Chips with 0.35-micron circuit widths are at least two product generations more advanced than today's leading-edge mass-produced chips, which have circuit widths in the 0.8-micron range. A micron is one millionth of a meter.

- o Strengthening the Supplier Base. SEMATECH will provide a framework and incentives for closer cooperation between U.S. chipmakers and their U.S. suppliers, and among the suppliers themselves. The consortium will interact with U.S. materials and equipment firms through SEMI/SEMATECH, an independent chapter of the international Semiconductor Equipment and Materials Institute (SEMI).
- o Strengthening the Technology Base. Working through the Semiconductor Research Corporation (SRC), SEMATECH will finance about \$10 million in research at U.S. universities and federal laboratories to generate new technical knowledge and build the national stock of electronics science and engineering expertise.
- o Supporting National Security. SEMATECH's own purposes are chiefly commercial. The consortium will bolster U.S. military strength primarily by contributing to a strong U.S. electronics industry.

Operating Objectives

SEMATECH will implement its R&D strategy in three related phases, all now under way:

- o Phase I. SEMATECH's immediate (1989) objective is to demonstrate capacity for high-yield, factory-scale production of two devices incorporating 0.8-micron manufacturing technology--i.e., 4Mb DRAMs and 64K SRAMs.*
- o Phase II. SEMATECH plans to begin factory-scale application of 0.5-micron manufacturing technology in 1990. Equipment and materials for the consortium's second generation fab line will be developed and supplied, where possible, by U.S. companies, and should be competitive in performance and cost with the world's best.
- o Phase III. At Phase III, SEMATECH's operating and strategic targets merge. The main goal in each case is world leadership in technologies required for low-cost manufacture of semiconductors with 0.35-micron circuitry by 1993.
- o Subsequent Phases. SEMATECH's planning horizon has been formally extended to 10 years. The 1989 Operating Plan sets planning for Phase IV and Phase V as a 1989 operating objective. Both efforts are projected for the 1990s.

* DRAMs and SRAMs (dynamic and static random access memory chips) are standard-design, high-volume products used mainly in computers. SRAMs are faster than DRAMs and require manufacturing technology that can be used for various semiconductor devices. 4Mb DRAMs store 4 million bits, or 4 megabits (Mb) of information. 64K SRAMs store 64,000 bits, or 64 kilobits (K) of information.

Operating Modes

SEMATECH has adopted three basic operating modes for achieving Phase II and Phase III manufacturing technology objectives:

- o Leveraging and Networking. The consortium will contract for technology R&D with suppliers, the federal labs, and universities on a cost-sharing basis.
- o Accelerated Learning. Accelerated learning in the development and application of advanced manufacturing equipment, materials, and processes is the core of SEMATECH's enterprise--the means by which it will compress development schedules for achieving high-yield production of advanced devices.
- o Technology R&D. To identify the most promising technology paths to Phase II and III objectives, SEMATECH consulted the collective expertise of scientists and engineers from industry, government, and academe in a series of technology workshops during 1987 and 1988. R&D priorities for 1989 will include all major areas of lithographic technology, etch and deposition processes and equipment, and manufacturing systems.

Technology Transfer

Schedules for the development and formal delivery of manufacturing technology to members of the consortium are embedded in SEMATECH's strategic and operating plans. Also, member companies will be able to consult their Austin assignees in areas of special concern. Rotating assignees will carry technical and practical knowledge back to parent firms. Teams of member-company engineers will train on SEMATECH production lines, or advisory teams may be sent out from Austin to support member companies on their home turf. SEMATECH has also taken steps to control excessively rapid dissemination of consortium-developed technology to foreign competitors--e.g., limiting membership in the consortium to U.S. firms. Technology patented by SEMATECH may later be licensed to non-members.

Progress in 1988

By the close of 1988, SEMATECH had made significant progress toward Phase I objectives and established elements of the groundwork for Phases II and III. Construction of a state-of-the-art fab had been completed in less than half the time normally needed to build such facilities. All equipment for Phase I had been ordered; most had arrived in Austin; and partial wafer processing had begun. The consortium had also used its extensive advisory apparatus to develop consensus R&D agendas for Phase II/III and establish six university-based research projects.

SEMATECH's most important accomplishments in 1988, however, probably had less to do with meeting operational goals than with the difficult and occasionally contentious work of self-definition:

- o Expanding the Consortium's Strategic Focus. Some early proposals for SEMATECH focused on the manufacture of standard-design memory chips, using present-generation process technology. During 1988, however, consortium planners expanded this strategic vision to include increased emphasis on flexible manufacturing of special application chips (ASICs), and accelerated development of commercially feasible X-ray technology.
- o Developing a Detailed Operating Plan and a Disciplined Planning Process. At the beginning of 1988, DOD shifted project responsibility for SEMATECH to the Defense Advanced Research Projects Agency (DARPA). DARPA, in turn, called for greater specificity on R&D timetables, responsibilities, and costs in the consortium's 1988 Operating Plan. A new plan--the 1989 Operating Plan--submitted on December 1, 1988 has received DARPA's full approval. In subsequent years, updates of SEMATECH's operating plan will be prepared each March for consideration in the federal budget cycle.
- o Increasing the Amount and Efficiency of R&D Spending. SEMATECH has trimmed projected labor and P&E costs, cutting back projected employment from 750 to 650 and deciding against construction of a new fab for Phase II of the project, while increasing the R&D share of consortium spending, setting clear R&D project priorities, and putting more stress on leveraged financing of off-site projects. Forty percent (\$104 million) of the consortium's scheduled spending commitment in CY 1989 will go for leveraged off-site R&D.
- o Building Members' Commitment. Senior SEMATECH officials contend that member commitment grew over the year "from casual to urgent." A major reason for this change, according to CEO Robert Noyce, was the federal decision to participate in the project and resulting industry confidence in SEMATECH's durability. Other explanations include the consortium's sprouting physical presence on the Austin landscape.
- o Improving Supplier Relations. Spokesmen for SEMATECH and SEMI/SEMATECH seem to agree that by creating a framework and incentives for communication, SEMATECH has succeeded in founding a more open and cooperative relationship with suppliers. In addition, some suppliers appear to have made preliminary plans to locate R&D and production facilities in Austin.

Issues for Consideration in Future Advisory Committee Reports

In its next annual report, the Advisory Council should be able to evaluate SEMATECH's progress in relation to all Phase I objectives and to Phase II/III contracting and early contract performance goals. The 1990 report should also be able to gauge the continuing strength of member commitment to the project (e.g., as reflected in the quality of assignees), and whether recent improvements in chipmaker-supplier relations have been sustained (e.g., by fairness and an open exchange of information in the Phase II/III contracting process).

Additional areas for future consideration include: (i) the potential for technology transfer to foreigners inherent in the existing system of international business alliances in both the chipmaking and vendor industries; (ii) the ability and willingness of U.S. firms to translate leadership in manufacturing technology into increased market strength, especially by reentering the world DRAM market; and (iii) the possibility that foreign industry-government programs paralleling SEMATECH may neutralize the consortium's effect on U.S. industrial competitiveness.

FEDERAL PARTICIPATION IN SEMATECH

Experience in 1988 should help to allay concern that DOD funding may lead to the subordination of SEMATECH's commercial objectives to specific defense production needs. Early tensions between DARPA and SEMATECH on the issues of production flexibility, planning discipline, and project leadership/industry commitment were largely resolved by late summer. At yearend, DARPA officials were pleased with SEMATECH's overall progress.

ALTERNATIVE MODES OF FEDERAL PARTICIPATION

At least two civilian agencies--the Department of Energy and the Commerce Department's National Institute of Standards and Technology--have the authority and technical expertise to join or supplant DOD in funding and managing the SEMATECH project. Neither, however, has unprogrammed resources that it could easily commit to the project. A decision to alter the current funding and oversight structure, therefore, would entail either the reprogramming of currently planned civilian-agency expenditures, a shift of resources from DOD, or an increase in the federal budget. It might also require basic adjustments in priorities and operating modes of the civilian agencies. In addition, any joint oversight arrangement would make federal management more cumbersome.

CONCLUSIONS AND RECOMMENDATIONS

The Council has considered three policy matters: (i) whether federal participation in SEMATECH should continue and in what form; (ii) SEMATECH's early lessons about industry-government efforts to increase U.S. commercial strength; and (iii) an agenda for the newly-created National Advisory Committee on Semiconductors.

Funding and Management.

The Advisory Council recommends continuation of federal funding for SEMATECH at the present \$100-million level in FY 1990. It is too soon to consider altering the terms of federal participation based on anything the consortium has done or failed to do. Moreover, a withdrawal of federal support now would seriously limit SEMATECH's operations and prospects for success.

The Council further recommends against any shift or division in project funding responsibilities. SEMATECH has scored important preliminary successes and developed a cooperative working relationship with DARPA. In contrast to possible civilian alternatives, DARPA has both the financial and technical resources to perform its current role. DARPA also has a strong institutional interest in SEMATECH's success, in part because of the agency's emphasis on the development of dual-use technology, but also because a commercially strong semiconductor industry is critical to U.S. military strength.

SEMATECH as a model.

Discussions of consortia to promote U.S. competitive strength in areas other than semiconductors (e.g., superconductivity, high definition television) often cite "the SEMATECH model." As a model, however, SEMATECH should be treated with care. Characteristics of the SEMATECH case that have contributed to the consortium's early progress may not be present in all cases--e.g., a widely-shared belief in the importance of a strong semiconductor industry to national military and economic strength; the existence of a large and resourceful U.S. industry and active involvement of the industry's largest firms; clear technology objectives that are far enough removed from the product end of the R&D spectrum to allow members to cooperate, yet near enough to be practically useful in a commercially significant time-frame; and skillful oversight by a federal agency vested in the project's commercial objectives. Absent such factors, the problems of creating and operating consortia probably increase.

Areas for Further Policy Consideration

SEMATECH is a national project, not a national policy. Even if the consortium were a complete success in its own terms, major issues now affecting the competitiveness of U.S. chipmakers would remain--e.g., limited marketing opportunities at home and abroad, and a range of tax, antitrust, and trade policy issues. In addition, the United States would still trail the Japanese and Europeans in developing technologies necessary for competitive leadership in semiconductors in the late 1990s--e.g., X-ray lithography. These economic and technology policy issues should be considered by the newly-formed National Advisory Committee on Semiconductors.

CONTENTS

INTRODUCTION

<u>SEMATECH</u>	1
<u>THE ADVISORY COUNCIL</u>	1
<u>REASONS FOR SEMATECH</u>	2
(1) THE EROSION OF U.S. MARKET STRENGTH	2
(2) THE SPECTER OF CONTINUING DECLINE	3
(3) THE THREAT TO NATIONAL SECURITY	3
(4) THE NEED FOR A CONSTRUCTIVE RESPONSE TO FOREIGN INDUSTRIAL STRATEGIES.....	4
<u>HOW MOST SEMICONDUCTORS ARE MADE</u>	4
<u>THE IMPORTANCE OF HIGH-YIELD PRODUCTION</u>	5
<u>SEMATECH'S OPERATING FOCUS</u>	6

PART I

SEMATECH'S OBJECTIVES AND PROGRESS TOWARD ACHIEVING THEM IN 1988

A. <u>STRATEGIC OBJECTIVES</u>	7
(1) DEVELOPMENT AND DISSEMINATION OF ADVANCED MANUFACTURING TECHNOLOGY	7
(2) STRENGTHENING THE SUPPLIER BASE--FINDING "A NEW WAY TO DO BUSINESS"	8
(3) STRENGTHENING THE TECHNOLOGY BASE	9
(4) NATIONAL SECURITY OBJECTIVES	10
(5) SEMATECH IS NOT A NATIONAL POLICY FOR SEMICONDUCTORS	11
B. <u>OPERATING OBJECTIVES</u>	11
(1) PHASE I	12
(a) <u>Targets</u>	12
(b) <u>Vehicles</u>	12
(c) <u>Why Do Phase I At All?</u>	13

(2)	PHASE II	13
(a)	<u>Targets</u>	13
(b)	<u>Tactics</u>	13
	(i) <u>Leveraging and Networking</u>	14
	(ii) <u>Accelerated Learning</u>	14
	(iii) <u>Technology Research and Development</u>	16
(c)	<u>Technology Transfer</u>	17
	(i) <u>Mechanisms of Technology Transfer</u>	18
	(ii) <u>Translating Technology Gains into Competitive Advantages for American Firms</u> ..	18
(3)	PHASE III	19
(4)	SUBSEQUENT PHASES	19
C.	<u>PROGRESS IN 1988</u>	19
(1)	MOVEMENT TOWARD PHASE I OBJECTIVES	20
	(a) <u>Fab Construction</u>	20
	(b) <u>Technology Transfer</u>	20
(2)	MOVEMENT TOWARD PHASE II AND III OBJECTIVES	20
(3)	MOVEMENT IN OTHER AREAS	21
	(a) <u>Expansion of the Consortium's Strategic Focus: More emphasis on Production Flexibility and Long-Range R&D</u>	21
	(b) <u>Developing A Detailed Operating Plan and a Disciplined Planning Process</u>	22
	(c) <u>Increasing the Amount and Efficiency of R&D Spending</u>	22
	(d) <u>Building Members' Commitment</u>	22
	(e) <u>Improving Supplier Relations</u>	23
D.	<u>ISSUES FOR CONSIDERATION IN FUTURE ADVISORY COMMITTEE REPORTS</u>	24
(1)	MEETING TECHNOLOGY R&D AND TECHNOLOGY TRANSFER OBJECTIVES	24
(2)	SUSTAINING MEMBER SUPPORT	24
(3)	STRENGTHENING THE VENDOR BASE	24
(4)	CONTROLLING TECHNOLOGY TRANSFER	25
(5)	EFFECTS ON THE COMPETITIVENESS OF U.S. CHIPMAKERS ..	25
(6)	TRACKING FOREIGN INITIATIVES	26

PART II

FEDERAL PARTICIPATION IN SEMATECH:
DESCRIPTION AND ASSESSMENT

A. DOD/DARPA 27
 (1) CONCERNS ABOUT DOD FUNDING AND OVERSIGHT 27
 (2) DOD/DARPA APPROACH TO PROJECT OVERSIGHT 28
B. THE NATIONAL LABORATORIES 29
C. THE NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY 30
D. THE ADVISORY COUNCIL 30

PART III

ALTERNATIVE MODES OF FEDERAL
PARTICIPATION

A. CIVILIAN AGENCIES THAT COULD SHARE OR SUPPLANT
DOD'S ROLE IN SEMATECH 31
 (1) DOE NATIONAL LABORATORIES 31
 (2) NIST ADVANCED TECHNOLOGY PROGRAM 32
 (3) NSF 33
B. RECOUPMENT 33

PART IV

CONCLUSIONS AND RECOMMENDATIONS

A. CONTINUED FEDERAL PARTICIPATION IN SEMATECH 35
B. SEMATECH AS A MODEL FOR FUTURE COOPERATIVE
EFFORTS -- SOME EARLY LESSONS 36
C. AREAS FOR FURTHER POLICY CONSIDERATION 37

NOTES

INTRODUCTION

SEMATECH

SEMATECH is a consortium of 14 U.S. semiconductor makers and the Department of Defense aimed at achieving global leadership in semiconductor manufacturing technology by 1993. The consortium will develop advanced manufacturing technology and transfer this technology to its members.

SEMATECH's members include both "merchant" and "captive" firms (i.e., firms that manufacture semiconductors mainly for sale and firms that manufacture mainly for their own use), each assessed a percentage of sales and each with a vote on the consortium's Board.¹ Budgets are projected at roughly \$200 million a year for the period 1989-93, half to be provided by the member companies, and half by federal, state, and local government.² DOD funding for SEMATECH totalled \$100 million in FY 1988 and a similar amount for FY 1989. Additional funding and in-kind benefits offered to the consortium as location incentives by the the University of Texas, the State of Texas, and the City of Austin are valued at \$68 million over the life of the program.³

SEMATECH is a not-for-profit membership corporation, barred by its charter from the commercial sale of semiconductor products, and prohibited under its by-laws from considering matters related to the development, marketing and pricing of semiconductor products by individual members. The consortium's only product will be generic technology--i.e., new knowledge about how to make semiconductors rather than knowledge about specific chip designs. "SEMATECH" is the acronym for SEMiconductor MANufacturing TECHNOlogy.

A Memorandum of Understanding (MOU) between SEMATECH and the Defense Department allows DOD to use technology developed by the consortium in the same manner as any consortium member and to transfer such technology to contractors in connection with DOD requirements, but not for wider commercial use.

THE ADVISORY COUNCIL

The legislation authorizing DOD funding for SEMATECH (P.L.100-180) also created an Advisory Council on Federal Participation in the project. Chaired by the Under Secretary of Defense for

Acquisition, and otherwise composed of federal officials and private citizens from outside the defense community, the Council is empowered to advise SEMATECH periodically on its research agenda, and to report annually to the Secretary of Defense and various committees of the Congress on SEMATECH's progress.

The Omnibus Trade and Competitiveness Act of 1988 (P.L. 100-418) elaborates this reporting responsibility by requiring the Council to: (i) assess SEMATECH's performance in relation to its technological, commercial, and national security goals; (ii) describe and assess federal participation in SEMATECH; (iii) identify possible alternative modes of federal participation and funding; and (iv) consider related policy issues. Parts I-IV of this report address these issues.

REASONS FOR SEMATECH

SEMATECH is the product of two key developments: increased cooperation of major semiconductor firms among themselves and with their suppliers, and the federal decision to share project costs. These developments, in turn, have four major causes:

(1) THE EROSION OF U.S. MARKET STRENGTH

Between 1981 and 1986, U.S. merchant semiconductor manufacturers saw their world market share decline from 57 percent to 43 percent. Deterioration in memory chip markets was especially severe; by 1986, only two U.S. merchant firms were still making dynamic random access memory chips (DRAMs). Upstream, the effects were comparable. Between 1982 and 1987, the world market share of U.S. equipment makers fell from 70 percent to 59 percent. The leading beneficiaries of U.S. losses in both cases were Japanese.⁴

Problems of the U.S. chipmakers and their domestic suppliers are partly a result of major downswings in world-wide demand. U.S. merchant producers lost an estimated \$2 billion in 1985-86. Effects of the downturn on U.S. equipment suppliers were lagged and magnified. Sales by U.S. chipmakers fell about 7.5 percent in 1985, and then began to pick up. U.S. equipment sales were off marginally in 1985; in 1986, however, they fell 25 percent.⁵

Japanese semiconductor firms also sustained major losses in 1985-86. By keeping capacity in use and pricing aggressively, however, they emerged from the experience with a strengthened market position. In addition, though capital spending by Japan's chipmakers fell briefly in 1986, the cutbacks were selective. Purchases of Japanese-made equipment held fairly steady; while purchases from U.S. suppliers, joint ventures, and others fell sharply.⁶

U.S. chipmakers and their suppliers have also been hurt by non-cyclical developments--by growing import penetration of the U.S. electronic equipment market, by the atrophy of U.S. consumer electronics manufacturing, and by the inability of U.S. semiconductor firms to increase their share of the large and growing Japanese market.

In addition, some observers suggest that if U.S. merchant firms and their U.S. suppliers were larger, more integrated, and better financed they would be more able to weather hard times, make large investments in advanced manufacturing capability, and speed product development cycles for equipment and devices. Others contend that the qualities of innovativeness and entrepreneurship that propelled U.S. device and equipment firms to market dominance in the 1970s are of less value today when many chips and manufacturing tools are more standardized, advanced technology is widely available, and competitive success depends increasingly on manufacturing excellence.⁷

(2) THE SPECTER OF CONTINUING DECLINE

The fear that U.S. chipmakers and their suppliers may fall permanently behind their Japanese competitors stems in part from comparative investment trends. In the 1982-86 period, capital spending by U.S. merchant semiconductor firms averaged about 15 percent of sales, compared with more than 30 percent for Japanese firms; R&D spending by U.S. merchant firms averaged about 12 percent of sales, compared with about 14 percent for the Japanese. Absolute amounts of R&D spending in the two countries were relatively similar.⁸

More importantly, the evidence shows that Japanese firms have outspent and outperformed their U.S. rivals in key areas of manufacturing process R&D and capital equipment development. A 1986 study by the National Research Council found that U.S. producers held a contested edge in three areas of current semiconductor process technology. But Japanese firms had recently moved ahead in a fourth (optical lithography), and held early leads in seven areas of emerging technological importance, including X-ray lithography and compound semiconductor applications. The reviewers noted that work in these areas was underway in at least 10 Japanese firms at a level matched by only two U.S. companies.⁹

(3) THE THREAT TO NATIONAL SECURITY

U.S. military forces depend heavily on superior technology, especially in electronics, to offset the quantitative advantages of potential adversaries. From a defense perspective,

therefore, continued economic and technological decline in the U.S. semiconductor industry poses vexing short- and long-term problems. The immediate issue is growing U.S. dependence on foreign sources for state-of-the-art weapons components--in the judgment of the Defense Science Board (DSB), "an unacceptable situation." A more ominous possibility, however, is that decline in the U.S. semiconductor industry may ultimately undermine the competitive and technological leadership of U.S. computer and communications equipment makers.¹⁰

(4) THE NEED FOR A CONSTRUCTIVE RESPONSE TO FOREIGN INDUSTRIAL STRATEGIES

SEMATECH also reflects a growing concern in U.S. policy circles that foreign export-oriented industrial development strategies have damaged a succession of U.S. industries in addition to semiconductors and semiconductor manufacturing equipment--e.g., steel, automobiles, machine tools, construction equipment, bearings, ceramics. Japanese business-government-academic alliances have been the most prominent and expert practitioners of export-oriented industrial development. But the Japanese approach has been widely copied by industrializing countries in Asia and South America. The Europeans, with mixed success, have experimented with industrial strategies of their own.

Whether these efforts prove to be successful in financial terms, they have the potential to weaken the United States economically and militarily. The challenge for federal policymakers is to blunt this potential without injury to long-term U.S. trade liberalization objectives. Observers have suggested that the SEMATECH model--i.e., federally sponsored pre-competitive industry cooperation--may be one answer to this problem.

HOW MOST SEMICONDUCTORS ARE MADE

Most semiconductors are built, hundreds at a time, on thin, flat, highly polished "wafers" of ultra-pure and structurally uniform silicon. Though the order of process steps varies, basic processes and tools are common to all high-volume chip production.

- o Lithography. An oxide film is deposited on each wafer, followed by a coating of light-sensitive "photoresist." Ultra-violet light focused through a glass template, or "mask," then projects minute circuit patterns on the resist. To ensure clarity, only a few copies of each image can be exposed on the resist at a time; so the projection machine, or "stepper," must move and repeat the process again and again over the entire wafer surface.

- o Etching. Next, the circuit patterns are developed and removed, exposing the oxide undercoating. Reactive gases or chemical solutions etch the oxide away, opening circuit paths on the surface of the silicon "substrate."
- o Ion Implantation. Bombardment of the wafer surface with a high energy beam of "dopant" atoms--e.g., arsenic or boron--alters the crystal structure of the exposed silicon, raising its conductivity. To produce complex circuits, the oxidation/lithography/etch cycle is repeated as many as 20 times. Each successive circuit segment must be aligned precisely with all the rest.
- o Attaching Circuit Contacts. Near the end of the process, a metal film is deposited and patterned to interconnect the circuit components and provide contact areas for external leads.
- o Testing, Dicing, and Assembly. Once the contacts are in, an electronic probe tests each device on the wafer surface and marks defective ones with a spot of ink. Then the wafers are sliced into single chips and the inked devices discarded. Survivors are inspected microscopically, given protective casings and external leads, retested, and shipped.

SEMATCH will focus on "front end" steps of the production process, beginning with the polished wafer and ending with the probe test of devices on wafer surface.

THE IMPORTANCE OF HIGH-YIELD PRODUCTION

Because defective circuits cannot be identified and discarded until late in the process and wafer processing is expensive, competitive production depends on getting a high percentage of usable devices--i.e., a high "yield"--from each wafer. In early factory production of complex devices, yields can be as low as 10 or 15 percent. As manufacturing experience grows, however, yields improve to 80 percent or more.

High-yield production of advanced semiconductors requires large volumes of pure material, manufacturing atmospheres that are almost perfectly clean, and tools and processes that are precisely controlled and contamination-free. Impure material, defective photomasks, stepper misalignment, air-borne particles in the fabricating plant ("fab"), contaminants generated by the manufacturing equipment itself--anything that impairs precise imaging and etching of circuit patterns or prevents regular modification of the silicon surface in each circuit path--can ruin a chip and raise production costs.

SEMATECH'S OPERATING FOCUS

In 1989, SEMATECH will install and demonstrate capacity for high-yield, factory-scale production of advanced dynamic and static random access memory chips--i.e., DRAMs and SRAMs. DRAMs and SRAMs are standard-design, high-volume products used chiefly in computers. DRAMs are used primarily for main memory. SRAMs, which are faster but have less storage capacity, provide quick-access cache memory. In addition, SRAMs require manufacturing technology that can be used to make a variety of other semiconductor devices.

The latest generation of factory-made DRAMs can store more than four million bits--i.e., four megabits (4Mb)--of information. Because their circuitry is more complex, leading-edge SRAMs store only about 256,000 bits (256K) of information. A bit of information is either a "1" or a "0" in the binary language of computers. In each product generation, memory circuit densities quadruple, production processes grow more complex, and tooling becomes more expensive.

Circuit paths in 4Mb DRAMs measure less than a millionth of a meter (i.e., one micron) across. At 16Mb, geometries shrink to 0.5 microns, and at 64Mb to 0.35 microns--smaller than the finest level of detail that can be seen clearly with a high-powered light microscope. IBM and several Japanese firms are now lab testing 16Mb DRAMs and designing 64Mb chips.

PART I

SEMATECH'S OBJECTIVES AND PROGRESS TOWARD
ACHIEVING THEM IN 1988

This section discusses SEMATECH's phased strategic and operating objectives, considers the consortium's accomplishments in 1988, and flags issues for consideration in future reports.

A. STRATEGIC OBJECTIVES

SEMATECH has three fundamental purposes: (i) to develop and transfer advanced manufacturing technology, thereby providing important commercial advantages to U.S. semiconductor manufacturers; (ii) to strengthen the semiconductor industry's supplier base; and (iii) to strengthen the national electronics technology base. By achieving these goals, SEMATECH will also generate important national security benefits.

(1) DEVELOPMENT AND DISSEMINATION OF ADVANCED
MANUFACTURING TECHNOLOGY

SEMATECH aims at developing the machinery, processes, and materials needed to give member companies "the capability of achieving a world-leadership manufacturing position by the mid-1990s."¹ The consortium's strategic plan calls for high-yield, factory-scale application of 0.35 micron production technology in SEMATECH's own fab by 1993--an estimated six to twelve months ahead of leading foreign chipmakers.

Memory chips incorporating 0.35-micron production technology are at least two product generations more advanced than the most advanced memory devices now manufactured in the United States and Japan--e.g., 4Mb DRAMs. In the past, new generations of such devices have appeared roughly every two-and-a-half years.² If this pattern continues, as experts predict, the world's leading-edge chipmakers will begin factory-scale production of chips incorporating 0.5-micron technology (e.g., 16Mb DRAMs) by 1991, and factory-scale production of devices incorporating 0.35-micron technology (e.g., 64Mb DRAMs) in 1993. Private forecasters suggest that, discounting the impact of SEMATECH, most U.S. merchant firms are unlikely to be comfortable with 0.35-micron technology until 1996.³

If SEMATECH achieves its main R&D objectives, therefore, it will enable each of its members to apply 0.35-micron production technology in a factory setting before any of them--even the very largest--might have applied this technology alone, and before the most advanced foreign producers are expected to apply it. The resulting commercial advantage for SEMATECH's members could be substantial. World-wide competition in the semiconductor industry is intensely time-dependent; six-month production leads are considered substantial.

(2) STRENGTHENING THE SUPPLIER BASE--FINDING
"A NEW WAY TO DO BUSINESS"

Signs of weakness in the semiconductor industry's U.S. supplier base include the equipment makers' declining market share, the slow start that U.S. equipment and chipmakers have made in developing production technology for future-generation devices, and the virtual eclipse of an American-based and -owned materials industry.⁴

Business practices by the supplier industry itself are partly to blame for these developments.⁵ However, the most powerful causes of industry weakness are structural. The U.S. supplier industry has been marked from birth by fragmentation and by estrangement from its principal market.

Of an estimated 500 U.S.- and foreign-owned equipment makers now operating in the United States, only a handful are multi-line firms with annual sales above \$50 million. Many more are one-product companies; and most have sales below \$10 million.⁶ Small size limits the staying power of these firms in the face of wide demand swings and rising R&D costs.

U.S. chipmakers have traditionally kept their suppliers at arm's length, preferring "cooperation with [performance] specs" to co-development and testing of equipment, partly at least to protect proprietary circuit designs. Compared with captive equipment makers in integrated Japanese and European electronics firms, U.S. equipment makers lack the advantages of predictable internal markets, access to broad scientific expertise, and deep pockets for high-cost R&D.⁷ They also lack the opportunity for joint development and internal site testing of new equipment, and the benefit of systematic high-quality feed-back on product performance.

SEMATECH is an effort to compensate for some of these structural disadvantages--to change the way the equipment firms and their customers do business. It will lower the cost and increase the efficiency of supplier R&D. It will promote

cooperation within the supplier base by contracting R&D to multi-company teams. It will provide a structure and incentives for regular and open communication among supplier firms, and between suppliers and SEMATECH members. It will advance the start point and accelerate the process of equipment development by giving suppliers complete information on performance standards and production objectives at the beginning of the development cycle, and by "de-bugging" and "proofing-in" equipment prototypes at the end of the cycle. It will also spur sales of proven equipment to member companies.

Bringing U.S. chipmakers and their U.S. suppliers closer together, not only within the SEMATECH framework but in general, should measurably strengthen the supplier base. Equipment firms should be quicker to market with new products and more responsive to customers' cost and quality needs. Related signs/sources of strength would include U.S. firms regaining parity, then leadership, in key production technologies and market segments (e.g., microlithography) or reentering abandoned markets. A stronger supplier base would probably also have larger firms, less turn-over of industry membership, even higher average rates of R&D spending, and more teaming on major R&D projects.

SEMATECH will interact with U.S. equipment and materials firms through SEMI/SEMATECH--an independent chapter of the international Semiconductor Equipment and Materials Institute (SEMI), limited to U.S.-owned firms. SEMI/SEMATECH's principal missions are to aid communication and cooperation between its members and SEMATECH, and to ensure that its members "receive a fair, open, cooperative, and competitive opportunity to participate in the program."⁸ SEMI/SEMATECH's Chairman is a member of SEMATECH's Board of Directors.

(3) STRENGTHENING THE TECHNOLOGY BASE

SEMATECH addresses three technology base issues: (i) building the stock of national expertise in electronics science and production engineering; (ii) generating new technical knowledge for SEMATECH's Phase III production program, and beyond; and (iii) tapping and channeling the commercial potential of research facilities at U.S. universities, the national labs, and other institutions.

To accomplish the first two goals, SEMATECH will build on existing strengths of the Semiconductor Research Corporation (SRC), allocating about \$10 million annually for SRC-managed research.⁹ SRC will place and monitor contracts for research on SEMATECH's out-year production problems at university-based

Centers of Excellence (COE). By-products of these contracts should be improved curricula and increased student interest in electronics science and engineering.

SEMATECH's most immediate impact on the nation's research base, however, may be to establish priorities and mobilize resources--especially resources of the federal laboratories--in support of commercial objectives.¹⁰ These results should follow, first, from the broad involvement of the U.S. electronics science and engineering community in establishing SEMATECH's research agenda and, second, from the consortium's decision to contract directly for technology development with the national laboratories and selected universities teamed with vendor companies.

(4) NATIONAL SECURITY OBJECTIVES

SEMATECH's own purposes are primarily commercial. Its main contribution to national security results from the importance of a strong domestic electronics industry to U.S. military strength and political influence.

The national security rationale for federal sponsorship of SEMATECH is partially explained in the DSB report on Defense Semiconductor Dependency. According to the DSB, though DOD purchases absorb only a fraction of U.S. semiconductor output, only competitive strength in the U.S. industry at large can assure military access to state-of-the-art supplies on a continuing basis. From a defense acquisitions perspective, moreover, the issue is not simply assured supply but access to production efficiencies through increased reliance on commercially strong "dual-use" manufacturing capacity.¹¹

DOD will also be free to use SEMATECH-developed manufacturing technology in its own chipmaking facilities and to transfer such technology to defense contractors, on condition that it not be used for commercial purposes. SEMATECH members who are also DOD contractors may already have assimilated this technology and exploited its cost, quality, and production flexibility benefits.¹²

Another piece of the national security rationale for SEMATECH is that strength in the semiconductor industry can help to prevent erosion in the competitive and technological leadership of U.S. computer and communications equipment firms. In the DSB's view, such erosion would have "profound implications for the Department of Defense." Others have noted as well that technological superiority in semiconductors, computers, and other R&D-intensive industries translates directly into military advantage--e.g., into technological leadership in

weaponry and command and control systems. It also supports the nation's ability to project influence by non-military means.¹³

In a more general sense, SEMATECH also contributes to national security by supporting a healthy and growing economy able to meet the cost of America's world-wide security obligations.¹⁴

(5) SEMATECH IS NOT A NATIONAL POLICY
FOR SEMICONDUCTORS

Even if SEMATECH achieved all of its technology goals, major issues now affecting the competitive position of U.S. chip-makers would remain--e.g., continued Japanese resistance to U.S. semiconductor imports; atrophy in the nation's consumer electronics industry; foreign penetration of U.S. electronic equipment markets; and an array of tax, regulatory, and trade policy issues.

Moreover, the United States would still trail its major industrial rivals in the development of technologies considered vital to competitive leadership in semiconductors in the late 1990s --e.g., lithographic sources, compound semiconductor processing, optoelectronic integrated circuits, and three-dimensional device structures.

These economic and technological issues are likely to be considered by the newly-formed National Advisory Committee on Semiconductors (NACS), which will advise the President and Congress on a national semiconductor competitiveness strategy, including national research priorities.

A fair assessment of SEMATECH's performance must focus on projected outcomes that are within the consortium's control. These outcomes have to do mainly with accelerated development and dissemination of advanced manufacturing technology. Since a high proportion of semiconductor manufacturing technology is embedded in manufacturing equipment and materials, however, SEMATECH should also have a direct and visible impact on the economic health of U.S. supplier industries. Other outcomes that are within the consortium's control include improving the efficiency of defense production and strengthening the nation's technology base, though these results may be less visible and take longer to assess.

B. OPERATING OBJECTIVES

SEMATECH will implement its R&D strategy in three related phases, all now under way.

(1) PHASE I

(a) Targets

SEMATECH's immediate (1989) objective is to demonstrate capacity for high-yield, factory-scale production of 4Mb DRAMs and 64K SRAMs on a single fabrication line. The consortium's Austin fab began partial processing of SRAMs at the end of November 1988, with full-line production now projected for the second quarter of 1989. Full-line production of DRAMs should begin in the fourth quarter. One reason for the staggered start is that while 64K SRAMs and 4Mb DRAMs can be made on the same line, the former require fewer machines and fewer process steps. In essence, Phase I "clones" existing AT&T 64K-SRAM and IBM 4Mb-DRAM production lines, using commercially available equipment and materials.

(b) Vehicles

AT&T and IBM have contributed SEMATECH's Phase-I "manufacturing demonstration vehicles" (MDV)--64K SRAM and 4Mb DRAM devices--along with the engineering support needed to get the Austin fab into operation quickly.¹⁵

SEMATECH will not make semiconductors for sale. The main function of devices selected for production at each phase of the project is to drive the development of manufacturing technology, and to provide a vehicle for the demonstration and refinement of this technology. Application of the technology for commercial purposes is left to individual member firms.

The choice of Phase-I MDVs reflects the range of SEMATECH's technological objectives. Historically, DRAM production has driven manufacturing technology in the semiconductor industry, in part because of the commodity nature of DRAM products and the competitive pressure to market chips of ever-higher density. Also, because memory devices are thousand- or million-fold repetitions of identical circuit segments and their interconnections, they permit tighter process control and faster yield improvement than more complex devices that exhibit variable interactions among circuit segments.

Phase I MDVs also give SEMATECH the opportunity to demonstrate and develop flexible manufacturing capability. The consortium's production line will use a modular architecture that allows for the manufacture of DRAMs, SRAMs, or logic chips with only minor changes in process sequence. Also, AT&T's SRAM uses a process technology designed for making other kinds of circuits-- e.g., logic chips, microprocessors, and application-specific integrated circuits (ASICs).¹⁶

According to industry observers, AT&T's and IBM's contribution of SEMATECH's Phase I MDVs will allow the consortium to begin manufacturing with 0.7- and 0.8-micron technology six months to a year ahead of U.S. merchant firms. SEMATECH's fab will be using machinery geared for high-volume production but on a small manufacturing scale. The Austin plant will turn out hundreds of wafers a day compared with the thousands now produced at IBM's 4Mb-DRAM facility. However, SEMATECH considers its production targets more than sufficient to achieve rapid process learning.¹⁷

(c) Why Do Phase I At All?

Because leading U.S. chipmakers already use 0.7- and 0.8-micron production technology, some industry experts have questioned the need for Phase I. SEMATECH's view is that Phase I will establish a benchmark for measuring the consortium's common technological achievements. Phase I is also a discipline for rapid start-up--an occasion to create and drill an organizational team; and an opportunity to establish and season working relationships with vendors, the R&D community, and DOD.

In addition, important elements of Phase I process technology will carry over to Phase II. The Phase I fab line will process 6-inch wafers, but tooling will be compatible with 8-inch wafers. SEMATECH's 4Mb-DRAM production sequence incorporates lithographic processes and circuit interconnect methods that meet Phase II requirements. Important 64K-SRAM process technologies are also transferable to Phase II.¹⁸

(2) PHASE II

(a) Targets

SEMATECH plans to begin factory-scale production of semiconductor devices incorporating 0.5-micron technology--e.g., 16Mb DRAMs or comparably complex devices--in 1990. To the extent possible, equipment and materials for the consortium's second generation fab line will be developed and supplied by U.S. companies, and will be competitive in performance and cost with the world's best. Chips will be processed on 8-inch wafers, and yield rates will match levels normally achieved by the most efficient U.S. plants much later in the product cycle.

(b) Tactics

SEMATECH has adopted three basic operating modes for achieving Phase II and Phase III manufacturing technology objectives: (i) leveraging and networking, (ii) accelerated learning, and (iii) technology research and development. (Phase III objectives are discussed on p. 19, below)

(i) Leveraging and Networking

The need to "leverage and network" is dictated partially by SEMATECH's large research mission and limited budget. It is also a reflection of the organization's role in mobilizing and focusing national R&D assets. Some examples of SEMATECH's leveraging are straightforward--e.g., cost-sharing in contracts for equipment R&D with vendor firms and the national laboratories. The consortium will share equipment development costs with vendor contractors on roughly a 1:3 basis.¹⁹

In a broader sense, SEMATECH's leverage is the possibility it creates to accomplish things that might not have been accomplished otherwise--e.g., applying group intelligence to common technological and production problems; setting "common performance objectives" for equipment and materials firms; sharing information on the manufacturing capabilities of foreign competitors; helping to build a national consensus on semiconductor R&D priorities; and coordinating U.S. research efforts.

SEMATECH's leverage should also help to overcome two major impediments to R&D investment, especially in maturing high-tech industries: (i) the high cost and risk of investing in advanced process development; and (ii) the difficulties associated with internalizing the benefits of such investments. Within the SEMATECH framework, members will obtain more R&D and assume less risk for their research dollar than they would individually. They are also likely to gain a head-start over non-members in applying the results of this research.²⁰

(ii) Accelerated Learning

Accelerated learning in the development and application of advanced manufacturing equipment, materials, and processes is the core of SEMATECH's enterprise--the means by which it will compress the development schedules for achieving high-yield production of advanced MDVs. Success here depends on two things: a tighter relationship between the chipmakers allied in SEMATECH and their U.S. suppliers to speed development and insertion of new equipment; and accelerated learning in the production cycle itself.²¹

Improved Supplier Relations. SEMATECH aims at producing "a sea change" in the sometimes distant and litigious relationship between U.S. chipmakers and their suppliers. Part of this change is open and regular communication. SEMATECH is consulting with U.S. vendors on R&D priorities and equipment needs, and on the development of "common performance objectives" for equipment and material. As a result, vendors should be able to focus and

coordinate their R&D efforts; they should also understand, in advance, both the terms of measurement and the standards of performance required for competitive production of 0.5- and 0.35-micron semiconductor devices.

Vendors will also know more quickly and with greater precision how well prototype equipment performs. A third of the clean space in the Austin fab has been set aside as a tool applications process facility (TAPF) in which SEMATECH and vendor company engineers will co-develop and demonstrate new equipment. In many cases, this equipment will have been built under contract expressly for SEMATECH. When resources and space allow, however, the consortium will partner with vendor companies to develop and test other equipment as well.²²

Performance data will be shared with all participating vendor firms and SEMATECH companies. Having met performance "specs," equipment will be available for immediate insertion into SEMATECH's production line and the lines of all member companies without further testing. The hardware cycle will be telescoped, and SEMATECH and its member firms will begin factory production of advanced devices from a higher base of process learning.

SEMATECH aims at a general compression of design and development cycles for manufacturing equipment, in part through heavier reliance on computer modeling and simulation. Historically, the interval from conception to full-scale production of new-generation lithographic machines has averaged about five years. At Phase II and III, SEMATECH will rely mainly on refinements in current technology rather than new-generation equipment. Nonetheless, projected cycle times are demanding--one year for prototype development and one year for testing of Phase II machinery; less if the vendor locates in Austin.²³

Faster Operations Learning. In chip manufacturing, rapid process learning translates directly into higher yield rates. To accelerate process learning, SEMATECH intends to concentrate on (i) reducing production cycle time, (ii) increasing equipment availability/reliability, and (iii) improving process control.

SEMATECH planners project cycle times of twice the theoretical minimum (2x) at Phase I, declining to 1.5x at Phase II, and 1.3x at Phase III.²⁴ In fact, they aim at keeping raw cycle times roughly constant as device complexity and, therefore, process complexity increase. Relatively shorter cycles will permit quicker detection and treatment of process anomalies--i.e., quicker process learning.

To shorten cycle times, equipment must be designed for maximum availability (i.e., so that set-ups and servicing are quick and easy). It must also meet high standards of reliability (i.e., it must operate "up to specs" for extended periods). SEMATECH planners say that Phase II and III yield-learning objectives will require tool availability rates in the 90-percent range. Mean time between failures for individual tools will need to approach 500 hours at Phase II, and 5000 hours at Phase III, far above the reliability levels of current equipment. To meet these standards, tool designs will probably include more redundancy and greater capacity for self-diagnosis and repair. In addition, contamination control in major tool sets will need to improve dramatically.

Tight process control--i.e., the ability to anticipate within a narrow range the characteristics of a given product--contributes directly to yield learning by letting production engineers know at once when tool operations begin to drift out of alignment. SEMATECH estimates that achieving Phase III objectives will require predictable control of device characteristics within a range of +/-1 percent. The best current production technology probably allows process control in the +/-5 percent range.²⁵

SEMATECH's problem here results partly from the limits of measurement science itself. Current metrology simply cannot register variations of +/-1 percent in some characteristics of microelectronic devices. Another part of the problem is designing tools and tool clusters to keep process complexity on a linear growth path despite geometric growth in product complexity.

SEMATECH's three process learning objectives overlap and support one another. Easier servicing and fewer breakdowns shorten cycle times. Shorter cycles mean faster problem finding--i.e., better process control. Better control means shorter cycles. Faster learning drives production costs down more quickly in part because the expense of processing each wafer can be spread over a growing percentage of salable chips per wafer, but also because producers can make fuller use of machines with short economic lives.²⁶

(iii) Technology Research and Development

To identify the most promising technology paths to Phase II and III objectives, SEMATECH consulted the collective expertise of scientists and engineers from industry, government, and academe in a series of technology workshops during 1987 and 1988.

Distilled conclusions of these workshops, filtered by SEMATECH's Strategic Assessment and Planning Group and authorized by its

Board of Directors, are embodied as technology "roadmaps" in the consortium's five-year strategic plan.²⁷ Each roadmap highlights advances in equipment, materials, and process technology needed in a key production area at Phase II and Phase III.

The technology roadmaps also provide a basis for operational planning. The consortium's 1989 Operating Plan identifies problems along each selected technology path, defines a solution approach, schedules elements of the approach on a flow chart, and projects necessary personnel and budgetary commitments. Operating priorities for 1989 include all major areas of lithographic technology, etch and deposition processes and equipment, and manufacturing systems.

Microolithography. SEMATECH proposes to meet Phase II lithography objectives by up-grading optical steppers that are currently available from U.S. suppliers and borrowing IBM's proprietary I-line photoresist--the only U.S.-made resist now effective for 0.5-micron processing. The consortium will also support work on optical resists, advanced mask-making, ultraviolet light sources, and lithographic metrology.

During 1989, SEMATECH may begin to evaluate the commercial utility of synchrotron- and laser-generated X-rays by splitting production lots and comparing the results of X-ray processing at facilities outside the Austin area with results achieved by optical tools in the Phase I fab line. The consortium will also join DARPA and the Naval Research Laboratory in a project to develop commercially affordable photomasks capable of withstanding the destructive effects of prolonged X-ray exposure.

Etch and Deposition Processes and Equipment. The 1989 Plan calls for SEMATECH to sponsor R&D aimed at increasing the reliability and availability of low pressure etch and deposition equipment, improving process control in etch and deposition steps, and developing methods of "planarization."²⁸

Manufacturing Systems. The Plan also outlines efforts to provide an improved foundation for computer integrated manufacturing--e.g., projects aimed at improving process sensor technology, automating device inspection, and accelerating data collection and analysis.

(c) Technology Transfer

Technology developed by SEMATECH will be embodied in improved semiconductor manufacturing equipment, materials, and processes, and also take other forms--e.g., process control standards and systems, training programs, and management models. Most of this technology will be generated in Phases II and III of the

project. No R&D is planned for Phase I; though Phase I efforts have produced important new knowledge in at least one area-- i.e., advanced fab design and construction.

SEMATECH faces two technology transfer problems: disseminating technology effectively to a membership with diverse needs and absorptive capabilities; and ensuring that the commercial and national security benefits of this technology are captured mainly by the U.S. economy.

(i) Mechanisms of Technology Transfer

SEMATECH's technology transfer apparatus will resemble in size and function the marketing arm of a commercial enterprise. An Austin-based staff will work with technology transfer managers at member firms to identify member needs, develop multi-media transfer methodologies (e.g., an on-line data base), manage formal training and transfer sessions, provide continuing after-transfer technical support, and evaluate transfer effectiveness.²⁹

Schedules for the development and formal delivery of manufacturing technology are embedded in SEMATECH's strategic and operating plans. The consortium will also transfer technology in less formal ways. Useful exchanges of technical knowledge have already occurred, for example, in SEMATECH's many standing and special purpose advisory boards. As the project matures, member companies will be able to consult their Austin assignees in areas of special concern. Rotating assignees will carry technical and practical knowledge back to their parent firms. Teams of member-company engineers will train on SEMATECH fab lines, or advisory teams may be sent out from Austin to support member companies on their home turf. SEMATECH-sponsored technology will also flow to member firms in equipment and materials purchased from SEMI/SEMATECH companies.

(ii) Translating Technology Gains into Competitive Advantages for American Firms

The consortium has also taken steps to give member firms and their U.S. suppliers a head start in turning SEMATECH-sponsored technology to competitive advantage. SEMATECH's by-laws limit membership to firms that are based in the United States and owned and operated mainly by Americans. In addition, its announced aim is to rely entirely on U.S. equipment suppliers at all project phases. The vendors will market where they can, but assure SEMATECH and its members a "right of first refusal." Members themselves may use SEMATECH-developed technology in overseas plants that are at least 51-percent U.S.-owned.³⁰

Other means that SEMATECH will use to retard technology leakage include: channeling proprietary information to SEMATECH and member employees with a "need to know"; encrypting on-line data; requiring non-disclosure statements from outside advisors; and cautioning staff to be discreet. A poster in the consortium's Austin headquarters warns: "Loose Lips Sink Chips." Technology patented by SEMATECH would be freely available to member firms and DOD, and in time could be licensed to non-members.

(3) PHASE III

At Phase III, SEMATECH's operating and strategic targets merge. The main goal in each case is world leadership in 0.35-micron semiconductor manufacturing technology. Tactical modes for Phase III are the same as those for Phase II--i.e., leveraged R&D, telescoped equipment development, and accelerated yield-learning.

Though SEMATECH seems likely to generate useful knowledge in every project phase, the consortium's progress in Phases I and II will be measured chiefly against interim performance goals. By 1993, however, the organization will have reached its major technological objectives, or fallen short of them. Its impacts on U.S. semiconductor manufacturing, on up-stream industries, and on the electronics technology base should be measurable. Related effects on U.S. industrial competitiveness should be clear.

(4) SUBSEQUENT PHASES

SEMATECH's planning horizon has been formally extended to 10 years. The 1989 Operating Plan sets planning for Phase IV and Phase V as a 1989 operating objective. Both efforts are projected for the 1990s.

C. PROGRESS IN 1988

By the close of 1988, SEMATECH had made significant progress toward Phase I objectives and established elements of the groundwork for Phases II and III. It had also refined its technology development strategy and tactics, disciplined its planning process, recruited widely-respected leadership, and cultivated alliances with key constituencies.

(1) MOVEMENT TOWARD PHASE I OBJECTIVES

(a) Fab Construction

The decision to locate in Austin required SEMATECH to build a Class-1 wafer processing facility.³¹ Construction was completed in less than half the building time normally required for such facilities, and at lower cost per square foot. Observers suggest a variety of reasons for the accelerated schedule--e.g., a widely shared sense of urgency; the fact that builders were converting an already existing structure; slack in the Austin construction market (crews worked on the fab in two 10-hour shifts, 7 days a week); and strong support from local officials. Also, the fab designer set up offices on-site to speed consideration of requests for changes and clarifications in building specs.

The new fab's clean room was certified Class 1 on December 23. All equipment for the Phase I fab line has been ordered and most has arrived in Austin. Equipping and "proofing-in" of each Phase I production module is proceeding on a separate parallel track. Wafer processing in the lithography module began in the last week of November 1988.³²

(b) Technology Transfer

Building and management technology generated in the fab construction effort was formally transferred to SEMATECH members on November 28-30, 1988. Informal transfers had already occurred--e.g., IBM engineers had studied the Austin example in developing designs for a proposed 64Mb DRAM IBM facility; engineer-assignees who worked on the fab had carried practical knowledge of Class-1 fab construction back to parent firms. Major transfers of manufacturing technology are planned for later in the project. The first such transfer--i.e., complete tooling and technical support for an 0.8-micron lithography module with 0.5-micron capability--is scheduled for the first quarter of 1990.

(2) MOVEMENT TOWARD PHASE II and III OBJECTIVES

Some of the consortium's 1988 achievements support both Phase I and Phase II objectives--e.g., key Phase I process technologies carry over to Phase II; the new fab will house both the Phase I and Phase II production lines. SEMATECH's most visible progress toward out-year objectives in 1988, however, has been in using its extensive advisory apparatus to develop consensus R&D agendas, and in marshalling the research assets of university consortia and the national laboratories. Six university-based Centers of Excellence had been fully or nearly established by the end of 1988, with four others planned for 1989.³³

(3) MOVEMENT IN OTHER AREAS

SEMATECH's most important accomplishments in 1988 probably had less to do with meeting operational goals than with the difficult and occasionally contentious work of self-definition.

(a) Expansion of the Consortium's Strategic Focus:
More Emphasis on Production Flexibility and
Long-Range R&D

Flexible Manufacturing--ASICs. SEMATECH's early plans reflected the view, also adopted by the DSB, that competitive resurgence in high-volume memory-chip markets is the key to renewed strength in the U.S. semiconductor industry at large. A different perspective--shared by small custom-chip firms outside SEMATECH, their philosophic admirers, and most importantly, DOD--is that the consortium's initial planning underestimated the growing importance of markets for small-lot special application chips (ASICs) and the potential of ASICs as drivers of flexible manufacturing technology.³⁴

Evolution in SEMATECH's position on this point may account for its decision at the beginning of February 1988 to produce two Phase-I MDVs, rather than only one, on a single fab line. However, DOD's concern with SEMATECH's fuller commitment to flexible manufacturing was not finally satisfied until May 12, when a joint MOU was finally signed and the federal share of the consortium's 1988 operating budget was released.

X-Ray Technology. SEMATECH also resolved a second strategic issue in 1988--this one concerning its commitment to X-ray technology.³⁵ Observers have suggested that despite the uncertainty and expense involved in developing commercially practicable X-ray lithography, U.S. investment in this area must increase as a hedge against the major Japanese and European X-ray efforts and the possibility that optical lithography may be less effective than expected at 0.35-micron geometries.

SEMATECH's initial argument against including work on X-rays in its near-term planning was financial. The consortium clearly lacks the resources for a full-scale initiative to develop X-ray technology on its own. As noted above, however, it now plans to accelerate and intensify its efforts in X-ray technology. This change may reflect the general movement in SEMATECH's operating philosophy toward greater leveraging of off-site R&D. SEMATECH-sponsored X-ray research is likely to be done at facilities outside the Austin area in cooperative ventures involving the consortium's largest members, university-based resources, and assets of the national laboratories.

(b) Developing A Detailed Operating Plan and a Disciplined Planning Process

At the beginning of 1988, DOD shifted funding and oversight responsibility for SEMATECH from the Office of the Under Secretary for Acquisitions to the Defense Advanced Research Projects Agency (DARPA).

DARPA's well publicized dissatisfaction with SEMATECH's 1988 Operating Plan touched not only issues of general strategy, but the need for greater specificity on R&D timetables, responsibilities, and costs.³⁶ Consortium efforts to develop a new plan benefited substantially from the installation in August of a permanent senior management team and planning staff, and from the close involvement of DARPA's project officer. The new plan--the 1989 Operating Plan--submitted on December 1, 1988 has received DARPA's full approval.³⁷

In subsequent years, updates of SEMATECH's operating plan will be prepared each March for consideration in the federal budget cycle. The current 1989 Plan will itself be updated in March. In effect, SEMATECH's operating plan is a "one-year rolling window" providing detailed project implementation schedules for the first year of a rolling five-year strategic plan. The five-year plan, in turn, is the first and most detailed portion of a 10-year strategic "vision." Neither the one-year operating plan nor the five-year strategic plan is permanently fixed; either may be adapted quickly to shifting competitive conditions.

(c) Increasing the Amount and Efficiency of R&D Spending

Since joining SEMATECH in late July, CEO Robert Noyce and COO Paul Castrucci have trimmed the consortium's projected labor and P&E costs, cutting back projected employment from 750 to 650 full-time employees (FTE) and deciding against construction of a new fab for Phase II of the project. At the same time, they have increased the R&D share of consortium spending, set clear R&D project priorities (in the annual operating plan), and placed more stress on leveraged financing of off-site projects. Forty percent (\$104 million) of the consortium's scheduled spending commitment in CY 1989 will go for leveraged off-site R&D.³⁸

(d) Building Members' Commitment

Member commitment--expressed especially in the contribution of able staff--is crucial to the success of the consortium model. Powerful centrifugal forces work against such commitment. Market upswings dilute the sense of urgency. Market downswings sap financial will. Members may begin to suspect that costs

and benefits are not being fairly distributed. Mergers or divestitures may disrupt operating chemistry. In SEMATECH's particular case, economic factors encouraging U.S. chipmakers to seek foreign alliances are an added problem.³⁹

Given these potential distractions, SEMATECH rightly includes "gaining industry consensus on a core program" as one of its principal first-year accomplishments. Consortium officials contend that member company commitment has grown over the year "from casual to urgent." A major reason for this change, according to CEO Noyce, is the federal decision to participate in the project and resulting industry confidence in SEMATECH's durability. A second reason, in the view of key staffers, is the fact that members interact within the SEMATECH framework on a daily basis and that familiarity, in this case, breeds cooperation.⁴⁰

Other explanations include SEMATECH's sprouting physical presence on the Austin landscape and the organization's success after considerable travail in recruiting highly respected top leadership. Ultimately, however, each member's commitment to the project is sustained and limited by its own perception of business interest.⁴¹

(e) Improving Supplier Relations

SEMATECH's effort to strengthen the semiconductor industry's U.S. supplier base faces two major obstacles: (i) the historic disjunction between U.S. chipmakers and their U.S. suppliers; and (ii) the fact that improved cooperation in up-stream industries is discouraged by the same centrifugal influences that act on SEMATECH itself. A key intramural challenge for SEMI/SEMATECH, according to its President Sam Harrell, has been "coupling the bigs and the smalls."⁴²

Spokesmen for SEMATECH and SEMI/SEMATECH seem to agree that by creating a framework and incentives for communication, SEMATECH has succeeded in founding a more open and cooperative relationship with key suppliers. In addition, some suppliers appear to have made preliminary plans to locate R&D and production facilities in Austin. So far, there are no examples of vertical or horizontal teaming among supplier firms. But the opportunities and inducements for teaming are likely to grow in 1989, as SEMATECH begins Phase II and III contracting.⁴³

Erosion in the U.S.-owned materials industry continued in 1988. Despite SEMATECH's efforts to find a U.S. buyer, Huels AG of West Germany agreed to purchase Monsanto Electronic Materials Company, the last major U.S.-owned merchant producer of silicon wafers.

D. ISSUES FOR CONSIDERATION IN FUTURE
ADVISORY COMMITTEE REPORTS

SEMATECH's track record is far too short to allow substantive assessment of its achievements relative to its strategic and operating objectives. In subsequent reports, however, the Advisory Committee may consider a range of performance indices which are noted and discussed briefly here.

(1) MEETING TECHNOLOGY R&D AND TECHNOLOGY
TRANSFER OBJECTIVES

In its next annual report, the Council should be able to evaluate SEMATECH's progress in relation to all Phase I objectives, and to Phase II and III R&D contracting and early contract performance goals. In addition, though the consortium plans no formal transfers of manufacturing technology until the first quarter of 1990, informal transfers are almost certain to result from the practical experience of setting up, proofing in, and operating the Phase I production line.

(2) SUSTAINING MEMBER SUPPORT

Members' commitment to SEMATECH may be tested in the coming year by several developments--e.g., a projected softening in world demand for semiconductors and the consortium's continuing effort to fill mid-level engineering and management positions with talented assignees. SEMATECH's full-time staff grew from 40 to 417 between January and December 1988. The 1989 Operating Plan projects full staffing (650 FTE) by December. Of this group, 400 are expected to be two-year assignees from member companies (200 will be permanent SEMATECH employees and the rest will be contract staff).

Senior officers of the consortium indicate that recruitment of people who are "among the best" in their home companies has not been a problem.⁴⁴ The question remains, however, whether able people on accelerated career tracks will be willing, as a rule, to serve two-year tours in Austin, away from the politics and the opportunities of their home companies. Part of the answer certainly lies in SEMATECH's own performance and in the way industry people come to regard it. Another part may involve changes in the evaluation and reward systems of member firms.

(3) STRENGTHENING THE VENDOR BASE

Reports of improved relations between SEMATECH and U.S. equipment and materials firms are encouraging but preliminary.

Generalization and consolidation of the new relationship will depend on whether the consortium and, indeed, SEMI/SEMATECH satisfy most vendors on the openness and fairness of Phase II/III contracting and information sharing, and whether the risks of greater openness are sufficiently balanced by the benefit of increasing sales.

Other indices of SEMATECH's influence on upstream firms could include decisions by vendors to co-locate in Austin, increased incidence of vertical and horizontal teaming, and competitive resurgence in key market segments--e.g., optical lithography. Such a resurgence would also mean reestablishment of U.S. mid-range technology leadership.

(4) CONTROLLING TECHNOLOGY TRANSFER

A premise of public participation in SEMATECH is that results of the consortium's technology R&D will flow mainly to U.S.-owned firms--i.e., that the consortium can transfer technology not only effectively but selectively. The existing system of international business alliances in both the chip-making and vendor industries appears to provide avenues for uncontrolled technology transfer. At least five SEMATECH members currently have joint product development, manufacturing, or marketing arrangements with Japanese firms; the largest U.S. equipment makers have similar overseas links.⁴⁵

However, the potential in this situation for international dissipation of U.S. technology gains should not be exaggerated. U.S. firms are probably able to cooperate with foreigners in some segments of the product design/manufacturing/marketing spectrum and compete with them in other segments. The presumption that U.S. firms have such capacity in relation to one another underlies SEMATECH itself. In subsequent reports, the Advisory Council should be able to assess member cooperation, and the cooperation of SEMI/SEMATECH firms, in controlling the transfer of U.S. technology to foreign competitors.

(5) EFFECTS ON THE COMPETITIVENESS OF U.S. CHIPMAKERS

A second premise of public participation in SEMATECH is that member firms will be able and willing to translate leadership in manufacturing technology into increased market strength. SEMATECH is not a comprehensive approach to achieving this outcome. Nonetheless, if the public investment in SEMATECH is not followed by an increase in the competitive strength of U.S. chipmakers and their suppliers, SEMATECH as a public policy will not have been successful.

As the consortium was gaining momentum in 1988, U.S. chipmakers continued to lose ground commercially. U.S. merchant firms' market share slipped to 37 percent, three percentage points below 1987 levels. In contrast, Japanese firms captured 50 percent of the market in 1988, up two points from the year before.⁴⁶ The question for policymakers is whether U.S. firms can check and reverse these trends.

One indication of U.S. merchant firms' competitive intent may be the willingness of these firms to reenter the world DRAM markets. The costs of reentry are high, perhaps \$500 million, and so are the risks. Japan's six largest chipmakers recently announced plans to invest nearly \$3 billion in new capacity--chiefly for 1Mb DRAMs, but also for 4Mb DRAMs and ASICs. The two U.S. merchant producers still making DRAMs are reportedly also adding capacity. So far, however, Motorola is the only U.S. firm to restart DRAM production--as part of an agreement with Toshiba to co-produce 1Mb devices in the United States, Japan, and Scotland.⁴⁷

(6) TRACKING FOREIGN INITIATIVES

SEMATECH's regularly up-dated strategic plan takes account of foreign production capabilities and initiatives in relation to the consortium's own objectives, timetables, and resources. Nonetheless, in future reports, the Advisory Council may wish to consider comparable European and Japanese efforts as a guide to continuing deliberation on SEMATECH's appropriate scale and technological focus.

At least three of these efforts seem to bear watching. JESSI (for Joint European Sub-Micron Silicon), an alliance of West Germany's Siemens, Netherlands' Philips, and the Franco-Italian group SGS-Thomson is asking the EC to fund 50 percent of its projected \$500 million annual budget for 12 years to pursue objectives very similar to SEMATECH's--i.e., development of flexible chipmaking techniques and support of local equipment and materials industries.

In addition, two Japanese industry-government consortia launched in 1986 with 10-year planning horizons are developing technologies thought necessary for competitive production of 256Mb DRAMs and comparably complex devices. SORTEC (for Synchrotron Orbital Radiation Technologies), an alliance of 13 large Japanese companies begun with \$100 million of government support is focused on X-ray lithography and X-ray generation methods. The Optical IC program, also involving 13 firms, is developing manufacturing techniques for integrating optical and electronic properties in a single chip.⁴⁸

PART II

FEDERAL PARTICIPATION IN SEMATECH:
DESCRIPTION AND ASSESSMENT

SEMATECH's main institutional contact points at the federal level during 1988 were the Office of the Under Secretary of Defense for Acquisitions, DARPA, and several of the Energy Department's national laboratories. Consortium research managers also explored contracting options with the National Institute for Standards and Technology (NIST).

A. DOD/DARPA

Experience in 1988 helped to allay concern that DOD funding might lead to the subordination of SEMATECH's commercial objectives to specific defense production needs. Early tensions between DARPA and SEMATECH on the issues of production flexibility, planning discipline, and project leadership/industry commitment were largely resolved by late summer. At yearend, DARPA officials were pleased with the SEMATECH's overall progress. SEMATECH's view of the relationship, according to CEO Noyce, was: "Worries, but no problems."¹

(1) CONCERNS ABOUT DOD FUNDING AND OVERSIGHT

Concerns about DOD funding and oversight of SEMATECH are partly an outgrowth of experience in the Department's Very High Speed Integrated Circuit (VHSIC) program. Begun in 1978, and now in its concluding phase, VHSIC aimed at developing and producing fast, reliable, radiation-hard semiconductor devices for special military applications. Many SEMATECH members participated directly or indirectly in the program. By all accounts, VHSIC achieved its major production and applications objectives. However, VHSIC's strategy differed from that of SEMATECH in that it stressed device performance rather than low-cost production, technology commercialization, or development of advanced manufacturing techniques.²

A second set of concerns is not specific to DOD, but applies to all federal initiatives focused on particular industries--i.e., that such programs are inherently insensitive to market signals.

In SEMATECH's case, this generic criticism has been expressed as a caution against federal micro-management.³

(2) DOD/DARPA APPROACH TO PROJECT OVERSIGHT

DOD's relations with SEMATECH during 1988 appear to reflect a basic shift in Departmental thinking about the relationship between commercial and defense production. In past decades, defense production took precedence. R&D undertaken for this purpose generated clear benefits for the commercial economy. However, recent DOD assessments recognize a significant potential for reverse benefit flows. In "dual-use" industries, a strong commercial base is increasingly considered essential to cost-efficient military sourcing.

The DSB Report expresses this view with particular regard to semiconductors. The Under Secretary's July 1988 report on Bolstering Defense Industrial Competitiveness applies the idea more generally. The latter report asserts that many defense production programs could benefit from increased use of commercial designs, engineering, and production capacity. Advantages include shorter lead-times, lower costs, better quality, and increased surge potential.⁴

Similar thinking seems to be reflected in DOD's decision early in 1988 to vest DARPA with SEMATECH oversight responsibility. Though DARPA's main customers are the military and intelligence communities, the agency has a long history of developing dual-application technologies and an avowed interest in promoting technology transfer to the private sector. An estimated 60 percent of DARPA's current budget is allocated to dual-use R&D--e.g., computer and materials sciences, robotics, manufacturing technology, superconductivity.⁵ The agency also has a major continuing interest in advanced microelectronics research. Several of its current projects complement SEMATECH--e.g., projects in X-ray lithography, compound semiconductors, and computer integrated manufacturing.

DARPA sees itself as a kind of R&D impresario, bringing the best available talent to bear on emerging scientific and technological problems. The agency has no research facilities of its own. Its projects are normally done under contract at facilities in industry, universities, and the national labs. DARPA scientist/engineer-managers assemble project teams and take an active role in their work.⁶

SEMATECH differs from other DARPA projects in ways that seem likely to contribute to the consortium's operating independence.

First, it is not a contractor, and DARPA is not its primary customer. SEMATECH is funded by grant to pursue an overall mission established in the project MOU. The MOU also defines DARPA's consultative role in the consortium's operational planning. The funding mechanism has given DARPA constructive leverage in formative stages of the SEMATECH project, but is not conducive to micro-management--as long as grant disbursements are in large annual blocks, as they have been.

A second condition contributing to SEMATECH's operating independence is the fact that at least 50 percent of program funds must be supplied by consortium members themselves. A third condition, mainly affecting the operating flexibility of member firms, is that SEMATECH's design and purpose facilitate the rapid transfer and commercial application of project-generated technology.

B. THE NATIONAL LABORATORIES

DOE's nine national laboratories conduct basic and applied research for DOE, other federal agencies, and the private sector on a cost-reimbursable basis. As a consequence of the Technology Transfer Act of 1986, all of the labs now have joint R&D ventures with individual private firms or consortia.

Under DOE's user facility policy, qualified scientists and engineers from industry and academe are permitted to use lab facilities for their research, including proprietary research. The Department has issued class waivers granting patent rights in advance for work done in the labs for or by outsiders.

The national labs spent an estimated \$62 million in FY 1987 on semiconductor manufacturing technology. Most of this expenditure was directed at radiation-hardening semiconductors for space and weapons systems. The National Research Council has suggested that the labs can play more of a role in semiconductor R&D, if they can overcome constraints imposed by their institutional mission and basic-research orientation, and if the nation at large can agree on a semiconductor R&D agenda.⁷

SEMATECH is a partial solution to the second problem. So far, however, lab involvement in the consortium's program has been slow to develop. A major exception is the SETECH center for equipment reliability research now being established with partial SEMATECH funding at Sandia National Laboratory. SETECH will draw on Sandia's expertise in reliability analysis, testing, and process modeling to help U.S. equipment firms improve the quality of their products. Selected pieces of equipment being co-developed by SEMATECH and its suppliers will be chosen as early test vehicles.⁸

The Sandia lab will also participate with the University of New Mexico in a SEMATECH Center of Excellence that will develop technologies for improved manufacturing process control--i.e., on-line analysis and metrology.

In addition to its involvement at Sandia, SEMATECH may use the National Synchrotron Light Source at Brookhaven National Laboratory in cooperative arrangements with member firms and others to test commercial applications of X-ray technology. The consortium is also exploring joint research possibilities with the Oak Ridge National Laboratory.

C. THE NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY

NIST's Center for Electronics and Electrical Engineering has held preliminary discussions with SEMATECH on several metrological research proposals--e.g., projects to improve understanding of the chemistry and physics of plasma processes and to improve the accuracy of measurements in semiconductor processing.⁹

D. THE ADVISORY COUNCIL

The Advisory Council on Federal Participation in SEMATECH is not yet fully operational. Five members of the Council are senior federal officials who serve ex officio. DARPA and SEMATECH have proposed the names of seven nominees and two alternates for the seven non-governmental Council positions. Presidential appointments for these or other candidates have been delayed by the change of Administration. On November 15, 1988, SEMATECH held a detailed briefing in Austin for the ex officio Council members and proposed non-governmental nominees. Those present were asked for their "input on holes in the program."

PART III

ALTERNATIVE MODES OF FEDERAL
PARTICIPATION

The Trade Act (Sec. 5422) directs the Advisory Council to consider alternative modes of federal financing and oversight of SEMATECH and to review options for recouping public investment in the project. This section examines the authorities, resources, and operating modes of three civilian agencies that have significant semiconductor R&D programs--DOE's national laboratory system, NIST, and the National Science Foundation (NSF). It also discusses methods of recoupment.

A. CIVILIAN AGENCIES THAT COULD SHARE OR
SUPPLANT DOD'S ROLE IN SEMATECH

At least two civilian agencies--DOE and NIST--have the authority and technical expertise to join or supplant DOD in funding and managing the SEMATECH project. Neither, however, has unprogrammed resources that it could easily commit to the project. A decision to alter the current funding and oversight structure, therefore, would entail either the reprogramming of currently planned civilian-agency expenditures, a shift of resources from DOD, or an increase in the federal budget. It might also require basic adjustments in priorities and operating modes of the civilian agencies. In addition, any joint oversight arrangement would slow federal reaction time and add to the problem of securing proprietary information.¹

(1) DOE NATIONAL LABORATORIES

The legislation creating SEMATECH directs the Secretary of Energy to establish an "Initiative" on semiconductor manufacturing technology R&D and authorizes him to conduct this program in a manner complementing SEMATECH's operations and objectives (P.L. 100-180, Part D). Each of the national laboratories is authorized to enter into joint R&D agreements with DOD, SEMATECH, other industry consortia, and academic institutions, and to make its facilities available to these organizations on a reimbursable basis and to an extent consistent with the laboratory's basic mission.

Congress authorized \$25 million in FY 1988 to support the DOE Initiative, but appropriated no new funds for this purpose. As a result, the labs appear to be redirecting some existing resources to support SEMATECH's research program. For example, Sandia National Laboratory will shoulder the major share of funding responsibility for its joint project with SEMATECH on reliability testing (SETECH); and cooperative projects involving SEMATECH and other national labs (e.g., Brookhaven) now seem likely.² In a modest and decentralized way, therefore, joint funding of the SEMATECH program will soon be a reality.

An effort to expand DOE's participation in SEMATECH substantially, however, would face several hard questions, apart from the issue of financing. One such question concerns the extent to which the national labs can be reoriented toward commercial R&D and away from their traditional basic research mission. DOE officials have expressed ambivalence on this point.³ Like DOD, the national labs have a standing agenda that is not market oriented. Increasing DOE's role in SEMATECH, therefore, would not necessarily make the consortium's commercial character more secure or increase its chances for success, especially if DOE did not assign project oversight responsibility to a strong in-house advocate.

A related issue concerns the opportunity cost of committing too large a share of national labs' limited capacity to support commercial R&D for a single industry--semiconductors.

(2) NIST ADVANCED TECHNOLOGY PROGRAM

NIST currently spends about \$6 million annually on semiconductor metrology R&D in the areas of materials characterization, process metrology, device characterization, and process control test methods.⁴

The 1988 Trade Act authorizes the Institute to establish a new Advanced Technology Program to aid specific U.S. industries in accelerating the development and commercialization of generic technology. The Act empowers NIST to enter into R&D contracts and cooperative agreements with businesses and other research organizations, and to provide such joint efforts with start-up funding and a minority share of operating costs (for up to five years), management and technical advice, and access to NIST equipment, facilities and personnel.

The Act also establishes a Visiting Committee on Advanced Technology to advise the Director of NIST, and report annually to the Secretary of Commerce and Congress on NIST resources and expertise that could support joint R&D ventures in areas important to U.S. industrial competitiveness.

Though NIST now has the authority to participate in industry consortia on the SEMATECH model, such involvement on a large scale would be difficult for several reasons. The first of these is financial: NIST's entire budget for semiconductor R&D is a small fraction of the current cost of federal participation in SEMATECH. Moreover, very little of this budget appears to be available for new uses.

In addition, NIST's management experience has been mainly in small projects focused on problems of scientific measurement. Substantial involvement in efforts as large as SEMATECH would require major new financial and managerial resources. Steps would also be needed to ensure maintenance of the strength and status of the Institute's traditional scientific programs.

(3) NATIONAL SCIENCE FOUNDATION

NSF funds an estimated \$25 million to \$30 million of semiconductor research annually including projects on new semiconductor materials, thin film deposition, lithography, resists, three-dimensional device structures, and computer aided design of silicon devices. The largest individual grants in this area are about \$2 million a year. NSF now participates in SEMATECH indirectly through its involvement in SRC.⁵

NSF supports basic research in wide-ranging areas through grants to scientists and engineers at academic institutions. Agency planning does not anticipate specific research outcomes, but targets general areas for support. Grant awards--normally for one to five years--are based on the scientific merit of individual proposals as determined by peer review. Grant renewals are also determined by peer review. Between reviews, there is little direct oversight of grantees. Given this operating mode, NSF officials have suggested that the agency's most useful role in support of SEMATECH may be to ensure that innovative R&D is brought to the consortium's attention.

B. RECOUPMENT

The legislation authorizing federal funding for SEMATECH makes no provision for monetary recoupment, but ensures DOD access to SEMATECH-generated R&D on the same terms that apply to private members of the the consortium. DOD is free to use this technology in its own chipmaking facilities and to lend the technology to defense contractors who are not SEMATECH members, on condition that it not be used for broader commercial ends. In

addition, if the consortium is dissolved for any reason, its charter provides for the Board of Directors to distribute residual assets in a manner that would allow recoupment of a share of these assets by the federal government.

Ultimately, however, the most important returns on the federal investment in SEMATECH will be indirect. If the consortium contributes to a more competitive U.S. semiconductor industry, the federal government will recoup its investment in the form of more cost-efficient defense purchasing, greater assurance of technology leadership in defense electronics, and a generally healthier economy.

PART IV

CONCLUSIONS AND RECOMMENDATIONS

The Council has considered three policy matters: (i) whether federal participation in SEMATECH should continue and in what form; (ii) SEMATECH's early lessons about industry-government efforts to increase U.S. commercial strength; and (iii) issues for review by the newly-created National Advisory Committee on Semiconductors.

A. CONTINUED FEDERAL PARTICIPATION IN SEMATECH

The Advisory Council recommends continued federal funding for SEMATECH at the present \$100-million level in FY 1990. The Council further recommends against any shift or division in project funding and management responsibility at this time.

Continued funding at current levels is warranted for two reasons. SEMATECH is just getting under way. A decision now to alter the terms of federal support based on anything the organization has done or failed to do would be premature. In addition, the project's success depends heavily on industry commitment. SEMATECH's senior officers believe that the intensity of this commitment is significantly influenced by federal participation. Though SEMATECH could carry on without federal sponsorship, its programs would be truncated.¹

Several considerations favor leaving the current project funding and oversight structure intact. Experience in 1988 has helped to allay fears that, under DOD management, SEMATECH's commercial objectives might be subordinated to defense production needs. The consortium has scored important preliminary successes and developed a cooperative working relationship with DARPA. DARPA itself has a strong institutional interest in SEMATECH's commercial goals, in part because of the agency's emphasis on developing dual-use technology, but also because a commercially strong semiconductor industry is critical to U.S. military strength. Continued funding for SEMATECH at the current level is included in DARPA's FY 1990 budget request.

For the near term, DOE is the only civilian agency capable of supplanting or sharing DARPA's funding and oversight role in SEMATECH. DOE officials have expressed concern, however, that such involvement might divert the national laboratories from their basic research mission. Also, any sharing of responsibility would make project management more cumbersome.

B. SEMATECH AS A MODEL--SOME EARLY LESSONS

Recent discussions of industry-government consortia to promote U.S. competitive strength in areas other than semiconductors (e.g., superconductivity, biotechnology, high definition TV) often cite the SEMATECH model.² As a model, however, SEMATECH should be treated with care. Factors that have contributed to the consortium's early progress may not be present in all cases. Absent such factors, the problems of creating and operating a consortium probably increase.

Basic to the SEMATECH model is a widely-shared view that erosion in the semiconductor industry's market position is a serious threat to U.S. economic and military strength. Industry participation in SEMATECH has been driven by declining market shares and the perception that U.S. merchant firms, acting alone, are no longer competitive in key areas of manufacturing technology. Government participation is rooted in a similar perception and in the view that a strong U.S. semiconductor industry is vital to U.S. military capability. These perceptions and a resulting belief in the consortium's national importance are responsible not only for SEMATECH's creation, but for much of the project's current cohesion, and for the high motivation of project staff.

Other key aspects of the model include the existence of a large and resourceful U.S. semiconductor industry and the central involvement in SEMATECH of the industry's largest firms. SEMATECH is essentially an industry endeavor. Private firms are the principal active participants, and their commitment, especially their willingness to share advanced technology and highly-skilled staff, is crucial to the project's chances for success. Moreover, active involvement in the project by IBM and others has probably contributed to the view that remedial action in the semiconductor industry is needed, and has increased industry (and government) confidence that SEMATECH has the resources to achieve its goals.

Some recent proposals for consortia involve technologies or products for which U.S. industries are in their infancy, do not yet exist, or no longer exist. Questions of program objectives and design in such cases may be more complicated than they have been in SEMATECH's case.

Another characteristic of the SEMATECH model is the existence of a range of technology R&D problems that provide both scope and incentive for cooperative effort. SEMATECH will develop technology that is far enough removed from the product end of the R&D spectrum to allow members to cooperate, yet near enough to be practically useful in a commercially significant time frame. In addition, SEMATECH's technology R&D objectives are clearly defined, and an elaborate system is in place for the rapid and equitable distribution of technology benefits.

A final characteristic of the model concerns the spirit and style of federal program management. DARPA appears to have exercised a firm and constructive influence during SEMATECH's formative stage, and to have avoided the pitfall of micro-management. If federal influence had been ambivalent or more directive during the project's early months, industry commitment would probably have been harder to sustain.

A further interesting feature of the SEMATECH model relates to the problem of tapping and coordinating resources of the federal laboratory system to support competitiveness objectives. Potentially at least, SEMATECH is a demand-side answer to this problem. The consortium is shopping the federal laboratory system for resources that meet its commercially-oriented needs. Its shopping list is a plan for coordinating the use of federal resources in one important area of R&D affecting U.S. industrial competitiveness. Its effectiveness in implementing the plan is directly related to the size of its budget.

C. AREAS FOR FURTHER POLICY CONSIDERATION

SEMATECH is a national project, not a national policy. Even if the consortium were a complete success in its own terms, major issues now affecting the competitiveness of U.S. chipmakers would remain--e.g., limited marketing opportunities, and a range of tax, antitrust, and trade policy issues. In addition, the United States would still trail the Japanese and Europeans in developing technologies necessary for competitive leadership in semiconductors in the late 1990s--e.g., compound semiconductor processing and X-ray technology.

The entire range of economic, antitrust, trade, and R&D issues affecting the U.S. semiconductor industry's competitive status should be on the agenda for consideration by the new National Advisory Committee on Semiconductors.

NOTES

INTRODUCTION

1. The SEMATECH members are: Advanced Micro Devices, AT&T, Digital Equipment Corporation, Harris Corporation, Hewlett-Packard, Intel, IBM, LSI Logic, Micron Technology Inc., Motorola, National Semiconductor, NCR, Rockwell International, and Texas Instruments.
2. SEMATECH's 1989 Operating Plan. Spending is expected to stabilize at a rate of \$200 million per year by end of 1989. In 1988, actual commitments were about 30 percent below the projected stable rate; commitments for 1989 are expected to be about 30 percent above that level. Much of the state and local share of program financing--e.g., tax abatements, low-cost leases--translates into operating savings and is not shown in operating budgets.
3. "SEMATECH Goes to Austin," Dataquest Research Newsletter (February 1988) reviews the regional bidding for SEMATECH. Of this incentive package, \$38 million was provided by the University of Texas to help cover initial construction costs at the Austin site.
4. Semiconductor market share data reported in Thomas Howell and others, The Microelectronics Race (Westview Press; Boulder, 1988), Appendix A. When captive producers (e.g., IBM) are included in the calculation, U.S. market share declines less steeply. Howell notes (p. 56) that the Japanese share of world memory shipments increased by 8 percentage points in 1986; about the same amount as shipments by U.S. firms declined. Equipment sales data are reported by VLSI Research, Inc., in VLSI Manufacturing Outlook. Share data are dollar-denominated and are not adjusted for exchange-rate variations.
5. VLSI Manufacturing Outlook.
6. According to VLSI, Japanese equipment purchases from Japanese sources increased from \$750 million to \$942 million between 1985 and 1986; Japanese purchases from U.S. sources declined from \$769 million to \$475 million. These data reflect current exchange rates. The pattern probably reflects continued purchasing from captive suppliers by integrated Japanese electronics firms.

7. U.S. Department of Commerce, A Competitive Assessment of the U.S. Semiconductor Manufacturing Equipment Industry (Washington, D.C., 1985), p. 63; according to the DOC study, some decline in U.S. technological leadership in manufacturing equipment results from U.S. chipmakers' conservative production strategies. See also pp. 30-31 on the relation between semiconductor production and equipment demand.
8. Howell, op. cit., Appendix A. Estimates of Japanese R&D spending are for the period 1982-85.
9. Panel on Materials Science, National Materials Advisory Board, National Research Council, Advanced Processing of Electronic Materials in the United States and Japan (National Academy Press: Washington, D.C., 1986). In a more sweeping 1987 comparison, the Defense Science Board (DSB) found that of 25 semiconductor products and processes, Japan led in 12, U.S. firms led in 5, and in 8 there was relative parity. In 19 of the 25 areas, however, counting 4 of the 5 areas of U.S. leadership, the U.S. position was judged to be declining; Report of the Defense Science Board Task Force on Semiconductor Dependency (U.S. Government Printing Office: Washington, D.C., February 1987). A recent study by the Congressional Budget Office (CBO), The Benefits and Risks of Federal Funding for SEMATECH (September 1987), p. 25, notes that Japanese firms are already the world's leading producers of semiconductor materials. In 1986, six of the world's top 10 materials firms were Japanese. Japanese firms supplied 92 percent of the world market for ceramic packages, 80 percent of the frames on which semiconductor chips are mounted, and almost half the world's chip-quality silicon.
10. DSB Report, p. 2 on the supply dependency question; pp. 10, 65-66, 78, 82 on the defense and economic implications of downstream erosion in the electronics industries.

PART I

1. Noted by Pat O'Hagan, SEMATECH's Director for Total Quality Deployment, at a briefing for Congressional staff and others (September 15, 1988).
2. DSB Report, p. 18.
3. Dataquest Research Newsletter (February 1988), p. 6; also "The World of Silicon: It's Dog Eat Dog," Spectrum, a publication of the Institute of Electronics and Electrical Engineering (September 1988), p. 32. In the DSB's

judgment, 1996 will be too late: "American merchant producers are no longer able to develop and produce in the U.S. low-price, reliable DRAMs in a time scale necessary to achieve significant market penetration" (Report, p. 5-6).

4. See "VLSI Lithography: Thin Lines, Thinner Profits," Electronic Business (EB) (March 1, 1988), p. 68. GCA's loss of market leadership in microlithography to Nikon in 1985 represents a symbolic and substantive watershed in the general competitive decline of the U.S. equipment sector. GCA accounted for 175 of the 240 wafer steppers sold worldwide in 1981; compared with 15 for Nikon. Four years later, apparently because of superior quality and service, Nikon sold 145 steppers, compared with GCA's 115. See fn. 9, above, on the U.S. materials industry.
5. See DOC, Competitive Assessment, p. 46. During demand surges in the late 1970s and early 1980s, foreign chip-makers sometimes found U.S. equipment firms unreliable and turned to domestic sources. In addition, once delivered, U.S.-made equipment has not always met performance specifications; and U.S. firms have been slow to understand the competitive importance of customer service. GCA's CEO, Peter Simone, cited in EB (March 1, 1988), p. 68, explains his company's loss of market share: "Some mistakes were made....We had to do more work...on helping a customer apply a system to his process....We also had to address performance issues, and we were late getting a solid 1-micron machine to market."
6. Estimate based on data supplied by VSLI Research.
7. Semiconductor equipment firms invest heavily in product R&D. An industry rule of thumb is that investment at a rate of 15 percent of sales is necessary simply to survive as an equipment maker. It is not clear, however, that current investment rates in the industry are sufficient by themselves to meet the competitive challenge from Japan and Europe. See for example, the article by John Markoff, "Experts Warn of U.S. Lag In Vital Chip Technology," New York Times (December 12, 1988) comparing U.S. and Japanese R&D efforts in X-ray lithography. Also, some analysts argue that current R&D spending by U.S. equipment firms is duplicative and wasteful.
8. SEMI/SEMATECH fact sheet distributed at a September 15, 1988 briefing for Congressional staff and others by Sam Harrell, President of SEMI/SEMATECH. SEMI/SEMATECH will also help to integrate SEMATECH's work on performance standards with SEMI's ongoing efforts in this area. On November 15, 1988, 151 firms were SEMI/SEMATECH members; 17 had annual sales of more than \$50 million; 81 had annual sales of less than \$5 million.

9. In 1986, SRC's 35 members included all major U.S. chip-makers and some equipment and materials suppliers. Roughly 90 percent of the organization's \$20-million annual budget is provided by private members; the rest--\$2.4 million in 1987--is provided by NSF, DOD, NSC, and NIST. In 1986, SRC supported 200 research projects at 43 universities aimed at improving semiconductor reliability and performance and helping to develop young engineers. See Larry Sumney and Robert Burger, "Revitalizing the U.S. Semiconductor Industry," Issues in Science and Technology (Summer 1987), p. 41; also Robert Williams, Harvard Business School case study on SEMATECH (1988), p.8.
10. On the untapped commercial potential of the federal laboratory system, see National Materials Advisory Board, op. cit., p.36; also The Semiconductor Industry and the National Laboratories, a workshop report of the Manufacturing Studies Board and the National Materials Advisory Board of the National Research Council (National Academy Press: Washington, D.C., 1987), p. 8. Recognition of the need to mobilize and coordinate national R&D resources is reflected in recent legislation--e.g., the creation of new incentives for commercially oriented R&D in federal labs under the 1986 Technology Transfer Act; and assignment of new technology commercialization responsibilities to the Departments of Commerce and Energy by the 1988 Trade Act.
11. See Bolstering Defense Industrial Competitiveness, a report to the Secretary of Defense by the Under Secretary of Defense for Acquisitions (July 1988), p.53.
12. SEMATECH hand-out, "SEMATECH Benefits to the Department of Defense" (undated). SEMATECH will develop manufacturing technology that is compatible with many radiation-hardened processes and processes used to meet military temperature specifications. This technology, including software to support flexible manufacturing, should also be applicable to low-volume production of specialized chips for military uses.
13. See Rachel McCulloch, "The Challenge to U.S. Leadership in High-Technology Industries." National Bureau of Economic Research, Working Paper No. 2513 (NBER: Cambridge, Mass., February 1988) p. 21: "For the major economic rivals of the United States, the challenge to U.S. worldwide preeminence in high-technology production implies a challenge to U.S. political and military hegemony as well as to established commercial interests."
14. Bolstering Defense Industrial Competitiveness, p. 28. See also CBO, The Benefits and Risks of Federal Funding for SEMATECH, p.48: "Its [SEMATECH's] greatest contribution to national security may lie in maintaining the vitality of the U.S. industrial base."

15. IBM and ATT retain ownership of all proprietary technologies used in the production of these devices. SEMATECH member companies will share ownership only of those technologies actually developed by SEMATECH.
16. SEMATECH press release (January 26, 1988), "SEMATECH Announces Manufacturing Demonstration Vehicles for Full Range of Product Families." Also, Dataquest Research Newsletter (February 1988). In addition, SEMATECH's choice of Phase I MDVs would directly support efforts by member firms to reclaim DRAM market share or compete more effectively in world ASIC markets.
17. Comments by Paul Castrucci, SEMATECH's Chief Operating Officer, at a briefing for members of the Advisory Council on Federal Participation (Austin, November 15, 1988).
18. Comments of Ashok Sinha, Phase I project director, at SEMI/SEMATECH's Presidents Meeting (November 16, 1988).
19. Comments of SEMI/SEMATECH President Sam Harrell in an interview for this report (November 15, 1988).
20. See CBO, op. cit., p. 31, on the reasons for semiconductor industry underinvestment in commonplace improvements that result in the evolution of devices and manufacturing processes. See the section on technology transfer, below, on steps SEMATECH will take to "internalize" the benefit of its R&D investments.
21. CBO, op. cit., p. 24, suggests that Japanese firms' real edge in global semiconductor competition comes not from superior equipment, but from rapidly learning how to make conventional equipment more productive--from constantly servicing, recalibrating and improving the materials handling capabilities of their machines.
22. The TAPF is scheduled to begin operating in April 1989, with room for 25 pieces of equipment. Engineers from different vendor firms will work in close proximity. There will be individual cells for "de-bug and prove-out," and secure areas for proprietary work. An early TAPF project will compare GCA and Nikon steppers to see how to improve the U.S. models. Electronic News (EN), (November 28, 1988), p. 8 reports on an un-contracted-for piece of equipment that may be bound for TAPF testing: Perkin-Elmer's new step and scan lithography system with 0.5-micron resolution. IBM will buy four of the first five production models; one is destined for SEMATECH. In conjunction with the TAPF, SEMATECH will co-sponsor a major equipment reliability

testing program at the Sandia National Laboratory. The Sandia program, discussed in more detail in Part II, should give U.S. equipment firms access to a standard of performance data that only the largest U.S. chipmakers can now provide their suppliers.

23. On the five-year development cycle for lithographic equipment, see "VLSI Lithography," EB (March 1, 1988), p. 69; also VLSI Research. SEMATECH's two-year equipment development target was noted by Paul Castrucci in an interview for this report (October 28, 1988).
24. Theoretical cycle time is the time needed to process a wafer from start to finish assuming continuous processing--i.e., that all equipment is usable, there are no queues, and set-up and transportation time is zero. In practice, no plant achieves all of these conditions. There are more than 500 wafer processing steps in 4Mb DRAM production. Actual cycle times may be several weeks.
25. NIST estimate. SEMATECH's availability/reliability, process control, and contamination control objectives are noted by Paul Castrucci in "The Semiconductor Technology Chain," a speech at the Dallas Techcon '88 conference (October 12, 1988). Cycle time targets were noted by A.S. Oberai, SEMATECH's Director of Strategic Planning at SEMI/SEMATECH's Presidents' Meeting (November 16, 1988) and in an interview for this report.
26. The U.S. Tax Code includes semiconductor manufacturing equipment in the five-year property category and allows accelerated depreciation by the double-declining balance method--i.e., 40 percent of a machine's purchase price can be written off in the first year, 24 percent in the second, and 14.4 percent in the third. Because semiconductor product life cycles are short and major equipment changes are needed for each new product generation, competitive manufacturing depends on making machines as productive as possible as quickly as possible.
27. SEMATECH' five-year strategic plan is regularly up-dated with the advice of the consortium's Strategic Assessment and Planning Group. Comprised of senior SEMATECH officials and outside experts, this group meets quarterly to assess and project foreign and domestic developments in semiconductor manufacturing technology. Final decisions on technology R&D and dissemination are made by SEMATECH's Board of Directors. Roughly 100 technology "deliverables" are now scheduled for transfer to member companies over the next five years.

28. Planarization usually refers to a process in which wafers are coated (e.g., with a thin layer of glass) to round the corners of etched circuit channels, thus helping to prevent cracks in the metal overlays that connect circuit segments in each device.
29. Material in this section is based chiefly on comments by Larry Novak, SEMATECH's Manager of Technology Transfer in an interview for this report (November 16, 1988).
30. Robert S. Williams, SEMATECH, case study prepared for the Harvard Business School (1988), p. 11.
31. The atmosphere in a Class-1 clean room is cleansed so that there is no more than one particle larger than 0.5 microns per cubic foot of air. An equivalent relationship is one particle the size of a dried pea per cubic mile of air.
32. On projected schedules for full scale production of 64K SRAMs and 4Mb DRAMs in the Austin fab, see p. 12. A status report on equipment arrivals was provided by Phase-I project managers Ashok Sinha and Gary Thornburg at SEMI/SEMATECH's Presidents Meeting (November 16, 1988). On sourcing for major pieces of equipment for the Phase-I fab line see "4MB DRAM, 64K SRAM Gear Ordered by SEMATECH," EN (December 12, 1988).
33. SEMATECH press release (May 31, 1988). Centers established in 1988 were at the University of Arizona (for contamination/defect control), UC/Berkeley for optical lithography, a New Jersey consortium of universities for plasma etching, the University of New Mexico for metrology, the Massachusetts Microelectronics Center for single wafer processing, and a Texas university consortium for manufacturing systems. Centers proposed for 1989 are in Florida, North Carolina, Wisconsin, and New York.
34. As reported in Dataquest monthly newsletter, I.C.USA (April 25, 1988), p.2, DOD faulted SEMATECH's initial 1988 work plan for reflecting the high-volume manufacturing interests of many of its members rather than the realities of the world semiconductor market. On movement in this market toward more specialized production by many small firms working closely with their customers, see "Falling Chips: Is a Big Federal Role the Way to Revitalize Semiconductor Firms," Wall Street Journal (WSJ) (February 17, 1987); also "America's New-Wave Chip Firms," WSJ (May 27, 1988); also Lawrence Stevens, "ASICs: An Industry Savior?," in Computer World (July 27, 1987), citing a Dataquest estimate that ASICs will account for 35 percent of all U.S. computer industry chip consumption in 1990; also CBO, op. cit., on projected rapid growth in demand for ASICs.

35. DARPA pressure on SEMATECH to address X-ray lithography sooner than originally planned is reported in "Report DARPA Presses SEMATECH," EN (April 25, 1988). On the cost of a full-scale national effort to develop commercial X-ray lithographic sources, see the report on Japan's \$1-billion joint industry-government program: "Experts Warn of U.S. Lag in Vital Chip Technology," New York Times (NYT) (December 12, 1988). On the risks of a major R&D commitment in X-ray technology, see DOE National Laboratories and the Semiconductor Industry: Continuing the Joint Planning, a report of the Manufacturing Studies Board and National Materials Advisory Board, (National Academy Press: Washington, D.C., 1987), pp. 9-11.
36. On DARPA's criticism of SEMATECH's initial operating plan and events surrounding the MOU signing see, EN (April 25 and May 2, 1988); also Dataquest, I.C.USA (April 25, 1988). Also Harvard case study, p. 21.
37. Comments of Craig Fields, DARPA's Deputy Director, in an interview for this report (December 9, 1988). William Bandy, DARPA's project officer for SEMATECH, described cooperative efforts to establish a structured planning cycle in an interview for this report (September 29, 1988).
38. 1989 Operating Plan. In SEMATECH's early plans, only 15-20 percent of projected spending was allocated to contract R&D. See "Defense Dept. May Flex Its Muscle With SEMATECH," Electronic Buyers News (October 5, 1987).
39. On the disintegrative influences affecting consortia see CBO, op. cit., pp. 50-52; also "Possible Justification for Federal Support to SEMATECH," an NSF staff paper (July 16, 1987).
40. SEMATECH's accomplishments were recounted in a briefing for Congressional staff and others by Pat O'Hagan, Director for Total Quality Deployment (September 15, 1988). A.S. Oberai and Turner Hasty, Director for External Resources, commented on member companies' growing interest in SEMATECH in an interview for this report (October 27, 1988). Bob Noyce's view on the importance of federal participation was expressed in an interview for this report (October 28, 1988).
41. On SEMATECH's extended effort to recruit top leadership, see "Hear Offer Lured Away SEMATECH CEO Choice," EN (May 2, 1988). SEMATECH Board member and IBM Vice President Sanford Kane attributes IBM's support for the consortium to its preference for local sourcing and interest in averting dependency on Japanese competitors for chips and chipmaking equipment (Harvard case, p. 10).

42. Comments at a briefing for the Advisory Council (November 15, 1988).
43. From SEMATECH's perspective, the relationship has evolved from "a sales mode to a more open spirit of mutual problem solving" (comments of Oberai and Hasty on October 27, 1988). SEMI/SEMATECH's Harrell speaks of suppliers operating in a "new business environment" (interview on November 15, 1988).
44. Comments of Hasty and Oberai (October 27, 1988); also Peter Mills, SEMATECH's Senior Vice President for Administration, in an interview for this report (October 28, 1988).
45. Examples of such arrangements include the recently announced joint venture by Texas Instruments and Hitachi to develop a 16Mb DRAM. The companies will share their chip technology but manufacture separately: "Texas Instruments, Hatachi in Chip Venture," NYT (December 23, 1988). In a well-publicized 1987 deal with Toshiba, Motorola agreed to exchange its most advanced chip technology over five years in return for Toshiba's help in penetrating the Japanese market (Business Week, April 20, 1987). The Business Week story notes that LSI Logic, National Semiconductor, and Advanced Micro Devices also have cooperative arrangements with Japanese firms. On joint venturing by U.S. and foreign equipment firms, see DOC, Competitive Assessment, p. 43.
46. Study by Dataquest, Inc., cited in "Japanese Solidify Dominance of Semiconductor Market," Washington Post (January 4, 1989).
47. On DRAM market reentry costs, see "The World of Silicon," Spectrum, p. 31. In "Motorola Resumes U.S. DRAM Production," EN reports that Motorola spent \$100 million to revamp its Mesa, Arizona fab (November 28, 1988). On planned Japanese capacity expansions, see "A New Japanese Push on Chips," NYT (November 11, 1988). Plans by Texas Instruments and and Micron Technology to add DRAM production capacity are noted in Business Week (January 9, 1989).
48. On JESSI, see Spectrum, p. 35; also Business Week (November 14, 1988). SORTEC is also discussed in Spectrum (p. 36). On the Opitcal IC project, see Bureau of National Affairs, Analysis and Reports, "U.S. Semiconductor Industry Hopes High That SEMATECH Will Boost Competitiveness In International Markets" (February 25, 1988), p. C-3.

PART II

1. October 28 interview. Craig Fields expressed DARPA's satisfaction with the consortium's revised operating plan in an interview for this report (December 9, 1988).

2. On the VHSIC program, see The Microelectronics Race, pp. 118-21; also Glenn McLoughlin and Nancy Miller, The U.S. Semiconductor Industry and the SEMATECH Proposal, (Congressional Research Service: April 23, 1987), p. 10; also Leslie Bruekner and Michael Borrus, "Assessing the Commercial Impact of the VHSIC Program," Berkeley Roundtable on the International Economy working paper (December 1984).
3. In Hearings of the Senate Government Affairs Committee (June 9, 1987), p. 75, Bob Noyce stated: "One of the concerns we have had in SEMATECH and possible government funding...is the level of micromanagement. We would like to see in any of these projects the ability to get things done by those who know what needs to be done...." CBO's report on SEMATECH, op. cit., p. 52, concludes: "SEMATECH's prospects will depend to a great extent on the willingness of the government to take a cooperative and, in many respects, passive role in the consortium, once SEMATECH's basic policies have been set."
4. Report to the Secretary of Defense, p. 53. The term "dual-use" refers to products and manufacturing capacity that can be applied to both commercial and defense needs.
5. Craig Fields (December 9, 1988).
6. DARPA's organizational culture is characterized by Craig Fields in testimony before the Senate Government Affairs Committee (June 9, 1987). DARPA's project officer for SEMATECH, William Bandy, describes his role as "making sure that the consortium is moving in the right direction, and otherwise becoming totally integrated in the process" (interview on September 30, 1988). Bandy has been especially active in the effort to establish a disciplined planning process, in the consortium's technical advisory committees, and as a link to related DARPA programs.
7. The Semiconductor Industry and the National Laboratories, pp. 2-3, 13, 16 on the research orientation of the national labs; pp. 2-3, 18-19 on the need for a national research agenda. The report calls for the creation of a National Advisory Committee on Semiconductors. It also gives a detailed account of the national lab resources that could support SEMATECH or a broader national effort to restore U.S. competitiveness in semiconductor manufacturing.
8. Material on SETECH supplied by Turner Hasty, SEMATECH's Director for External Resources.
9. Telephone conversation with Robert Scace, Deputy Director of the NIST Center for Electronics and Electrical Engineering (November 14, 1988).

PART III

1. Craig Fields notes that DARPA's support for SEMATECH is partly a function of the agency's ability to provide full project funding (interview on December 9, 1988). Shared management would be inconsistent with DARPA's internal operating practice which is to assign responsibility for a project's success or failure, along with significant decision-making authority, to a single project officer.
2. Comments of Turner Hasty in an interview for this report (October 28, 1988).
3. In an interview for this report, James Decker, Deputy Director of DOE's Office of Energy Research suggested that DOE could share SEMATECH funding and oversight responsibility with DARPA, but would not seek this responsibility. He also cautioned that any large scale reorientation of the national labs toward commercial R&D might jeopardize their basic research capability. The need for "some change in operating style on the part of the laboratories" is discussed in The Semiconductor Industry and the National Laboratories, p. 16. Congressional interest in tapping more of the labs' commercial potential is reflected in two bills introduced in the 100th Congress: H.R. 5132, introduced by Rep. Marilyn Lloyd whose district includes the Oak Ridge National Laboratory; and S. 1480, introduced by Sen. Pete Dominici, whose district includes the Sandia National Laboratory.
4. Material in this section is drawn partly from an NIST draft (October 26, 1988) of the semiconductor section of the President's report to Congress on federal technology policies as required by the 1988 Trade Act (Sec. 5141).
5. Material in this section is based on comments of Carl Hall, NSF's Deputy Director for Engineering, and Frank Huband, Director of NSF's Division of Engineering Technologies in an interview for this report (November 4, 1988).

PART IV

1. Comments of SEMATECH's Senior Vice President Peter Mills, in a telephone conversation (January 10, 1989). Bob Noyce commented on the importance of federal participation to industry confidence in SEMATECH at an interview for this report (October 28, 1988). DOD Under Secretary for Acquisitions Robert Costello pointed to industry financial commitment as a criterion for federal participation in SEMATECH and other consortia (Austin press conference;

November 15, 1988). Continued funding for SEMATECH at the \$100-million level is included in DOD's FY 1990 budget request and the President's FY 1990 Budget.

2. See, for example, "Need for High-Tech Consortia Stressed," NYT (January 12, 1989); also "Pentagon Seeks to Spur U.S. Effort To Develop 'High Definition' TV," WSJ (January 5, 1988); also "Consortia Urged to Develop Superconductors," Washington Post (January 4, 1989). In January 1989, DARPA set aside \$30 million to support two industry consortia to develop high definition television technology. In addition, a Presidential advisory panel proposed the creation of as many as six consortia to develop commercial applications for superconductors. Observers have suggested that the consortium approach may also have applications in other areas--e.g., X-ray lithography for semiconductor manufacturing, biotechnology, opto-electronics, and computer disk drives.