PUBLIC

UNITED STATES OF AMERICA
BEFORE FEDERAL TRADE COMMISSION

In the Matter of RAMBUS INCORPORATED, a corporation.	Docket No. 9302

COMPLAINT COUNSEL'S REPLY TO RESPONDENT'S PROPOSED FINDINGS OF FACT

Volume I

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Introductory Matter

Complaint Counsel files these Reply Findings in response to Respondent's Proposed Findings of Fact filed September 5, 2003.

The format of this document is intended to comply with the directions set forth in the Order on Post Trial Briefs, dated July 10, 2003. The Respondent's headings and numbered proposed findings are reproduced, single-spaced. Following each numbered proposed finding of the Respondent is Complaint Counsel's response, double-spaced.

These Reply Findings use the forms of citation set forth in Complaint Counsel's Proposed Findings of Fact filed September 5. In addition, the following forms of citation are used:

- Respondents's Proposed Findings of Fact are cited by paragraph, as follows: (RPF 507) or (RPF 743-45).
- These Complaint Counsel's Reply Findings are cited by paragraph, as follows: (CCRF 507) or (CCRF 743-45).

- Complaint Counsel's Proposed Findings of Fact are cited by paragraph, as follows: (CCFF 507) or (CCFF 743-45).

Complaint Counsel's responses follow.

* * *

I. INTRODUCTION.

1. There exists a standard-setting organization called the JEDEC Solid State Technology Association ("JEDEC"), which was throughout most of the 1990's an unincorporated activity within the engineering department of the Electronic Industries Association ("EIA"). (Rhoden, Tr. 289). JEDEC undertakes to adopt standards for semiconductor devices and related technologies. (Complaint, ¶ 14).

Response to Finding No. 1: Complaint Counsel does not disagree. For a more complete discussion of the history and purpose of JEDEC, *see* CCFF 200-208.

2. The particular JEDEC committee most relevant to this case is the "JC 42" committee, which has responsibility within JEDEC for many computer memory devices. (Complaint, ¶ 25). The members of JC 42 have included such computer memory manufacturers and users as Siemens (now Infineon), Micron, NEC, Samsung, Toshiba, IBM, Texas Instruments and Hewlett-Packard. (JX 10 at 1). The particular subcommittee most involved in this case is the "JC 42.3" subcommittee, whose focus throughout the 1990's was dynamic random access memory devices, or "DRAMs." (Complaint, ¶ 26).

Response to Finding No. 2: Complaint Counsel does not disagree that for purposes of this case the most relevant JEDEC committee is the JC 42 Committee. Complaint Counsel does not disagree that the JC 42.3 subcommittee figures prominently in the DRAM standard-setting activity that is at the core of this case (*see* CCFF 500-658). However, there are other relevant JEDEC committees and subcommittees affected by the Rambus misconduct, including the JC 16 Committee and the JC 42.5 Subcommittee. Discussions of technologies in both these groups were monitored and reported upon by Rambus representatives during the course of the participation by Rambus as a JEDEC member, without disclosure of any claims of Rambus intellectual property in the matters under discussion. (*See* CCFF 557, 601, 645, 1031, 3171).

Complaint Counsel does not disagree that the listed computer memory manufacturers were members of the JEDEC JC 42 Committee. However, the membership of the JC 42 Committee and subcommittees was not limited to these particular firms or to memory manufacturers alone; the membership also included manufacturers of other products such as computer systems (e.g. Apple Computer, AT&T, Cray Research, Sharp, Sun Microsystems), and and chipset and other component manufacturers (e.g. Intel, AMD, VLSI, ATI, nVidia), as well as Rambus itself, which never intended to and did not engage in the manufacture of any semiconductor product. (JX0010 at 1; CCFF 705, 825).

3. A DRAM differs from other types of memory devices in part because it is "dynamic," that is, the memory cells it contains must be refreshed periodically in order to retain their values. (Rhoden, Tr. 266-7, 279).

Response to Finding No. 3: Complaint Counsel does not disagree. For a more complete discussion of the characteristics of DRAM memory, *see* CCFF 10-24.

4. Respondent Rambus Inc. ("Rambus") is a company that, among other things, develops and licenses memory technologies to companies that manufacture semiconductor memory devices. (First Set of Stipulations, April 24, 2003, p. 1, item 1).

Response to Finding No. 4: Complaint Counsel does not disagree. For a more complete discussion of the founding and early business strategy of Rambus, *see* CCFF 700-13, 732-66.

5. Rambus attended its first JEDEC 42.3 meeting as a guest in December 1991. (JX 10 at 2; CX 2054, Mooring Depo. Tr., 44). Rambus formally joined JEDEC in early 1992. (CX 601 at 1).

Response to Finding No. 5: Complaint Counsel does not disagree that Rambus first attended a meeting of the JC 42.3 Committee as a guest in early December 1991, and that it applied for membership in JEDEC shortly thereafter. *See* CCFF 871-78. The handwritten notations on the Rambus membership application indicate that Rambus paid its initiation fee on December 10, 1991 (just 5 days after the December 1991 meeting) and was formally added to the

roll of JEDEC members in December 1991. (CX0601 at 1 ("OK to add ... paid 12/10/91"; "Added 12/20/91 Heather")).

6. Rambus attended its last JEDEC 42.3 meeting in December 1995. (Crisp 8/10/01 Micron Depo. Tr., 853:18-854:1).

Response to Finding No. 6: Complaint counsel does not disagree that the December 1995 meeting of the JC 42.3 Committee was the last such meeting that was attended by Rambus representative Richard Crisp. (CCFF 1078-82). Shortly thereafter, in December 1995 and January 1996, Rambus made a decision to cease participation in standards organizations including JEDEC. (CCFF 1083-91). Although Rambus did not attend any further JEDEC meetings, it continued to receive written materials from JEDEC, including minutes of a meeting of the JC 42.3 Committee in January 1996. (CCFF 1096-99).

7. After receiving a bill for 1996 dues, Rambus sent a letter confirming its withdrawal from JEDEC in June 1996. (CX 887 at 1).

Response to Finding No. 7: This proposed finding is inaccurate and misleading insofar as it suggests that the Rambus letter withdrawing from JEDEC was "confirming" some earlier communication with the organization. The text of the June 17, 1996, letter, which is the only cited record reference in support of the proposed finding, states that the letter by Rambus was to "inform" JEDEC that Rambus was "not renewing its membership in JEDEC." (CX0887 at 1). There is no record evidence that Rambus acted earlier to withdraw from JEDEC.

Rambus made an internal decision by January 1996 to cease attending meetings of standards organizations including JEDEC, but Rambus continued to receive JEDEC minutes and to circulate them to staff members (including Tony Diepenbrock, for the purpose of ensuring that Rambus obtained patent coverage over competing technologies). (CCFF 1083-91, 1096-99; CX0831). Prior to sending the June 17, 1996, withdrawal letter, a number of drafts had been prepared reflecting more complete disclosures of Rambus patents than were contained in the final

version of the letter sent to JEDEC. (CCFF 1113; *see* CCFF 1109-14). The version of the withdrawal letter as sent to JEDEC included a list of patents that had been issued or assigned to Rambus, but omitted any listing of patent applications. (CCFF 1111). The withdrawal letter also omitted any reference to the '327 patent that had been issued to Rambus dealing with dual-edge clock technology, which had been the subject of repeated discussion at JEDEC. (CCFF 1111, 1114). The same day that Rambus sent its withdrawal letter to JEDEC omitting reference to the '327 patent, Rambus sent a letter to its outside patent counsel seeking an enforcement-readiness opinion with respect to the '327 patent. (CCFF 1112; *see* CCFF 1100-08).

8. The Complaint in this matter asserted that, while a member of JEDEC, Rambus representatives observed efforts at JEDEC to promulgate an industry standard for a synchronous DRAM device called "SDRAM." (Complaint, ¶ 40). The Complaint asserted that Rambus should have disclosed to JEDEC that it had filed or intended to file or amend patent applications relating to certain features of the SDRAM device standardized by JEDEC. (Complaint, ¶¶ 55-56).

Response to Finding No. 8: The first sentence of this proposed finding is an accurate but incomplete summarization of ¶ 40 of the Complaint, which speaks for itself. The second sentence of this proposed finding inaccurately summarizes the referenced ¶¶ 55-56 of the Complaint, which contain no reference to what Rambus "should have disclosed." The referenced portion of the Complaint states accurately that Rambus never disclosed to JEDEC the fact that, throughout the duration of its membership in the organization, Rambus had on file with the PTO, and was actively prosecuting, patent applications that, in its view, either covered or could easily be amended to cover elements of the existing and future SDRAM standards (Complaint ¶ 55), and that among the specific technologies adopted or proposed for inclusion in the SDRAM standards during this period, that Rambus believed were covered by its then-pending patent applications or could be covered through amendments to such applications, were the four technologies that are involved in the relevant technology markets as set forth in the Complaint. (Complaint ¶ 56).

9. After discovery had closed, and shortly before trial began, the parties stipulated that "[p]rior to the adoption of the JEDEC SDRAM standard in 1993, Rambus had no claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard." (First Set of Stipulations, April 24, 2003, p. 2, item 9).

Response to Finding No. 9: This proposed finding accurately repeats the text of the referenced stipulation. Despite the belief of Rambus that the JEDEC SDRAM standard embodied its intellectual property (*see, e.g.*, CCFF 811, 853, 862-66) and despite its efforts to amend and perfect its patent applications to cover crucial components of the SDRAM standard by filing, inter alia, an amendment to its '651 application on May 17, 1993, a little more than a week before the JEDEC Council adopted the SDRAM standard (*see, e.g.*, CCFF 809, 810, 832, 834, 958), prior to the time the JEDEC SDRAM standard was formally adopted in November 1993 (CCFF 977) Rambus had not successfully amended its patent applications to include claims that clearly read on the content of the SDRAM standard.

However, throughout the time Rambus was a member of JEDEC it continued its efforts to perfect its patent claims and did amend its patent applications to state claims that clearly read on crucial elements of the SDRAM standard. These include the January 1995 amendments to Rambus patent application 07/847,961 (the '961 application), which cover the the programmable burst length and programmable CAS latency features of JEDEC-compliant SDRAMs. (CCFF 1125-63). In addition, the June 1995 amendments to Rambus patent application no. 08/469,490 (the '490 application), which was a continuation of the '961 application, contained claims covering a JEDEC-compliant SDRAM, the use of such an SDRAM, and a computer system incorporating a JEDEC-compliant SDRAM. (CCFF 1164-82).

During the time Rambus was a member of JEDEC it also made efforts to perfect its patent claims pertaining to technologies under discussion at JEDEC for inclusion in the "next generation" SDRAM standard, which ultimately became the DDR standard. Amendments dated June 28,

1993, to Rambus patent application 07/847,692 (the '692 application) contained claims covering a phase lock loop (PLL) incorporated into a JEDEC-complaint SDRAM. (CCFF 963-966, 1183-1198). This is a technology that was discussed at JEDEC during the period Rambus was a member, including in a September 14, 1994, presentation by NEC Corporation to JEDEC Committee 42.3 proposing that the SDRAM standard incorporate an on-chip PLL. (CCFF 1009-17, 1186; *see* CCFF 843, 855-57, 1072, 1079, 1080). The amendments to the Rambus '692 patent application were specifically intended by Rambus to target "future SDRAMs" (CCFF 963) and had been discussed by Rambus executives with Rambus patent counsel as early as September 1992. (CCFF 932-36).

On September 6, 1994, while it was a JEDEC member, Rambus filed a preliminary amendment to Rambus patent application 08/222,646 (the '646 application) that contained claims that covered a JEDEC-compliant SDRAM incorporating a proposed dual-edged clocking feature. (CCFF 1008, 1199-1215). Dual-edge clocking was another feature that had long been under discussion at JEDEC in connection with the "next generation" SDRAM standard, including discussions that began before and continued throughout the time that Rambus was a member of JEDEC. (CCFF 522, 524-26, 581, 585, 623-25, 628-33, 635, 637-40, 1072, 1079, 1200-03). The United States Patent and Trademark Office sent Rambus patent counsel a Notice of Allowance of claims with respect to the '646 application on October 6, 1995, while Rambus was a JEDEC member; a Notice of Allowance occurs when the patent office has reason to believe that claims in a particular application should be issued. (CCFF 1076).

The '646 application issued as Patent No. 5,513,327 (the '327 patent) to Rambus on April 30, 1996, before Rambus withdrew as a JEDEC member. (CCFF 1074-1077, 1214). The Rambus '327 patent contains claims covering the most feasible way to implement the dual-edged clocking feature, as proposed to JEDEC in May 1992, December 1995 and March 1996, in a JEDEC-

compliant SDRAM, and also contains claims covering DDR SDRAM as ultimately implemented in JEDEC Specification JESD 79 (June 2000). (CCFF 1216-37).

10. The Complaint also alleged that JEDEC considered improvements to the SDRAM standard in the early and mid-1990s, and that these discussions ripened into the formal development of a new standard, called "DDR SDRAM," in the 1996-1999 time period. (Complaint, ¶¶ 27-28).

Response to Finding No. 10: This proposed finding is an inaccurate summarization of ¶¶ 27-28 of the Complaint, which among other things discuss the issuance of the DDR SDRAM standard in August 1999 after work by JEDEC that commenced at least as early as 1993. The cited portion of the Complaint makes no reference to any "ripening" of discussions into any "formal" development of a new standard in the 1996-1999 time period. The development of the JEDEC DDR SDRAM standard is discussed in detail at CCFF 500-658.

11. The Complaint asserted that Rambus should have disclosed to JEDEC that it had filed or intended to file or amend patent applications relating to certain features of the DDR SDRAM device standardized by JEDEC. (Complaint, ¶¶ 64-70).

Response to Finding No. 11: This proposed finding is an inaccurate summarization of ¶¶ 64-70 of the Complaint, which contain no reference to what Rambus "should have disclosed." The referenced portion of the Complaint, which speaks for itself, among other things describes the conduct of Rambus in monitoring the work of JEDEC in connection with certain features that ultimately were embodied in the JEDEC DDR standard, and discusses the failure by Rambus to disclose its belief that it had intellectual property covering these features, its efforts to secure patent protection for them, or its having secured patent protection in the form of the '327 patent. The obligations of JEDEC members to act in good faith, avoid anticompetitive results, and disclose intellectual property claims related to JEDEC work are discussed at CCFF 300-443.

12. The Complaint alleged that while it was a JEDEC member, Rambus had misled JEDEC members into believing that it had no actual or potential intellectual property claims in the technologies being considered for standardization by JEDEC. (Complaint, ¶ 71).

Response to Finding No. 12: This proposed finding is an incomplete summarization of ¶ 71 of the Complaint. That portion of the Complaint alleges that Rambus's participation in JEDEC, coupled with its failure to make required patent-related disclosures, conveyed a materially false and misleading impression – namely, that JEDEC, by incorporating into its SDRAM standards technologies openly discussed and considered during the tenure of Rambus in the organization, was not at risk of adopting standards that Rambus could later claim to infringe upon its patents. This allegation of the Complaint is supported by the record evidence. (*See* CCFF 300-443, 1238-1276).

13. The Complaint alleged that had Rambus disclosed to JEDEC that it had filed or intended to file patent applications relating to technologies being considered for standardization, JEDEC would have incorporated alternative technologies into its standards that avoided Rambus's intellectual property claims. (Complaint, ¶¶ 62, 65, 69).

Response to Finding No. 13: This proposed finding is an inaccurate summarization of the referenced portions of the Complaint. The Complaint alleges that had Rambus made timely disclosure, such disclosure likely would have impacted the content of the standards, the terms on which Rambus would later be able to license any pertinent patent rights, or both. (Complaint, ¶¶ 62, 65, 69). This allegation of the Complaint is supported by the record evidence. (*See* CCFF 2100-2464).

14. The Complaint asserted that by the use of "anticompetitive and exclusionary acts and practices," Rambus has obtained monopoly power in various markets and submarkets in violation of section 5 of the FTC Act, 15 U.S.C. § 45. The Complaint also asserted that Rambus has engaged in the aforementioned acts and practices with the specific intent to monopolize various markets and submarkets, in violation of section 5 of the FTC Act. (Complaint, ¶¶ 122-3).

Response to Finding No. 14: This proposed finding is an incomplete summarization of the referenced portions of the Complaint. The Complaint charges as the first

violation that Rambus has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices, whereby it has obtained monopoly power in the synchronous DRAM technology market and narrower markets encompassed therein, in violation of Section 5 of the FTC Act. (Complaint ¶ 122). The Complaint charges as a separate second violation that Rambus has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices, with a specific intent to monopolize the synchronous DRAM technology market and narrower markets encompassed therein, resulting, at a minimum, in a dangerous probability of monopolization in each of the markets, in violation of Section 5 of the FTC Act. (Complaint ¶ 123). The Complaint charges as a separate third violation that Rambus has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices, whereby it has unreasonably restrained trade in the synchronous DRAM technology market and narrower markets encompassed therein, which acts and practices constitute unfair methods of competition in violation of Section 5 of the FTC Act. (Complaint ¶ 124). The Complaint alleges these as three separate violations. *See* Complaint Counsel's Post-Hearing Brief at 15-19.

15. Rambus's Answer denied the material allegations of the Complaint and asserted that the evidence would show that JEDEC's rules and policies did not impose, and were not commonly understood to impose, the disclosure obligations set out in the Complaint. (Answer, pp. 1-2).

Response to Finding No. 15: The first clause of this proposed finding is inaccurate; while the Rambus Answer did in large part deny the allegations of the Complaint, it contained admissions of various material facts that are relevant to the resolution of this matter. (*See* CCFF 701, 871, 1083, 1085, 1088, 1755, 1950, 1958, 1992, 1995, 1999, 2003, 2016, 2019-20, 2022-23, 2026, 3190, 3212). The balance of the proposed finding accurately summarizes one of the assertions made by Rambus in its Answer. The assertion is repeated here without record support, and is contradicted by the record evidence. (*See* CCFF 300-443).

16. Rambus also asserted in its Answer that the evidence would show that it did not have, until after it had left JEDEC, any undisclosed patents or patent applications that contained claims reading on devices manufactured in accordance with any JEDEC standard. (Answer, p. 2).

Response to Finding No. 16: This proposed finding accurately summarizes one of the assertions made by Rambus in its Answer. The assertion is repeated here without record support, and is contradicted by the evidence in the record. (*See* CCFF 1122-1237).

17. Rambus also asserted in its Answer that the evidence would show that JEDEC did not rely on any purported silence on Rambus's part at JEDEC meetings and instead chose to adopt certain technologies because of the cost/performance advantages of those technologies and the absence of reasonable alternatives. (Answer, p. 2).

Response to Finding No. 17: This proposed finding accurately summarizes one of the assertions made by Rambus in its Answer. The assertion is repeated here without record support, and is contradicted by the evidence in the record. (*See* CCFF 2100-2464).

18. Rambus's Answer asserted that in light of the absence of a duty to disclose, in light of the absence of pending claims reading on JEDEC standards, and in light of the other evidence to be considered at trial, it would be clear by the close of trial that Rambus's alleged failure to disclose its potential intellectual property claims had no anticompetitive effect in any market and that Rambus had not violated section 5. (Answer, pp. 1-3).

Response to Finding No. 18: This proposed finding accurately summarizes several of the assertions made by Rambus in its Answer. The assertions are repeated here without record support, and are contradicted by the evidence in the record. (*See* CCFF 2500-3060).

II. PROCEDURAL BACKGROUND

19. The Complaint in this matter issued on June 18, 2002. (Complaint, p. 37, available at www.ftc.gov/os/adjpro/d9302/020618admincmp.pdf).

Response to Finding No. 19: Complaint Counsel does not disagree.

20. Rambus filed its Answer on July 29, 2002. (Answer, p. 49, available at www.ftc.gov/os/adjpro/d9302/020729arri.pdf).

Response to Finding No. 20: Complaint Counsel does not disagree.

21. An initial scheduling order was issued by Chief Administrative Law Judge James P. Timony on August 6, 2002. (Available at www.ftc.gov/os/adjpro/d9302/020806so.pdf). The

Scheduling Order was subsequently amended by stipulation and order on October 31, 2002. (Available at www.ftc.gov/os/adjpro/d9302/02103aljrevisedschedulinorder.pdf).

Response to Finding No. 21: Complaint Counsel does not disagree.

22. After Judge Timony retired as of January 29, 2003, the matter was assigned to Chief Administrative Law Judge Stephen J. McGuire on February 28, 2003. (Available at www.ftc.gov/os/adjpro/d9302/030228ordreassigncase.pdf).

Response to Finding No. 22: Pursuant to the cited order, the Honorable James P. Timony, who had not retired at the time he signed the order, reassigned the matter to the Honorable Stephen J. McGuire on February 28, 2003.

23. Trial commenced on April 30, 2003.

Response to Finding No. 23: Complaint Counsel does not disagree.

24. The last day on which testimony was received was August 1, 2003. The parties subsequently submitted a substantial volume of deposition designations. The trial transcript exceeded 11,000 pages.

Response to Finding No. 24: Complaint Counsel does not disagree.

25. The parties filed and served Proposed Findings of Fact and Conclusions of Law on September 5, 2003.

Response to Finding No. 25: Complaint Counsel does not disagree.

26. The parties filed and served Reply Findings of Fact and Conclusions of Law on September 26, 2003.

Response to Finding No. 26: Neither party filed and served its reply findings on this date.

III. RAMBUS AND ITS INVENTIONS

A. The Computer Industry Faced A Memory Bottleneck

27. Dr. Michael Farmwald, one of the two founders of Rambus, received his bachelor's degree in mathematics from Purdue University in 1974. (Farmwald, Tr. 8058). He then went on to earn a Ph.D. in computer science from Stanford University in 1981. (Farmwald, Tr. 8059). While a graduate student at Stanford, Dr. Farmwald was in charge of a supercomputer project at Lawrence Livermore National Labs. (Farmwald, Tr. 8059). After obtaining his Ph.D, he continued to work at Livermore for four years and then founded a company called FTL (which

stood for "Faster Than Light"), whose goal was to build very fast computers. (Farmwald, Tr. 8060-61). In 1988, Dr. Farmwald went to the University of Illinois to teach in the computer science department. (Farmwald, Tr. 8063-64).

Response to Finding No. 27: Complaint Counsel does not disagree.

28. While working as a professor at the University of Illinois, Dr. Farmwald realized that developments in microprocessor technology would lead to significant speed increases in microprocessors while memory chip performance would not keep up. (Farmwald, Tr. 8063, 8067). He recognized that the result of these trends would be a "bottleneck" – memory technology would limit computer system performance. (Farmwald, Tr. 8068-69).

Response to Finding No. 28: Complaint Counsel does not disagree. However, it was a general perception in the DRAM industry (not Dr. Farmwald's alone) that new generation of memory was needed because the industry anticipated that microprocessor and computer speeds would increase and the industry demanded memory that could operate at the same speeds. (CCFF 502, 504).

29. "Moore's law," named after Intel founder Gordon Moore, predicts that processor speeds will increase by a factor of four every three years. (Farmwald, Tr. 8068). This "law" has held true for over the last two decades. (Farmwald, Tr. 8068). The performance of DRAMs, however, was increasing at a lesser rate; while DRAMs were fast in comparison to microprocessors in the early 1980s, as an historical matter, DRAM performance had increased very slowly over time. (Farmwald, Tr. 8072).

Response to Finding No. 29: Complaint Counsel does not disagree. *See* CCFF 502, 504.

30. Graphing predicted microprocessor speeds against memory performance, Dr. Farmwald predicted an ever increasing gap between microprocessor performance and DRAM performance. (Farmwald, Tr. 8071-73). To meet the memory needs of future microprocessors, computer designers would either have to use a large number of DRAM working in parallel or obtain faster DRAM.

Response to Finding No. 30: Complaint Counsel has no specific response to the first sentence of this proposed finding. However, the second sentence of the proposed finding lacks any reference to the record. Complaint Counsel submits that this portion of the finding

should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

31. Assuming that the predicted DRAM speeds were not improved, Dr. Farmwald projected that the number of DRAMs needed to support future microprocessors would become extremely large over time. (Farmwald, Tr. 8073).

Response to Finding No. 31: Complaint Counsel does not disagree.

32. The increasing number of DRAMs needed to support faster computers was also consistent with Dr. Farmwald's experience that microprocessors were demanding higher and higher bandwidth memory systems ("bandwidth" being the amount of information that can be transferred over a specific period of time). (Farmwald, Tr. 8076-79).

Response to Finding No. 32: Complaint Counsel does not disagree. The need to accommodate increasing processor speeds was perceived generally in the industry. (*See* CCFF 502-504)

33. Dr. Farmwald also plotted the projected price for computers, which showed that the cost for computer systems was dropping over time. (Farmwald, Tr. 8074-75 (illustrated by DX 251)). Comparing these projected costs with the number of DRAMs that would be required to support the bandwidth needs of faster microprocessors, Dr. Farmwald knew that "there was something broken" – the costs of the thousands of DRAMs needed at higher microprocessor speeds would prevent the decline of computer system prices. (Farmwald, Tr. 8075-76). Later, a 1992 Rambus "Corporate Backgrounder" described the issue: "One of the most serious problems is the chronic speed mismatch between processors and main memory. Designers refer to this as the memory bottleneck. The data transfer rates of memory ICs lag far behind a processor's ability to handle the data." (RX 81 at 4).

Response to Finding No. 33: Complaint Counsel has no specific response.

34. To meet the higher bandwidth needs of microprocessors without the overwhelming cost of thousands of DRAMs, DRAM performance had to increase at a higher rate. (Farmwald, Tr. 8076).

Response to Finding No. 34: Complaint Counsel does not disagree.

35. Years later, Dr. Farmwald's 1988 observations were recognized by others in the industry. For example, an April 1992 Siemens internal memorandum states that "[a]s a result of the trend toward increasingly faster RISC and CISC processors, the DRAM interface has become more and more of a problem for system developers. In order to eliminate this data transmission rate bottleneck, various competing concepts regarding the design of newer DRAMS have emerged . . . ." (RX 285A at 1).

Response to Finding No. 35: Complaint Counsel has no specific response.

36. Similarly, an October 1992 article published in IEEE Spectrum warned, "If the price-to-performance ratio of computer systems is to keep improving, the gap in speed between processors and memory must be closed." (RX 329 at 1). IEEE Spectrum is the overall general magazine for the IEEE, a professional organization of electronic and electrical engineers. (Prince, Tr. 8972-3). The article went on to explain that "the accepted dynamic RAM (DRAM) architectures and solutions have been pushed to their limits. A basic change in architecture seems the only way to obtain an urgently needed increase in memory speed." (RX 329 at 1). This article reflected a general discussion within the industry in 1992 that computer companies needed faster DRAMs. (Prince, Tr. 8977-78).

Response to Finding No. 36: Complaint Counsel has no specific response.

37. Another article in the October 1992 IEEE Spectrum flatly stated, "If dynamic RAMs and processors are to trade data at close to top speed, the interface between them must be re-engineered. . . . None of the types of interfaces now popular can do this while conserving power and cost to the desired degree." (RX 333 at 1).

Response to Finding No. 37: Complaint Counsel does not disagree.

38. In February 1994, Dr. Betty Prince, a long-time consultant in the DRAM industry and the author of five books on DRAM technologies (Prince, Tr. 8970-72), wrote in an article published in IEEE Spectrum that "[t]he mismatched bandwidths of fast processors and the slower memory chips they must employ are a problem of long standing. Processors now as always require more data per unit time than many standard memory chips have been designed to provide." (RX 465 at 1). She also provided a graph showing that this performance gap was increasing over time. (RX 465 at 1). Dr. Prince agreed that the performance gap she wrote about created a bottleneck. (Prince, Tr. 8990-91).

Response to Finding No. 38: Complaint Counsel does not disagree.

39. Intel saw the memory bottleneck coming at least as early as 1995, and the recognition of this bottleneck prompted Intel to investigate various memory technologies in an effort to remedy the situation. (MacWilliams, Tr. 4929-30).

Response to Finding No. 39: Complaint Counsel does not disagree.

40. Richard Heye, the Vice President and General Manager of the Microprocessor Business Unit at AMD (Heye, Tr. 3615), analogized how the continued improvements in microprocessor performance mandate faster memory and improvements of other parts of a computer system to placing a high-performance engine into an ill-fitting frame:

> "The best way to describe it is by analogy. Another way to look at the microprocessor, if that's your high performance of the car, and as you continue to improve and improve your engine on the car, you've got to improve the rest of the car to take advantage of

> that engine. So, for example, you take a Porsche engine, drop it into a Ford pick-up truck, that Ford pick-up truck is just not going to perform like a Porsche that has the exact same engine. So, all the other stuff that Porsche does to make that car run really well, Ford pick-up trucks don't have that.
>
> So, it's to the same extent, is that if the performance of my processor keeps getting better and better and better, that the components of the system which feed the microprocessor need to also get better and better and better to take advantage of the technology of the microprocessor."

(Heye, Tr. 3651-52).

Response to Finding No. 40: Complaint Counsel does not disagree.

B. The Farmwald and Horowitz Inventions Solved the Problem.

1. Dr. Farmwald Enlists Dr. Horowitz.

41. Determined to solve the memory bottleneck problem, in 1988, Dr. Farmwald conceived the general idea of a new memory interface and protocol (an organization of the bits and timing of bits transferred by a memory chip) that would allow a single DRAM chip to have higher performance than a board Dr. Farmwald had designed containing 320 existing DRAM chips. (Farmwald, Tr. 8086-88).

Response to Finding No. 41: Complaint Counsel does not disagree. For a more complete discussion of the founding of Rambus, *see* CCFF 700-709.

42. In order to progress beyond his initial ideas, however, Dr. Farmwald realized that he needed the assistance of an expert in circuit design. (Farmwald, Tr. 8089). Dr. Farmwald sought the help of a former colleague – Dr. Mark Horowitz (a professor at Stanford). (Farmwald, Tr. 8089-90).

Response to Finding No. 42: Complaint Counsel does not disagree. For a more complete discussion of the founding of Rambus, *see* CCFF 700-709.

43. Dr. Horowitz had completed both his bachelors and masters degrees in electrical engineering from MIT in four years, receiving the degrees in 1978. (Horowitz, Tr. 8477). He then went on to earn a Ph.D. in integrated circuit design from Stanford University in 1983. (Horowitz, Tr. 8480). Aside from a year's leave of absence to work on what became Rambus, Dr. Horowitz has been a professor in the electrical engineering and computer science departments at Stanford University since the mid-1980s. (Horowitz, Tr. 8476). Dr. Horowitz currently holds two endowed chairs at Stanford. (Horowitz, Tr. 8482).

Response to Finding No. 43: Complaint Counsel does not disagree, except insofar as it omits the fact that Dr. Horowitz testified that after obtaining his degree at MIT, he worked at Signetics for one year before pursuing his Ph.D. (Horowitz, Tr. 8477-8480).

44. Dr. Farmwald convinced Dr. Horowitz to take a year's leave from Stanford to further explore their ideas. (Farmwald, Tr. 8092-93). Starting in the spring of 1989, the two worked from Dr. Horowitz's Palo Alto home. (Farmwald, Tr. 8093-94).

Response to Finding No. 44: Complaint Counsel does not disagree. For a more complete discussion of the founding of Rambus, *see* CCFF 700-713.

45. Dr. Horowitz's goal in working on what was to become Rambus was to build the fastest possible DRAM interface. (Horowitz, Tr. 8486). Drs. Horowitz and Farmwald determined that 500 megahertz DRAM operation might be possible, and they worked toward that goal. (Horowitz, Tr. 8505-06).

Response to Finding No. 45: Complaint Counsel does not disagree. For a more complete discussion of the founding of Rambus and its early technology, *see* CCFF 700-731.

C. Farmwald And Horowitz Formed Rambus To Promote Their Inventions As An Open Standard.

46. Early on, Dr. Farmwald and Professor Horowitz recognized that any company they formed would not be able to actually manufacture the DRAM parts that they were designing; a DRAM manufacturing facility costs a half a billion dollars. (Farmwald, Tr. 8095). Given this limitation, in order to commercialize their inventions, "the only possible business model that made any sense was to patent it, convince others to build it, and charge them royalties." (Farmwald, Tr. 8095). They formed Rambus with that limitation in mind. (Farmwald, Tr. 8247-48).

Response to Finding No. 46: Complaint Counsel does not disagree.. For a more complete discussion of the founding of Rambus, *see* CCFF 700-709.

47. Rambus's "Business Strategy," as reflected in a revised business plan prepared in November 1990 by Geoff Tate, was to develop its technology and "[p]rotect the intellectual property rights to the technology through a basic, broad patent filed in all major industrial nations and follow up with additional patents on inventions created during the development of the technology. Further protect the intellectual property through signing nondisclosures with all parties exposed to the technology." (RX 1091 at 1). As that same business plan reflects, Rambus implemented this strategy by filing its original patent application in 1990. (RX 1091 at 4). The original application had "been reviewed by all partners who've signed and several others and found to be a strong, broad patent with high odds of being issued largely as filed." (RX 1091 at 4; *see also* Farmwald, Tr. 8175-76).

Response to Finding No. 47: This proposed finding is accurate but incomplete. The document quoted also contemplated that Rambus, in addition to the steps set forth above, would "only license partners to use the technology in a specific manner specified by Rambus (the Rambus Interface). Result: impossible or very difficult for anyone to develop a competitive technology to Rambus." (RX1091 at 1). For a more complete discussion of the early Rambus business plan, *see* CCFF 734-35.

48. An early slide presentation that Drs. Farmwald and Horowitz used with venture capitalists set forth the business model. (RX 82 at 18; Farmwald, Tr. 8141, 8149-50). Rambus would sell its technology directly to semiconductor companies and computer companies, and it would earn revenue from consulting (working with the DRAM companies to implement the technology) and royalties (payment for the use of Rambus's intellectual property in the resulting products). (RX 82 at 18; Farmwald, Tr. 8150).

Response to Finding No. 48: Complaint Counsel notes that Dr. Farmwald testified that RX82 at 18 "pretty much" set forth the early Rambus business model. (Farmwald, Tr. 8149). For a more complete discussion of the Rambus early efforts to fund its operation, *see* CCFF 710-713.

49. Rambus's strategy was to make its technology a *de facto* standard. As Andreas Bechtelsheim, one of the founders of Sun Microsystems testified, a DRAM that is manufactured by multiple companies is a "standard" regardless of whether or not it has been officially standardized by JEDEC or some similar body. (Bechtelsheim, Tr. 5757-58). Rambus planned for its technology to be widely used throughout the industry: "It was the part everybody used. There was a specification. Everybody would implement that specification and they would all be compatible with each other, so they're standard parts you could interchange one for the other." (Farmwald, Tr. 8163).

Response to Finding No. 49: Complaint Counsel does not disagree. *See* CCFF 732-33.

50. To accomplish this, Rambus intended to "license it to everybody " so that every DRAM manufacturer could manufacture the part. (Farmwald, Tr. 8097). As a 1989 draft business plan explained, Rambus hoped to establish a *de facto* standard "by offering all interested DRAM and CPU vendors a sufficiently low licensing fee (2%) that it will not be worth their time and effort to attempt to circumvent or violate the patents." (RX 15 at 9). Dr. Farmwald explained, "We were going to try and find customers for our parts, big customers, and we were going to try

and license all the DRAM makers to build our part to supply those customers," which would lead to *de facto* standardization. (Farmwald, Tr. 8124-25).

Response to Finding No. 50: Complaint Counsel does not disagree, though the record shows that Rambus intended to use a program of phased licensing and promotion of its proprietary RDRAM technology in order to induce the industry to adopt its proprietary technology as the industry standard. (CCFF 736). For a more complete discussion of the early Rambus efforts in this regard, *see* CCFF 736-45.

51. Rambus's plan was for its technology to be an "open standard"; it refused to license its technology on exclusive terms. (Farmwald, Tr. 8185; RX 25 at 16 ("Second sources are important for all concerned")). An "open standard" in the DRAM industry is a standard for which any patents that apply to it are available on reasonable and non-discriminatory terms. (Bechtelsheim, Tr. 5897; CX 2112, Mooring Depo. at 190-91; Kelly, Tr. 1778; Rhoden, Tr. 301). Rambus wanted to avoid what happened to the Sony Betamax, which was hampered in the market by restrictive licensing. (Farmwald, Tr. 8165). Instead, Rambus's goal was to license its technology "openly and fairly to everybody so everyone is on equal footing with a relatively low royalty." (Farmwald, Tr. 8165-66).

Response to Finding No. 51: Complaint Counsel does not disagree that Rambus intended to seek licenses throughout the DRAM industry for its proprietary technology, through a program of phased licensing and promotion. (CCFF 736-45). The use of the term "open standard" to describe this objective, however, is different from the term "open standard" as understood by JEDEC and its members as a purpose of the organization, which are standards free from hidden or restrictive intellectual property rights. (CCFF 265, 300-304).

The early business plans of Rambus indicate that it was aware that it would be necessary early on to charge lower royalties in order foster acceptance of its proprietary technology. Rambus recognized that there was a "trade-off of royalty size vs. incentive to develop alternatives" to the Rambus technology (CX0533 at 14), and initially intended to offer licenses at "[l]ow enough royalties to discourage 'rolling your own.'"(CX0533 at 15). However, early planning also suggests that once Rambus was established as an industry standard, Rambus intended to charge

larger royalty payments. (CX0533 at 19 ("RamBus must be established as a standard to effect large royalty payments.")).

Contrary to the assertion made in this proposed finding, the overwhelming weight of the contemporaneous record evidence demonstrates that the Rambus business plan was not consistent with licensing its technology to others on reasonable and non-discriminatory terms. (CCFF 1091, 2419-32).

52. To ensure that the Rambus technology was standardized, i.e., that parts from one manufacturer were interchangeable with parts from another manufacturer, Rambus planned to cooperate with its partners (i.e., the licensees who would manufacture the devices) to ensure that feedback was propagated to all partners so that everyone would use the same good ideas instead of creating customized parts. (Farmwald, Tr. 8148; RX 82 at 17).

Response to Finding No. 52: Complaint Counsel does not disagree. Ultimately, however, the failure by Rambus to fully execute this plan was one of the reasons for the failure of the Rambus proprietary RDRAM technology. (CCFF 1862-66, 1877-94).

53. Rambus and its founders believed that they had compelling, revolutionary ideas, that their patents would be significant, and that a small royalty would be palatable given the performance leap of the technology. (Farmwald, Tr. 8112-13).

Response to Finding No. 53: Complaint Counsel does not disagree that Rambus and its founders believed that they had compelling, revolutionary ideas, that their patents would be significant. However, from the start the objective of Rambus was not merely to secure patent rights over widely adopted DRAM industry standards, but to "Make A Lot of Money At The Same Time." (CX1282 at 5). Its early business planning recognized that "RamBus must be established as a standard to effect large royalty payments." (CX0533 at 19). In other words, they believed that large royalty payments would be palatable if Rambus could establish itself as the industry standard. (*See* CCFF 706-09, 732-35).

54. Rambus hoped that success would come through the strength of the technology and the patents. (Farmwald, Tr. 8121-22). As the 1989 draft business plan stated, "Rambus technology provides several strong barriers to entry for potential competitors, the strongest of which are its

patents and the overwhelming 'unfair' advantage its technology enjoys." (RX 15 at 9). In other words, after thoroughly considering the technology, Drs. Farmwald and Horowitz concluded that some of their inventions were "absolutely necessary" to create fast DRAMs. (Farmwald, Tr. 8123).

Response to Finding No. 54: Complaint Counsel does not disagree that Rambus hoped that success would come through the strength of the proprietary RDRAM technology. Throughout its entire time at JEDEC and continuing thereafter, Rambus continued to persuade the market to adopt and license its RDRAM technology. (CCFF 746-56, 1238-53). However, beginning in 1992, Rambus developed a second plan to monopolize the market for technologies used in synchronous DRAMs, one that did not depend on the market adopting RDRAMs. This second plan was to obtain and later enforce patents covering technologies used in SDRAMs, including JEDEC-compliant SDRAMs. (CCFF 757-66, 911-18, 937-38).

55. Drs. Farmwald and Horowitz also realized that the keystone of their company would be the strength and depth of their patents. They recognized that even with a low royalty rate of 2 to 3%, manufacturers might try to get out of paying for the technology if they could. (Farmwald, Tr. 8129). Whether their patents would be "enforceable and broad enough to stop imitators" was a risk from the very beginning. (RX 15 at 19).

Response to Finding No. 55: Complaint Counsel agrees that the Rambus founders believed that "[r]oyalties are the lifeblood [of] Rambus" (CX2106 at 220 (Farmwald, Dep.)), and that Rambus placed great importance on promoting and protecting its proprietary technology.After they had fleshed out their ideas, Drs. Farmwald and Horowitz proceeded to seek funding from three prominent and well-respected Silicon Valley venture capital firms – Kleiner Perkins; Merrill, Pickard, Anderson and Eyre; and Mohr Davidow. (Farmwald, Tr. 8098-99). Kleiner Perkins hired a well-known patent attorney, Roger Borovoy, to investigate how strong Rambus's patents could be. (Farmwald, Tr. 8133-34). As Dr. Farmwald's August 28, 1989 notes show, Mr. Borovoy concluded that the Farmwald and Horowitz ideas were very significant and that potentially a lot of patents could derive from them. (CX 1702 at 3; Farmwald, Tr. 8135). Kleiner Perkins also told

Rambus that the key to success was that they "had to find a number of high-volume customers and high-volume producers to produce the part so that it became the part that everybody was using" in order for Rambus to become a *de facto* standard. (Farmwald, Tr. 8140; CX 1750 at 1).

Response to Finding No. 55: Complaint Counsel does not disagree that Drs. Farmwald and Horowitz sought funding from the three venture capital firms identified in the first sentence of this proposed finding. (Farmwald, Tr. 8098-99). Complaint Counsel does not disagree with the balance of the proposed finding.

56. After they had fleshed out their ideas, Drs. Farmwald and Horowitz proceeded to seek funding from three prominent and well-respected Silicon Valley venture capital firms – Kleiner Perkins; Merrill, Pickard, Anderson and Eyre; and Mohr Davidow. (Farmwald, Tr. 8098-99). Kleiner Perkins hired a well-known patent attorney, Roger Borovoy, to investigate how strong Rambus's patents could be. (Farmwald, Tr. 8133-34). As Dr. Farmwald's August 28, 1989 notes show, Mr. Borovoy concluded that the Farmwald and Horowitz ideas were very significant and that potentially a lot of patents could derive from them. (CX 1702 at 3; Farmwald, Tr. 8135). Kleiner Perkins also told Rambus that the key to success was that they "had to find a number of high-volume customers and high-volume producers to produce the part so that it became the part that everybody was using" in order for Rambus to become a *de facto* standard. (Farmwald, Tr. 8140; CX 1750 at 1).

Response to Finding No. 56: Complaint Counsel does not disagree that Drs. Farmwald and Horowitz sought funding from the three venture capital firms identified in the first sentence of this proposed finding (Farmwald, Tr. 8098-99), but the cited reference does not contain any reference supporting their prominence. Complaint Counsel does not disagree with the balance of the proposed finding.

57. To this end, the Rambus inventions were designed to be produced using existing DRAM manufacturing technology. (Farmwald, Tr. 8142-43; RX 82 at 6).

Response to Finding No. 57: Complaint Counsel does not disagree. For a more complete discussion of the DRAM manufacturing process *see* CCFF 35-45.

58. Even early on, Rambus believed that to succeed, it needed Intel to buy into the Rambus technology. (Farmwald, Tr. 8153). Bill Davidow of Mohr Davidow arranged for Drs. Farmwald and Horowitz to present their ideas to Gordon Moore, the founder of Intel, who was very excited by their ideas and wanted Intel to work with Rambus. (Farmwald, Tr. 8154-55). All three venture

capital firms saw the value of the Rambus inventions and chose to invest funds in the company. (Farmwald, Tr. 8155-56).

Response to Finding No. 58: Complaint Counsel does not disagree that Dr. Farmwald testified as set forth in this proposed finding, or that the finding sets forth Dr. Farmwald's impressions of the views of Mr. Moore and the venture capital firms.

1. Drs. Farmwald And Horowitz Developed Numerous Inventions In Solving The Memory Bottleneck Problem.

59. In working toward their goal, Drs. Farmwald and Horowitz had to solve numerous problems. (Horowitz, Tr. 8487). They realized that current memory interfaces could not run at high speeds as a result of electrical issues, clocking issues, and issues relating to the protocol, and that they would need innovations in each of these areas in order to meet their goal. (Horowitz, Tr. 8487-88).

Response to Finding No. 59: This proposed finding, while accurate, is misleading because it suggests that Drs. Farmwald and Horowitz were the only ones developing technology to overcome the "memory bottleneck" issue. (*See* CCFF 500 - 658 regarding the development of the JEDEC SDRAM and DDR SDRAM standards). Furthermore, this entire series of RPFs (Nos. 59-71) is misleading because it ignores other evidence suggesting that the "basic notion" of the Rambus technology was the use of a narrow, high speed multiplexed bus to carry control, address and data information. (*See* CCFF 717 - 724).

a. Inventions Related to Electrical Issues.

60. With respect to electrical issues, Drs. Farmwald and Horowitz needed to develop driver and receiver circuitry that could generate very high-speed signals, and they also needed to develop a bus that would allow the signals to propagate. (Farmwald, Tr. 8118-20; Horowitz, Tr. 8488).

Response to Finding No. 60: Complaint Counsel has no specific response, except to state that this entire series of RPFs (Nos. 59-71) is misleading because it ignores other evidence suggesting that the "basic notion" of the Rambus technology was the use of a narrow, high speed multiplexed bus to carry control, address and data information. *See* CCFF 717 - 724.

61. Drs. Farmwald and Horowitz developed a number of solutions to the electrical issues that arose. First, they realized that reflected signals from the end of the bus lines would be a serious problem at high speeds and conceived the idea of introducing resistors to "terminate" the bus lines and reduce reflections. (Horowitz, Tr. 8492-93).

Response to Finding No. 61: The reference in the first sentence of this proposed finding to "a number of solutions" is not supported by record evidence. Furthermore, this entire series of RPFs (Nos. 59-71) is misleading because it ignores other evidence suggesting that the "basic notion" of the Rambus technology was the use of a narrow, high speed multiplexed bus to carry control, address and data information. *See* CCFF 717 - 724.

62. Second, Drs. Farmwald and Horowitz realized that the high voltage signaling then in use would generate too much power at high speeds, and they developed low voltage signaling using a particular kind of driver called a "current mode" driver. (Farmwald, Tr. 8119, 8144-45; Horowitz, Tr. 8494-95; RX 82 at 9).

Response to Finding No. 62: This entire series of RPFs (Nos. 59-71) is misleading because it ignores other evidence suggesting that the "basic notion" of the Rambus technology was the use of a narrow, high speed multiplexed bus to carry control, address and data information. *See* CCFF 717 - 724.

63. Third, Drs. Farmwald and Horowitz realized that they could not build a 500 MHz DRAM with current technology and so, to transmit data at the highest possible speed, they conceived the idea of transmitting and receiving data on both edges of a 250 MHz clock. (Farmwald, Tr. 8118; Horowitz, Tr. 8495-97).

Response to Finding No. 63: This entire series of RPFs (Nos. 59-71) is misleading because it ignores other evidence suggesting that the "basic notion" of the Rambus technology was the use of a narrow, high speed multiplexed bus to carry control, address and data information. *See* CCFF 717 - 724.

b. Inventions Related to Clocking Issues.

64. With respect to clocking issues, Drs. Farmwald and Horowitz realized that, although current memory chips were asynchronous, they would have to develop a synchronous device with mechanisms for exercising very tight control over timing with respect to the clock to make sure

that each bit of data – traveling at a very high speed – was sampled at the right time. (Horowitz, Tr. 8488-89).

Response to Finding No. 64: This proposed finding, while accurate, is misleading because it suggests that Drs. Farmwald and Horowitz were the only ones developing synchronous memory devices. *See* CCFF 513 - 564 relating to the development of the JEDEC first generation SDRAM. Also, the record should be clear that the testimony of Dr. Horowitz was limited to his personal experience with respect to developing and designing the Rambus technology (Horowitz, Tr. 8512-13, 8558-59) and should therefore not be viewed as more general observations about alternatives that may or may not have been available to JEDEC at a different point in time. *See* CCFF 2228 - 2233 for evidence relating to asynchronous alternatives to the synchronous DRAMs being considered at JEDEC in the early to mid 1990s.

This entire series of RPFs (Nos. 59-71) is misleading because it ignores other evidence suggesting that the "basic notion" of the Rambus technology was the use of a narrow, high speed multiplexed bus to carry control, address and data information. *See* CCFF 717 - 724.

65. Drs. Farmwald and Horowitz decided to design a synchronous system since the timing reference provided by a clock could be used to limit timing uncertainties in the system and allow for high speed performance. (Horowitz, Tr. 8499-8502).

Response to Finding No. 65: *See* Response to RPF 64. This entire series of RPFs (Nos. 59-71) is misleading because it ignores other evidence suggesting that the "basic notion" of the Rambus technology was the use of a narrow, high speed multiplexed bus to carry control, address and data information. *See* CCFF 717 - 724.

66. Even in a synchronous system, however, there remain some timing uncertainties; for example, expected delays of the buffers may vary from DRAM to DRAM due to differences in their fabrication. (Horowitz, Tr. 8503-04). In order to have the highest speed possible, Drs. Farmwald and Horowitz wanted to minimize this remaining uncertainty to the extent possible; they therefore came up with the idea of using a delay locked loop (DLL) or a phase locked loop (PLL) on-chip. (Farmwald, Tr. 8118; Horowitz, Tr. 8504). Dr. Horowitz believed that a DLL or PLL circuit on the DRAM was necessary for 500 megahertz operation. (Horowitz, Tr. 8506).

Response to Finding No. 66: This proposed finding is misleading and inaccurate when it suggests Drs. Farmwald and Horowitz where the first who "came up with" the idea of using a delay locked loop. As Dr. Horowitz testified on cross, the generic concept of a delay locked loop had been around long before Rambus. (Horowitz, Tr. 8607-08). Furthermore, with respect to the 500 megahertz figure, as Dr. Horowitz testified on direct examination, "It wasn't through a lot of detailed technical analysis that we came up with that [figure]." (Horowitz, Tr. 8505-06).

This entire series of RPFs (Nos. 59-71) is misleading because it ignores other evidence suggesting that the "basic notion" of the Rambus technology was the use of a narrow, high speed multiplexed bus to carry control, address and data information. *See* CCFF 717 - 724.

c. Inventions Related to the Memory Interface Protocol.

67. With respect to the design of the protocol, additional optimizations developed for high speed operation included returning a variable amount of data in response to a request rather than a single bit of data and by putting registers and associated control circuitry directly on the DRAM. (Farmwald, Tr. 8115; Horowitz, Tr. 8489-90).

Response to Finding No. 67: This entire series of RPFs (Nos. 59-71) is misleading because it ignores other evidence suggesting that the "basic notion" of the Rambus technology was the use of a narrow, high speed multiplexed bus to carry control, address and data information. *See* CCFF 717 - 724.

68. With respect to the protocol, Drs. Farmwald and Horowitz again came up with various innovations. As one example, they decided to put registers on the DRAM to make the interface more efficient. (Farmwald, Tr. 8115-16; Horowitz, Tr. 8506). These registers would be programmed with parameters such as the address range that a particular DRAM would respond to, or the access time of the DRAM. (Horowitz, Tr. 8507, 8509-10).

Response to Finding No. 68: The reference in the first sentence of this proposed finding to "various innovations" with respect to the protocol is not supported by record evidence. This entire series of RPFs (Nos. 59-71) is misleading because it ignores other evidence suggesting

that the "basic notion" of the Rambus technology was the use of a narrow, high speed multiplexed bus to carry control, address and data information. *See* CCFF 717 - 724.

69. Drs. Farmwald and Horowitz wanted to make the access time variable for two reasons. First, if the bus were improved so that it could operate at a faster clock frequency, the access time of the DRAM could be adjusted so that it would operate with that faster clock. Second, a variable access time would allow the access times of all the DRAMs in a system to be adjusted to have the same access time. (Horowitz, Tr. 8510-11). As noted above, they conceived the idea of using a register on the DRAM to store the variable access time value. *See* Findings, ¶ 68. "Access time" and "latency" are synonymous, so variable access time includes programmable latency. (Horowitz, Tr. 8511).

Response to Finding No. 69: This proposed finding is misleading because it suggests that Drs. Farmwald and Horowitz were the only ones to develop the concept of using registers on a DRAM to store variable access time. As noted in Complaint Counsel's proposed findings, the concept of programmable CAS latency was discussed at JEDEC before Rambus became a member. *See* CCFF 513 - 514. In particular, the programmable methodology represented an "evolutionary" concept was similar to concepts that had been used by the industry in prior years. *See* CCFF 534. Furthermore, Dr. Horowitz's view that "access time" and "latency" were synonymous is inconsistent with other evidence suggesting that the concept of "access time" as described in the original '898 patent application is not the same as the concept of programmable CAS latency as used in a JEDEC-compliant SDRAM. *See* CCFF 1319 - 1326.

This entire series of RPFs (Nos. 59-71) is misleading because it ignores other evidence suggesting that the "basic notion" of the Rambus technology was the use of a narrow, high speed multiplexed bus to carry control, address and data information. *See* CCFF 717 - 724.

70. As another example of an innovation related to the protocol, Drs. Farmwald and Horowitz allowed the response to a request to include a variable amount of data, a feature known as "variable block size" or "variable burst length." (Farmwald, Tr. 8116-17, 8146; Horowitz, Tr. 8512; RX 82 at 9).

Response to Finding No. 70: This proposed finding is misleading because it suggests that Drs. Farmwald and Horowitz were the first to develop the concept of variable block

size or variable burst and that this was a unique "innovation" developed by Rambus. As noted in Complaint Counsel's proposed findings, the concept of programmable burst length (also known as "wrap length") was discussed at JEDEC in connection with the first generation SDRAM standard. *See* CCFF 527 - 539. In particular, the programmable burst length methodology represented an "evolutionary" concept was similar to concepts that had been used by the industry in prior years. *See* CCFF 534. Furthermore, the cited testimony is inconsistent with other evidence suggesting that the concept of "block size" as described in the original '898 patent application is not the same as the concept of programmable burst length as used in a JEDEC-compliant SDRAM. *See* CCFF 1309 - 1318.

This entire series of RPFs (Nos. 59-71) is misleading because it ignores other evidence suggesting that the "basic notion" of the Rambus technology was the use of a narrow, high speed multiplexed bus to carry control, address and data information. *See* CCFF 717 - 724.

71. In addition to the various innovations described above, Drs. Farmwald and Horowitz had to solve many other problems with other innovative solutions. (Horowitz, Tr. 8513).

Response to Finding No. 71: The citation, while accurate, is of little or no probative value because of the lack of additional evidence in the record identifying or describing these so-called "other innovative solutions." Furthermore, this series of RPFs (Nos. 59-71) is misleading because it ignores other evidence suggesting that the "basic notion" of the Rambus technology was the use of a narrow, high speed multiplexed bus to carry control, address and data information. (*See* CCFF 717 - 724).

2. The '898 Application.

72. By early 1990, Drs. Farmwald and Horowitz had put together a set of their ideas that they proceeded to describe in a patent application. (Horowitz, Tr. 8514). This patent application, serial number 07/510,898 (the "'898 application"), named Drs. Farmwald and Horowitz as inventors and was filed on April 18, 1990. (CX 1451 at 2).

Response to Finding No. 72: This proposed finding is misleading to the extent that, in combination with RPF 59-71, it suggests the "ideas" as described by Drs. Farmwald and Horowitz in the '898 application related to programmable CAS latency, programmable burst length, on-chip delay locked loop or dual-edged clocking as used independently of the Rambus proprietary narrow, multiplexed, packetized bus, or as proposed for use, or used, in JEDEC-compliant SDRAM and DDR SDRAM. The '898 application described a narrow, multiplexed bus architecture with various features, of the kind embodied in the proprietary Rambus RDRAM technology. (CCFF 1284-1340).

73. After the filing of the '898 application, Rambus received an 11-way restriction requirement from the PTO – that is, the Patent Examiner determined that Rambus was claiming 11 distinct categories of inventions in the '898 application. (Nusbaum, Tr. 1510).

Response to Finding No. 73: Complaint Counsel does not disagree. (CCFF 729).

74. After receiving the restriction requirement, Rambus elected one group of claims to prosecute in its original application and filed 10 divisional applications to pursue the other groups of claims identified in the restriction requirement. (Nusbaum, Tr. 1511).

Response to Finding No. 74: Complaint Counsel does not disagree. (CCFF 729).

3. The Patent Application Process

75. The main parts of a patent application are the written description, the drawings, and the claims. (Nusbaum, Tr. 1496-97). Together, these are sometimes called the patent "specification."

Response to Finding No. 75: The second sentence of the proposed finding is incomplete and contrary to the cited testimony. The term "specification" is also used to refer to the description portion of a patent and the drawings, excluding the claims. (Nusbaum, Tr. 1496-97, CCFF 1277).

76. The function of a claim in a patent application is to define the boundaries of the applicant's right to exclude others from making, using, or selling the claimed invention in the event that the claim is allowed by the United States Patent and Trademark Office ("PTO"). (Nusbaum, Tr. 1497).

Response to Finding No. 76: Complaint Counsel does not disagree. (CCFF 1277).

77. When a patent application is filed, the patent examiner reads the disclosure in the application, including the claims, to make sure that the disclosure requirements of the patent laws are satisfied and to gain an understanding of the claimed invention. (Nusbaum, Tr. 1498).

Response to Finding No. 77: Complaint Counsel does not disagree that an examiner performs these and other things in examining an application.

78. As discussed further below, one of these disclosure requirements, the "written description requirement" of patent law, provides that the specification must "support" the claims; that is, the specification must clearly disclose to one of ordinary skill in the art that the applicant is in possession of the inventions being claimed. *See* Findings, ¶¶ 86-87. The applicant need not claim every invention disclosed in the specification when the application is first filed. Rather, claims can be added through amendments and follow-on applications known as "continuations" and "divisionals," discussed below, so long as those later-added claims are supported by the specification as originally filed. *See* Findings ¶¶ 83-85.

Response to Finding No. 78: Complaint Counsel does not disagree. *See* CCRF 86-87, 83-85.

79. The patent examiner then does a search of prior art to determine whether there is prior art that may invalidate the proposed claims of the application. (Nusbaum, Tr. 1498).

Response to Finding No. 79: Complaint Counsel does not disagree that an examiner performs these and other things in examining an application.

80. The patent examiner next compiles the various objections to or rejections of the claims in the application, if any, and sends them to the applicant in what is called an "office action." (Nusbaum, Tr. 1498).

Response to Finding No. 80: Complaint Counsel does not disagree that an examiner performs these and other things in examining an application.

81. The patent applicant must respond to each and every objection and rejection raised by the patent examiner in an office action. The applicant may either argue that the examiner was incorrect for legal or technical reasons, or the applicant may choose to amend the claims. (Nusbaum, Tr. 1498-9).

Response to Finding No. 81: Complaint Counsel does not disagree.

82. After the examiner receives the response, he may be convinced by the arguments or amendments and choose to allow the claims. If the examiner rejects the claims again, however, that is typically a final rejection of the claims. (Nusbaum, Tr. 1499).

Response to Finding No. 82: This proposed finding is misleading insofar as it fails to state that an applicant may, and frequently does, continue to pursue identical or substantially similar claims by filing a continuation application. (*See* RPF 83).

a. Continuation and Divisional Applications.

83. Patent applicants may file so-called "continuation" applications not only to continue the prosecution of a patent application that has received a final rejection, but also in order to obtain claims that are supported by the written description but different in scope from those in the prior application. (Nusbaum, Tr. 1513).

Response to Finding No. 83: Complaint Counsel does not disagree.

84. A continuation application names one or more of the inventors of an identified prior application and adds no "new matter" (*i.e.*, no subject matter not in the parent application) to the disclosure of the parent application. (Nusbaum, Tr. 1508-9).

Response to Finding No. 84: Complaint Counsel does not disagree.

85. A divisional application is much like a continuation application, and likewise adds no new matter to the disclosure, but typically arises when a patent examiner determines that the original or "parent" application is claiming multiple distinct inventions. (Nusbaum, Tr. 1509-10). In such a circumstance, the examiner will impose a so-called "restriction requirement," requiring that the applicant elect one group of claims, corresponding to one of the distinct inventions, to prosecute in the original application. (Nusbaum, Tr. 1510). The applicant may choose to file divisional applications directed to the groups of claims that were not elected. (*Id.*).

Response to Finding No. 85: Complaint Counsel does not disagree.

b. Adequacy of a Patent Application's Disclosure

86. With respect to adequacy of disclosure of a patent application, patent examiners consider three requirements that the specification must satisfy: the "written description" requirement, the "enablement" requirement, and the "best mode" requirement.

Response to Finding No. 86: Complaint Counsel does not disagree. (Nusbaum, Tr. 1501).

87. The "written description" requirement provides, with respect to later added claims, that the originally filed application has to clearly disclose to one of ordinary skill in the art to which the

patent pertains that the applicant was in possession of the later claimed invention as of the original filing date. (Nusbaum, Tr. 1502, 1613-14; Fliesler, Tr. 8806-09).

Response to Finding No. 87: Complaint Counsel does not disagree.

88. The "enablement" requirement provides that the patent application must be set forth in such full, clear, concise and exact language that a person of ordinary skill in the art is enabled to make and use the claimed invention without having to resort to undue experimentation. (Nusbaum, Tr. 1501-02).

Response to Finding No. 88: Complaint Counsel does not disagree.

89. The "best mode" requirement provides that an applicant must disclose the best way that he has contemplated of implementing a claimed invention. (Nusbaum, Tr. 1502).

Response to Finding No. 89: Complaint Counsel does not disagree.

c. Definiteness of Claims.

90. Patent examiners also consider the "definiteness" of the claims in an application. A claim in an application must particularly point out and distinctly claim the invention, that is, the words of the claim must circumscribe a particular subject matter with a reasonable degree of precision and particularity such that the bounds of the invention being claimed are reasonably precise. If the examiner determines that a claim does not satisfy this requirement, the claim will be rejected as indefinite. (Nusbaum, Tr. 1502-03).

Response to Finding No. 90: The proposed finding is misleading because it is incomplete. The patent statute requires claims to be "definite," to particularly point out and distinctly claim the invention. (Nusbaum, Tr. 1502). However, an examiner's rejection of an application claim based on indefiniteness does not mean that a particular patent application claim violates this statutory requirement. It is very common for examiners to reject claims based on indefiniteness in order to have applicants amend claim language to be more precise and in conformity with the examiner's own preferences, even when that language complies with the statutory requirement. (Nusbaum, Tr. 1502-04).

d. The Need to Maintain the Confidentiality of Information Regarding Patent Applications.

91. Prior to 1999, patent applications were kept strictly confidential by the PTO until patent issuance. (Fliesler, Tr. 8830).

Response to Finding No. 91: Complaint Counsel does not disagree.

92. Patent applications are generally kept confidential by applicants for as long as possible. (Fliesler, Tr. 8829-30). Applicants have no enforceable rights until a patent issues and generally do not want to have their technology disclosed to competitors until such time as they do have enforceable patent rights. (*Id.*). In the 1990 to 1996 time frame, if a patent ultimately did not issue from an application, the application would remain secret and the applicant could retain trade secret protection over the material in the application. (Fliesler, Tr. 8836-37).

Response to Finding No. 92: The proposed finding does not support the conclusion that Rambus maintained trade secret protection over the '898 application and its progeny. On April 16, 1991, Rambus filed an international patent application pursuant to the Patent Cooperation Treaty (the "PCT application"). (CX1454 at 1). The PCT application is identical in all material respects to the '898 application. In particular, the PCT application contains the same written description, drawings, and 150 claims as the '898 application. (CX1451; CX1454; Fliesler, Tr. 8811). The PCT application was published and made publicly available as of October 31, 1991. (CCFF 1267; CX1454 at 1; The Parties First Set of Stipulations, Stipulation 8). As of October 31, 1991, Rambus had no trade secret protection over the written description, drawings, and original 150 claims of the '898 application. (Fliesler, Tr. 8894).

Rambus's first U.S. Patent, No. 5,243,703 (the '703 patent), issued on September 7, 1993 (RX 425). The '703 patent issued from a divisional application of the original '898 application. (RX 425 at 1; Fliesler, Tr. 8812). The written description and drawings of the '703 patent are substantially the same as the written description and drawings in the '898 application. (RX 425; CX1451; Fliesler, Tr. 8812, 8817). In addition to listing the original '898 application, the '703 patent's written description also contains a list of the nine other divisional applications stemming from the '898 application. (RX 425 at 11; Fliesler, Tr. 8813-14). As of September 7, 1993, Rambus had no trade secret protection over the fact that it had pursued 10 divisional applications of the '898 application. (Fliesler, Tr. 8813-14; 8894).

93. Companies often are wary of disclosing patent applications because to do so would be to disclose to competitors the areas of technology that the company is developing and the areas of technology for which the company is seeking patent protection. (Fliesler, Tr. 8840).

Response to Finding No. 93: The proposed finding does not support the conclusion that a concern over the confidentiality of patent applications excuses a JEDEC member's failure to disclose a patent application to the organization. Mr. Fliesler offered no opinion on whether any concern for the confidentiality of patent applications affected the scope of the JEDEC disclosure policy. (Fliesler, Tr. 8893). He did not testify that any confidentiality concerns would prevent a standard setting organization from requiring its members to disclose patent applications. (Fliesler, Tr. 8893).

The proposed finding does not support the conclusion that Rambus failed to disclose patents and patent applications to JEDEC for the reason stated. To the extent the proposed finding suggests otherwise, it is unreliable. Mr. Fliesler does not know whether this concern was played any role in Rambus's decision not to disclose patents and patent applications to JEDEC. (Fliesler, Tr. 8892-93). The contemporaneous documents indicate that the reason Rambus did not disclose its patent applications to JEDEC was because Rambus did not want to provide JEDEC the opportunity to design around its patents – in other words, its leverage was better to wait. (CX0711 at 68, 73 (Crisp e-mail, 5/24/95: "[I]t makes no sense to alert them to a potential [patent] problem they can easily work around."); CX0919 (Tate e-mail, 2/10/97: "do NOT tell customers/partners that we feel DDR may infringe – our leverage is better to wait"); CX0942 (Tate e-mail, 8/4/97: "our policy so far has been NOT to publicize our patents and i think we should continue with this"); CX0960 (Tate e-mail, 10/1/97: "when joel [karp] starts we need to have our spin control ready for partners/etc as to why we are hiring him and what he will be doing."); CX0987 at 4 (Tate e-mail, 1/19/98: "ddr infringes our patents (question: when do we start saying this publicly?)");

CX1089 (Tate e-mail, 12/9/99: "it's important NOT to indicate/hint/wink/etc what we expect the results of our infringement analysis to be!!!")).

94. Even when a patent has issued from an original application – which results in disclosure of the drawings and written description – the applicant would still have reasons to keep confidential other applications claiming priority back to that original application. (Fliesler, Tr. 8837-38). It would be very valuable to a competitor to know what claims the applicant is actually pursuing in those other applications from the entirety of inventions that could be claimed based on the written description. (Fliesler, Tr. 8838, 8900-02).

Response to Finding No. 94: The proposed finding says nothing about whether a standard setting organization can require members to disclose patent applications. The proposed finding does not support the conclusion that a concern over the confidentiality of patent application claims excuses a JEDEC member's failure to disclose a patent application to the organization. (*See* CCRF 93.) The proposed finding does not support the conclusion that Rambus failed to disclose patents and patent applications to JEDEC for the reason stated. To the extent the proposed finding suggests otherwise, it is unreliable. (*See* CCRF 93). The contemporaneous documents indicate that the reason Rambus did not disclose its patent applications to JEDEC was because Rambus did not want to provide JEDEC the opportunity to design around its patents – in other words, its leverage was better to wait. (CX0711 at 68, 69; CX0919 at 1).

95. Similarly, even if a corresponding international patent application is published, there remain business reasons for not disclosing a United States patent application, because information about the particular claims being pursued constitutes strategic business and technical information that a company would want to keep from its competitors. (Fliesler, Tr. 8840-41, 8894-96).

Response to Finding No. 95: The proposed finding does not support the conclusion that a concern over the confidentiality of patent application claims excuses a JEDEC member's failure to disclose a patent application to the organization. (*See* CCRF 93.) The proposed finding does not support the conclusion that Rambus failed to disclose patents and patent applications to JEDEC for the reason stated. To the extent the proposed finding suggests otherwise, it is unreliable. (*See* CCRF 93). The contemporaneous documents indicate that the

reason Rambus did not disclose its patent applications to JEDEC was because Rambus did not want to provide JEDEC the opportunity to design around its patents – in other words, its leverage was better to wait. (CX0711 at 68, 69; CX0919 at 1).

96. In addition, if information about pending applications were disclosed by a company to a competitor, the competitor could potentially slow down or interfere with the prosecution of the application. (Fliesler, Tr. 8841). The competitor could disclose prior art to the company, for example. Even if it is not relevant prior art, it could cause a dilemma for the company about whether the information triggered a duty to disclose prior art to the PTO, potentially confusing or delaying the patent prosecution. (Fliesler, Tr. 8841-42).

Response to Finding No. 96: Patent applicants have a duty to disclose material prior art of which they are aware to the Patent Office. (Fliesler, Tr. 8841). The proposed finding does not support the conclusion that a desire to remain unaware of material prior art, or to keep the Patent Office unaware of that prior art, excuses a JEDEC member's failure to disclose a patent application to the organization. (*See* CCRF 93.) The proposed finding does not support the conclusion that Rambus failed to disclose patents and patent applications to JEDEC because it wished to remain unaware of material prior art. To the extent the proposed finding suggests otherwise, it is unreliable. (*See* CCRF 93). The contemporaneous documents indicate that the reason Rambus did not disclose its patent applications to JEDEC was because Rambus did not want to provide JEDEC the opportunity to design around its patents – in other words, its leverage was better to wait. (CX0711 at 68, 69; CX0919 at 1).

97. The competitor could also try to provoke an "interference" at the patent office – that is, a proceeding to determine which of two applicants claiming the same invention was actually the first to invent and entitled to a patent – by claiming the same invention in one of the competitor's applications. (Fliesler, Tr. 8834-35, 8842).

Response to Finding No. 97: When two patent applicants submit claims to the Patent Office covering the same invention, the applicant who was the first to invent the claimed invention is entitled to the patent under United States law. (Fliesler, Tr. 8834-35.) In that situation, the Patent Office may declare an "interference" proceeding by which the two applicants

present evidence and arguments as to who was the first to invent the claimed invention and is, therefore, entitled to the patent. (Fliesler, Tr. 8835). The proposed finding does not support the conclusion that a desire to avoid a determination of the true inventor of claimed subject matter excuses a JEDEC member's failure to disclose a patent application to the organization. (*See* CCRF 93.) The proposed finding does not support the conclusion that Rambus failed to disclose patents and patent applications to JEDEC in order to avoid an interference. To the extent the proposed finding suggests otherwise, it is unreliable. (*See* CCRF 93). The contemporaneous documents indicate that the reason Rambus did not disclose its patent applications to JEDEC was because Rambus did not want to provide JEDEC the opportunity to design around its patents – in other words, its leverage was better to wait. (CX0711 at 68, 69; CX0919 at 1).

98. Also, disclosing information about pending applications could jeopardize an applicant's ability to get foreign patents.

Response to Finding No. 98: The proposed finding cites to no supporting record evidence and is unsupported by record evidence. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Moreover, the proposed finding does not support the conclusion that any disclosure by Rambus after the April 18, 1990 filing date of the '898 application would have jeopardized Rambus's ability to get foreign patents corresponding to the '898 application. The proposed finding does not support the conclusion that a concern about foreign patent rights motivated Rambus's decision to not disclose patents and patent applications to JEDEC. (*See* CCRF 99-100).

Rambus had no legitimate concern that disclosures to JEDEC concerning the '898 patent application after April 18, 1990 would jeopardize it foreign patent rights based on the '898 application by acting as prior art. Rambus's PCT application and its other foreign patents based on

the ‘898, have a “priority date,” meaning a legally effective filing date, of April 18, 1990, the filing date of the U.S. ‘898 application. (Fliesler, Tr. 8839-40; 8883-8884, 8888; CCFF 1118-20, 1669-74, 2024). A public statement made after April 18, 1990, could not have had any effect as prior art to these foreign applications. (Fliesler, Tr. 8889-90).

99. In the United States, patents are generally awarded to the applicant who was the first to invent a given invention. (Fliesler, Tr. 8834-35). Most foreign jurisdictions, however, have a first to file rule: The first applicant to file an application that is otherwise entitled to a patent will be awarded the patent. (Fliesler, Tr. 8838-39).

Response to Finding No. 99: The proposed finding is incomplete. Through treaties to which the United States is a party, a patent applicant has up to one year following the filing date of his U.S. patent application to file a corresponding application in foreign countries. If he does so, the foreign country accords the application a priority date, meaning a legally effective filing date in that foreign country, of the U.S. application. (Fliesler, Tr. 8839-40). Which applicant is the first to file an application in a foreign country will be judged according to the priority date. *Id.*

100. If a competitor learned of an application before the applicant had filed all of its foreign applications, the competitor could claim to be an independent inventor and race to the foreign patent office ahead of the original applicant.

Response to Finding No. 100: The proposed finding cites to no supporting record evidence. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court’s July 10, 2003 Order on Post Trial Briefs. Moreover, the proposed finding does not support the conclusion that any disclosure by Rambus after the April 18, 1990 filing date of the ‘898 application would have jeopardized Rambus’s ability to get foreign patents corresponding to the ‘898 application.

Rambus had no legitimate concern that disclosures to JEDEC concerning the ‘898 patent application after April 18, 1990, and October 31, 1991, would jeopardize it foreign patent rights

based on the ‘898 application because another inventor might “race to the foreign patent office” ahead of it. Rambus’s PCT application and foreign patent applications based on the ‘898 application had a “priority date,” meaning a legally effective filing date, of April 18, 1990. (Fliesler, Tr. 8839-40; 8883-8884, 8888; CCFF 1118-20, 1669-74, 2024). Any competitor that “raced” to a foreign patent office to file a patent application after April 18, 1990, could not claim to be the first-to- file a patent application for any invention described in the PCT or other foreign patent applications, simply because the competitor would have the later filing date.

The PCT application was published and publicly available by October 31, 1991. (CCFF 1267; CX1454 at 1; The Parties First Set of Stipulations, Stipulation 8). Competitors who attempted to file foreign patent applications after October 31, 1991 on inventions described in the PCT application would face that publication as prior art. Generally, prior art may be thought of as prior technological developments that are public prior to a patent application’s filing date. (Nusbaum, Tr. 1501). After the publication of the PCT application, a competitor could not claim patent rights on any invention described in it.

To the extent that Rambus relies on the testimony of it patent law expert, Mr. Fliesler, to suggest that any disclosure made after April 18, 1990 concerning the ‘898 application or its continuations and divisionals could jeopardize foreign applications based on the ‘898, that testimony is unreliable. Mr. Fliesler named no foreign country in which this would be a concern. (Fliesler, Tr. 8838-40). In direct conflict with this suggestion, he explained that foreign applications would be accorded the benefit of the U.S. filing date. (Fliesler, Tr. 8839-40). He admitted that he could not name a foreign country in which the foreign application would not receive the benefit of the U.S. filing date, but would seek the advice of foreign counsel. (Fliesler, Tr. 8886-87).

The proposed finding does not support the conclusion that a concern about foreign patent rights motivated Rambus's decision to not disclose patents and patent applications to JEDEC. (*See* CCRF 93). The record evidence shows that Rambus filed patent applications with all key foreign authorities during 1991, including those in Europe, Israel, Japan, Korea, Taiwan & India. (CCFF 1115-21). The evidence does not show that Rambus filed a patent application in any other country at any time from 1992 to 2003. The contemporaneous documents indicate that the reason Rambus did not disclose its patent applications to JEDEC was because Rambus did not want to provide JEDEC the opportunity to design around its patents – in other words, its leverage was better to wait. (CX0711 at 68, 69; CX0919 at 1).

101. Martin Fliesler, a patent attorney with over 30 years of experience prosecuting patent applications, advises his clients that they should not disclose patent applications but should, instead, keep them confidential. (Fliesler, Tr. 8765-72, 8842-43).

Response to Finding No. 101: The proposed finding does not support the conclusion that a concern over the confidentiality of patent application claims excuses a JEDEC member's failure to disclose a patent application to the organization. (*See* CCRF 93.) The proposed finding does not support the conclusion that Rambus failed to disclose patents and patent applications to JEDEC for the reason stated. To the extent the proposed finding suggests otherwise, it is unreliable. (*See* CCRF 93). The contemporaneous documents indicate that the reason Rambus did not disclose its patent applications to JEDEC was because Rambus did not want to provide JEDEC the opportunity to design around its patents – in other words, its leverage was better to wait. (CX0711 at 68, 69; CX0919 at 1).

102. If a client wants to disclose an application in the context of negotiations over an agreement (such as a license agreement or joint venture agreement) with a competitor, Mr. Fliesler advises it to follow a "tiered system" of disclosure: first, the client should disclose only the general area of the application without details, and even that level of disclosure should be done pursuant to a nondisclosure agreement; if the talks proceed, the specification of the application might be disclosed pursuant to a tighter nondisclosure agreement, but the claims would still be held back; finally, if the talks are moving forward well, the client might disclose the claims and all of the

applications in the chain subject to an even tighter nondisclosure agreement. (Fliesler, Tr. 8843-45).

Response to Finding No. 102: The proposed finding does not support the conclusion that a standard setting organization cannot require its members to disclose patent applications or that a concern over the confidentiality of patent application claims excuses a JEDEC member's failure to disclose a patent application to the organization. (*See* CCRF 93.) The proposed finding does not support the conclusion that Rambus failed to disclose patents and patent applications to JEDEC for the reason stated. To the extent the proposed finding suggests otherwise, it is unreliable. (*See* CCRF 93). The contemporaneous documents indicate that the reason Rambus did not disclose its patent applications to JEDEC was because Rambus did not want to provide JEDEC the opportunity to design around its patents – in other words, its leverage was better to wait. (CX0711 at 68, 69; CX0919 at 1).

103. The need to keep patent applications confidential was well recognized in the semiconductor industry. JEDEC members were informed in 1992 of potential negative consequences flowing from premature disclosure of inventions. In October 1992, JC 42 Chairman Jim Townsend circulated an article entitled "Don't Lose Your Patent Rights" to members of the JC 42 committee. (CX 342 at 8). The article advises inventors to "Keep It Under Your Hat" because disclosure of an invention may waive any rights to obtain a patent. The article states that in the United States, a disclosure made one year before filing an application can bar a patent, while in some foreign jurisdictions, any disclosure before filing an application will bar a patent. (CX 342 at 8).

Response to Finding No. 103: The cited reference on its face does not support the proposition asserted. As noted in the proposed finding itself, the article make reference to risk of disclosure of an invention before a patent application is filed. (CX0342 at 8). This risk by definition does not exist after a patent application is filed. Indeed, the patent tracking list to which the article was attached and which was circulated to JEDEC members reflects several "pending" patent applications that had been disclosed to JEDEC by various JEDEC members. (CX0342 at 4).

104. Similarly, Robert Goodman, the CEO of Kentron, testified that Kentron's policy is to treat patent applications as trade secrets and to preserve their confidence. (Goodman, Tr. 6072). Mr. Goodman testified that when his company was asked by members of a JEDEC committee to disclose a pending patent application, Kentron resisted the request. (Goodman, Tr. 6059-60, 6067-68). Mr. Goodman viewed the request as inappropriate, and Kentron never disclosed its actual pending claims. (Goodman, Tr. 6059-60, 6070).

Response to Finding No. 104: This proposed finding profoundly misrepresents the testimony of Mr. Goodman of Kentron. In fact, Kentron made a showing and a later presentation to the JEDEC 42.5 Committee in September and December 2000 concerning a patent pending version of a low profile memory module design. (CX2608 at 1). In connection with the presentation, the Kentron representative was asked to disclose the actual wording of the claims set forth in the pending patent application, which Kentron resisted. (Goodman, Tr. 6059-60, 6067-68). However, Kentron did disclose to JEDEC not only the existence of the pending patent application, but also provided a written explanation of the subject matter of the application. (CX2606; Goodman, Tr. 6067-68). Mr. Goodman wrote and spoke with John Kelly, who was then JEDEC president, expressing Kentron's willingness to abide by the JEDEC disclosure rules and his belief that Kentron had in fact done so. (CX2608 at 2; Goodman, Tr. 6068-69). Mr. Kelly reassured Mr. Goodman that the actions of Kentron had complied with JEDEC rules. (CX2610).

In short, the episode of Kentron and JEDEC demonstrates that Kentron was able to fully protect its perceived interest in the confidentiality of its patent application but still provide JEDEC with not only notice of the existence of the pending application but also a description of the subject matter of the pending claims. It is meaningful information about pending applications that is required to be disclosed by the JEDEC policy – sufficient information to put the committee on notice as to the nature of the relationship between the proposed standard and the intellectual property that might relate to the proposed standard. (CCFF 331-32). Kentron's experience of meaningful disclosure in no way resembles or justifies the Rambus multi-year campaign of

misleading concealment of its pending patent claims. Indeed, Kentron emphatically informed JEDEC that it believed it would be "not only unethical but also illegal" to take information learned from the association's activities and incorporate it in pending patent claims, and pledged not to engage in such conduct. (CX2608 at 2).

105. Richard Crisp was informed in 1992 of the importance of keeping patent applications confidential by Rambus's outside patent counsel, Lester Vincent. (Crisp, Tr. 3495-96). Mr. Crisp testified that he also obtained from Mr. Vincent an understanding of the potential negative consequences of disclosing patent applications:

> "I understood that companies could potentially file interference actions on our patent applications in the patent office; that in certain countries where the rules are first to file, somebody could potentially file a claim before we actually did; and that we basically would be disclosing trade secrets that could work against us in terms of our competitive position in the marketplace."

(Crisp, Tr. 3496).

Response to Finding No. 105: Complaint Counsel does not disagree that Mr. Crisp so testified at trial. However, this proposed finding fails to accurately portray the advice that was given to Rambus by Mr. Vincent with respect to its participation in JEDEC. (*See* CCRF 449, 450, 454).

Moreover, there is no credible evidence that patent application confidentiality was a realistic concern, that this was the reason for the Rambus campaign of concealment, or that concerns about patent confidentiality can be legitimate justification in light of the voluntary decision by Rambus to participate as a member in JEDEC, an organization whose rules mandated disclosure of meaningful information concerning patent applications. (CCRF 93-102, 456).

The contemporaneous documents indicate that the reason Rambus did not disclose its patent applications to JEDEC was because Rambus did not want to provide JEDEC or its members the opportunity to design around its patents – in other words, its leverage was better to wait. (CX0711 at 68, 73 (Crisp e-mail, 5/24/95: "[I]t makes no sense to alert them to a potential [patent]

problem they can easily work around."); CX0919 (Tate e-mail, 2/10/97: "do NOT tell customers/partners that we feel DDR may infringe – our leverage is better to wait"); CX0942 (Tate e-mail, 8/4/97: "our policy so far has been NOT to publicize our patents and i think we should continue with this"); CX0960 (Tate e-mail, 10/1/97: "when joel [karp] starts we need to have our spin control ready for partners/etc as to why we are hiring him and what he will be doing."); CX0987 at 4 (Tate e-mail, 1/19/98: "ddr infringes our patents (question: when do we start saying this publicly?)"); CX1089 (Tate e-mail, 12/9/99: "it's important NOT to indicate/hint/wink/etc what we expect the results of our infringement analysis to be!!!")).

Finally, even if there had been concerns by Rambus about the confidentiality of its patent applications and patents, this in no way can justify its campaign of concealment at JEDEC. For more than four years, Rambus chose to be a member in an organization that was dedicated to open standard-setting (CCFF 300-304) with rules that required the disclosure of meaningful information concerning patents and patent applications that related to the work of JEDEC (CCFF 310-56). Mr. Crisp attended meeting after meeting of the organization, reporting back to his colleagues as JEDEC members continually disclosed and discussed patent-related issues pertaining to the standards work. (CCFF 867-1121). If Rambus truly believed its interests required concealment of its patent claims in violation of JEDEC rules, it had no business continuing for years as a JEDEC member.

106. In his letters transmitting copies of Rambus's patent applications, Mr. Vincent repeatedly reminded Mr. Crisp to "keep in mind that this information is confidential." (CX 1951 at 2; CX 1945 at 2).

Response to Finding No. 106: There is no evidence that remotely suggests that Mr. Vincent intended his boilerplate transmittal letters to be construed as advice to Rambus about refusing to comply with JEDEC rules. (*See* CCRF 449, 450, 454).

107. Mr. Crisp followed Mr. Vincent's advice and did not disclose Rambus's patent applications to third parties. (Crisp, Tr. 3496-97).

Response to Finding No. 107: This proposed finding is misleading insofar as it purports to set forth accurately the advice that Mr. Vincent gave Rambus concerning participation in JEDEC. (*See* CCRF 449, 450, 454). The fact is that Rambus chose *not* to follow the advice of Mr. Vincent, who told Rambus that *it was not a good idea* to participate in JEDEC. (CX3125 at 320-21 (Vincent, Dep.); CCRF 449). Mr. Vincent's further advice was that if Rambus insisted on participating in JEDEC, the least it should do is don't do anything to mislead anybody. (CX2092 at 98 (Crisp, Infineon Trial Tr.)). Rambus disregarded this advice by participating in JEDEC for years, all the while simultaneously pursuing patent applications covering JEDEC work while withholding from JEDEC any meaningful information concerning Rambus intellectual property rights. (CCFF 867-1121).

IV. THE EIA/JEDEC PATENT POLICY.

A. Introduction.

108. During much of the 1990's, JEDEC was an unincorporated standards-setting activity within the engineering department of a trade association known as the Electronic Industries Association ("EIA"). (Rhoden, Tr. 289).

Response to Finding No. 108: Complaint Counsel does not disagree. For a more complete discussion of the legal status of JEDEC, *see* CCFF 200-204.

109. Rambus joined JEDEC at the beginning of 1992, and it attended its last JEDEC meeting in December 1995. (CX 601 at 1; Crisp 8/10/01 Micron Depo. Tr., 853:18-854:1). Rambus did not pay its 1996 membership dues and formally notified JEDEC in June 1996 that it had withdrawn from the organization. (CX 887 at 1).

Response to Finding No. 109: This proposed finding is inaccurate. Rambus attended its first JEDEC meeting in December 1991 (*see* JX0010 at 2 (listing Billy Garrett of Rambus in attendance), signed up to join JEDEC five days later, and was formally added to the JEDEC member roll in December 1991 (CCRF 5). Rambus's membership in JEDEC continued

until Rambus formally withdrew from JEDEC in June 1996. (*see* JX0033 at 2-3 (Rambus listed as member)). CCFF 217-18. Finally, the cited testimony from Mr. Crisp's Micron deposition is has not been admitted into evidence and, therefore, should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

110. The Complaint asserts that Rambus was obligated by certain policies in effect while Rambus was a JEDEC member to disclose that it had filed or intended to file or amend patent applications relating to certain features of the SDRAM or DDR SDRAM devices standardized by JEDEC. (Complaint, ¶¶ 55-56).

Response to Finding No. 110: Complaint Counsel does not disagree. However, the JEDEC patent policy is not the only policy that Rambus violated. The Complaint also alleges that Rambus violated its duty to participate in JEDEC in good faith. (Complaint ¶¶ 1-2). Indeed, Mr. Crisp understood that JEDEC required that its programs be conducted in good faith. *See* CCFF 835-36. The complaint also alleges that Rambus violated the "basic rule that standardization programs conducted by the organization 'shall not be proposed for or indirectly result in … restricting competition, giving a competitive advantage to any manufacturer, [or] excluding competitors from the market'" (Complaint, ¶ 19). For a more complete discussion of the basic rules of EIA standardization programs, *see* CCFF 300-422.

111. Rambus asserted in its Answer that the applicable policies did not impose the disclosure obligations set out in the Complaint. (Answer at 1-2).

Response to Finding No. 111: Complaint Counsel has no specific response to this proposed finding.

B. The Governing (And Other) Manuals And Policies.

112. The patent disclosure policy or policies that governed JEDEC's standardization activities while Rambus was a JEDEC member were contained in various EIA manuals, including: (1) the EIA "Legal Guides," published in March 1983 (CX 204); (2) the *Manual for Committee, Subcommittee, and Working Group Chairmen and Secretaries*, Engineering Publication EP-3-F ("EP-3-F"), published in October 1981 (RX 9); (3) the *Style Manual for Standards and*

Publications of EIA, TIA, and JEDEC, EIA Engineering Publication EP-7-A ("EP-7-A"), published in August 1990 (JX 54); and (4) a revised version of EP-7-A, published in October 1995, called EP-7-B (RX 616). (Kelly, Tr. 1824-5; 1905-6; 2082-3).

Response to Finding No. 112: This proposed finding is incomplete and misleading. The work of JEDEC committees, including the patent disclosure policy, is governed by the JEDEC Manual of Organization and Procedure. (CX0208; *see also* CCFF 403-18). In addition to publication and distribution of the Manual of Organization and Procedure, JEDEC undertook to inform participants of their disclosure obligations through a variety of other methods, including presentations at JEDEC meetings, the patent tracking list and memoranda from Jim Townsend, the New Member Orientation, the sign-in sheets, the patent-related discussions contained in meeting minutes, and the JEDEC ballots. For a more complete discussion of the sources of information concerning the JEDEC patent policy, *see* CCFF 357-418

113. During the time period when Rambus was a JEDEC member, EIA policies governed the conduct of JEDEC meetings and the obligations of its members. (Kelly, Tr. 1918).

Response to Finding No. 113: This proposed finding is incomplete. In addition to the rules and procedures articulated in the EIA manuals and interpretations of EIA General Counsel, JEDEC's operating procedures are found in the JEDEC Manual of Organization and Procedure. (CX0208; *see* CCFF 403-418). As indicated by their testimony, JEDEC participants understood that the JEDEC Manual of Organization and Procedure governed JEDEC's processes. *See* CCFF 404, 840-46. When Richard Crisp requested a copy of the JEDEC patent disclosure rules in 1995, he received a copy of the JEDEC Manual of Organization and Procedure, Version 21-I. *See* CCFF 418. Finally, the Federal Circuit already has found against Rambus on this issue in holding that the expectations of the participants also governed the conduct of JEDEC programs. *See Rambus v. Infineon Technologies*, 318 F.3d 1081, 1098 (Fed. Cir. 2003).

114. Between 1990 (or earlier) and 1998, "JEDEC was a subpart" of the EIA that "existed inside the engineering department" of the EIA. (Rhoden, Tr. 289). *See also* EIA Manual of

Organization and Procedure EP-1-J, published in June 1989 (CX 206 at 30) (organizational chart showing JEDEC's position within EIA Engineering Department).

Response to Finding No. 114: Complaint Counsel does not disagree. For a more complete discussion of the legal status of JEDEC, *see* CCFF 200-204.

115. JEDEC's relationship with EIA changed in 1999, when JEDEC became a more autonomous entity. (Rhoden, Tr. 667; Kelly, Tr. 1752). Prior to that time, JEDEC "fell completely under the umbrella of the EIA for legal guides." (RX 1179 at 1).

Response to Finding No. 115: Complaint Counsel does not disagree. For a more complete discussion of the legal status of JEDEC, *see* CCFF 200-204.

116. In addition to policy manuals published by the EIA, the Complaint cites a "Manual of Organization and Procedure" published in 1993 not by EIA but by JEDEC, which was referred to as "JEP 21-I" or simply as "21-I." (Complaint, ¶ 21).

Response to Finding No. 116: This proposed finding is incomplete and misleading. In addition to the Complaint, witnesses testified that the JEDEC Manual of Organization and Procedure is the manual that governs the JEDEC standardization process. *See* CCFF 404. In addition, the JEDEC Manual of Organization and Procedure was published by EIA. (J. Kelly, Tr. 1914). The cover of the Manual contains the following legend: "Electronic Industries Association. Engineering Department." (CX0208 at 1.) The Manual also displays the trademarks of both JEDEC and EIA. (CX0208 at 1). Finally, the 21-I Manual was approved by EIA General Counsel. (J. Kelly, Tr. 1924-25).

117. EIA General Counsel John Kelly testified at trial that in the event of a conflict, the JEDEC manual was subordinate to the EIA manual. (Kelly, Tr. 1915-6).

Response to Finding No. 117: This proposed finding is misleading and incomplete because Mr. Kelly also testified that during his time at EIA, which began in 1990, he has not understood there to be any conflict between the JEDEC Manual of Organization and Procedure and any EIA manual. (J. Kelly, Tr. 1916 ("Q. Just to be clear, are you aware of any

conflict that has existed between JEDEC's separate rules and EIA rules at any time during your tenure as EIA general counsel? A. No, sir.")).

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

118. Mr. Kelly also testified that to be effective, JEDEC Manual 21-I needed approval by the EIA's Engineering Department Executive Council ("EDEC"). (Kelly, Tr. 2105).

Response to Finding No. 118: This proposed finding is incomplete, misleading, and does not support the conclusion that the 21-I Manual was not effective because the procedure for revising the 21-H manual is described within the manual itself. *See* CX0205 at 15 ("revisions . . . shall be submitted to the Council through the Council Secretary. . . Such revisions shall be considered at two regular meetings of the Council with a favorable vote at both meeting for final approval. If approved by the Council, approval by the EIA Legal Department is also required. The revisions shall then be incorporated into the Manual.") (emphasis added). The steps for revising the 21-H manual were followed. (CX0054 at 7; CX0055 at 2; G. Kelley, Tr. 2423-28; J. Kelly, Tr. 1924-25). In addition, witnesses testified that the JEDEC Manual of Organization and Procedure is the manual that governs the JEDEC standardization process. *See* CCFF 404. Finally,

the JEDEC Manual of Organization and Procedure was published by EIA. (J. Kelly, Tr. 1914). The cover of the Manual contains the following legend: "Electronic Industries Association. Engineering Department." (CX0208 at 1.) The Manual also displays the trademarks of both JEDEC and EIA. (CX0208 at 1).

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

119. Mr. Kelly testified that he did not know whether JEDEC Manual 21-I had ever received EDEC approval. (Kelly, Tr. 2105).

Response to Finding No. 119: This proposed finding is incomplete, misleading, and does not support the conclusion that the 21-I Manual was not effective because the procedure for revising the 21-H manual is described within the manual itself. *See* CX0205 at 15 ("revisions . . . shall be submitted to the Council through the Council Secretary. . . Such revisions shall be considered at two regular meetings of the Council with a favorable vote at both meeting for final approval. If approved by the Council, approval by the EIA Legal Department is also required. The revisions shall then be incorporated into the Manual.") (emphasis added). The steps for revising the 21-H manual were followed. (CX0054 at 7; CX0055 at 2; G. Kelley, Tr. 2423-28; J.

Kelly, Tr. 1924-25). In addition, witnesses testified that the JEDEC Manual of Organization and Procedure is the manual that governs the JEDEC standardization process. *See* CCFF 404. Finally, the JEDEC Manual of Organization and Procedure was published by EIA. (J. Kelly, Tr. 1914). The cover of the Manual contains the following legend: "Electronic Industries Association. Engineering Department." (CX0208 at 1.) The Manual also displays the trademarks of both JEDEC and EIA. (CX0208 at 1).

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

120. No witness testified at trial that JEDEC Manual 21-I had received EDEC approval.

Response to Finding No. 120: This proposed finding is incomplete, misleading, and does not support the conclusion that the 21-I Manual was not effective because the procedure for revising the 21-H manual is described within the manual itself. *See* CX0205 at 15 ("revisions . . . shall be submitted to the Council through the Council Secretary. . . Such revisions shall be considered at two regular meetings of the Council with a favorable vote at both meeting for final approval. If approved by the Council, approval by the EIA Legal Department is also required. The revisions shall then be incorporated into the Manual.") (emphasis added). The steps for

revising the 21-H manual were followed. (CX0054 at 7; CX0055 at 2; G. Kelley, Tr. 2423-28; J. Kelly, Tr. 1924-25). In addition, witnesses testified that the JEDEC Manual of Organization and Procedure is the manual that governs the JEDEC standardization process. *See* CCFF 404. Finally, the JEDEC Manual of Organization and Procedure was published by EIA. (J. Kelly, Tr. 1914). The cover of the Manual contains the following legend: "Electronic Industries Association. Engineering Department." (CX0208 at 1.) The Manual also displays the trademarks of both JEDEC and EIA. (CX0208 at 1).

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

121. Complaint Counsel did not meet their burden of proof to show that JEDEC Manual 21-I ever became effective.

Response to Finding No. 121: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Furthermore, RPF 121 is contrary to the weight of the evidence. *See* CCFF 403-18, CCRF 118-20.

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

122. An earlier version of JEP 21-I, called JEP 21-H, was in effect when Rambus joined JEDEC. (CX 205 at 1; Kelly, Tr. 1914).

Response to Finding No. 122: Complaint Counsel does not disagree.

123. Another manual was issued in 1994 called the "JC 42 Members' Manual." (RX 507 at 1). The JC 42 Members' Manual was intended to "assist new (and established) members [of the JC 42 committee] in achieving full effectiveness in the standards making process." (RX 507 at 2).

Response to Finding No. 123: This proposed finding is incorrect and misleading because the JC 42 Members' Manual was not "issued" by JEDEC or EIA. As is indicated from the cover of the document, the Members' Manual was a document that was put together by Jim Townsend, not JEDEC or EIA. (RX0507 at 1). Unlike the JEDEC Manual of Organization and Procedure, Mr. Townsend's Members' Manual does not display the JEDEC or EIA trademarks or otherwise purport to be an official EIA publication. Unlike the JEDEC Manual of Organization and Procedure, there is no evidence that Mr. Townsend's Members' Manual was approved by the JEDEC Council (*cf.* CX0054 at 7; CX0055 at 2; G. Kelley, Tr. 2423-28) or considered by participants to be an official articulation of the rules of JEDEC. In fact the uncontradicted

evidence demonstrates that Mr. Townsend's Members' manual was not an official document and that JEDEC participants were well aware of this fact. *See* JX0031 at 4 ("Members Manual. A copy of some Committee procedures was circulated by Mr. Townsend. Some of this material is not approved by JEDEC . . . It should be clear that this manual is not a publication of JEDEC because it has not been balloted by Committee or Council"). *Cf.* CCFF 404. That explains why, unlike the JEDEC Manual of Organization and Procedure, Mr. Townsend's Members' Manual does not display the JEDEC or EIA trademarks or otherwise purport to be an official EIA publication.

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

124. Another policy in effect during the time that Rambus was a JEDEC member was called the "ANSI Patent Policy." The American National Standards Institute ("ANSI") was and is an umbrella organization that accredits standards-setting organizations, including EIA. (Kelly, Tr. 1947-8; 2074-5).

Response to Finding No. 124: This proposed finding is incorrect because the ANSI Patent Policy was not "in effect" at JEDEC. There is no evidence that the ANSI patent policy was approved by the JEDEC Council or EIA General Counsel. As explained by EIA

General Counsel, John Kelly, EIA and JEDEC policies differ from the ANSI policy in certain material respects, including the treatment of patent applications. *See* CCFF 442.

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

125. ANSI published "Guidelines" regarding its Patent Policy. The ANSI Patent Policy Guidelines were circulated to JEDEC 42.3 members in 1994 at the request of EIA General Counsel John Kelly. (CX 353 at 1). The ANSI Guidelines were also attached to the May 1992 JC 42.3 meeting minutes. (CX 34 at 19).

Response to Finding No. 125: This proposed finding does not support the conclusion that the ANSI patent policy had any effect at JEDEC because, *inter alia*, the ANSI patent policy guidelines specifically contemplate that standard setting organizations like JEDEC may adopt provisions that differ materially from the ANSI patent policy and still comply with the guidelines. (RX1712 at 3). Of particular relevance in this matter, ANSI patent policy guidelines specifically provide that "a standards developer may wish to encourage participants to disclose the existence of pending U.S. patent applications." (RX1712 at 8). For a more complete discussion of the relationship between the ANSI Patent Policy, the ANSI Patent policy guidelines, and the JEDEC patent policy, *see* CCFF 435-43.

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

126. EIA General Counsel John Kelly caused the ANSI Patent Policy Guidelines to be circulated to JC 42.3 members in 1994 because he "thought they provided insight into the proper interpretation of the EIA and JEDEC patent policy." (Kelly, Tr. 1950).

Response to Finding No. 126: This proposed finding does not support the conclusion that the ANSI patent policy had any effect at JEDEC because, *inter alia*, the ANSI patent policy guidelines specifically contemplate that standard setting organizations like JEDEC may adopt provisions that differ materially from the ANSI patent policy and still comply with the guidelines. (RX1712 at 3). Of particular relevance in this matter, ANSI patent policy guidelines specifically provide that "a standards developer may wish to encourage participants to disclose the existence of pending U.S. patent applications." (RX1712 at 8). For a more complete discussion of the relationship between the ANSI Patent Policy, the ANSI Patent policy guidelines, and the JEDEC patent policy, *see* CCFF 435-43. In addition, Respondent appears to concede that Mr. Kelly never sent the actual ANSI patent policy to JEDEC participants, only the guidelines. This underscores the fact that the ANSI patent policy was never adopted by JEDEC.

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

127. EIA Manual EP-7-B, published in October 1995, provided that "[s]tandards and publications are adopted by EIA in accordance with the American National Standards Institute (ANSI) patent policy." (RX 616 at 2).

Response to Finding No. 127: This proposed finding does not support the conclusion that the ANSI patent policy had any effect at JEDEC because, *inter alia*, the ANSI patent policy guidelines specifically contemplate that standard setting organizations like JEDEC may adopt provisions that differ materially from the ANSI patent policy and still comply with the guidelines. (RX1712 at 3). Of particular relevance in this matter, ANSI patent policy guidelines specifically provide that "a standards developer may wish to encourage participants to disclose the existence of pending U.S. patent applications." (RX1712 at 8). From time to time, EIA standards are proposed to be American National Standards through a review process conducted by ANSI. *See* CCFF 436. As a part of that process, such EIA standards must have been adopted pursuant to a process that complies with ANSI Guidelines. EIA's patent policy is in compliance with ANSI Guidelines. *See* CCFF 440. Furthermore, the ANSI patent policy and guidelines have even less relevance within JEDEC because JEDEC is not an ANSI accredited organization (J. Kelly, Tr.

1949) and, therefore, is not even required to comply with the ANSI guidelines, much less the ANSI patent policy itself.. For a more complete discussion of the relationship between the ANSI Patent Policy, the ANSI Patent policy guidelines, and the JEDEC patent policy, *see* CCFF 435-43.

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

C. The Manuals And Policies That Governed JEDEC's Standardization Activities While Rambus Was A Member Encouraged, But Did Not Require, Disclosure Of Intellectual Property Interests.

128. One of the issues addressed at trial was whether the manuals and policies governing EIA/JEDEC standardization activities while Rambus was a JEDEC member *encouraged*, or instead *required*, the disclosure at certain times and in certain circumstances of a member's intellectual property interests.

Response to Finding No. 128: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Furthermore, RPF 121 is contrary to the weight of the evidence. *See* CCFF 403-18. Finally, the Federal Circuit has held against Rambus on this very issue and found that disclosure of relevant patent information

was an obligation of JEDEC participants. *Rambus, Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1098 (Fed. Cir. 2003).

1. The EIA Legal Guides Do Not Require The Disclosure Of Intellectual Property Interests.

129. The EIA Legal Guides state that they govern "all EIA engineering standardization and related programs." (CX 204 at 4).

Response to Finding No. 129: This proposed finding is incomplete and misleading because, in addition to the basic rules set forth in the EIA Legal Guides, the procedures specifically applicable to the JEDEC standardization process are contained in the JEDEC Manual of Organization and Procedure. *See* CCFF 404; J. Kelly, Tr. 1914 (Manual of Organization and Procedure. Applied to sector-specific JEDEC engineering programs).

130. The EIA Legal Guides were required to be followed by JEDEC members. (Kelly, Tr. 1829-30; CX 206 at 6).

Response to Finding No. 130: This proposed finding is incomplete and misleading because, in addition to the basic rules set forth in the EIA Legal Guides, the procedures specifically applicable to the JEDEC standardization process are contained in the JEDEC Manual of Organization and Procedure. *See* CCFF 404; J. Kelly, Tr. 1914 (Manual of Organization and Procedure. Applied to sector-specific JEDEC engineering programs).

131. The EIA Legal Guides provide that a "basic objective" of EIA standardization activity was that "[s]tandards are proposed or adopted by EIA without regard to whether their proposal or adoption may in any way involve patents on articles, materials, or processes." (CX 204 at 4). The EIA Legal Guides state that this "basic objective" applies to "all EIA engineering standardization and related programs." (CX 204 at 4).

Response to Finding No. 131: This proposed finding is incomplete and misleading because, in addition to the basic rules set forth in the EIA Legal Guides, the procedures specifically applicable to the JEDEC standardization process are contained in the JEDEC Manual

of Organization and Procedure. *See* CCFF 404; J. Kelly, Tr. 1914 (Manual of Organization and Procedure. Applied to sector-specific JEDEC engineering programs).

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

132. The EIA Legal Guides do not contain any reference to any disclosure obligation in connection with a member's intellectual property interests. (CX 204).

Response to Finding No. 132: The obligations of JEDEC members included the the obligation to act in good faith and avoid anticompetitive results, in addition to the obligation to disclose intellectual property claims related to JEDEC work. *See* CCFF 300-443. This finding is incomplete because it omits the fact that the EIA Legal Guides anticipate that EIA sponsored standard-setting groups will enact their own "policies and procedures" in order to ensure compliance with the basic standards of conduct that are set forth in the Guides. (*See, e.g.*, CX0204 at 6 ("All EIA standardization programs shall be conducted in accordance with the following basic rules: (1) They shall be carried on in good faith under polices and procedures which will assure fairness and unrestricted participation; . . .") (emphasis added)).

Because each EIA-sponsored standard-setting group must establish its own policies and procedures to guarantee compliance with the basic standards of conduct set forth in the EIA Legal Guides, the proposed finding is irrelevant. The 21-I Manual contains the relevant policy for the patent disclosure obligation. Even the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

2. <u>The EIA Manuals That Were In Effect When Rambus Joined JEDEC Did Not Contain Any Reference To Any Disclosure Obligation</u>.

133. The EP-3-F manual and the EP-7-A manual were in effect when Rambus joined JEDEC. (Kelly, Tr. 1824-5; 1905-6; 2082-3). Neither the EP-3-F manual nor the EP-7-A manual makes any explicit reference to an obligation on the part of EIA members or others to disclose patents or patent applications. (CX 203A; JX 54).

<u>Response to Finding No. 133</u>: This proposed finding is misleading because, as Rambus concedes in RPF 134 and RPF 138 below, EP-3-F and EP-7-A, respectively, both contain a requirement that no standard shall refer to a product on which there is a known patent unless all the technical information covered by the patent is known to the committee or working group. (CX0203A at 11-12; JX0054 at 9). It is axiomatic that a patent or patent application cannot be "known" to the committee or the Chairman unless the patent has been disclosed. John Kelly, EIA

General Counsel, testified that the EP-3-F and EP-7-A manuals required members to "facilitate" compliance with the provision in these manuals against EIA standards containing patented material unless the necessary technical information is known by "disclosing on an early basis known patents and patent applications that relate to the work of the committee." (Kelly, Tr. 1870 (discussing EP-3-F); *Id.* 1905-06 (describing Section 3.4 of EP-7-A and Section 8.3 of EP-3-F as imposing an obligation to disclose relevant patents or patent applications on participants of EIA standardization activities); *see also* Rhoden, Tr. 347-48).

134. The October 1981 EIA manual known as "EP-3-F" provides in part:

> "8.3 Reference to Patented Products In EIA Standards
>
> Requirements in EIA Standards which call for the use of patented items should be avoided. No program of standardization shall refer to a product on which there is a known patent unless all the technical information covered by the patent is known to the Formulating committee, subcommittee or working group. The Committee Chairman must have also received a written expression from the patent holder that he is willing to license applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination. Additionally, when a known patented item is referred to in an EIA Standard, a Caution Notice, as outlined in the Style Manual, EP-7, shall appear in the EIA Standard."

(CX 203A at 11).

Response to Finding No. 134: This proposed finding does not support the conclusion that EP-3-F does not contain a disclosure obligation. *See* CCRF 133.

135. The language used in paragraph 8.3 of EP-3-F does not call for disclosure of intellectual property interests by anyone. It instead describes the approach to be implemented if a standard refers to, or calls for the use of, "known patents." (CX 203A at 11).

Response to Finding No. 135: This proposed finding is incomplete and misleading because paragraph 8.3 of EP-F-3 contains more than the approach to be implemented when patents or patent applications are disclosed. Specifically, paragraph 8.3 states "Requirements in EIA Standards which call for the use of patented items should be avoided. No

program of standardization shall refer to a product on which there is a known patent unless all the technical information covered by the patent is known to the Formulating committee, subcommittee or working group." (CX0203A at 11). These two sentences represent substantive rules that admonish participants to avoid standards that include patented technology *and* require the disclosure of patents and patent applications before the committee may consider including patented technology in a standard. EIA interpreted this language as "an obligation to disclose." (J. Kelly, Tr. 1905). The only "approaches" to be implemented according to paragraph 8.3 are the requirements that the Chairman obtain the appropriate licensing assurance and that the appropriate notice be included in the publication of a standard that does contain known patented or patentable material.

136. EP-3-F clearly states that *if* a standard calls for the use of a "known patent," the Committee Chairman "must" have received an assurance from the patent holder that it is willing to license the patent on reasonable and nondiscriminatory terms.

Response to Finding No. 136: This proposed finding does not support the conclusion that EP-3-F does not contain a disclosure obligation. *See* CCRF 133, 135.

137. It is reasonable to assume that if this section of EIA Manual EP-3-F was intended to impose a mandatory obligation of patent disclosure upon a standards participant, it would have: (1) mentioned disclosure; and (2) used mandatory language such as "must." (CX 203A at 11).

Response to Finding No. 137: This proposed finding is contrary to the weight of the evidence and unsupported by record evidence. (J. Kelly, Tr. 1870, 1905 (EIA interpreted this language as "an obligation to disclose.")). For a more complete description of EP-3-F, *see* CCFF 396-98 and CCRF 133, 135.

138. The 1990 EIA manual known as "EP-7-A" provides in part:

> 3.4 Patented Items or Processes
>
> Avoid requirements in EIA standards that call for the exclusive use of a patented item or process. No program [of] standardization shall refer to a patented item or process unless all of the technical

> information covered by the patent is known to the formulating committee or working group, and the committee chairman has received a written expression from the patent holder that one of the following conditions prevails:
>
> (1) a license shall be made available without charge to applicants desiring to utilize the patent for the purpose of implementing the standard, or
>
> (2) a license shall be made available to applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination.
>
> . . . An appropriate footnote shall be included in the standard identifying the patented item and describing the conditions under which the patent holder will grant a license (*see* 6.5.2).

(JX 54 at 9-10).

Response to Finding No. 138: This proposed finding does not support the conclusion that EP-3-F does not contain a disclosure obligation. *See* CCRF 133. *See also* (J. Kelly, Tr. 1870, 1905 (EIA interpreted this language as "an obligation to disclose.")).

139. The language used in paragraph 3.4 of EP-7-A does not call for disclosure of intellectual property interests by anyone. It instead describes the approach to be implemented if a standard is to refer to, or call for the exclusive use of, a patented item or process.

Response to Finding No. 139: This proposed finding is incomplete and misleading because paragraph 3.4 of EP-7-A contains more than the approach to be implemented when patents or patent applications are disclosed. Specifically, paragraph 3.4 states "Avoid requirements in EIA standards that call for the exclusive use of a patented item or process. No program [of] standardization shall refer to a patented item or process unless all of the technical information covered by the patent is known to the formulating committee or working group. . ." (JX0054 at 9-10). These two sentences represent substantive rules that admonish participants to avoid standards that include patented technology *and* require the disclosure of patents and patent applications before the committee may consider including patented technology in a standard. EIA

interpreted this language as "an obligation to disclose." (J. Kelly, Tr. 1905). The only "approaches" to be implemented according to paragraph 8.3 are the requirements that the Chairman obtain the appropriate licensing assurance and that the appropriate notice be included in the publication of a standard that does contain known patented or patentable material.

140. It is reasonable to assume that like EP-3-F, EIA Manual EP-7-A would have used mandatory language such as "must" if its framers had intended it to communicate to readers the existence of a mandatory disclosure obligation.

Response to Finding No. 140: This proposed finding is contrary to the weight of the evidence and unsupported by record evidence. (Kelly, Tr. 1870, 1905-06 discussed, *supra*, at CCRF 133; *see also* Rhoden, Tr. 347-48). For a more complete description of EP-7-A, *see* CCFF 399-402.

3. The ANSI Patent Policy, Which Was Officially Adopted By The EIA At Least As Early As October 1995, Does Not RequireThe Disclosure Of Intellectual Property Interests. The EIA Informed The FTC In 1996 That Its Patent Policy Did Not Require Such Disclosure.

141. The ANSI Patent Policy was officially adopted by the EIA at least as early as October 1995, when EIA Manual EP-7-B was published. (RX 616 at 2). The EP-7-B manual provides that "[s]tandards and publications are adopted by EIA in accordance with the American National Standards Institute (ANSI) patent policy." (RX 616 at 2).

Response to Finding No. 141: This proposed finding is incorrect and misleading because it is unsupported by any witness testimony and it fundamentally misapprehends the meaning of the phrase "adopted by EIA in accordance with" in the EP-7-B Manual. ANSI does not require standard setting organizations to adhere rigidly to the precise metes and bounds of the ANSI patent policy. *See* CCFF 441. Indeed, the ANSI patent policy guidelines specifically contemplate that standard setting organizations like EIA may adopt provisions that differ materially from the ANSI patent policy and still comply with the guidelines. (RX1712 at 3). Of particular relevance in this matter, ANSI patent policy guidelines specifically provide that "a standards developer may wish to encourage participants to disclose the existence of pending U.S.

patent applications." (RX1712 at 8). From time to time, EIA standards are proposed to be American National Standards through a review process conducted by ANSI. *See* CCFF 436. As a part of that process, such EIA standards must have been adopted pursuant to a process that is consistent with minimum ANSI guidelines. Thus, EIA standards may be adopted in accordance with the ANSI Patent Policy and Guidelines, notwithstanding the fact that there are substantive differences between EIA patent policy and the ANSI patent policy. EIA is in compliance with ANSI guidelines. *See* CCFF 440. For a more complete discussion of the relationship between the ANSI patent policy, the ANSI patent policy guidelines, and the JEDEC patent policy, *see* CCFF 435-43. Furthermore, the ANSI patent policy and its guidelines have even less relevance within JEDEC because JEDEC is not an ANSI accredited organization (*see* J. Kelly, Tr. 1949) and, therefore, not even required to comply with the guidelines, much less the ANSI patent policy itself.

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

142. In a January 1996 letter to the Federal Trade Commission, the EIA stated that it "endorse[d] and follow[ed] the ANSI intellectual property rights (IPR) policy as it relates to essential patents." (RX 669 at 2). The EIA's January 1996 letter to the FTC, and its statement that the EIA "endorse[d] and follow[ed] the ANSI intellectual property rights (IPR) policy," are

consistent with EIA's formal adoption of the ANSI Patent Policy in October 1995, when EP-7-B was published. (RX 616 at 2; RX 669 at 2).

Response to Finding No. 142: This proposed finding is incorrect and misleading because it fundamentally misapprehends the meaning of the phrase "endorse[d] and follow[ed] the ANSI intellectual property rights (IPR) policy." ANSI does not require standard setting organizations to adhere rigidly to the precise metes and bounds of the ANSI patent policy. *See* CCFF 441. Indeed, the ANSI patent policy guidelines specifically contemplate that standard setting organizations like EIA may adopt provisions that differ materially from the ANSI patent policy and still comply with the guidelines. (RX1712 at 3). Of particular relevance in this matter, ANSI patent policy guidelines specifically provide that "a standards developer may wish to encourage participants to disclose the existence of pending U.S. patent applications." (RX1712 at 8). From time to time, EIA standards are proposed to be American National Standards through a review process conducted by ANSI. *See* CCFF 436. As a part of that process, such EIA standards must have been adopted pursuant to a process that is consistent with minimum ANSI guidelines. Thus, EIA standards may be adopted in accordance with the ANSI Patent Policy and Guidelines, notwithstanding the fact that there are substantive differences between EIA patent policy and the ANSI patent policy. EIA is in compliance with ANSI Guidelines. *See* CCFF 440. For a more complete discussion of the relationship between the ANSI Patent Policy, the ANSI Patent policy guidelines, and the JEDEC patent policy, *see* CCFF 435-43. Furthermore, the ANSI patent policy and its guidelines have even less relevance within JEDEC because JEDEC is not an ANSI accredited organization (*see* J. Kelly, Tr. 1949) and, therefore, not even required to comply with the guidelines, much less the ANSI patent policy itself.

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See*

CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

143. The EIA's January 1996 letter to the FTC states that the "EIA and TIA encourage the early, voluntary disclosure of patents that relate to the standards in work." (RX 669 at 3).

Response to Finding No. 143: This proposed finding is misleading because it fundamentally misapprehends the meaning on the term "voluntary" as it relates to JEDEC. JEDEC is a voluntary organization (CCFF 323) and JEDEC is unable to impose sanctions on members for failure to comply with any part of the patent policy. (CCFF 419-20). JEDEC, therefore, necessarily depends upon the good faith, voluntary cooperation of participants in complying with the requirements of the patent policy. (CCFF 314). The requirements of the patent policy, however, are mandatory for all companies that choose to be members. (CCFF 324).

144. The ANSI Patent Policy encourages, but does not require, disclosure of intellectual property interests by participants in standards-setting organizations. (Kelly, Tr. 1961).

Response to Finding No. 144: Complaint Counsel does not disagree. However, this proposed finding does not support the conclusion that EIA adopted the ANSI Patent Policy. The EIA Patent Policy contains material differences from the ANSI Patent Policy, but is in compliance with the ANSI Patent Policy and Guidelines. CCFF 442-43. As noted previously, JEDEC is not ANSI accredited and, therefore, not bound by ANSI's patent policy of guidelines. (J. Kelly, Tr. 1949).

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

145. The EIA's statement in the January 1996 letter to the FTC that it "encourage[d]" the "voluntary" disclosure of patents is consistent with the EIA's formal adoption of the ANSI Patent Policy in EIA Manual EP-7-B. (RX 616 at 2).

Response to Finding No. 145: This proposed finding is inaccurate and misleading because, as explained in CCRF 141, EIA did not adopt the ANSI Patent Policy. (*See also* CCFF 439-443).

146. The EIA's statement in the January 1996 letter to the FTC that disclosure of patents by EIA members was "encouraged" and "voluntary" is wholly inconsistent with the proposition that the EIA manuals then in effect required disclosure of patents by EIA members. (RX 669 at 2).

Response to Finding No. 146: This proposed finding is contrary to the weight of the evidence. EIA/JEDEC manuals, presentation made at JEDEC meetings, Mr. Townsend's memoranda, the New Member Orientation, the sign-in sheets, the discussions of the patent policy contained in meeting minutes, and JEDEC ballots make clear that the obligation to disclose was mandatory. *See* CCFF 357-418. In addition, the testimony of JEDEC participants confirms that the obligation to disclose was mandatory. *See* CCFF 324. Finally, the *Infineon* court also found

that the rules of JEDEC imposed a disclosure duty. *See Rambus, Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1098 (Fed. Cir. 2003).

147. By 1990, the EIA had selected Webster's Third New International Dictionary, Unabridged as the official reference guide for the language used in EIA publications and standards. (JX 54 at 3).

Response to Finding No. 147: Complaint Counsel does not disagree.

148. The Administrative Law Judge may and does take official notice that the definitions of "voluntary" in Webster's Third New International Dictionary include an act "performed, made, or given of one's own free will" and an act performed "without any present legal obligation to do the thing done or any such obligation that can accrue from the existing state of affairs. . . ." Webster's Third New International Dictionary, Unabridged (1986), p. 2564.

Response to Finding No. 148: This proposed finding does not support the conclusion that the disclosure of patents and patent applications at JEDEC was voluntary. "Voluntary" as it relates to JEDEC refers to the fact that JEDEC is a voluntary organization (CCFF 323) and JEDEC is unable to impose sanctions on members for failure to comply with any part of the patent policy. (CCFF 419-20). JEDEC, therefore, necessarily depends upon the good faith, voluntary cooperation of participants in complying with the requirements of the patent policy. (CCFF 314). The requirements of the patent policy, however, are mandatory for all companies that choose to be members. (CCFF 324). *See also Rambus, Inc. v. Infineon Technologies AG*, 318 F.2d 1081, 1098 (Fed. Cir. 2003).

149. The January 1996 letter to the FTC was submitted on behalf of EIA and its unincorporated divisions and departments (including JEDEC), as well as on behalf of the Telecommunications Industries Association ("TIA"). (RX 669 at 5; Kelly, Tr. 2094).

Response to Finding No. 149: Complaint Counsel does not disagree. However, this proposed finding does not support the conclusion that the disclosure of patents and patent applications at JEDEC is voluntary because RPF 149, in conjunction with RPF 143, fundamentally misapprehends the meaning on the term "voluntary" as it relates to JEDEC. JEDEC is a voluntary organization (CCFF 323) and JEDEC is unable to impose sanctions on members for failure to

comply with any part of the patent policy. (CCFF 419-20). JEDEC, therefore, necessarily depends upon the good faith, voluntary cooperation of participants in complying with the requirements of the patent policy. (CCFF 314). The requirements of the patent policy, however, are mandatory for all companies that choose to be members. (CCFF 324). *See also Rambus, Inc. v. Infineon Technologies AG*, 318 F.2d 1081, 1098 (Fed. Cir. 2003).

150. The EIA's January 1996 letter to the FTC was reviewed and approved by EIA General Counsel John Kelly before it was sent to the FTC. (Kelly, Tr. 2092-3). Mr. Kelly's name appears in the signature block, along with the name of Mr. Dan Bart, the Vice President for Standards and Technology for both the EIA and the TIA, and the name of Mr. Paul Vishny, outside counsel for the TIA. (RX 669 at 5).

Response to Finding No. 150: This proposed finding does not support the conclusion that the disclosure of patents and patent applications at JEDEC is voluntary because RPF 150, in conjunction with RPF 143, fundamentally misapprehends the meaning on the term "voluntary" as it relates to JEDEC. JEDEC is a voluntary organization (CCFF 323) and JEDEC is unable to impose sanctions on members for failure to comply with any part of the patent policy. (CCFF 419-20). JEDEC, therefore, necessarily depends upon the good faith, voluntary cooperation of participants in complying with the requirements of the patent policy. (CCFF 314). The requirements of the patent policy, however, are mandatory for all companies that choose to be members. (CCFF 324). *See also Rambus, Inc. v. Infineon Technologies AG*, 318 F.2d 1081, 1098 (Fed. Cir. 2003).

151. In July 1996, the FTC responded to the EIA's January 1996 letter in a letter signed by FTC Secretary Donald Clark. The FTC's letter states in part that:

> "EIA and TIA, following ANSI procedures, encourage the early, voluntary disclosure of patents, but do not require a certification by participating companies regarding potentially conflicting patent interests."

(RX 740 at 1).

Response to Finding No. 151: This proposed finding is not reliable and does not support the conclusion that the disclosure of patents and patent applications at JEDEC is

voluntary. Secretary Clark's letter is a response to confirm receipt of a letter from the EIA, written within a few days of receiving the EIA letter. It is not probative evidence of the understanding of the Commission, Secretary Clark, of any employee of the Commission with respect to the EIA patent policy. Interpreting Secretary Clark's letter to mean that the JEDEC patent policy was voluntary is contrary to the weight of the evidence. *See* CCFF 324; Rhoden, Tr. 618-19 ("I believe you're asking to make a judgment in terms of the legal aspects [of Secretary Clark's letter], and I'm not sure I'm either qualified or prepared to do that. What I can give you as an answer is that in the functioning of the JEDEC committees, inside of EIA, with the patent policies that were in place at the time, that were reiterated at every single meeting, that you were obligated to disclose if you had IP that you felt was relevant and should do so.").

152. The FTC's July 10, 1996 letter points out that the EIA's patent policy was different from the policy of the standard-setting organization involved in the *Dell* case, where the policy *did* require a certification regarding "potentially conflicting patent interests." (RX 740 at 2).

Response to Finding No. 152: This proposed finding does not support the conclusion that the disclosure of patents and patent applications at JEDEC is voluntary. *See* CCRF 151. The fact that JEDEC does not utilize a written certification is not evidence that the disclosure obligation is voluntary.

153. The FTC's statement distinguishing the EIA's patent policy from the policy at issue in the *Dell* matter, and the FTC's explanation that the differences in the two patent policies meant that the "expectations of participants in the two standard-setting processes differ," show that the FTC staff and Secretary Clark interpreted the EIA's January 1996 letter to mean what it says – that the EIA encouraged, but did not require, the disclosure by members of intellectual property interests. (RX 740 at 2; RX 669 at 2).

Response to Finding No. 153: This proposed finding is misleading, unreliable, and does not support the conclusion that the disclosure of patents and patent applications at JEDEC is voluntary. As an initial matter, as Respondent concedes in RPF 152 above, the *Dell* case involved the requirement for members to sign a written certification. Complaint Counsel

agree that, unlike the *Dell* case, JEDEC require members to sign a written certification. The absence of such a requirement, however, is not evidence that the disclosure obligation is voluntary. In addition, there is no evidence that the Commission, Secretary Clark, or any employee of the Commission "interpreted" anything relating to the EIA patent policy. Complaint Counsel notes that Rambus did not call Mr. Clark as a witness to establish that he did anything other than repeat the language of the EIA letter. Mr. Clark was available, and travel expenses would have been negligible. Secretary Clark's letter is not probative evidence of the understanding of the Commission, Secretary Clark, of any employee of the Commission with respect to the EIA patent policy. Finally, interpreting Secretary Clark's letter to mean that the JEDEC patent policy was voluntary is contrary to the weight of the evidence. *See* CCFF 324; Rhoden, Tr. 618-19 ("I believe you're asking to make a judgment in terms of the legal aspects [of Secretary Clark's letter], and I'm not sure I'm either qualified or prepared to do that. What I can give you as an answer is that in the functioning of the JEDEC committees, inside of EIA, with the patent policies that were in place at the time, that were reiterated at every single meeting, that you were obligated to disclose if you had IP that you felt was relevant and should do so.").

154. No evidence was submitted at trial that the FTC staff or Secretary Clark in fact understood from the EIA's January 1996 letter that the EIA's policies required mandatory disclosure of any intellectual property interests.

Response to Finding No. 154: This proposed finding is unreliable because Secretary Clark's letter is not probative evidence of the understanding of the Commission, Secretary Clark, of any employee of the Commission with respect to the EIA patent policy. Interpreting Secretary Clark's letter to mean that the JEDEC patent policy was voluntary is contrary to the weight of the evidence. *See* CCFF 324; Rhoden, Tr. 618-19 ("I believe you're asking to make a judgment in terms of the legal aspects [of Secretary Clark's letter], and I'm not sure I'm either qualified or prepared to do that. What I can give you as an answer is that in the

functioning of the JEDEC committees, inside of EIA, with the patent policies that were in place at the time, that were reiterated at every single meeting, that you were obligated to disclose if you had IP that you felt was relevant and should do so.").

155. No evidence was submitted at trial that any EIA official had informed the FTC in 1996 that the FTC had misunderstood the "voluntary" nature of patent disclosure under the EIA's policies.

Response to Finding No. 155: This proposed finding is misleading and unreliable because there is no evidence that the Commission, Secretary Clark, or any employee of the Commission had an "understanding" of EIA policies in 1996. Secretary Clark's letter is not probative evidence of the understanding of the Commission, Secretary Clark, of any employee of the Commission with respect to the EIA patent policy. Interpreting Secretary Clark's letter to mean that the JEDEC patent policy was voluntary is contrary to the weight of the evidence. *See* CCFF 324; Rhoden, Tr. 618-19 ("I believe you're asking to make a judgment in terms of the legal aspects [of Secretary Clark's letter], and I'm not sure I'm either qualified or prepared to do that. What I can give you as an answer is that in the functioning of the JEDEC committees, inside of EIA, with the patent policies that were in place at the time, that were reiterated at every single meeting, that you were obligated to disclose if you had IP that you felt was relevant and should do so.").

156. Complaint Counsel did not call Secretary Clark to testify at trial about the July 10, 1996 letter to the EIA and TIA.

Response to Finding No. 156: Complaint Counsel did not call Mr. Clark to testify at trial about the July 10, 1996, letter because the letter is not probative of any issue in this case. This proposed finding does not support the conclusion that the Commission, Secretary Clark, or any employee of the Commission understood the members' obligations under the JEDEC patent policy. Furthermore, RPF 156 does not support the ultimate conclusion that the disclosure of

patents and patent applications at JEDEC was voluntary. Moreover, Rambus had the opportunity to call Secretary Clark to better understand his ministerial involvement in the process of replying to persons who comment on proposed Commission consent orders, but chose not to do so. Mr. Clark was available to Rambus as a witness and his travel expenses would have been negligible.

157. On July 10, 1996, JEDEC Secretary Kenneth McGhee sent a memorandum to "JEDEC Council Members and Alternates" regarding the FTC's Final Consent Order in the *Dell* case, which memorandum stated in part that:

> "ANSI and EIA do however, encourage early, voluntary disclosure of any known essential patents."

(RX 742 at 1).

Response to Finding No. 157: Complaint Counsel does not disagree. However, this proposed finding does not support the conclusion that the disclosure of patents and patent applications at JEDEC is voluntary because RPF 150, in conjunction with RPF 143, fundamentally misapprehends the meaning on the term "voluntary" as it relates to JEDEC. JEDEC is a voluntary organization (CCFF 323) and JEDEC is unable to impose sanctions on members for failure to comply with any part of the patent policy. (CCFF 419-20). JEDEC, therefore, necessarily depends upon the good faith, voluntary cooperation of participants in complying with the requirements of the patent policy. (CCFF 314). The requirements of the patent policy, however, are mandatory. (CCFF 324). Further, RPF 157 is incomplete and misleading because, as is clear from the face of the document, the purpose of Mr. McGhee's memorandum was to inform JEDEC Council members and alternates that EIA "filed Comments with the FTC . . . requesting the FTC to limit its application of the law to the narrow facts of [the *Dell*] case and not to impose a general obligation on participants in standard-setting activities to search their patent portfolios" (RX0742 at 1). Finally, it also is clear that EIA understood the Commission's action did not "signal a general duty to search for patents when a company engages in standards setting." (RX0742 at 1).

158. Mr. McGhee's July 10, 1996 memorandum is dated the same day as the FTC's July 10, 1996 letter to the EIA and TIA. (RX 742 at 1; RX 740 at 1).

Response to Finding No. 158: Complaint Counsel does not disagree.

159. Mr. McGhee's July 10, 1996 memorandum stating in part that the EIA "encourage[s] early, voluntary disclosure of any known essential patents" was subsequently shown to JEDEC 42.3 members. (RX 742 at 1; Calvin, Tr. 1076).

Response to Finding No. 159: Complaint Counsel does not disagree. However, this proposed finding does not support the conclusion that the disclosure of patents and patent applications at JEDEC is voluntary because RPF 150, in conjunction with RPF 143, fundamentally misapprehends the meaning on the term "voluntary" as it relates to JEDEC. JEDEC is a voluntary organization (CCFF 323) and JEDEC is unable to impose sanctions on members for failure to comply with any part of the patent policy. (CCFF 419-20). JEDEC, therefore, necessarily depends upon the good faith, voluntary cooperation of participants in complying with the requirements of the patent policy. (CCFF 314). The requirements of the patent policy, however, are mandatory. (CCFF 324). Further, RPF 157 is incomplete and misleading because, as is clear from the face of the document, the purpose of Mr. McGhee's memorandum was to inform JEDEC Council members and alternates that EIA "filed Comments with the FTC . . . requesting the FTC to limit its application of the law to the narrow facts of [the *Dell*] case and not to impose a general obligation on participants in standard-setting activities to search their patent portfolios" (RX0742 at 1). Finally, it also is clear that EIA understood the Commission's action did not "signal a general duty to search for patents when a company engages in standards setting." (RX0742 at 1).

4. JEDEC Manual 21-H, Which Was In Effect When Rambus Joined JEDEC, Contains No Reference To A Disclosure Obligation.

160. JEDEC Manual of Organization and Procedure 21-H, which was in effect when Rambus joined JEDEC in 1992, provided that "JEDEC standards are adopted without regard to whether or not their adoption may involve patents on articles, materials or processes." (CX 205A at 11).

Response to Finding No. 160: Complaint Counsel does not disagree. However, this proposed finding is incomplete because the 21-H Manual specifically incorporates the EIA Legal Guides (*see* CCFF 406; CX0205 at 14), which require all EIA programs to be conducted in good faith and in a manner that would not result in giving competitive advantage to any company. *See* CCFF 310-15. Further, RPF 160 does not support the conclusion that JEDEC did not have a disclosure policy from 1991 to 1993. *See* CCFF 321, 416. In addition, this finding is misleading and ignores substantial evidence in the record that this and similar language were disclaimers that "EIA does not conduct patent searches, and therefore, can't assume any liability if patents somehow creep into standards unbeknownst to us." (J. Kelly, Tr. 1835).

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

161. JEDEC manual 21-H contains no other reference to intellectual property. (CX 205A; Kelley, Tr. 2685).

Response to Finding No. 161: Complaint Counsel does not disagree. However, this proposed finding is incomplete because the 21-H Manual specifically incorporates the EIA Legal Guides (*see* CCFF 406; CX0205 at 14), which require all EIA programs to be conducted in

good faith and in a manner that would not result in giving competitive advantage to any company. *See* CCFF 310-15. In addition, this finding is misleading and ignores substantial evidence in the record that this and similar language were disclaimers that "EIA does not conduct patent searches, and therefore, can't assume any liability if patents somehow creep into standards unbeknownst to us." (J. Kelly, Tr. 1835). Further, RPF 161 does not support the conclusion that JEDEC did not have a disclosure policy from 1991 to 1993. *See* CCFF 321, 416.

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

5. <u>The Application Form Used By Rambus When Joining JEDEC Contains No Reference To A Disclosure Obligation</u>.

162. The application form that Rambus filled out when it applied to join JEDEC says nothing about intellectual property or about its disclosure by JEDEC members. (CX 601 at 1-2).

<u>Response to Finding No. 162</u>: Complaint Counsel does not disagree. However, this proposed finding is misleading and does not support the conclusion either that Rambus was not subject to JEDEC's patent policy or that Rambus was not informed of JEDEC's patent policy. As the Federal Circuit held, JEDEC's rules imposed a disclosure duty on its members. *See Rambus, Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1098 (Fed. Cir. 2003). Further,

Rambus was informed of its obligations under the patent policy through presentations at JEDEC meetings, Mr. Townsend's memoranda, the New Member Orientation, sign-in sheets, discussions of patent-related issues in JEDEC meting minutes, JEDEC ballots, and JEDEC manuals. *See* CCFF 357-418.

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

6. JEDEC Manual 21-I, Published In October 1993, Does Refer To A Disclosure Obligation. The Record Contains No Evidence, However, That The 21-I Manual Received The Necessary EDEC Approval.

163. JEDEC Manual of Organization and Procedure 21-I, also known as "JEP 21-I," bears an October 1993 publication date. (CX 208 at 1).

Response to Finding No. 163: Complaint Counsel does not disagree. However, this proposed finding is incomplete because it fails to mention that the proposed revisions were discussed at JEDEC meetings at which Rambus was present in 1992 and 1993. *See* CCFF 411-13.

164. JEP 21-I refers to an obligation on the part of committee chairpersons to "call attention to the obligation of all participants to inform the meeting of any knowledge they may have of any patents, or pending patents, that might be involved in the work they are undertaking." (CX 208 at 19).

Response to Finding No. 164: Complaint Counsel does not disagree. For a more complete statement of the disclosure obligation of all participants contained in the JEDEC Manual of Organization and Procedure, *see* CCFF 319.

165. JEP 21-I needed approval by the EIA's Engineering Department Executive Council ("EDEC") in order to be effective. (Kelly, Tr. 2105).

Response to Finding No. 165: This proposed finding is incomplete, misleading, and does not support the conclusion that the 21-I Manual was not effective because the procedure for revising the 21-H manual is described within the manual itself. *See* CX0205 at 15 ("revisions . . . shall be submitted to the Council through the Council Secretary. . . Such revisions shall be considered at two regular meetings of the Council with a favorable vote at both meeting for final approval. If approved by the Council, approval by the EIA Legal Department is also required. The revisions shall then be incorporated into the Manual.") (emphasis added). The steps for revising the 21-H manual were followed. *See* CX0054 at 7 (Initial JEDEC Council approval of 21-I manual); CX0055 at 2 (Second approval of 21-I manual be JEDEC Council); G. Kelley, Tr. 2423-28 (discussing first and second approvals of 21-I manual by JEDEC Council). Further, witnesses testified that the JEDEC Manual of Organization and Procedure is the manual that governs the JEDEC standardization process. *See* CCFF 404. Finally, the JEDEC Manual of Organization and Procedure is an EIA publication. (J. Kelly, Tr. 1914; CX0208 at 1 (The cover of the Manual contains the following legend: "Electronic Industries Association. Engineering Department.")).

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there

for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

166. EIA General Counsel John Kelly testified that JEP 21-I needed a "final stamp of approval" from EDEC. (Kelly, Tr. 2105).

Response to Finding No. 166: This proposed finding incomplete, misleading, and does not support the conclusion that the 21-I Manual was not effective because the procedure for revising the 21-H manual is described within the manual itself. *See* CX0205 at 15 ("revisions . . . shall be submitted to the Council through the Council Secretary. . . Such revisions shall be considered at two regular meetings of the Council with a favorable vote at both meeting for final approval. If approved by the Council, approval by the EIA Legal Department is also required. The revisions shall then be incorporated into the Manual.") (emphasis added). The steps for revising the 21-H manual were followed. *See* CX0054 at 7 (Initial JEDEC Council approval of 21-I manual); CX0055 at 2 (Second approval of 21-I manual be JEDEC Council); G. Kelley, Tr. 2423-28 (discussing first and second approvals of 21-I manual by JEDEC Council). Further, witnesses testified that the JEDEC Manual of Organization and Procedure is the manual that governs the JEDEC standardization process. *See* CCFF 404. Finally, the JEDEC Manual of Organization and Procedure is an EIA publication. (J. Kelly, Tr. 1914; CX0208 at 1 (The cover of the Manual contains the following legend: "Electronic Industries Association. Engineering Department.")).

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

167. Mr. Kelly testified that he did not know one way or the other if JEP 21-I had ever received EDEC's approval. (Kelly, Tr. 2105).

Response to Finding No. 167: This proposed finding incomplete, misleading, and does not support the conclusion that the 21-I Manual was not effective because the procedure for revising the 21-H manual is described within the manual itself. *See* CX0205 at 15 ("revisions . . . shall be submitted to the Council through the Council Secretary. . . Such revisions shall be considered at two regular meetings of the Council with a favorable vote at both meeting for final approval. If approved by the Council, approval by the EIA Legal Department is also required. The revisions shall then be incorporated into the Manual.") (emphasis added). The steps for revising the 21-H manual were followed. *See* CX0054 at 7 (Initial JEDEC Council approval of 21-I manual); CX0055 at 2 (Second approval of 21-I manual be JEDEC Council); G. Kelley, Tr. 2423-28 (discussing first and second approvals of 21-I manual by JEDEC Council). Further, witnesses testified that the JEDEC Manual of Organization and Procedure is the manual that governs the JEDEC standardization process. *See* CCFF 404. Finally, the JEDEC Manual of

Organization and Procedure is an EIA publication. (J. Kelly, Tr. 1914; CX0208 at 1 (The cover of the Manual contains the following legend: "Electronic Industries Association. Engineering Department.")).

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

168. Mr. Kelly testified that he had not intended, in responding to questions posed by Complaint Counsel, to testify that JEP 21-I had been formally approved by EDEC. (Kelly, Tr. 2105).

Response to Finding No. 168: This proposed finding is incomplete, misleading, and does not support the conclusion that the 21-I Manual was not effective because the procedure for revising the 21-H manual is described within the manual itself. *See* CX0205 at 15 ("revisions . . . shall be submitted to the Council through the Council Secretary. . . Such revisions shall be considered at two regular meetings of the Council with a favorable vote at both meeting for final approval. If approved by the Council, approval by the EIA Legal Department is also required. The revisions shall then be incorporated into the Manual.") (emphasis added). The steps for revising the 21-H manual were followed. *See* CX0054 at 7 (Initial JEDEC Council approval of 21-I manual); CX0055 at 2 (Second approval of 21-I manual be JEDEC Council); G. Kelley, Tr.

2423-28 (discussing first and second approvals of 21-I manual by JEDEC Council). Further, witnesses testified that the JEDEC Manual of Organization and Procedure is the manual that governs the JEDEC standardization process. *See* CCFF 404. Finally, the JEDEC Manual of Organization and Procedure is an EIA publication. (J. Kelly, Tr. 1914; CX0208 at 1 (The cover of the Manual contains the following legend: "Electronic Industries Association. Engineering Department.")).

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

169. No witness testified at trial that EDEC approval of the JEP 21-I manual was ever obtained.

Response to Finding No. 169: This proposed finding is incomplete, misleading, and does not support the conclusion that the 21-I Manual was not effective because the procedure for revising the 21-H manual is described within the manual itself. *See* CX0205 at 15 ("revisions . . . shall be submitted to the Council through the Council Secretary. . . Such revisions shall be considered at two regular meetings of the Council with a favorable vote at both meeting for final approval. If approved by the Council, approval by the EIA Legal Department is also required.

The revisions shall then be incorporated into the Manual.") (emphasis added). The steps for revising the 21-H manual were followed. *See* CX0054 at 7 (Initial JEDEC Council approval of 21-I manual); CX0055 at 2 (Second approval of 21-I manual be JEDEC Council); G. Kelley, Tr. 2423-28 (discussing first and second approvals of 21-I manual by JEDEC Council). Further, witnesses testified that the JEDEC Manual of Organization and Procedure is the manual that governs the JEDEC standardization process. *See* CCFF 404. Finally, the JEDEC Manual of Organization and Procedure is an EIA publication. (J. Kelly, Tr. 1914; CX0208 at 1 (The cover of the Manual contains the following legend: "Electronic Industries Association. Engineering Department.")).

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

170. Complaint Counsel did not meet their burden to show that the JEP 21-I manual ever became effective.

Response to Finding No. 170: This proposed finding does not contain any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge*

and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Furthermore, RPF 121 is contrary to the weight of the evidence. *See* CCFF 403-18.

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

171. The JEP 21-I manual states that committee chairpersons would satisfy the requirement that they call attention to a member's obligations under 21-I by showing, at committee meetings, "viewgraphs" that were contained in Appendix E of JEP 21-I. (CX 208 at 19).

Response to Finding No. 171: This proposed finding is incomplete because showing the viewgraphs is one method in which a committee chairman *may* satisfy the chairman's obligations. (CX0208 at 26). Committee chairmen also satisfied their obligations by informing participants of their obligations under the patent policy through presentations at JEDEC meetings, Mr. Townsend's memoranda, the New Member Orientation, sign-in sheets, discussions of patent-related issues in JEDEC meting minutes, JEDEC ballots, and JEDEC manuals. *See* CCFF 357-418.

172. The viewgraphs in Appendix E to the JEP 21-I manual contain no reference to the disclosure of intellectual property interests. (CX 208 at 19).

Response to Finding No. 172: This proposed finding is inaccurate because the relevant viewgraphs are not located at CX0208 at 19, but instead are located at CX0208 at 26-28. Further, the viewgraphs in Appendix E specifically reference pending patents. (CX0208 at 27). In addition, Appendix F also specifically references pending patents. (CX0208 at 29).

173. At the September 1993 42.3 meeting, the committee chairman showed a viewgraph containing proposed language from an appendix to the not-yet-published JEP 21-I manual. This viewgraph was expressly marked "DRAFT" and contained a footnote stating that the "material is a proposed revision" that "has not been approved by JEDEC." (JX 17 at 12). In any event, this "draft" viewgraph does not contain language requiring intellectual property disclosures by JEDEC members. (*Id.*).

Response to Finding No. 173: This proposed finding is incomplete because it fails to disclose that Richard Crisp was in attendance at the September 1993 JC-42.3 meeting. (JX0017 at 1). RPF 173 is also incomplete because it fails to disclose that the committee chairman also showed a draft of the 21-I Manual at the December 1992 JEDEC JC-42.3 meeting, and that richard Crisp and David Mooring of Rambus both attended that meeting. (CCFF 940-44). RPF 173 is inaccurate because the language in the viewgraph shown at the December 1992 and September 1993 meetings (which is identical to the language approved for and published in the 21-I manual) does contain a disclosure requirement and specifically discusses pending patents. (JX0017 at 12). Further, RPF 173 does not support the conclusion that 21-I was not an official statement of the JEDEC patent policy because witnesses testified that the JEDEC Manual of Organization and Procedure is the manual that governs the JEDEC standardization process. *See* CCFF 404. In addition, the 21-I manual was approved twice by the JEDEC Council and approved by EIA General Counsel. *See* (CX0054 at 7; CX0055 at 2; G. Kelley, Tr. 2423-28; J. Kelly, Tr. 1924-25).

174. The JEP 21-I manual also includes an "Appendix F" that is entitled "Patent Policy Application Guidelines." These guidelines state that the discussion of "pending or existing patents" is "a permissible activity." (CX 208 at 29).

Response to Finding No. 174: Complaint Counsel does not disagree. However, this proposed finding is misleading because, as John Kelly and many other witnesses testified, JEDEC participants may consider the inclusion of patented or patentable material in JEDEC standards provided that the proper disclosures are made and that the owner of the intellectual property provides a written assurance that it will license the intellectual property for free or on reasonable and non-discriminatory terms. *See* CCFF 318-20, 331, 347, 349, 353. Thus, there is no inconsistency between the disclosure obligation and the freedom of participants to discuss the impact of those patent applications once properly disclosed.

175. JEP 21-I also states, in Appendix D, that JEDEC standards "are adopted without regard to whether or not their adoption may involve patents [on] articles, materials, or processes." (CX 208 at 25).

Response to Finding No. 175: Complaint Counsel does not disagree. However, this proposed finding does not support the conclusion that the 21-I manual was not an official statement of the JEDEC patent policy. The proposed finding also is misleading to the extent it suggest that JEDEC had no view on whether patented material was included in JEDEC standards. Mr. Kelly testified that EIA would prefer not to include patented technologies in EIA standards, but that such technologies could be included in EIA standards provided that disclosure had been made early in the process and the written licensing assurances had been provided. (J. Kelly, Tr. 1839-40). The quoted language "is in essence a disclaimer saying the EIA does not conduct patent searches, and therefore, can't assume any liability is patents somehow creep into standards unbeknownst to us." (J. Kelly, Tr. 1835). Further, John Kelly and many other witnesses testified that JEDEC participants may consider the inclusion of patented or patentable material in JEDEC standards provided that the proper disclosures are made and that the owner of the intellectual property provides a written assurance that it will license the intellectual property for free or on reasonable and non-discriminatory terms. *See* CCFF 318-20, 331, 347, 349, 353.

7. The JC 42 Members' Manual Refers To A Disclosure Obligation On The Part Of Presenters.

176. Another manual that was published while Rambus was a JEDEC member was the "JC 42 Members' Manual," which bears a publication date of September 1994. (RX 507 at 1).

Response to Finding No. 176: This proposed finding is misleading in its use of the term "published." There is no evidence from any source whatsoever that JEDEC or EIA published Mr. Townsend's Members' Manual. As is indicated from the cover of the document, the Members' Manual was a document that was put together by Jim Townsend, not JEDEC or EIA. (RX0507 at 1). Unlike the JEDEC Manual of Organization and Procedure, Mr. Townsend's Members' Manual does not display the JEDEC or EIA trademarks or otherwise purport to be an official EIA publication. Unlike the JEDEC Manual of Organization and Procedure, there is no evidence that Mr. Townsend's Members' Manual was approved by the JEDEC Council (*see* CX0054 at 7; CX0055 at 2; G. Kelley, Tr. 2423-28) or considered by participants to be an official articulation of the rules of JEDEC. In fact, the uncontradicted evidence shows that Mr. Townsend's Members' manual was not an official document and that JEDEC participants were well aware of this fact. *See* JX0031 at 4 ("Members Manual. A copy of some Committee procedures was circulated by Mr. Townsend. Some of this material is not approved by JEDEC . . . It should be clear that this manual is not a publication of JEDEC because it has not been balloted by Committee or Council"). *Cf.* CCFF 404.

177. The introduction to the JC 42 Members' Manual is signed by Jim Townsend, Chair of the JC 42 Executive Committee, and states in part that "[t]his manual was compiled to assist new (and established) members in achieving full effectiveness in the standards-making process." (RX 507 at 2).

Response to Finding No. 177: Complaint Counsel does not disagree. However, this proposed finding does not support the conclusion that Mr. Townsend's Members' Manual was a publication of JEDEC or EIA or that Mr. Townsend's Members' Manual contained a complete

statement of the JEDEC patent policy. As is indicated from the cover of the document, the Members' Manual was a document that was put together by Jim Townsend, not JEDEC or EIA. (RX0507 at 1). Unlike the JEDEC Manual of Organization and Procedure, Mr. Townsend's Members' Manual does not display the JEDEC or EIA trademarks or otherwise purport to be an official EIA publication. Unlike the JEDEC Manual of Organization and Procedure, there is no evidence that Mr. Townsend's Members' Manual was approved by the JEDEC Council (*see* CX0054 at 7; CX0055 at 2; G. Kelley, Tr. 2423-28) or considered by participants to be an official articulation of the rules of JEDEC. In fact, the uncontradicted evidence shows that Mr. Townsend's Members' manual was not an official document and that JEDEC participants were well aware of this fact. *See* JX0031 at 4 ("Members Manual. A copy of some Committee procedures was circulated by Mr. Townsend. Some of this material is not approved by JEDEC . . . It should be clear that this manual is not a publication of JEDEC because it has not been balloted by Committee or Council"). *Cf.* CCFF 404.

178. The JC 42 Members' Manual contains no reference to JEP 21-I. (RX 507). Instead, the JC 42 Members' Manual refers to EP-7-A and EP-3-F in reference to the "patent policy." (RX 507 at 15).

Response to Finding No. 178: This proposed finding does not support the conclusion that Mr. Townsend's Members' Manual was a publication of JEDEC or EIA or that Mr. Townsend's Members' Manual contained a complete statement of the JEDEC patent policy. As is indicated from the cover of the document, the Members' Manual was a document that was put together by Jim Townsend, not JEDEC or EIA. (RX0507 at 1). Unlike the JEDEC Manual of Organization and Procedure, there is no evidence that Mr. Townsend's Members' Manual was approved by the JEDEC Council (*see* CX0054 at 7; CX0055 at 2; G. Kelley, Tr. 2423-28) or considered by participants to be an official articulation of the rules of JEDEC. In fact, the uncontradicted evidence shows that Mr. Townsend's Members' manual was not an official

document and that JEDEC participants were well aware of this fact. *See* JX0031 at 4 ("Members Manual. A copy of some Committee procedures was circulated by Mr. Townsend. Some of this material is not approved by JEDEC . . . It should be clear that this manual is not a publication of JEDEC because it has not been balloted by Committee or Council"). *Cf.* CCFF 404.

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

179. No witness testified at trial that the JC 42 Members' Manual had received EDEC approval.

Response to Finding No. 179: Complaint Counsel does not disagree. In addition, no witness testified that Mr. Townsend's Members' Manual was reviewed or approved by the JEDEC Council or EIA Legal Counsel or the the Members' Manual was considered by JEDEC participants to be an official JEDEC manual. *See also* JX0031 at 4 ("Members Manual. A copy of some Committee procedures was circulated by Mr. Townsend. Some of this material is not approved by JEDEC . . . It should be clear that this manual is not a publication of JEDEC because it has not been balloted by Committee or Council").

In any event, this finding is irrelevant, since the Rambus JEDEC representative admitted that he understood that the 21-I Manual set forth the JEDEC patent disclosure requirement. (*See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right.")).

180. According to the version of the JC 42 Members' Manual that was published in 1994, a member that was *presenting* a technology to JEDEC for standardization "must reveal any known or expected patents, *within his company*, on the material presented." (RX 507 at 15) (emphasis in original).

Response to Finding No. 180: This proposed finding does not support the conclusion that Mr. Townsend's Members Manual was "published" by JEDEC or that presenters were the only participants with an obligation to disclose patent applications. As indicated above, Mr. Townsend's Members' Manual was not a publication of JEDEC or EIA and did not state the JEDEC patent policy. *See* CCRF 176-78. In addition, such a conclusion is contrary to the weight of the evidence because official JEDEC and EIA publications make no distinction between presenters and other participants. *See* CCFF 330. In addition, the overwhelming weight of the evidence demonstrates that all participants were obligated to disclose patents and patent applications and there was no difference for presenters. *See* CCFF 320, 324, 330.

181. There is no evidence, and Complaint Counsel do not allege, that Rambus ever proposed or advocated the adoption of any standard or technology while a JEDEC member. In fact, Rambus made no presentations at all, and it voted at only one meeting, when it voted *against* four proposals. (Calvin, Tr. 1071; Crisp., Tr. 3083-4; JX 13 at 9-11; Wiggers, Tr. 10590). There

was also testimony by Gordon Kelley, 42.3 committee chair, that he had twice *barred* Rambus from presenting its technology for standardization at JEDEC. (Kelley, Tr. 2649-58). Kelley also testified that he had never barred any other company from making a presentation (*id.*), and that he was only empowered to do so with respect to Rambus by virtue of a completely undocumented "hand vote" at the May 1991 JC 42.3 meeting. (*Id.*).

Response to Finding No. 181: This proposed finding does not support the conclusion that only presenters were required to disclose pending patent applications. Such a conclusion is contrary to the weight of the evidence because official JEDEC and EIA publications make no distinction between presenters and other participants. *See* CCFF 330. In addition, the overwhelming weight of the evidence demonstrates that all participants were obligated to disclose patents and patent applications and there was no difference for presenters. *See* CCFF 320, 324, 330. RPF 181 *does,* however, support the conclusion that JEDEC members were unwilling to even consider including in a standard Rambus patented or proprietary technology without at least an assurance that Rambus would license on RAND terms.

8. JEDEC's Ballots Encouraged, But Did Not Require, Disclosure By Members Of Relevant Patents.

182. The ballots used by JEDEC to record votes on standardization proposals during the time that Rambus attended JEDEC meetings contained the phrase "If anyone receiving this ballot is aware of patents involving this ballot, please alert the committee accordingly during your voting response." (CX 252A at 2).

Response to Finding No. 182: Complaint Counsel does not disagree. However, this proposed finding does not support the conclusion that disclosure of intellectual property at the ballot stage was purely voluntary. The evidence demonstrates that the disclosure requirement was mandatory for companies that chose to participate in JEDEC. (CCFF 323-24, 330). As the Federal Circuit held, JEDEC rules imposed a disclosure duty on all participants. *See Rambus, Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1098 (Fed. Cir. 2003).

183. When the ballot language regarding patents was first added to JEDEC ballots, a JEDEC member asked during a JEDEC meeting about the purpose of the new language. The minutes of the JC 42.1 meeting held on September 13, 1989 state that:

> "Council discussed patent issue at their June meeting at the request of JC-42.3. The result was not to change EIA legal requirements as outlined in document EP-7, but to add some wording on JEDEC ballot voting sheets about informing the Committee if any patent covers the balloted material.
>
> TI was concerned that Committee members could be held liable if they didn't inform Committee members correctly on patent matters. Committee responded that the question was added on ballot voting sheets for information only and was not going to be checked to see who said what."

(CX 3 at 6).

Response to Finding No. 183: This proposed finding is misleading and does not support the conclusion that the disclosure of intellectual property at the time of a ballot was purely voluntary. The evidence demonstrates that the disclosure requirement was mandatory for companies that chose to participate in JEDEC. (CCFF 323-24, 330). As the Federal Circuit held, JEDEC rules imposed a disclosure duty on all participants. *See Rambus, Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1098 (Fed. Cir. 2003). In addition, this proposed finding is misleading because the language cited by Respondent relates to the purported concern of the Texas Instruments representative with being "held liable" by JEDEC for failure to disclose. As the minutes indicate, Texas Instruments's concern with legal liability to JEDEC was misplaced. JEDEC is a voluntary organization (CCFF 323) and JEDEC, therefore, is unable to impose sanctions on members for failure to comply with any part of the patent policy. (CCFF 419-20). JEDEC merely was concerned with getting the "information" relating to intellectual property.

184. The statements in the official JEDEC meeting minutes that the patent-related question on the ballot was added "for information only" and that the ballots were "not going to be checked to see who said what" are inconsistent with the proposition that the ballot language was intended to, or did, express any mandatory disclosure obligation. (CX 3 at 6).

Response to Finding No. 184: This proposed finding does not support the conclusion that disclosure of intellectual property at the ballot stage was purely voluntary. The

evidence demonstrates that disclosure is the obligation of all participants (*see* CCFF 324, 330) irrespective of "who said what." Provided that good faith disclosure is made, the identity of the participant making the disclosure is of little relevance. The disclosure rules are designed to get JEDEC the "information" it needs to make an informed decision. Thus, disclosure "for information only" is consistent with JEDEC's need for disclosure of relevant patent information, regardless of the identity of the participant disclosing. Further, the conclusion that disclosure of intellectual property at the ballot stage was purely voluntary is contrary to the weight of the evidence. *See* CCFF 383-86. *See also* Rhoden, Tr. 582.

185. Desi Rhoden, the current JEDEC Chairman and President of AMI2, testified that he understood the phrase "please alert the committee" on the ballot form to mean that a member "must" alert the Committee. (Rhoden, Tr. 582). Mr. Rhoden's testimony on this issue is not credible in light of the express statement in the JEDEC meeting minutes that the language had been added to the ballots for "information only and was not going to be checked to see who said what" and in light of the fact that the ballot form uses the term "Mandatory" to refer to *other* information sought by the ballot (CX 252a at 2), but does not use that term or any similar term with respect to patent-related information.

Response to Finding No. 185: This proposed finding does not support the conclusion that disclosure of intellectual property at the ballot stage was purely voluntary. Mr. Rhoden clearly explained the reason for including the term "MANDATORY" after the space reserved for members voting "no" on a proposal. (Rhoden, Tr. 583 ("the term "MANDATORY" is intended to imply that when you vote no, it is required that you provide -- that you provide a comment.")). JEDEC does not require all members to vote on all proposals. (J. Kelly, Tr. 1807). Because, however, JEDEC is a consensus-based organization, participants who choose to vote and vote "no" must provide comments so that the committee can work in good faith to resolve the comments. (J. Kelly, Tr. 1784-85). Indeed, members often vote "no" and comment that their "no" vote was based on patent concerns. *See* JX0028 at 45 (In response to the survey ballot, Hyundai commented that it was "wondering DLL may be MOSAID patent."); CX0711 at 44 (Richard Crisp

noting that Micron cited patents as reason for its "No" vote). Thus, comments to "no" votes were mandatory, whether the "no" vote was based on a technical reason or a patent concern.

The evidence demonstrates that the disclosure requirement was mandatory for companies that chose to participate in JEDEC. (CCFF 323-24, 330). Provided that good faith disclosure is made, the identity of the participant making the disclosure is of little relevance. The disclosure rules are designed to get JEDEC the "information" it needs to make an informed decision. Thus, disclosure "for information only" is consistent with JEDEC's need for disclosure of relevant patent information, regardless of the identity of the participant disclosing. Further, the conclusion that disclosure of intellectual property at the ballot stage was not mandatory is contrary to the weight of the evidence. *See* CCFF 383-86. *See also* Rhoden, Tr. 582.

D. There Is Substantial Evidence That JEDEC Members And The JEDEC Leadership Understood During The Time That Rambus Was A JEDEC Member That Members Were *Encouraged*, But Not *Required*, To Make A Disclosure Of Their Intellectual Property In Certain Circumstances.

186. EIA officials stated in writing in January 1996 that the EIA "encourage[d]" the "voluntary" disclosure of patents relating to standardization efforts. (RX 669 at 2).

Response to Finding No. 186: This proposed finding, which addresses the same issue as RPF 143-150, is misleading because it fundamentally misapprehends the meaning on the term "voluntary" as it relates to JEDEC. JEDEC is a voluntary organization (CCFF 323) and JEDEC is unable to impose sanctions on members for failure to comply with any part of the patent policy. (CCFF 419-20). JEDEC, therefore, necessarily depends upon the good faith, voluntary cooperation of participants in complying with the requirements of the patent policy. (CCFF 314). The requirements of the patent policy, however, are mandatory for all companies that choose to be members. (CCFF 324).

187. In addition, on March 29, 1994, JEDEC Secretary Ken McGhee sent a memorandum to JC 42 Chairman Jim Townsend that stated that JEDEC's "legal counsel" had said that "he

didn't think it was a good idea to require people at JEDEC standards meetings to sign a document assuring anything about their company's patent rights. . . ." (RX 486 at 1).

Response to Finding No. 187: This proposed finding is misleading and does not support the conclusion that the *disclosure* of intellectual property was not mandatory. As is clear from the face of the document, Mr. McGhee's memo is concerned with a mandatory *licensing assurance* such as the policy adopted by ETSI. (RX0486 at 1). ETSI is the European Telecommunications Standards Institute. As indicated in the EIA/TIA letter to the Federal Trade Commission commenting on the *Dell* consent order, ETSI adopted a policy "to force compulsory licensing." (RX0669 at 3) (emphasis added). EIA legal counsel, John Kelly, concluded that requiring participants to "sign a document assuring anything about their company's patent rights" as is done in ETSI was not a good idea. (RX0486 at 1) (emphasis added). Both ANSI and TIA agreed with Mr. Kelly and "joined the U.S. Government in opposing . . . force[d] compulsory licensing." (RX0669 at 3).

188. Secretary McGhee's March 29, 1994 memorandum to Mr. Townsend states that legal counsel had given the "following reasons" why he did not believe that it would be a good idea to require JEDEC representatives to sign an assurance regarding their company's patent rights:

> "(1) It would have a chilling effect at future meetings.
> (2) A general assurance wouldn't be worth that much anyway.
> (3) It needs to come from a VP or higher within the company – engineers can't sign such documents.
> (4) It would need to be done at each meeting slowing down the business at hand."

(RX 486 at 1).

Response to Finding No. 188: This proposed is misleading and does not support the conclusion that the *disclosure* of intellectual property was not mandatory. As is clear from the face of the document, Mr. McGhee's memo is concerned with a mandatory *licensing assurance* such as the policy adopted by ETSI. (RX0486 at 1). ETSI is the European Telecommunications Standards Institute. As indicated in the EIA/TIA letter to the Federal Trade Commission

commenting on the *Dell* consent order, ETSI adopted a policy "to force compulsory licensing." (RX0669 at 3) (emphasis added). EIA legal counsel, John Kelly, concluded that requiring participants to "sign a document assuring anything about their company's patent rights" as is done in ETSI was not a good idea. (RX0486 at 1) (emphasis added). Both ANSI and TIA agreed with Mr. Kelly and "joined the U.S. Government in opposing . . . force[d] compulsory licensing." (RX0669 at 3).

189. The statement in Secretary McGhee's March 29, 1994 memorandum that requiring a written assurance about a company's patent rights "would have a chilling effect" is inconsistent with the proposition that as of March 1994, a member's mere presence or silence at JEDEC meetings was understood by JEDEC members to constitute such an assurance.

Response to Finding No. 189: This proposed finding is misleading and does not support the conclusion that the *disclosure* of intellectual property was not mandatory. As is clear from the face of the document, Mr. McGhee's memo is concerned with a mandatory *licensing assurance* such as the policy adopted by ETSI. (RX0486 at 1). ETSI is the European Telecommunications Standards Institute. As indicated in the EIA/TIA letter to the Federal Trade Commission commenting on the *Dell* consent order, ETSI adopted a policy "to force compulsory licensing." (RX0669 at 3) (emphasis added). EIA legal counsel, John Kelly, concluded that requiring participants to "sign a document assuring anything about their company's patent rights" as is done in ETSI was not a good idea. (RX0486 at 1) (emphasis added). Both ANSI and TIA agreed with Mr. Kelly and "joined the U.S. Government in opposing . . . force[d] compulsory licensing." (RX0669 at 3). Finally, Complaint Counsel has made no allegation that a members's mere presence or silence at a JEDEC meeting constitutes any licensing assurance. *See* CCFF 347-56. Indeed, JEDEC policy requires that licensing assurances be provided in writing from a person with authority to bind the company. CCFF 349-53. It is, however, a violation of JEDEC policy for a JEDEC participant to remain silent when that participant is under an obligation to disclose

patent related information. *See* CX2957 at 2 (Declaration of Joel Karp) ("contrary to industry practice and understanding for an intellectual property owner to remain silent during the standard-setting process – and then after a standard has been adopted and implemented – later attempt to assert that its intellectual property covers the standard")).

190. The statements in Secretary McGhee's March 29, 1994 memorandum that an assurance would need to be obtained "from a VP or higher within the company" and that "engineers can't sign such documents" are inconsistent with the proposition that the engineers present at JEDEC meetings were obligated to make disclosures on behalf of their companies.

Response to Finding No. 190: This proposed finding is misleading and does not support the conclusion that the *disclosure* of intellectual property was not mandatory. As is clear from the face of the document, Mr. McGhee's memo is concerned with a mandatory *licensing assurance* such as the policy adopted by ETSI. (RX0486 at 1). ETSI is the European Telecommunications Standards Institute. As indicated in the EIA/TIA letter to the Federal Trade Commission commenting on the *Dell* consent order, ETSI adopted a policy "to force compulsory licensing." (RX0669 at 3) (emphasis added). EIA legal counsel, John Kelly, concluded that requiring participants to "sign a document assuring anything about their company's patent rights" as is done in ETSI was not a good idea. (RX0486 at 1) (emphasis added). Both ANSI and TIA agreed with Mr. Kelly and "joined the U.S. Government in opposing . . . force[d] compulsory licensing." (RX0669 at 3). Further, the conclusion that JEDEC did not require engineers participating in JEDEC to make disclosures is contrary to the weight of the evidence because official JEDEC and EIA publications impose an obligation on all participants. *See* CCFF 319. In addition, the overwhelming weight of the evidence demonstrates that all participants were obligated to disclose patents and patent applications. *See* CCFF 318-20, 324, 330.

191. In a similar e-mail sent in February 2000, JEDEC Secretary Ken McGhee informed JEDEC 42.4 members that "[t]he JEDEC patent policy concerns items that are known to be patented that are included in JEDEC Standards. *Disclosure of patents is a very big issue for*

Committee members and cannot be required of members at meetings." (RX 1582 at 1) (emphasis added).

Response to Finding No. 191: This proposed finding is misleading and does not support the conclusion that the JEDEC patent policy did not require the disclosure of patent applications. As an initial matter, the cited exhibit was the result of an error by Mr. McGhee concerning Micron's disclosure of a patent application.

On January 28, 2000, Micron drafted a written disclosure of a patent application relating to a proposed standard under consideration in the JC-42.4 subcommittee. (RX1559 at 2). On February 1, 2000, Mr. McGhee sent an email to members of the subcommittee stating "I would like to point out that this letter is well intentioned, but lacks a patent number, so it does not complete the requirements for JEDEC patent policy. If, however, a follow-up letter is issued after the patent is issued, then it would comply with JEDEC's patent policy." (RX1559 at 1). Upon receiving Mr. McGhee's email that Micron had not complied with the patent policy because Micron's disclosure did not include an application number, Mr. Walther of Micron caused the matter to be placed on the agenda for the next JEDEC board meeting. (RX1568 at 25). Logically, because patent applications do not have patent numbers, the lack of a patent number cannot be the basis for holding a member in violation of the disclosure policy.

Mr. McGhee's subsequent email (RX1582) was written for the purpose of attempting to clarify to the committee that his earlier email stating that Micron had not complied with the patent policy because it lacked a patent number was in error. In that email, Mr. McGhee noted that Micron's written disclosure, which came after its oral disclosure at a JEDEC meeting, was "one step beyond" the patent policy. As Mr. Kelly testified, a company can "fully comply with its disclosure obligation by providing an oral explanation to the relevant EIA or JEDEC committee", and that if a company "orally discloses a patent or patent application" and follows up "by sending

a letter making disclosures in writing" it would "be going beyond" what JEDEC's rules actually require. (J. Kelly, Tr. 2004-05).

192. IBM informed JEDEC members and JEDEC leaders on several occasions between 1992 and 1996 that it would not disclose its intellectual property position at JEDEC meetings. (JX 15 at 6; RX 420 at 1; JX 18 at 8; JX 19 at 4).

Response to Finding No. 192: This proposed finding is inaccurate, misleading, contrary to the weight of the evidence, and ignores substantial evidence in the record because IBM representatives stated that they would disclose pending or issued patents of which IBM's representatives were aware. *See* CCFF 325-29. As explained by Mr. Kelley and Mr. Kellogg, IBM could not commit to providing a list of all its relevant patents because such a search of the company's patent portfolio would be difficult and, even if undertaken, could not be guaranteed to find all relevant patents. IBM did, however, agree to evaluate any purported patent or patent application that other participants could identify. *See* CCFF 327-28. The testimony of Mr. Kelley and Mr. Kellogg is consistent with contemporaneous IBM business documents. *See, e.g.*, (RX0578 at 2 ("I do not suggest that IBM list applicable patent numbers. Such a list could be construed as complete when it is not. *I plan to alert the committee when I know of applicable patent(s) but not list the patent numbers*."); G. Kelley, Tr. 2455-58). This is in direct contrast to the conduct of Rambus, which intentionally concealed applicable patents and patent applications. CCFF 813-16, 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111, 1238-59, 1676-1700.

In addition, RPF 192 does not support the conclusion that JEDEC "leaders" understood the patent disclosure policy to be anything other than mandatory. Such a conclusion is contrary to the overwhelming weight of contemporaneous evidence (including the 21-I Manual, the Townsend presentations, the Townsend memoranda, and the sign-in sheets) and witness testimony (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer,

and Kelley) that confirms that JEDEC intended the disclosure obligation to be mandatory. *See* CCFF 318-19, 324, 330, 360, 363, 367, 370, 378.

193. The minutes of the March 1993 meeting of JEDEC 42.3 state in part that "IBM noted that their view has been to ignore [the] patent disclosure rule because their attorneys have advised them that if they do then a listing may be construed as complete." (JX 15 at 6).

Response to Finding No. 193: This proposed finding is inaccurate, misleading, contrary to the weight of the evidence, and ignores substantial evidence in the record because IBM representatives stated that they would disclose pending or issued patents of which IBM's representatives were aware. *See* CCFF 325-29. As explained by Mr. Kelley and Mr. Kellogg, IBM could not commit to providing a list of all its relevant patents because such a search of the company's patent portfolio would be difficult and, even if undertaken, could not be guaranteed to find all relevant patents. IBM did, however, agree to evaluate any purported patent or patent application that other participants could identify. *See* CCFF 327-28. The testimony of Mr. Kelley and Mr. Kellogg is consistent with contemporaneous IBM business documents. *See, e.g.*, (RX0578 at 2 ("I do not suggest that IBM list applicable patent numbers. Such a list could be construed as complete when it is not. *I plan to alert the committee when I know of applicable patent(s) but not list the patent numbers*."); G. Kelley, Tr. 2455-58). Indeed, IBM disclosed known relevant patents and patent applications to JEDEC, yet consistent with its lawyers' advice specifically offered the disclaimer that it could not provide a complete list of all relevant patents. CCFF 325-29, 872, 2433. Rambus ignored its lawyers' warnings regarding equitable estoppel and intentionally concealed relevant patents and patent applications, while creating the impression (through its disclosure of the '703 patent and its withdrawal letter) that it was disclosing all relevant intellectual property. *See* CCFF 813-16, 821, 850-52, 859-66, 1066, 1109-14.

In addition, RPF 192 does not support the conclusion that JEDEC "leaders" understood the patent disclosure policy to be anything other than mandatory. Such a conclusion is contrary to the

overwhelming weight of contemporaneous evidence (including the 21-I Manual, the Townsend presentations, the Townsend memoranda, and the sign-in sheets) and witness testimony (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer, and Kelley) that confirms that JEDEC intended the disclosure obligation to be mandatory. *See* CCFF 318-19, 324, 330, 360, 363, 367, 370, 378.

194. In an August 1993 memo to JEDEC leaders entitled "BGA Patent/License Rights," IBM JEDEC representative (and JEDEC 42.3 subcommittee chair) Gordon Kelley stated that:

> "IBM Intellectual Property Law attorneys have informed me that we will not use JEDEC as a forum for discussing this subject. It is the responsibility of the producer to evaluate the subject and to work out the proper use of rights. So, I can not confirm or deny any IPL rights."

(RX 420 at 1).

Response to Finding No. 194: This proposed finding is inaccurate, misleading, contrary to the weight of the evidence, and ignores substantial evidence in the record because IBM representatives stated that they would disclose pending or issued patents of which IBM's representatives were aware. *See* CCFF 325-29. As explained by Mr. Kelley and Mr. Kellogg, IBM could not commit to providing a list of all its relevant patents because such a search of the company's patent portfolio would be difficult and, even if undertaken, could not be guaranteed to find all relevant patents. IBM did, however, agree to evaluate any purported patent or patent application that other participants could identify. *See* CCFF 327-28. The testimony of Mr. Kelley and Mr. Kellogg is consistent with contemporaneous IBM business documents. *See, e.g.*, (RX0578 at 2 ("I do not suggest that IBM list applicable patent numbers. Such a list could be construed as complete when it is not. *I plan to alert the committee when I know of applicable patent(s) but not list the patent numbers*."); G. Kelley, Tr. 2455-58). This is in direct contrast to the conduct of Rambus, which intentionally concealed applicable patents and patent applications.

CCFF 813-16, 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111, 1238-59, 1676-1700.

Indeed, IBM disclosed known relevant patents and patent applications to JEDEC, yet consistent with its lawyers' advice specifically offered the disclaimer that it could not provide a complete list of all relevant patents. CCFF 325-29, 872, 2433. Rambus ignored its lawyers' warnings regarding equitable estoppel and intentionally concealed relevant patents and patent applications, while creating the impression (through its disclosure of the '703 patent and its withdrawal letter) that it was disclosing all relevant intellectual property. *See* CCFF 813-16, 821, 850-52, 859-66, 1066, 1109-14.

In addition, RPF 192 does not support the conclusion that JEDEC "leaders" understood the patent disclosure policy to be anything other than mandatory. Such a conclusion is contrary to the overwhelming weight of contemporaneous evidence (including the 21-I Manual, the Townsend presentations, the Townsend memoranda, and the sign-in sheets) and witness testimony (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer, and Kelley) that confirms that JEDEC intended the disclosure obligation to be mandatory. *See* CCFF 318-19, 324, 330, 360, 363, 367, 370, 378.

195. The December 1993 JEDEC 42.3 minutes state in part that "[a]s a side issue, IBM noted that in the future they will not come to the committee with a list of applicable patents on standards proposals. It is up to the user of the standard to discover which patents apply." (JX 18 at 8).

Response to Finding No. 195: This proposed finding is inaccurate, misleading, contrary to the weight of the evidence, and ignores substantial evidence in the record because IBM representatives stated that they would disclose pending or issued patents of which IBM's representatives were aware. *See* CCFF 325-29. As explained by Mr. Kelley and Mr. Kellogg, IBM could not commit to providing a list of all its relevant patents because such a search of the

company's patent portfolio would be difficult and, even if undertaken, could not be guaranteed to find all relevant patents. IBM did, however, agree to evaluate any purported patent or patent application that other participants could identify. *See* CCFF 327-28. The testimony of Mr. Kelley and Mr. Kellogg is consistent with contemporaneous IBM business documents. *See, e.g.*, (RX0578 at 2 ("I do not suggest that IBM list applicable patent numbers. Such a list could be construed as complete when it is not. *I plan to alert the committee when I know of applicable patent(s) but not list the patent numbers*."); G. Kelley, Tr. 2455-58). Indeed, IBM did continue to inform JEDEC of patent-related issues. *See, e.g.*, JX0039 at 14 ("IBM: . . . We are not aware of any patent issues"). This is in direct contrast to the conduct of Rambus, which intentionally concealed applicable patents and patent applications. CCFF 813-16, 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111, 1238-59, 1676-1700.

In addition, RPF 192 does not support the conclusion that JEDEC "leaders" understood the patent disclosure policy to be anything other than mandatory. Such a conclusion is contrary to the overwhelming weight of contemporaneous evidence (including the 21-I Manual, the Townsend presentations, the Townsend memoranda, and the sign-in sheets) and witness testimony (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer, and Kelley) that confirms that JEDEC intended the disclosure obligation to be mandatory. *See* CCFF 318-19, 324, 330, 360, 363, 367, 370, 378.

196. Between December 1993 and December 1995 (Rambus's last meeting), no IBM patent or patent application was added to the "patent tracking list" maintained by JC 42 Chairman Jim Townsend. (JX 18 at 14-21; JX 19 at 17-23; JX 20 at 15-18; JX 21 at 14-18; JX 22 at 12-17; JX 25 at 18-26; JX 26 at 15-24; JX 27 at 20-25; JX 28 at 12-23).

Response to Finding No. 196: This proposed finding is misleading and does not support a conclusion that JEDEC "leaders" understood the patent disclosure policy to be anything

other than mandatory. As an initial matter, the Patent Tracking List kept by Mr. Townsend was not a complete listing of all patents and patent applications disclosed at JEDEC. *See* CCFF 369. In addition, IBM continued to provide patent disclosures and respond to inquiries as it's representatives had promised. *See, e.g.*, JX0039 at 14 ("IBM: . . . We are not aware of any patent issues").

197. Several JEDEC participants testified that they had heard Gordon Kelley state that IBM would not disclose its intellectual property interests at JEDEC meetings. (Calvin, Tr. 1074-5; Rhoden, Tr. 590; Crisp, Tr. 3503-4). No witness testified that IBM was criticized for its position.

Response to Finding No. 197: This proposed finding is inaccurate, misleading, contrary to the weight of the evidence, and ignores substantial evidence in the record because IBM representatives stated that they would disclose pending or issued patents of which IBM's representatives were aware. *See* CCFF 325-29. As explained by Mr. Kelley and Mr. Kellogg, IBM could not commit to providing a list of all its relevant patents because such a search of the company's patent portfolio would be difficult and, even if undertaken, could not be guaranteed to find all relevant patents. IBM did, however, agree to evaluate any purported patent or patent application that other participants could identify. *See* CCFF 327-28. The testimony of Mr. Kelley and Mr. Kellogg is consistent with contemporaneous IBM business documents. *See, e.g.*, (RX0578 at 2 ("I do not suggest that IBM list applicable patent numbers. Such a list could be construed as complete when it is not. *I plan to alert the committee when I know of applicable patent(s) but not list the patent numbers*."); G. Kelley, Tr. 2455-58). Indeed, IBM did continue to inform JEDEC of patent-related issues. *See, e.g.*, JX0039 at 14 ("IBM: . . . We are not aware of any patent issues"). This is in direct contrast to the conduct of Rambus, which intentionally concealed applicable patents and patent applications. CCFF 813-16, 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111, 1238-59, 1676-1700.

In addition, RPF 192 does not support the conclusion that JEDEC "leaders" understood the patent disclosure policy to be anything other than mandatory. Such a conclusion is contrary to the overwhelming weight of contemporaneous evidence (including the 21-I Manual, the Townsend presentations, the Townsend memoranda, and the sign-in sheets) and witness testimony (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer, and Kelley) that confirms that JEDEC intended the disclosure obligation to be mandatory. *See* CCFF 318-19, 324, 330, 360, 363, 367, 370, 378.

198. Rambus itself declined to comment on two separate occasions, in 1992 and 1995, when asked about its intellectual property. (Crisp, Tr. 3490; JX 27 at 26; Calvin, Tr. 1068-70; RX 297 at 1; CX 673 at 1; RX 290 at 3). There is no evidence that anyone informed Rambus on these occasions that disclosure was mandatory rather than voluntary. (*Id.*).

Response to Finding No. 198: This proposed finding is misleading and incomplete because it fails to state that in 1992 many JEDEC participants did not understand that Richard Crisp knew that Rambus had relevant intellectual property that it failed to disclose. *See* CCFF 811, 856, 857, 866. The finding is misleading and incomplete because it fails to state that in 1995 Richard Crisp pointed to his earlier disclosure of the Rambus '703 patent to imply that Rambus was abiding by the JEDEC disclosure policy and did in fact disclose when it had relevant intellectual property. CCFF 550, 1066. The finding is also misleading and incomplete because it fails to state that, when members perceived or later learned that Rambus in 1995 had intellectual property relating to Ramlink or SyncLink that it failed to disclose at JEDEC, they believed that Rambus acted in bad faith. (G. Kelley, Tr. 2745-46 (Richard Crisp "was not dealing in good faith with me."); Sussman, Tr. 1460-61 (Rambus did not comply with "the good faith requirements set forth [in the EIA Legal Guides]")).

In fact, Rambus was informed on numerous occasions that the disclosure obligation was mandatory. *See* CCFF 357-418. Further, Rambus understood that the disclosure policy was

mandatory. *See* CX0711 at 188 (Richard Crisp noting that "So the conclusion I reach here is that we can abide by the patent policy on a case by case basis. . . As long as we mention that there are potential patent issues when a showing or ballot comes to the floor, the we have not engaged in 'inequitable behavior. . . The things we should not do are to not speak up when we know that there is a patent issue."). Finally, the Federal Circuit has held against Rambus on this very issue and found that disclosure of relevant patent information was an obligation of JEDEC participants. *Rambus, Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1098 (Fed. Cir. 2003).

E. Some JEDEC Representatives Believed That No Disclosure Was Required As Long As The Member Company Ultimately Licensed Its Relevant Patents To All Comers On Reasonable Terms.

199. Hans Wiggers, a JEDEC representative from Hewlett-Packard in the early to mid 90's, testified that it was his understanding of the JEDEC patent policy that as long as a company licensed its patents after they issued on reasonable and non-discriminatory terms to all interested parties, it had no obligation under the patent policy to disclose its intellectual property. (Wiggers, Tr. 10591).

Response to Finding No. 199: This proposed finding is unreliable because Hewlett-Packard's official representative to JEDEC during the relevant time period, Thomas Landgraf, testified that disclosure was mandatory. (Landgraf, Tr. 1695-96). Further, RPF 199 is contrary to the weight of the evidence because numerous other witnesses testified that the disclosure obligation was mandatory, regardless of a company's licensing position. *See* CCFF 324. In addition, Respondent understood that the disclosure policy was mandatory. *See* CX0711 at 188 (Richard Crisp noting that "As long as we mention that there are potential patent issues when a showing or ballot comes to the floor, we have not engaged in 'inequitable behavior'. . . The things we should not do are to not speak up when we know that there is a patent issue."). The Federal Circuit has held against Rambus on this very issue and found that disclosure of relevant patent information was an obligation of JEDEC participants. *Rambus, Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1098 (Fed. Cir. 2003). In any event, this issue is irrelevant

because the overwhelming weight of the evidence demonstrates that Rambus would not have promised to license its technologies on reasonable and non-discriminatory terms. CCFF 2418-32.

200. Gordon Kelley, a JEDEC representative from IBM who served as the chair of the 42.3 subcommittee in the early and mid-1990's, testified that he did not disclose IBM patents relating to "toggle mode" in 1990 in part because IBM was "prepared to meet the requirements of the JEDEC committee" to license the patents on reasonable and non-discriminatory terms. (Kelley, Tr. 2715-16).

Response to Finding No. 200: Ths proposed finding is inaccurate and misleading. Mr. Kelley testified that he did not disclose IBM patents relating to toggle mode *again* in 1990 because he had previously disclosed them in 1988. (G. Kelley, Tr. 2714). RPF 200 is contrary to the weight of the evidence because numerous other witnesses testified that the disclosure obligation was mandatory, regardless of a company's licensing position. *See* CCFF 324. In addition, Respondent understood that the disclosure policy was mandatory. *See* CX0711 at 188 (Richard Crisp noting that "As long as we mention that there are potential patent issues when a showing or ballot comes to the floor, the we have not engaged in 'inequitable behavior'. . . The things we should not do are to not speak up when we know that there is a patent issue."). The Federal Circuit has held against Rambus on this very issue and found that disclosure of relevant patent information was an obligation of JEDEC participants. *Rambus, Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1098 (Fed. Cir. 2003). In any event, this issue is irrelevant because the overwhelming weight of the evidence demonstrates that Rambus would not have promised to license its technologies on reasonable and non-discriminatory terms. CCFF 2418-32.

201. Desi Rhoden, who is currently the Chairman of the Board of JEDEC and President of AMI2, gave similar testimony about whether intellectual property disclosures made to JEDEC by AMI2's corporate predecessor had complied with JEDEC's patent policy. Rhoden testified that a statement by AMI2's predecessor that it "might have IP relating" to its presentation and would license it "under the JEDEC patent policy" was a sufficient disclosure of the intellectual property under the policy. (Rhoden, Tr. 1304-5).

Response to Finding No. 201: This proposed finding is misleading and inaccurate because SyncLink Consortium did inform JEDEC that patents had been applied for that related to the SyncLink proposal. (Rhoden, Tr. 1304). As Mr. Rhoden explained, he could not be certain that every single patent application was disclosed because many of the patents that ultimately issued had not even been filed at the time the SyncLink project was discussed within JEDEC. (Rhoden, Tr. 1304 ("At the time of disclosure, many of these had not been filed, and so I'm not certain and I could not testify that each and every one of the applications and ultimate patents by word or by description were disclosed in that manner."). Once the SyncLink proposal failed to generate much interest at JEDEC, due in large part to patent concerns (*see* CX0711 at 171 (Mr. Crisp reported that one of the meeting participants told Mr. Crisp that he thought the reason there would be no second showings of the SyncLink technology at JEDEC was that "we [Rambus] have cast doubt over the patent issue."), there was no reason to continue making subsequent disclosures to JEDEC. In any event, this issue is irrelevant because the overwhelming weight of the evidence demonstrates that Rambus would not have promised to license its technologies on reasonable and non-discriminatory terms. CCFF 2418-32.

202. The January 1996 letter by EIA and TIA to the FTC also points out that "[e]ven if knowledge of a patent comes later in time due to the pending status of the patent while the standard was being created, the important issue is the license availability to all parties on reasonable, non-discriminatory terms." (RX 669 at 4).

Response to Finding No. 202: Complaint Counsel does not disagree. RPF 202 is misleading, however, because disclosure of the patent was both mandatory and important if knowledge of the patent existed at the time of the JEDEC work. *See* CCFF 316-24. In any event, this issue is irrelevant because the overwhelming weight of the evidence demonstrates that Rambus would not have promised to license its technologies on reasonable and non-discriminatory terms. CCFF 2418-32.

203. EIA General Counsel John Kelly similarly testified that there is no objection to having standards that incorporate patented technologies as long as the patents are available to all comers on reasonable and nondiscriminatory terms. (Kelly, Tr. 2072).

Response to Finding No. 203: This proposed finding does not support the conclusion that disclosure of patents and patent applications is not mandatory and important. As indicated in the JEDEC Manual of Organization and Procedure, the Chairman of the committee is required to obtain a licensing assurance letter before a JEDEC standard may refer to patented or patentable material. (CX0208 at 19). Obviously, a committee Chairman cannot obtain an assurance letter if the patent or patent application is not disclosed. Further, a conclusion that the disclosure of patents and patent applications was not mandatory is contrary to the weight of the evidence. *See* CCFF 318-19, 324, 330. In any event, this issue is irrelevant because the overwhelming weight of the evidence demonstrates that Rambus would not have promised to license its technologies on reasonable and non-discriminatory terms. CCFF 2418-32.

F. If There Were A Disclosure Requirement, It Extended Only To Issued Patents And Not To Patent Applications.

204. Assuming that JEDEC members were obligated to disclose some intellectual property interests at JEDEC meetings while Rambus was a member, Complaint Counsel did not meet their burden of proving that that obligation extended to patent applications.

Response to Finding No. 204: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Furthermore, RPF 204 is contrary to the weight of the evidence. *See* CCFF 319-22. Furthermore, the Federal Circuit has held against Respondent on this very issue and found that disclosure of relevant patent information was an obligation of JEDEC participants. *Rambus, Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1098 (Fed. Cir. 2003).

1. The ANSI Patent Policy, Which Was Formally Adopted By The EIA At Least By October 1995, Does Not Require The Disclosure Of Patent Applications.

205. It was undisputed at trial that the ANSI Patent Policy does not require the disclosure of patent applications by standards participants. (Kelly, Tr. 1958; 2074).

Response to Finding No. 205: Complaint Counsel does not disagree. This proposed finding, however, is misleading and does not support the conclusion that JEDEC did not require disclosure of patent applications. In any event, the specific terms of the ANSI policy are irrelevant in the face of the overwhelming weight of the evidence that JEDEC members understood the JEDEC policy to require disclosure of patent application as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 at 2 (draft JEDEC minutes of Townsend presentation "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

Furthermore, the overwhelming weight of the evidence indicates that Rambus representatives understood that the JEDEC disclosure obligation applied to both patents and patent applications. *See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.)

("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); *see also* CX0685 at 1 (Mooring e-mail, 12/11/92: IBM stated that some "offenders" had "patents pending" on SDRAMs that they had not made the Committee aware of).

206. The EIA officially adopted the ANSI Patent Policy at least as early as October 1995, when it published EIA Manual EP-7-B. (RX 616 at 2). The EP-7-B manual, which would have been generally available to JEDEC members after its publication (Kelly, Tr. 2082), provides that "[s]tandards and publications are adopted by EIA in accordance with the [ANSI] patent policy." (RX 616 at 2).

Response to Finding No. 206: This proposed finding is incorrect and misleading because it fundamentally misinterprets the meaning of the phrase "adopted by EIA in accordance with." ANSI does not require standard setting organizations to adhere rigidly to the precise metes and bounds of the ANSI Patent Policy. *See* CCFF 441. Indeed, the ANSI patent policy guidelines specifically contemplate that standard setting organizations like EIA may adopt provisions that differ materially from the ANSI patent policy and still comply with the guidelines. (RX1712 at 3). Of particular relevance in this matter, ANSI patent policy guidelines specifically provide that "a standards developer may wish to encourage participants to disclose the existence of pending U.S. patent applications." (RX1712 at 8). From time to time, EIA standards are proposed to be American National Standards through a review process conducted by ANSI. *See* CCFF 436. As a part of that process, such EIA standards must have been adopted pursuant to a process that complies with ANSI guidelines. EIA's patent policy is in compliance with ANSI Guidelines. *See* CCFF 440. Furthermore, the ANSI patent policy and its guidelines have even less relevance within JEDEC because JEDEC is not an ANSI accredited organization (*see* J. Kelly, Tr.1949) and, therefore, is not even required to comply with the ANSI guidelines, much less the ANSI patent policy itself.

In any event, the specific terms of the ANSI policy are irrelevant in the face of the overwhelming weight of the evidence that JEDEC members understood the JEDEC policy to require disclosure of patent application as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 at 2 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

Furthermore, the overwhelming weight of the evidence indicates that Rambus representatives understood that the JEDEC disclosure obligation applied to both patents and patent applications. *See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); *see also* CX0685 at 1 (Mooring e-mail, 12/11/92: IBM stated that some "offenders" had "patents pending" on SDRAMs that they had not made the Committee aware of).

207. During the time that Rambus was a JEDEC member, EIA manuals and policies governed JEDEC standardization activities. (Kelly, Tr. 1918; RX 1179 at 1). In the event of a conflict, the EIA manual would control over the JEDEC manual. (Kelly, Tr. 1915-16).

Response to Finding No. 207: This proposed finding is incomplete and misleading because in addition to the basic rules set forth in the EIA Legal Guides, the procedures specifically applicable to the JEDEC standardization process are contained in the JEDEC Manual of Organization and Procedure. *See* CCFF 404. In addition, the EIA Legal Guides specifically state that they "supplement[] the procedures contained in the Engineering Department 'Manual of Organization and Procedure.'" (CX0204 at 4). JEP-21 is the Manual of Organization and Procedure. (CX0208). In addition, RPF 207 is misleading and incomplete because Mr. Kelly also testified that during his time at EIA, which began in 1990, there has been no conflict between the JEDEC Manual of Organization and Procedure and any EIA manual. (J. Kelly, Tr. 1916 ("Q. Just to be clear, are you aware of any conflict that has existed between JEDEC's separate rules and EIA rules at any time during your tenure as EIA general counsel? A. No, sir.")).

In any event, the specific terms of the EIA rules are irrelevant in the face of the overwhelming weight of the evidence that JEDEC members understood the JEDEC policy to require disclosure of patent application as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 at 2 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

Furthermore, the overwhelming weight of the evidence indicates that Rambus representatives understood that the JEDEC disclosure obligation applied to both patents and patent applications. *See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of

the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); *see also* CX0685 at 1 (Mooring e-mail, 12/11/92: IBM stated that some "offenders" had "patents pending" on SDRAMs that they had not made the Committee aware of).

208. ANSI published "Guidelines" regarding its patent policy. The ANSI patent policy guidelines were circulated to JC 42.3 members in 1994 at the request of EIA General Counsel John Kelly. (CX 353 at 1; Kelly, Tr. 1950).

Response to Finding No. 208: This proposed finding does not support the conclusion that the ANSI patent policy guidelines reflect the JEDEC disclosure policy because the ANSI patent policy guidelines specifically contemplate that standard setting organizations like JEDEC may adopt provisions that differ materially from the ANSI patent policy and still comply with the Guidelines. (RX1712 at 3). Of particular relevance in this matter, ANSI patent policy guidelines specifically approve that "a standards developer may wish to encourage participants to disclose the existence of pending U.S. patent applications." (RX1712 at 8). For a more complete discussion of the relationship between the ANSI patent policy, the ANSI patent policy guidelines, and the JEDEC patent policy, *see* CCFF 435-43, CCRF 141-44.

In any event, the specific terms of the ANSI guidelines are irrelevant in the face of the overwhelming weight of the evidence that JEDEC members understood the JEDEC policy to require disclosure of patent application as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules

governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 at 2 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

Furthermore, the overwhelming weight of the evidence indicates that Rambus representatives understood that the JEDEC disclosure obligation applied to both patents and patent applications. *See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); *see also* CX0685 at 1 (Mooring e-mail, 12/11/92: IBM stated that some "offenders" had "patents pending" on SDRAMs that they had not made the Committee aware of).

209. Mr. Kelly caused the ANSI Guidelines to be circulated to JC 42.3 members in 1994 because he "thought they provided insight into the proper interpretation of the EIA and JEDEC patent policy." (Kelly, Tr. 1950).

Response to Finding No. 209: This proposed finding does not support the conclusion that the ANSI patent policy guidelines reflect the JEDEC disclosure policy because the ANSI patent policy guidelines specifically contemplate that standard setting organizations like JEDEC may adopt provisions that differ materially from the ANSI patent policy and still comply

with the guidelines. (RX1712 at 3). Of particular relevance in this matter, ANSI patent policy guidelines specifically approve that "a standards developer may wish to encourage participants to disclose the existence of pending U.S. patent applications." (RX1712 at 8). For a more complete discussion of the relationship between the ANSI patent policy, the ANSI patent policy guidelines, and the JEDEC patent policy, *see* CCFF 435-43, CCRF 141-44. In addition, the specific issue that instigated the distribution of the ANSI guidelines did not relate in any way to the disclosure of patent applications. *See* (J. Kelly, Tr. 2077 (J. Kelly, Tr. 2077 ("I don't believe that [disclosure of patent applications] was the issue TI raised")). Mr. Kelly's memorandum was in response to a request from Texas Instruments to clarify whether JEDEC participants must make a factual determination that a standard requires the use of the patent. (CX0353 at 1). Mr. Kelly responded that "[w]ritten assurances must be provided by the patent holder when it appears to the committee that the candidate standard may require the use of a patented invention." (CX0353 at 1) (underline in original). For a more complete discussion of the Quad CAS controversy, *see* CCFF 424-32.

In any event, the specific terms of the ANSI guidelines are irrelevant in the face of the overwhelming weight of the evidence that JEDEC members understood the JEDEC policy to require disclosure of patent application as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

Furthermore, the overwhelming weight of the evidence indicates that Rambus representatives understood that the JEDEC disclosure obligation applied to both patents and patent applications. *See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); *see also* CX0685 at 1 (Mooring e-mail, 12/11/92: IBM stated that some "offenders" had "patents pending" on SDRAMs that they had not made the Committee aware of).

210. At the time that he caused the ANSI Guidelines to be circulated to JC 42.3 members, Mr. Kelly understood that the ANSI Patent Policy did not require the disclosure of patent applications. (Kelly, Tr. 2075).

Response to Finding No. 210: This proposed finding does not support the conclusion that the ANSI patent policy guidelines reflect the JEDEC disclosure policy because the ANSI patent policy guidelines specifically contemplate that standard setting organizations like JEDEC may adopt provisions that differ materially from the ANSI patent policy and still comply with the Guidelines. (RX1712 at 3). Of particular relevance in this matter, ANSI patent policy guidelines specifically approve that "a standards developer may wish to encourage participants to disclose the existence of pending U.S. patent applications." (RX1712 at 8). For a more complete discussion of the relationship between the ANSI patent policy, the ANSI patent policy guidelines, and the JEDEC patent policy, *see* CCFF 435-43, CCRF 141-44. In addition, the specific issue that instigated the distribution of the ANSI guidelines did not relate in any way to the disclosure of

patent applications. *See* (J. Kelly, Tr. 2077 (J. Kelly, Tr. 2077 ("I don't believe that [disclosure of patent applications] was the issue TI raised")). Mr. Kelly's memorandum was in response to a request from Texas Instruments to clarify whether JEDEC participants must make a factual determination that a standard requires the use of the patent. (CX0353 at 1). Mr. Kelly responded that "[w]ritten assurances must be provided by the patent holder when it appears to the committee that the candidate standard may require the use of a patented invention." (CX0353 at 1) (underline in original). For a more complete discussion of the Quad CAS controversy, *see* CCFF 424-32.

In any event, the specific terms of the ANSI guidelines are irrelevant in the face of the overwhelming weight of the evidence that JEDEC members understood the JEDEC policy to require disclosure of patent application as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 at 2 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

Furthermore, the overwhelming weight of the evidence indicates that Rambus representatives understood that the JEDEC disclosure obligation applied to both patents and patent applications. *See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.)

("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); *see also* CX0685 at 1 (Mooring e-mail, 12/11/92: IBM stated that some "offenders" had "patents pending" on SDRAMs that they had not made the Committee aware of).

211. The ANSI Guidelines themselves were one basis for Mr. Kelly's view, at the time he circulated the ANSI Guidelines to JC 42.3 members, that the ANSI Patent Policy did not require the disclosure of patent applications. (Kelly, Tr. 2077).

Response to Finding No. 211: This proposed finding does not support the conclusion that the ANSI patent policy guidelines reflect the JEDEC disclosure policy because the ANSI patent policy guidelines specifically contemplate that standard setting organizations like JEDEC may adopt provisions that differ materially from the ANSI patent policy and still comply with the guidelines. (RX1712 at 3). Indeed, ANSI patent policy guidelines specifically approve that "a standards developer may wish to encourage participants to disclose the existence of pending U.S. patent applications." (RX1712 at 8). For a more complete discussion of the relationship between the ANSI patent policy, the ANSI patent policy guidelines, and the JEDEC patent policy, *see* CCFF 435-43, CCRF 141-44. In addition, the specific issue that instigated the distribution of the ANSI guidelines did not relate in any way to the disclosure of patent applications. *See* (J. Kelly, Tr. 2077 (J. Kelly, Tr. 2077 ("I don't believe that [disclosure of patent applications] was the issue TI raised")). Mr. Kelly's memorandum was in response to a request from Texas Instruments to clarify whether JEDEC participants must make a factual determination that a standard requires the use of the patent. (CX0353 at 1). Mr. Kelly responded that "[w]ritten assurances must be provided by the patent holder when it appears to the committee that the candidate standard may require the use of a patented invention." (CX0353 at 1) (underline in original). For a more complete discussion of the Quad CAS controversy, *see* CCFF 424-32.

In any event, the specific terms of the ANSI guidelines are irrelevant in the face of the overwhelming weight of the evidence that JEDEC members understood the JEDEC policy to require disclosure of patent application as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

Furthermore, the overwhelming weight of the evidence indicates that Rambus representatives understood that the JEDEC disclosure obligation applied to both patents and patent applications. *See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); *see also* CX0685 at 1 (Mooring e-mail, 12/11/92: IBM stated that some "offenders" had "patents pending" on SDRAMs that they had not made the Committee aware of).

212. At the time that the ANSI Guidelines were circulated to JC 42.3 members in 1994, the language of the EIA patent policy and the ANSI patent policy was essentially identical. (Kelly, Tr. 2077-78).

Response to Finding No. 212: This proposed finding does not support the conclusion that the ANSI patent policy guidelines reflect the JEDEC disclosure policy because the ANSI patent policy guidelines specifically contemplate that standard setting organizations like JEDEC may adopt provisions that differ materially from the ANSI patent policy and still comply with the Guidelines. (RX1712 at 3). Of particular relevance in this matter, ANSI patent policy guidelines specifically approve that "a standards developer may wish to encourage participants to disclose the existence of pending U.S. patent applications." (RX1712 at 8). For a more complete discussion of the relationship between the ANSI patent policy, the ANSI patent policy guidelines, and the JEDEC patent policy, *see* CCFF 435-43, CCRF 141-44. In addition, the specific issue that instigated the distribution of the ANSI guidelines did not relate in any way to the disclosure of patent applications. *See* (J. Kelly, Tr. 2077 (J. Kelly, Tr. 2077 ("I don't believe that [disclosure of patent applications] was the issue TI raised")). Mr. Kelly's memorandum was in response to a request from Texas Instruments to clarify whether JEDEC participants must make a factual determination that a standard requires the use of the patent. (CX0353 at 1). Mr. Kelly responded that "[w]ritten assurances must be provided by the patent holder when it appears to the committee that the candidate standard may require the use of a patented invention." (CX0353 at 1) (underline in original). For a more complete discussion of the Quad CAS controversy, *see* CCFF 424-32.

In any event, the specific terms of the ANSI Guidelines are irrelevant in the face of the overwhelming weight of the evidence that JEDEC members understood the JEDEC policy to require disclosure of patent application as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 (draft JEDEC minutes

regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

Furthermore, the overwhelming weight of the evidence indicates that Rambus representatives understood that the JEDEC disclosure obligation applied to both patents and patent applications. *See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); *see also* CX0685 at 1 (Mooring e-mail, 12/11/92: IBM stated that some "offenders" had "patents pending" on SDRAMs that they had not made the Committee aware of).

213. The cover memorandum that accompanied the ANSI Guidelines when they were circulated to JC 42.3 members in 1994 said nothing that would have alerted recipients that the EIA, unlike ANSI, supposedly required disclosure of patent applications. (CX 353 at 1).

Response to Finding No. 213: This proposed finding does not support the conclusion that the ANSI Patent policy guidelines reflect the JEDEC disclosure policy because the ANSI Patent policy guidelines specifically contemplate that standard setting organizations like JEDEC may go beyond the ANSI patent policy and still comply with the Guidelines. (RX1712 at 3). Indeed, ANSI Patent policy guidelines specifically approve that "a standards developer may wish to encourage participants to disclose the existence of pending U.S. patent applications." (RX1712 at 8). For a more complete discussion of the relationship between the ANSI Patent

policy, the ANSI Patent policy guidelines, and the JEDEC patent policy, *see* CCFF 435-43, CCRF 141-44. In addition, the specific issue that instigated the distribution of the ANSI guidelines did not relate in any way to the disclosure of patent applications. *See* (J. Kelly, Tr. 2077 (J. Kelly, Tr. 2077 ("I don't believe that [disclosure of patent applications] was the issue TI raised")). Mr. Kelly's memorandum was in response to a request from Texas Instruments to clarify whether JEDEC participants must make a factual determination that a standard requires the use of the patent. (CX0353 at 1). Mr. Kelly responded that "[w]ritten assurances must be provided by the patent holder when it appears to the committee that the candidate standard may require the use of a patented invention." (CX0353 at 1) (underline in original). For a more complete discussion of the Quad CAS controversy, *see* CCFF 424-32.

In any event, the specific terms of the ANSI Guidelines are irrelevant in the face of the overwhelming weight of the evidence that JEDEC members understood the JEDEC policy to require disclosure of patent application as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

Furthermore, the overwhelming weight of the evidence indicates that Rambus representatives understood that the JEDEC disclosure obligation applied to both patents and patent applications. *See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must

have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); *see also* CX0685 at 1 (Mooring e-mail, 12/11/92: IBM stated that some "offenders" had "patents pending" on SDRAMs that they had not made the Committee aware of).

2. The EIA's January 1996 Comment Letter To The FTC Refers Only To Voluntary Disclosure Of Patents, Not Patent Applications.

214. The EIA's January 1996 comment letter to the FTC states that the EIA "endorse[s] and follow[s] the ANSI Intellectual Property Rights ("IPR") policy . . . ." (RX 669 at 2).

Response to Finding No. 214: This proposed finding is misleading because it fundamentally misinterprets the meaning of the phrase "endorse[d] and follow[ed] the ANSI intellectual property rights (IPR) policy" As noted in CCRF 127, from time to time, EIA standards are proposed to be American National Standards through a review process conducted by ANSI. *See* CCFF 436. As a part of that process, such EIA standards must have been adopted pursuant to a process that complies with minimum ANSI policies, including the ANSI Patent policy and the ANSI Patent policy guidelines. ANSI does not require standard setting organizations to adhere rigidly to the precise metes and bounds of the ANSI Patent policy. *See* CCFF 441. Indeed, ANSI specifically contemplates that organizations will choose different substantive rules, including rules relating to the disclosure of patent applications. *See* CCFF 442-43. Thus, EIA standards may be adopted in accordance with the ANSI Patent policy and Guidelines, notwithstanding the fact that there are substantive differences between EIA patent policy and the ANSI patent policy. EIA is in

compliance with ANSI Guidelines. *See* CCFF 440. Furthermore, the ANSI patent policy and guidelines have even less relevance within JEDEC because JEDEC is not and ANSI accredited organization (*see* J. Kelly, Tr. 1949) and, therefore, is not even required to comply with the ANSI guidelines, much less the ANSI patent policy itself. For a more complete discussion of the relationship between the ANSI Patent policy, the ANSI Patent policy guidelines, and the JEDEC patent policy, *see* CCFF 435-43.

In any event, the specific terms of the EIA's comment letter and the ANSI Guidelines are irrelevant in the face of the overwhelming weight of the evidence that JEDEC members understood the JEDEC policy to require disclosure of patent application as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

Furthermore, the overwhelming weight of the evidence indicates that Rambus representatives understood that the JEDEC disclosure obligation applied to both patents and patent applications. *See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.)

("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); *see also* CX0685 at 1 (Mooring e-mail, 12/11/92: IBM stated that some "offenders" had "patents pending" on SDRAMs that they had not made the Committee aware of).

215. EIA General Counsel John Kelly reviewed and approved the EIA's January 1996 comment letter to the FTC before it was submitted, and Mr. Kelly's name and title appear in the signature block. (RX 669 at 5; Kelly, Tr. 2092-3).

Response to Finding No. 215: Complaint Counsel does not disagree. However, this proposed finding does not support the conclusion that the disclosure of patents and patent applications at JEDEC is voluntary because RPF 215 fundamentally misapprehends the meaning on the term "voluntary" as it relates to JEDEC. JEDEC is a voluntary organization (CCFF 323) and JEDEC is unable to impose sanctions on members for failure to comply with any part of the patent policy. (CCFF 419-20). JEDEC, therefore, necessarily depends upon the good faith, voluntary cooperation of participants in complying with the requirements of the patent policy. (CCFF 314). The requirements of the patent policy, however, are mandatory. (CCFF 324).

In any event, the specific terms of the EIA's comment letter are irrelevant in the face of the overwhelming weight of the evidence that JEDEC members understood the JEDEC policy to require disclosure of patent application as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent

applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

Furthermore, the overwhelming weight of the evidence indicates that Rambus representatives understood that the JEDEC disclosure obligation applied to both patents and patent applications. *See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); *see also* CX0685 at 1 (Mooring e-mail, 12/11/92: IBM stated that some "offenders" had "patents pending" on SDRAMs that they had not made the Committee aware of).

216. The EIA's January 1996 comment letter to the FTC states that the "EIA and TIA encourage the early, voluntary disclosure of patents that relate to the standards in work." (RX 669 at 3). The letter does not state that the EIA requires (or even encourages) the disclosure of patent applications. (*Id.*).

Response to Finding No. 216: This proposed finding does not support the conclusion that the disclosure of patents and patent applications at JEDEC is voluntary because RPF 216 fundamentally misapprehends the meaning on the term "voluntary" as it relates to JEDEC. JEDEC is a voluntary organization (CCFF 323) and JEDEC is unable to impose sanctions on members for failure to comply with any part of the patent policy. (CCFF 419-20). JEDEC, therefore, necessarily depends upon the good faith, voluntary cooperation of participants in complying with the requirements of the patent policy. (CCFF 314). The requirements of the

patent policy, however, are mandatory. (CCFF 324). Finally, the Federal Circuit has held against Rambus on this very issue and found that disclosure of relevant patent information was an obligation of JEDEC participants. *Rambus, Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1098 (Fed. Cir. 2003).

In any event, the specific terms of the EIA's comment letter are irrelevant in the face of the overwhelming weight of the evidence that JEDEC members understood the JEDEC policy to require disclosure of patent application as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

Furthermore, the overwhelming weight of the evidence indicates that Rambus representatives understood that the JEDEC disclosure obligation applied to both patents and patent applications. *See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); *see also*

CX0685 at 1 (Mooring e-mail, 12/11/92: IBM stated that some "offenders" had "patents pending" on SDRAMs that they had not made the Committee aware of).

217. The EIA's January 1996 comment letter to the FTC also states that ". . . if knowledge of a patent comes later in time due to the pending status of the patent while the standard was being created, the important issue is the license availability to all parties on reasonable, non-discriminatory terms." (RX 669 at 4).

Response to Finding No. 217: Complaint Counsel does not disagree. This proposed finding is incomplete, however, because it fails to state that the JEDEC patent policy contains a continuing duty to disclose, even if the patent was applied for or discovered after adoption of the relevant standard. *See* CCFF 346. In other words, the JEDEC duty to disclose was mandatory from the time of knowledge of the patents.

In any event, the specific terms of the EIA's comment letter are irrelevant in the face of the overwhelming weight of the evidence that JEDEC members understood the JEDEC policy to require disclosure of patent application as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

Furthermore, the overwhelming weight of the evidence indicates that Rambus representatives understood that the JEDEC disclosure obligation applied to both patents and patent applications. *See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must

have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); *see also* CX0685 at 1 (Mooring e-mail, 12/11/92: IBM stated that some "offenders" had "patents pending" on SDRAMs that they had not made the Committee aware of).

218. On July 10, 1996, JEDEC Secretary Ken McGhee sent a memorandum to all JEDEC Council members and alternates that stated in part that ANSI and the EIA "encourage early, voluntary disclosure of any known essential patents." (RX 742 at 1). Mr. McGhee's memorandum does not state that ANSI or the EIA requires (or even encourages) disclosure of patent applications. (*Id.*).

Response to Finding No. 218: This proposed finding does not support the conclusion that the disclosure of patents and patent applications at JEDEC is voluntary because RPF 216 fundamentally misapprehends the meaning on the term "voluntary" as it relates to JEDEC. JEDEC is a voluntary organization (CCFF 323) and JEDEC is unable to impose sanctions on members for failure to comply with any part of the patent policy. (CCFF 419-20). JEDEC, therefore, necessarily depends upon the good faith, voluntary cooperation of participants in complying with the requirements of the patent policy. (CCFF 314). The requirements of the patent policy, however, are mandatory for all companies that choose to be members. (CCFF 324). *See Rambus, Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1098 (Fed. Cir. 2003). Further, this proposed finding is incomplete and misleading because, as is clear from the face of the document, the purpose of Mr. McGhee's memorandum was to inform JEDEC Council members and alternates that EIA "filed Comments with the FTC . . . requesting the FTC to limit its application of the law to the narrow facts of [the *Dell*] case and not to impose a general obligation

on participants in standard-setting activities to search their patent portfolios" (RX0742 at 1). It also is clear that EIA understood the Commission's action did not "signal a general duty to search for patents when a company engages in standards setting." (RX0742 at 1).

In any event, the specific terms of the EIA's comment letter are irrelevant in the face of the overwhelming weight of the evidence that JEDEC members understood the JEDEC policy to require disclosure of patent application as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

Furthermore, the overwhelming weight of the evidence indicates that Rambus representatives understood that the JEDEC disclosure obligation applied to both patents and patent applications. *See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); *see also*

CX0685 at 1 (Mooring e-mail, 12/11/92: IBM stated that some "offenders" had "patents pending" on SDRAMs that they had not made the Committee aware of).

3. Gordon Kelley's Testimony About The So-Called "Hand Vote" Is Not A Credible Basis For Finding A Disclosure Obligation.

219. Gordon Kelley, the IBM representative who chaired the 42.3 subcommittee and who later chaired the JEDEC Council as well, testified that he understood that the word "patent" as used in EIA manuals meant only "issued patents," not "patents and patent applications." (Kelley, Tr. 2686-7; 2696-7).

Response to Finding No. 219: This proposed finding is contrary to the weight of the evidence because numerous witnesses testified that the term "patent" was interpreted to include patent applications. *See* CCFF 320. As an initial matter, there is no evidence that Gordon Kelley has any role with respect to the EIA manuals to which Respondent refers. Further, Gordon Kelley is not the authoritative interpreter of the JEDEC patent policy – that authority resides with EIA Legal Counsel, which was John Kelly during the entire relevant time period. *See* CCFF 226-27. Mr. Kelly testified that EIA's interpretation has always been that the term "patents" as used within EIA and JEDEC includes patent applications. (J. Kelly, Tr. 1886-88). As Mr. Kelly explained, the patent policy required disclosure of patent applications because "[t]he industry probably moves even more quickly, particularly in high technology industries like the ones that EIA works with, and frequently patent applications move at a measured pace through the patent application policy to the issuance of final patents. So, if the work of the committee was held up, in effect, by the condition that only issued patents needed to be disclosed, then the standard development process could reach a very late stage or, in fact, already be concluded by the time a patent finally issued and there was disclosure that the patent was required to comply with the work by the committee on the standard under development, and that would produce exactly the same kind of anti-competitive result that we're trying to prevent by the disclosure." (J. Kelly, Tr. 1896-97). As Mr. Kelly further explained, the textual changes in the 21-I manual to include a reference

to pending patents "was a restatement of the patent policy, and it in no way varied the policy itself." (J. Kelly, Tr. 1925). Even Mr. Gordon Kelley, among other participants, testified that the change in language did not change the substance of the patent policy. *See* CCFF 416.

220. Mr. Kelley testified that he did not believe at any time prior to Rambus's departure from JEDEC that the EIA had changed its interpretation of the word "patents" to include "patents *and* patent applications." (Kelley, Tr. 2695; 2697).

Response to Finding No. 220: This proposed finding is incomplete and misleading. Mr. Kelley testified that the JEDEC disclosure policy called for disclosure of anything in the patent process, including patents and patent applications. CCFF 335, 343-44. Furthermore, the proposed finding does not support the conclusion that the JEDEC patent policy did not require the disclosure of patent applications. EIA Legal Counsel John Kelly testified that EIA's interpretation has always been that the term "patents" as used within EIA and JEDEC includes patent applications. (J. Kelly, Tr. 1886-88). Both Mr. Gordon Kelley and Mr. John Kelly testified that the textual changes in the 21-I manual to include a reference to pending patents "was a restatement of the patent policy, and it in no way varied the policy itself." (G. Kelley, Tr. 2415-16; J. Kelly, Tr. 1925). Because EIA has always interpreted the term "patents" to include patent applications, there was no need to EIA to "change" its interpretation prior to Rambus's resignation from JEDEC.

221. Mr. Kelley testified that prior to May 1991, he did not understand that JEDEC members had any obligation to disclose patent applications relating to the work of JEDEC. (Kelley, Tr. 2686-7; 2692).

Response to Finding No. 221: This proposed finding is contrary to the weight of the evidence because EIA has always interpreted the JEDEC patent policy to require the disclosure of patent applications. EIA Legal Counsel, John Kelly testified that EIA's interpretation has always been that the term "patents" as used within EIA and JEDEC includes patent applications. (J. Kelly, Tr. 1886-88). As Mr. Kelly explained, the patent policy required disclosure of patent

applications because "[t]he industry probably moves even more quickly, particularly in high technology industries like the ones that EIA works with, and frequently patent applications move at a measured pace through the patent application policy to the issuance of final patents. So, if the work of the committee was held up, in effect, by the condition that only issued patents needed to be disclosed, then the standard development process could reach a very late stage or, in fact, already be concluded by the time a patent finally issued and there was disclosure that the patent was required to comply with the work by the committee on the standard under development, and that would produce exactly the same kind of anti-competitive result that we're trying to prevent by the disclosure." (J. Kelly, Tr. 1896-97). In addition, numerous other participants also understood prior to May 1991 that the JEDEC patent policy required disclosure of patent applications. *See* CCFF 320 (citing Rhoden, Tr. 317-21; Sussman, Tr. 1342). In fact, as Mr. Kelley conceded, his erroneous personal interpretation prior to May 1991 was not shared by the other participants. (G. Kelley, Tr. 2695 ("it was very clear on the committee that the committee considered the issue of patent to be issued patents as well as material that might become issued patents.")).

222. Mr. Kelley testified that at the May 1991 meeting of the JC 42.3 subcommittee, a "hand vote" was supposedly taken at which the subcommittee agreed to adopt a "new definition of patents" within JC 42.3. According to Mr. Kelley, the JC 42.3 members voted to include "patent applications" within the definition of "patents" and to require disclosure of both. (Kelley, Tr. 2669; 2691).

Response to Finding No. 222: This proposed finding does not support the conclusion that the obligation to disclose patent applications did not exist prior to May 1991. In consideration of the fact that prior to May 1991 EIA interpreted and JEDEC participants understood that the disclosure obligation extended to patent applications, the logical conclusion to be drawn by Mr. Kelley's testimony is that the "hand vote" was a confirmation of what JEDEC participants already understood. This conclusion is further supported by the concern within the committee the arose from the *Wang* litigation, which involved allegations of a failure to disclosure

a patent application. For a more complete discussion of the *Wang* litigation, the concern it generated within JEDEC, and the additional efforts to educate JEDEC participants concerning their disclosure obligation that were begun in the wake of the *Wang* litigation, *see* CCFF 362, 377, 434. What also is clear is that there was an extensive discussion of the patent policy at the May 1991 JC-42.3 meeting. (JX0005 at 3-4, 20). It was at this meeting that Mr. Townsend proposed to have a presentation of the patent policy at each meeting. Mr. Townsend noted that due to the turnover of the participants "many reps do not know what the policies are." (JX0005 at 3). He further noted that :the important thing is disclosure." (JX0005 at 4). Thus the "hand vote" that Mr. Kelley discussed likely took place during this extensive discussion of the JEDEC patent policy. This conclusion is further supported by the events at the March 1994 JC-42.3 committee meeting, at which members were asked to indicate by hand vote whether the JEDEC disclosure policy was clear. CCFF 985.

Finally, Respondent had ample opportunity to ask questions of other witnesses who were present at the May 1991 meeting. A number of witnesses, including witnesses called by Rambus, were present at the May 1991 JC-42.3 meeting and could have been asked questions relating to this issue. *See* JX0005 at 1-2 (listing Alan Grossmeier, Farhad Tabrizi, Howard Sussman, Desi Rhoden, Mark Kellogg, and Betty Prince as present). In addition, the following witnesses who were on Rambus's final witness list whom Rambus failed to call also were present: David Chapman, Gil Russell, Ernest Powell, Ken McGhee, and Joel Karp. *See* (JX0005 at 1-2).

223. While Mr. Kelley initially testified that the "hand vote" occurred at the May 1992 JC 42.3 meeting, he later changed his testimony to say that it had occurred at the May 1991 meeting. (Kelley, Tr. 2669; 2691).

Response to Finding No. 223: This proposed finding is misleading to the extent it implies that Mr. Kelley's confusion with dates was anything more than a honest mistake with respect to an event that occurred more than twelve years ago. Indeed, when Complaint Counsel

attempted to apprise the Court and Rambus that Mr. Kelley had become confused with respect to the date of the hand vote, Mr. Kelley quickly corrected the date and Rambus summarily rejected any further attempt to clarify the record. *See* Colloquy, Tr. 2687-88.

224. There is no reference to the "hand vote" in the May 1991 or May 1992 JC 42.3 meeting minutes. (Kelley, Tr. 2670; JX 5; CX 34).

Response to Finding No. 224: This proposed finding does not support either the conclusion that the hand vote did not occur or the conclusion that the JEDEC patent policy did not require disclosure of patent applications prior to May 1991. Because JEDEC's patent policy had always included a requirement to disclose patent applications (*see* CCFF 320), it is likely that the secretary of the meeting (who is a JEDEC employee) did not regard the hand vote as a substantive event. It is worth noting that the hand vote in the March 1994 meeting also was not recorded in the minutes, although the minutes do reflect the conclusion that the Committee felt that the JEDEC disclosure policy was clear. (JX0019 at 4-5 ("The Committee was asked if the policy is clear. The Committee felt it was clear."); *see* CCFF 985).

225. Mr. Kelley agreed that it was "important" that the meeting minutes reflect that this policy change had occurred. He stated that he did not know why the "hand vote" was not mentioned in the minutes. (Kelley, Tr. 2670).

Response to Finding No. 225: This proposed finding does not support either the conclusion that the hand vote did not occur or the conclusion that the JEDEC patent policy did not require disclosure of patent applications prior to May 1991. Because JEDEC's patent policy had always included a requirement to disclose patent applications (*see* CCFF 320), it is likely that the secretary of the meeting (who is a JEDEC employee) did not regard the hand vote as a substantive event.

226. Mr. Kelley did not mention the "hand vote" in his IBM trip report for the May 1991 JEDEC meeting. (Kelley, Tr. 2675-6).

Response to Finding No. 226: Complaint Counsel does not disagree. This proposed finding does not support either the conclusion that the hand vote did not occur or the conclusion that the JEDEC patent policy did not require disclosure of patent applications prior to May 1991.

227. Mr. Kelley testified that there was a separate "hand vote" on the same issue at the JC 16 meeting in May 1991, although he later qualified this to say that he "believe[d]" there was a separate vote in the JC 16 meeting. (Kelley, Tr. 2670, 2676).

Response to Finding No. 227: Complaint Counsel does not disagree.

228. There was no written evidence presented at trial that a "hand vote" relating to the disclosure of patent applications ever occurred in a JC 42.3 or JC 16 meeting.

Response to Finding No. 228: This proposed finding does not support either the conclusion that the hand vote(s) did not occur or the conclusion that the JEDEC patent policy did not require disclosure of patent applications prior to May 1991. Because JEDEC's patent policy had always included a requirement to disclose patent applications (*see* CCFF 320), it is likely that the secretary of the meeting(s) (who is a JEDEC employee) did not regard the hand vote as a substantive event. It is worth noting that the hand vote in the March 1994 meeting also was not recorded in the minutes, although the minutes do reflect the conclusion that the Committee felt that the JEDEC disclosure policy was clear. (JX0019 at 4-5 ("The Committee was asked if the policy is clear. The Committee felt it was clear."); *see* CCFF 985).

229. No witness other than Mr. Kelley testified that a "hand vote" relating to the disclosure of patent applications had ever occurred in a JC 42.3 or JC 16 meeting.

Response to Finding No. 229: This proposed finding is misleading and incomplete because no other witness was questioned concerning a hand vote at either the JC-42.3 meeting or the JC-16 meeting. A number of witnesses, including witnesses called by Rambus, were present at the May 1991 JC-42.3 meeting and could have been asked questions relating to this issue. *See* JX0005 at 1-2 (listing Alan Grossmeier, Farhad Tabrizi, Howard Sussman, Desi Rhoden, Mark

Kellogg, and Betty Prince as present). In addition, the following witnesses who were on Rambus's final witness list whom Rambus failed to call also were present: David Chapman, Gil Russell, Ernest Powell, Ken McGhee, and Joel Karp. (JX0005 at 1-2).

230. The complete absence of corroborating evidence of a "hand vote" regarding the disclosure of patent applications renders Mr. Kelley's testimony on that issue not credible.

Response to Finding No. 230: This proposed finding is misleading and incomplete because no other witness was questioned by Rambus in order to corroborate or contradict Mr. Kelley's testimony that a hand vote occurred at the JC-42.3 meeting or the JC-16 meeting. A number of witnesses, including witnesses called by Rambus, were present at the May 1991 JC-42.3 meeting and could have been asked questions relating to this issue. *See* JX0005 at 1-2 (listing Alan Grossmeier, Farhad Tabrizi, Howard Sussman, Desi Rhoden, Mark Kellogg, and Betty Prince as present). In addition, the following witnesses who were on Rambus's final witness list whom Rambus failed to call also were present: David Chapman, Gil Russell, Ernest Powell, Ken McGhee, and Joel Karp. *Id.* The hand vote regarding the JEDEC disclosure policy taken under similar circumstances at the March 1994 committee meeting (CCFF 985) renders Mr. Kelley's testimony very credible.

231. There was also no evidence presented at trial that anyone ever mentioned the alleged "hand vote" to Rambus or in its presence. Rambus was not a JEDEC member when the "hand vote" supposedly occurred.

Response to Finding No. 231: This proposed finding is irrelevant because Rambus was informed of the obligation to disclose patents and patent applications in the same manner as every other member of JEDEC. *See* CCFF 357-418. The overwhelming weight of the evidence indicates that Rambus representatives understood that the JEDEC disclosure obligation applied to both patents and patent applications. *See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of the 21-I Manual] in 1995? A: I had made a request to be given whatever

kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); *see also* CX0685 at 1 (Mooring e-mail, 12/11/92: IBM stated that some "offenders" had "patents pending" on SDRAMs that they had not made the Committee aware of).

4. Complaint Counsel Did Not Prove That JEDEC Manual 21-I Ever Became Effective.

232. Although JEDEC manual 21-I refers, indirectly, to an obligation to disclose information regarding both patents and "pending patents," Complaint Counsel did not meet their burden of showing that the 21-I manual had ever become effective. (CX 208 at 19; Kelley, Tr. 2105). *See* Findings, ¶¶ 165-169.

Response to Finding No. 232: This proposed finding is incorrect to the extent that it suggests that the obligation to disclose patent applications articulated in the 21-I manual is indirect. The JEDEC Manual of Organization and Procedure states that it is the "obligation of all participants to inform the meeting of any knowledge they may have of any patents, or *pending patents*, that might be involved in the work they are undertaking." (CX0208 at 19). In addition, RPF 232 constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Furthermore, RPF 121 is contrary to the weight of the evidence. *See* CCFF 403-18; CCRF 118.

Furthermore, the overwhelming weight of the evidence indicates that Rambus representatives understood that the JEDEC disclosure obligation applied to both patents and patent applications. *See* CX2104 at 851-53 (Crisp, Dep.) ("Q: And how did you come to get that copy [of

the 21-I Manual] in 1995? A: I had made a request to be given whatever kind of manual they must have had there for members that outlined what the patent policy was"; Crisp understood from the 21-I Manual that JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC"); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); *see also* CX0685 at 1 (Mooring e-mail, 12/11/92: IBM stated that some "offenders" had "patents pending" on SDRAMs that they had not made the Committee aware of).

5. The February 2000 Meeting Of The JEDEC Board Of Directors Shows That Disclosure Of Patent Applications Was Not Required.

233. Substantial evidence that JEDEC did not, in fact, require the disclosure of patent applications is found in the official minutes of the February 2000 meeting of the JEDEC Board of Directors. (RX 1570 at 13).

Response to Finding No. 233: This proposed finding is incomplete, unreliable, inaccurate, misleading, and does not support the conclusion that the JEDEC patent policy did not require the disclosure of patent applications. As an initial matter, RX1570 is not the official minutes of the February 2000 meeting, because they are not the minutes approved by EIA Legal Counsel or the JEDEC Chairman. *See, e.g.,* CX0206 at 6 ("approval is required from the EIA Legal Counsel on minutes of meetings before circulation"). In an effort to mislead Your Honor, Rambus selected a discredited draft of the minutes as an exhibit and failed to ask any questions of any witness concerning the drafting of the minutes. In addition, although the approved minutes were the subject of extensive discovery, Rambus chose to not admit them into evidence.

On January 28, 2000, Micron disclosed (as it was obligated to do) a patent application relating to a proposed standard under consideration in the JC-42.4 subcommittee. (RX1559 at 2).

On February 1, 2000, Mr. McGhee sent an email to members of the subcommittee stating "I would like to point out that this letter is well intentioned, but lacks a patent number, so it does not complete the requirements for JEDEC patent policy. If, however, a follow-up letter is issued after the patent is issued, then it would comply with JEDEC's patent policy." (RX1559 at 1). Upon receiving Mr. McGhee's email that Micron had not complied with the patent policy because Micron's disclosure did not include an application number, Mr. Walther of Micron caused the matter to be placed on the agenda for the next JEDEC board meeting. (RX1568 at 25). Logically, because patent applications do not have patent numbers, the lack of a patent number cannot be the basis for holding a member in violation of the disclosure policy. This was the issue discussed at the February 2000 board meeting (RX1568 at 25) and Your Honor would have this information had Respondent chosen to ask a single question of any witness who was present or sought to admit the approved minutes of that meeting. Finally, the Federal Circuit has held against Rambus on this very issue and found that disclosure of relevant patent information was an obligation of JEDEC participants. *Rambus, Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1098 (Fed. Cir. 2003).

In any event, this ambiguous, discredited draft document from 2000, unsupported by any witness testimony, cannot overcome the overwhelming weight of the evidence that the JEDEC policy created an obligation to disclose patent applications as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378

(including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

234. The minutes of the February 2000 meeting of the JEDEC Board of Directors state as follows:

> "D. Disclosure on Patents Pending
>
> Mr. Walther noted that Micron had sent a letter indicating they have patents pending on items that may affect committee standards. The issue was whether companies should make public that a patent is pending. The BoD discussed it and noted they encourage companies to make this kind of disclosures even though they were not required by JEDEC bylaws."

(RX 1570 at 13).

Response to Finding No. 234: This proposed finding is incomplete, unreliable, inaccurate, misleading, and does not support the conclusion that the JEDEC patent policy did not require the disclosure of patent applications. As an initial matter, Rambus has failed to inform Your Honor that RX1570 are not the minutes approved by the EIA Legal Counsel or the JEDEC Chairman. In an effort to mislead Your Honor, Rambus selected a discredited draft of the minutes as an exhibit and failed to ask any questions of any witness concerning the drafting of the minutes. In addition, although the approved minutes were the subject of extensive discovery, Rambus chose to not admit them into evidence. *See also* CCRF 233.

In any event, this ambiguous, discredited draft document from 2000, unsupported by any witness testimony, cannot overcome the overwhelming weight of the evidence that the JEDEC policy created an obligation to disclose patent applications as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356

(draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

235. The February 2000 Board minutes state unambiguously that a disclosure by a JEDEC member "that a patent is pending" is "not required by JEDEC bylaws." (RX 1570 at 13). Such a disclosure is instead "encouraged." (*Id.*).

Response to Finding No. 235: This proposed finding is incomplete, unreliable, inaccurate, misleading, and does not support the conclusion that the JEDEC patent policy did not require the disclosure of patent applications. As an initial matter, Rambus has failed to inform Your Honor that RX1570 are not the minutes approved by the EIA Legal Counsel or the JEDEC Chairman. In an effort to mislead Your Honor, Rambus selected a discredited draft of the minutes as an exhibit and failed to ask any questions of any witness concerning the drafting of the minutes. In addition, although the approved minutes were the subject of extensive discovery, Rambus chose to not admit them into evidence. *See also* CCRF 233.

In any event, this ambiguous, discredited draft document from 2000, unsupported by any witness testimony, cannot overcome the overwhelming weight of the evidence that the JEDEC policy created an obligation to disclose patent applications as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378

(including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

236. Although this JEDEC Board meeting occurred in 2000, no witness testified that JEDEC had *lessened* the disclosure obligations contained in the JEDEC patent policy after Rambus left JEDEC. These Board minutes are, therefore, substantial evidence that JEDEC encouraged, but did not require, the disclosure of patent applications while Rambus was a member.

Response to Finding No. 236: This proposed finding is misleading and incomplete because no witness was *asked* this question. Further, no witness was asked *any* questions relating to the 2000 board minutes. There is no discussion whatsoever of RX1570 anywhere in the record.

In any event, this ambiguous, discredited draft document from 2000, unsupported by any witness testimony, cannot overcome the overwhelming weight of the evidence that the JEDEC policy created an obligation to disclose patent applications as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley)

237. In an e-mail written a few days after the February 2000 board meeting, JEDEC Secretary Ken McGhee, who had been present at the meeting (RX 1570 at 2), reported to a JEDEC subcommittee that the JEDEC Board had discussed Micron's "patent pending" disclosure "at their February 8 meeting." (RX 1585 at 1). Secretary McGhee stated that:

> "The JEDEC patent policy concerns items that are known to be patented that are included in JEDEC standards. Disclosure of

> patents is a very big issue for Committee members and cannot be required of members at meetings. However, if a company gives early disclosure on a patent they are working on, it definitely gives a lot of assurance to the Committee members regarding development of any standards affecting it.
>
> Therefore, in Micron's letter, *by giving early disclosure, they have gone one step beyond the patent policy and have complied with the spirit of the law. JEDEC encourages this type of activity from any member*."

(RX 1585 at 1) (emphasis added).

Response to Finding No. 237: This proposed finding is misleading and incomplete. On January 28, 2000, Micron drafted a written disclosure of a patent application relating to a proposed standard under consideration in the JC-42.4 subcommittee. (RX1559 at 2). On February 1, 2000, Mr. McGhee sent an email to members of the subcommittee stating "I would like to point out that this letter is well intentioned, but lacks a patent number, so it does not complete the requirements for JEDEC patent policy. If, however, a follow-up letter is issued after the patent is issued, then it would comply with JEDEC's patent policy." (RX1559 at 1). Upon receiving Mr. McGhee's email that Micron had not complied with the patent policy because Micron's disclosure did not include an application number, Mr. Walther of Micron caused the matter to be placed on the agenda for the next JEDEC board meeting. (RX1568 at 25). Logically, because patent applications do not have patent numbers, the lack of a patent number cannot be the basis for holding a member in violation of the disclosure policy.

Mr. McGhee's subsequent email (RX1585) was written for the purpose of attempting to clarify to the committee that his earlier email stating that Micron had not complied with the patent policy because it lacked a patent number was in error. In that email, Mr. McGhee noted that Micron's written disclosure, which came after its oral disclosure at a JEDEC meeting, was "one step beyond" the patent policy. As Mr. Kelly testified, a company can "fully comply with its

disclosure obligation by providing an oral explanation to the relevant EIA or JEDEC committee", and that if a company "orally discloses a patent or patent application" and follows up "by sending a letter making disclosures in writing" it would "be going beyond" what JEDEC's rules actually require. (J. Kelly, Tr. 2004-05).

In addition, Mr. McGhee was listed on Rambus's final witness, list and scheduled to testify on July 28, 2003, until Rambus refused to call him. Moreover, Rambus did not ask a single witness to testify concerning the receipt of this email or their understanding of what it conveyed, notwithstanding the fact that Desi Rhoden and John Kelly also were present at the meeting. (RX1570 at 1-2).

In any event, this ambiguous, discredited draft document from 2000, unsupported by any witness testimony, cannot overcome the overwhelming weight of the evidence that the JEDEC policy created an obligation to disclose patent applications as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley).

238. Secretary McGhee's February 11, 2000 e-mail corroborates the minutes of the February 2000 JEDEC Board meeting and provides further evidence that disclosure of patent applications was encouraged but not required.

Response to Finding No. 238: This proposed finding is misleading and does not support the conclusion that disclosure of patent applications at JEDEC was not mandatory

because, as indicated above, RX1570 is not the approved minutes of the February 2000 JEDEC board of directors meeting. *See* CCRF 233. In addition, RPF 238 is incomplete and unreliable because there is no testimony to support Rambus's interpretation of the document. *See* CCRF 237.

In any event, this ambiguous, discredited draft document from 2000, unsupported by any witness testimony, cannot overcome the overwhelming weight of the evidence that the JEDEC policy created an obligation to disclose patent applications as well as patents. CX0208 at 19 (21-I Manual: obligation to disclose "patents, or pending patents"); CX0042A at 7 (Townsend memorandum: "EIA rules governing patentable matters," obligation to indicate "the intent of your company to patent or not patent the subject matter"); CX0336 (same); CX0342 (same); CX0347 (same); CX0306 at 1 (sign-in sheet: subjects involving "patentable or patented item"); RX0356 (draft JEDEC minutes regarding Townsend presentation: "members are cautioned to disclose their relevant patent applications"); CCFF 319-20, 324, 331, 335, 339, 363, 366, 367, 370, 378 (including testimony of Messrs. Kelly, Rhoden, Lee, Sussman, Landgraf, Williams, Brown, Calvin, Meyer and Kelley). Finally, the Federal Circuit has held against Rambus on this very issue and found that disclosure of relevant patent information was an obligation of JEDEC participants. *Rambus, Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1098 (Fed. Cir. 2003).

6. The Disclosures That Were *Not* Made By JEDEC Members In The Early And Mid-1990s Are Further Evidence That JEDEC Members Did Not Understand That Patent Applications Had To Be Disclosed.

239. The behavior of JEDEC members also makes clear that many members did not understand that they were obligated to disclose patent applications that were related to JEDEC standard-setting work.

Response to Finding No. 239: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel

submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

240. For example, a Hewlett-Packard representative to JEDEC, Mr. Hans Wiggers, testified that he had attended a JEDEC meeting where IBM representative Gordon Kelley:

> "said 'Look, I cannot disclose – my company would not let me disclose all the patents that IBM is working on because, you know, I just can't do that. The only thing we will do is we will follow the JEDEC guidelines and – or rules on whatever and we will make them available.'"

(Wiggers, Tr. 10592-93).

Response to Finding No. 240: This proposed finding is unreliable, contrary to the weight of the evidence and does not support the conclusion that JEDEC members dis not understand that the JEDEC patent policy included a requirement to disclose patent applications. First, Hewlett-Packard's official representative to JEDEC during the relevant time period, Thomas Landgraf, testified that disclosure of patent applications was required. (Landgraf, Tr. 1693-94). Second, the JEDEC Manual of Organization and Procedure makes it explicit that disclosure of pending patents is an obligation of all participants. *See* CCFF 319. Further, numerous other witnesses testified that the disclosure of patent applications was required. *See* CCFF 320. Further, Rambus understood that the disclosure of patent applications was mandatory. *See* CCFF 841-46 (noting, *inter alia*, that Mr. Crisp received a copy of the 21-I Manual and understood that it required the disclosure of patent applications). Finally, the Federal Circuit has held against Rambus on this very issue and found that disclosure of relevant patent applications was an obligation of JEDEC participants. *Rambus, Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1098 (Fed. Cir. 2003).

241. Mr. Wiggers testified that when Mr. Kelley stated his position at the JEDEC meeting regarding IBM's non-disclosure of patent applications, Mr. Wiggers told the meeting attendees that HP took the same position. (Wiggers, Tr. 10593-4).

Response to Finding No. 241: This proposed finding is unreliable because, as noted previously, Mr. Kelley committed that IBM would disclose patents and patent applications of which its JEDEC participants were aware and that IBM would evaluate any other patents or patent applications that other JEDEC participants brought to the attention of IBM representatives. Moreover, the evidence shows that IBM fulfilled this commitment. *See* CCRF 192-97.

242. In numerous other instances, although named inventors on patent applications were present at JEDEC meetings while standards relating to those applications were being discussed, the inventors did not disclose their patent applications.

Response to Finding No. 242: This proposed finding lacks any reference to the record. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

a. Members of the SyncLink Consortium Did Not Disclose Pending Patent Applications.

243. On May 24, 1995, Hyundai and Mitsubishi made presentations at a meeting of the JC-42.3 subcommittee regarding a type of DRAM known as SLDRAM. (JX 26 at 10-11; Rhoden, Tr. 469-71). The minutes note that "[t]he proposal was brought to JEDEC for a pinout standard." (JX 26 at 10). The Mitsubishi presentation showed the pinout for an SLDRAM. (JC 26 at 111; Rhoden, Tr. 471).

Response to Finding No. 243: Complaint Counsel does not disagree.

244. At a JEDEC meeting on December 9-10, 1997, the SLDRAM pinout standard ballot was approved by the JC-42.3 subcommittee. (JX 41 at 22, 24; RX 1114 at 1; Rhoden, Tr. 1206-08).

Response to Finding No. 244: Complaint Counsel does not disagree.

245. United States Patent No. 6,442,644 issued on August 27, 2002. (RX 2086 at 1). Among the inventors named on the patent were JEDEC representatives Hans Wiggers of Hewlett-Packard, Kevin Ryan and Terry Lee of Micron, and Desi Rhoden, formerly of VLSI. (RX 2086 at 1). Claim 3 of the patent claims the precise SLDRAM pinout that had been standardized by JEDEC. (RX 2086 at 41; Rhoden, Tr. 1211).

Response to Finding No. 245: Complaint Counsel does not disagree.

246. The ’644 patent claims priority to a number of provisional applications, including provisional application 60/069,092 which was filed on December 10, 1997, the very same day that the JEDEC meeting approving the SLDRAM patent was being held. (RX 2086 at 1; RX 2099-43). The ’092 provisional application discloses the SLDRAM pinout claimed in the ’644 patent. (RX 2099-43 at 250).

Response to Finding No. 246: Complaint Counsel does not disagree.

247. Messrs. Wiggers, Ryan and Rhoden were all present at the December 1997 JC-42.3 subcommittee meeting where the SLDRAM pinout standard was balloted and approved. (JX 41 at 2). They were each involved in or affiliated with the “SLDRAM Consortium” or SLDRAM Inc., which became AMI2, to whom the ’644 patent has been assigned. (RX 870 at 1; Rhoden, Tr. 696-97, 1235; RX 2086 at 1). The minutes of the meeting do not indicate that any of the three disclosed the ’092 provisional application. (JX 41 at 22, 24).

Response to Finding No. 247: This proposed finding is incomplete and misleading to the extent that it suggests that persons connected with SLDRAM did not disclose patent applications to JEDEC. As Mr. Rhoden testified, his recollection was that Mr. Peter Gillingham made the first disclosure of SLDRAM or SyncLink intellectual property to JEDEC. (Rhoden, Tr. 723, 1212). In addition, Mr. Rhoden testified that he also made disclosures to JEDEC. (Rhoden, Tr. 1212). There are other instances in which the minutes do not record disclosure of patent applications. Indeed, the Rambus representative himself observed and recorded disclosures of patent applications that were not recorded in the minutes. At the February 1992 JC-42.3 meeting Fujitsu disclosed a patent application relating to a 16Mb DRAM in a VSMP package. Respondent’s representative, Billy Garrett, reported Fujitsu’s discloure to executives at Rambus. (CX00672 at 1 (“INTERESTING TID-BIT . . Fujitsu indicated that they do have patents applied for, but that they will comply with the JEDEC requirements to make it a standard.”)). Much like the SLDRAM disclosure, the Fujitsu disclosure was not recorded in the minutes by the secretary of the meeting. (JX0012 at 11).

Further, Complaint Counsel also agrees with the logical conclusion of this proposed finding that the duty to disclose is triggered by the subjective knowledge or belief of a reasonable

engineer, such as Messrs. Rhoden, Wigger, Ryan or Mr. Crisp, as to the relationship between content of the patent application and the work of the JEDEC committee. As RPF 247 suggests, disclosure is not triggered by a finding (after expert testimony from patent lawyers) that the proposed standard does, in fact, infringe the patent application.

b. Fujitsu Did Not Disclose Pending Patent Applications.

248. The Complaint in this matter alleges that Rambus should have disclosed pending patent claims to "on-chip PLL/DLL technology" and that such technology was ultimately incorporated into the DDR SDRAM standard that was adopted in August 1999. (Complaint at 64).

Response to Finding No. 248: Complaint Counsel does not disagree.

249. The Court has taken official notice of United States Patent No. 6,028,816, which issued on February 22, 2000 and is assigned to Fujitsu. The application for the '816 patent was filed on September 5, 1997 (although the patent claims priority back to a number of Japanese patent applications filed earlier in 1997 and in 1996). ('816 patent at 1). The '816 patent has claims directed to a semiconductor device, such as a DRAM, with "an input timing adjusting circuit" for receiving an external clock signal and outputting and adjusting the phase of an internal clock signal. ('816 patent at 101).

Response to Finding No. 249: This proposed finding lacks any reference to the record and encompasses legal conclusions. Therefore, RPF 249 is inappropriate for findings of fact. Respondent did not present expert testimony to support a finding that U.S. Patent No. 6,028,816 might involve the work of JEDEC. Furthermore, Respondent did not present ay secondary evidence that Fujitsu or anyone else believed that the '816 patent might involve the work of JEDEC.

The interpretation of patent claims involving complex technology, and the comparison of a product or potential product to that claim, cannot properly be resolve without the development of evidence, inlcuding expert testimony, before the finder of fact. *See NeoMagic Corp. v. Trident Microsystems, Inc.*, 287 F.3d 1062, 1074 (Fed. Cir. 2002) ("given the complex technology involved in this case, we think this matter [interpretation of a claim to a DRAM memory chip controller] can only be resolved by further evidentiary hearings, including expert testimony, before

the district court."). A determination that a patent claim covers a product is a two step process. The first step requires that the court interpret the patent claim as it would be understood by a person of ordinary skill in the art as a question of law. RPF 249 cites no expert testimony or other evidence to establish the proper interpretation of the patent claims.

The second step requires a factual determination that each element of the properly interpreted claim is present in the product. (Nusbaum, Tr. 1565-66). RPF 249 cites no expert testimony or other evidence to establish that each element of any claim of this patent correspond to elements of the proposed alternative.

The Court's judicial notice of this patent, without evidence supporting a proper claim interpretation and infringement analysis, is insufficient to support the finding because the Court has "decline[d] to take official notice of what the patents in question relate to or cover, and decline[d] to engage in any analysis or interpretation of the substance or content" of the patent. *See* Order on Respondent's Request for Official Notice at 3 (August 27, 2003). Complaint Counsel submits that this finding should be disregarded pursuant to Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

250. As Complaint Counsel's technical expert, Professor Bruce Jacob explained in the context of describing an NEC presentation, a PLL is a timing adjustment circuit that "can be used to synchronize an external clock and an internal clock." (Jacob, Tr. 5533-34).

Response to Finding No. 250: Complaint Counsel does not disagree. However, this proposed finding does not support the conclusion that Fujitsu did not disclose a relevant patent application. *See* CCRF 249.

251. One of the inventors of the '816 patent, Masao Nakano, was present at meetings 81-85, spanning December 11, 1996 through December 9, 1997, of the JEDEC 42.3 Subcommittee. (JX 35 at 2; JX 36 at 2; JX 38 at 2; JX 40 at 2; JX 41 at 2). On-chip PLLs or DLLs were discussed at these meetings. For example, at the December 1996 meeting, Fujitsu made a presentation on DDR SDRAMs including an "internal DLL circuit." (JX 35 at 34). However, the minutes do not reflect that Mr. Nakano disclosed his pending patent application.

Response to Finding No. 251: This proposed finding does not support the conclusion that Fujitsu did not disclose a relevant patent application. First, there is no record evidence that the patent application was relevant to JEDEC's work. *See* CCRF 249. Indeed it appears that the patent application was *not* related to the JEDEC work, as there is no evidence that Fujitsu ever sought to enforce a patent against any JEDEC-compliant product. Second, if the

patent was relevant, there is no record evidence that it was not disclosed. Many disclosures were not recorded in the minutes. CCRF 247. In addition, RPF 251 is incomplete because there it contains no citation to any evidence of the subjective knowledge or belief of Mr. Nakano or any other Fujitsu employee concerning the relationship (if any) between the '816 patent and the work of any JEDEC committee. RPF 251 also ignores substantial evidence of Fujitsu's disclosure of patent applications to JEDEC during Rambus's tenure as a member. At the February 1992 JC-42.3 meeting Fujitsu disclosed a patent application relating to a 16Mb DRAM in a VSMP package. (CX00672 at 1 ("INTERESTING TID-BIT . . Fujitsu indicated that they do have patents applied for, but that they will comply with the JEDEC requirements to make it a standard." recorded in notes of Billy Garrett of Rambus)). This disclosure was not recorded in the minutes. *See* (JX0012 at 11). Also, at the May 1992 JC-42.3 meeting, Fujitsu disclosed pending patents on its LOC package proposal. The motion to ballot the proposal failed. (CX0034 at 7). In addition, at the September 1995 JC-16 meeting, Fujitsu disclosed a patent application relating to SSTL. (CX0711 at 169 (notes of Richard Crisp)). There also is no record of this disclosure of a patent application in any minutes.

Complaint Counsel does agree with the logical conclusion of RPF 251 that the duty to disclose is triggered by the subjective knowledge or belief of a reasonable engineer, such as Mr. Nakano or Mr. Crisp, as to the relationship between content of the patent application and the work of the JEDEC committee. As RPF 251 suggests, disclosure is not triggered by a finding (after expert testimony from patent lawyers) that the proposed standard does, in fact, infringe the patent application.

c. <u>IBM Did Not Disclose Pending Patent Applications</u>.

252. The Court has taken official notice of United States Patent No. 6,289,413, which issued on September 11, 2001 and is assigned to IBM. The '413 patent claims priority to an application filed on October 18, 1996. ('413 patent at 1). Claim 1 of the '413 patent claims a

"cached SDRAM" device including means for programming the device to operate in "Write Transfer mode" or "No Write Transfer mode" during a write cycle. ('413 patent at 21).

Response to Finding No. 252: This proposed finding lacks any reference to the record and encompasses legal conclusions. Therefore, RPF 252 is inappropriate for findings of fact. Respondent did not present expert testimony to support a finding that U.S. Patent No. 6,289,413 might involve the work of JEDEC. Furthermore, Respondent did not present ay secondary evidence that IBM or anyone else believed that the '413 patent might involve the work of JEDEC.

The interpretation of patent claims involving complex technology, and the comparison of a product or potential product to that claim, cannot properly be resolve without the development of evidence, inlcuding expert testimony, before the finder of fact. *See NeoMagic Corp. v. Trident Microsystems, Inc.*, 287 F.3d 1062, 1074 (Fed. Cir. 2002) ("given the complex technology involved in this case, we think this matter [interpretation of a claim to a DRAM memory chip controller] can only be resolved by further evidentiary hearings, including expert testimony, before the district court."). A determination that a patent claim covers a product is a two step process. The first step requires that the court interpret the patent claim as it would be understood by a person of ordinary skill in the art as a question of law. RPF 252 cites no expert testimony or other evidence to establish the proper interpretation of the patent claims.

The second step requires a factual determination that each element of the properly interpreted claim is present in the product. (Nusbaum, Tr. 1565-66). RPF 252 cites no expert testimony or other evidence to establish that each element of any claim of this patent correspond to elements of the proposed alternative.

The Court's judicial notice of this patent, without evidence supporting a proper claim interpretation and infringement analysis, is insufficient to support the finding because the Court

has "decline[d] to take official notice of what the patents in question relate to or cover, and decline[d] to engage in any analysis or interpretation of the substance or content" of the patent. *See* Order on Respondent's Request for Official Notice at 3 (August 27, 2003). Complaint Counsel submits that this finding should be disregarded pursuant to Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

253. At meeting No. 86 of the JEDEC JC-42.3 Subcommittee on March 3, 1998, a "No Write Transfer mode" for a cached SDRAM known as ESDRAM was balloted. (JX 42 at 10). The "No Write Transfer mode" was ultimately incorporated into the JEDEC standard for ESDRAM – Section 3.11.5.3.5 of standard 21-C provides for a programming such a mode in which write data is not written to the cache. (CX 234 at 180).

Response to Finding No. 253: Complaint Counsel does not disagree.

254. Jim Rogers, one of the inventors of the '413 patent, was present during meeting No. 86, but the minutes do not reflect that he disclosed his pending application. (JX 42 at 2, 10).

Response to Finding No. 254: This proposed finding does not support the conclusion that IBM did not disclose a relevant patent application. First, there is no record evidence that the patent application was relevant to JEDEC's work. *See* CCRF 251. Indeed it appears that the patent application was *not* related to the JEDEC work, as there is no evidence that IBM ever sought to enforce a patent against any JEDEC-compliant product. Second, if the patent was relevant, there is no record evidence that it was not disclosed. Many disclosures were not recorded in the minutes. CCRF 247. In addition, RPF 254 is incomplete because there it contains no citation to any evidence of the subjective knowledge or belief of Mr. Rogers or any other JEDEC participant concerning the relationship (if any) between the '413 patent and the work of any JEDEC committee.

RPF 254 also ignores substantial evidence that IBM did disclose patent applications to JEDEC during the time that Rambus participated in JEDEC. For example, at the September 1991 JC-42.5 meeting, Mark Kellogg of IBM made a presentation concerning an eight-byte SIMM

module. (CX0021 at 43; Kellogg, Tr. 5030-31). Mr. Kellogg's eight-byte SIMM proposal originated from IBM's personal computer division. (Kellogg, Tr. 5031). Personnel in the personal computer division requested that Mr. Kellogg propose an eight-byte memory module that the personal computer division was considering using in some of its future products. (Kellogg, Tr. 5031). Mr. Kellogg asked the engineers in the personal computer division whether they had any patent activity planned related to the eight-byte SIMM proposal. (Kellogg, Tr. 5031-32). The engineers informed Mr. Kellogg that IBM did have patent activity related to the eight-byte SIMM proposal. (Kellogg, Tr. 5032). As of September 1991, IBM had not yet filed any patent application relating to the eight-byte SIMM proposal. (Kellogg, Tr. 5032). The fact that IBM had patent activity that related to the eight-byte SIMM proposal affected Mr. Kellogg's proposal and disclosures within JEDEC. (Kellogg, Tr. 5032). IBM wanted to disclose to JEDEC the full details of the eight-byte SIMM proposal, including the fact that "potential patent issues" needed to be resolved prior to showing. (CX0021 at 45; Kellogg, Tr. 5032-33). Mr. Kellogg warned the committee of expected or planned patent activity within IBM Corporation associated with the material that he was showing. (Kellogg, Tr. 5033).

Mr. Kellogg made another presentation of the eight-byte SIMM proposal at the December 1991 JC-42.5 committee meeting. (JX0009 at 21; Kellogg, Tr. 5034). Mr. Kellogg informed the committee that IBM had a patent application on the eight-byte SIMM product proposal for which no final determination has been made regarding the breadth of claims nor the final disposition of the application. (JX0009 at 23; Kellogg, Tr. 5035-36). Although Mr. Kellogg's written presentation stated that IBM had a patent application on the eight-byte SIMM proposal, no application had been filed as of time of the meeting. (Kellogg, Tr. 5036; G. Kelley, Tr. 2345). Thus, IBM disclosed the *patentable* material to JEDEC even prior to filing the patent application. At the February 1992 JC-42.5 meeting, Mr. Kellogg presented a revised eight-byte SIMM

proposal. (CX0030 at 6; Kellogg, Tr. 5039-40). The changes in the February eight-byte presentation had compared to the previous presentations made it such that the patent activity that Mr. Kellogg disclosed in September 1991 and December 1991 no longer applicable. (CX0030 at 6; Kellogg, Tr. 5039-40). Mr. Kellogg informed the committee that the IBM patent application related to a 180-pin version of the device, but not the 162-pin version of the device. (CX0030 at 6; Kellogg, Tr. 5040-41).

Complaint Counsel does agree with the logical conclusion of RPF 254 that the duty to disclose is triggered by the subjective knowledge or belief of a reasonable engineer, such as Mr. Rogers or Mr. Crisp, as to the relationship between content of the patent application and the work of the JEDEC committee. As RPF 254 suggests, disclosure is not triggered by a finding (after expert testimony from patent lawyers) that the proposed standard does, in fact, infringe the patent application.

d. Micron Did Not Disclose Pending Patent Applications.

255. The Court has taken official notice of United States Patent No. 5,526,320, entitled "Burst EDO Memory Device," which issued on June 11, 1996 and is assigned to Micron. The application for the '320 patent, application serial no. 370,761, was filed on December 23, 1994. ('320 patent at 1). Approximately 20 patents have issued that claim priority to the '761 application. (Williams, Tr. 934).

Response to Finding No. 255: Complaint Counsel does not disagree.

256. In connection with the prosecution of the '320 patent, Micron submitted to the Patent and Trademark Office a JEDEC presentation by OKI Electronics Industries in September 1994 and another JEDEC presentation by Toshiba in December 1994 as material to the application. (Williams, Tr. 926–928).

Response to Finding No. 256: Complaint Counsel does not disagree.

257. Brett Williams of Micron put together a presentation on Burst EDO that was presented at a January 1995 JEDEC DRAM Task Group Meeting. (JX 23 at 68-77; Williams, Tr. 825-26). Mr. Williams is an inventor on the '320 patent and was present at the January 1995 meeting. (JX 23 at 1; '320 patent at 1). Mr. Williams was aware that Micron's Burst EDO patent application was not listed on the patent tracking list shown at the January 1995 meeting.

(Williams, Tr. 963-64). Nevertheless, Mr. Williams did not disclose his pending application. (Williams, Tr. 964-65).

Response to Finding No. 257: This proposed finding ignores evidence that Micron did disclose to JEDEC patent applications relating to burst EDO, and agreed to license them on reasonable and non-discriminatory terms. (CX0364 at 1). This proposed finding also ignores substantial evidence that Micron did disclose patent applications to JEDEC both during and after time that Rambus was a JEDEC member. In addition to the April 1996 disclosures (*see* CX0364 at 1), Respondent has discussed extensively (*see* RPF 233-38), Micron's disclosure of a patent application relating to a proposed JC-42.4 standard in January 2000.

Complaint Counsel does agree with the logical conclusion of RPF 257 that the duty to disclose is triggered by the subjective knowledge or belief of a reasonable engineer, such as Mr. Williams or Mr. Crisp, as to the relationship between content of the patent application and the work of the JEDEC committee. As RPF 257 suggests, disclosure is not triggered by a finding (after expert testimony from patent lawyers) that the proposed standard does, in fact, infringe the patent application.

258. Burst EDO was passed unanimously as a JEDEC standard in March 1995. (RX 585 at 1; Williams, Tr. 929-31). Micron did not disclose its pending patent application on Burst EDO in connection with that vote. (RX 585 at 3-4; Williams, Tr. 936-37).

Response to Finding No. 258: This proposed finding ignores evidence that Micron did disclose to JEDEC patent applications relating to burst EDO, and agreed to license them on reasonable and non-discriminatory terms. (CX0364 at 1). This proposed finding also ignores substantial evidence that Micron did disclose patent applications to JEDEC both during and after time that Rambus was a JEDEC member. In addition to the April 1996 disclosures (*see* CX0364 at 1), Respondent has discussed extensively (*see* RPF 233-38), Micron's disclosure of a patent application relating to a proposed JC-42.4 standard in January 2000.

Complaint Counsel does agree with the logical conclusion of RPF 258 that the duty to disclose is triggered by the subjective knowledge or belief of a reasonable engineer, such as Mr. Williams or Mr. Crisp, as to the relationship between content of the patent application and the work of the JEDEC committee. As RPF 258 suggests, disclosure is not triggered by a finding (after expert testimony from patent lawyers) that the proposed standard does, in fact, infringe the patent application.

e. Mitsubishi Did Not Disclose Pending Patent Applications.

259. The Court has taken official notice of United States Patent No. 6,356,484, which issued on March 12, 2002 and is assigned to Mitsubishi. The '484 patent claims priority to an application filed on April 15, 1992. ('484 patent at 1). The '484 patent claims a synchronous memory device that takes "an external signal in response to rising and falling edges of the single clock signal." ('484 patent at 276).

Response to Finding No. 259: This proposed finding lacks any reference to the record and encompasses legal conclusions. Therefore, RPF 259 is inappropriate for findings of fact. Respondent did not present expert testimony to support a finding that U.S. Patent No. 6,356,484 might involve the work of JEDEC. Furthermore, Respondent did not present ay secondary evidence that Mitsubishi or anyone else believed that the '484 patent might involve the work of JEDEC.

The interpretation of patent claims involving complex technology, and the comparison of a product or potential product to that claim, cannot properly be resolve without the development of evidence, inlcuding expert testimony, before the finder of fact. *See NeoMagic Corp. v. Trident Microsystems, Inc.*, 287 F.3d 1062, 1074 (Fed. Cir. 2002) ("given the complex technology involved in this case, we think this matter [interpretation of a claim to a DRAM memory chip controller] can only be resolved by further evidentiary hearings, including expert testimony, before the district court."). A determination that a patent claim covers a product is a two step process. The first step requires that the court interpret the patent claim as it would be understood by a

person of ordinary skill in the art as a question of law. RPF 249 cites no expert testimony or other evidence to establish the proper interpretation of the patent claims.

The second step requires a factual determination that each element of the properly interpreted claim is present in the product. (Nusbaum, Tr. 1565-66). RPF 259 cites no expert testimony or other evidence to establish that each element of any claim of this patent correspond to elements of the proposed alternative.

The Court's judicial notice of this patent, without evidence supporting a proper claim interpretation and infringement analysis, is insufficient to support the finding because the Court has "decline[d] to take official notice of what the patents in question relate to or cover, and decline[d] to engage in any analysis or interpretation of the substance or content" of the patent. *See* Order on Respondent's Request for Official Notice at 3 (August 27, 2003). Complaint Counsel submits that this finding should be disregarded pursuant to Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

260. One of the inventors of the '917 application, Hisashi Iwamoto, attended meeting no. 90 of JEDEC's 42.3 Subcommittee in March 1999. (JX 46 at 2). Although there were numerous presentations related to DDR SDRAMs at that meeting, Mr. Iwamoto did not disclose his pending application. (JX 46 at 9-13, 17-18).

Response to Finding No. 260: This proposed finding does not support the conclusion that Mitsubishi did not disclose a relevant patent application. First, there is no record evidence that the patent application was relevant to JEDEC's work. *See* CCRF 259. Indeed it appears that the patent application was *not* related to the JEDEC work, as there is no evidence that IBM ever sought to enforce a patent against any JEDEC-compliant product. Second, if the patent was relevant, there is no record evidence that it was not disclosed. Many disclosures were not recorded in the minutes. CCRF 247. In addition, RPF 260 is incomplete because there it contains no citation to any evidence of the subjective knowledge or belief of Mr. Iwamoto or any other

Mitsubishi employee concerning the relationship (if any) between the '917 patent and the work of any JEDEC committee.

Complaint Counsel does agree with the logical conclusion of RPF 260 that the duty to disclose is triggered by the subjective knowledge or belief of a reasonable engineer, such as Mr. Iwamoto or Mr. Crisp, as to the relationship between content of the patent application and the work of the JEDEC committee. As RPF 260 suggests, disclosure is not triggered by a finding (after expert testimony from patent lawyers) that the proposed standard does, in fact, infringe the patent application.

f. Samsung Did Not Disclose Pending Patent Applications.

261. United States Patent No. 5,835,956 issued on November 10, 1998 and is assigned to Samsung. (RX 1308). The '956 patent claims priority to a United States application filed on October 4, 1993, and earlier Korean applications dating to October 2, 1992. (RX 1308 at 1). The '956 patent has claims directed at "[a] synchronous memory device capable of receiving latency mode information to select one of a plurality of latency modes." (RX 1308 at 90).

Response to Finding No. 261: This proposed finding encompasses legal conclusions. Therefore, RPF 261 is inappropriate for findings of fact. Respondent did not present expert testimony to support a finding that U.S. Patent No. 5,835,956 might involve the work of JEDEC. Furthermore, Respondent did not present ay secondary evidence that Samsung or anyone else believed that the '956 patent might involve the work of JEDEC.

The interpretation of patent claims involving complex technology, and the comparison of a product or potential product to that claim, cannot properly be resolve without the development of evidence, including expert testimony, before the finder of fact. *See NeoMagic Corp. v. Trident Microsystems, Inc.*, 287 F.3d 1062, 1074 (Fed. Cir. 2002) ("given the complex technology involved in this case, we think this matter [interpretation of a claim to a DRAM memory chip controller] can only be resolved by further evidentiary hearings, including expert testimony, before the district court."). A determination that a patent claim covers a product is a two step process.

The first step requires that the court interpret the patent claim as it would be understood by a person of ordinary skill in the art as a question of law. RPF 261 cites no expert testimony or other evidence to establish the proper interpretation of the patent claims.

The second step requires a factual determination that each element of the properly interpreted claim is present in the product. (Nusbaum, Tr. 1565-66). RPF 261 cites no expert testimony or other evidence to establish that each element of any claim of this patent correspond to elements of the proposed alternative.

Complaint Counsel submits that this finding should be disregarded pursuant to Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

262. The Court has taken official notice of U.S. Patent No. 5,838,990 which claims priority to the same United States and Korean applications as the '956 patent. ('956 patent at 1). Claim 1 of the '990 patent claims a semiconductor memory containing "code registers" which "store a code in response to the mode set signal, wherein the codes determine the operation modes of the semiconductor memory. ('990 patent at 90). Dependent claim 2 of the '990 patent specifies that the codes in the code registers determine "a burst length mode." (*Id.*). Dependent claim 4 of the '990 patent specifies that the codes in the code registers determine "a latency mode." (*Id.*).

Response to Finding No. 262: This proposed finding lacks any reference to the record and encompasses legal conclusions. Therefore, RPF 262 is inappropriate for findings of fact. Respondent did not present expert testimony to support a finding that U.S. Patent No. 5,838,990 might involve the work of JEDEC. Furthermore, Respondent did not present ay secondary evidence that Samsung or anyone else believed that the '990 patent might involve the work of JEDEC.

The interpretation of patent claims involving complex technology, and the comparison of a product or potential product to that claim, cannot properly be resolve without the development of evidence, including expert testimony, before the finder of fact. *See NeoMagic Corp. v. Trident Microsystems, Inc.*, 287 F.3d 1062, 1074 (Fed. Cir. 2002) ("given the complex technology

involved in this case, we think this matter [interpretation of a claim to a DRAM memory chip controller] can only be resolved by further evidentiary hearings, including expert testimony, before the district court."). A determination that a patent claim covers a product is a two step process. The first step requires that the court interpret the patent claim as it would be understood by a person of ordinary skill in the art as a question of law. RPF 262 cites no expert testimony or other evidence to establish the proper interpretation of the patent claims.

The second step requires a factual determination that each element of the properly interpreted claim is present in the product. (Nusbaum, Tr. 1565-66). RPF 262 cites no expert testimony or other evidence to establish that each element of any claim of this patent correspond to elements of the proposed alternative.

The Court's judicial notice of this patent, without evidence supporting a proper claim interpretation and infringement analysis, is insufficient to support the finding because the Court has "decline[d] to take official notice of what the patents in question relate to or cover, and decline[d] to engage in any analysis or interpretation of the substance or content" of the patent. *See* Order on Respondent's Request for Official Notice at 3 (August 27, 2003). Complaint Counsel submits that this finding should be disregarded pursuant to Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

263. SDRAMs have a "mode register" containing binary codes that determine burst length and CAS latency. (JX 56 at 114).

Response to Finding No. 263: Complaint Counsel does not disagree.

264. One of the inventors of the '956 and '990 patents, Yun Ho Choi, attended JC-42.3 meetings at which SDRAMs were discussed in December 1991, February 1992, December 1992, September 1993 and December 1995. (JX 10 at 2; JX 12 at 2; JX 14 at 2; JX 17 at 2; JX 28 at 2). Yet, the minutes do not reflect that Mr. Choi disclosed the existence of his patent applications. As of December 1995, there were no Samsung patents or patent applications listed on the patent tracking list. (JX 28 at 15-18).

Response to Finding No. 264: This proposed finding does not support the conclusion that Samsung did not disclose a relevant patent application. First, there is no record evidence that the patent application was relevant to JEDEC's work. *See* CCRF 261-62. Indeed it appears that the patent application was *not* related to the JEDEC work, as there is no evidence that IBM ever sought to enforce a patent against any JEDEC-compliant product. Second, if the patent was relevant, there is no record evidence that it was not disclosed. Many disclosures were not recorded in the minutes. CCRF 247. In addition, RPF 264 is incomplete because there it contains no citation to any evidence of the subjective knowledge or belief of Mr. Choi or any other Samsung employee concerning the relationship (if any) between the '956 and '990 patents and the work of any JEDEC committee.

Complaint Counsel does agree with the logical conclusion of RPF 264 that the duty to disclose is triggered by the subjective knowledge or belief of a reasonable engineer, such as Mr. Choi or Mr. Crisp, as to the relationship between content of the patent application and the work of the JEDEC committee. As RPF 264 suggests, disclosure is not triggered by a finding (after expert testimony from patent lawyers) that the proposed standard does, in fact, infringe the patent application. In addition, as noted previously, Mr. Townsend's patent tracking list was not a complete listing of all intellectual property disclosed at JEDEC. *See* CCFF 369.

g. Texas Instruments Did Not Disclose Pending Patent Applications.

265. The Court has taken official notice of United States Patent No. 5,808,958 which issued on September 15, 1998 and is assigned to Texas Instruments. The '958 application claims priority to an application filed on April 23, 1991. ('958 patent at 1). The '958 patent has claims directed to a synchronous random access memory with an "output circuit for producing a predetermined number of data bits from the storage cells." ('958 patent at 22).

Response to Finding No. 265: RPF 265 lacks any reference to the record and encompasses legal conclusions. Therefore, RPF 265 is inappropriate for findings of fact.

Respondent did not present expert testimony to support a finding that U.S. Patent No. 5,808,958 might involve the work of JEDEC. Furthermore, Respondent did not present ay secondary evidence that Texas Instruments or anyone else believed that the '958 patent might involve the work of JEDEC.

The interpretation of patent claims involving complex technology, and the comparison of a product or potential product to that claim, cannot properly be resolve without the development of evidence, including expert testimony, before the finder of fact. *See NeoMagic Corp. v. Trident Microsystems, Inc.*, 287 F.3d 1062, 1074 (Fed. Cir. 2002) ("given the complex technology involved in this case, we think this matter [interpretation of a claim to a DRAM memory chip controller] can only be resolved by further evidentiary hearings, including expert testimony, before the district court."). A determination that a patent claim covers a product is a two step process. The first step requires that the court interpret the patent claim as it would be understood by a person of ordinary skill in the art as a question of law. RPF 265 cites no expert testimony or other evidence to establish the proper interpretation of the patent claims.

The second step requires a factual determination that each element of the properly interpreted claim is present in the product. (Nusbaum, Tr. 1565-66). RPF 265 cites no expert testimony or other evidence to establish that each element of any claim of this patent correspond to elements of the proposed alternative.

The Court's judicial notice of this patent, without evidence supporting a proper claim interpretation and infringement analysis, is insufficient to support the finding because the Court has "decline[d] to take official notice of what the patents in question relate to or cover, and decline[d] to engage in any analysis or interpretation of the substance or content" of the patent. *See* Order on Respondent's Request for Official Notice at 3 (August 27, 2003). Complaint

Counsel submits that this finding should be disregarded pursuant to Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

266. SDRAMs have a programmable burst length feature that results in the production of a predetermined number of data bits from the storage cells depending on the value stored in a mode register. (Rhoden, Tr. 380, 392; CX 234 at 150).

Response to Finding No. 266: Complaint Counsel does not disagree.

267. The Court has taken official notice of United States Patent No. 5,982,694, which lists the same inventors as the '958 patent and claims priority to an application filed on October 21, 1994. (RX 2310 at 1). The '694 patent has claims directed to a synchronous random access memory that outputs data on both "the positive-going edge of the system clock signal" and "the negative-going edge of the system clock signal." (RX 2310 at 21-22).

Response to Finding No. 267: This proposed finding lacks any reference to the record and encompasses legal conclusions. Therefore, RPF 266 is inappropriate for findings of fact. Respondent did not present expert testimony to support a finding that U.S. Patent No. 5,982,694 might involve the work of JEDEC. Furthermore, Respondent did not present ay secondary evidence that Texas Instruments or anyone else believed that the '694 patent might involve the work of JEDEC.

The interpretation of patent claims involving complex technology, and the comparison of a product or potential product to that claim, cannot properly be resolve without the development of evidence, including expert testimony, before the finder of fact. *See NeoMagic Corp. v. Trident Microsystems, Inc.*, 287 F.3d 1062, 1074 (Fed. Cir. 2002) ("given the complex technology involved in this case, we think this matter [interpretation of a claim to a DRAM memory chip controller] can only be resolved by further evidentiary hearings, including expert testimony, before the district court."). A determination that a patent claim covers a product is a two step process. The first step requires that the court interpret the patent claim as it would be understood by a person of ordinary skill in the art as a question of law. RPF 267 cites no expert testimony or other evidence to establish the proper interpretation of the patent claims.

The second step requires a factual determination that each element of the properly interpreted claim is present in the product. (Nusbaum, Tr. 1565-66). RPF 267 cites no expert testimony or other evidence to establish that each element of any claim of this patent correspond to elements of the proposed alternative.

The Court's judicial notice of this patent, without evidence supporting a proper claim interpretation and infringement analysis, is insufficient to support the finding because the Court has "decline[d] to take official notice of what the patents in question relate to or cover, and decline[d] to engage in any analysis or interpretation of the substance or content" of the patent. *See* Order on Respondent's Request for Official Notice at 3 (August 27, 2003). Complaint Counsel submits that this finding should be disregarded pursuant to Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

268. DDR SDRAMs output data on both the positive-going, or rising, edge of the system clock signal and the negative-going, or falling, edge of the system clock signal. (Rhoden, Tr. 389).

Response to Finding No. 268: Complaint Counsel does not disagree.

269. Four of the inventors of the '958 and '694 patents, Wilbur Vogley, Anthony Balistreri, Joseph Hartigan, and Roger Norwood, were regular attendees of JC 42.3 subcommittee meetings. For example, Mr. Hartigan, who became Texas Instruments' JEDEC representative, was at various meetings between July 1992 and September 1997. (JX 13 at 2; JX 40 at 1) Mr. Vogley was at a number of meetings including March 1995 and March 1996. (JX 25 at 2; JX 31 at 2). Neither the various meeting minutes nor the patent tracking list reflect the disclosure of the applications that led to the '958 and '964 patents. (JX 28 at 15-18).

Response to Finding No. 269: RPF 269 does not support the conclusion that Texas Instruments did not disclose relevant patent applications. First, there is no record evidence that the patent application was relevant to JEDEC's work. *See* CCRF 265, 267. Indeed it appears that the patent application was *not* related to the JEDEC work, as there is no evidence that IBM ever sought to enforce a patent against any JEDEC-compliant product. Second, if the patent was relevant, there is no record evidence that it was not disclosed. Many disclosures were

not recorded in the minutes. CCRF 247. In addition, RPF 269 is incomplete because there it contains no citation to any evidence of the subjective knowledge or belief of Mr. Vogley, Mr. Balisteri, Mr. Hartigan, Mr. Norwood, or any other TI employee concerning the relationship (if any) between the '958 and '694 patents and the work of any JEDEC committee.

Complaint Counsel does agree with the logical conclusion of RPF 269 that the duty to disclose is triggered by the subjective knowledge or belief of a reasonable engineer, such as Mr. Vogley, Mr. Balisteri, Mr. Hartigan, Mr. Norwood, or Mr. Crisp, as to the relationship between content of the patent application and the work of the JEDEC committee. As RPF 269 suggests, disclosure is not triggered by a finding (after expert testimony from patent lawyers) that the proposed standard does, in fact, infringe the patent application.

h. Toshiba Did Not Disclose Pending Patent Applications.

270. The Court has taken official notice of United States Patent No. 5,986,968, which issued on November 16, 1999 and is assigned to Toshiba. The '968 patent claims priority to a United States application filed on March 16, 1993 and an earlier Japanese application filed on March 19, 1992. ('968 patent at 1). Claim 42 of U.S. Patent No. 5,986,968 claims a semiconductor device comprising a "memory array," "control means" for outputting data N clock cycles ("latency N") after receiving a read command, and "programming means for variably programming the latency N." ('968 patent at 18).

Response to Finding No. 270: RPF 270 lacks any reference to the record and encompasses legal conclusions. Therefore, RPF 270 is inappropriate for findings of fact. Respondent did not present expert testimony to support a finding that U.S. Patent No. 5,986,968 might involve the work of JEDEC. Furthermore, Respondent did not present ay secondary evidence that Toshiba or anyone else believed that the '968 patent might involve the work of JEDEC.

The interpretation of patent claims involving complex technology, and the comparison of a product or potential product to that claim, cannot properly be resolve without the development of evidence, including expert testimony, before the finder of fact. *See NeoMagic Corp. v.*

Trident Microsystems, Inc., 287 F.3d 1062, 1074 (Fed. Cir. 2002) ("given the complex technology involved in this case, we think this matter [interpretation of a claim to a DRAM memory chip controller] can only be resolved by further evidentiary hearings, including expert testimony, before the district court."). A determination that a patent claim covers a product is a two step process. The first step requires that the court interpret the patent claim as it would be understood by a person of ordinary skill in the art as a question of law. RPF 270 cites no expert testimony or other evidence to establish the proper interpretation of the patent claims.

The second step requires a factual determination that each element of the properly interpreted claim is present in the product. (Nusbaum, Tr. 1565-66). RPF 270 cites no expert testimony or other evidence to establish that each element of any claim of this patent correspond to elements of the proposed alternative.

The Court's judicial notice of this patent, without evidence supporting a proper claim interpretation and infringement analysis, is insufficient to support the finding because the Court has "decline[d] to take official notice of what the patents in question relate to or cover, and decline[d] to engage in any analysis or interpretation of the substance or content" of the patent. *See* Order on Respondent's Request for Official Notice at 3 (August 27, 2003). Complaint Counsel submits that this finding should be disregarded pursuant to Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

271. SDRAMs contain a programmable latency feature whereby latency is programmed in the mode register. (CX 234 at 150; Rhoden, Tr. 393-94).

Response to Finding No. 271: Complaint Counsel does not disagree.

272. One of the inventors of the '968 patent, Hitoshi Kuyama, attended the May 1992 meeting of the JC-42.3 subcommittee. (CX 34 at 2). Presentations relating to programmable latency were made at that meeting, but the minutes do not reflect that Mr. Kuyama disclosed his pending application and the application does not appear on the patent tracking list. (CX 34 at 59; JX 28 at 15-18).

Response to Finding No. 272: This proposed finding does not support the conclusion that Toshiba did not disclose relevant patent applications. First, there is no record evidence that the patent application was relevant to JEDEC's work. *See* CCRF 270. Indeed it appears that the patent application was *not* related to the JEDEC work, as there is no evidence that IBM ever sought to enforce a patent against any JEDEC-compliant product. Second, if the patent was relevant, there is no record evidence that it was not disclosed. Many disclosures were not recorded in the minutes. CCRF 247. In addition, RPF 272 is incomplete because there it contains no citation to any evidence of the subjective knowledge or belief of Mr. Kuyama or any other Toshiba employee concerning the relationship (if any) among the original patent applications, the later filed amendments, and the work of any JEDEC committee.

Complaint Counsel does agree with the logical conclusion of RPF 272 that the duty to disclose is triggered by the subjective knowledge or belief of a reasonable engineer, such as Mr. Kuyama or Mr. Crisp, as to the relationship between content of the patent application and the work of the JEDEC committee. As RPF 272 suggests, disclosure is not triggered by a finding (after expert testimony from patent lawyers) that the proposed standard does, in fact, infringe the patent application.

i. Summary.

273. The evidence thus shows that numerous JEDEC attendees who were aware of patent applications (because they were named inventors on those applications) that were related to JEDEC's standard-setting work did not disclose those applications. This evidence supports the conclusion that JEDEC members did not understand that they were required to disclose such applications before they became issued patents.

Response to Finding No. 273: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Further, the Court's judicial notice of 28 patents is insufficient to establish that the patent applications were required to be disclosed at JEDEC because there is no record evidence: (1) "of what the patents in

question relate to or cover"; (2) whether the prior patent applications related to JEDEC work and, if so, how, and (3) whether any company employee had knowledge or belief that any of the cited patents might involve the work of a JEDEC committee. Complaint Counsel submits that this finding (and all related findings) should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

G. The EIA/JEDEC Patent Policy At Most Required Disclosure Of "Essential" Patents.

274. Assuming that JEDEC members were obligated to disclose some intellectual property interests at JEDEC meetings while Rambus was a member, the evidence shows that that obligation could have extended only to patents that were "essential" to a standard, *i.e.*, those patents that were necessary for the manufacture or use of a product that complied with the standard.

Response to Finding No. 274: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

In any event, this issue is irrelevant, as Rambus has asserted that its patents are essential to use of the four technologies at issue, and thus to practicing the standard. (CCFF 1950-2032).

275. EIA Manual EP-3-F refers only to standards that "*call for the use* of patented items." (CX 203A at 11) (emphasis added).

Response to Finding No. 275: This proposed finding is incomplete and misleading because EP-3-F also states that "[n]o program of standardization shall refer to a product on which there is a known patent unless all the technical information covered by the patent is known to the Formulating Committee." (CX0203A at 11). In addition, RPF 275 is contrary to the weight of the evidence and ignores substantial evidence that JEDEC required disclosure by "all participants" of "patents, or pending patents, that might be involved in the work they are undertaking." (CX0208 at 19) (emphasis added). *See also* CCFF 335-38.

In any event, this issue is irrelevant, as Rambus has asserted that its patents are essential to use of the four technologies at issue, and thus to practicing the standard. (CCFF 1950-2032).

276. EIA Manual EP-7-A refers only to standards "that *call for the exclusive use* of a patented item or process." (JX 54 at 9) (emphasis added).

Response to Finding No. 276: This proposed finding is incomplete and misleading because EP-7-A also states that "[n]o program [of] standardization shall refer to a patented item or process unless all of the technical information covered by the patent is known to the formulating committee or working group." In addition, RPF 276 is contrary to the weight of the evidence and ignores substantial evidence that JEDEC required disclosure by "all participants" of "patents, or pending patents, that might be involved in the work they are undertaking." (CX0208 at 19) (emphasis added). *See also* CCFF 335-38.

In any event, this issue is irrelevant, as Rambus has asserted that its patents are essential to use of the four technologies at issue, and thus to practicing the standard. (CCFF 1950-2032).

277. The EIA's January 1996 letter to the FTC states that the EIA "follows the ANSI intellectual property rights (IPR) policy as it relates to *essential* patents." (RX 669 at 2) (emphasis added).

Response to Finding No. 277: This proposed finding does not support the conclusion that JEDEC required disclosure only of those patents and patent applications that actually infringed upon a final standard. As an initial matter, the ANSI patent policy is not in evidence. The ANSI patent policy guidelines are in evidence (RX1712), but there was no testimony concerning whether the actual ANSI patent policy encourages or requires disclosure only of intellectual property that actually is infringed by a final standard. Further RPF 277 is contrary to the weight of the evidence and ignores substantial evidence that JEDEC required disclosure by "all participants" of "patents, or pending patents, that might be involved in the work they are undertaking." (CX0208 at 19) (emphasis added). *See also* CCFF 335-38.

In any event, this issue is irrelevant, as Rambus has asserted that its patents are essential to use of the four technologies at issue, and thus to practicing the standard. (CCFF 1950-2032).

278. JEDEC Secretary Ken McGhee's July 10, 1996 memorandum to JEDEC Council members and alternates states that the EIA encourages disclosure of "known *essential* patents." (RX 742 at 1) (emphasis added).

Response to Finding No. 278: This proposed finding is contrary to the weight of the evidence and ignores substantial evidence that JEDEC required disclosure by "all participants" of "patents, or pending patents, that might be involved in the work they are undertaking." (CX0208 at 19) (emphasis added). *See also* CCFF 335-38.

In any event, this issue is irrelevant, as Rambus has asserted that its patents are essential to use of the four technologies at issue, and thus to practicing the standard. (CCFF 1950-2032).

279. JEDEC's policy manual JEP 21-I similarly refers only to standards that "*require the use* of patented items." (CX 208 at 19) (emphasis added).

Response to Finding No. 279: This proposed finding is contrary to the weight of the evidence and ignores substantial evidence that JEDEC required disclosure by "all participants" of "patents, or pending patents, that might be involved in the work they are undertaking." (CX0208 at 19) (emphasis added). *See also* CCFF 335-38.

In any event, this issue is irrelevant, as Rambus has asserted that its patents are essential to use of the four technologies at issue, and thus to practicing the standard. (CCFF 1950-2032).

280. When writing on behalf of the EIA in August 1995 to an EIA member called Echelon, EIA General Counsel John Kelly explained that the "ANSI and EIA patent policy . . . requires an SDO to secure a commitment to license a patented item or process from a patent holder when a standard refers to a patented technology *or, as a practical matter, conformance to a standard requires use of the patented technology*." (RX 2299 at 2) (emphasis added).

Response to Finding No. 280: This proposed finding does not support the conclusion that JEDEC required disclosure only of those patents and patent applications that actually infringed upon a final standard because the quoted language specifically relates to "a

commitment to license." Respondent's use of RX2299 is misleading because Mr. Kelly's letter concerned only the licensing requirement of the JEDEC patent policy, not the disclosure requirement. Obviously, there is no need to license a patent or patent application where a determination has been made that such patent or patent application is not required to practice a standard. The cited language simply does not relate to the mandatory disclosure obligation.

In any event, this issue is irrelevant, as Rambus has asserted that its patents are essential to use of the four technologies at issue, and thus to practicing the standard. (CCFF 1950-2032).

281. Infineon's JEDEC representative Willi Meyer testified that it was his understanding the disclosure duty applied only to patents "related to the work at JEDEC in the sense that it described features that were *necessary to meet the standard*." (Meyer, 5/7/01 *Infineon* Trial Tr. at 117:12-14) (emphasis added).

Response to Finding No. 281: RPF 281 is misleading because it mischaracterizes Mr. Meyer's testimony. Mr. Meyer understood that disclosure was required if the patent or patent application was "was sufficiently close to the current work in progress in JEDEC." (CX2057 at 203-04 (Meyer 12/13/00 Dep.)). Further, RPF 281 ignores substantial evidence that the disclosure obligation extended to patents or patent applications that "might involve" the work of a JEDEC committee. *See* CCFF 319, 335-38.

In any event, this issue is irrelevant, as Rambus has asserted that its patents are essential to use of the four technologies at issue, and thus to practicing the standard. (CCFF 1950-2032).

282. A Hewlett-Packard JEDEC representative, Thomas Landgraf, testified that he understood the patent policy to involve disclosure if "the standard required someone else's idea to be used . . . in order for it to operate." (Landgraf, Tr. 1693-5).

Response to Finding No. 282: RPF is incomplete and misleading because it mischaracterizes Mr. Landgraf's testimony. Mr. Landgraf testified that "[t]he policy, as I understood it, was that if you as a member of JEDEC knew of a patent or application for a patent that would potentially be impacting the standard or proposed standard, you were to disclose it to

the committee." (Landgraf, Tr. 1693-94). *See* CCFF 319, 335. Further, RPF 282 ignores substantial evidence that the disclosure obligation extended to patents or patent applications that "might involve" the work of a JEDEC committee. *See* CCFF 319, 335-38.

In any event, this issue is irrelevant, as Rambus has asserted that its patents are essential to use of the four technologies at issue, and thus to practicing the standard. (CCFF 1950-2032).

283. Another Hewlett-Packard JEDEC representative, Ilan Krashinsky, testified that he had not disclosed any Hewlett-Packard patents to JEDEC because he did not think that they were "infringed" by any JEDEC standards proposals. (Krashinsky, Tr. 2848-9).

Response to Finding No. 283: This proposed finding does not support the conclusion that JEDEC required disclosure only of those patents and patent applications that actually infringed upon a final standard. When a JEDEC participant makes a good faith determination that there is no nexus between a patent or patent application and a proposed standard, then there is no requirement to disclose. *See* CCFF 310-14. Further, RPF 283 ignores substantial evidence that the disclosure obligation extended to patents or patent applications that "might involve" the work of a JEDEC committee. *See* CCFF 319, 335-38.

In any event, this issue is irrelevant, as Rambus has asserted that its patents are essential to use of the four technologies at issue, and thus to practicing the standard. (CCFF 1950-2032).

284. JEDEC 42.3 subcommittee chairman and IBM representative Gordon Kelley testified that the disclosure duty was triggered by a patent claim that "reads on or applies" to the standard, meaning that "if you exercise the design or production of the component that was being standardized [it] would require use of the patent." (Kelley, Tr. 2706-7).

Response to Finding No. 284: This proposed finding is inaccurate and misleading because Mr. Kelley testified that "[m]y definition says that any claim that might apply to the work of the committee it was required to disclose." (G. Kelley, Tr. 2705). Further, RPF 284 ignores substantial evidence that the disclosure obligation extended to patents or patent applications that "might involve" the work of a JEDEC committee. *See* CCFF 319, 335-38.

In any event, this issue is irrelevant, as Rambus has asserted that its patents are essential to use of the four technologies at issue, and thus to practicing the standard. (CCFF 1950-2032).

285. Another IBM JEDEC representative, Mark Kellogg, testified that his understanding was that "you have to disclose intellectual property that reads on the standard." (Kellogg, Tr. 5310-1). Mr. Kellogg also stated that "[s]ometimes we disclose intellectual property that doesn't [read on the standard] and one would question why. It adds confusion." (Kellogg, Tr. 5311).

Response to Finding No. 285: This proposed finding does not support the conclusion that JEDEC required disclosure only of those patents and patent applications that actually infringed upon a final standard. Indeed, Rambus did not clarify what Mr. Kellogg intended by the term "reads." For example, a patent that covers some, but not all, implementations of a standard could be considered to "read" on the standard. Further, RPF 285 ignores substantial evidence that the disclosure obligation extended to patents or patent applications that "might involve" the work of a JEDEC committee. *See* CCFF 319, 335-38.

In any event, this issue is irrelevant, as Rambus has asserted that its patents are essential to use of the four technologies at issue, and thus to practicing the standard. (CCFF 1950-2032).

H. JEDEC Members Were Not Required To Disclose Foreign Patents Or Foreign Patent Applications.

286. It is undisputed in this case that JEDEC "does not require its members to disclose foreign patents." (Complaint Counsel's Pre-Trial Brief, p. 259).

Response to Finding No. 286: Complaint Counsel does not disagree. As discussed in Complaint Counsel's pretrial brief, although JEDEC does not require its members to disclose foreign patents, its disclosure policy is based on the assumption that any member with significant foreign patent rights will at least have filed a patent application in the United States to protect those rights, so that disclosure of U.S. patent rights will effectively disclose rights in other parts of the world. (Complaint Counsel's Corrected Pre-Trial Brief at 265).

287. Siemens' JEDEC representative Willi Meyer testified that "[n]obody disclosed European patents" at JEDEC meetings. (Meyer, 5/7/01 Infineon Trial Tr., p. 119:3).

Response to Finding No. 287: Complaint Counsel does not disagree.

I. If Disclosure Of Intellectual Property Interests Was Required, It Was Required Only When JEDEC Participants Had "Actual Knowledge" Of The Intellectual Property And Its Relationship To JEDEC Standardization.

288. Assuming that JEDEC members were obligated to disclose some intellectual property interests at JEDEC meetings while Rambus was a member, the evidence shows that that obligation was triggered by the "actual knowledge" of the JEDEC representative of the intellectual property and its relationship to a standard.

Response to Finding No. 288: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. The proposed finding is also misleading by implying that "knowledge' is equivalent to certainty; in fact, the scope of a patent's coverage usually is not known with certainty until all relevant patent infringement litigation has been resolved. JEDEC requires its programs be conducted in good faith. *See* CCFF 310-14. Thus, "actual knowledge" as used by JEDEC does not require that a participant has made a determination that the standard does, in his or her opinion, infringe the patent or patent application. Instead, the duty to disclose is triggered by the good faith knowledge or belief of a participant that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335.

In any event, this issue is irrelevant, as Richard Crisp had actual knowledge of the potential scope of Rambus's patent claims based on his meetings and conversations with patent attorney Lester Vincent, his work helping to draft some of the relevant patent claims, and through other means. (CCFF 853-55, 857, 886 (late 1991 work with Lester Vincent on low swing

signals); 900-01 (May 1992 Crisp proposal to add claims covering use of mode register to control latency and asking about “blocks”); 910 (late May 1992 telephone conversation between Crisp and Vincent); 920 (June 1992 telephone conversation between Crisp and Vincent); 928 (August 1992 telephone conversation between Crisp and Vincent); 932-36 (September 1992 meeting between Crisp and Vincent regarding programmable CAS latency, multiple open rows (banks), on-chip PLLs and source synchronous clocking); 939 (November 1992 meeting among Crisp, Farmwald and Vincent regarding multiple open rows (banks)); 947-49 (February 1993 Crisp e-mail identifying programmable access latency, multiple open rows (banks) and on-chip PLL/DLL circuit as claims in process); 955, 958 (May 1993 conference among Crisp, Farmwald and Vincent regarding preliminary amendments, including the ‘651 regarding programmable access time); 962-66 (June 1993 e-mail exchange with Fred Ware confirming that claims covering programmable CAS latency, directed at SDRAMs, had been filed, that claims covering use of multiple open rows (banks) and on-chip PLLs, directed against SDRAMs and future SDRAMs respectively, were being written up, that claims covering externally supplied reference voltage were being considered, and that claims covering low voltage swing signals had already been filed); 967 (July 1993 meeting among Crisp, Ware and Vincent regarding low voltage swing signals and externally supplied reference voltage); 997 (March 1994 Crisp e-mail noting that Rambus might be able to “collect from” JEDEC members using externally supplied reference voltage if its patent claim was allowed); 1010-15 (September 1994 Crisp and Roberts e-mails recognizing that Rambus might have to fight patent infringement litigation with JEDEC members regarding use of on-chip PLL, programmable access latencies and other technologies); 1018-23 (October 1994 e-mails on same subject); 1031-38 (March 1995 Crisp e-mails regarding possibility that JEDEC work involving externally supplied reference voltage and source synchronous clocking might infringe Rambus patent claims); 1045 (May 1995 Crisp e-mail

noting that Rambus pending patent claims involving low swing signaling and programmable access latency might apply to the SyncLink proposal at JEDEC); 1050-55 (Crisp review of patents and applications and work with Vincent regarding claims to cover SyncLink in June-September 1995). Mr. Crisp received copies of the amendments to the '651 and '692 applications at the time they were filed in mid-1993. CCFF 955, 958, 966-67. Complaint Counsel is unable to establish whether Mr. Crisp received copies of the amendments to the '961 and '490 applications at the time they were filed in part because Lester Vincent, acting at the instructions of Rambus, destroyed copies of his correspondence with Rambus from the left-hand side of many of his files. CCFF 1746-48. In any event, Mr. Crisp had full access to all of Rambus's patents and patent applications, and reviewed a number of them in June 1995. CCF 1050.)

Furthermore, in addition to Mr. Crisp's knowledge, if others within Rambus knew that Rambus patents or patent applications might be involved in JEDEC work, they had an obligation to inform Mr. Crisp or another Rambus representative at JEDEC, so that they could inform JEDEC. (CCFF 334). A number of other Rambus officers and employees had knowledge both of events at JEDEC (in part through Mr. Crisp's trip reports) and the scope of Rambus's pending patent claims. (CCFF 900-01 (Vice President Roberts meeting with Vincent regarding use of mode register to control latency); 911-18 (June 1992 draft business plan, sent by Tate to the Board of Directors: "we believe that Sync DRAMs infringe on some claims in our filed patents; and that there are additional claims we can file for our patents that cover features of Sync DRAMs."); 938 (presentation to Board of Directors regarding the status of SDRAM activity at JEDEC and the Rambus patent strategy); 939 (Director Farmwald involved in November 1992 meeting with Vincent regarding multiple open rows (banks)); 947-49 (Vice President Roberts copied on February 1993 Crisp e-mail identifying programmable access latency, multiple open

rows (banks) and on-chip PLL/DLL circuit as claims in process); 955, 958 (Director Farmwald involved in May 1993 conference with Vincent regarding preliminary amendments, including the '651 regarding programmable access time); 962-66 (Director Farmwald and Vice President Roberts copied on June 1993 e-mails confirming that claims covering programmable CAS latency, directed at SDRAMs, had been filed, that claims covering use of multiple open rows (banks) and on-chip PLLs, directed against SDRAMs and future SDRAMs respectively, were being written up, that claims covering externally supplied reference voltage were being considered, and that claims covering low voltage swing signals had already been filed); 981 (conference among CEO Tate, Vice President Roberts, CFO Harmon and Mr. Vincent regarding enforcement of Rambus patents against Synchronous DRAMs, with specific reference to low voltage swing, programmable CAS latency and on-chip PLLs); 987-92 (Vice President Roberts' letter to Vincent proposing to add claims covering use of registers to control CAS latency, use of multiple banks and clocking data on both edges of the clock); 997 (executives copied on March 1994 Crisp e-mail noting that Rambus might be able to "collect from" JEDEC members using externally supplied reference voltage if its patent claim was allowed); 1000-03 (CEO Tate and Vice President Roberts copied on Dillon e-mail regarding claims covering auto-precharge); 1004-08 (Vice President Roberts circulated copy of the amendment to the '646 application with claims regarding dual edge clock, multiple banks and auto-precharge); 1010-15 (all executives copied on September 1994 Crisp and Roberts e-mails recognizing that Rambus might have to fight patent infringement litigation with JEDEC members regarding use of on-chip PLL, programmable access latencies and other technologies); 1018-23 (all executives copied on October 1994 e-mails on same subject); 1031-38 (all executives copied on March 1995 Crisp e-mails regarding possibility that JEDEC work involving externally supplied reference voltage and source synchronous clocking might infringe Rambus patent claims); 1045 (all executives copied

on May 1995 Crisp e-mail noting that Rambus pending patent claims involving low swing signaling and programmable access latency might apply to the SyncLink proposal at JEDEC); 1050-55 (Crisp review of patents and applications and work with Vincent regarding claims to cover SyncLink in June-September 1995); 1058 (meetings between CEO Tate and in-house counsel Diepenbrock regarding claims to cover current and future SDRAMs); 1069 (Diepenbrock presentation regarding "offensive" patent strategy, including DLLs and dual edge clocking); 1073 (when they saw the JEDEC survey ballot, Vice President Mooring and others thought Rambus had invented certain key features); 1074-75 (Diepenbrock meeting with Vincent regarding DLLs and an amendment to the '692 application); 1076-77 (notice of allowance for the '327 patent); 1100-05 (correspondence between Diepenbrock and Vincent, at the instruction of CEO Tate, concerning the enforcement readiness of the '327 patent)).

289. JEDEC Board Chairman Desi Rhoden testified that the disclosure obligations under the JEDEC patent policy were "triggered by the actual knowledge of the people that were involved. . . ." (Rhoden, Tr. 624).

Response to Finding No. 289: This proposed finding is misleading because "actual knowledge" as used by JEDEC does not require that a participant has made a determination that the standard does, in fact, infringe the patent or patent application. Instead, the duty to disclose is triggered by the good faith knowledge or belief of a participant that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335. The proposed finding is also misleading by implying that "knowledge" is equivalent to certainty; in fact, the scope of a patent's coverage usually is not known with certainty until all relevant patent infringement litigation has been resolved.

In any event, this issue is irrelevant, as Richard Crisp had actual knowledge of the potential scope of Rambus patent claims based on his meetings and conversations with patent attorney Lester Vincent, his work helping to draft some of the relevant patent claims, and through

other means. Furthermore, a number of other Rambus officers and employees had knowledge both of events at JEDEC (in part through Mr. Crisp's trip reports) and the scope of Rambus pending patent claims. (CCRF 288).

290. EIA General Counsel John Kelly testified that the disclosure obligations applied "to all participants with actual knowledge." (Kelly, Tr. 1970).

Response to Finding No. 290: This proposed finding is misleading because "actual knowledge" as used by JEDEC does not require that a participant has made a determination that the standard does, in fact, infringe the patent or patent application. Instead, the duty to disclose is triggered by the good faith knowledge or belief of a participant that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335. The proposed finding is also misleading by implying that "knowledge" is equivalent to certainty; in fact, the scope of a patent's coverage usually is not known with certainty until all relevant patent infringement litigation has been resolved.

In any event, this issue is irrelevant, as Richard Crisp had actual knowledge of the potential scope of Rambus patent claims based on his meetings and conversations with patent attorney Lester Vincent, his work helping to draft some of the relevant patent claims, and through other means. Furthermore, a number of other Rambus officers and employees had knowledge both of events at JEDEC (in part through Mr. Crisp's trip reports) and the scope of Rambus pending patent claims. (CCRF 288).

291. Mr. Kelly explained some of the reasons for the "actual knowledge" requirement:

> "Q. . . . you'd agree with me that EIA doesn't want people giving false information in patent disclosures?
> A. Absolutely.
>
> Q. And they want the information that comes in to be true and accurate?
> A. And open and honest and good faith, yes.

Q. And that's one of the reasons that you've talked before about actual knowledge on the part of the representative?
A. That's correct.

Q. And that the representative needs to have that actual knowledge so that they can make a truthful and accurate disclosure of IP to the committee?
A. That is correct."

(Kelly, Tr. 2171-2).

Response to Finding No. 291: This proposed finding is misleading because "actual knowledge" as used by JEDEC does not require that a participant has made a determination that the standard does, in fact, infringe the patent or patent application. Instead, the duty to disclose is triggered by the good faith knowledge or belief of a participant that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335. The proposed finding is also misleading by implying that "knowledge" is equivalent to certainty; in fact, the scope of a patent's coverage usually is not known with certainty until all relevant patent infringement litigation has been resolved.

In any event, this issue is irrelevant, as Richard Crisp had actual knowledge of the potential scope of Rambus patent claims based on his meetings and conversations with patent attorney Lester Vincent, his work helping to draft some of the relevant patent claims, and through other means. Furthermore, a number of other Rambus officers and employees had knowledge both of events at JEDEC (in part through Mr. Crisp's trip reports) and the scope of Rambus pending patent claims. (CCRF 288).

292. Mr. Rhoden did not know what obligation might exist where a representative had a *question* about whether his company might have intellectual property interests relating to a particular feature under discussion, but did not know if those interests existed. (Rhoden, Tr. 625).

Response to Finding No. 292: This proposed finding does not support the conclusion that JEDEC participants were not obligated to make good faith disclosures when the

participant knew or believed that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335. In addition, JEDEC participants were instructed to consult EIA Counsel when the participants had questions concerning the application of the patent policy. *See* CCFF 226, 380-81, 407. *See also* (CX0208 at 18).

In any event, this issue is irrelevant, as Richard Crisp had actual knowledge of the potential scope of Rambus patent claims based on his meetings and conversations with patent attorney Lester Vincent, his work helping to draft some of the relevant patent claims, and through other means. Furthermore, a number of other Rambus officers and employees had knowledge both of events at JEDEC (in part through Mr. Crisp's trip reports) and the scope of Rambus pending patent claims. (CCRF 288).

293. No witness testified that a JEDEC representative who had a question about whether his company might have intellectual property interests relating to a feature under discussion at JEDEC meetings had an obligation to disclose that he had that question.

Response to Finding No. 293: This proposed finding does not support the conclusion that JEDEC participants were not obligated to make good faith disclosures when the participant knew or believed that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335. In addition, JEDEC participants were instructed to consult EIA Counsel when the participants had questions concerning the application of the patent policy. *See* CCFF 226, 380-81, 407. *See also* (CX0208 at 18).

In any event, this issue is irrelevant, as Richard Crisp had actual knowledge of the potential scope of Rambus patent claims based on his meetings and conversations with patent attorney Lester Vincent, his work helping to draft some of the relevant patent claims, and through other means. Furthermore, a number of other Rambus officers and employees had knowledge both of events at JEDEC (in part through Mr. Crisp's trip reports) and the scope of Rambus pending patent claims. (CCRF 288).

294. It was undisputed at trial that JEDEC representatives had no obligation to do any investigation, research or inquiry of their company or its lawyers regarding possible intellectual property interests relating to JEDEC work. (Rhoden, Tr. 623-4; Kelley, Tr. 2451, 2700; Kelly, Tr. 1966-68; Meyer 12/13/00 Depo. Tr., 188:24-189:18).

Response to Finding No. 294: Complaint Counsel does not disagree. RPF 294, does not, however, support the conclusion that JEDEC participants were not obligated to make good faith disclosures when the participant knew or believed that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335. In addition, JEDEC participants were instructed to consult EIA Counsel when the participants had questions concerning the application of the patent policy. *See* CCFF 226, 380-81, 407. *See also* (CX0208 at 18).

In any event, this issue is irrelevant, as Richard Crisp had actual knowledge of the potential scope of Rambus patent claims based on his meetings and conversations with patent attorney Lester Vincent, his work helping to draft some of the relevant patent claims, and through other means. Furthermore, a number of other Rambus officers and employees had knowledge both of events at JEDEC (in part through Mr. Crisp's trip reports) and the scope of Rambus pending patent claims. (CCRF 288).

295. The EIA's January 10, 1996 comment letter to the FTC also spoke to the "actual knowledge" requirement and noted the "chilling effect" that a broader disclosure obligation would have:

> "EIA and TIA strongly agree that the FTC must limit the application of the *Dell* rule to cases involving *actual knowledge* of the existence of a patent and intentional failure to disclose the patent interest. Extending *Dell* to situations involving negligent failure to disclose or imputed knowledge ('should have known') of the existence of a patent interest would have a profound chilling effect on companies that participate in the process of voluntary standard development."

(RX 669 at 3) (emphasis added).

Response to Finding No. 295: This proposed finding does not support the conclusion that JEDEC participants were not obligated to make good faith disclosures when the participant knew or believed that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335. The language cited in RPF 295 relates solely to the issue of the lack of a duty to conduct a search of a company's patent portfolio when there is no good faith knowledge or belief that a relevant patent or patent application exists.

In any event, this issue is irrelevant, as Richard Crisp had actual knowledge of the potential scope of Rambus patent claims based on his meetings and conversations with patent attorney Lester Vincent, his work helping to draft some of the relevant patent claims, and through other means. Furthermore, a number of other Rambus officers and employees had knowledge both of events at JEDEC (in part through Mr. Crisp's trip reports) and the scope of Rambus pending patent claims. (CCRF 288).

J. If Disclosure Of Intellectual Property Interests Was Required, It Was Required Only At The Time Of Balloting.

296. Assuming that JEDEC members were obligated to disclose some intellectual property interests at JEDEC meetings while Rambus was a member, the evidence shows that that obligation was not triggered until the time that a proposal was balloted for approval.

Response to Finding No. 296: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, RPF 296 is contrary to the weight of the evidence. (*See* CCFF 339-46).

297. JC 42.3 Committee Chairman Gordon Kelley testified that as he understood the JEDEC patent policy, disclosure was required only at the time of balloting, although it was encouraged earlier in the process. (Kelley, Tr. 2707).

Response to Finding No. 297: This proposed finding is contrary to the weight of the evidence. (*See* CCFF 339-46). This finding does not support the argument that a company that recognized the relationship between its potential patent claims and ongoing JEDEC work could avoid any obligation to disclose by withdrawing from JEDEC before the final ballot. Rather a company that deliberately sought to withdraw from JEDEC in an effort to avoid an obligation to disclose relevant intellectual property acted in bad faith. (CCFF 343-44). In addition, RPF 297 misstates the weight of Mr. Kelley's testimony. Mr. Kelley testified that "[t]he policy at JEDEC was that disclosure *should* occur as soon as possible in the discussion of the material and certainly by the time it was balloted. (G. Kelley, Tr. 2702).

298. Siemens JEDEC representative Willi Meyer testified (via deposition) that although it was "good practice" to notify the committee before balloting, "the ballot was considered the deadline when it should have been done." (CX 2057, Meyer 12/13/00 Depo. Tr., p. 211). Cray's JEDEC representative, Alan Grossmeier, agreed. (Grossmeier, Tr. 10945). The viewgraphs that were routinely shown at JC 42.3 meetings reinforced this view, since they ask the committee chair to "resolve patent status prior to (choose one)," followed by a list of events, almost all of which relate to balloting. (*See, e.g.*, JX 20 at 15-18; JX 21 at 14-18; JX 22 at 12-17).

Response to Finding No. 298: This proposed finding is contrary to the weight of the evidence. (*See* CCFF 339-46). In addition, RPF 298 is unreliable because Mr. Grossmeier admitted that patent issues were not a priority for him and that John Kelly was a more authoritative source for the scope of the JEDEC patent policy. (Grossmeier, Tr. 10957). Mr. Kelly, and others, testified that disclosure is not tied to any particular procedural formality in the JEDEC process. *See* CCFF 340.

299. EIA General Counsel John Kelly testified that ". . . the participant needs to exercise some judgment" on the question of when a disclosure requirement was triggered. (Kelly, Tr. 1981). According to Mr. Kelly,

> "[T]here's a gray area there where, to put it this way, the standard is evolving, their IP may be evolving, and the question is, is there a sufficient relationship between the IP – if this is what you're driving at – the IP and the work on the committee to trigger that duty to disclose? So, there's a – there's an area of judgment, and

> the area of judgment is probably more apparent earlier in the process and less apparent later in the process, and in theory – again, if this is what you're driving at, and I thought it was where you were going – at some point when there's an issued patent and the work on the committee is complete, the judgmental area becomes much narrower, and there may, in fact, be very little judgment involved by the participant in whether they are sufficient knowledge to trigger the duty to disclose."

(Kelly, Tr. 1981).

Response to Finding No. 299: This proposed finding does not support the conclusion that disclosure was required only at the time of a JEDEC ballot. The cited testimony cannot be understood outside of the context of Mr. Kelly's response to the very next question: "Q. When you say that judgment is involved in complying with the JEDEC/EIA patent policy, by that do you mean that members or participants are free not to disclose even in instances in which they subjectively know or believe that their patents or patent applications relate to the committee's work? A. No, because . . .overriding this whole process is a duty to act in good faith. So, regardless of their subjective beliefs, if those beliefs are not held in good faith, then they're in violation of the good faith portion of the Legal Guides and the overriding principles that govern our activities. . . If, on the other hand, in good faith they have reached that point where they can say, yeah, I can see that there's enough relationship here that I should be disclosing something, then clearly they ought to be disclosing." (J. Kelly, Tr. 1982).

300. As Kelly's testimony points out, even assuming that there is a disclosure requirement for patent applications, its implementation involves "gray area[s]" and the exercise of "judgment" on the part of the participant, especially where the standard is still "evolving." (Kelly, Tr. 1981).

Response to Finding No. 300: This proposed finding is misleading and does not support the conclusion that disclosure was required only at the time of a JEDEC ballot. The cited testimony, read in context (*see* CCRF 299), does not discuss the issue of the timing of disclosure.

Instead, the testimony concerns the level of judgment a participant must use in determining, in good faith, whether the patent or patent application might involve the work of the committee.

K. Summary Of Findings Regarding Patent Policy Issues.

301. The manuals and policies that governed JEDEC's standardization activities while Rambus was a member encouraged, but did not require, disclosure of intellectual property interests.

Response to Finding No. 301: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is contrary to the weight of the evidence. *See* CCFF 318-46.

302. The EIA legal guides do not require the disclosure of intellectual property interests.

Response to Finding No. 302: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is contrary to the weight of the evidence. *See* CCRF 129-32.

303. The EIA manuals in effect prior to June 1996 contained no reference to any disclosure obligation.

Response to Finding No. 303: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is contrary to the weight of the evidence. *See* CCRF 133-40.

304. The ANSI patent policy, which was officially adopted by the EIA at least as early as October 1995, encouraged but did not require the disclosure of intellectual property interests.

Response to Finding No. 304: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is contrary to the weight of the evidence because EIA did not adopt the ANSI patent policy. *See* CCFF 435-43; CCRF 141-59.

305. JEDEC manual 21-H, which was in effect when Rambus joined JEDEC and when the SDRAM standard was adopted in 1993, contains no reference to a disclosure obligation.

Response to Finding No. 305: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is misleading and ignores substantial evidence that JEDEC participants were obligated to disclose patents and patent applications that might involve the work of a JEDEC committee at the time Rambus joined JEDEC. *See* CCFF 403-18.

306. JEDEC manual 21-H, which was in effect when Rambus joined JEDEC in 1992 and when the SDRAM standard was adopted in 1993, states that JEDEC standards "are adopted without regard to whether or not their adoption may involve patents on articles, materials or processes."

Response to Finding No. 306: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is misleading and does not support the conclusion that JEDEC participants were not obligated to disclose patents and patent applications at the time Rambus joined JEDEC and at the time the SDRAM standard was adopted. *See* CCFF 403-18.

307. The application form used by Rambus when joining JEDEC contains no reference to a disclosure obligation.

Response to Finding No. 307: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is misleading and does not support the conclusion that JEDEC participants were not obligated to disclose patents and patent applications. *See* CCFF 318-56. RPF 307 also does not support the conclusion that Rambus was not informed of its obligations under the JEDEC patent policy. *See* CCFF 357-418.

308. JEDEC manual 21-I, published in October 1993, does refer – indirectly – to a disclosure obligation. Complaint Counsel did not show, however, that the 21-I manual had ever received the necessary EDEC approval.

Response to Finding No. 308: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is contrary to the weight of the evidence. The disclosure obligation in the JEDEC Manual or Organization and Procedure is explicit and the 21-I Manual governed JEDEC procedures from the time it was adopted in 1993 until the time it was superceded. *See* CCFF 319, 408-18; CCRF 163-75.

309. The appendices contained in the 21-I manual that relate to intellectual property state only that discussion of patent applications is "permissible," and do not state that any such discussion is required.

Response to Finding No. 309: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is misleading and

does not support the conclusion that disclosure of patent applications is not required. *See* CCFF 319-20; CCRF 174.

310. The JC 42 members' manual refers to a disclosure obligation on the part of presenters. Rambus made no presentations to JEDEC.

Response to Finding No. 310: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding does not support the conclusion that the obligation to disclose patent applications was limited to presenting companies because, *inter alia*, Mr. Townsend's Members' Manual was not a JEDEC or EIA publication. *See* CCFF 319, 324, 330; CCRF 176-81.

311. JEDEC's ballot forms encouraged, but did not require, disclosure by members of relevant patents.

Response to Finding No. 311: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is contrary to the weight of the evidence. *See* CCFF 383-86; CCRF 182-85.

312. There is substantial evidence that JEDEC members and the JEDEC leadership understood during the time that Rambus was a JEDEC member that members were encouraged, but not required, to make a disclosure of their intellectual property.

Response to Finding No. 312: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is contrary to the weight of the evidence. *See* CCFF 319, 324, 330; CCRF 186-98.

313. Some JEDEC representatives believed that no disclosure was required as long as the member company ultimately licensed its relevant patents to all comers on reasonable terms.

Response to Finding No. 313: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is contrary to the weight of the evidence and does not support the conclusion that disclosure of patents and patent applications that might be involved in the work of JEDEC was not mandatory. *See* CCFF 357-418; CCRF 199-203.

314. If there were a disclosure requirement, it extended only to issued patents and not to patent applications.

Response to Finding No. 314: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is contrary to the weight of the evidence. *See* CCFF 319-20; CCRF 204-73.

315. If there were a disclosure requirement, it was only triggered by the "actual knowledge" of the JEDEC representative himself.

Response to Finding No. 315: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is misleading to the extent it suggests that "actual knowledge" means certainty that the patent or patent application is infringed by a final JEDEC standard. *See* CCFF 310-14, 333; CCRF 288-95.

316. The EIA/JEDEC patent policy at most required disclosure of "essential" patents.

Response to Finding No. 316: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is contrary to the weight of the evidence. *See* CCFF 319, 335-38; CCRF 274-85.

317. If disclosure of intellectual property interests was required, it was required only at the time of balloting.

Response to Finding No. 317: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is contrary to the weight of the evidence. *See* CCFF 339-46; CCRF 296-300.

V. RAMBUS DID NOT VIOLATE ANY EIA/JEDEC RULES.

A. Introduction And Summary Of Findings.

318. Because the EIA/JEDEC patent policies in effect while Rambus was a JEDEC member encouraged, but did not require, a member to disclose its intellectual property interests, Rambus's alleged non-disclosure violated no policies or rules.

Response to Finding No. 318: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the underlying assumption of RPF 318 is contrary to the weight of the evidence because the JEDEC patent policy did require participants to disclose intellectual property that a participant knew or believed might involve the work of a JEDEC committee. *See* CCFF 318-46. Therefore, the conclusion is not supported by the record.

319. If the EIA/JEDEC patent policies in effect while Rambus was a JEDEC member did require disclosure of intellectual property interests, but required such disclosure only by *presenters* who were trying to encourage JEDEC's adoption of a particular technology, Rambus violated no policies or rules, for Complaint Counsel have not proved that Rambus made any such presentations.

Response to Finding No. 319: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, the finding is contrary to the weight of the evidence because JEDEC required all participants to disclose intellectual property that they knew or believed might involve the work of a JEDEC committee. *See* CCFF 324, 330. Therefore, the conclusion is not supported by the record.

320. If the EIA/JEDEC patent policies in effect while Rambus was a member required disclosure of intellectual property interests only by members who did not license their patents on reasonable and non-discriminatory terms, then Rambus violated no policies or rules, for Complaint Counsel have not proved that Rambus's license terms are unreasonable or discriminatory. *See* Findings ¶¶ 1359-1420.

Response to Finding No. 320: The underlying assumption of RPF 320 is contrary to the weight of the evidence because the JEDEC patent policy required all participants to disclose irrespective of the position of the participant's company with respect to licensing. *See* (J. Kelly, Tr. 1969-70); CCFF 330. Therefore, the conclusion is not supported by the record.

321. If the EIA/JEDEC patent policies in effect while Rambus was a member required disclosure only of issued patents (and not patent applications) that read on or were "essential" to the use of technology proposed for standardization, then Rambus violated no policies or rules, for Complaint Counsel have not proved that Rambus had any such patents. *See* Findings ¶¶ 327-360.

Response to Finding No. 321: The underlying assumption of RPF 321 is contrary to the weight of the evidence because the JEDEC patent policy required the disclosure of patents and patent applications that "might involve" the work of a JEDEC committee. *See* CCFF 335-38. Therefore, the conclusion is not supported by the record. Furthermore, the finding is

inaccurate because Complaint Counsel has proven that the Rambus '327 patent satisfied even the criteria stated in this proposed finding. CCFF 1216-37.

322. If the EIA/JEDEC patent policies in effect while Rambus was a member required disclosure of both patents *and* patent applications that read on or were "essential" to the use of a technology proposed for standardization, then Rambus violated no policies or rules, for Complaint Counsel have not proved that Rambus had any such patents or patent applications. *See* Findings ¶¶ 361-396.

Response to Finding No. 322: The underlying assumption of RPF 322 is contrary to the weight of the evidence because the JEDEC patent policy required the disclosure of patents and patent applications that "might involve" the work of a JEDEC committee. *See* CCFF 335-38. Therefore, the conclusion is not supported by the record. Furthermore, the finding is inaccurate because Complaint Counsel has proven that the Rambus '327 patent and '692, '646, '961 and '490 patent applications satisfied even the criteria stated in this proposed finding. CCFF 1122-1237.

323. If the EIA/JEDEC patent policies in effect while Rambus was a member required disclosure of patents and/or patent applications where the JEDEC representative had "actual knowledge" that the claims of the patent or application covered the technology proposed for standardization, then Rambus violated no policies or rules, for Complaint Counsel have not proved that Rambus's representatives had any such knowledge. *See* Findings ¶¶ 417-431.

Response to Finding No. 323: The underlying assumption of this proposed finding is contrary to the weight of the evidence because the JEDEC patent policy does not require that a JEDEC participant have actual knowledge *that the claims cover* the standard. Instead, the JEDEC patent policy requires that the JEDEC participant know or believe that a patent or patent application *might involve* the work of a JEDEC committee. *See* CCFF 335-38. Therefore, the conclusion is not supported by the record.

In any event, this issue is irrelevant, as Richard Crisp had actual knowledge of the potential scope of Rambus patent claims based on his meetings and conversations with patent attorney Lester Vincent, his work helping to draft some of the relevant patent claims, and through

other means. Furthermore, a number of other Rambus officers and employees had knowledge both of events at JEDEC (in part through Mr. Crisp's trip reports) and the scope of Rambus pending patent claims. (CCRF 288).

324. If the EIA/JEDEC patent policies in effect while Rambus was a member required disclosure of intellectual property interests at the time of balloting, as JC 42.3 Chairman Gordon Kelley testified, then Rambus could not have violated any policy or rule except as to programmable latency and programmable burst, for those are the only two features complained of by Complaint Counsel that were balloted while Rambus was a JEDEC member. *See* Findings ¶¶ 397-416.

Response to Finding No. 324: The underlying assumption of RPF 324 is contrary to the weight of the evidence because the JEDEC patent policy required disclosure of patents and patent applications as soon as a participant had knowledge or believed that the patent or patent application might involve the work of a JEDEC committee. *See* CCFF 333, 339-45. Therefore, the conclusion that Rambus could only have violated the patent policy with respect to the programmable latency and programmable burst features is not supported by the record.

This finding does not support the argument that a company that recognized the relationship between its potential patent claims and ongoing JEDEC work could avoid any obligation to disclose by withdrawing from JEDEC before the final ballot. Rather, a company that deliberately sought to withdraw from JEDEC in an effort to avoid an obligation to disclose relevant intellectual property acted in bad faith. (CCFF 343-44).

325. Rambus did not violate any JEDEC rule or policy simply by seeking or obtaining patent protection for inventions that related to JEDEC standards, for no rule or policy prohibited such patents. *See* Findings ¶¶ 432-443.

Response to Finding No. 325: Complaint Counsel does not disagree. The violation of the JEDEC patent policy occurred when Rambus failed to disclose such conduct to JEDEC. *See* CCFF 318–46.

326. Complaint Counsel have not met their burden of showing that Rambus intentionally sought to violate any patent policy governing its conduct as a JEDEC member. *See* Findings, ¶¶ 417-431, 444-463.

Response to Finding No. 326: RPF 326 constitutes legal argument and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. The proposed finding also is contrary to the overwhelming weight of the evidence. (CCFF 800-66).

B. While It Was A JEDEC Member, Rambus Never Had Any Intellectual Property Interests That It Was Required To Disclose To JEDEC.

1. Rambus Had No Undisclosed Patents That It Was Required To Disclose To JEDEC.

327. The parties stipulated that as of January 1996, Rambus held no issued U.S. patents that were essential to the manufacture or use of any device manufactured in compliance with any JEDEC standard. (The Parties' First Set of Stipulations, Stipulation 10).

Response to Finding No. 327: This proposed finding accurately cites the stipulation but ignores several key points: (1) the intellectual property that was required to be disclosed to JEDEC included pending as well as issued patents (*see* CCFF 320); (2) the intellectual property required to be disclosed was not limited to intellectual property deemed "essential" (*see* CCFF 335, 338); and (3) the disclosure requirement applied in the case of all JEDEC work, not just JEDEC standards or final adoption of JEDEC standards. (CCFF 335 - 338). In addition, the proposed finding ignores the fact that, as of January 1996, the Rambus '327 patent, for which a Notice of Allowance of claims had been issued by the U. S. Patent Office, was "essentially a done deal." (*See* CCFF 1076, quoting Joel Karp, who served as Rambus Vice President of Intellectual Property from 1997 to 2000).

328. The only patent that Complaint Counsel allege should have been disclosed to JEDEC by Rambus is U.S. Patent 5,513,327 (the '327 patent). Complaint Counsel allege that

disclosure of the ’327 patent was required because, they say, claims 1 and 7 of the patent could have been reasonably construed by an engineer to cover a JEDEC-compliant SDRAM that also incorporated certain dual-edged clocking proposals and because those claims would, they say, read on the JEDEC DDR SDRAM standard. (Jacob, Tr. 5541-49, 5551-60). The proposals or presentations that Complaint Counsel raise in this regard are: (1) a presentation by William Hardell of IBM referenced in the May 1992 minutes of the JEDEC 42.3 subcommittee (the “Hardell presentation”) (CX 34 at 32; Jacob, Tr. 5542), (2) a “Future SDRAM Features Survey Ballot” referenced in the December 1995 minutes of the JEDEC 42.3 subcommittee (the “Survey Ballot”) (JX 28 at 34-35; Jacob, Tr. 5543-44), and (3) a presentation by Samsung entitled “Future SDRAM,” referenced in the March 1996 minutes of the JEDEC 42.3 subcommittee (the “Samsung presentation”) (JX 31 at 71; Jacob, Tr. 5544).

Response to Finding No. 328: The proposed finding is an incomplete and inaccurate statement of Complaint Counsel’s allegations. Complaint Counsel alleges that Rambus should have disclosed its patent and patent applications to JEDEC, including the ‘327 patent, based on Rambus’s understanding of its patent rights, its extensive efforts to obtain patent rights covering a JEDEC-compliant SDRAM and JEDEC-compliant SDRAMs incorporating JEDEC work and proposals, and its eventual success in obtaining patent rights that it now asserts over the dual-edged clocking feature of a JEDEC DDR SDRAM.

Moreover, although Complaint Counsel’s technical expert compared the claims of the ‘327 patent only to the three dual-edged clocking proposals listed in RPF 328, Complaint Counsel presented other evidence of JEDEC work involving dual-edged clocking that generated a duty to disclose patents and patent applications related to dual-edged clocking. The three dual-edged clocking proposals identified by Complaint Counsel’s technical expert are properly understood in the context of JEDEC’s ongoing work on this feature. (CCFF 620-642). Dual-edge clocking was a feature that had long been under discussion at JEDEC in connection with the “next generation” SDRAM standard, including discussions that began before and continued throughout the time that Rambus was a member of JEDEC. (CCFF 522, 524-26, 581, 585, 623-25, 628-33, 635, 637-40, 1072, 1079, 1200-03).

329. The ’327 patent issued on April 30, 1996 and was publicly available as of that date. (CX 1494 at 1). All of the proposals or presentations referenced by Complaint Counsel as supposedly triggering a disclosure obligation with respect to the ’327 patent were made *before* the ’327 patent issued.

Response to Finding No. 329: The proposed finding is misleading. The ‘327 patent issued from Rambus patent application 08/222,646, which Rambus filed on March 31, 1994. The ‘646 application claims priority based on the original Rambus ‘898 application. (CX1493 at 002; CCFF 1204). On September 6, 1994, Rambus submitted new claims 151 and 152, among others, in the ‘646 application that relate to the dual-edged clocking proposals. (CCFF 1205-1215). On, April 26, 1995, Rambus amended claims 152 and 158 of the ‘646 application so that they were in the form issued as claims 1 and 7 in the ‘327 patent. (CX1493 at 222-25). During the period from September 1994 (when Rambus filed its new claims 151 and 152 to its ‘646 application) through the withdrawal of Rambus from JEDEC in June 1996, there were discussions at JEDEC of dual-edge clock technology on multiple occasions. (CCFF 633-41, 1072, 1079, 1201-02).

The patent examiner allowed the claims of the ‘646 application on June 16, 1995. Rambus had notice as of June 16, 1995 (prior to the December 1995 and March 1996 dual-edged clocking proposals) that it would receive a patent containing claims 1 and 7 of what would be the ‘327 patent. (CX1493 at 237, 249). During the period from June 1995 (when Rambus learned that its ‘646 application) through the withdrawal of Rambus from JEDEC in June 1996, there were discussions at JEDEC of dual-edge clock technology on multiple occasions. (CCFF 633-41, 1072, 1079, 1201-02).

Dual-edge clocking was a feature that had long been under discussion at JEDEC in connection with the “next generation” SDRAM standard, including discussions that began before

and continued throughout the time that Rambus was a member of JEDEC. (CCFF 522, 524-26, 581, 585, 623-25, 628-33, 635, 637-40, 1072, 1079, 1200-03).

330. None of the proposals or presentations referenced by Complaint Counsel as triggering a disclosure obligation with respect to the '327 patent were balloted for approval at JEDEC while Rambus was a member.

Response to Finding No. 330: This proposed finding accurately cites from the stipulation but ignores several key points: (1) the intellectual property that was required to be disclosed to JEDEC included pending as well as issued patents (*see* CCFF 320); (2) the disclosure requirement applied in the case of all JEDEC work, not just JEDEC standards or final adoption of JEDEC standards. (CCFF 335 - 338); and (3) the disclosure obligation arose in connection with any JEDEC work, not only formal balloting of proposals or presentations for approval (CCFF 340). The disclosure obligation arises in connection with discussions at JEDEC (CCFF 341) and is intended to result in disclosure as early as practicable in the JEDEC process (CCFF 342).

331. Complaint Counsel did not show that Rambus's JEDEC representative had actual knowledge of the claim of the '327 patent at the time of the proposals or presentations that supposedly triggered a disclosure obligation with respect to the '327 patent.

Response to Finding No. 331: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

In fact, the record could not be clearer that Richard Crisp had broad ongoing actual knowledge of the developing scope of the Rambus patent claims based on his meetings and conversations with patent attorney Lester Vincent, his work helping to draft some of the relevant patent claims, and through his close involvement with other Rambus executives, throughout the period he served as Rambus representative to JEDEC. (*See* CCFF 867-1114, CCRF 288).

Furthermore, in addition to Mr. Crisp's knowledge, if others within Rambus knew that Rambus patents or patent applications might be involved in JEDEC work, they had an obligation to inform Mr. Crisp or another Rambus representative at JEDEC, so that they could inform JEDEC. (CCFF 334). A number of other Rambus officers and employees had knowledge both of events at JEDEC (in part through Mr. Crisp's trip reports) and the scope of pending Rambus patent claims. (*See* CCFF 867-1114, CCRF 288).

The record contains substantial evidence that Mr. Crisp was well aware of Rambus claims to dual-edge clock technology. In June1995, for example, Mr. Crisp did a "general sort of read" of Rambus intellectual property. (Crisp, Tr. 3274). Mr. Crisp had access to the entire set of Rambus patent files. (CX0798; Crisp, Tr. 3585-86). Rambus patent documents at the time included the amended '646 application with claims that related to dual-edged clocking, which in the summer of 1995 was approved for issuance as what would ultimately be the '327 patent. (CCFF 1205-1215). Mr. Crisp's review of the Rambus intellectual property was part of an extensive internal effort over the course of the summer by Rambus personnel in response to the JEDEC presentation in May 1995 concerning SyncLink technology; the focus of the Rambus effort was among other things on strategies to block the SyncLink technology on the basis of Rambus intellectual property claims. (Crisp, Tr. 3274; CCFF 1050-55). On July 21, 1995, Don Stark, an engineer at Rambus, circulated an e-mail to all Rambus staff calling specific attention to the SyncLink clocking scheme, and the fact that SyncLink used both edges of the clock to input data. (CX0711 at 156, 157; Crisp, Tr. 3261-62).

In the fall of 1995, Mr. Crisp began to work with the newly-hired Rambus Intellectual Property Manager Anthony Diepenbrock. (Crisp, Tr. 2937-38, 3004-05, 3305, 3317, 3324-25, 3327). In this time period, Mr. Diepenbrock gave a presentation to Rambus employees on "Rambus IP strategy." (CX1267; Diepenbrock, Tr. 6129-30). The "Offensive" patent strategy,

according to Mr. Diepenbrock, meant "finding key or essential areas of Rambus intellectual property and claiming them as broadly as possible." (Diepenbrock, Tr. 6131). An example of the "Offensive" strategy was dual edge clocking technology, or transmitting or receiving data on both edges of the clock. (CX1267; Diepenbrock, Tr. 6132-33). At the time of the presentation, Rambus had notice that it would receive a patent containing claims 1 and 7 of what would be the '327 patent, pertaining to dual-edge clock technology. (CX1493 at 237, 249). During this same period, Mr. Crisp and Mr. Diepenbrock were working closely on issues pertaining to Rambus participation in JEDEC. (CCFF 1059-61).

In October 1995 a next generation SDRAM survey ballot was prepared and distributed to JC-42.3 Committee members including Mr. Crisp of Rambus. (Crisp, Tr. 3328-29; CX0260 at 1). Among the issues inquired about in the survey ballot was whether Committee members believed future generations of SDRAM could benefit from using both edges of the clock for sampling inputs. (CX0260 at 12). The survey ballot was received by Mr. Crisp and distributed to the business development and marketing groups of Rambus. (Crisp, Tr. 3329; CX2056 at 264 (Mooring, Dep.)). Rambus Vice-President Mooring summarized the reaction at Rambus: "We [Rambus] believe we invented key aspects of several of the things on this list." (CX2056 at 268 (Mooring, Infineon Dep.)).

In January 1996, the JEDEC JC-42.3 Committee held an interim meeting in Sunnyvale, California. (JX0029 at 1; Rhoden, Tr. 484). Mr. Crisp of Rambus did not attend this Committee meeting, but he received the minutes and circulated copies by email to others at Rambus (Crisp, Tr. 3561). His email, which was sent to Rambus CEO Tate, Vice Presidents Mooring and Roberts, Intellectual Property Manager Diepenbrock, and others, called special attention to a presentation at the meeting by Micron, and "especially the part about the separate transmit and

receive clocks." (CX0868 at 1). Mr. Crisp suggested that this presentation should be evaluated with "a long hard look at our IP." (*Id.*).

During 1996, beginning before Rambus withdrew from JEDEC, Rambus began to consider enforcement of its '327 patent against a firm called Mosys. (CCFF 1100-05). Rambus documents suggest that a "competitive analysis" of the Mosys device had been prepared in January of 1996 (CX1316) and again in March of 1996 (CX1319). Richard Crisp, Rambus' JEDEC representative, attended meetings in the 1996 time frame involving representatives of Rambus and Mosys where the alleged infringement of Rambus patents by Mosys was discussed. (Crisp, Tr. 3368-3369). These discussions related, in part, to a particular implementation of dual edge clocking technology contained in the Rambus '327 patent. (*Id.*)

In August 1996, shortly after having withdrawn from JEDEC, Mr. Crisp shared with others at Rambus a presentation, based in part on confidential JEDEC material, about SDRAM using double clocked data. (CCFF 1107-08). Mr. Crisp's presentation discussed SDRAM using double clocked data. (CX1320 at 4 ("What about double clocked Data?" with a timing diagram referencing the rising and falling edges of a clock signal); *id.* at 5 ("Double Clocked Data (read case)" and "Double Clocked Data (write case)")).

In short, there is substantial evidence that Mr. Crisp, and others in the group at high levels in Rambus who were closely involved with the participation of Rambus in JEDEC, were well aware of the Rambus claim to patent rights to the dual-edge clock technology embodied in what was to become, and in fact became, the 'Rambus '327 patent.

332. Complaint Counsel's patent law expert, Mark Nusbaum, did not testify as to whether claims of the '327 related to JEDEC work.

Response to Finding No. 332: The proposed finding is misleading. Mr. Nusbaum testified on the relationship between claim 151 of the '646 application that led to the

'327 patent and JEDEC work. (CCFF 1199-1211). Claim 151 contains language that was incorporated into claim 1 of the '327 patent. (CX1493 at 184; CX1494 at 23).

333. Professor Jacob, who did testify regarding the alleged relationship between the ’327 patent and JEDEC work, has no patents to his name and has never previously done any claims analysis of the type he presented in this matter with respect to the ’327 patent. (Jacob, Tr. 5624, 5650).

Response to Finding No. 333: The proposed finding is irrelevant to an assessment of Professor Jacob’s testimony. Patent claims are interpreted and analyzed from the viewpoint of one of ordinary skill in the art to which the patent pertains. (Fliesler, Tr. 8933). The Court properly qualified Professor Jacob as an expert in the art to which the ‘327 patent and the patent applications in the ‘898 family pertain, the field of memory architectures and systems. (Jacob, Tr. 5363). Professor Jacob has extensive experience studying and designing memory architectures and systems. (Jacob, Tr. 5352-5364). He is therefore well-qualified to interpret and analyze the claims of the ‘327 patent and other patents and applications in the ‘898 family.

334. In order to show that a claim of a patent would cover a JEDEC-compliant device, it is necessary to show that all of the elements or “limitations” in the claim are found in that device. (Nusbaum, Tr. 1565-66). If there are limitations in the claim that are not found in a JEDEC-compliant device, then there would be no infringement of the claim. (Nusbaum, Tr. 1625).

Response to Finding No. 334: The proposed finding does not support a conclusion that a patent or patent application relates to JEDEC work only if every limitation of a patent claim within that patent or application is present in a JEDEC-compliant device. In fact, the scope of a patent’s coverage usually is not known with certainty until all relevant patent infringement litigation has been resolved. JEDEC requires its programs be conducted in good faith. *See* CCFF 310-14. The JEDEC disclosure requirement does not apply only where there is a determination that any and all products built to conform to the standard, in all possible implementations, will infringe the patent or patent application. Instead, the duty to disclose is

triggered by the good faith knowledge or belief of a participant that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335.

a. The Relevant Claims of the '327 Patent Contain Various Limitations.

335. As Professor Jacob concedes, Claim 1 of the '327 patent "describes a specific implementation" of dual edge clocking, including the "implementation detail" that the DRAM contains two input receivers with one receiver latching information in response to the rising edge of a clock signal and the other receiver latching information in response to the falling edge of the clock signal. (CX 1494 at 23; Jacob, Tr. 5546-47).

Response to Finding No. 335: The proposed finding is incomplete. Claim 1 of the '327 patent recites a "first input receiver for latching information provided by the bus via the conductor in response to the rising edge of the clock signal," and a "second input receiver for latching information from the bus in response to the falling edge of the clock signal." (CX1494 at 23; CCFF 1218). In describing the receivers, or latches, as "an implementation detail," Professor Jacob explained that there was no way, other than having two input receivers as recited in the claim, to implement dual-edged clocking. (Jacob, Tr. 5546-47) ("so this is sort of an implementation detail - that's how you would implement dual-edged clocking because any given latch cannot operate on both edges of a clock, a latch can only respond to either the rising edge or the falling edge, so the only way to perform this is really to have two latches, one in response to the rising edge, one in response to the falling edge."). DDR SDRAM in fact uses two input receivers as recited in claim 1 of the '327. (CCFF 1224-1228).

Because the Rambus '327 patent contains claims covering the most feasible way to implement the dual-edged clocking feature, as proposed to JEDEC in May 1992, December 1995 and March 1996, in a JEDEC-compliant SDRAM, and also contains claims covering DDR SDRAM as ultimately implemented in JEDEC Specification JESD 79 (June 2000). (CCFF

1216-37), there can be no doubt that the patent involved the work of JEDEC and was required to be disclosed. (*See* CCFF 310-14, 331-33, 335).

336. Professor Jacob also concedes that claim 7 of the ’327 patent describes a specific implementation of dual edged clocking where the DRAM “toggle[s] between two output drivers through a multiplexer.” (CX 1494 at 23; Jacob, Tr. 5548).

Response to Finding No. 336: The proposed finding is incomplete. Professor Jacob testified that using a multiplexer for outputting data, as recited in claim 7 of the ‘327 patent, “is the most reasonable implementation” of a read operation using dual-edged clocking. (Jacob, Tr. 5548-49; CCFF 1233). DDR SDRAM uses a multiplexer for outputting data on the rising and falling edge of a clock. (CCFF 1234-1237).

Because the Rambus ‘327 patent contains claims covering the most feasible way to implement the dual-edged clocking feature, as proposed to JEDEC in May 1992, December 1995 and March 1996, in a JEDEC-compliant SDRAM, and also contains claims covering DDR SDRAM as ultimately implemented in JEDEC Specification JESD 79 (June 2000). (CCFF 1216-37), there can be no doubt that the patent involved the work of JEDEC and was required to be disclosed. (*See* CCFF 310-14, 331-33, 335).

b. The Hardell Presentation Triggered No Disclosure Obligation With Respect To The ’327 Patent.

337. The Hardell presentation related to IBM’s “toggle mode” DRAM. (Kelley, Tr. 2514). IBM’s toggle mode was an asynchronous design. (Jacob, Tr. 5608; Soderman, Tr. 9398; Sussman, Tr. 1472).

Response to Finding No. 337: The proposed finding is incomplete and misleading. IBM’s toggle mode was in fact a partially asynchronous and partially synchronous part, in that it had asynchronous inputs but synchronous outputs. (CCFF 509, 629) In fact while both Professor Jacob and Howard Sussman are cited in support of Respondent’s contention that

IBM's toggle mode was an asynchronous design, both actually testified that toggle mode is partially asynchronous and partially synchronous. (Jacob, Tr. 5394; Sussman, Tr. 1471)

338. The Hardell presentation noted that it has "A-Synchronous RAS/CAS." (CX 34 at 32). This makes it an asynchronous DRAM, according to Professor Jacob's definition of asynchronous DRAMs as "those who are driven off the RAS and CAS signals where the RAS and CAS actually control the operation of the DRAM rather than a clock." (Jacob, Tr. 5394).

Response to Finding No. 338: The proposed finding is incomplete and misleading. In fact, Professor Jacob testified that IBM's toggle mode fell into a gray area between asynchronous and synchronous because it has an asynchronous capture of commands but a synchronous capture of data. (Jacob, Tr. 5608)

339. Claims 1 and 7 of the '327 patent cannot be construed as covering a JEDEC-compliant SDRAM that also incorporated dual-edge clocking as described in the Hardell presentation because such a device cannot exist. JEDEC-compliant SDRAMs are synchronous DRAMs with synchronous RAS and CAS signals; the Hardell presentation described an asynchronous DRAM with an asynchronous RAS/CAS interface. (CX 34 at 30-32).

Response to Finding No. 339: The proposed finding is incomplete and misleading. In fact as noted in the immediately preceding reply findings, the Hardell presentation described a partially asynchronous and partially synchronous DRAM. A number of JEDEC members present at the meeting testified that Mr. Hardell was proposing using both edges of the clock for transmitting data and information. (Rhoden, Tr. 443 (Mr. Hardell was "proposing using both edges of the clock for the transition of data and information inside the Synchronous DRAM."); G. Kelley, Tr. 2514 (Mr. Hardell was proposing that JEDEC use the IBM invention, "an asynchronous DRAM with a synchronous output using both edges of the clock, the rising edge of the clock and falling edge of the clock to output data."); Sussman, Tr. 1386 ("Hardell . . . is still pushing a double edge clock version of the part.") There is also testimony that a JEDEC member with intellectual property relating to dual edge clocking technology should disclose that property. (Sussman, Tr. 1386).

Because the Rambus '327 patent contains claims covering the most feasible way to implement the dual-edged clocking feature, as proposed to JEDEC in May 1992, December 1995 and March 1996, in a JEDEC-compliant SDRAM, and also contains claims covering DDR SDRAM as ultimately implemented in JEDEC Specification JESD 79 (June 2000). (CCFF 1216-37), there can be no doubt that the patent involved the work of JEDEC and was required to be disclosed. (*See* CCFF 310-14, 331-33, 335).

340. The Hardell presentation gave no details about implementation of the dual-edged clocking feature, stating simply: "dual clock edge." (CX 34 at 32).

Response to Finding No. 340: The proposed finding is incomplete. A number of JEDEC members present at the meeting testified that Mr. Hardell was proposing using both edges of the clock for transmitting data and information. (Rhoden, Tr. 443 (Mr. Hardell was "proposing using both edges of the clock for the transsition of data and information inside the Synchronous DRAM."); G. Kelley, Tr. 2514 (Mr. Hardell was proposing that JEDEC use the IBM invention, "an asynchronous DRAM with a synchronous output using both edges of the clock, the rising edge of the clock and falling edge of the clock to output data."); Sussman, Tr. 1386 ("Hardell . . . is still pushing a double edge clock version of the part.")).

Because the Rambus '327 patent contains claims covering the most feasible way to implement the dual-edged clocking feature, as proposed to JEDEC in May 1992, December 1995 and March 1996, in a JEDEC-compliant SDRAM, and also contains claims covering DDR SDRAM as ultimately implemented in JEDEC Specification JESD 79 (June 2000) (CCFF 1216-37), there can be no doubt that the patent involved the work of JEDEC and was required to be disclosed. (*See* CCFF 310-14, 331-33, 335).

341. The Hardell presentation was referenced in a memorandum discussing presentations at a meeting of a task group in Dallas in April 1992. (CX 34 at 4, 30). There was no evidence at trial that the Hardell presentation was ever balloted at JEDEC.

Response to Finding No. 341: The proposed finding is incomplete and misleading. In fact, the Hardell proposal eventually wound up in the DDR standard. (Rhoden, Tr. 445-446 ("The differences [between Mr. Hardell's presentation and the dual edge clock proposed for the DDR SDRAM ballot] was almost none. What Mr. Hardell was proposing is essentially what we ultimately wound up with in the standard for DDR."); Rhoden, Tr. 483; Kellogg, Tr. 5176).

Because the Rambus '327 patent contains claims covering the most feasible way to implement the dual-edged clocking feature, as proposed to JEDEC in May 1992, December 1995 and March 1996, in a JEDEC-compliant SDRAM, and also contains claims covering DDR SDRAM as ultimately implemented in JEDEC Specification JESD 79 (June 2000) (CCFF 1216-37), there can be no doubt that the patent involved the work of JEDEC and was required to be disclosed. (*See* CCFF 310-14, 331-33, 335). The disclosure obligation arose in connection with any JEDEC work, not only formal balloting of proposals or presentations for approval (CCFF 340). The disclosure obligation arises in connection with discussions at JEDEC (CCFF 341) and is intended to result in disclosure as early as practicable in the JEDEC process (CCFF 342).

342. Complaint Counsel did not show that a Rambus JEDEC representative had actual knowledge of the claims of the '327 patent (or any related application that led to the issuance of the '327 patent) at the time of the Hardell presentation.

Response to Finding No. 342: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

It is correct that neither the Rambus '327 patent, nor the '646 patent application on which it was based, were in existence at the time of the Hardell presentation in 1992. However, dual-edge clocking was a feature that had long been under discussion at JEDEC in connection

with the "next generation" SDRAM standard, including discussions that began before and continued throughout the time that Rambus was a member of JEDEC. (CCFF 522, 524-26, 581, 585, 623-25, 628-33, 635, 637-40, 1072, 1079, 1200-03). The JEDEC disclosure duty is a continuing duty (CCFF 346), and arises as soon as a participant knows of a relevant patent or application (CCFF 339-45). In light of the ongoing discussions at JEDEC of dual-edge clock technology, Rambus had a duty to disclose its '646 application and '327 patent promptly after they came into existence embodying claims relating to dual-edge clock technology.

c. The Survey Ballot.

343. The Survey Ballot was presented to JEDEC members as a survey to determine what features JEDEC members might want to include in future DRAMs. (JX 28 at 34-48).

Response to Finding No. 343: Complaint Counsel does not disagree. For a more complete discussion of JEDEC-work related to dual-edged clocking, *see* CCFF 620-644.

344. The Survey Ballot was circulated on or about October 30, 1995. (CX0260; Lee, Tr. 6636).

Response to Finding No. 344: Complaint Counsel does not disagree. For a more complete discussion of the Survey Ballot, *see* CCFF 637-638, 1070-1073, 1079-1082.

345. The Survey Ballot was circulated shortly *after* the September 1995 JEDEC meeting, at which Rambus made the statement that: "Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property." (RX 602 at 1; JX 27 at 4, 26).

Response to Finding No. 345: The proposed finding is incomplete and misleading to the degree that Respondent is attempting to imply that the cited Rambus statement put JEDEC members on notice that it would remain silent as to its intellectual property on all JEDEC work. In fact, the statement cited in the proposed finding was made in a Rambus letter responding to an inquiry directed to a particular SyncLink proposal that had earlier been the subject of a JEDEC presentation. (RX 602 at 1). In fact, the immediately preceding sentence to

the quoted sentence reads "At this time Rambus elects not to make a specific comment on our intellectual property position relative to the Synclink proposal. Our presence or silence . . ." (*Id.*) As Mr. Crisp reported to his Rambus colleagues later, Gordon Kelley of IBM commented concerning the Rambus letter at the September 1995 meeting that "he heard a lot of words but did not hear anything sa*id.*" (CX0711 at 166).

The proposed finding neglects to state that Mr. Crisp rendered the Rambus letter even more ambiguous by his verbal representations at the meeting. In the course of the discussion of the Rambus letter at the September 1995 Committee meeting, Mr. Crisp reminded the Committee that Rambus in the past had reported a Rambus patent to the Committee. (Crisp, Tr. 3312). This was a reference to the disclosure to the Committee of the Rambus '703 patent in September 1993. (*Id.*). Mr. Crisp was saying that Rambus was in the category of JEDEC members that had disclosed patents. (Crisp, Tr. at 3313). In fact, the entire conduct of Rambus as a JEDEC member, accomplished in large part through its principal representative Mr. Crisp, was intended to and did mislead JEDEC members concerning the extent of intellectual property claims by Rambus in the standards that were the work of JEDEC. (*See* CCRF 454).

346. Several witnesses testified that in their understanding, survey ballots were for information only and triggered no patent disclosure obligations of any kind. (Rhoden, Tr. 480, 587; Kelley, Tr. 2701; Crisp, Tr. 3517).

Response to Finding No. 346: The proposed finding is incomplete and misleading. The proposed finding cites three witnesses in support of its contention that several witnesses testified that survey ballots triggered no patent disclosure obligations. In fact, of those three one is Mr. Crisp, a less than neutral witness.

The testimony of the second witness, Mr. Rhoden, does not in fact support the contention it is cited to support. Page 480 of Mr. Rhoden's testimony makes no reference to patent obligations and on page 587 he simply states that the actual physical survey ballot may or may

not contain a patent disclosure box to check. This is, of course, far different than testifying that disclosure is not required. In fact, Mr. Rhoden testified that the duty to disclose was triggered by "discussion, presentations, ballots, anything that's taking place inside the committee." (Rhoden, Tr. 488-489).

The third witness cited by Respondent in support of the contention in the finding is Gordon Kelley. Mr. Kelley, however, testifies at the cited page that survey ballots did, in fact, require disclosure if they involved an active item of the committee. The survey ballot at issue was official Committee work and was given a ballot number (CX0260 at 1) and therefore was an active item of the committee. Further, Mr. Kelley testified elsewhere that "there were many work items that occurred on the committee that did not become standards . . . My definition says that any claim that might apply to the work of the committee it was required to disclose." (Kelley, Tr. 2705). Mr. Kelley also testified that a member that observes a presentation while it is a member and then chooses to withdraw before the matter comes to ballot is not relieved of its obligation to disclose relevant patents or patent applications. (G. Kelley, Tr. 2758).

The clear weight of the evidence shows that survey ballots did require disclosure. (Sussman, Tr. 1419 ("Q. Does the patent policy apply to a survey ballot based on your experience at JEDEC? A. And I've already answered that basically yes, as soon as possible in the discussion, we'd like to know."). Tom Landgraf of Cisco and previously of Hewlett Packard testified when questioned about the October 1995 survey ballot that not only did survey ballots require disclosure but this specific survey ballot required disclosure of patents or patent applications that related to on-chip PLL/DLL or dual edge clocking. (Landgraf, Tr. 1716-1717). There is also overwhelming evidence that disclosure was required as soon as the participant knows about patents or patent applications that might involve JEDEC work. (CCFF 339) and that the duty to disclose is not tied to any procedural formality in the JEDEC process. (CCFF 340).

347. With respect to dual-edge clocking, the result of the Survey Ballot was that there was "mixed support" for "using both edges of the clock for sampling inputs." (JX 28 at 35). The Survey Ballot provided no further details of the implementation of dual-edge clocking.

Response to Finding No. 347: The proposed finding is incomplete and misleading. In fact, the ballot itself provided further details regarding the implementation of dual-edge clocking. The Clock Background section of the survey states in part "SDRAMs currently use one clock pin, CLK, to sample all inputs" and continues "[o]ne of the most difficult specifications to obtain with an SDRAM is a fast data access time from the clock". It goes on to state that other possible issues that relate to the clock include "using both edges of the clock to sample the inputs to allow a lower clock frequency and thus lower related power consumption." (CX0260 at 12) Further, two specific comments relating to dual edge clock technology were recorded in the results of the survey ballot, both supportive of using the technology. (JX0028 at 45 ("Mitsubishi . . . Dual CLK (input/output) is simple and effective.") ("HP . . . Use positive edge for address/command & both edges for data.")). There was also testimony that the question in the survey related to dual edge clocking. (Calvin, Tr. 1033 ("Q. So, in your understanding, this SDRAMs benefitting from both edges of the clock for sampling inputs, that's in your understanding dual edge clock? A. I wouldn't know how to interpret both edges of a clock any other way. A clock only has two edges."); Lee, Tr. 6689 ("Q. Now, based on your understanding when you reviewed this survey ballot in late 1995, what, if any, was the relationship between dual edge clocking and the clocking scheme being asked about in question 3.9-4? A. In this case, they're asking if we felt that the SDRAM would benefit -- the future SDRAMs would benefit from using both edges of the clock for sampling inputs. In other words, using a dual edge clock. Q. So, in other words, using both edges of the clock was similar to using or the same as using dual edge clock? A. Yes.")).

In short, the dual-edge clocking under consideration in the survey ballot in the Fall of 1995 was sufficiently clearly defined to put any good faith participant on notice that the claims embodied in the Rambus '646 application, which would become the Rambus '327 patent, were relevant to the work of JEDEC. The duty to disclose is triggered by the good faith knowledge or belief of a participant that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335.

348. Complaint Counsel did not show that a Rambus JEDEC representative had actual knowledge of the claims of the '327 patent (or any related application that led to the issuance of the '327 patent) at the time of the Survey Ballot.

Response to Finding No. 348: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. The proposed finding is also without factual basis, for the reasons set forth in CCRF 331.

d. The Samsung Presentation.

349. With respect to dual-edge clocking, the Samsung presentation stated only that "Data in sampled at both edge of Clock into memory." (JX 31 at 71). No further details of the implementation of dual edge clocking were provided.

Response to Finding No. 349: The proposed finding is incomplete. The presentation went on to state: "Use both edges of the Strobe clock to sample the memory Data into Controller" (JX0031 at 71)

Further, a number of witnesses testified that the Samsung presentation included a dual edge clock. (Rhoden, Tr. 512 (Responding to a question as to what was meant by the statement in the proposed finding, Mr. Rhoden stated "this would be something we talked about yesterday, a dual edge clocking or clocking with a rising and falling edge. It's simply -- basically the same type of approach to sampling data. So, if you had rising edge and falling edge, you would be

sampling both edges of the clock."); Calvin, Tr. 1035 (Responding to a question as to what was meant by the statement in the proposed finding: "Q. Did you understand at this time that what Samsung was proposing in this presentation was dual edge clock? A. That was my understanding, although I don't know that they specifically said those terms."); Landgraf, Tr, 1719-1720 ((Responding to a question as to what was meant by the statement in the proposed finding: "What Samsung is doing is they are proposing a clocking scheme for next generation SDRAM, and one of the salient points is that the data into or data out of the memory device is to be sampled on both edges of the -- of the clock. As I mentioned before, using a single clock, they refer to a single clock here, and so you would sample data in on one edge and another piece of data on the second edge, et cetera, so... Q. In your understanding, does that describe dual edge clock? A. Yes, this is a definition of a dual edge clock."); G. Kelley, Tr. 2581-2582 (Responding to a question as to what was meant by the statement in the proposed finding: "My understanding is that they were proposing continued consideration of what they called the double data rate, where you clocked the data on the rising and falling edges of a strobe clock. Q. You referred to double data rate I believe. Is that the same as dual-edge clock? A. That's the same as dual-edge clock, yes.").

In short, the dual-edge clocking under consideration at the time of the Samsung presentation was sufficiently clearly defined to put any good faith participant on notice that the claims embodied in the Rambus '646 application, which would become the Rambus '327 patent, were relevant to the work of JEDEC. The duty to disclose is triggered by the good faith knowledge or belief of a participant that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335.

350. There was no evidence at trial that the Samsung presentation was ever balloted at JEDEC.

Response to Finding No. 350: The proposed finding is incomplete. The dual edge technology described in the Samsung presentation was included in the JEDEC DDR SDRAM standard. (CCFF 656; Landgraf, Tr. 1720 (responding to a question as to whether the Samsung presentation required disclosure of related intellectual property, Mr. Landgraf pointed out that "the committee was driving towards a set of features for next generation SDRAM for higher performance, and all of these were in the direction of a proposed standard. So, all these presentations were bits and pieces that ended up into the double data rate standard.")).

Because the Rambus '327 patent contains claims covering the most feasible way to implement the dual-edged clocking feature, as proposed to JEDEC in May 1992, December 1995 and March 1996, in a JEDEC-compliant SDRAM, and also contains claims covering DDR SDRAM as ultimately implemented in JEDEC Specification JESD 79 (June 2000) (CCFF 1216-37), there can be no doubt that the patent involved the work of JEDEC and was required to be disclosed. (*See* CCFF 310-14, 331-33, 335). The disclosure obligation arose in connection with any JEDEC work, not only formal balloting of proposals or presentations for approval (CCFF 340). The disclosure obligation arises in connection with discussions at JEDEC (CCFF 341) and is intended to result in disclosure as early as practicable in the JEDEC process (CCFF 342).

351. Complaint Counsel did not show that a Rambus JEDEC representative had actual knowledge of the claims of the '327 patent (or any related application that led to the issuance of the '327 patent) at the time of the Samsung presentation.

Response to Finding No. 351: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. The proposed finding is also without factual basis, for the reasons set forth in CCRF 331.

e. Claims 1 and 7 of the '327 Patent Do Not Cover the Presentations Raised by Complaint Counsel.

352. Claim 1 of the '327 patent cannot be construed as covering a JEDEC-compliant SDRAM that also incorporated dual-edge clocking as described in the Hardell presentation, the Survey Ballot, or the Samsung presentation, because none of those presentations provided any implementation details and because none included the implementation details required by claim 1.

Response to Finding No. 352: The proposed finding is misleading and inaccurate. Although the presentations did not explicitly mention the limitations recited in claim 1 of the '327 patent, a DRAM engineer would understand that each of those limitations is inherent in an SDRAM that incorporates the proposed dual-edged clocking feature. (CCFF 1218-1223).

In any event, the proposed finding does not support a conclusion that a patent or patent application relates to JEDEC work only if every limitation of a patent claim within that patent or application is present in a JEDEC-compliant device. In fact, the scope of a patent's coverage usually is not known with certainty until all relevant patent infringement litigation has been resolved. JEDEC requires its programs be conducted in good faith. *See* CCFF 310-14. The JEDEC disclosure requirement does not apply only where there is a determination that any and all products built to conform to the standard, in all possible implementations, will infringe the patent or patent application. Instead, the duty to disclose is triggered by the good faith knowledge or belief of a participant that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335.

353. Claim 7 of the '327 patent cannot be construed as covering a JEDEC-compliant SDRAM that also incorporated dual-edge clocking as described in the Hardell presentation, the Survey Ballot, or the Samsung presentation, because none of those presentations provided any implementation details and because none included the implementation details required by claim 7.

Response to Finding No. 353: The proposed finding is misleading and inaccurate. Although the presentations did not explicitly mention the limitations recited in claim 7 of the '327 patent, a DRAM engineer would understand that each of those limitations is either inherent in an SDRAM that incorporates the proposed dual-edged clocking feature, or the most reasonable way to implement that feature. (CCFF 1229-1233). The Rambus '327 patent contains claims covering the most feasible way to implement the dual-edged clocking feature, as proposed to JEDEC in May 1992, December 1995 and March 1996, in a JEDEC-compliant SDRAM, and also contains claims covering DDR SDRAM as ultimately implemented in JEDEC Specification JESD 79 (June 2000) (CCFF 1216-37).

In any event, the proposed finding does not support a conclusion that a patent or patent application relates to JEDEC work only if every limitation of a patent claim within that patent or application is present in a JEDEC-compliant device. In fact, the scope of a patent's coverage usually is not known with certainty until all relevant patent infringement litigation has been resolved. JEDEC requires its programs be conducted in good faith. *See* CCFF 310-14. The JEDEC disclosure requirement does not apply only where there is a determination that any and all products built to conform to the standard, in all possible implementations, will infringe the patent or patent application. Instead, the duty to disclose is triggered by the good faith knowledge or belief of a participant that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335.

f. Claims 1 and 7 of the '327 Patent Do Not Cover the JEDEC DDR SDRAM Standard.

354. Devices could be built to the JEDEC DDR SDRAM standard without infringing Claim 1 of the '327 patent. (Fliesler, Tr. 8860-61). Claim 1 calls for the use of a clock signal to write data to the DRAM, while the DDR SDRAM standard uses a different signal, the DQS strobe signal, for that purpose. (CX 1494 at 23; CX 234 at 164; JX 57 at 5; Fliesler, Tr. at 8861; Jacob, Tr. 5641-42). A clock signal and a strobe signal are different: a clock is a "free-running"

signal, that is running all the time, while the strobe in DDR SDRAMs is not free-running. (Macri, Tr. 4634).

Response to Finding No. 354: The proposed finding is inaccurate because the term "clock signal," as it is used in Claim 1 of the '327 patent, can reasonably be interpreted as a periodic signal, which would include the DQS signal used in DDR SDRAM. (Jacob, Tr. 5553-54). An engineer could reasonably conclude that devices built to the JEDEC DDR SDRAM standard infringe claim 1 of the '327 patent. (CCFF 1224-1228).

Mr. Fliesler's testimony to the contrary is unreliable. Patent claims must be interpreted as they would be understood by a person ordinary skill in the art. (Fliesler, Tr. 8933). Unlike Professor Jacob, Mr. Fliesler is an attorney, and not a person skilled in the art of DRAM design and architecture. (Fliesler, Tr. 8867-69, 8781). Even in his work as a patent attorney, Mr. Flielser has had minimal exposure to technical DRAM issues. (Fliesler, Tr. 8782). Moreover, Mr. Fliesler did not discuss his claim interpretation, including his understanding of the term "clock" in claim 1, and his analysis of the DDR SDRAM standard with any person skilled in the pertinent art. Rather, he relied on his own analysis. (Fliesler, Tr. 8783, 8934, 8948).

In any event, the proposed finding does not support a conclusion that a patent or patent application relates to JEDEC work only if every limitation of a patent claim within that patent or application is present in a JEDEC-compliant device. In fact, the scope of a patent's coverage usually is not known with certainty until all relevant patent infringement litigation has been resolved. JEDEC requires its programs be conducted in good faith. *See* CCFF 310-14. The JEDEC disclosure requirement does not apply only where there is a determination that any and all products built to conform to the standard, in all possible implementations, will infringe the patent or patent application. Instead, the duty to disclose is triggered by the good faith

knowledge or belief of a participant that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335.

355. Devices could be built to the JEDEC DDR SDRAM standard without infringing Claim 7 of the '327 patent. (Fliesler, Tr. 8861-2). Claim 7 calls for a multiplexer in the DRAM output path while the DDR SDRAM standard does not require the use of a multiplexer. (CX 1494 at 23; CX 234; Fliesler, Tr. 8863; Jacob, Tr. 5642-43).

Response to Finding No. 355: The proposed finding is inaccurate. Schematic drawings in the JEDEC DDR SDRAM standard show a "MUX," indicating that the standard requires a multiplexer. (CCFF 1234-1237; JX0057 at 8; Jacob, Tr. 5558-60). Mr. Fliesler's testimony to the contrary is unreliable for the reasons discussed above. CCRF 354. He did not discuss his view that the DDR SDRAM standard does not require a multiplexer with any technical experts. (Fliesler, Tr. 8948).

In any event, the proposed finding does not support a conclusion that a patent or patent application relates to JEDEC work only if every limitation of a patent claim within that patent or application is present in a JEDEC-compliant device. In fact, the scope of a patent's coverage usually is not known with certainty until all relevant patent infringement litigation has been resolved. JEDEC requires its programs be conducted in good faith. *See* CCFF 310-14. The JEDEC disclosure requirement does not apply only where there is a determination that any and all products built to conform to the standard, in all possible implementations, will infringe the patent or patent application. Instead, the duty to disclose is triggered by the good faith knowledge or belief of a participant that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335.

356. Rambus has not asserted the '327 patent against any SDRAM or DDR SDRAM devices. (Patent tree attached to the Parties' First Set of Stipulations).

Response to Finding No. 356: The proposed finding is misleading. Rambus did consider the '327 patent to cover dual-edged clocking feature. (CCFF 1684-85). It asserted that

patent against a dual-edged clocking feature used by Mosys. (CCFF 1100-05). Moreover, Rambus has asserted patents, which like the '327, flow from and claim priority based on the '898 application, over the dual-edged clocking feature of a DDR SDRAM. (CCFF 858, 2022).

g. Summary of Findings Regarding Undisclosed Patents.

357. Complaint Counsel did not meet their burden of proving that Rambus had any undisclosed patents while it was a JEDEC member that were required to be disclosed under EIA/JEDEC policies.

Response to Finding No. 357: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Further, the proposed finding is inaccurate. Complaint Counsel has demonstrated that the '327 patent did cover proposals for dual-edged clocking made while Rambus was a member of JEDEC. (CCFF 1216-1237; CCRF 335-56). This showing goes far beyond what is necessary to demonstrate a disclosure duty under the JEDEC policy. In fact, the scope of a patent's coverage usually is not known with certainty until all relevant patent infringement litigation has been resolved. JEDEC requires its programs be conducted in good faith. *See* CCFF 310-14. The duty to disclose is triggered by the good faith knowledge or belief of a participant that a patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335.

358. Complaint Counsel did not meet their burden of proving that Rambus's JEDEC representative, Richard Crisp, had actual knowledge of the claims contained in the '327 patent during the time that Rambus was a JEDEC member.

Response to Finding No. 358: . The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket

9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. The proposed finding is also without factual basis, for the reasons set forth in CCRF 331.

359. Complaint Counsel did not meet their burden of proving that the claims of the '327 patent were "essential" to or "read on" any technology described in any presentation made while Rambus was a JEDEC member.

Response to Finding No. 359: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Further, the proposed finding is inaccurate. The Rambus '327 patent contains claims covering the most feasible way to implement the dual-edged clocking feature, as proposed to JEDEC in May 1992, December 1995 and March 1996, in a JEDEC-compliant SDRAM, and also contains claims covering DDR SDRAM as ultimately implemented in JEDEC Specification JESD 79 (June 2000). (CCFF 1216-37).

In any event, the proposed finding is inaccurate in asserting that the intellectual property required to be disclosed under the JEDEC policy was limited to intellectual property deemed "essential" to or that "read on" JEDEC work. (CCFF 335, 338). In fact, the scope of a patent's coverage usually is not known with certainty until all relevant patent infringement litigation has been resolved. JEDEC requires its programs be conducted in good faith. *See* CCFF 310-14. The JEDEC disclosure requirement is triggered by the good faith knowledge or belief of a participant that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335.

360. Complaint Counsel did not meet their burden of proving that the claims of the '327 patent were "essential" to or "read on" any technology that was balloted while Rambus was a JEDEC member.

Response to Finding No. 360: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Further, the proposed finding is inaccurate. Complaint Counsel has demonstrated that the '327 patent did cover proposals for dual-edged clocking made while Rambus was a member of JEDEC, and which were the subject of a survey ballot in the Fall of 1995. (CCFF 1216-1237; CCPF 335-56). Proposals for dual-edge clocking were the subject of discussions that began before and continued throughout the time that Rambus was a member of JEDEC. (CCFF 522, 524-26, 581, 585, 623-25, 628-33, 635, 637-40, 1072, 1079, 1200-03). Dual-edge clocking was balloted for approval, leading ultimately to its inclusion in the JEDEC DDR SDRAM standard, after Rambus withdrew as a JEDEC member.

The proposed finding is misleading insofar as it suggests that disclosure was required only at the time a proposal was balloted for approval. In fact, the disclosure obligation arose in connection with any JEDEC work, not only formal balloting of proposals or presentations for approval (CCFF 340). The disclosure obligation arises in connection with discussions at JEDEC (CCFF 341) and is intended to result in disclosure as early as practicable in the JEDEC process (CCFF 342).

2. Rambus Had No Undisclosed Patent Applications That It Was Required To Disclose To JEDEC.

361. The parties have stipulated that prior to the adoption of the JEDEC SDRAM standard in 1993, Rambus had no undisclosed claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard. (The Parties' First Set of Stipulations, Stipulation 9).

Response to Finding No. 361: This proposed finding accurately references of the identified stipulation. Despite the belief of Rambus that the JEDEC SDRAM standard embodied its intellectual property (*see, e.g.,* CCFF 811, 853, 862-66) and despite its efforts to amend and perfect its patent applications to cover crucial components of the SDRAM standard by filing, inter alia, an amendment to its '651 application on May 17, 1993, a little more than a week before the JEDEC Council adopted the SDRAM standard (*see, e.g.*, CCFF 809, 810, 832, 834), prior to the time the JEDEC SDRAM standard was formally adopted in November 1993 (CCFF 977) Rambus had not successfully amended its patent applications to include claims that clearly read on the content of the SDRAM standard.

However, throughout the time Rambus was a member of JEDEC it continued its efforts to perfect its patent claims and did amend its patent applications to state claims that clearly read on crucial elements of the SDRAM standard. These include the January 1995 amendments to Rambus patent application 07/847,961 (the '961 application), which cover the the programmable burst length and programmable CAS latency features of JEDEC-compliant SDRAMs. (CCFF 1125-63). In addition, the June 1995 amendments to Rambus patent application no. 08/469,490 (the '490 application), which was a continuation of the '961 application, contained claims covering a JEDEC-compliant SDRAM, the use of such an SDRAM, and a computer system incorporating a JEDEC-compliant SDRAM. (CCFF 1164-82).

During the time Rambus was a member of JEDEC it also made efforts to perfect its patent claims pertaining to technologies under discussion at JEDEC for inclusion in the "next generation" SDRAM standard, which ultimately became the DDR standard. Amendments dated June 28, 1993, to Rambus patent application 07/847,692 (the '692 application) contained claims covering a phase lock loop (PLL) incorporated into a JEDEC-complaint SDRAM. (CCFF 963-966, 1183-1198). This is a technology that was discussed at JEDEC during the period Rambus

was a member, including in a September 14, 1994, presentation by NEC Corporation to JEDEC Committee 42.3 proposing that the SDRAM standard incorporate an on-chip PLL. (CCFF 1009-17, 1186; *see* CCFF 843, 855-57, 1072, 1079, 1080). The amendments to the Rambus '692 patent application were specifically intended by Rambus to target "future SDRAM" (CCFF 963), and had been discussed by Rambus executives with Rambus patent counsel as early as September 1992. (CCFF 932-36).

On September 6, 1994, while it was a JEDEC member, Rambus filed a preliminary amendment to Rambus patent application 08/222,646 (the '646 application) that contained claims that covered a JEDEC-compliant SDRAM incorporating a proposed dual-edged clocking feature. (CCFF 1008, 1199-1215). Dual-edge clocking was another feature that had long been under discussion at JEDEC in connection with the "next generation" SDRAM standard, including discussions that began before and continued throughout the time that Rambus was a member of JEDEC. (CCFF 522, 524-26, 581, 585, 623-25, 628-33, 635, 637-40, 1072, 1079, 1200-03). The United States Patent and Trademark Office sent Rambus patent counsel a Notice of Allowance of claims with respect to the '646 application on October 6, 1995, while Rambus was a JEDEC member; a Notice of Allowance occurs when the patent office has reason to believe that claims in a particular application should be issued. (CCFF 1076).

The '646 application issued as Patent No. 5,513,327 (the '327 patent) to Rambus on April 30, 1996, before Rambus withdrew as a JEDEC member. (CCFF 1074-1077, 1214). The Rambus '327 patent contains claims covering the most feasible way to implement the dual-edged clocking feature, as proposed to JEDEC in May 1992, December 1995 and March 1996, in a JEDEC-compliant SDRAM, and also contains claims covering DDR SDRAM as ultimately implemented in JEDEC Specification JESD 79 (June 2000). (CCFF 1216-37).

362. Complaint Counsel allege that the following claims of Rambus patent applications should have been disclosed to JEDEC:

(1) Claims 151, 159, 160, 164, 165 and 168 of application serial no. 07/847,961 (the "'961 application"), because they allegedly cover JEDEC-compliant SDRAMs (Nusbaum, Tr. 1544-45; Jacob, Tr. 5507, 5523-28);
(2) Claims 183, 184, and 185 of application serial no. 08/469,490 (the "'490 application"), because they allegedly cover JEDEC-compliant SDRAMs (Nusbaum, Tr. 1572-3; Jacob, Tr. 5528-32);
(3) Claims 151, 152, 166 and 167 of application serial no. 07/847,692 (the "'692 application"), because they allegedly cover a presentation made by NEC that is contained in the September 1994 minutes of the JEDEC 42.3 subcommittee (JX 21 at 91; Nusbaum, Tr. 1584; Jacob, Tr. 5535, 5540); and
(4) Claim 151 of application serial no. 08/222,646 (the "'646 application), because it allegedly covers the Hardell presentation, the Survey Ballot, and the Samsung presentation (Nusbaum, Tr. 1597-98; Jacob, Tr. 5550).

Response to Finding No. 362: The proposed finding is an incomplete statement of Complaint Counsel's allegations. Complaint Counsel alleges that Rambus should have disclosed its patent and potential patent rights to JEDEC, including (but not limited to) the '961, '490, '692 and '646 applications, based on Rambus's understanding of its patent rights, its extensive efforts to obtain patent rights covering a JEDEC-compliant SDRAM and JEDEC-compliant SDRAMs incorporating JEDEC work and proposals, throughout the period that it was a JEDEC member. (CCFF 867-1121). During the period that it was a JEDEC member Rambus in fact knew of a wide variety of technologies and features under discussion at JEDEC, beyond those specified in this proposed finding, that involved what it believed were its intellectual property. (*See* CCFF 856-57). Rambus never disclosed to JEDEC its belief that these technologies and features were its intellectual property, or its efforts to secure patent rights over these aspects of JEDEC standards work. (CCFF 859-66).

a. The '961 Application Does Not Cover JEDEC-Compliant SDRAMs.

363. The claims of the '961 application that Complaint Counsel allege covered JEDEC-compliant SDRAMs, claims 151, 159, 160, 164, 165 and 168, were added in an amendment filed on January 6, 1995, well after the SDRAM standard was adopted. (CX 1504 at 216-26;

Nusbaum, Tr. 1544-45; Fliesler, Tr. 8847). In an office action dated April 16, 1995, the patent examiner rejected all of the claims pending in the '961 application. (CX 1504 at 227-39). Among other grounds, claims 151-165 were rejected as indefinite. (CX 1504 at 229). All of the claims in the '961 application that allegedly covered JEDEC-compliant SDRAMs were cancelled by Rambus on June 23, 1995. (CX 1504 at 258; Fliesler, Tr. 8847-48).

Response to Finding No. 363: The proposed finding is accurate in that it confirms that the listed claims of the '961 application were pending during the time that Rambus was a member of JEDEC. These were claims covering, or that a reasonable engineer could interpret as covering, the programmable burst length and programmable CAS latency features of JEDEC-compliant SDRAMs. (Nusbaum, Tr. 1540-72; Jacob, Tr. 5507-28; CCFF 1125-63).

The proposed finding is incomplete and misleading insofar as it suggests that the cancellation of these claims in June 1995 meant that Rambus no longer claimed intellectual property rights in programmable burst length and programmable CAS latency features of JEDEC-compliant SDRAMs. Rambus in fact has asserted patents against JEDEC-member companies using programmable CAS latency and programmable burst length technologies in JEDEC-compliant SDRAMs, SGRAMs, DDR SDRAMs and DDR SGRAMs, as well as memory controllers that interface with them. (CCFF 1961-65, 1967-69, 1971-72, 1974). Every patent that Rambus has asserted against SDRAM and DDR SDRAM products in patent litigation resulted, like the '961 application, from continuation or divisional patent applications flowing from the original '898 application. The asserted patents, like the '961 application, claim the benefit of the '898 application's April 18, 1990 filing date. (First Stipulation, no. 22; Exhibit A to First Stipulation, no. 22; Nusbaum Tr. 1506-1508; *see also* DX0014).

The proposed finding also is incomplete and misleading insofar as it suggests that Rambus was under no duty to disclose its '961 application because at the time it was pending the JEDEC SDRAM standard had already been adopted. The JEDEC disclosure duty is not tied to any procedural formality in the JEDEC process (CCFF 340) and is a continuing duty for a

JEDEC member when relevant patents or patent applications come to the member's attention even after a standard has issued (CCFF 346). Moreover, programmable CAS latency and programmable burst length were continuing subjects of discussion at JEDEC in connection with the future SDRAM discussions. (CCFF 586-93). These ongoing discussions should have prompted disclosure by Rambus, had it been acting in good faith.

364. The Federal Circuit has concluded that claims 151, 159, 160, 164, 165 and 168 of the '961 application would not read on a device built to the JEDEC SDRAM standard. (Fliesler, Tr. 8848-51). The Federal Circuit stated:

> "This court has examined the claims of the cited applications [which includes the '961 application] as well as the relevant portions of the SDRAM standard. Based on this review, this court has determined that substantial evidence does not support the finding that these applications had claims that read on the SDRAM standard."

Rambus Inc. v. Infineon Technologies AG, 318 F.3d 1081, 1103 (Fed. Cir. 2003). The Court further held that "claims in the '961 application were limited to the device identifier feature" that is not "present in the SDRAM standard." (*Id.*).

Response to Finding No. 364: The proposed finding is misleading. The Federal Circuit's sole statement explicitly referring to the '961 application was that the "claims in the '961 application were limited to the device identifier feature." *Id.* The court made no particular reference to claims 151, 159, 160, 164, 165 and 168. The court identified no language in any claim of the '961 application, including those relied on here by Complaint Counsel, that required a device identifier feature. The court further stated that the parties had not developed evidence concerning the proper interpretation of the claims in the '961 application, either at trial or on appeal. *Id.* at 1104 ("Infineon does not directly address Rambus's arguments" that its application claims do not cover a JEDEC-compliant SDRAM); *Id.* at 1117 (Prost, J., dissenting) ("I do not believe that we, as an appellate court of review, are in a position to make this finding [that

Rambus had no claims relating to the SDRAM standard] because neither party appears to have given the jury the necessary evidence to make such an analysis in the first instance.").

There is no such insufficiency of evidence on the record here. In contrast to the record in that other proceeding as described by the Federal Circuit, Complaint Counsel here have presented particular and detailed testimony that claims 151, 159, 160, 164, 165 and 168 were not limited to a device identifier feature and that those claims covered a JEDEC-compliant SDRAM. (CCFF 1128-1163). Some claims of the '961 application contain clear limitations to a device identifier feature. For instance, claim 161 recites "an identification register" that stores "an identification number that uniquely identifies the semiconductor device." (CX1504 at 222). This suggests that claim 160, from which claim 161 depends, should not be interpreted as requiring a device identifier feature. (CCFF 1139). Moreover, Rambus's own patent expert, Mr. Fliesler, presented no contrary explanation and no testimony that would support the Federal Circuit's statement concerning the '961 application. He did not offer an independent opinion that claims 151, 159, 160, 164, 165 and 168 were limited to a device identifier feature. (Fliesler, Tr. 8937).

In short, the Federal Circuit's conclusion, which was based firmly on its interpretation of the limited record in the case before it, is not persuasive in light of the abundant and detailed evidence in the record here.

365. Complaint Counsel did not show that Rambus's JEDEC representative had actual knowledge of claims 151, 159, 160, 164, 165 or 168 of the '961 application while Rambus was a JEDEC member.

Response to Finding No. 365: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

In fact, the record could not be clearer that Richard Crisp had broad ongoing actual knowledge of the developing scope of the Rambus patent claims based on his meetings and conversations with patent attorney Lester Vincent, his work helping to draft some of the relevant patent claims, and through his close involvement with other Rambus executives, throughout the period he served as Rambus representative to JEDEC. (*See* CCFF 867-1114, CCRF 288). Furthermore, in addition to Mr. Crisp's knowledge, if others within Rambus knew that Rambus patents or patent applications might be involved in JEDEC work, they had an obligation to inform Mr. Crisp or another Rambus representative at JEDEC, so that they could inform JEDEC. (CCFF 334). A number of other Rambus officers and employees had knowledge both of events at JEDEC (in part through Mr. Crisp's trip reports) and the scope of pending Rambus patent claims. (*See* CCFF 867-1114, CCRF 288).

The record contains substantial evidence that Mr. Crisp was well aware of Rambus claims to programmable CAS latency and programmable burst length technology. (CCFF 900-01 (May 1992 Crisp proposal to add claims covering use of mode register to control latency and asking about "blocks"); 910 (late May 1992 telephone conversation between Crisp and Vincent); 920 (June 1992 telephone conversation between Crisp and Vincent); 928 (August 1992 telephone conversation between Crisp and Vincent); 932-36 (September 1992 meeting between Crisp and Vincent regarding programmable CAS latency, multiple open rows (banks), on-chip PLLs and source synchronous clocking); 947-49 (February 1993 Crisp e-mail identifying programmable access latency, multiple open rows (banks) and on-chip PLL/DLL circuit as claims in process); 955, 958 (May 1993 conference among Crisp, Farmwald and Vincent regarding preliminary amendments, including the '651 regarding programmable access time); 962-66 (June 1993 e-mail exchange with Fred Ware confirming among other things that claims covering programmable CAS latency, directed at SDRAMs, had been filed); 1010-15 (September 1994 Crisp and Roberts

e-mails recognizing that Rambus might have to fight patent infringement litigation with JEDEC members regarding use of on-chip PLL, programmable access latencies and other technologies); 1018-23 (October 1994 e-mails on same subject); 1045 (May 1995 Crisp e-mail noting that Rambus pending patent claims involving low swing signaling and programmable access latency might apply to the SyncLink proposal at JEDEC); 1050-55 (Crisp review of patents and applications and work with Vincent regarding claims to cover SyncLink in June-September 1995).

Complaint Counsel is unable to establish whether Mr. Crisp received copies of the amendments to the '961 application at the time they were filed in part because Lester Vincent, acting at the instructions of Rambus, destroyed copies of his correspondence with Rambus from the left-hand side of many of his files. CCFF 1746-48. In any event, Mr. Crisp had full access to all of Rambus's patents and patent applications, and reviewed a number of them in June 1995. CCFF 1050).

Furthermore, in addition to Mr. Crisp's knowledge, others within Rambus knew that Rambus patents or patent applications might be involved in JEDEC work and had an obligation to inform Mr. Crisp or another Rambus representative at JEDEC, so that they could inform JEDEC. (CCFF 334). A number of other Rambus officers and employees had knowledge both of events at JEDEC (in part through Mr. Crisp's trip reports) and the scope of Rambus's pending patent claims, including Rambus claims to programmable CAS latency and programmable burst length technology. (CCFF 900-01 (Vice President Roberts meeting with Vincent regarding use of mode register to control latency); 911-18 (June 1992 draft business plan, sent by Tate to the Board of Directors: "we believe that Sync DRAMs infringe on some claims in our filed patents; and that there are additional claims we can file for our patents that cover features of Sync DRAMs."); 938 (presentation to Board of Directors regarding the status of SDRAM activity at

JEDEC and the Rambus patent strategy); 947-49 (Vice President Roberts copied on February 1993 Crisp e-mail identifying programmable access latency, multiple open rows (banks) and on-chip PLL/DLL circuit as claims in process); 955, 958 (Director Farmwald involved in May 1993 conference with Vincent regarding preliminary amendments, including the '651 regarding programmable access time); 962-66 (Director Farmwald and Vice President Roberts copied on June 1993 e-mails confirming that claims covering programmable CAS latency, directed at SDRAMs, had been filed); 981 (conference among CEO Tate, Vice President Roberts, CFO Harmon and Mr. Vincent regarding enforcement of Rambus patents against Synchronous DRAMs, with specific reference to low voltage swing, programmable CAS latency and on-chip PLLs); 987-92 (Vice President Roberts' letter to Vincent proposing to add claims covering use of registers to control CAS latency, use of multiple banks and clocking data on both edges of the clock); 1010-15 (all executives copied on September 1994 Crisp and Roberts e-mails recognizing that Rambus might have to fight patent infringement litigation with JEDEC members regarding use of on-chip PLL, programmable access latencies and other technologies); 1018-23 (all executives copied on October 1994 e-mails on same subject); 1045 (all executives copied on May 1995 Crisp e-mail noting that Rambus pending patent claims involving low swing signaling and programmable access latency might apply to the SyncLink proposal at JEDEC); 1050-55 (Crisp review of patents and applications and work with Vincent regarding claims to cover SyncLink in June-September 1995); 1058 (meetings between CEO Tate and in-house counsel Diepenbrock regarding claims to cover current and future SDRAMs); 1073 (when they saw the JEDEC survey ballot, Vice President Mooring and others thought Rambus had invented certain key features)).

In short, there is no credible basis to suggest that Mr. Crisp and those working with him at Rambus and knowledgeable about the company's participation in JEDEC were not well aware

of the claims by Rambus to ownership of the programmable CAS latency and programmable burst length features embodied in the SDRAM standard.

b. The '490 Application Does Not Cover JEDEC-Compliant SDRAMs.

366. The claims of the '490 application that Complaint Counsel allege covered JEDEC-compliant SDRAMs, claims 183, 184 and 185, were added in a preliminary amendment filed on June 23, 1995, well after the SDRAM standard was adopted in 1993. (CX 1504 at 258, 264-66; Nusbaum, Tr. 1572-73; Fliesler, Tr. 8852). After a restriction requirement from the patent office, Rambus elected to pursue other claims. Claims 183, 184 and 185 were withdrawn from further consideration as of November 27, 1995. (CX 1504 at 274-75; Fliesler, Tr. 8852-54).

Response to Finding No. 366: The proposed finding is accurate in that it confirms that the listed claims of the '490 application were pending during the time that Rambus was a member of JEDEC. These were claims covering, or that a reasonable engineer could interpret as covering, JEDEC-compliant SDRAMs, and computer systems incorporating JEDEC-compliant SDRAMs, with the programmable CAS latency feature. (Nusbaum, Tr. 1573-1578; Jacob, Tr. 5528-32; CCFF 1164-82).

The proposed finding is incomplete and misleading, however, in its allegations concerning the withdrawal of the referenced claims. Rambus did not formally withdraw claims 183-185 from further consideration by the PTO until February 26, 1996. (CX1504 at 279) ("Please cancel claims . . . 183-185 without prejudice to the filing of continuations or divisionals")). Moreover, Rambus resubmitted those claims to the PTO on February 10, 1997, in application 08/798,520, which also claims priority to the '898 application. (CX1509 at 187-89; CX1504 at 264-266; First Stipulation, no. 22; Exhibit A to First Stipulation, no. 22; *see also* DX0014).

The withdrawal of these claims did not mean that Rambus no longer claimed intellectual property rights in JEDEC-compliant SDRAMs with the programmable CAS latency feature. Rambus in fact has asserted patents against JEDEC-member companies using programmable

CAS latency in JEDEC-compliant SDRAMs, SGRAMs, DDR SDRAMs and DDR SGRAMs, as well as memory controllers that interface with them. (CCFF 1961-65, 1967-69, 1971-72, 1974). Every patent that Rambus has asserted against SDRAM and DDR SDRAM products in patent litigation resulted, like the '490 application, from continuation or divisional patent applications flowing from the original '898 application. The asserted patents, like the '490 application, claim the benefit of the '898 application's April 18, 1990 filing date. (First Stipulation, no. 22; Exhibit A to First Stipulation, no. 22; Nusbaum Tr. 1506-1508; *see also* DX0014).

The proposed finding also is incomplete and misleading insofar as it suggests that Rambus was under no duty to disclose its '490 application because at the time it was pending the JEDEC SDRAM standard had already been adopted. The JEDEC disclosure duty is not tied to any procedural formality in the JEDEC process (CCFF 340) and is a continuing duty for a JEDEC member when relevant patents or patent applications come to the member's attention even after a standard has issued (CCFF 346). Moreover, programmable CAS latency were continuing subjects of discussion at JEDEC in connection with the future SDRAM discussions. (CCFF 586-93). These ongoing discussions should have prompted disclosure by Rambus, had it been acting in good faith.

367. Claims 183, 184 and 185 of the '490 application are substantially similar to the claims raised by Complaint Counsel in the '961 application, which the Federal Circuit has held do not read on SDRAMs. (Nusbaum, Tr. 1572, 1629-30).

Response to Finding No. 367: The proposed finding does not support the conclusion that the claims of the '490 application are limited to a device identifier feature or that they do not cover a JEDEC-compliant SDRAM. The Federal Circuit decision made no mention of the '490 application. *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1103 (Fed. Cir. 2003). Complaint counsel has presented detailed and specific evidence that claims 183-185 of the '961 application cover a JEDEC-compliant SDRAM. (CCFF 1164-1182). These

circumstances mean that the conclusion of the Federal Circuit has little relevance to the record here. (*See* CCFF 364).

368. Claims 183 and 184 contain the limitation that the semiconductor device be operative to wait for the access time "in response to a request specifying the semiconductor device." (CX 1504 at 264-65). Claim 185 contains the similar limitation that the semiconductor device wait the access time before responding "to transaction requests specifying the semiconductor device." (CX 1504 at 265-66).

Response to Finding No. 368: Complaint Counsel does not disagree. For a complete discussion of claims 183-184, *see* CCFF 1164-82.

369. Claims 183, 184 and 185 of the '490 application would not cover a device built to the JEDEC SDRAM standard. (Fliesler, Tr. 8855). The limitation that the request "specify[] the semiconductor device" is specific language calling for a device identifier feature that is not a part of the JEDEC SDRAM standard. (Fliesler, Tr. 8943-44). Because this limitation is not found in JEDEC-compliant SDRAMs, the claims do not cover devices built to the JEDEC SDRAM standard.

Response to Finding No. 369: The proposed finding is inaccurate. The limitation a "request" or a "transaction request specifying a semiconductor device" encompasses a read or write request that includes a chip-select signal, as used with a JEDEC-compliant SDRAM. (Nusbaum, Tr. 1558-61, 1577; Jacob, Tr. 5525, 5530-31). The phrase is not limited to a "device identifier feature" that excludes a chip-select line. (CCFF 1172, 1179, 1182). Only this interpretation, and not that now proposed by Rambus, is consistent with the definition of "transaction request" that Rambus adopted in patent litigation involving other patents in the '898 family as encompassing a "transaction request" submitted to a JEDEC-compliant SDRAM. (Nusbaum, Tr. 1558-61, 1577; Jacob, Tr. 5522-23, 5525, 5530-31).

The cited evidence, the testimony of Mr. Fliesler, does not support a finding that the language "a request specifying a semiconductor device" in claims 183 and 184, and the language "transaction request specifying the semiconductor device" in claim 185, requires the use of a type of device identifier feature that is not used in a JEDEC-compliant SDRAM. In his testimony,

Mr. Fliesler relied only on unexplained "similarities" between claims 183-185 to the claims of the '961 application to support his opinion that the claims 183-185 would not cover a JEDEC-compliant SDRAM. He did not refer to the claim language cited in the proposed finding, explain how that language required a device identifier feature, or how it excluded the chip select line that an SDRAM system uses to identify an individual semiconductor device. (Fliesler, Tr. 8855, 8893-94). No record evidence supports the proposed finding.

The testimony by Mr. Fliesler regarding the proper interpretation and analysis of claims 183-185 also is unreliable for the reasons discussed in CCRF 354.

370. Complaint Counsel did not show that Rambus's JEDEC representative had actual knowledge of claims 183, 184 or 185 of the '490 application while Rambus was a JEDEC member.

Response to Finding No. 370: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

In fact, the record could not be clearer that Richard Crisp had broad ongoing actual knowledge of the developing scope of the Rambus patent claims based on his meetings and conversations with patent attorney Lester Vincent, his work helping to draft some of the relevant patent claims, and through his close involvement with other Rambus executives, throughout the period he served as Rambus representative to JEDEC. (*See* CCFF 867-1114, CCRF 288). Furthermore, in addition to Mr. Crisp's knowledge, if others within Rambus knew that Rambus patents or patent applications might be involved in JEDEC work, they had an obligation to inform Mr. Crisp or another Rambus representative at JEDEC, so that they could inform JEDEC. (CCFF 334). A number of other Rambus officers and employees had knowledge both of events

at JEDEC (in part through Mr. Crisp's trip reports) and the scope of pending Rambus patent claims. (*See* CCFF 867-1114, CCRF 288).

The record contains substantial evidence that Mr. Crisp was well aware of Rambus claims to programmable CAS latency technology. (CCFF 900-01 (May 1992 Crisp proposal to add claims covering use of mode register to control latency and asking about "blocks"); 910 (late May 1992 telephone conversation between Crisp and Vincent); 920 (June 1992 telephone conversation between Crisp and Vincent); 928 (August 1992 telephone conversation between Crisp and Vincent); 932-36 (September 1992 meeting between Crisp and Vincent regarding programmable CAS latency, multiple open rows (banks), on-chip PLLs and source synchronous clocking); 947-49 (February 1993 Crisp e-mail identifying programmable access latency, multiple open rows (banks) and on-chip PLL/DLL circuit as claims in process); 955, 958 (May 1993 conference among Crisp, Farmwald and Vincent regarding preliminary amendments, including the '651 regarding programmable access time); 962-66 (June 1993 e-mail exchange with Fred Ware confirming among other things that claims covering programmable CAS latency, directed at SDRAMs, had been filed); 1010-15 (September 1994 Crisp and Roberts e-mails recognizing that Rambus might have to fight patent infringement litigation with JEDEC members regarding use of on-chip PLL, programmable access latencies and other technologies); 1018-23 (October 1994 e-mails on same subject); 1045 (May 1995 Crisp e-mail noting that Rambus pending patent claims involving low swing signaling and programmable access latency might apply to the SyncLink proposal at JEDEC); 1050-55 (Crisp review of patents and applications and work with Vincent regarding claims to cover SyncLink in June-September 1995)).

Complaint Counsel is unable to establish whether Mr. Crisp received copies of the amendments to the '490 application at the time they were filed in part because Lester Vincent, acting at the instructions of Rambus, destroyed copies of his correspondence with Rambus from

the left-hand side of many of his files. CCFF 1746-48. In any event, Mr. Crisp had full access to all of Rambus's patents and patent applications, and reviewed a number of them in June 1995, at almost precisely that the relevant amendment to the '490 application was being filed. (CCFF 1050).

Furthermore, in addition to Mr. Crisp's knowledge, others within Rambus knew that Rambus patents or patent applications might be involved in JEDEC work, including Rambus claims to programmable CAS latency technology. (CCFF 900-01 (Vice President Roberts meeting with Vincent regarding use of mode register to control latency); 911-18 (June 1992 draft business plan, sent by Tate to the Board of Directors: "we believe that Sync DRAMs infringe on some claims in our filed patents; and that there are additional claims we can file for our patents that cover features of Sync DRAMs."); 938 (presentation to Board of Directors regarding the status of SDRAM activity at JEDEC and the Rambus patent strategy); 947-49 (Vice President Roberts copied on February 1993 Crisp e-mail identifying programmable access latency, multiple open rows (banks) and on-chip PLL/DLL circuit as claims in process); 955, 958 (Director Farmwald involved in May 1993 conference with Vincent regarding preliminary amendments, including the '651 regarding programmable access time); 962-66 (Director Farmwald and Vice President Roberts copied on June 1993 e-mails confirming that claims covering programmable CAS latency, directed at SDRAMs, had been filed); 981 (conference among CEO Tate, Vice President Roberts, CFO Harmon and Mr. Vincent regarding enforcement of Rambus patents against Synchronous DRAMs, with specific reference to low voltage swing, programmable CAS latency and on-chip PLLs); 987-92 (Vice President Roberts' letter to Vincent proposing to add claims covering use of registers to control CAS latency, use of multiple banks and clocking data on both edges of the clock); 1010-15 (all executives copied on September 1994 Crisp and Roberts e-mails recognizing that Rambus might have to fight patent infringement litigation with

JEDEC members regarding use of on-chip PLL, programmable access latencies and other technologies); 1018-23 (all executives copied on October 1994 e-mails on same subject); 1045 (all executives copied on May 1995 Crisp e-mail noting that Rambus pending patent claims involving low swing signaling and programmable access latency might apply to the SyncLink proposal at JEDEC); 1050-55 (Crisp review of patents and applications and work with Vincent regarding claims to cover SyncLink in June-September 1995); 1058 (meetings between CEO Tate and in-house counsel Diepenbrock regarding claims to cover current and future SDRAMs); 1073 (when they saw the JEDEC survey ballot, Vice President Mooring and others thought Rambus had invented certain key features)).

In short, there is no credible basis to suggest that Mr. Crisp and those working with him at Rambus and knowledgeable about the company's participation in JEDEC were not well aware of the claims by Rambus to ownership of the programmable CAS latency features embodied in the SDRAM standard.

c. The '692 Application Does Not Cover the September 1994 NEC Presentation.

371. Claims 151 and 152 of the '692 application were filed in a preliminary amendment on June 28, 1993. (CX 1502 at 205, 208; Fliesler, Tr. 8864-65). In an amendment filed on October 23, 1995, claims 151 and 152 were amended and claims 166 and 167 were added. (CX 1502 at 233-35; Fliesler, Tr. 8864-65).

Response to Finding No. 371: Complaint Counsel does not disagree with the proposed finding. The complete "life-cycle" of claim 151 is described in CCFF 1642-45. A slightly modified version of claim 151 issued as claim 1 of Rambus patent no. 5,657,481 (the '481) patent on August 12, 1997. (CX1503 at 1).

372. The claims raised by Complaint Counsel, namely claims 151 and 152 of the '692 application (whether before or after the October 23, 1995 amendment) and claims 166 and 167, would not cover devices built according to the September 1994 NEC presentation "because the claims contain limitations that would not be found in such devices." (JX 21 at 91; Fliesler, Tr. at 8866-67).

Response to Finding No. 372: The proposed finding is inaccurate. Claims 151, 152, 166 and 167 of the '692 application contains claims that read on, or that an engineer could reasonably construe as reading on, an SDRAM built according to the September 1994 NEC presentation. CCFF 1183-98; CCRF 373-74.

373. All of the claims raised by Complaint Counsel call for the generation of a local clock signal for "performing" or "controlling" memory operations with respect to the memory array. (CX 1502 at 208, 233-35). In the 1994 NEC presentation, however, the internal clock signal (designated as "ICLK") controls the timing of an output buffer but does not perform or control operations with respect to the memory array. (JX 21 at 91; Nusbaum, Tr. 1632-34; Fliesler, Tr. 8870-75). In fact, the ICLK signal generated by the PLL in the NEC presentation cannot affect the timing of *anything* within the memory array. (Fliesler, Tr. 8959).

Response to Finding No. 373: The proposed finding is inaccurate. In the circuit block diagram shown in the 1994 NEC presentation, the output buffer (shown by a triangle) outputs data that is stored in the memory array. (JX0021 at 91; Jacob, Tr. 5538; Fliesler, Tr. 8946). The internal clock signal, ICLK, is coupled to the memory array through the output buffer. (*Id.*). By using the local clock signal to control outputting data that is stored in the memory array, the NEC proposal satisfies the limitation of claim 151 of a memory device having "a local clock signal for performing memory operations with respect to the memory array." CCFF 1190.

The testimony of Mr. Fliesler also is unreliable for the reasons discussed in CCRF 354.

374. All of the claims raised by Complaint Counsel call for a "phase locked loop" that is coupled to the memory array. (CX 1502 at 208, 233-35). In the 1994 NEC presentation, however, the box designated as the "PLL" is coupled to the output buffer, not the memory array. (JX 21 at 91; Fliesler, Tr. 8870-75).

Response to Finding No. 374: The proposed finding is inaccurate. The internal clock signal, ICLK, is coupled to the memory array through the output buffer. (JX0021 at 91; Jacob, Tr. 5538). The testimony of Mr. Fliesler also is unreliable for the reasons discussed in CCRF 354.

375. As the terms are generally understood by persons of ordinary skill in the art, a DLL uses variable delay circuitry and a feedback loop to delay one signal so that it is in sync with another signal, while a PLL uses a voltage-controlled oscillator instead of variable delay circuitry. (Nusbaum, Tr. 1637; Jacob, Tr. 5443, 5617; Soderman, Tr. 9401, 9411).

Response to Finding No. 375: The proposed finding is misleading because it suggests that a DLL, but not a PLL, provides a variable delay signal to delay one signal so that it is in sync with another signal. This is inaccurate. Both a DLL and a PLL perform the same function - that of providing a variable delay to one signal so that it will be in sync with another. (Jacob, Tr. 5617 (Q: But both [a PLL and DLL] can be used for that same purpose, to get one clock signal in sync with another, right? A: Both can be used to produce two clock signals that are in sync with each other.")). The cited evidence states only that a DLL and PLL use different mechanisms to perform this same function. A DLL uses variable delay circuitry and a PLL uses a voltage-controlled oscillator. (See, Jacob, Tr. 5617).

376. Although the claims of the '692 application refer to a "phase locked loop" or "PLL," the claims describe this circuit as providing "a variable delay to the local signal." As a result, the circuit is actually a delay locked loop or DLL. (Jacob, Tr. 5633-34).

Response to Finding No. 376: The cited evidence does not support the proposed finding. Professor Jacob offered no testimony suggesting that the claims of the '692 application, which explicitly include the phrase "a phase locked loop (PLL)" would be understood by a person of ordinary skill in the art as not encompassing a phased lock loop. (Jacob, Tr. 5633-34). To the contrary, Professor Jacob testified that claims of the '692 application cover the 1994 NEC proposal for incorporating a PLL onto an SDRAM. CCFF 1183-93.

The proposed finding is an inaccurate statement regarding the content of the claims. Claim 151 recites "a phase locked loop (PLL) . . . for providing a variable delay . . . ." CX1502 at 208). Claim 151 recites a PLL that performs the function of all PLLs - providing a variable delay

to one signal to make it in synch with another. (Jacob, Tr. 5617). Claim 151 does not require a "variable delay circuit" as the proposed finding states, only the variable delay function.

Moreover, at the time the '481 patent issued, in internal documents, Rambus described the '481 patent, which contains a slightly modified version of claim 151 that also recites a PLL (CCFF 1642-45), as covering a memory device that includes phase lock loop circuitry. (CX0948 ("The 5 independent claims cover the following: (a) A memory device that . . . includes phase locked loop circuitry which varies the delay of the local clock signal to create an internal, synchronized clock to operate the interface circuitry on the memory device."); *see also* CX1244 at 1 ("pll-on-a-memory-device patents/'481")).

377. There was no evidence at trial that the 1994 NEC presentation was ever balloted at JEDEC.

Response to Finding No. 377: Complaint Counsel does not disagree. However, the proposed finding does not support a conclusion that Rambus had no intellectual property interests that it was required to disclose to JEDEC. The disclosure obligation arose in connection with any JEDEC work, not only formal balloting of proposals or presentations for approval (CCFF 340). The disclosure obligation arises in connection with discussions at JEDEC (CCFF 341) and is intended to result in disclosure as early as practicable in the JEDEC process (CCFF 342).

378. Complaint Counsel did not show that Rambus's JEDEC representative had actual knowledge of claims 151, 152, 166 or 167 of the '692 application while Rambus was a JEDEC member.

Response to Finding No. 378: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

This proposed finding is flatly wrong. Mr. Crisp received copies of the amendments to the '692 application at the time they were filed in mid-1993. (CCFF 955, 958, 966-67).

Moreover, the record could not be clearer that Richard Crisp had broad ongoing actual knowledge of the developing scope of the Rambus patent claims based on his meetings and conversations with patent attorney Lester Vincent, his work helping to draft some of the relevant patent claims, and through his close involvement with other Rambus executives, throughout the period he served as Rambus representative to JEDEC. (*See* CCFF 867-1114, CCRF 288). Furthermore, in addition to Mr. Crisp's knowledge, if others within Rambus knew that Rambus patents or patent applications might be involved in JEDEC work, they had an obligation to inform Mr. Crisp or another Rambus representative at JEDEC, so that they could inform JEDEC. (CCFF 334). A number of other Rambus officers and employees had knowledge both of events at JEDEC (in part through Mr. Crisp's trip reports) and the scope of pending Rambus patent claims. (*See* CCFF 867-1114, CCRF 288).

The record contains substantial evidence that Mr. Crisp was well aware of Rambus claims to the use of PLL circuits on SDRAMS. (CCFF 932-36 (September 1992 meeting between Crisp and Vincent regarding programmable CAS latency, multiple open rows (banks), on-chip PLLs and source synchronous clocking); 947-49 (February 1993 Crisp e-mail identifying programmable access latency, multiple open rows (banks) and on-chip PLL/DLL circuit as claims in process); 962-66 (June 1993 e-mail exchange with Fred Ware confirming that claims covering use of on-chip PLLs, directed against future SDRAMs respectively, were being written up); 1010-15 (September 1994 Crisp and Roberts e-mails recognizing that Rambus might have to fight patent infringement litigation with JEDEC members regarding use of on-chip PLL, programmable access latencies and other technologies); 1018-23 (October 1994 e-mails on same subject); 1050-55

(Crisp review of patents and applications and work with Vincent regarding claims to cover SyncLink in June-September 1995)).

Furthermore, in addition to Mr. Crisp's knowledge, others within Rambus knew that Rambus patents or patent applications might be involved in JEDEC work, including Rambus claims to on-chip PLL technology. (CCFF 911-18 (June 1992 draft business plan, sent by Tate to the Board of Directors: "we believe that Sync DRAMs infringe on some claims in our filed patents; and that there are additional claims we can file for our patents that cover features of Sync DRAMs."); 938 (presentation to Board of Directors regarding the status of SDRAM activity at JEDEC and the Rambus patent strategy); 947-49 (Vice President Roberts copied on February 1993 Crisp e-mail identifying programmable access latency, multiple open rows (banks) and on-chip PLL/DLL circuit as claims in process); 962-66 (Director Farmwald and Vice President Roberts copied on June 1993 e-mails confirming that claims covering use of on-chip PLLs, directed against future SDRAMs, were being written up); 981 (conference among CEO Tate, Vice President Roberts, CFO Harmon and Mr. Vincent regarding enforcement of Rambus patents against Synchronous DRAMs, with specific reference to low voltage swing, programmable CAS latency and on-chip PLLs); 1010-15 (all executives copied on September 1994 Crisp and Roberts e-mails recognizing that Rambus might have to fight patent infringement litigation with JEDEC members regarding use of on-chip PLL and other technologies); 1018-23 (all executives copied on October 1994 e-mails on same subject); 1050-55 (Crisp review of patents and applications and work with Vincent regarding claims to cover SyncLink in June-September 1995); 1058 (meetings between CEO Tate and in-house counsel Diepenbrock regarding claims to cover current and future SDRAMs); 1069 (Diepenbrock presentation regarding "offensive" patent strategy, including DLLs and dual edge clocking); 1073 (when they saw the JEDEC survey ballot, Vice

President Mooring and others thought Rambus had invented certain key features); 1074-75 (Diepenbrock meeting with Vincent regarding DLLs)).

In short, there is no credible basis to suggest that Mr. Crisp and those working with him at Rambus and knowledgeable about the company's participation in JEDEC were not well aware of the claims by Rambus to ownership of on-chip PLL technology.

d. <u>The '646 Application Does Not Cover the Presentations Raised By Complaint Counsel or the DDR SDRAM Standard</u>.

379. Claim 151 of the '646 application was filed on September 6, 1994. (CX 1493 at 183-85; Fliesler, Tr. 8856). In an office action dated January 24, 1995, the patent examiner rejected claim 151 for, among other reasons, being indefinite. (CX 1493 at 212, 215). Claim 151 was canceled in an amendment filed on September 14, 1995. (CX 1493 at 243; Fliesler, Tr. 8856-57). The '327 patent, which issued from the '646 application, did not contain claim 151. (CX 1494; Nusbaum, Tr. 1617).

<u>Response to Finding No. 379</u>: The proposed finding is accurate in that it confirms that the listed claim of the '646 application was pending during the time that Rambus was a member of JEDEC. This claim covered a JEDEC-compliant SDRAM incorporating a proposed dual-edged clocking feature. (Nusbaum, Tr. 1595-1603; Jacob, Tr. 5549-50, CCFF1199-1211).

The proposed finding is incomplete and misleading, however, in its allegations concerning the disposition of the referenced claim. In fact, claim 1 of the issued Rambus '327 patent contains the language of claim 151, along with additional limitations. (CX1494 at 23). Rambus in fact has asserted patents against JEDEC-member companies using dual-edge clock technology in JEDEC-compliant SDRAMs, SGRAMs, DDR SDRAMs and DDR SGRAMs, as well as memory controllers that interface with them. (CCFF 1960, 1962, 1967-68). Every patent that Rambus has asserted against SDRAM and DDR SDRAM products in patent litigation resulted, like the '646 application, from continuation or divisional patent applications flowing from the original '898 application. The asserted patents, like the '646 application, claim the

benefit of the '898 application's April 18, 1990 filing date. (First Stipulation, no. 22; Exhibit A to First Stipulation, no. 22; Nusbaum Tr. 1506-1508; *see also* DX0014).

380. Claim 151 was filed over two years after the Hardell presentation, and before the Samsung presentation or the issuance of the Survey Ballot. (CX 1493 at 183-85; Fleisler, Tr. 8856; CX 34 at 32; JX 28 at 34-35; JX 31 at 71). Thus, claim 151 was not pending at the time of any of the presentations that allegedly triggered its disclosure.

Response to Finding No. 380: The proposed finding is incomplete and misleading insofar as it suggests that Rambus was under no duty to disclose its '646 application because claim 151 was not formally pending at the time of the Hardell presentation, the Survey Ballot or the Samsung presentation. In fact, dual-edge clock technology was a continuing subject of discussion at JEDEC, in connection with the SDRAM standard and the future SDRAM discussions, throughout the period that Rambus was a member of JEDEC. (CCFF 623-641). The JEDEC disclosure duty is not tied to any procedural formality in the JEDEC process (CCFF 340) and is a duty for a JEDEC member when relevant patents or patent applications come to the member's attention. (CCFF 333-34). The duty extends to any patent or application that might be involved in JEDEC work. (CCFF 335-338). The ongoing discussions of dual-edge clock technology should have prompted disclosure by Rambus, had it been acting in good faith.

Moreover, the formal cancellation of claim 151 in September 1995 did not remove the relevant language from consideration by the PTO; as noted above (CCRF 380), claim 1 of the issued Rambus '327 patent contains the language of claim 151, along with additional limitations. The Rambus claim to dual-edge clock technology therefore was substantively pending in its application before the PTO at the time of the Survey Ballot in October 1995 and the Samsung presentation in March 1996. In fact, both these events occurred after a Notice of Allowance of claims had been issued in June 1995 by the U. S. Patent Office for the Rambus '646 application embodying its claim to dual-edge clock technology. (CCFF 1076). In short, there can be no

credible claim that the Rambus claim to dual-edge clocking technology was not part of a pending Rambus patent application or issued patent of Rambus at the time that the technology was the subject of ongoing discussion at JEDEC. (*See* CCRF 329).

381. The presentations raised by Complaint Counsel contain no implementation details, thus, they do not contain the implementation details that are *required* by claim 151 of the '646 application. (CX 1493 at 184-85).

Response to Finding No. 381: The proposed finding is inaccurate and not supported by the cited evidence. The proposed finding lists no implementation details that are allegedly required by claim 151 but lacking in the dual-edged clocking proposals. Complaint Counsel presented detailed and specific evidence explaining that each limitation of claim 151 was present in an SDRAM that implemented dual-edged clocking proposals made to JEDEC while Rambus was a member. (CCFF 1199-1215).

Moreover, the proposed finding is misleading insofar as it suggests that the JEDEC disclosure requirement applies only where there is a determination that any and all products built to conform to the standard, in all possible implementations, will infringe the patent or patent application. Rather, the duty to disclose is triggered by the good faith knowledge or belief of a participant that the patent or patent application might involve the work of the committee. *See* CCFF 310-14, 331-33, 335. There can be no credible assertion that the Rambus claim to dual-edge clocking technology as set forth in claim 151 was not a claim that might in good faith involve the work of JEDEC.

382. Claim 151 of the '646 application would not read on a device built to the JEDEC DDR SDRAM standard. (Fliesler, Tr. 8857). Claim 151 calls for writing data to the DRAM in response to the rising edge of a clock signal and the falling edge of a clock signal, while the JEDEC DDR SDRAM standard discusses using a different signal called the DQS or data strobe signal to write the data to the DRAM. (CX 1493 at 184-85; CX 234 at 164; JX 57 at 5; Fliesler, Tr. at 8857-58).

Response to Finding No. 382: The proposed finding is inaccurate because the term "clock signal," as it is used in Claim 151 can reasonably be interpreted as a periodic signal, which would include the DQS signal used in DDR SDRAM. (Jacob, Tr. 5553-54).

Mr. Fliesler's testimony to the contrary is unreliable. Patent claims must be interpreted as they would be understood by a person ordinary skill in the art. (Fliesler, Tr. 8933). Unlike Professor Jacob, Mr. Fliesler is an attorney, and not a person skilled in the art of DRAM design and architecture. (Fliesler, Tr. 8867-69, 8781). Even in his work as a patent attorney, Mr. Flielser has had minimal exposure to technical DRAM issues. (Fliesler, Tr. 8782). Moreover, Mr. Fliesler did not discuss his claim interpretation, including his understanding of the term "clock" in claim 1, and his analysis of the DDR SDRAM standard with any person skilled in the pertinent art. Rather, he relied on his own analysis. (Fliesler, Tr. 8783, 8934, 8948).

383. Complaint Counsel did not show that Rambus's JEDEC representative had actual knowledge of claim 151 of the '646 application while Rambus was a JEDEC member.

Response to Finding No. 383: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding also is wrong. In fact, the record could not be clearer that Richard Crisp had broad ongoing actual knowledge of the developing scope of the Rambus patent claims. There is substantial evidence that Mr. Crisp, and others in the group at high levels in Rambus who were closely involved with the participation of Rambus in JEDEC, were well aware of the Rambus claim to patent rights to the dual-edge clock technology embodied in what was to become, and in fact became, the 'Rambus '327 patent. (CCRF 331).

e. Summary of Findings Regarding Undisclosed Patent Applications.

384. Complaint Counsel have not met their burden of proving that Rambus had any undisclosed patent applications while it was a JEDEC member that were required to be disclosed under EIA/JEDEC policies.

Response to Finding No. 384: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding also is wrong. (CCFF 1122-1237, CCRF 361-83).

385. Complaint Counsel have not met their burden of proving that Rambus's JEDEC representative, Richard Crisp, had actual knowledge of claims 151, 159, 160, 164, 165 and/or 168 of the '961 application during the time that Rambus was a JEDEC member.

Response to Finding No. 385: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding also is wrong. (CCRF 365).

386. Complaint Counsel have not met their burden of proving that claims 151, 159, 160, 164, 165 and/or 168 of the '961 application were "essential to" or "read on" any technology described in any presentation made while Rambus was a JEDEC member.

Response to Finding No. 386: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding also is wrong. Complaint Counsel has demonstrated that the cited claims read on, or that an engineer could reasonably interpret them to read on Release 4 of the JEDEC SDRAM standard. (CCFF 1125-63; CCRF 363-64). The proposed finding is also misleading insofar as it purports to describe the JEDEC disclosure duty as pertaining only to

applications that are "essential to" or "read on" technologies under discussion at JEDEC. (CCRF 334).

387. Complaint Counsel have not met their burden of proving that claims 151, 159, 160, 164, 165 and/or 168 of the '961 application were "essential to" or "read on" any technology that was balloted while Rambus was a JEDEC member.

Response to Finding No. 387: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding also is wrong. Complaint Counsel has demonstrated that the cited claims read on, or that an engineer could reasonably interpret them to read on Release 4 of the JEDEC SDRAM standard, which was approved in 1993. (CCFF 1125-63; CCRF 363-64). The proposed finding is also misleading insofar as it purports to describe the JEDEC disclosure duty as pertaining only to applications that are "essential to" or "read on" technologies under discussion at JEDEC. (CCRF 334).

388. Complaint Counsel have not met their burden of proving that Rambus's JEDEC representative, Richard Crisp, had actual knowledge of claims 183, 184 and/or 185 of the '490 application during the time that Rambus was a JEDEC member.

Response to Finding No. 388: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding also is wrong. (CCRF 370).

389. Complaint Counsel have not met their burden of proving that claims 183, 184 and/or 185 of the '490 application were "essential to" or "read on" any technology described in any presentation made while Rambus was a JEDEC member.

Response to Finding No. 389: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding also is wrong. Complaint Counsel has demonstrated that the cited claims read on, or that an engineer could reasonably interpret them to read on Release 4 of the JEDEC SDRAM standard, which was approved in 1993. (CCFF 1164-82; CCRF 366-69). The proposed finding is also misleading insofar as it purports to describe the JEDEC disclosure duty as pertaining only to applications that are "essential to" or "read on" technologies under discussion at JEDEC. (CCRF 334).

390. Complaint Counsel have not met their burden of proving that claims 183, 184 and/or 185 of the '490 application were "essential to" or "read on" any technology that was balloted while Rambus was a JEDEC member.

Response to Finding No. 390: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding also is wrong. Complaint Counsel has demonstrated that the cited claims read on, or that an engineer could reasonably interpret them to read on Release 4 of the JEDEC SDRAM standard, which was approved in 1993. (CCFF 1164-82; CCRF 366-69). The proposed finding is also misleading insofar as it purports to describe the JEDEC disclosure duty as pertaining only to applications that are "essential to" or "read on" technologies under discussion at JEDEC. (CCRF 334).

391. Complaint Counsel have not met their burden of proving that Rambus's JEDEC representative, Richard Crisp, had actual knowledge of claims 151, 152, 166 and/or 167 of the '692 application during the time that Rambus was a JEDEC member.

Response to Finding No. 391: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Complaint Counsel have not met their burden of proving that claims 151, 152, 166 and/or 167 of the '692 application were "essential to" or "read on" any technology described in any presentation made while Rambus was a JEDEC member.

392. Complaint Counsel have not met their burden of proving that claims 151, 152, 166 and/or 167 of the '692 application were "essential to" or "read on" any technology described in any presentation made while Rambus was a JEDEC member.

Response to Finding No. 392: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding is inaccurate. Complaint Counsel has demonstrated that the cited claims read on, or that an engineer could reasonably interpret them to read on the 1994 NEC proposal to incorporate PLL onto an SDRAM. (CCFF 1183-98; CCRF 371-76). The proposed finding is also misleading insofar as it purports to describe the JEDEC disclosure duty as pertaining only to applications that are "essential to" or "read on" technologies under discussion at JEDEC. (CCRF 334).

393. Complaint Counsel have not met their burden of proving that claims 151, 152, 166 and/or 167 of the '692 application were "essential to" or "read on" any technology that was balloted while Rambus was a JEDEC member.

Response to Finding No. 393: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel

submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding also is wrong. Complaint Counsel has demonstrated that the cited claims read on, or that an engineer could reasonably interpret them to read on the 1994 NEC proposal to incorporate PLL onto an SDRAM. (CCFF 1183-98; CCRF 371-76). The proposed finding is also misleading insofar as it purports to describe the JEDEC disclosure duty as pertaining only to applications that are "essential to" or "read on" technologies under discussion at JEDEC. (CCRF 334).

394. Complaint Counsel have not met their burden of proving that Rambus's JEDEC representative, Richard Crisp, had actual knowledge of claim 151 of the '646 application during the time that Rambus was a JEDEC member.

Response to Finding No. 394: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding also is wrong. (CCRF 383).

395. Complaint Counsel have not met their burden of proving that claim 151 of the '646 application was "essential to" or "read on" any technology described in any presentation made while Rambus was a JEDEC member.

Response to Finding No. 395: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding also is wrong. Complaint Counsel has demonstrated that claim 151 of the '646 application reads on, or that an engineer could reasonably interpret it to read on dual-edged clocking proposal made to JEDEC while Rambus was a member. (CCFF 1199-1215;

CCRF 379-82). The proposed finding is also misleading insofar as it purports to describe the JEDEC disclosure duty as pertaining only to applications that are "essential to" or "read on" technologies under discussion at JEDEC. (CCRF 334).

396. Complaint Counsel have not met their burden of proving that claim 151 of the '646 application was "essential to" or "read on" any technology that was balloted while Rambus was a JEDEC member.

Response to Finding No. 396: The proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding is also misleading insofar as it purports to describe the JEDEC disclosure duty as pertaining only to applications that are "essential to" or "read on" technologies under discussion at JEDEC. (CCRF 334). The proposed finding is also misleading insofar as it purports to describe the JEDEC disclosure duty as pertaining only to technologies that are balloted for approval by JEDEC. In fact, the disclosure obligation arises in connection with any JEDEC work, not only formal balloting of proposals or presentations for approval (CCFF 340). The disclosure obligation arises in connection with discussions at JEDEC (CCFF 341) and is intended to result in disclosure as early as practicable in the JEDEC process (CCFF 342).

C. Rambus Withdrew From JEDEC Before The Standardization Of The DDR SDRAM Began.

397. An additional reason why Rambus had no disclosure obligation with respect to dual edge clocking and on-chip PLL/DLL is that it withdrew from JEDEC before the standardization process of the DDR SDRAM, which incorporated those features, began.

Response to Finding No. 397: The statement in RPF 397 [An additional reason why Rambus had no disclosure obligation with respect to dual edge clocking and on-chip PLL/DLL is that it withdrew from JEDEC before the standardization process of the DDR

SDRAM, which incorporated those features, began.] lacks any reference to the record. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. It is also inaccurate because Rambus did not withdraw from JEDEC before the standardization process of the DDR SDRAM began. (CCFF 578-644).

398. Rambus attended its last JEDEC meetings as of December 1995. In June 1996, Rambus notified the JEDEC office that it would not pay its dues for 1996 and that it would no longer be a JEDEC member. (CX 2104, Crisp 8/10/01 Micron Depo. Tr. 853:18-854:1; CX 887 at 1).

Response to Finding No. 398: Complaint Counsel does not disagree.

399. The DDR SDRAM standard received JC 42.3 committee approval in March 1998, but was not published until 2000. (CX 375 at 1; JX 57).

Response to Finding No. 399: The statement in RPF 399 [The DDR SDRAM standard received JC 42.3 committee approval in March 1998] is misleading and incomplete and is not supported by the evidence cited. CX0375 in fact states that there were numerous ballots approved by the JC-42.3 committee prior to March 1998 that were DDR SDRAM related. Further, the author of CX0375, Desi Rhoden, testified that the DDR SDRAM standardization process had begun years previously. (Rhoden, Tr. 1200) A number of witnesses testified that work on the DDR SDRAM standard had begun years prior to Rambus leaving JEDEC. (CCFF 578-644) In fact, the DDR SDRAM standard included many features that had been adopted by JC-42.3 as part of the first generation SDRAM standard. (CCFF 653).

The statement in RPF 399 [the DDR SDRAM standard . . . was not published until 2000.] is incomplete. Although the DDR SDRAM standard was published together as one document in JESD79 in 2000, it had previously been published as part of Release 9 of the 21-C standard in August of 1999. (CCFF 649-652).

400. The DDR SDRAM standard received JEDEC Board of Director approval in 1999. (Rhoden, Tr. 743).

Response to Finding No. 400: The proposed finding is incomplete because it fails to acknowledge that the DDR SDRAM standardization process had begun years previously. (Rhoden, Tr. 1200; CCFF 5785) In 1997 alone, JEDEC had handled about 200 DDR SDRAM related ballots. (CX0375 at 1) Further, A number of witnesses testified that work on the DDR SDRAM standard had begun years prior to Rambus leaving JEDEC. (CCFF 578-644) In fact, the DDR SDRAM standard included many features that had been adopted by JC-42.3 as part of the first generation SDRAM standard. (CCFF 653).

401. The first time that a balloted item was approved as part of the JEDEC DDR SDRAM standard was June 1997. (CX 375 at 2).

Response to Finding No. 401: The statement in RPF [The first time that a balloted item was approved as part of the JEDEC DDR SDRAM standard was June 1997.] is incomplete. CX0375 in fact states that there were numerous ballots approved by the JC-42.3 committee prior to March 1998 that were DDR SDRAM related. Further, the author of CX0375, Desi Rhoden, testified that the DDR SDRAM standardization process had begun years previously. (Rhoden, Tr. 1200) A number of witnesses testified that work on the DDR SDRAM standard had begun years prior to Rambus leaving JEDEC. (CCFF 578-644) In fact, the DDR SDRAM standard included many features that had been adopted by JC-42.3 as part of the first generation SDRAM standard. (CCFF 653).

402. As described below, an e-mail authored by JEDEC Board Chairman Desi Rhoden in March 1998 shows that the first *presentation* leading to the DDR SDRAM standard occurred in December 1996, after Rambus had left JEDEC. (CX 375 at 1-2).

Response to Finding No. 402: The statement in RPF 402 [As described below, an e-mail authored by JEDEC Board Chairman Desi Rhoden in March 1998 shows that the first

presentation leading to the DDR SDRAM standard occurred in December 1996, after Rambus had left JEDEC.] is incomplete and misleading. Desi Rhoden testified that although the name DDR was created and invented in December of 1996, prior to that time, JC-42.3 had been talking about individual features that became included in the DDR SDRAM standard. Those features were collected in the Fujitsu presentation in December of 1996. He further stated and other members agreed that the DDR standardization process had actually begun many years previous to the Fujitsu presentation. (Rhoden, Tr. 2000; CCRR 578-585

403. On March 9, 1998, Mr. Rhoden sent an e-mail to Ken McGhee, the JEDEC Secretary, for forwarding to all JC 42 members. (Rhoden, Tr. 1192-93; CX 375). The e-mail was an effort by Rhoden to recap what had transpired in the DDR SDRAM standardization process. (Rhoden, Tr. 1195).

Response to Finding No. 403: The statement in RPF 403 [The e-mail was an effort by Rhoden to recap what had transpired in the DDR SDRAM standardization process.] is misleading. Mr. Rhoden actually testified that the e-mail reasonably recaps what had transpired with DDR and not what had transpired in the DDR SDRAM standardization process. (Rhoden, Tr. 1195)

404. Mr. Rhoden's March 9, 1998 e-mail states in part:

> "[W]e could have finished the DDR standard sooner if only we had started earlier. Let us recap what has transpired with DDR:
>
> 1. A lot of private and independent work *outside of JEDEC* for most of 1996 (here is where we missed a good opportunity to start early).
> 2. December 96 – A single overview presentation of a DDR proposal at a JC 42 meeting.
> 3. March 97 – Many (5 as I remember) presentations of very different proposals at JEDEC (no where near the consensus that was supposedly built outside of the committee). None of these were compatible with each other. At this meeting the decision was made to finally get serious and set up a special meeting for April 97.
> 4. April 97 – Real, focused, dedicated work begins at a special meeting. Many very good ideas and a lot of truly animated discussion.

5. June 97 – First ballots on DDR pass committee.
6. July 1997 – A second special meeting where the last of the basic concepts were articulated and send out for ballot.
7. Sept 97 – The diamond in the rough took its basic shape (there were 2 very similar, but still different forms.)"

(CX 375 at 1-2).

Response to Finding No. 404: Complaint Counsel does not disagree.

405. Mr. Rhoden's March 1998 e-mail thus dates the first presentation to JEDEC of a DDR SDRAM proposal to December 1996. (CX 375 at 1).

Response to Finding No. 405: This proposed finding is incomplete. Desi Rhoden testified that although the name DDR was created and invented in December of 1996, prior to that time, JC-42.3 had been talking about individual features that became included in the DDR SDRAM standard. Those features were collected in the Fujitsu presentation in December of 1996. He further stated and other members agreed that the DDR standardization process had actually begun many years previous to the Fujitsu presentation. (Rhoden, Tr. 2000; CCRR 578-585)

406. Mr. Rhoden's email states that the DDR device was being developed "outside of JEDEC" in 1996. (CX 375 at 1).

Response to Finding No. 406: The statement in RPF 406 is incomplete and misleading. CX0375 at 1 states with regard to DDR that there was "a lot of private and independent work outside of JEDEC for most of 1996". Desi Rhoden testified that such work was based on JEDEC work (Rhoden, Tr. 1196 ("Q. What did you mean by "work outside of JEDEC" in 1996? What's that mean? A. The feature set that we had been discussing in many meetings throughout JEDEC in -- during 1996, various people had worked -- had taken that feature set in pulling it together. Rather than trying to pull the feature set that was under discussion under JEDEC during '96, they waited until later to bring these features that had been under discussion in the industry and within JEDEC for -- for, I don't know, for the better part of the last decade and

put it together and create a codified proposal that would encompass the framework, if you will, of the next generation.")

407. In an April 1997 presentation, Mr. Rhoden stated: "DDR & SLDRAM were Introduced In JEDEC in Dec 1996." (RX 911 at 3).

Response to Finding No. 407: The statement in RPF 407 [In an April 1997 presentation, Mr. Rhoden stated: "DDR & SLDRAM were Introduced In JEDEC in Dec 1996."] is incomplete and misleading. Desi Rhoden testified that by this statement he meant that the name DDR was created in December 1996 when a number of features that that prior to that time had been previously discussed at JEDEC were gathered by Fujitsu. (Rhoden, Tr. 1200) Mr. Rhoden and other JEDEC members testified that the DDR standardization process had actually begun many years previous to the Fujitsu presentation. (Rhoden, Tr. 2000; CCRR 578-585)

408. The initial DDR SDRAM presentation that Mr. Rhoden referred to in his March 1998 e-mail and his April 1997 presentation was made by Fujitsu in December 1996. (Rhoden, Tr. 1198; RX 911 at 3; CX 375 at 1). This presentation, identified in the minutes of the JC 42.3 subcommittee as "Fujitsu Double Data Rate SDRAM," was designated as a "first showing." (JX 35 at 6, 34-42).

Response to Finding No. 408: The reference in RPF 408 to the Fujitsu presentation as the initial DDR SDRAM presentation is incomplete and misleading. In fact, the large weight of the evidence shows that there were numerous presentations relating to the DDR SDRAM standard prior to the Fujitsu presentation in December 1996. (CCFF 578-658)

409. Mr. Rhoden's March 1998 e-mail also states that the decision to "finally get serious" about DDR SDRAM was not made until March 1997. (Rhoden, Tr. 1201). "Real, focused, dedicated work" on the DDR SDRAM standard did not take place until April 1997. (Rhoden, Tr. 1202). The DDR SDRAM standard did not take "its basic shape" until September 1997. (Rhoden, Tr. 1202).

Response to Finding No. 409: The statements in RPF 409 are misleading and incomplete. Desi Rhoden testified that by this statement he meant that the name DDR was created in December 1996 when a number of features that that prior to that time had been

previously discussed at JEDEC were gathered by Fujitsu. (Rhoden, Tr. 1200) Mr. Rhoden and other JEDEC members testified that the DDR standardization process had actually begun many years previous to the Fujitsu presentation. (Rhoden, Tr. 2000; CCRR 578-585)

410. Desi Rhoden was in a position to know about the dates described in his March 1998 e-mail. He has played a leadership role at JEDEC for quite some time. (Rhoden, Tr. 1191). He is currently chairman of the JC 42 committee, which contains the JC 42.3 subcommittee. (Rhoden, Tr. 1191). He has also been chairman of the 42.3 subcommittee and is currently chairman of the JEDEC Board of Directors. (Rhoden, Tr. 1190). In 1998, Mr. Rhoden was very actively involved in the DDR SDRAM standardization process within the JEDEC 42 committee. (Rhoden, Tr. 1191-92).

Response to Finding No. 410: Complaint Counsel does not disagree.

411. There is other contemporaneous evidence that work on the DDR SDRAM device did not begin, even outside of JEDEC, until the summer of 1996. An IBM presentation on DDR SDRAM dated March 17, 1997 notes that "Industry has been working on DDR definition for 6-9 months," that is, beginning at some point between approximately mid-June and mid-September 1996. (RX 892 at 1). Initially, this work consisted of "small supplier consortiums and individual supplier/user meetings." (*Id.*). Like Mr. Rhoden, the IBM document dates the first "Official DDR presentations" at JEDEC to December 1996, referring (again) to the first showing by Fujitsu. (*Id.*).

Response to Finding No. 411: The statements in RPF 411 are unreliable. Rambus did not use the document with any witnesses at trial. The statements in the document are not self-evident. Rambus had the opportunity to present the document to IBM witnesses Gordon Kelley and Mark Kellogg, both of who testified at trial. Mr. Kelley who was IBM's primary representative in the JC-42.3 committee testified that work on the standardization of the DDR SDRAM standard had begun a many years prior to 1996 with IBM's toggle mode presentations. (CCFF 578, 579)

412. A March 10, 1997 Mitsubishi memorandum regarding "DDR SDRAM Specification Planning History and Recent Trends" confirms that DDR efforts began outside of JEDEC in the summer of 1996, with "eight companies . . . meeting once every 2 weeks to quickly plan DDR specifications." (RX 885A at 1). The Mitsubishi memorandum's first mention of JEDEC work relating to DDR SDRAM is the first showing by Fujitsu in December 1996. (*Id.*)

Response to Finding No. 412: The statements in RPF 412 are unreliable. Rambus did not use the document with any witnesses at trial. The statements in the document are not self-evident. Rambus had the opportunity to present the document to Sam Chen, a Mitsubishi employee who was deposed on. Rambus did not show the document to Mr. Chen.

A July 1997 official JEDEC ballot form regarding a proposed DDR SDRAM pinout states: "DDR SDRAMs has been under discussion within JEDEC since September 1996." (RX 967 at 1).

Response to Finding No. 412: The statement in RFP 413 cites to a document that is not in evidence and therefore should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

413. As noted above, Rambus attended its last JC 42.3 meeting in December 1995, and it sent a letter confirming its withdrawal from JEDEC in June 1996. (CX 2104, Crisp 8/10/01 Micron Depo. Tr. 853:18-854:1; CX 887 at 1).

Response to Finding No. 413: Complaint Counsel does not disagree.

414. As Gordon Kelley, Chairman of the JC 42.3 subcommittee, explained, after a company left JEDEC, it had no duty to disclose anything to JEDEC. (Kelley, Tr. 2700).

Response to Finding No. 414: Complaint Counsel has no specific response.

415. The district court in the *Infineon* case granted judgment in Rambus's favor on the question of whether it had committed fraud with respect to the DDR SDRAM standard. The district judge held that "substantial evidence did not support the jury's verdict *because Rambus withdrew from JEDEC before formal consideration of the DDR SDRAM standard*." *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1105 (Fed. Cir. 2003) (emphasis added). The Federal Circuit agreed (and the panel was unanimous on this point), finding that:

> "[T]he disclosure duty, as defined by the EIA/JEDEC policy, did not arise before legitimate proposals were directed to and formal consideration began on the DDR-SDRAM standard. None of the evidence relied on by Infineon (e.g., survey ballot, technology proposals on the SDRAM standard) provides substantial evidence for the implicit jury finding that Rambus had patents or applications 'related to' the DDR-SDRAM standard that should have been disclosed before the standard came under formal consideration."

(*Id.*).

Response to Finding No. 415: RPF 416 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

D. Rambus Had No Reasoned And Considered Belief Before Late 1998 That It Had Pending Claims That Could Potentially Be Asserted Against JEDEC-Compliant SDRAM Or DDR SDRAM Products.

416. Complaint Counsel have asserted that a JEDEC member was obligated to disclose its *beliefs* that it had sought or could seek intellectual property protection over features or technologies under discussion at JEDEC meetings. (Opening Statement, Tr. 17).

Response to Finding No. 416: This Proposed finding is potentially misleading as it takes the statement out of context, the full text which reads: "When a JEDEC member company understands or believes that its patents bear upon specific aspects of JEDEC's standardization work, that knowledge on the part of the company triggers a duty to disclose." (Opening Statement, p. 17). This view is consistent with record evidence developed at trial as to knowledge or belief on the part of a JEDEC participant that would trigger a disclosure obligation. (*See* CCFF 333 - 334)

417. There is substantial evidence that it was a JEDEC representative's "actual *knowledge*," not his *beliefs*, that triggered whether disclosure obligations might exist. (Rhoden, Tr. 624; Kelly, Tr. 1970, 2171-2; RX 669 at 3). The Federal Circuit agreed, stating:

> The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard. Otherwise the standard would exempt a member from disclosure, if it truly, but unreasonably, believes its claims do not cover the standard. As discussed above, the JEDEC test in fact depends on whether claims reasonably might read on the standard. A member's subjective beliefs, hopes, and desires are irrelevant.

(*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003).)

Response to Finding No. 417: The second sentence of the proposed finding and the citation to the Federal Circuit opinion constitutes legal argument and is inappropriate for findings of fact. Complaint Counsel submits that this portion of the finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The balance of the proposed finding takes both Mr. Rhoden's and Mr. Kelly's testimony of out context and mis-cites a document (RX0669). Mr. Rhoden in fact testified that disclosure was "triggered by the actual knowledge of the people that were involved, and that would be not just the representative at the meeting, but all of the people ... involved in the process." (Rhoden, Tr. 624). Mr. Kelly testified that the disclosure obligation "applies across the board to all participants with actual knowledge." (J. Kelly, Tr. 1970). RX0669 (which is also cited) does not provide any specific information about the application of the JEDEC patent disclosure policy.

The proposed finding is misleading in a more fundamental way as well. The record evidence shows that the JEDEC disclosure duty is triggered by the participant's knowledge of a patent or patent application that might be involved in JEDEC work. (CCFF 333-345). The rule is intended to prompt disclosure as early in the process as possible so that the implications of the intellectual property can be effectively considered. (CCFF 340; Sussman, Tr. 1343 ("The earlier that we have the information that something may have some IP on it, the better it turns out to be, so we don't waste time talking of this rather than an alternate.")).

The rule, therefore, necessarily requires an exercise of good-faith belief by JEDEC participants. For example, Mr. Rhoden testified that disclosure is required of "everything in the patent process;" when asked to describe what he meant, Mr. Rhoden responded, "the best way to answer . . . is if you believe you have ownership of it, then you are obligated to disclose it." (Rhoden, Tr. 317-18). Mr. Sussman described the disclosure situation as one with an "individual

standing up and saying I believe my company has IP or I believe your company has IP." (Sussman, Tr. 1376). Mr. Calvin testified that "as you began to realize that the direction the standard was going could be affected by those [patents or patent applications], you would have a similar obligation [to disclose]." (Calvin, Tr. 1012).

Contrary to the assertion contained in the proposed finding, Mr. Kelly, the man responsible for interpretation and application of the disclosure rule, in fact emphasized that "the participant needs to exercise some judgment certainly given the fact that the goal is early disclosure." (J. Kelly, Tr. 1981). As he put it, "overriding this whole process is a duty to act in good faith." (*Id.* at 1982).

418. Assuming, however, that a representative's beliefs did trigger a disclosure obligation, Complaint Counsel nevertheless did not meet their burden of proving that Rambus's JEDEC representative, Richard Crisp, held such a belief at any relevant time.

Response to Finding No. 418: This proposed finding constitutes legal argument and is inappropriate for findings of fact, therefore Complaint Counsel submits that this portion of the finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. The Proposed finding is contrary to the weight of the evidence in that it ignores substantial record evidence demonstrating Mr. Crisp's very substantive involvement in, and knowledge of, Rambus' patent prosecution efforts, in the 1992-1996 time frame when he was active as Rambus' JEDEC representative. (*See* CCFF 809-10, 854, 856-57, 886, 888-92, 900-01, 910, 920, 928, 932-36, 938-39, 947-49, 955-58, 962-67, 997-98, 1010-15, 1018-23, 1030, 1032, 1037, 1045, 1050-55). Mr. Crisp, in fact, was the Rambus official asked to report to the Rambus Board of Directors in 1992 about "the SDRAM status at JEDEC, the Rambus patent strategy and system level difficulties with SDRAM." (CX0606 at 2).

419. Complaint Counsel rely upon a draft of a Rambus business plan, prepared in June of 1992, that states that "we believe that Sync DRAMs infringe on some claims in our filed patents." (CX 543A at 17).

Response to Finding No. 419: The Proposed finding is accurate but incomplete; for more details about this document, *see* CCFF 911 - 918.

420. Mr. Crisp is not among the individuals listed as receiving the draft plan. (CX 543A at 1).

Response to Finding No. 420: This Proposed finding, by focusing solely on Mr. Crisp and his knowledge of the Rambus business plan, is misleading and ignores other evidence. For example, Rambus Vice President (now President) David Mooring, who is one of the individuals who received the June 1992 Business plan (CX0543A at 1), accompanied Mr. Crisp to the next JEDEC meeting in July of 1992 and made no effort to inform the meeting about Rambus intellectual property while the results of ballots that led to the SDRAM standard were discussed at JEDEC. (*See generally* CCFF 921 - 927 for more details on the July 1992 JEDEC meeting attended by Messrs. Crisp and Mooring). Furthermore, the suggestion that Mr. Crisp was somehow unfamiliar with the Rambus business plan is contradicted by other evidence; as noted above, Mr. Crisp reported to the Board about Rambus patent strategy in 1992 (CX0606 at 2) and later documentation from Mr. Crisp indicates he was well aware of the conflicts between the Rambus business model, on the one hand, and the JEDEC "open standards" policy, on the other. (*See* CX0903 at 2 ("Open standards seem at odds with our business model ... [t]he job of JEDEC is to create standards which steer clear of patents")).

421. Complaint Counsel did not show that Mr. Crisp had received a copy of the June 1992 draft business plan.

Response to Finding No. 421: This Proposed finding cites to no record evidence. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge*

and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

422. Rambus CEO Geoff Tate testified that the statement in the June 1992 draft plan that "we believe that Sync DRAMs infringe on some claims in our filed patents"was based on a "feeling" that "synchronous DRAMs sure looked like they stem[med] from [our] inventions." (CX 2073, Tate Micron Depo. at 221-22). Mr. Tate had "assumed" that broad patent applications had been filed to protect all of Rambus's inventions. (CX 2073, Tate Micron Depo. at 222; CX 2088, Tate Infineon Trial Testimony at 57). At the time that he wrote the 1992 Business Plan, Mr. Tate did not know of any particular claim that might be infringed by SDRAMs. (*Id.*).

Response to Finding No. 422: This Proposed finding is incomplete and therefore misleading. The more complete statement from Mr. Tate in his Micron deposition, as noted previously at CCFF 811, is "I recall that our feeling was that synchronous DRAMS sure looked like they were stemming form our inventions that we had done first, and that our understanding is that patents are supposed to protect your inventions, and we assumed that our patents had been filed to do so. And that led us to a conclusion that, hey, we must have some claims they are infringing ..." (CX2073 at 221-22 (Tate, Micron Dep.)). This knowledge or belief, as stated in the testimony and in the 1992 Rambus Business plan, was sufficient to trigger a disclosure obligation. (*See* CCFF 333 - 340).

423. After the 1992 Business Plan was prepared, a Rambus employee was assigned the task of determining what filed claims would be infringed by SDRAMs. (CX 2073, Tate Micron Depo. at 222-3). The employee subsequently informed Mr. Tate that the filed claims were not as broad as previously thought and did not cover the full range of what had been invented and disclosed in the '898 application. (CX 2073, Tate Micron Depo. at 222-24; CX 2088, Tate Infineon Trial Testimony at 57-58).

Response to Finding No. 423: The Proposed finding is misleading and unreliable since the mysterious "Rambus employee" referenced in this Proposed finding is not identified in Mr. Tate's testimony or anywhere else in the record . In addition, the Proposed finding ignores other evidence that Rambus' clear intent was to obtain patent coverage that would "cover" the SDRAM standard. (*See* CCFF 803 - 806 and CCFF cited therein). Additionally, the Proposed

finding is misleading because it ignores other evidence that the duty to disclose at JEDEC was not triggered by a claim or application that actually covered the work being discussed, but that the intellectual property activity needed only to be reasonably related to the technology under consideration. (*See* CCFF 335 - 337).

424. Complaint Counsel also point to a June 1993 e-mail by Rambus engineer Fred Ware that states that a claim in a Rambus patent application was "directed against SDRAMs." (CX 1959 at 1). Complaint Counsel did *not* contend at trial, however, that in June 1993 Rambus had *any* claim in a pending application that covered *any* feature of SDRAMs. To the contrary, as noted above, the only Rambus patent claims that are even alleged by Complaint Counsel to cover SDRAMs are claims in the '961 and '490 applications; these claims were not filed until 1995. *See* Findings ¶ 362.

Response to Finding No. 424: While the citation to CX1959 is accurate, the Proposed finding is misleading in that it assumes that the duty to disclose intellectual property at JEDEC was triggered only by a relevant claim or patent application that literally "covered" the JEDEC work; as noted elsewhere, that is not the standard. (*See* CCFF 335-37). For the relationship between the '651 application, described in Mr. Ware's e-mail, and the JEDEC SDRAM standard, *see* CCFF 876, 894, 900-01, 910, 920-27, 932-34, 947-48, 955, 958-61.

425. In their opening statement, Complaint Counsel asserted that Mr. Ware's June 1993 e-mail referred to a May 1993 "amendment to Rambus's pending '651 application [application serial no. 07/847,651] related to the concept of programmable CAS latency and that this amendment was intended to cover programmable CAS latency when used in DRAMs generally, including SDRAMs that were the subject of JEDEC work." (Opening Statement, Tr. 84-85). However, all the claims in the May 1993 amendment to the '651 application contained the limitation that data, address, and control information be "in the form of packets," a feature that, according to Complaint Counsel, is not found in SDRAMs. (CX 1458 at 5-8). Complaint Counsel elicited testimony from numerous witnesses that SDRAMs, unlike RDRAMs, do not receive information in the form of packets. (Rhoden, Tr. 402; Sussman, Tr. 1431-32; Kelley, Tr. 2573-74; Kellogg, Tr. 5298; Jacob, Tr. 5466-67). Complaint Counsel did *not* contend at trial that the claims contained in the May 1993 amendment to the '651 application covered programmable latency as used in JEDEC-compliant SDRAMs.

Response to Finding No. 425: *See* CCRF 425. The Proposed finding is misleading because it suggests that the relevant JEDEC disclosure rules applied only to patent applications that literally "covered" JEDEC work or a JEDEC standard, implying that an

infringement analysis is required; as noted in response to the two previous proposed findings, this is not the case. (*See* CCFF 335 - 337). For the relationship between the '651 application, described in Mr. Ware's e-mail, and the JEDEC SDRAM standard, *see* CCFF 876, 894, 900-01, 910, 920-27, 932-34, 947-48, 955, 958-61.

Furthermore, the proposed finding ignores other evidence that the restrictions in the claims were removed in another patent application in the '898 family by January 1995 such that the then pending application could be interpreted to cover the JEDEC SDRAM standard (CCFF 1125 - 1163), and in January 1995 Rambus was still an active member of JEDEC. (CCFF 1124).

426. Rambus's JEDEC representative, Richard Crisp, testified that during the time that Rambus was a JEDEC member, he: (1) had not seen any Rambus patent application with claims over an SDRAM that used any of the four features at issue here; and (2) did not know one way or the other whether Rambus's pending patent applications covered JEDEC-compliant SDRAMs using any of those features. (Crisp, Tr. 3540-43; 3461-66).

Response to Finding No. 426: This proposed finding is misleading because it is not fully supported by the cited testimony and contradicted by other record evidence in the form of both documents and testimony from the same witness, Mr. Crisp, indicating that he was aware of Rambus patent activity with the intent to cover JEDEC-complaint SDRAMs and/or festures and technologies being discussed at JEDEC. (*See* CCFF 854 (prior testimony indicating that Mr. Crisp was aware that claims being drafted with intent to cover SDRAM standard; CX2092 at 192 (Crisp, Infineon Trial Tr.) ("Q: Am I right, sir, that Rambus was intentionally drafting claims to intentionally cover JEDEC SDRAMs? A: Partially true, yes.");CX2092 at 258-59 (Crisp, Infineon Trial Tr.) ("Q: And those are the very features that you saw at JEDEC and that you met with your lawyer about and that Rambus' patent applications ultimately changed into; isn't that right? A: I think those issues were discussed there in some form or another, and we certainly had patent applications that covered aspects of those, of those technologies."); CX0711 at 36-37 ("What is the exact status of the patent with the PLL claim?****" appears in Crisp-authored e-

mail after observing JEDEC presentation on on-chip PLL technology); *see generally* CCFF 856 - 857 and CCFF cited therein). In addition, the Proposed finding is also misleading because it ignores evidence that the JEDEC disclosure rules did not apply only to instances where claims in a patent or application actually "cover' the standard. (*See* CCFF 335 - 337). As Mr. Crisp has previously testified, JEDEC "wanted to know about both patents and patent applications that might relate to the works that were going on within JEDEC." (CX2104 at 852-53 (Crisp, Dep.), cited previously at CCFF 820).

427. During the time Rambus was attending JEDEC, Dr. Farmwald did not believe that Rambus's patents were infringed by SDRAMs. (CX 2106, Farmwald FTC Depo at 70).

Response to Finding No. 427: This Proposed finding is incomplete and misleading as Dr. Farmwald's deposition testimony is taken out of context; in the same answer, he admitted this was a "vague recollection" of his thoughts, emphasizing that "it's not the company view at all." (CX2106 at 70 (Farmwald, Dep.)). Complaint Counsel would also note that Respondent objected to the cited testimony on the grounds of "no foundation, improper opinion" (*See* Master List of Designated Deposition Testimony filed August 25, 2003) thus indicating that Respondent has some question about the reliability of the cited testimony.

428. In March 1998, Joel Karp informed Rambus's board of directors that Rambus's existing patent claims were narrowly framed. (Farmwald, Tr. 8231-34; CX 615 at 2). Mr. Karp also informed the board that he believed that he could improve the strength of the patent portfolio, but that it would take a year or two to do so. (Farmwald, Tr. 8231-32).

Response to Finding No. 428: This Proposed finding is misleading and inaccurate; nowhere in the cited testimony or document does it say that the patent claims were "narrowly framed.." There is some testimony from Dr. Farmwald about being informed that there were "a lot of unnecessary restrictions" in certain claims (Farmwald, Tr. 8231) but this does not mean that the claims were narrowly framed. The cited document (CX0615) states that Mr. Karp, among other items, reviewed "the results of his review of potential weaknesses in the Company's

intellectual property portfolio" (CX0615 at 2) and thus does not provide any direct support for the proposed finding. Furthermore, the Proposed finding ignores the portion of Dr. Farmwald's testimony where he states his awareness that "we felt very strongly that we either had or could get patents on DDR." (Farmwald, Tr. 8232).

429. By July 1999, Mr. Karp had done a thorough review of Rambus's patent portfolio, observed a number of weaknesses that could be repaired, recognized new patent applications or amendments that could be filed, and was actively working on these projects. (Farmwald, Tr. 8237-38; CX 622 at p.2 (July 14, 1999 board minutes referring to Karp presentation)).

Response to Finding No. 429: This Proposed finding is misleading and inaccurate. Dr. Farmwald testified that he had no recollection of a specific meeting, and there is nothing in the cited transcript about new applications or amendments; Dr. Farmwald's recollection that "a lot of new patents that could be filed" (Farmwald, Tr. 8238) does not itself suggest that prior patent claims or coverage were inadequate. The cited document (CX0622) states that "Mr. Karp reviewed the Company's strategic portfolio of current intellectual property and plans for an additional strategic portfolio for extending the life of Rambus IP" (CX0622 at 2) and thus does not provide any support for the proposed finding.

430. It was not until mid-1999 that a Rambus patent issued with claims that were infringed by JEDEC-compliant SDRAMs or DDR SDRAMs. (Farmwald, Tr. 8239-40; CX 623 (October 14, 1999 board minutes referring to strategic IP issues)).

Response to Finding No. 430: This Proposed finding is inaccurate and misleading and contradicted by other evidence. The cited testimony and documents do not state that mid-1999 was the first patent issued to Rambus with claims covering JEDEC-complaint SDRAMs or DDR SDRAMs. While it is true that the patents that Rambus chose to enforce against DRAM manufacturers in patent litigation did not issue until 1999, that does not mean that earlier issued patents did not contain relevant claims as well. The Proposed finding ignores other record evidence that two claims in the '327 patent (issued to Rambus some three years earlier, in

April 1996) could be construed to cover the dual-edge clocking feature used in the JEDEC DDR SDRAM standard. (*See* CCFF 1224 - 1228, 1234 - 1237). In addition, the '481 patent, which issued in August of 1997, had claims relating to phase lock loop circuitry and PLLs on memory devices. (*See* CCFF 1644 - 1645) There was expert testimony that an earlier version of these claims, pending while Rambus was a member of JEDEC, covered the on-chip PLL feature that had been presented to JEDEC in 1994. (*See* CCFF 1183 - 1198; *see* also CCFF 1642 - 1644 (explaining subsequent patent prosecution by Rambus)). Complaint Counsel would also note that Rambus has vigorously asserted attorney-client privilege with respect to certain post-June 1996 documents which, if produced, likely would shed light on any decision not to seek to enforce the earlier-issued patents against JEDEC-compliant DDR SDRAM devices.

E. Rambus Did Not Violate Any JEDEC Rule Or Policy Simply By Seeking Patent Protection For Inventions That Related To JEDEC Standards, For There Was No Such Rule Or Policy.

431. Complaint Counsel have suggested at times that JEDEC's rules or policies discourage or even preclude members from seeking patent coverage for inventions that relate to JEDEC standards. The evidence does not support such a view.

Response to Finding No. 431: RPF 432 lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, Complaint Counsel submits that the obligation to disclose relevant intellectual property extends to those instances in which (1) a member engages in efforts to patent technologies that might be involved in the work of a JEDEC committee; and (2) knows or believes that it has patents or patent applications that could be amended to relate to technologies that might be involved in the work of a JEDEC committee. *See* CCFF 319-20.

432. The EIA Legal Guides, which governed JEDEC standardization activities while Rambus was a JEDEC member, state explicitly that "[s]tandards are proposed or adopted by EIA without regard to whether their proposal or adoption may in any way involve patents on articles, materials, or processes." (CX 204 at 4).

Response to Finding No. 432: Complaint Counsel does not disagree. This proposed finding is incomplete, however, because the JEDEC patent disclosure policy also governs the standardization activities of JEDEC. *See* CCFF 318-434. This proposed finding also is misleading because the cited language acted as a disclaimer that "EIA does not conduct patent searches, and therefore, can't assume any liability if patents somehow creep into standards unbeknownst to us." (J. Kelly, Tr. 1835).

433. The EIA's January 22, 1996 comment letter to the FTC states in part that "[a]llowing patented technology in standards is procompetitive." (RX 669 at 2). The letter explains that "[b]y allowing standards based on patents, American consumers are assured of standards that reflect the latest innovation and high technology the great technical minds can deliver." (RX 669 at 2-3).

Response to Finding No. 433: Complaint Counsel does not disagree. This proposed finding is misleading, however, to the extent that it suggests that JEDEC was indifferent to the inclusion of patented technology in its standards. Mr. Kelly testified that "[T]here are times when patented technology may represent the best technological solution, and in that case, *notwithstanding our preference not to include patents or patent applications*, as the case may be, in standards, we will consider the inclusion of that technology, provided there's early disclosure and provided there are written assurances . . . either without charge or reasonable and nondiscriminatory." (J. Kelly, Tr. 1868-69).

434. The EIA's January 22, 1996 comment letter to the FTC also states that "[s]tandards in these high-tech industries must be based on the leading edge technologies. Consumers will not buy second-best products that are based only on publicly available information. They demand and deserve the best technology these industries can offer." (RX 669 at 4).

Response to Finding No. 434: Complaint Counsel does not disagree. In fact, it is because of the high-tech nature of JEDEC standards that JEDEC requires participants to disclose

patent applications in addition to issued patents. Mr. Kelly explained the reason why, in his view, it makes sense for EIA and JEDEC to have more demanding patent disclosure policies by comparison to other ANSI affiliates: "It's because we're in a high technology, fast-moving, fast-paced industry in terms of product development and intellectual property development, but ANSI deals with a number of different industries." Tr. 1959; *id.* at 1912 ("in the IT area where we operate, our space, it is critically important to get out information about relevant IP as early in the process as possible, and that means patent applications as well as patents").

435. The EIA's January 22, 1996 comment letter to the FTC also states that "[e]ven if knowledge of a patent comes later in time due to the pending status of the patent while the standard was being created, the important issue is the licensing availability to all parties on reasonable, non-discriminatory terms." (RX 669 at 4).

Response to Finding No. 435: Complaint Counsel does not disagree. Indeed, RPF 436 supports the conclusion that the obligation to disclose was continuing in nature. *See* CCFF 346.

436. EIA General Counsel John Kelly testified that there is no objection to having standards that incorporate patented technologies as long as the patents are available to all potential licensees on reasonable and nondiscriminatory terms. (Kelly, Tr. 2072).

Response to Finding No. 436: RPF 437 is misleading. Mr. Kelly testified that EIA would prefer not to include patented technologies in EIA standards, but that such technologies could be included in EIA standards provided that disclosure had been made early in the process and the written licensing assurances had been provided. (J. Kelly, Tr. 1839-40).

437. It is also clear that throughout the time period that Rambus was a member, JC 42.3 routinely passed ballots to adopt technology as part of its standards despite its awareness of patent-related issues.

Response to Finding No. 437: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding

should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding is also misleading because there is no evidence that JEDEC adopted standards that included patented technology where there was no assurance given by the owner of the intellectual property.

438. At the March 1993 JC 42.3 meeting, for example, the committee voted to pass a ballot on Mode Register Timing for the SDRAM draft specification even though Hitachi raised a "patent alert." (JX 15 at 5).

Response to Finding No. 438: Complaint Counsel does agree that Hitachi made a patent-related disclosure at the March 1993 JC-42.3 meeting. It is not clear from the record whether this disclosure related to an issued patent, a patent application, or the expectation of seeking a patent. Moreover, there is no evidence in the record that any technology covered by the patent ever was included in a JEDEC standard. Given the context of the disclosure, it is reasonable to assume that the disclosure included an understanding of how the intellectual property might involve the work of the committee. Thus, the committee could have determined that the patent did not apply to the work of the committee. In addition, given that there is no evidence that the owner(s) of any of the cited intellectual property ever sought to collect royalties, it also is reasonable to assume that the patents, if actually required to comply with the standard, were licensed for free or, at a minimum, on terms that were reasonable and demonstrably free of unfair discrimination.

439. At the March 1993 JC 42.3 meeting, the committee also considered ballots for Self-Refresh Entry/Exit, DQM Latency Reads/Writes, and Auto-Refresh for the SDRAM draft specification. (JX 15 at 8). The minutes state that both Hitachi and Mosaid raised a "patent alert" or a "patent concern" with respect to each of these features. (JX 15 at 8, 9). The committee voted unanimously to pass these ballots. (JX 15 at 8, 9).

Response to Finding No. 439: Complaint Counsel does agree that Hitachi and Mosaid made patent-related disclosures at the March 1993 JC-42.3 meeting. It is not clear from

the record whether these disclosures related to issued patents, patent applications, or the expectation of seeking patents. Moreover, there is no evidence in the record that any technology covered by the patent(s) ever was included in a JEDEC standard. Given the context of the disclosures, it is reasonable to assume that the disclosure included an understanding of how the intellectual property might involve the work of the committee. Thus, the committee could have determined that the patent did not apply to the work of the committee. In addition, given that there is no evidence that the owner(s) of any of the cited intellectual property ever sought to collect royalties, it also is reasonable to assume that the patents, if actually required to comply with the standard, were licensed for free or, at a minimum, on terms that were reasonable and demonstrably free of unfair discrimination.

440. At the March 1993 JC 42.3 meeting, the committee also considered a ballot for a Write Latency = 0 for the SDRAM draft specification. With regard to this ballot, the minutes state that Mosaid raised a patent issue. (JX 15 at 5-6). The minutes also state, "The Committee is aware of the Hitachi patent. It was noted that Motorola has already noted they have a patent. IBM noted that their view has been to ignore patent disclosure rule because their attorneys have advised them that if they do then a listing maybe construed as complete." (JX 15 at 6). The committee voted unanimously to pass this ballot. (JX 15 at 6). At that meeting, the committee also voted unanimously to send all SDRAM ballots to the JEDEC Council for standardization. (JX 15 at 14).

Response to Finding No. 440: Complaint Counsel does agree that Motorola, Hitachi, and Mosaid made patent-related disclosures at the March 1993 JC-42.3 meeting. It is not clear from the record whether these disclosure related to issued patents, patent applications, or the expectation of seeking patents. Moreover, there is no evidence in the record that any technology covered by the patent(s) ever was included in a JEDEC standard. Given the context of the disclosures, it is reasonable to assume that the disclosure included an understanding of how the intellectual property might involve the work of the committee. Thus, the committee could have determined that the patent did not apply to the work of the committee. In addition, given that there is no evidence that the owner(s) of any of the cited intellectual property ever sought to

collect royalties, it also is reasonable to assume that the patents, if actually required to comply with the standard, were licensed for free or, at a minimum, on terms that were reasonable and demonstrably free of unfair discrimination.

RPF 441 also is misleading and contrary to the weight of the evidence to the extent it suggests that IBM refused to comply with the JEDEC patent policy. *See* CCFF 327-29; CCRF 192-97.

441. At the very next JC 42.3 meeting, which was held *before* the SDRAM ballots had been voted on by the JEDEC Council, the 42.3 Committee reviewed an analysis of patents relating to SDRAMs. The analysis, which was prepared by Chipworks, included a discussion of several Hitachi patents related to SDRAMs that were described as "powerful" (CX 53A at 13), as well as SDRAM-related patents held by Motorola and other JEDEC members. (CX 53A at 14).

Response to Finding No. 441: Complaint Counsel does agree that Chipworks provided an analysis of certain patents that had been disclosed to JEDEC *before* the JEDEC Council voted on the SDRAM ballots. RPF 442 supports the conclusion that the requirement to disclosure intellectual property is not limited to the final ballot to create a JEDEC standard. In addition, there is no evidence in the record that any technology covered by the patent(s) ever was included in a JEDEC standard. Given the context of the disclosures, it is reasonable to assume that the disclosures included an understanding of how the intellectual property might involve the work of the committee. Thus, the committee could have determined that the patents or patent applications did not apply to the work of the committee. In addition, given that there is no evidence that the owner(s) of any of the cited intellectual property ever sought to collect royalties, it also is reasonable to assume that the patents, if actually required to comply with the standard, were licensed for free or, at a minimum, on terms that were reasonable and demonstrably free of unfair discrimination.

442. No witness who was present at the March and May 1993 JC 42.3 meetings testified that any criticism was leveled against JEDEC members who had obtained patents relating to SDRAMs.

Response to Finding No. 442: Complaint Counsel does not disagree. The patents were disclosed to the committee. Given the context of the disclosures, it is reasonable to assume that the disclosure included an understanding of how the intellectual property might involve the work of the committee. Thus, the committee could have determined that the patents or patent applications did not apply to the work of the committee. In addition, given that there is no evidence that the owner(s) of any of the cited intellectual property ever sought to collect royalties, it also is reasonable to assume that the patents, if actually required to comply with the standard, were licensed for free or, at a minimum, on terms that were reasonable and demonstrably free of unfair discrimination.

F. Rambus Had No Intent To Violate the Rules Or To Mislead Other JEDEC Members.

443. Complaint Counsel have asserted that Rambus "acted with knowledge that it was violating" JEDEC's rules relating to intellectual property disclosures. (Complaint Counsel's Pre-Trial Brief, p. 196).

Response to Finding No. 443: Complaint Counsel does not disagree.

444. Complaint Counsel did not meet their burden of showing that Rambus intended to violate the patent policies that governed JEDEC standardization activities while Rambus was a member.

Response to Finding No. 444: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. It is also inaccurate. (CCFF 800-66).

1. Rambus Sought And Followed Legal Advice Upon Joining JEDEC To Assist It In Understanding And Complying With Its Legal Obligations.

445. Rambus attended its first JEDEC meeting, in December 1991, at Toshiba's recommendation and as Toshiba's guest. (CX 2054, Mooring 11/15/00 Depo. Tr., 43-44).

Response to Finding No. 445: Complaint Counsel does not disagree. (*See* CCFF 871-78).

446. Rambus decided to join JEDEC because of the prospect of standardizing the RDRAM device, because it seemed to be a useful place to learn marketplace and competitive information, and because it was a good place for "meeting and greeting" potential customers. (CX 2101, Horowitz Depo. Tr., 279; CX 2099, Tate Depo. Tr., 739; CX 2054, Mooring 11/15/00 Depo. Tr., 44).

Response to Finding No. 446: Complaint Counsel does not disagree that these were among the reasons why Rambus decided to join JEDEC. By June 1992, Rambus was also motivated to participate in JEDEC by the prospect of monitoring the JEDEC SDRAM standard development activities and enforcing or threatening to enforce patent claims against firms that at some point practiced the JEDEC SDRAM standard then under development. (CCFF 757-766, 911-18).

447. Shortly after it joined JEDEC, Rambus sought the legal advice of its outside patent counsel, Mr. Lester Vincent, in connection with its participation in JEDEC.

Response to Finding No. 447: Complaint Counsel does not disagree. The advice pertained to the possibility of asserting patent claims against firms applying potential JEDEC standards – specifically, the risk of possible equitable estoppel against Rambus in connection with the assertion of such claims – and the filing of patent application claims on behalf of Rambus relevant to matters under discussion at JEDEC. (*See* CCFF 885-92, 900-01).

448. In March 1992, Richard Crisp and his supervisor, Allen Roberts, talked to Mr. Vincent about JEDEC-related issues. (CX 3125, Vincent 4/11/01 Depo. Tr., 310-315). After discussing JEDEC with Mr. Vincent, "the two key things that [Mr. Crisp] walked away from the meeting understanding was that Rambus should not go and promote a standard, and we should not mislead JEDEC into thinking that we wouldn't enforce our property rights." (Crisp, Tr. 3470-71).

Response to Finding No. 448: This proposed finding is inaccurate and misleading. Mr. Crisp and Mr. Roberts, as well as Rambus CEO Tate, talked to Mr. Vincent on several

occasions in March and April 1992 about JEDEC-related issues and the enforcement of possible patent claims. (CCFF 885-92).

The proposed finding misstates the advice that Mr. Vincent gave to Rambus at or around that time. Mr. Crisp recalled that in a meeting in late March 1992 Mr. Vincent advised Messrs. Roberts and Crisp that even if Rambus did go to JEDEC meetings, stayed silent and didn't do anything else, there was *still* a risk that Rambus patents might be unenforceable by reason of equitable estoppel. (CX2092 at 98 (Crisp, Infineon Trial Tr.)). According to Mr. Crisp, Mr. Vincent was trying to tell Messrs. Roberts and Crisp that if Rambus insisted on going, the least it should do is don't do anything to mislead anybody. (*Id.*).

Mr. Vincent recalled that in this same time period he advised Mr. Crisp and Mr. Roberts that he "didn't think it was a good idea" for Rambus to continue participating in JEDEC, given the downside risk associated with potential equitable estoppel claims that might prevent enforcement of Rambus patents. (CX3125 at 320-21 (Vincent, Dep.) ("Q. Did you tell Richard Crisp and Allen Roberts that at this March 27th, 1992, meeting, that they should not participate in JEDEC? . . . A. . . . I believe at some point early on . . . I believe I said I didn't think it was a good idea"; "Q. The downside risk was that someone was going to raise the issue of equitable estoppel if Rambus attended JEDEC? A. Right. . . .")).

The fact is, of course, that Rambus chose *not* to follow the advice of Mr. Vincent, who told Rambus that *it was not a good idea* to participate in JEDEC. Rambus participated in JEDEC for years, all the while simultaneously pursuing patent applications covering JEDEC work while withholding from JEDEC any meaningful information concerning Rambus intellectual property rights. (CCFF 867-1121).

449. Mr. Vincent's time sheets show that at around the time he gave Mr. Crisp this advice, he reviewed one or more "JEDEC publications." (CX 1937 at 12). At that time, JEDEC

manual 21-H was in effect, and the only language in it relating to intellectual property was the following:

> "JEDEC standards are adopted without regard to whether or not their adoption may involve patents or articles, materials or processes."

(CX0205A at 11).

Response to Finding No. 449: Complaint Counsel does not disagree that Mr. Vincent's time records around this time indicate that he reviewed "JEDEC publications." (CCFF 892). The proposed finding is misleading, however, in suggesting that there is any record evidence of *what* it was that Mr. Vincent reviewed. Mr. Vincent had no recollection of the review, other than seeing the cryptic entry in his time records. (CX3128 at 185-86 (Vincent, Dep.)).

Had Mr. Vincent reviewed the JEDEC 21-H Manual, he would have seen that it was not the sole document setting out the rules for participation in JEDEC. The 21-H Manual specifically states that all JEDEC meetings are to be conducted in accordance with the EIA Legal Guides, and indeed the 21-H Manual specifically incorporates the Legal Guides by reference. (CX0205 at 14; *see* J. Kelly, Tr. 1916-17)). The Legal Guides set forth the basic rules under which EIA and JEDEC engineering standardization programs must operate, including the duty to act "in good faith" and the requirement that EIA and JEDEC standardization programs be operated in a manner that does not result anticompetitive effects, including "excluding competitors from the market." (CX0202 at 6). Had Mr. Vincent reviewed the 21-H Manual, he also would have seen that the Manual states that EIA Legal Counsel was authorized to advise the committees concerning interpretation of the Legal Guides. (CX0205 at 14; *see* J. Kelly, Tr. 1916-17)). There is no record evidence that Mr. Vincent was aware of any of this. (CCFF 852).

Indeed, the record strongly suggests that Rambus was not thorough or forthcoming in keeping Mr. Vincent apprised of the details of its involvement in JEDEC over the period it was a member. Lester Vincent did not not recall being aware of the EIA Legal Guides, the JEDEC Manual 21-I, the Townsend presentations at the JC-42.3 meetings, the patent tracking list, the JEDEC sign-in sheet, internal Rambus emails discussing disclosures within JEDEC, specific requests made to Rambus regarding Rambus patents, any specific presentations made within JEDEC, or emails within Rambus commenting on whether presentations at JEDEC would be covered by Rambus patent rights. (Vincent, Tr. 7996-98). Yet he repeatedly advised Rambus that there was a downside risk that somebody could raise the issue of equitable estoppel. (CX3124 (Vincent Dep. at 191, 197, 320); CX3127 (Vincent Dep. at 114-115); *see also* CX1928 (Vincent notes: ("– No further participation in any standards body (if there has been any) – do not even get close!!")). He came to be joined in this by other counsel for Rambus, inside and outside the company. (*See* CCFF 851).

The fact is, of course, that Rambus chose *not* to follow the advice of Mr. Vincent, who told Rambus that *it was not a good idea* to participate in JEDEC. (CX3125 at 320-21 (Vincent, Dep.)). Mr. Vincent's further advice was that if Rambus insisted on participating in JEDEC, the least it should do is don't do anything to mislead anybody. (CX2092 at 98 (Crisp, Infineon Trial Tr.)). Rambus disregarded this advice by participating in JEDEC for years, all the while simultaneously pursuing patent applications covering JEDEC work while withholding from JEDEC any meaningful information concerning Rambus intellectual property rights. (CCFF 867-1121).

450. Mr. Crisp testified that he followed Mr. Vincent's advice and did not promote a technology for standardization. (Crisp, Tr. 3470).

Response to Finding No. 450: Complaint Counsel does not disagree that Mr. Crisp so testified at trial. But the proposed finding is misleading insofar as it purports to set forth accurately the advice that Mr. Vincent gave Rambus concerning participation in JEDEC. The fact is that Rambus chose *not* to follow the advice of Mr. Vincent, who told Rambus that *it was not a good idea* to participate in JEDEC. (CX3125 at 320-21 (Vincent, Dep.); CCRF 449). Mr. Vincent's further advice was that if Rambus insisted on participating in JEDEC, the least it should do is don't do anything to mislead anybody. (CX2092 at 98 (Crisp, Infineon Trial Tr.)). Rambus disregarded this advice by participating in JEDEC for years, all the while simultaneously pursuing patent applications covering JEDEC work while withholding from JEDEC any meaningful information concerning Rambus intellectual property rights. (CCFF 867-1121).

451. An e-mail that Mr. Crisp wrote in December 1995, almost four years later, shows that he was still mindful of Mr. Vincent's advice at that time. He wrote that he understood that Rambus should not "intentionally propose something as a standard and quietly have a patent in our back pocket. . . ." (CX 711 at 188). As he also stated at the time, he was "unaware of us doing any of this or of any plans to do this." (*Id.*). Mr. Crisp testified that this December 1995 passage referred to "what we would have to do and what we should not do in the event that we were to propose the R-module as a standard." (Crisp, Tr. 3485).

Response to Finding No. 451: This proposed finding is misleading insofar as it purports to set forth accurately the advice that Mr. Vincent gave Rambus concerning participation in JEDEC. The fact is that Rambus chose *not* to follow the advice of Mr. Vincent, who told Rambus that *it was not a good idea* to participate in JEDEC. (CX3125 at 320-21 (Vincent, Dep.); CCRF 449). Mr. Vincent's further advice was that if Rambus insisted on participating in JEDEC, the least it should do is don't do anything to mislead anybody. (CX2092 at 98 (Crisp, Infineon Trial Tr.)). Rambus disregarded this advice by participating in JEDEC for years, all the while simultaneously pursuing patent applications covering JEDEC work while withholding from JEDEC any meaningful information concerning Rambus intellectual property rights. (CCFF 867-1121).

The proposed finding is misleading as well in its selective quotation from Mr. Crisp's email, which makes no reference at all to any advice from Mr. Vincent. The risk at JEDEC, according to the email, was not in proposing a standard for adoption but rather in keeping silent about patent issues: "As long as we mention that there are potential patent issues when a showing or ballot comes to [the] floor, then we have not engaged n [sic] inequitable behavior. . . . The things we should not do are to not speak up when we know that there is a patent issue. . . ." (CX0711 at 188).

452. Rambus did not propose the Rambus module, or "R-module," for JEDEC standardization after Mr. Crisp wrote his December 1995 e-mail. In fact, *no* witness testified that Mr. Crisp promoted *any* technology for standardization at JEDEC at any time during Rambus's membership.

Response to Finding No. 452: Complaint Counsel does not disagree. This proposed finding is irrelevant, however, to the obligation of Rambus to comply with JEDEC rules concerning patent disclosure, which are not limited to parties making presentations at JEDEC. (CCFF 330).

453. Mr. Crisp also followed Mr. Vincent's 1992 advice not to mislead JEDEC members into thinking that Rambus would not enforce its intellectual property. When Mr. Crisp was asked at JEDEC meetings on two occasions to comment about Rambus's intellectual property, he *declined* to comment each time, and the JEDEC members who testified at trial uniformly understood that he had declined to comment. *See* Findings of Fact 492-514, *infra*, and citations contained therein. Mr. Crisp also testified that no one had informed him that his refusal to comment violated any JEDEC rule or policy. (Crisp, Tr. 3490-91).

Response to Finding No. 453: This proposed finding is flatly wrong. The entire conduct of Rambus as a JEDEC member, accomplished in large part through its principal representative Richard Crisp, was intended to and did mislead JEDEC members concerning the extent of intellectual property claims by Rambus in the standards that were the work of JEDEC. For more than four years, Rambus chose to be a member in an organization that was dedicated to open standard-setting (CCFF 300-304) with rules that required the disclosure of meaningful

information concerning patents and patent applications that related to the work of JEDEC (CCFF 310-56). Mr. Crisp attended meeting after meeting of the organization, reporting back to his colleagues as JEDEC members continually disclosed and discussed patent-related issues pertaining to the standards work. (CCFF 867-1121).

Because Rambus was a willing and dues-paying participant in the JEDEC organization, it was reasonable for the other participants to assume that Rambus was a good-faith participant that was willing to abide by the rules of the organization. The Rambus refusals to comment on two occasions in May 1992 and September 1995 (CCFF 902-09, 1062-68) were not open repudiations by Rambus of the JEDEC rules. For a JEDEC member that credited Rambus with participating in good faith in an organization that required disclosure, the "no comment" responses by Rambus could only be interpreted as indications that Rambus *did not have* any relevant intellectual property to disclose. If in fact this had been true, then the Rambus "no comment" responses would have been fully consistent with the JEDEC rules.

In fact, not only by his attendance for Rambus but in other ways, Mr. Crisp affirmatively portrayed Rambus to other JEDEC members as a firm that intended to comply with the JEDEC patent disclosure rules. In September 1993, Mr. Crisp disclosed to JEDEC the issuance of the Rambus '703 patent, even though its content did not pertain to any JEDEC work. (CCFF 968-76). In September 1995, when there was discussion among JEDEC members in the aftermath of the reading of the Rambus "no comment" letter, Mr. Crisp reminded the 42.3 Committee that Rambus in the past had reported a Rambus patent to the Committee. (Crisp, Tr. 3312). This was a reference to the disclosure to the Committee of the Rambus '703 patent in September 1993. (*Id.*). Mr. Crisp was saying that Rambus was in the category of JEDEC members that *had disclosed* patents. (Crisp, Tr. at 3313). Rambus continued to portray itself as a discloser of patents even in

its letter withdrawing from JEDEC, which included a list of Rambus patents but omitted the Rambus '327 patent that pertained to ongoing JEDEC work. (CCFF 1109-14).

The truth is that JEDEC members, and the DRAM industry generally, *were* misled. Throughout the 1990's, Rambus aggressively promoted its proprietary RDRAM technology while at the same time concealing its intellectual property claims to the JEDEC standard technology. (CCFF 1238-1259, 1676-1700). Even firms that initially had Rambus patent concerns came to believe that their suspicions were unfounded. (CCFF 1260-65). Only when Rambus began asserting its patent claims in late 1999 against firms practicing the JEDEC standards did firms begin to understand that Rambus claimed patent rights to the JEDEC standard technology. (CCFF 1950-74).

454. Mr. Crisp's refusal to comment at the September 1995 JEDEC meeting could not have been clearer:

> "At this time, Rambus elects to not make a specific comment on our intellectual property position relative to the Synclink proposal. Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property."

(RX 602 at 1; JX 27 at 4, 26).

Response to Finding No. 454: The supposed clarity of the letter referred to in this proposed finding is belied on its very face. The letter did not repudiate JEDEC or the JEDEC rules. It did not say that Rambus had, or did not have, intellectual property claims pertaining to the SyncLink technology that had been inquired about at a meeting in May 1995. (*See* CCFF 1043-44). As Mr. Crisp reported to his Rambus colleagues later, Gordon Kelley of IBM commented concerning the Rambus letter at the September 1995 meeting that "he heard a lot of words but did not hear anything sa*id*." (CX0711 at 166).

The proposed finding neglects to state that Mr. Crisp rendered the Rambus letter even more ambiguous by his verbal representations at the meeting. In the course of the discussion of the Rambus letter at the September 1995 Committee meeting, Mr. Crisp reminded the Committee that Rambus in the past had reported a Rambus patent to the Committee. (Crisp, Tr. 3312). This was a reference to the disclosure to the Committee of the Rambus '703 patent in September 1993. (*Id.*). Mr. Crisp was saying that Rambus was in the category of JEDEC members that had disclosed patents. (Crisp, Tr. at 3312).

There is nothing in the letter informing the Committee that Rambus had pending patent applications relating to specific SDRAM technologies of programmable CAS latency, programmable burst length, on-chip PLL or DLL, and dual edge clocking. (CX2056 at 274 (Mooring, Dep.)). There is nothing in the letter informing JEDEC members that Rambus was actively pursuing patent claims directed to the SyncLink technology in order to, in Mr. Crisp's words, "shoot SyncLink in the head." (CX0797; CCFF 1050-55, 1067).

455. Mr. Crisp was also advised by Mr. Vincent, in the 1992 time frame, about the importance of keeping patent applications confidential. Mr. Crisp testified as follows:

> "Q: Did [Vincent] at any time give you any legal advice with respect to the disclosure of patent applications?
> A: Yes, he d*id.*
>
> Q: What was that advice?
> A: He told us to not disclose our patent applications. They were confidential.
>
> Q: Did you have an understanding in that time period of any consequences that might result from disclosure of applications?
> A: Yes, I d*id.*
>
> Q: What was your understanding at the time?
> A: I understood that companies could potentially file interference actions on our patent applications in the patent office; that in certain countries where the rules are first to file, somebody could potentially file a claim before we actually did; and that we basically

> would be disclosing trade secrets that could work against us in terms of our competitive position in the marketplace.
>
> Q: Did you do anything with this advice from Mr. Vincent?
> A: Yes, I d*id.*
>
> Q: What did you do?
> A: I followed it."

(Crisp, Tr. 3496).

Response to Finding No. 455: Complaint Counsel does not disagree that Mr. Crisp so testified at trial. However, there is no credible evidence that patent application confidentiality was a realistic concern, that this was the reason for the Rambus campaign of concealment, or that concerns about patent confidentiality can be legitimate justification in light of the voluntary decision by Rambus to participate as a member in JEDEC, an organization whose rules mandated disclosure of meaningful information concerning patent applications.

Rambus had no legitimate concern that disclosures to JEDEC concerning the Rambus '898 patent application after April 18, 1990, and October 31, 1991, would jeopardize its foreign patent rights based on the '898 application because another inventor might "race to the foreign patent office" ahead of it. Rambus's PCT application and foreign patent applications based on the '898 application had a "priority date," meaning a legally effective filing date, of April 18, 1990. (Fliesler, Tr. 8839-40; 8883-8884, 8888; CCFF 1118-20, 1669-74, 2024). Any competitor that "raced" to a foreign patent office to file a patent application after April 18, 1990, could not claim to be the first-to- file a patent application for any invention described in the PCT or other foreign patent applications, simply because the competitor would have the later filing date.

The PCT application was published and publicly available by October 31, 1991. (CCFF 1267; CX1454 at 1; The Parties First Set of Stipulations, Stipulation 8). Competitors who attempted to file foreign patent applications after October 31, 1991 on inventions described in the

PCT application would face that publication as prior art. Generally, prior art may be thought of as prior technological developments that are public prior to a patent application's filing date. (Nusbaum, Tr. 1501). After the publication of the PCT application, a competitor could not claim patent rights on any invention described in it. The Rambus patent law expert, Mr. Fliesler, confirmed at trial that foreign applications would be accorded the benefit of the U.S. filing date. (Fliesler, Tr. 8839-40). He admitted that he could not name a foreign country in which the foreign application would not receive the benefit of the U.S. filing date, but would seek the advice of foreign counsel. (Fliesler, Tr. 8886-87).

There is also no credible support for the conclusion that a concern about foreign patent rights motivated Rambus's decision to not disclose patents and patent applications to JEDEC. (*See* CCRF 93). The record evidence shows that Rambus filed patent applications with all key foreign authorities during 1991, including those in Europe, Israel, Japan, Korea, Taiwan & India. (CCFF 1115-21). The evidence does not show that Rambus filed a patent application in any other country at any time from 1992 to 2003. The implication is unmistakable: for almost all the time it was a JEDEC member, Rambus knew it was not in any race to file foreign patent applications.

The contemporaneous documents indicate that the reason Rambus did not disclose its patent applications to JEDEC was because Rambus did not want to provide JEDEC the opportunity to design around its patents – in other words, its leverage was better to wait. (CX0711 at 68, 73 (Crisp e-mail, 5/24/95: "[I]t makes no sense to alert them to a potential [patent] problem they can easily work around."); CX0919 (Tate e-mail, 2/10/97: "do *NOT* tell customers/partners that we feel DDR may infringe – our leverage is better to wait"); CX0942 (Tate e-mail, 8/4/97: "our policy so far has been NOT to publicize our patents and i think we should continue with this"); CX0960 (Tate e-mail, 10/1/97: "when joel [karp] starts we have to have our spin control ready for partners/etc as to why we are hiring him and what he will be

doing."); CX0987 at 4 (Tate e-mail, 1/19/98: "ddr infringes our patents (question: when do we start saying this publicly?)"); CX1089 (Tate e-mail, 12/9/99: "it's important NOT to indicate/hint/wink/etc what we expect the results of our infringement analysis to be!!!")).

Finally, even if there had been concerns by Rambus about the confidentiality of its patent applications and patents, this in no way can justify its campaign of concealment at JEDEC. For more than four years, Rambus chose to be a member in an organization that was dedicated to open standard-setting (CCFF 300-304) with rules that required the disclosure of meaningful information concerning patents and patent applications that related to the work of JEDEC (CCFF 310-56). Mr. Crisp attended meeting after meeting of the organization, reporting back to his colleagues as JEDEC members continually disclosed and discussed patent-related issues pertaining to the standards work. (CCFF 867-1121). If Rambus truly believed its interests required concealment of its patent claims in violation of JEDEC rules, it had no business continuing for years as a JEDEC member.

456. In addition, in his letters transmitting copies of Rambus's patent applications, Mr. Vincent reminded Rambus employees to "keep in mind that this information is confidential." (CX1951 at 2; CX1945 at 2).

Response to Finding No. 456: There is no evidence that remotely suggests that Mr. Vincent intended his boilerplate transmittal letters to be construed as advice to Rambus about refusing to comply with JEDEC rules.

457. Mr. Crisp described his thinking about Rambus's reasons not to disclose patent applications in a September 23, 1995 e-mail:

> "[w]e decided that we really could not be expected to talk about potential infringement for patents that had not issued both from the perspective of not knowing what would wind up being acceptable to the examiner, and from the perspective of not disclosing our trade secrets any earlier than we are forced to."

(CX0387 at 2).

Response to Finding No. 457: This proposed finding is incomplete and misleading. The excerpt from CX0837 (Respondent erroneously cited to CX0387) confirms that it was not the JEDEC rules but rather "We" – Rambus – who decided what it could be expected to talk about at JEDEC. But the excerpt fails to reflect that the quoted passage pertains explicitly to "the beginning of the period" when Rambus was attending meetings of JEDEC, a time when Rambus had no issued patents. (CX0837 at 2). The text, from September 1995, goes on to note that "As time passed some of the patents issued and then we have not really made the committees aware of this fact ... ." (*Id.*). Mr. Crisp went on to argue to his colleagues that "we should re-evaluate our position relative to what we decide to keep quiet about, and what we say we have." (*Id.*). The text argues that disclosure in some form should be made to JEDEC "to be clean on this." (*Id.*).

In short, the text itself makes clear that, to Mr. Crisp, Rambus was not being "clean" with JEDEC, and that by 1995 any hypothetical concern about confidentiality no longer justified the position of concealment that Rambus had continued to take with respect to JEDEC. The fact is that Rambus chose not to make even the limited disclosure argued for by Mr. Crisp in this email. (*See* CCFF 1062-68). This simply confirms what the other evidence makes abundantly clear – that it was not patent application confidentiality concerns that motivated Rambus, but rather the strategic benefits of concealing its intellectual property claims to the JEDEC standard technology that was under continuing development.

458. Mr. Crisp testified that this e-mail passage reflects the advice he had received from Mr. Vincent. (Crisp, Tr. 3473).

Response to Finding No. 458: Complaint Counsel does not disagree that Rambus counsel elicited this testimony from Mr. Crisp at trial, though he did not recall any particular meeting when Mr. Vincent provided him the advice and gave no details of the discussion. (Crisp,

Tr. 3473). Rambus counsel did not attempt to elicit any such testimony from Mr. Vincent, however.

459. Mr. Crisp was present at a JEDEC meeting when an IBM representative stated that he would not disclose intellectual property at JEDEC meetings. Mr. Crisp understood from that statement that such disclosures were not required. (Crisp, Tr. 3505-07).

Response to Finding No. 459: The cited testimony does not remotely resemble the proposed finding. At Tr. 3507, Rambus counsel quoted from a document prepared by TI that stated in part "IBM has advised the committee that in the future it will not come to the committee with a list of applicable patents." When asked whether he had heard Gordon Kelley of IBM say this, Mr Crisp said, "Yes, I think so."

The document quoted by counsel profoundly mis-states the position that IBM took at the time, which is discussed at CCFF 327-29. More to the point, however, the cited testimony of Mr. Crisp expressed no understanding whatever that disclosure of intellectual property at JEDEC meetings is not required. Such testimony would have been contrary to abundant evidence making clear that Mr. Crisp clearly understood the JEDEC disclosure rules. (*See, e.g.,* CCFF 823, 835-47).

460. In sum, Complaint Counsel failed to meet their burden of proving that Rambus knew of and intentionally violated a JEDEC disclosure requirement.

Response to Finding No. 460: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

461. Complaint Counsel also failed to meet their burden of showing that any JEDEC disclosure obligation that is based on the "actual knowledge" of a JEDEC representative was ever triggered with respect to Mr. Crisp. (Crisp, Tr. 3540-43; 3461-66). *See also* Findings ¶¶ 342, 348, 351, 358, 365, 370, 378, 383. Instead, the unrebutted evidence is that while Mr. Crisp may have *hoped* that Rambus might have rights to certain technologies, he did not, while attending JEDEC meetings, know "one way or the other" whether Rambus had pending patent applications

that would cover SDRAMs that incorporated or made use of those technologies. (*Id.*). Indeed, after a review in June or July 1995 of Rambus patents and patent applications, he "didn't see that we had anything that applied to SDRAM" or to the SyncLink device. (Crisp, Tr. 3540-43).

Response to Finding No. 461: This proposed finding constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. For Complaint Counsel's response to Rambus arguments concerning these issues, *see* CCRF 342, 348, 351, 358, 365, 370, 378, 383.

462. It is thus apparent that even if a mandatory disclosure obligation applied to JEDEC members when they had "actual knowledge" of patents (or applications) that covered a proposed standard, those disclosure obligations were not triggered as to Mr. Crisp or Rambus.

Response to Finding No. 462: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

VI. RAMBUS DID NOT LULL ANY JEDEC MEMBER INTO BELIEVING THAT RAMBUS WOULD NOT HAVE OR WOULD NOT ENFORCE INTELLECTUAL PROPERTY WITH RESPECT TO FEATURES INCORPORATED WITHIN THE SDRAM OR DDR SDRAM STANDARDS.

463. The Complaint alleges that Rambus intentionally gave the members of JEDEC 42.3 the "materially false and misleading impression . . . that JEDEC, by incorporating into its SDRAM standards technologies openly discussed and considered during Rambus's tenure in the organization, was not at risk of adopting standards that Rambus could later claim to infringe upon its patents." (Complaint, ¶ 71).

Response to Finding No. 463: The weight of the evidence in the record supports the allegation in the Complaint that this proposed finding refers to. (*See* CCFF 902-909 (showing that when Mr. Crisp was asked to comment on Rambus's intellectual property during the May 1992 JEDEC meeting, he declined); CCFF 1238-1243 (showing that even though Rambus actively promoted its technology while it was a JEDEC member, Rambus did not begin to tell

people that its patents applied beyond RDRAM until late 1999 or early 2000); CCFF 1244-1259 (showing that until late 1999 or early 2000 several JEDEC participants, who had attended presentations by Rambus on its RDRAM architecture, concluded that Rambus patents were limited to its RDRAM architecture and continued to believe that SDRAM and DDR SDRAM were royalty free architectures); CCFF 1260-1265 (showing that firms with concerns about Rambus intellectual property claims came to believe that their suspicions were unfounded); CCFF 1676-1700 (showing that even after Rambus withdrew from JEDEC, it continued to conceal its JEDEC-related intellectual property); *see also* CCFF 746-756).

464. The evidence demonstrates, however, that Rambus said nothing and did nothing to mislead JEDEC 42.3 members into believing that Rambus would not seek or enforce intellectual property rights over features incorporated in JEDEC standards.

Response to Finding No. 464: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Furthermore, it is contrary to the weight of the evidence as set forth in CCRF 464.

A. JEDEC Members And JEDEC Committee Leaders Were Aware As Early As 1992 That Rambus Might Obtain Patent Rights With Respect To Features Being Considered For Incorporation Into JEDEC Standards, And Rambus Did Nothing To Dispel Or Alleviate Those Concerns.

1. Rambus's Conduct At The May 1992 JEDEC Meeting Did Not Mislead JEDEC Members Or Leaders On Issues Relating To Rambus's Intellectual Property.

465. Several witnesses testified at trial about an exchange at the May 1992 JEDEC meeting that involved the JEDEC representatives from IBM, Siemens and Rambus, respectively, during which issues relating to Rambus's intellectual property were raised.

Response to Finding No. 465: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding

should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

466. In order to understand fully the significance of this May 1992 exchange involving Siemens, IBM and Rambus representatives, it is useful to examine Siemens' and IBM's DRAM development efforts in the spring of 1992.

Response to Finding No. 466: RPF 467 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

467. In the spring of 1992, IBM and Siemens (whose former semiconductor division is now called Infineon Technologies) were cooperating on a joint venture to develop and produce a new DRAM design. (Kelley, Tr. 2532; Meyer, Infineon Trial Tr. 4/25/01, 277:18-23, 310:6-11).

Response to Finding No. 467: Complaint Counsel does not disagree.

468. Both the Siemens JEDEC representative, Willi Meyer, and the IBM JEDEC representative, Gordon Kelley, were involved in the Siemens/IBM DRAM development efforts in the spring of 1992. (Kelley, Tr. 2620-21). The efforts included a consideration of the Rambus technology. (Kelley, Tr. 2627).

Response to Finding No. 468: Complaint Counsel has no specific response.

469. In March 1992, Mr. Kelley prepared a memorandum regarding Rambus. (RX 240 at 1). Mr. Kelley's March 19, 1992 memorandum refers to "a unique (and probably patented) Rambus protocol" and "a special Microprocessor and DRAM interface (other than industry standard)." (RX 240 at 1). Mr. Kelley's memorandum also states that he had asked an IBM in-house lawyer "to get me a copy of Rambus patents." (*Id.*).

Response to Finding No. 469: The statement in RPF 470 is incomplete. Mr. Kelley testified that he did not receive a copy of the Rambus patents. Nor did he receive a copy of any Rambus patent applications, including the Rambus European patent application. (G. Kelley, Tr. 2627-2629). Further, Mr. Kelley testified that after attending a presentation by Rambus at IBM he believed that Rambus RDRAM was fundamentally different from the SDRAM

technology under discussion at JEDEC and that no intellectual property rights that Rambus had on RDRAM could be applicable to SDRAM at JEDEC. (CCFF 1246; *see also* CCFF 1247-1248).

470. On April 23, 1992, Mr. Kelley attended a presentation at IBM by Rambus founder Mike Farmwald and Rambus executive David Mooring. (Kelley, Tr. 2631; RX 273 at 1).

Response to Finding No. 470: Complaint Counsel does not disagree.

471. According to handwritten notes of the April 23, 1992 Rambus/IBM meeting that were produced in discovery by IBM, a Rambus representative stated at the meeting that Rambus intended to obtain "license fees + royalties from IC company." (CX 2355 at 1). The notes also state that Rambus "want to set industry std." (CX 2355 at 1).

Response to Finding No. 471: The statements in RPF 472 are incomplete. Gordon Kelley testified that following the April presentation he believed that Rambus RDRAM was fundamentally different from the SDRAM technology under discussion at JEDEC and that no intellectual property rights that Rambus had on RDRAM could be applicable to SDRAM at JEDEC. (CCFF 1246). Further, Mr. Kelley testified that after the April presentation and prior to the May 1992 JEDEC JC-42.3 subcommittee meeting, he had a conversation with Mr. Crisp of Rambus. Mr. Crisp asked about the possibility of Rambus making a presentation at JEDEC. On the basis of that conversation, Mr. Kelley understood that there was Rambus intellectual property but that it applied only to Rambus RDRAM technology. (CCFF 1247) Mr. Kelley further testified that through the time he left JEDEC in 1998, Rambus never indicated to him that it might have patent rights over on-chip PLL or dual edge clock technology. (CCFF 1248). David Mooring of Rambus who attended the April presentation testified that the first time that Rambus ever advised any SDRAM manufacturer that Rambus had claims covering features of SDRAMs was to Hitachi in late 1999 or early 2000. (CCFF 1241). Craig Hampel, Rambus technical director who beginning in 1993 participated in numerous meetings and presentations with DRAM manufacturers and other firms to discuss Rambus technology (Hampel, Tr. 8672-73, 8729-31), was not aware of any instance in which Rambus representatives told the DRAM manufacturers

which aspects of RDRAM were Rambus inventions, or were protected by Rambus patents or patent applications. (Hampel, Tr. 8732-33).

472. In April 1992, Gordon Kelley prepared a "Rambus Assessment" along with two other IBM employees, Dr. Beilstein and Michael Clinton. (RX 279 at 1). The "Rambus Assessment" is dated April 24, 1992, the day after Mr. Kelley had attended the presentation by Rambus. (RX 279 at 1; Kelley, Tr. at 2635).

Response to Finding No. 472: Complaint Counsel has no specific response.

473. The April 1992 "Rambus Assessment" that Mr. Kelley co-authored refers to "Unique Rambus Features/Attributes." (RX 279 at 1). The "Rambus Assessment" also states that "Intel is Rambus licensee" and notes a "potential future Intel memory strategy to marry . . . 586/686 processor with Rambus protocol to corner PC/notebook market with state of the art performance." (RX 279 at 4).

Response to Finding No. 473: Complaint Counsel has no specific response except to note that RX 279 is consistent with Complaint Counsel's proposed findings that Rambus was promoting its proprietary RDRAM technology while it was a member of JEDEC. (CCFF 1238-1259). The exhibit recommends that IBM should take an RDRAM license "for as little as possible-royalty oriented" as a form of "insurance for the future in case Rambus really catches on." (RX0279 at 8). Nowhere in the document does it indicate IBM was aware that it would need a license from Rambus in order to manufacture SDRAM. To the contrary, a page titled, "Rambus DRAM versus Synchronous DRAM," shows that RDRAM and SDRAM are substantially different from each other apart from the fact that they are both "clocked" and "multibank." (RX0279 at 2). IBM concluded that even without an IBM endorsement, Rambus stood a "reasonable chance although reduced" of becoming a standard. (RX0279 at 7; *see also* G. Kelley, Tr. 2637-38). However, if Rambus failed to become a standard, then IBM concluded that "the SDRAM has a significant chance of being standard." (*Id.*).

474. The "Rambus Assessment" co-authored by Gordon Kelley states that "Rambus can work technically" and notes "the risk is whether it becomes a standard for the low end-bulk of DRAM bit volume – and that it provides a simple low end solution for anyone to get into the PC business." (RX 279 at 8).

Response to Finding No. 474: The statement in RPF 475 is incomplete. Gordon Kelley testified that he did not identify that there was a risk for IBM if Rambus became a standard. In fact, he testified that his hope was that Rambus would bring its RDRAM technology to JEDEC and make it a standard. (G. Kelley, Tr. 2637).

475. The "Rambus Assessment" co-authored by Gordon Kelley states that "[i]f Rambus fails to become standard, then it is business as usual for BTV [the acronym for IBM's Burlington, Vermont operations] and the SDRAM has a significant chance of being standard." (RX 279 at 7).

Response to Finding No. 475: The statements in 476 is incomplete. Gordon Kelley testified that he did not identify that there was a risk for IBM if Rambus became a standard. In fact, he testified that his hope was that Rambus would bring its RDRAM technology to JEDEC and make it a standard. (G. Kelley, Tr. 2637)

476. It is apparent from Mr. Kelley's March and April 1992 analyses of Rambus that he was aware of and focused on Rambus, its technology, and its prospects for success in the spring of 1992. (RX 279; RX 273; RX 240; CX 2355).

Response to Finding No. 476: The statement in RPF 477 is misleading. Mr. Kelley testified that he attended one meeting with Rambus and that only non-confidential information was shared by Rambus. He further testified that he avoided Rambus information (G. Kelley, Tr. 2731) and that he never saw any Rambus intellectual property (G. Kelley, Tr. 2627-2629). He can, therefore, hardly be said to have focused on Rambus, its technology and its prospects for success. The weight of the evidence indicates that Mr. Kelley, like others at the time, understood Rambus's technology to include a "multiplexed protocol" and a "byte [or 8 bit wide] I/O" bus (RX0279 at 2; *see also* CCFF 714-724, 746-756) and that Rambus DRAM was different from SDRAM technology under discussion at JEDEC and that no intellectual property rights that Rambus had on RDRAM could be applicable to SDRAM or JEDEC. (G. Kelley, Tr. 2537-38, 2546).

PUBLIC

UNITED STATES OF AMERICA
BEFORE FEDERAL TRADE COMMISSION

In the Matter of RAMBUS INCORPORATED, a corporation.	Docket No. 9302

COMPLAINT COUNSEL'S REPLY TO RESPONDENT'S PROPOSED FINDINGS OF FACT

Volume II

CCRF 478 - 1044

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478. One week after Mr. Kelley finalized the April 24, 1992 "Rambus Assessment," he participated in a conference call with Siemens JEDEC representative Willi Meyer. The call included a discussion of Rambus. (RX 286A at 1).

Response to Finding No. 478: Complaint Counsel does not disagree.

479. Trial exhibit RX 286A is a memorandum dated April 30, 1992 prepared by Mr. Meyer about a telephone conference involving Meyer, Siemens executive Dr. Martin Peisl, and IBM's Gordon Kelley. (RX 286A; Meyer, Infineon Trial Tr. 4/25/01, 317-319).

Response to Finding No. 479: Complaint Counsel does not disagree.

480. Meyer's April 30, 1992 memorandum states in part: "Rambus: Visited key in-house IBM users. IBM is still keeping its eye on Rambus. Rambus has announced a claim against Samsung for USD 10 million due to the similarity of the SDRAM with the Rambus storage device architecture. For that reason, IBM is seriously considering to preemptively obtain a license as soon as possible (at an introductory price)." (RX 286A at 2).

Response to Finding No. 480: Complaint Counsel does not disagree.

481. Mr. Meyer testified that during the conference call, Gordon Kelley had provided the Rambus-related information contained in Meyer's April 30, 1992 memorandum. (RX 286A; Meyer, Infineon Trial Tr. 4/25/01, 317:5-319:9).

Response to Finding No. 481: Complaint Counsel does not disagree.

482. Siemens executive Martin Peisl similarly testified that the information regarding Rambus that is contained in Meyer's April 30, 1992 memorandum "seems to be information coming from IBM or Gordon Kelley." (Peisl, Tr. 4517).

Response to Finding No. 482: Complaint Counsel does not disagree.

483. Gordon Kelley testified at trial, however, that he did *not* provide the information regarding Rambus that is contained in Meyer's April 30, 1992 memorandum. (RX 286A; Kelley, Tr. 2643). Kelley testified that *Meyer* had provided the information. (Kelley, Tr. 2643).

Response to Finding No. 483: Complaint Counsel does not disagree.

484. Regardless of whether it was Mr. Kelley or Mr. Meyer who provided the Rambus-related information contained in Mr. Meyer's April 30, 1992 memorandum, it is clear that the IBM JEDEC representative (who was also the JC 42.3 chair) and the Siemens JEDEC representative were aware as of April 30, 1992 of a possibility that Rambus might assert intellectual property claims "due to the similarity of the SDRAM with the Rambus storage device architecture." (RX 286A at 2).

Response to Finding No. 484: The statement in RPF 484 is misleading. Gordon Kelley testified that following the April presentation Rambus made to IBM he believed that Rambus RDRAM was so different from the SDRAM technology under discussion at JEDEC and that no intellectual property rights that Rambus had on RDRAM could be applicable to SDRAM at JEDEC. (CCFF 1246) Further, Mr. Kelley testified that after the April presentation and prior to the May 1992 JEDEC JC-42.3 subcommittee meeting, he had a conversation with Mr. Crisp of Rambus. Mr. Crisp asked about the possibility of Rambus making a presentation at JEDEC. On the basis of that conversation, Mr. Kelley understood that there was Rambus intellectual property but that it applied only to Rambus RDRAM technology. (CCFF 1247). Mr. Kelley further testified that through the time he left JEDEC in 1998, Rambus never indicated to him that it might have patent rights over on-chip PLL or dual edge clock technology. (CCFF 1248).

Mr. Meyer testified that after reviewing the Rambus WIPO application and witnessing Mr. Crisp's disclosure of the Rambus '703 patent to JEDEC in September 1993, he made a report to

colleagues at Siemens stating that the JEDEC standard was free of intellectual property (CCFF 1261).

Furthermore, the totality of the evidence in the record indicates that Mr. Meyer's and Mr. Kelley's "awareness" of the possibility of Rambus seeking royalties to SDRAM was limited in two respects. First, it was based on double, perhaps even triple, hearsay. (RX0278A at 2). Someone from Samsung, the evidence does not indicate who, told either Mr. Kelley or Mr. Meyer that Rambus had told Samsung that they wanted money because of the similarity of the "storage device architecture" between SDRAM and RDRAM. (*Id.*). It is not clear whether the source from Samsung who told either Mr. Kelley or Mr. Meyer about Rambus's demand was present when Rambus made that demand or whether he learned about it from someone else at Samsung. (*Id.*).

Second, when this conference call is put in context, it appears that on April 29, 1992, Mr. Kelley and Mr. Meyer learned from someone at Samsung that Rambus might have claims to the multibank, or dual bank, feature that Samsung had been considering for use in an SDRAM. (*See* RX0286A at 2 (Meyer's notes indicate that Mssrs. Meyer and Kelley had information that Samsung was considering both a 2-bank and 1-bank version of SDRAM)). To prepare for a meeting with key designers from IBM and Siemens, Mr. Meyer prepared a document dated May 5, 1992 that lists the following as a negative factor to consider about SDRAM: "2-Bank Sync May Fall Under Rambus Patents." (G. Kelley, Tr. 2530-31; RX0289 at 1). Two days later, during the May 1992 JC 42.3 meeting, both Mr. Kelley and Mr. Meyer indicated their concern that Rambus might have potential patents on multibank design. (CX2089 at 130-135 (Meyer, Infineon Trial)).

At the meeting on May 7, 1992, the JC 42.3 Committee had been discussing a single bank design versus a dual bank design. (*Id.*133). Someone from Phillips stood up during this meeting and "communicated some rumors he had heard that others had made patents on [the dual bank

approach] and also the Rambus was mentioned." (*Id.*). Motorola was also mentioned as possibly having relevant patents. (*Id.*). No one at the meeting "had any fundamental knowledge" about who might have patents on the dual bank approach. (*Id.*). When the discussion about patents over dual bank design appeared to be dying out, Mr. Meyer stated that he was not satisfied with the outcome of the discussion. (*Id.*). Motorola subsequently stated that it would get the Committee the relevant patent numbers if there were any. Perceiving that the discussion was leaving Rambus out, Mr. Meyer asked Mr. Kelley to address the person from Rambus and ask him whether they would like to comment. (*Id.* 133-34). In response to Mr. Kelley's inquiry, Mr. Crisp shook his head no. (*Id.* 136-37).

Even though the JC 42.3 Committee discussed programmable CAS latency and burst length at the May 1992 meeting (CCFF 538), the discussion about intellectual property rights related to SDRAM at this meeting, which identified Rambus as a potential concern, was limited to the dual bank feature. (CX2089 at 130-135 (Meyer, Infineon Trial)). The weight of the evidence, therefore, indicates that Messrs. Meyer and Kelley were not aware that Rambus might have patents over SDRAM in any meaningful way.

485. The privilege log provided by IBM in this matter reflects that on May 1, 1992, there was a presentation about Rambus patents by an in-house lawyer named J. Walter, although Mr. Kelley does not recall whether he attended. (Kelley, Tr. 2647-8). An April 16, 1992 IBM memorandum referenced the fact that Mr. Walter had been asked to review and comment upon Rambus-related intellectual property issues. (RX 272 at 2).

Response to Finding No. 485: The statement in RPF 485 is unreliable. No IBM witnesses were questioned about the document. The only reference to Mr. Walter at RX 272 at 2 states "J. Walter - IP Law Position / Patent Claims."

486. Mr. Meyer also wrote a separate memorandum dated April 30, 1992 that stated in part that "[t]he original idea behind the SDRAM is based on the basic principle of a simple pulse input (IBM toggle pin) and the complex RAMBUS structure." (RX 285A at 5). This memorandum also demonstrates Mr. Meyer's awareness of similarities between the SDRAM device and the "Rambus structure." (RX 285A at 5).

Response to Finding No. 486: Complaint Counsel has no specific response except to note that, viewing this document in context, it is likely that when Mr. Meyer wrote "complex RAMBUS structure" he meant to indicate that both SDRAM and RDRAM used a multibank architecture for the reasons set forth in CCRF 484. Part I of Mr. Meyer's memo is titled, "Standardization Status," and outlines the various features of SDRAM. (RX0285A at 2-5). Subsection b of Part I states, "Similar to the RAMBUS, the plan is to divide the memory chip into at least two separately addressable and time-staggered 'banks' to be operated." (*Id.* at 3).

487. On May 6, 1992, Mr. Meyer prepared a chart showing the "Pros" and "Cons" of "Sync DRAM," "Rambus DRAM," and "Cached DRAM." (RX 289 at 1).

Response to Finding No. 487: Complaint Counsel has no specific response.

488. In his May 6, 1992 "Pros" and "Cons" chart, Mr. Meyer states that the "2-bank" synchronous DRAM "may fall under Rambus patents." (RX 289 at 1).

Response to Finding No. 488: The statement in RPF 588 is incomplete. Mr. Meyer testified that he did not think Rambus had patents at the time covering 2-bank synchronous DRAM but that there was the potential it could obtain such patents. (CX2089 at 44 (Infineon Trial)). Mr. Meyer testified that after reviewing the Rambus WIPO application and witnessing Mr. Crisp's disclosure of the Rambus '703 patent to JEDEC in September 1993, he made a report to colleagues at Siemens stating that the JEDEC standard was free of intellectual property (CCFF 1261).

489. Mr. Meyer testified that at the time, he thought there was a potential that Rambus would obtain patents that would cover synchronous DRAMs. (CX 2089, Meyer, Infineon Trial Tr. 4/26/01, 44:3-23).

Response to Finding No. 489: The statement in RPF 489 is incomplete and misleading. Mr. Meyer testified that there was a potential that Rambus would obtain patents covering 2-bank features that may be included in SDRAMs. (CX 2088, Meyer, Infineon Trial Tr. 4/26/01, 44:3-23).

490. Mr. Meyer also testified that in 1992, "we were absolutely sure that Rambus was trying to get patents." (CX 2088, Meyer, Infineon Trial Tr. 4/26/01, 75:4-14).

Response to Finding No. 490: Complaint Counsel has no specific response.

491. On May 6, 1992, the same date as on Mr. Meyer's "Pros" and "Cons" chart, Mr. Meyer and Mr. Kelley attended a JC 42.3 subcommittee meeting in New Orleans, Louisiana. (CX 34).

Response to Finding No. 491: Complaint Counsel does not disagree.

492. The May 1992 meeting was Richard Crisp's first JC 42.3 subcommittee meeting as Rambus's JEDEC representative. (CX 34 at 1; Crisp, Tr. 2929).

Response to Finding No. 492: The statement in RPF 492 [The May 1992 meeting was Richard Crisp's first JC 42.3 subcommittee meeting as Rambus's JEDEC representative.] is incomplete and misleading because it omits the fact that Richard Crisp attended a JC 42.3 task group meeting on April 9 and 10, 1992. (CX1708; Crisp, Tr. 3009-10).

493. Complaint Counsel predicted in his opening statement that the evidence would show that at the May 1992 JEDEC meeting, JEDEC 42.3 subcommittee chairman Gordon Kelley had asked Rambus representative Richard Crisp "point blank": "Do you have anything to disclose relating to two-bank design" of an SDRAM? (Opening Statement, Tr. 66). Complaint Counsel also predicted that "some" witnesses would testify "that Mr. Crisp shook his head no" in response to this question, suggesting that Rambus had no intellectual property claims in the area. (Opening Statement, Tr. 66).

Response to Finding No. 493: RPF 493 lacks any reference to any admissible evidence in the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

494. The evidence at trial did not show that Mr. Crisp had stated or suggested at the May 1992 JC 42.3 meeting, by word or by movement, that Rambus did not have or would not seek intellectual property rights relating to a two-bank design or any other feature of an SDRAM.

Response to Finding No. 494: The statement in RPF 494 is misleading and incomplete because Gordon Kelley of IBM did in fact ask Mr. Crisp if he would like to comment

on whether Rambus had patents or potential patents covering 2 bank design. Mr. Crisp declined to comment. (CX0673 at 1 (Crisp e-mail: "Siemens expressed concern over potential Rambus Patents covering 2 bank designs. Gordon Kelly of IBM asked me if we would comment which I declined."); CCFF 904-905; CX2089 at 130-31, 136-37).

495. No witness who testified at trial about the May 1992 exchange between Mr. Kelley and Mr. Crisp testified that he or she had understood Mr. Crisp to be stating or suggesting that Rambus did not have or would not seek intellectual property rights with respect to a two-bank design or any other feature of an SDRAM.

Response to Finding No. 495: RPF 495 lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Additionally, the statement in RPF 495 [No witness who testified at trial about the May 1992 exchange between Mr. Kelley and Mr. Crisp testified that he or she had understood Mr. Crisp to be stating or suggesting that Rambus did not have or would not seek intellectual property rights with respect to a two-bank design or any other feature of an SDRAM] is misleading and incomplete because, as Mr. Crisp testified at trial, Howard Sussman stated at the same May 1992 meeting that he had seen the foreign Rambus patent application and that he believed would not be a concern for the JEDEC SDRAM standardization effort. Mr. Crisp further testified that he did not contradict what Mr. Sussman stated. (Crisp, Tr. 3067-68; CCFF 906; CX2092 at 128-130).

496. Instead, every witness who testified at trial about the May 1992 exchange between Mr. Kelley and Mr. Crisp testified that Mr. Crisp had *declined to comment* in response to the question asked of him.

Response to Finding No. 496: RPF 496 lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

497. The witnesses who testified about the May 1992 exchange between Mr. Kelley and Mr. Crisp were Mr. Kelley, Mr. Crisp, Siemens representative Willi Meyer, IBM representative Mark Kellogg and Intel representative Samuel Calvin. (Kelley, Tr. 2662; Crisp, Tr. 3066; Kellogg, Tr. 5055-6; Calvin, Tr. 1066-9; CX 2088, Meyer, Infineon Trial Tr. 4/26/01, 164:6-23, 136:3-5).

Response to Finding No. 497: RPF 497 cites, in part, the incorrect record evidence. Complaint Counsel assumes Respondent intended to cite to CX2089 and not to CX2088. Otherwise, Complaint Counsel does not disagree or have a specific response.

498. Mr. Calvin, the Intel representative, testified that he recalls that at a JEDEC meeting (whose date he could not remember), Mr. Crisp was asked if he cared to comment about whether Rambus had patents or intellectual property that covered a particular subject. (Calvin, Tr. 1068-9). Mr. Calvin recalls that Mr. Crisp declined to comment. (Calvin, Tr. 1068-70).

Response to Finding No. 498: The statement in RPF 498 [Mr. Crisp was asked if he cared to comment about whether Rambus had patents or intellectual property that covered a particular subject. ... Mr. Calvin recalls that Mr. Crisp declined to comment] is misleading and incomplete because, as Mr. Crisp testified at trial, Howard Sussman stated at the same May 1992 meeting that he had seen the foreign Rambus patent application and that he believed would not be a concern for the JEDEC SDRAM standardization effort. Mr. Crisp further testified that he did not contradict what Mr. Sussman stated. (Crisp, Tr. 3067-68; CCFF 906; CX2092 at 128-130).

499. Mr. Meyer, who was Siemens' primary JEDEC representative between 1992 and 1996, testified that at the May 1992 meeting, he asked Mr. Kelley to ask Mr. Crisp "whether [he] would like to comment" about whether Rambus had patents relating to the use of two banks in a

DRAM. (CX 2088, Meyer, Infineon Trial Tr. 4/26/01, 133:1-134:13; Meyer, Infineon Trial Tr. 5/7/01 87:12-19); CX 2057, 12/13/00 Infineon Meyer Depo. Tr., 66:7-11).

Response to Finding No. 499: RPF 499 cites, in part, the incorrect record evidence. Complaint Counsel assumes Respondent intended to cite to CX2089 and not to CX2088. The statement in RPF 499 [Mr. Meyer, who was Siemens' primary JEDEC representative between 1992 and 1996, testified that at the May 1992 meeting, he asked Mr. Kelley to ask Mr. Crisp "whether [he] would like to comment" about whether Rambus had patents relating to the use of two banks in a DRAM.] is incomplete because it ignores the fact that Mr. Meyer also testified that after Rambus disclosed the '703 patent, that he concluded Rambus "had nothing to report which related any more to the work of our committee ... and developing the synchronous DRAM" (CX2089, Meyer, Infineon Trial Tr., 149-150).

500. Mr. Meyer testified that "[t]he way how Mr. Kelley formulated the question was: Do you want to give a comment on this?" (CX 2088, Meyer, Infineon Trial Tr.4/26/01, 136:3-5, 164:21-23 ("Q. The question Mr. Kelley asked was did Rambus care to comment, right? A. Right.")). Mr. Meyer testified that Mr. Crisp "just shook his head." (*Id.*).

Response to Finding No. 500: RPF 500 cites the incorrect record evidence. Complaint Counsel assumes Respondent intended to cite to CX2089 and not to CX2088. Even with that in mind RPF 500 is incomplete because it ignores the fact that Mr. Meyer also testified that after Rambus disclosed the '703 patent, that he concluded Rambus "had nothing to report which related any more to the work of our committee ... and developing the synchronous DRAM" (CX2089, Meyer, Infineon Trial Tr., 149-150). Lastly, RPF 500 is incomplete because Mr. Meyer testified that when Chairman Gordon Kelley asked Mr. Crisp if he had any comment, "it was clear to all the participants..." that "the committee was trying to figure out whether Motorola or Rambus had anything to report to the committee..." (*Id.*, 135-37). To this question, Mr. Crisp "just shook his head" (*Id.*).

501. Mr. Meyer's trip report of the May 1992 meeting states in part that:

> "Siemens and Philips concerned about patent situation with regard to Rambus and Motorola. No comments given."

(RX 297 at 5).

Response to Finding No. 501: RPF 501 is incomplete because it omits Mr. Meyer's testimony where he clarifies that when Motorola's name was discussed at the May 1992 meeting, and Motorola did in fact give comments. When asked, the Motorola representative stated "yes, we can get you the patent numbers if we have one." (CX2089, Meyer, Infineon Trial Tr., 133). At the next meeting in July, Motorola identified the patent in question and submitted an assurance letter for the patent. (JX0013 at 136).

502. Mr. Crisp testified that Mr. Meyer had raised a concern during the May 1992 meeting about potential Rambus patents relating to the two bank design of the SDRAM. (Crisp, Tr. 2993-4; 3490-1). Mr. Crisp testified that Mr. Kelley then asked Mr. Crisp if he would comment, and that he declined to do so. (Crisp, Tr. 2994; 3490).

Response to Finding No. 502: RPF 502 is incomplete because, as Mr. Crisp testified at trial, Howard Sussman stated at the same May 1992 meeting that he had seen the foreign Rambus patent application and that he believed would not be a concern for the JEDEC SDRAM standardization effort. Mr. Crisp further testified that he did not contradict what Mr. Sussman stated. (Crisp, Tr. 3067-68; CCFF 906; CX2092 at 128-130).

503. Mr. Crisp sent an e-mail on May 6, 1992 that described his exchange with Mr. Kelley in this manner:

> "Siemens expressed concern over potential Rambus Patents covering designs. Gordon Kelley of IBM asked me if we would comment which I declined."

(CX 673 at 1).

Response to Finding No. 503: RPF 503 is incomplete because, as Mr. Crisp testified at trial, Howard Sussman stated at the same May 1992 meeting that he had seen the foreign Rambus patent application and that he believed would not be a concern for the JEDEC

SDRAM standardization effort. Mr. Crisp further testified that he did not contradict what Mr. Sussman stated. (Crisp, Tr. 3067-68; CCFF 906; CX2092 at 128-130).

504. Gordon Kelley testified that Siemens representative Willi Meyer had raised an "issue of concern with Rambus and Rambus patents" at the May 1992 meeting. (Kelley, Tr. 2662). Mr. Kelley recalls that Mr. Meyer had asked Mr. Crisp if he knew whether Rambus "had patentable material on the concept of the synchronous DRAM." (Kelley, Tr. 2543). Mr. Kelley recalls that Mr. Crisp declined to comment in response to that question. (Kelley, Tr. 2662).

Response to Finding No. 504: RPF 504 is incomplete because it fails to point out that Mr. Kelley was not sure if he said anything with respect to "any potential Rambus patent rights" at the May 1992 meeting. (G. Kelley, Tr. 2544).

505. Mr. Kelley testified that he could not recall whether he had said anything at the May 1992 JEDEC meeting about possible Rambus patent claims. (Kelley, Tr. 2544).

Response to Finding No. 505: RPF 505 is incomplete because, as Mr. Crisp testified at trial, Howard Sussman stated at the same May 1992 meeting that he had seen the foreign Rambus patent application and that he believed would not be a concern for the JEDEC SDRAM standardization effort. Mr. Crisp further testified that he did not contradict what Mr. Sussman stated. (Crisp, Tr. 3067-68; CCFF 906; CX2092 at 128-130).

506. Mr. Kelley also testified that a "no comment" from a JEDEC member in response to a question about intellectual property is "unusual" and "surprising" and "is notification to the committee that there should be a concern. . . ." (Kelley, Tr. 2579).

Response to Finding No. 506: RPF 506 is misleading and incomplete because Mr. Kelley's testimony relates not to the spontaneous question asked of Mr. Crisp at the May 1992 meeting mentioned here, but rather Rambus's deliberate, premeditated written response in September 1995 to a specific request to come to the meeting with an answer to a specific question. Moreover, the letter Rambus submitted did not concern SDRAM, but instead was an example of Rambus's failure to comply with JEDEC's disclosure requirements related to SyncLink. Mr.

Kelley testified at trial that, to his knowledge, JEDEC never standardized the SyncLink architecture. (Kelley, Tr. 2579).

507. IBM representative Mark Kellogg prepared contemporaneous handwritten notes at the May 1992 JEDEC meeting that refer to the concerns Mr. Meyer had raised. (RX 290 at 3). Mr. Kellogg's notes state:

> "Siemens: Kernel of chip similar to Rambus. Patent concerns? (No Rambus comments)."

(RX 290 at 3).

Response to Finding No. 507: RPF 507 is incomplete and misleading because it fails to acknowledge Mr. Kellogg's testimony at trial that, following this meeting, he did not have an understanding that Rambus had intellectual property applicable to SDRAMs. (Kellogg, Tr. 5056).

508. Mr. Kellogg testified that when he used the phrase "kernel of the chip" in his notes, he was referring to Mr. Meyer's concern that "the fundamental architecture of the SDRAM device" was "similar to Rambus." (Kellogg, Tr. 5324).

Response to Finding No. 508: RPF 508 is incomplete and misleading because it fails to acknowledge Mr. Kellogg's testimony at trial that, following this meeting, he did not have an understanding that Rambus had intellectual property applicable to SDRAMs. (Kellogg, Tr. 5056).

509. Mr. Kellogg testified that he took his notes at the May 1992 meeting in part to act as "a log of events" and "also to initiate action on my part or the part of others." He said that this discussion "would have been a flag, which is why I wrote it down." (Kellogg, Tr. 5322 (quoting deposition testimony, which Mr. Kellogg agreed was truthful)).

Response to Finding No. 509: RPF 509 is incomplete and misleading because it fails to acknowledge Mr. Kellogg's testimony at trial that, following this meeting, he did not have an understanding that Rambus had intellectual property applicable to SDRAMs. (Kellogg, Tr. 5056). Mr. Kellogg also testified at trial that "I use the term 'flag' a lot. I flag comments by all kinds of people in the meeting and I flag actions." (Kellogg, Tr. 5322).

510. Mr. Kellogg testified that he considered the discussion a "flag" because JEDEC members were "describing possible intellectual property concerns which may affect our decision process for synchronous DRAM." He testified that "[t]hat is a concern" and that "[t]he lack of response by Rambus is also a concern." (Kellogg, Tr. 5323 (quoting deposition testimony, which Mr. Kellogg agreed was truthful)).

Response to Finding No. 510: RPF 510 is incomplete and misleading because it fails to acknowledge Mr. Kellogg's testimony at trial that, following this meeting, he did not have an understanding that Rambus had intellectual property applicable to SDRAMs. (Kellogg, Tr. 5056). Mr. Kellogg also testified at trial that "I use the term 'flag' a lot. I flag comments by all kinds of people in the meeting and I flag actions." (Kellogg, Tr. 5322).

511. In sum, the evidence shows that: (1) Mr. Crisp was asked at the May 1992 JC 42.3 meeting if he would care to comment about whether Rambus had intellectual property with respect to the SDRAM device; (2) Mr. Crisp declined to comment; and (3) JEDEC leaders and members were aware that Mr. Crisp had declined to comment.

Response to Finding No. 511: RPF 511 lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

512. Three conclusions are evident from the May 1992 JEDEC meeting and the events leading up to it.

Response to Finding No. 512: RPF 512 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

513. First, it is clear that the chairman of the JC 42.3 committee was aware in April and May 1992 that Rambus might have intellectual property claims relating to one or more technologies being considered for JEDEC standardization.

Response to Finding No. 513: RPF 513 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits

that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Moreover, the statement in RPF 513 is contrary to the weight of evidence because numerous witnesses testified at trial that they did not have the understanding that Rambus had intellectual property claims relating to one or more technologies being considered for JEDEC standardization. (Kellogg, Tr. 5056; G. Kelley, Tr. 2562; CCFF 1260-61; CX2089 at 151-52 (Meyer, Infineon Trial Tr.)). Rambus witnesses have testified that they did not notify any SDRAM manufacturers until late 1999 or 2000 that Rambus had claims covering features of SDRAMs. (CX2079 at 157-58; *see also* CX2098 at 442-43 (Mooring, Dep.); Hampel, Tr. 8732-33).

514. Second, it is clear that Rambus did nothing and said nothing at the May 1992 JEDEC meeting to suggest that Rambus did not have or would not obtain intellectual property claims relating to the SDRAM device.

Response to Finding No. 514: RPF 514 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

515. Third, it is apparent that Rambus's refusal to comment about its intellectual property at the May 1992 meeting occurred in the presence of, and was a concern to, JEDEC leaders and members.

Response to Finding No. 515: RPF 515 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

516. There was an additional discussion of Rambus's potential intellectual property claims at the May 1992 JEDEC meeting. After the exchange between Mr. Kelley and Mr. Crisp, NEC representative Howard Sussman stated that he had reviewed Rambus's "PCT" patent application. (RX 290 at 3; CX 673 at 1).

Response to Finding No. 516: RPF 516 is incomplete because, as Mr. Crisp testified at trial, Howard Sussman stated at the same May 1992 meeting that he had seen the foreign Rambus patent application and that he believed would not be a concern for the JEDEC SDRAM standardization effort. Mr. Crisp further testified that he did not contradict what Mr. Sussman stated. (Crisp, Tr. 3067-68; CCFF 906; CX2092 at 128-130).

517. A "PCT" application is an international patent application filed pursuant to the Patent Cooperation Treaty. (CX 1454 at 1). Rambus had filed a PCT application on April 16, 1991 that was identical in all material respects to the '898 application it had filed at the same time in the U.S. (CX 1451; CX 1454; Fliesler, Tr. 8811).

Response to Finding No. 517: Complaint Counsel does not disagree or have a specific response.

518. Pursuant to the procedures governing applications filed under the Patent Cooperation Treaty, Rambus's PCT application became publicly available as of October 31, 1991. (CX 1454 at 1; First Set of Stipulations, April 24, 2003, p. 2, item 8).

Response to Finding No. 518: Complaint Counsel does not disagree or have a specific response.

519. At the May 1992 JEDEC meeting, NEC representative Howard Sussman stated that he had reviewed Rambus's PCT application, that it contained 150 claims, and that many of the claims were, in Mr. Sussman's opinion, barred by prior art. (RX 290 at 3; CX 673 at 1).

Response to Finding No. 519: RPF 519 is incomplete and misleading because it fails to acknowledge Mr. Sussman's own testimony at trial, where he testified that he did not find anything in the PCT application that "related to the work ongoing at JEDEC." (Sussman, Tr. 1445). Moreover, Respondent cites to Mr. Kellogg's notes (RX 290), but fails to include Mr. Kellogg's testimony at trial that he did not have the understanding following this meeting in May 1992 that Rambus had intellectual property claims relating to one or more technologies being considered for JEDEC standardization. (Kellogg, Tr. 5056). At no point during its cross-

examination of Mr. Sussman, did Respondent choose to ask Mr. Sussman himself if he made these remarks at the May 1992 meeting. (Sussman, Tr. 1462-73).

520. Mr. Crisp's May 6, 1992 e-mail states that:

> In response to the patent issue, Sussman stated that our patent application is available from foreign patent offices, that he has a copy, and noted many, many claims that we make that are anticipated by prior art. He also stated the Motorola patent predated ours (not the filing date!) and it too was anticipated by prior art."

(CX 673 at 1).

Response to Finding No. 520: RPF 520 is incomplete because it fails to acknowledge Mr. Sussman's own testimony at trial, where he testified that he did not find anything in the PCT application that "related to the work ongoing at JEDEC." (Sussman, Tr. 1445). Moreover, at no point during its cross-examination of Mr. Sussman, did Respondent choose to ask Mr. Sussman himself if he made these remarks at the May 1992 meeting. (Sussman, Tr. 1462-73).

521. The handwritten notes taken contemporaneously at the May 1992 meeting by IBM representative Mark Kellogg similarly state that:

> "NEC: Rambus International Patent 150 pages, Motorola patents/Rambus patents – suspect claims won't hold."

(RX 290 at 3).

Response to Finding No. 521: RTF 521 is incomplete because Respondent cites to Mr. Kellogg's notes (RX 290), but fails to include Mr. Kellogg's own testimony at trial that he did not have the understanding following this meeting in May 1992 that Rambus had intellectual property claims relating to one or more technologies being considered for JEDEC standardization. (Kellogg, Tr. 5056)

522. Roughly one week after the May 1992 meeting, Siemens' JEDEC representative Willi Meyer also reported that: "Siemens and Philips concerned about patent situation with

regard to Rambus and Motorola. No comments given. Motorola patents have priority over Rambus'. Rambus patents filed but pending." (RX 297 at 5).

Response to Finding No. 522: RTF 522 is incomplete because it ignores the fact that Mr. Meyer also testified that after Rambus disclosed the '703 patent, that he concluded Rambus "had nothing to report which related any more to the work of our committee ... and developing the synchronous DRAM" (CX2089, Meyer, Infineon Trial Tr., 149-150).

523. In June 1992, Gordon Kelley gave a presentation about Rambus to a group of about 30 engineers. Half of the engineers were from IBM; half were from Siemens. (Kelley, Tr. 2658-9).

Response to Finding No. 523: Complaint Counsel has no specific response.

524. Any question about whether JC 42.3 Chairman Kelley had been misled or "lulled" by Mr. Crisp's refusal to comment at the May 1992 meeting is resolved by Mr. Kelley's testimony about his June 1992 presentation. (Kelley, Tr. 2545; 2658-9).

Response to Finding No. 524: The statement in RPF 524 [Any question about whether JC 42.3 Chairman Kelley had been misled or "lulled" by Mr. Crisp's refusal to comment at the May 1992 meeting is resolved by Mr. Kelley's testimony about his June 1992 presentation.] is incomplete and misleading. Contrary to the assertion in RPF 524, Mr Kelley testified that at the time of the June presentation he personally did not believe that Rambus had patents covering SDRAMs. (G. Kelley, Tr. 2545-2546).

525. In connection with his June 1992 presentation, Mr. Kelley prepared a chart entitled "COMPARE ALTERNATIVES for Future High Performance, High Volume DRAM Designs." The chart listed "Pros" and "Cons" of Sync DRAMs and Rambus DRAMs. One of the two "cons" listed for Sync DRAMs was "Patent Problems? (Motorola/Rambus)." (RX 303 at 1; Kelley, Tr. 2544).

Response to Finding No. 525: The statement in RPF 525 [The chart listed "Pros" and "Cons" of Sync DRAMs and Rambus DRAMs] is incomplete and misleading. The chart also included pros and cons of Cached DRAMs. (RX 303 at 1).

526. Mr. Kelley testified that he included the reference to possible "patent problems" involving Motorola and Rambus in his June 1992 "Pros" and "Cons" chart because he "was

notifying the people involved in the design of the joint work that was going on between IBM and Siemens that there was concern about potential patent problems as I had heard at the JEDEC meeting about Motorola and Rambus intellectual property, and I wanted the group to recognize that there was this concern." (Kelley, Tr. 2545).

Response to Finding No. 526: The statement in RPF 526 is incomplete and misleading. Mr. Kelley testified that at the time of the June presentation he personally did not believe that Rambus had patents covering SDRAMs. (G. Kelley, Tr. 2545-2546).

527. Mr. Meyer testified that in September 1992, he had prepared a presentation entitled "What Is Rambus?" (RX 321 at 1; CX 2088, Meyer Infineon Trial Tr. 4/26/01, 66-67). Meyer delivered this presentation to, among others, Dr. Schumacher, the current CEO of Infineon. (*Id.*).

Response to Finding No. 527: Complaint Counsel has no specific response.

528. In his September 1992 presentation, Mr. Meyer referred to Rambus as a "deadly menace to the established computer industry." (RX 321 at 2). He also suggested that to "protect" the computer industry, someone could "buy Rambus and dump it." (RX 321 at 3). Mr. Meyer testified that he thought that some of his competitors were so worried about Rambus that they might purchase the entire company and "bury the technology." (CX 2088, Meyer Infineon Trial Tr. 4/26/01, 89-90).

Response to Finding No. 528: The statement in RPF 528 [In his September 1992 presentation, Mr. Meyer referred to Rambus as a "deadly menace to the established computer industry."] is incomplete. Mr. Meyer testified that he did not view Rambus as a deadly menace but was exaggerating for the purposes of the presentation. He further testified that he was discussing concern of engineers in the computer industry but not of DRAM manufacturers such as Infineon that are suppliers of the computer industry. (CX2088, Meyer Trial Tr. 4/26/01, 79-85). The statements in RPF 528 [He also suggested that to "protect" the computer industry, someone could "buy Rambus and dump it." (RX 321 at 3). Mr. Meyer testified that he thought that some of his competitors were so worried about Rambus that they might purchase the entire company and "bury the technology."] are also incomplete and misleading. Mr. Meyer testified that buying Rambus was not an option for Infineon. Further Mr. Meyer never states in the cited pages that it was his competitors that were so worried about Rambus that they may purchase the company.

Rather, the context suggests that he was talking about purchasers of DRAMs rather than DRAM manufacturers who may consider this course of action. (CX2088, Meyer Trial Tr. 4/26/01, 89-91, 79-85)

529. Mr. Kelley testified, in a 2001 deposition, that he had had conversations with Mr. Meyer *after* 1992 that related to the potential applicability of Rambus patents to SDRAM devices. He could not recall the substance of these conversations. (Kelley, Tr. 2664-5).

Response to Finding No. 529: Complaint Counsel has no specific response.

2. Rambus Did Not Mislead JEDEC Members Or Leaders After The May 1992 Meeting With Respect To Its Intellectual Property. The Evidence Shows Instead That JEDEC Members Believed That If Rambus Did Obtain Patents Relating To SDRAMs, The Patents Would Be Invalid Because Of Prior Art.

530. There was an additional discussion of Rambus's PCT application at a JEDEC meeting in September 1993, after Rambus representative Richard Crisp disclosed that Rambus had obtained its first U.S. patent (the '703 patent). According to Siemens' JEDEC representative Willi Meyer:

> "During the meeting, which was the same meeting in which the Rambus '703 patent was disclosed with its full patent number, and a participant, I'm not quite sure, either the participant or the chairman or the JEDEC official, somebody at the meeting said by the way, there is also something called like a WIPO, World Intellectual Property, and he offered to anybody who was interested in it to get the number from him, the reference number, and to step up to him after the meeting to do so."

(CX 2057, Meyer, 12/13/00 Infineon Depo. Tr., 298:10-20).

Response to Finding No. 530: Complaint Counsel has no specific response.

531. A PCT application is sometimes referred to as a "WIPO" application because it is filed with the World Intellectual Property Organization. (CX 1454 at 1; Vincent, Tr. 7883).

Response to Finding No. 531: Complaint Counsel does not disagree.

532. Mr. Meyer testified that this statement about the "WIPO" application was made "during the official meeting session," and he testified that whoever had brought up the application described it as "a collection of prior art:"

> "He said everything else regarding the Rambus intellectual property is stuck in the patent office and is not proceeding right now. Other comments from this person were it's basically because they are checking for prior art and that it seems to be that what Rambus has submitted is mainly a collection of prior art, this is what I recall very specifically, and then he brought up this WIPO, saying maybe this is because everything else is stuck, this is a way around that, and Rambus has chosen to document all that which they could not get through the U.S. Patent Office through this World Intellectual Property Organization, whatever it is. And then came the mentioning, I have the number and reference number of that WIPO and if you want to step up after the meeting, you can get it from me, the number."

(CX 2057, Meyer 12/13/00 Infineon Depo. Tr., 300:7-23).

Response to Finding No. 532: The cite in the proposed finding to CX2057 is erroneous. The cite should be CX2058. The statement in the proposed finding [Mr. Meyer testified that this statement about the "WIPO" application was made "during the official meeting session," and he testified that whoever had brought up the application described it as "a collection of prior art:"] is inaccurate. Mr. Meyer did not describe the WIPO application as "a collection of prior art" Rather he stated in the cited testimony that the person speaking at the meeting conjectured that Rambus may be using the WIPO to get around the US PTO. (CX 2058, Meyer 12/13/00 Infineon Depo. Tr., 300:7-23). Further the statement is incomplete. Meyer testified that he read the WIPO application and concluded that it described an RDRAM and had nothing to do with the work on SDRAMs being undertaken at JEDEC. (CX2089, Meyer Infineon Trial Tr. 4/26/01, 147-148).

533. Mr. Meyer also testified that he obtained the serial number for Rambus's "WIPO" application at the JEDEC meeting and "sent it back to the [Siemens] patent department." (CX 2088, Meyer Infineon Trial Tr., 4/26/01, 112:13-24).

Response to Finding No. 533: RPF 533 is incomplete. Mr. Meyer testified that the patent department sent him a copy of the WIPO and that he read it and concluded that it

described an RDRAM and had nothing to do with the work on SDRAMs being undertaken at JEDEC. (CX2089, Meyer Infineon Trial Tr. 4/26/01, 112-113, 147-148).

534. A few months later, in March 1994, Mr. Meyer prepared a memorandum about Rambus to a Siemens engineering manager named Penzel. The memorandum stated in part that "[a]ll computers will (have to be) built like this some day, but hopefully without royalties to Rambus." (RX 488A at 1; CX 2088, Meyer Infineon Trial Tr., 4/26/01, 124).

Response to Finding No. 534: The statement in RPF 534 [The memorandum stated in part that "[a]ll computers will (have to be) built like this some day, but hopefully without royalties to Rambus." (RX 488A at 1; CX 2088, Meyer Infineon Trial Tr., 4/26/01, 124).] is incomplete and misleading. First, the cited statement in RX 488A is given in the context of discussing video RAMs. Second, the cited sentence read in conjunction with the immediately preceding sentence ["RAMBUS is not a memory, but rather a memory system that includes, controller, bus, interface protocol and memory. All computers will (have to be) built like this some day, but hopefully without royalties to Rambus."] indicates that Mr. Meyer did not mean that all computers would have to be built using RDRAMs but that they will have to be built using memory systems and not just memory.

535. As noted in findings 659-706, below, and as demonstrated by the Mitsubishi documents and other evidence cited in support of those findings, a patent lawyer or person of ordinary engineering skill would understand from reviewing the PCT application that Rambus might seek broad patent claims covering the use in memory devices of programmable CAS latency, programmable burst length, dual-edge clocking and on-chip DLL.

Response to Finding No. 535: RPF 535 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

536. Rambus was also asked at a May 1995 JEDEC meeting to respond to questions about its intellectual property. At the May 24, 1995 JEDEC meeting, presentations were made by several JEDEC members regarding a "next generation" memory technology called "SyncLink." (JX 26 at 10-11). Rambus representative Richard Crisp was asked at the meeting to "get a

statement from his company on the issue of whether they held patents on the concepts of the SyncLink DRAM. . . ." (Kelley, Tr. 2578). Mr. Crisp provided a statement at the next JEDEC meeting. *See* Findings ¶¶ 544-548.

Response to Finding No. 536: The proposed finding is incomplete and does not support Respondent's contention that Rambus did not mislead JEDEC members or leaders after the May 1992 meeting with respect to its intellectual property. At the May 1995 meeting there were a number of inquiries about possible patent issues pertaining to Synclink. Gordon Kelley of IBM asked whether or not HP, Hyundai, Mitsubishi or TI had any patents covering any of the matters being presented; all of these companies stated that they did not. (CX0711 at 72; Crisp, Tr. 3264-3265) Sam Calvin of Intel and Mr. Kelley also inquired whether there were any Rambus patents covering the Synclink technology. (CX0711 at 73; Crisp, Tr. 3264-3265) It was only when Mr. Crisp did not respond to this inquiry at the meeting that he was asked by Mr. Kelley to go back to Rambus and then report back to the Committee whether Rambus knew of any patents, especially Rambus patents, that may read on the Synclink technology. (CX0711 at 73; CX0794 at 4; Crisp, Tr. 3267-3268)

Crisp immediately wrote an e-mail informing the Rambus executives, engineering managers and business development and marketing groups of this development. In that e-mail he listed a few ideas he had of Rambus intellectual property relating to Synclink (CX0711 at 68, 73) He also suggested that Rambus review its current issued patents and see what it had to work against Synclink (CX0711, 68, 73) He recommended that Rambus consider responding to the JEDEC request by "simply provid[ing] a list of patent numbers which have issued" and telling members to decide for themselves what does and does not infringe. He added, however, that if the Rambus patents were "not a really key issue . . . then it makes no sense to alert them to a potential problem they can easily work around," and that "we may not want to make it easy for all to figure our what we have especially if nothing looks really strong." (CX0711, 68, 73) Rambus

executives heeded Mr. Crisp's advice and Mr. Crisp testified at trial that at the September meeting, he made "no statement to the 42.3 subcommittee that [he] believed that SyncLink would violate Rambus patents." (Crisp, Tr. 3316). The letter that he presented at the meeting contains nothing to inform the Committee that Rambus had pending patents relating to specific SDRAM technologies. (CCFF 1063).

The finding also does not support Respondent's contention that JEDEC members believed that if Rambus did obtain patents relating to SDRAMs, the patents would be invalid because of prior art. Synclink was a "totally different architecture" compared to EDO, page mode and synchronous DRAMs (i.e. SDRAM and DDR). (Sussman, Tr. 1404-5). Like RDRAM and unlike SDRAMs, Synclink was a packetized device. (Sussman, Tr. 1404-1405; Kelley, Tr. 2573-2574) As stated in the reply to Respondent's Findings 550-551, no-one outside Rambus knew that Rambus believed it had intellectual property relating to SDRAMs and DDR SDRAMs. This was not surprising because they viewed the technologies as being very different. Gordon Kelley testified on attending a presentation by Rambus at IBM that he believed that Rambus RDRAM was fundamentally different from the SDRAM technology under discussion at JEDEC and that no intellectual property rights that Rambus had on RDRAM could be applicable to SDRAM or JEDEC. (G. Kelley, Tr. 2537-38, 2546).

The finding also does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

537. A few days after the May 1995 meeting, Mr. Crisp sent an e-mail to Reese Brown, a JEDEC consultant, that included a reference to "Ramlink," the foundation for the proposed

SyncLink device. (CX 711 at 80-81; Gustavson, Tr. 9281-3). Mr. Crisp's e-mail stated in part that Ramlink "has numerous patent issues associated with it." (CX 711 at 80-81).

Response to Finding No. 537: RPF 537 is incomplete and misleading. Richard Crisp sent an e-mail to Reese Brown in which he took exception to the fact that Mr. Brown had posted a copy of the ballot for the proposed IEEE Ramlink standard on the JEDEC reflector. (CX0711 at 76-77; Crisp, Tr. 3280-82). It was only when Mr. Brown responded to Mr. Crisp and kiddingly suggested that Mr. Crisp's exception was partly due to the fact that he saw the standard as competition to Rambus that Mr. Crisp responded that the proposed IEEE standard was not real and had patent issues associated with it. (CX0711 at 79-80; Crisp, Tr. 3282-83). Mr. Crisp admitted that he had not planned ahead of time to disclose this but did it in the heat of the moment. (Crisp, Tr. 3282-3283) It is clear that Mr. Crisp wanted to keep this information from getting to persons beyond Mr. Brown because he complained to Mr. Brown when he learned that Mr. Brown had forwarded Mr. Crisp's comments to Hans Wiggers. (CX0711 at 102) The finding also does not support Respondent's contention that JEDEC members believed that Rambus patents might relate to SDRAMs for the reasons outlined in CCRF 536.

538. Mr. Brown forwarded Mr. Crisp's e-mail to Hans Wiggers, the JEDEC representative for Hewlett-Packard, who was chairing the Ramlink/SyncLink working group. (CX 711 at 88-91; Gustavson, Tr. 9282-3).

Response to Finding No. 538: RPF 538 is incomplete because it fails to acknowledge that Mr. Crisp objected to the fact that Mr. Brown had forwarded Crisp's comments to Mr. Wiggers. (CX0711 at 102 and 103) The finding also does not support Respondent's contention that JEDEC members believed that Rambus patents might relate to SDRAMs for the reasons outlined in CCRF 536. The finding also does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled

an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

539. On June 10, 1995, Mr. Wiggers forwarded Mr. Crisp's comments to, among others, Gordon Kelley, the Chairman of the JC 42.3 subcommittee, along with a request that Mr. Crisp clarify his comments about patents relating to Ramlink. (CX 711 at 90-1). On June 12, 1995, Mr. Kelley prepared an internal IBM memorandum that stated with respect to the SyncLink device that "the Rambus patents should be closely reviewed." (RX 575 at 7).

Response to Finding No. 539: RPF 539 is incomplete and misleading. Mr. Wiggers did not forward Mr. Crisp's comments to Gordon Kelley and others. Rather, Mr. Wiggers cc'd his response to Mr. Crisp to Mr. Kelley and others. The response contained Mr. Crisp's comments. (CX0711 at 90-91). Mr. Wiggers stated in that response that as Chairman of the Ramlink working group he took Mr. Crisp's comment about patents "very seriously." (CX0711 at 90-91; Wiggers, Tr. 10595) Mr. Wiggers stated in his response that he assumed Mr. Crisp had attended the IEEE working group meetings in "good faith" and if Mr. Crisp knew of any way in which the proposed Ramlink standard violated patents held by Rambus or others, he thought Mr. Crisp had a "moral obligation" to bring to his attention information about which patents were being violated. (CX0711 at 90-91; Crisp, Tr. 3284-86). Mr. Crisp made it clear to Mr. Wiggers that he did not appreciate Mr. Brown forwarding his comments to Mr. Wiggers and Mr. Wiggers in turn making them known to others. (CX0711 at 103)

The finding also does not support Respondent's contention that JEDEC members believed that Rambus might obtain patents relating to SDRAMs for the reasons outlined in CCRF 536. The finding also does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

540. On June 13, 1995, Mr. Crisp sent an e-mail to Mr. Wiggers that stated:

> "[R]egarding patents, I have stated to several persons that my personal opinion is that the Ramlink/SyncLink proposals will have a number of problems with Rambus intellectual property. We were the first out there with high bandwidth, low pincount, DRAMs, our founders were busily at work on their original concept before the first Ramlink meeting was held, and their work was documented, dated and filed properly with the US patent office. *Much of what was filed has not yet issued, and I cannot comment on specifics as these filings are confidential.*"

(RX 576 at 2) (emphasis added).

Response to Finding No. 540: The proposed finding is incomplete in that Mr. Crisp once again sought to prevent information regarding Rambus patents from being circulated. He stated in his e-mail that he claimed and withheld all copyrights for the material in his e-mail and asked Mr. Wiggers to respect this request not to copy and distribute his e-mail to others. (RX0576 at 4)

The finding also does not support Respondent's contention that JEDEC members believed that Rambus might obtain patents relating to SDRAMs for the reasons outlined in CCRF 536. The finding also does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

541. Mr. Crisp's e-mail to Mr. Wiggers also stated that:

> "I was asked at the last JEDEC 42.3 meeting to report on our patent coverage relative to SyncLink as proposed at JEDEC 42.3 at the next meeting in Crystal City in September. Our attorneys are currently working on this, so I think I will be in a position to make some sort of official statement at that time and plan to do so. In the meantime, I have nothing else to say to you or the rest of the committee about our patent position. If you want to search for issued patents held by Rambus, then you may learn something about what we clearly have covered and what we do not. *But I must caution you that there is a lot of material that is currently pending and we will not make any comment at all about it until it issues.*"

(RX 576 at 2) (emphasis added).

Response to Finding No. 541: The proposed finding is incomplete and misleading in that it once again fails to acknowledge that Mr. Crisp sought to prevent the information contained in the finding from being circulated to others. (*See* CCRF 540)

The finding also does not support Respondent's contention that JEDEC members believed that Rambus might obtain patents relating to SDRAMs for the reasons outlined in CCRF 536. The finding also does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

542. In August 1995, Rambus warned the SyncLink working group that its work might infringe Rambus's intellectual property. The minutes of the August 21, 1995, meeting of the SyncLink working group state in part as follows:

> "Richard Crisp, of RamBus, informed us that in their opinion both RamLink and SyncLink may violate RamBus patents that date back as far as 1989. Others commented that the RamLink work was public early enough to avoid problems, and thus might invalidate such patents to the same extent that they appear to be violated. However, the resolution of these questions is not a feasible task for this committee, so it must continue with the technical work at hand."

(RX 592 at 2).

Response to Finding No. 542: The proposed finding is incomplete. It fails to note the efforts by Mr. Crisp to prevent the working group from finding out that Rambus had patents that it thought Synclink may infringe. (CCRF 537-541). Further, as Gordon Kelley noted, by not making the same type of disclosure at the May and September JEDEC committee meetings but rather making no comment, Mr. Crisp was lying and acting in bad faith. (Kelley, Tr. 2742-2745; *See* CCRF 544)

The finding also does not support Respondent's contention that JEDEC members believed that Rambus might obtain patents relating to SDRAMs for the reasons outlined in CCRF 536. The finding also does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

543. Although the August 22, 1995 SyncLink meeting was held under the auspices of a standards-setting body called the IEEE, not JEDEC, each of the seven companies represented at the SyncLink meeting was also a JEDEC member company, and at least five of the engineers present at the SyncLink meeting were JEDEC representatives who attended the next JEDEC 42.3 meeting on September 11, 1995. (First Set of Stipulations, April 24, 2003, p. 3, item 21).

Response to Finding No. 543: The proposed finding is incomplete and misleading. The relevant question is not how many persons present at the August Synclink meeting were also at the September JC-42.3 meeting but rather how many JEDEC members were not at the Synclink meeting. The minutes of the September 1995 JC-42.3 meeting lists approximately 42 companies as being represented at the meeting and another 21 as being absent (JX-0021 at 1-3). Consequently there were at least 37 member companies represented at the September JC-42.3 meeting, and another 21 who were absent but would have received minutes of the meeting, who were not at the Synclink meeting to hear Mr. Crisp's disclosure at that meeting. Further, the proposed finding is misleading because the IEEE membership is made up of individuals and not companies. (CCFF 1502) Therefore, none of the JEDEC member companies were in fact represented at the Synclink meeting because under the bylaws of the IEEE working groups, attendees represent themselves only, not their employers. (CCFF 1503)

Furthermore, even with respect to the five individuals present at both the Synclink meeting and the JEDEC meeting, the finding does not support Respondent's contention that these members believed that Rambus might obtain patents relating to SDRAMs for the reasons outlined

in CCRF 536. The finding also does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

544. At the September 1995 JEDEC meeting, Mr. Crisp presented a written response to the questions about intellectual property that had been raised at the May 1995 meeting. The statement included this passage:

> "At this time, Rambus elects to not make a specific comment on our intellectual property position relative to the Synclink proposal. *Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property*."

(JX 27 at 26) (emphasis added). Rambus's statement was published in full in the official JEDEC minutes of the September 1995 meeting. (JX 27 at 26).

Response to Finding No. 544: The proposed finding is incomplete. Gordon Kelley testified that the Rambus statement was not an adequate response to the question that he had given Crisp at the May meeting. (Kelley, Tr.2578-2579) He stated that in the past, members affirmatively stated either that they did or did not have relevant intellectual property. (Kelley, Tr. 2579). Mr. Kelley further testified that he believed that by not notifying the committee that Rambus had applicable intellectual property to the Synclink proposal as he had acknowledged to the Synclink committee, Richard Crisp was in fact lying to JEDEC and acting in bad faith. (G. Kelley, Tr. 2742- 2745 ("I experienced Richard Crisp being asked directly at an earlier meeting than the September '95 meeting if he was aware that Rambus owned intellectual property on the ideas that or the material that JEDEC had seen on SyncLink at the September -- or at the earlier meeting, and then at the September '95 meeting he came and basically said, No comment, and then I learned that right after this he attended a SyncLink meeting and in fact told the SyncLink

membership that they in fact had intellectual property that they thought applied to the presentations, and to me that was -- that was not the kind of treatment, fair treatment, that I expected under the requirements of good faith and open standards . . . If [Mr. Crisp] told the JEDEC committee in September of 1995 that he had no comment on any intellectual property that Rambus held pertaining to the SyncLink proposals that had been disclosed at the prior meeting and then later told members of SyncLink that that in fact was not true, that he was aware of intellectual property that applied to SyncLink proposals, then I believe, yes, that he lied to the JEDEC committee by saying, No comment.")

The finding also does not support Respondent's contention that JEDEC members believed that Rambus might obtain patents relating to SDRAMs, for the reasons outlined in CCRF 536. The finding also does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

545. JC 42.3 chair Gordon Kelley testified that Rambus's "comment of no comment" was "unusual on the committee and is surprising. . . ." Kelley, Tr. 2579.

Response to Finding No. 545: The proposal is incomplete. Mr. Kelley also testified that the statement was not an adequate response and that by making no comment, Mr. Crisp was lying and acting in bad faith. (G. Kelley, Tr. 2742-2745; *See* CCRF 544)

The finding also does not support Respondent's contention that JEDEC members believed that Rambus might obtain patents relating to SDRAMs for the reasons outlined in CCRF 536.

546. Kelley explained that "[a] comment of no comment is notification to the committee that there should be a concern" about intellectual property issues. Kelley, Tr. 2579.

Response to Finding No. 546: The proposed finding is incomplete. Mr. Kelley also testified that the statement was not an adequate response and that by making no comment, Mr. Crisp was lying and acting in bad faith. (Kelley, Tr. 2742-2745; *See* CCRF 544)

The finding also does not support Respondent's contention that JEDEC members believed that Rambus might obtain patents relating to SDRAMs for the reasons outlined in CCRF 536.

This proposed finding does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

547. A September 1995 meeting report prepared by Motorola JEDEC representative Mark Farley noted that Mr. Crisp had:

> "[m]ade a non-statement statement to the committee saying that Rambus has been developing this technology for five+ years and has a substantial number of patents relating to high bandwidth DRAMs." (RX 615 at 1).

Mr. Farley also reported that "SyncLink told Motorola confidentially that there were very likely patents violated by their proposal." (RX 615 at 1).

Response to Finding No. 547: The proposed finding is unreliable. No witness ever testified about the document cited in the finding. It is therefore unclear what is meant by "high bandwidth DRAMs." There is no indication that it had any relationship to SDRAMs. It is also unclear who at Synclink discussed the likelihood of patent coverage or when and where the discussion took place.

The finding also does not support Respondent's contention that JEDEC members believed that Rambus might obtain patents relating to SDRAMs for the reasons outlined in CCRF 536.

This proposed finding does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

548. Intel representative Samuel Calvin testified that he understood from Rambus's September 11, 1995 statement that any silence by Rambus at JEDEC meetings should not be taken as an indication that it did not have intellectual property relating to JEDEC's work. (Calvin, Tr. 1070).

Response to Finding No. 548: The proposed finding is incomplete, misleading and unreliable. Mr. Calvin's recollection was hazy and he testified that he did not know at which meeting the statement was given, only that it was in the "'95 time frame". (Calvin, Tr. 1070) The proposed finding is misleading to the extent it implies that Mr. Calvin's testimony related to anything other than Synclink.

The finding also does not support Respondent's contention that JEDEC members believed that Rambus might obtain patents relating to SDRAMs for the reasons outlined in CCRF 536. The finding also does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

549. In this same time period – the fall of 1995 – Rambus CEO Geoff Tate and Rambus Vice President Allen Roberts held a series of meetings with DRAM manufacturers in Asia in an effort to convince the manufacturers to become Rambus licensees. As set out below, Mr. Tate's notes of those meetings reflect that he told DRAM manufacturers LG Semicon, Samsung, NEC, and Oki that Rambus expected to have intellectual property that would read on the SyncLink architecture and on devices manufactured in compliance with the SDRAM standard.

Response to Finding No. 549: RPF 549 lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be

disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

This proposed finding does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

Further, as set out in the following Reply Findings the great weight of the evidence shows that Mr. Tate did not in fact inform manufacturers that Rambus expected to have intellectual property that would read on devices manufactured in compliance with the SDRAM standard. Finally, even if Mr. Tate had informed manufacturers that Rambus expected to have intellectual property that would read on the Synclink architecture, such evidence is irrelevant to the current litigation which is concerned with JEDEC compliant SDRAMs and DDR SDRAMs.

550. During a meeting in Korea in October 1995, Rambus informed LG Semiconductor that Rambus had or might obtain intellectual property rights that might apply to SDRAMs. (CX 2111, Tate Depo. at 314-15; CX 1729 at 96)

Response to Finding No. 550: This proposed finding does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to ownership of the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

The cited testimony was given by Mr. Tate in response to a question that Complaint Counsel objected to as calling for speculation, vague and ambiguous, lacking foundation and leading. Complaint Counsel, therefore, argues that this finding therefore should be disregarded.

The proposed finding is, in any case, incomplete and misleading. The proposed finding cites as support notes of Geoff Tate and his testimony about those notes. However, Mr. Tate testified that the notes reflected "the topics that I intended and wanted to ensure that we would discuss during the meeting." (CX2111 at 316 (Tate Dep.)) and not what was actually discussed. Further, although the proposed finding refers to SDRAMs, Mr.Tate testified that although he wrote SDRAMs in his notes he believes he was probably actually referring to future DRAMs or in other words DRAMs including PLLs [ie. DDR SDRAMs]. (CX2111 at 317 (Tate, Dep.)).

Even if the reference were truly to SDRAMs, the general premise that Mr. Tate was informing others that Rambus might have intellectual property relating to SDRAMs is contradicted by other more credible testimony from Mr. Tate and others as well as contemporaneous documents to the contrary. Gary Harmon, former Rambus Chief Financial Officer recalled being involved in discussions with numerous DRAM manufacturers, including LG Semicon (CX2070 at 42-43 (Harmon Dep.)). He did not recall any discussions on the scope or extent of Rambus patents during these negotiations. (CX2070 at 45-46 (Harmon, Micron Dep.)). Specifically, Mr. Harmon testified that: "I don't believe we ever specifically stated that we had intellectual property that applied to – outside of the Rambus-compatible area." (CX2070 at 47 (Harmon Dep.)). Craig Hampel, Rambus technical director who since 1993 participated in numerous meetings and presentations with DRAM manufacturers and other firms to discuss Rambus technology (Hampel, Tr. 8672, 8729-31) testified that he was not aware of any instance in which Rambus representatives told the DRAM manufacturers which aspects of RDRAM were Rambus inventions, or were protected by Rambus patents or patent applications. (Hampel, Tr. 8732-8733). Rambus President, David Mooring, testified that the first time Rambus ever advised any SDRAM manufacturer that Rambus had claims covering features of SDRAMs was Hitachi in late 1999 or early 2000. (CX2098 at 442-43 (Mooring Dep.); *see also* CX2112 at 171-72

(Mooring, FTC Dep.) Mr. Tate, himself, testified during the Infineon trial in Richmond, Virginia that Rambus did not tell Infineon that it had patents that covered SDRAMs or DDR SDRAMs until about June 2000. (CX2088 at 75-76 (Tate, Infineon Trial Tr.)).

If, as Mr. Tate testifies, the reference to SDRAMs in his notes was actually to future SDRAMs including PLLs [ie. DDR SDRAMs], then further evidence suggests that Mr. Tate did not in fact inform LG Semiconductor executives that Rambus had relevant patents. When Mr. Tate once again met with executives from LG Semiconductor in 1997 it is clear that the executives were still unaware that Rambus had patents that it believed covered DDR SDRAMs. At that meeting an LG executive explained to Mr. Tate that LG's reason for favoring DDR was that it understood DDR to be a "royalty-free . . . open, jedec standard." (CX0957 at 1). It appears that Mr. Tate did nothing to disabuse LG's beliefs regarding the "open" and "royalty-free" nature of JEDEC's DDR SDRAM standard. (CX0957 at 1-2) This is not surprising because Mr. Tate had orchestrated a deliberate plan to hide the fact that Rambus believed it had patents relating to DDR SDRAMs. There were numerous instances prior to 2000 when Mr. Tate continued to advise his staff not to let customers and partners know that it felt DDR SDRAMs infringed its patents. (*See* CCFF 1676-1678, 1686, 1696-1697) For example, in early 1997, he advised his staff: "do *NOT* tell customers/partners that we feel DDR may infringe - our leverage is better to wait" (CX0919 at 1) Richard Crisp acknowledged that Mr. Tate gave such instructions: "Mr. Tate had explained to people . . . that he didn't want us to make any allegations that there might be some infringement. . . . we were basically told to not be telling customers and partners that we thing DDR might infringe our patents." (Crisp, Tr. 3408) (*See* CCFF 1263, 1682). Rambus's Chairman, Bill Davidow also acknowledged the plan stating in a July 1997 e-mail: "One of the things we have avoided discussing with our partners is intellectual property problem discussed in the fourth paragraph [referring to Rambus's thinking that SLDRAM and SDRAM DDR infringed

Rambus's patents]" (CX0939 at 1) In another July e-mail he similarly stated: "We have not discussed [possible infringement] with the DRAM manufacturers. We hope we never have to." (CX0936 at 1)

551. During a meeting in Korea in October 1995, Rambus informed Samsung that SyncLink and fast SDRAMs were heading in the direction where they might infringe future Rambus patents. (CX 2111, Tate Depo. at 316-18; CX 1729 at 109).

Response to Finding No. 551: The cited testimony does not support this proposed finding. While Mr. Tate did recall some statements being made with respect to SyncLink, with respect to "fast SDRAMs" the best he could do is to "assume" his notes referred to features like phase lock loops or dual-edge clocking (CX2111 (Tate, Depo.) at 318). Mr. Tate's incomplete and hazy recollection based on these cryptic handwritten notes should not be given much weight. The finding does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

There is overwhelming evidence, on the other hand, to the effect that Rambus did not disclose that its intellectual property extended more broadly beyond the RDRAM architecture to other products, such as SDRAMs and DDR SDRAMs. (See, for example: Complaint Counsel's reply to Respondent's Finding No. 550 ; CX1069 (Karp e-mail, 5/1/99: "They probably think they avoid our IP if they don't [use a narrow, packet-based bus]"); CX0770 (Harmon e-mail, 10/11/94: "[L]et's not rock the boat" by telling Samsung we have patent applications relating to on-chip PLL); CX0783 at 2 (Crisp e-mail, 2/26/95: "I certainly do not want to bring this intellectual property issue up without careful consideration. I especially do not want it all over JEDEC."); CX0711 at 68, 73 (Crisp e-mail, 5/24/95: "[I]t makes no sense to alert them to a potential [patent] problem they can easily work around."); CX1727A at 2 (Tate notes, 6/8/95 (quoting Horowitz

regarding disclosing Rambus intellectual property relating to SyncLink: "Stirring pot now makes us look like bad guys"); CX0837 at 2 (Crisp e-mail, 9/23/95: "we should re-evaluate our position relative to what we decide to keep quiet about, and what we say we have"); CX1277A at 1, 2 (Presentation, 3/96: "200Mhz SDRAM Myth:" "Challenges (do not tell them :-)"); CX0919 (Tate e-mail, 2/10/97: "do NOT tell customers/partners that we feel DDR may infringe – our leverage is better to wait"); CX0938 (Davidow e-mail, 7/11/97: "One of the things we have avoided discussing with our partners is intellectual property problem. . . . We have not yet told Siemens that we think SLDRAM and SDRAM-DDR infringe our patents."); CX0942 (Tate e-mail, 8/4/97: "our policy so far has been NOT to publicize our patents and i think we should continue with this"); CX0947 at 1 (Clarke e-mail, 8/15/97: "Q. Do Double Data Rate (DDR) SDRAMs use this patent? A. We don't know yet."); CX0960 (Tate e-mail, 10/1/97: "when joel [karp] starts we need to have our spin control ready for partners/etc as to why we are hiring him and what he will be doing."); CX0987 (Tate e-mail, 1/19/98: "ddr infringes our patents (question: when do we start saying this publicly?)"); CX1089 (Tate e-mail, 12/9/99: "it's important NOT to indicate/hint/wink/etc what we expect the results of our infringement analysis to be!!!"); CCFF 749 -750, 1240 - 1243, 1263, 1682).

552. During a meeting in Japan in October 1995, Rambus informed NEC that SyncLink and new SDRAMS (SDRAMs using a PLL or dual-edge clock) might end up in a position where they infringed future Rambus patents. (CX 2111, Tate Depo. at 319-20; CX 1729 at 119).

Response to Finding No. 552: The finding also does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies. The cited testimony was given by Mr. Tate in response

to a question that Complaint Counsel objected to as calling for speculation. Complaint Counsel, therefore, argues that this finding should be disregarded.

Further, Mr. Tate's incomplete and hazy recollection based on these cryptic handwritten notes should not be given much weight, particularly when it is contrasted to the great weight of evidence that Mr. Tate had successfully orchestrated a plan at Rambus to not disclose its belief that it had patents that related to SDRAMs and DDR SDRAMs (or as Mr. Tate puts it, SDRAMs using a PLL or dual-edge clock). (*See* CCRF 550-551). Further, the degree to which Mr. Tate disclosed that Rambus patents may relate to Synclink is irrelevant. Synclink was a "totally different architecture" compared to EDO, page mode and synchronous DRAMs (i.e. SDRAM and DDR). (Sussman, Tr. 1404-5) Like RDRAM and unlike SDRAMs, Synclink was a packetized device. (Sussman, Tr. 1404-1405) As stated in the reply to Respondent's Findings 550-551, no-one outside Rambus knew that Rambus believed it had intellectual property relating to SDRAMs and DDR SDRAMs. This was not surprising because they viewed the technologies as being very different. Gordon Kelley testified on attending a presentation by Rambus at IBM that he believed that Rambus RDRAM was fundamentally different from the SDRAM technology under discussion at JEDEC and that no intellectual property rights that Rambus had on RDRAM could be applicable to SDRAM or JEDEC. (G. Kelley, Tr. 2537-38, 2546).

553. During a meeting in Japan in October 1995, Rambus informed OKI of the possibility that there would be Rambus intellectual property that might apply to SyncLink and new SDRAMs. (CX 2111, Tate Depo. at 320-21; CX 1729 at 123).

Response to Finding No. 553: The cited testimony was given by Mr. Tate in response to a question that Complaint Counsel objected to as calling for speculation and lacking foundation. Complaint Counsel, therefore, argues that this finding therefore should be disregarded.

The finding does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

Further, Mr. Tate's incomplete and hazy recollection based on these cryptic handwritten notes should not be given much weight, particularly when it is contrasted to the great weight of evidence that Mr. Tate had successfully orchestrated a plan at Rambus to not disclose its belief that it had patents that related to SDRAMs and DDR SDRAMs (i.e. SDRAMs using a PLL or dual-edge clock). (*See* CCRF 550-551). Further, the degree to which Mr. Tate disclosed that Rambus patents may relate to Synclink is irrelevant. Synclink was a "totally different architecture" compared to EDO, page mode and synchronous DRAMs (i.e. SDRAM and DDR). (Sussman, Tr. 1404-5). Like RDRAM and unlike SDRAMs, Synclink was a packetized device. (Sussman, Tr. 1404-1405) As stated in the reply to Respondent's Findings 550-551, no-one outside Rambus knew that Rambus believed it had intellectual property relating to SDRAMs and DDR SDRAMs. This was not surprising because they viewed the technologies as being very different. Gordon Kelley testified on attending a presentation by Rambus at IBM that he believed that Rambus RDRAM was fundamentally different from the SDRAM technology under discussion at JEDEC and that no intellectual property rights that Rambus had on RDRAM could be applicable to SDRAM or JEDEC. (G. Kelley, Tr. 2537-38, 2546).

554. During a meeting with Intel in October 1995, Rambus informed Intel that it did not see how future memory chips could meet performance goals without using some or all of Rambus's inventions. (CX 2111, Tate Depo. at 322-24; CX 1729 at 134-36).

Response to Finding No. 554: The finding does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available

would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

The proposed finding also is incomplete and misleading. In fact, as late as January 1998, Mr. Tate was still considering whether he should inform Intel that he believed DDR SDRAMS and Synclink DRAMs infringed Rambus patents. (CX0984 at 3 (Tate January 1998 e-mail: "should we also disclose our position on patents and that we believe ddr's/sldram/etc. will likely infringe our patents? this is to show that whatever path the market takes it infringes our IP. should we tell intel this?") Even if Mr. Tate had shared this information with Intel in 1995, Intel was prevented under non-disclosure agreements with Rambus from sharing confidential information with third parties. (CCFF 1695).

555. DRAM manufacturer Micron Technology demonstrated its concern about Rambus's patents in 1995 and 1996. On November 7, 1995, Micron executive Jeff Mailloux sent a memo entitled "Rambus Inc. Patents" to several other Micron employees, including JEDEC representative Terry Walther. (RX 629; RX 630). Mr. Mailloux's memorandum stated in part as follows:

> "Attached are abstracts for the patents that have been granted to RAMBUS Inc. so far . . . . Please consider both the quality (is there prior art?) and the breadth (apply to more than just RAMBUS?) of the patents."

(RX 629 at 1; RX 630 at 1).

Response to Finding No. 555: This proposed finding is incomplete and misleading because it fails to state that the Micron investigation of Rambus patents occurred in connection with negotiation of a license for RDRAMs and related to an analysis for the Rambus patents on RDRAMs. (Appleton, Tr. 6534-6536; Lee, Tr. 6619) Terry Lee testified that he and Kevin Ryan reviewed the abstracts. (Lee, Tr. 6607) Mr. Lee testified that he did not do a specific investigation on Rambus prior art but that Mr. Mailloux had asked for what he and Mr. Ryan already knew based on their experience. (Lee, Tr. 6610) He further testified that the Rambus intellectual property he reviewed applied specifically to the RDRAM architecture. (Lee, Tr. 6610-

6611) Mr. Lee also testified that he was unaware of any other research done within Micron on Rambus intellectual property. (Lee, Tr. 6621) The proposed finding also ignores other record evidence that Micron was never told by Rambus that Rambus intellectual property might extend beyond the RDRAM architecture. (*See* CCFF 1679 - 1680).

The finding does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

556. Mitsubishi's Japanese patent department was also busy looking for prior art to Rambus's patents in November 1995. (RX 1041A at 1) ("[W]e have obtained Cray Corporation's patents to investigate the prior art for the patents owned by Rambus Inc. . . .").

Response to Finding No. 556: RPF 556 is unreliable. There was no testimony regarding this document at trial. The purpose behind the document is unclear. There has been no showing that the analysis of the Cray patents, even if it took place had any relevance to the current litigation.

The finding does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

557. In January 1996, the concerns of Micron and others about Rambus's intellectual property were reflected in the minutes of the SyncLink Consortium:

> "Rambus has 16 patents already with more pending. Rambus says their patents may cover our SyncLink approach even though our method came out of early RamLink work. Micron is particularly concerned to avoid the Rambus patents, though all of us share this concern."

(RX 663 at 2).

Response to Finding No. 557: The proposed finding is incomplete and does not support Respondent's contention that JEDEC members believed that if Rambus did obtain patents relating to SDRAMs, the patents would be invalid because of prior art. The concerns stated in the proposed finding were the relationship between the Synclink technology and Rambus patents. However, Synclink was a "totally different architecture" compared to EDO, page mode and synchronous DRAMs (i.e. SDRAM and DDR). (Sussman, Tr. 1404-5). Like RDRAM and unlike SDRAMs, Synclink was a packetized device. (Sussman, Tr. 1404-1405)

As stated in CCRF 550-551, no-one outside Rambus knew that Rambus believed it had intellectual property relating to SDRAMs and DDR SDRAMs. This was not surprising because they viewed the technologies as being very different. Gordon Kelley testified on attending a presentation by Rambus at IBM that he believed that Rambus RDRAM was fundamentally different from the SDRAM technology under discussion at JEDEC and that no intellectual property rights that Rambus had on RDRAM could be applicable to SDRAM or JEDEC. (G. Kelley, Tr. 2537-38, 2546). The finding does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

558. Others who took a close look at Rambus's intellectual property in this time period included Dr. David Gustavson, the Secretary of the SyncLink Consortium, who reviewed several European patent applications that Rambus had filed. (Gustavson, Tr. 9286). Dr. Gustavson has testified that he recognized immediately upon reviewing the Rambus patent applications that they had a broad scope that would apply to virtually any memory device, but that he believed the applications would never be allowed in light of their breadth. (Gustavson, Tr. 9287).

Response to Finding No. 558: This proposed finding is incomplete and misleading. Dr. Gustavson testified that he only looked at the Rambus European patent

applications once. (Gustavson, Tr. 9313) He testified that he never examined the applications with respect to Synclink. (Gustavson, Tr. 9313) He testified that he never looked at the specification with regard to trying to predict what Rambus may claim in the future. (Gustavson, Tr. 9313) In fact, he could not specifically recall whether he even looked at the specifications in the European applications. (Gustavson, Tr. 9313) He never considered whether the claims might relate to SDRAMs or DDR SDRAMs.(Gustavson, Tr. 9313-9314)

The proposed finding also is unreliable. Dr. Gustavson testified that he only looked at the European patent applications once and does not recall whether he even looked at the specifications. (Gustavson, Tr. 9313). Further he testified that he was not particularly interested in DRAMs and had never been a DRAM designer.(Gustavson, Tr. 9313-9314) He also testified that he is not a patent attorney. (Gustavson, Tr. 9316).

The finding does not support any inference that Rambus provided meaningful information concerning its intellectual property claims to the technologies at issue in this case. There is no basis to conclude that the information available would have enabled an informed decision whether to use the technologies that Rambus claimed to own or to pursue alternative technologies.

559. Dr. Gustavson testified that two Apple engineers, David James and Glen Stone, reviewed the Rambus patent applications along with him. (Gustavson, Tr. 9286).

Response to Finding No. 559: Complaint Counsel does not disagree.

560. Rambus's separation from JEDEC was formalized on June 17, 1996, when Rambus sent a letter to the JEDEC office that stated:

> "I am writing to inform you that Rambus Inc. is not renewing its membership in JEDEC.
>
> Recently at JEDEC meetings the subject of Rambus patents has been raised. Rambus plans to continue to license its proprietary technology on terms that are consistent with the business plan of Rambus, and those terms may not be consistent with the terms set by standards bodies, including JEDEC. A number of major companies are already licensees of Rambus technology. We trust

> that you will understand that Rambus reserves all rights regarding its intellectual property. Rambus does, however, encourage companies to contact Dave Mooring of Rambus to discuss licensing terms and to sign up as licensees.
>
> To the extent that anyone is interested in the patents of Rambus, I have enclosed a list of Rambus U.S. and foreign patents. *Rambus has also applied for a number of additional patents in order to protect Rambus technology*."

(CX 887 (emphasis added)).

Response to Finding No. 560: The proposed finding is incomplete. Rambus included with the letter a list of patents that were irrelevant to the work of JEDEC and failed to include any reference to patent applications. (CCFF 1111) Nor did the list include the '327 patent even though Rambus was seeking an enforcement readiness opinion on the '327 patent at the very time the withdrawal letter was sent to JEDEC. (Compare CCFF 1100 - 1104 with CCFF 1109 - 1112; *see also* CX3129 (Vincent, Micron Dep.) at 380-82). Furthermore, Rambus never informed JEDEC about the '327 patent (CCFF 1111) and knowledge of this non-disclosure reached the highest levels of Rambus, as illustrated when Rambus' CEO, Geoffrey Tate, wrote that "we already have the 327 patent but few people are aware of what it means." (CX0942 at 1; CCFF 1684).

561. Complaint Counsel have contended that Rambus deliberately omitted its newly issued '327 patent from the list of patents attached to its June 17, 1996 letter to JEDEC, and that the claims of the '327 patent would have alerted JEDEC members to the breadth of Rambus's potential patent claims. Complaint Counsel have pointed to the omission of the '327 patent as evidence of an intent to mislead. There was no evidence at trial, however, to support this contention. Instead, the only evidence presented on the issue showed that the '327 patent was left off the list of Rambus's patents by mistake. It was Lester Vincent's responsibility to compile the list of patents sent to JEDEC with the letter confirming Rambus's withdrawal. (CX 3129, Vincent Micron Depo. at 538.) Mr. Vincent did not purposely leave the '327 patent off the list. (*Id.*). The list was compiled in connection with an earlier draft of the letter in late March 1996 and was not updated when the letter was sent in June 1996. (CX 879 at 3; CX 3129, Vincent Micron Depo. at 490-91.) There was also no evidence at trial that any JEDEC member had reviewed or relied upon the list of patents. In any event, as discussed at Findings 591-3, the '327 patent was on a list of Rambus patents circulated in 1998 by Hyundai to a large group of DRAM

manufacturers, putting them in the same position as if the ’327 patent had been identified by Rambus.

Response to Finding No. 561: This Proposed finding is misleading, inaccurate, and not supported by record evidence. There was evidence presented at trial that the issuance of the ‘327 patent was a noteworthy event at Rambus and that the Notice of Allowance of claims that became the ‘327 patent occurred in October of 1995, well before any consideration of preparation of a withdrawal letter from JEDEC. (*See* CCFF 1076 - 1077, 1092 - 1095). The cited testimony from Mr. Vincent (which twice in both excerpts, at pages 491 and 538 is qualified as reflecting his “belief” as to what happened as opposed to direct testimony of what actually happened) needs to be weighed against other evidence showing that Rambus was seeking an enforcement readiness opinion on the ‘327 patent at the very time the withdrawal letter was sent to JEDEC. (Compare CCFF 1100 - 1104 with CCFF 1109 - 1112; *see also* CX3129 (Vincent, Micron Dep.) at 380-82). Furthermore, Rambus never informed JEDEC about the ‘327 patent (CCFF 1111) and knowledge of this non-disclosure reached the highest levels of Rambus, as illustrated when Rambus’ CEO, Geoffrey Tate, wrote that “we already have the ‘327 patent but few people are aware of what it means.” (CX0942 at 1; CCFF 1684).

See also CCRF 591 - 593.

B. There Is Substantial Evidence That After Rambus Left JEDEC, JEDEC Leaders and Members Were Aware Of Possible Rambus Intellectual Property Claims.

562. The evidence shows that after Rambus confirmed its departure from JEDEC in June 1996, JEDEC members and leaders were aware of possible Rambus intellectual property claims and even investigated the prior art that might defeat those claims.

Response to Finding No. 562: RPF 562 lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this

Court's July 10, 2003 Order on Post Trial Briefs. The statement that Rambus "confirmed its departure" from JEDEC is contradicted by the record evidence. Rambus has presented no evidence that it withdrew from JEDEC at any time prior to June 17, 1996, and the evidence shows that Rambus continued to enjoy the benefits of membership (including receipt of the meeting minutes) up to that time. (CCRF 7).

563. In October 1996, for example,

(RX 781 at 2) (*in camera*).

Response to Finding No. 563: The statement in RPF 563 is unreliable. First, the document was never used with any witness at trial. Second, the cited statement is vague. It is unclear what Rambus intellectual property was at issue and who was disputing its legality. Third, there is no evidence that this relates in any way to JEDEC or SDRAMs; rather it appears to be a statement relating to Rambus intellectual property on RDRAMs.

564. In December 1996, Micron executive Jeff Mailloux wrote a memorandum to Micron CEO Steve Appleton that stated in part that:

> "We have been investigating high speed DRAMs and the intellectual property associated with them for some time now. . . . We have also been investigating the prior art related to the area of high-speed DRAMs. From our research, we think many Rambus patents read on prior art or other patents."
> (RX 829 at 2).

Response to Finding No. 564: This proposed finding is incomplete and misleading because it fails to state that the Micron investigation of Rambus patents occurred in connection with negotiation of a license for RDRAMs and related to an analysis for the Rambus patents on RDRAMs. (Appleton, Tr. 6534-6536; Lee, Tr. 6619) Further, Steve Appleton, the recipient of the e-mail, testified that nothing in the cited e-mail indicates that internally within Micron there was any understanding that Rambus at this time possessed or believed that it could obtain patent rights extending to either SDRAM or DDR SDRAM. (Appleton, Tr. 6540). Terry

Lee, who was cc'd on the e-mail testified that the cited statement in Mr. Mailloux's e-mail was strictly based on information that he and Kevin Ryan had given to Mr. Mailloux. (Lee, Tr. 6621) Mr. Lee testified that he did not do a specific investigation on Rambus prior art but that Mr. Mailloux had asked for what he and Mr. Ryan already knew based on their experience. (Lee, Tr. 6610) He further testified that the Rambus intellectual property he reviewed applied specifically to the RDRAM architecture. (Lee, Tr. 6610-6611) Mr. Lee also testified that he was unaware of any other research done within Micron on Rambus intellectual property. (Lee, Tr. 6621) The proposed finding also ignores other record evidence that Micron was never told by Rambus that Rambus intellectual property might extend beyond the RDRAM architecture. (*See* CCFF 1679 - 1680).

565. Micron has also withheld several documents from this time period that relate to Rambus patent claims. For example, a May 28, 1997 e-mail from a Micron employee to a Micron attorney is described on Micron's privilege log as a "[c]onfidential communication regarding persons knowledgeable about Rambus patents." (RX 1920 at 422). Two months earlier, on March 26, 1997, a Micron lawyer sent an e-mail to Micron JEDEC representatives Terry Lee and Kevin Ryan that is described on the Micron privilege log as a "[c]onfidential communication regarding Rambus patents." (RX 1920 at 152). In April 1997, Mr. Ryan sent an e-mail to Mr. Lee and to attorney David Westergard that is again described as a "[c]onfidential communication regarding Rambus patents." (RX 1920 at 153).

Response to Finding No. 565: This proposed finding is misleading because citations to three entries from a 444-page privilege log does not show Micron was ever informed by Rambus as to the extent of Rambus intellectual property, in light of substantial evidence that Rambus did not inform others that its intellectual property extended beyond RDRAMs. (*See* CCFF 1679 - 1680 with respect to Micron and *see generally* CCFF 749 -750, 1240 - 1243, 1263, 1682). Complaint Counsel also notes that Micron entered into a RDRAM licensing agreement with Rambus around the time of these privilege log entries (*see* CCFF 1613), so it is not surprising that Micron was examining the very Rambus patents it would be licensing for the RDRAM.

566. These latter two e-mails coincide with the March 1997 JEDEC meeting, where Micron's JEDEC representatives demonstrated that they were well aware that Rambus's intellectual property reached *beyond* the RDRAM architecture and its so-called "packetized" and "narrow bus" features.

Response to Finding No. 566: This Proposed finding is misleading, inaccurate and not supported by record evidence. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Further, the statement in the proposed finding that Micron's JEDEC representatives demonstrated that they were well aware that they were well aware that Rambus's intellectual property reached beyond the RDRAM architecture is incorrect. In fact, Terry Lee, the Micron representative who raised the issue of potential Rambus intellectual property at the March 1997 meeting directly testified to just the opposite. (Lee, Tr. 6961-6962 ("Q. So by March '97 at least you believed that Rambus might have intellectual property claims that extended beyond the narrow bus, multiplexed, packetized RDRAM architecture; right? A. No. My concerns were strictly about a clocking scheme.")). Mr. Lee testified that the NEC presentation looked similar to a "loop-back" clock described in the Rambus '703 patent. (Lee, Tr. 6695) which he described as "a free-running clock that went to the end of bus and came back and was tapped off by the DRAMs for use of a read clock". (Lee, Tr. 6698) Others at JEDEC considered that a loop-back clock was part of the Rambus architecture as described in the '703 patent. (*See* Kellogg, Tr. 5059; *see also* Jacob, Tr. 5493-98 (describing the three categories of Rambus patent claims, covering (1) the narrow bus architecture, (2) the loop-back clock, and (3) the Rambus packaging)). The loop-back clock is also described as a "U-shaped" clock. (Jacob, Tr. 5467, 5500) The loop-back or U-shaped clock described in the '703 patent was not adopted as a part of the JEDEC SDRAM or DDR SDRAM standards. (CCFF 1354-1355)

567. The minutes of the March 1997 JC 42.3 meeting reflect that during a presentation regarding an NEC proposal involving DDR SDRAM, a representative stated that "[s]ome on the committee felt that Rambus had a patent on that type of clock design." (JX 36 at 7).

Response to Finding No. 567: Complaint Counsel agree that the quoted passage appears in the document, but there is nothing to indicate that "a representative" made the statement. Further, Complaint Counsel points out the type of clock design being described was the loop-back clock that members considered was part of the Rambus architecture and potentially was covered by Rambus's '703 patent. (Lee, Tr. 6695; Kellogg, Tr. 5059)

568. Micron representative Terry Lee was present at the March 1997 JC 42.3 meeting. He testified that he had raised the concern about a possible Rambus patent at the meeting that is reflected in the minutes. (Lee, Tr. 6957-8; JX 36 at 7).

Response to Finding No. 568: Complaint Counsel would add that the cited passage from Mr. Lee's testimony refers specifically to a "loop back" clocking system as described in the Rambus '703 patent that had been disclosed to JEDEC. (Lee, Tr. 6695, 6957).

569. The NEC representative's trip report for the March 1997 JEDEC meeting supports Mr. Lee's recollection, for it includes the following summary of the discussion regrading the NEC DDR proposal:

"

Company	Comments
Micron	This technique is patented by Rambus and they will not agree to the JEDEC patent policy.
Mosaid/VLSI	This may be a future bus concept. Future bus was invented before Rambus became a company, so this may not be a valid patent."

(RX 880 at 25).

Response to Finding No. 569: The Proposed finding does not support the conclusion that JEDEC would have disregarded Rambus intellectual property because some members questioned whether there might be prior art. Rather, the fact that members insisted that JEDEC abandon any consideration of the loop-back clock, and the fact that the loop-back clock

was never considered again at JEDEC (Lee, Tr. 6695-6696) demonstrates that JEDEC selected alternatives to technologies potentially covered by Rambus patents despite some members' questions as to whether there might be prior art on Rambus patents.

570. Mr. Lee also sent an e-mail on April 17, 1997 to Micron attorney David Westergard "regarding meeting summary and DDR." (RX 1920 at 421). This e-mail has been withheld by Micron on privilege grounds. (*Id.*).

Response to Finding No. 570: This Proposed finding is misleading to the extent it suggests that it related at all to Rambus intellectual property, as the word "Rambus" does not even appear in the cited entry. If it did, it likely related to the loop-back clock issue at the March 1997 meeting, as that is the only meeting involving DDR at which Rambus intellectual property was discussed.

571. Complaint Counsel have contended that JEDEC members had long believed that Rambus's intellectual property claims would reach only to the "packetized," "narrow bus" RDRAM architecture. As Mr. Lee testified, however, the NEC DDR proposal did *not* involve a "narrow bus" and was *not* "packetized." (Lee, Tr. 6961).

Response to Finding No. 571: This Proposed finding is potentially misleading and needs to be read in context with the next question and answer, where Mr. Lee testified that at the time of the NEC DDR proposal in March 1997 he did not believe that Rambus's claims reached beyond the narrow bus, multiplexed, packetized RDRAM architecture. (Lee, Tr. 6961-6962 ("Q. So by March '97 at least you believed that Rambus might have intellectual property claims that extended beyond the narrow bus, multiplexed, packetized RDRAM architecture; right?

A. No. My concerns were strictly about a clocking scheme.")).

572. Mr. Lee agreed that by March 1997, he thought that Rambus might have intellectual property claims relating not just to RDRAMs but to the work of the JC 42.3 committee as well. (Lee, Tr. 6962-2).

Response to Finding No. 572: The Proposed finding is incorrect in suggesting that Mr. Lee was aware of broad intellectual property rights by Rambus; as Mr. Lee testified, in

March 1997 he did not believe that Rambus's claims reached beyond the narrow bus, multiplexed, packetized RDRAM architecture. (Lee, Tr. 6961-6962 ("Q. So by March '97 at least you believed that Rambus might have intellectual property claims that extended beyond the narrow bus, multiplexed, packetized RDRAM architecture; right? A. No. My concerns were strictly about a clocking scheme.")).

573. In April 1997 – two years *before* the DDR SDRAM device was standardized by JEDEC – Mr. Lee and other Micron JEDEC representatives learned that Rambus intended to seek intellectual property rights with respect to the use of dual edge clocking in *all* memory devices.

Response to Finding No. 573: This Proposed finding is misleading, inaccurate, and not supported by record evidence. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. As noted elsewhere, Mr. Lee specifically testified that his concern related to a particular clocking scheme that appeared to be similar to something he had seen described in the Rambus '703 patent. (Lee, Tr. 6695, 6957, 6961-62). Furthermore, the clocking system described by NEC was never incorporated into any JEDEC standard. (Lee, Tr. 6696). If RPF 573 relates to the April 1997 email, that e-mail related to a industry "rumor" coming from an Intel employee and not from Rambus. (*See* CCRF 574 - 585).

574. On April 16, 1997, a Micron employee named Keith Weinstock sent an e-mail to various Micron employees that stated in part that "Rambus plans legal action to request royalties on all DDR memory efforts." (RX 920 at 2).

Response to Finding No. 574: The Proposed finding is misleading because the rumor contained in the cited portion of the email appears to have originated from James Akiyama, an employee in Intel's graphics department, and not from anyone at Rambus. (Lee, Tr. 6704) Micron did not regard the source of this rumor to be credible. (Lee, Tr. 6702)

575. At the time he prepared his April 16, 1997 e-mail, Mr. Weinstock was a Micron account representative with responsibility for Intel. (Lee, Tr. 6700, 6968).

Response to Finding No. 575: Complaint Counsel have no specific response.

576. Mr. Weinstock sent his April 16, 1997 e-mail, and its statement that "Rambus plans legal action to request royalties on all DDR memory efforts," to Jon Biggs, with a copy to Terry Walther, Jeff Mailloux, Terry Lee, Kevin Ryan, Gary Welch and Steve Trick. (RX 920 at 1).

Response to Finding No. 576: Complaint Counsel have no specific response.

577. At the time, Mr. Biggs was Mr. Weinstock's predecessor as the Micron account representative for Intel. (Lee, Tr. 6967). Mr. Mailloux was Micron's DRAM Marketing Manager at the time. (CX 3133, Mailloux Micron Depo. Tr. 4/5/01, 44:20-45:6). Mr. Walther was a JEDEC representative for Micron. (Lee, Tr. 6594, 6953). Mr. Welch was in Product Marketing at Micron, with responsibility for Rambus product. (Lee, Tr. 6967). Mr. Trick was a Micron employee responsible for module development. (Lee, Tr. 6973). Mr. Lee was in the Strategic Marketing department at Micron, reporting to Mr. Mailloux. He also attended JEDEC meetings frequently in the 1997-2000 time period. (Lee, Tr. 6591-95). Mr. Ryan was in a similar position as Mr. Lee and also attended JEDEC meetings in this time period. (Lee, Tr. 6601; JX 37 at 2; JX 39 at 2; JX 41 at 2; JX 43 at 1; JX 46 at 2, JX 49 at 1).

Response to Finding No. 577: Complaint Counsel have no specific response.

578. On April 17, 1997, Micron JEDEC representative Terry Walther responded to Mr. Weinstock's e-mail and asked him to confirm the report about Rambus's intellectual property claims:

> "Does Rambus believe they have a patent on changing data on both edges of the clock? . . . I think that is old technology. Can you find out what they think they have?"

(RX 920 at 1).

Response to Finding No. 578: Complaint Counsel have no specific response.

579. Mr. Weinstock responded to Mr. Walther's question:

> "*Yes, Rambus feels DDR for any memory is under their patent coverage*. James [Akiyama, an Intel employee] said that Rambus has more IP than Intel has seen. He further stated the determining factor would be whether the courts take a broad or a narrow view of the patents."

(RX 920 at 1) (emphasis added).

Response to Finding No. 579: Complaint Counsel notes that there is no emphasis in the original document. Further, the proposed finding is incomplete. Terry Lee testified that because the rumor contained in the cited portion of the email originated from James Akiyama, an Intel employee in its graphics department (Lee, Tr. 6704) Micron did not regard the source of this rumor to be credible. (Lee, Tr. 6702).

580. The April 17, 1997 response by Mr. Weinstock was copied to Mr. Mailloux, Mr. Lee and all of the other recipients of Mr. Weinstock's original e-mail. (RX 920 at 1).

Response to Finding No. 580: Complaint Counsel have no specific response.

581. Mr. Lee testified that he understood Mr. Weinstock's statement about Rambus's intellectual property claims over "DDR for any memory" to be a reference to the DDR SDRAM device that was then being discussed at JEDEC. (Lee, Tr. 6968).

Response to Finding No. 581: The Proposed finding is misleading because it does not take into account the prior answer, where Mr. Lee said he "was not sure what his intent was," referring to Mr. Weinstock's use of the phrase "for any memory." (Lee, Tr. 6968). Furthermore, as noted elsewhere, Mr. Lee testified that he did not view the information being conveyed from Mr. Akiyama at Intel to be credible. (Lee, Tr. 6702-03, 6980-83).

582. Mr. Lee also understood that Mr. Weinstock was referring to possible patent infringement lawsuits by Rambus when Mr. Weinstock wrote:

> "Rambus plans legal action to request royalties on all DDR memory efforts."

(Lee, Tr. 6971-2; RX 920 at 2).

Response to Finding No. 582: The Proposed finding is inaccurate and incomplete; when asked, Mr. Lee testified that his interpretation of portions of the document were that "it could" involve lawsuits, but he also referenced the Patent and Trademark Office. (Lee, Tr. 6971-72).

583. Mr. Lee testified that he did nothing at all to follow up on the reference to Rambus's intellectual property claims regarding "DDR for any memory." (Lee, Tr. 6702, 6972; RX 920 at 1).

Response to Finding No. 583: The testimony is incomplete because it fails to state the reasons given by Mr. Lee that the information "wasn't credible." (Lee, Tr. 6702-03).

584. Mr. Lee testified that as far as he knows, none of the other recipients of Mr. Weinstock's April 17, 1997 e-mail did anything to follow up on the reference to Rambus's intellectual property claims. (Lee, Tr. 6972-3).

Response to Finding No. 584: This Proposed finding is not supported by record evidence. Mr. Lee was not questioned about his knowledge of actions by some of the email recipients. Further, there is no reason to expect that Mr. Lee would know whether Micron took any follow-up steps.

585. Mr. Lee explained that he had not followed up with respect to the information regarding Rambus's possible intellectual property claims, and did not consider asking JEDEC to request "RAND" assurances from Rambus, because he "didn't believe this was true." (Lee, Tr. 6981).

Response to Finding No. 585: The Proposed finding is misleading and incomplete because it does not include all the reasons given for Mr. Lee's belief that the information was not viewed as credible. Mr. Lee also testified that (1) the rumor was hearsay, (2) Rambus while a JEDEC member had not made disclosures of such intellectual property claims, (3) Rambus in licensing negotiations with Micron had not made such claims, and (4) there was general "misinformation" in the industry given Rambus' desire to have Intel support its direct RDRAM product. (Lee, Tr. 6702-03).

586. After reviewing the April 16 and 17, 1997 Micron e-mails during trial, 42.3 chairman Gordon Kelley testified that he believed that the Micron JEDEC representatives who received the e-mails were obligated under the JEDEC patent policy to tell the JC 42.3 committee the information about Rambus's claims that is contained in the e-mails. (Kelley, Tr. 2748-9).

Response to Finding No. 586: This Proposed finding is misleading and inaccurate because the quoted testimony is taken out of the context. There is no evidence that Mr.

Kelley had ever seen the document before trial and had an understanding of the contents. Further, the question, to which Mr. Kelley responded "I believe that they were" assumed that the JEDEC representatives had believed the information to be credible. (*See* G. Kelley, Tr. 2749). As noted elsewhere, Mr. Lee of Micron testified at trial that he did not find the information to be credible. (*See* Lee, Tr. 6702-03, 6980-83).

587. In May 1997, Rambus engineer Richard Crisp met with the Vice President of Engineering for VIA Technologies, a chipset manufacturer based in Taiwan. (RX 924 at 1).

Response to Finding No. 587: The proposed finding is unreliable. The document cited was never used with any witnesses.

588. Mr. Crisp's e-mail regarding the May 1997 meeting states in part that the VIA executive had:

> ". . . told me that he thinks that SyncLink is going to be stepping all over Rambus patents. I told him that no one can know for sure about any of that until chips exist, but that since we were first and have a lot of fundamental patents, it would not be a surprise to find that to be the case, and if it were, that I felt quite sure we would pursue protection of our IP rights."

(RX 924 at 1).

Response to Finding No. 588: The proposed finding is unreliable. The document cited was never used with any witnesses. Further, the proposed finding is irrelevant. Synclink was a "totally different architecture" compared to EDO, page mode and synchronous DRAMs (i.e. SDRAM and DDR). (Sussman, Tr. 1404-5). Like RDRAM and unlike SDRAMs, Synclink was a packetized device. (Sussman, Tr. 1404-1405) As stated in the reply to Respondent's Findings 550-551, no-one outside Rambus knew that Rambus believed it had intellectual property relating to SDRAMs and DDR SDRAMs. This was not surprising because they viewed the Rambus and JEDEC SDRAM technologies as being very different. Gordon Kelley testified on attending a presentation by Rambus at IBM that he believed that Rambus RDRAM was fundamentally

different from the SDRAM technology under discussion at JEDEC and that no intellectual property rights that Rambus had on RDRAM could be applicable to SDRAM or JEDEC. (G. Kelley, Tr. 2537-38, 2546).

589. In July 1997, the official SyncLink Consortium minutes reflect a concern that the Consortium should "collect information relevant to prior art and Rambus filings" in anticipation that "Rambus will sue individual companies" for patent infringement. (RX 966 at 3).

Response to Finding No. 589: RPF 589 is incomplete because it neglects to point out that members of the SyncLink Consortium attempted to avoid Rambus patents. (CX0488 at 2 ("Micron is particularly concerned to avoid the Rambus patents, though all of us share this concern.")). Also, in February 1996, Mr. Crisp called Mr. Gustavson because he believed that Mr. Gustavson "was misinterpreting Rambus's position relative to Ramlink etc." (RX0593 at 1.) Mr. Crisp reported that Rambus was "not able to determine at this time" whether there was a conflict between the RamLink standard and Rambus's patents. (*Id.* at 1-2). Mr. Gustavson concluded, "I expect they won't try to interfere with the standardization process." (*Id.* At 2.) Further, for reasons described in Complaint Counsel's Response to Finding No. 588, the proposed finding is irrelevant.

590. At the next SyncLink Consortium meeting, some attendees were re-thinking their desire to obtain information relating to Rambus patents. As one attendee pointed out, "you may not want to know because that multiplies the damages," an apparent reference to the treble damages available from willful infringers. (RX 1001 at 5).

Response to Finding No. 590: The statement in this proposed finding is misleading and unreliable. No witnesses testified as to remembering the cited paragraph. Further, there is nothing in the document cited, itself, to connect the statement cited to Rambus patents and to the contention in the Finding that it indicates that some Synclink Consortium attendees were re-thinking their desire to obtain information relating to Rambus patents. RPF 590 is also incomplete because it neglects to point out that members of the SyncLink Consortium attempted

to avoid Rambus patents. (CX0488 at 2 ("Micron is particularly concerned to avoid the Rambus patents, though all of us share this concern.")). Also, in February 1996, Mr. Crisp called Mr. Gustavson because he believed that Mr. Gustavson "was misinterpreting Rambus's position relative to Ramlink etc." (RX0593 at 1.) Mr. Crisp reported that Rambus was "not able to determine at this time" whether there was a conflict between the RamLink standard and Rambus's patents. (*Id.* at 1-2). Mr. Gustavson concluded, "I expect they won't try to interfere with the standardization process." (*Id.* At 2.) Further, for reasons described in Complaint Counsel's Response to Finding No. 588, the proposed finding is irrelevant.

591. In January 1998, Micron JEDEC representative Terry Lee

(RX 1095 at 4). **[IN CAMERA]**.

Response to Finding No. 591: This proposed finding is incomplete and misleading.

) **[IN CAMERA**

TESTIMONY]

592. In July 1998, a Hynix executive sent an e-mail containing "a list of Rambus patents" to a large group of DRAM engineers and JEDEC representatives from such companies as Micron, Texas Instruments, IBM, VLSI, Compaq, Mosaid and Siemens. (RX 1214 at 1).

Response to Finding No. 592: The proposed finding is unreliable. Only one fact witness was questioned about the cited e-mail and he was not asked whether he could recall the document. He had no recollection of taking any action in response to the e-mail. (Lee, Tr.6994-6995) Further, if the e-mail was in fact circulated, it was in the context of Synclink rather than JEDEC. As noted in CCFR 588, the Synclink architecture is different than SDRAM and DDR SDRAM. Further, distributing the e-mail to the persons listed on e-mail is not the same as distributing it to JEDEC members.

593. The list of patents provided by the Hynix executive included the '327 patent that Rambus had left off the list of patents submitted with its JEDEC resignation letter. (RX 1214 at 1).

Response to Finding No. 593: The proposed finding is unreliable. There is no evidence that the cited e-mail was ever actually distributed. Only one fact witness was questioned about the cited e-mail and he was not asked whether he could recall the document. He had no recollection of taking any action in response to the e-mail. (Lee, Tr.6994-6995)

594. Complaint Counsel's technical expert, Dr. Bruce Jacob, who has testified (contrary to Rambus's expert) that claims contained in the '327 patent are infringed by memory devices that comply with the DDR SDRAM standard, has *also* testified that if the engineers who received the July 1998 e-mail (RX 1214), were reasonable engineers, *they would have known* from looking at the '327 patent that it covered the DDR SDRAM device they were working on at the time. (Jacob, Tr. 5675).

Response to Finding No. 594: The proposed finding is misleading and unreliable. It assumes that the engineers cc'd in the e-mail received and read the e-mail and the attached list, collected all of the patents contained on the attached list, completed a thorough analysis of the claims in each of those patents, and correctly assessed the scope of coverage of those patents. There is no evidence that any of the listed engineers actually did any of this. Only one fact witness was questioned about the cited e-mail and he was not asked whether he could recall the

document. He had no recollection of taking any action in response to the e-mail. (Lee, Tr.6994-6995)

595. In light of the foregoing, it is clear that after Rambus left JEDEC, various JEDEC members were aware of possible Rambus patent claims relating to the work of the JC 42.3 committee. There is no record evidence that any of these members contacted Rambus to make any further inquiry regarding those possible claims or to ask Rambus for "RAND" assurances.

Response to Finding No. 595: The proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, to the degree that it purports to reference prior findings, it is unclear as to what findings it is referring.

VII. RAMBUS INFORMED THE INDUSTRY AND THE WORLD OF ITS INTENT TO OBTAIN BROAD PATENT PROTECTION FOR ALL OF ITS INVENTIONS.

A. Introduction.

596. It is not surprising that JEDEC leaders and JEDEC members were aware of and concerned about the possibility that Rambus could obtain patent protection that extended beyond the RDRAM architecture. As discussed below, Rambus informed the public and the DRAM industry throughout the early 1990's that it was seeking broad intellectual property protection. Moreover, as discussed below, a review of any of Rambus's published patents or patent applications would have made it clear to a reasonably experienced engineer or patent lawyer that Rambus's patents could cover the use of various features in any synchronous DRAM.

Response to Finding No. 596: This proposed finding is not supported by record evidence. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding is also contrary to the weight of substantial evidence that (1) Rambus did not inform the industry that their patents might extend beyond the RDRAM architecture to cover features incorporated in the JEDEC standards (*see* CCFF 1238 - 1265) and

(2) those who reviewed the publicly available information in the early 1990s (i.e., issued patents and/or public foreign patent applications) did *not* reach the conclusion that Rambus intellectual property would be broad enough to cover the SDRAM standards or features such as dual-edge clocking and on-chip PLLs or DLLs. (*See* CCFF 1266 - 1276). At a minimum, the fact that there is contrary testimony on these issues (i.e., *compare* RPF 597 - 702 *with* CCFF 1238 - 1357) suggests that it was not "clear" at all that Rambus had patents coving features of synchronous DRAMs, and therefore, the conclusion expressed in this finding is erroneous and contrary to the record evidence.

B. Rambus's Public Disclosures In 1992 Told The World Of Rambus's Desire To Obtain Broad Patent Coverage.

597. On March 9, 1992, Rambus held simultaneous events in the Silicon Valley and in Tokyo to publicly announce its technology and its business plan. (Farmwald, Tr. 8182-84; RX 67 at 1). Prior to this date, Rambus had presented its technology to companies on an individual basis and had secured licenses from three of the top five DRAM manufacturers: Fujitsu, NEC, and Toshiba. (RX 67 at 2).

Response to Finding No. 597: The Proposed finding is incomplete and misleading because it does not acknowledge the context in which such announcement of the Rambus technology occurred. The cited document (RX 67) talks about "major architectural innovation" and "[a] major change to DRAM architecture," indicating that this (the narrow bus, multiplexed architecture) is the key innovation offered by Rambus technology. (RX 67 at 1) In addition, the references to license fees and royalties relate to situations where "Rambus Inc. provides licensees a full range of documentation, engineering and implementation services" relating to the Rambus-compatible interface. (RX 67 at 2)

598. The press release announcing these events stated that Rambus's revolutionary technology would offer a tenfold improvement over traditional DRAMs and would solve the memory bottleneck. (RX 67 at 1). The press release also described Rambus's business plan as licensing its technology in return for license fees and royalties. (RX 67 at 2). By controlling the Rambus interface standard, Rambus would ensure compatibility. (RX 67 at 2). The press release

also made it clear that Rambus's "open standard" would be "available for license by any IC company." (RX 67 at 2; *see also* Farmwald, Tr. 8185).

Response to Finding No. 598: *See* CCRF 597. The cited text (RX0067 at 2) makes clear Rambus was announcing an intent to seek license fees and royalties for products that were compatible with the Rambus RDRAM design and RDRAM interface; it states nothing about Rambus technology or intellectual property extending to other, non-compatible products. Complaint Counsel contend that Rambus used the term the term "open standard" in this context in a manner fundamentally different from the term "open standard" as used by industry standard setting organizations, such as JEDEC. (*See* CCFF 300-304; CX0903 at 2 ("the job of JEDEC is to create standards which steer clear of patents . . . ."); *id.* ("Open standards seem at odds with our business model . . . Rambus would want to retain ownership of IP developed so that we could tax the makers")).

599. At the events, Rambus made available a "Corporate Backgrounder" that provided an overview of Rambus's business strategy and its technology. (RX 81; Farmwald, Tr. 8186). The Backgrounder explicitly detailed Rambus's intellectual property strategy: "Rambus Inc. is fully protecting the intellectual property rights of its technology by filing basic, broad patents in all major industrial nations around the world." (RX 81 at 3). This statement reflected Rambus's patent application activity. (Farmwald, Tr. 8186-87).

Response to Finding No. 599: This Proposed finding is misleading to the extent it suggests this document would put anyone on notice that Rambus had intellectual property beyond the Rambus RDRAM architecture. The reference to "its technology" in the cited passage (RX0081 at 3) suggests Rambus claims related only to technology as applied to Rambus-compatible DRAMs, as indicated in the first paragraph of the "corporate overview" section of the document where it refers to "a revolutionary DRAM architecture and high speed chip-to-chip date transfer technology" with specific reference to trademarked "RDRAM" and "the Rambus channel" which is further described as "a narrow, high speed bus." (RX 81 at 3)

600. Later in this same public document, there are descriptions of Rambus's technology. (RX 81 at 8-11). The Backgrounder states that Rambus's "dramatic performance improvements were achieved through numerous technical breakthroughs" and then proceeds to describe "[s]ome of the major technical highlights of the Rambus solution" (RX 81 at 8). The technology descriptions included the use of dual-edge clocking: "An innovative electrical interface permits the Rambus Channel to operate at 500 Megabytes/second by using both edges of a 250 MHz clock." (RX 81 at 8). Moreover, the technology descriptions explicitly state that Rambus used the on-chip PLL/DLL technology: "Clock skew and capacitance loading are minimized by a phase lock loop circuit on board both the master and the RDRAM." (RX 81 at 8).

Response to Finding No. 600: This Proposed finding is misleading and incomplete as it ignores the fact that there is nothing in the document to indicate that Rambus might have intellectual property on either of these features outside the context of the RDRAM architecture and interface (i.e., *see* references to "Rambus Channel" and "RDRAM" in the quoted passages), as discussed in response to RPF 599 above.

601. The Backgrounder also made it clear that Rambus's technology was divided into three distinct elements of the memory system: the Rambus Channel (the high-speed bus); the Rambus Interface (the circuitry that connects a device, such as a controller or DRAM, to the bus); and the Rambus DRAM (the memory itself). (RX 81 at 7; Farmwald, Tr. 8188-8190).

Response to Finding No. 601: The Proposed finding, while accurate, is misleading because the quoted passage does nothing to suggest that Rambus might have intellectual property on any of these features outside the context of the RDRAM architecture and interface. In fact, the three headings on the cited page – "Rambus Channel," "Rambus Interface" and "Rambus DRAM - RDRAM" suggest that the applicability of the technology – and hence any intellectual property associated with that technology – is limited to use in Rambus-compatible systems. (*See* RX 81 at 7)

602. The Backgrounder also informed every reader that Rambus's business strategy was to license its technology, work with the licensee to help implement the technology, and to receive fees and royalties in return. (RX 81 at 3; see also Farmwald, Tr. 8187). Moreover, it stated that "Rambus technology is an open standard that Rambus Inc. will license to any IC company." (RX 81 at 3).

Response to Finding No. 602: *See* CCRF 598, which involves similar language in another document. The cited text here (RX0081 at 3) makes clear Rambus was announcing an intent to seek license fees and royalties for products that were compatible with the Rambus RDRAM design and RDRAM interface; it states nothing about Rambus technology or intellectual property extending to other, non-compatible products. Complaint Counsel contend that the term "open standard" as used by Rambus in this context is different than the term "open standard" as used by industry standard setting organizations, such as JEDEC. *See* CCFF 300 - 304.

603. Later that year, at the invitation of Betty Prince (Prince, Tr. 8986-87), Dr. Farmwald and David Mooring of Rambus published an article in the October 1992 issue of IEEE Spectrum, which gave a brief description of the Rambus technology and stated that the "technology behind the architecture can be licensed for a royalty fee comparable to that for other patented technologies." (RX 332 at 1).

Response to Finding No. 603: The cited passage references licensing of the Rambus "memory architecture" and does not suggest that Rambus has any intellectual property extending beyond the RDRAM architecture that is described in the article. (RX 332 at 1).

604. Testimony at trial confirms that Rambus's business model was well known in the industry during the time Rambus attended JEDEC meetings. Brett Williams, a JEDEC representative for Micron testified that in 1992, "I knew it was [Rambus's] business model to patent their technology, and that's how they would gain their revenues." (Williams, Tr. 857). Similarly, Martin Peisl of Infineon stated that he was aware of Rambus's business model in the early 1990's and expected Rambus to get patents to cover their technology. (Peisl, Tr. 4505).

Response to Finding No. 604: The Proposed finding is incomplete because it does not provide the full context in which the cited testimony was given. For example, in response to the same line of questioning, Mr. Williams testified, "I did not know on exactly what they had patents on." (Williams, Tr. 856-57). Similarly, Mr. Peisl testified that, as of 1999, he had assumed the JEDEC SDRAM and DDR standards would be free of royalties, which was the opposite of his understanding with respect to parts using the proprietary Rambus technology. (Peisl, Tr. 4430-31; CCFF 1256). Additionally, Mr. Peisl testified that he did not learn that Rambus was claiming its

intellectual property extended to SDRAMs until March of 2000, when he received new about the patent dispute between Rambus and Hitachi. (Peisl, Tr. 4441, 4443).

605. According to Andreas Bechtelsheim, formerly of Sun Microsystems, Rambus made very clear to Sun that it intended to seek patent coverage for all of its inventions and developments, and Rambus explained to various companies, including Sun, that it was seeking patent coverage for its inventions because it intended to obtain revenue or earn revenue through licensing its technology to both memory manufacturers and system manufacturers. (Bechtelsheim, Tr. 5819).

Response to Finding No. 605: This Proposed finding is misleading and, as is clear from the surrounding testimony, taken out of context. Reading from an answer on the prior page, it is clear that Mr. Bechtelsheim was referring to Rambus technology relating to "the nature of their interface, the so-called Rambus memory protocol, and the performance clock rates associated with that interface." (Becthelsheim, Tr. 5818). Furthermore, as noted in Complaint Counsel's proposed findings, Mr. Bechtelsheim also testified that he had not heard any rumor or suggestion that Rambus might have patents that would extend to JEDEC-compliant SDRAMs or DDR prior to press reports in 2000 about Rambus patent enforcement activity, and that such information was a "complete surprise" to Mr. Bechtelsheim. (Bechtelsheim, Tr. 5880-81, CCFF 1251; *see also* CCFF 1250 (Rambus did not suggest that its patents extended to SDRAM or other memory architectures)).

C. Rambus Disclosed Its Inventions To The DRAM Industry.

1. Rambus Disclosed Its Inventions During Visits To DRAM Manufacturers And Systems Companies.

606. In 1989-90, Drs. Farmwald and Horowitz made visits to many DRAM manufacturers and systems companies to try to convince them about the benefits of their approach and to get feedback from them. (Horowitz, Tr. 8515).

Response to Finding No. 606: Complaint Counsel have no specific response.

607. Among the DRAM manufacturers that Drs. Farmwald and Horowitz visited in 1989-90 were Texas Instruments, IBM, Toshiba, Fujitsu, Mitsubishi, NEC, Matsushita, Micron and Siemens. (Horowitz, Tr. 8515; Farmwald, Tr. 8166).

Response to Finding No. 607: Complaint Counsel have no specific response.

608. Among the systems companies that Drs. Farmwald and Horowitz visited in 1989-90 were IBM (both a DRAM manufacturer and a systems company), Sun Microsystems, Motorola, Apple, SGI and Tandem. (Horowitz, Tr. 8515-16; Farmwald, Tr. 8166-7).

Response to Finding No. 608: Complaint Counsel have no specific response.

609. The response to the early presentations in 1989-90 was "just disbelief" that Drs. Farmwald and Horowitz would be able to achieve a 500 megabit per second DRAM data rate. (Horowitz, Tr. 8516). People who listened to these presentations were also skeptical about many of the specific features of the technology. For example, it was felt that putting registers on a DRAM was too expensive for a commodity part and that one could not put a phase locked loop or a delay locked loop on the DRAM itself. (Horowitz, Tr. 8517).

Response to Finding No. 609: Complaint Counsel agree that many customers were skeptical about the Rambus technology, in part because of its "revolutionary" nature as well as its high cost. (*See* CCFF 125 - 128, 869, 1606; *see also* CCFF 1839 - 1849, 1851 - 1854, 1857 - 1859)

610. The four inventions at issue in this case were described in these early presentations. For example, one of the early presentations that Dr. Horowitz gave, with slides dated January 31, 1990, states that the Rambus interface "allows 'block mode' transfer from an individual DRAM" with "1-1024 byte long blocks supported." (RX 29 at 9; Horowitz, Tr. 8518-20). This describes variable block size or variable burst length. (Horowitz, Tr. 8520).

Response to Finding No. 610: This Proposed finding is misleading and incomplete. As noted elsewhere, to the extent these "inventions" were described to customers, they were always described in the context of the Rambus-compatible, narrow bus architecture. *See* CCFF 746 - 756, 1238 - 1265. The cited document is also taken out of context, as it describes the basic "RamBus concept" as "a new DRAM interface and packaging concept" (RX 29 at 6) and specifically contrasts the Rambus design with "conventional DRAMs" (RX 29 at 7), again with nothing to indicate that any of the Rambus technology or intellectual property might apply in a more conventional DRAM architecture. Furthermore, on cross examination Dr. Horowitz testified

that "variable block size" was not exactly the same as programmable burst length. (Horowitz, Tr. 8570).

611. The January 31, 1990 presentation also describes the use of a delay locked loop on the DRAM to reduce clock skew. (RX 29 at 33-34; Horowitz, Tr. 8521-22).

Response to Finding No. 611: This Proposed finding is misleading. The cited document uses the term "delay lines," not "delay locked loop" and certainly does not indicate that Rambus intellectual property is likely to extend to all forms of on-chip PLLs or DLLs used on all DRAMs. (*See* RX 29 at 33). The self-serving testimony from Dr. Horowitz, solicited after a leading objection by Complaint Counsel was sustained (Horowitz, Tr. 8521-22), should be discounted given Dr. Horowitz's admitted strong financial interest in the outcome of this case. (Horowitz, Tr. 8565-66 (witness owns "about two million shares of Rambus stock")).

612. The January 31, 1990 presentation also refers to the dual-edge clocked or double data rate technique. (RX 29 at 34; Horowitz, Tr. 8522-23).

Response to Finding No. 612: This Proposed finding is misleading. The cited document does not use the term "dual-edge clocking" or "double data rate" (*see* RX 29 at 34); rather, this statement is a conclusion offered by Dr. Horowitz, a witness with a stake in the outcome, based on the phrase Furthermore, nothing in the document or the testimony suggests that this put anyone on notice that

2. Rambus Disclosed Its Inventions In Technical Descriptions Of The Rambus Technology.

613. In the 1990-91 period, Dr. Horowitz prepared detailed technical descriptions of the Rambus technology. (Horowitz, Tr. 8523). These documents were for Rambus's internal use and were also used with customers and potential customers to convince them of the merits of Rambus technology and to help them build it. (Horowitz, Tr. 8523-24).

Response to Finding No. 613: Complaint Counsel have no specific response, except to note that the cited testimony is consistent with other evidence that the only information

disclosed related to use in Rambus proprietary RDRAM architecture and interface. (*See* CCFF 746 - 756, 1238 - 1265).

a. <u>The May 1990 Technical Description Discloses the Rambus Inventions</u>.

614. One of these technical descriptions is dated May 7, 1990 and was generated at about that time. (RX 63; Farmwald, Tr. 8168-69; Horowitz, Tr. 8524-25).

<u>Response to Finding No. 614</u>: Complaint Counsel have no specific response.

615. The fax line on the May 7, 1990 technical description indicates that it was sent to Siemens. (Farmwald, Tr. 8168).

<u>Response to Finding No. 615</u>: Complaint Counsel have no specific response.

616. The May 7, 1990 technical description discloses all four of the technological features at issue here. (Horowitz, Tr. 8525). For example, the technical description disclosed dual-edge clocking in a figure with two input receivers, one clocked by a signal designated "CLK" (clock) and the other clocked by the complement of CLK (clock bar), a signal that is zero when clock is one and vice versa. (RX 63 at 10; Horowitz, Tr. 8525-26). This means that one receiver samples an input when the clock goes high (the rising edge of the clock) and the other when the clock goes low (the falling edge). (Horowitz, Tr. 8526). This is the dual-edge clocking feature.

<u>Response to Finding No. 616</u>: This Proposed finding is misleading because it takes the cited document out of context. At the outset, it states: "This document describes a high speed bus" (RX 63 at 1). The document also states that the "fundamental idea" is the concept of "a bus which provides high-speed, multiplexed communication between processing devices and memory devices." (RX 63 at 4). The "disclosure" cited in the document does not even reference the term dual-edge clocking. (*See* RX 63 at 10). Even accepting Dr. Horowitz's interpretation of the figure as dual-edge clocking, nothing in the document suggests Rambus has intellectual property on all dual-edge clocking as used in all DRAMs, not just those in connection with the RDRAM concept.

617. The May 7, 1990 technical description also discloses a delay-locked loop on the DRAM. (Horowitz, Tr. 8527-28). A figure in the technical description shows two delay locked loops generating the internal clocks for Rambus design. (RX 63 at 14; Horowitz, Tr. 8527). This is the on-chip DLL feature.

Response to Finding No. 617: This proposed finding is misleading. The figure pointed out by Dr. Horowitz (RX 63 at 14) referred to a specific implementation of "variable delay lines" in connection with the RDRAM architecture and did nothing to inform third parties that Rambus might have intellectual property extending to all uses of on-chip PLLs and DLLs outside the RDRAM concept. Finally, there is other testimony in the record about a similar figure suggesting that a reasonable engineer would not interpret this figure to represent a DLL. *See* CCFF 1335 -1340 for a discussion of Figure 12 from Rambus '898 application..

618. The May 7, 1990 technical description also discloses programmable latency. (Horowitz, Tr. 8528). In the "device registers" section of the document an "access time" or latency register is listed. (RX 63 at 18; Horowitz, Tr. 8528). "Latency" refers to the time between request and response. (Horowitz, Tr. 8530). The document explains that a fixed value for latency "does not allow for technology improvements," and, consequently, the Rambus system "set[s] the time between request and response during system reset." (RX 63 at 5; Horowitz, Tr. 8530-31). In other words, the value in the access time or latency register would be fixed when the system was started up and probably would not be changed after that time. (Horowitz, Tr. 8531). This is the programmable latency feature.

Response to Finding No. 618: This Proposed finding is misleading to the extent it suggests this technical description put third parties on notice that Rambus might have intellectual property covering a programmable CAS latency feature as used in SDRAMs. The document says nothing about the scope of Rambus intellectual property; furthermore, the document describes only access time registers used in the Rambus narrow bus RDRAM architecture. For example, on one of the cited pages in the immediately prior paragraph the document makes clear that the "DRAM implementation" being described is a system where "all of data, address, and control information are multiplexed on a single set of wires." (RX 63 at 5) While the document does refer to "access time registers" (RX 63 at 18), word "latency" not used. Furthermore, as Dr. Horowitz testified on cross-examination that the term "access time register" is not exactly the same thing as programmable CAS latency. (Horowitz, Tr. 8570). Furthermore, the Proposed finding ignores

expert testimony that the concept of "access time" as used in the Rambus RDRAM protocol is different than the concept of programmable CAS latency as used in JEDEC-compliant SDRAMs. (*See* CCFF 1322 - 1326).

619. The May 7, 1990 technical description also discloses variable burst length. (Horowitz, Tr. 8528-29). The document contains a table showing a variable number of bytes in the block size or burst length depending on the value in the "BlockType" field. (RX 63 at 21; Horowitz, Tr. 8528-29). This is the variable burst feature.

Response to Finding No. 619: This Proposed finding is misleading to the extent it suggests this technical description put third parties on notice that Rambus might have intellectual property covering a programmable burst length feature as used in SDRAMs. Block size in the cited document is described in the context of a narrow bus, multiplexed, packetized system, which is different from the programmable burst length feature used in JEDEC-complaint SDRAMs. (RX 63 at 5, 21; *see* CCFF 1314 - 1318 (expert testimony discussing similar sections of the '898 patent application)). Furthermore, as Dr. Horowitz testified on cross-examination that the term "variable block size" is not exactly the same thing as programmable burst length. (Horowitz, Tr. 8570).

b. The November 1990 Technical Description Discloses The Rambus Inventions.

620. A later Rambus technical description, dated November 5, 1990, was generated at around that time. (RX 94; Farmwald, Tr. 8169; Horowitz, Tr. 8535).

Response to Finding No. 620: Complaint Counsel have no specific response.

621. The November 5, 1990 technical description was sent to Siemens. (RX 99; Farmwald, Tr. 8169-70).

Response to Finding No. 621: Complaint Counsel have no specific response.

622. The November 5, 1990 technical description disclosed dual-edged clocking. First, the document contains the same figure relating to inputting data on both edges of the clock as in the May 7, 1990 description. (RX 63 at 10; RX 94 at 15; Horowitz, Tr. at 8535). Second, the document shows that the output data is also being transmitted on both edges of the clock. (RX 94 at 19; Horowitz, Tr. 8536).

Response to Finding No. 622: *See* CCRF 616, which relates to the figure in RX 63. The November 1990 document (RX 94) contains similar language, indicating that the "Rambus invention" involved "a small number of high-speed signals that carry all address, data and control information," (RX 94 at 9) and as with the earlier document there is nothing to put anyone on notice that Rambus was likely to have intellectual property claims outside the narrow bus, multiplexed RDRAM architecture.

623. The November 5, 1990 technical description disclosed two alternatives for the DRAM clock circuitry. One alternative was to use a phase locked loop. (RX 94 at 45; Horowitz, Tr. 8536-37). The other alternative was to use delay locked loops. (RX 94 at 46; Horowitz, Tr. 8537).

Response to Finding No. 623: *See* CCRF 617 and 622. The diagrams pointed out by Dr. Horowitz do nothing to inform third parties that Rambus might have intellectual property extending to all uses of on-chip PLLs and DLLs outside the RDRAM concept.

624. The November 5, 1990 technical description disclosed variable latency using a data delay field in the request packet. (RX 94 at 59; Horowitz, Tr. 8537-38).

Response to Finding No. 624: *See* Response to RPFs 618 and 622. The RPF ignores expert testimony that the concept of "access time" as used in the Rambus RDRAM protocol is different than the concept of programmable CAS latency as used in JEDEC-compliant SDRAMs. (*See* CCFF 1322 - 1326)

625. The November 5, 1990 technical description disclosed variable block size or burst length with a table similar to that in the May 7, 1990 technical description. (RX 63 at 21; RX 94 at 60; Horowitz, Tr. at 8538).

Response to Finding No. 625: *See* Response to RPFs 619 and 622. Block size in the cited document is described in the context of a narrow bus, multiplexed, packetized system, which is different from the programmable burst length feature used in JEDEC-complaint SDRAMs. (RX 63 at 5, 21; *see* CCFF 1314 - 1318 (expert testimony discussing similar sections of the '898 patent application)).

c. Siemens Responded to the Technical Descriptions with a List of Questions about Rambus's Inventions.

626. Both Dr. Farmwald and Dr. Horowitz received feedback from Siemens regarding the November 5, 1990 technical description. (RX 102; RX 117; Farmwald, Tr. 8171-72; Horowitz, Tr. 8541-42).

Response to Finding No. 626: Complaint Counsel have no specific response.

627. A fax from K. Horninger of Siemens to Dr. Farmwald, dated December 7, 1990, contained a detailed list of questions relating to the November 5, 1990 technical description. (RX 102; Farmwald, Tr. 8171-73).

Response to Finding No. 627: Complaint Counsel have no specific response.

628. A fax from H.J. Neubauer of Siemens to Dr. Horowitz, dated January 29, 1991, stated "Dear Dr. Horowitz, concerning the RAMBUS Technical Description some basic items remained open. In the following we present a list of detailed questions to you which we would like to get answered." (RX 117 at 2; Horowitz, Tr. 8542).

Response to Finding No. 628: Complaint Counsel have no specific response.

629. A number of the questions in the fax that Siemens sent to Dr. Horowitz related to the four features of Rambus technology at issue in this case. Question number one in the Siemens fax asked about the details of how eight bits of data would be transmitted by the DRAM and relates to Rambus's variable block size feature. (RX 117 at 2; Horowitz, Tr. 8543-44).

Response to Finding No. 629: The first sentence of the proposed finding that "a number" of questions related to the four technologies is unsubstantiated by record evidence. Question number one actually relates to Siemens' concern as to whether or not the Rambus interface will support the then predominant technology, fast page mode: "A RAMBUS-DRAM has to support Fast Page Mode." (RX 117 at 2). As noted elsewhere, fast page mode had been standardized at JEDEC and became the predominant DRAM technology in the early to mid-1990s. (*See* CCFF 85, 566, 2563, 2642)

630. Question number two in the Siemens fax asked about the implementation of variable latency in the Rambus technology. (RX 117 at 2; Horowitz, Tr. 8544).

Response to Finding No. 630: As noted in Response to RPFs 617 and 623 above, the information about the "variable latency" as used in the RDRAM protocol was insufficient to

put third parties on notice with respect possible Rambus intellectual property covering the concept of programmable CAS latency as used in JEDEC-compliant SDRAMs.

631. Another question in the Siemens fax referenced Figure 13 on internal page 14 of the November 5, 1990 technical description. (RX 117 at 4). That figure showed dual-edge clocking or double data rate on the output. Dr. Horowitz's understanding was that Siemens' question related to the implementation of the double data rate drivers as shown in the November 5, 1990 technical description. (RX 94 at 19; RX 117 at 4; Horowitz, Tr. 8546).

Response to Finding No. 631: This Proposed finding is misleading. There is no evidence in the record as to Siemens's understanding or interpretation that Figure 13 represented dual-edge clocking; the cited portion of the document itself does not reference dual-edge clocking (*see* RX0117 at 4), and, as indicated elsewhere, an experienced engineer would have no reason to believe that the clocking concept disclosed by Rambus in the early 1990s would be broad enough to cover dual-edge clocking as used in JEDEC-compliant DDR SDRAMs. (*See* CCFF 1327 - 1334) Additionally, the self-serving testimony from Dr. Horowitz, which was limited after an objection from Complaint Counsel (*see* Horowitz, Tr. 8545-46), cannot serve as a substitute for the lack of any understanding by Siemens or any other DRAM manufacturer of the extent of any Rambus intellectual property. In fact, there is other evidence in the record suggesting that Siemens, later Infineon, did not view double date rate or DDR SDRAM (which adopted the dual-edge clocking feature) as subject to possible royalty claims by Rambus. (*See* CCFF 1256)

632. Another question in the Siemens fax referenced Figure 28 on internal page 41 of the November 5, 1990 technical description. (RX 117 at 4). That figure shows a delay locked loop and Siemens' question was about the delay locked loop. (RX 94 at 46; RX 117 at 4; Horowitz, Tr. 8546).

Response to Finding No. 632: This Proposed finding is misleading and ignores other evidence in the reord. The figure in question is entitled "delay line clock generator" and does not reference a "delay locked loop." (RX 94 at 46; *see* RX 117 at 4, referencing Figure 28). Furthermore, Dr. Horowitz's self-serving testimony is not credible evidence of the extent of

knowledge or lack of knowledge third parties may have had about Rambus intellectual property coverage. As noted previously, there is expert testimony suggesting that a similar figure (Figure 12 from the '898 patent application) does not show a phase lock loop or delay lock loop. (*See* CCFF 1335 - 1340).

d. The April 1991 Technical Description Discloses the Rambus Inventions.

633. A still later Rambus technical description was released on April 1, 1991 and was a more complete version with many more technical details. (RX 130; Farmwald, Tr. 8171; Horowitz, Tr. 8538).

Response to Finding No. 633: Complaint Counsel have no response, except to note that Dr. Farmwald testified that RX 130 was a "later version," not that it was "more complete." (Farmwald, Tr. 8171).

634. The April 1, 1991 technical description disclosed dual-edged clocking. The document contains the same figure relating to inputting data on both edges of the clock as in the May 7, 1990 and November 5, 1990 descriptions. (RX 63 at 10; RX 94 at 15; RX 130 at 36; Horowitz, Tr. at 8539).

Response to Finding No. 634: This Proposed finding is misleading in that what is "disclosed" was a series of technical features relating to the Rambus RDRAM interface and architecture which, as stated elsewhere in the document, related to a design with "a small number of high-speed signals that carry all address, data and control information." (RX 130 at 10). As noted elsewhere, an engineer examining the Rambus clocking system would find it different than the system used in JEDEC- compliant DDR SDRAMs. (*See* CCFF 1327 - 1334).

635. The April 1, 1991 technical description disclosed using a phase locked loop on the DRAM. (RX 130 at 56; Horowitz, Tr. 8539).

Response to Finding No. 635: *See* CCRF 634. As noted elsewhere, the specific implementation relating to using a PLL on the unique Rambus clocking system would not be

sufficient to put an engineer on notice that Rambus might have intellectual property on phase lock loops or delay lock loops as used in JEDEC-complaint DDR SDRAMs. (*See* CCFF 1327 - 1340).

636. The April 1, 1991 technical description disclosed programmable latency through the use of a "read delay" or latency register. (RX 130 at 94; Horowitz, Tr. 8539-40).

Response to Finding No. 636: This Proposed finding is misleading because the term "programmable latency" is not used in the document, and the term "delay register" as used in the Rambus RDRAM architecture and interface is not the same as used in a JEDEC SDRAM. (*See* CCFF 1319 - 1326).

637. The April 1, 1991 technical description disclosed variable block size or burst length, with the value in a "count" field representing the number of bytes to be transferred. (RX 130 at 64; Horowitz, Tr. at 8539).

Response to Finding No. 637: This Proposed finding is misleading because the cited passage does not provide information about the extent of the Rambus intellectual property, particularly as relates to programmable burst length as used in JEDEC-compliant SDRAMs. As noted previously, and engineer reviewing information about the Rambus technology would not have reason to conclude it was broad enough to encompass the concept of programmable burst length as used in JEDEC-compliant SDRAMs. (*See generally* CCFF 1309 - 1318)

3. Rambus Disclosed Its Inventions In A Series Of Public Documents.

a. Rambus Disclosed Its Inventions In A Marketing Brochure.

638. In early 1992, Rambus produced and distributed its first marketing brochure about Rambus technology. (RX 2183; Horowitz, Tr. 8547). The 1992 marketing brochure disclosed the four features of Rambus technology at issue here. (Horowitz, Tr. 8547-48).

Response to Finding No. 638: The Proposed finding is misleading to the extent it suggests that the "Rambus technology" or "inventions" disclosed in the cited document extend beyond the RDRAM architecture. As the document states on the very first paragraph of text, "The [Rambus] Channel uses a small number of very high speed signals to carry all address, data and

control information." (RX 2183 at 5). It was this feature that served to distinguish the "revolutionary" Rambus technology from previous generations of DRAMs. (*See generally* CCFF 717 - 724).

639. The 1992 marketing brochure states that the "heart of [the Rambus] Interface is high performance PLL (phase-locked-loop) circuitry which provides the clocks for transmitting and receiving Rambus Channel data." (RX 2183 at 6).

Response to Finding No. 639: *See* CCRF 638. The context of the quoted statement is a description of the Rambus interface; as noted elsewhere, the PLL circuitry used in the Rambus design was not sufficiently similar to that used in JEDEC complaint DDR SDRAMs to put an engineer on notice that Rambus might have intellectual property extending beyond the RDRAM architecture. (*See* CCFF 1335 - 1340).

640. The 1992 marketing brochure also states that there can be "Transfers of 1 to 256 Bytes per Request . . . ." (RX 2183 at 7). This discloses variable burst length, because data transfers could involve a variable amount of data.

Response to Finding No. 640: The Proposed finding is misleading and incomplete in that the remainder of the sentence references a "packet-oriented protocol" that was a unique feature of the Rambus RDRAM as opposed to other RDRAMs. (*See* CCFF 722, 1298 - 1308). Furthermore, there is no record evidence support for the second sentence in the proposed finding. The context of the quoted statement is a discussion of the features and benefits of the Rambus RDRAM and, as noted elsewhere, the variable block size feature was implemented differently than in JEDEC-compliant SDRAMs. (*See* CCFF 1309 - 1318).

641. The 1992 marketing brochure also states that "Data is effectively transferred on both edges of the clock." (RX 2183 at 9). This discloses dual-edge clocking.

Response to Finding No. 641: *See* CCRF 638 - 640. The context of the quoted statement is in the context of the Rambus RDRAM clocking system which, as noted previously, is

different from dual-edge clocking as used in JEDEC-compliant DDR SDRAMs. (*See* CCFF 1327 - 1334). There is no record evidence support for the second sentence of the proposed finding.

642. The 1992 marketing brochure also states that "the Read Data Packet is returned a time ReadDelay after the Request Packet" and that this delay value is "programmed into the configuration registers of all devices during system initialization." (RX 2183 at 11). This discloses programmable latency.

Response to Finding No. 642: *See* CCRF 6318 - 641. Again, the context of the quoted statement is a discussion of the RDRAM interface and its features, and the latency or "delay value" features operated differently than the programable CAS latency feature as used in JEDEC-complaint SDRAMs. (*See* CCFF 1319 - 1326). There is no record evidence support for the second sentence of the proposed finding.

b. Rambus Disclosed Its Inventions In Publications Describing The First Rambus DRAM

643. The first Rambus DRAM was a 4.5 megabit Rambus DRAM produced by Toshiba in the 1991-92 time frame. (Horowitz, Tr. 8548-49).

Response to Finding No. 643: Complaint Counsel have no specific response.

644. A paper about the Toshiba 4.5 megabit Rambus DRAM was presented at the 1992 International Symposium on VLSI Circuits (VLSI Circuits Symposium) and published in the proceedings of that symposium. (RX 301 at 76-77; Horowitz, Tr. 8552-54).

Response to Finding No. 644: Complaint Counsel have no specific response.

645. The VLSI Circuits Symposium is held annually and is one of the top two conferences in the world for circuit designers (Horowitz, Tr. 8552). The "technical program committees" of the Symposium read all the papers submitted and choose the better ones for publication at the conference. (Horowitz, Tr. 8552-53). The technical program committees for the 1992 VLSI Circuits Symposium that selected the paper about the Toshiba 4.5 megabit Rambus DRAM included representatives from IBM, Texas Instruments, Siemens, Sun Microsystems, Intel, Hitachi, Samsung, Matsushita, Mitsubishi, Fujitsu, Sanyo, Oki, and NEC. (RX 301 at 5).

Response to Finding No. 645: Complaint Counsel have no specific response.

646. The paper published in the proceedings of the 1992 VLSI Circuits Symposium about the Toshiba 4.5 megabit Rambus DRAM discusses the four features of Rambus technology at issue in this case. (Horowitz, Tr. 8554). Figure 2 of the paper shows a block size transfer and read latency. (RX 301 at 77; Horowitz, Tr. 8555). Figure 3 of the paper shows double data rate input

receivers. (*Id.*). The paper also states that "[t]o eliminate skew caused by the internal circuitry, the DRAM contains two PLLs." (RX 301 at 76; Horowitz, Tr. 8555).

Response to Finding No. 646: This Finding is misleading because it suggests that these discussions in the context of the RDRAM produced by Toshiba were sufficient to put others on notice of the extent of Rambus intellectual property on these four features. First of all, nothing in the article suggests any intellectual property that might extend beyond the RDRAM architecture, or even if the holder of the intellectual property is Rambus or Toshiba. The cited portions of the document are all in the context of a bus "that carries all the address, control and data to and from the DRAM." (RX 301 at 76, second paragraph of article). As noted previously, the implementation of all of these features in the context of the Rambus RDRAM design was not sufficient to put readers on notice about any intellectual property rights that might extend to the features of programmable CAS latency, programmable burst length, dual-edge clocking and on-chip PLL or DLL as used in JEDEC-compliant SDRAMs. (*See generally* CCFF 1266 - 1350).

647. At the end of the 1992 VLSI Circuits Symposium, the authors of the top papers were invited to provide a longer version to be published in the Journal of Solid State Circuits. (Horowitz, Tr. 8555-56). The Journal of Solid State Circuits is the most widely read journal for circuit designers. (*Id.*). The paper about the Toshiba 4.5 megabit Rambus DRAM was selected, and a longer version of that paper was published in the Journal of Solid State Circuits in April 1993. (RX 385; Horowitz, Tr. 8556).

Response to Finding No. 647: Complaint Counsel have no specific response.

D. Rambus's Inventions Were Discussed In The Press In Early 1992.

648. In connection with the public announcement of Rambus's technology and its business plan in March 1992, Rambus provided information to the press regarding Rambus's inventions, and numerous articles about Rambus appeared. (RX 1446).

Response to Finding No. 648: Complaint Counsel does not disagree that in furtherance of its business plan to promote and license its proprietary RDRAM technology, Rambus discussed its technology and business plan with the press, including in connection with the

various news articles collected as RX1446. The Rambus efforts to promote and license its proprietary technology in the early 1990's are discussed at CCFF 700-709, 714-24, 732-56.

Even a brief perusal of these articles makes clear that their content and timing is directed at the Rambus promotion efforts for the proprietary RDRAM technology. (E.g., RX1446 at 4 (S.F. Chronicle: Rambus "has developed revolutionary memory chip technology"), 6 (San Jose Mercury News: Rambus "has concocted a novel system for speeding memory chips"), 13 (EE Times: Rambus "unveiled a unique 500-MHz 9-bit data channel"), 20 (Electronic News: the "Rambus channel" is "a short and narrow bus in which signals transition every 2 nanoseconds")). The articles contain repeated references to Rambus having negotiated by March 1992 licenses for its RDRAM technology with Fujitsu, NEC and Toshiba. (E.g., RX1446 at 4, 7, 9, 10, 12, 13, 17, 18). These early licenses were part of the Rambus strategy of phased promotion of its proprietary technology, in hopes of developing a base of industry support for its RDRAM technology and preventing the development of competing technologies. (*See* CCFF 736, 740).

Nothing in any of the collected articles remotely suggests the existence of the alternative Rambus business strategy, which consisted of secretly perfecting and later asserting Rambus intellectual property rights against competing technologies, including specifically the JEDEC SDRAM standard that was under development in March 1992. *See* CCFF 757-763, 911-920. By late March 1992, when this collection of press clippings was compiled (RX1446 at 1), Rambus executives had already begun to meet with Rambus patent counsel to discuss the assertion of patent claims against firms that might utilize technologies contained in the SDRAM standard under development. (CCFF 885-892).

649. Many of these articles provided a significant amount of technical detail. For example, an article entitled "Rambus Unveils Revolutionary Memory Interface" in the March 4, 1992 Microprocessor Report describes Rambus's technology in some depth. (RX 1446 at 22-26).

Response to Finding No. 649: Complaint Counsel does not disagree that several of the articles compiled in RX1446 contain technical descriptions of the proprietary RDRAM technology, including the article reproduced at pages 22-26 of that exhibit. As with the promotional efforts and presentations made by Rambus over the course of the 1990's (CCFF 750-56, 1238-59), the technical discussions contained in these articles provide information about the characteristics of the "revolutionary" RDRAM technology. As with the Rambus technical presentations (*id.*), the articles contain no reference whatever to the extent of any claims by Rambus to intellectual property rights in the technical details described, and certainly do not remotely suggest that Rambus believed it owned the rights to the technical details if implemented in any context other than the RDRAM technology that is the subject of the articles. A reasonable reader of such articles would likely come to the same conclusion as numerous witnesses who learned about the Rambus technology through the Rambus technology presentations – that the scope of any Rambus intellectual property rights would extend to the proprietary RDRAM technology described. (*See* CCFF 1244-53). At trial Rambus elicited no testimony whatever from any witness concerning this exhibit to suggest any other conclusion.

650. The March 4, 1992 Microprocessor Report article discloses three of the four features of Rambus technology at issue here, as well as aspects of the fourth.

Response to Finding No. 650: This proposed finding is vague and ambiguous in that it uses the term "discloses" without specifying a precise meaning for the term. For the reasons set forth in CCRF 649 above and CCRF 651-54 below, the referenced article (reproduced at pages 22-26 of RX1446) does not remotely suggest that Rambus believed it owned the rights to the referenced features if implemented in any context other than the proprietary RDRAM technology.

651. The article states: "The Rambus Channel is a 500-Mbyte/s interface operating with a 250-MHz clock and transferring a byte of data on each clock edge." (RX 1446 at 22). This discloses dual-edged clocking.

Response to Finding No. 651: Complaint Counsel agrees that the quoted language from RX1446 could be read to describe dual-edge clocking in the context of the proprietary RDRAM technology. Indeed, the quoted language itself refers to the use of dual edge clocking in the "Rambus Channel," which is described elsewhere in the article as involving a "counter-intuitive" approach utilizing a "narrow bus." (RX1446 at 22). This proposed finding is vague and ambiguous in that it uses the term "discloses" without specifying a precise meaning for the term. The referenced article does not remotely suggest that Rambus has intellectual property rights to the dual-edge clock feature if implemented in any context other than the proprietary RDRAM technology.

652. The article states: "A phase-locked loop on each Rambus device limits clock skew within the chip." (RX 1446 at 23). This discloses on-chip PLL.

Response to Finding No. 652: Complaint Counsel agrees that the quoted language from RX1446 describes the use of on-chip PLL in the context of the proprietary RDRAM technology. Indeed, the quoted language itself refers to the use of PLL on "each Rambus device." This proposed finding is vague and ambiguous in that it uses the term "discloses" without specifying a precise meaning for the term. The referenced article does not remotely suggest that Rambus has intellectual property rights to the on-chip PLL feature if implemented in any context other than the proprietary RDRAM technology.

653. The article states: "The six-byte request packet encodes a 36-bit address, a 4-bit operation code, an 8-bit transfer length count (in bytes). Byte addressing and block sizes of up to 256 bytes are supported." (RX 1446 at 24). This discloses variable burst length.

Response to Finding No. 653: Complaint Counsel agrees that the quoted language from RX1446 could be read to describe the use of variable burst length in the context of the proprietary RDRAM technology. Indeed, the quoted language is extracted from an extensive passage in the article specifically addressing the functioning of "RDRAMs." (RX1446 at 24).

This proposed finding is vague and ambiguous in that it uses the term "discloses" without specifying a precise meaning for the term. The referenced article does not remotely suggest that Rambus has intellectual property rights to the on-chip PLL feature if implemented in any context other than the proprietary RDRAM technology.

654. The article also notes that "control registers" on the DRAM can be used to specify certain parameters. (RX 1446 at 23). This is related to programmable CAS latency which, in SDRAMs, is programmed in a control register called a "mode register" on the DRAM.

Response to Finding No. 654: Complaint Counsel agrees that the quoted language from RX1446 could be read to have some relation to the use of programmable CAS latency in the context of the proprietary RDRAM technology. Indeed, the quoted language is extracted from an extensive passage in the article specifically addressing the functioning of "RDRAMs." (RX1446 at 23). This proposed finding is vague and ambiguous in that it uses the term "related to" without specifying a precise meaning for the term. The referenced article does not remotely suggest that Rambus has intellectual property rights to the programmable CAS latency feature if implemented in any context other than the proprietary RDRAM technology.

1. Rambus's Early Patent Disclosures Gave Notice That Rambus Could Obtain Patents On The Four Technologies.

a. The History of the '898 Application.

655. After the filing of the '898 application, Rambus received an 11-way restriction requirement from the PTO – that is, the Patent Examiner determined that Rambus was claiming 11 distinct categories of inventions in the '898 application. (Nusbaum, Tr. 1510).

Response to Finding No. 655: Complaint Counsel does not disagree. *See* CCFF 729.

656. After receiving the restriction requirement, Rambus elected one group of claims to prosecute in its original application and filed 10 divisional applications to pursue the other groups of claims identified in the restriction requirement. (Nusbaum, Tr. 1511).

Response to Finding No. 656: Complaint Counsel does not disagree. *See* CCFF 729.

657. The patents that Rambus has asserted against DRAM manufacturers have all issued from applications that are continuations or divisionals stemming from the original '898 application and all share a specification with that original application. (Stipulated Patent Tree, attached to Parties' First Set of Stipulations; Nusbaum, Tr. 1513-14).

Response to Finding No. 657: Complaint Counsel does not disagree. *See* CCFF 731.

658. Pursuant to the "written description" requirement for a patent's validity, the PTO determined that the claims of this patents were supported by the specification of the original '898 application, that is, that a person of ordinary skill in the art who was reviewing the '898 application would have understood that Rambus was in possession of the inventions claimed in the later patents as of the April 1990 filing date of the '898 application. *See* Findings ¶¶ 78, 87. Complaint Counsel have not challenged the validity of Rambus's issued patents.

Response to Finding No. 658: Complaint Counsel takes no position on the infringement and validity of those patent that Rambus has asserted against DRAM manufactures. Those questions, on which no court has ruled, are not at issue in this case. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1106 (Fed. Cir. 2003) (remanding case to district court for infringement determination and making no ruling on validity).

The proposed finding does not support the conclusion that Rambus's early patent disclosures, in particular its '703 patent, gave JEDEC notice that Rambus could obtain patents on the four technologies as they are used in the SDRAM and DDR SDRAM standards before claims that Rambus now asserts over those technologies were public. The written description analysis as conducted by a patent examiner or in a validity analysis begins with a drafted claim and looks for support in the specification. (Nusbaum, Tr. 1502). The written description requirement does not require that a person of ordinary skill in the art be able to predict the claims that could potentially come out of a patent specification before those claims are drafted. (Fliesler, Tr. 8903). An engineer or patent lawyer could not have known for certain what claims Rambus would pursue in

the ‘898 family from reading the ‘898 application, regardless of what claims the PTO eventually allowed. (Fliesler, Tr. 8902).

Rambus’s proposed finding RPF 94 explains that even when the written description of a patent application is public, actual knowledge of the pending claims is valuable information. RPF 94. It is valuable because the written description does not provide notice of what will be claimed. (*See*, Fliesler, Tr. 8902).

As fully explained in Complaint Counsel’s proposed findings, Rambus’s early patent disclosures did not, in fact, give notice that Rambus could obtain patents on the four technologies. CCFF 1273-1357.

b. The PCT Application.

659. On April 16, 1991, Rambus filed an international patent application pursuant to the Patent Cooperation Treaty (the “PCT application”). (CX 1454 at 1).

Response to Finding No. 659: Complaint Counsel does not disagree. *See* CCFF 1267.

660. The PCT application is identical in all material respects to the ’898 application. In particular, the PCT application contains the same written description, drawings, and 150 claims as the ’898 application. (CX 1451; CX 1454; Fliesler, Tr. 8811).

Response to Finding No. 660: Complaint Counsel does not disagree. *See* CCFF 1267.

661. The PCT application was published and made publicly available as of October 31, 1991. (CX 1454 at 1; The Parties First Set of Stipulations, Stipulation 8). Several JEDEC members obtained the PCT application in the early 1990's, including Mitsubishi and IBM. (RX 379A at 1; RX 201 at 1).

Response to Finding No. 661: Complaint Counsel does not disagree that the Rambus PCT application was made public on or about the date specified. *See* CCFF 1267. Complaint Counsel also does not disagree that several JEDEC members reviewed the Rambus

PCT application in the early 1990's; however the record shows that JEDEC members concluded that the application did not address the SDRAM standards under development at JEDEC. CCFF 1273-76. On one occasion in May 1992, a JEDEC member announced to the JC 42.3 Committee that he had obtained a copy of the the Rambus international patent application, had read it, and concluded that it should not be a concern for the JEDEC standardization effort. Mr. Crisp, the JEDEC representative for Rambus, was present at the meeting and did not contradict this statement. CCFF 1273-74.

c. The '898 and PCT Applications Disclose Numerous Inventions.

662. The '898 and PCT applications each contain a lengthy disclosure consisting of a 62-page written description, 15 drawings, and 150 claims. (CX 1451, CX 1454).

Response to Finding No. 662: Complaint Counsel does not disagree. *See* CCFF 1283, 1342. Insofar as this or any of the following proposed findings is intended to support the assertion made in the heading above, the proposed finding is vague and ambiguous in that it uses the term "disclose" without specifying a precise meaning for the term.

663. The written description of the '898 and PCT applications contain numerous headings and subheadings, such as "Device Address Mapping," "Bus," "Protocol and Bus Operation," "Retry Format," "Bus Arbitration," "System Configuration/Reset," "ECC," "Low Power 3-D Packaging," "Bus Electrical Description," "Clocking," "Device Interface," "Electrical Interface - Input/Output Circuitry," and "DRAM Column Access Modification." (CX 1451 at 18, 20, 21, 30, 32, 37, 40, 43, 45, 47, 54; CX 1454 at 18, 20, 21, 30, 32, 37, 41, 44, 46, 48, 55).

Response to Finding No. 663: Complaint Counsel does not disagree that the specification portions of the Rambus '898 and PCT patent applications contain the listed headings and subheadings.

664. A person of ordinary skill in the art to which the '898 and PCT applications pertain would have an electrical engineering degree and at least two to three years of experience in designing computer memory circuits. (Nusbaum, Tr. 1613; Fliesler, Tr. 8779-80).

Response to Finding No. 664: Complaint Counsel does not disagree that a person of ordinary skill in the art pertinent to these applications would be someone with an engineering

background with knowledge of electrical engineering and knowledge of computer systems or random access memory, in the field of DRAM memory. (Nusbaum, Tr. 1613).

665. A person of ordinary skill in the art, an experienced DRAM designer, or a patent lawyer reviewing the '898 application or PCT application would not have thought that the inventions described in them were limited to a particular bus architecture. (Fliesler, Tr. 8788, 8811; Geilhufe, Tr. 9559). Instead, such individuals would recognize that although the applications describe how an entire system is to be put together, they also describe numerous technical features that can be used independently of one another and of the system. (Fliesler, Tr. 8788-89).

Response to Finding No. 665: This proposed finding is contrary to the weight of the evidence. In fact, the record shows that on several occasions persons with engineering backgrounds, knowledge of computer systems and DRAM memory, and substantial practical familiarity with the design of DRAM memory, reviewed the substance of the Rambus '898 or PCT patent applications and concluded that the applications described the proprietary Rambus RDRAM technology.

One of these occasions was the review by the Rambus JEDEC representative Richard Crisp, who at the time he first read the original '898 patent application in the early 1990's and believed that it was intended to describe the RDRAM system invention, and that it was limited to the proprietary RDRAM technology. (Crisp, Tr. 2927-28; CCFF 727). (Crisp subsequently came to believe that the '898 application could be amended to add claims covering technologies used in other architectures, including SDRAMs, thorough his conversations with patent attorney Lester Vincent and others. (Crisp, Tr. 2928-29)). Another occasion was the review by Howard Sussman, the experienced DRAM memory designer, who in 1992 obtained a copy of the Rambus European patent application and concluded after reviewing it that the patent pertained to the proprietary RDRAM technology and did not pose a problem for the SDRAM standardization activity at JEDEC. (CCFF 1273-1274). When Mr. Sussman announced this conclusion at a JEDEC meeting, Mr. Crisp of Rambus was present and did not contradict the statement. (*Id.*). Another occasion

was the review by the experienced DRAM memory designer Willi Meyer of Infineon, who in 1992 had concerns about rumors of possible Rambus patents on dual-bank technology; after reviewing the Rambus European patent application and witnessing Mr. Crisp's disclosure of the Rambus '703 patent at JEDEC, Mr. Meyer wrote his colleagues in late 1993 that the SDRAM standard adopted by JEDEC had avoided patented technology. (CCFF 1275). Another occasion was the review of Rambus patents conducted by knowledgeable Micron employees in 1995 in connection with the possible licensing by Micron of RDRAM technology. (CCFF 1276). After this review, Micron concluded that the Rambus patents applied specifically to the RDRAM bus architecture. (*Id.*).

In fact, the content of the specification contained in the '898 and PCT applications contains numerous specific terms describing a technology that is different in multiple respects from the typical synchronous DRAM memory architecture, and from the memory architecture reflected in the JEDEC SDRAM and DDR standards. The specification describes a narrow, multiplexed bus structure (CCFF 1284-97) that uses packetized data transmission. (CCFF 1298-1308). Although the specification describes numerous technical features, each of those features is significantly different than those used in SDRAM technology. The specification describes a system with variable block size that is variable by packet and operates on a narrow, multiplexed bus, rather than one like that in the SDRAM technology with a burst length set once, on chip start-up. (CCFF 1309-18). It describes a system with access time that is variable by packet and operates on a narrow, multiplexed bus, rather than one like that in the SDRAM technology with access time set once, on chip start-up. (CCFF 1319-26). It describes a U-shaped clocking scheme that uses one wire to transmit two clock signals, rather than two wires to transmit one clock signal, as implemented in the later DDR standard, and differs in other respects from the standard technologies. (CCFF 1327-40). It neither describes nor illustrates a delay-locked loop circuit or a phase-locked loop circuit. (CCFF 1335-40).

Mr. Fliesler's testimony to the contrary is unreliable because he lacks the expertise and experience to conclude what a JEDEC member, an experienced DRAM design engineer, would have concluded from a review of the PCT application. Unlike Professor Jacob, Mr. Fliesler is an attorney, and not a person skilled in the art of DRAM design and architecture. (Fliesler, Tr. 8867-69, 8781). Even in his work as a patent attorney, Mr. Flielser has had minimal exposure to technical DRAM issues. (Fliesler, Tr. 8782). Moreover, Mr. Fliesler did not discuss his understanding of what the PCT application discloses with any technical experts. (Fliesler, Tr. 8783, 8905).

Mr. Guilhufe's testimony to the contrary is also unreliable because he lacks the expertise and experience to conclude what a JEDEC member, an experienced DRAM design engineer, would have concluded from a review of the PCT application in the early to mid-1990s. During the relevant time period, he was not involved in or supervising the design of DRAMs. Geilhufe, Tr. 9627-28. The last time Mr. Geilhufe formally contributed to a DRAM design was sometime in the mid to late 1980s. (Geilhufe, Tr. 9625-26). His last hands-on DRAM design experience was in 1978. (Geilhufe, Tr. 9626).

666. Indeed, as discussed further below, Mitsubishi engineers reviewed the PCT application in 1993 and did, in fact, recognize that the various innovations described therein were not limited to a particular bus architecture and could be used independently of one another. *See* Findings ¶¶ 669-671.

Response to Finding No. 666: *See* CCRF 669-71.

667. The '898 and PCT applications themselves note that, although a preferred implementation of the invention contains 8 bus data lines, "[p]ersons skilled in the art will recognize that 16 bus data lines or other numbers of bus data lines can be used to implement the teaching of this invention." (CX 1451 at 10; CX 1454 at 10). A person of ordinary skill in the art would recognize from this clear statement alone that the Rambus inventions were not limited to a particular "narrow" bus.

Response to Finding No. 667: Complaint Counsel agree that the Rambus '898 and PCT applications contain the language quoted in the first sentence of this proposed finding.

Insofar as the second sentence of the proposed finding is intended to suggest that the applications describe features without regard to whether the bus is narrow or wide, the finding is incomplete, inaccurate and misleading. A more complete quotation of the paragraph in which the cited language appears, states:

> The new bus includes clock signals, power and multiplexed address, data and control signals. In a preferred implementation, 8 bus data lines and an AddressValid bus line carry address, data and control information for memory address up to 40 bits wide. Persons skilled in the art will recognize that 16 bus data lines or other numbers of bus data lines can be used to implement the teaching of this invention. The new bus is used to connect elements such as memory, peripheral, switch and processing units.

(CX1451 at 9-10; CX1454 at 9-10). As is clear from this more complete quotation, a bus having 16 or more lines, as described here, will nonetheless be a "new bus" having "multiplexed address, data and control signals." (CX1451 at 10; CX1454 at 10). The characteristic of a multiplexed bus is fundamentally different than the bus used in an SDRAM, which has dedicated address, data and control lines. CCFF 1295.

In addition, the language quoted in this proposed finding follows other language in the immediately preceding paragraph of the applications which states that an essential characteristic of the Rambus invention is the use of a bus that "has substantially fewer bus lines than the number of bits in a single address." (CX1451 at 9, CX1454 at 9). This characteristic is fundamentally different from the broad-bus architecture of the typical synchronous DRAM , which utilizes 100 or more parallel bus lines to communicate between the memory chip and the controller, each bus line dedicated to a distinct address, data or control signal. (*See* CCFF 718, 1292). Such a broad bus architecture necessarily requires at least as many dedicated bus lines as the number of bits in a single address. While the quoted language in the proposed finding suggests that there may be some flexibility in how narrow the Rambus bus may be (i.e. 8 or 16 or some other small number of bus

lines), the quoted language in no way can be read to suggest that the applications describe features implemented in the context of a broad-bus synchronous DRAM with dedicated address, control and data lines. (*See* CCFF 1284-97).

668. It was Dr. Horowitz's understanding when the patent application was filed that the various solutions to problems described in the application could be used independently of one another. Thus, if one did not want quite the level of performance that Drs. Farmwald and Horowitz envisioned, one could use only a subset of the techniques described in the patent application. (Horowitz, Tr. 8514-15).

Response to Finding No. 668: Insofar as the proposed finding is intended to suggest anything about the content of the Rambus patent applications, it is inaccurate and misleading. The cited testimony of Dr. Horowitz was in response to a general question concerning his understanding of the techniques for solving the technical problems that his invention was intended to address. (Horowitz, Tr. 8514-15). The testimony was not addressed to any specific language contained in the patent applications, and does not in any way support any implication that the Rambus patent applications placed others in the industry on notice that Rambus claimed intellectual property rights to the various features in any context but the narrow bus architecture described in the '898 and PCT patent applications. Moreover, the proposed finding ignores the overwhelming record evidence that Rambus, over the course of nearly a decade, sought to and did effectively conceal the scope of its intellectual property claims from the memory chip industry. (CCFF 1238-76, 1676-1700). There is no record evidence to suggest that during the period of this concealment Dr. Horowitz communicated to anyone outside Rambus the view that the Rambus invention was the basis for intellectual property claims against the JEDEC standard technologies.

669. Dr. Farmwald never thought of his ideas as implementing a "narrow" bus. (Farmwald, Tr. 8143). Rambus originally used a 9-bit wide bus because that corresponded to the number of pins that could fit on the edges of the chips that existed at the time; later Rambus used wider buses because more pins could be placed on the chip. (Farmwald, Tr. 8143-44). While some of the inventions of Drs. Farmwald and Horowitz might enable narrower busses to work better, the inventions are not specific to a particular bus width. (Farmwald, Tr. 8144).

Response to Finding No. 669: Insofar as the proposed finding is intended to suggest anything about the content of the Rambus patent applications, it is inaccurate and misleading. The cited testimony of Dr. Farmwald was not addressed to any specific language contained in the Rambus patent applications (Tr. 8143-44), and does not in any way support any implication that the Rambus patent applications placed others in the industry on notice that Rambus claimed intellectual property rights to the various features in any context but the narrow bus architecture described in the '898 and PCT patent applications. Moreover, the proposed finding ignores the overwhelming record evidence that Rambus, over the course of nearly a decade, sought to and did effectively conceal the scope of its intellectual property claims from the memory chip industry. (CCFF 1238-76, 1676-1700). There is no record evidence to suggest that during the period of this concealment Dr. Farmwald communicated to anyone outside Rambus the view that the Rambus invention was the basis for intellectual property claims against the JEDEC standard technologies.

670. As discussed below, Mitsubishi engineers who reviewed the PCT application came to the conclusion that the various technologies disclosed therein could be used independently of one another and independently of the bus architectures described in the application.

Response to Finding No. 670: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

671. A March 12, 1993 Mitsubishi memorandum begins by stating that "A need has arisen to evaluate in detail all of the claims in a patent being applied for by Rambus (1 patent, a total number of claims is 150)." (RX 2214A at 1). The memorandum goes on to list guidelines for this evaluation, including "1) Do not discuss Rambus interface. 2) Determine whether or not any other areas contain technologies that will be important in increasing memory speed in the future." (RX 2214A at 1).

Response to Finding No. 671: Complaint Counsel agrees that the cited exhibit, which contains a proffered translation of an original Japanese language document, contains the quoted language. At trial Rambus elicited no testimony whatever from any witness concerning the preparation of the translation, the preparation of the original document or the subject matter of the document.

672. A June 10, 1993 Mitsubishi document with the heading "RAMBUS Patent (summary of responses)" states: "In addition to the technologies of narrower bus width and communication by protocol that are described above, the RAMBUS patent includes a variety of requirements such as memory system configuration, packaging method, and device configuration, and it can be achieved through a combination of these factors." (RX 406 at 4). The document continues: "The individual technologies that appear in the RAMBUS patent will be used independently in the future." (RX 406 at 4).

Response to Finding No. 672: Complaint Counsel agrees that the cited exhibit, which contains a proffered translation of an original Japanese language document, contains the quoted language. At trial Rambus elicited no testimony whatever from any witness concerning the preparation of the translation, the preparation of the original document or the subject matter of the document.

Insofar as the proposed finding is intended to suggest that the that the Rambus '898 and PCT patent applications placed others in the industry on notice that Rambus claimed intellectual property rights to various features in contexts other than the narrow bus architecture described in those patent applications, the finding is inaccurate, misleading and contrary to the weight of the evidence. As noted above, numerous knowledgeable persons with background and direct involvement in the memory chip industry reviewed these Rambus patent applications and concluded exactly the contrary – that the applications pertained to the proprietary Rambus RDRAM technology. (*See* CCRF 665). Moreover, Rambus, over the course of nearly a decade, sought to and did effectively conceal the scope of its intellectual property claims from the memory chip industry. (CCFF 1238-76, 1676-1700).

Even taking at face value the language of the cited translation, however, the document contradicts the view that its author was placed on notice by the PCT application of the scope of Rambus intellectual property claims being pursued in other patent applications. While the document may be read as reflecting a suspicion that Rambus could be pursuing other patents on features independently of its narrow bus architecture, the document states (accurately) that to evaluate such intellectual property claims, it would be necessary to examine the "patent claims to determine whether individual technologies used independently will infringe on the RAMBUS patent." (RX0406 at 4). Indeed, as a Rambus expert witness testified at trial, an engineer or patent lawyer could not have known for certain what claims Rambus would pursue in the '898 family from reading the '898 application, or the identical PCT application. (Fliesler, Tr. 8902). In short, even if the author of the Mitsubishi document suspected that other claims were being pursued independently, neither he nor anyone else other than Rambus and its lawyers could know on the basis of the PCT application alone the scope of the additional Rambus claims.

d. The '898 and PCT Applications Disclose Programmable Latency.

673. The '898 application and the PCT application describe access time registers that store latency, that is the amount of time between receiving a request and driving data onto the bus in response to that request. (CX 1451 at 16, 23; CX 1454 at 16, 23; Jacob, Tr. 5481). The applications state that "Each slave may have one or several access-time registers," where "slave" can refer to a DRAM. (CX 1451 at 16; CX 1454 at 16; Jacob, Tr. 5649).

Response to Finding No. 673: Complaint Counsel agrees that the Rambus '898 and PCT applications include descriptions of means for programming access time. (*See* CCFF 1319-26). Complaint Counsel agrees that the applications contain the language quoted in the second sentence of this proposed finding.

The proposed finding is incomplete and misleading because it fails to state that the '898 application does not describe the use of access time registers in any context other than that of a narrow, multiplexed bus operating in a packetized system. (Jacob, Tr. 5476-77; Fliesler, Tr. 8915;

CCFF 1324). The description of access time registers beginning at page 21 of the '898 application (CX1451 at 23), which the proposed finding cites, includes a description of Figure 4. Figure 4 illustrates a "packet" of information traveling over nine bus lines, each of which is multiplexed to carry address, data and control information. (CX1451 at 23, 131; Fliesler, Tr. 8910-12). Figure 4 illustrates that each packet carries access type information that controls the timing of the response to the request packet. (CX1451 at 25,131; Fliesler, Tr. 8912-13)

Insofar as this or any of the following proposed findings is intended to support the assertion made in the heading above, the proposed finding is vague and ambiguous in that it uses the term "disclose" without specifying a precise meaning for the term.

674. In common use, programmable CAS latency in the mode register of an SDRAM is set at initialization. (Jacob, Tr. 5648-49). Likewise, the '898 application and PCT application state with respect to the access time registers (and other registers): "Most of these registers can be modified and preferably are set as part of an initialization sequence . . . ." (CX 1451 at 16; CX 1454 at 16).

Response to Finding No. 674: Complaint Counsel agrees that in SDRAM the CAS latency is set at initialization, as set forth in the first sentence of this proposed finding. However, to the extent that the second sentence of this proposed finding is intended to suggest that the programmable CAS latency feature described in the Rambus '898 and PCT applications is equivalent to that in SDRAM, the proposed finding is inaccurate and misleading.

In a JEDEC SDRAM, the CAS latency is programed at system start-up. The CAS latency is not changed during operation. The CAS latency cannot be changed with each request. (JX0056 at 114; Jacob, Tr. 5483; Fliesler, Tr. 8920). As described in the '898 specification and illustrated in Figure 4, however, each request packet contains information that specifies the access time. (CX1451 at 23, 25, 29, 131; Jacob, Tr. 5482). This allows the bus master to efficiently change the access time with each new request packet. (CX1451 at 29, Jacob, Tr. 5483).

The implementation of the access time feature described in the ‘898 specification is inherently tied to narrow, multiplexed bus and packetized system described in the specification. (Jacob, Tr. 5483-84). By allowing changes to the access time on a request-by-request basis, the system described in the ‘898 specification resolves inefficiencies that result from the use of a narrow, multiplexed, packetized bus in which address and control information must share lines with data. (Jacob, Tr. 5484). The specification explains that the access time allows the shared bus to be used for other requests during the access time: “The bus to be used in the intervening bus cycles [between request and response] by the same or other masters for additional requests or brief bus accesses. Thus, multiple, independent accesses are permitted, allowing maximum utilization of the bus for transfer of short blocks of data.” (CX1451 at 17-18). By contrast, in a JEDEC SDRAM, programmable CAS latency is used as a convenience to allow parts that have different performance to exist in the same system. (Jacob, Tr. 5484).

675. A person of ordinary skill in the art reviewing the ’898 application or PCT application would understand that CAS latency on an SDRAM could be programmed using access time registers like those described therein. (Fliesler, Tr. 8784-85, 8791-93, 8811, 8904).

Response to Finding No. 675: This proposed finding is contrary to the evidence, inaccurate and misleading. The ‘898 application does not describe the use of access time registers in any context other than that of a narrow, multiplexed bus operating in a packetized system. (Jacob, Tr. 5476-77; Fliesler, Tr. 8915; CCFF 1324). Figure 4 illustrates that each packet carries access type information over relatively few multiplexed bus lines that controls the timing of the response to the request packet. (CX1451 at 23, 25,131; Fliesler, Tr. 8912-13)

As described in CCRF 674 and CCFF 1319-25, the function of the programmable CAS latency feature as described in the Rambus ‘898 and PCT applications differs significantly from that of the SDRAM technology. Because of the difference between the implementation and function of access time in the ‘898 specification and programable CAS latency as used in the

JEDEC SDRAM standard, an engineer reading the '898 application in the early to mid-1990s would not have understood that Rambus might obtain patent rights over programmable CAS latency as that feature was used in the JEDEC SDRAM standard. (Jacob, Tr. 5484-85).

Mr. Fliesler's testimony to the contrary is unreliable because he lacks the expertise and experience to conclude what a JEDEC member, an experienced DRAM design engineer, would have concluded from a review of the PCT application. *See* CCRF 665.

676. Indeed, Mitsubishi engineers who reviewed the PCT application recognized the correspondence between the access time registers in the PCT application and programmable CAS latency in SDRAMs. Thus, a Mitsubishi document headed "Assessment of Rambus Patents (Second Half) states next to the numbers 95, 97 and 103: "Modifiable Access Time Register (Similar to SDRAM latency control)." (RX 2213A at 25, 27). Claim 103 of the PCT application (and '898 application) is directed at a "modifiable access-time register." (CX 1454 at 105). Thus, Mitsubishi recognized that the PCT application and, in particular, Claim 103 of that application, related to the sort of mode register used to store a latency value in SDRAMs.

Response to Finding No. 676: Insofar as this proposed finding asserts that Mitsubishi engineers "recognized the correspondence" between the PCT application and SDRAMs, the proposed finding is vague and ambiguous in that it uses the quoted language without specifying a precise meaning. The finding cites no credible record support for the proposition that Mitsubishi engineers in fact interpreted the PCT application in the fashion described.

The trial transcript contains no reference to Rambus offering or the ALJ admitting the exhibit numbered RX2213A, consisting of 27 pages of largely handwritten Japanese, of which only a small portion apparently was translated. There was admitted over Complaint Counsel's objection the five-page exhibit RX2213 (Tr. 1660). However, the latter document, which includes a proffered translation of an original handwritten Japanese language document, does not contain the quoted sentence fragment referred to in the second sentence of this proposed finding. Complaint Counsel notes, moreover, that both the admitted and the proffered translations of handwritten Japanese contained in RX2213 and 2213A contain multiple notations apparently by the translator

stating "illegible" and "guess" with respect to the translation of the original handwritten Japanese. Neither translation appears to be a translation of the entire original document. Neither translation contains any indication of the name or position of the person or persons who prepared the document. At trial Rambus elicited no testimony whatever from any witness concerning the preparation of the translation, the preparation of the original document or the subject matter of the document, other than to offer the same interpretation of the document that it offers here as a hypothetical question in the cross-examination of Mr. Nusbaum. (Tr. 1650-51).

The proposed finding is incomplete and misleading to the extent that it suggests that claim 103 of the PCT application is directed only to a "modifiable access-time register." Claim 103 also contains a limitation reciting a bus having "substantially fewer bus lines than the number of bits in a single address." (CX1451 at 104). Because SDRAMs lack this limitation, claim 103 is not applicable to them. CCFF 1345.

677. In a claim-by-claim analysis of the PCT application produced by Mitsubishi, a marginal note identifies claim 103 of the application as relating to "latency" and "SDRAM." (RX 2213A at 7). The analysis further indicates that Mitsubishi determined that this claim relating to latency in SDRAMs was particularly important, for Claim 103 was given a grade of "A." (*Id.*). A later page of the document explains that an "A" grade means that a technology is "important for increasing DRAM speed. . . ." (RX 2213A at 27).

Response to Finding No. 677: The proposed finding is without credible record support for the proposition that Mitsubishi engineers interpreted the PCT application in the fashion described. Exhibit RX2213A was neither offered nor admitted in evidence at trial, and does not provide credible support for the proposition asserted. *See* CCRF 676. The admitted exhibit RX2213 (Tr. 1660), does not contain the referenced language.

e. The '898 and PCT Applications Disclose Variable Burst Length.

678. The '898 application and the PCT application describe varying the "block size," that is the amount of data transmitted in response or received in response to a request. (CX 1451 at 29-30; CX 1454 at 29-30; Jacob, Tr. 5477-78). The applications each state that "BlockSize [0:3] specifies the size of the data block transfer." (CX 1451 at 29; CX 1454 at 29). The applications

each contain a table showing the "Number of Bytes in Block" corresponding to the value in the "BlockSize" field. (CX 1451 at 30; CX 1454 at 30).

Response to Finding No. 678: Complaint Counsel agrees that the Rambus '898 and PCT applications contain the language quoted in this proposed finding.

The proposed finding is incomplete and misleading because it fails to state that the '898 application does not describe the use of variable block size in any context other than that of a narrow, multiplexed bus operating in a packetized system. (Jacob, Tr. 5478; CCFF 1316). The reference to "BlockSize [0:3]" at page 27 of the '898 application (CX1451 at 29), which the proposed finding cites, describe bits in the multiplexed, narrow bus, request packet as illustrated in Figure 4. (CX1451 at 29-30, 131; Fliesler, Tr. 8918-19). Figure 4 illustrates that each packet carries block size information. (CX1451 at 29-30,131; Fliesler, Tr. 8919).

Insofar as this or any of the following proposed findings is intended to support the assertion made in the heading above, the proposed finding is vague and ambiguous in that it uses the term "disclose" without specifying a precise meaning for the term.

679. "Burst length" as the term is used in SDRAMs, refers to the amount of data to be transferred per read or write transaction. (Rhoden, Tr. 379-80; Jacob, Tr. 5396-97.) Likewise, "block size," as used in Rambus's patents encodes the amount of data to be transferred per read or write transaction. (Jacob, Tr. 5477.) The two terms describe the same function and are used interchangably. (Horowitz, Tr. 8661-62; Geilhufe, Tr. 9643.)

Response to Finding No. 679: Complaint Counsel agrees that the Rambus '898 and PCT applications include descriptions of means for variable block size. (*See* CCFF 1309-18). However, to the extent that the last sentence of this proposed finding is intended to suggest that the block size feature described in the Rambus '898 and PCT applications is equivalent to that the programmable burst length function in SDRAM, the proposed finding is inaccurate and misleading.

In a JEDEC-compliant SDRAM, the burst length feature is programmed during initialization. (JX0056 at 114; Fliesler, Tr. 8920). The burst length is typically set once at system start-up and never changed again. The burst length cannot be easily and efficiently changed with each new request. (Jacob, Tr. 5479). The JEDEC SDRAM standard requires only two possible values for the burst length, four and eight. (JX0056 at 114).

In contrast, The '898 specification describes the operation of the block size feature at pages 27 and 28. (CX1451 at 29-30). This portion of the specification includes a table illustrating that the block size can be varied from 0 to 1024 bytes. (CX1451 at 30; Jacob, Tr. 5477-78). Mr. Guilhufe's statement that the block size feature of the '898 application and the burst length feature of the an SDRAM "generate the same result in terms of the number of bits that get either written or read" is incorrect. (Guilhufe, Tr. 9649-50; JX0056 at 114; CX1451 at 30). The last four bits of information transmitted in the sixth bus cycle shown in the packet of Figure 4 (CX1451 at 131) in the '898 specification give block size information. The block size information specifies the size of the data block to be transferred. (CX1451 at 29-30, 131; Jacob, Tr. 5475-77; Fliesler, Tr. 8918). Because, in the system described in the '898 specification, the block size information is transmitted with each request packet, the block size information can be easily and efficiently changed with each new request. (Jacob, Tr. 5479; Fliesler, Tr. 8919).

The variable block size feature described in the '898 specification addresses a scheduling problem inherent in the narrow, multiplexed, packetized bus system of the '898 specification. An inefficiency results from the data and address information sharing relatively few bus lines. The variable block size feature increases efficiency by maximizing the amount of data that can be transferred in response to a request as needed. (Jacob, Tr. 5479-80). The description and use of the variable block size feature described in the '898 specification in inherently tied to the narrow, multiplexed bus architecture and packetized system. (Jacob, Tr. 5479-81).

In a JEDEC-compliant SDRAM, the programmable burst length feature is present as a convenience. It is not needed to address the bus scheduling and inefficiency concerns generated by the use of a narrow, multiplexed bus. (Jacob, Tr. 5480). The '898 specification describes the use of a variable block size feature only in the context of a narrow, multiplexed bus architecture and a packetized system. (Jacob, Tr. 5478). The '898 specification does not describe the use of a variable block size feature in any other context, including in the context of a DRAM generally. (Jacob, Tr. 5478).

To the extent that Mr. Guilhufe testified to the contrary, his testimony is unreliable because he lacks the expertise and experience to draw conclusions concerning what a DRAM engineer would understand from reading the '898 application. (CCRF 665)

680. A person of ordinary skill in the art reviewing the '898 application or PCT application would understand that variable burst length is disclosed in it. (Fliesler, Tr. 8784-85, 8794-95, 8811, 8904-05).

Response to Finding No. 680: This proposed finding is contrary to the evidence, inaccurate and misleading. As described in CCRF 679 and CCFF 1309-18, the function of the variable block size feature as described in the Rambus '898 and PCT applications differs significantly from the programmable burst length feature of SDRAM technology. An engineer reading the '898 specification in the early to mid-1990s would not have thought that Rambus could obtain patent rights over the programmable burst length feature as it is used in JEDEC SDRAM due to the difference between the JEDEC system and the system described in the '898 specification. (Jacob, Tr. 5480-81).

To the extent that Mr. Fliesler testified to the contrary, his testimony is unreliable because he lacks the expertise and experience to draw conclusions concerning what a DRAM engineer would understand from reading the '898 application. (CCRF 665)

f. The '898 and PCT Applications Disclose Dual-Edge Clocking.

681. The '898 and PCT applications state: "Clock distribution problems can be further reduced by using a bus clock and device clock rate equal to the bus cycle data rate divided by two, that is, the bus clock period is twice the bus cycle period. Thus a 500 MHz bus preferably uses a 250 MHz clock rate." (CX 1451 at 49; CX 1454 at 50). Since the clock rate is half the data rate on the bus, both edges of the clock are used to transmit data. (Fliesler, Tr. 8801-02).

Response to Finding No. 681: Complaint Counsel agrees that the Rambus '898 and PCT applications contain the quoted language. However, the proposed finding is incomplete and misleading because it fails to state that the '898 application describes on a "U-shaped" clocking scheme that uses an early clock and a late clock signal to generate an imaginary mid-point clock signal. (CCFF 1327-31). The quoted statement regarding the "clock rate" and "both edges of the clock" is part of a section with the heading "Clocking" that begins at page 46 of the specification (CX1451 at 47) and provides a detailed explanation of Figures 8a and 8b that illustrates the "U-shaped" clocking scheme that generates the imaginary, mid-point clock signal. (CX1451 at 47-49, 145; Jacob, Tr. 5485-86; Fliesler 8923-26).

Insofar as this or any of the following proposed findings is intended to support the assertion made in the heading above, the proposed finding is vague and ambiguous in that it uses the term "disclose" without specifying a precise meaning for the term.

682. Figure 10 in the '898 and PCT applications shows two input receivers clocked by "clock" and "clock bar" as in the Rambus technical descriptions. (CX 1451 at 147; CX 1454 at 148; Fliesler, Tr. 8799). Since "clock bar" is high when "clock" is low, and vice versa, data is input on both the rising and falling edges of clock. (Fliesler, Tr. 8799-8800).

Response to Finding No. 682: The proposed finding is incomplete and misleading. The circuitry illustrated in Figure 10 uses the internal clock, labeled 73 and its complement, labeled 74 to drive data input. (CX1451 at 54-55, 147). Internal clock 73 in Figure 10 is the imaginary, mid-point clock generated by the U-shaped clocking scheme illustrated in Figure 8a. (*Id.*; Fliesler, Tr. 8922-24). The imaginary mid-point clock is not in synch with any external

clock. (CCFF 1330). Data is input only on the rising and falling edge of the imaginary mid-point clock, internal clock 73. (CX1451 at 55; CCFF 1331).

683. Figure 13 in the '898 and PCT applications shows a timing diagram with data being input, as indicated by the arrows along the bottom of the figure, on both the rising and falling edges of the clock. (CX 1451 at 149; CX 1454 at 150). Howard Sussman, the JEDEC representative for Sanyo and formerly the JEDEC representative of NEC, testified that Figure 13 of the PCT application shows "input being sampled on the high and low edge of the clock" and that is "double data rate input." (Sussman, Tr. 1322, 1467-68).

Response to Finding No. 683: The proposed finding is incomplete and misleading. The timing diagram illustrated in Figure 13 shows data being input only on the rising and falling edges of the internal clock, labeled 73. (CX1451 at 58-59, 149; CCFF 1330). Internal clock 73 is the imaginary, mid-point clock generated by the U-shaped clocking scheme illustrated in Figure 8a. (*Id.*; Fliesler, Tr. 8921-25). The imaginary mid-point clock is not in synch with any external clock. (CCFF 1330).

684. A person of ordinary skill in the art reviewing the '898 application or PCT application would understand that dual edge clocking is disclosed in it. (CX 1451 at 49, 147, 149; CX 1454 at 50, 148, 150; Sussman, Tr. 1465-68; Fliesler, Tr. 8784-85, 8795, 8798-802, 8811, 8905).

Response to Finding No. 684: The proposed finding is vague and ambiguous in that it uses the term "disclose" without specifying a precise meaning for the term. Insofar as the proposed finding is intended to suggest that an engineer reading the '898 patent application during the 1990s would have thought that Rambus could obtain patent rights over the dual-edged clocking feature as it was proposed for and used in the JEDEC DDR SDRAM standard, the finding is inaccurate and misleading because it ignores the substantial difference between the two clocking schemes. (Jacob, Tr. 5493).

According to the "Brief Description of the Drawings" section of the '898 specification, "Figures 8a and 8b show the connection and timing between bus clocks and devices on the bus." (CX1451 at 12). Figure 8a (CX1451 at 145) depicts the U-shaped clock organization described in

the specification at pages 46-48. (CX1451 at 47-49, 145; Jacob, Tr. 5485). In Figure 8a (CX1451 at 145), the clock (labeled CLK) sends a clock signal, clock 1, along a wire. Each chip in the system connects to the wire and receives an "early bus clock signal." At the end of the system, the clock wire turns, are returns to the clock. On the return, the wire transmits the clock 2 signal to each chip, which receives a "late clock signal. (CX1451 at 47-48; Jacob, Tr. 5485-86).

In the clocking system described in the '898 specification, each DRAM has circuitry that synthesizes an internal, midpoint clock signal from the early clock and the late clock signals. (CX1451 at 48-49; Jacob, Tr. 5467-69; *see* DX0096). Figure 13 of the '898 specification is a timing diagram showing the early clock, late clock and internal clock signal that represents the time average, or midpoint, between the early and late clock. The internal midpoint clock is not in synch with either of the external clocks (early and late clock). (CX1451 at 149; Jacob, Tr. 5491; Fliesler, Tr. 8922). In the clocking scheme described in the '898 specification, a DRAM latches data in sync with the internal, time average, midpoint, clock and not any external clock. (CX1451 at 149; Jacob, Tr. 5492).

By contrast, A JEDEC-compliant DDR SDRAM does not generate an internal, time average, midpoint clock from external clock signals. (Jacob, Tr. 5492-93). A JEDEC-compliant DDR SDRAM latches (inputs) data in sync with an external clock, DQS. (Jacob, Tr. 5493; JX0057 at 32). A JEDEC-compliant DDR SDRAM outputs data in sync with the external clock signals, CLK and CLK bar. (Jacob, Tr. 5557-60; 5493, JX0057 at 32).

The clocking scheme described in the '898 application differs from the clocking scheme used in the JEDEC DDR SDRAM standard because the application's clocking scheme uses one wire to transmit two clock signals (the early and late signals) whereas the standard uses two wires (clock and clock bar) to transmit one, differential clock signal. (Jacob, Tr. 5492-93; JX0057). A differential clock signal, consisting of the signal and its inverse, is, by definition, one clock signal.

(Jacob, Tr. 5493). An engineer reading the '898 patent application during the 1990s would not have thought that Rambus could obtain patent rights over the dual-edged clocking feature as it was proposed for and used in the JEDEC DDR SDRAM standard because of the difference between the two clocking schemes. (Jacob, Tr. 5493).

Mr. Fliesler's testimony to the contrary is not reliable because he has no DRAM engineering experience or expertise. (CCRF 665)

g. <u>The '898 and PCT Applications Disclose On-Chip DLL</u>.

685. Figure 12 of the applications shows variable delay circuitry and a feedback loop. (CX 1451 at 148; CX 1454 at 149; Jacob, Tr. 5649-50). The figure would be recognized by an electrical engineer as containing a DLL. (Geilhufe, Tr. 9656).

<u>Response to Finding No. 685</u>: This proposed finding is contrary to the evidence, inaccurate and misleading. Insofar as this or any of the following proposed findings is intended to support the assertion made in the heading above, the proposed finding is vague and ambiguous in that it uses the term "disclose" without specifying a precise meaning for the term.

Figure 12 does not show a delay lock loop (DLL). (Jacob, Tr. 5488). A comparison of a DLL circuit and the circuit of Figure 12 indicates that they have different structures. (Jacob, Tr. 5488-89, *see* DX0097). The circuit of Figure 12 performs a different function than a DLL. The circuit of Figure 12 uses the early clock signal and the late clock signal of the "U-shaped" clock shown in figure 8a to generate the internal clock signal, labeled 73, that is the midpoint, time-average of the two original clock signals. (CX1451 at 58, 137; Fliesler, Tr. 8926-27; CCFF 1336). A DLL delays one input signal so that it will be synchronized with a second signal. (Jacob, Tr. 5488-89). The '898 application never refers to a delay-locked loop or DLL. (Jacob, Tr. 5489-90; Geilhufe, Tr. 9663).

Mr. Geilhufe's testimony that Figure 12 shows a DLL is unreliable because he lacks the expertise and experience to draw conclusions concerning what a DRAM engineer would

understand from reading the '898 application. (CCRF 665). Moreover, Mr. Guilhufe incorrectly believed that Geilhufe that the circuit of Figure 12 aligned one clock with another clock, which is the function of a DLL. (Geilhufe, Tr. 9657-58). This is incorrect. As Mr. Fliesler admitted, the only output of the circuit shown in Figure 12 is internal clock 73, the imaginary, mid-point signal generated from the early and late clock signals. (Fliesler, Tr. 8926-27).

686. A person of ordinary skill in the art or patent lawyer reviewing the '898 application or PCT application would understand that on-chip DLL is disclosed therein. (CX 1451 at 58-60, 148; CX 1454 at 59-61, 149; Fliesler, Tr. 8805, 8811, 8905).

Response to Finding No. 686: This proposed finding is inaccurate and contrary to the evidence. Engineers reading the '898 application in the mid to late 1990s would not necessarily have thought that Rambus might obtain patent rights to on-chip DLL as it was used in the JEDEC DDR SDRAM standard due to differences between the implementation, circuit structure and function of the circuit in Figure 12 compared to a DLL circuit. (Jacob, Tr. 5490). (*See* CCRF 685, CCFF 1335-40).

Mr. Fliesler's testimony to the contrary is not reliable because he has no DRAM engineering experience or expertise. CCPF 665.

687. When Joel Karp, then of Samsung, reviewed Rambus's PCT application in 1991, Figure 12 "jumped out" at him as evidencing a DLL. (CX 2078, Karp Micron Depo. at 119; CX 2114, Karp FTC Depo. at 276-77).

Response to Finding No. 687: Complaint Counsel does not disagree that Mr. Karp gave deposition testimony as summarized in this proposed finding.

688. In its license negotiations with Rambus in 1994, Samsung was motivated to seek a non-assertion provision for non-Rambus-compatible uses of Rambus's inventions because of the on-chip DLL shown in Rambus's PCT application. (CX 2078, Karp Micron Depo. at 107-08, 119-20).

Response to Finding No. 688: Complaint Counsel agrees that Samsung in its negotiations with Rambus in 1994 insisted upon and obtained a non-assertion provision for non-

Rambus-compatible uses of Rambus technology. Complaint Counsel also agrees that Mr. Karp testified that when he negotiated the license on behalf of Samsung in 1994 he was motivated in part by a concern that Rambus patents might extend to on-chip DLL. Mr. Karp was later employed by Rambus in the late 1990's to oversee the Rambus patent enforcement preparations, including the Rambus document destruction efforts. (CCFF 1701-58).

To the extent that this proposed finding is intended to suggest that Samsung, or the memory chip industry generally, understood from the Rambus PCT application that Rambus was asserting patent rights over on-chip DLL features outside the context of the Rambus proprietary RDRAM technology, the finding is contrary to the evidence. In a contemporaneous statement made after he became Rambus Vice President of Intellectual Property, Mr. Karp himself acknowledged that in 1999 most of the DRAM industry did not think Rambus's patents applied to SDRAMs and DDR SDRAMs. (CX1069 at 1 ("They probably think they avoid our IP if they don't go 'packetbased'")).

Samsung's insistence on the non-assertion provision in its license in 1994 made it an exception among the firms that negotiated licenses from Rambus. The predominant pattern was the one preferred by Rambus as a matter of strategy – licenses that were restricted to a narrow field consisting of RDRAM-compatible products. (CCFF 738, 740, 743-45). The negotiation of the non-assertion provision in the license with Samsung in 1994 prompted an extensive internal debate at Rambus (CCFF 1018-25). This included consideration of the possibility that the license agreement with Samsung might be good for Rambus because, as Samsung pulled the market along in the direction of using PLLs or DLLs on SDRAMs, Rambus would "get opportunities to sue" other companies that followed Samsung's lead. (CCFF 1023; CX0766 at 1).

As with Hyundai, the other firm that negotiated an exception to the narrow scope-of-use terms of the Rambus licenses (*see* CCFF 1264-65), Samsung did not continue to insist on the non-

assertion provision in later years. By December 1996, Samsung had negotiated new license terms that eliminated the provision. (CCFF 1608). As late as early 2000, Rambus continued to mislead Samsung about whether it claimed intellectual property rights over the SDRAM and DDR standards. (CCFF 1996). Ultimately, of course, Rambus did threaten to assert its patent claims against Samsung, and in October 2000 Rambus extracted a license from Samsung requiring the payment of royalties for SDRAM and DDR products. (CCFF 2008).

h. Review of the '898 or PCT Applications Would Raise Concerns that Rambus Might Be Able to Get Claims Over the Four Inventions.

689. A person of ordinary skill in the art or patent lawyer reviewing the '898 application or PCT application would have realized that Rambus might have claims broad enough to cover programmable CAS latency, programmable burst length, dual-edge clocking, and on-chip DLL. (Fliesler, Tr. 8784-85, 8810-11).

Response to Finding No. 689: This proposed finding is inaccurate, misleading, and contrary to the weight of the evidence for the reasons set forth in CCFF 1277-1350 and CCRF 659-688.

690. An experienced DRAM designer reviewing the PCT application would reach the conclusion that there is considerable similarity in form and function between programmable latency, variable burst length, dual-edge clocking, and on-chip DLL as disclosed in the PCT application and the corresponding features in SDRAMs or DDR SDRAMs. (Geilhufe, Tr. 9556-57).

Response to Finding No. 690: This proposed finding is inaccurate, misleading, and contrary to the weight of the evidence for the reasons set forth in CCFF 1277-1350 and CCRF 659-688.

691. If an experienced DRAM designer working on designing an SDRAM incorporating programmable latency and burst length in the early 1990s had reviewed the PCT application, he likely would have become concerned that Rambus might have claims to those features and would have raised the issue with management. (Geilhufe, Tr. 9558). Indeed, the evidence shows that experienced DRAM designers at IBM and Siemens reviewed Rambus's patent applications and did become concerned that Rambus might obtain patents that would cover SDRAMs. *See* Findings ¶¶ 468-482.

Response to Finding No. 691: This proposed finding is inaccurate, misleading, and contrary to the weight of the evidence for the reasons set forth in CCFF 1277-1350 and CCRF 659-688. Mr. Geilhufe's suppositions about what a DRAM engineer likely would do are sheer speculation unsupported by any evidence. With respect to the stated assertions involving concerns by IBM and Siemens, the record shows that those firms came to believe that the concerns were unfounded, based on their review of the publicly available Rambus patent information including the Rambus PCT application, and by the conduct of Rambus as a JEDEC member. (CCFF 1260-63, CCRF 468-482).

692. A manager faced with this issue, in light of the potential for substantial economic consequences if a DRAM design infringes a patent, would likely have gathered additional technical analysis from specialists and, if there remained a concern, would have taken the issue to corporate counsel for a careful review. (Geilhufe, Tr. 9558-59).

This conclusion is supported by the Mitsubishi documents, discussed below, that demonstrate a detailed analysis of Rambus's PCT application. It is further supported by the privilege logs and other documents produced by Micron and IBM which indicate that attorneys at those companies reviewed certain Rambus patents or applications. *See* Findings ¶¶ 485, 565-566.

Response to Finding No. 692: The first sentence of this proposed finding is inaccurate, misleading, speculative, unsupported by record evidence, and contrary to the weight of the evidence for the reasons set forth in CCFF 1277-1350 and CCRF 659-688. The second sentence of the proposed finding is inaccurate and misleading for the reasons set forth in CCRF 485, 565-66, and 693-702.

To the extent that this finding is intended to suggest that managers, faced with the information available from a review of the Rambus PCT application, would have sought expert assistance and concluded that there was a substantial risk that the developing SDRAM and DDR standards violated Rambus patent rights, the finding is contradicted by the very record references that it cites. In fact, there were some firms in the industry who had concerns about potential Rambus patents. But among these, several came to believe that the fears were unfounded based in

part on a review of the publicly available Rambus patent applications and issued patents (*see* CCFF 1260-65), or abandoned contractual provisions they had negotiated with Rambus that would have protected them against the risk of patent litigation by Rambus (CCFF 1264-65 (Hyundai); CCRF 688 (Samsung)). The fact that Mitsubishi and others monitored the Rambus patent activity but failed to conclude that Rambus had intellectual property rights affecting SDRAM or DDR strongly undermines the position urged by Rambus here, that the PCT application on its face should have provided notice of Rambus intellectual property claims.

693. When Mitsubishi reviewed the PCT application, it quickly undertook an in-depth study. A March 3, 1993 Mitsubishi memorandum has the subject line "Request for cooperation on evaluating Rambus (U.S.)'s patent application" and states in part:

> "Rambus Inc. of the U.S. has been approaching various Japanese companies to sell its high-speed data transfer technology . . . . Recently, we found a patent application (PCT International application) that appears to be related to [said technology] and began evaluating it, and realized that the technology is related not only to stand-alone semiconductor devices but also to systems. . . . [W]e would like to request the cooperation of your specialists in evaluating the contents of Rambus Inc.'s patent application. Please let us know which technology departments will be able to help us."

(RX 379A at 1).

Response to Finding No. 693: Complaint Counsel does not disagree that the cited exhibit, which apparently is a commercial translation of the original Japanese language document RX0379, contains the quoted language. At trial Rambus elicited no testimony whatever from any witness concerning the preparation of the translation, the author or position of the original document, the preparation of the original document or the subject matter of the document. Complaint Counsel note that the text of the translation makes reference to the author or others having begun to evaluate the Rambus PCT application (RX0379A at 1), but does not indicate any conclusion, based on the language of the PCT application, that Rambus may possess intellectual property claims with respect to the SDRAM or DDR standard technologies.

694. A June 10, 1993 Mitsubishi document again stressed the need for expert analysis of Rambus's patent application to determine the scope of the claims, particularly as to individual technologies disclosed in the patent application: "There is a need to examine the specifications of the patent claims to determine whether individual technologies used independently will infringe on the RAMBUS patent, and for that we will have to obtain the views and interpretations of experts." (RX 406 at 4).

Response to Finding No. 694: Complaint Counsel does not disagree that page 4 of the cited exhibit, which apparently is a commercial translation of original Japanese language text elsewhere in the document, contains the quoted language. At trial Rambus elicited no testimony whatever from any witness concerning the preparation of the translation, the author of the original document or his position, the preparation of the original document or the subject matter of the document. While Complaint Counsel did not object to the admission of the document, we did note our view that the document should be entitled to no weight because of the lack of any testimony from anyone who had ever seen the document before. (Tr. 6820). The only testimony concerning the document was the perfunctory statement by Mr. Fliesler, a Rambus expert, that he had reviewed it. (Tr. 8824). Presumably Mr. Fliesler was referring to the translation.

The quoted language undermines the position urged by Rambus here, that the PCT application on its face should have provided notice of Rambus intellectual property claims. The text of the letter indicates that the author or someone else had in fact done some sort of review of the application, but was unable from that review to conclude whether the particular technologies would infringe the Rambus patent. (RX0406 at 4). The document does not indicate any conclusion, based on the language of the PCT application, that Rambus possesses intellectual property claims with respect to the SDRAM or DDR standard technologies.

695. On July 17, 1993, a Mitsubishi manager wrote:

> "The claims regarding the DRAM part expand in a variety of ways upon the specifications for DRAM on a Rambus, and, as a reference, *I translated and looked at those parts that looked the most like they could be investigated separately from the bus*. I would like to have a

> thorough search and investigation of the validity of these patents. . . ."

(RX 416A at 1) (emphasis added).

Response to Finding No. 695: Complaint Counsel does not disagree that page 1 of the cited exhibit, which apparently is a commercial translation of original Japanese language text contained in RX0416, contains the quoted language. At trial Rambus elicited no testimony whatever from any witness concerning the preparation of the translation, the author of the original document or his position, the preparation of the original document or the subject matter of the document.

The quoted language undermines the position urged by Rambus here, that the PCT application on its face should have provided notice of Rambus intellectual property claims. The text of the letter indicates that the author or someone else had in fact done some sort of review focusing on the description of the Rambus invention, but was unable from that review to conclude without further expert review whether particular technologies would infringe the Rambus patent. (RX0416A at 1). The document does not indicate any conclusion from the language of the PCT application that Rambus possessed intellectual property claims with respect to the SDRAM or DDR standard technologies.

696. An August 16, 1993 Mitsubishi document again raised the issue of whether Rambus could have claims on features separate from any particular bus architecture:

> "[B]ecause there is the possibility that the claims will be narrowed to become a patent wherein the bus part is removed when Rambus itself is rejected, the DRAM folks will continuously perform detailed investigations into the applicability and into prior art." (RX 419A at 1).

Response to Finding No. 696: Complaint Counsel does not disagree that page 1 of the cited exhibit, which apparently is a commercial translation of original Japanese language text contained in RX0419, contains the quoted language. At trial Rambus elicited no testimony

whatever from any witness concerning the preparation of the translation, the author of the original document or his position, the preparation of the original document or the subject matter of the document.

The quoted language undermines the position urged by Rambus here, that the PCT application on its face should have provided notice of Rambus intellectual property claims. The text of the letter indicates that there had been some review of public Rambus patent documents, but does not conclude that particular technologies would infringe the Rambus patent. (RX0406 at 4). The document does not indicate any conclusion from the language of the PCT application that Rambus possessed intellectual property claims with respect to the SDRAM or DDR standard technologies.

697. Mitsubishi continued to keep a close watch on Rambus's patent portfolio. A January 11, 1996 memorandum indicates that Mitsubishi conducted an "investigation of the US patents owned by Rambus" that were granted by the end of October 1995 and that 18 patents met that criteria. (RX 528A at 1).

Response to Finding No. 697: Complaint Counsel does not disagree that page 1 of the cited exhibit, which apparently is a commercial translation of original Japanese language text contained in RX0419, contains the quoted language. At trial Rambus elicited no testimony whatever from any witness concerning the preparation of the translation, the author of the original document or his position, the preparation of the original document or the subject matter of the document.

The quoted language undermines the position urged by Rambus here, that the PCT application on its face should have provided notice of Rambus intellectual property claims. The text of the letter indicates that there had been an investigation of 18 issued Rambus U.S. patents, but does not conclude that particular technologies would infringe any of the Rambus patents. (RX0406 at 4). The document does not indicate any conclusion from the language of the PCT

application that Rambus possessed intellectual property claims with respect to the SDRAM or DDR standard technologies.

698. Mitsubishi also maintained a chart tracking all of Rambus's issued U.S. patents. For example, one version of this chart begins with Rambus's first issued U.S. Patent, 5,243,703, at number 1 and concludes with U.S. Patent no. 5,578,940 which issued on November 26, 1996 at number 27. (RX 2216 at 2, 4). Rambus's '327 patent is listed at number 23 on the chart. (RX 2216 at 3).

Response to Finding No. 698: Complaint Counsel does not disagree that the cited exhibit appears to be a chart of issued Rambus patents. At trial Rambus elicited no testimony whatever from any witness concerning the preparation of the translation, the author of the original document or his position, the preparation of the original document or the subject matter of the document.

The existence of this chart in no way supports the position urged by Rambus here, that the PCT application on its face should have provided notice of Rambus intellectual property claims. The document does not indicate any conclusion from the language of the PCT application that Rambus possessed intellectual property claims with respect to the SDRAM or DDR standard technologies.

699. A later version of the Mitsubishi chart contains 37 Rambus patents and includes patents that issued in early 1998. (RX 2218 at 3-6).

Response to Finding No. 699: Complaint Counsel does not disagree that the cited exhibit appears to be a chart of issued Rambus patents. At trial Rambus elicited no testimony whatever from any witness concerning the preparation of the translation, the author of the original document or his position, the preparation of the original document or the subject matter of the document.

The existence of this chart in no way supports the position urged by Rambus here, that the PCT application on its face should have provided notice of Rambus intellectual property claims.

The document does not indicate any conclusion from the language of the PCT application that Rambus possessed intellectual property claims with respect to the SDRAM or DDR standard technologies.

700. In its analyses of Rambus's patents, Mitsubishi focused on some of the four features at issue here. For example, as noted above, a Mitsubishi analysis of the claims of the PCT application specifically calls out the "modifiable access time register" and note its similarity to "SDRAM latency control." (RX 2213A at 27).

Response to Finding No. 700: This proposed finding is without any record support, for the reasons set forth at CCRF 676-77.

701. Mitsubishi also was clearly aware of potential Rambus patent claims over dual edged clocking. An August 24, 1996 report on a "Rambus meeting" states: "Rambus' patents. Issued: 16, filed: 80. For example, data is transferred at both edges." (RX 756A at 1).

Response to Finding No. 701: Complaint Counsel does not disagree that page 1 of the cited exhibit, which apparently is a commercial translation of original Japanese language text contained in RX0756, contains the quoted language. At trial Rambus elicited no testimony whatever from any witness concerning the preparation of the translation, the author of the original document or his position, the preparation of the original document or the subject matter of the document. The only testimony concerning the document was the perfunctory statement by Mr. Fliesler, a Rambus expert, that he had reviewed it. (Tr. 8826)

To the extent that this proposed finding is intended to suggest that by 1996 Mitsubishi had formed definite views of serious risks from Rambus intellectual property claims outside the scope of the proprietary RDRAM technology, it is contrary to the overwhelming weight of the evidence. In February 1997, Mitsubishi entered into a license agreement with Rambus for the Rambus proprietary Direct RDRAM technology. (CCFF 1611). In contrast to other licensees who took efforts to attempt to protect themselves from the risk of potential intellectual property claims by Rambus (CCFF 1264-65 (Hyundai); CCRF 688 (Samsung)), the scope of the Mitsubishi license

agreement was limited to Rambus-compatible DRAMs and interfaces. (CCFF 1611; CX1609 at 1-2). By April 2000, Rambus threatened Mitsubishi with charges of patent infringement based on its production of SDRAM and DDR products (CCFF 1954), and after negotiations Mitsubishi, like other DRAM producers, entered into a license to pay Rambus royalties for its production of SDRAM and DDR products. (CCFF 1984, 2011). This course of business conduct by Mitsubishi belies any contention that Mitsubishi by 1996 or earlier had concluded, based on publicly available Rambus patents or applications, that there was serious business risk that it would be sued for infringement by Rambus for its production of SDRAM or DDR products.

702. A set of undated notes produced by Mitsubishi has the heading Rambus and picks out, among other features, "PLL," clock and clock-bar, and "modifiable register . . . Access Time (~ SDRAM @ Latency)." (RX 2211 at 1). "Clock" and "clock-bar" relate to the dual-edge clocking implementation disclosed in Rambus's '898 and PCT applications.

Response to Finding No. 702: Complaint Counsel does not disagree that the cited exhibit appears to be a collection of handwritten Japanese-language notes, with at page 3-4 what appears to be a commercial translation of some or all of the notes. Throughout the translation pages there are multiple notations apparently by the translator stating "illegible" and "guess" and "half guess" with respect to the translation of the original handwritten Japanese. At trial Rambus elicited no testimony whatever from any witness concerning the preparation of the translation, the author of the original document or his position, the preparation of the original document or the subject matter of the document. The only testimony concerning the document was the perfunctory statement by Mr. Fliesler, a Rambus expert, that he had reviewed it. (Tr. 8824). The proposed finding itself notes that the handwritten notes are undated.

The total lack of any indicia of reliability with respect to the underlying document means that proposed finding lacks any support for the assertion that the notes relate to the dual-edge

clocking implementation disclosed in Rambus's '898 and PCT applications, or indeed any support for any proposition whatever pertinent to this case.

i. The Patent Office Has Determined That a Person of Ordinary Skill in the Art Would Understand from A Review of the '898 Application That Rambus Was in Possession of the Four Inventions.

703. As Complaint Counsel concede, Rambus has obtained patent claims that cover programmable CAS latency, variable burst length, dual-edge clocking, and on-chip DLL as those features are used in SDRAMs and/or DDR SDRAMs. (Complaint, ¶ 91). Rambus has asserted claims covering these four features against SDRAMs and DDR SDRAMs. (Complaint, ¶ 92).

Response to Finding No. 703: The first sentence of the proposed finding is unsupported by record evidence and inaccurate. Paragraph 91 of the Complaint, cited in RPF 703 does not support the stated concession. It states that "Rambus had succeeded in obtaining numerous patents, not expressly limited to a narrow-bus RDRAM architecture, *that purported* to cover [the four technologies]." (Complaint, ¶ 91 (emphasis added)). Complaint Counsel takes no position on the infringement and validity of those patents that Rambus has asserted against DRAM manufactures. Those questions, on which no court has ruled, are not at issue in this case. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1106 (Fed. Cir. 2003) (remanding case to district court for infringement determination and making no ruling on validity).

The proposed finding, and those that follow, do not set forth any record support for the proposition contained in the immediately preceding heading, which states a legal conclusion that is not appropriate for a finding of fact.

704. For example, claim 1 of Rambus's U.S. Patent 5,953,263, which issued on September 14, 1999, claims:

> "A synchronous semiconductor memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises:
> a programmable register to store a value which is representative of a delay time after which the memory device responds to a read request."

(CX 1517 at 29). This claim reads on an SDRAM or DDR SDRAM device containing a mode register to store a CAS latency value.

Response to Finding No. 704: Complaint Counsel does not disagree that CX1517 contains the language quoted. The second sentence of the proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this portion of the finding should be disregarded pursuant to Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

705. When examining claims, patent examiners use the broadest reasonable interpretation of the claim terms consistent with the patent specification. (Nusbaum, Tr. 1517-18). As Complaint Counsel's patent law expert explained:

> "This claim interpretation approach is used in the Patent & Trademark Office because it's very important that once a patent issues, and is asserted in a litigation, that a patentee doesn't assert an interpretation of a claim that's actually broader than what the patent examiner was using when he was searching for the prior art in determining patentability with respect to the prior art."

(Nusbaum, Tr. 1518-19).

Response to Finding No. 705: Complaint Counsel does not disagree that patent examiners are trained to apply the broadest reasonable interpretation to claim terms for this reason.

706. Thus, the PTO has issued claims to Rambus that the PTO interpreted as broad enough to cover programmable CAS latency, variable burst length, dual-edge clocking and on-chip DLL as those features are used in SDRAMs and/or DDR SDRAMs. It follows from the written description requirement that, in issuing those claims, the PTO has determined that the '898 application would clearly disclose to one of ordinary skill in the art that Rambus was in possession of these inventions as of the filing date of the '898 application. *See* Findings ¶¶ 78, 87. In other words, a person of ordinary skill in the art would, from reviewing the '898 application, identify broad inventions covering programmable CAS latency, variable burst length, dual edge clocking, and on-chip DLL, as those features are used in SDRAMs and DDR SDRAMs.

Response to Finding No. 706: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. The stated proposition is made without reference to any record support, even opinion from Rambus's own patent expert. Complaint Counsel submits that this portion of the finding should be disregarded pursuant to

Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding is unsupported by record evidence. Rambus has provided no evidence demonstrating the patent examiners' views of claims that it now purports cover the four technologies. Rambus has provided no evidence demonstrating the patent examiners' views of the descriptive portion of the '898 application.

The proposed finding does not support the conclusion that a JEDEC member reading the '898 application would have predicted that Rambus might obtain claims that it purports cover JEDEC- compliant SDRAMs and DDR SDRAMs. The written description analysis as conducted by a patent examiner or in a validity analysis begins with a drafted claim and looks for support in the specification. (Nusbaum, Tr. 1502). The written description requirement does not require that a person of ordinary skill in the art be able to predict the claims that could potentially come out of a patent specification before those claims are drafted. (Fliesler, Tr. 8903). An engineer or patent lawyer could not have known for certain what claims Rambus would pursue in the '898 family from reading the '898 application, regardless of what claims the PTO eventually allowed. (Fliesler, Tr. 8902). Rambus's proposed finding RPF 94 explains that even when the written description of a patent application is public, actual knowledge of the pending claims is valuable information. RPF 94. It is valuable because the written description does not provide notice of what will be claimed in the future. (*See*, Fliesler, Tr. 8902).

The proposed finding is contrary to the weight of the evidence for the reasons set forth in CCFF 1277-1350 and CCRF 659-658.

j. <u>Professor Jacob's Testimony Regarding What an Engineer Reading the '898 Application Would Have Understood Is Entitled to Little Weight</u>.

707. Professor Jacob has no patents to his name. (Jacob, Tr. 5650). There is no evidence in the record that he has ever applied for a patent or testified about patent issues, nor does he appear to have any patent-related experience at all. By contrast, many DRAM engineers, including many JEDEC representatives, are named inventors on patents or applications. For example, Desi Rhoden, formerly VLSI's JEDEC representative, testified that he was a named inventor on 15-20 patents. (Rhoden, Tr. 633). Mark Kellogg of IBM testified that he was an inventor on several patents. (Kellogg, Tr. 5307). Terry Lee of Micron testified that he was an inventor on many patents. (Lee, Tr. 6833). Brett Williams of Micron and Martin Peisl of Infineon also have patents to their names. (Williams, Tr. 960; Peisl, Tr. 4505-06).

Response to Finding No. 707: Complaint Counsel agrees that Professor Jacob has not been issued a patent, and was not offered as an expert in the patent application process or the process of creating an invention. Professor Jacob was offered as an expert in the field of memory architectures and systems. (Tr. 5362-63). Complaint Counsel also agrees that each of the witnesses identified is a holder of one or more, and in some instances numerous, patents.

Insofar as this proposed finding is intended to support the assertion made in the immediately preceding heading, that Professor Jacob's opinion concerning the Rambus '898 application is entitled to little weight, the finding is in fact contradicted by the citations to the listed witnesses. Professor's Jacob's opinion, based on his background in the field and his review of the language of the '898 application, was that reasonable engineers in the early to mid-1990s would not have understood from Rambus' '898 patent application that Rambus might be able to obtain patents with claims covering the technologies in question as proposed for use in JEDEC's SDRAM and DDR SDRAM standards. (Jacob, Tr. 5460-61). Rather than contradicting Professor Jacob on this conclusion, each and every one of the listed witnesses reinforced its accuracy.

None of the listed witnesses testified that he had concluded from a review of the '898 application that Rambus might assert patent rights over the SDRAM or DDR stand technologies. On the contrary, despite their substantial professional qualifications, longtime involvement in the DRAM industry, and close involvement in JEDEC activities or matters affecting the production of SDRAM or DDR standard memory products, each and every one of the listed witnesses believed

that any Rambus intellectual property claims did not pertain to the SDRAM and DDR standards. (Rhoden, Tr. 521 (believed that any Rambus patents pertained to the proprietary RDRAM technology) (*see* CCFF 1249); Kellogg, Tr. 5053 (expected that any Rambus patent activity would be associated with the Rambus proprietary RDRAM product) (*see* CCFF 1252); Lee, Tr. 6610-11 (participated with Micron colleagues in review of Rambus patents, concluded that patents applied specifically to the RDRAM bus architecture) (*see* CCFF 1253); Williams, Tr. 829-35 (in 1993, described SDRAM as royalty-free, in contrast to Rambus RDRAM); Peisl, Tr. 4430-31 (confirming Infineon conclusion in 1999 that DDR standard was royalty-free)).

In short, these witnesses confirm the accuracy of Professor Jacob's view that the language of the '898 patent application, or other publicly available Rambus patent documents containing this language, would not place knowledgeable members of the DRAM industry on notice of the possibility of Rambus patent claims as to the SDRAM or DDR standard technologies. This conclusion is consistent with the overwhelming weight of evidence in the record as a whole, which demonstrates that Rambus was successful in its campaign of concealing its claims to intellectual property rights in JEDEC standard technology. (*See* CCFF 1238-65, 1273-76).

Professor Jacob has extensive experience in DRAM architecture design and in depth knowledge of the JEDEC SDRAM standard. CCRF 708. His conclusions regarding the disclosure of the '898 application were based on an in-depth understanding of DRAM technology and his analysis of the significant differences between the narrow-bus, multiplexed, packetized system and U-shaped clock described in the '898 specification and the SDRAM system standardized by JEDEC. (*See* CCFF 1284-1340). The fact that he is not named the inventor on any patent does not undermine that analysis.

708. As an academic who has never worked in the DRAM industry, Professor Jacob does not deal with intellectual property issues that arise in the industry. Professor Jacob is poorly

equipped to opine as to what an engineer with patent experience would have understood from reading a patent application.

Response to Finding No. 708: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this portion of the finding should be disregarded pursuant to Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Professor Jacob began in-depth research into DRAM architecture as a graduate student in the early 1990's. He continues that research to this day as a tenured professor in the electrical and computer engineering department at the University of Maryland. (Jacob, Tr. 5353, 5356-62). In the course of his work for this matter, he reviewed an enormous number of JEDEC minutes and presentations, including the standards and discussed his understanding of those minutes with numerous DRAM engineers. (Jacob, Tr. 5367-69). His conclusions regarding the disclosure of the '898 application were based on an in-depth understanding of DRAM technology as it developed through the 1990s and his analysis of the significant differences between the narrow-bus, multiplexed, packetized system and U-shaped clock described in the '898 specification and the SDRAM system standardized by JEDEC. (*See* CCFF 1284-1340). The fact that his in depth knowledge is based on research done in an academic setting is irrelevant to the reliability of his conclusions.

709. Given Professor Jacob's background, Rambus challenged his qualifications to render an opinion as to what a reasonable engineer in the early to mid-1990s would have understood from Rambus's '898 patent application. Complaint Counsel responded that "what we are doing is looking at the Rambus '898 application in order to determine the understanding that can be drawn out of that application." (Jacob, Tr. 5461). In other words, Complaint Counsel suggested that they were engaging in an objective inquiry, presumably based on Professor Jacob's current understanding from reviewing the '898 application. Complaint Counsel made no showing, however, that Professor Jacob's current understanding is relevant to the understanding of DRAM engineers in the early to mid-1990s.

Response to Finding No. 709: Complaint Counsel does not disagree that Rambus objected to Professor Jacob's qualifications to render an opinion on the issue indicated; the objection was overruled. (Tr. 5461). Professor Jacob's began academic research into DRAMs in the early 1990s that continues to this day. He performed an in depth study of the development of the JEDEC SDRAM standard during the early to mid 1990s for this case. (CCRF 709). His conclusions regarding how an engineer would have viewed the '898 specification in the early to mid 1990s are well-supported.

The last two sentences of this proposed finding lack any reference to the record, constitute legal argument, and are inappropriate for findings of fact. Complaint Counsel submits that this portion of the finding should be disregarded pursuant to Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Insofar as this finding asserts that a current understanding of the language of the '898 application is irrelevant, Complaint Counsel notes that the assertion is inconsistent with numerous proposed findings of Rambus that are based on representations by Rambus counsel concerning the contents of the '898 application. (RPF 663, 667, 673, 674, 681, 683, 685). Professor Jacob's qualification as an expert in the field of memory architecture and systems (Tr. 5363) provides valuable assistance in interpreting the content and meaning of the language of the '898 application.

710. Professor Jacob's testimony regarding what an engineer would have understood from reviewing the '898 application is also internally inconsistent. Professor Jacob testified that an engineer reading the '898 application during the 1990s would not have realized that Rambus could obtain patent rights over the dual-edge clocking feature as it was proposed for use or used in DDR SDRAMs because, in his opinion, the implementation described in the patent specification is different from that in DDR SDRAMs. (Jacob, Tr. 5493). Professor Jacob also testified that the claims of the '327 patent would read on DDR SDRAMs. (Jacob, Tr. 5660). But, the specification of the '327 patent is identical in all material respects to the specification of the '898 application and, in particular, the two documents describe the same implementation of dual-edge clocking. Professor Jacob's opinion is, therefore, inconsistent with the legal determination made by the PTO in issuing the patent that the claims of the '327 patent are supported by its specification (and thus by the specification of the '898 application) from the point of view of a person of ordinary skill in the art.

Response to Finding No. 710: The proposed finding lacks supporting reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this portion of the finding should be disregarded pursuant to Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The proposed finding is misleading and inaccurate. Professor Jacob's testimony regarding the content of the '898 specification is not inconsistent with his testimony that an engineer could reasonably interpret the claims of the '327 patent to cover on-going JEDEC work or the DDR SDRAM standard that resulted from that work. Professor Jacob reviewed the '898 application and determined that a reasonable engineer would not have understood from it that Rambus could obtain patent claims covering dual edge clocking as proposed for use in JEDEC-compliant SDRAMs because (1) the clocking scheme described in the specification of the '898 application differed from dual edge clocking as proposed for use with JEDEC-compliant SDRAMs, CCFF 1327-34, (2) the use of dual edge clocking described in the specification of the '898 application was limited to the context of Rambus's unique loop-back clock arrangement, CCFF 1283-1308, and (3) none of the original claims covered use of dual edge clocking outside of the unique Rambus loop back clock arrangement, CCFF 1343-50. Professor Jacob reviewed the claims of the '327 patent and demonstrated how each element of two independent claims of the '327 patent corresponded to features of JEDEC work and the DDR SDRAM standard, leading to his conclusion that a reasonable engineer could have concluded that the claims of the '327 patent covered on-going JEDEC work. (CCFF 1216-37).

Complaint Counsel agrees that patent examiners are instructed to consider whether a person of ordinary skill in the are would find support for the claims of a patent in the specification. RPF 710 is misleading, however, for three reasons. First, there has been no judicial finding that the '327 patent is valid, so it is unclear whether such a determination, assuming it was made by the

patent examiner, is correct. Second, Rambus's analysis is backwards. Rambus assumes that, because an engineer starting with the clear terms of the claims of the '327 patent could then find support for those claims among the 67 pages of description in the specification and the drawings, an engineer therefore must also be able to start with the 67 page specification and, despite its emphasis throughout on the unique Rambus bus architecture, predict that Rambus could – and would – pursue the precise claims set forth in the '327 patent. Patent law does *not* contemplate any such result, and Rambus's own expert admitted that the written description element of patent law does not require that a person of ordinary skill in the art be able to predict all claims that potentially could come out of a patent specification. (Fliesler, Tr. 8903).

Third, and most importantly, the relevant issue is not what JEDEC engineers should have understood, but what they did understand. Even if Rambus's backwards analysis were legitimate and JEDEC engineers should have understood from Rambus's '898 application that Rambus could obtain the claims contained in the '327 patent, the fact of the matter is that they didn't. CCFF 746-56, 1238-59. Indeed, Rambus was aware that JEDEC members did not understand the potential scope of Rambus's claims, and acted to take advantage of that lack of knowledge. *See* CX770 (Harmon e-mail, 10/11/94: "[L]et's not rock the boat" by telling Samsung we have patent applications relating to on-chip PLL); CX783 at 2 (Crisp e-mail, 2/26/95: "I certainly do not want to bring this intellectual property issue up without careful consideration. I especially do not want it all over JEDEC."); CX711 at 68, 73 (Crisp e-mail, 5/24/95: "[I]t makes no sense to alert them to a potential [patent] problem they can easily work around."); CX837 at 2 (Crisp e-mail, 9/23/95: "we should re-evaluate our position relative to what we decide to keep quiet about, and what we say [to JEDEC] we have"); CX1277A at 1, 2 (Presentation, 3/96: "200Mhz SDRAM Myth:" "Challenges (do not tell them :-)"); CX919 (Tate e-mail, 2/10/97: "do NOT tell customers/partners that we feel DDR may infringe – our leverage is better to wait"); CX938 (Davidow e-mail, 7/11/97: "One of

the things we have avoided discussing with our partners is intellectual property problem. . . . We have not yet told Siemens that we think SLDRAM and SDRAM-DDR infringe our patents."); CX942 (Tate e-mail, 8/4/97: "our policy so far has been NOT to publicize our patents and i think we should continue with this"); CX947 at 1 (Clarke e-mail, 8/15/97: "Q. Do Double Data Rate (DDR) SDRAMs use this patent? A. We don't know yet."); CX960 (Tate e-mail, 10/1/97: "when joel [karp] starts we need to have our spin control ready for partners/etc as to why we are hiring him and what he will be doing."); CX987 (Tate e-mail, 1/19/98: "ddr infringes our patents (question: when do we start saying this publicly?)"); CX1069 (Karp e-mail, 5/1/99: "They probably think they avoid our IP if they don't [use a narrow, packet-based bus]"); CX1089 (Tate e-mail, 12/9/99: "it's important NOT to indicate/hint/wink/etc what we expect the results of our infringement analysis to be!!!")).

Rambus cannot excuse its deliberate failure to disclose its '327 patent and relevant patent applications by pointing to the alleged incompetence of JEDEC members to figure it out for themselves. The fundamental purpose of the JEDEC disclosure rules was to prevent members from having to try to figure it out for themselves by putting the disclosure obligation on the one party that has complete information and is best positioned to say what the scope of the potential intellectual property rights are – the intellectual property holder itself. (CCFF 316-46).

711. In reaching his opinions about what an engineer in the 1990s would have realized from reviewing the '898 application, Professor Jacob did not consider the evidence in the record regarding what engineers in the 1990s actually did realize from reviewing the '898 application or the corresponding PCT application. In particular, Professor Jacob did not consider documents indicating that IBM and Mitsubishi had reviewed Rambus's PCT application and had concerns about the scope of Rambus's intellectual property coverage. (Jacob, Tr. 5661-67).

Response to Finding No. 711: Complaint Counsel does not disagree that the focus of Professor Jacobs' opinion on the '898 application was on the language of the application, bringing to bear Professor Jacobs' expertise in the field of memory architecture and systems. (*See*

Jacobs, Tr. 5661). Professor Jacobs was not called on to review the determinations made by industry members concerning the scope of the intellectual property claims of Rambus, though in fact, the record shows that on several occasions persons with engineering backgrounds, knowledge of computer systems and DRAM memory, and substantial practical familiarity with the design of DRAM memory, reviewed the substance of the Rambus '898 or PCT patent applications and concluded that the applications described the proprietary Rambus RDRAM technology.

One of these occasions was the review by the Rambus JEDEC representative Richard Crisp, who at the time he first read the original '898 patent application in the early 1990's and believed that it was intended to describe the RDRAM system invention, and that it was limited to the proprietary RDRAM technology. (Crisp, Tr. 2927-28; CCFF 727). (Crisp subsequently came to believe that the '898 application could be amended to add claims covering technologies used in other architectures, including SDRAMs, thorough his conversations with patent attorney Lester Vincent and others. (Crisp, Tr. 2928-29)). Another occasion was the review by Howard Sussman, the experienced DRAM memory designer, who in 1992 obtained a copy of the Rambus European patent application and concluded after reviewing it that the patent pertained to the proprietary RDRAM technology and did not pose a problem for the SDRAM standardization activity at JEDEC. (CCFF 1273-74). When Mr. Sussman announced this conclusion at a JEDEC meeting, Mr. Crisp of Rambus was present and did not contradict the statement. (*Id.*). Another occasion was the review by the experienced DRAM memory designer Willi Meyers of Infineon, who in 1992 had concerns about rumors of possible Rambus patents on dual-bank technology; after reviewing the Rambus European patent application and witnessing Mr. Crisp's disclosure of the Rambus '703 patent at JEDEC, Mr. Meyers wrote his colleagues in late 1993 that the SDRAM standard adopted by JEDEC had avoided patented technology. (CCFF 1275). Another occasion was the review of Rambus patents conducted by knowledgeable Micron employees in 1995 in

connection with the possible licensing by Micron of RDRAM technology. (CCFF 1276). After this review, Micron concluded that the Rambus patents applied specifically to the RDRAM bus architecture. (*Id.*).

This record evidence thus confirms the opinion of Professor Jacob, which was focused on a review of the content of the language of the '898 application and application of his professional expertise in memory architecture and systems.

712. Although Professor Jacob spoke to various JEDEC members in connection with his work in this case, he did not ask any of them whether they had read the PCT application and, if so, what conclusions they had drawn. (Jacob, Tr. 5666-67).

Response to Finding No. 712: Complaint Counsel does not disagree.

713. The evidence of what engineers actually *did* realize when they reviewed the PCT application is more persuasive than Professor Jacob's opinion of what an engineer "would have" realized.

Response to Finding No. 713: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this portion of the finding should be disregarded pursuant to Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Complaint Counsel agrees that it is pertinent what engineers actually *did* realize when they reviewed the PCT application. The record evidence in this regard in fact confirms the accuracy of Professor Jacob's view that the language of the '898 patent application, or other publicly available Rambus patent documents containing this language, would not place knowledgeable members of the DRAM industry on notice of the possibility of Rambus patent claims as to the SDRAM or DDR standard technologies. (*See* CCRF 661, 665, 688, 691, 692, 707, 711). Record evidence makes clear that numerous knowledgeable members of the industry *did* review the Rambus PCT application and concluded that it did *not* pertain to JEDEC-standard technology. (*See* CCRF 711).

k. Rambus's '703 Patent Gave Notice that Rambus Could Obtain Patents Over the Four Inventions.

714. Rambus's first United States patent, U.S. patent no. 5,243,703 ("the '703 patent"), issued on September 7, 1993. (RX 425). Rambus disclosed the '703 patent to JEDEC during a committee meeting in September 1993. (The Parties' First Set of Stipulations, Stipulation 11). The '703 patent was subsequently added to the "patent tracking list" maintained by JEDEC, where it was described as involving a "Sync Clock." (JX 18 at 18).

Response to Finding No. 714: Complaint Counsel does not disagree with the substance of this proposed finding. (*See* CCFF 1351, 968-76).

715. The '703 patent can be traced back to a divisional application of the original '898 application. (RX 425 at 1; Fliesler, Tr. 8812).

Response to Finding No. 715: Complaint Counsel does not disagree. (*See* CCFF 1351).

716. The written description and drawings of the '703 patent, like all the issued patents that claim priority to the '898 application, are substantially the same as the written description and drawings in the '898 application. (RX 425 at 1; CX 1451 at 1; Fliesler, Tr. 8812, 8817). Thus, the '703 patent contains the same descriptions of programmable latency, variable burst length, dual-edge clocking, and on-chip DLL as in the '898 application and PCT application. (RX 425 at 7, 8, 9, 14-17, 21; Fliesler, Tr. 8819-20).

Response to Finding No. 716: Complaint Counsel does not disagree that the '703 patent contains substantially the same written description and drawings as the '898 application. (*See* CCFF 1352). To the extent that the second sentence of the proposed finding suggests that the '703 patent describes the four technologies, it is contrary to the weight of the evidence for the reasons set forth in CCFF 1277-1350 and CCRF 659-688.

717. In addition to listing the original '898 application, the '703 patent's written description also contains a list of the nine other divisional applications stemming from the '898 application that were pending at the time. (RX 425 at 11; Fliesler, Tr. 8813-14). An engineer with some familiarity with the patent system or a patent attorney would understand that the PTO had determined that the original '898 application disclosed multiple inventions and that Rambus was pursuing at least ten other inventions in related applications.

Response to Finding No. 717: Complaint Counsel does not disagree with the first sentence of the proposed finding. The second sentence of the proposed finding is inaccurate. The

PTO issued the restriction requirement that led to the 10 other related applications on the basis that the original 150 claims of the '898 application sought to cover 11 different inventions. (Nusbaum, Tr. 1510-11). The PTO's restriction requirement was not based on what the '898 application *disclosed* as stated in the proposed finding, only what it *claimed*. *See* 37 C.F.R. § 1.142 ("If two or more independent and distinct inventions are *claimed* in a single application, the examiner in an Office Action will require the applicant in the reply to that action to elect an invention to which the claims will be restricted . . . .) (emphasis added).

The proposed finding does not support the conclusion in the heading that the '703 patent gave JEDEC members notice that Rambus could obtain patents over the four technologies. The identical specification of each of the divisional applications did not provide that notice for the reasons set forth in CCFF 1277-1350 and CCRF 659-688. None of the original 150 claims of the '898 application, which were the basis for 10 divisional applications, related to SDRAM technology. (CCFF 1343-1359).

718. The subheadings in the "Detailed Description" section of the '703 patent would be one indication to a person of ordinary skill in the art that the inventors had worked not only on a whole system, but also on individual components and subcomponents of that system (RX 425 at 13-25; Fliesler, Tr. 8818).

Response to Finding No. 718: Complaint Counsel agrees that the description contained in the '703 patent is substantially the same as the '898 application, including the headings. (*See* CCFF 1352). However, the headings in the description in the '703 patent are no more illuminating concerning the possibility of broad Rambus intellectual property claims than they were in the '898 application. (*See* CCFF 1277-1350 and CCRF 659-688). For instance, a section of the '898 application that Rambus cites as describing programmable CAS latency and programmable burst length falls under the heading "Protocol and Bus Operation." (CX1451 at 21-30; *see* RPF 673, 678). The entire description under that heading is limited to a narrow,

multiplexed bus and packetized system in which all bus lines carry address, control and data information. (*Id.*; Fliesler, Tr. 8914). The paragraph of the '898 specification that Rambus cites as describing dual edged clocking fall under the heading "Clocking," which describes only the U-shaped clocking scheme illustrated in Figure 8a. (*See* RPF 681 citing CX1451 at 49; CX1451 at 47-49; Fliesler, Tr. 8923-26).

719. A person of ordinary skill in the art or patent attorney reviewing the '703 patent would have understood that Rambus was claiming a number of different inventions claiming priority to the '898 application. (RX 425 at 24-25; Fliesler, Tr. 8818-19).

Response to Finding No. 719: This proposed finding is inaccurate and contrary to the overwhelming weight of the evidence.

The '703 patent contains claims over a U-shaped or reflected clock technology; neither the claims nor the specification of the '703 patent would have alerted an engineer at the time it was issued that Rambus might seek to obtain patent rights over features contained the JEDEC SDRAM standard. (CX1460; Jacob, Tr. 5498-5501; *see* CCFF 1277-1340, 1351-55). The claims of the '703 patent recite a "U-shaped clocking scheme" having an early clock and a late clock signal and generating the time average of those two clock signals. (CX1460 at 24; Jacob, Tr. at 5499-5500). The JEDEC SDRAM and DDR SDRAM standards do not use the "U-shaped clocking scheme." (Jacob, Tr. 5492-93, 5497). The claims of the '703 patent did not read on anything other than Rambus-compatible devices. (CX2102 at 321 (Karp, Dep.)).

The knowledge of the '898 application and the other nine divisional applications that might have been obtained through a review of the '703 patent would not have alerted a person of ordinary skill in the art, a patent attorney or a JEDEC member that Rambus might pursue claims to SDRAM technology. None of the original 150 claims of the '898 application, which were the basis for 10 divisional applications, related to SDRAM technology. (CCFF 1343-1359). Each of the claims is limited to either a narrow, multiplexed bus system or the U-shaped clocking scheme.

(CCFF 1344-48). In fact, a patent attorney reviewing the original 150 claims would not have assumed that they contained unnecessary limitations because of the massive effort required to draft the relatively lengthy specification and the large number of claims. (Nusbaum, Tr. 1537-40).

Though Rambus contends that what industry members *did* realize is important (RPF 713), Rambus has not and cannot cite any evidence that disclosure of the '703 patent to JEDEC members or to the public in general caused any knowledgeable member of the DRAM industry to conclude that there was a risk that Rambus intellectual property claims outside the realm of its proprietary RDRAM technology. Indeed, the overwhelming evidence is to the contrary. Despite the fact that the '703 patent was disclosed to JEDEC in 1993, the common belief by JEDEC members and throughout the DRAM industry throughout the 1990's was that Rambus did not have intellectual property claims to the SDRAM and DDR standards. Rambus made continuing efforts to be sure that the extent of its intellectual property claims was concealed. (*See* CCFF 1238-65, 1273-76, 1676-1700).

IX. JEDEC WOULD NOT HAVE ADOPTED DIFFERENT STANDARDS HAD RAMBUS MADE ADDITIONAL DISCLOSURES.

720. Even if Rambus made the additional disclosures Complaint Counsel allege should have been made, JEDEC would have adopted the same Rambus technologies into the SDRAM and DDR standards. This conclusion is supported by three distinct lines of evidence. Any one of these lines of evidence is sufficient to show that JEDEC would not have adopted alternative technologies.

Response to Finding No. 720: RPF 720 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

721. First, what technologies JEDEC would have adopted had Rambus made the additional disclosures can be inferred from JEDEC's technology choices in the real world. As discussed below, the doctrine of revealed preference shows that JEDEC would have adopted Rambus's

technologies because JEDEC adopted them in the real world - even after Rambus began asserting its patents against DRAM manufacturers.

Response to Finding No. 721: RPF 721 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. As described below, RPF 721 is also misleading because it misstates the record regarding the application of revealed preferences. CCRF 726. As described below, RPF 721 is also contrary to the weight of the evidence because an application of revealed preferences to the choices made by JEDEC could also be seen as an implementation of JEDEC's preference for timely standards. (CCRF 726).

722. Second, a comparison of the alleged alternative technologies with the Rambus technologies in cost-performance terms demonstrates that the alternatives were inferior - even accounting for the royalties that Rambus is paid for the use of its technologies. This demonstrates two things: (1) JEDEC would have adopted the Rambus technologies because they are the best choice in terms of cost-performance characteristics and (2) both DRAM manufacturers and consumers are better off licensing the Rambus technologies than they would be using alternative technologies.

Response to Finding No. 722: RPF 722 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. As described below, RPF 722 is also contrary to the weight of the evidence for two reasons: First, there is no evidence that JEDEC members ever evaluated alternative technologies using Respondent's "cost-performance characteristics" as a measurement. In fact, the weight of the evidence is to the contrary. (CCRF 726) Second, the weight of the evidence is that, even using the measurement proposed by Respondent, a number of the alternatives proposed at the hearing would have had

better "cost-performance characteristics" than the technologies in the current standard. (CCFF 2102-2413).

723. Third, a decision analysis examining both JEDEC's and Rambus's economic incentives and past behavior shows that had Rambus made the additional disclosures that Complaint Counsel allege should been made, JEDEC would have adopted the very same standard that it did in the real world, and JEDEC members would have negotiated with Rambus for licenses in the same circumstances that they did in the real world. In other words, assuming that Rambus had made the additional disclosures that Complaint Counsel allege should have been made, the outcome in this "but-for" world is the same as in the real world - nothing would have changed.

Response to Finding No. 723: RPF 723 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. As described below, the statement in RFP 723 that "had Rambus made the additional disclosures that Complaint Counsel allege should been made, JEDEC would have adopted the very same standard that it did in the real world, and JEDEC members would have negotiated with Rambus for licenses in the same circumstances that they did in the real world" is contrary to the weight of evidence. (CCFF 2433-2464).

A. JEDEC Repeatedly Chose Rambus's Technologies, Even When Warned Of Rambus's Potential Patents, And Even After Rambus Began To Assert Its Patents.

724. The economic theory of revealed preference teaches that one should not look to what people say but at what they actually do. (Teece, Tr. 10366).

Response to Finding No. 724: Complaint Counsel does not disagree.

725. In simple terms, the theory of revealed preference is that you draw inferences about people's preferences by observing their choices. (Rapp, Tr. 9804). For example, if a person purchases $70 worth of groceries, the inference is that there is no combination of goods that could be purchased for $69 that is worth as much to that person as the bundle of goods actually purchased. (Rapp, Tr. 9804).

Response to Finding No. 725: Complaint Counsel does not disagree.

726. According to the theory of revealed preference, the choices of JEDEC and DRAM manufacturers to use the Rambus technologies when there were opportunities to use other technologies, shows that the Rambus technologies were superior to any alternatives in cost-performance terms. (Rapp, Tr. 9803-05).

Response to Finding No. 726: RFP 726 is not supported by the cited evidence and is contrary to the weight of evidence. Application of revealed preferences requires that one look "at what [decision-makers] actually do." RFP 724. Dr. Rapp, in coming to the conclusion cited in RFP 726, did nothing to determine what the JEDEC 42.3 committee actually did in developing the DRAM standards. As a consequence, Dr. Rapp made assumptions regarding the operation of JEDEC that led him to the incorrect conclusions reflected in RPF 726.

When Dr. Rapp reached his conclusions regarding the effect of Rambus's non-disclosures to JEDEC on whether JEDEC would have adopted the Rambus technologies anyway, he was not familiar with the details of the process that JEDEC went through in the real world in selecting the Rambus-claimed technologies. (Rapp, Tr. 10106-109). Before completing his expert report, Dr. Rapp did not look at the evidence relating to the process through which JEDEC made the decisions that it made in developing the relevant standards. (Rapp, Tr. 10111). Dr. Rapp did not know whether, prior to their ultimate adoption, there was any opposition within JEDEC to the use of any of the technologies in the standard. (Rapp, Tr. 10109). Nor did Dr. Rapp, give consideration to JEDEC's specific processes or rules for dealing with patent disclosure issues. (Rapp, Tr. 10116 ("Well, I understood in general terms what they were, but I didn't delve into them in forming that conclusion.")). Finally, when Dr. Rapp reached his conclusions regarding the effect of Rambus's non-disclosures to JEDEC on whether JEDEC would have adopted the Rambus technologies anyway, he did not know whether any alternatives to those technologies were discussed within JEDEC. (Rapp, Tr. 10109).

As a consequence of Dr. Rapp's lack of familiarity with the record evidence in this case, he made the incorrect assumption that JEDEC simply attempts to find the best cost-performance solution. (Rapp, Tr. 9806). Since, as described above, Dr. Rapp did not look at the evidence relating to the process through which JEDEC made the decisions that it made in developing the relevant standards, he had no basis in the record for that assumption. The weight of the evidence demonstrates that the choices actually made by JEDEC are as likely to reflect the need for timely standards as they are to reflect any cost performance evaluations. First, standardization in the DRAM industry is very time consuming. (CCFF 122). DRAM industry participants consider time to market to be an important factor in developing standards. (CCFF 123). Because of the length of time required to develop DRAM standards at JEDEC and the importance of timely standards, JEDEC members are inclined to make compromises in order to avoid delay in the passage of the DRAM standard. (CX2383 ("[W]e are willing to make compromises if necessary to reach a quick resolution on a standard"); Bechtelsheim, Tr. 5794-95; Lee, Tr. 6635 (Although it preferred the SDRAM-Lite device, Micron "agreed in the interests of schedule to just go ahead and accept the full-feature proposal.") and 6683 ("Our preference was still not to have [strobes], but our action was to -- to go along with the committee in general with this compromise, because there was -- because of these differences of opinion, it was causing some delay in the standardization process.")).

As described by Professor McAfee, if you "want to actually understand how the marketplace decides, you have to understand how the decisions are made. That is, you have to understand the process by which decisions are actually made, and that is not accounted for in Dr. Rapp's approach." (McAfee, Tr. 11235). Because the one of the important factors influencing JEDEC's decision-making process is the industry's need for timely standards, it is more correct to view that process as "satisficing." (CCFF 2772-2773; McAfee, Tr. 7255-7256). Satisficing is a

term introduced by Nobel laureate Herbert Simon and it refers to a process where a decision-maker would look for a solution that was good enough rather than spend time and resources looking for the best solution. (McAfee, Tr. 7255-7256). That JEDEC satisfices is confirmed by the willingness of JEDEC members to compromise in order to avoid delay to the standard, as described above. As a result of the fact that JEDEC satisficed in choosing the technologies to include in the standard, the technologies actually chosen are not necessarily "superior to any alternatives in cost-performance terms." (McAfee, Tr. 7256 ("And so its importance in terms of the economic analysis is that this says generally you can't conclude from the very choice of the technology that it was necessarily even the best of the available alternatives.")).

727. JEDEC selected Rambus's technologies over all others in the real world. For SDRAM, JEDEC selected two Rambus technologies: programmable CAS latency and programmable burst length over all available alternatives. As Gordon Kelley testified, JEDEC considered the available technologies and selected what was considered to be the best. (Kelley, Tr. 2707-09).

Response to Finding No. 727: The statement in RPF 727 that "JEDEC selected Rambus's technologies over all others in the real world," lacks any reference to the record and is inaccurate. There is no evidence in the record that JEDEC had access to, or even attempted to have access to, "all" technologies in the real world. Instead, the weight of the evidence establishes that JEDEC found a workable solution to each of its problems and moved on. (CCFF 2772-2777, CCRF 726). In addition, the statement in RPF 727 that Gordon Kelley testified that "JEDEC considered the available technologies and selected what was considered to be the best" is misleading because it implies that JEDEC evaluated all technologies, an implication that is contrary to the weight of the evidence and is not supported by the referenced testimony. Instead, Gordon Kelley agreed that the committee pursued what it felt was the best option available to it *based on the information it had*. (G. Kelley, Tr. 2708).

728. In the process of developing the SDRAM standard, JEDEC considered and rejected many of the alternatives that Complaint Counsel now assert JEDEC could have adopted in place of the Rambus technologies. Instead of Rambus's programmable CAS latency technology, JEDEC considered the alternatives of fixed latency and the use of fuses to set the latency. (Kellogg, Tr. 5136). With regard to Rambus's programmable burst length technology, JEDEC considered the alternatives of fixed burst length, the use of pins to set the burst length, and the use of fuses to set the burst length. (Kellogg, Tr. 5111-12).

Response to Finding No. 728: The statement in RPF 728 that "JEDEC considered and rejected many of the alternatives that Complaint Counsel now assert JEDEC could have adopted in place of the Rambus technologies" is misleading because it implies, without supporting evidence, that JEDEC specifically rejected those alternatives. Instead, the weight of the evidence demonstrates that, although different members had different preferences, JEDEC as a whole simply needed to choose between the alternatives to set the latency and burst length for SDRAM. (Rhoden, Tr. 449 ("The committee itself actually discusses, as you saw, the many different options that you see, and in the process of standardization, we can't really have a plethora of approaches on how to support -- how to approach something. The concept is to just pick one. And so, the committee picked one to move forward, and this was the item that they picked to move forward."). The evidence cited in this finding is only relevant for the assertion that JEDEC did consider alternatives to the Rambus technologies, a point with which Complaint Counsel agrees.

729. For DDR, JEDEC selected four Rambus technologies over all others: programmable CAS latency, programmable burst length, dual-edge clocking, and on-chip PLL/DLL.

Response to Finding No. 729: The statement in RPF 729 that "JEDEC selected four Rambus technologies over all others," lacks any reference to the record and is inaccurate. There is no evidence in the record that JEDEC had access to, or even attempted to have access to, "all" technologies in the real world. Instead, the weight of the evidence establishes that JEDEC found a workable solution to each of its problems and moved on. (CCFF 2772-2777; CCRF 726-727).

730. Just as with the SDRAM standard, for the DDR standard JEDEC considered and rejected several alternatives for Rambus's technologies that Complaint Counsel now assert JEDEC could have adopted in place of the Rambus technologies. In the place of Rambus's dual-edge clocking technology, JEDEC considered increasing the speed of the clock and interleaving banks on a module. (Kellogg, Tr. 5178). Instead of Rambus's on-chip PLL/DLL technology, JEDEC considered using verniers and relying only on data strobes. (Kellogg, Tr. 5156).

Response to Finding No. 730: The statement in RPF 730 that "JEDEC considered and rejected several alternatives Rambus's technologies that Complaint Counsel now assert JEDEC could have adopted in place of the Rambus technologies" is misleading because it implies, without supporting evidence, that JEDEC specifically rejected those alternatives. Instead, the weight of the evidence demonstrates that, although different members had different preferences, JEDEC as a whole simply needed to choose between the alternatives then available. (CCRF 726-727). The evidence cited in this finding is only relevant for the assertion that JEDEC did consider alternatives to the Rambus technologies, a point with which Complaint Counsel agrees.

731. Instead of these alternatives, JEDEC selected Rambus's technologies. Applying the theory of revealed preference shows that none of these alternatives met JEDEC's needs as well as the Rambus technologies.

Response to Finding No. 731: RPF 731 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Furthermore, RPF 731 is contrary to the weight of evidence. Because of the importance of delay to the DRAM industry, JEDEC's choice of a particular standard cannot be taken as evidence that the choice meets JEDEC's needs better than alternatives. (CCRF 726).

732. Complaint Counsel allege that JEDEC members were unaware at the time of the selection of the Rambus technologies for SDRAM and DDR that Rambus could possibly obtain patents that covered these technologies. This allegation is refuted by the evidence discussed above. But even if the allegation were correct, it would not undermine the application of the theory of revealed preference. JEDEC demonstrated that it would choose Rambus's technologies even if

patented when it adopted the four Rambus technologies in the DDR2 standard even after Rambus began asserting its patents against DRAM manufacturers.

Response to Finding No. 732: RPF 732 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003), and this Court's July 10, 2003 Order on Post Trial Briefs. Furthermore, RPF 732 is misleading and contrary to the weight of evidence. RPF 732 is misleading because it implies that JEDEC's use of the disputed technologies in DDR-2 was motivated by the technical characteristics of the technologies and not by the fact that by 2000 JEDEC was already locked in to dual-edged clocking and on-chip PLL/DLL. The weight of the evidence demonstrates that by 2000, changing the DDR-2 standard to remove those features and replace them with others would have delayed the DDR-2 standard, would have damaged the investments already made by firms in developing products compliant to the new standard, and could have hindered the acceptance of the new standard if it had used alternative technologies that were not compatible with DDR SDRAM. (CCFF 3229-3261).

733. The development of the DDR2 standard began in April 1998. (Macri, Tr. 4598). From that date through June 2000, JEDEC specified many of the architectural attributes for DDR2. (Macri, Tr. 4598-99).

Response to Finding No. 733: Complaint Counsel does not disagree. For a more complete discussion of the of the development of the DDR2 SDRAM standard, *see* CCFF 3229-3261.

734. In late 1999, well prior to the close of the DDR2 specification period, Rambus began asserting its patents against JEDEC-compliant SDRAM and DDR products that incorporated the technologies at issue in this case. (Complaint, ¶ 92). This assertion of patent rights was widely publicized and well-known in the industry. (CX 1864 at 1; Macri, Tr. 4667-8). JEDEC's development of the DDR2 standard continued in the face of this knowledge.

Response to Finding No. 734: RPF 734 is misleading because it implies that Mr. Macri and others in the industry knew about Rambus's assertions of its patent rights in late 1999. The referenced evidence does not support that implication. In particular, CX1864 is a press release dated June of 2000 and the cited testimony can only standard for the proposition that Mr. Macri learned of the Rambus patent lawsuits prior to September of 2000. Furthermore, RPF 734 is contrary to the weight of the evidence. Rambus filed suit against Hitachi in January of 2000. (CCFF 1995). Rambus only approached other DRAM manufacturers in June of 2000, after licensing Toshiba and settling its case with Hitachi. (CCFF 1954-1958). RPF 734 also implies that the general knowledge gained from press accounts of the Rambus lawsuits is sufficient to inform JEDEC members of Rambus's plans. This implication is misleading and is contrary to the weight of the evidence that even while the Rambus lawsuit against Hitachi proceeded, Rambus sought to spread misinformation to important industry members about its plans, telling them instead that Rambus sued Hitachi because "they are not a Rambus supporter or promoter but they are aggressively promoting DDR." (CX1099A at 1; CCFF1996).

735. From June 2000 to June 2001, even as more companies announced licenses for Rambus's technologies in SDRAM and DDR, JEDEC continued to flesh out the DDR2 specification. According to Mr. Macri, "Well, once you have kind of a -- you know, a list of attributes, major attributes, to create a, you know, a real standard which is in the end a specification, you must add an infinite amount of detail to those attributes. So, this was – during June of 2000 to June of 2001, we were adding the meat, you know, the real description that an engineer would need to truly understand these -- these concepts." (Macri, Tr. 4598-99).

Response to Finding No. 735: The statement in RPF 735 that "JEDEC continued to flesh out the DDR2 specification" is vague and misleading because it implies that during the period June 2000 to June 2001 the DDR-2 standard was being changed. The quoted language makes clear that the work being done in this period involved generating the "real description [of the standard] that an engineer would need to truly understand [it]." Contrary to the implication of

RPF 735, by June of 2000, the committee had reached a "stable point" in its definition of the new standard. (Macri, Tr. 4598).

736. All of this JEDEC work from June 2000 to June 2001 was done in full view of Rambus's patents and in full view of Rambus's assertion – accepted by the over one-half of the industry that had licensed the technologies -- that SDRAM and DDR SDRAM devices infringed certain claims of those patents.

(Macri, Tr. 4753-56 (*in camera*)).

Response to Finding No. 736: The statement in RPF 736 that "all of this JEDEC work from June 2000 to June 2001 was done in full view of Rambus's patents ..." is vague and misleading because it implies that during the period June 2000 to June 2001 the DDR-2 standard was being changed. During this period, the "JEDEC work" on DDR-2 consisted solely of generating a description of the new standard that would allow engineers in the industry to use the standard. (CCRF 735).

737. Even after this fleshing out period described by Mr. Macri, JEDEC still made architectural changes to the DDR2 standard. From June 2001 through September 2001, JEDEC made further architectural changes to the DDR2 standard. (Macri, Tr. 4599). Again, these changes were made with knowledge of Rambus's patents and demands for royalties.

Response to Finding No. 737: RPF 737 is misleading because it implies that the changes made to the DDR-2 specification during the period June 2001 through September 2001 were in some way similar to the changes that the Future DRAM Task Group needed to make to avoid the Rambus patents. The weight of evidence demonstrates that the changes actually made to the DDR-2 standard during this period were not disruptive to the standard because the changes did not remove any functionality, but instead added functionality. (CCFF 3251). Removal of functionality to avoid the Rambus patents at that point would have been disruptive to the DDR-2 standard. (Macri, Tr. 4600-4601 ("[S]ome systems take a very long time to design, and it's really important that,... we provide stability to the designers. If we were to make a change that would cause them to go back and essentially tear up their design, we would be forcing companies to incur

great expense, enormous expense, not only on the design period but also on their product lines. Time to market is extremely critical in this world. You could really devastate a company, even a large company. You could cause such an economic impact to it that, you know, it's possible they may not recover.")).

738. Even as of May 2003, the DDR2 specification had not been finalized. (Rhoden, Tr. 411-12).

Response to Finding No. 738: Complaint Counsel does not disagree.

739. Although JEDEC's design philosophy for DDR2 was to borrow as much as possible from other technologies (CX 140 at 3; Macri, Tr. 4709-10; RX 2234 at 3 (intent of DDR2 design to borrow as many features as possible from other designs); Macri, Tr. 4693)), it is plain from the record that JEDEC did not have to use the Rambus technologies in DDR2 merely because they were used in SDRAM and DDR.

Response to Finding No. 739: Complaint Counsel does not disagree that JEDEC's design philosophy is to borrow as much as possible from previous standards. (CCFF 3236-3237, 3244-3249). However, the statement in RPF 739 that "JEDEC did not have to use the Rambus technologies in DDR2 merely because they were used in SDRAM and DDR" lacks any reference to the record and is contrary to the weight of the evidence. The Future DRAM Task Group had to use DDR SDRAM as the baseline for DDR-2 SDRAM because the benefit to the industry of doing so was that it allowed DDR-2 SDRAM to be backward compatible with the DDR SDRAM. (CCFF 3244). Backward compatibility means that DRAM manufacturers and memory controller manufacturers can design their products to be compatible with both the new standard and the old standard. (CCFF 3245-3246). The benefit of backward compatibility is that it allows the DRAM manufacturers and memory controller manufacturers to produce products that comply with the new standard without subjecting them to the risk that the new standard will be slow to enter the marketplace. (CCFF 3247-3249). The four disputed technologies are in the DDR-2 standard because they were in the previous standard. (CCFF 3250).

740. The April 1998 meeting minutes of the Future DRAM Task Group (the JEDEC subcommittee that developed DDR2) reveal that JEDEC considered entirely different architectures for the next generation DRAM, including architectures based on SLDRAM, Rambus and DDR, as well as packetized and non-packetized architectures. (CX 379A at 9). About one-third of the Task Group voted to base the next generation DRAM on the SLDRAM architecture and one-third voted to use a packetized architecture. (CX 379A at 9).

Response to Finding No. 740: Complaint Counsel agrees that at the very first meeting of the Future DRAM Task Group meeting in April of 1998, the committee discussed what standard should be the baseline for DDR-2 SDRAM. At that meeting the vote in favor of using DDR as the baseline over SLDRAM or RDRAM was: 22 votes for DDR to be the baseline, 12 votes for SLDRAM to be the baseline and 0 votes for RDRAM to be the baseline. (CCFF 3236). As a consequence, by the summer of 1998, DDR SDRAM was chosen to be the baseline for DDR-2 SDRAM. (CCFF 3237).

741. Similarly, a few months later, in September and October of 1998, Joe Macri, the Task Group Chair, presented four possible choices on how to proceed with DDR2 definition, from simply tightening the DDR specifications to a complete change of the logic interface, I/O, and core architecture. (RX 1306 at 9; Macri, Tr. 4621-22).

Response to Finding No. 741: The cited language in RX1306 is unclear as to how it relates to the issues in this case. The cited testimony does not relate to the portion of the document cited. Mr. Macri was a witness in the case but was never asked about the cited language.

1. JEDEC Considered Foregoing Rambus's On-chip PLL/DLL Technology, But Chose to Adopt It Instead of Alternatives.

742. It is plain from the record that JEDEC explored alternatives to the use of Rambus technologies in DDR2. In late 1998, the Future DRAM Task Group wanted to explore eliminating both on-chip DLL and programmable burst length. (RX 1306 at 10; Macri, Tr. 4705). HP was assigned the first task, and IBM the second. (RX 1306 at 10; Macri, Tr. 4705).

Response to Finding No. 742: Complaint Counsel agrees that the record reflects that the Future DRAM task Group assigned action items to HP and IBM to study the impact of removing the DLL from the DDR-2 SDRAM and also of eliminating variable burst lengths. (RX1306 at 8; Macri, Tr. 4705). The record also indicates that the reason that the DLL was

retained was to maintain backward compatibility between DDR and DDR-2 (CCFF 3254; Macri, Tr. 4624 ("Well, we were DDR-based, and you know, the DLL is a part of the clock system of the DDR SDRAM standard, and the clock system is ... one of the most fundamental aspects of the standard, and it was decided since we were DDR-based that we should preserve the clock system to keep the backwards compatibility, that overriding issue of backwards compatibility, you know, keep that easy, and that's why the DLL was left in.")).

743. The December 1998 Future DRAM Task Group Minutes record that HP proposed to eliminate the on-chip PLL in DDR2. (CX 137 at 3, 27). Those minutes also show that IBM proposed to use a vernier mechanism in place of on-chip PLL. (CX 137 at 4).

Response to Finding No. 743: Complaint Counsel agrees that HP made a presentation in December of 1998 to the effect that eliminating the PLL from the DRAM would have numerous benefits including reducing standby power, reducing die area, and making it easier for DRAM designers to implement the new standard in CMOS. (CX0137 at 27 ("(personal) Experience has shown brute force approaches to be superior.")). In the end, the on-chip PLL was retained to ensure backwards compatibility. (CCRF 742).

744. Despite this investigation, and despite Rambus's assertion of its patents in 1999, no alternative to on-chip PLL/DLL was adopted. (RX 1854 at 12-14 (preliminary DDR2 specification showing mode register and extended mode register using DLL Reset, and DLL Enable/Disable, "passed committee ballots and went to council at June 2001 meeting")).

Response to Finding No. 744: RPF 744 is misleading because it implies that the motivation for the discussion described in RPF 742 and 743 were motivated by Rambus's assertion of its patents in 1999. However, the work described in RPF 742 and 743 occurred in late 1998, well before Rambus made its patent position known to the industry. *See* CCFF 1950-1958 for a more complete description of the timing of the Rambus lawsuits. Furthermore, by the time that Rambus made its intentions known, additional reasons existed that eliminated the possibility that the Future DRAM Task Group could change the standard to remove the on-chip PLL/DLL or to

replace dual edged clocking with an alternative technology. *See* CCFF 3253-3261 for a more complete description of difficulties that the industry would have faced if the Task Group had removed those technologies in favor of alternatives in 2000.

745. IBM's Mark Kellogg testified that he would, today, support going to an alternative for on-chip DLL or PLL if there were "predatory IP," that is, intellectual property that is not licensed on reasonable and nondiscriminatory terms. Kellogg also testified that he has no knowledge of Rambus's royalty rates. (Kellogg, Tr. 5245-47).

Response to Finding No. 745: RPF 745 is inaccurate because Mr. Kellogg never testified that he "would, today, support going to an alternative for on-chip DLL or PLL if there were "predatory IP," that is, intellectual property that is not licensed on reasonable and nondiscriminatory terms." Instead, Mr. Kellogg testified repeatedly that he would support the consideration of alternatives for on-chip DLL or PLL if there existed predatory intellectual property on that feature. (Kellogg, Tr. 5245-47).

2. JEDEC Selected Rambus's Technologies With Knowledge Of Rambus's Issued Patents.

746. Even knowing of Rambus's issued patents, JEDEC insisted on choosing Rambus's technologies. While JEDEC considered alternatives, it rejected them and decided to use the Rambus technologies.

Response to Finding No. 746: RPF 746 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

747. Steve Polzin of AMD testifed that he had discussions with DRAM manufacturers in 2000 about alternatives for programmable CAS latency, programmable burst length and dual-edge clocking. (Polzin, Tr. 3988, 3996, 4044). At the time, the DDR2 standard was still winding its way through JEDEC. (Polzin, Tr. 4044-45). Mr. Polzin understood at the time of these discussions that Rambus patents cover these technologies. (Polzin, Tr. 4047-48). The DDR2 standard, however, still specifies programmable CAS latency, programmable burst length, and dual-edge clocking. (Polzin, Tr. 4046-48).

Response to Finding No. 747: Complaint Counsel agrees that Steve Polzin of AMD testified that he had discussions with DRAM manufacturers in 2000 about alternatives for programmable CAS latency, programmable burst length and dual-edge clocking. Mr Polzin testified that Rambus patents were "pretty simple things to work around if we had known about them a long time ago." (Polzin, Tr. 3987-89). By the time Rambus disclosed its patents, it was too late to change the standards. (CCFF 2500-2584, 3229-3261).

748. Complaint Counsel's economic expert conceded that it is unlikely that JEDEC would discuss alternatives in the year 2000 unless at least some significant number of JEDEC members thought that the adoption of the alternatives was feasible at that point in time. (McAfee, Tr. 7571).

Response to Finding No. 748: RPF 748 is inaccurate because Professor McAfee testified only that he agreed that JEDEC would not spend a lot of time discussing technologies in the year 2000 if there was not a sense among at least some significant number of members that those technologies were commercially viable at that point in time. (McAfee, Tr. 7571). There is no record evidence of whether Professor McAfee concluded that JEDEC did, in fact, spend a lot of time discussing technologies in the year 2000.

a. JEDEC Chose Rambus's Programmable CAS Latency Technology Despite Rambus's Issued Patents.

749. In March and April 2000, JEDEC considered alternatives for programmable CAS latency in SDRAM, DDR, and DDR2, including fixed latency, scaling latency with clock frequency, and using pins or additional commands in DDR2. (RX 1626 at 6). At the March 2000 meeting of JC42.3, Micron made a proposal entitled, "Simplifying Read Latency for DDRII." (CX 154A at 27; CX 2758 at 1; Lee, Tr. 6779-80). The proposal included a section on "Avoiding Programmable Latency in SDR/DDR SDRAMs." (CX 154A at 29) The presentation also included a proposed alternative for programmable CAS latency in DDR2. (CX 154A at 30-31; Lee, Tr. 6779-80).

Response to Finding No. 749: Complaint Counsel does not disagree.

750. In response to these proposals, Bob Fusco at Hitachi wrote, "For DDR-2, we have no legacy to live with, so I like the Micron proposal. For DDR-1 it's not too late for minor, carefully considered changes, so I'm open to either proposal." (RX 1626 at 4). This response demonstrates that JEDEC could have adopted alternatives if doing so were preferable.

Response to Finding No. 750: Complaint Counsel does not disagree that RX1626 contains the cited language. However, the language is subject to multiple interpretations. For example, when Mr. Fusco writes that he is "open" to either proposal, it is unclear whether he means that he is willing to consider that proposal or agrees with the proposal. In addition, Mr. Fusco's reference to "legacy" is unclear even to other industry members. (Kellogg, Tr. 5245 ("Bob is a supplier, so when he says "legacy," does he mean supplier legacy or customer legacy")). Mr. Fusco was not called to trial to testify as to his understanding of the document, and there is no evidence that he was unavailable. The final sentence in RPF 750 lacks any reference to the record, constitutes legal argument, and is contrary to the weight of the evidence. (*See* CCFF 2500-2584). In particular, this statement by Mr. Fusco cannot be evidence of what JEDEC would do because Mr. Fusco was not Hitachi's JEDEC representative at the time he made these statements. There is no evidence in the record regarding whether Hitachi's official, voting representatives at the March JEDEC 42.3 meeting, Mr. Udagawa, agreed with Mr. Fusco's sentiments. (CX0154a).

751. Bill Hovis of IBM rejected the proposals regarding alternatives to programmable CAS latency because of cost concerns: "What are we really saving here? . . . Any cost savings has to be off-set with the additional component costs associated with adding new part numbers to satisfy CL=2 and CL=3 demands." (RX 1626 at 3). For DDR, Mr. Hovis still supported programmable CAS latency because "ultimately the flexibility of supporting multiple CAS latencies in one device can result in benefits to the customers that end up buying the memory." (RX 1626 at 3). Mr. Hovis similarly insisted that DDR2 retain programmable CAS latency, even though he was "not currently locked in": "On DDR II devices, I still want multiple CAS latencies supported for the same reasons. Obviously here, the situation with the system is that I am not currently locked in, so the ability to deal with an additional limitation is not as compelling . . . . However, the same arguments given above apply here. One part number is a benefit to system users, not a deficit. Unless the cost delta is significant (DRAM cost difference >2%, 5%???), I suggest we drop this as an issue." (RX 1626 at 3-4).

Response to Finding No. 751: Complaint Counsel does not disagree that RX1626 contains the cited language. However, the language is subject to multiple interpretations and the relevance of the document to the issues in this case is unclear. Mr. Hovis was not called to trial to testify as to his understanding of the document, and there is no evidence that he was unavailable.

Furthermore, Mr. Hovis was not IBM's JEDEC representative in the March 2000 meeting referred to in RX1626. As Mr. Kellogg, IBM's official, voting representative to the JEDEC 42.3 meeting testified, "Bill is actually speaking for customers. He's not the designer. So did I talk to him about it? We discussed it, but it wasn't his decision." (Kellogg, Tr. 5244). In fact, Mr. Kellogg did testify at trial regarding fixed CAS latency and thought it could measurably improve performance over the use of the mode register. (CCFF 2145).

752. In July 2000, Micron made a presentation entitled, "Pin Selectable Posted CAS for DDR II (JEDEC- July 2000- Kevin Ryan)." (CX 2766 at 1). The proposal included using multiple pins "to select specific latency values," which had the trade off of "higher overhead for pins/traces, lower overhead associated with mode register." (CX 2766 at 3). The proposal also stated, "Latency select pin(s) on DRAM can be: hardwired (directly or through jumpers) to the appropriate voltage levels on the module PCB; brought out to pins on the module (requires new/additional latency selection pins on the DIMM); driven by modified SPD device." (CX 2766 at 4).

Response to Finding No. 752: Complaint Counsel does not disagree.

753. JEDEC ultimately opted to use Rambus's programmable CAS latency technology in DDR2. (Polzin, Tr. 4046; RX 1854 at 12-14 (preliminary DDR2 specification showing mode register and extended mode register using programmable CAS latency has passed committee ballots and went to the JEDEC council in June 2001)).

Response to Finding No. 753: Complaint Counsel does not disagree.

b. JEDEC Chose Rambus's Programmable Burst Length Technology Despite Rambus's Issued Patents.

754. JEDEC also decided to adopt Rambus's programmable burst length technology even though it was well aware that Rambus's patents covered the technology.

Response to Finding No. 754: RPF 754 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

755. The preliminary DDR2 specification, published in July 2001, specified a fixed burst length of 4. (RX 1854 at 20; Macri, Tr. 4733-34; Krashinsky, Tr. 2834 (JEDEC based preliminary DDR2 specification on single (fixed) burst length)).

Response to Finding No. 755: Complaint Counsel does not disagree.

756. After that specification was published, both AMD and Intel proposed to change the DDR2 specification to add programmable burst length. (Macri, Tr. 4675). At the September 2001 JC42.3 meeting, Intel proposed that DDR2 have burst length of 8 in addition to 4. (CX 174 at 7-8). At that same meeting, AMD also proposed the addition of a burst length of 8. (CX 174 at 8). According to Intel, adding a burst length of 8 would result in a "[p]otential improvement of 4-10% on high-bandwidth applications." (CX 174 at 37). The vote to ballot this proposal was unanimous. (CX 174 at 7-8).

Response to Finding No. 756: Complaint Counsel does not disagree.

757. Joe Macri, the Future DRAM Task Group chairman, admitted that he was aware when adding programmable burst length to DDR2 that Rambus would believe it infringes its patents. (Macri, Tr. 4679-83).

Response to Finding No. 757: Complaint Counsel does not disagree.

758. JEDEC adopted Rambus's programmable burst length technology in DDR2 despite complete awareness of Rambus's issued patents and demands for royalties. (Polzin, Tr. 4046-47). It is also clear that there was no technological force other than the superiority of Rambus's technology that required JEDEC to adopt Rambus's programmable burst length technology.

Response to Finding No. 758: The first sentence in RPF 757 is not supported by the cited testimony. Mr. Polzin, who was never a JEDEC representative for AMD (Polzin, Tr. 3973), did not testify about JEDEC's "complete awareness" of anything. The second sentence of RPF 758 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Furthermore, the last sentence of RPF 758 is contrary to the weight of evidence that the industry was locked in to the disputed technologies by the time Rambus disclosed their patent rights. (CCFF 2500-2584).

c. JEDEC Chose Rambus's Dual-Edge Clocking Technology Despite Rambus's Issued Patents.

759. JEDEC also tried to find viable alternatives to Rambus's dual-edge clocking technology. The reason the JEDEC committee was looking at alternative clocking schemes was to

avoid Rambus patents. (Krashinsky, Tr. 2828). JEDEC failed to find an acceptable alternative and adopted Rambus's dual-edge clocking technology. (Polzin, Tr. 4047).

Response to Finding No. 759: RPF 759 is inaccurate because it states that JEDEC failed to find an acceptable alternative to dual-edged clocking, citing Mr. Polzin. However, the cited testimony does not include any testimony by Mr. Polzin that JEDEC failed to find an acceptable alternative to dual-edged clocking. In fact, Mr. Polzin testified that he believed that there were acceptable alternatives to dual edged clocking. (Polzin, Tr. 3995 ("Well, the placement of your clock edges and your data is more or less arbitrary. We could have slowed the clock down by half the rate or doubled the rate of the clock itself. Either way would have been reasonable to implement to capture the data.")). Furthermore, RPF 759 is contrary to the weight of the evidence that there were acceptable alternatives to dual-edged clocking (CCFF 2322-2365), and that the reason JEDEC did not adopt those alternatives is that the industry was locked in to the technologies in the standard. (CCFF 2500-2584).

760. At the September 2000 JEDEC meeting, Micron made a proposal that DDR2 incorporate single data rate technology instead of dual-edge clocking. (CX 2769 at 13). Micron made this proposal to convince the committee that they had a better clocking scheme. (Macri, Tr. 4719-20).

Response to Finding No. 760: Complaint Counsel does not disagree.

761. In a November 2000 conference call, committee members discussed going to a single data rate ("SDR") technology. (Macri, Tr. 4639-42). The minutes of that meeting reflect a consensus to try to adopt SDR if it would work. Those minutes state, "HP – prefers SDR" and indicate that for IBM, "Single data rate clocks are acceptable provided that it works." (CX 426 at 2). The minutes also indicate that IBM agreed "with the need to avoid I.P. issues." (CX 426 at 3). The minutes continue, "Majority of companies prefers single data rate clocks but not all of them." (CX 426 at 3). "Discussion on single data rate clock vs. doble [sic] data rate clock . . . . Fundamentally question is that is single data rate clock possible? Micron believes that SDR has some advantages as it gets [rid] of duty cycle issue, it has old prior art, and the inherent bandwidth is better with write than with read. . . . In general, everyone agreed that SDR clock is ok provided that it works." (CX 426 at 4). The overall consensus of the group was: "Single data rate clock is preferred provided we can make it work." (CX 426 at 4).

Response to Finding No. 761: Complaint Counsel does not disagree that CX0426 contains the language cited. However, RPF 763 is misleading because it suggests that there was a consensus at the conference call to replace dual edged clocking with single edged clocking if single edged clocking will work. Testimony at trial indicates that CX0426 was ambiguous on that point. For example, when the representative from HP was shown the portion of CX0426 that states that "HP – prefers SDR" that representative testified "I'm really not sure in which context I -- what it means, exactly refers -- I really don't know if that's exactly what it means." (Krashinsky, Tr. 2825). The representative from ATI, when shown language in the document that stated "prefers single data rate" testified that "[s]ingle data rate – if we were going to make a change, I thought going with a single data rate, you know, a higher speed single data rate clock was the way to go." (Macri, Tr. 4641). The weight of the evidence is that the statements by various representatives in CX0426 that they would prefer single data rate over double data rate is always conditioned by the assertion that they would prefer to keep dual edged clocking, but that they thought that single data rate clocking was acceptable. (Macri, Tr. 4725 - 4726 ("So they first – you know, I think what they're first stating is they want to keep DDR2 as it is, and then if they consider other things, they would go down a different path, and SDR may be a preference.")).

762. Mr. Macri, the chair of the Task Group, believed that everyone knew about Rambus IP at this time; therefore, there was no need to discuss the issue and the JEDEC rules were satisfied even though he did not disclose his knowledge of Rambus patents. (Macri, Tr. 4639-42).

Response to Finding No. 762: Complaint Counsel does not disagree.

763. Despite the consensus to use SDR in place of dual-edge clocking "provided we can make it work," JEDEC incorporated dual-edge clocking into DDR2. (Polzin, Tr. 4047).

Response to Finding No. 763: RPF 763 is misleading because it implies that there was a consensus to replace dual-edged clocking with single edged clocking, but that JEDEC did not replace dual-edged clocking because it could not make single edged clocking work. As

described above, CX0426 reflects a consensus that if dual-edged clocking were to be removed from the DDR-2 SDRAM standard, single-edged clocking was the preferred solution. (CCRF 761). The weight of the evidence also demonstrates that there were a number of concerns in the industry that led to the result that single-edged clocking was not used in the DDR-2 SDRAM standard after the clocking conference call described in CX0426. First, such a change would make the industry's investment in the DDR-2 SDRAM standard up to that time useless as the investments would not be compatible with the DDR-2 SDRAM standard. (CCFF 3258). Second, if the Task Group had attempted to adopt single data rate in the new standard, that had the potential to delay the standard significantly. (CCFF 3259). Third, changing the DDR-2 SDRAM standard to use single-edged clocking would have made the new standard less backward compatible with DDR, making it difficult to design a controller that could support both. (CCFF 3260). Finally, the committee did not adopt single-edged clocking in the DDR-2 SDRAM standard because DRAM customers were opposed to the change. (CCFF 3261).

d. JEDEC Members' Views on the Likely Invalidity of Rambus's Patents Have Influenced Their Design Choices.

764. Complaint Counsel have contended that JEDEC chose the Rambus technologies in DDR2 because the industry was "locked in" to those technologies. As discussed above, however, JEDEC members knew of Rambus's patents while the DDR2 design phase was still ongoing, and they chose the Rambus technologies even though they acknowledged that "[f]or DDR-2, we have no legacy to live with" and are "not currently locked in . . . ." (RX 1626 at 3-4).

Response to Finding No. 764: The proposed finding is contrary to the weight of the evidence which shows that the DRAM industry was already locked-in with regard to DDR2 by the time that it became aware that Rambus believed its patents were applicable. (CCFF 3229-3261; CCRF 732-747). The finding is also misleading because the cited document does not support the contention in the finding that JEDEC members acknowledged that "[f]or DDR-2, we have no legacy to live with" and are "not currently locked in . . ." Rather the cited document

reflects the opinion of two individuals, neither of whom testified with regard to the cited e-mails. Further the context of the cited language restricts the comments to one technology, CAS latency.

765. There is also substantial evidence that JEDEC members have based their adoption of the Rambus technologies in part on their view that any Rambus patents covering those technologies are, or are likely to be held to be, invalid because of prior art.

Response to Finding No. 765: RPF 765 lacks any reference to the record and is inappropriate for findings of fact]. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Mark Kellogg of IBM testified, for example, that he examined Rambus's patents in 2001. (Kellogg, Tr. 5301). With respect to the technologies in SDRAM and DDR, Mr. Kellogg testified that he believed that there was prior art to Rambus's patents, and he said that he had conveyed his opinion to other DRAM manufacturers. (Kellogg, Tr. 5301-02). According to Mr. Kellogg, the DRAM manufacturers "were considering the fact that some of the Rambus patents might be overturned" when making decisions about whether to try to design around Rambus patents. (Kellogg, Tr. 5303-04).

766. Mark Kellogg of IBM testified, for example, that he examined Rambus's patents in 2001. (Kellogg, Tr. 5301). With respect to the technologies in SDRAM and DDR, Mr. Kellogg testified that he believed that there was prior art to Rambus's patents, and he said that he had conveyed his opinion to other DRAM manufacturers. (Kellogg, Tr. 5301-02). According to Mr. Kellogg, the DRAM manufacturers "were considering the fact that some of the Rambus patents might be overturned" when making decisions about whether to try to design around Rambus patents. (Kellogg, Tr. 5303-04).

Response to Finding No. 766: The statement in the proposed finding [Mark Kellogg of IBM testified, for example, that he examined Rambus's patents in 2001. (Kellogg, Tr. 5301)] implies that Mr. Kellogg examined all of Rambus's patents in 2001. Mr. Kellogg, in fact, testified at the cited pages that he was "involved in studies of some number of Rambus patents". The statement in the proposed finding [With respect to the technologies in SDRAM and DDR, Mr. Kellogg testified that he believed that there was prior art to Rambus's patents, and he

said that he had conveyed his opinion to other DRAM manufacturers.] is incomplete and misleading. Mr. Kellogg testified that he did not believe he shared his opinion on whether Rambus' patents would be eventually held invalid because of prior art. He also testified that prior art and the applicability to patents is not determined by engineers. (Kellogg, Tr.5302) He further testified that he did not share any official position and any documentation that he had prepared. (Kellogg, Tr. 5302)

767. JEDEC members have on many occasions expressed the view that any Rambus patents would be barred by prior art.

Response to Finding No. 767: RPF 767 lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. On the very first occasion that Rambus's potential patents were discussed at JEDEC, one or more members asserted that any such patents would likely not issue or be held invalid because of prior art.

768. On the very first occasion that Rambus's potential patents were discussed at JEDEC, one or more members asserted that any such patents would likely not issue or be held invalid because of prior art.

Response to Finding No. 768: RPF 768 lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Additionally, RPF 768 is incomplete because, as Mr. Crisp testified at trial, Howard Sussman stated at the same May 1992 meeting that he had seen the foreign Rambus patent application and that he believed would not be a concern for the JEDEC SDRAM standardization effort. Mr. Crisp further testified that he did not contradict what Mr. Sussman stated. (Crisp, Tr. 3067-68; CCFF 906; CX2092 at 128-130).

769. At the May 1992 JEDEC meeting, NEC representative Howard Sussman stated that he had reviewed the claims in Rambus's PCT application and that, in his opinion, many of the 150 claims were barred by prior art. (RX 290 at 3; CX 673 at 1).

Response to Finding No. 769: RPF 769 is incomplete because, as Mr. Crisp testified at trial, Howard Sussman stated at the same May 1992 meeting that he had seen the foreign Rambus patent application and that he believed would not be a concern for the JEDEC SDRAM standardization effort. Mr. Crisp further testified that he did not contradict what Mr. Sussman stated. (Crisp, Tr. 3067-68; CCFF 906; CX2092 at 128-130).

770. Notes taken at the May 1992 JC 42.3 meeting by IBM representative Mark Kellogg state: "NEC: Rambus International Patent 150 pages, Motorola patents/Rambus patent – suspect claims won't hold." (RX 290 at 3; Kellogg, Tr. 5319).

Response to Finding No. 770: RPF 770 is incomplete because, as Mr. Crisp testified at trial, Howard Sussman stated at the same May 1992 meeting that he had seen the foreign Rambus patent application and that he believed would not be a concern for the JEDEC SDRAM standardization effort. Mr. Crisp further testified that he did not contradict Mr. Sussman. (Crisp, Tr. 3067-68; CCFF 906; CX2092 at 128-130).

771. In an email recounting the meeting, Richard Crisp wrote, "Siemens expressed concern over potential Rambus Patents covering 2 bank designs. . . . In response to the patent issue, Sussman stated that our patent application is available from foreign patent offices, that he has a copy, and has noted many, many claims that we make that are anticipated by prior art. He also stated the Motorola patent predated ours (not the filing date!) and it too was anticipated by prior art." (RX 673 at 1). Mr. Crisp understood the gist of Mr. Sussman's statement to be that "everything that he thought Rambus had invented, somebody else had invented first." (Crisp, Tr. 3492-93).

Response to Finding No. 771: RPF 771 is incomplete because, as Mr. Crisp testified at trial, Howard Sussman stated at the same May 1992 meeting that he had seen the foreign Rambus patent application and that he believed would not be a concern for the JEDEC SDRAM standardization effort. Mr. Crisp further testified that he did not contradict Mr. Sussman. (Crisp, Tr. 3067-68; CCFF 906; CX2092 at 128-130).

772. Siemens' JEDEC representative Willi Meyer prepared a trip report from the May 1992 JC 42.3 meeting that states, "Siemens and Philips concerned about patent situation with regard to Rambus and Motorola. No comments given. *Motorola patents have priority over Rambus'*. Rambus patents filed but pending." (RX 297 at 5) (emphasis added).

Response to Finding No. 772: RPF 772 is incomplete because it ignores the fact that Mr. Meyer also testified that after Rambus disclosed the '703 patent, that he concluded Rambus "had nothing to report which related any more to the work of our committee . . . and developing the synchronous DRAM" (CX2089, Meyer, Infineon Trial Tr., 149-150). RPF 772 is also incomplete because Mr. Meyer testified that when Chairman Gordon Kelley asked Mr. Crisp in May 1992 if he had any comment, "it was clear to all the participants..." that "the committee was trying to figure out whether Motorola or Rambus had anything to report to the committee..." (*Id.*, 135-37). To this question, Mr. Crisp "just shook his head" (*Id.*).Mr. Meyer also testified that sixteen months later, at the September 1993 JC 42 meeting, there was an additional discussion of Rambus's patent applications in which someone said that the applications were "stuck in the patent office" and not proceeding right now." (CX 2057 12/13/00 Depo., 300:7-23). The speaker then referred to Rambus's patent applications as "a collection of prior art." (*Id.*).

773. Mr. Meyer also testified that sixteen months later, at the September 1993 JC 42 meeting, there was an additional discussion of Rambus's patent applications in which someone said that the applications were "stuck in the patent office" and not proceeding right now." (CX 2057 12/13/00 Depo., 300:7-23). The speaker then referred to Rambus's patent applications as "a collection of prior art." (*Id.*).

Response to Finding No. 773: RPF 773 is incomplete because it ignores the fact that Mr. Meyer also testified that after Rambus disclosed the '703 patent, that he concluded Rambus "had nothing to report which related any more to the work of our committee . . . and developing the synchronous DRAM" (CX2089, Meyer, Infineon Trial Tr., 149-150).

774. In 1994, during a presentation to Samsung, Dr. Betty Prince summarized the sentiment in the industry that Rambus's patents were anticipated by prior art. Dr. Prince's presentation stated that "[m]any of the large systems houses believe that Rambus patents are challengeable by previous internal work and/or patents." (RX 153 at 10). This was public

information that Dr. Prince had gathered for Samsung. (Prince, Tr. 9003). The presentation went on to state, "The early concern about the impact of the Rambus patents on the major systems houses seems to have diminished considerably." (RX 2153 at 10).

Response to Finding No. 774: The proposed finding does not support Respondent's contention that views on the likely invalidity of Rambus's patents have influenced their design choices. In fact, it supports exactly the opposite view. Dr. Prince testified that she gave the cited presentation to Samsung to help Samsung determine whether or not to license the Rambus DRAM. (Prince, Tr. 9015) The fact that Samsung licensed the Rambus DRAM (CX1592) even though it had been made aware of the fact that Rambus patents may be challengeable on a prior art basis indicates that they were not influenced by this knowledge.

The proposed finding is also incomplete. First, the context from the cited page of RX 2153 cites four technologies that are potential areas for patents. None of these four technologies are at issue in the current litigation. In fact, Dr. Prince testified that she did not contemplate that the four technologies at issue in the current litigation (Programmable CAS latency and burst length, dual edge clocking and on-chip PLL/DLL) may be covered by Rambus patents and did not include them in the list of technologies that Rambus patents might cover. (Prince, Tr. 9022-9028. Further, Dr. Prince testified that the large systems houses mentioned in the finding referred to users rather than vendors of DRAMs.

775. As Dr. Prince explained at trial, industry participants believed that Rambus's patents would be invalid due to prior art: "When Rambus first started talking about their product, they were very secretive and nobody really knew what they had. After it was clear what they had, then many of the big companies reviewed the patents that they had already – prior work that they had already had and there was discussion various places in the industry that much of this seemed to have prior art." (Prince, Tr. 9004). Dr. Prince testified that this information was from public sources. (Prince, Tr. 9004).

Response to Finding No. 775: The proposed finding is incomplete and does not support Respondent's contention that views on the likely invalidity of Rambus's patents have influenced their design choices. In fact, despite the cited testimony that companies believed there

may applicable prior art, the evidence shows that the DRAM manufacturers entered into license agreements with Rambus for its RDRAMs and Direct RDRAMs. (CCFF 1605-1615; *See* e.g.CX1592; CX1599; CX1600; CX1609; CX1617; CX1646; CX1680; CX1681; CX1683; CX1685; CX1686; CX1687; CX1689) which indicates that knowledge of potentially applicable prior art did not influence their design choices.

776. A November 6, 1995 Mitsubishi memorandum regarding "Request for Cray Patent Investigation as a Countermeasure for the Rambus Patent" states: "In response to the directive from the U Memory Department, we did a prior art search regarding the patents owned by Rambus, emphasizing the patents by Cray Corporation, and have found at least three issues that are potentially prior art for the Rambus patent." (RX 660A at 3).

Response to Finding No. 776: The proposed finding is incomplete and does not support Respondent's contention that views on the likely invalidity of Rambus's patents have influenced their design choices. In fact, it supports the opposite contention because Mitsubishi, in fact, signed a license agreement with Rambus covering Direct RDRAM in February 1997 (CCFF 1611) despite the fact that it had knowledge of potentially applicable prior art.

777. Mitsubishi followed up with Cray Corporation, and received some additional reassurance. In a November 28, 1995 e-mail, Alan Grossmeier of Cray wrote to Kazutami Ariomoto in Mitsubishi's Memory Devices Department that, based on Cray work, "[w]e have not been concerned about infringing on Rambus patent since if dispute would occur we believe we have sufficient *prior art* to show." (RX 660 at 1).

Response to Finding No. 777: The proposed finding is unreliable. The cited e-mail is partially in Japanese. Further the cited statement is made in reference to patents on Cray's "memory architecture design" which is according to the e-mail "similar in some ways to the Rambus architecture". (RX-660 at 1) The e-mail does not state what the Cray memory architecture design is and how it is similar to Rambus. The exhibit was never shown to a witness, despite the fact that Rambus called Alan Grossmeir to testify.

Further, the proposed finding does not support Respondent's contention that views on the likely invalidity of Rambus's patents have influenced their design choices because Mitsubishi in

fact signed a license agreement with Rambus covering Direct RDRAM in February 1997 (CCFF 1611) despite the fact that it had knowledge of potentially applicable prior art.

778. A 1996 Micron email also shows that Micron believed Rambus's patents would be invalid due to prior art: "We have also been investigating the prior art related to the area of high-speed DRAMs. From our research, we think many RAMBUS patents read on prior art or other patents." (RX 829 at 2).

Response to Finding No. 778: This RPF is misleading in suggesting that "Micron believed Rambus's patents would be invalid due to prior art" because the quoted portion is taken out of context. The reference to "prior art" is in the context of licensing discussions for the Rambus RDRAM and appears under the heading "reasons for lower royalty." (RX 829 at 2).

779. It is clear that JEDEC engineers were confident of their ability to detect the existence of prior art in the DRAM arena. As Howard Sussman, who represented NEC and then Sanyo at JEDEC meetings, explained, although the engineers who attended JEDEC meetings were "not really the experts" on construing patent claims, "[f]or prior art, we most likely have knowledge." (Sussman, Tr. 1344).

Response to Finding No. 779: The opening sentence that JEDEC engineers were confident of their ability to detect the existence of prior art is unsupported by evidence. The statement from Mr. Sussman used as an example in the proposed finding when cited in full shows that the engineers at JEDEC were not in fact qualified to determine the validity of a patent (including, supposedly the applicability of prior art) as well as construing claims. (Sussman, Tr. 1344 ("You know, we're a grouping of engineers, not a grouping of patent attorneys, so what is the real validity of a patent, how is it constructed, what are the claims, we're not really the experts.")

780. It is also clear that in the face of explicit warnings that the Ramlink and SyncLink devices may violate Rambus's intellectual property rights, the DRAM manufacturers developing these devices continued to do so. For example, although there was no assurance that Ramlink did not infringe Rambus's patents, the Ramlink standard was issued by the IEEE. (Gustavson, Tr. 9300-01). The SyncLink work also proceeded, despite warnings by Rambus that the device might violate Rambus's patents. As Mr. Wiggers explained at trial, "the SyncLink work went forward, yes, based on the fact that we still felt we were in the public domain, that everything we had done was, you know, based on things that had been done in the public domain. . ." (Wiggers, Tr. 10604). Mr. Wiggers testified that he did not take Rambus's patent position very seriously. (Wiggers, Tr. 10604).

Response to Finding No. 780: RPF 780 constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.Furthermore, this proposed finding is irrelevant for the reasons discussed in CCRF 1491-1492. IEEE was a separate organization to JEDEC with a different membership and patent disclosure rules. The IEEE membership were individuals rather than companies (CCFF 1502) and the IEEE procedures did not impose any obligation on companies with respect to patent disclosure. (CCFF 1503). Dr. Gustavson testified that he has never been a member of JEDEC and has no knowledge of the JEDEC disclosure policy. (Gustavson, Tr. 9316)

Further, Dr. Gustavson's testimony shows that when IEEE was made aware of Rambus patents, it did not proceed. Rather it suspended balloting of the Ramlink standard because of concerns about the Rambus intellectual property. (Gustavson, Tr. 9292). It then sought RAND assurance from Rambus. (CCFF 1538). When Rambus refused to give such an assurance, the IEEE requested that the Ramlink working group redesign the Ramlink standard so that it wouldn't violate Rambus patent claims. (Gustavson, Tr. 9296-9297; CCFF 1540). Although the IEEE eventually issued the proposed Ramlink standard, no product implementing the Ramlink standard ever came to market. (Prince, Tr. 9012)

The proposed finding is incomplete and misleading because it fails to take into account that Synclink consortium members were concerned to avoid Rambus patents. (CCFF 1572) Further, the Synclink architecture was not accepted within the industry and never went into volume production. (CCFF 1587)

781. Also in 1997, Craig Hampel of Rambus was informed that Desi Rhoden, currently JEDEC's Chairman of the Board, "was commenting that it looked like there was going to be prior art on Rambus, that would make our patents difficult to defend." (RX 908 at 1).

Response to Finding No. 781: The proposed finding is unreliable. The cited document was never used with a witness despite the fact that both Mr. Rhoden and Mr. Hampel testified at trial. The e-mail does not indicate who noted Mr. Rhoden's comment. Mr. Harmon notes in the e-mail that no specifics were given as to what prior art may cover Rambus patents. The finding also does not support Respondent's contention that views on the likely invalidity of Rambus's patents have influenced DRAM manufacturer design choices.

782. Mr. Rhoden testified that he recalls hearing discussions at dinner parties in the 1997 time period about there being prior art with respect to the Rambus patents. (Rhoden, Tr. 712).

Response to Finding No. 782: The proposed finding is incorrect, incomplete and misleading. Mr. Rhoden testified that he probably [emphasis added] heard statements about prior art with respect to the Rambus patents and testified that it was not unusual for people to talk about prior art for many things (Rhoden, Tr. 714-715 ("Some people would talk about prior art for many things, and when something was very active, there were discussions at that time was IP around, something relevant to what was going on at that company, and I think at that time Rambus was probably pretty active in the press, and so I suppose the topic of Rambus came up, perhaps because of that.")) The finding does not support Respondent's contention that views on the likely invalidity of Rambus's patents have influenced DRAM manufacturer design choices.

783. Hans Wiggers of HP testified that if Richard Crisp had claimed at a JEDEC meeting that Rambus had invented dual-edge clocking, he would have said that Rambus could not patent that technology because it was a known technology. (Wiggers, Tr. 10588). This is understandable; Mr. Wiggers thought he had a patent on that technology. (Wiggers, Tr. 10607).

Response to Finding No. 783: The proposed finding is incomplete. Mr. Wiggers also testified that he has not formed an opinion as to whether Rambus patents are inval*id.* (Wiggers, Tr. 10584) The cited testimony is also contrary to the weight of the evidence which establishes that JEDEC members would have pursued alternative technologies or negotiated

acceptable royalty rates if they had known that Rambus believed its intellectual property covered dual edge clocking. (CCFF 2101-2107, 2322-2365, 2441-2464)

784. Given these views, it is not surprising that the DRAM manufacturers have continued to use Rambus's technologies despite knowing of Rambus's patents.

Response to Finding No. 784: The proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

B. There Were No Viable Non-Infringing Alternatives To Rambus's Technologies.

785. Though JEDEC continued to adopt Rambus's technologies into new standards despite knowledge of Rambus's issued patents and demands for royalties, Complaint Counsel nonetheless contend that there were several alternatives that JEDEC would have adopted had Rambus made the additional disclosures Complaint Counsel allege should have been made. Complaint Counsel's technical expert, Professor Jacob, testified that several alternatives were "technically viable." Complaint Counsel's economic expert, Professor McAfee, testified that certain of these "technically viable" alternatives were "commercially viable." The evidence shows, however, that each of the alternatives identified by Complaint Counsel's experts are either covered by Rambus's patents or are inferior to the Rambus technologies in cost-performance terms.

Response to Finding No. 785: Respondent does not cite any evidentiary support for RPF 785. Because RPF 785 lacks any reference to the record, Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. The first sentence in RPF 785 is inaccurate because the record evidence does not support Rambus's contention that the alternative technologies were inferior to Rambus's technologies in terms of cost and performance. (*See, e.g.*, CCFF 2108-2129, 2132, 2236, 2335, 2394).

The last sentence in the RPF 785 is also contrary to the weight of the evidence. (CCFF 2101-2464). In those instances where Rambus actually presented evidence at trial that a Rambus patent covered an alternative technology, that evidence was unreliable. (CCFF 2182 (scaling cas

latency with clock frequency), 2292-2295 (using a dedicated pin to set burst length), 2300-2303 (identifying burst length in the command)). In those instances where Rambus actually presented evidence at trial that the alternative technology would still require use of Rambus's technology, that evidence is unreliable. (CCFF 2207-2210 (using a dedicated pin to store cas latency), 2224-2225 (identifying cas latency in the command), 2348-2349 (interleaving on-chip banks)).

1. The Testimony Of Professor Jacob Regarding Allegedly Viable Alternatives Is Entitled To Little Weight.

a. Professor Jacob Does Not Have Sufficient Experience In Circuit Design.

786. Complaint Counsel's expert witness regarding viable alternatives, Professor Jacob, has never done DRAM circuit design. (Jacob, Tr. 5588). Indeed, Professor Jacob had never designed any circuits for computer chips (even apart from DRAMs) that were to be fabricated prior to 2002. (*Id.*). Aside from looking at some DRAM data sheets, Professor Jacob, who was a student at the time, had no particular DRAM-related experience in the mid-1990s. (Jacob, Tr. 11148).

Response to Finding No. 786: RPF 786 is incomplete because it ignores the substantial amount of familiarity and experience that Professor Jacob has with DRAMs. Professor Jacob has specialized in the study of computer memory systems, "meaning DRAM systems and cache systems." (Jacob, Tr. 5353-54). In the mid-1990s, Professor Jacob obtained a master's and a Ph.D. in computer engineering from the University of Michigan, where he was trained as a computer architect and "studied the design of complex chips and systems of chips, so, for example, CPU chips, memory controller chips and DRAM chips." (*Id.* 5356-57). Both his master's thesis and dissertation involved the study and performance of DRAM-based memory systems. (*Id.* 5356-57).

In the fall of 1997, Professor Jacob became a professor at the University of Maryland where he has continued to study DRAM architectures. (Jacob, Tr. 5357). Starting in the late 1990s, Professor Jacob has researched and published comparative studies on the performance of EDO

DRAM, SDRAM, DDR SDRAM, SLDRAM, and DDR II SDRAM. (*Id.* 5357-62). Three papers on that comparative research have been subject to peer review and published in two prestigious computer engineering journals: the International Symposium on Computer Architecture and IEEE Transactions on Computers. (*Id.* 5359-61). Today, Professor Jacob continues to direct a large group of Ph.D. students "who are investigating advanced issues in the design of DRAMs and DRAM systems." (*Id.* 5362). Currently, Professor Jacob and his studies are taking their combined research efforts and collaborating to write a treatise on DRAM systems and architectures. (*Id.*).

For his work in DRAM systems and architectures, Professor Jacob received the Prestigious Career Award from the National Science Foundation. (Jacob, Tr. 5360).

787. By contrast, Respondent's technical experts have a wealth of relevant experience in the DRAM and semiconductor industries. Dr. Soderman was employed in the semiconductor industry for over 30 years during which time he designed DRAMs as well as various other types of integrated circuits. (Soderman, Tr. 9329-36).

Response to Finding No. 787: RPF 787 is inaccurate. (*See* CCFF 2108-2115). Contrary to Professor Jacob's experience throughout the 1990s, most of Dr. Soderman's experience in that time frame did not involve DRAM. (CCFF 2109-2111, 2113). Instead, Dr. Soderman's primary experience from 1981 to 1997, at ASIC Design & Marketing, Xilinx, Intel, and LSI Logic, involved programmable logic and gate arrays, not DRAMs. (Soderman, Tr. 9338-43). Much of Dr. Soderman's recent experience has involved the sale of software. (*Id.* 9337-38).

Dr. Soderman never designed an SDRAM and DDR SDRAM, nor did he design a JEDEC-compliant DRAM. (Soderman, Tr. 9342-44). Dr. Soderman's DRAM-related design experience ended in the late 1970s. (*Id.* 9342-43). The DRAM he designed was used in typewriters. (*Id.* 9343).

788. Likewise, Mr. Geilhufe worked in the semiconductor industry for over 30 years. (Geilhufe, Tr. 9543-52). Mr. Geilhufe holds four patents for DRAM design, and managed Intel's international manufacturing operations which involved working closely with DRAM manufacturers such as Samsung. (Gelhufe, Tr. 9549-50, 9553).

Response to Finding No. 788: RPF 788 is incomplete. (*See* CCFF 2108-2109, 2112-2114). During the relevant time period, Mr. Geilhufe was not involved in or supervising the design of DRAMs. (Geilhufe, Tr. 9627-28). The last time Mr. Geilhufe formally contributed to a DRAM design was sometime in the late 1980s. (*Id.* 9625-26). Mr. Geilhufe's last hands-on DRAM design experience was in 1978. (*Id.* 9626).

From 1999-2000, Mr. Geilhufe worked at Winbond. (Geilhufe, Tr. 9628). Winbond did not design any DRAMs. (*Id.* 9628-29). Mr. Geilhufe's manufacturing experience at Winbond was limited to being aware of the volumes and types of DRAMs that were being manufactured and the profitability of the DRAM business. (*Id.* 9629).

789. Professor Jacob's relatively recent experience also pales beside that of Drs. Farmwald and Horowitz. When Drs. Farmwald and Horowitz made their inventions in the late 1980s and early 1990s, Dr. Farmwald had already founded a computer company, while Dr. Horowitz had been a professor of electrical engineering for a number of years. *See* Findings ¶¶ 27, 43). Professor Jacob did not obtain his graduate degree and begin to teach electrical engineering until 1997. (Jacob, Tr. 5357).

Response to Finding No. 789: The first sentence in RPF 789 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that the first sentence of RPF 789 should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Respondent states that Professor Jacob's experience "pales" in comparison to Drs. Farmwald and Horowitz without identifying any foundation in the record to make such a statement.

Respondent has failed to articulate how the relative experience of Drs. Farmwald and Horowitz in comparison to Professor Jacob, as presented in RPF 789, is relevant to determining the sufficiency of Professor Jacob's experience to render opinions in this case. Both Drs. Farmwald and Horowitz were fact witnesses, and not experts, in this case, and testified primarily with respect to their experiences with RDRAM. Dr. Farmwald testified that he never considered alternatives to

the technologies at issue in this case. (*See, e.g.*, Farmwald, Tr. 8289-90 (Dr. Farmwald did not believe there were any alternatives to Rambus's technology and therefore he did not remember thinking about alternatives "one way or the other.")). To the extent that Dr. Horowitz considered alternatives to the technologies at issue in this case, he testified that he discussed a number of the alternatives proposed by Professor Jacob with his students. (Horowitz, Tr. 8559 (he discussed asynchronous as an alternative to synchronous memory with Ph.D. students), 8561 (he discussed several alternatives to the use of on-chip PLL/DLL with former students who worked at Rambus), 8563 (he discussed the use of simultaneous bi-directional I/O with students)).

The work that Professor Jacob did to evaluate alternatives to the technologies at issue in this case goes beyond any personal understanding that Drs. Farmwald and Horowitz has or may have had regarding alternatives. Professor Jacob consulted a large range of engineering material, including treatises, technical articles, and material that was available on the Web to evaluate alternative technologies. (Jacob, Tr. 5367-68). He read all the relevant JEDEC minutes from the 1991-1996 time period, and read through the presentations made at those JEDEC meetings as well as a large volume of additional documents. (*Id.* 5368, 5369). He also reviewed a considerable number of deposition and trial transcripts.

RPF 789 is misleading because it fails to identify the type of experience at issue. Professor Jacob has a different type of experience from that of all the fact witnesses in this case. While most of the fact witnesses focused on architectural design, specific circuit design, or business aspects of their jobs, Professor Jacob studied the performance of different types of memory in various computer architectures. Professor Jacob's knowledge of the performance parameters and characteristics of various types of memory designs and architectures compliments the many, many years of specific architectural, design, and manufacturing experience of fact witnesses such as Messrs. Sussman, Rhoden, Kelley, Kellogg, Lee, Peisl, Macri, Shirley, and Reczek. The fact that

Professor Jacob – relying on his academic and experimental experience modeling, building, and testing various alternative memory systems – included among his set of available alternatives many of the same technologies that the fact witnesses proposed for use at JEDEC or otherwise considered based on their professional design work, serves to confirm that these alternatives were viable from both a performance and a practical design point of view.

b. Professor Jacob's Analysis of His Proposed Alternatives Was Inadequate.

790. By contrast to his publications comparing certain DRAM architectures, in which Professor Jacob tried to model their performance as precisely as possible using software simulation, Professor Jacob did no such software simulation with respect to the alternatives that he proposed to Rambus's technology. (Jacob, Tr. 5589).

Response to Finding No. 790: RPF 790 does not support the conclusion that Professor Jacob's analysis of his proposed alternatives was inadequate because the questions he was asked to answer regarding alternative technologies in this case was substantially different from the questions he was attempting to address in his publications. (*Cf.* Jacob, Tr. 5363 (explaining the question he was asked to address regarding alternatives in this case) with 5358 (explaining the nature of his 1998 research on different DRAM architectures)).

In this case, Professor Jacob was asked to determine whether alternatives gained from his past studies and simulations to the four technologies at issue in this case existed at the time that JEDEC was considering whether to include those technologies into the standards. (*Id.* 5363). He therefore relied extensively on his understanding of different features of various types of DRAM as well as features used in other types of products such as SRAM and VRAM. In his 1998 study, Professor Jacob did a very accurate modeling of different DRAM architectures, including SDRAM, concurrent Rambus, and direct Rambus, in order "to determine what the performance differences would be and why." (*Id.* 5358). He also modeled additional architectures for his 2001 publication and a memory controller for his later publication. (*Id.* 5360, 5361, respectively). To

confirm his conclusions, Professor Jacob consulted a lot of JEDEC related material and confirmed his interpretation of that material with JEDEC participants and other DRAM engineers. (Jacob, Tr. 5367-69). Professor Jacob's review of these documents indicated that engineers in JEDEC considered many of the same technology that Professor Jacob did and in some cases actually did work with them or had practical experience with them. (CCFF 2102-07, 2130-2414). While Professor Jacob consulted an enormous amount of JEDEC meeting minutes, reviewed presentations that were made at those meetings, and confirmed his understanding about those presentations with JEDEC participants and other DRAM engineers (Jacob, Tr. 5368-69), Messrs. Soderman, Geilhufe, and Rapp failed to adequately consider JEDEC materials in their analysis. (CCFF 2115, 2117, 2119-2120 (Soderman); CCFF 2115, 2118-2119, 2121 (Geilhufe); CCFF 2698-2700 (Rapp)).

Dr. Soderman failed to consider a number of critical presentations at JEDEC. (Soderman, Tr. 9493, 9493-94, 9503-04). Mr. Geilhufe never reviewed any JEDEC meeting minutes or any JEDEC policy manuals. (Geilhufe, Tr. 9622). Dr. Soderman and Mr. Geilhufe failed to interview anybody who attended JEDEC meetings during the relevant time period. (Soderman, Tr. 9447-48, 9472, 9488, 9491, 9503, 9506-07; Geilhufe, Tr. 9623). Mr. Geilhufe did not do anything to ensure that the analysis that he did was the type of analysis that was done at JEDEC. (Geilhufe, Tr. 9622).

Dr. Rapp reviewed no JEDEC materials/minutes other than two technical specifications. (Rapp, Tr. 9994; *see* DX0324; CCFF 2698). Nor did he review any notes or reports on JEDEC activities. (Rapp, Tr. 9995; *see* DX0324; CCFF 2699). Nor did he review any of the Rambus/JEDEC/third-party records cited in Professor McAfee's report. (Rapp, Tr. 9999; *see* DX0324; CCFF 2700).

791. With the exception of three of his alternatives (using a burst terminate command, increasing the number of pins on the DRAM, and increasing the number of pins on the module),

Professor Jacob did no simulation or modeling of any kind to try to assess the alternative's performance. (Jacob, Tr. 5590-91).

Response to Finding No. 791: RPF 791 does not support the conclusion that Professor Jacob's analysis of the remaining proposed alternatives was inadequate for the same reasons stated in response to RPF 790.

792. Professor Jacob's proposed alternatives were not sufficiently detailed to enable an actual circuit design. (Geilhufe, Tr. 9673).

Response to Finding No. 792: PRF 792 is misleading; Professor Jacob's proposed alternatives were at the same level of detail as the various alternatives proposed at JEDEC, and thus reflected the analysis that JEDEC likely would have undertaken had Rambus disclosed the potential scope of its patent rights. (CCFF 2101-07, 2130-2414).

793. Professor Jacob did not do any investigation to determine whether any of his proposed alternatives was covered by patents owned by Rambus or others. (Jacob, Tr. 5601).

Response to Finding No. 793: Complaint Counsel has no specific response to RPF 793, although it should be noted that Respondent has not presented any reliable evidence that patents owned by Rambus or others cover any of Professor Jacob's proposed alternatives. (*See generally* CCFF 2125-2129; *see also* CCFF 2183, 2292-2295, 2300).

2. To Understand Whether A Particular Alternative Is Viable, The Relevant Cost Factors Must Be Considered.

794. The primary cost factors to be considered in evaluating an alternative DRAM technology are costs relating to: (1) process and storage cell/array; (2) product design; (3) wafer plant; (4) photo tooling; (5) wafer sort; (6) good die yield; (7) packaging; (8) final test and good unit yield; (9) inventory; (10) qualification; and (11) board complexity. (Geilhufe, Tr. 9564-74).

Response to Finding No. 794: RFP 794 does not support the conclusion that each of the cost factors must be considered in order to understand whether a particular alternative is viable because it ignores the fact that JEDEC often does not and cannot consider all of these factors when deciding which technologies to incorporate into standards.

Mr. Geilhufe used his own methodology to evaluate the commercial viability of proposed alternatives. (Geilhufe, Tr. 9674). Mr. Geilhufe did not attempt to understand whether his methodology was consistent with how JEDEC evaluated technologies for inclusion in a standard. (*Id.* ("I have no knowledge of how JEDEC folks did their analysis or if they did an analysis.")). The only factors that are relevant to evaluate commercially viable alternatives in this case, however, are the factors that enter into JEDEC's decision-making process. (McAfee, Tr. 7335; CCFF 2772).

RPF 794 and Mr. Geilhufe ignore the fact that JEDEC is a consensus-based organization. (CCFF 2650; *see also* CCFF 239-255). JEDEC does not make choices about what to include in a standard based upon a determination of what the best available technology is. (CCFF 2650). Instead, JEDEC "satisfices" in choosing technologies to incorporate into the standard, which means that JEDEC will choose an adequate solution to a problem it faces rather than expending the effort to find the perfect solution. (CCFF 2650, 2656; *see also* CCFF 124).

Furthermore, RPF 794 and Mr. Geilhufe ignore the fact that some uncertainties about a technology may exist when it is selected for incorporation into the standard. (CCFF 130-131). Nor do they take into account the substantial evidence that factors besides cost influence whether or not a particular technology is included in a standard. (CCFF 122-124 (indicating that time to market influences JEDEC members); CCFF 129 (indicating the degree to which there is an existing need for a particular technology will influence whether or not JEDEC will adopt it for standardization); CCFF 130-131 (indicating that the lack of sufficient information on a particular technology will influence what is adopted and/or when it is adopted)).

795. The largest part of a DRAM, approximately 90 percent of the active area, consists of the memory array, that is the memory cells and related circuitry. (Geilhufe, Tr. 9560). The remaining 10 percent consists of peripheral circuitry. (*Id.*). Circuitry for implementing the four features at issue here – programmable CAS latency, programmable burst length, dual edge clocking, and on-chip DLL – would be found in the peripheral circuitry. (Geilhufe, Tr. 9559).

Response to Finding No. 795: Complaint Counsel has no specific response to RPF 795. Complaint Counsel notes, however, that the memory array consists largely of a single cell array repeated over and over (Rhoden, Tr. 359-60), whereas the peripheral circuitry consists of many different types of circuits. (Rhoden, Tr. 361-63).

796. The vast majority of DRAM development costs is spent on the memory array portion of the DRAM, including the manufacturing process and equipment development. (Geilhufe, Tr. 9560-61). Development costs for the peripheral circuitry is much lower. (*Id.*).

Response to Finding No. 796: RPF 796 is incomplete and misleading. Historically, development costs of peripheral circuitry has been lower because the industry has focused on evolutionary change and has reused as much as prior circuitry design as possible. (CCFF 127-128). Development costs for peripheral circuitry would be much higher if the industry tried to make significant changes to the peripheral circuitry over time. (CCFF 2648).

797. The "process and storage cell/array" cost factor relates to the development of processes to reduce the size of memory cells or to increase the density of the memory array. (Geilhufe, Tr. 9565). This is a fixed, or one-time, cost. (Geilhufe, Tr. 9565-66).

Response to Finding No. 797: Complaint Counsel agrees that RPF 797 accurately describes what Mr. Geilhufe meant by his "process and storage cell/array" cost factor. There is no evidence that this factor has any significance other than being part of Mr. Geilhufe's testimony.

798. The "product design" cost factor relates to the manpower, computer time, and simulations to create the design for a particular alternative. (Geilhufe, Tr. 9566). This is a fixed cost. (*Id.*).

Response to Finding No. 798: Complaint Counsel agrees that RPF 798 accurately describes what Mr. Geilhufe meant by his "product design" cost factor. There is no evidence that this factor has any significance other than being part of Mr. Geilhufe's testimony.

799. The "wafer plant" cost factor relates to new equipment in the wafer factory that may be required to support a particular alternative. (Geilhufe, Tr. 9566-67). This is a fixed cost. (Geilhufe, Tr. 9567).

Response to Finding No. 799: Complaint Counsel agrees that RPF 799 accurately describes what Mr. Geilhufe meant by his "wafer plant" cost factor. There is no evidence that this factor has any significance other than being part of Mr. Geilhufe's testimony.

800. The "photo tooling" cost factor relates to the "reticles," also known as "masks," required to process a silicon wafer. (Geilhufe, Tr. 9567). This is a fixed cost. (*Id.*).

Response to Finding No. 800: Complaint Counsel agrees that RPF 800 accurately describes what Mr. Geilhufe meant by his "photo tooling" cost factor. There is no evidence that this factor has any significance other than being part of Mr. Geilhufe's testimony.

801. The "wafer sort" cost factor relates to the electrical test operation that separates the good from the bad die on a wafer. (Geilhufe, Tr. 9568). This is a variable cost, i.e., one that increases with the number of units produced. (*Id.*).

Response to Finding No. 801: Complaint Counsel agrees that RPF 801 accurately describes what Mr. Geilhufe meant by his "wafer sort" cost factor. There is no evidence that this factor has any significance other than being part of Mr. Geilhufe's testimony.

802. The "good die yield" cost factor relates to the percentage of total die that are good die. (Geilhufe, Tr. 9569). This is a variable cost.

Response to Finding No. 802: Complaint Counsel agrees that RPF 802 accurately describes what Mr. Geilhufe meant by his "good die yield" cost factor. There is no evidence that this factor has any significance other than being part of Mr. Geilhufe's testimony.

803. The "packaging" cost factor relates to the packages that potentially good die are placed in so that they can be attached to a circuit board. (Geilhufe, Tr. 9569). This is a variable cost. (Geilhufe, Tr. 9570).

Response to Finding No. 803: Complaint Counsel agrees that RPF 803 accurately describes what Mr. Geilhufe meant by his "packaging" cost factor. There is no evidence that this factor has any significance other than being part of Mr. Geilhufe's testimony.

804. The "final test and good unit yield" cost factor relates to post-packaging testing that results in some further units that are rejected. (Geilhufe, Tr. 9570). This is a variable cost. (*Id.*).

Response to Finding No. 804: Complaint Counsel agrees that RPF 804 accurately describes what Mr. Geilhufe meant by his "final test and good unit yield" cost factor. There is no evidence that this factor has any significance other than being part of Mr. Geilhufe's testimony.

805. The "inventory" cost factor has two elements: First, the "work-in-process" inventory in the fabrication and assembly plants relating to the time period, approximately six to eight weeks, required to complete all of the processing steps to create a finished wafer. Second, the "finished product" inventory, at the DRAM manufacturer, distribution channel and user, after a product passes final test and is determined to be a good unit (Geilhufe, Tr. 9571). Inventory is a variable cost. (*Id.*).

Response to Finding No. 805: Complaint Counsel agrees that RPF 805 accurately describes what Mr. Geilhufe meant by his "inventory" cost factor. There is no evidence that this factor has any significance other than being part of Mr. Geilhufe's testimony.

806. The "qualification" cost factor relates to the reliability and specification qualification that is done for a particular product. (Geilhufe, Tr. 9572). This is a fixed cost. (Geilhufe Tr. 9572-73).

Response to Finding No. 806: Complaint Counsel agrees that RPF 806 accurately describes what Mr. Geilhufe meant by his "qualification" cost factor. There is no evidence that this factor has any significance other than being part of Mr. Geilhufe's testimony.

807. The "board complexity" cost factor relates to the motherboard and the possibility that a change to the DRAM may require a larger board area or more traces or other circuitry on the board. (Geilhufe, Tr. 9573). This is a variable cost. (*Id.*).

Response to Finding No. 807: Complaint Counsel agrees that RPF 807 accurately describes what Mr. Geilhufe meant by his "board complexity" cost factor. There is no evidence that this factor has any significance other than being part of Mr. Geilhufe's testimony.

808. In estimating the costs of various alternative technologies proposed by Professor Jacob, Respondent's expert, Michael Geilhufe, tried to be conservative, that is, to err on the low end with respect to cost increases. (Geilhufe, Tr. 9746).

Response to Finding No. 808: Mr. Geilhufe's effort to be conservative in his cost estimates for various alternative technologies is contradicted by the weight of the evidence. For

example, Mr. Geilhufe testified that fixed CAS latency parts would add a photo tool cost of $50,000 per part. (Geilhufe, Tr. 9576; CCFF 2154). However, SDRAM lite, which was a proposal for a fixed CAS latency part, would not have involved extra photo tool costs. (Lee, Tr. 11016; CCFF 2155). Even if SDRAM lite would have included two different CAS latencies, it still would not necessarily have involved extra photo tool costs. (Lee, Tr. 11017; CCFF 2156).

Mr. Geilhufe testimony is also unreliable because he made the assumption that volume production for a first tier manufacturer was twenty million units. (Geilhufe, Tr. 9562-63). Mr. Geilhufe's model takes the fixed costs of proposed alternatives and divides them by twenty million units to estimate the additional fixed cost per unit. (*Id.* at 9579). Terry Lee testified that Micron runs their 64-meg and 128-meg SDRAM productions at a volume of around 900 million units over the course of the products' lifetime. (Lee, Tr. 10997-98).

Additionally, the substantial weight of the evidence shows that Mr. Geilhufe's cost estimate for placing the DLL on the module was not conservative. (CCFF 2387-2388). Mr. Geilhufe assumed that it would cost $3.80 to pay for the DLL circuit necessary to move the DLL onto the module. (Geilhufe, Tr. 9613; CCFF 2387). However,

(Lee, Tr. 11179, *in camera*); *see also* Goodman, Tr. 6048-49 (a standard PLL generally costs around $1.00)).

3. There Were No Viable Non-Infringing Alternatives To The Rambus Technologies Adopted In The SDRAM.

a. Programmable Latency.

809. Complaint Counsel have suggested, through their technical expert, Professor Jacob, the following possible alternatives to programmable CAS latency in SDRAMs:

(1) Use fixed CAS latency parts;
(2) Program CAS latency by blowing fuses on the DRAM;
(3) Scale CAS latency with clock frequency;
(4) Use dedicated pins to transmit latency information from the controller to the DRAM;

(5) Explicitly identify CAS latency in the read command;
(6) Stay with an asynchronous-style DRAM.

(Jacob, Tr. 5370-96).

Response to Finding No. 809: Complaint Counsel agrees that RPF 809 accurately represents a list of Professor Jacob's proposed alternatives to programmable CAS latency.

(1) The Use of Fixed CAS Latency Parts Was Not a Viable Alternative.

810. One of the alternatives proposed by Professor Jacob for programmable CAS latency was to fix the CAS latency at the design stage, the manufacturing stage, or the packaging stage. (Jacob, Tr. 5371). Fixing CAS latency at the design stage would result in a single part with only one CAS latency. (Jacob, Tr. 5373). Fixing CAS latency at the processing stage would involve a "metal mask option" that would fix the CAS latency to one value or another. (Jacob, Tr. 5373-75). Fixing CAS latency during packaging would require a multiplexer that would be hardwired to either power or ground during the packaging process to select one of two latency values. (Jacob, Tr. 5375-76).

Response to Finding No. 810: The last sentence in RPF 810 is inaccurate to the extent that it suggests that fixing CAS latency during the packaging would require a multiplexor. At trial, Professor Jacob described how a manufacturer could use a multiplexor during the packaging phase to fix CAS latency. (Jacob, Tr. 5375). He did not further testify that a manufacturer who wanted to fix CAS latency during that packaging phase would have had to use a multiplexor. (*Id.*).

811. Complaint Counsel did not meet their burden of showing that the use of fixed CAS latency parts was a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs.

Response to Finding No. 811: This finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Furthermore, RPF 811 is contrary to the weight of the evidence in the record. (*See* CCFF 2133-2156).

812. To the contrary, the evidence in the record shows that the use of fixed CAS latency parts was not a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs because multiple fixed CAS latency parts would have been required, leading to higher costs and logistical difficulties for DRAM manufacturers and users.

Response to Finding No. 812: RPF 812 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, RPF 812 ignores the substantial evidence in the record that indicates that fixed CAS latency parts would not have necessarily led to higher costs compared to programmable CAS latency. Assuming that burst length and burst type were also fixed, a fixed CAS latency part would eliminate the mode register. (CCFF 2137). This means that the die size of a fixed CAS latency part would be smaller than the die size of a programmable CAS latency part, thereby reducing its cost. (*Id.*). Additionally, lower test costs are associated with fixed CAS latency parts. (*Id.*).

RPF 812 also ignores the substantial evidence in the record that indicates that, contrary to Mr. Geilhufe's testimony, there would be no extra photo tool costs associated with fixed CAS latency. (Lee, Tr. 11016-17; *see also* CCFF 2154-2156). Nor does it take into account the substantial evidence that indicates that, contrary to Dr. Soderman's testimony, fixed CAS latency would not interfere with a manufacturer's ability to speed grade parts. (CCFF 2140-2148). Lastly, RPF 812 fails to account for the substantial evidence in the record that indicates that, contrary to Dr. Soderman and Mr. Geilhufe's testimony, two fixed CAS latency parts would have served most of the market. (CCFF 2149-2153). Most fundamentally, RPF 812 ignores the fact that fixed CAS latency was proposes and considered seriously at JEDEC for the specific purpose of reducing cost. (CCFF 572, 2139, 2142-44).

813. Multiple CAS latency values are required for SDRAMs because users of DRAMs would prefer to buy parts that they can insert in a variety of systems with different bus speeds. (RX 1626 at 3-4; Soderman, Tr. 9346-47). The appropriate CAS latency for a part will depend on the bus speed and the access time of the DRAM. (Soderman, Tr. 9347-48). Therefore, using fixed latency parts would require multiple fixed latency parts, as opposed to a single, programmable latency part. (*Id.*).

Response to Finding No. 813: The first sentence in RPF 813 is misleading because it cites to evidence that does not support the proposition that users prefer to buy parts that can work with multiple CAS latency values. Instead, any "preference" suggested by this document is best described as a preference for maintaining the status quo from a system-level and even a supplier-level perspective because of lock-in rather than an inherent preference for a single part that can support multiple CAS latencies. (RX 1626 at 3-4). By April 2000, the date of the document cited in RPF 813, the industry was already locked in to JEDEC's SDRAM and DDR SDRAM standards. (CCFF 2500-2584). From a supplier's perspective, in 2000, any attempt to switch from programmable CAS latency to fixed CAS latency would have required a design change involving major expense and delay. (CCFF 2530-2532).

Mr. Hovis admitted he had a bias when he wrote RX 1626. (*Id.* at 3 ("The only confession I will make here is that I am approaching this from a systems perspective, not a suppliers . . .")). The only witness that Respondent questioned on this document, Mr. Kellogg, confirmed that Mr. Hovis was speaking on behalf of users, or customers of DRAM components, rather than suppliers. (Kellogg, Tr. 5241, 5244).

From a system's perspective, in 2000, any attempt to switch from programmable CAS latency to fixed CAS latency would require changes in other components to the system to ensure compatibility. (CCFF 2550-2562). As Mr. Hovis recognized, in 2000, the legacy systems issues associated with SDRAM and DDR SDRAM made switching to fixed CAS latency prohibitive. (RX 1626 at 3). With respect to SDRAM, Mr. Hovis explained, "Forcing such a change requires

creating entirely new card assemblies, updating system code to now recognize new cards, and systems must also appropriately reject cards that don't have components with the necessary CL support for that system. I translate that into significant extra cost for creating this entire infrastructure on what is clearly a mature technology on legacy systems." (*Id.* at 3).

With respect to DDR SDRAM, Mr. Hovis articulated the same argument for keeping programmable CAS latency. (RX 1626 at 3 (arguing that it made sense to keep programmable CAS latency in spite of the additional test cost associated with it because by now that additional cost is "off-set by fewer part numbers and simpler parts logistics and fewer card assemblies.")).

With respect to DDR II SDRAM, Mr. Hovis stated his personal belief that there had been no lock-in by 2000. (RX 1626 at 3). However, it is not clear that Mr. Hovis's use of the term "lock-in" is fully consistent with what Complaint Counsel means by lock-in. (For the evidence in the record supporting Complaint Counsel's "lock-in" allegations, refer to CCFF 2500-2584). The goal of the DDR II Task Group was to create a standard that was backwards compatible with DDR SDRAM. (Kellogg, Tr. 5193; Macri, Tr. 4627-29; CX0392 at 3; *see also* CCFF 3245). There is a strong preference for backwards compatibility in the DRAM industry. (CCFF 3247-3249). It is simply not clear from reading RX 1626 whether Mr. Hovis had a genuine preference for programmable CAS latency, or was expressing the more general preference in the industry to keep programmable CAS latency in order to maintain backwards compatibility. (*Id.* at 4). As Mr. Hovis, himself, explains, most systems manufacturers may not require a memory part that works with multiple latencies in a given system, but instead want a memory "that [ ] likely gets used or supported across multiple systems." At a minimum, Mr. Hovis's statements are as consistent with evidence support Complaint Counsel's lock-in allegations as they are with RPF 814.

It should be noted that Respondent had the opportunity to call Mr. Hovis as a witness, and they instead chose not to.

814. Mark Kellogg of IBM testified that, in the 1992 time frame, "we weren't convinced that we knew the right latency and we did expect that the DRAM frequency would go up over time -- that we knew the correct latency if we were to select one and we expected that the DRAM frequency would increase over time, which meant we might wish to change the CAS latency." (Kellogg, Tr. 5139).

Response to Finding No. 814: RPF 814 does not support the conclusion that fixed CAS latency was not a viable alternative. If JEDEC could not settle upon the "right" CAS latency, DRAM manufacturers could have designed chips with circuitry for multiple CAS latencies and used either a bond wire option during the packaging phase or metal mask option during the processing phase to determine what CAS latency the part would operate with. (CCFF 2135-3136).

815. The mode register in SDRAMs and DDR SDRAMs reserves three bits for CAS latency, allowing for up to eight different CAS latency values. (CX 234 at 150).

Response to Finding No. 815: Complaint Counsel does not disagree that RPF 815 makes an accurate statement about the mode register in SDRAMs and DDR SDRAMs. However, this statement does not support the conclusion that fixed CAS latency was not a viable alternative because it ignores the substantial evidence in the record that indicates that it was not necessary to allow for up to eight different CAS latency values. (CCFF 2149-2153, 2253 (indicating that at most JEDEC would have needed to standardize two different CAS latency values)). Furthermore, it ignores the fact that Mr. Sussman testified that he "had a lot of arguing to do to get the degree of programmable features [programmable CAS latency and burst length] into the [JEDEC standard]." (Sussman, Tr. 1380).

816. Release 4 of JEDEC Standard 21-C (November 1993), which contains the first published SDRAM standard, specified three required CAS latency values (1, 2, and 3) and one optional CAS latency value (4). (JX 56 at 114; Lee, Tr. 11003-04). Release 9 of JEDEC Standard 21-C (August 1999), which contains the first published DDR SDRAM standard, specified two required CAS latency values for SDRAMs (2 and 3) and one optional value (4); it also specified two required CAS latency values for DDR SDRAMs (2 and 2.5) and three optional values (1.5, 3, and 3.5). (CX 234 at 150; Lee, Tr. 11068-72).

Response to Finding No. 816: Complaint Counsel does not disagree that RPF 816 makes an accurate statement about the number of required and optional CAS latencies in Release 4 and Release 9 of JEDEC Standard 21-C. However, this statement does not support the conclusion that fixed CAS latency was not a viable alternative because it ignores the substantial evidence in the record that indicates that the requirements of the industry would have predominantly been served if JEDEC had standardized CAS latencies 2 and 3. (CCFF 2149-2153, 2253; *see also* CCRF 815).

817. Although not all of the eight possible values of CAS latency are used in SDRAMs and DDR SDRAMs, the other possibilities were reserved to preserve flexibility for future additions. (Lee, Tr. 11072-73).

Response to Finding No. 817: Complaint Counsel has no specific response to RPF 817 except to note that this statement does not support the conclusion that fixed CAS latency was not a viable alternative because it ignores the substantial evidence in the record that indicates that the requirements of the industry would have predominantly been served if JEDEC had standardized only CAS latencies 2 and 3. (CCFF 2149-2153, 2253; *see also* CCRF 815).

818. Desi Rhoden gave a presentation on "Future SDRAM" at the March 1996 meeting of the JEDEC 42.3 subcommittee. (JX 31 at 64; Rhoden, Tr. 489-90). The presentation indicates that CAS latencies of 2, 3, 4, 5 and 6 would be required for different generations of SDRAMs. (JX 31 at 64; Rhoden, Tr. 490-91).

Response to Finding No. 818: RPF 818 is misleading because JEDEC did not ultimately adopt Mr. Rhoden's proposal for future SDRAM.

In March 1996, Mr. Rhoden proposed that JEDEC adopt a new interface technology, SSTL 3, for future SDRAM that would allow SDRAM to run at speeds up to 300 mhz using a single edged clocking scheme. (JX0031 at 64; Rhoden, Tr. 490-91, 542-43; CCFF 2332). Mr. Rhoden's testimony and his presentation, at most, supports the following statement: CAS latencies 2, 3, 4, 5 and 6 might have been required if JEDEC had decided to drive SDRAM faster in the future by

keeping mostly everything the same except the interface technology and the use of an on-chip PLL/DLL.

But JEDEC did not adopt Mr. Rhoden's scheme for future SDRAM and instead decided to double the data rate by using both edges of the clock. (CCFF 653, 656).

819. JEDEC's DDR2 SDRAM standard intends to expand the use of programmable latency. (Soderman, Tr. 9351-53). Preliminary DDR2 SDRAM data sheets from both Hynix and Samsung indicate that DDR2 SDRAMs will continue to have three bits in the mode register reserved for CAS latency, allowing for up to eight different CAS latency values. (RX 2099-14 at 21; RX 2099-39 at 20; Soderman, Tr. 9351). Hynix's part provides three different CAS latency values (3, 4, 5), while Samsung's part provides four different CAS latency values (3, 4, 5 and 6). (*Id.*). DDR2 SDRAMs also reserve three bits in an "extended mode register" for "additive latency," allowing for up to eight different additive latency values. (RX 2099-14 at 24; RX 2099-39 at 22; Soderman, Tr. 9351-53; Lee, Tr. 11068). Hynix's part provides six different additive latency values (0, 1, 2, 3, 4, and 5), while Samsung's part provides five different additive latency values (0, 1, 2, 3 and 4). (*Id.*). The "read latency" in DDR2 SDRAMs (that is, the number of clock cycles from receipt of a CAS command until data is output onto the bus) is the sum of the CAS latency and the additive latency. (RX 2099-14 at 32; RX 2099-39 at 37).

Response to Finding No. 819: RPF 819 is unreliable because there was no witness testimony to establish the purpose of including these various CAS latencies and additive CAS latencies, how widely they were used, or whether the needs of the industry could have been met with fewer CAS latencies. RPF 819 does not support the conclusion that fixed CAS latency was not a viable alternative because it ignores the substantial evidence in the record that indicates that the requirements of the industry would have predominantly been served if JEDEC had standardized CAS latencies 2 and 3. (CCFF 2149-2153, 2253).

Furthermore, the there is no evidence in the record which supports that additive latency is relevant, or that it somehow supports the assertion that JEDEC is expanding the use of programmable latency. Dr. Soderman testified that the Samsung part included additive latency in an expanded mode register, but did not explain how that undermined the viability of fixed CAS latency. (Soderman, Tr. 9351-53). When Respondent's Counsel questioned Mr. Lee about

additive latency, he did not ask Mr. Lee to explain why additive latency was included in the standard. (Lee, Tr. 11067-68, 11080).

820. In 1993, Micron's first SDRAM design allowed for four different CAS latencies (1, 2, 3, and 4). (Lee, Tr. 11063-64).

Response to Finding No. 820: This statement is incomplete because it omits the fact that the typical CAS latencies for SDRAM are 2 and 3. (Rhoden, Tr. 394; Lee, Tr. 11004-05).

821. Micron currently sells an SDRAM for the graphics market allowing for three different CAS latencies (1, 2, and 3). (Lee, Tr. 11064-67).

Response to Finding No. 821: This statement is incomplete because it omits the fact that the typical CAS latencies for SDRAM are 2 and 3. (Rhoden, Tr. 394; Lee, Tr. 11004-05).

RPF 821 is also incomplete because it omits the fact that graphics parts do not share the same die as main memory parts. (Lee, Tr. 11064). This means that the cost analysis for main memory parts must be separated from the cost analysis for graphics memory. (Lee, Tr. 11065 ("Q. And the 64-meg x32 SDRAM that's used for graphic purposes that has a CAS latency of one meets a JEDEC standard, does it not? A. Yeah, but I guess I'm a little confused about your question, because I think you're establishing amortization of the costs, and that's a different die. The parts for graphics are usually on a completely different die than main memory, so the number of latencies supported on graphics doesn't necessarily correspond with what we're doing in the main memory part.").

JEDEC tends to focus on main memory parts when it develops standards. (Wagner, Tr. 3828 ("In the graphics space, they don't really put a lot of effort in JEDEC focused on our specific needs.")). Consequently, for the purposes of evaluating whether JEDEC would have considered fixed CAS latency to be a viable alternative, facts about the latency needs of the main memory industry may be more relevant than facts about the latency needs of the graphics segment.

822. The total unit cost for a mature product built by a first tier DRAM manufacturer in the mid-1990s was approximately $2.00. (Geilhufe, Tr. 9564). Multiple fixed latency parts would have been an expensive alternative, for several reasons. (Soderman, Tr. 9348-49).

Response to Finding No. 822: RPF 822 is not supported by record evidence. In his testimony, Mr. Geilhufe *assumed* that the total cost of a first-tier DRAM manufacturer in the mid-1990's was approximately $2.00. (Geilhufe, Tr. 9564). Mr. Geilhufe had no direct experience with a DRAM manufacturer during the 1990s; his indirect experience was limited to working with the Kihun 1 and 2 fabs which were outdated and apparently were no longer manufacturing DRAMs at the time. (Geilhufe, Tr. 9629-31). Thus, Mr. Geilhufe had no personal knowledge of the per unit cost of a DRAM manufacturer. Rambus has provided no record evidence to support this finding or Mr. Geilhufe's assumption. This key assumption of Mr. Geilhufe renders many, if not most, of Mr. Geilhufe's conclusions unreliable.

Further, the statement that multiple fixed CAS latency parts would have been an expensive alternative is contrary to the weight of the evidence. (CCFF 2137-2156).

823. First, manufacturing multiple fixed latency parts would decrease a DRAM manufacturer's yield due to speed distribution. (Soderman, Tr. 9348; Geilhufe, Tr. 9577). DRAMs cannot be accurately tested for speed until after packaging; fixing the CAS latency prior to that time would result in some parts that are not capable of performing at the CAS latency that has been fixed and, therefore, would not be usable. (Soderman, Tr. 9347-49; Geilhufe, Tr. 9577-8). If CAS latency were programmable, those slower parts would be usable at a higher CAS latency value. (*Id.*).

Response to Finding No. 823: In their testimony, Dr. Soderman and Mr. Geilhufe assumed that manufacturing fixed latency parts would decrease yield and that DRAMs cannot accurately be tested for speed until after packaging. (CCFF 2140). Based on their assumptions, they concluded that fixed CAS latency would increase cost. (*Id.*). Neither Dr. Soderman, nor Mr. Geilhufe, nor Rambus provided any factual evidence to support these assumptions. In fact, these assumptions are contrary to the weight of the evidence because the weight of the evidence suggests

that using fixed CAS latency would not have interfered with a manufacturer's ability to speed grade parts. (CCFF 2140-2148).

Complaint Counsel does not disagree that the second sentence accurately reflects the testimony of Dr. Soderman and Mr. Geilhufe. However, the second sentence is incomplete because it ignores the testimony of Professor Jacob who testified that it was possible to fix CAS latency during the design, processing, and packaging phases. (Jacob, Tr. 5371). In his work on behalf of this matter, it should be noted that Professor Jacob consulted with roughly one dozen to two dozen engineers in reaching his conclusions. (Jacob, Tr. 5369).

824. Second, fixing CAS latency would result in DRAM manufacturers losing some of the price premium associated with their fastest (i.e. lowest CAS latency) parts which can sell for 50 percent or more over their standard parts. (Soderman, Tr. 9348-50; Lee, Tr. 11074-75). This is again because the latency would be fixed prior to accurate speed testing and, consequently, some parts that would be capable of faster performance (i.e. operating at a low CAS latency) will be set to a CAS latency higher than necessary. (*Id.*).

Response to Finding No. 824: RPF 824 is misleading because Mr. Lee only testified that parts with lower CAS latencies sometimes demand a higher price. (Lee, Tr. 11074-75). He did not, however, testify further that the inference to be drawn from that fact is that fixed CAS latency would result in the loss of some of the price premium associated with lower CAS latency parts.

Furthermore, the second sentence is wholly unsupported by Mr. Lee's testimony at the designated pages. (Lee, Tr. 11074-75). Mr. Lee did not expand upon, nor was he asked to expand upon, his testimony that he would agree that lower CAS latency parts sometimes demand a higher price. (*Id.*).

Lastly, RPF 824 is unreliable because it is based on Dr. Soderman's conclusion that the loss of a price premium was associated with fixed CAS latency. That conclusion was based on the assumption that fixed CAS latency would interfere with a manufacturer's ability to speed grade

parts. (Soderman, Tr. 9348). As previously argued in CCRF 825, however, that assumption is contrary to the weight of the evidence. (CCFF 2140-2148).

825. Steve Polzin of AMD testified that "Fixed CAS latency would have been pretty onerous for the DRAM manufacturers." (Polzin, Tr. 3992). Mr. Polzin explained:

> Probably [fixed CAS latency] had -- would have a significant cost impact for the DRAM manufacturers. One of the advantages of programmable CAS latency is that DRAM manufacturers can bin their devices. They can have fast devices with a short CAS latency and sell them for more money, and parts that were perhaps yielding slower, they could be programmed with a longer CAS latency and sold for less cost.

(*Id.*).

Response to Finding No. 825: This statement from Mr. Polzin about how DRAM manufacturers would have been impacted by fixed CAS latency is unreliable because Mr. Polzin is not a DRAM manufacturer. Mr. Polzin is a chief platform architect at AMD, a microprocessor and chipset company. (Polzin, Tr. 3932-33).

Furthermore, this testimony was in response to a follow-up question about which workarounds to Rambus patents had AMD considered after it became aware of Rambus patents in 2000. (Polzin, Tr. 3987-90). At that time, AMD would have been motivated to encourage DRAM manufacturers to stay with the technologies that they had been planning to use before Rambus began to assert its SDRAM and DDR SDRAM patents. When AMD learned about Rambus patents, it was in the middle of trying to launch its DDR-based chipset, IGD4. (Polzin, Tr. 3989). Although each of the Rambus technologies involved pretty easy workarounds, Mr. Polzin testified that it would have been "pretty tough" to change things in the middle of a ramp. (*Id.*). Mr. Polzin recommended to his superiors that they not interfere with the CAS latency feature that AMD's products used because that could cause a "big hiccup" in the production ramp. (*Id.* 3993).

826. Joe Macri of ATI testified that

in camera).

(Macri, Tr. 4762-63, **in camera**).

Response to Finding No. 826: RFP 826 is incomplete because it fails to mention that

(Macri, Tr. 4762-63, *in camera*).

(Macri, Tr. 4762, *in camera*

(*Id., in camera*).

Additionally,

(Macri, Tr. 4763-64, *in camera*).

827. Third, there would have been an increase in design, photo tooling and qualification costs because multiple products would have had to be designed and manufactured, rather than just one. (Geilhufe, Tr. 9679, 9682-83, 9690).

Response to Finding No. 827: Mr. Geilhufe assumed that use of fixed CAS latency would have required multiple products and further assumed that these products would have been designed and manufactured separately; from this, he considered that there would have been an increase in design, photo tooling, and qualification costs. (Geilhufe, Tr. 9578). Neither Mr. Geilhufe, nor Rambus provided any factual evidence to support Mr. Geilhufe's conclusions. Indeed, Mr. Geilhufe's assumptions and conclusions are contrary to the weight of the evidence. (CCFF 2150-2153, 2154-56). As a result, Mr. Geilhufe's conclusion is unreliable and contrary to the weight of the evidence.

828. Some design effort would have been required for each different CAS latency; one mask would have had to be changed for each different CAS latency; and each different CAS latency part would have had to be qualified before it could be sold. (Geilhufe, Tr. 9575-76, 9578-79).

Response to Finding No. 828: This proposed finding is unreliable and contrary to the weight of the evidence for the reasons set forth in CCRF 828.

829. Fourth, multiple fixed latency parts in place of a single programmable latency part would result in substantial inventory costs. (Soderman, Tr. 9349-50).

Response to Finding No. 829: Dr. Soderman assumed that use of fixed CAS latency would require multiple parts, and concluded that this would lead to an increase in inventory costs. (Soderman, Tr. 9349-50). Neither Dr. Soderman nor Rambus provide factual evidence to support his assumptions. Indeed, Dr. Soderman's assumption is contrary to the weight of the evidence (CCFF 2149-2153, 2253). As a result, Dr. Soderman's conclusion is unreliable and contrary to the weight of the evidence.

830. Gordon Kelley of IBM testified about the benefits of programmability as follows: "One of the advantages of that is that that drives low cost. The producer does not have to maintain multiple part numbers. One part number fits many applications. That's one of the drivers to low cost." (Kelley, Tr. 2550-51).

Response to Finding No. 830: Complaint Counsel does not disagree that one of the advantages of programmability is that it reduces cost because producers do not have to maintain multiple part numbers. This statement, however, is incomplete to the extent that it omits the advantages associated with fixed CAS latency that are not associated with programmable CAS latency. (CCFF 2137, 2139, 2145). Fixed CAS latency promised to reduce test costs and, assuming that burst length and burst type were fixed also, reducing the die size compared to programmable CAS latency. (CCFF 2137, 2139).

Furthermore, Mr. Kellogg, also from IBM, testified that there would have been a performance advantage to fixed CAS latency "if 'fixed' implied no circuitry in the access path." (Kellogg, Tr. 5138).

831. When first developing the Rambus technology, Drs. Farmwald and Horowitz considered having a fixed latency. (Horowitz, Tr. 8532). Dr. Horowitz learned from an early visit to a DRAM manufacturer the importance of having a single, as opposed to multiple, parts. At that time, there were two different packages for DRAMs, and the DRAM manufacturer was making a single die that could fit into either package even though this entailed 10 percent additional die area. (Horowitz, Tr. 8532-33). Dr. Horowitz's understanding at the time was that the reason for making a single part despite the die size penalty was that inventory costs from having two different designs during the manufacturing process would be too expensive. (Horowitz, Tr. 8533-34).

Response to Finding No. 831: RPF 831 is inaccurate to the extent that it suggests that Dr. Farmwald considered fixed latency. It is not clear that Dr. Farmwald developed any kind of personal understanding about alternative technologies because he testified that he never considered alternatives to the technologies at issue in this case. (*See, e.g.*, Farmwald, Tr. 8289-90 (Dr. Farmwald did not believe there were any alternatives to Rambus's technology and therefore he did not remember thinking about alternatives "one way or the other.")).

Furthermore, the testimony of Drs. Farmwald and Horowitz was strictly limited to their experience with RDRAMs. Their experience with RDRAMs does not appear to be relevant to the viability of fixed CAS latency for SDRAM as the RDRAM architecture is fundamentally different from SDRAM architecture. (CCFF 1268, 1272, 1306, 1357).

832. Multiple fixed latency parts would also be inferior from the user's standpoint. Because the part could no longer be programmed to operate in various systems, a user would have to pay attention to the part's detailed specifications to determine whether it would work in its system. (Soderman, Tr. 9350-51).

Response to Finding No. 832: Complaint Counsel does not disagree that RPF 832 accurately represents Dr. Soderman's testimony during trial on the subject of fixed CAS latency.

The portion of RPF 832 that describes that a disadvantage of multiple fixed latency parts would be that users would have to pay attention to the part's detailed specifications is incomplete.

It ignores Professor Jacob's testimony that such a consequence was not inevitable. There are technical solutions to the engineering problem associated with the use two or more fixed cas latency parts, which was described by Professor Jacob, (Jacob, Tr. 5377-78), and alluded to by the testimony cited in RPF 832.

Engineers would need to prevent a situation in which, for example, a DIMM with cas latency 2 parts is plugged into the same computer as a DIMM with cas latency 3 parts. (Jacob, Tr. 5377-78). Professor Jacob suggested two ways that would have avoided the need for users to consult detailed specifications. First, a slightly more sophisticated memory controller could have detected when there are incompatible DIMMs in the system. (Jacob, Tr. 5377-78). Second, DIMMs could be labeled in such a way to prevent OEMs from plugging incompatible DIMMs into the system. (*Id.*).

833. In an April 11, 2000 e-mail responding to a proposal to fix CAS latency in DDR2, Bill Hovis of IBM rejected the idea both because of cost concerns and because of the benefits to DRAM users from programmable CAS latency. With respect to cost concerns, Mr. Hovis stated: "What are we really saving here? . . . . Any cost savings has to be off-set with the additional component costs associated with adding new part numbers to satisfy CL=2 and CL=3 demands." (RX 1626 at 3). With respect to user benefits from programmable CAS latency, Mr. Hovis stated that "ultimately the flexibility of supporting multiple CAS latencies in one device can result in benefits to the customers that end up buying the memory." (RX 1626 at 3).

Response to Finding No. 833: Bill Hovis's statements regarding fixed CAS latency are unreliable for the reasons set forth in CCRF 813.

834. Using fixed latency would not allow for the elimination of the mode register in SDRAMs and DDR SDRAMs because the mode register is used for purposes other than programming CAS latency. In the JEDEC SDRAM standard, the mode register is used for storing CAS latency, burst length and burst type. (CX 234 at 150). Certain SDRAMs being manufactured use the mode register for additional purposes as well, such as for programming operating mode and write burst mode. (RX 2100-13 at 3). The DDR SDRAM standard adds an extended mode register used to enable or disable a DLL. (CX 234 at 176). The DDR2 SDRAM standard expands the use of the mode register even further, with the mode register being used to program burst length, burst type, CAS latency, test mode, DLL reset, and tWR, and the extended mode register being used to program DLL enable, output driver impedance control, RTT, additive latency, OCD, /DQS enable and RDQS enable. (RX 2099-14 at 21, 24; RX 2099-39 at 20, 22).

Response to Finding No. 834: Complaint Counsel does not disagree with the statement that using fixed CAS latency alone would not eliminate the mode register entirely in SDRAMs and DDR SDRAMs unless burst length and burst type were also fixed or determined by another means. However, the record evidence indicates that alternative means for determining both burst length and type existed, that JEDEC considered alternatives for both and that, had JEDEC selected fixed CAS latency, it likely would have used other means to set burst length and type and eliminated the mode register. (CCFF 2234-2321; JX0010 at 71, 74-75; CX0034 at 149; JX0027 at 64-69; Jacob, Tr. 5375-76 (testifying that one of the advantages of fixed CAS latency is that it would have eliminated the need for a mode register)). The record evidence indicates that JEDEC chose to expand the mode register to add additional features in later standards solely because it already existed and was available; later decisions to expand the mode register are irrelevant to the question of whether JEDEC would have chosen to eliminate the mode register to save cost in the SDRAM standard had it known of Rambus's potential patent rights.

835. Although there would have been a decrease in testing costs because each part would have had to be tested for a single CAS latency, rather than for multiple CAS latencies (Geilhufe, Tr. 9576), this cost saving would have been far outweighed by the cost increases due to other factors.

Response to Finding No. 835: The last portion of RPF 835 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9302 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, the last portion of RPF 835 is contrary to the weight of the evidence which indicates that the manufacturing associated with fixed CAS latency compared to programmable CAS latency were relatively similar. (Kellogg, Tr. 5143; CCFF 2133-2156). Record evidence

indicates that overall costs of fixed CAS latency would be less than programmable CAS latency. (CCFF 2142-2144, 2150-2156).

836. The fixed CAS latency alternative would have resulted in the following approximate net costs compared to the cost of SDRAM in the mid-1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: $100,000 increase in product design costs per latency; $50,000 increase in photo tooling costs per latency; one cent decrease per unit in testing costs at wafer sort; three cents per unit cost increase due to reduced good die yield; two cents per unit increase in inventory costs; and $250,000 increase in qualification costs per latency. (Geilhufe, Tr. 9562-64, 9575-79).

Response to Finding No. 836: Mr. Geilhufe's analysis is unreliable for the reasons set forth in CCRF 790.

Furthermore, the statement about added photo tool costs is contracted by the weight of the evidence. (*See* CCFF 2154-2154).

837. The net increase in variable costs for the fixed CAS latency alternative is, therefore, approximately 4 cents per unit. The total cost increase is approximately 6 cents per unit, calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9579).

Response to Finding No. 837: This proposed finding is unreliable because the methodology that Mr. Geilhufe used to reach his conclusions about the costs of alternative technologies was unreliable and irrelevant for the reasons set forth below.

To the extent that the alternatives were implemented in some fashion, one way to verify Mr. Geilhufe's cost estimates would have been to ask a DRAM manufacturer. (Geilhufe, Tr. 9666). Mr. Geilhufe recognized that his estimates were "rough estimates." (Geilhufe, Tr. 9696). Mr. Geilhufe did not compare his projections in this case with any actual data because he assumed that none of the alternative technologies had ever been implemented. (Geilhufe, Tr. 9665-66 ("Well, since the vast majority of these never got implemented, it was not possible to test them.")).

Mr. Geilhufe reviewed no evidence in this case relating to the costs of DRAM manufacturers for the product design cost element or the good die yield cost element from the relevant period other than the Peisl deposition. (Geilhufe, Tr. 9680, 9698).

Mr. Geilhufe's cost estimates are inaccurate because his methodology failed to account for certain cost savings. Furthermore, the per unit fixed cost estimates, product design are qualification costs, are unreliable because they are based on an inaccurate assumption that volume production for a first-tier manufacturer like Samsung, Infineon, or Micron, was approximately 20 million units for a product that was well into its life cycle. (Geilhufe, Tr. 9562, 9726). Neither Mr. Geilhufe nor Rambus provided any record evidence to support this assumption. Mr. Geilhufe reviewed no evidence related to the cost to DRAM manufacturers for final test and good unit yield for the relevant period, other than the Peisl deposition, and some "confidential" evidence that is not in the record. (Geilhufe, Tr. 9706). He failed to interview anybody who attended JEDEC meetings during the relevant time period. (Geilhufe, Tr. 9623). Furthermore, Mr. Geilhufe did not do anything to ensure that the analysis that he did was the type of analysis that was done at JEDEC. (Geilhufe, Tr. 9622).

The record evidence suggests that the volume production level for a particular part is between 500 million and 1 billion units. The volume production for Micron's 64 meg SDRAM, including shrinks, was approximately 900 million units. (Lee, Tr. 10997). The volume production for Micron's 128 meg SDRAM part was also approximately 900 million units. (*Id.* 10998). The 256 meg SDRAM, which started it's life cycle in 2000, has already reached a volume production level of approximately 400 million units. (*Id.*). Even if Mr. Geilhufe's estimates of fixed costs were correct, if allocated over 900 million units, the per unit cost would be much lower than 2 cents; rather, it would be a tiny fraction of a cent.

Lastly, Mr. Geilhufe's methodology is not the relevant methodology for this case because it ignores the fact that JEDEC is a consensus-based organization. (CCFF 2650; *see also* CCFF 239-255). Mr. Geilhufe did nothing to ensure that this methodology bore any relationship to JEDEC's decision-making process (CCFF 2121).

While Professor Jacob consulted an enormous amount of JEDEC meeting minutes, reviewed presentations that were made at those meetings, and confirmed his understanding about those presentations with JEDEC participants and other DRAM engineers (Jacob, Tr. 5368-69), Mr. Geilhufe failed to adequately consider JEDEC materials in his analysis. (CCFF 2115, 2118-2119, 2121 (Geilhufe)).

Mr. Geilhufe did not attend JEDEC meetings during the relevant time period. (CCFF 2115). He never reviewed any JEDEC meeting minutes or any JEDEC policy manuals. (Geilhufe, Tr. 9622).

838. The additional inventory cost estimate is based on three different fixed latency parts being manufactured, the number of required CAS latencies in the original SDRAM standard, instead of a single programmable latency part. (Geilhufe, Tr. 9578; JX 56 at 114). The estimate of three parts is conservative given the number of CAS latencies in use and projected to be in use in the future in SDRAMs, DDR SDRAMs and DDR2 SDRAMs. *See* Findings ¶¶ 815-821.

Response to Finding No. 838: The characterization of Mr. Geilhufe's additional inventory cost estimate as conservative is inaccurate because the weight of the evidence contradicts his assumption that three different fixed latency parts were required.

In the 1995-1996 time frame, there was substantial support for one fixed CAS latency of 3. (JX0029 at 13-14; Lee, Tr. 6627-31 (discussing SDRAM lite survey ballot results). There was unanimous support that no values other than CAS latencies of 2 and 3 were needed. (*Id.*).

Furthermore, the weight of the evidence indicates that there has been no more than two different CAS latencies in use at any given time. (CCFF 2150-2153). Although other values have existed, the typical CAS latencies for SDRAM are 2 and 3. (Rhoden, Tr. 394). For SDRAM,

customers primarily use CAS latencies of 2 and 3. (Lee, Tr. 11004-05). At most, JEDEC would have needed to standardize two different CAS latencies for SDRAM and DDR SDRAM. (CCFF 2253).

839. The estimate for increased inventory costs is very conservative, because inventory costs due to multiple products can be much larger. For example, in 1989, Apple Computer reported $27 million quarterly loss attributed entirely to purchasing a DRAM part that they could no longer use in their systems. (Geilhufe, Tr. 9587). This amounted to a loss of about five to six dollars per unit. (Geilhufe, Tr. 9588).

Response to Finding No. 839: The statement that Mr. Geilhufe's estimate for increased inventory costs is "very conservative" is inaccurate because it is contrary to the weight of the evidence. (Refer to CCRF 838).

Furthermore, the statement about Apple Computer's loss as a result of purchasing the wrong DRAM part is both irrelevant and unreliable. There is no evidence in the record to indicate how a one-time loss to Apple 14 years ago due to a mistake in the purchase of an unknown quantity of unidentified DRAMs for an undisclosed purpose that could not be used for an unknown reason relates the inventory cost of fixed CAS latency 2 and CAS latency 3 parts.

If CAS latency of 2 and 3 parts were available in the market, a memory controller could be designed to detect and support both which would greatly reduce if not eliminate any inventory issue. (Jacob, Tr. 5377-78).

(2) Programming CAS Latency with Fuses Was Not a Viable Alternative.

840. Professor Jacob's proposed alternative of programming CAS latency with fuses is similar to his fixed CAS latency alternative because, once the fuse is blown, the part has a fixed CAS latency. (Jacob, Tr. 5378-79).

Response to Finding No. 840: RPF 840 is misleading because it fails to reflect that up until the time the fuses are blown, a part with fuses has all the flexibility of a programmable part.

841. Complaint Counsel did not meet their burden of showing that programming CAS latency with fuses was a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs.

Response to Finding No. 841: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (*See* CCFF 2157-2177 (Complaint Counsel's findings which support the conclusion that blowing fuses to set CAS latency was a viable alternative)).

842. To the contrary, the evidence in the record shows that programming CAS latency with fuses was not a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs because, as with the fixed CAS latency alternative, multiple parts with different CAS latencies would have been required, leading to higher costs and logistical difficulties for DRAM manufacturers and users.

Response to Finding No. 842: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding ignores the substantial evidence in the record that indicates that the manufacturing cost of using fuses to program CAS latency was relatively similar to the manufacturing cost of using a mode register to program CAS latency. (Kellogg, Tr. 5143; *see also* CCFF 2132). Before 1996, it was potentially simpler and cheaper to use fuses to determine latency. (Jacob, Tr. 5382).

843. Fuses can be blown by lasers or electrically. (Jacob, Tr. 5380).

Response to Finding No. 843: Complaint Counsel does not disagree.

844. Laser-blown fuses are more reliable than electrically-blown fuses. (Soderman, Tr. 9356-57). Certain products using electrically blown fuses were discontinued at Intel for reliability reasons. (Geilhufe, Tr. 9581-82).

Response to Finding No. 844: The statement that laser-blown fuses are more reliable than electrically-blown fuses is unreliable and contrary to the weight of the evidence. (*See* CCFF 2171-2177).

(Lee, Tr. 11170, *in camera*).

(Lee, Tr. 11170-71, *in camera*).

(*Id.*).

Furthermore, Dr. Soderman's testimony concerning fuses was unreliable because of his lack of experience with electronically-blown fuses. He used Micron data sheets to determine which products had electronically blown fuses, but failed to account for times when blown fuses are not transparent to the user. (Soderman, Tr. 9444-45). The statement that Intel discontinued certain products using electrically blown fuses for reliability reasons is incomplete, uncorroborated, and therefore unreliable. In testifying about Intel's decision to discontinue products that used electrically-blown fuses, Mr. Geilhufe was not asked to testify about what caused the products to be unreliable. (Geilhufe, Tr. 9581-82). Were defective electrically-blown fuses being used? Were the fuses being used in an unusual way? Did the product in which they were being used have electrical characteristics different from those of SDRAM that would make it more difficult to blow fuses electronically? It simply is not clear from the evidence in the record what the source of the unreliability of the product Intel discontinued was.

Furthermore, the substantial evidence in the record that indicates that DRAM manufacturers have used electrically-blown fuses reliably for redundancy repair since 1989, CCFF

2173-2174, casts significant doubt upon the reliability of Intel's decision to discontinue products as evidence of the unreliability of electrically blown fuses.

845. In the 1995 time frame, the dominant fuse technology used by major DRAM manufacturers was laser fuse technology. (Geilhufe, Tr. 9581-82). There are DRAM manufacturers who do not have the technology to blow fuses electrically and did not have such technology in the 1995-2000 time frame. (Jacob, Tr. 5596; Geilhufe, Tr. 9740-41).

Response to Finding No. 845: RPF 845 is not supported by the evidence. Rambus and its experts failed to identify a single major DRAM manufacturer that did not have the technology to blow fuses electronically in the 1995-2000 time frame. The reference to Professor Jacob's testimony is misplaced. He did not imply in any way that other DRAM manufacturers were not able to blow fuses electronically. (Jacob, Tr. 5596). To the contrary, he testified that Micron, Infineon, and possibly Hynix use electrically blown fuses, and further that a substantial number of Micron's DRAM parts used electrically blown fuses.

Furthermore, this proposed finding ignores the the weight of the evidence in the record that indicates that DRAM manufacturers have used electrically-blown fuses reliably since 1989 and continue to use them reliably today. (CCFF 2172-2176).

846. Fixing the CAS latency with laser-blown fuses prior to packaging would lead to the same logistical difficulties as Professor Jacob's fixed CAS latency alternative. (Soderman, Tr. 9354).

Response to Finding No. 846: This proposed finding is incomplete because it omits the fact that use of laser blown fuses prior to packaging would have permitted flexible manufacturing and inventory, with the fuse being blown and the part packaged immediately before shipping. (Jacob, Tr. 5380). It also omits the possibility of resolving any remaining logistical issues associated with fixing CAS latency by blowing fuses before packaging by the use of a slightly more sophisticated memory controller that could detect when incompatible DIMMs are

placed in the same system. (Jacob, Tr. 5382-83). Or, it might require more sophisticated labeling of DIMMs. (*Id.*).

Furthermore, the logistical issues would not arise if OEMs were to blow the fuses to set CAS latency. (CCFF 2170).

This proposed finding also ignores the advantages associated with using fuses to set CAS latency parts. (Jacob, Tr. 5375; Kellogg, Tr. 5138).

847. Another disadvantage of using fuses is that the manufacturer would have to blow the fuses after receiving orders for parts, leading to a "time lag from request to delivery of parts." (Kellogg, Tr. 5131).

Response to Finding No. 847: This proposed finding is incomplete because it omits that Mr. Kellogg also testified that the manufacturing costs associated with blowing fuses to set CAS latency were relatively similar to the use of a mode register to program CAS latency. (Kellogg, Tr. 5143).

Furthermore, it ignores the advantages associated with using fuses to set CAS latency parts. (Jacob, Tr. 5375; Kellogg, Tr. 5138).

848. Laser blown fuses could not be blown by OEMs (original equipment manufacturers) because they cannot be blown after packaging. (Jacob, Tr. 5378-80; Soderman, Tr. 9354-56). Electrically-blown fuses can be blown after packaging, but they still could not be blown by OEMs because the part must be tested after the fuse is blown to make sure it is operating correctly. (Soderman, Tr. 9517). OEMs do not have the capability to perform such testing. (Jacob, Tr. 5597-98; Soderman, Tr. 9354-56).

Response to Finding No. 848: This statement that OEMs could not use laser-blown fuses to set CAS latency after packaging is incomplete because it omits the fact that they could have used electrically-blown fuses. (Jacob, Tr. 5380-81).

Furthermore, the last two sentences in this proposed finding assume that it would have been necessary for OEMs to test parts after the fuses were blown. There is no evidence in the record to support that this is a valid assumption.

To the contrary, Professor Jacob proposed a way to avoid having OEMs test parts. (Jacob, Tr. 5597). DRAM manufacturers could have tested parts before they shipped them to OEMs in order to make sure that the part would work with multiple CAS latencies. (*Id.*). The proposed finding also fails to note that OEMs already test DRAMs. (Bechtelsheim, Tr. 5835-38). There is nothing in the record to indicate that OEMs couldn't also test the CAS latency function when they test DRAMs.

849. Programming CAS latency with fuses would have resulted in increased costs.

Response to Finding No. 849: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding ignores the substantial evidence in the record that indicates that the manufacturing cost of using fuses to program CAS latency was relatively similar to the manufacturing cost of using a mode register to program CAS latency. (Kellogg, Tr. 5143; *see also* CCFF 2132). Before 1996, it was potentially simpler and cheaper to use fuses to determine latency. (Jacob, Tr. 5382).

850. There would have been an increase in design costs due to the design effort to provide the fuses required. (Geilhufe, Tr. 9575, 9584-85).

Response to Finding No. 850: This proposed finding is contrary to the weight of the evidence which indicates that the costs associated with using fuses to set CAS latency were relatively similar to the costs associated with using a mode register to program CAS latency. (Kellogg, Tr. 5143; *see also* CCFF 2177).

851. There would have been an increase in testing costs due to the time required to blow a fuse and perform certain additional steps. (Geilhufe, Tr. 9585).

Response to Finding No. 851: This proposed finding is contrary to the weight of the evidence which indicates that the costs associated with using fuses to set CAS latency were relatively similar to the costs associated with using a mode register to program CAS latency. (Kellogg, Tr. 5143; *see also* CCFF 2177).

852. There would have been reduced good die yield, inventory, and qualification costs of the same magnitude as the corresponding increases for the fixed CAS latency alternative because, once the fuse is blown, the part is a fixed latency part. (Geilhufe, Tr. 9585-89).

Response to Finding No. 852: Mr. Geilhufe assumes that using fuses to set CAS latency is equivalent to use of fixed CAS latency. This assumption is contradicted by the weight of the evidence. *See* CCRF 845-846. Furthermore, this proposed finding is contrary to the weight of the evidence which indicates that the costs associated with using fuses to set CAS latency were relatively similar to the costs associated with using a mode register to program CAS latency. (Kellogg, Tr. 5143; *see also* CCFF 2177; refer also to CCRF 823, 827, 829).

853. Programming CAS latency by blowing fuses would have resulted in the following approximate net costs compared to SDRAM in the mid-1990s, assuming a first-tier DRAM manufacturer using existing laser fuse technology and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: $100,000 increase in product design costs per latency; one cent increase per unit in testing costs at wafer sort; three cents per unit cost increase due to reduced good die yield; two cents per unit increase in inventory costs; and $250,000 increase in qualification costs per latency. (Geilhufe, Tr. 9562-64, 9584-86, 9589).

Response to Finding No. 853: This proposed finding is unreliable because the methodology that Mr. Geilhufe used to reach his conclusions about the costs of alternative technologies was unreliable and irrelevant for the reasons set forth below.

To the extent that the alternatives were implemented in some fashion, one way to verify Mr. Geilhufe's cost estimates would have been to ask a DRAM manufacturer. (Geilhufe, Tr. 9666). Mr. Geilhufe recognized that his estimates were "rough estimates." (Geilhufe, Tr. 9696). Mr. Geilhufe did not compare his projections in this case with any actual data because he assumed that

none of the alternative technologies had ever been implemented. (Geilhufe, Tr. 9665-66 ("Well, since the vast majority of these never got implemented, it was not possible to test them.")).

Mr. Geilhufe reviewed no evidence in this case relating to the costs of DRAM manufacturers for the product design cost element or the good die yield cost element from the relevant period other than the Peisl deposition. (Geilhufe, Tr. 9680, 9698).

Lastly, Mr. Geilhufe's methodology is not the relevant methodology for this case because it ignores the fact that JEDEC is a consensus-based organization. (CCFF 2650; *see also* CCFF 239-255). Mr. Geilhufe did nothing to ensure that this methodology bore any relationship to JEDEC's decision-making process (CCFF 2121). While Professor Jacob consulted an enormous amount of JEDEC meeting minutes, reviewed presentations that were made at those meetings, and confirmed his understanding about those presentations with JEDEC participants and other DRAM engineers (Jacob, Tr. 5368-69), Mr. Geilhufe failed to adequately consider JEDEC materials in his analysis. (CCFF 2115, 2118-2119, 2121).

Mr. Geilhufe did not attend JEDEC meetings during the relevant time period. (CCFF 2115). He never reviewed any JEDEC meeting minutes or any JEDEC policy manuals. (Geilhufe, Tr. 9622).

854. The net increase in variable costs for the alternative of programming CAS latency by blowing fuses is, therefore, approximately 6 cents per unit. The total cost increase is approximately 7 cents per unit, calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9589).

Response to Finding No. 854: Mr. Geilhufe's cost estimates are inaccurate because his methodology failed to account for certain cost savings. Furthermore, the per unit fixed cost estimates, product design are qualification costs, are unreliable because they are based on an inaccurate assumption that volume production for a first-tier manufacturer like Samsung, Infineon,

or Micron, was approximately 20 million units for a product that was well into its life cycle. (Geilhufe, Tr. 9562, 9726). Neither Mr. Geilhufe nor Rambus provided any record evidence to support this assumption. Mr. Geilhufe reviewed no evidence related to the cost to DRAM manufacturers for final test and good unit yield for the relevant period, other than the Peisl deposition, and some "confidential" evidence that is not in the record. (Geilhufe, Tr. 9706). He failed to interview anybody who attended JEDEC meetings during the relevant time period. (Geilhufe, Tr. 9623). Furthermore, Mr. Geilhufe did not do anything to ensure that the analysis that he did was the type of analysis that was done at JEDEC. (Geilhufe, Tr. 9622).

The record evidence suggests that the volume production level for a particular part is between 500 million and 1 billion units. The volume production for Micron's 64 meg SDRAM, including shrinks, was approximately 900 million units. (Lee, Tr. 10997). The volume production for Micron's 128 meg SDRAM part was also approximately 900 million units. (*Id.* 10998). The 256 meg SDRAM, which started it's life cycle in 2000, has already reached a volume production level of approximately 400 million units. (*Id.*). Even if Mr. Geilhufe's estimates of fixed costs were correct, if allocated over 900 million units, the per unit cost would be much lower than 2 cents; rather, it would be a tiny fraction of a cent.

855. If the DRAM manufacturer did not have antifuse or electrically blown fuse technology available and wished to use that technology, adding it to the manufacturing process would entail several million dollars in additional development costs. (Geilhufe, Tr. 9583-84).

Response to Finding No. 855: This proposed finding is incomplete in that it ignores the fact that the use of electrically-blown fuses by DRAM manufacturers is common. (CCFF 2159, 2172-2176).

(3) Scaling CAS Latency with Clock Frequency Was Not a Viable Alternative.

856. Professor Jacob's proposed alternative of scaling CAS latency with clock frequency involves having the DRAM either being informed of the frequency by the memory controller or

using some sort of internal circuitry to sense the frequency. The DRAM would then calculate the appropriate CAS latency to use based upon its own inherent latency. (Jacob, Tr. 5383).

Response to Finding No. 856: Complaint Counsel has no specific response to this proposed finding.

857. Complaint Counsel did not meet their burden of showing that scaling CAS latency with a clock frequency was a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs.

Response to Finding No. 857: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, it is incomplete because it omits the substantial evidence in the record that suggests that scaling CAS latency with clock frequency was a viable alternative. (CCFF 2178-2183).

858. To the contrary, the evidence in the record shows that scaling CAS latency with clock frequency was not a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs. First, implementation of scaling CAS latency with clock frequency would have resulted in higher costs. Second, scaling CAS latency with clock frequency is not an "alternative" at all because it would still infringe Rambus's patents.

Response to Finding No. 858: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Furthermore, the statement in this proposed finding about "higher costs" is contrary to the weight of the evidence which shows that scaling CAS latency with clock frequency would not have added any significant costs. (CCFF 2180-2183).

Furthermore, the only evidence in the record to suggest that this alternative would have been covered by Rambus patents was from Dr. Soderman. (Soderman, Tr. 9359). His testimony is unreliable for the following reasons.

A determination that a patent claim covers a product is a two step process. The first step requires that the court interpret the patent claim as it would be understood by a person of ordinary skill in the art as a question of law. (Fliesler, Tr. 8778). RPF 858 cites no expert testimony or other evidence to establish the proper interpretation of the patent claims.

The second step requires a factual determination that each element of the properly interpreted claim is present in the product. (Nusbaum, Tr. 1565-66). RPF 858 cites no expert testimony or other evidence to establish that each element of any claim of this patent correspond to elements of the proposed alternative.

Dr. Soderman's testimony in support of the legal conclusion that scaling CAS latency with clock frequency would infringe Rambus patents is not supported by reliable evidence. (Soderman, Tr. 9359). He did not identify which Rambus patent would be infringed. (*Id.*). He did not engage in any patent analysis whatsoever beyond testifying that the alternative would require "some sort of a register." (*Id.*). Dr. Soderman, therefore, did not testify that scaling CAS latency with frequency satisfied every element of a claim within a Rambus patent. He did not even testify that a "register," which he assumed this alternative would require, would be equivalent to the type of register claimed within Rambus patents.

Dr. Soderman's testimony in support of a proposed finding that Rambus patents cover scaling CAS latency with clock frequency is, therefore, unreliable.

859. Professor McAfee did not testify that this alternative was commercially viable. (McAfee, Tr. 7363).

Response to Finding No. 859: This proposed finding is misleading because it is also true that Professor McAfee did not testify that this alternative was not commercially viable. Furthermore, neither Dr. Rapp or Mr. Geilhufe provided testimony that this alternative was not commercially viable. (Rapp, Tr. 9810-11; Geilhufe, Tr. 9575-92 (discussion of CAS latency alternatives did not include scaling CAS latency with clock frequency)). For a more complete discussion of the evidence in support of its commercial viability, refer to CCFF 2178-2183.

860. Having the controller send the bus speed information to the DRAM would require extra pins and circuitry on the controller and, potentially, extra pins on the DRAM, adding manufacturing expense. (Soderman, Tr. 9359-60).

Response to Finding No. 860: This proposed finding is unreliable because it assumes that it would be necessary to have the memory controller send the bus speed information to the DRAM. However, it is not necessary to make that assumption. As Professor Jacob testified, in order to implement this alternative, the DRAM could sense the speed of the bus and internally calculate its own CAS latency. (Jacob, Tr. 5383-84).

Furthermore, this proposed finding is contrary to the weight of the evidence which shows that scaling CAS latency with clock frequency would not have added any significant costs. (CCFF 2180-2183).

861. Having the DRAM sense the bus speed would require complex and costly circuitry on the DRAM. (Soderman, Tr. 9358).

Response to Finding No. 861: This proposed finding is contrary to the weight of the evidence which shows that scaling CAS latency with clock frequency would have only required a simple circuit to implement. (*See* CCFF 2181).

862. In any event, scaling CAS latency with clock frequency is not an alternative to using a register to store a latency value because the latency value would still have to be stored in a register, violating Rambus's patents to the same extent as current SDRAMs do. (RX 1626 at 2; Soderman, Tr. 9359).

Response to Finding No. 862: This proposed finding is unreliable because it requires two assumptions that are not supported by the evidence in the record. First, it assumes that scaling CAS latency requires the use of a register. At trial, Dr. Soderman jumped from the conclusion that this alternative required storage to the conclusion that this alternative would require a register. (Soderman, Tr. 9359). However, there is evidence in the record that indicates that it is possible to store information by using a latch, which is not a register. (CCFF 2209). Second, this proposed finding assumes that the "register" which Dr. Soderman assumed was necessary to implement this alternative would satisfy all of the elements in Rambus's mode register claims. There is no evidence in the record to support that assumption for the reasons set forth in CCRF 858.

Furthermore, Respondent's use of RX 1626 is misleading because it is based on an assumption for which there is no evidentiary support in the record. RX 1626 refers to programming operating frequency in the mode register. (*Id.* at 2). However, it is not clear from RX 1626 standing alone whether the technology it discusses, programming operating frequency in the mode register, is the same technology that Dr. Jacob referred to as scaling CAS latency with clock frequency. (*Id.*). There is evidence, in fact, to suggest the contrary. In explaining scaling CAS latency with clock frequency, Dr. Jacob only mentioned that it could require a simple circuit to detect the bus frequency, not a mode register. (Jacob, Tr. 5384).

863. For example, this alternative would be covered by claim 1 of U.S. Patent 5,953,263, assigned to Rambus, which claims:

> "A synchronous semiconductor memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises:
> a programmable register to store a value which is representative of a delay time after which the memory device responds to a read request."

(CX 1517 at 29).

Response to Finding No. 863: This proposed finding is not supported by any evidence whatsoever in the record. Dr. Soderman did not identify any Rambus patent that contained claims covering the use of a register to scale CAS latency with clock frequency. (Soderman, Tr. 9359). He merely testified that this alternative would require "some sort of register." (*Id.*). For the reasons set forth in CCRF 862, it is inappropriate to assume that this alternative requires a register. It is also inappropriate to assume that if JEDEC had required the use of a register to implement this alternative, that it would have been equivalent to the "programmable register" described in claim 1 of U.S. Patent 5,953,263. There is no evidence in the record to support the latter. (Soderman, Tr. 9359 (could require some sort of register); Jacob, Tr. 5384 (could require a simple circuit)).

864. A claim covers a device if each and every claim element or "limitation" is found in that device. (Nusbaum, Tr. 1565-66). SDRAMs are synchronous memory devices that have memory sections containing a plurality of memory cells. (Rhoden, Tr. 359-60, 369-70). Moreover, "CAS latency" in SDRAMs refers to the delay time after which the SDRAM responds to a read request. (Rhoden, Tr. 382). As noted above, if CAS latency is scaled with clock frequency, CAS latency information would still have to be stored in a programmable register. Thus, each and every element of claim 1 of the '263 patent would be found in SDRAMs that implemented scaling CAS latency with clock frequency.

Response to Finding No. 864: The last statement in this proposed finding is a legal conclusion, which lacks any citation to the record and is therefore inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Dr. Soderman did not do anything approaching a claims analysis that could support the last sentence, and the testimony that he provided regarding the need for "some sort of register" to implement this alternative is unreliable for the reasons set forth in CCRF 858 and 863.

865. Scaling CAS latency with clock frequency was actually proposed by Micron as an alternative to programmable CAS latency for DDR2. At the March 2000 meeting of the JEDEC JC-42.3 subcommittee, Micron made a first showing entitled "Simplifying Read Latency for DDRII." (CX 154A at 9, 25-32). In its presentation, Micron noted that one approach would be to "offer devices with a fixed read latency." (CX 154A at 26). Under this approach, "[v]endors can offer different speed devices, each with a different fixed latency," but there would be the "[d]isadvantage" that "[u]sers may need to order different parts to cover different applications." (*Id.*).

Response to Finding No. 865: Respondent's use of CX0154A is misleading for the same reason that Respondent's use of RX 1626 was misleading. (Refer to CCRF 862). It is based on an assumption for which there is no evidentiary support in the record. CX1 154A refers to programming operating frequency in the mode register. (*Id.* at 29). However, it is not clear from CX0154A standing alone whether the technology it discusses, programming operating frequency in the mode register, is the same technology as what Dr. Jacob referred to as scaling CAS latency with clock frequency. (*Id.*). There is evidence, in fact, to suggest the contrary. In explaining scaling CAS latency with clock frequency, Dr. Jacob only mentioned that it could require a simple circuit to detect the bus frequency, not a mode register. (Jacob, Tr. 5384)

866. Micron went on to present a second approach: "offer devices with a programmable operating frequency; each operating frequency has a fixed read latency associated with it." (CX 154A at 27). In other words, Micron proposed to scale CAS latency with clock frequency.

Response to Finding No. 866: This proposed finding is misleading for the reasons set for in CCRF 862 and 865. It is simply not self-evident from CX0154A standing alone that what it refers to as "programmable operating frequency" is equivalent to Dr. Jacob's concept of scaling CAS latency with clock frequency. (CCRF 862 and 865). Because there is no testimony in the record to support that the two terms mean the same thing, this proposed finding is wholly unsupported by the evidence in the record. (*Id.*).

867. In an e-mail dated April 13, 2000 from Mark Kellogg of IBM to Art Kilmer of IBM, Mr. Kellogg discussed the proposals made by Micron at the March 2000 JEDEC meeting in the context of "the Rambus patents." (RX 1626 at 2). Mr. Kellogg noted that "[i]n the last JEDEC meeting, the option of a single latency device was pooh-poohed." (*Id.*). Mr. Kellogg went on to

discuss Micron's alternative proposal of scaling CAS latency with clock frequency. Mr. Kellogg stated:

> "[T]he alternate proposal from Micron (programming the frequency range instead of CAS Latency) was better received. The problem with the latter proposal (in my mind), was that nothing changed except the name assigned to the command register bits (originally defined as CAS Latency, now to be defined as frequency range or something similar). As such, I felt they were walking a fine line and that this change would not hold up in court as being anything other than an attempt to circumvent possible patent infringement via a term redefinition."

(*Id.*).

Response to Finding No. 867: This proposed finding is misleading for the reasons set for in CCRF 862. It is simply not self-evident from RX 1626 standing alone that what it refers to as "programmable operating frequency" is equivalent to Dr. Jacob's concept of scaling CAS latency with clock frequency. (CCRF 862). Because there is no testimony in the record to support that the two terms mean the same thing, this proposed finding is wholly unsupported by the evidence in the record. (*Id.*).

(4) Using Dedicated Pins to Identify the Latency Was Not a Viable Alternative.

868. Professor Jacob's proposed alternative of using an existing or dedicated pin to identify the latency involves a pin on the DRAM that would select one CAS latency if it received a high voltage and a different CAS latency if it received a low voltage. (Jacob, Tr. 5386-87).

Response to Finding No. 868: Complaint Counsel has no specific response to this proposed finding.

869. Complaint Counsel did not meet their burden of showing that using dedicated pins on the DRAM to select CAS latency was a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs.

Response to Finding No. 869: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*,

Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs. Furthermore, this proposed finding is incomplete because it omits the weight of the evidence in the record that indicates that using dedicated pins to set CAS latency was a viable alternative. (CCFF 2184-2218).

870. To the contrary, the evidence in the record shows that using dedicated pins on the DRAM to select CAS latency was not a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs, because it would be costlier and less reliable.

Response to Finding No. 870: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs. Furthermore, the statement in RPF 870 that using dedicated pins on the DRAM to select CAS latency was not a viable alternative because it was costlier or less reliable ignores the weight of the evidence in the record to the contrary. (Bechtelsheim, Tr. 5811 ("Personally, I actually preferred the pins because it was simpler, less effort on the system side"); Macri, Tr. 4765-77, *in camera* (

); *see also* CCFF 2190 - 2205).

871. This alternative would require additional wiring in the DIMM and from the DIMM to the memory controller. These additional wires can have a "noise glitch" – that is, the signals could be perturbed by adjacent signals – that would upset the CAS latency value and lead to improper operation of the DRAM. (Soderman, Tr. 9361-62).

Response to Finding No. 871: This proposed finding is unreliable because it is based on an assumption that is contrary to the weight of the evidence. This alternative would not require the use of additional wiring in order to avoid the use of a register. (*See* CCFF 2206-2211). If JEDEC had chosen to use a DC pin to implement this alternatives, the DC pin could hold the CAS latency value during system operation without a register. (Kellogg, Tr. 5126). Even if JEDEC had chosen not to use a DC pin, it still would not need a register to implement this

alternative. (Kellogg, Tr. 5126-27). It could have used a latch, which is not a register, to store the CAS latency value. (*Id.*).

872. Certain configurations of SDRAMs had no "no-connect" pins. (CX 234 at 84; Geilhufe, Tr. 9741-42). Certain others had only a single "no-connect" pin. (RX 2100-13 at 1; Polzin, Tr. 4026-28).

Response to Finding No. 872: This proposed finding is misleading because it omits the weight of the evidence in the record that indicates that almost all of the pinouts in Release 9 of JEDEC Standard 21-C have two or more no-connect pins available. (*See* CCFF 2196). JEDEC almost always provides for no-connect pins in its SDRAM and DDR SDRAM pinouts (Lee, Tr. 11037 (" I believe there's almost always no-connects provided.")). In Release 9 of Standards 21-C, forty-four out of forty-seven pinouts for SDRAM and DDR SDRAMs have no-connect pins that are available to use to set CAS latency. (CX0234 at 80-142).

Furthermore, the vref pin is hardly ever used. (Lee, Tr. 11035). It is, thereofre, available as a no-connect pin. (*Id.*). Counting the vref pin, forty-four out of forty-seven pinouts for SDRAMs and DDR SDRAMs have two or more no-connect pins available. (Lee, Tr. 11037; *see also* CCFF 2196).

873. Moreover, pins designated as "no connect" are not necessarily available for other uses because they may be used in testing. (Soderman, Tr. 9463-65).

Response to Finding No. 873: This proposed finding is unreliable because it is based on two assumptions that are not supported by any evidence in the record. First, there is no evidence in the record to support the assumption that no-connect pins are used in testing. Second, there is no evidence in the record to support the assumption that if a no-connect pin is used for testing, it cannot also be used to set CAS latency. To the contrary, there is substantial evidence in the record that indicates that a single pin can be used for two different purposes. (CCFF 2199-2201).

874. Pins designated as "no connect" also may be unavailable because they are reserved for uses in other configurations. For example, if a manufacturer used the same mask for x4, x8 and x16 configurations, and if a pin designated "no connect" in the x4 and x8 configurations was used as a data pin in the x16 configuration, that pin could not be used for other purposes in the x4 and x8 configurations; in other words, the pin would need to remain a "no connect" pin in the x4 and x8 configurations. (Lee, Tr. 11084-87).

Response to Finding No. 874: This proposed finding is inaccurate because Mr. Lee's testimony does not support the proposition. Instead, Mr. Lee's testimony supports the opposite proposition. During cross-examination, Mr. Lee was asked to assume a pinout that included x4, x8, and x16 configurations. (Lee, Tr. 11084; *see* CX0234 at 129 (showing the pinout that Mr. Lee was asked to testify about)). In the x4 and x8 configurations, there were several no-connect pins. (*Id.*). In the x16 configuration, one of those no-connect pins was used as a data pin. (*Id.*). The testimony of Terry Lee supports the proposition that even if the same mask is used for the x4, x8, x16 configurations, the fact that one of the no-connect becomes a data pin in the x16 configuration does not mean that there are effectively fewer no-connect pins in the x4 and x8 configurations. (Lee, Tr. 11086-87 ("Q. So, your options, if you're using the same set of masks, are either to use it as a co-connect or use it as DQ10?. . . A. In the x16, you're required to use it as a DQ10. . . And the x4, x8, it would be no-connect.")).

875. Pins designated as "no connect" may also be valuable for use in future, higher density generations of the product. As Gordon Kelley of IBM testified, using up a pin is not something that was done "easily, because once you use that pin up for a function, you don't have it available to you in the future for generation advance. As the memory densities increase, we need pins for more addressing of more address locations and those pins are very valuable for that feature, so this would have limited the number of generations of DRAM design that we could have used if we were to use up this pin." (Kelly, Tr. 2552-53).

Response to Finding No. 875: This proposed finding is unreliable because it assumes that Mr. Kelley's testimony on the use of an address pin to set CAS latency applies equally to the use of a "no-connect" pins to set CAS latency. There is no evidence in the record to support that assumption. Mr. Kelley provided testimony on the use of a pin to "address which burst

length you wanted to choose." (G. Kelley, Tr. 2551). Mr. Kelley's testimony was, therefore, limited to assessing the merits of adding an address pin to identify the burst length or CAS latency of a part. (*Id.* 2551-53). Based on his testimony, it appears that JEDEC would have had to weigh the value of adding an address pin in order to implement a new function against the need to add new address pins in order to support future densities. (*Id.*). However, the weight of the evidence in the record indicates that JEDEC would not have had to weigh the addition of an address pin to set CAS latency against the need to add new pins in order to support future densities. Instead, it supports that JEDEC would not have needed to add an address pin in order to implement this alternative. (*See* CCFF 2191-2196). JEDEC could have used existing no-connect pins. (*Id.*). Or, it could have multiplexed existing pins in order to implement this alternative. (*Id.* 2197-2201).

876. To achieve the same level of flexibility as SDRAMs and DDR SDRAMs which have three bits in the mode register for storing a CAS latency value, a manufacturer would have to add three pins to a DRAM with no pins available. (Soderman, Tr. 9362; Geilhufe, Tr. 9589-90). Moreover, since the packages in use in the 1990s were all rectangular and required pins to be added in multiples of two, four pins would have to be added. (Soderman, Tr. 9362-63; Geilhufe, Tr. 9590; Lee, Tr. 11082).

Response to Finding No. 876: This proposed finding is unreliable because it is based on the assumption that it would have been necessary to preserve all of the optional values for CAS latency that currently exist in the mode register. (Soderman, Tr. 9362, 9462-63). That assumption is contrary to the weight of the evidence. Dr. Soderman admitted that if the industry had decided that they only wanted two CAS latency values, then it would have had to use only one pin to implement this alternative. (Soderman, Tr. 9463). The weight of the evidence indicates that two CAS latency values would have served the needs of the predominant share of the market. (CCFF 2214-2218).

Furthermore, the weight of the evidence indicates that JEDEC could have used an existing pin to implement this alternative and would, therefore, not have had to add pins to the package.

(CCFF 2191-2201). JEDEC could have used existing no-connect pins to implement this alternative. (CCFF 2191-2196). Before the SDRAM standard was adopted, it could have reassigned an existing pin to set the CAS latency. (CCFF 2197). JEDEC could have asserted a super-voltage on an existing pin. (CCFF 2198). Or, it could have multiplexed existing pins in order to implement this alternative. (CCFF 2199-2201).

877. In its license negotiations with Rambus in 1994, Samsung was motivated to seek a non-assertion provision for non-Rambus-compatible uses of Rambus's inventions because of the on-chip DLL shown in Rambus's PCT application. (CX 2078, Karp Micron Depo. at 107-08, 119-20).

Response to Finding No. 877: This proposed finding about Samsung's effort to obtain a non-assertion provision for non-Rambus-compatible uses, in 1994, does not support the conclusion that the use of pins to set CAS latency was not a viable alternative.

Furthermore, the proposed finding is misleading because it suggests that Samsung understood that Rambus might assert claims to technologies within SDRAM, and that is not supported by Mr. Karp's testimony.

(CX2078 at 106-07 (Karp, Dep.), *in camera*). At best, Mr. Karp's testimony supports the proposition that

(*Id.* 107).

Mr. Karp did not believe at the time that SDRAM would compete with Rambus DRAM as a future high-performance memory. By the time Samsung began negotiating an agreement with Rambus in 1994, it had already been looking at using DLLs in future products. (CX2078 at 108 (Karp, Dep.)). Even though Mr. Karp assumed at that time that Samsung would try to run

SDRAMs faster and that they would therefore require DLLs,

(78 at 106-07 (Karp, Dep.), *in camera*). To the contrary, Mr. Karp testified that he did not think SDRAM would compete with Rambus DRAMs in the future. (CX2078 at 109 (Karp, Dep.)). When asked directly about whether anyone representing Rambus during negotiations with Samsung in 1994 told him that Rambus believed it had intellectual property rights that would cover SDRAM, Mr. Karp testified that he could not recall that. (CX2078 at 116-117 (Karp, Dep.)).

878. The number of pins required could not be reduced by having more than two voltage levels per pin. Although Professor Jacob has suggested that this could be done, he has never designed a circuit that would detect more than two voltage levels at high frequency. (Jacob, Tr. 11126). No SDRAM or DDR SDRAM parts support more than two voltage levels per pin in normal operation. (Jacob, Tr. 11125-26). Having more than two voltage levels on a pin would require sophisticated circuitry that would be easily perturbed by noise. (Soderman, Tr. 9363-64).

Response to Finding No. 878: The second sentence in this proposed finding is unreliable as evidence that it was not possible to implement this alternative by asserting a super-voltage on a pin. Professor Jacob has sufficiently reliable experience to testify that it was viable to assert more than two voltage levels on a pin for the reasons previously set forth in CCRF 786 and 790. The weight of the evidence indicates that JEDEC could have asserted a super voltage on an existing pin in order to implement this alternative. (CCFF 2198).

Furthermore, it ignores the weight of the evidence that indicates that JEDEC could have implemented this alternative by using no-connect pins (CCFF 2192-2196), multiplexing existing pins (CCFF 2199-2201), or adding DC pins (CCFF 2202-2205).

879. The first Rambus DRAM, the 4.5 megabit part built by Toshiba in the early 1990s, had a pin with three voltage levels. (Horowitz, Tr. 8549). Rambus did not want to use an extra pin for entering test mode and, instead, created an extra voltage level on one of the existing pins for that purpose. (*Id.*). Although Rambus, believed that the part had been built and designed with enough separation between the voltage levels to prevent confusion, in fact the part sometimes

failed because it entered test mode accidentally. (Horowitz, Tr. 8550-51). Rambus never used a pin with more than two voltage levels on subsequent Rambus DRAMs. (Horowitz, Tr. 8551).

Response to Finding No. 879: The statement in RPF 879 that Rambus never used a pin with more than two voltage levels on subsequent Rambus DRAMs is unreliable because evidence showing that a technology was not viable in an RDRAM-based architecture does not necessarily indicate that it would not be viable in an SDRAM-based architecture. DRAMs have a packetized architecture that operates differently from JEDEC-compliant SDRAMs and DDR SDRAMs (*see* CCFF 722, 751, 755, 1268, 1298, 1306 ("JEDEC-compliant SDRAM does not operate as a packetized system such as that described in the '898 specification.")). It is, therefore, entirely possible that technologies that are viable in an SDRAM-based system are not necessarily viable in an RDRAM-based system. There is no evidence in the record to support that the latter would not be true in the case of asserting multiple voltages on a pin.

880. Assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement, programming CAS latency by using dedicated pins would have resulted in approximately 4 cents in increased packaging costs per unit, compared to the cost of SDRAMs in the mid-1990s, because of the need for additional four pins. (Geilhufe, Tr. 9562-64, 9589-91). This 4-cent increase is a variable cost.

Response to Finding No. 880: This proposed finding is unreliable because the methodology that Mr. Geilhufe used to analyze the costs of alternative technologies is based on inaccurate assumptions, not the appropriate methodology to rely on to determine the viability of alternative technologies in this case, and more generally unreliable for the reasons set forth in CCRF 837.

In this proposed finding, the four cent increase in packaging costs per unit is based on the assumption that it would have been necessary to add four pins to implement this alternative. That assumption is invalid for the reasons set forth in CCRF 876.

881. The four cent increase cost estimate for this alternative is very conservative. First, standard packages generally add more than four pins – for example, the JEDEC SDRAM standards move from a 44-pin package to a 54-pin package, adding 10 pins, and then to a 66-pin package, adding 12 pins. (Geilhufe, Tr. 9590; CX 234 at 99-106). Thus, if there were not enough pins available on a certain standard package, one might have to move up to the next standard package, adding many more than the bare minimum of four pins.

Response to Finding No. 881: This proposed finding is inaccurate and unreliable for the reasons set forth in CCRF 880.

882. Second, in addition to the four pins on the DRAM, more pins would also be required on the memory controller; however, every pin on controllers is fully utilized, so pins would have to be added there. (Soderman, Tr. 9363; Geilhufe, Tr. 9591).

Response to Finding No. 882: This proposed finding is inaccurate and unreliable for the reasons set forth in CCRF 880.

883. Third, both a new, more expensive connector may be required to connect the DIMM to the motherboard, and more lines on the bus. (Geilhufe, Tr. 9590-91).

Response to Finding No. 883: This proposed finding is inaccurate and unreliable for the reasons set forth in CCRF 880.

(5) Identifying CAS Latency in the Read Command Was Not a Viable Alternative.

884. Professor Jacob's proposed alternative of identifying CAS latency in the read command would involve a different command sent from the controller to the DRAM for each desired CAS latency. (Jacob, Tr. 5389).

Response to Finding No. 884: Complaint Counsel has no specific response to this proposed finding.

885. Complaint Counsel did not meet their burden of showing that identifying CAS latency in the read command was a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs.

Response to Finding No. 885: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel

submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, it is incomplete because it omits the substantial evidence in the record that suggests that identifying CAS latency in the read command was a viable alternative. (CCFF 2219-2227).

886. To the contrary, the evidence in the record shows that, as with the alternative of scaling CAS latency with clock frequency, this is not really an alternative because it would still require storing latency information in a programmable register like the mode register in SDRAMs. (Soderman, Tr. 9365).

Response to Finding No. 886: As with Respondent's parallel proposed finding for scaling CAS latency with clock frequency, RPF 858, this proposed finding is not supported by any reliable evidence in the record. The only evidence in the record to suggest that this alternative would have been covered by Rambus patents was from Dr. Soderman. (Soderman, Tr. 9365).

A determination that a patent claim covers a product is a two step process. The first step requires that the court interpret the patent claim as it would be understood by a person of ordinary skill in the art as a question of law. (Fliesler, Tr. 8778). RPF 886 cites no expert testimony or other evidence to establish the proper interpretation of the patent claims.

The second step requires a factual determination that each element of the properly interpreted claim is present in the product. (Nusbaum, Tr. 1565-66). RPF 886 cites no expert testimony or other evidence to establish that each element of any claim of this patent correspond to elements of the proposed alternative.

Dr. Soderman's testimony in support of a legal conclusion that identifying CAS latency in the read command would infringe Rambus patents is not supported by any evidence. (Soderman, Tr. 9365 (testifying that identifying CAS latency in the read command would "need a register similar to a mode register")). He did not identify which Rambus patent would be infringed. (*Id.*).

He did not engage in any patent analysis whatsoever beyond testifying that the alternative would require a register that was similar to a mode register. (*Id.*). Dr. Soderman, therefore, did not testify that identifying CAS latency in the read command satisfied every element of a claim within a Rambus patent. He did not even testify that a "register," which he assumed this alternative would require, would be equivalent to the type of register claimed within Rambus patents.

Furthermore, this proposed finding is unreliable because it assumes that a register is necessary to implement this alternative. (CCFF 2224). To the contrary, a latch could be used as storage after the command which identified the CAS latency had been sent over the bus. (Jacob, Tr. 5393). The weight of the evidence indicates that a latch is not a register. (Jacob, Tr. 5395; Kellogg, Tr. 5126-27; *see also* (CCFF 2208-2210)).

887. For example, this alternative would be covered by claim 1 of U.S. Patent 5,953,263, *assigned to Rambus, which claims*:

> A synchronous semiconductor memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises:
> a programmable register to store a value which is representative of a delay time after which the memory device responds to a read request.

(CX 1517 at 29).

Response to Finding No. 887: This proposed finding is not supported by any evidence whatsoever in the record. Dr. Soderman did not identify any Rambus patent that contained claims covering the use of a register to identify CAS latency in the read command. (Soderman, Tr. 9364-65). He merely testified that this alternative would require a register that "looks like a mode register." (*Id.*). For the reasons set forth in CCRF 886, it is inappropriate to assume that this alternative requires a register. It is also inappropriate to assume that if JEDEC had required the use of a register to implement this alternative, that it would have been equivalent to the "programmable register" described in claim 1 of U.S. Patent 5,953,263. There is no evidence

in the record to support the latter. (Soderman, Tr. 9365 (could require a register that "looks like a mode register"); Jacob, Tr. 5393 (could require a latch)).

888. A claim covers a device if each and every claim element or "limitation" is found in that device. (Nusbaum, Tr. 1565-66). SDRAMs are synchronous memory devices that have memory sections containing a plurality of memory cells. (Rhoden, Tr. 359-60, 369-70). Moreover, "CAS latency" in SDRAMs refers to the delay time after which the SDRAM responds to a read request. (Rhoden, Tr. 382). As noted above, if CAS latency is identified in the read command, CAS latency information would still have to be stored in a programmable register. Thus, each and every element of claim 1 of the '263 patent would be found in SDRAMs that implemented identifying CAS latency in the read command.

Response to Finding No. 888: The last statement in this proposed finding is a legal conclusion, which lacks any citation to the record and is therefore inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Dr. Soderman did not do anything approaching a claims analysis that could support the last sentence, and the testimony that he provided regarding the need for a register to implement this alternative is unreliable for the reasons set forth in CCRF 886 and 887.

889. Professor Jacob testified that this alternative would not require a register because a "latch" could be used to store the latency information instead. (Jacob, Tr. 5393). This distinction is of no consequence because a register is a generic class of storage (Soderman, Tr. 9450-51), and one type of register is a latch. (*Id.*; Horowitz, Tr. 8508-09).

Response to Finding No. 889: This proposed finding is unreliable because the weight of the evidence indicates that a latch is not a register. (CCFF 2225).

Furthermore, this proposed finding is misleading because Dr. Horowitz only testified that a latch *might* be a register. (Horowitz, Tr. 8508). It depends on how the latch is used and what circuitry is put in. (*Id.*). His testimony only supports RPF 889 if one makes two assumptions. First, one assumes that using a latch to identify CAS latency in the read command is an example of the kind of use that could convert a latch into a register. Second, one must assume that the

circuitry required to convert a latch into a register would be required in order to implement this alternative. There is no evidence in the record to support either assumption.

890. Professor Jacob concedes that "a register might be built out of latches." (Jacob, Tr. 5393). He testified that: "A latch is a specific implementation. A register implies how a piece of storage is being used." (*Id.*). In this case, if latches were used to store latency information, they would be used for precisely the same purpose as the mode register in an SDRAM.

Response to Finding No. 890: The last sentence in this proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, the last sentence is misleading because it fails to account for the complete lack of evidence in the record that would allow Respondent to equate the storage of latency information identified by a read command with the storage of CAS latency information in a mode register. There is a significant difference between identifying CAS latency in the read command and the use of a mode register in SDRAM. For the mode register in an SDRAM, a mode register set command programs CAS latency. (CCFF 1135). However, there would be no need for a mode register set command if every read command contained encoded CAS latency information. There is no evidence in the record to support that a person of ordinary skill in the art would overlook this distinction and equate the use of a latch to identify CAS latency in the read command with the use of a mode register to program CAS latency.

891. Identifying CAS latency in the command would have the negative side effect of limiting the simultaneous issuing of independent commands that is possible with the current command set. (Jacob, Tr. 5599).

Response to Finding No. 891: This proposed finding is incomplete because it ignores Dr. Jacob's testimony about the advantages associated with identifying CAS latency in the

read command. (Jacob, Tr. 5391 ("The advantage would be that you would eliminate the mode register and the circuitry required to decode special commands and put that information into the mode register, so it would make the part potentially smaller and simpler.")).

892. This alternative may also be covered by U.S. Patent No. 5,835,956, which is assigned to Samsung and was not considered by Professor Jacob. (RX 1308; Jacob, Tr. 5599-601). Claim 1 of that patent claims a synchronous memory device that is capable of receiving latency mode information and selecting one of a plurality of latency modes in response to the information. (RX 1308 at 90).

Response to Finding No. 892: This proposed finding is unreliable. There is no evidence in the record to support that U.S. Patent No. 5,835,956 (the '956 patent) is relevant to this case. Consequently, there is no evidence to support that Dr. Jacob should have considered this patent.

A determination that a patent claim covers a product is a two step process. The first step requires that the court interpret the patent claim as it would be understood by a person of ordinary skill in the art as a question of law. (Fliesler, Tr. 8778). RPF 892 cites no expert testimony or other evidence to establish the proper interpretation of claim 1 of the 956 patent. For example, in his discussion of identifying CAS latency in the read command, Dr. Soderman did not identify this patent. (Soderman, Tr. 9364-65).

The second step requires a factual determination that each element of the properly interpreted claim is present in the product. (Nusbaum, Tr. 1565-66). RPF 892 cites no expert testimony or other evidence to establish that each element of claim 1 of the 956 patent corresponds to elements of the proposed alternative.

(6) Staying with Asynchronous Technology Was Not a Viable Alternative.

893. Complaint Counsel did not meet their burden of showing that staying with asynchronous technology was a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs.

Response to Finding No. 893: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs. Furthermore, this proposed finding is contrary to the weight of the evidence. (CCFF 2228-2233).

894. To the contrary, the evidence in the record shows that staying with asynchronous technology was not a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs because asynchronous technology was not capable of achieving the performance necessary for high speed operation.

Response to Finding No. 894: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs. Furthermore, this proposed finding is contrary to the weight of the evidence. (CCFF 2228-2233). This proposed finding is unreliable. The evidence in the record shows that, in 1995, asynchronous BEDO could have performed better than SDRAM in 66 mhz busses. (CX2632 at 5). Micron had been cycling BEDO at speeds up to 125 mhz in this time period. (*Id.*). Furthermore, asynchronous memory could have been improved incrementally just as synchronous memory has been. (Williams, Tr. 829-30; *see* CCFF 2233).

895. SDRAM, SLDRAM and RDRAM are all synchronous designs. (Jacob, Tr. 5601-02).

Response to Finding No. 895: The fact that SDRAM, SLDRAM and RDRAM are synchronous memories does not support the conclusion that JEDEC could not have chosen an asynchronous memory path. For the evidence in the record that supports that asynchronous memory was a viable alternative to programmable CAS latency, *see* CCFF 2228-2233.

896. Despite the success of SDRAM, a substantial amount of work on asynchronous technology has continued during the last decade at both the academic and commercial levels. (Jacob, Tr. 5602; Horowitz, Tr. 8560-61).

Response to Finding No. 896: Complaint Counsel has no specific response to this proposed finding.

897. When Dr. Horowitz began working on what was to become RDRAM, he had substantial experience in asynchronous designs. Some of Dr. Horowitz's Ph.D. students had done their dissertations in asynchronous design, and Dr. Horowitz had himself done studies comparing asynchronous to synchronous designs. (Horowitz, Tr. 8559).

Response to Finding No. 897: This proposed finding is irrelevant because Dr. Horowitz's testimony at trial is limited to the viability of an asynchronous protocol for an RDRAM-based memory. (Horowitz, Tr. 8559-60). Evidence showing that a technology was not viable for a narrow bus architecture like RDRAM does not necessarily indicate that it would not be viable in a wide bus architecture like SDRAM. DRAMs have a packetized architecture that operates differently from JEDEC-compliant SDRAMs and DDR SDRAMs (*see* CCFF 722, 751, 755, 1268, 1298, 1306 ("JEDEC-compliant SDRAM does not operate as a packetized system such as that described in the '898 specification.")). It is, therefore, entirely possible that technologies that are viable for wide bus architectures are not necessarily viable for narrow bus architectures like RDRAM. There is no evidence in the record to support that the latter would not be true in the case of using an asynchronous protocol for a wide bus architecture.

898. Dr. Horowitz decided that a synchronous design would be necessary for RDRAM because he did not believe that one could build a very high-performance asynchronous interface. (Horowitz, Tr. 8498). As a circuit designer, Dr. Horowitz realized that when a signal passes through a block of circuitry, the amount by which it is delayed is subject to some uncertainty because of fluctuations in certain parameters such as temperature and voltage. (Horowitz, Tr. 8499-500). In the absence of a timing reference, like the clock in a synchronous system, as the signal continues to travel through more and more blocks, the amount of uncertainty will grow so that it will not be possible to predict with any accuracy when data will arrive. (*Id.*). For high performance, the amount of uncertainty must be kept to a small, predictable amount; this requires a synchronous system. (Horowitz, Tr. 8501-02).

Response to Finding No. 898: This proposed finding is unreliable for the reasons set forth in CCRF 897.

899. Asynchronous memories are very dependent on loading on the bus – that is, how many other chips are on the bus. In a general purpose environment, the loading of the bus can vary; consequently, asynchronous memories do not perform well in a bus environment at high frequencies. (Soderman, Tr. 9366).

Response to Finding No. 899: This proposed finding is incomplete because it omits the substantial evidence in the record that shows that asynchronous memory was a viable alternative to programmable CAS latency. (CCFF 2228-2233).

900. It was generally understood in the 1990s that asynchronous memories were not capable of reaching the speeds that would be required for future DRAMs. For example, an article by a Fujitsu engineer published in 1996 states that "[a]synchronous DRAMs, be that EDO or Burst EDO, can not keep up with bus speeds of over 66 MHz." (RX 2099-4 at 4). Jacquelyn Gross of Hewlett-Packard, formerly of Compaq, testified that it was Compaq's view in the 1996-97 time frame that asynchronous technology was limited in the bandwidth it could achieve and that synchronous technology "provided higher benefits." (Gross, Tr. 2347). Steve Polzin of AMD testified that in the 1996-97 time frame it was his opinion that, due to inherent limitations, asynchronous technology had less "headroom," that is less of an ability to offer improved performance over time, than synchronous technology. (Polzin, Tr. 4033-35).

Response to Finding No. 900: This proposed finding is incomplete because it omits the substantial evidence in the record that shows that asynchronous memory was a viable alternative to programmable CAS latency. (CCFF 2228-2233).

901. Burst EDO was an asynchronous type of DRAM that Micron was "strongly pushing" in the mid-1990s. (Williams, Tr. 822-823, 879). A 1995 Micron publication entitled "The Burst EDO DRAM Advantage" raises a question about the viability of Burst EDO ("BEDO") at bus speeds greater than 75 MHz and states that "BEDO will probably reach its limit somewhere around 100 MHz." (CX 2632 at 5).

Response to Finding No. 901: This proposed finding is misleading because it fails to appropriately qualify the language quoted from the document. The statement indicating a limit to BEDO operation around 100 mhz was characterizing the limits of BEDO parts that met the current specification for BEDO. (CX2632 at 5). As the document states, to reach frequencies beyond 100 mhz, "the actual I/O interface w[ould] probably need to change also from the current

LVTTL, to something more appropriate for the higher frequencies." (*Id.*). Mr. Williams, the author of CX2632, testified that improvements could have been made to increase the performance of BEDO devices. (Williams, Tr. 829-30).

902. Burst EDO was standardized by JEDEC in March 1995. (Williams, Tr. 873, 879-80; RX 585 at 1). However, Burst EDO failed in the marketplace in competition with SDRAM. (Williams, Tr. 829).

Response to Finding No. 902: The statement that BEDO failed in the marketplace mischaracterizes the evidence in the record. The weight of the evidence is contrary to the latter. (CCFF 2228-2233). As Mr. Williams' testified, BEDO failed to achieve sufficient market acceptance because, by 1995, SDRAM had already gained too much momentum. (Williams, Tr. 829 ("[T]he momentum behind the Synchronous DRAM actually killed burst EDO.")).

b. Programmable Burst Length.

903. Complaint Counsel, through Professor Jacob, have suggested the following possible alternatives to programmable burst length in SDRAMs:

(1) Use fixed burst length parts;

(2) Program burst length by blowing fuses on the DRAM;

(3) Use dedicated pins to transmit burst length information from the controller to the DRAM;

(4) Explicitly identify burst length in the read command;

(5) Use a burst terminate command;

(6) Use a CAS pulse to control data output.

(Jacob, Tr. 5397-5412).

Response to Finding No. 903: Complaint Counsel agrees that RPF 903 accurately represents a list of Dr. Jacob's proposed alternatives to programmable burst length.

(1) Use of Fixed Burst Length Parts Was Not a Viable Alternative.

904. Professor Jacob's proposed alternative of using fixed burst length parts, similar to his fixed CAS latency alternative, involves fixing the burst length of the DRAM during the design phase, manufacturing phase or packaging phase.

Response to Finding No. 904: Complaint Counsel agrees that this finding accurately represents Dr. Jacob's testimony that the burst length of a part could have been fixed during the design phase, manufacturing phase or packaging phase. (Jacob, Tr. 5398-99).

905. Complaint Counsel did not meet their burden of showing that the use of fixed burst length parts was a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs.

Response to Finding No. 905: This finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Furthermore, RPF 905 is contrary to the weight of the evidence in the record. (*See* CCFF 2237-2260).

906. To the contrary, the evidence in the record shows that the use of fixed burst length parts was not a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs because multiple fixed burst length parts would have been required, leading to higher costs and logistical difficulties for DRAM manufacturers and users.

Response to Finding No. 906: This finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Furthermore, RPF 905 is contrary to the weight of the evidence in the record. (*See* CCFF 2237-2260).

The weight of the evidence suggests that the cost of fixed burst length would have been relatively similar to programmable burst length. (Kellogg, Tr. 5132).

907. Different burst lengths are required for different applications, so multiple fixed burst length parts would be required for this alternative. (Soderman, Tr. 9368-69). As Gordon Kelley of IBM testified with respect to programmable burst length:

> "The programmable feature allowing you to make that selection when the PC or the computer powered up was a nice feature because it allowed you to use devices that were common from multiple suppliers, put them into many different types of machines. Some of them would be a burst length of one, some would be a burst length of four, with the same part that was programmed at power-up. One of the advantages of that is that that drives low cost. The producer does not have to maintain multiple part numbers. One part number fits many applications. That's one of the drives to low cost."

(Kelley, Tr. 2550-51).

Response to Finding No. 907: This finding is incomplete because it ignores the evidence in the record indicating the disadvantages associated with programmable burst length and the advantages associated with fixed burst length parts.

Mr. Kellogg, himself, provided testimony outlining the advantages of fixing burst length at the design phase in the 1991-1992 time frame. (Kellogg, Tr. 5117-18). He testified that it would have simplified the design and thereby reduced the design cycle time necessary to implement it. (*Id.*). It would have improved the performance of SDRAM by eliminating the propagation delay that occurs when the circuitry necessary to implement programmable burst length is driven. (*Id.*). It would reduce the test costs associated with programmable burst length because it would not have been necessary to test a part for its ability to work with different burst length options. (*Id.*).

Furthermore, assuming that CAS latency and burst type were fixed as well, a fixed burst length could have potentially eliminated the mode register, which would have made the part smaller and therefore potentially cheaper. (Jacob, Tr. 5401-02).

908. The mode register in SDRAMs and DDR SDRAMs reserves three bits for burst length, allowing for up to eight different burst length values. (CX 234 at 150).

Response to Finding No. 908: This proposed finding does not support the conclusion that fixed burst length was not a viable alternative because it ignores the substantial evidence in the record that indicates that it was not necessary to allow for up to eight different CAS

latency values. (CCFF 2247-2255 (indicating that at most JEDEC would have needed to standardize two different burst length values)). Furthermore, it ignores the fact that Mr. Sussman testified that he "had a lot of arguing to do to get the degree of programmable features [programmable CAS latency and burst length] into the [JEDEC standard]." (Sussman, Tr. 1380).

909. Release 4 of JEDEC Standard 21-C (November 1993), which contains the first published SDRAM standard, provided specified two required burst length values (4 and 8) and three optional burst length values (1, 2, and full page). (JX 56 at 114). Release 9 of JEDEC Standard 21-C (August 1999), which contains the first published DDR SDRAM standard, specified three required burst length values for SDRAMs (2, 4, and 8) and two optional values (1 and full page); it also specified three required burst length values for DDR SDRAMs (2, 4, and 8). (CX 234 at 150).

Response to Finding No. 909: Complaint Counsel does not disagree that finding makes an accurate statement about the number of required and optional burst lengths in Release 4 and Release 9 of JEDEC Standard 21-C. However, this statement does not support the conclusion that fixed burst latency was not a viable alternative because it ignores the weight of the evidence in the record that indicates that the requirements of the industry would have predominantly been served if JEDEC had standardized burst lengths of 4 and 8. (CCFF 2254).

910. Burst lengths of one are used in graphics applications. (Lee, Tr. 11076).

Response to Finding No. 910: This finding is incomplete because the weight of the evidence indicates that, at most, JEDEC would have needed to standardize burst lengths of 4 and 8. (CCFF 2254). Use of burst lengths of 1 and 2 has not been widespread. (Lee, Tr. 11014).

This finding is unreliable as evidence that fixed burst length was not a viable alternative because it omits the fact that graphics parts do not share the same die as main memory parts. (Lee, Tr. 11064). This means that the cost analysis for main memory parts must be separated from the cost analysis for graphics memory. (Lee, Tr. 11065 ("Q. And the 64-meg x32 SDRAM that's used for graphic purposes that has a CAS latency of one meets a JEDEC standard, does it not? A. Yeah, but I guess I'm a little confused about your question, because I think you're establishing

amortization of the costs, and that's a different die. The parts for graphics are usually on a completely different die than main memory, so the number of latencies supported on graphics doesn't necessarily correspond with what we're doing in the main memory part.")).

JEDEC tends to focus on main memory parts when it develops standards. (Wagner, Tr. 3828 ("In the graphics space, they don't really put a lot of effort in JEDEC focused on our specific needs.")). Consequently, for the purposes of evaluating whether JEDEC would have considered fixed burst length to be a viable alternative, facts about the burst length needs of the main memory industry may be more relevant than facts about the burst length needs of the graphics segment.

911. Micron sells SDRAMs that allow for five different burst lengths (1, 2, 4, 8 and full page). (RX 2100-13 at 1; Lee, Tr. 11078-80).

Response to Finding No. 911: This finding is unreliable because even though Micron may sell a part that could operate with five different burst lengths does not mean that customers actually use five burst lengths. To the contrary, the weight of the evidence indicates that, at most, JEDEC would have needed to standardized burst lengths of 4 and 8. (CCFF 2254). Use of burst lengths of 1 and 2 has not been widespread. (Lee, Tr. 11014; *see also* CCFF 2248-2250, 2252).

912. Mark Kellogg of IBM noted that a disadvantage of fixing burst length in the manufacturing process would be that if a manufacturer did not have enough parts of the right burst length in stock, there could be a time lag of two weeks to one month before parts could be delivered. (Kellogg, Tr. 5119). Mr. Kellogg recommended to his company in 1992 that they support the programmable burst length feature because "[i]t offered us the greatest flexibility. We had a lot of applications." (Kellogg, Tr. 5132).

Response to Finding No. 912: This proposed finding is incomplete because it omits that Mr. Kellogg also testified that the manufacturing costs associated with fixed burst length and the use of a mode register to program burst length are "relatively similar." (Kellogg, Tr. 5132).

Furthermore, it ignores the advantages associated with fixed burst length parts. (CCFF 2239-2240).

913. A fixed burst length would have been "very, very bad for AMD." (Polzin, Tr. 3994). AMD designed processors to use a burst length of eight "for performance reasons," but because Intel processors use a burst length of four, fixing burst length would have meant that manufacturers would most likely produce burst length four parts. (*Id.*).

Response to Finding No. 913: The statement in this finding that fixed burst length would have been "very, very bad for AMD" is misleading because it fails to appropriately qualify the statement in order to accurately reflect Mr. Polzin's testimony. Mr. Polzin testified that a fixed burst length of four would have been very bad for AMD, in 2000, because of lock-in related concerns like compatibility and delay in schedule. (Polzin, Tr. 3993-3994 (AMD had fine-tuned its processors over the years to work best with a burst length of 8 and was in the middle of a product launch)). His testimony does not support the conclusion that fixed burst length was not a viable alternative before 1996. To the contrary, his testimony supports the conclusion that JEDEC could have served the predominant share of the market if it had standardized fixed burst length parts of 4 and 8. (Polzin, Tr. 3994; CCFF 2254). It is also fair to use Mr. Polzin's testimony to support the proposition that AMD either would have supported the standardization of either a fixed burst length of 8 part, or fixed burst length parts of 4 and 8. (Polzin, Tr. 3994).

Mr. Polzin's testimony was in response to a follow-up question about which workarounds to Rambus patents had AMD considered after it became aware of Rambus patents in 2000. (Polzin, Tr. 3987-90). At that time, AMD would have been motivated to encourage DRAM manufacturers to stay with the technologies that they had been planning to use before Rambus began to assert its SDRAM and DDR SDRAM patents. When AMD learned about Rambus patents, it was in the middle of trying to launch its DDR-based chipset, IGD4. (Polzin, Tr. 3989).

Switching to fixed burst length in 2000 would have interfered with AMD's planned product launch. (Polzin, Tr. 3989).

Furthermore, Mr. Polzin assumed that JEDEC would have standardized a fixed burst length of four. (Polzin, Tr. 3994). He, therefore, concluded that fixed burst length of four would have been very bad for AMD because AMD processors are fine-tuned to operate with a burst length of eight. (*Id.* ("AMD designed its microprocessors to have its natural burst length to be 64 bytes, which is eight cycles of data. Knowing that the DRAMs had that capability, we decided to take advantage of that capability for performance reasons.")). Had Mr. Polzin assumed that JEDEC would have standardized fixed burst lengths of 4 and 8, his testimony likely would have been different.

914. JEDEC originally intended to fix the burst length at four in the DDR2 SDRAM standard . (Soderman, Tr. 9369; Macri, Tr. 4673-74). After further review by the DRAM manufacturers and the user community, it was determined that programmable burst length needed to be retained. (Soderman, Tr. 9369). DDR2 SDRAMs continue to have three bits in the mode register reserved for burst length, allowing for up to eight different burst length values. (RX 2099-14 at 21; RX 2099-39 at 20; Soderman, Tr. 9370). DDR2 SDRAMs currently require burst lengths of four and eight. (RX 2099-14 at 21; RX 2099-20 at 22; Soderman, Tr. 9369). This may change in the future; thus, the flexibility provided by the mode register is very important. (Soderman, Tr. 9370).

Response to Finding No. 914: This proposed finding is misleading because it omits the fact that lock-in explains the need to retain programmable burst length in DDR II SDRAM. (*See* CCFF 3251-3252).

The goal of the DDR II Task Group was to create a standard that was backwards compatible with DDR SDRAM. (Kellogg, Tr. 5193; Macri, Tr. 4627-29; CX0392 at 3; *see also* CCFF 3245). There is a strong preference for backwards compatibility in the DRAM industry. (CCFF 3247-3249).

The weight of the evidence indicates that JEDEC retained programmable burst length in the standard because of a need to ensure backwards compatibility, not because programmable burst

length is a superior technology in comparison to fixed burst length. (*See* CCFF 3251-3252). In 2000, changing to a single fixed burst length that was not compatible with the preferred burst length of a particular user would have required several years of design work in order to accommodate a burst length that the user had not anticipated as being the only burst length available. (*See* CCFF 3252).

915. The fixed burst length alternative would have resulted in increased costs.

Response to Finding No. 915: This finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Furthermore, RPF 905 is contrary to the weight of the evidence in the record. (*See* CCFF 2237-2260).

The weight of the evidence suggests that the cost of fixed burst length would have been relatively similar to programmable burst length. (Kellogg, Tr. 5132).

916. There would have been an increase in design, photo tooling and qualification costs because multiple products would have had to be designed and manufactured rather than just one. (Geilhufe, Tr. 9679, 9682-83, 9690). As in the fixed CAS latency alternative, a minimal design effort would have been required for each different burst length; one mask would have had to be changed for each different burst length; and each different burst length part would have had to be qualified before it could have been sold. (Geilhufe, Tr. 959).

Response to Finding No. 916: This proposed finding is unreliable for the reasons set forth in CCRF 790 (explaining why Mr. Geilhufe's methodology for this case, in contrast to Dr. Jacob's, is unreliable).

Furthermore, the statement about added photo tool costs is contracted by the weight of the evidence. (*See* CCFF 2256-2258 (fixed burst length would not have involved extra photo tool costs) and CCFF 2259-2260 (fixed burst length would not have involved extra design cost)).

917. There would have been a decrease in testing costs due to the fact that each part would have had to be tested for a single burst length rather than multiple burst lengths. (Geilhufe, Tr. 9594).

Response to Finding No. 917: Complaint Counsel does not disagree with Mr. Geilhufe's testimony about the reduced test costs associated with fixed burst length, as it is supported by the weight of the evidence. (*See* CCFF 2239).

918. There would have been additional inventory cost due to four different burst lengths parts being manufactured, one less than the number of required and optional burst lengths in the original SDRAM standard, instead of a single programmable burst length part. (Geilhufe, Tr. 9595; JX 56 at 114). Mark Kellogg of IBM testified that there would be an "economic disadvantage" from having multiple part numbers corresponding to different burst lengths. (Kellogg, Tr. 5119).

Response to Finding No. 918: This proposed finding is unreliable because it assumes that it would have been necessary to manufacture four different burst length parts. That assumption is contrary to the weight of the evidence. The weight of the evidence indicates that JEDEC at most would have had to standardize two different burst lengths at any given time. (*See* CCFF 2247-2250, 2252-2255)). Furthermore, there is substantial evidence in the record to support the conclusion that JEDEC would have supported a single fixed burst length part before 1996. (*See* CCFF 2250).

The reference to Mr. Kellogg's testimony in this finding is misleading and incomplete. It omits that fact that Mr. Kellogg qualified his testimony. He testifed that there would be "some economic disadvantage" (Kellogg, Tr. 5119) without specifying how significant that disadvantage would have been perceived, in 1991-1992, in comparison to a Rambus royalty that was associated with programmable burst length. It also omits the fact that Mr. Kellogg testified that the cost associated with fixed burst length was relatively similar to the cost of programmable burst length. (Kellogg, Tr. 5132).

919. The fixed burst length alternative would have resulted in the following approximate net costs compared to SDRAM in the mid-1990s, assuming a first-tier DRAM manufacturer and a

product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: $100,000 increase in product design costs per latency; $50,000 increase in photo tooling costs per latency; one cent decrease per unit in testing costs at wafer sort; three cents per unit increase in inventory costs; and $250,000 increase in qualification costs per latency. (Geilhufe, Tr. 9562-64, 9594-95).

Response to Finding No. 919: This proposed finding is unreliable and irrelevant because it is based upon Mr. Geilhufe's methodology, which is unreliable and irrelevant for the reasons set forth in CCRF 837. As previously set forth , Mr. Geilhufe's assumption that the volume production level for a first tier manufacture is 20 million units is contrary to the weight of the evidence. The record evidence suggests that the volume production level for a particular part is between 500 million and 1 billion units. (Lee, Tr. 10997). The volume production for Micron's 64 meg SDRAM was approximately 900 million units. (*Id.* 10998). The volume production for Micron's 128 meg SDRAM was approximately 900 million units. (*Id.*).

Furthermore, the statement about added photo tool costs is contracted by the weight of the evidence. (*See* CCFF 2256-2258). The weight of the evidence in the record indicates that there would have been no added photo tool costs. (*Id.*).

Additionally, the statement about added design costs is contradicted by the weight of the evidence. (*See* CCFF 2259-2260). To the contrary, the weight of the evidence indicates the design cost associated with fixed burst length would have been lower than the design cost associated with programmable burst length. (*Id.*). Even if Mr. Geilhufe's estimate of fixed costs were correct, if allocated over 900 million units, the per unit cost would be much lower than 2 cents, but rather would be a tiny fraction of a cent.

920. The net increase in variable costs for the fixed burst length alternative is, therefore, approximately 2 cents per unit. The total cost increase is approximately 4 cents per unit, calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9595-96).

Response to Finding No. 920: The total cost increase per unit in this finding is unreliable because Mr. Geilhufe's estimates for added fixed costs per unit are unreliable. Mr. Geilhufe's fixed cost estimates, product design and qualification costs, are based on the inaccurate assumption that volume production for a first-tier manufacturer like Samsung, Infineon, or Micron, was approximately 20 million units for a product that was well into its life cycle. (Geilhufe, Tr. 9562, 9726). Although Mr. Geilhufe agreed that further DRAM shrinks were possible off of the DRAM design whose cost he was estimating, he did not consider the effect of a shrink on the volume production level of a particular part. (Geilhufe, Tr. 9726 ("It's possible that there are further shrinks, but I -- I assumed that 20 million units could be built off that one design effort.")).

The weight of the evidence suggests that the volume production level for a particular part is substantially higher than 20 million units. The volume production for Micron's 64 meg SDRAM, including shrinks, was approximately 900 million units. (Lee, Tr. 10997). The volume production for Micron's 128 meg SDRAM part was also approximately 900 million units. (*Id.* 10998). The 256 meg SDRAM, which started it's life cycle in 2000, has already reached a volume production level of approximately 400 million units. (*Id.*).

Furthermore, the variable per unit cost estimates are unreliable for the reasons set forth in CCRF 837.

921. If both CAS latency and burst length were fixed, one would need to multiply the number of latencies by the number of burst lengths to calculate the total number of parts required. For example, if there were three latencies and four burst lengths, 12 parts would be required. (Geilhufe, Tr. 9601). Fixing both CAS latency and burst length would thus increase inventory costs by far more than the increase that woudl result from fixing CAS latency or burst length, but not both. (*Id.*).

Response to Finding No. 921: This proposed finding is unreliable because it is based on the assumption that it would have been necessary to standardize three fixed CAS latency parts and four burst length parts. (Geilhufe, Tr. 9601). That assumption is contrary to the weight

of the evidence. The weight of the evidence indicates that, at most, JEDEC would have needed to standardize two fixed CAS latencies and two fixed burst lengths. (*See* CCFF 2149-2153, 2247-2250, 2252-2255). Using Mr. Geilhufe's methodology to calculate the total number of parts needed to implement fixed CAS latency and burst length, the weight of the evidence indicates that, at most, only four parts per density would have been required if both fixed CAS latency and burst length were required. (CCFF 2255).

(2) Programming Burst Length with Fuses Was Not a Viable Alternative.

922. Professor Jacob's proposed alternative of setting burst length with fuses is similar to his corresponding proposed alternative for programming CAS latency with fuses. (Jacob, Tr. 5403).

Response to Finding No. 922: Complaint Counsel has not specific response to this finding.

923. Complaint Counsel did not meet their burden of showing that setting burst length with fuses was a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs.

Response to Finding No. 923: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (*See* CCFF 2261-2269 (Complaint Counsel's findings which support the conclusion that blowing fuses to set burst length was a viable alternative)).

924. To the contrary, the evidence in the record shows that setting burst length with fuses was not a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs because multiple parts with different burst lengths would have been required, leading to higher costs and logistical difficulties for DRAM manufacturers and users.

Response to Finding No. 924: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding ignores the substantial evidence in the record that indicates that the manufacturing cost of using fuses to program burst length was relatively similar to the manufacturing cost of using a mode register to program burst length. (Kellogg, Tr. 5132; *see also* CCFF 2236). Before 1996, it was potentially cheaper to design, produce, and test the use of fuses to determine burst length than the use of a mode register to program burst length. (Jacob, Tr. 5404-05).

925. Professor McAfee did not testify that this alternative was commercially viable. (McAfee, Tr. 7372).

Response to Finding No. 925: This proposed finding is misleading because it is also true that Professor McAfee did not testify that this alternative was not commercially viable. (McAffee, Tr. 7372 ("I didn't conclude it not to be commercially viable, but I did not reach a determination for using fuses to set burst length.")).

Indeed, the fact that JEDEC considered the use of fuses in 1991 and 1992 would seem to indicate that it is a commercially viable alternative to the use of mode register to program burst length. (McAfee, Tr. 7332-33; *see* DX-176 (serious consideration at JEDEC indicates that a technology is commercial viable)). JEDEC considered the use of fuses to set burst length in December 1991 and May 1992. (*See* CCFF 2265-2266).

Furthermore, Dr. Rapp did not provide testimony that this alternative was not commercially viable. (Rapp, Tr. 9810-11; *see* DX0306). For a more complete discussion of the evidence in support of its commercial viability, refer to CCFF 2261-2269).

926. Once the fuse is blown, the DRAM becomes a fixed burst length part under this alternative. (Jacob, Tr. 5404; Soderman, Tr. 9370). As with fixing the CAS latency, having multiple fixed burst length parts would lead to logistical difficulties exacerbated by the fact that the fuse could not be blown by OEMs. (Soderman, Tr. 9370-71; Kellogg, Tr. 5142).

Response to Finding No. 926: This proposed finding is misleading. Mr. Kellogg did not testify that OEMs could not blow fuses to set burst length. (Kellogg, Tr. 5142). Furthermore, this proposed finding fails to note that OEMs already test DRAMs. (Bechtelsheim, Tr. 5835-38). There is nothing in the record to indicate that OEMs could not also test the CAS latency function when they test DRAMs.

This proposed finding is incomplete because it omits the fact that the logistical issues associated with fixing CAS latency by blowing fuses before packaging could have been overcome by the use of a slightly more sophisticated memory controller that could detect when incompatible DIMMs are placed in the same system. (Jacob, Tr. 5382-83). Or, more sophisticated labeling of DIMMs. (*Id.*). The logistical difficulties associated with fixed burst length by blowing fuses could similarly have been overcome.

Furthermore, the logistical issues would not arise if OEMs were to blow the fuses to set CAS latency. (CCFF 2170). Similarly, the logistical issues associated with blowing fuses to set burst length would not arise if OEMs were to blow the fuses.

This proposed finding also ignores the advantages associated with fixed burst length parts. (Jacob, Tr. 5404-05 (cheaper); Kellogg, Tr. 5131, 5141-42 (the use of fuses to set burst length would allow one part to serve a variety of applications)).

927. Setting burst length with fuses would have resulted in increased costs.

Response to Finding No. 927: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel

submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding ignores the substantial evidence in the record that indicates that the manufacturing cost of using fuses to program burst length was relatively similar to the manufacturing cost of using a mode register to program burst length. (Kellogg, Tr. 5132; *see also* CCFF 2236). Before 1996, it was potentially cheaper to design, produce, and test the use of fuses to determine burst length than the use of a mode register to program burst length. (Jacob, Tr. 5404-05).

928. There would have been an increase in design costs due to the design effort to provide the fuses required. (Geilhufe, Tr. 9575, 9584-85).

Response to Finding No. 928: Mr. Geilhufe assumes that using fuses to set burst length is equivalent to use of fixed burst length. This assumption is contradicted by the weight of the evidence. *See* CCRF 922-927. The proposed finding is unreliable because it ignores the evidence in the record that indicates that the designs costs associated with the use of fuses to set burst length would have been lower than the design costs associated with the use of a mode register to program burst length. (CCFF 2263).

929. There would have been increased inventory and qualification costs of the same magnitude as the corresponding costs for the fixed burst length alternative because, once the fuse is blown, the part would be a fixed burst length part. (Geilhufe, Tr. 9585-89).

Response to Finding No. 929: Mr. Geilhufe assumes that using fuses to set burst length is equivalent to use of fixed burst length. This assumption is contradicted by the weight of the evidence. *See* CCRF 922-927. This proposed finding is incomplete because the weight of the evidence indicates that the costs associated with the use of fuses to set burst length were relatively similar to the costs associated with the use of a mode register to program burst length. (Kellogg, Tr. 5132; *see also* CCFF 2236, 2267-2268).

930. Setting burst length by blowing fuses would have resulted in the following approximate net costs compared to SDRAM in the mid-1990s, assuming a first-tier DRAM manufacturer using existing laser fuse technology and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: $100,000 increase in product design costs per latency; three cents per unit increase in inventory costs; and $250,000 increase in qualification costs per latency. (Geilhufe, Tr. 9562-64, 9596-98).

Response to Finding No. 930: This proposed finding is unreliable and irrelevant because it is based upon Mr. Geilhufe's methodology, which is unreliable and irrelevant for the reasons set forth in CCRF 837. As previously set forth , Mr. Geilhufe's assumption that the volume production level for a first tier manufacture is 20 million units is contrary to the weight of the evidence. The record evidence suggests that the volume production level for a particular part is between 500 million and 1 billion units. (Lee, Tr. 10997). The volume production for Micron's 64 meg SDRAM was approximately 900 million units. (*Id.* 10998). The volume production for Micron's 128 meg SDRAM was approximately 900 million units. (*Id.*).

Even if Mr. Geilhufe's estimate of fixed costs were correct, if allocated over 900 million units, the per unit cost would be much lower than 2 cents, but rather would be a tiny fraction of a cent.

Furthermore, the statement about added inventory costs, which Mr. Geilhufe characterized as a variable cost (Geilhufe, Tr. 9571), is contracted by the weight of the evidence. (*See* CCRF 926). The weight of the evidence in the record indicates that the increase in inventory costs per unit would have been less than 3 cents. (*Id.*).

931. The net increase in variable costs for the alternative of setting burst length by blowing fuses is, therefore, approximately 3 cents per unit. The total cost increase is approximately 5 cents per unit calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9598).

Response to Finding No. 931: Mr. Geilhufe's cost estimates are inaccurate because his methodology failed to account for certain cost savings. Furthermore, the per unit fixed

cost estimates, product design are qualification costs, are unreliable because they are based on an inaccurate assumption that volume production for a first-tier manufacturer like Samsung, Infineon, or Micron, was approximately 20 million units for a product that was well into its life cycle. (Geilhufe, Tr. 9562, 9726). Neither Mr. Geilhufe nor Rambus provided any record evidence to support this assumption. Mr. Geilhufe reviewed no evidence related to the cost to DRAM manufacturers for final test and good unit yield for the relevant period, other than the Peisl deposition, and some "confidential" evidence that is not in the record. (Geilhufe, Tr. 9706). He failed to interview anybody who attended JEDEC meetings during the relevant time period. (Geilhufe, Tr. 9623). Furthermore, Mr. Geilhufe did not do anything to ensure that the analysis that he did was the type of analysis that was done at JEDEC. (Geilhufe, Tr. 9622).

The record evidence suggests that the volume production level for a particular part is between 500 million and 1 billion units. The volume production for Micron's 64 meg SDRAM, including shrinks, was approximately 900 million units. (Lee, Tr. 10997). The volume production for Micron's 128 meg SDRAM part was also approximately 900 million units. (*Id.* 10998). The 256 meg SDRAM, which started it's life cycle in 2000, has already reached a volume production level of approximately 400 million units. (*Id.*). Even if Mr. Geilhufe's estimates of fixed costs were correct, if allocated over 900 million units, the per unit cost would be much lower than 2 cents, but rather would be a tiny fraction of a cent.

Furthermore, the statement about added inventory costs, which Mr. Geilhufe characterized as a variable cost (Geilhufe, Tr. 9571), is contracted by the weight of the evidence. (*See* CCRF 926). The weight of the evidence in the record indicates that the increase in inventory costs per unit would have been less than 3 cents. (*Id.*).

932. If the DRAM manufacturer did not have antifuse or electrically blown fuse technology available and wished to use that technology, adding it to the manufacturing process

would entail several million dollars in development costs in addition to the costs above. (Geilhufe, Tr. 9583-84).

Response to Finding No. 932: This proposed finding is misleading because the weight of the evidence indicates that the use of antifuses and/or electrical fuse technology is widespread among DRAM manufacturers. (CCFF 2159, 2172-2177).

(3) Using Dedicated Pins to Identify Burst Length Was Not a Viable Alternative.

933. Professor Jacob's proposed alternative of using an existing or a new, dedicated pin to identify burst length is similar to his corresponding proposed alternative for using pins to identify CAS latency. (Jacob, Tr. 5405).

Response to Finding No. 933: Complaint Counsel offers no specific response to RPF 933.

934. Complaint Counsel did not meet their burden of showing that using dedicated pins on the DRAM to identify burst length was a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs.

Response to Finding No. 934: This proposed finding lacks any reference to the record. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs. Furthermore, RPF 934 ignores the weight of the evidence in the record which indicates that the use of a dedicated pin to set burst length was a viable alternative. (CCFF 2270-2295).

935. To the contrary, the evidence in the record shows that using dedicated pins on the DRAM to identify burst length was not a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs, because it would be significantly costlier. Moreover, using dedicated pins to identify burst length is not an "alternative" at all because it is covered by Rambus's patents.

Response to Finding No. 935: The statement in RPF 935 lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs.

The weight of the evidence indicates that the cost of the use of a dedicate pin to set burst length would have been relatively similar to programmable burst length. (Kellogg, Tr. 5132). It also indicates that using a pin to set burst length would not violate Rambus patents because implementing this alternative would not require a register. (Jacob, Tr. 5406; CCFF 2281-2286). Neither Dr. Soderman or Mr. Geilhufe provided expert testimony that this alternative would infringe Rambus patents. (Soderman, Tr. 9371-73 (Soderman's testimony on use of a pin to set burst length does not identify infringement as a concern); Geilhufe, Tr. 9599-9600 (Geilhufe's testimony on use of a pin to set burst length does not identify infringement as a concern)). Lastly, Respondent did not present any secondary evidence that Rambus believed it could cover the concept of interleaving on-chip banks or that Rambus was trying to broaden its patents to capture that concept.

936. As with the use of pins to set CAS latency, this alternative would lead to additional costs associated with adding pins to the DRAM, wiring to the module and the motherboard, and adding pins to the controller. (Soderman, Tr. 9371).

Response to Finding No. 936: The statement that this alternative would lead to additional costs associated with adding pins to the DRAM is inaccurate because the weight of the evidence indicates that this alternative would not have required adding new pins. (CCFF 2277). JEDEC could have used a no-connect pin to implement this alternative. (CCFF 2276-2278). JEDEC could have asserted a super-voltage level on a pin to define the burst length of a part. (CCFF 2280). JEDEC could have multiplexed a column address pin to implement this alternative. (CCFF 2279).

937. When asked about the advantages of using pins to set burst length, Gordon Kelley of IBM responded:

> "I can't think of a lot of advantages compared to the programmable feature, which did not require a pin. I can think of the disadvantage that having a pin or using up a pin to do burst length selection was not a thing that we did easily, because once you use that pin up for a

> function, you don't have it available to you in the future for generation advance. As the memory densities increase, we need pins for more addressing of more address locations and those pins are very valuable for that feature, so this would have limited the number of generations of DRAM design that we could have used if we were to use up this pin."

(Kelley, Tr. 2552-53).

Response to Finding No. 937: The first sentence in this proposed finding is misleading because Mr. Kelley's testimony is more limited in its potential application than it suggests. Mr. Kelley provided testimony on the use of a pin to "address which burst length you wanted to choose." (G. Kelley, Tr. 2551). He did not provide testimony on the use of no-connect pins to set CAS latency. (*Id.* 2552-53). Mr. Kelley's testimony appears to be limited to assessing the merits of adding an address pin to identify the burst length or CAS latency of a part. (*Id.* 2551-53). Based on his testimony, it appears that JEDEC would have had to weigh the value of adding an address pin in order to implement a new function against the need to add new address pins in order to support future densities. (*Id.*).

The statement in RPF 875 is incomplete because it fails to take into account the different opinions within the industry. With respect to the JEDEC standard-setting process, most members almost always have a difference of opinion (Rhoden, Tr. 415). Mark Kellogg, of the same company as Gordon Kelley, testified that use of a dedicated pin provided the same advantage of flexibility as programmable CAS latency without the need for circuitry on the DRAM (CCFF 2188). In the case of systems manufacturers, Andy Bechtelsheim, co-founder of Sun, testified that from a systems perspective he would have preferred the use of pins to set CAS latency. (CCFF 2187).

938. This "alternative" is not really an alternative at all since it is covered by the same Rambus patents that cover SDRAMs and DDR SDRAMs. For example, this alternative would be covered by claim 1 of U.S. Patent 6,324,120, assigned to Rambus, which claims:

> "A method of operation of a synchronous memory device, wherein the memory device includes an array of memory cells, the method of operation comprises:
> receiving an external clock signal;
> receiving block size information, wherein the block size information defines an amount of data to be output by the memory device in response to a first operation code;
> sampling the first operation code synchronously with respect to the external clock signal wherein the first operation code instructs the memory device to perform a read operation; and
> outputting the amount of data in response to the first operation code."

(RX 2099-52 at 31-32; Soderman, Tr. 9371-72).

Response to Finding No. 938: This proposed finding is unreliable. The only evidence in the record to suggest that this alternative would have been covered by claim 1 of Rambus's 120 patent was from Dr. Soderman. (Soderman, Tr. 9371, 9373-74).

A determination that a patent claim covers a product is a two step process. The first step requires that the court interpret the patent claim as it would be understood by a person of ordinary skill in the art as a question of law. (Fliesler, Tr. 8778). Dr. Soderman did not consult technical dictionaries, treatises or textbooks, or the expert reports in the private litigation to determine the ordinary meaning in the industry of the terms used in the 120 patent. (Soderman, Tr. 9456-57; CCFF 2302).

The second step requires a factual determination that each element of the properly interpretted claim is present in the product. (Nusbaum, Tr. 1565-66). Dr. Soderman failed to present a proper claims analysis demonstrating that every element of the claim would be satisfied. (Soderman, Tr. 9456-57). He did not testify that using dedicated pins to set burst length satisfied every element in claim 1 of Rambus's '120 patent. Furthermore, Dr. Soderman interpreted "operation code," which is one of the terms in claim 1, in a way that would appear to limit claim 1 of the 120 patent to Rambus's packetized system. (Soderman, Tr. 9456-57).

939. A claim covers a device if each and every claim element or "limitation" is found in that device. (Nusbaum, Tr. 1565-66). SDRAMs are synchronous memory devices that contain an array of memory cells. (Rhoden, Tr. 359-60, 369-70). Moreover, the claim's reference to "receiving block size information" includes receiving burst length information using a pin. (Soderman, Tr. 9372-73). Thus, each and every element of claim 1 of the '120 patent would be found in SDRAMs that implemented the use of dedicated pins to identify burst length.

Response to Finding No. 939: The last statement in this proposed finding is a legal conclusion, which lacks any citation to the record and is therefore inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Dr. Soderman did not do anything approaching a claims analysis that could support the last sentence, and any testimony that he did give that indicated that using a pin to set burst length would infringe the '120 patent is unreliable at best for the reasons set forth in CCRF 938.

Furthermore, this proposed finding is misleading to the extent that it suggests that Mr. Nusbaum and Mr. Rhoden provided testimony interpreting the '120 patent. They did not provide any testimony interpreting that patent.

940. Programming burst length by using dedicated pins would have resulted in the following approximate net costs compared to SDRAM in the mid-1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: 2 cents in increased packaging costs per unit due to an additional two pins. (Geilhufe, Tr. 9562-64, 9599). This 2-cent increase is a variable cost.

Response to Finding No. 940: This proposed finding is unreliable because the methodology that Mr. Geilhufe used to analyze the costs of alternative technologies is based on inaccurate assumptions, not the appropriate methodology to rely on to determine the viability of alternative technologies in this case, and more generally unreliable for the reasons set forth in CCRF 837, 853, and 854.

Furthermore, this proposed finding arrives at a two cent increase in packaging costs per unit by assuming that it would have been necessary to add two pins to implement this alternative. That assumption is invalid for the reasons set forth in CCRF 936. At most, JEDEC would have needed to support two different burst lengths. (CCFF 2289-2291). JEDEC could have used an existing no-connect pin to support two different burst lengths. (CCFF 2280; Soderman, Tr. 9463 (one pin can support two different options)).

941. Although SDRAMs use three bits to program burst length, the cost calculation above involves the addition of only two pins based on the assumption that if pins were being used to set burst length, they would also be used to set CAS latency. (Geilhufe, Tr. 9599). Because pins have to be added in even increments, four pins were added to program CAS latency although only three were required. That extra pin, plus two additional pins, are sufficient to set burst length. (Id). If burst length were being set using pins, but not CAS latency, then an additional four pins would be required to achieve the same degree of flexibility as provided in the SDRAM standard. (Geilhufe, Tr. 9599-9600).

Response to Finding No. 941: This proposed finding is unreliable because it assumes that it would have been necessary to add pins to the package in order to implement this alternative. This assumption is not supported by the weight of the evidence, which indicates that it would not have been necessary to add pins to implement this alternative for both CAS latency and burst length.

Counting the vref pin, forty-four out of forty-seven pinouts for SDRAMs and DDR SDRAMs have two or more no-connect pins available. (CCFF 2196). It would not have been necessary to add pins to set CAS latency. (CCRF 880). Instead, JEDEC could have used an existing no-connect pin to set CAS latency. (*Id.*). Neither would it have been necessary to add pins to set burst length for the reasons set forth in CCRF 940. Instead, the weight of the evidence indicates that JEDEC could have used an existing no-connect pin to set burst length. (*Id.*).

Even if JEDEC decided to add pins to set burst length and CAS latency, at most it would have had to add two pins. A predominant share of the market is served by two different CAS

latencies (CCFF 2214-2218), which requires only one pin to implement (CCFF 2213), and two different burst lengths (CCFF 2289-2291), which also would require only one pin to implement (CCFF 2213). Furthermore, the pins required to implement this alternative would have been less expensive than data pins (CCFF 2202, 2205) and could have eliminated the need for a register entirely assuming that burst type was also set via pins (CCFF 2207, 2286).

942. As in the case of using dedicated pins for CAS latency, the estimated two cent increase cost for this alternative is very conservative. (Geilhufe, Tr. 9599).

Response to Finding No. 942: The statement is inaccurate and unreliable for the reasons set forth in CCRF 941.

(4) Explicitly Identifying Burst Length in the Read Command Was Not a Viable Alternative.

943. Professor Jacob's proposed alternative of identifying burst length in the read command is similar to his corresponding proposed alternative for identify CAS latency in the read command. (Jacob, Tr. 5407).

Response to Finding No. 943: Complaint Counsel has no specific response to this proposed finding.

944. Complaint Counsel did not meet their burden of showing that identifying burst length in the read command was a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs.

Response to Finding No. 944: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (*See* CCFF 2296-2305 (Complaint Counsel's findings which support the conclusion that identifying burst length in the command was a viable alternative)).

945. To the contrary, the evidence in the record shows that, as with the alternative of using dedicated pins to identify burst length, this is not really an alternative because it would be covered by the same Rambus patents that read on SDRAMs and DDR SDRAMs.

Response to Finding No. 945: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

946. For example, claim 1 of the '120 patent, reproduced above, would cover this alternative because it covers "receiving block size information" including when the block size (equivalently, burst length) information is embedded in a read command. (RX 2099-52 at 31-32; Soderman, Tr. 9373-74).

Response to Finding No. 946: This proposed finding is unreliable. The only evidence in the record to suggest that this alternative would have been covered by claim 1 of Rambus's 120 patent was from Dr. Soderman. (Soderman, Tr. 9371, 9373-74).

A determination that a patent claim covers a product is a two step process. The first step requires that the court interpret the patent claim as it would be understood by a person of ordinary skill in the art as a question of law. (Fliesler, Tr. 8778). Dr. Soderman did not consult technical dictionaries, treatises or textbooks, or the expert reports in the private litigation to determine the ordinary meaning in the industry of the terms used in the 120 patent. (Soderman, Tr. 9456-57).

The second step requires a factual determination that each element of the properly interpretted claim is present in the product. (Nusbaum, Tr. 1565-66). Dr. Soderman failed to present a proper claims analysis demonstrating that every element of the claim would be satisfied. (Soderman, Tr. 9456-57). He did not testify that identifying burst length with the command satisfied every element in claim 1 of Rambus's '120 patent. Furthermore, Dr. Soderman interpreted "operation code," which is one of the terms in claim 1, in a way that would appear to limit claim 1 of the 120 patent to Rambus's packetized system. (Soderman, Tr. 9456-57).

(5) Using a Burst Terminate Command Was Not a Viable Alternative.

947. Professor Jacob's proposed alternative of using a burst terminate command rather than programming burst length through the mode register would involve defining all parts to have a fixed, long burst length and then sending a command to terminate the burst if a shorter burst length were desired. (Jacob, Tr. 5409).

Response to Finding No. 947: Complaint Counsel has no specific response to this proposed finding.

948. Complaint Counsel did not meet their burden of showing that using a burst terminate command was a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs.

Response to Finding No. 948: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (*See* CCFF 2306-2318 (Complaint Counsel's findings which support the conclusion that using a burst terminate command was a viable alternative)).

949. To the contrary, the evidence in the record shows that using a burst terminate command was not a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs, because it would result in significantly lower performance.

Response to Finding No. 949: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (*See* CCFF 2311-2312, 2318).

950. A burst terminate command is an optional feature in SDRAMs. (CX 234 at 161). The burst terminate command is required in DDR SDRAMs, but can be used only to terminate

"read" bursts, not "write" bursts. (CX 234 at 174). Although DDR SDRAMs have this burst terminate command available, DDR SDRAMs program burst length in the mode register. (CX 234 at 150).

Response to Finding No. 950: There is no evidence in the record to support the relevance of the fact that the burst terminate command, in DDR SDRAMs, cannot terminate "write" bursts. Furthermore, this proposed finding is misleading to the extent that it suggests that it is not technologically possible to use the burst terminate command to terminate a write burst. The evidence cited only supports the proposition that JEDEC did not define a burst terminate command to interrupt a write burst. (CX0234 at 174). There is evidence in the record to support the proposition that JEDEC could have defined a burst terminate command to interrupt a write burst. (CX0234 at 165 (Release 9 of Standard 21-C provides for interrupted write bursts in DDR SDRAM); RX-2099-39 at 69 (Samsung's DDR II SDRAM specifications provides for interrupted write bursts)).

In addition, the fact that DDR SDRAMs use the mode register to program burst length does not mean that, had Rambus disclosed the scope of its patent applications while JEDEC was still working on the DDR SDRAM standard, it would not have considered the use of the burst terminate command to be a viable alternative.

JEDEC included a modified version of the burst terminate command in the DDR II standard as a way to terminate a burst length of eight in order to effect a burst length of four. (CCFF 2318). Using burst terminate command to effect a burst length of 4 and 8 would have served the interests of the predominant share of the market. (CCFF 2254, 2315-2318).

951. A burst length of one would not have been possible with a burst terminate command because when a read command is issued it takes one cycle to execute before a burst terminate command could be encountered and, but that point, there are already two bits of data coming out. (Geilhufe, Tr. 9598-99).

Response to Finding No. 951: This proposed finding is relevant only if one assumes that it would have been necessary to use an alternative technology that could support a burst length of 1 option. The weight of the evidence does not support that assumption. Instead, it indicates that a burst length of 1 is rarely used in the industry. (CCFF 2315-2318).

952. Professor Jacob's proposed alternative of using a burst terminate command would lead to inefficiencies on the bus. (Jacob, Tr. 5411. For example, terminating a read burst when the next command is a write leads to inefficient bus utilization because data already in the pipeline to be read out must be cleared before data can be written to the DRAM. (Soderman, Tr. 9374-76). Moreover, when the burst terminate command was on the bus, the controller would not be able to send a command to another bank. (Jacob, Tr. 11126).

Response to Finding No. 952: Dr. Soderman testified that the burst terminate command causes a wasted cycle when a write interrupts a read. (Soderman, Tr. 9374-75). This proposed finding is misleading because it omits the fact that using a burst terminate command would not have led to significant inefficiencies on the bus. (Jacob, Tr. 11109-10 (testifying that the wasted cycle caused when a write interrupts a read is not a significant problem, because SDRAMs and DDR SDRAMS are already designed to handle wasted cycles); CCFF 2311-2312).

953. In fact, according to a study performed by Professor Jacob and a graduate student, this alternative could lead to a 10-15 percent decrease in the efficiency of the system. (Jacob, Tr. 5604-06).

Response to Finding No. 953: This proposed finding is incomplete because it omits the fact that Dr. Jacob testified that he could not recall exactly what the results of the statistical study were, but that the overhead "was 10-15 percent, or less." (Jacob, Tr. 5606). Furthermore, the proposed finding omits the fact that Dr. Jacob considered that the results of his statistical study indicated that there would not have been a significant amount of overhead associated with the burst terminate command. (*Id.* 5605).

954. JEDEC participants considered "burst terminate" an "internal device timing nightmare." (CX 415 at 10).

Response to Finding No. 954: This proposed finding is incomplete and unreliable because it fails to account for the fact that JEDEC made improvements to the burst terminate command as it had been adopted for DDR SDRAM. For DDR II SDRAM, JEDEC decided to modify the burst terminate command in a way that made it more reliable and easier to implement than before. (CCFF 2318).

955. Steve Polzin of AMD testified that use of a burst terminate command would interfere with pipelining and make the system less efficient overall. (Polzin, Tr. 4038-40).

Response to Finding No. 955: This proposed finding is unreliable because Mr. Polzin lacks sufficient foundation to testify about the intricacies of the burst terminate command. (Polizin, Tr. 4037-38 (In response to a question about the difficulty of engineering a burst terminate command at high data rates, Mr. Polzin stated, "[T]his is referring to the details of a DRAM design of which I'm not expert in.")). Furthermore, Mr. Polzin is not a DRAM manufacturer. Mr. Polzin is a chief platform architect at AMD, a chipset company. (Polzin, Tr. 3932-33).

In addition, this proposed finding is misleading because it fails to appropriately qualify Mr. Polzin's testimony in way that accurately reflects what he sa*id.* Mr. Polzin merely testified that a burst terminate command could be implemented in such a way that would "waste bandwidth." (Polzin, Tr. 4038-40). Because it is not clear whether Mr. Polzin knows enough about how JEDEC ultimately implemented the burst terminate command, Mr. Polzin's testimony about burst terminate is speculative at best.

956. The JEDEC Future DRAM Task Group considered eliminating the burst terminate command, also known as "burst interrupt," from DDR2 because at "high data rates burst interrupt commands are of less value, and are more difficult to engineer." (CX 392 at 5). The Task Group also noted that elimination of burst terminate would "reduce[] test costs" and "increase[] yield due to elimination of speed critical path." (RX 2234 at 10).

Response to Finding No. 956: This proposed finding is incomplete because it fails to account for the fact that JEDEC ultimately decided to include a burst terminate command for DDR II SDRAM. (CCFF 2318).

The last statement in this finding, which relies on one document without any supporting testimony, does not support a conclusion that there are significant costs associated with the burst terminate command. It ignores the weight of the evidence in the record that indicates that the costs associated with relying on the burst terminate command to set burst length would have been relatively similar, if not lower, than the costs associated with using a mode register to program burst length. (Kellogg, Tr. 5132; Jacob, Tr. 5411-12 (Dr. Jacob testified that the burst terminate command could have potentially made the part simpler to design, test, and manufacture.)).

957. Although JEDEC retained some form of burst terminate in DDR2 SDRAM, the timing difficulties led JEDEC to limit its use. (Soderman, Tr. 9376-77). As Joe Macri, chairman of the JEDEC Future DRAM Task Group focusing on DDR2, testified:

(Macri, Tr. at 4774, **in camera**). Thus, in the DDR2 standard, burst terminate can be used only to truncate a burst of eight to four, and it can be used only when reads are followed by reads or writes are followed by writes, not when a read is followed by a write or a write is followed by a read. (RX 2099-39 at 63; Soderman, Tr. 9376-77). Despite including this limited form of a burst terminate command in the DDR2 standard, JEDEC also included the programmable burst length feature. (RX 2099-39 at 20).

Response to Finding No. 957: The statement in this proposed finding that the burst terminate in the DDR II standard can only be used to truncate a burst of eight to four does not support the conclusion that burst terminate is not a viable alternative because the predominant

share of the market would have been served by an option to use either a burst length of four or eight. (CCFF 2313-2317). Burst lengths of 1 and 2 are used infrequently, if at all, in the DRAM market. (Lee, Tr. 11014).

The statement in this finding that a burst terminate command can only be used when reads are followed by reads or when writes are followed by writes is not supported by the weight of the evidence. Dr. Soderman testified that using a write to interrupt a read would cause a wasted cycle. (Soderman, Tr. 9376-77). He did not also testify that a write could not interrupt a read. (*Id.*). Dr. Jacob testified the the wasted cycle caused when a write interrupts a read is not a significant problem, because SDRAMs and DDR SDRAMS are already designed to handle wasted cycles. (Jacob, Tr. 11109-10; CCFF 2311-2312)).

In addition, the last statement in this proposed finding that DDR SDRAMs use the mode register to program burst length does not mean that, had Rambus disclosed the scope of its patent applications while JEDEC was still working on the DDR SDRAM standard, it would not have considered the use of the burst terminate command to be a viable alternative.

(6) Using CAS Pulse to Control Data Output Was Not a Viable Alternative.

958. Professor Jacob's proposed alternative of using a CAS pulse to control data output involves toggling the CAS line to the DRAM once for each bit of data desired – thus, if a burst of four were required, the CAS line would be toggled four times. (Jacob, Tr. 5411-12).

Response to Finding No. 958: Complaint Counsel has no specific response to this finding.

959. Complaint Counsel did not meet their burden of showing that using a CAS pulse to control data output was a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs.

Response to Finding No. 959: The statement in RPF 959 lacks any reference to the record. Complaint Counsel submits that this finding should be disregarded pursuant to

Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs. Furthermore, the statement that CAS pulse to control data output was not a viable alternative is contrary to the weight of the evidence that suggests this alternative would have been less costly and simpler to implement and test. (CCFF 2321).

960. To the contrary, the evidence in the record shows that using a CAS pulse to control data output was not a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs, because it would lead to cost, testing and performance problems.

Response to Finding No. 960: The statement in RPF 960 lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs. Furthermore, the statement that this alternative would lead to cost, testing, and performance problems is contrary to the weight of the evidence. Using a CAS pulse to control data output, instead of programming it in the mode register, is simpler to design. (Jacob, Tr. 5412 ("You would have eliminated the mode register and the circuitry required to initialize it, which would make the part simpler, smaller, easier to test")).

961. Professor McAfee did not testify that this was a commercially viable alternative.

Response to Finding No. 961: This proposed finding is misleading because it is also true that Professor McAfee did not testify that this alternative was not commercially viable. RPF 961 cites to no supporting record evidence that Professor McAfee does not believe this alternative to be commercially viable.

962. This alternative would not work as Professor Jacob described it because it is not clear how the DRAM would be able to determine whether a signal on the CAS line were intended to be a "toggle" that was part of a burst of data or a new command. (Soderman, Tr. 9378-79). Sophisticated additional circuitry would have to be added to allow the DRAM to recognize the toggling of the CAS line, and that would add cost and create testing problems. (Soderman, Tr. 9379).

Response to Finding No. 962: The statement in RPF 962 that the alternative would not work is unreliable. Dr. Soderman's testimony that this alternative would add cost and create testing problems is contrary to evidence that suggests that the alternative would actually simplify the technology. Assuming that determining CAS latency and burst type did not require a mode register, using the CAS pulse to determine the burst length would have eliminated the mode register and the complicated circuitry required to initialize the register. (Jacob, Tr. 5412).

963. In addition, this alternative would not allow efficient interleaving between banks without adding more CAS lines. (Soderman, Tr. 9379-80). Currently, while one bank of an SDRAM is reading out data, the CAS line can be used to send a command to a second bank, a process known as interleaving. Under the proposed CAS pulse alternative, the CAS line would be toggling in connection with the burst and additional CAS lines would have to be added to the other banks to enable this sort of operation. (*Id.*). Because there are four banks on each DRAM, three CAS lines would have to be added requiring additional pins on the DRAM and the controller, as well as additional circuitry on the DIMMs and the motherboard. (Soderman, Tr. 9380).

Response to Finding No. 963: The statement in RPF 963, that additional pins and circuitry would have to be added to this alternative is unreliable. It fails to take into account the advantages of this particular proposal. As mentioned in the previous response, this alternative could eliminate the need for a mode register and the complicated circuitry associated with it (Jacob, Tr. 5412).

c. There Is Evidence That Some Of Complaint Counsel's Proposed Alternatives To Programmable CAS Latency and Programmable Burst Length Would Infringe Rambus Patents.

964. Rambus has come forward with a number of patents that it contends cover certain of the alternatives to programmable CAS latency and programmable burst length proposed by Complaint Counsel through their technical expert, Professor Jacob. In particular, as set forth above, there is evidence to support Rambus's contention that the alternatives of scaling CAS latency with clock frequency and identifying CAS latency in the read command are covered by Rambus's '263 patent. *See* Findings ¶¶ 862-864, 886-890. The latter alternative also may be covered by Samsung's '956 patent. *See* Findings ¶ 892.

Response to Finding No. 964: The statement in this proposed finding that Rambus has come forward with "a number of patents" that cover certain alternatives to programmable CAS

latency and programmable burst length is inaccurate. Rambus came forward with only two patents, the '263 patent and the '956 patent, that it contends cover scaling CAS latency with clock frequency and/or identifying CAS latency in the read command. Rambus cannot, and has not, further proposed findings that these two patents relate to any of the additional proposed CAS latency alternatives or any of the proposed burst length alternatives based on evidence in the record. (*See generally* RPF 810-855, 868-883, 893-902, 903-963).

Each statement in this proposed finding is unreliable because the evidence in the record to support Rambus's proposed finding that the '263 patent and '956 patent relate to scaling CAS latency with clock frequency and/or identifying CAS latency in the command is either non-existent or inadequate.

The only evidence to support the relevance of the '263 patent to scaling CAS latency with clock frequency to scaling the CAS latency with clock frequency and identifying CAS latency in the read command is the ambiguous testimony from Dr. Soderman that these proposed alternative required something like a register. (Soderman, Tr. 9359 (scaling CAS latency with clock frequency requires "some sort of a register"), 9365 (identifying CAS latency in the read command would require "a register similar to a mode register")). Dr. Soderman did not identify the '263 patent during his testimony on either of these two proposed alternatives to programmable CAS latency. (*Id.*). Nor did he identify which claim(s) in the '263 patent covered either of these alternatives. (*Id.*). Nor did he analyze whether or not certain elements of claims within the '263 patent would limit the claims to the RDRAM architecture. (*Id.*). What remains, then, to support a proposed finding that the '263 patent is relevant to this case is Rambus's unsubstantiated, self-serving, interpretation of the patent.

There is no evidence in the record to support that Samsung's '956 patent covers identifying CAS latency in the read command. (*See* CCRF 892). Dr. Soderman did not provide any expert

testimony on the 956 patent and neither did Mr. Geilhufe. (Soderman, Tr. 9364-65; Geilhufe, Tr. 9580-81). What remains, then, to support a proposed finding that the '956 patent is relevant is Rambus's unsubstantiated, self-serving, interpretation of the patent.

965. Likewise, there is evidence to support Rambus's contention that the proposed alternatives of using dedicated pins to set burst length and identifying burst length in the read command are covered by Rambus's '120 patent. *See* Findings ¶¶ 938-939, 945-946.

Response to Finding No. 965: This proposed finding is not supported by any reliable evidence for the reasons set forth in CCRF 938-939 and 945-46.

966. Professor Jacob did not consider any of the patents raised by Rambus in his analysis of proposed alternatives; indeed, Professor Jacob did no investigation at all as to whether his proposed alternatives were encumbered by patents. *See* Findings ¶¶ 793, 892.

Response to Finding No. 966: This proposed finding assumes that Professor Jacob failed to consider relevant patents. This assumption is contrary to the weight of the evidence in the record. The weight of the evidence in the record indicates that these patents are not relevant to this case. (CCRF 858, 862-864 (showing that evidence used to support a finding that scaling CAS latency with clock frequency infringes is unreliable); CCRF 886-888 (showing evidence used to support a finding that identifying CAS latency with the command infringes is unreliable); CCRF 938-939 (showing that evidence used to support a finding that using pins to set the burst length infringes is unreliable); CCRF 945-946 (showing that evidence used to support a finding that identifying burst length in the read command infringes is unreliable)).

967. Professor McAfee has testified that one of the alternatives proposed by Professor Jacob to dual-edge clocking, interleaving on-module ranks, would require royalty payments to Kentron. (McAfee, Tr. 7404). In considering whether the other alternatives proposed by Professor Jacob were commercially viable, he assumed that they were unencumbered by patents. (McAfee, Tr. 7582-84). Professor McAfee admitted that, if this assumption was incorrect and there were patents attached to alternatives that he had concluded were commercially viable, "it could be in principle upset my conclusion that they were commercially viable." (McAfee, Tr. 7584).

Response to Finding No. 967: The statement in this proposed finding and Dr McAfee's testimony that the interleaving on-module ranks alternative would require royalties to Kentron is incomplete because it omits his testimony that the latter alternative would still be commercially viable in comparison to the Rambus technology. (McAfee, Tr. 7404-05).

The statement in this proposed finding with respect to Dr. McAfee's assumption that the other alternatives proposed by Dr. Jacob were unencumbered by patents is incomplete because it omits the fact that the weight of the evidence supports the validity of that assumption. (CCRF 858, 862-864 (showing that evidence used to support a finding that scaling CAS latency with clock frequency infringes is unreliable); CCRF 886-888 (showing evidence used to support a finding that identifying CAS latency with the command infringes is unreliable); CCRF 938-939 (showing that evidence used to support a finding that using pins to set the burst length infringes is unreliable); CCRF 945-946 (showing that evidence used to support a finding that identifying burst length in the read command infringes is unreliable)).

968. Complaint Counsel has introduced no evidence that the patents raised by Rambus do not cover certain of the proposed alternatives. Even with his assumption of no patent coverage, Professor McAfee could not testify that the alternative of scaling CAS latency with clock frequency was commercially viable. As for Professor McAfee's opinions that identifying CAS latency in the read command, using dedicated pins to set burst length, and identifying burst length in the read command were each commercially viable, these opinions are based on the incorrect assumption that these alternatives are not encumbered by patents. It follows that Professor McAfee's opinions in this regard are entitled to no weight.

Response to Finding No. 968: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The second statement in this proposed finding, which states that Dr. McAfee could not testify that scaling CAS latency with clock frequency was commercially viable, is unreliable. It

fails to account for the fact that it is also true that Dr. McAfee did not testify that this alternative was not commercially viable. Furthermore, neither Dr. Rapp or Mr. Geilhufe provided testimony that this alternative was not commercially viable. (Rapp, Tr. 9810-11; Geilhufe, Tr. 9575-92 (discussion of CAS latency alternatives did not include scaling CAS latency with clock frequency)). For a more complete discussion of the evidence in support of its commercial viability, refer to CCFF 2178-2183.

The third sentence in this proposed finding, which refers to three different alternative technologies, is incomplete. It states that Dr. McAfee assumed that the alternatives were unencumbered by patents, but omits the fact that the weight of the evidence indicates that this was a valid assumption. (CCRF 858, 862-864 (showing that evidence used to support a finding that scaling CAS latency with clock frequency infringes is unreliable); CCRF 886-888 (showing evidence used to support a finding that identifying CAS latency with the command infringes is unreliable); CCRF 938-939 (showing that evidence used to support a finding that using pins to set the burst length infringes is unreliable); CCRF 945-946 (showing that evidence used to support a finding that identifying burst length in the read command infringes is unreliable)).

d. Given The Cost-Performance Differences, An Economically Rational DRAM Manufacturer Would Have Adopted And Licensed The Rambus Technologies Incorporated In SDRAM If It Had Known Of Rambus's Royalty Rates In Advance.

969. JEDEC-compliant SDRAM parts use two of the four Rambus technologies at issue: programmable CAS latency and programmable burst length. In order to determine whether the use of alternatives to the Rambus technologies used in SDRAM is more costly than paying the Rambus royalties, one can determine the additional variable costs associated with the alternatives and compare them to the Rambus royalties that would be paid under the a license from Rambus. (Rapp, Tr. 9830-33). Costs for alternatives to different features are additive; that is, to calculate the costs associated with implementing alternatives to more than one feature simultaneously, one would simply add the costs associated with the individual alternatives. (Geilhufe, Tr. 9614).

Response to Finding No. 969: The statement in RPF 969 that "[i]n order to determine whether the use of alternatives to the Rambus technologies used in SDRAM is more costly than paying the Rambus royalties, one can determine the additional variable costs associated with the alternatives and compare them to the Rambus royalties that would be paid under the a license from Rambus" is misleading and contrary to the weight of the evidence because it implies that each member of JEDEC is faced with the same costs to comply with the standard. However, JEDEC is composed of broad array of companies and individuals. (*See, e.g.*, CCRF 4). These companies represent a broad cross-section of the semiconductor supply chain from around the world and so would experience costs differently depending on where they are in the semiconductor supply chain. (CX0212-CX0213). Furthermore, the comparison of manufacturing costs and royalties is misleading because that comparison does not take into account the differences between the two types of costs. In particular, manufacturing costs are not subject to hold-up and royalties are. (McAfee, Tr. 11241-11243). Finally, there is no evidence in the record that JEDEC members conducted this type of analysis in making decisions regarding what technologies to put into the standards. Mr. Geilhufe did nothing to ensure that the analysis that he did was the type of analysis done at JEDEC. (CCFF 2121). Similarly, Dr. Rapp simply assumed that JEDEC would perform the same type of analysis that he d*id.* (CCFF 2825-2827).

Mr. Geilhufe's opinions regarding the costs of alternative technologies are not actual costs but estimated costs. (Geilhufe, Tr. 9665). As a result of the fact that Mr. Geilhufe was presenting estimates, all of the information presented in his testimony was approximate. (Geilhufe, Tr. 9665). Mr. Geilhufe agreed at trial that the margin of error for each of the cost elements described in his presentation is as high as 25 percent. (Geilhufe, Tr. 9665). Mr. Geilhufe did not compare his projections in this case to any actual results to see if the results actually were within 25 percent of actual cost. (Geilhufe, Tr. 9665-66 ("Well, since the vast majority of these never got implemented,

it was not possible to test them.")). Since many of the alternates Mr. Geilhufe evaluated never got implemented, it would be impossible for even a DRAM manufacturer to verify the costs of many of the alternatives. (Geilhufe, Tr. 9666). But to the extent that they were implemented in some fashion, one way to verify Mr. Geilhufe's cost estimates would be to ask a DRAM manufacturer. (Geilhufe, Tr. 9666). Mr. Geilhufe never attempted to verify the numbers he came up with the DRAM manufacturers. (Geilhufe, Tr. 9666-67). Mr. Geilhufe never asked Rambus to conduct discovery from DRAM manufacturers relating to his cost estimates. (Geilhufe, Tr. 9667). Because the costs that he estimated are based on his experience, he cannot say what the actual costs were for any of the DRAM manufacturers in the relevant time period. (Geilhufe, Tr. 9667 ("Clearly -- as I stated, cost information is highly confidential, and I cannot speak for the actual costs at a DRAM manufacturer. I can only speak for the model that I feel is a credible model that I used.")).

970. To make this comparison, the total additional cost of each alternative is divided by the weighted average of the selling price ("ASP") of SDRAM for the period 1996 to 2006. (Rapp, Tr. 9816-17, 9830-33). For SDRAM, the ASP is $4.87. (Rapp, Tr. 9816-17). This calculation shows the additional cost of the alternative as a percentage of selling price.

Response to Finding No. 970: Complaint Counsel does not disagree that RPF 970 describes the procedure used by Dr. Rapp. However, RPF 970 is misleading when it states that this procedure is capable of arriving at one "additional cost of the alternative as a percentage of selling price" for every member of JEDEC. (CCRF 969).

971. The Rambus royalty rate for the use of its technologies in SDRAM is 0.75%. (Rapp, Tr. 9832).

Response to Finding No. 971: Complaint Counsel does not disagree.

972. The alternatives for programmable CAS latency identified as "commercially viable" by Complaint Counsel's economic expert were: fixed CAS latency, explicitly identify latency in the read command, programming latency with fuses, and using multiple pins to set a latency value. (Rapp, Tr. 9810-11; McAfee, Tr. 7354-63).

Response to Finding No. 972: Complaint Counsel does not disagree. However, Complaint Counsel's technical expert identified an additional option, "scale CAS latency with clock frequency." (CCFF 2178-2183). Professor McAfee did not express an opinion on whether that alternative could constrain the price of using the mode register to set CAS latency because he saw no evidence that it was presented at JEDEC. (McAfee, Tr. 7363). However, Professor McAfee did not testify that the technology was not commercially viable.

973. The total additional incremental costs associated with the use of the fixed latency alternative is $0.04 per part. (Rapp, Tr. 9814). This total consists of the following additional incremental costs per part: a $0.01 wafer sort cost savings, a $0.03 good die yield cost increase, and a $0.02 inventory cost increase. (Rapp, Tr. 9814). As a percentage of ASP, this total additional incremental cost is 0.82%. (Rapp, Tr. 9817). (These numbers are illustrated in DX307.)

Response to Finding No. 973: RPF 973 is unreliable because it is based on cost determinations of Mr. Geilhufe that are themselves unreliable. (CCRF 969). Additionally, Mr. Geilhufe's cost estimates for both the inventory cost element and the good die yield cost element depend critically on his assumption that JEDEC would have specified the same number of CAS latencies in a fixed CAS latency standard as it currently has. (Geilhufe, Tr. 9702-9703, 9706-9707). Mr. Geilhufe agreed that if JEDEC were to specify only a single fixed latency rather than duplicating the current standard that these costs would be eliminated. (Geilhufe, Tr. 9578, 9701, 9709-9710). But Mr. Geilhufe did nothing to ensure that his assumption was appropriate. In making his assumption that the number of new part numbers that would be required for a fixed CAS latency and a fixed burst length should be derived from the JEDEC standard, Mr. Geilhufe never looked at the market today to see how many of those different types of parts are sold. (Geilhufe, Tr. 9707). Mr. Geilhufe never saw any evidence from JEDEC regarding how many different types of DRAMs would have been sold had there been a fixed CAS latency and a fixed burst length. (Geilhufe, Tr. 9707-9708). Mr. Geilhufe never read any testimony, either from deposition or at the Hearing, from a current industry participant regarding how many different

types of DRAMs would have been sold had there been a fixed CAS latency and a fixed burst length. (Geilhufe, Tr. 9708).

Had Mr. Geilhufe reviewed the record evidence he would have realized that the assumption that JEDEC would have retained the same number of CAS latencies if it had standardized a fixed CAS latency DRAM rather than a programmable CAS latency DRAM is contrary to the weight of the evidence. In particular, when a proposal for fixed CAS latency was actually made at JEDEC, the proposal often included only one CAS latency rather than a number of fixed latencies. (CCFF 2138-2139, 2142, 2152). In addition, had Mr. Geilhufe reviewed the record evidence he would have understood that the purpose of proposals that used fixed CAS latency was to reduce costs. (CCFF 2139, 2142).

If Mr. Geilhufe's assumption is incorrect and JEDEC would have standardized a single fixed latency DRAM then both the inventory cost and the good die yield cost elements would be zero, resulting in a projection that the fixed latency DRAM would in fact be $0.01 cheaper to manufacture than the current standard.

974. The total additional incremental costs associated with the use of the alternative of explicitly identifying latency in the read command is $0.01 per part, which is the additional incremental costs associated with packaging. (Rapp, Tr. 9814-15). As a percentage of ASP, this total additional incremental cost is 0.21%. (Rapp, Tr. 9817). (These numbers are illustrated in DX307.) As discussed above, this alternative is covered by Rambus's patents.

Response to Finding No. 974: RPF 974 is unreliable because it is based on cost determinations of Mr. Geilhufe that are themselves unreliable. (CCRF 969). Additionally, RPF 974 is unreliable because it is based on a misstatement of the opinion of Mr. Geilhufe. Mr. Geilhufe's opinion regarding the cost of this alternative is that there is no increase in the variable cost of manufacturing this DRAM unless the implementation requires an additional pin. The assumption that more pins would be required to implement the alternative of using two voltage levels via pin to set CAS latency and burst length was based solely on Mr. Geilhufe's reading of

Professor Jacob's report. (Geilhufe, Tr. 9722). Mr. Geilhufe did not do anything to ensure that it was the case that more pins would actually be required to implement the alternative of using two voltage levels via pin to set CAS latency and burst length. (Geilhufe, Tr. 9722). In fact, Mr. Geilhufe's own demonstrative describing these costs indicates his opinion that there would be a negligible cost change under the packaging element if no additional pin were required to implement this alternative. (DX0298). If no additional pin is required to implement this alternative then there are no additional variable costs to manufacture DRAMs corresponding to the alternative.

975. The total additional incremental cost associated with the use of the alternative of programming latency with fuses is $0.06 per part. (Rapp, Tr. 9815). This total consists of the following additional incremental costs per part: a $0.01 wafer sort cost increase, a $0.03 good die yield cost increase, and a $0.02 inventory cost increase. (Rapp, Tr. 9815). As a percentage of ASP, this total additional incremental cost is 1.23%. (Rapp, Tr. 9817-18). (These numbers are illustrated in DX307.)

Response to Finding No. 975: RPF 975 is unreliable because it is based on cost determinations of Mr. Geilhufe that are themselves unreliable. (CCRF 969). Additionally, Mr. Geilhufe's cost estimates for both the inventory cost element and the good die yield cost element depend critically on his assumption that the only type of fuses that could be used to implement this alternative are laser fuses that are burned before packaging, making the cost of the use of fuses identical to the cost of the use of fixed CAS latency DRAMs for the good die yield and inventory cost elements. (Geilhufe, Tr. 9586, 9705-9706, 9732; CCFF 2168). Mr. Geilhufe based his assumption that only laser blown fuses would be used to implement this alternative on his understanding that anti-fuse technology has a reliability factor which is inconsistent with the cost objectives of DRAM manufacturing. (Geilhufe, Tr. 9732-9733). However, the only documentary evidence in this case is that

(CCFF 2158, 2172-2175). If the Geilhufe assumption that anti-fuse technology is inappropriate for DRAMs is incorrect, and

DRAM manufacturers could use anti-fuses to set CAS latency then the cost of manufacturing DRAMs that use fuses to set CAS latency would only include the incremental $0.01 cost of burning fuses at wafer sort.

976. The total additional incremental costs associated with the use of the alternative of using multiple pins to set latency is $0.04 per part, which is the additional incremental costs associated with packaging. (Rapp, Tr. 9815). As a percentage of ASP, this total additional incremental cost is .82%. (Rapp, Tr. 9818). (These numbers are illustrated in DX 307).

Response to Finding No. 976: RPF 976 is unreliable because it is based on cost determinations of Mr. Geilhufe that are themselves unreliable. (CCRF 969). Additionally, Mr. Geilhufe's cost estimates depend on his twin assumptions that JEDEC would use the same number of CAS latencies that are used in the current standard, and that there are not enough "no-connect" pins available to identify all of the alternatives. (CCFF 2191). However, a review of Release 9 of the JEDEC 21-C standard reveals that forty-four out of forty-seven pinouts described in that standard have no-connect pins that could be used to determine CAS latency. (CCFF 2196). In addition, the Geilhufe assumptions require that JEDEC not change the pinouts despite the fact that it has changed the standard to use pins to set latency. This assumption is contrary to the weight of the evidence that before a standard is adopted, there is some flexibility with respect to assigning functions to pins. (CCFF 2193-2197). If no pins need to be added to implement this alternative then Mr. Geilhufe's analysis dictates that it have zero additional incremental costs over the current standard.

977. In addition to the additional incremental costs, each of the alternatives for programmable CAS latency either has performance disadvantages when compared to Rambus's technology or is covered by Rambus's patents. (Rapp, Tr. 9819-23). (These disadvantages are illustrated in DX308.)

Response to Finding No. 977: RPF 977 does not cite to record evidence. The evidence cited is testimony by an economic expert that is cited as substantive evidence on a matter outside of his stated expertise. Furthermore, RPF 977 is contrary to the weight of the evidence. For

a discussion of the costs and benefits of the alternatives described in RPF 973-976, as well as others described in this case for replacing the use of a mode register to set CAS latency, *see* CCFF 2130-2233.

978. The alternatives for programmable burst length identified as "commercially viable" by Complaint Counsel's economic expert were: fixed burst length, explicitly identify burst length in the read command, using a burst terminate command, and using multiple pins to set the burst length. (Rapp, Tr. 9810-11; McAfee, Tr. 7366-72).

Response to Finding No. 978: Complaint Counsel does not disagree. However, Complaint Counsel's technical expert identified an additional option, "program burst length by blowing fuses on the DRAM." (CCFF 2261-2269). Professor McAfee did not express an opinion on whether that alternative could constrain the price of using the mode register to set burst length because he saw no evidence that it was presented at JEDEC. (McAfee, Tr. 7372). However, Professor McAfee did not testify that the technology was not commercially viable, and it turns out the feature was proposed to JEDEC. (CCFF 2266).

979. The total additional incremental costs associated with the use of the fixed burst length alternative is $0.02 per part. (Rapp, Tr. 9824-25). This total consists of the following additional incremental costs per part: a $0.01 wafer sort cost savings and a $0.03 inventory cost increase. (Rapp, Tr. 9825). As a percentage of ASP, this total additional incremental cost is 0.41%. (Rapp, Tr. 9825). (These numbers are illustrated in DX309.)

Response to Finding No. 979: RPF 979 is unreliable because it is based on cost determinations of Mr. Geilhufe that are themselves unreliable. (CCRF 969). Additionally, Mr. Geilhufe's cost estimates for the inventory cost element depends critically on his assumption that JEDEC would have specified the same number of burst lengths in a fixed burst length standard as it currently has. (Geilhufe, Tr. 9594-9595, 9706-9707). Mr. Geilhufe based his determination of inventory costs on the number of different DRAM chips he thought would be produced. (Geilhufe, Tr. 9595). Mr. Geilhufe agreed that if JEDEC were to have adopted a standard that only had a single burst length that would have reduced those inventory costs. (Geilhufe, Tr. 9710). But Mr.

Geilhufe did nothing to ensure that his assumption, that JEDEC would have specified the same number of burst lengths in a fixed burst length standard as it currently has, was appropriate. In making his assumption that the number of new part numbers that would be required for a fixed CAS latency and a fixed burst length should be derived from the JEDEC standard, Mr. Geilhufe never looked at the market today to see how many of those different types of parts are sold. (Geilhufe, Tr. 9707). Mr. Geilhufe never saw any evidence from JEDEC regarding how many different types of DRAMs would have been sold had there been a fixed CAS latency and a fixed burst length. (Geilhufe, Tr. 9707-9708). Mr. Geilhufe never read any testimony, either from deposition or at the Hearing, from a current industry participant regarding how many different types of DRAMs would have been sold had there been a fixed CAS latency and a fixed burst length. (Geilhufe, Tr. 9708).

Had Mr. Geilhufe reviewed the record evidence he would have realized that the assumption that JEDEC would have retained the same number of burst lengths if it had standardized a fixed burst length DRAM rather than a programmable burst length DRAM is contrary to the weight of the evidence. In particular, when a proposal for fixed burst length was actually made at JEDEC, the proposal often included only one burst length rather than a number of fixed burst lengths. (CCFF 2243-2244, 2250, 2252). In addition, had Mr. Geilhufe reviewed the record evidence he would have understood that the purpose of proposals that fixed burst length was to reduce costs. (CCFF 2245-46).

If Mr. Geilhufe's assumption is incorrect and JEDEC would have standardized a single fixed burst length DRAM then both the inventory cost element would be zero, resulting in a projection that the fixed burst length DRAM would in fact be $0.01 cheaper to manufacture than the current standard.

980. The total additional incremental costs associated with the use of the alternative of explicitly identifying burst length in the read command is $0.01 per part, which is the additional incremental costs associated with packaging. (Rapp, Tr. 9825-26). As a percentage of ASP, this total additional incremental cost is 0.21%. (Rapp, Tr. 9826). (These numbers are illustrated in DX309.) As discussed above, this alternative is covered by Rambus's patents.

Response to Finding No. 980: RPF 980 is unreliable because it is based on cost determinations of Mr. Geilhufe that are themselves unreliable. (CCRF 969). Additionally, RPF 980 is unreliable because it is based on a misstatement of the opinion of Mr. Geilhufe. Mr. Geilhufe's opinion regarding the cost of this alternative is that the there is no increase in the variable cost of manufacturing this DRAM unless the implementation requires an additional pin. The assumption that more pins would be required to implement the alternative of using two voltage levels via pin to set CAS latency and burst length was based solely on Mr. Geilhufe's reading of Professor Jacob's report. (Geilhufe, Tr. 9722). Mr. Geilhufe did not do anything to ensure that it was the case that more pins would actually be required to implement the alternative of using two voltage levels via pin to set CAS latency and burst length. (Geilhufe, Tr. 9722). In fact, Mr. Geilhufe's own demonstrative describing these costs indicates his opinion that there would be a negligible cost change under the packaging element if no additional pin were required to implement this alternative. (DX0299). If no additional pin is required to implement this alternative then there are no additional variable costs to manufacture DRAMs corresponding to the alternative.

981. There is no additional incremental cost associated with the use of the alternative of using a burst terminate command to set burst length. (Rapp, Tr. 9826). As discussed above, this alternative suffers from performance drawbacks.

Response to Finding No. 981: Complaint Counsel agrees that there is no additional incremental cost associated with the use of the alternative of using a burst terminate command to set burst length.

982. The total additional incremental costs associated with the use of the alternative of using multiple pins to set latency is $0.02 per part, which is the additional incremental costs associated with packaging. (Rapp, Tr. 9826). As a percentage of ASP, this total additional

incremental cost is .41%. (Rapp, Tr. 9826). (These numbers are illustrated in DX 309.) As discussed above, this alternative is covered by Rambus's patents.

Response to Finding No. 982: RPF 982 is unreliable because it is based on cost determinations of Mr. Geilhufe that are themselves unreliable. (CCRF 969). Additionally, Mr. Geilhufe's cost estimates depend on his twin assumptions that JEDEC would use the same number of burst lengths that are used in the current standard, and that there are not enough no-connect pins available to identify all of the alternatives. (CCFF 2191). However, a review of Release 9 of the JEDEC 21-C standard reveals that forty-four out of forty-seven pinouts described in that standard have no-connect pins that could be used to determine CAS latency. (CCFF 2276). In addition, the Geilhufe assumptions require that JEDEC not change the pinouts despite the fact that it has changed the standard to use pins to set burst length. This assumption is contrary to the weight of the evidence that before a standard is adopted, there is some flexibility with respect to assigning functions to pins. (CCFF 2193-2197). If no pins need to be added to implement this alternative then Mr. Geilhufe's analysis dictates that it have zero additional incremental costs over the current standard.

983. In addition to the additional incremental costs, each of the alternatives for programmable burst length either has performance disadvantages when compared to Rambus's technology or is covered by Rambus's patents. (Rapp, Tr. 9828-30). (These disadvantages are summarized in DX 310.)

Response to Finding No. 983: RPF 983 does not cite to record evidence. The evidence cited is testimony by an economic expert that is cited as substantive evidence on a matter outside of his stated expertise. Furthermore, RPF 983 is contrary to the weight of the evidence. For a discussion of the costs and benefits of the alternatives described in RPF 979-982, as well as others relating to burst length described in this case, *see* CCFF 2234-2321.

984. The most costly alternatives to the two identified Rambus technologies that are used in JEDEC-compliant SDRAM that are not covered by Rambus's patents are the use of fuses to set latency and the use of fixed burst length. (Rapp, Tr. 9832). The total additional incremental cost

of using these two alternatives is $0.08 per part. (Rapp, Tr. 9832). As a percentage of ASP, this additional incremental cost is 1.64%, which exceeds the 0.75% Rambus royalty rate. (Rapp, Tr. 9832). (These numbers are illustrated in DX 311.)

Response to Finding No. 984: RPF 984 is unreliable because it is based on cost determinations of Mr. Geilhufe that are themselves unreliable. (CCRF 969). Additionally, this proposed finding is premised on a number of unsupportable assumptions that determine Mr. Geilhufe's cost estimates. (CCRF 973-976, 979-982). Once these cost estimates are adjusted to be more in line with the record evidence, the total additional incremental cost of the use of fuses to set latency (CCRF 975) and the use of fixed burst length (CCRF 979) is $0.00. This results in a cost that is lower than the 0.75% Rambus royalty rate.

985. The least costly alternatives to the two Rambus technologies that are used in JEDEC-compliant SDRAM that are not covered by Rambus's patents are the use of fixed CAS latency and the use of a burst terminate command to set burst length. (Rapp, Tr. 9831). The total additional cost of using these two alternatives is $0.04 per part. (Rapp, Tr. 9831-32). As a percentage of ASP, this additional incremental cost is 0.82%, which exceeds the 0.75% Rambus royalty rate. (Rapp, Tr. 9832). (These numbers are illustrated in DX 311.)

Response to Finding No. 985: RPF 985 is unreliable because it is based on cost determinations of Mr. Geilhufe that are themselves unreliable. (CCRF 969). Additionally, this proposed finding is premised on a number of unsupportable assumptions that determine Mr. Geilhufe's cost estimates. (CCRF 973-976, 979-982). Once these cost estimates are adjusted to be more in line with the record evidence, the total additional incremental cost of the use of fixed CAS latency (CCRF 973) and the use of a burst terminate command to set burst length (CCRF 981) is -$0.01. This results in a cost that is not only lower than the 0.75% Rambus royalty rate, it is lower than the cost of the current standard without the Rambus royalties.

986. In order to determine what royalty a rational decision-maker would have expected Rambus to charge (in the absence of direct knowledge), the standard assumption and methodology in economics is to assume that the royalty rate actually charged is the best estimate of the royalty rate a decision-maker would have expected at an earlier time. (Rapp, Tr. 10207-09). Similarly, the standard assumption and methodology in economics is to assume that the actual weighted average selling price over the product life cycle is the best estimate of an ASP that a decision-maker would

have predicted in advance. (Rapp, Tr. 10212-13). Using the standard assumptions and methodology in economics, a rational DRAM manufacturer or group of manufacturers would have expected the additional costs of any alternatives to outweigh the costs of Rambus's royalties.

Response to Finding No. 986: RPF 986 is misleading because it conflates what it terms to be the "standard assumption and methodology on economics" regarding the expectations of JEDEC members with the actual expectations they had. Dr. Rapp testified at trial that he understood that Mr. Geilhufe did not testify as to what cost information JEDEC or JEDEC participants had when they were setting the standard. (Rapp, Tr. 10203). Dr. Rapp agreed that he did not know what information any individual JEDEC participant in fact did have relating to any specific alternative that he considered. (Rapp, Tr. 10205). However, Dr. Rapp also agreed that if in the relevant time period, JEDEC participants had information about the costs of the alternatives that Dr. Rapp considered that was different from Mr. Geilhufe's cost information, that might undermine the economic conclusions that Dr. Rapp made about what decisions would be rational for JEDEC or JEDEC participants to make in the but-for world. (Rapp, Tr. 10203-04). Dr. Rapp agreed that if it were the case that JEDEC or JEDEC participants had different information about the costs of the alternatives that Dr. Rapp considered, that might suggest that JEDEC participants could have reached different conclusions than the conclusions that he reached and still have been acting in an economically rational manner. (Rapp, Tr. 10204). Dr. Rapp cannot rule out the possibility that for some of the companies that were participants of JEDEC in the relevant time, based on the information that they possessed, the economically rational thing would have been to support the use of various alternatives over the use of Rambus' technologies. (Rapp, Tr. 10205-206).

Regarding the expectations that JEDEC members had regarding royalties, Dr. Rapp agreed at trial that JEDEC and/or specific JEDEC participants would not have known specifically what royalties Rambus would seek in connection with the technologies that Rambus has claimed in the

event that those technologies were adopted as part of JEDEC's standards. (Rapp, Tr. 10206-207). Dr. Rapp also agreed that, to the extent that JEDEC participants were uncertain about what royalty would apply, there could be varying projections from JEDEC participant to JEDEC participant regarding what royalty rates would apply to the Rambus technologies and those projections could differ from the royalty rates that he assumed in material ways. (Rapp, Tr. 10209).

Despite the importance of the actual expectations of JEDEC members on his opinions, Dr. Rapp did nothing to ensure that his assumptions were reasonable. Dr. Rapp reviewed no third-party business records. (Rapp, Tr. 9992; *see* DX0324). Dr. Rapp reviewed no deposition testimony. (Rapp, Tr. 9993; *see* DX0324). Dr. Rapp reviewed no JEDEC materials/minutes other than two technical specifications. (Rapp, Tr. 9994; *see* DX0324). Dr. Rapp reviewed no notes/reports on JEDEC activities. (Rapp, Tr. 9995; *see* DX0324). Dr. Rapp reviewed none of the Rambus / JEDEC / third-party records cited in McAfee's report. (Rapp, Tr. 9999; *see* DX0324).

987. Even without any reference to performance penalties, a rational manufacturer or group of manufacturers in JEDEC would have chosen to take a license from Rambus at 0.75% for SDRAM rather than use any combination of the alternatives identified by Complaint Counsel's economic expert as "commercially viable" that are not covered by Rambus's patents because all of those alternatives are more costly than licensing the Rambus technologies for SDRAM. (Rapp, Tr. 9833). Taking performance issues into account would have reinforced the decision to license rather than to substitute any of these alternatives because most of the alternatives have performance problems as well. (Rapp, Tr. 9833).

Response to Finding No. 987: This proposed finding is unreliable and contrary to the weight of the evidence. This proposed finding is unreliable for a number of reasons. First, a rational JEDEC member's choice during the relevant period is based on the information in its possession, and neither Dr. Rapp nor Mr. Geilhufe did anything to attempt to arrive at that information. (CCRF 986). Second, this finding relies on the assumption made by Dr. Rapp that JEDEC members conducted the same analysis in making decisions regarding what technologies to put into the standards that he d*id.* (CCFF 2825-2827). Neither Dr. Rapp nor Mr. Geilhufe did

anything to ensure that the analysis that he did was the type of analysis done at JEDEC. (CCFF 2121, 2825-2827). Third, this finding relies on the assumption made by Dr. Rapp that JEDEC would treat costs relating to manufacturing the same way they treat costs relating to royalties. However, manufacturing costs are not subject to hold-up and royalties are. (McAfee, Tr. 11241-11243). Fourth, this finding relies on assumptions made by Dr. Rapp regarding whether Rambus has patents covering some of the alternatives. (CCFF 2872-2873). If Dr. Rapp's assumptions in this regard are incorrect, then, even using the cost estimates provided by Mr. Geilhufe, Dr. Rapp's conclusions are incorrect. (CCFF 2874). Fifth, Dr. Rapp relied on Mr. Geilhufe's cost estimates to the exclusion of other record evidence that shows that Mr. Geilhufe's cost estimates were too high. (CCFF 2828, 2884). An analysis using alternative cost estimates that are more in line with the record evidence demonstrates that the alternatives would not be more expensive than the current standard burdened by the Rambus royalties. (CCRF 970-985). Finally, neither Dr. Rapp nor Mr. Geilhufe take into account the effect of productivity gains on manufacturing costs that would reduce the manufacturing costs below what Mr. Geilhufe estimated over the relevant period. (CCFF 2879-2883). Substituting alternative cost figures that take into account productivity gains reverses Dr. Rapp's conclusions regarding what would have been "rational" for JEDEC to have adopted had Rambus disclosed. (CCFF 2880-2881).

This proposed finding is contrary to the weight of the evidence because it depends on assumptions that are themselves contrary to the weight of the evidence. For example, Dr. Rapp ignores the importance of the differences between royalties and manufacturing costs contrary to the evidence that JEDEC members specifically avoided using technologies that were burdened by royalties, (CCFF 107-111, 300-303, 2433-2464) and contrary to the lock-in and hold-up concerns in the DRAM industry. (CCFF 2682-2756). Another example, of how this finding is contrary to the weight of the evidence is that, by ignoring productivity improvements, Dr. Rapp in effect

assumes that there is no productivity improvements in the DRAM industry. But the weight of the evidence shows that DRAM manufacturers must reduce costs by 30% per year on a per bit basis simply to stay competitive in the industry. (CCFF 95-98; Geilhufe, Tr. 9586 - 9587 ("Well, the DRAM industry is an interesting industry because of the cost reductions that take place in the industry over a relatively short time period. A 64-meg DRAM in 1994 may be $40 or $50 in cost, and 12 to 15 months later, it may only be $4 or $3 or $2 in cost, a very steep cost reduction.... [T]he cost reductions are caused by the changes in manufacturing processes that we use; that is, we go from 0.18 micron to -- 180 nanometers to 150 or 160 nanometers, so we can improve the cost very quickly, and we solve yield problems very quickly. You know, hundreds of engineers work on what is causing yield problems. So, we get down the learning curve very, very quickly.")).

988. Accordingly, a rational standard-setting organization that knew that Rambus had patent interests on those two technologies but did not know precisely what Rambus's royalty rates would be to license the technologies would have selected the Rambus technologies. (Rapp, Tr. 9838-39). That is true even if the standard-setting body were acting in a satisficing manner. (Rapp, Tr. 9839-40). If satisficing means that small cost differences are overlooked, then a satisficing standard-setting body would be indifferent to the prospect of paying royalties; therefore, the theory of satisficing does not contribute to the analysis. (Rapp, Tr. 9839-40).

Response to Finding No. 988: This finding is unreliable and contrary to the weight of the evidence. (*See* CCRF 987).

4. There Were No Viable Non-Infringing Alternatives To The Specified Rambus Technologies Adopted In DDR SDRAM.

989. The discussion above applies to the two specified Rambus technologies that were carried over from SDRAM to DDR SDRAM, namely programmable CAS latency and programmable burst length.

Response to Finding No. 989: Complaint Counsel has no specific response to this proposed finding.

a. Dual-Edge Clocking.

990. Complaint counsel, through Professor Jacob, have suggested the following possible alternatives to dual-edge clocking in DDR SDRAMs:

(1) Interleave on-chip banks;
(2) Interleave on-module ranks;
(3) Increase the number of pins on the DRAM;
(4) Increase the number of pins on the module;
(5) Double the clock frequency;
(6) Use simultaneous bidirectional input/output;
(7) Use toggle mode.

(Jacob, Tr. 5415-5438).

Response to Finding No. 990: Complaint Counsel agrees that RPF 990 accurately represents a list of Dr. Jacob's proposed alternatives to dual edged clocking.

(1) Interleaving On-Chip Banks Was Not a Viable Alternative.

991. Professor Jacob's alternative of interleaving on-chip banks involves sending a clock signal to one bank on the DRAM and a second clock signal, a delayed version of the first, to another bank. (Jacob, Tr. 5419-20, 5614). Data would then be output or input on only a single edge of each clock signal, alternating between the two banks. (*Id.*).

Response to Finding No. 991: This proposed finding is misleading because it only represents one of the two different implementations that Dr. Jacob proposed to interleave on-chip banks in order to double the data rate. (*See* CCFF 2344).

992. Complaint Counsel did not meet their burden of showing that interleaving on-chip banks was a viable alternative to dual-edge clocking in DDR SDRAMs.

Response to Finding No. 992: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (*See* 2344-2350 (Complaint Counsel's findings which support the conclusion that interleaving on-chip banks was a viable alternative)).

993. To the contrary, the evidence in the record shows that interleaving on-chip banks was not a viable alternative to dual-edge clocking in DDR SDRAMs, because it suffers from

performance and cost disadvantages. Moreover, interleaving on-chip banks is not an alternative because it is covered by Rambus patents.

Response to Finding No. 993: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, the weight of the evidence suggests that there were no significant costs associated with interleaving on-chip banks. (CCFF 2344-2350). There is substantial evidence in the record to indicate that it may have even been less expensive to interleave on-chip banks than use dual edge clocking. (*See* CCFF 2345, 2349-50 (this alternative would not require symmetric clocks, which means that cheaper clocks that were easier to design could have been used to implement this alternative)).

994. Professor McAfee did not testify that interleaving on-chip banks was a commercially viable alternative. (McAfee, Tr. 7376-81).

Response to Finding No. 994: This proposed finding is misleading because Dr. McAfee did not testify regarding whether this alternative was commercially viable. (McAfee, Tr. 7377-81; *see* DX0200 (only identifying one of the proposed dual edged clocking alternatives, increasing the number of pins per DRAM module, as not commercially viable)). For a more complete discussion of the evidence in support of its commercial viability, refer to CCFF 2344-2350.

995. Efficient implementation of interleaving on-chip banks would still require dual-edge clocking and, therefore, is not an alternative. (Soderman, Tr. 9366). That is because the successive data signals from each bank should be given equal amounts of time on the bus. If one bank were given a shorter time window for detection of data signals than the other, the data given the shorter time window might not be detected accurately; if, the data could be detected accurately in such a short time window, then it would be more efficient to restrict both banks to such a time window and run the bus at a faster speed. (Soderman, Tr. 9384-85). Also, a multiplexer would be used to select which bank is outputting data onto the bus at a given time. (Soderman, Tr. 9384). But the multiplexer must have a timing reference to tell it when to switch from one bank to the

other. If one of the two clocks required by Professor Jacob's alternative is used for this reference, then data will be output onto the bus on both the rising and falling edge of this clock (since the falling edge of one of these clocks corresponds to the rising edge of the other); if, on the other hand, a third clock (not specified by Professor Jacob) is used to time the multiplexer, data would have to be output on the rising and falling edges of that clock. (Soderman, Tr. 9384-86).

Response to Finding No. 995: This proposed finding is misleading and unreliable because Dr. Soderman made assumptions regarding the operation of this alternative that were different from those made by Professor Jacob. Dr. Soderman's opinion that efficient operation of this alternative requires dual-edge clocking is based on his erroneous assumptions that a "multiplexor" or "mux" is required to operate this alternative, and that the clocks driving the data off of the DRAM are perfect clocks, spending the same amount of time rising and falling (50% duty cycle), and having the ability to transition from a rising edge to a falling edge at the same rate that it transitions from a falling edge to a rising edge ("slew rate"). (*Cf.* Soderman, Tr. 9384-86 (discussing DX0293 and assuming a "50% duty" and the need for a "mux") *with* Jacob, Tr. 5418-19 (discussing DX0089, which does not identify the need for a mux) and Jacob, Tr. 11117, 11119-20 (discussing DX0358, which illustrates that the use of a 10% duty cycle would mean that the positive edge of clock and delayed clock would drive data in a system that interleaved on-chip banks)).

These assumptions by Dr. Soderman regarding Professor Jacob's alternative are contradicted by Professor Jacob's testimony. (*See* CCFF 2347-2350). Consequently, Dr. Soderman's testimony about the interleaving on-chip banks is unreliable to discredit Dr. Jacob's testimony because Dr. Soderman and Dr. Jacob were analyzing different implementations of interleaving on-chip banks.

996. Even if interleaving on-chip banks did not require dual-edge clocking, it would still not be an alternative to Rambus's technology because it is covered by U.S. Patent No. 5,915,105, assigned to Rambus. (RX 1472).

Response to Finding No. 996: This proposed finding is not supported by any evidence in the record. Respondent did not present expert testimony to support a proposed finding that U.S. Patent No. 5,915,105 (the '105 patent), covers the use of interleaving on-chip banks. Furthermore, Respondent did not present any evidence that Rambus believed it could cover the concept of interleaving on-chip banks or that Rambus was trying to broaden its patents to capture that concept.

The interpretation of patent claims involving complex technology, and the comparison of a product to that claim, cannot be properly resolved without the development of evidence, including expert testimony, before the finder of fact. *See NeoMagic Corp. v. Trident Microsystems, Inc.*, 287 F.3d 1062, 1074 (Fed. Cir. 2002) ("given the complex technology involved in this case, we think that this matter [interpretation of a claim to a DRAM memory chip controller] can only be resolved by further evidentiary hearings, including expert testimony, before the district court.").

A determination that a patent claim covers a product is a two step process. The first step requires that the court interpret the patent claim as it would be understood by a person of ordinary skill in the art. (Fliesler, Tr. 8893). RPF 996 cites no expert testimony or other evidence to establish the proper interpretation of the patent claims.

The second step requires a factual determination that each element of the properly interpreted claim is present in the product. (Nusbaum, Tr. 1565-66). RPF 996 cites no expert testimony or other evidence to establish that each element of any claim of this patent correspond to elements of the proposed alternative.

997. For example, claim 27 of the '105 patent claims:

> A memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises:
>
> a first clock receiver to receive a first external clock signal;

a second clock receiver to receive a second external clock signal; and

input receiver circuitry, coupled to the first and second clock receivers, to sample information on a bus synchronously with respect to the first and second external clock signals.

Response to Finding No. 997: This proposed finding is irrelevant because there is no evidence in the record to support that claim 27 of the '105 patent is relevant to this case for the reasons set forth in CCRF 996.

998. A claim covers a device if each and every claim element or "limitation" is found in that device. (Nusbaum, Tr. 1565-66). SDRAMs are memory devices that have memory sections containing a plurality of memory cells. (Rhoden, Tr. 359-60, 369-70). Interleaving on-chip banks involves two external clock signals, with the first going to one bank on the DRAM and the second to another bank. (Jacob, Tr. 5419-20, 5614). Data would then be input or "sampled" synchronously with respect to the first and second external clock signals. (*Id.*). Thus, each and every element of claim 27 of the '105 patent would be found in DDR SDRAMs that implemented interleaving on-chip banks.

Response to Finding No. 998: This proposed finding is misleading because it incorrectly implies that there has been evidence, of the type described in CCRF 996, submitted in this case that goes to the definitions of the terms of claim 27 of the '105 patent, and that there has been evidence submitted that the alternative infringes that patent claim. The statement in this proposed finding that "SDRAMs are memory devices that have memory sections containing a plurality of memory cells" is not supported by the cited testimony. Mr. Rhoden did not testify as to the meaning of the term "plurality of memory cells" and was not asked to do so in the context of any Rambus patent. Furthermore, the statement "data would then be input or 'sampled' synchronously with respect to the first and second external clock signals" is also not supported by the cited testimony. Professor Jacob was not testifying as to the meaning of the claim and was not asked to do so. Furthermore, the statement is not accurate as professor Jacob's alternative involves data being "sampled" synchronously with respect to the first *or* second external clock signals. (Jacob, Tr. 5418-5420).

The statement in this proposed finding that "each and every element of claim 27 of the '105 patent would be found in DDR SDRAMs that implemented interleaving on-chip banks" is a legal conclusion, which lacks any citation to the record and is therefore inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

999. Professor Jacob did not consider the '105 patent when he proposed interleaving on-chip banks as an alternative. (Jacob, Tr. 5615-16).

Response to Finding No. 999: This proposed finding is misleading to the extent that it suggests that there is evidence in the record that supports the proposition that Dr. Jacob should have considered the '105 patent. To the contrary, there is no evidence in the record to support that the '105 patent is relevant to the issues in this case for the reasons set forth in CCRF 996.

1000. Performance disadvantages of interleaving on-chip banks include significant increased power dissipation because of the power consumed by the additional clocks and the fact that two banks are being accessed alternately. Keeping both banks active doubles the number of precharge cycles, and the precharge operation may be the most power consuming part of the whole DRAM operation. (Soderman, Tr. 9387).

Response to Finding No. 1000: This proposed finding ignores substantial evidence in the record that there were advantages associated with this proposed alternative and that any disadvantages associated with this alternative were not significant. (*See* CCFF 2345-2346).

1001. The alternative of interleaving on-chip banks would also have resulted in increased costs.

Response to Finding No. 1001: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, the weight of the evidence suggests that there were no significant costs associated with interleaving on-chip banks. (CCFF 2344-2350). There is substantial evidence in the record to indicate that it would have been cheaper to interleave on-chip banks than use dual edge clocking. (*See* CCFF 2345, 2349-50 (this alternative would not require symmetric clocks, which means that cheaper clocks that were easier to design could have been used to implement this alternative)).

1002. There would have had to be a significant design effort for this alternative. (Geilhufe, Tr. 9602-03).

Response to Finding No. 1002: This proposed finding is incomplete because it omits testimony by Mr. Geilhufe that he believed that the additional design cost for this alternative was only $250,000 for an entire production run. (Geilhufe, Tr. 9602-03).

Furthermore, this proposed finding ignores substantial evidence that there were no significant costs associated with this proposed alternative. (*See* CCFF 2344-2350).

1003. There would have been a reduction in good die yield due to additional critical die area. (Geilhufe, Tr. 9603-04). So-called "redundancy technology" can be used to replace a defective part of the memory array on a DRAM, but the peripheral circuitry is "critical" in the sense that a defect in that circuitry will cause the unit to fail. (Geilhufe, Tr. 9603). The additional peripheral circuitry that would have been required to implement this alternative – such as multiplexing circuitry and timing circuitry – is critical in nature and defects in this circuitry would have reduced the good die yield. (Geilhufe, Tr. 9603-04).

Response to Finding No. 1003: This proposed finding is unreliable because it is based on Mr. Geilhufe's assumption that interleaving on-chip banks would require a multiplexor. This assumption contradicts testimony by Professor Jacob that interleaving on-chip banks would not have required a multiplexor. (Jacob, Tr. 11136-37; *see* CCFF 2347).

Furthermore, Mr. Geilhufe's methodology to evaluate the impact of a proposed alternative on "good die yield" was unreliable for the following reasons.

Mr. Geilhufe recognized that in order to determine the effect on good die yield of some of the alternatives that he analyzed, he had to look at the changes in circuitry that would be required to implement the alternative as compared to the current standard. (Geilhufe, Tr. 9696). However, Mr. Geilhufe did no circuit design or circuit layout for his work on this case to determine precisely what circuitry needed to be added. (Geilhufe, Tr. 9696-97 ("That's correct, there was no circuit design and no layout done.")).

Mr. Geilhufe did not look at removing the circuitry for any dual edged clocking alternative to determine precisely what circuitry could be removed from the current standard. (Geilhufe, Tr. 9697).

Mr. Geilhufe simply "estimated if some circuitry could be removed or some circuitry had to be added." (Geilhufe, Tr. 9697).

Mr. Geilhufe recognized that his estimates were "rough estimates." (Geilhufe, Tr. 9696). Once he made the determination that the circuit size would be larger for the alternative than for the original, Mr. Geilhufe simply assumed that the increase in circuit size would lead to a reduction in yield. (Geilhufe, Tr. 9697). Mr. Geilhufe reviewed no evidence from this case relating to the costs of DRAM manufacturers for the good die yield cost element, from the relevant period other than the Peisl deposition. (Geilhufe, Tr. 9698).

1004. This alternative would have also complicated final testing and led to a slightly higher fall-out at that stage due to the necessity to activate two banks and to test the additional clocking circuitry. (Geilhufe, Tr. 9604).

Response to Finding No. 1004: This proposed finding is unreliable because the methodology that Mr. Geilhufe used to analyze these cost factors was unreliable. In particular, Mr. Geilhufe assumed that the changes involved would have led to higher test costs, and that assumption was based in part on his assumption that extra circuitry was required. (Geilhufe, Tr. 9604). Mr. Geilhufe reviewed no evidence related to the cost to DRAM manufacturers for final

test and good unit yield for the relevant time period, other than the Peisl deposition, and some "confidential" evidence that is not in the record. (Geilhufe, Tr. 9706).

1005. The alternative of interleaving on-chip banks would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: $250,000 increase in product design costs; three cents per unit cost increase due to reduced good die yield; two cents per unit increase in final testing and good unit yield costs. (Geilhufe, Tr. 9562-64, 9602-04).

Response to Finding No. 1005: This proposed finding is unreliable for a number of reasons. The product design costs estimate is unreliable because it is based on an inaccurate assumption that volume production for a first-tier manufacturer like Samsung, Infineon, or Micron, was approximately 20 million units for a product that was well into its life cycle. (Geilhufe, Tr. 9562, 9726). The weight of the evidence is that the volume production level for a particular part is substantially higher than 20 million units. The volume production for Micron's 64 meg SDRAM, including shrinks, was approximately 900 million units. (Lee, Tr. 10997). The volume production for Micron's 128 meg SDRAM part was also approximately 900 million units. (*Id.* 10998). The 256 meg SDRAM, which started its life cycle in 2000, has already reached a volume production level of approximately 400 million units. (*Id.*).

Furthermore, this proposed finding is incomplete because it omits testimony by Mr. Geilhufe that the costs of all of the alternatives could fall over time due to further die shrinks. (Geilhufe, Tr. 9726 ("It's possible that there are further shrinks, but I -- I assumed that 20 million units could be built off that one design effort.")).

Furthermore, the variable per unit cost estimates are unreliable for the reasons set forth in CCRF 837, 1002-1004.

1006. The net increase in variable costs for the alternative of interleaving on-chip banks is, therefore, approximately 5 cents per unit. The total costs increase is approximately 6 cents per unit, calculated by converting the fixed costs to per unit costs through division by 20 million (the

unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9604-05).

Response to Finding No. 1006: This proposed finding is unreliable because the methodology that Mr. Geilhufe used to analyze the costs of alternative technologies is based on inaccurate assumptions, is not the appropriate methodology to rely on to determine the viability of alternative technologies in this case, and is more generally unreliable for the reasons set forth in CCRF 837 and CCRF 1005.

(2) Interleaving On-Module Ranks Was Not a Viable Alternative.

1007. Professor Jacob's proposed alternative of interleaving banks on the DIMM or memory module is similar to his proposed alternative of interleaving on-chip banks except that data from different chips in a module, rather than data from different banks on the same chip, would be interleaved. (Jacob, Tr. 5426).

Response to Finding No. 1007: Complaint Counsel has no specific response to this finding.

1008. Complaint Counsel did not meet their burden of showing that interleaving on-module ranks was a viable alternative to dual-edge clocking in DDR SDRAMs.

Response to Finding No. 1008: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs.

Furthermore, RPF 1008 ignores the weight of the evidence in the record that indicates that interleaving on-module ranks was a viable alternative. (CCFF 2351-2355).

1009. To the contrary, the evidence in the record shows that interleaving on-module ranks was not a viable alternative to dual-edge clocking in DDR SDRAMs, because it would be significantly costlier, in addition to having performance problems. Moreover, interleaving on-module ranks would provide less flexibility than dual-edge clocking and would not be available for all applications.

Response to Finding No. 1009: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs.

Furthermore, the statement in RPF 1009 that "interleaving on-module ranks was not a viable alternative to dual-edge clocking in DDR SDRAMs, because it would be significantly costlier, in addition to having performance problems" ignores significant record evidence. (Jacob, Tr. 5427; CCFF 2352). This alternative would not have required asymmetric duty cycles or slew rates. (Jacob, Tr. 5428). Instead, JEDEC would have chosen asymmetric clocks to implement this alternative. (Jacob, Tr. 11124 ("Because it's cheaper, it's easier to build, it's just a simpler design.")). (CCFF 2354).

1010. Implementing this technology would require high speed bidirectional switches or multiplexers. (Soderman, Tr. 9389). Such bidirectional switches would require sophisticated engineering and would add appreciable cost. (*Id.*). Moreover, additional hardware would be required to drive the switches. (*Id.*).

Response to Finding No. 1010: The statement in RPF 1010, that this alternative would add cost by requiring additional components and hardware is incomplete because it fails to take into account the advantages of this particular proposal. (CCFF 2352, 2354).

Furthermore, this proposed finding is incomplete because it omits the substantial evidence in the record that this alternative would have only slightly increased the complexity of the module. (Jacob, Tr. 5428; Kellogg, Tr. 5185-86).

1011. Professor Jacob testified that this alternative would have significant advantages and that the only disadvantage would be a slight complication of the memory module because of an extra clock line. (Jacob, Tr. 5427-28). Professor Jacob did not testify about any need for expensive high speed switches. (*Id.*). Unlike most of Professor Jacob's proposed alternatives, his opinion about this alternative can be tested because a company, Kentron Technologies, has actually tried to implement the alternative of interleaving on module ranks. (Soderman, Tr. 9388).

Response to Finding No. 1011: This proposed finding is misleading because it implies that Professor Jacob ignored the potential use of switches to implement this alternative. However, Professor Jacob recognized that this alternative could complicate the DRAM module slightly. (Jacob, Tr. 5428 (The use of interleaving on the DIMM "pushes the complexity out of the DRAM onto the shoulders of the module designer so that now your module, for instance, would have to have an extra clock line or would have to have that delay element that's pictured in the figure, so it would complicate the module slightly.")).

Furthermore, this proposed finding is misleading because it implies that such switches are required to implement this alternative.

1012. Kentron's "QBM" technology involves interleaving between chips on the module. (Goodman, Tr. 5997, 6002-03). Robert Goodman, Kentron's Chief Executive Officer, testified that the QBM technology requires the use of advanced switches. (Goodman, Tr. 6082). Mr. Goodman further testified that each module would require eight switches at a dollar apiece in high-volume production, for a total of eight dollars per module. (Goodman, Tr. 6046-47, 6083). Additional circuitry, such as a PLL on the module is also required. (Goodman, Tr. 6048).

Response to Finding No. 1012: This proposed finding is misleading because it implies that the only way to implement the alternative was to use the technology used by Kentron.

Furthermore, the statement in this proposed finding that "Robert Goodman, Kentron's Chief Executive Officer, testified that the QBM technology requires the use of advanced switches" is misleading because Mr. Goodman testified that he is not a DRAM engineer and only had a "top level" understanding of DRAM technology. (Goodman, Tr. 5996 ("[Mr. Goodman's understanding of DRAM technologies was] just at a top level, just enough to understand and communicate how Kentron uses memory technologies to improve density and speed.")).

1013. Although Kentron now uses DDR SDRAM chips in its QBM technology, it initially called the technology "DBR" for "double bus rate" and used SDRAM chips. (CX 409 at 2). Kentron asserted that it could achieve the "same performance as 'DDR' using standard SDRAM single data rate." (*Id.*).

Response to Finding No. 1013: Complaint Counsel does not disagree.

1014.

(RX 1976 at 49) **[In Camera]** .

Response to Finding No. 1013: This proposed finding is misleading because it cites a document that is unsupported by testimony, even though an Intel employee testified at trial, to imply that an analysis by Intel in 2002 of the use of Kentron's technology with DDR SDRAM at *400 MHz* is the same analysis that would have been done by JEDEC members in 1996 of the use of this technology with SDRAM at 100 MHz.

Furthermore, this proposed finding ignores substantial evidence in the record that, whatever the view of the Kentron technologies at Intel, this alternative has been adopted by at least one of Intel's competitors in the chipset industry. VIA Technologies is one of Kentron's partners and has built a chipset to support QBM technology. (Goodman, Tr. 6004, 6011).

1015. AMD's preliminary evaluation of the Kentron QBM technology concluded that it would have signal integrity problems. (Polzin, Tr. 4035-36).

Response to Finding No. 1015: This proposed finding is misleading because it implies that Mr. Polzin testified that AMD did an "evaluation" of the Kentron technology. However, Mr. Polzin's testimony made it clear that he only had a "top-level familiarity" with the technology, and that no "evaluation" occurred. (Polzin, Tr. 4035 ("Q. Did you do a preliminary evaluation of that technology? A. Very preliminary. Basically I saw their presentation.)).

Furthermore, this proposed finding is misleading to the extent that it implies that Mr. Polzin's understanding of the technology is coincident with that of his company, AMD (Polzin, Tr. 4035).

1016. At the September 2000 JEDEC meeting, Kentron's motion to ballot QBM technology failed for lack of a second. (CX 160 at 1).

Response to Finding No. 1016: The statement in RPF 1016 is incomplete because it fails to include the additional meeting minutes, "The Committee wanted to see more information on how the spec would look before balloting it." (CX0160 at 1). The JC-42.5 Committee's response is consistent with JEDEC's desire to be as well informed as possible about proposed technologies to ensure the development of open standards. (*See generally* CCFF 300-04, 316-17, 339-46).

1017. Kentron has no customers for its QBM technology. (Goodman, Tr. 6008).

Response to Finding No. 1017: RPF 1017 is incomplete because omits testimony that Kentron has been partnering with VIA Technologies, who has built a chipset to support QBM technology. (Goodman, Tr. 6004, 6011).

1018. Interleaving on-module ranks suffers from additional disadvantages. First, it would lead to a less flexible memory increment: Because high bandwidth is achieved by interleaving between DRAMs, twice as many DRAMs would be required on the DIMM to achieve the same bandwidth as is available using dual-edge clocking. (Soderman, Tr. 9389-90).

Response to Finding No. 1018: This proposed finding ignores substantial evidence in the record that the flexibility of the memory increment or "granularity" of the DRAM was an issue that could be resolved by using the technology in applications that required two ranks of memory. (Jacob, Tr. 5428; Kellogg, Tr. 5185-86 ("I would minimize [costs relating to granularity] by, first of all, using this in applications that required two ranks of memory. Therefore, I'm not incurring any additional cost for the memory itself.")).

1019. Moreover, this alternative would not be available in all applications since many applications do not use modules at all but, rather, have the DRAM soldered directly onto the motherboard. (Soderman, Tr. 9390-91; Wagner, Tr. 3871-72).

Response to Finding No. 1019: This proposed finding is misleading because it is based, in part, on Mr. Wagner's testimony, which does not support the proposition. Mr. Wagner testified only that some applications do not use the kind of memory modules referred to as DIMMs. (Wagner, Tr. 3871). Graphics applications use graphics cards, which house a graphic chip and memory and power components. (*Id.* 3871-72). The mobile market uses a MAP, which is a "little memory graphics module." (*Id.* 3872). There is no evidence in the record to support the proposition that interleaving on-module banks could not have been implemented with graphics cards or MAPs.

1020. The alternative of interleaving on-module ranks would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: four dollars per module for multiplex and driver circuitry. (Geilhufe, Tr. 9562-64, 9605-06).

Response to Finding No. 1020: This proposed finding is unreliable because the methodology that Mr. Geilhufe used to analyze the costs of alternative technologies is based on inaccurate assumptions, not the appropriate methodology to rely on to determine the viability of alternative technologies in this case, and more generally unreliable for the reasons set forth in CCRF 837 and 853.

Furthermore, this proposed finding ignores substantial evidence that indicates that this alternative would have only slightly increased the complexity of the module. (Jacob, Tr. 5428; Kellogg, Tr. 5185-86).

1021. This four dollar per module cost translates into a 25 cent per DRAM cost for DIMMs, which are memory modules containing 16 DRAMs each.(Geilhufe, Tr. 9606). This 25-cent increase is a variable cost.

Response to Finding No. 1021: This proposed finding is inaccurate and unreliable for the reasons set forth in CCRF 1020.

(3) Increasing the Number of Pins on the DRAM Was Not a Viable Alternative.

1022. Professor Jacob's proposed alternative of increasing the number of pins per DRAM involves achieving high bandwidth by using only a single edge of a clock but doubling the number of data pins. (Jacob, Tr. 5429).

Response to Finding No. 1022: Complaint Counsel has no specific response to this proposed finding.

1023. Complaint Counsel did not meet their burden of showing that increasing the number of pins on the DRAM was a viable alternative to dual-edge clocking in DDR SDRAMs.

Response to Finding No. 1023: The statement in RPF 1023 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs.

Furthermore, RPF 1023 ignores the weight of the evidence that indicates that increasing DRAM width was a viable alternative. (CCFF 2356-58).

1024. To the contrary, the evidence in the record shows that increasing the number of pins on the DRAM was not a viable alternative to dual-edge clocking in DDR SDRAMs, because it would be significantly costlier, in addition to having performance problems.

Response to Finding No. 1024: The statement that increasing the number of pins on the DRAM was not a viable alternative lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs.

Furthermore, the statement in RPF 1024 that this alternative would be costlier ignores substantial evidence in the record that increasing the number of pins on the DRAM in order to

double the data rate would have required a far simpler clock circuit than dual edged clocking. (Jacob, Tr. 5430 ("Q. Now, what, if any, would have been the advantages had JEDEC chosen to increase the number of pins per DRAM rather than using a dual-edged clock? A. Again, you could retain the use of the single-edged clocking scheme, which means that you could use a far simpler clock circuit design. It would mean that your signals are transitioning at a slower rate than, for instance, a DDR-type interface, so rather than having a 200-megabit-per-second data pin, now you stick with a 100-megabit-per-second data pin, so the power of the DRAM actually goes down comparatively.")). Slower clock circuits and pins indicates that this alternative might consume less power than dual edged clocking. (*Id.*). Increasing the number of pins would not have resulted in a significant increase in noise relative to dual edged clocking. (*Id.* 5430-31). (CCFF 2358).

1025. Professor McAfee did not testify that this alternative is commercially viable. (McAfee, Tr. 7376-81).

Response to Finding No. 1025: This proposed finding is misleading because Dr. McAfee did not testify regarding whether this alternative was commercially viable. (McAfee, Tr. 7376-81; *see* DX0196).

1026. In addition to doubling the number of data pins, this alternative would require increasing the number of power and ground pins in order to support the added data pins. (Jacob, Tr. 5429-30). The number of pads and receivers on the DRAM would also have to be increased, leading to an increase in the size of the DRAM die and the size of the package. (Jacob, Tr. 5430-31).

Response to Finding No. 1026: Complaint Counsel does not disagree that this alternative would require increasing the number of pins. However, the statement in RPF 1026 is incomplete because it fails to mention that this alternative would not require an increase in the number of address pins (Jacob, Tr. 5430). The proposed finding also fails to mention the

advantages that could be associated with this alternative such as retaining a far simpler clock circuit design. (*Id.*).

1027. The additional data signals would toggle very fast and cause noise that could perturb the DRAM or other circuitry on the board. (*Id.*).

Response to Finding No. 1027: This proposed finding is not supported by the cited testimony. Dr. Jacob did not testify that the increase in noise in the DRAM would perturb the DRAM or other circuitry on the board. To the contrary, he testified that any increase in noise *would not perturb* the DRAM or other circuitry on the board because there would be more pins on the DRAM to spread the noise across. (Jacob, Tr. 5431).

1028. Tom Landgraf of Hewlett-Packard testified that his company was in favor of including dual-edged clocking in the DDR standard because of cost concerns. (Landgraf, Tr. 1709). Mr. Landgraf explained:

> "In DDR, double data rate memory, you need -- you're essentially transitioning data twice as fast as at a single data rate, and since memory systems tend to be very cost-competitive, one of our goals was to minimize the number of new pins we had to add to the next generation of memory. So, by using the double edged clock to transfer data, we were using the package and the pins more efficiently."

(Landgraf, Tr. 1709-10).

Response to Finding No. 1028: The statement in RPF 1028 that Hewlett Packard was in favor of including dual-edged clocking in the DDR standard does not support the conclusion that increasing the number of pins of the DRAM was not a viable alternative.

Furthermore, the proposed finding is incomplete. Mr. Landgraf stresses the importance of being cost competitive in his testimony. (Landgraf, Tr. 1709-10). Directly after he gave this testimony, he added that intellectual property coverage was also an important consideration. ((Landgraf, Tr. 1710 ("Q. Now, you mentioned a number of factors in your response that HP was considering. Did Hewlett Packard consider whether or not there were patents or patent

applications on dual edge clock when it was considering the DDR standard? A. If we knew about them, we would have -- we would have raised it as a consideration.")).

The weight of the evidence indicates that the valuation of dual edged clocking as a technology would have changed had Rambus disclosed the scope of its patent applications while JEDEC was still working on the standards. (CCFF 2101 (citing testimony from Sussman, Lee, Prince, Oh, Meyer, and Kellogg as support)).

1029. The alternative of increasing the number of pins on the DRAM would be very expensive because of the number of additional pins required. (Soderman, Tr. 9391-92). For example, DRAMs with 16 data pins would have to have 16 additional data pins, plus additional power and ground pins. (*Id.*). Moreover, the pins would need to be interconnected through the DIMM to the motherboard, increasing the cost of the whole system. (Soderman, Tr. 9392).

Response to Finding No. 1029: RPF 1029 ignores substantial record evidence because it fails to take into consideration the cost savings associated with the alternative's advantages. The DRAM mechanism is simpler because bandwidth is increased with no increase in the speed of the data pins. (Jacob, Tr.5429). This would have required a far simpler clock circuit design. (*Id* at 5430).

1030. There would have been additional product design costs because of the significant design effort associated with adding 16 input/output drivers and related multiplexing circuitry. (Geilhufe, Tr. 9607).

Response to Finding No. 1030: This proposed finding is incomplete because it omits testimony by Mr. Geilhufe that he believed that the additional design cost for this alternative was only $250,000 for the entire DRAM production run. (Geilhufe, Tr. 9607).

Furthermore, the proposed finding is unreliable because the methodology that Mr. Geilhufe used to reach his conclusions about the costs of alternative technologies was unreliable and irrelevant for the reasons set forth in CCRF 837.

Furthermore, his fixed cost estimate for additional product design costs is unreliable because it is based on an inaccurate assumption that volume production for a first-tier manufacturer

like Samsung, Infineon, or Micron, was approximately 20 million units for a product that was well into its life cycle. (Geilhufe, Tr. 9562, 9726). The evidence suggests that the volume production level for a particular part is substantially higher than 20 million units. The volume production for Micron's 64 meg SDRAM, including shrinks, was approximately 900 million units. (Lee, Tr. 10997). The volume production for Micron's 128 meg SDRAM part was also approximately 900 million units. (*Id.* at 10998). The 256 meg SDRAM, which started its life cycle in 2000, has already reached a volume production level of approximately 400 million units. (*Id.*).

1031. There would have been a reduction in good die yield because of the considerable amount of critical die area added by the additional input/output circuitry. (Geilhufe, Tr. 9607).

Response to Finding No. 1031: This proposed finding is unreliable because the methodology that Mr. Geilhufe used to analyze the costs of alternative technologies is based on inaccurate assumptions, not the appropriate methodology to rely on to determine the viability of alternative technologies in this case, and more generally unreliable for the reasons set forth in CCRF 837 and 853.

Furthermore, this proposed finding is incomplete because it fails to take into consideration this proposal's advantages such as retaining the single edge clocking design. (Jacob, Tr. 5429). The power of the DRAM would also go down because slower data pins could be used. (*Id.*).

1032. There would have been additional packaging costs associated with a more sophisticated and packaging technology known as a "ball grid array," which would have been required by the addition of 16 input/outputs. (Geilhufe, Tr. 9607-08).

Response to Finding No. 1032: The statement in this proposed finding that "there would have been additional packaging costs associated with a more sophisticated and packaging technology known as a 'ball grid array,' which would have been required by the addition of 16 input/outputs is not supported by the cited testimony." Mr. Geilhufe simply assumed that such a package would be required. Furthermore, this assumption is not supported by substantial record

evidence, rendering Mr. Geilhufe 's opinion unreliable. During the course of this work, Mr. Geilhufe did not consult with DRAM engineers or manufacturers to confirm whether his understanding that increasing the DRAM width would require "ball grid array" packaging was correct. (Geilhufe, Tr. 9623 (never consulted with JEDEC members), 9666-67 (never attempted to verify his numbers with DRAM manufacturers)).

1033. The alternative of increasing the number of pins on the DRAM, assuming that the data width would be doubled from 16 to 32, would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: $250,000 increase in product design costs; five cent per unit cost increase due to reduced good die yield; 25 cent per unit increase in packaging costs. (Geilhufe, Tr. 9562-64, 9607-08).

Response to Finding No. 1033: The proposed finding is unreliable because the methodology that Mr. Geilhufe used to reach his conclusions about the costs of alternative technologies was unreliable and irrelevant for the reasons set forth in CCRF 1030.

1034. The net increase in variable costs for the alternative of increasing the number of pins on the DRAM is, therefore, approximately 30 cents per unit. The total cost increase is approximately 31 cents per unit, calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9579).

Response to Finding No. 1034: The proposed finding is inaccurate and unreliable for the reasons set forth in CCRF 1030.

(4) Increasing the Number of Pins on the Module Was Not a Viable Alternative.

1035. Professor Jacob's proposed alternative of increasing the number of pins per module would not change the single data rate DRAM at all but would achieve the desired bandwidth by adding data pins to the module. (Jacob, Tr. 5431).

Response to Finding No. 1035: Complaint Counsel has no specific response to this finding.

1036. Complaint Counsel did not meet their burden of showing that increasing the number of pins per module was a viable alternative to dual-edge clocking in DDR SDRAMs.

Response to Finding No. 1036: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs.

Furthermore, RPF 1036 is contrary to the weight of the evidence that indicates that increasing pins on the module was a viable alternative. (CCFF 2356-2360).

1037. To the contrary, the evidence in the record shows that increasing the number of pins per module was not a viable alternative to dual-edge clocking in DDR SDRAMs, because it would be significantly costlier and would be unavailable in certain applications.

Response to Finding No. 1037: The statement in RPF 1037 lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs.

Furthermore, this proposed finding ignores substantial evidence in the record that of advantages to increasing the number of pins on the module in order to double the data rate. (Jacob, Tr. 5431-32). It would have been a "far cheaper design to build and test." (*Id.*) Compared to DDR SDRAM, noise and power levels would have been reduced. (*Id.*). (CCFF 2360).

1038. Professor McAfee testified that this alternative is *not* commercially viable. (McAfee, Tr. 7378).

Response to Finding No. 1038: This proposed finding is incomplete because it omits the fact that Dr. McAfee acknowledged, in his testimony, that there was some evidence to the contrary. (McAfee, Tr. 7378 ("There is some contrary evidence to that, although the evidence is recent and in fact involves a graphics design, a graphics card designer.")). He testified that Nvidia had doubled the data bus width. (*Id.*; *see* DX0198 ("But data bus has been doubled in recent years by Nvidia")).

1039. This alternative would require 128 wires on the motherboard and 128 pins on the memory controller. (Jacob, Tr. 5432-33).

Response to Finding No. 1039: This proposed finding is incomplete because it omits additional testimony from Dr. Jacob to the effect that while this alternative may increase the cost of the memory controller and motherboard, it would not necessarily increase the cost of the memory module. (Jacob, Tr. 5433). It also ignores the advantages that are associated with this alternative. (CCFF 2360).

1040. This alternative would be expensive because of the extra pins and wires required. (Soderman, Tr. 9392-93).

Response to Finding No. 1040: The statement in RPF 1040 is incomplete because it fails to take into consideration the cost savings associated with the alternative's advantages. The DRAM mechanism is simpler (Jacob, Tr. 5432 ("[Y]ou don't have to use a dual-edged clock, you don't have to have the DRAM pins transitioning at twice the rate, so it's a far simpler design, it's a far cheaper design to build and test. And -- so yes, the noise and the energy levels are reduced compared to a DDR part.")).

1041. This alternative would not be available in all applications because many applications do not use modules at all but, rather, have the DRAM soldered directly onto the motherboard. (Soderman, Tr. 9390-91; CX 2833; Wagner, Tr 3871-72).

Response to Finding No. 1041: This proposed finding is not supported by the cited evidence. First, Dr. Soderman's testimony related to the alternative of interleaving banks on the module, and not the alternative of increasing the number of pins on the module. Second, Mr. Wagner's testimony, does not support the proposition because he testified only that some applications do not use the kind of memory modules referred to as DIMMs. (Wagner, Tr. 3871-72). Graphics applications use graphics cards, which house a graphic chip and memory and power components. (*Id.* 3871-72). The mobile market uses a MAP, which is a "little memory graphics module." (*Id.* 3872).

(5) Doubling the Clock Frequency Was Not a Viable Alternative.

1042. In Professor Jacob's proposed alternative of doubling the clock frequency, rather than using both the rising and falling edges of a clock, only a single edge of a clock running at twice the frequency would be used to achieve the same bandwidth. (Jacob, Tr. 5433-34).

Response to Finding No. 1042: Complaint Counsel has no specific response to this proposed finding.

1043. Complaint Counsel did not meet their burden of showing that doubling the clock frequency was a viable alternative to dual-edge clocking in DDR SDRAMs.

Response to Finding No. 1043: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (CCFF 2324-2343).

1044. To the contrary, the evidence in the record shows that doubling the clock frequency was not a viable alternative to dual-edge clocking in DDR SDRAMs, because it would be significantly costlier, in addition to being difficult to implement and having performance problems.

Response to Finding No. 1044: This proposed finding lacks any reference in the record. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (*See* CCFF 2324-43 (Complaint Counsel's findings which support the conclusion that a single edge clock with double clock frequency was a viable alternative)).

PUBLIC

UNITED STATES OF AMERICA
BEFORE FEDERAL TRADE COMMISSION

In the Matter of RAMBUS INCORPORATED, a corporation.	Docket No. 9302

COMPLAINT COUNSEL'S REPLY TO RESPONDENT'S PROPOSED FINDINGS OF FACT

Volume III

CCRF 1045 - 1618

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Dated: September 29, 2003

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Volume III

1045. This alternative would require a clock signal that transitions at twice the rate of present systems and would, therefore, burn twice as much power as present systems. (Jacob, Tr. 5434-35).

Response to Finding No. 1045: This proposed finding ignores substantial evidence in the record that DRAM systems can accommodate higher frequency signals. In DDR SDRAM, for example, the command bus currently uses the single edge of the system clock. (JX0057 at 5 (JESD 79 states that "Commands entered on each positive CK edge.")). Furthermore, there are DDR SDRAMs that use clock chips running at speeds up to 500 MHz (CCFF 2329), which means that for those parts the command use the single edge of a 500 MHz clock chip.

Furthermore, this proposed finding ignores the evidence in the record that indicates that what is or is not considered a very high speed signal changes over time. (Kellogg, Tr. 5182). In the 1996-1997 time frame, signals that traveled at speeds of greater than or equal to 533 MHz were

considered "very high speed signals." (Kellogg, Tr. 5182-83). Today, signals that are greater than or equal to 2.5 GHz are considered to be very high. (*Id.*).

1046. This alternative would cause clock distribution problems, because routing the clock signal through the DIMM to the various DRAMs is a critical task that becomes much more difficult at higher frequencies. (Soderman, Tr. 9393-94).

Response to Finding No. 1046: This proposed finding is contrary to the weight of the evidence which indicates that double the clock frequency would not cause clock distribution problems. (Lee, Tr. 11039-40; *see also* CCFF 2336-2337).

1047. This alternative would also lead to increased electromagnetic radiation from the higher frequency clock. (Soderman, Tr. 9395). Both DRAM manufacturers and systems companies are very careful about the amount of electromagnetic radiation generated because it can interfere with other circuitry and because there are strict FCC guidelines as to how much such radiation is permissible. (*Id.*).

Response to Finding No. 1047: This proposed finding is unreliable because Dr. Soderman has no experience with FCC guidelines. (*See* CCFF 2340 (Soderman is not an expert in the FCC's regulation of electromagnetic interference, nor does he have any personal experience with trying to comply with FCC guidelines)).

1048. Mark Kellogg of IBM testified that at the time that JEDEC was considering using dual-edged clocking in DDR SDRAMs, the "predominant disadvantage" of using a higher frequency clock was "electromagnetic interference, radiation, the fact that fast pulses tend to radiate. And we've constantly been concerned, and at that time was no different, about our ability to distribute very high-speed signals throughout a system." (Kellogg, Tr. 5182).

Response to Finding No. 1048: This proposed finding is incomplete because it omits testimony be Mr. Kellogg that when he described "concerns" about distributing "very high-speed signals," he was referring to a clock speed of 533 MHz, far in excess of the clock speeds under consideration in 1996. (Kellogg, Tr. 5182). Furthermore, Mr. Kellogg also testified that the concerns about EMI diminish over time as the industry gets better at dealing with the problems. (Kellogg, Tr. 5183 ("We're not worried about 500 anymore. Now we're worried about 5 – two and a half gigahertz. We get smarter over time.")).

1049. In July 1997, Texas Instruments made a proposal involving a high speed single-edge clock (CX 371 at 2-3; Lee, Tr. 6710-12). Terry Lee of Micron wrote the following in an e-mail about the Texas Instruments proposal: "A single frequency clock is not practical. There is no real support yet for the higher frequency clock idea yet." (Lee, Tr. 11039, 11087-89).

Response to Finding No. 1049: This proposed finding is incomplete and misleading. This proposed finding is incomplete because it ignores testimony in the record by Mr. Lee regarding this document. As Mr. Lee testified at trial, in evaluating TI's proposal in 1997, he assumed that there would have been no accompanying change to the existing bus topology. (Lee, Tr. 11088, 11089). Therefore, what Mr. Lee meant by his statement in 1997 was that he did not believe a single frequency clock was practical in light of the existing bus topology or infrastructure. (*Id.* 11088).

Texas Instruments ("TI") proposed two different implementations of a single edged clock with double clock frequency. (CX0371 at 3; *see also* CCFF 2333). One of the proposed implementations called for use of a high speed clock throughout the entire system. (CCFF 2333). The other implementation called for the use of an on-chip clock frequency doubler to double the clock speed of the external clock signal. (*Id.*). As Mr. Lee further clarified at trial, TI's proposal to use an on-chip clock frequency doubler was technically feasible. (Lee, Tr. 6713). TI's proposal to run a high speed clock through the entire system was technically feasible at well but would have required "changes to the bus topology to make it work at the data rates [TI] wanted to make it work at."(Lee, Tr. 6713).

1050. In September 2000, Micron proposed using a double frequency, single-edge clock in DDR2. (CX 2769 at 13; Lee, Tr. 6795-98).

Response to Finding No. 1050: Complaint Counsel has no specific response to this proposed finding.

1051. As late as November 2000, JEDEC was considering using a single data rate clock in DDR2. In an e-mail dated November 29, 2000, Terry Lee of Micron circulated a summary of a conference call regarding "clocking issues" in DDR2. (CX 426). The conference call included

representatives of ATI, Micron, Hewlett-Packard, IBM, Intel, Mitsubishi, AMD, Texas Instruments, and others. (CX 426 at 2-4). The summary of the conference call includes the following statement:

> "Discussion on single data rate clock vs. double data rate clock
> Fundamentally question is that is single data rate clock possible?
> Micron believes that SDR has some advantages as it gets ride [sic] of duty cycle issue, it has old prior art, and the inherent bandwidth is better with write than read . . . .
> In general, everybody agreed that SDR clock is ok provided that it works."

(CX 426 at 4). The conference call participants ultimately concluded that "single data rate clock is preferred provided that we can make it work." (*Id.*).

Response to Finding No. 1051: Complaint Counsel has no specific response to this proposed finding.

1052. DDR2 SDRAMs use dual edge clocking. (RX 2099-14 at 3; RX 2099-39 at 5-6).

Response to Finding No. 1052: This proposed finding is misleading to the extent that it suggests, in light of the prior two proposed findings, that JEDEC could not make a single data rate clock work for DDR II SDRAM. There is no evidence in the record to support that JEDEC could not have made a single data rate clock work for DDR II SDRAM. To the contrary, the weight of the evidence in the record indicates that a single edge clock with double clock frequency was viable. (*See* CCFF 2325-2343).

This proposed finding ignores substantial evidence in the record that the industry was locked in to dual-edged clocking by the end of 2000, and that was the cause of JEDEC's decision to continue to use dual edged clocking for DDR II SDRAM. (*See* CCFF 3256-3261).

1053. The alternative of doubling the clock frequency would have resulted in increased costs.

Response to Finding No. 1053: This proposed finding lacks any reference in the record. Complaint Counsel submits that this proposed finding should be disregarded pursuant to

Chicago Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, it is contrary to the weight of the evidence that indicates that there were no significant costs associated with using a single edge clock with double clock frequency. (*See* CCFF 2327-2331, 2336-2343).

1054. There would have been additional design costs associated with additional circuitry required for the faster clock. (Geilhufe, Tr. 9608-9).

Response to Finding No. 1054: This proposed finding is incomplete because it omits testimony by Mr. Geilhufe that he believed that the additional design cost for this alternative was only $100,000 for the entire DRAM production run. (Geilhufe, 9608-9609).

Furthermore, this proposed finding is unreliable because Mr. Geilhufe's methodology to evaluate the costs associated with proposed alternatives was irrelevant and unreliable for the reasons set forth in CCRF 837.

1055. There would have been additional final testing costs associated with testing involving a clock that is running at the speed of current technology. This would have been a significant step up in testing that would have required changes in the test equipment and would have lowered yield. (Geilhufe, Tr. 9609).

Response to Finding No. 1055: This proposed finding is unreliable because Mr. Geilhufe's methodology to evaluate the costs associated with proposed alternatives was irrelevant and unreliable for the reasons set forth in CCRF 837.

1056. To distribute a double frequency clock on the DIMM would have required an on-DIMM clock. (Geilhufe, Tr. 9609). At the required frequency, that clock would have cost approximately $3.80. Because the cost of a clock is a function of frequency, such a clock could cost as much as $7 to $8 dollar for the highest frequency parts and much less for lower frequencies. (Geilhufe, Tr. 9609-10).

Response to Finding No. 1056: Mr. Geilhufe's opinion regarding the cost of this alternative is unreliable because it is based on the assumption that a PLL-type chip would be required on the module in order to implement this alternative. (Geilhufe, Tr. 9715-9716). That

assumption is contrary to substantial evidence in the record. In particular, in 1997, Texas Instruments made a proposal to JEDEC to use a fast single edge clock. (CCFF 2333-2335). JEDEC members did not understand there to be clock distribution problems with this proposal despite the fact that the proposal did not include any clock circuitry or DLL on the module to assist in clock distribution. (Lee, Tr. 11039-11040).

Furthermore, this proposed finding ignores the weight of the evidence that Mr. Geilhufe's cost estimates for the on-DIMM clock circuitry that he assumed would required in order to implement a higher frequency clock were inaccurate. (*See* CCFF 2342-2343). Mr. Geilhufe testified that he based his cost estimates on the cost of on-DIMM PLL/DLL circuits that were currently available. (Geilhufe, Tr. 9609-10). The weight of the evidence indicates, however, that the cost of on-DIMM PLL/DLL circuits is substantially less than $3.80. (*See* CCFF 2343).

Micron currently pays roughly per unit for the PLLs it uses on its registered DIMMs. (Lee, Tr. 11179, *in camera*).

Mr. Goodman of Kentron testified that a standard on-DIMM PLL generally costs around $1. (Goodman, Tr. 6048-49).

1057. The alternative of doubling the clock frequency would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: $100,000 increase in product design costs; four cent per unit cost increase due to higher speed final testing; $3.80 per module for an on-module clock. (Geilhufe, Tr. 9562-64, 9608-10).

Response to Finding No. 1057: This proposed finding is unreliable for the reasons described in CCRF 1056.

Furthermore, the product design costs estimate is unreliable because it is based on an inaccurate assumption that volume production for a first-tier manufacturer like Samsung, Infineon, or Micron, was approximately 20 million units for a product that was well into its life cycle.

(Geilhufe, Tr. 9562, 9726). The weight of the evidence is that the volume production level for a particular part is substantially higher than 20 million units. The volume production for Micron's 64 meg SDRAM, including shrinks, was approximately 900 million units. (Lee, Tr. 10997). The volume production for Micron's 128 meg SDRAM part was also approximately 900 million units. (*Id.* 10998). The 256 meg SDRAM, which started it's life cycle in 2000, has already reached a volume production level of approximately 400 million units. (*Id.*).

Furthermore, this proposed finding is incomplete because it omits testimony by Mr. Geilhufe that the costs of all of the alternatives could fall over time due to further die shrinks. (Geilhufe, Tr. 9726 ("It's possible that there are further shrinks, but I -- I assumed that 20 million units could be built off that one design effort.")).

Furthermore, the variable per unit cost estimates are unreliable for the reasons set forth in CCRF 837.

1058. The net increase in variable costs for the alternative of doubling the clock frequency is approximately 28 cents per unit, obtained by dividing the "per module" costs by 16 corresponding to the number of DRAMs on a DIMM and adding this to the other variable costs. (Geilhufe, Tr. 9610). Since the increase in fixed costs is relatively small, the total cost increase, calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs, is also approximately 28 cents per unit.

Response to Finding No. 1058: This proposed finding is unreliable because the methodology that Mr. Geilhufe used to analyze the costs of alternative technologies is based on inaccurate assumptions, is not the appropriate methodology to rely on to determine the viability of alternative technologies in this case, and is more generally unreliable for the reasons set forth in CCRF 837 and CCRF 1057.

(6) Using Simultaneous Bidirectional I/O Drivers Was Not a Viable Alternative.

1059. Professor Jacob's proposed alternative of using simultaneous bidirectional input/output drivers involves a signaling scheme that allows read data and write data to exist on the bus simultaneously, potentially increasing bandwidth. (Jacob, Tr. 5435-36).

Response to Finding No. 1059: Complaint Counsel has no specific response to this proposed finding.

1060. Complaint Counsel did not meet their burden of showing that using simultaneous bidirectional I/O drivers was a viable alternative to dual-edge clocking in DDR SDRAMs.

Response to Finding No. 1060: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (*See* 2361-2362 (Complaint Counsel's findings which support the conclusion that simultaneous bidirectional I/O was a viable alternative)).

1061. To the contrary, the evidence in the record shows that using simultaneous bidirectional I/O drivers was not a viable alternative to dual-edge clocking in DDR SDRAMs, because it would be very costly and difficult, if not impossible, to implement and would, in any event, not provide the performance of dual-edge clocking.

Response to Finding No. 1061: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is incomplete because it omits the potential advantages associated with using simultaneous bidirectional I/O. (*See* CCFF 2361 (could improve bus performance) and 2362 (would not increase the power consumption of the clock)).

1062. Professor McAfee did not testify that simultaneous bidirectional I/O drivers was a commercially viable alternative. (McAfee, Tr. 7376-81).

Response to Finding No. 1062: This proposed finding is misleading because it is also true that Professor McAfee did not testify that this alternative was not commercially viable. (McAfee, Tr. 7376-81; *see also* DX0200). For a more complete discussion of the evidence in support of its commercial viability, refer to CCFF 2361-2364.

1063. Simultaneous bidirectional input/output drivers involve a more complex driver design. (Jacob, Tr. 5437).

Response to Finding No. 1063: This proposed finding is incomplete because it omits the evidence in the record that indicate the advantages associated with using simultaneous bidirectional I/O. (*See* CCFF 2361 (could improve bus performance) and 2362 (would not increase the power consumption of the clock)).

1064. This complex technology has been used in point-to-point systems in which there is only a single transmitter and receiver sending data back and forth and the time it takes to get from one to the other is known and built into the design parameters of the system. (Soderman, Tr. 9396-97). It would not work in a high-speed, bus-based system, such as used in general purpose computers, where there might be differing numbers of DRAMs connected to the bus and the components do not know precisely when signals being sent will arrive at other components. (*Id.*).

Response to Finding No. 1064: Complaint Counsel does not disagree that this proposed finding accurately represents Dr. Soderman's testimony on the disadvantages associated with simultaneous bidirectional I/O.

1065. Even if this alternative could be made to work, the amount of additional bandwidth that would result from the ability to read from and write to the DRAM simultaneously would depend on the application and on whether the read and write operations are balanced. (Jacob, Tr. 5437). For most systems, which require a burst of data to be read from the DRAM prior to writing to the DRAM and for which the read and write operations are thus not balanced, this alternative would not achieve the same high bandwidth as DDR SDRAMs. (Soderman, Tr. 9397-98). In the extreme case of an application that only read data from the DRAM but never wrote data to the DRAM, no benefit whatsoever would be obtained. (*Id.*).

Response to Finding No. 1065: The first statement in this proposed finding is misleading to the extent that it suggests that Dr. Jacob questioned the feasibility of simultaneous

bidirectional I/O. To the contrary, Dr. Jacob testified that this proposed alternative was feasible for "most applications." (Jacob, Tr. 5437-38).

1066. Rambus has considered using simultaneous bidirectional input/output for high speed signaling. (Horowitz, Tr. 8563). It has never been used, however, because Rambus could not implement it in a way that was not likely to cause errors. (Horowitz, Tr. 8563-64).

Response to Finding No. 1066: This proposed finding is unreliable because the fact that Rambus was not able to implement simultaneous bidirectional I/O for an RDRAM architecture does not mean that it could not have been implemented in an SDRAM architecture. The two architectures are fundamentally different from each other. RDRAM uses a narrow bus in which command/address/data are multiplexed, while SDRAM uses a wide, parallel bus. (Lee, Tr. 6610-11; Rhoden, Tr. 401-02).

(7) Using Toggle Mode Was Not a Viable Alternative.

1067. By his proposed "toggle mode" alternative, Professor Jacob meant a DRAM like IBM's toggle mode DRAM. (Jacob, Tr. 5417).

Response to Finding No. 1067: Complaint Counsel has no specific response to this proposed finding.

1068. Complaint Counsel did not meet their burden of showing that toggle mode was a viable alternative to dual-edge clocking in DDR SDRAMs.

Response to Finding No. 1068: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (*See* 2363-2365 (Complaint Counsel's findings which support the conclusion that toggle mode DRAM was a viable alternative)).

1069. To the contrary, the evidence in the record shows that toggle mode was not a viable alternative to dual-edge clocking in DDR SDRAMs, because it would be significantly costlier and could not achieve the performance of DDR SDRAMs with dual-edge clocking.

Response to Finding No. 1069: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1070. IBM's "toggle mode" DRAM was an asynchronous design. (Jacob, Tr. 5608; Soderman, Tr. 9398; Sussman, Tr. 1472). Asynchronous technology could not achieve the same performance in a general purpose, bus type architecture as could synchronous technology. (Soderman, Tr. 9398-99)

Response to Finding No. 1070: The second sentence in this proposed finding ignores the substantial evidence in the record that indicates that asynchronous memory could have been improved incrementally just as synchronous memory has been. (*See, e.g.,* Williams, Tr. 829-30 (testifying that improvements could have been made to increase the performance of burst EDO devices)).

1071. An IBM researcher described IBM's toggle mode DRAM as "very big, very hot, and very nonstandard." (RX 2099-7 at 16; Soderman, Tr. 9399-9400). The researcher went on to conclude that "in the commodity market, these attributes are disastrous." (*Id.*).

Response to Finding No. 1071: This proposed finding ignores substantial evidence in the record that toggle mode was presented a number of times at JEDEC and there is no evidence that it was rejected for the reasons that the "IBM researcher" described. (CCFF 513-525). Instead, the weight of the evidence is that it was rejected in the early 1990s because it provided more performance than the industry needed at the time. (CCFF 578).

Furthermore, this proposed finding is incomplete because it omits the advantages to toggle mode DRAM that were identified in RX 2099-7. (RX 2099-7 at 16 (toggle mode DRAM was "very fast and very RAS-friendly")).

The second sentence in this proposed finding is misleading to the extent that it suggests that RX 2099-07 is evidence for the proposition that no implementation of toggle mode DRAM was viable as a commodity part. The quoted statement is far more limited in its potential application. RX 2099-07 acknowledges that there is more than one way to implement toggle mode DRAM. (*Id.* at 16). It states, only, that the design tradeoffs associated with the toggle mode DRAM that was implemented with a "low multibit piecepart architecture" made it unsuitable as a commodity part. (*Id.*).

1072. The toggle mode alternative would have resulted in increased costs.

Response to Finding No. 1072: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1073. The toggle mode alternative would have required signficant additional design costs. (Geilhufe, Tr. 9611).

Response to Finding No. 1073: This proposed finding is incomplete because it omits testimony by Mr. Geilhufe that he believed that the additional design cost for this alternative was only $250,000 for the entire DRAM production run. (Geilhufe, 9610-11). The reliability of his testimony is questionable for the reasons set forth in CCRF 837. (Refer also to CCFF 2108-2129).

1074. The good die yield would have been reduced due to additional critical die area. (Geilhufe, Tr. 9611).

Response to Finding No. 1074: The reliability of his testimony alone is questionable for the reasons set forth in CCRF 837. (Refer also to CCFF 2108-2129).

1075. The toggle mode alternative would also have required an additional pin for the data toggle signal. Because pins must be added in pairs, two additional pins would have to be added. (Geilhufe, Tr. 9611).

Response to Finding No. 1075: Complaint Counsel does not disagree that this proposed finding accurately represents Mr. Geilhufe's testimony on toggle mode DRAM.

1076. The toggle mode alternative would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million units, that is, a product that has already realized its cost improvement: $250,000 increase in product design costs; 10 cents cost increase per unit due to reduced good die yield; one cent cost increase per unit for an additional pin. (Geilhufe, Tr. 9562-64, 9610-11).

Response to Finding No. 1076: This cost analysis is unreliable for the reasons set forth in CCRF 837.

1077. The net increase in variable costs for the toggle mode alternative is, therefore, approximately 12 cents per unit. The total cost increase is approximately 13 cents per unit, calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9611-12).

Response to Finding No. 1077: This cost analysis is unreliable for the reasons set forth in CCRF 837.

b. On-chip DLL.

1078. Complaint Counsel has suggested, through Professor Jacob, the following possible alternatives to on-chip DLL in DDR SDRAMs:

(1) Put a DLL on the memory controller;
(2) Put a DLL on the module;
(3) Use a vernier method;
(4) Increase the number of pins on the DRAM;
(6) Rely on the DQS data strobe for timing.

(Jacob, Tr. 5443-5458).

Response to Finding No. 1078: This proposed finding represents a partial list of Dr. Jacob's proposed alternatives to on-chip DLL. That list omits that there was a seventh alternative to on-chip DLL. JEDEC could have adopted read clocks in order to avoid replicating DLL circuits on each DRAM chip. (Lee, Tr. 6664, 6666-67).

1079. The purpose of the on-chip DLL in DDR SDRAMs is to compensate for internal delays on the DRAM and thereby to remove uncertainty in the timing of the system. (Jacob, Tr. 5442-43; Soderman, Tr. 9404).

Response to Finding No. 1079: This proposed finding is vague and potentially misleading. The term "compensate" and the phrase "remove uncertainty in the timing of the system" are not defined in this proposed finding. Depending on their meaning this proposed finding may be misleading.

The weight of the evidence in the record is that JEDEC included on-chip DLL circuits in the DDR SDRAM standard to align the "data valid window" of each DRAM chip with the system clock. (Jacob, Tr. 5438-42; *see* DX0093; JX0029 at 17; Kellogg, Tr. 5145-55). The way that on-chip DLLs accomplish that goal is by comparing the signals inside of the DRAM, which experience delay, to the external clock signal and compensating for the disparity between the two signals. (Jacob, Tr. 5442-43). There is no record evidence that the DLL in the DRAM in DDR SDRAMs does anything else to "remove uncertainty in the timing of the system."

1080. This timing uncertainty varies from DRAM to DRAM because of differences in process, temperature and voltage. (Soderman, Tr. 9402-03).

Response to Finding No. 1080: This proposed finding is vague and potentially misleading. The phrase "timing uncertainty " is not defined in this proposed finding. Depending on its meaning this proposed finding may be misleading.

1081. The timing uncertainty compensated for by the DLL is more of a problem at high speeds because, as speeds increase, the window of time in which data is valid becomes smaller and the timing uncertainty reduces the size of the window even more. (Soderman, Tr. 9404-05).

Response to Finding No. 1081: This proposed finding is vague and potentially misleading. The phrase "timing uncertainty " is not defined in this proposed finding. Depending on its meaning this proposed finding may be misleading.

Furthermore, this proposed finding is incomplete because it omits the weight of the evidence in the record that indicates that it was not necessary for high speed operation to use DLLs in order to guarantee that the memory controller will capture data only during the data valid window. (*See* CCFF 2368-2380).

1082. At high enough bus speeds, a DLL or PLL on the DRAM to compensate for individual timing uncertainties is required for correct operation. (Soderman, Tr. 9401-05).

Response to Finding No. 1082: This proposed finding is contrary to the weight of the evidence that an on-chip PLL or DLL is not required for correct operation. (*See* CCFF 2368-2380).

The on-chip DLL in DDR SDRAM ensures that the system's memory controller can capture data sent by the DRAMs during the data valid window. (Jacob, Tr. 5442-43; Lee, Tr. 6662-63; Kellogg, Tr. 5145-55, 5161). Numerous mechanisms were available, at that time, besides on-chip PLL/DLL to accomplish that goal. (Jacob, Tr. 5443; Kellogg, Tr. 5154-55; *see* DX0059; CX2109 at 67-68 (based on internal discussions at Rambus, Davidow concluded that there were "many ways to improve performance" without using an on-chip DLL)).

1083. In the mid-1990s, DRAM engineers believed that a DLL or PLL on the DRAM would be necessary at future bus speeds. (RX 2099-29; RX 2099-13; Soderman, Tr. 9408-10).

Response to Finding No. 1083: This proposed finding is misleading because RX 2099-29 and RX 2099-13 do not support the proposition that engineers believed that a DLL or PLL on the DRAM "would be necessary at future bus speeds." Instead, they support the proposition

that several DRAM engineers, who assumed a design goal to minimize the time window between the clock and valid data, believed that a DLL or PLL on the DRAM should be used to run SDRAMs at speeds greater than 150 MHz. (RX 2099-29 at 1 ("To minimize the access time from the clock, Tac, the delay between the clock bond pad and the internal clock signal used in the output buffer must be minimized."); RX 2099-13 at 1 ("This paper describes the key technologies used in a 256-MB synchronous DRAM with a clock access time of 1 ns.")). As RX 2099-29 states, "The access time from the clock, Tac, is reduced by the use of a digital DLL." (RX 2099-29 at 1).

The weight of the evidence in the record indicates that, in 1996-1997, it was not necessary to minimize the time window between the clock and valid data. (*See* CCFF 2372). The only thing that was necessary, at this time, was to design a system that would guarantee that the memory controller would capture data during the data valid window. (*See* CCFF 2373).

1084. In a presentation on "Future SDRAM" at the March 1996 meeting of the JEDEC 42.3 subcommittee, Desi Rhoden presented a chart with columns representing clock speeds and rows representing certain features. (JX 31 at 64; Rhoden, Tr. 542-43). The chart indicates that "on-chip PLL/DLL" would be a "no" at 100 MHz, "maybe" at 150 MHz, and "yes" at 200 MHz and above. (*Id.*). Indeed, Mr. Rhoden testified that: "We discussed [on-chip PLL/DLL] at length inside of JEDEC, and I don't think we ever had any question whether we would use the technology. It was just a question of when." (Rhoden, Tr. 546).

Response to Finding No. 1084: This proposed finding is incomplete and misleading because it implies that Mr. Rhoden testified that an on-DRAM PLL or DLL was required. In fact, Mr. Rhoden testified that he did not believe that such circuitry was required. (Rhoden, Tr. 543-544 ("I was proposing that these would be the – a reasonable alternative at these particular speeds. I – I never would suggest that they would be required, certainly.")).

Furthermore, this proposed finding ignores substantial evidence in the record that there was substantial debate within JEDEC, in the 1996-1997 time frame, about whether or not to include on-chip PLLs or DLLs in future SDRAM standards. (*See* CCFF 2371-2373, 2378-2379). The weight

of the evidence indicates that there were two camps at JEDEC, one which wanted to rely on the bidirectional DQS strobe and one which did not. (*See* CCFF 2379; *see* also RX 1060 (suggesting that the position a company took with respect to on-chip DLL depended on whether or not the company was pro-strobe or against the strobe)). JEDEC eventually included both the strobe and on-chip DLL in an effort to "satisfice," or to allow the standard to accommodate those few companies who wanted to use DDR parts in applications that would not rely on the data strobe. (*See* CCFF 2650-2651; Lee, Tr. 6683 ("Our preference was still not to have [strobes], but our action was to – to go along with the committee in general with this compromise, because there was – because of these differences of opinion, it was causing some delay in the standardization process.")).

1085. In an e-mail dated November 18, 1997, Bill Gervais of Transmeta wrote that "a DLL must be onchip and enabled for the Intel spec." (RX 1060). In other words, an on-chip DLL was required to meet Intel's timing requirements.

Response to Finding No. 1085: This proposed finding is misleading because it fails to mention that Bill Gervasi was giving "[his] reading" of the Intel specification. In fact, the weight of the evidence is that the DLL has never been required as part of the "Intel spec" for DDR SDRAM. Neither dual-edged clocking, nor DLL on the DRAM are in the Intel Addendum to the JEDEC specification because both technologies are present in the JEDEC specification itself. (MacWilliams, Tr. 4917-18 ("So it's a base part of the DDR and we're not proposing to add it, we're not proposing to take it away or change it, so we wouldn't include it in the addendum.")). In fact, the only Intel employee who testified at trial regarding the need for an on-chip PLL or DLL, Pete MacWilliams, testified that Intel had been concerned that DLLs on the DRAM were "a very high risk item for DRAM vendors to put on the device." (MacWilliams, Tr. 4919). As a result, Intel studied the question of whether one was necessary and found and determined that one was not

necessarily required. (MacWilliams, Tr. 4919 ("We basically concluded that for the speeds that we're looking at that, which was DDR 200, we didn't need the DLL for the systems we were going to build. You know, we had a pretty good experienced group at the time that had built high-speed caches for our Pentium II and Pentium III processors up to 400 megahertz without DLLs in the memory devices, so we thought we can do the same for system memory if this was going to be a risky item for the DRAM vendors.")).

This proposed finding of fact is also incomplete because it omits additional written statements from Hans Wiggers of HP in the document, in which he proposed two ways to avoid the use of DLLs. (RX 1060 at 1 ("Yes I can make a large memory system work without a DLL. I just have to add a FIFO like structure to make sure the data is stable.")).

(1) Putting a DLL on the Memory Controller Was Not a Viable Alternative.

1086. Professor Jacob's proposed alternative of putting the DLL on the memory controller involves putting a DLL circuit on the memory controller rather than on each individual DRAM. (Jacob, Tr. 5445).

Response to Finding No. 1086: Complaint Counsel has no specific response to this proposed finding.

1087. Complaint Counsel did not meet their burden of showing that putting a DLL on the memory controller was a viable alternative to on-chip DLL in DDR SDRAMs.

Response to Finding No. 1087: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (*See* CCFF 2381-2384 (Complaint Counsel's findings which support the conclusion that using a DLL in the memory controller was a viable alternative)).

1088. To the contrary, the evidence in the record shows that putting a DLL on the memory controller was not a viable alternative to on-chip DLL in DDR SDRAMs, because it would not be sufficient for high speed performance.

Response to Finding No. 1088: This proposed finding lacks any reference in the record. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence which indicates that there were no significant performance penalties associated with using a DLL in the memory controller. (*See* CCFF 2381-2384).

1089. This alternative is not sufficient for high speed performance because a DLL on the controller will broadcast the same delayed clock to all of the DRAMs and, therefore, cannot compensate for timing differences between DRAMs. (Soderman, Tr. 9405-06).

Response to Finding No. 1089: This proposed finding is contrary to the weight of the evidence that indicates that JEDEC could have used a DLL or PLL in the memory controller in order to ensure valid data capture. (*See* CCFF 2382 (a finding that using DLL in the controller could eliminate outbound, internal, and return delays in the system), CCFF 2383 (identifying an advantage to using a DLL in the controller), and CCFF 2384 (showing that Samsung, in March 1996, proposed how JEDEC could use a PLL in the controller to ensure valid data capture and thereby avoid replicating PLL circuits in each DRAM)).

1090. Dr. Horowitz and other Rambus engineers have considered moving the DLLs off of the DRAMs and onto the memory controller on a number of occasions. (Horowitz, Tr. 8561-62). However, they determined that they were unable to meet the necessary timing requirements without a DLL on the DRAM. (*Id.*).

Response to Finding No. 1090: This proposed finding demonstrates that moving DLLs off of the DRAM was a reasonable solution in general. However, this proposed finding is unreliable as evidence to support the conclusion that using a DLL in the controller was not a viable alternative for use in DDR SDRAMs because Dr. Horowitz's testimony is only relevant to assess the question of whether the use of a DLL in the controller was viable for an RDRAM-based architecture. (Horowitz, Tr. 8561-62).

(2) Putting a DLL on the Module Was Not a Viable Alternative.

1091. Professor Jacob's proposed alternative of putting the DLL on the module involves putting an additional chip on the module containing either one or more DLL circuits rather than having a DLL on each individual DRAM. (Jacob, Tr. 5448-49).

Response to Finding No. 1091: Complaint Counsel has no specific response to this proposed finding.

1092. Complaint Counsel did not meet their burden of showing that putting a DLL on the module was a viable alternative to on-chip DLL in DDR SDRAMs.

Response to Finding No. 1092: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs.

Furthermore, RPF 1092 is contrary to the weight of the evidence . (CCFF 2385-2388).

1093. To the contrary, the evidence in the record shows that putting a DLL on the module was not a viable alternative to on-chip DLL in DDR SDRAMs, because it would be significantly costlier and difficult to implement.

Response to Finding No. 1093: This proposed finding lacks any reference to the record. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs.

This proposed finding is also contrary to the weight of the evidence which indicates that there are no significant costs or implementation difficulties associated with this alternative. (CCFF 2386-2388).

1094. At high speeds, a single DLL would be insufficient and a separate DLL would be required for each DRAM on the module. (Jacob, Tr. 5449; Soderman, Tr. 9406-07).

Response to Finding No. 1094: This proposed finding is incomplete and misleading because it omits Professor Jacob's testimony that, although it was possible that a separate DLL per DRAM might be required if "you envision going to much higher rates of speed," all of the DLLs could be placed on the same chip. (Jacob, Tr. 5449). Furthermore, Dr. Jacob testified that, at the rates of speed needed at the time this alternative would have been considered, only one DLL on the module was necessary to ensure that all DRAMs on a module are synchronized with the system clock. (Jacob, Tr. 5449).

1095. Professor Jacob's suggestion that multiple DLLs be put on a single chip would not solve the problem. A DLL on the DRAM could sense the DRAM's performance in order to compensate for timing uncertainties, while a DLL on a chip outside the DRAM would require significant extra circuitry on the DRAM to communicate with the DLL chip about the DRAMs performance. (Soderman, Tr. 9407). Such circuitry would be difficult and expensive to implement and would require extra traces on the module which would further increase the cost of the system. (Soderman, Tr. 9407-08).

Response to Finding No. 1095: This proposed finding is unreliable because it is premised on the unsupported assumption that it is necessary for a DLL to be able to "sense the DRAM's performance in order to compensate for timing uncertainties."

Furthermore, this proposed finding is contrary to the weight of the evidence which indicates that there are no significant costs associated with this alternative. (CCFF 2386-2388).

1096. Tom Landgraf of Cisco, formerly at Hewlett-Packard, testified that Hewlett-Packard was in favor of including an on-chip PLL or DLL in the DDR SDRAM standard because putting a PLL on the motherboard or module would have led to lower performance at higher cost. Mr. Landgraf explained:

> "One way to implement PLL is to put it on a – on the system, on the motherboard or on the memory module, and what we were suggesting, what we were in favor of doing was any time you can take a function which is on the motherboard that is common to a memory system, if you can incorporate that in the memory system itself, it reduces the overall cost of the system and also improves the performance of the system."

(Landgraf, Tr. 1709).

Response to Finding No. 1096: This proposed finding is misleading because the potential application of Mr. Langraf's testimony is limited to evaluating the cost impact that a system manufacturer, like HP, would perceive from moving the DLL to the module. Mr. Landgraf testified that he was in favor of on-chip PLL/DLL because requiring a PLL or DLL circuit to be on the motherboard or memory module, instead, would increase system-level costs. (Landgraf, Tr. 1709). His testimony has no bearing whatsoever on the costs that DRAM manufacturers would have associated with putting a DLL on the module. The weight of the evidence indicates that DRAM manufacturers likely would have perceived a decrease in costs associated with putting the DLL on the module because they would not longer have to replicate these circuits inside every DRAM chip. (Jacob, Tr. 5450 ("You eliminate the on-chip DLL from the DRAM, thereby reducing its power consumption, reducing its cost, reducing the design time.")).

Furthermore, this proposed finding is incomplete. Mr. Landgraf stresses the importance of being cost competitive in his testimony. (Landgraf, Tr. 1709-10). Directly after he gave this testimony, he added that intellectual property coverage was also an important consideration. ((Landgraf, Tr. 1710 ("Q. Now, you mentioned a number of factors in your response that HP was considering. Did Hewlett Packard consider whether or not there were patents or patent applications on dual edge clock when it was considering the DDR standard? A. If we knew about them, we would have -- we would have raised it as a consideration.")).

The weight of the evidence indicates that the valuation of on-chip DLL as a technology would have changed had Rambus disclosed the scope of its patent applications while JEDEC was still working on the standards. (CCFF 2101 (citing testimony from Sussman, Lee, Prince, Oh, Meyer, and Kellogg as support)).

1097. The alternative of putting a DLL on the module would have resulted in increased costs.

Response to Finding No. 1097: This proposed finding lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's Order on Post Trial Briefs.

This proposed finding is also contrary to the weight of the evidence which indicates that there are no significant costs associated with this alternative. (CCFF 2386-2388).

1098. The test time at wafer sort would have been decreased because the DLL on the DRAM would no longer have had to be tested. (Geilhufe, Tr. 9612-13).

Response to Finding No. 1098: This proposed finding is unreliable because the methodology that Mr. Geilhufe used to analyze the costs of alternative technologies is based on inaccurate assumptions, not the appropriate methodology to rely on to determine the viability of alternative technologies in this case, and more generally unreliable for the reasons set forth in CCRF 837 and 853.

1099. There would have been an increase in good die yield due to the decrease in critical die area resulting from removal of the DLL from the DRAM. (Geilhufe, Tr. 9613).

Response to Finding No. 1099: This proposed finding is unreliable because the methodology that Mr. Geilhufe used to analyze the costs of alternative technologies is based on inaccurate assumptions, not the appropriate methodology to rely on to determine the viability of alternative technologies in this case, and more generally unreliable for the reasons set forth in

CCRF 837 and 853. Mr. Geilhufe reviewed no evidence from this case relating to the costs of DRAM manufacturers for the good die yield cost element, from the relevant period other than the Peisl deposition. (Geilhufe, Tr. 9698).

1100. The cost of an on-DIMM DLL is a function of the frequencies supported. For the DLL required for DDR SDRAMs, it would have cost approximately $3.80. (Geilhufe, Tr. 9613).

Response to Finding No. 1100: The second statement in RPF 1100 is inaccurate and unreliable for the following reasons.

In arriving at his estimate of the costs for the on-DIMM DLL, Mr. Geilhufe never considered the cost of similar components on registered DIMMs. (Geilhufe, Tr. 9719). Mr. Geilhufe continued to use his cost estimate of $3.80 per on-DIMM DLL even though he reviewed evidence that indicated that similar components were used by other companies at $2. (CX2613 at 7; Geilhufe, Tr. 9718-719).

Furthermore, this proposed finding is contrary to the weight of the evidence. (CCFF 2387-2388). Terry Lee who supervises engineering and layout staff working on module design at Micron testified that his company uses on-DIMM PLLs for its registered DIMMs to redistribute the clock to all of the DRAMs on the module. (Lee, Tr. 11040-42). Micron currently pays roughly cents per unit for the PLLs it uses on its registered DIMMs. (Lee, Tr. 11179, *in camera*); *see also* Goodman, Tr. 6048-49 (a standard PLL generally costs around $1.00)). (CCFF 2388). This figure is far lower than Mr. Geilhufe's approximation.

1101. The alternative of putting the DLL on the module would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million units, that is, a product that has already realized its cost improvement: two cent cost decrease due to decreased test time at wafer sort; one cent cost decrease due to increased good die yield; $3.80 per module for an on-DIMM DLL. (Geilhufe, Tr. 9562-64, 9612-14).

Response to Finding No. 1101: This proposed finding is unreliable because the methodology that Mr. Geilhufe used to analyze the costs of alternative technologies is based on

inaccurate assumptions, not the appropriate methodology to rely on to determine the viability of alternative technologies in this case, and more generally unreliable for the reasons set forth in CCRF 837, 853, and 1100.

1102. These costs would lead to an approximate 21 cent increase in the cost per unit, calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run), dividing the "per module" costs by 16 corresponding to the number of DRAMs on a DIMM, and adding the resulting per unit fixed costs and per unit variable costs to the other variable costs. (Geilhufe, Tr. 9614). This 21-cent cost increase is a variable cost.

Response to Finding No. 1102: This proposed finding is unreliable because the methodology that Mr. Geilhufe used to analyze the costs of alternative technologies is based on inaccurate assumptions, not the appropriate methodology to rely on to determine the viability of alternative technologies in this case, and more generally unreliable for the reasons set forth in CCRF 837, 853, and 1100.

(3) Using a Vernier Method to Account for Skew Was Not a Viable Alternative.

1103. Professor Jacob proposed using a "vernier method" to "account for skew," that is timing uncertainties. (Jacob, Tr. 5444). A "vernier" is a circuit that provides a static delay, that is, it is a variable delay circuit that does not contain a feedback loop like a DLL for changing the size of the delay. (Jacob, Tr. 5450; Soderman, Tr. 9411).

Response to Finding No. 1103: Complaint Counsel has no specific response to this proposed finding.

1104. Complaint Counsel did not meet their burden of showing that using a vernier method was a viable alternative to on-chip DLL in DDR SDRAMs.

Response to Finding No. 1104: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (*See* CCFF 2389-2399 (Complaint Counsel's findings which support the conclusion that using vernier circuits was a viable alternative)).

1105. To the contrary, the evidence in the record shows that using a vernier method was not a viable alternative to on-chip DLL in DDR SDRAMs, because it would not be sufficient for high speed performance. Moreover, using a vernier method is not free of patent coverage.

Response to Finding No. 1105: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence that indicates that no significant costs were associated with this alternative. (*See* CCFF 2390-2391 (identifying the advantages of using vernier circuits), CCFF 2393-2397 (there was support for the use of vernier circuits as a commercially and technically viable solution)).

1106. Unlike a DLL, Professor Jacob's proposed alternative of using a vernier method to account for skew would not account for dynamic changes in skew caused by, for example, fluctuations in temperature or voltage without recalibration, that is adjustment of the amount of the delay, by the memory controller. (Jacob, Tr. 5452-53).

Response to Finding No. 1106: This proposed finding is incomplete because it omits that fact that Dr. Jacob also testified that the use of vernier circuits with periodic recalibration would allow the system to compensate for dynamic changes in skew caused by temperature and voltage fluctuations. (Jacob, Tr. 5453).

1107. These temperature and voltage changes can occur on the order of milliseconds and microseconds, respectively, and without the DLL's feedback loop the vernier will not be able to take these fluctuations into account and minimize the timing uncertainty. (Soderman, Tr. 9411-12).

Response to Finding No. 1107: This proposed finding is inaccurate because the weight of the evidence indicates that periodically recalibrating vernier circuits would have

compensated for temperature and voltage fluctuations that cause skew in a memory system. (Jacob, Tr. 5453).

Furthermore, this proposed finding is incomplete because it omits the testimony of engineers in the industry who had experience using vernier circuits and considered them to be a technically and commercially viable alternative to the use of on-chip DLLs. (*See* CCFF 2394-2397). Some IBM systems were using memory busses with vernier circuits instead of DLL circuits. (Kellogg, Tr. 5161-62). For example, the z900 memory card had a vernier circuit. (*Id.*). Mr. Kellogg believed that vernier circuits were the optimal solution to the data capture issue. (Kellogg, Tr. 5168).

1108. Moreover, the recalibration necessary to make the vernier more precise would consume bus bandwidth, because the recalibration information would have to be transmitted over the bus from the controller to the DRAM, and would make the system less efficient. (Soderman, Tr. 9412).

Response to Finding No. 1108: This proposed finding is unreliable because the amount of bandwidth "consumed" by recalibration of the verniers is not specified, nor is the importance of that consumption described in either this finding or Dr. Soderman's testimony.

Furthermore, this proposed finding is contrary to the evidence that there were not significant costs associated with the use of vernier circuits to ensure valid data capture. (*See* CCFF 2393-2398).

1109. The SyncLink consortium tried to design a chip, called an "SLDRAM," using verniers alone without PLLs or DLLs on the DRAM. (RX 2099-43 at 158; Soderman, Tr. 9412-14).

Response to Finding No. 1109: This proposed finding is potentially misleading because it implies that the Synclink consortium failed to design a DRAM using verniers alone without the use of PLLs or DLLs on the DRAM. However, none of the evidence cited in this

finding supports that inference. RX2099-43 in particular contradicts that inference as it clearly states that "no PLL or DLL required in SL-DRAM components." (RX2099-43 at 158).

1110. Ultimately, however, SyncLink's SLDRAM chip did use a DLL in each DRAM, in addition to the vernier, in order "to make that timing a little bit more accurate." (Jacob, Tr. 5620-21; RX 2099-11; Soderman, Tr. 9414-15). '

Response to Finding No. 1110: This proposed finding is misleading because it implies that the SyncLink consortium failed to design a DRAM using verniers alone without the use of PLLs or DLLs on the DRAM. However, none of the evidence cited in this finding supports that inference. In particular, Dr. Soderman simply noted that an article (RX 2099-11) showed the use of a DLL on the SL-DRAM. (Soderman, Tr. 9414).

Furthermore, this proposed finding is incomplete and misleading because it implies that Professor Jacob testified that the DLL used on the SL-DRAM was for the same purpose it is used in DDR SDRAM. In fact, Professor Jacob testified his understanding was the opposite: that the vernier was being used instead of the DLL in SL-DRAM chips and the DLL on SL-DRAM chips was used for a different purpose than it is in DDR SDRAM. (Jacob, Tr. 5620-5621 ("QUESTION: And what did Mr. Lee tell you about the use of verniers in DLLs and SLDRAMs? ANSWER: He said that contrary to what Soderman had said, that the SLDRAM part that was built did use verniers. Soderman had said that they abandoned the use of a vernier in favor of a DLL and therefore that the vernier is a useless mechanism. Lee said that the verniers were used at both the controller side and the DRAM side to capture data. They were used to, quote-unquote, level the bus so that all DRAMs responded to transactions at nominally the same time so that even though a nearby DRAM would receive a request sooner than a faraway DRAM, the nearby DRAM would delay its response so that it appeared -- so that it would write things out onto the bus at the same time that the further-away DRAM would. And so this static calculation was done, and the vernier was set in each of the DRAMs, and that the DLL was used to make that timing a little bit more

accurate, and that the verniers were used to delay the data with respect to the strobe so that the strobe captured the data. So the verniers, according to Mr. Lee, were used in the capture of data and not the DLL. That's my recollection.")).

Furthermore, this proposed finding does not support the conclusion that vernier circuits were not a viable alternative to on-chip DLLs in DDR SDRAMs. SLDRAMs, which were packet-based, and DDR SDRAMs, which were not, were very different architectures. (*See* CCFF 1504, 1508, 1513). A proposed finding, therefore, which states that the SL-DRAM Consortium added on-chip DLL does not support a conclusion that DDR SDRAMs also require a DLL.

Furthermore, this proposed finding is contrary to the weight of the evidence that the SLDRAM Consortium relied on vernier circuits to ensure valid data capture. (Lee, Tr. 11044; *see* CCFF 2399). The Consortium did not add DLL circuits to assist in data capture. (*Id.* 11046). In SDRAM, the on-chip DLL circuits served another purpose entirely. (*Id.*).

1111. In addition, the use of verniers is covered by U.S. Patent no. 6,115,318, "Clock Vernier Adjustment" assigned to Micron Technology (RX 1701), and as used in SLDRAM by U.S. Patent no. 5,917,760, "Deskewing Data Signals in a Memory System, assigned to SLDRAM, Inc. (RX 1479). Professor Jacob did not consider these patents when he proposed the use of verniers as an alternative. (Jacob, Tr. 5622-23).

Response to Finding No. 1111: The statement in this proposed finding that "the use of verniers is covered by U.S. Patent no. 6,115,318, "Clock Vernier Adjustment" assigned to Micron Technology (RX 1701), and as used in SLDRAM by U.S. Patent no. 5,917,760, "Deskewing Data Signals in a Memory System, assigned to SLDRAM, Inc." is not supported by any evidence in the record. Respondent did not present expert testimony to support a proposed finding that either U.S. Patent No.6,115,318 (the '318 patent) or U.S. Patent No. 5,917,760 (the '760 patent) covers the use of vernier circuits. (Soderman, Tr. 9410-15; *see* DX291 (Dr. Soderman's testimony on vernier circuits does not identify infringement of a Micron patent as a disadvantage); Geilhufe, Tr. 9612-14 (Mr. Geilhufe's testimony on alternatives to on-chip DLL

does not mention the possible infringement of a Micron patent)). Furthermore, Respondent did not present any other evidence that Rambus believed it could cover the concept of interleaving on-chip banks or that Rambus was trying to broaden its patents to capture that concept.

The interpretation of patent claims involving complex technology, and the comparison of a product to that claim, cannot be properly resolved without the development of evidence, including expert testimony, before the finder of fact. *See NeoMagic Corp. v. Trident Microsystems, Inc.*, 287 F.3d 1062, 1074 (Fed. Cir. 2002) ("given the complex technology involved in this case, we think that this matter [interpretation of a claim to a DRAM memory chip controller] can only be resolved by further evidentiary hearings, including expert testimony, before the district court.").

A determination that a patent claim covers a product is a two step process. The first step requires that the court interpret the patent claim as it would be understood by a person of ordinary skill in the art. (Fliesler, Tr. 8893). RPF 1111 cites no expert testimony or other evidence to establish the proper interpretation of the patent claims.

The second step requires a factual determination that each element of the properly interpreted claim is present in the product. (Nusbaum, Tr. 1565-66). RPF 1111 cites no expert testimony or other evidence to establish that each element of any claim of this patent correspond to elements of the proposed alternative.

(4) Increasing the Number of Pins on the DRAM Was Not a Viable Alternative.

1112. Professor Jacob's proposed alternative of achieving high bandwidth using more DRAM pins and not clock frequency is the same as the alternative he proposed of using more pins per DRAM rather than using dual-edge clocking. (Jacob, Tr. 5453-54).

Response to Finding No. 1112: Complaint Counsel has not specific response to this proposed finding.

1113. This alternative suffers from the same infirmities and the same additional costs as the same alternative when it was proposed as an alternative for dual-edge clocking. (Geilhufe, Tr. 9612).

Response to Finding No. 1113: This proposed finding is contrary to the weight of the evidence for the reasons previously set forth in response to Respondent's proposed findings contesting the viability of increasing DRAM width in order to double the data rate. (*See* CCRF 1023-34).

1114. Professor McAfee did not testify that this was a commercially viable alternative. (McAfee, Tr. 7385).

Response to Finding No. 1114: This proposed finding is misleading because Professor McAfee did not testify regarding whether increasing the number of pins on the DRAM was not commercially viable. Instead, he testified that he did not make a determination one way or another as to whether or not this alternative was commercially viable. (McAfee, Tr. 7385).

(5) Relying on the DQS Data Strobe Was Not a Viable Alternative.

1115. Professor Jacob's proposed alternative of relying on the DQS data strobe involves using the DQS signal that already exists in DDR SDRAMs to time the data which would no longer necessarily be aligned with the system clock. (Jacob, Tr. 5456-57).

Response to Finding No. 1115: This proposed finding is incomplete because it omits Dr. Jacob's testimony that reliance on the DQS strobe provides an alternative method of alignment for the purpose of valid data capture. (Jacob, Tr. 5457).

1116. Complaint Counsel did not meet their burden of showing that relying on the DQS data strobe was a viable alternative to on-chip DLL in DDR SDRAMs.

Response to Finding No. 1116: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (*See* CCFF 2403-2410 (Complaint Counsel's findings which support the conclusion that relying on the DQS strobe was a viable alternative)).

1117. To the contrary, the evidence in the record shows that relying on the DQS data strobe was not a viable alternative to on-chip DLL in DDR SDRAMs, because it would not be sufficient for high speed performance.

Response to Finding No. 1117: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (*See* CCFF 2403-2410 (Complaint Counsel's findings which support the conclusion that relying on the DQS strobe was a viable alternative)).

1118. Using the DQS signal without the DLL is not sufficient for high speed performance. (Soderman, Tr. 9415-16).

Response to Finding No. 1118: This proposed finding of fact is contrary to the weight of the evidence which indicates that a majority of JEDEC members, in the 1996-1997 time frame, believed that relying on the DQS strobe was sufficient for high speed performance. (*See* CCFF 2410). The only reason that JEDEC included on-chip DLLs in addition to the DQS strobe was as part of a compromise to accommodate the interest of a few companies who did no want to rely on the DQS strobe. (*Id.*).

1119. DDR SDRAMs already have the DQS signal available, but DDR SDRAMs also contain a DLL for accurate operation, even though DRAM manufacturers incur a cost to put the DLL on the DRAM. (Soderman, Tr. 9416-17).

Response to Finding No. 1119: This proposed finding is unreliable to support the conclusion that relying on the DQS strobe was not a viable alternative to on-chip DLL for the reasons set forth in CCRF 1118.

1120. DDR2 SDRAMs have DQS data strobe signals as well as on-chip DLLs, even though DRAM manufacturers incur a cost to put the DLL on the DRAM. (RX 2099-14 at 3; RX 2099-39 at 5, 7).

Response to Finding No. 1120: This proposed finding is incomplete because it omits the substantial evidence in the record that indicates that "lock-in" was the cause of JEDEC's decision to continue to use on-chip DLL for DDR II SDRAM. (*See* CCFF 3253-3255 (describing the need to maintain backwards compatibility between the different generations of SDRAM standards and to avoid delay in the production of DDR II SDRAM parts)).

c. There Is Evidence That Some of Complaint Counsel's Proposed Alternatives to Dual-Edge Clocking and On-Chip DLL Would Infringe Rambus Patents.

1121. Rambus has come forward with a number of patents that it contends cover certain of the alternatives to dual-edge clocking and on-chip DLL proposed by Complaint Counsel through their technical expert, Professor Jacob. In particular, as set forth above, there is evidence to support Rambus's contention that the alternative of interleaving on-chip banks is covered by Rambus's '105 patents. Findings ¶¶ 996-998.

Response to Finding No. 1121: The statement in this proposed finding that Rambus "has come forward with a number of patents it contends that cover certain alternatives" to dual edge clocking and on-chip DLL is inaccurate. Rambus came forward with only one patent, the '105 patent, that it contends covers interleaving on-chip banks. It came up with two patents, owned by other organizations, the '318 patent and the '760 patent, that it contends covers the use of vernier circuits. Rambus has not produced further proposed findings that these three patents relate to any of the additional proposed alternatives to dual edged clocking or on-chip DLL based on evidence in the record. (*See generally* RPF 1007-1077 (additional proposed findings related to alternatives to dual edged clocking do not identify the infringement of patents as a concern), 1078-

1102, 1112-1114 (additional proposed findings related to alternatives to on-chip DLL do not identify infringement as a concern)).

Furthermore, the second sentence in this proposed finding is misleading because there is no evidence in the record to support that the '105 patent relates to this case for the reasons set forth in CCRF 996-997.

1122. Likewise, there is evidence to support Rambus's contention that Professor Jacob's proposed alternative of using a vernier method to remove skew is covered by certain Micron and SLDRAM patents. *See* Findings ¶ 1111.

Response to Finding No. 1122: This proposed finding is misleading because there is no evidence in the record to support that the patents relate to this case for the reasons set forth in CCRF 1111.

1123. As discussed above, Professor Jacob did not consider these, or any other, patents in his investigation of these proposed alternatives, but Professor McAfee based his conclusions of commercial viability on the assumption that the alternatives were unencumbered by patents. *See* Findings ¶¶ 999, 1111.

Response to Finding No. 1123: This proposed finding is misleading for the reasons set forth in CCRF 999 and 1111, which indicate that there was no reason for Dr. Jacob to consider any of the patents raised by Rambus in his analysis of proposed alternatives.

1124. Complaint Counsel has introduced no evidence that the patents raised by Rambus do not cover certain of the proposed alternatives. Even with his assumption of no patent coverage, Professor McAfee could not testify that the alternative of interleaving on-chip banks was commercially viable. As for Professor McAfee's opinion that using a vernier method was commercially viable, this opinion is based on the incorrect assumption that this alternative is not encumbered by patents. It follows that Professor McAfee's opinions in this regard is entitled to no weight.

Response to Finding No. 1124: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The statement in this proposed finding that Professor McAfee made an "incorrect assumption that this alternative is not encumbered by patents" is contrary to the weight of the evidence. (*See* CCRF 1121-1123 (and the cross-references cited in those reply findings)).

d. Given The Cost-Performance Differences, Economically Rational DRAM Manufacturers Would Have Adopted And Licensed The Rambus Technologies Incorporated In DDR.

1125. JEDEC-compliant DDR parts use all four of the Rambus technologies at issue: programmable CAS latency, programmable burst length, dual-edge clocking, and on-chip PLL/DLL. In order to determine whether the use of alternatives to these Rambus technologies used in DDR is more costly than paying the Rambus royalties, one can determine the additional incremental costs associated with the alternatives and compare that to the Rambus royalties that would be paid to Rambus under a license from Rambus. (Rapp, Tr. 9850-54). Costs for alternatives to different features are additive; that is, to calculate the costs associated with implementing alternatives to more than one feature simultaneously, one would simply add the costs associated with the individual alternatives. (Geilhufe, Tr. 9614).

Response to Finding No. 1125: The statement in this proposed finding that "[i]n order to determine whether the use of alternatives to the Rambus technologies used in SDRAM is more costly than paying the Rambus royalties, one can determine the additional variable costs associated with the alternatives and compare them to the Rambus royalties that would be paid under the a license from Rambus" is misleading and contrary to the weight of the evidence because it implies that each member of JEDEC is faced with the same costs to comply with the standard. (*See* CCRF 969). Furthermore, this proposed finding fails take into account the differences between manufacturing costs and royalties. (*See* CCRF 969). Additionally this proposed finding is premised on the faulty assumption, without support in the record, that JEDEC members conducted this type of analysis in making decisions regarding what technologies to put into the standards. (*See* CCRF 969).

1126. To make this comparison, the total additional incremental costs of alternatives are summed and divided by the weighted average of the actual and forecast selling price ("ASP") of DDR for the period 2000 to 2006. (Rapp, Tr. 9844-45, 9850-54). For DDR, the ASP is $5.13. (Rapp, Tr. 9844-45).

Response to Finding No. 1126: Complaint Counsel does not disagree that this proposed finding describes the procedure used by Dr. Rapp. However, RPF 1126 is misleading when it states that this procedure is capable of arriving at one "additional cost of the alternative as a percentage of selling price" for every member of JEDEC. (CCRF 969).

1127. The Rambus royalty rate for the use of its technologies in DDR is 3.5%. (Rapp, Tr. 9853).

Response to Finding No. 1127: The royalty rate that Rambus has charged some users for DDR is 3.5%. Rambus has charged, and has threatened to charge, other users a higher royalty rate. (CCFF 1975-2001). As a result, JEDEC members may have chosen to use alternatives to Rambus technologies even if the cost of doing so was greater than 3.5%.

1128. The same additional incremental costs and performance disadvantages that apply to the alternatives to programmable CAS latency and programmable burst length as used in SDRAM also apply to the use of those alternatives in DDR. (Rapp, Tr. 9842-43).

Response to Finding No. 1128: This proposed finding does not cite to record evidence. The evidence cited is testimony by an economic expert that is cited as substantive evidence on a matter outside of his stated expertise. Furthermore, RPF 1128 is contrary to the weight of the evidence. For a discussion of the costs and benefits of the alternatives described in this case for replacing the use of a mode register to set CAS latency or burst length, *see* CCFF 2130-2233 and 2235-2321.

1129. The alternatives for dual-edge clocking identified as "commercially viable" by Complaint Counsel's economic expert were: interleaving banks on the module, doubling the clock frequency, and the use of toggle mode. (Rapp, Tr. 9841; McAfee, Tr. 7380-81).

Response to Finding No. 1129: Complaint Counsel does not disagree. However, Complaint Counsel's technical expert identified additional options, including "use two or more interleaved memory banks on chip." (CCFF 2344-2350). Professor McAfee did not express an opinion on whether that alternative could constrain the price of using dual-edged clocking because

he saw no evidence that it was presented at JEDEC. However, Professor McAfee did not testify that the technology was not commercially viable.

1130. The total additional incremental cost associated with the use of the alternative of interleaving banks on a module is $0.25 per part, which is the additional incremental cost associated with board complexity. (Rapp, Tr. 9844). As a percentage of ASP, this total additional incremental cost is 4.88%. (Rapp, Tr. 9844-45). These numbers are illustrated in DX313.

Response to Finding No. 1130: This proposed finding is unreliable because it is based on cost determinations of Mr. Geilhufe that are themselves unreliable. (CCRF 969). This cost estimate is particularly unreliable because, to arrive at it, Mr. Geilhufe depends on third party cost quotes for his estimate of the board complexity cost element. (Geilhufe, Tr. 9711). Mr. Geilhufe asserts he obtained these quotes through telephone conversations with manufacturers and suppliers, but no evidence was ever provided of those conversations other than Mr. Geilhufe's testimony. In addition, Mr. Geilhufe never identified in his report, his deposition, or his trial testimony what products he assumed would be used to implement this alternative. (Geilhufe, Tr. 9711-9712). In particular, Mr. Geilhufe never provided the part numbers that would have allowed Complaint Counsel to determine whether the parts he proposed were necessary to implement the alternatives, or whether the prices of the parts were correct. (Geilhufe, Tr. 9711-9712). Mr. Geilhufe did not even state in his report that the basis for his cost estimates under the board complexity element were quotes that he acquired by identifying and calling suppliers and distributors, thus eliminating the possibility that Complaint Counsel could prepare to depose him by independently investigating those quotes. (Geilhufe, Tr. 9711-9712).

In the absence of any indicia of reliability for his assertion that the board complexity element is $4.00 per DIMM, Complaint Counsel submits that this cost be disregarded. If it is disregarded, then the interleave memory banks on DIMM cost is no different, even under Mr. Geilhufe's analysis, than the cost to manufacture DRAMs that use dual-edged clocking, since other

than the board complexity cost element, Mr. Geilhufe could identify no area where the use of interleaving memory banks on the DIMM was more expensive than using dual-edged clocking. (*See* DX0300).

1131. The total additional incremental cost associated with the use of the alternative of doubling the clock frequency is $0.28 per part. (Rapp, Tr. 9845-46). This total consists of the following additional incremental costs per part: a $0.04 final test and good yield cost increase and a $0.24 circuit board area cost increase. (Rapp, Tr. 9845-46). As a percentage of ASP, this total additional incremental cost is 5.46%%. (Rapp, Tr. 9846). These numbers are illustrated in DX313.

Response to Finding No. 1131: This proposed finding is unreliable because it is based on cost determinations of Mr. Geilhufe that are themselves unreliable. (CCRF 969). This cost estimate is unreliable for four reasons. First, Mr. Geilhufe's cost estimates assume that this alternative would require a PLL or a DLL on the module. (Geilhufe, Tr. 9609 ("To distribute this much higher frequency signal on – the double frequency signal on the DIMM would require a – an on-DIMM clock circuitry, possibly on-DIMM PLL/DLL.")). Mr. Geilhufe provided no basis, however, for his opinion that this alternative would require an on-DIMM PLL/DLL other than his opinion that one was required. This opinion is contrary to the weight of the evidence (CCFF 2333-2335, 2338). In particular, presentations were made at JEDEC to increase the clock speed of the DRAMs using a single-edged clock where no on-chip PLL or DLL was needed. (CX0371 at 2-3; Lee, Tr. 6710-6714, 11039-11040).

Second, there is no evidence that Mr. Geilhufe accounted for the cost savings of using a single edge of the clock rather than both edges of the clock. There is substantial evidence in the record that it is easier and less expensive to generate and use a system clock when only one edge of the clock is used (as in SDRAM) rather than when both edges are used (as in DDR SDRAM). (Jacob, Tr. 5420-5421 ("[R]ather than having a dual-edged clocking scheme, you'd have a single-edged clocking scheme, which means that your design of the clock is significantly simpler.

In a dual-edged clocking scheme you have data transitioning on both edges of the clock, and so to have data being sent across the bus at a regular rate, then your clock needs to be very symmetric. ... Whereas, ... for a single-edged clocking scheme, your edge rates, meaning the rise time and the fall time, need not be the same and your duty cycle need not be 50 percent. And you still get, you know, very good behavior. So it's simpler to design a single-edged clock than it is to design a clock with a dual-edged clocking scheme.")).

Third, Mr. Geilhufe depends on third party cost quotes for his estimate of the cost of the on-DIMM PLL/DLL. (Geilhufe, Tr. 9711). Mr. Geilhufe's failure to provide any semblance of a basis in his report for the cost quote that he relied on made it impossible to properly depose him. (*See* CCRF 1130). Additionally, Mr. Geilhufe repeatedly failed to provide the part numbers that would have allowed Complaint Counsel to determine whether the parts he proposed were necessary to implement the alternatives, or even whether the prices of the parts were correct. (Geilhufe, Tr. 9711-9712).

Fourth, record evidence regarding the cost of an on-DIMM PLL/DLL shows that the cost of the component is substantially less than Mr. Geilhufe says it is. (CCFF 2343). In particular, PLLs are regularly used on registered DIMMs. (CCFF 2388). In arriving at his estimate of the costs for the on-DIMM PLL/DLL, Mr. Geilhufe never considered the cost of similar components on registered DIMMs. (Geilhufe, Tr. 9719). The weight of the evidence is that the cost of a PLL on a DIMM can cost as little as (CCFF 2388, *in camera*). Since Mr. Geilhufe determined the price per DRAM for this cost element by dividing the component cost by the number of DRAMs per module, 16, the weight of the evidence is that, assuming that such a PLL is required, the contribution to the cost of the double clock frequency alternative is . (Geilhufe, Tr. 9605). This means that the overall cost of the double clock frequency alternative, assuming that an on-DIMM PLL/DLL is required, is and, assuming that no on-DIMM PLL/DLL is

required, $0.04. This corresponds to an incremental cost increase of less than 2% even if an on-DIMM PLL/DLL is required and less than 1% if it is not required, and does not include the cost savings that the alternative would have because it does not use both edges of the clock.

1132. These two technologies also have performance disadvantages when compared to Rambus's dual-edge clocking technology. (Rapp, Tr. 9846-48). These disadvantages are summarized in DX314.

Response to Finding No. 1132: This proposed finding is not supported by record evidence. The evidence cited is testimony by an economic expert that is cited as substantive evidence on a matter outside of his stated expertise. Furthermore, RPF 1132 is contrary to the weight of the evidence. For a discussion of the costs and benefits of the alternatives described in RPF 1130-1131, as well as others described in this case for replacing the use of a mode register to set CAS latency, *see* CCFF 2322-2365.

1133. The final alternative, toggle mode, is an asynchronous technology that is not technically viable. (Rapp, Tr. 9841, 9856-57).

Response to Finding No. 1133: This proposed finding is not supported by record evidence. The evidence cited is testimony by an economic expert that is cited as substantive evidence on a matter outside of his stated expertise. For a discussion of the costs and benefits of the alternatives described in RPF 1130-1131, as well as others described in this case for replacing the use of a mode register to set CAS latency, *see* CCFF 2363-2365.

1134. The alternatives for on-chip PLL/DLL identified as "commercially viable" by Complaint Counsel's economic expert were: the use of a vernier mechanism, placing the DLL on the module, and relying on the DQS data strobe. (Rapp, Tr. 9841-42). Each of these alternative has performance disadvantages when compared to Rambus's on-chip PLL/DLL technology. (Rapp, Tr. 9848-50). (These disadvantages are summarized in DX 315).

Response to Finding No. 1134: This proposed finding is incorrect. In addition to the alternatives to on-chip PLL/DLL listed in RPF 1134, Professor McAfee found that moving the PLL/DLL to the memory controller was a commercially viable alternative to on-chip PLL/DLL.

(McAfee, Tr. 7382; *see* DX0203). For the technical feasibility of this alternative *see* CCFF 2368-2380. (*See also* MacWilliams, Tr. 4918-4921). The statement regarding supposed performance disadvantages in RPF 1134 is without support by record evidence. The evidence cited is testimony by an economic expert that is cited as substantive evidence on a matter outside of his stated expertise. For a discussion of the costs and benefits of the alternatives to PLL/DLL on the DRAM, *see* CCFF 2366-2414.

1135. The most costly alternatives to the four specified Rambus technologies that are used in JEDEC-compliant DDR that are not covered by Rambus's patents are the use of fuses to set latency, the use of fixed burst length, any on-chip PLL/DLL alternative, and doubling the clock frequency. (Rapp, Tr. 9850-52). The total additional cost of using these four alternatives is $0.36 per part. (Rapp, Tr. 9852). As a percentage of ASP, this additional cost is 7.02%, which exceeds the 3.5% Rambus royalty rate by a substantial margin. (Rapp, Tr. 9853). (These numbers are illustrated in DX 316).

Response to Finding No. 1135: This proposed finding is unreliable because it is based on cost determinations of Mr. Geilhufe that are themselves unreliable. (CCRF 969). Additionally, this proposed finding is premised on a number of unsupportable assumptions that determine Mr. Geilhufe's cost estimates. (CCRF 973-976, 979-982, 1130-1131). Once these cost estimates are adjusted to correspond to the record evidence, the total additional incremental cost of the use of fuses to set latency (CCRF 975) and the use of fixed burst length (CCRF 979) is $0.00. The cost of doubling the clock frequency instead of using a dual-edged clock is between $0.04 and , even without considering the cost savings of not having to use both edges of the clock. (CCRF 1130-1131). This results in a total cost that is, at most, between $0.04 and . Dividing these cost figures by Dr. Rapp's ASP of $5.13 leaves a percentage of ASP of, at most, between .78% and , which are both less than the 3.5% Rambus royalty rate by substantial margins. (RPF 1126).

1136. The least costly alternatives to the four specified Rambus technologies that are used in JEDEC-compliant DDR that are not covered by Rambus's patents are the use of fixed latency, the use of a burst terminate command, any on-chip PLL/DLL alternative, and interleaving banks on

a module. (Rapp, Tr. 9850-52). The total additional cost of using these four alternatives is $0.29 per part. (Rapp, Tr. 9852). As a percentage of ASP, this additional cost is 5.65%, which exceeds the 3.5% Rambus royalty rate by a substantial margin. (Rapp, Tr. 9853). (These numbers are illustrated in DX 316).

Response to Finding No. 1136: This proposed finding is unreliable because it is based on cost determinations of Mr. Geilhufe that are themselves unreliable. (CCRF 969). Additionally, this proposed finding is premised on a number of unsupportable assumptions that determine Mr. Geilhufe's cost estimates. (CCRF 973-976, 979-982, 1130-1131). Once these cost estimates are adjusted to be more in line with the record evidence, the total additional incremental cost of the use of fixed CAS latency (CCRF 973) and the use of a burst terminate command to set burst length (CCRF 981) is -$0.01. This combination of four alternatives, would only be more expensive under Mr. Geilhufe's analysis if the total cost of the board complexity element asserted by Mr. Geilhufe were accepted (in that case, this alternative would be the most expensive alternative considered by Mr. Geilhufe). For the reasons stated in CCRF 1130, Mr. Geilhufe's extimates regarding board complexity should not be credited. If the board complexity element were discounted, then this alternative would, in fact, be less expensive under the Rapp/Geilhufe analysis than the current standard. (CCRF 973, 981, 1130).

1137. In order to determine what royalty a rational decision-maker would have expected Rambus to charge (in the absence of direct knowledge), the standard assumption and methodology in economics is to assume that the royalty rate actually charged is the best estimate of the royalty rate a decision-maker would have expected at an earlier time. (Rapp, Tr. 10207-09). Similarly, the standard assumption and methodology in economics is to assume that the actual weighted average selling price over the product life cycle is the best estimate of an ASP that a decision-maker would have predicted in advance. (Rapp, Tr. 10212-13). Using the standard assumptions and methodology in economics, a rational DRAM manufacturer or group of manufacturers would have expected the additional costs of any alternatives to outweigh the costs of Rambus's royalties.

Response to Finding No. 1137: This proposed finding is misleading and unreliable for the reasons described in CCRF 986, CCRF 1127, CCRF 1131-1132, and CCRF 1135-1136.

1138. Based on these cost calculations and in consideration of the performance advantages of the four Rambus technologies incorporated in DDR, it is clear that Rambus's technologies were superior in cost-performance terms. (Rapp, Tr. 9857-58). A rational manufacturer or group of manufacturers in JEDEC would have chosen to take a license from Rambus at 3.5% for DDR rather than use any combination of the alternatives identified by Complaint Counsel's economic expert as "commercially viable" that are not covered by Rambus's patents. (Rapp, Tr. 9857-59).

Response to Finding No. 1138: This proposed finding is unreliable and contrary to the weight of the evidence for the reasons described in CCRF 987, CCRF 1131-1132, and CCRF 1135-1136.

This finding is also inaccurate and misleading because using Mr. Geilhufe's own cost estimates, the lowest cost alternative for dual-edged clocking is interleaving on-chip memory banks, which has an added incremental cost of $0.06 compared to dual-edged clocking. (CCFF 2875; *see* DX300). Dr. Rapp did not analyze this alternative. Had he analyzed this alternative technology, using Mr. Geilhufe's cost estimates, he would have identified a combination of alternative technologies that his own methodology indicates JEDEC would have preferred to the current DDR SDRAM standard with the current Rambus royalties. (CCFF 2876). Furthermore, Dr. Rapp dismisses the use of asynchronous toggle mode based on his understanding that the technology is not technically viable. (RPF 1133). However, Mr. Geilhufe provided cost estimates for that alternative as well which would have been a low cost alternative to dual-edged clocking. (CCFF 2877). Had Dr. Rapp analyzed toggle mode, he would have been able to identify another combination of alternatives that his methodology would have indicated that JEDEC would have preferred to the current standard including the Rambus royalties. (CCFF 2878).

1139. Although DRAM manufacturing costs decline over time, this does not affect the additional incremental costs used for purposes of the calculations with regard to alternative technologies for either SDRAM or DDR because these costs were estimated for a mature product. (Rapp, Tr. 9854). Moreover, some of the estimated costs, such as inventory costs, are not subject to a decline over time because the decline in costs in the DRAM industry come from improvements in manufacturing technology and increased yields. (Rapp, Tr. 9854-55).

Response to Finding No. 1139: This proposed finding is misleading because, although Dr. Rapp apparently understood that the costs estimated by Mr. Geilhufe were for a "mature product," Mr. Geilhufe testified that the costs of the alternatives could still be reduced by further die shrinks. Mr. Geilhufe agreed that further DRAM shrinks were possible off of the DRAM design whose cost he was estimating. (Geilhufe, Tr. 9726 ("It's possible that there are further shrinks, but I -- I assumed that 20 million units could be built off that one design effort.")). The weight of the evidence further indicates that the number of DRAM chips manufactured off of a DRAM design is significantly in excess of the 20 millions units assumed by Mr. Geilhufe. (Lee, Tr. 10997 ("Q. Now, approximately how many units of the 64-meg SDRAM product has Micron produced? A. Of course, we're still producing today, but roughly over the course of the lifetime approximately 900 million.")).

1140. Complaint Counsel's technical expert did not provide any cost information that was useful for economic analysis because he provided no cost numbers. (Rapp, Tr. 9855-56). Economists cannot make useful statements about cost comparisons without some sort of a numerical calculation or comparison. (Rapp, Tr. 9856).

Response to Finding No. 1140: This proposed finding is misleading because it fails to consider substantial contrary record evidence in the form of Professor McAfee's testimony. (McAfee, Tr. 7360-7362, 7369-7370, 7382-7385; *see* DX0185, DX0186, DX0192, DX0203-DX0206, DX0209).

5. Rambus Also Has Patents Outside the '898 Family That Cover DDR SDRAMs.

1141. Even if Rambus were unable to enforce patents in the '898 family, it would still have patents, outside the '898 family, that cover DDR SDRAMs.

Response to Finding No. 1141: The proposed finding is not supported by the record evidence. CCRF 1042-46. The proposed finding is irrelevant to any issue in this case, including whether Rambus's failure to disclose patent applications in the '898 family to JEDEC

while simultaneously working to obtain patent claims covering JEDEC work amounted to exclusionary conduct.

a. Rambus's '405 Patent Covers DDR SDRAMs.

1142. The '405 patent issued on October 22, 2002 and claims priority to an application filed on October 19, 1995. (RX 2122-15 at 1; Fliesler, Tr. 8877-78). However, Claim 1 of the patent was not filed until May 29, 2001. (Fliesler, Tr. 8880).

Response to Finding No. 1142: The proposed finding is misleading. Rambus has failed to offer any evidence demonstrating that it had no duty to disclose the '405 patent's parent applications to JEDEC in light of the fact that, by asserting an effective filing date of October 19, 1995, Rambus represents that it had invented the subject matter claimed in the '405 patent while it was a JEDEC member. (*See*, Fliesler, Tr. 8877-80 (complete evidence regarding '405 patent)).

Mr. Fliesler testified that claim 1 of the '405 patent recited a "precharge" feature as used in DDR SDRAM. Release 4 of the JEDEC SDRAM standard indicates that as of 1993, the standard incorporated a precharge feature. (JX0056 at 115; Fliesler, Tr. 8951-52).

1143. Claim 1 of the '405 patent reads on the JEDEC DDR SDRAM standard. (RX 2122-15 at 45; Fliesler, Tr. 8879). Claim 1 of the patent contains precharge and strobe signal limitations that correspond to features of the DDR SDRAM standard. (RX 2122-15 at 45; CX 234 at 151, 164; JX 57 at 30; Fliesler, Tr. 8879).

Response to Finding No. 1143: The cited evidence does not support the proposed finding. Demonstrating that a JEDEC-compliant DDR SDRAM would necessarily infringe claim 1 requires showing that each limitation of claim 1 must necessarily be included in the accused device. (Nusbaum, Tr. 1565-66; RPF 334). Mr. Fliesler's conclusory statements regarding only the precharge feature and strobe signal limitations, but ignoring other limitations, are insufficient to establish infringement. (*See* Fliesler, Tr. 8879). Rambus provided no evidence that it has ever asserted that the '405 patent covers a JEDEC-compliant DDR SDRAM in licensing negotiations or otherwise. (Fliesler, Tr. 8949).

The cited evidence, Mr. Fliesler's testimony, is unreliable. Patent claims must be interpreted as they would be understood by a person of ordinary skill in the art. (Fliesler, Tr. 8933). Mr. Fliesler is an attorney, and not a person skilled in the art of DRAM design and architecture. (Fliesler, Tr. 8867-69, 8781-8782). Even in his work as a patent attorney, Mr. Flielser has had minimal exposure to technical DRAM issues. (Fliesler, Tr. 8782). Moreover, Mr. Fliesler did not discuss his claim interpretation and his analysis of the DDR SDRAM standard with any person skilled in the pertinent art. Rather, he relied on his own analysis. (Fliesler, Tr. 8783, 8877-80, 8934, 8948).

Claim 1 requires "receiving a first code." (RX2122-15 at 45). Mr. Fliesler's interpretation of this term and his analysis of whether it is required by the DDR SDRAM standard are unreliable. Despite the fact that he does not know whether the term "first code" is a commonly understood term in the field, he failed to consult technical dictionaries for the proper understanding of the term. (Fliesler, Tr. 8950).

b. Rambus's '353 Patent Covers DDR SDRAM.

1144. The Court has taken official notice of United States Patent No. 6,591,353 which issued on July 8, 2003 and is assigned to Rambus.

Response to Finding No. 1144: Complaint Counsel does not disagree that the Court has taken judicial notice of the '353 patent. However, the Court has "decline[d] to take official notice of what the patents in question relate to or cover, and decline[d] to engage in any analysis or interpretation of the substance or content" of the patent. *See* Order on Respondent's Request for Official Notice at 3 (August 27, 2003).

1145. Claim 1 of the '353 patent claims:

> "A method of operations of in a memory device that includes a plurality of memory cells, the method comprising:
> receiving a command to sample data;

> deferring sampling a first portion of the data until an external strobe signal is detected; and
> sampling the first portion of the data from an external signal line in response to detecting the external strobe signal."

Response to Finding No. 1145: Complaint Counsel does not disagree that claim 1 of the '353 patent contains these words. However, patent claims must be interpreted as they would be understood by a person of ordinary skill in the art. (Fliesler, Tr. 8933). The proposed finding cites no expert testimony or other evidence, including the patent's specification, its prosecution history, or technical dictionaries and treatises, to establish the proper interpretation of this claim. The words of the claim, without more, are insufficient to allow the court to establish the proper interpretation of the claim. *See NeoMagic Corp. v. Trident Microsystems, Inc.*, 287 F.3d 1062, 1074 (Fed. Cir. 2002) ("given the complex technology involved in this case, we think that this matter [interpretation of a claim to a DRAM memory chip controller] can only be resolved by further evidentiary hearings, including expert testimony, before the district court.").

The Court's judicial notice of the '353 patent, without evidence supporting a proper claim interpretation and infringement analysis, is insufficient to support a conclusion that Rambus has patents outside the '898 family that cover the DDR SDRAM standard because the Court has "decline[d] to take official notice of what the patents in question relate to or cover, and decline[d] to engage in any analysis or interpretation of the substance or content" of the patent. *See* Order on Respondent's Request for Official Notice at 3 (August 27, 2003).

1146. DDR SDRAMs are memory devices that include a plurality of memory cells. DDR SDRAMs receive commands to sample data (namely, write commands). DDR SDRAMs sample data from an external signal line (the bus) only when an external strobe signal (the DQS data strobe) is detected. (CX 234 at 164; JX 57 at 30). As JEDEC standard JESD79 for DDR SDRAMs states: "WRITE bursts are initiated with a WRITE command. . . . During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS." (JX 57 at 30).

This proposed finding is not supported by any evidence in the record explaining the relevant portions of DDR SDRAM standard.

The proposed finding does not support the conclusion that the '353 patent covers a JEDEC-compliant DDR SDRAM. A determination that a patent claim covers a product is a two step process. The first step requires that the court interpret the patent claim as it would be understood by a person of ordinary skill in the art as a question of law. (Fliesler, Tr. 8778, 8933). The proposed finding cites no expert testimony or other evidence to establish the proper interpretation of claim 1 of the '353 patent. The second step requires a factual determination that each element of the properly interpreted claim is present in the product. (Nusbaum, Tr. 1565-66). The proposed finding cites no expert testimony or other evidence to establish that each element of claim 1 corresponds to features of a JEDEC-compliant DDR SDRAM. The interpretation of patent claims involving complex technology, and the comparison of a product to that claim, cannot be properly resolved without the development of evidence, including expert testimony, before the finder of fact. *See NeoMagic Corp. v. Trident Microsystems, Inc.*, 287 F.3d 1062, 1074 (Fed. Cir. 2002) ("given the complex technology involved in this case, we think that this matter [interpretation of a claim to a DRAM memory chip controller] can only be resolved by further evidentiary hearings, including expert testimony, before the district court.").

The Court's judicial notice of the '353 patent, without evidence supporting a proper claim interpretation and infringement analysis, is insufficient to support a conclusion that Rambus has patents outside the '898 family that cover the DDR SDRAM standard because the Court has "decline[d] to take official notice of what the patents in question relate to or cover, and decline[d] to engage in any analysis or interpretation of the substance or content" of the patent. *See* Order on Respondent's Request for Official Notice at 3 (August 27, 2003).

D. Even Assuming That Alternatives Did Exist, JEDEC Would Not Have Rejected The Rambus Technologies.

1147. A wholly independent means to determine whether JEDEC would have adopted alternatives to Rambus's SDRAM and DDR technologies had Rambus made the additional disclosures that Complaint Counsel allege should have been made is to examine JEDEC's and Rambus's likely behavior in a but-for world.

Response to Finding No. 1147: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Furthermore, this finding is vague in describing a "wholly independent means" to determine whether JEDEC would have adopted Rambus's technologies.

1148. Rambus offered the testimony of Professor David Teece regarding this decision analysis. He is very well qualified to opine on this issue.

Response to Finding No. 1148: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1149. Professor Teece has a Master's degree in economics from the University of Canterbury, a Master's degree in economics from the University of Pennsylvania, and a Ph.D. in economics from the University of Pennsylvania. (Teece, Tr. 10297). The subject of his Ph.D. thesis was the resource costs of transferring technology between nations and amongst firms. (Teece, Tr. 10297). The thesis was published as a book, and two peer-reviewed articles came from it. (Teece, Tr. 10297). Professor Teece has over 150 publications and over a dozen books. (Teece, Tr. 10298).

Response to Finding No. 1149: Complaint Counsel does not disagree. Complaint Counsel notes, however, that this proposed finding is irrelevant to Professor Teece's knowledge, or lack of knowledge, of the factual record in this case. In fact, Dr. Teece either failed to review or cannot recall reviewing substantial portions of the key evidence in this case, including: any evidence relating to what Rambus executives considered to be reasonable baselines for royalties for the patents at issue (Teece, Tr. 10654-10655); Rambus internal documents relating to JEDEC or

JEDEC policies other than documents that were explained to him (Teece, Tr. 10523-10525); Rambus business records, other than some license agreements (Teece, Tr. 10524-10525); any depositions other than portions of the deposition of Farhad Tabrizi (Teece, Tr. 10525); Professor Teece conducted no interviews of JEDEC representatives or any other engineers other than Rambus's technical representatives (Teece, Tr. 10525-10526).

1150. Professor Teece is a chaired professor in the School of Business at the University of California at Berkeley. (Teece, Tr. 10295). He is also the Director of the Institute for Management, Innovation, and Organization at the University of California at Berkeley. (Teece, Tr. 10295). The Institute conducts research into questions of innovation, technology policy, and technology strategy. (Teece, Tr. 10295). The Institute has conducted a lengthy multi-country study of the global semiconductor industry. (Teece, Tr. 10295-96).

Response to Finding No. 1150: Complaint Counsel does not disagree. Complaint Counsel notes, however, that this proposed finding is irrelevant to Professor Teece's knowledge, or lack of knowledge, of the factual record in this case. In fact, Dr. Teece either failed to review or cannot recall reviewing substantial portions of the key evidence in this case, including: any evidence relating to what Rambus executives considered to be reasonable baselines for royalties for the patents at issue (Teece, Tr. 10654-10655); Rambus internal documents relating to JEDEC or JEDEC policies other than documents that were explained to him (Teece, Tr. 10523-10525); Rambus business records, other than some license agreements (Teece, Tr. 10524-10525); any depositions other than portions of the deposition of Farhad Tabrizi (Teece, Tr. 10525); Professor Teece conducted no interviews of JEDEC representatives or any other engineers other than Rambus's technical representatives (Teece, Tr. 10525-10526).

1151. Professor Teece has taught a number of courses over the years, including (with regularity) a Master's level course on management innovation and a Ph.D. seminar on technology strategy and related public policy issues. (Teece, Tr. 10296-97). In addition to teaching at Berkeley, Professor Teece has taught at the University of Pennsylvania, Stanford University, and Oxford University. (Teece, Tr. 10296). He was recently invited to give the Clarendon Lectures in the Business Economics at Oxford University. (Teece, Tr. 10296).

Response to Finding No. 1151: Complaint Counsel does not disagree. Complaint Counsel notes, however, that this proposed finding is irrelevant to Professor Teece's knowledge, or lack of knowledge, of the factual record in this case. In fact, Dr. Teece either failed to review or cannot recall reviewing substantial portions of the key evidence in this case, including: any evidence relating to what Rambus executives considered to be reasonable baselines for royalties for the patents at issue (Teece, Tr. 10654-10655); Rambus internal documents relating to JEDEC or JEDEC policies other than documents that were explained to him (Teece, Tr. 10523-10525); Rambus business records, other than some license agreements (Teece, Tr. 10524-10525); any depositions other than portions of the deposition of Farhad Tabrizi (Teece, Tr. 10525); Professor Teece conducted no interviews of JEDEC representatives or any other engineers other than Rambus's technical representatives (Teece, Tr. 10525-10526).

1152. Professor Teece has received the first international prize in technology strategy and he has been named one of the 50 most important business thinkers of our time. (Teece, Tr. 10298-99).

Response to Finding No. 1152: Complaint Counsel does not disagree. Complaint Counsel notes, however, that this proposed finding is irrelevant to Professor Teece's knowledge, or lack of knowledge, of the factual record in this case. In fact, Dr. Teece either failed to review or cannot recall reviewing substantial portions of the key evidence in this case, including: any evidence relating to what Rambus executives considered to be reasonable baselines for royalties for the patents at issue (Teece, Tr. 10654-10655); Rambus internal documents relating to JEDEC or JEDEC policies other than documents that were explained to him (Teece, Tr. 10523-10525); Rambus business records, other than some license agreements (Teece, Tr. 10524-10525); any depositions other than portions of the deposition of Farhad Tabrizi (Teece, Tr. 10525); Professor Teece conducted no interviews of JEDEC representatives or any other engineers other than Rambus's technical representatives (Teece, Tr. 10525-10526).

1153. Professor Teece co-founded a journal entitled Industrial and Corporate Change, published by Oxford University Press, which focuses on technology management, technology policy, and the economics of innovation. (Teece, Tr. 10299). He has also refereed several peer-reviewed journals. (Teece, Tr. 10299-300).

Response to Finding No. 1153: Complaint Counsel does not disagree. Complaint Counsel notes, however, that this proposed finding is irrelevant to Professor Teece's knowledge, or lack of knowledge, of the factual record in this case. In fact, Dr. Teece either failed to review or cannot recall reviewing substantial portions of the key evidence in this case, including: any evidence relating to what Rambus executives considered to be reasonable baselines for royalties for the patents at issue (Teece, Tr. 10654-10655); Rambus internal documents relating to JEDEC or JEDEC policies other than documents that were explained to him (Teece, Tr. 10523-10525); Rambus business records, other than some license agreements (Teece, Tr. 10524-10525); any depositions other than portions of the deposition of Farhad Tabrizi (Teece, Tr. 10525); Professor Teece conducted no interviews of JEDEC representatives or any other engineers other than Rambus's technical representatives (Teece, Tr. 10525-10526).

1154. Professor Teece's specialization within the field of industrial organization is in technology policy and particularly antitrust policy as it relates to high technology industries. (Teece, Tr. 10300). In the last 15 to 20 years, he has written numerous articles on technology strategy and on the interface of technology policy and antitrust policy. (Teece, Tr. 10300).

Response to Finding No. 1154: Complaint Counsel does not disagree. Complaint Counsel notes, however, that this proposed finding is irrelevant to Professor Teece's knowledge, or lack of knowledge, of the factual record in this case. In fact, Dr. Teece either failed to review or cannot recall reviewing substantial portions of the key evidence in this case, including: any evidence relating to what Rambus executives considered to be reasonable baselines for royalties for the patents at issue (Teece, Tr. 10654-10655); Rambus internal documents relating to JEDEC or JEDEC policies other than documents that were explained to him (Teece, Tr. 10523-10525); Rambus business records, other than some license agreements (Teece, Tr. 10524-10525); any

depositions other than portions of the deposition of Farhad Tabrizi (Teece, Tr. 10525); Professor Teece conducted no interviews of JEDEC representatives or any other engineers other than Rambus's technical representatives (Teece, Tr. 10525-10526).

1155. Professor Teece also has substantial expertise in the area of the economics of standard-setting. He began to study the economics of standard-setting organizations about a decade ago. (Teece, Tr. 10300-01). He was invited to speak twice at the joint FTC/DOJ hearings on the subject of standard-setting and antitrust. (Teece, Tr. 10301).

Response to Finding No. 1155: Complaint Counsel does not disagree. Complaint Counsel notes, however, that this proposed finding is irrelevant to Professor Teece's knowledge, or lack of knowledge, of the factual record in this case. In fact, Dr. Teece either failed to review or cannot recall reviewing substantial portions of the key evidence in this case, including: any evidence relating to what Rambus executives considered to be reasonable baselines for royalties for the patents at issue (Teece, Tr. 10654-10655); Rambus internal documents relating to JEDEC or JEDEC policies other than documents that were explained to him (Teece, Tr. 10523-10525); Rambus business records, other than some license agreements (Teece, Tr. 10524-10525); any depositions other than portions of the deposition of Farhad Tabrizi (Teece, Tr. 10525); Professor Teece conducted no interviews of JEDEC representatives or any other engineers other than Rambus's technical representatives (Teece, Tr. 10525-10526).

1156. In contrast, Complaint Counsel's economic expert has never published a single paper on the issue of standard-setting. (McAfee, Tr. 11345). He was not invited to speak at the joint FTC and DOJ hearings. (McAfee, Tr. 11345). He has never been invited to speak on the issue of standard-setting. (McAfee, Tr. 11345).

Response to Finding No. 1156: Complaint Counsel does not disagree. Complaint Counsel notes, however, that this proposed finding is irrelevant to Professor McAfee's knowledge of the factual record in this case. Professor McAfee conducted interviews of DRAM engineers, DRAM plant managers, DRAM users, and JEDEC participants and reviewed a wide range of documents prior to arriving at his opinions in this case. (McAfee, Tr. 7146-7149, 7150-7157).

1157. The but-for world may be analyzed by the use of a decision tree, which is a device commonly used in economics to understand the different possible scenarios and outcomes in a "but-for" world. (Teece, Tr. 10315-16). In this case, the decision tree starts with the but-for world assumption that Rambus made the additional disclosures that Compliant Counsel allege it should have made. (Teece, Tr. 10316). (A demonstrative exhibit that shows the decision tree – for illustration purposes, not as evidence – was marked as DX 332).

Response to Finding No. 1157: Complaint Counsel does not disagree, but notes that another demonstrative exhibit that shows the decision tree was marked as DX0377.

1158. The decision tree may be described as follows. Had Rambus made these additional disclosures, JEDEC would have a choice; it could either proceed without seeking a RAND letter from Rambus, or it could ask Rambus to provide a RAND letter. (Teece, Tr. 10316). Had JEDEC proceeded without asking for a RAND letter, the same outcome would have occurred in the but-for world as in the actual world – JEDEC would have adopted standards incorporating Rambus's technologies. (Teece, Tr. 10329-30). If JEDEC had asked for a RAND letter, Rambus would have to decide whether to give a RAND letter. (Teece, Tr. 10317). If Rambus agreed to give a RAND letter, JEDEC members would (as a theoretical matter) have sought to negotiate licenses from Rambus before the standard was adopted and before any relevant patents issued (*ex ante*) or it could have proceeded without such negotiations. (Teece, Tr. 10317-18). If there were no *ex ante* negotiations, JEDEC could have adopted the standards incorporating Rambus's technologies or it could have adopted different standards. (Teece, Tr. 10319). Had JEDEC adopted the same standards as it actually adopted, the same outcome would have occurred in the but-for world as in the actual world. (Teece, Tr. 10319).

Response to Finding No. 1158: The statement in this proposed finding that had "JEDEC proceeded without asking for a RAND letter, the same outcome would have occurred in the but-for world as in the actual world – JEDEC would have adopted standards incorporating Rambus's technologies," is contrary to the weight of the evidence. Had Rambus disclosed to JEDEC that it thought it had intellectual property on the developing standards, JEDEC members would then have known about that intellectual property, and the clear weight of the evidence is that JEDEC members sought to avoid intellectual property issues relating to the JEDEC standards, and so would have worked around that intellectual property. (CCFF 107-111, 300-304, 2101, 2447-2453).

1. Had Rambus Made The Disclosures Described By Complaint Counsel, JEDEC Might Have Proceeded Without Seeking a RAND Assurance from Rambus.

1159. As a matter of economic analysis, there are a number of considerations that suggest JEDEC might not have asked Rambus for a RAND letter, even if Rambus had made all of the disclosures described by Complaint Counsel. First, JEDEC might have perceived that Rambus was trying to derail the standard-setting process by gaming the system. (Teece, Tr. 10320-22). That is, JEDEC might have believed that Rambus was asserting that it had patent rights in order to provoke JEDEC into seeking a RAND letter so that Rambus could refuse to give the letter and thereby stopping or slowing the standardization process. (Teece, Tr. 10320-22).

Response to Finding No. 1159: This proposed finding is misleading and contrary to the weight of the evidence. This proposed finding is misleading because it posits a but-for world in which Rambus makes a less than good faith disclosure that leads JEDEC into believing that "Rambus was trying to derail the standard-setting process by gaming the system." However, Professor Teece agreed that from the standpoint of economic theory and methodology, in formulating a but-for world, the standard methodology is to conceptualize a world in which nothing changes except the challenged conduct does not occur. That is, the defendant, conforms its conduct in the but-for world with what it is challenged for not having done in the real world. (Teece, Tr. 10676-10677; *see also* CCFF 3018-3019 for similar testimony by Professor McAfee). As a result, if Rambus had conformed with the JEDEC rules, it would have made a good faith disclosure that it believed that it possessed intellectual property that "might be involved in the work they are undertaking" in the committee. (CCFF 318-322 (patent disclosure rule); CCFF 310-314 (EIA and JEDEC rely on the good faith of participants in the process to surface patent issues)). That disclosure, in order to conform with the rules of JEDEC would have included sufficient information to put the committee on notice as to the nature of the relationship between the proposed standard and the intellectual property that might relate to that standard. (CCFF 331). There is no reason to hypothesize that such a disclosure would lead JEDEC to the conclusion that Rambus was "gaming the system." (McAfee, Tr. 11329 ("it's my expectation if it's a good-faith disclosure that it's convincing that Rambus does in fact have coverage of that, which that's what I understand your hypothetical to be, ...")).

Furthermore, the weight of the evidence is that JEDEC rules require that RAND assurances be received by the committee prior to including technologies in the standard "when it appears to the committee that the candidate standard may require the use of a patented invention.." (CX0353 at 1 (underline in original)). Under those circumstances, "the committee chairperson must receive a written assurance from the organization holding rights to such patents that a license will be made available" on RAND terms before including the technology in the proposed standard. (CX0208 at 19; CX0203A at 11 ("The Committee Chairman must have also received a written expression from the patent holder that he is willing to license applicants under" RAND terms.)). The hypothesis that JEDEC might not have asked Rambus for a RAND letter because it "might have perceived that Rambus was trying to derail the standard-setting process by gaming the system" posits that JEDEC violate its own rules based on a good faith disclosure by Rambus and is unsubstantiated by the evidence.

1160. Second, JEDEC might not have asked for a RAND letter because it might have believed that Rambus would not obtain patents that would cover products complying with the JEDEC standard. (Teece, Tr. 10323). For example, JEDEC might have believed that Rambus's patent applications would not result in issued patents or that, if they did, the patents might not be valid because of prior art. (Teece, Tr. 10323).

Response to Finding No. 1160: This proposed finding is misleading and contrary to the weight of the evidence for the reasons stated in CCRF 1159. Furthermore, record evidence establishes that even when some member companies had questions as to whether there was prior art that might invalidate Rambus patents, JEDEC still sought to avoid those patents. For example, NEC made a proposal in March of 1997 involving "a read clock and a write clock." (CCFF 2436). Some members of the 42.3 committee stated their belief that Rambus might have a patent on that type of design. (CCFF 2437). Other members of the committee stated their belief "that the concept predated Rambus by decades." (JX0036 at 7). Nevertheless, JEDEC members refused to consider

the proposal because of the potential patent issues (CCFF 2438), and JEDEC ultimately adopted a different technology. (CCFF 2440).

Furthermore, if this proposed finding is independent from RPF 1159, then this proposed finding does not hypothesize that JEDEC might think that Rambus was potentially "gaming the system," and so JEDEC would have no reason to think that Rambus would not provide a RAND assurance if asked. In that case, this finding is misleading because it hypothesizes that JEDEC might violate its own rules that a RAND assurance must be obtained before including a potentially patented technology in the standard, but proposes no benefit to JEDEC of doing so. (CX0208 at 19; CX0203A at 11 ("The Committee Chairman must have also received a written expression from the patent holder that he is willing to license applicants under" RAND terms.)).

1161. Third, JEDEC might not have asked for a RAND letter from Rambus because, in the real world, JEDEC did not seek, and to this day has not sought, a RAND assurance from Rambus regarding SDRAM, DDR or DDR2 despite JEDEC's knowledge of and concerns about Rambus's patent coverage. (Teece, Tr. 10323-27).

Response to Finding No. 1161: The statement in this proposed finding that "in the real world, JEDEC did not seek, and to this day has not sought, a RAND assurance from Rambus regarding SDRAM, DDR or DDR2" is not supported by the cited testimony. Professor Teece is not competent to testify to the facts asserted. Consequently, this testimony can only be treated as an assumption by Professor Teece. Furthermore, this assumption is not supported by substantial record evidence, rendering Professor Teece's opinion that JEDEC might not have asked for a RAND letter from Rambus unreliable.

Furthermore, this proposed finding is misleading and incomplete. First, this proposed finding is misleading because it treats a disclosure made during the standard setting process the same as a disclosure made after the industry is locked into an already existing standard. The weight of the evidence is that the purpose of the patent disclosure rule is to inform the committee

of information regarding the existence of intellectual property in order to give the relevant committee the opportunity to understand whether it should change the standard to avoid the intellectual property. (CCFF 317). The weight of the evidence is also that, by the time Rambus began suing DRAM industry members, the industry was already locked in to the standards so JEDEC could not have changed the standard even if Rambus had issued a RAND letter at that point. (CCFF 2500-2585).

Second, this proposed finding is incomplete because it omits evidence that JEDEC had already been made aware of Rambus's position regarding the issuance of a RAND letter. In the real world, JEDEC learned of the Rambus patent coverage only after it became aware that Rambus believed that JEDEC's licensing policies were contrary to Rambus's business model, so there was no reason for JEDEC to have asked Rambus for RAND assurances that it knew would not be given. For example, in May of 1992, Richard Crisp, Rambus's JEDEC representative told the chairman of the 42.3 committee that he wanted to present at JEDEC, but that Rambus would not be willing to comply with the JEDEC licencing policies. (G. Kelley, Tr. 2487 ("I asked him if he agreed to the JEDEC policy on disclosure, and licensing, and he told me that he could not agree for Rambus on the policy for licensing.")). Because Rambus was not willing to comply with the JEDEC licensing policy, Mr. Crisp was not allowed to present. (G. Kelley, Tr. 2487). Approximately a year later Mr. Crisp again requested to present at JEDEC but again stated that Rambus was not willing to comply with the licensing policy. (G. Kelley, Tr. 2487-2488). This time, Gordon Kelley, the 42.3 committee chairman raised the issue of whether Rambus could present to the committee without agreeing to the JEDEC licensing policies. (G. Kelley, Tr. 2488 ("when I opened the DRAM task group meeting up, I asked the committee if they wanted to see a Rambus proposal for a new DRAM, but that Rambus would not agree to the JEDEC patent policy, especially regarding licensing..."); G. Kelley, Tr. 2488-2489 ("Q. When you made a reference to

Rambus did not adhere to the JEDEC patent policy, was Mr. Crisp saying to you that Rambus did not agree with the JEDEC disclosure policy or with the JEDEC licensing policy or was it something else? A. He had specified to me that the problem was with the licensing policy.")).

When Rambus notified JEDEC that it did not plan to renew its membership in JEDEC in June of 1996, the only reason Rambus gave for its non-renewal was that "Rambus plans to continue to license its proprietary technology on terms that are consistent with the business plan of Rambus, and those terms may not be consistent with the terms set by standards bodies, including JEDEC." (CX0888 at 1).

In the only opportunity on the record for Rambus to agree to comply with RAND terms, other than Rambus's statements to JEDEC, Rambus was asked for a RAND letter by the IEEE, for technologies incorporated into the proposed Synclink standard. (*See* CCFF 1500-1587 for a discussion of IEEE, Synclink, and their relation to the issues in this case). In December of 1995, IEEE requested a RAND letter from Rambus. (CCFF 1535). Rambus's attorney, Anthony Diepenbrock, believing that RAND licensing as requested by the IEEE, was inconsistent with Rambus's existing business practices, replied that Rambus would only license its technologies "in accordance with its existing business practices." (CCFF 1537-1539).

Members of the 42.3 JEDEC committee understood that Rambus was not willing to comply with the JEDEC patent policies. (JX0036 at 7 ("Rambus has also told JEDEC that they do not intend to comply with JEDEC patent policies.")).

1162. JEDEC's failure to seek a RAND letter from Rambus is not explained by speculation that JEDEC *may* have chosen not to ask for a RAND letter -- after Rambus began asserting its issued patents against DRAM manufacturers -- because of litigation between Rambus and the DRAM manufacturers. (Teece, Tr. 10328-29). This argument is inconsistent with JEDEC's real world behavior. In the real world, JEDEC sought a RAND letter from Texas Instruments regarding the Quad-CAS technology even though TI was in litigation with Micron at the time. (Teece, Tr. 10329; CX 348 at 2, 4).

Response to Finding No. 1162: The statement in this proposed finding that "[i]n the real world, JEDEC sought a RAND letter from Texas Instruments regarding the Quad-CAS technology even though TI was in litigation with Micron at the time" is not supported by the cited evidence. Professor Teece is not competent to testify to the facts asserted. Consequently, this testimony can only be treated as an assumption by Professor Teece. Furthermore, this assumption is not supported by substantial record evidence, rendering Professor Teece 's opinion that JEDEC might not have asked for a RAND letter from Rambus unreliable. In particular, the document cited does not support the proposition that JEDEC sought a RAND letter from Texas Instruments.

Furthermore, this proposed finding is incomplete because it omits evidence showing that TI had indicated it was willing to license on RAND terms while Rambus had indicated that it was unwilling to do so. As described in CCRF 1161, prior to its lawsuits against DRAM manufacturers, Rambus made clear to JEDEC that it was not willing to comply with the JEDEC licensing policies. In contrast, Texas Instruments made it clear, in a letter from Texas Instrument's Director of Standards to the Chair of the JEDEC Council regarding the Quad-CAS incident, that they *were* willing to comply with the JEDEC RAND licensing policies in November of 1993. (CX0346 at 7 ("This letter is to confirm that Texas Instruments does support the JEDEC patent policy, as it does the equivalent ANSI and ISO policies, where they pertain to the obligation to license others on a nondiscriminatory basis for a reasonable fee. Indeed, TI was a participant in the development of the ANSI patent policy itself as well as the *ad hoc* committee which drafted the guidelines for implementation."); *see* CCFF 424-432 for a more complete discussion of the Quad-CAS incident). This letter was distributed to the entire 42.3 committee in the December 1993 JEDEC minutes. (CX0060A at 29). However, in that same meeting the committee voted to withdraw the Quad-CAS DRAM standards. (CX0060A at 4-5). It was not until early 1995, when

JEDEC finally received the letter communicating those RAND assurances that the committee took Quad-CAS off hold. (CCFF 432).

1163. Had Rambus made the additional disclosures that Complaint Counsel contend it should have made and had JEDEC not sought a RAND letter, economic analysis shows that JEDEC would have adopted the same standards that it did in the real world - the standards incorporating Rambus's technology. (Teece, Tr. 10329-30). Complaint Counsel's economic expert conceded this to be true; he testified that had JEDEC not sought a RAND letter, "it would lead to the same outcome as the actual world." (McAfee, Tr. 11308). In that event, the alleged failure to disclose had no anticompetitive effect. (Teece, Tr. 10320).

Response to Finding No. 1163: This proposed finding is misleading and contrary to the weight of the evidence. The proposed finding is misleading because it cites Professor McAfee for his analysis of a hypothetical event that he believed had no significant possibility of occurring. (McAfee, Tr. 11309-11310). The question of whether JEDEC would have issued a RAND letter was not one studied by Professor McAfee for his direct testimony. (McAfee, Tr. 7680-81).

The proposed finding is contrary to the evidence because had Rambus disclosed to JEDEC that it thought it had intellectual property on the developing standards, JEDEC members would then have known about that intellectual property, and the clear weight of the evidence is that JEDEC members sought to avoid intellectual property issues relating to the JEDEC standards and, so would have worked around that intellectual property. (CCFF 107-111, 300-304, 2101, 2447-2453).

1164. While Complaint Counsel's economic expert testified that JEDEC would not have adopted Rambus's technologies, he based his opinions on the assumption that if JEDEC were informed of a patented technology, it would not proceed to adopt that technology into a standard without first requesting a RAND assurance. (McAfee, Tr. 7672). Complaint Counsel's economic expert made no study of JEDEC behavior in arriving at this assumption.

Response to Finding No. 1164: Complaint Counsel agrees that Professor McAfee testified that JEDEC would not have adopted Rambus's technologies if Rambus had disclosed its intellectual property rights.

The assertion in this proposed finding that Professor McAfee made no study of JEDEC behavior is inaccurate. Dr. McAfee testified that he reviewed the JEDEC minutes specifically to understand JEDEC's behavior. (McAfee, Tr. 11323-11324).

1165. Complaint Counsel's economic expert also admitted that if JEDEC was aware of patents that applied to SDRAM and not to previous generations of DRAM, and if JEDEC went forward with SDRAM without requesting a RAND letter, that would impact his assumption that JEDEC requires a RAND letter and therefore impact his opinions that rely on that assumption. (McAfee, Tr. 7708). As discussed above, JEDEC did go forward with the SDRAM standard despite knowing of applicable patents and without seeking RAND letters. As Complaint Counsel's expert testified it would, this evidence casts doubt on the validity of his assumption that a RAND letter was required in all circumstances.

Response to Finding No. 1165: Complaint Counsel does not disagree that Professor McAfee testified that "if JEDEC was aware of patents that applied to SDRAM and not to previous generations of DRAM, and if JEDEC went forward with SDRAM without requesting a RAND letter, that would impact his assumption that JEDEC requires a RAND letter and therefore impact his opinions that rely on that assumption."

The remaining passage in this proposed finding is without reference in the record and is contrary to the weight of the evidence. For a discussion of the evidence that JEDEC members did not have knowledge of the Rambus intellectual property when it developed the SDRAM standards, *see* CCFF 1238-1357.

1166. There was, in addition, an example in the 1995-1996 time frame where a RAND letter was *not* requested by an EIA standards body despite an assertion by an EIA member that it possessed a patent relating to the standard. In that case, an EIA member called Echelon gave notice to an EIA standards body, the Consumer Electronics Association ("CEA") that it had an issued patent that might cover a technology included in a CEA standards proposal. As discussed below, the EIA body chose not to ask for RAND assurances. (Kelly, Tr. 2122-3).

Response to Finding No. 1166: This proposed finding is incomplete because it omits evidence that the EIA body involved, the CEA, "chose not to ask for RAND assurances" because it appeared to the organization that Echelon had disclosed in bad faith, and so would not

provide those assurances. (Kelly, J., Tr. 2170 ("In this case, in the Echelon case, there was clear indication of bad faith.")).

The reason that the CEA believed that Echelon was acting in bad faith was that Echelon had spent a number of years openly attempting to halt the progress of the CEA standard, called "CEBus." (J. Kelly, Tr. 2158-2159). Prior to disclosing its patent to the CEA, Echelon had made it clear to the organization that it was very interested in stopping the progress of the standard. (J. Kelly, Tr. 2159-2160 ("They hired an attorney in Washington who contacted me on several occasions and indicated that if the standard-setting went forward that they would litigate in every forum available to them, and he also lobbied on Capitol Hill for legislation to block the standard-setting activity."); J. Kelly, Tr. 2165 ("[T]his entire process or this entire effort by Echelon was designed to stop the process, block the process, by their own admission, either through litigation or through legislation or otherwise.")).

When Echelon made a patent disclosure to the CEA, Echelon did not disclose why it believed the patent was relevant to the standard. (J. Kelly, Tr. 2160-2161 ("Chris pretty consistently indicated that the corporate position of Echelon was to block the ... standard, and at one meeting in particular he -- and I think I testified to this earlier -- proffered to me a copy, which was about six inches thick, maybe four inches thick, but it was a substantial document, which was an issued U.S. patent and he said, here, this may be relevant to something you're working on, take it for what it's worth, we just want to be covered.")). Despite repeated attempts by the CEA to clarify why the patent was relevant to the proposed standard, Echelon never disclosed why it believed the patent was relevant. (J. Kelly, Tr. 2161-2162).

In its disclosure of its patent to the standardizing committee, Echelon stated about its patent that: "Although Echelon cannot at this time determine whether use of its intellectual property is required by firms building CEBus-compatible power line devices, it might be the case

that CEBus power line transceivers would fall within the scope of the Echelon patent." (RX2300-001 at 5). In response, the CEA wrote back to Echelon that Echelon's disclosure still failed to disclose how the patent was necessary to practice the standard. (RX2299-001 at 2 (The ANSI and EIA patent policy "requires an SDO to secure a commitment to license a patented item or process from a patent holder when a standard refers to a patented technology or, as a practical matter, conformance to a standard requires use of the patented technology.... Echelon has been unable to explain or document how the CEBus standard refers to or requires use of any of Echelon's patented technology.")).

Given the circumstances, the CEA believed that the Echelon patent disclosure was not a good faith patent disclosure but a bad faith continuation of its attempts to halt the progress of the CEA standard. (J. Kelly, Tr. 2167 ("[I]t appeared to me and to others that this was the fulfillment of the threat that was made in our very first meeting with Echelon where they said: We will stop you. If it takes a million dollars, we'll stop you."); J. Kelly, Tr. 2167 ("Again, this was a special kind of situation in which there was an announced, in advance, an announced strategy to block the process and in a way that to me and to many others indicated bad faith. And that was why we dealt with the situation specially and that was really what I wanted to bring out this morning and may not have fully done so."); CCFF 332).

1167. Echelon was a participant in the standards-setting process that had voted against the proposed standard. Echelon was promoting its own technology in competition with certain technology included in the standard. (Kelly, Tr. 2122).

Response to Finding No. 1167: This proposed finding is incomplete for the reasons described in CCRF 1166.

1168. EIA General Counsel John Kelly was personally involved in the Echelon situation. He testified that RAND assurances were not sought from Echelon because "it appeared to us at the time . . . that Echelon was deliberately trying to impede the process, to stall it out for its own purposes . . . ." (Kelly, Tr. 2135).

Response to Finding No. 1168: This proposed finding is incomplete for the reasons described in CCRF 1166.

1169. Mr. Kelly testified that after Echelon asserted that it had a patent related to the standard, it tried to insist that the EIA request a RAND assurance from it under the EIA Patent Policy. (Kelly, Tr. 2166-7).

Response to Finding No. 1169: This proposed finding is incomplete for the reasons described in CCRF 1166.

1170. Mr. Kelly believed that Echelon was asserting its intellectual property claims, and insisting upon receiving a request for RAND assurances, in a bad faith effort "to block the process" of standardization. (Kelly, Tr. 2167). Mr. Kelly also believed that it was "reasonably clear" that "we weren't going to get those licensing assurances" from Echelon. (Kelly, Tr. 2166-7). Mr. Kelly believed that if a request for RAND assurances was made to Echelon, Echelon would refuse to give those assurances, and the standardization process would necessarily come to a stop. (Kelly, Tr. 2165-7).

Response to Finding No. 1170: This proposed finding is incomplete for the reasons described in CCRF 1166.

1171. The Echelon case thus provides useful insights into how JEDEC may have reacted if Rambus had announced that its patent applications might relate to features under consideration for inclusion in the SDRAM or subsequent standards. The evidence shows that: (1) Rambus, like Echelon, was promoting its own memory device in competition with the JEDEC standard device; (2) on the three occasions when Rambus's potential intellectual property interests were explicitly discussed at JEDEC meetings while Rambus was a member, JEDEC representatives expressed the view that Rambus's patents, if they issued, would be barred by prior art; (3) similar views about prior art were aired on the occasions when Rambus's potential intellectual property interests were raised at SyncLink meetings and at JEDEC meetings after Rambus left JEDEC; and (4) the chair of the SyncLink standards committee believed that Rambus was trying to "torpedo" the SyncLink standard by asserting invalid IP claims. In light of this evidence, there is a strong possibility that the JC 42.3 committee would have believed that Rambus, like Echelon, was trying to trigger a request for RAND assurances, which assurances it would then decline to give, in the hopes of using its intellectual property disclosures to bring the SDRAM or DDR SDRAM standardization process to a halt.

Response to Finding No. 1171: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1172. The concern that standard-setting organizations could be gamed in this manner was shared by others in the industry. For example, SyncLink Consortium Secretary David Gustavson testified that he was concerned about the issue:

> "My concern was that any person who wished to block a standard could simply assert that they had patents applied for which would interfere with that standard, and if they refused to say that they would make their patents available on a nondiscriminatory basis to others it would be impossible for the standard to complete. In my view it would make it possible for every standard in the IEEE to be blocked by a single individual."

(Gustavson, Tr. 9296). Dr. Gustavson expressed this same concern in an email to the IEEE. (RX 675 at 1 (complaining that the IEEE patent policy would allow a party to assert that it has a patent claim that would be infringed, block the standard, and the policy does not allow the IEEE to ensure the validity of the claim)). In fact, Dr. Gustavson believed that this situation occurred when Rambus claimed it had patent applications covering RamLink. (Gustavson, Tr. 9297).

Response to Finding No. 1172: The testimony cited in this proposed finding was allowed over a relevance objection only on the basis that it related to lock-in testimony of Professor McAfee. The testimony as cited here is clearly not being cited for that purpose and should be disregarded. (Gustavson, Tr. 9295-9296).

This proposed finding also is irrelevant for the reasons discussed in CCRF 1491-1492. IEEE was a separate organization to JEDEC with a different membership and patent disclosure rules. The IEEE membership were individuals rather than companies (CCFF 1502) and the IEEE procedures did not impose any obligation on companies with respect to patent disclosure. (CCFF 1503). Dr. Gustavson testified that he has never been a member of JEDEC and has no knowledge of the JEDEC disclosure policy. (Gustavson, Tr. 9316)

Further, the proposed finding does not support Respondent's contention that had Rambus made the disclosures described by Complaint Counsel, JEDEC might have proceeded without seeking a RAND assurance from Rambus. In fact, Dr. Gustavson's testimony suggests just the opposite. When made aware of Rambus patents, IEEE did not proceed. Rather it suspended balloting of the Ramlink standard because of concerns about the Rambus intellectual property.

(Gustavson, Tr. 9292). It then sought RAND assurance from Rambus. (CCFF 1538). When Rambus refused to give such an assurance, the IEEE requested that the Ramlink working group redesign the Ramlink standard so that it wouldn't violate Rambus patent claims. (Gustavson, Tr. 9296-9297; CCFF 1540).

1173. Additional evidence on this point comes from the reactions of Micron's JEDEC representatives in April 1997, when they learned from Micron's Intel account representative that "Rambus plans legal action to request royalties on all DDR memory efforts." (RX 920 at 2).

Response to Finding No. 1173: This proposed finding is misleading. The cited evidence does not support the proposition that "Micron's JEDEC representatives in April 1997, . . . learned from Micron's Intel account representative that 'Rambus plans legal action to request royalties on all DDR memory efforts.'" Instead, RX0920 indicates that an Intel account representative from Micron heard from an Intel employee that *he* understood that "Rambus plans legal action to request royalties on all DDR memory efforts." (RX0920 at 2). As noted below, this was a report of a rumor, not a statement of belief by Micron. (CCRF 1174).

1174. It appears that neither Mr. Ryan, Mr. Lee nor Mr. Walther, each of whom received this e-mail and each of whom attended JEDEC meetings on behalf of Micron, ever notified JEDEC about the information they had learned regarding Rambus's plans. (Lee, Tr. 6972-3).

Response to Finding No. 1174: This proposed finding is misleading in suggesting anyone at Micron had "information" regarding Rambus' plans for the reasons described in CCRF 1173. Furthermore, the proposed finding is misleading because it implies that Mr. Lee understood that he had information regarding "Rambus's plans." Instead, the weight of the evidence is that Mr. Lee understood that he was receiving rumors regarding Rambus from an Intel employee. (CCRF 1173; Lee, Tr. 6702 ("First of all, it was hearsay. It wasn't actually communicated to us by Rambus. It was third party. Intel said themselves they haven't seen Rambus' IP.")). Furthermore, Mr. Lee testified that Micron had been in communication with Rambus regarding Rambus's RDRAM patents and Mr. Lee expected that Micron would have heard about Rambus patents

regarding DDR SDRAM at that time. (Lee, Tr. 6703 ("Also, we had just -- the time frame here, we had just completed our licensing agreement with Rambus for direct RDRAM a month prior, and in the course of those negotiations, they never claimed or disclosed that they had patents that would relate to any other technology at that time.")).

Furthermore, this proposed finding is incomplete because it omits testimony by Mr. Lee that he was at JEDEC while Rambus was at JEDEC and was aware that Rambus had never disclosed patents or patent applications relating to the standard while Rambus was a member. (Lee, Tr. 6703 ("Rambus was a JEDEC member. They would have had a responsibility to disclose patents that may have related to the SDRAM or DDR work at the time when they were a member.")).

1175. Mr. Walther responded to the information in part by saying that he thought that "changing data on both edges of the clock" was "old technology." (RX 920 at 1).

Response to Finding No. 1175: This proposed finding is vague and potentially misleading for the reasons described in CCRF 1173-1174. Furthermore, the phrase "old technology" is undefined in this finding. Mr. Walther was available to be called as a witness at the hearing to explain what he meant in RX0920 by "old technology," but was never called by Respondent.

1176. Mr. Lee testified that he ignored the information about Rambus's plans "to request royalties on all DDR memory efforts" because he did not "believe this was true." (Lee, Tr. 6981). Instead, he believed that Rambus was trying to spread "misinformation." (Lee, Tr. 6983). As Lee explained, his "thought process was that they were trying to get Intel locked into designing RDRAM in on everything, direct RDRAM, and to try to tell [Intel] they had no other alternative, that they've eliminated all of their competition. . . ." (Lee, Tr. 6982-3).

Response to Finding No. 1176: This proposed finding is misleading for the reasons described in CCRF 1173-1174.

1177. Mr. Lee testified that "it was consistent with [Rambus's] prior behavior that they might tell Intel, 'Oh, we have patents on that, so you can't use DDR. . . .'" (Lee, Tr. 6983).

Response to Finding No. 1177: This proposed finding is incomplete and misleading for the reasons described in CCRF 1173-1174.

Furthermore, the quotation from Mr. Lee's testimony is taken out of context because the remainder of the sentence is "you can't use DDR there either," referring to a specific graphics memory application. (Lee, Tr. 6982-83).

1178. In other words, Mr. Lee believed that Rambus was doing exactly what Mr. Kelly thought Echelon had been doing – asserting intellectual property claims over a competing technology in the hopes of slowing or preventing its marketplace acceptance.

Response to Finding No. 1178: This RPF is misleading for the reasons described in CCRF 1173-1174.

Furthermore, this proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1179. Complaint Counsel's economic expert did not refute the evidence that JEDEC might have proceeded without seeking a RAND letter. In fact, he testified that if JEDEC determines that the technology is not patented, JEDEC may proceed without requesting a RAND letter or RAND assurance even if someone asserts that the technology is covered by a valid patent. (McAfee, Tr. 7676-77).

Response to Finding No. 1179: This proposed finding is not supported by the cited evidence because the testimony is cited for the truth of the matter asserted although it was admitted only as Professor McAfee's discussion of his assumptions regarding whether the JEDEC rules required that JEDEC request a RAND letter and whether the Echelon case is an exception to that rule. The overwhelming weight of the evidence is that JEDEC must obtain a RAND assurance before including a potentially patented technology in the standard. (CX0208 at 19; CX0203A at 11 ("The Committee Chairman must have also received a written expression from the patent holder that he is willing to license applicants under" RAND terms.)). The Echelon case is a

limited exception to the rule where it is clear in advance that the party disclosing the patent is acting in bad faith. (*See* CCRF 1166). Since in the but-for world, the appropriate assumption is that Rambus would have been acting in good faith, the Echelon exception does not apply to this case. (Teece, Tr. 10676-10677).

1180. Complaint Counsel's economic expert further conceded that if, in the but for world in which Rambus made the additional disclosures that Complaint Counsel allege should have been made, JEDEC had determined that the Rambus technology it sought to include into a standard would not be patented, JEDEC might not have requested a RAND letter. (McAfee, Tr. 7678).

Response to Finding No. 1180: This proposed finding is not supported by the cited evidence because the testimony is cited for the truth of the matter asserted although it was admitted only as Professor McAfee's discussion of his assumptions regarding the JEDEC rules. (McAfee, Tr. 7678 ("[T]his is -- the assumptions about JEDEC are assumptions and not -- and not economic conclusions")). This proposed finding also violates Respondent's express agreement to treat this testimony as a discussion of assumptions (Trial Tr. 7679 ("MR. STONE: Your Honor, if I might respond, I'm simply asking the witness questions about the assumptions he has made, and I'm asking him in a hypothetical way. I'm not asking him for any opinion as to these factual issues. JUDGE McGUIRE: I'll entertain that line of inquiry, but let's keep that very much tied to the context of his objection. MR. STONE: I will.")).

1181. Complaint Counsel's economic expert also admitted that he did not consider the possibility that had Rambus made the additional disclosures that Complaint Counsel allege should have been made, JEDEC might have proceeded to incorporate the technology without requiring a RAND letter. (McAfee, Tr. 7680-81). Although Professor McAfee said in his rebuttal testimony that he did not think that there was a significant possibility that JEDEC would not have asked for a RAND letter (McAfee, Tr. 11308), he *also* testified that if JEDEC thought that it was being "gamed" by Rambus, and if JEDEC thought that Rambus was unlikely to obtain patent coverage, it was a "logical possibility" that JEDEC would *not* ask for a RAND letter and would proceed to incorporate in its standards the technologies at issue. (McAfee, Tr. 11331).

Response to Finding No. 1181: This proposed finding is misleading because it implies that Professor McAfee simply disregarded the possibility that JEDEC might have thought

that Rambus was "gaming the system" when he arrived at his initial decision. However, Professor McAfee testified that the but-for world hypothesis in this case must start with the supposition that Rambus had not engaged in the challenged exclusionary conduct. (CCFF 3018-3019). Since in the but-for world, Rambus would have provided the required good faith disclosure, there is no reason to hypothesize that JEDEC would then believe that Rambus was acting in bad faith. (CCRF 1159).

1182. As noted above, the Echelon case, and the reactions by Mr. Lee, Mr. Wiggers and others when they learned of Rambus's intellectual property claims, make this scenario far more than just a "logical possibility."

Response to Finding No. 1182: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

2. If JEDEC Had Sought A RAND Assurance, It Would Still Have Adopted Rambus's Technologies.

1183. If JEDEC would have requested a RAND letter from Rambus, Rambus would have given the RAND assurance and JEDEC would have proceeded to adopt Rambus's SDRAM and DDR technologies.

Response to Finding No. 1183: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

a. Rambus Would Have Given a RAND Assurance.

1184. A RAND letter must state that the patent holder will license its patent either royalty free or on reasonable terms and conditions that are demonstrably free of any unfair competition; in the latter case the royalty rate is not specified in the letter. (Teece, Tr. 10331-32; JX 54 at 9; CX 203A at 11). In this case, given Rambus's business model, an economist would not expect Rambus to agree to license its technology royalty free. (Teece, Tr. 10314, 10331-32; McAfee, Tr.7492-93).

Response to Finding No. 1184: Complaint Counsel does not disagree.

1185. To determine whether Rambus would have provided a RAND letter, it is useful to examine the economic implications of that action.

Response to Finding No. 1185: This proposed finding lacks any reference to the record. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1186. A RAND assurance has three key provisions, each of which has economic implications for the patent holder. (Teece, Tr. 10333).

Response to Finding No. 1186: Complaint Counsel does not disagree.

1187. The first provision is that the patent holder must make licenses available to all interested parties. (Teece, Tr. 10333). This provision means that the patent holder gives up the right to pick and choose to whom it will license. (Teece, Tr. 10334). There is, however, a substantial economic motivation for a patent holder to agree to this provision. Agreeing to the provision makes it likely that firms will be willing to incorporate the patented technology because they are assured of not being frozen out. (Teece, Tr. 10334). The patent holder is therefore likely to receive royalties that it otherwise would not receive. (Teece, Tr. 10334-35). The economic literature teaches that patent holders may be willing to agree to this type of restriction because doing so gives confidence to the licensees that they can use the patent holder's technology and be competitive in the marketplace. (Teece, Tr. 10335).

Response to Finding No. 1187: This proposed finding ignores substantial evidence in the record that, whatever the hypothetical benefit to a firm of agreeing to license to all potential licensees, it was always Rambus's business plan that it needed to be capable of with-holding licenses from firms for strategic reasons. Indeed, in the real world, Rambus refused to promise RAND terms to IEEE and JEDEC for precisely this reason. (CCFF 2427, 2432). One of Rambus's licensing strategies with respect to SDRAM and DDR SDRAM was to with-hold licenses from firms that litigated against Rambus and lost. (CCFF 1992-1994). This demonstrates that Rambus would have been unwilling to offer RAND assurances in the but-for world. (*See* CCFF 3019-3020 (In defining the but-for world the appropriate thing is to change nothing except

the conduct that is challenged. In particular, Rambus's business strategy in the but-for world should mimic its business strategy in the real world.)).

1188. The second provision of a RAND assurance is that the licensor agrees to license on reasonable terms and conditions. (Teece, Tr. 10336). This provision prevents the patent holder from charging unreasonable terms. (Teece, Tr. 10336). This commitment assures the licensees that royalties will not be unreasonable, again making them more likely to adopt the patentee's technology. (Teece, Tr. 10336). A patentee therefore has an economic incentive to agree to this provision. (Teece, Tr. 10337-38).

Response to Finding No. 1188: This proposed finding ignores substantial evidence in the record that while the RAND assurances included the term "reasonable," they did not include royalty rates, leaving the determination of what constituted "reasonable" terms to negotiations between the parties and ultimately the courts. (CCFF 354-356). As a consequence, a RAND assurance does not necessarily ensure that potential licensees will see the royalty rates as reasonable absent *ex ante* negotiations between the parties. (McAfee, Tr. 7492-7493 (" And since a RAND letter doesn't specify a royalty rate, firms are at risk when they've incorporated patented technology that the royalty rates may turn out to be very large. The RAND letter does specify "reasonable," but to a great extent "reasonable" is in the eye of the beholder.")).

1189. In economic terms, reasonable terms and conditions means that the royalty rates are not so high as to negate the offer to license. (Teece, Tr. 10336-37). For example, if the rate is so high that it would put the licensee out of business, the rate is not reasonable. (Teece, Tr. 10337).

Response to Finding No. 1189: This proposed finding is misleading because it fails to account for the differences in "reasonable" rates between rates determined before a firm is locked in to the standard and after a firm is locked in to a standard. Before a firm is locked in to a standard it will not be willing to pay as much for a license as after it is locked in to a standard. (CCFF 2665-2666, 2674-2677). As a consequence of that, where lock-in is a concern, potential licensees are likely to be interested in negotiating with a patent holder *ex ante* (i.e., before the

potential licensee is locked in to the standard). (CCFF 2669). The weight of the evidence is that lock-in is a concern in the DRAM industry. (CCFF 2682-2756).

1190. Reasonable terms and conditions are understood to mean, as they are in the *Georgia Pacific* analysis in patent damages cases, terms to which a willing buyer and a willing seller would agree. (Teece, Tr. 10337).

Response to Finding No. 1190: This proposed finding is misleading for the reasons described in CCRF 1189. Furthermore, this proposed finding is incomplete because even Professor Teece agrees that the mere fact that an *ex post* royalty may have resulted from an arm's length negotiation does not mean that the royalty would be reasonable from the standpoint of what might have been negotiated *ex ante.* (Teece, Tr. 10512-13).

1191. The third provision of a RAND assurance is that the license be demonstrably free of any unfair discrimination. (Teece, Tr. 10338). This provision prevents arbitrary pricing differences among different licensees; it is designed to create a level playing field. (Teece, Tr. 10338). Again, this commitment is often attractive for a patent holder because it makes it more likely that licensees will adopt the patented technology, leading to royalties for the patentee. (Teece, Tr. 10338).

Response to Finding No. 1191: This proposed finding ignores substantial evidence in the record that, whatever the hypothetical benefit to a firm of agreeing to provide licenses that "create a level playing field," it was always Rambus's business plan that it needed to be capable of charging different license rates to different firms. (CCFF 1984-1989). Part of Rambus's whole patent licensing strategy was to demand higher royalty rates from those firms that initially refused to agree to a license. (CCFF 1990). Rambus's RDRAM licensing rates also show a business plan that relies on the ability of Rambus to charge different firms different rates. Rambus charged some firms 2% per DRAM (CCFF 1816), charged other firms 1.5% (CCFF 1824), and still other firms 1% (CCFF 1823). This demonstrates that Rambus would have been unwilling to offer RAND assurances in the but-for world. (*See* CCFF 3019-3020 (In defining the but-for world the appropriate thing is to change nothing except the conduct that is challenged. In

particular, Rambus's business strategy in the but-for world should mimic its business strategy in the real world.)).

1192. From an economic perspective, licensees would be most concerned about the third provision - that licenses be demonstrably free of any unfair discrimination. (Teece, Tr. 10339). A level playing field is more important to firms than the level of royalties because non-discriminatory licenses mean that the firm is not competitively disadvantaged. (Teece, Tr. 10320).

Response to Finding No. 1192: This proposed finding ignores substantial evidence in the record that the principal benefits of open standards are that they ensure that all members of the industry are allowed to practice the standard and that firms cannot be arbitrarily excluded. (CCFF 300-304; 316-317; Heye, Tr. 3716 ("Open standards is a term that says that there's a standard that is available to be used in the industry that is -- that effectively is royalty free, that if you follow the standard, one, you will be able to interact with other folks using that standard, and that there's basically no royalties associated with it.")).

1193. Economic analysis leads to the conclusion that if JEDEC had asked Rambus to provide a RAND letter, Rambus would have provided such a commitment. (Teece, Tr. 10340-41). First, in the but-for world in which Rambus makes the additional disclosures Complaint Counsel contends should have been made, Rambus would have already lost any benefits of keeping that information confidential. (Teece, Tr. 10344). Agreeing to give a RAND assurance at that point therefore involves less of a sacrifice. (Teece, Tr. 10344).

Response to Finding No. 1193: This proposed finding is misleading and contrary to the weight of the evidence. As described above, an examination of the economic implications of issuing a RAND letter indicates that Rambus would have considered doing so to be contrary to its business plans. (CCRF 1187-1192). Furthermore, the weight of the evidence is that Rambus itself considered issuing a RAND letter to be contrary to its business plans and refused to agree to license its technologies on RAND terms each time it was asked. (CCFF 2419-2432). RAND assurances are critical to JEDEC's ability to produce open standards. (J. Kelly Tr. 1776-1778; CCRF 1192). But open standards were at odds with Rambus's business model. (CX0903 at 2; Crisp, Tr. 2942-2943).

1194. Second, in Complaint Counsel's "but-for world," where commercially feasible alternatives to Rambus's technologies exist, Rambus would have been confronted with the choice of giving a RAND letter and obtaining royalties or potentially seeing its technologies excluded from the standard and not receiving royalties. (Teece, Tr. 10344-45). Rambus never had to make that choice in the real world. Rambus is a pure-play licensing company. That is, Rambus does not manufacture DRAM, but rather uses research and development to invent new DRAM technologies and makes its money by licensing its technology to others. (Teece, Tr. 10350-51). If Rambus does not license, it goes out of business. (Teece, Tr. 10341). Rambus therefore has an economic incentive to agree to terms that make it possible for it to license its technology. (Teece, Tr. 10341). If it does not give a RAND assurance, it forces JEDEC to look at alternative technologies. (Teece, Tr. 10345). But given Rambus's business model, it does not want JEDEC to look at alternatives; it wants JEDEC to adopt its technologies so that it can obtain royalties. (Teece, Tr. 10345).

Response to Finding No. 1194: This proposed finding is misleading and contrary to the weight of the evidence for the reasons described in CCRF 1193.

The statement in this proposed finding that Rambus "has an economic incentive to agree to terms that make it possible for it to license its technology" is misleading because it implies that Rambus believed that it received the same benefits from licensing SDRAM and DDR SDRAM as it did from licensing RDRAM. The weight of the evidence is that Rambus believed it obtained a greater benefit from the success of RDRAM. While Rambus was at JEDEC, its principal concern was that its own proprietary RDRAM succeed and JEDEC compliant SDRAM and DDR SDRAM fail. (Crisp, Tr. 2933 ("Q: You didn't have any particular interest in seeing JEDEC succeed in developing a widely used standard for SDRAM, did you? A: I think that answer is correct, yes. Q: You also didn't have any interest in seeing JEDEC succeed in developing a widely used standard for DDR SDRAM, did you? A: I was not interested in seeing potential competitive devices appear on the market."); CCFF 822-833, 1238-1240). Rambus considered JEDEC-compliant DRAM to be a source of competition for RDRAM. (CCFF 804-805). After Rambus began suing DRAM manufacturers, Rambus pursued a strategy of licensing DDR SDRAMs only at royalty rates higher than those charged for RDRAM in order to encourage the adoption of RDRAM. (CCFF 1977-1980).

Complaint Counsel does not disagree with the statement in this proposed finding that "Rambus never had to make that choice in the real world," as Rambus never disclosed its intellectual property to JEDEC. (CCFF 1238-1259).

1195. This incentive is especially great if there are in fact alternatives to Rambus's technologies. (Teece, Tr. 10341-42). If there were good alternatives to Rambus's technologies, Rambus would clearly have given a RAND assurance because refusing to do so would have cost it the opportunity to get significant revenue from licensing. (Teece, Tr. 10343). In that situation, it would have been economically irrational for Rambus to refuse to give a RAND letter. (Teece, Tr. 10345).

Response to Finding No. 1195: This proposed finding is misleading and contrary to the weight of the evidence for the reasons described in CCRF 1193 and 1194. First, as described in CCRF 1193, RAND licensing was in conflict with Rambus's business model. Second, as described in CCRF 1194, Rambus obtained a benefit by hindering the SDRAM standards in order to encourage the adoption of RDRAM.

This proposed finding is also misleading because it assumes that if Rambus had issued a RAND letter, JEDEC would have agreed to include their technologies in the JEDEC standards. (CCFF 2433-2440). In particular, because of lock-in and hold-up concerns in the DRAM industry (CCFF 2682-2756), the existence of alternatives means that JEDEC would have had a strong incentive to avoid using Rambus technologies in the JEDEC standard even if Rambus issued a RAND letter. (CCFF 3029-3033).

1196. This conclusion is consistent with the views of Complaint Counsel's economic expert. First, he admitted that his starting point would be that whatever information was known to JEDEC about alternative would be known to Rambus. (McAfee, Tr. 7729). Second, he admitted that one of the risks that Rambus would face if it chose not to give a RAND letter in the but-for world would have been that JEDEC would adopt a non-infringing alternative. (McAfee, Tr. 7729).

Response to Finding No. 1196: This proposed finding is misleading because it implies that Professor McAfee's opinion was consistent with the view that Rambus would have issued a RAND license. In fact, Professor McAfee testified that he thought there was a significant

likelihood that Rambus would not issue a RAND letter. (McAfee, Tr. 11311 ("In my understanding of Rambus' business strategy -- and I should say the business strategy that one uses in the but-for world should mimic the business strategy one sees in the actual world, and so the actual business strategy would be the relevant strategy -- I see not a certainty but a significant likelihood that Rambus would refuse to issue a RAND letter. In fact, I think more likely than not they may refuse to issue a RAND letter, based on their business strategy.")). Professor McAfee found that there would be costs to Rambus of issuing a RAND letter, including the lost possibility of delaying the JEDEC stadards by forcing JEDEC to pursue alternative technologies and the lost ability to charge royalties that would violate a RAND commitment. (McAfee, Tr. 7731).

1197. The conclusion that Rambus would have given a RAND letter is not affected by speculation that Rambus might have gained some marketplace benefit for RDRAM by refusing to give a RAND assurance. (Teece, Tr. 10345-46). Especially if there were alternatives to Rambus's technologies, any benefit to Rambus's goal of increasing the acceptance and sales of RDRAM that might flow from a refusal to give a RAND assurance for SDRAM and/or DDR would be minimal or nonexistent. (Teece, Tr. 10346). Moreover, giving a RAND assurance would lead to royalties in hand for Rambus rather than a mere potential benefit to RDRAM. (Teece, Tr. 10739-40).

Response to Finding No. 1197: This proposed finding is misleading and ignores substantial evidence in the record because it assumes that Rambus would not obtain an independent benefit from delaying the SDRAM standards. (*See* CCRF 1194). In particular, changing the standards to avoid the Rambus patents could have taken a significant period of time and delayed the introduction of the standards. (*See* CCFF 2564- 2573). It also ignores substantial evidence in the record that making a patent disclosure and refusing to offer RAND assurances has been used in the past to hinder EIA standards, where the patent holder has a competing product. (*See* RPF 1166-1167, CCRF 1166-1167).

1198. Finally, the conclusion that Rambus would have issued a RAND letter if asked is bolstered by the fact that the DRAM industry exhibits fairly rapid technological change. (Teece, Tr. 10346-47). Rambus is a "repeat player"; that is, its business model is such that it will often be engaging in licensing in the DRAM industry as it develops new technologies. (Teece, Tr. 10346-47). Rambus therefore has an incentive to behave in a reasonable and cooperative manner because

it is building an ongoing technology company (Teece, Tr. 10347), and it therefore has incentive to give a RAND letter because it wants to build relationships with the licensees for the future. (Teece, Tr. 10740-41).

Response to Finding No. 1198: This finding ignores substantial evidence in the record that Rambus did not see itself as a "repeat player" with an incentive to "behave in a reasonable and cooperative manner." In particular, the relationship between Rambus and the DRAM manufacturers was hindered by Rambus's attempts to extract higher payments from DRAM manufacturers making RDRAM than Rambus originally agreed to receive. (CCFF 1829; MacWilliams, Tr. 4841 ("I think, yeah, in general we heard back from the DRAM vendors many times that Rambus was taking maximum advantage of their position.")). This led Intel employees to believe that they should have negotiated a license for the entire industry when they adopted RDRAM. (RX1532 at 2 ("Intel made a decision NOT to negotiate a contract for the memory vendors . . . In retrospect, this was a mistake . . . RamBus took advantage of the memory vendors.")). The relationship between the DRAM manufacturers and Rambus got so bad that Intel attempted to improve those relations in order to improve the adoption of RDRAM but failed. (CCFF 1862-1866). By the Fall of 1999, just before Rambus began pursuing royalties against the DRAM industry, Intel doubted that Rambus was capable of working with the DRAM industry. (CCFF 1912-1914). By the time Rambus began suing the DRAM manufacturers, Intel saw those lawsuits as simply "yet another step in poisoning the industry," which led to the concern at Intel that the DRAM vendors "might not even want to do business with Rambus in the future." (CCFF 2002).

1199. Evidence that Rambus was concerned about agreeing to a RAND policy does not change this conclusion. First, in the but-for world, unlike the real world, Rambus has already disclosed its trade secrets. (Teece, Tr. 10716).

Response to Finding No. 1199: This proposed finding is vague and misleading because Rambus's concerns about agreeing to a RAND policy would have also had to have been in

the context of having disclosed its intellectual property. (J. Kelly, Tr. 1837-38 (The EIA/JEDEC patent policy "requires an early disclosure of intellectual property; that is, patents or patent applications that are or may be related to the work of a standard-setting committee. And then once the disclosure -- the early disclosure is made, if the patent owner is willing to give reasonable assurances that I alluded to earlier, that is, reasonable and nondiscriminatory licensing terms or without charge.")).

1200. Second, evidence that Rambus might have been reluctant in the actual world to give a RAND letter is affected by the fact that Rambus had apparently misunderstood what a JEDEC RAND assurance required. Had Rambus been confronted with a request from JEDEC to provide a RAND letter, it would have had an incentive to seek to determine what that commitment entailed. (Teece, Tr. 10716-17).

Response to Finding No. 1200: The first sentence of the proposed finding is not supported by record evidence, and Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. There is no evidence that Rambus misunderstood what a JEDEC RAND assurance required, and in fact the weight of the evidence strongly suggests Rambus would not have agreed to RAND requirements. (*See* CCFF 1091, 1535 - 1539, 2418 - 2432).

1201. This conclusion is supported by Rambus's conduct in December 1995 – just before Rambus left JEDEC – when Rambus was considering proposing the R-Module technology for standardization at JEDEC. Because Rambus realized that *proposing* a technology at JEDEC might require it to agree to license on RAND terms, Richard Crisp made inquiries about what RAND entailed. (Crisp, Tr. 3479-82). When he did so, Mr. Crisp learned from Mr. Sussman that "reasonable" terms and conditions meant "almost anything we wanted it to mean." (Crisp, Tr. 3480-81; CX 711 at 188). After learning this, Mr. Crisp wrote an e-mail to others at Rambus explaining, "So the conclusion I reach here is that we can abide by the patent policy on a case-by-case basis, are free to set the terms of our license arrangements to what we like (as long as we agree to license all-comers to build our modules), and we give up nothing else in the process." (CX 711 at 188; Crisp, Tr. 3483). He then concluded that with regard to RAND, the JEDEC policy was not "nearly as onerous as some of us had earlier believed." (CX 711 at 188; Crisp, Tr. 3483).

Response to Finding No. 1201: The Finding is misleading in that it references "Rambus's conduct" when in fact the only cited evidence is an email from Mr. Crisp recommended that Rambus consider agreeing to RAND terms. In fact, two months later, in February 1996. when confronted with a letter from the IEEE specifically referencing RAND requirements, Rambus' in-house counsel, Mr. Diepenbrock, Rambus' in-house intellectual property attorney, responded quickly to dispel any notion that Rambus would agree to be bound by RAND terms. (Diepenbrock, Tr. 6223-24; *see* CX0869, responding to CX0490). Agreeing to license on RAND terms was inconsistent with Rambus' business practices. (Diepenbrock, Tr. 6228; accord, CX0903 at 3 (JEDEC-type standards in "open conflict" with Rambus buisness model). Rambus has never submitted a RAND assurance letter to JEDEC or any other standard-setting body. (Diepenbrock, Tr. 6228-29).

1202. This evidence shows that (1) Rambus mistakenly believed that the RAND requirements were "onerous" and (2) when motivated to understand the RAND requirement, Rambus made inquiries in that regard. In the but-for analysis, therefore, it is reasonable to conclude that had Rambus been confronted with a request from JEDEC for a RAND letter concerning the technologies incorporated in SDRAM or DDR, it would have sought to understand the details of that commitment and would have dispelled its misunderstandings.

Response to Finding No. 1202: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1203. In contrast to this analysis, Complaint Counsel's economic expert admitted that he was unable to determine whether or not Rambus would have given a RAND letter in the but-for world (McAfee, Tr. 7730, 11333), and he admitted that he could not say "one way or the other" if it would have been in Rambus's economic interest to issue a RAND letter in the but-for world. (McAfee, Tr. 7733).

Response to Finding No. 1203: This proposed finding is incomplete because Professor McAfee testified that he believed that, while he could not state for certain whether

Rambus would have provided a RAND letter in the but-for world, he thought it was more likely that they would not. (CCRF 1196; McAfee, Tr. 11333 ("If I had only looked at their business plan, I would have concluded that they would have refused a RAND letter. But because they had an economic interest associated with issuing a RAND letter, as well as an economic interest in refusing a RAND letter, I was unable to more precisely say which was the more likely outcome, but yes, I have taken the economic incentives into account.")).

b. <u>There Would Not Have Been Any *Ex Ante* Negotiations</u>.

1204. Complaint Counsel's economic expert testified that once Rambus issued a RAND letter, JEDEC members would have an "incentive" to engage in *ex ante* negotiations, i.e., to negotiate with Rambus prior to the adoption of Rambus's technologies into the SDRAM and DDR standards. (McAfee, Tr. 7493-94). Complaint Counsel's economic expert also testified that if one firm engaged in *ex ante* negotiations with Rambus, that firm would "report" the royalty rates back to other JEDEC members. (McAfee, Tr. 7494). This analysis, however, is flawed. Firms have incentives to do lots of things that they do not actually do; a proper analysis must take into account all the pertinent factors, including those that would have prevented JEDEC members from asking on any incentive to negotiate *ex ante*. (Teece, Tr. 10353-54). Moreover, any such licensing negotiations would be done under confidentiality agreements (Teece, Tr. 10352-53), and companies would, or should, avoid such an exchange of pricing information because of antitrust concerns.

<u>Response to Finding No. 1204</u>: This proposed finding is inaccurate because it implies that Professor McAfee did not consider "all the pertinent factors, including those that would have prevented JEDEC members from asking on any incentive to negotiate *ex ante*." Even after hearing Professor Teece's testimony describing those factors, Professor McAfee continued to believe that *ex ante* negotiations were possible. (McAfee, Tr. 11313 ("Professor Teece has ruled out ex ante negotiations as not arising and I find that ex ante negotiations are a possibility.")).

1205. Here, *ex ante* negotiations would have to have occurred before Rambus's patents issued. Rambus's first patents that covered JEDEC-compliant products issued in mid-1999. *See* Findings ¶ 431.

<u>Response to Finding No. 1205</u>: The statement in this proposed finding, that Rambus's first patents that covered JEDEC-compliant products issued in mid-1999, is contrary to

the weight of the evidence that Rambus possessed patents and patent applications that read on JEDEC-compliant products while Rambus was still at JEDEC in 1996. (CCFF 1122-1237).

1206. Despite the opinion expressed by Complaint Counsel's economic expert regarding the likelihood of *ex ante* negotiations involving JEDEC members, there is no evidence of any *ex ante* negotiations occurring in the DRAM industry.

Response to Finding No. 1206: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding ignores substantial evidence in the record that such negotiations did in fact occur. Indeed, *ex ante* negotiations occurred between Rambus and some of its licensees: Samsung and Hyundai negotiated provisions in their RDRAM agreements relating to "other DRAMs in 1994 and 1995, respectively, as insurance just in case Rambus intellectual property extended beyond RDRAMs. (CCFF 1544-49; 2455-61). There are other examples of ex ante negotiations in the industry as well. For example, Kentron Technologies engaged in *ex ante* licensing with members of JEDEC. Robert Goodman, the president of Kentron Technologies testified that its "FEMMA" module technologies were presented to JEDEC. (Goodman, Tr. 5995-5996). Mr. Goodman further testified that Kentron Technologies then approached the DRAM industry in an attempt to license its technologies to the DRAM manufacturers in return for royalty payments. (Goodman, Tr. 6020 ("We had approached the industry with -- specifically with the FEMMA technology under a royalty-based license model.")). Since the FEMMA technologies have not been standardized at JEDEC, these were *ex ante* negotiations. (Goodman, Tr. 6073).

This proposed finding is also misleading because it implies that the amount of evidence of *ex ante* licensing indicates that technologies are incorporated into JEDEC standards without a license. This implication ignores substantial evidence in the record that there would be little

evidence of royalty-based *ex ante* licensing of JEDEC-standard technologies because the industry is not willing to include technologies into the standard that are encumbered by royalty payments without cross licenses. This implication also ignores substantial evidence in the record that the DRAM industry is characterized by broad cross licenses which might cover technologies being incorporated into the standard.

The weight of the evidence is that the DRAM industry avoids putting royalty-bearing technologies into the JEDEC standards. (CCFF 107-111, 300-304, 2446-2454, 3029-3033). For example, during the *ex ante* negotiations with members of the DRAM industry, Mr. Goodman began to understand that the DRAM industry does not incorporate royalty-bearing technologies into the JEDEC standards. (Goodman, Tr. 6020-6021 ("We basically were hearing that in general, people do not like paying royalties. They do not like the concept of having quarterly reports, quarterly payments, audit activities, and they considered that just a general royalty-based approach was not one that they viewed as being popular.")). Based on his experiences in attempting to negotiate *ex ante* licenses with the DRAM industry, Mr. Goodman changed Kentron's licensing strategy to a royalty-free licensing strategy. (Goodman, Tr. 6021 ("We had clearly received a message from the industry that a royalty-based approach was not one that had a high level of success for FEMMA and QBM.")).

Finally, this proposed finding is misleading because it ignores substantial evidence in the record that licenses in the DRAM industry are cross-licenses, where any new patent or patent application gets merged into already existing licenses between the companies in the industry. (Appleton, Tr. 6301 ("[A]ll of the royalties that we have paid historically was for what we know in the industry as broad patent cross-licenses. The royalties that we were paying were associated with the entire semiconductor product, if you will. So, it didn't really matter -- it didn't matter what type of device we were making, and it didn't really matter whether we were using a particular process.

The royalties were associated with a very broad patent cross-license."); Teece, Tr. 10639 ("Typically, you know, IBM would cross-license. I'm not aware of a specific, individual, stand-alone license that relates to a DRAM.")). As a result, even if technologies were being incorporated into the standard, there would be no evidence of *ex ante* licensing because firms in the industry would be licensed under broad cross licenses.

1207. There is also no evidence of *ex ante* negotiations for naked licenses for patent applications outside of the DRAM industry. (Teece, Tr. 10354). Professor Teece, who has studied licensing for over 20 years, did not know of a single example of a negotiation of a naked license for a patent application. (Teece, Tr. 10356, 10360).

Response to Finding No. 1207: This proposed finding is irrelevant and unreliable. This proposed finding is irrelevant because, by its terms it only applies outside of the DRAM industry. This proposed finding is unreliable because it is based solely on the *ipse dixit* of Professor Teece, who provided no supporting evidence. Furthermore, this proposed finding is misleading for the reasons described in CCRF 1206.

1208. There are several economic reasons for the absence of negotiations before patents issue. First, because patent applications are a bundle of rights that has not matured, the parties do not know for what they are bargaining. (Teece, Tr. 10357). Patent applications often change during the course of prosecution - claims get amended, claims get withdrawn, claims are abandoned - and it is not clear what claims will ultimately issue. (Teece, Tr. 10357-59). There is therefore great uncertainty about the rights that would be negotiated before a patent issues. (Teece, Tr. 10357). In essence, the licensee would buy a "pig in a poke." (Teece, Tr. 10357).

Response to Finding No. 1208: This finding ignores substantial evidence in the record that, whatever difficulties there were hypothetically in licensing patent applications, Rambus was capable of licensing its patent applications. Rambus had license agreements with at least three firms in 1992 (CCFF 740), even though it had only patent applications, and no patents until 1993. (CCFF 971). Furthermore, Rambus license agreements for both RDRAM and SDRAM/DDR SDRAM routinely include provisions licensing patent applications. (CX1600 at 4, 6-7 (RDRAM license with Hyundai); CX1609 at 3,6 (RDRAM license with Mitsubishi); CX1617

at 4,7 (RDRAM license with Siemens); CX1646 at 3,6 (RDRAM license with Micron); CX1680 at 12,19,24 (SDRAM/DDR SDRAM license with Toshiba); CX1681 at 2,3,10 (SDRAM/DDR SDRAM license with Hitachi); CX1683 at 2,7,10 (SDRAM/DDR SDRAM license with OKI); CX1685 at 2,8,12 (SDRAM/DDR SDRAM license with NEC); CX1686 at 2,7,11 (SDRAM/DDR SDRAM license with Elpida); CX1687 at 2,8,11-12 (SDRAM/DDR SDRAM license with Samsung); CX1689 at 2,7-8,13-14 (SDRAM/DDR SDRAM license with Mitsubishi)).

This proposed finding is also irrelevant because it fails to consider the likelihood that had Rambus disclosed, companies would have negotiated with Rambus for rights to make SDRAM at the same time they negotiated for RDRAM licenses. (*See* CCFF 1544-1549, 2455-2461).

1209. Uncertainty is the foundation for disagreements. (Teece, Tr. 10358-59). Because of the uncertainty about what if any claims in an application will issue, negotiations before patents issue are extraordinarily complex, extraordinarily costly, and in the real world, firms do not engage in this type of negotiations with any frequency. (Teece, Tr. 10357).

Response to Finding No. 1209: This finding ignores substantial evidence in the record that, whatever difficulties there were hypothetically in licensing patent applications, Rambus was capable of licensing its patent applications. Rambus had license agreements with at least three firms in 1992 (CCFF 740), even though it had only patent applications, and no patents until 1993. (CCFF 971). Furthermore, Rambus license agreements for both RDRAM and SDRAM/DDR SDRAM routinely include provisions licensing patent applications. (CX1600 at 4, 6-7 (RDRAM license with Hyundai); CX1609 at 3,6 (RDRAM license with Mitsubishi); CX1617 at 4,7 (RDRAM license with Siemens); CX1646 at 3,6 (RDRAM license with Micron); CX1680 at 12,19,24 (SDRAM/DDR SDRAM license with Toshiba); CX1681 at 2,3,10 (SDRAM/DDR SDRAM license with Hitachi); CX1683 at 2,7,10 (SDRAM/DDR SDRAM license with OKI); CX1685 at 2,8,12 (SDRAM/DDR SDRAM license with NEC); CX1686 at 2,7,11 (SDRAM/DDR

SDRAM license with Elpida); CX1687 at 2,8,11-12 (SDRAM/DDR SDRAM license with Samsung); CX1689 at 2,7-8,13-14 (SDRAM/DDR SDRAM license with Mitsubishi)).

This proposed finding is also irrelevant because it fails to consider the likelihood that had Rambus disclosed, companies would have negotiated with Rambus for rights to make SDRAM at the same time they negotiated for RDRAM licenses. (*See* CCFF 1544-1549, 2455-2461).

1210. Moreover, *ex ante* negotiations for a license regarding patent applications involve confidentiality concerns - the negotiations may be an avenue for the parties to discover each other's intellectual property strategies or information about future inventions. (Teece, Tr. 10359). This provides a disincentive to *ex ante* negotiations of this sort. (Teece, Tr. 10358-59).

Response to Finding No. 1210: This finding ignores substantial evidence in the record that, whatever difficulties there were hypothetically in licensing patent applications, Rambus was capable of licensing its patent applications. Rambus had license agreements with at least three firms in 1992 (CCFF 740), even though it had only patent applications, and no patents until 1993. (CCFF 971). Furthermore, Rambus license agreements for both RDRAM and SDRAM/DDR SDRAM routinely include provisions licensing patent applications. (CX1600 at 4, 6-7 (RDRAM license with Hyundai); CX1609 at 3,6 (RDRAM license with Mitsubishi); CX1617 at 4,7 (RDRAM license with Siemens); CX1646 at 3,6 (RDRAM license with Micron); CX1680 at 12,19,24 (SDRAM/DDR SDRAM license with Toshiba); CX1681 at 2,3,10 (SDRAM/DDR SDRAM license with Hitachi); CX1683 at 2,7,10 (SDRAM/DDR SDRAM license with OKI); CX1685 at 2,8,12 (SDRAM/DDR SDRAM license with NEC); CX1686 at 2,7,11 (SDRAM/DDR SDRAM license with Elpida); CX1687 at 2,8,11-12 (SDRAM/DDR SDRAM license with Samsung); CX1689 at 2,7-8,13-14 (SDRAM/DDR SDRAM license with Mitsubishi)).

This proposed finding is also irrelevant because it fails to consider the likelihood that had Rambus disclosed, companies would have negotiated with Rambus for rights to make SDRAM at the same time they negotiated for RDRAM licenses. (*See* CCFF 1544-1549, 2455-2461).

1211. Finally, *ex ante* negotiations for a naked license involving patent applications may require claim contingent licensing – agreements on different royalty rates depending on which claims in the application issue – which adds to the complexity and costs. (Teece, Tr. 10359).

Response to Finding No. 1211: This finding ignores substantial evidence in the record that, whatever difficulties there were hypothetically in licensing patent applications, Rambus was capable of licensing its patent applications. Rambus had license agreements with at least three firms in 1992 (CCFF 740), even though it had only patent applications, and no patents until 1993. (CCFF 971). Furthermore, Rambus license agreements for both RDRAM and SDRAM/DDR SDRAM routinely include provisions licensing patent applications. (CX1600 at 4, 6-7 (RDRAM license with Hyundai); CX1609 at 3,6 (RDRAM license with Mitsubishi); CX1617 at 4,7 (RDRAM license with Siemens); CX1646 at 3,6 (RDRAM license with Micron); CX1680 at 12,19,24 (SDRAM/DDR SDRAM license with Toshiba); CX1681 at 2,3,10 (SDRAM/DDR SDRAM license with Hitachi); CX1683 at 2,7,10 (SDRAM/DDR SDRAM license with OKI); CX1685 at 2,8,12 (SDRAM/DDR SDRAM license with NEC); CX1686 at 2,7,11 (SDRAM/DDR SDRAM license with Elpida); CX1687 at 2,8,11-12 (SDRAM/DDR SDRAM license with Samsung); CX1689 at 2,7-8,13-14 (SDRAM/DDR SDRAM license with Mitsubishi)).

This proposed finding is also irrelevant because it fails to consider the likelihood that had Rambus disclosed, companies would have negotiated with Rambus for rights to make SDRAM at the same time they negotiated for RDRAM licenses. (*See* CCFF 1544-1549, 2455-2461).

1212. The fact that Rambus entered into licenses for RDRAM does not undermine this conclusion. The licenses for RDRAM were not naked patent licenses (licenses that do not include rights other than a right to use the intellectual property). (*See, e.g.,* CX 1592 at 19-21; Teece, Tr. 10355-56) The RDRAM licenses included other provisions such as a technology transfer. *(See, e.g.*, CX 1592 at 19-21; Heye, Tr. 3689-90 (describing circuit design given by Rambus to its licensees that the licensee could "literally drop into our design")).

Response to Finding No. 1212: This proposed finding is unreliable because it is inconsistent with the previous proposed findings describing the testimony of Professor Teece. The

difficulties Professor Teece has associated with *ex ante* licensing of patent applications involved the uncertainties involved in licensing patent applications where the claims have not yet issued (RPF 1208-1209), the potential costs of negotiations that might reveal secret information (RPF 1210), and the difficulties and costs of "claim contingent licensing" (RPF 1211). Nowhere in the findings is it described how these difficulties are resolved if the licensing also includes technology transfers.

1213. Because of these costs and disincentives, *ex ante* negotiations for a naked license involving patent applications do not take place either inside or outside the DRAM industry. (Teece, Tr. 10354-10360).

Response to Finding No. 1213: This finding ignores substantial evidence in the record that, whatever difficulties there were hypothetically in licensing patent applications, Rambus was capable of licensing its patent applications. Rambus had license agreements with at least three firms in 1992 (CCFF 740), even though it had only patent applications, and no patents until 1993. (CCFF 971). Furthermore, Rambus license agreements for both RDRAM and SDRAM/DDR SDRAM routinely include provisions licensing patent applications. (CX1600 at 4, 6-7 (RDRAM license with Hyundai); CX1609 at 3,6 (RDRAM license with Mitsubishi); CX1617 at 4,7 (RDRAM license with Siemens); CX1646 at 3,6 (RDRAM license with Micron); CX1680 at 12,19,24 (SDRAM/DDR SDRAM license with Toshiba); CX1681 at 2,3,10 (SDRAM/DDR SDRAM license with Hitachi); CX1683 at 2,7,10 (SDRAM/DDR SDRAM license with OKI); CX1685 at 2,8,12 (SDRAM/DDR SDRAM license with NEC); CX1686 at 2,7,11 (SDRAM/DDR SDRAM license with Elpida); CX1687 at 2,8,11-12 (SDRAM/DDR SDRAM license with Samsung); CX1689 at 2,7-8,13-14 (SDRAM/DDR SDRAM license with Mitsubishi)).

This proposed finding is also irrelevant because it fails to consider the likelihood that had Rambus disclosed, companies would have negotiated with Rambus for rights to make SDRAM at the same time they negotiated for RDRAM licenses. (*See* CCFF 1544-1549, 2455-2461).

1214. Complaint Counsel's economic expert agreed that *ex ante* negotiations are less likely with respect to a patent application than an issued patent. (McAfee, Tr. 11335). He also agreed that the less certainty there is about the exact scope of a claim and whether or not it would issue, the lower the probability of *ex ante* negotiations. (McAfee, Tr. 11336).

Response to Finding No. 1214: This proposed finding is incomplete because it omits Professor McAfee's testimony that he believed that there would be incentives for DRAM manufacturers to pursue *ex ante* negotiations in the but-for world. (McAfee, Tr. 7492-7493 ("And since a RAND letter doesn't specify a royalty rate, firms are at risk when they've incorporated patented technology that the royalty rates may turn out to be very large. The RAND letter does specify "reasonable," but to a great extent "reasonable" is in the eye of the beholder. And as a consequence, the firms have an incentive for ex ante negotiation; that is to say, the firms that intend to practice the JEDEC standard have an incentive to say, Hey, what's this going to cost me? That is to say, to investigate what does the word "reasonable" mean in the RAND letter.")).

1215. Complaint Counsel's economic expert also admitted that if the potential licensee believed that the pending claims would be invalid or would not issue, it would be less likely to engage in *ex ante* negotiations. (McAfee, Tr. 11336). Here, the evidence shows that JEDEC members believed that Rambus's patents would be invalid or would not issue.

Response to Finding No. 1215: This proposed finding is incomplete for the reasons described in CCRF 1214. The statement in this proposed finding that "the evidence shows that JEDEC members believed that Rambus's patents would be invalid or would not issue," is contrary to the weight of the evidence. (CCFF 1238-1357; CCRF 773-784).

1216. Moreover, according to Complaint Counsel's economic expert, the likelihood of *ex ante* negotiations would be less if Rambus did not have pending claims that actually covered the relevant technologies at the time it gave the RAND letter because, "[i]f nothing else, it makes it harder to describe precisely what is being negotiated about." (McAfee, Tr. 11334-35). As described herein, Rambus did not have any pending claims that actually read on any of the four technologies during the time it was at JEDEC.

Response to Finding No. 1216: This proposed finding is incomplete for the reasons described in CCRF 1214. The statement in this proposed finding, that "Rambus did not have any pending claims that actually read on any of the four technologies during the time it was at JEDEC," is misleading and contrary to the weight of the evidence. (CCFF 1122-1237).

1217. In the but-for world, JEDEC members and Rambus would have recognized the costs of negotiating a license regarding patent applications as opposed to patents. (Teece, Tr. 10396). Complaint Counsel's economic expert agreed that JEDEC members might rationally conclude that the costs of *ex ante* negotiations exceed the costs of waiting to negotiate ex post. (McAfee, Tr. 11337).

Response to Finding No. 1217: This proposed finding ignores substantial evidence in the record that Rambus and its licensees entered into licence agreements regarding patent applications. (CCRF 1208-1211). Presumably both sides of those transactions recognized the costs of negotiating a license regarding patent applications as opposed to patents when they entered into those negotiations. The statement in this proposed finding, that "Complaint Counsel's economic expert agreed that JEDEC members might rationally conclude that the costs of *ex ante* negotiations exceed the costs of waiting to negotiate ex post," is incomplete for the reasons described in CCRF 1214.

1218. Complaint Counsel did not meet their burden of establishing that *ex ante* negotiations would have taken place in the but-for world. (Teece, Tr. 10360-61).

Response to Finding No. 1218: This proposed finding is not supported by the cited evidence as Professor Teece is not competent to testify as to what Complaint Counsel's burdens of proof are or whether Complaint Counsel has met those burdens of proof. In fact the record establishes that if Rambus had disclosed on a timely basis and JEDEC wanted to use the technologies in its standards, JEDEC members likely would have sought to negotiate acceptable royalty rates before becoming locked in to use of the JEDEC standards. (CCFF 2441-64).

c. JEDEC Would Have Adopted Rambus's Inventions With Rambus's RAND Assurance.

1219. Given that Rambus would have given a RAND assurance if asked, there are a number of reasons why JEDEC would have adopted the Rambus technologies. First, as demonstrated above, the alternatives were inferior, even when taking into account Rambus's royalties. (Teece, Tr. 10363, 10365. Second, the theory of revealed preference shows that JEDEC preferred Rambus's technologies. (Teece, Tr. 10365-66). These two points alone are sufficient to show that JEDEC would have adopted Rambus's technologies for both SDRAM and DDR. (Teece, Tr. 10366).

Response to Finding No. 1219: This proposed finding is contrary to the weight of the evidence. First, there is substantial evidence in the record that Rambus would not have given RAND assurances after disclosing its intellectual property. (CCFF3024-3025; CCRF 1184-1203). Second, at most the theory of revealed preferences indicates that JEDEC preferred the four technologies at issue over some of the alternatives when JEDEC thought the four technologies were free. That theory does not indicate what JEDEC would have done if JEDEC members knew the industry might have to pay royalties for the use of the technologies in question. Rather, the weight of the evidence is that, including the cost of the Rambus royalties, there were equal or superior alternatives to the standardized technologies available to JEDEC had Rambus disclosed. (CCFF 2102-2414; CCRF 726; CCRF 969-988).

1220. Third, JEDEC is willing to adopt patented technologies, and it would likely do the same thing with Rambus's technologies. (Teece, Tr. 10371-72). For example, JEDEC adopted the on-chip PLL/DLL technology for DDR knowing that Mosaid had a patent on the technology. (CX 400 at 2).

Response to Finding No. 1220: The statement in this proposed finding that JEDEC is willing to adopt patented technologies is not supported by the cited evidence as Professor Teece is not competent to testify as to the state of mind of JEDEC or the JEDEC members. Furthermore, that statement is contrary to the weight of the evidence. (CCFF 107-111, 300-304, 2446-2454, 3029-3033). The statement in this proposed finding that JEDEC adopted the on-chip PLL/DLL technology for DDR knowing that Mosaid had a patent on the technology, is

incomplete because JEDEC members also knew that the Mosaid patent was an implementation patent that was not required to practice the standard. (CX 400 at 2; *see* CCFF 611-612).

Furthermore, this proposed finding is contrary to the weight of the evidence which shows that JEDEC was generally unwilling to adopt patented technologies and likely would have avoided adopting the Rambus technologies. (CCFF 2433-2440).

1221. JEDEC has repeatedly adopted patented technologies so long as it received a RAND letter. Gordon Kelley, a long time chair of JC42.3 testified that he could not recall any instance in which JEDEC pursued alternatives after receiving a RAND commitment on what the committee thought was the best alternative. (Kelley, Tr. 2707-09). By contrast, Mr. Kelley did recall several instances in which all consideration of alternatives was dropped as soon as a RAND assurance was received. (Kelley, Tr. 2707-09).

Response to Finding No. 1221: The proposed finding is incomplete and contrary to the weight of the evidence. The goal of JEDEC is to avoid of patents wherever possible. (CCFF 300-304). Gordon Kelley testified to this very point. (G. Kelley, Tr. 2396 ("first requirement was to avoid patents")). Mr. Kelley also testified that the first consideration was to avoid patents and next to receive a RAND assurance if avoidance was not possible. (G. Kelley, Tr. 2566 ("the consideration of anything on patents required as a first consideration avoidance and as a next consideration a RAND statement. The ideal RAND statement would be free. The next ideal RAND requirement would be that it would meet the requirements of reasonable and nondiscriminatory.")).

Further, the evidence shows that there were instances of disclosure at JEDEC where the disclosing company had agreed to RAND terms but JEDEC nevertheless chose to investigate and ultimately work around technologies that would have been patented. (CCFF 4233) In fact, even Mr. Kelley's company, IBM, experienced instances of disclosure which were followed by a RAND letter after which JEDEC chose not to pursue IBM's technology. (CCFF 4233) There was testimony that even if RAMBUS had disclosed its intellectual property and provided JEDEC with a RAND letter, JEDEC would have had the option to pursue alternatives to the four technologies at

issue in this case. (CCFF 2435). A further example of JEDEC not pursuing a disclosed technology involved a company called Cypress. (Kellogg, Tr. 5047 ("One very good example I remember was associated with Cypress. Cypress disclosed a patent associated with a PLL power-down mode. ... The committee did consider the alternative of continuing to use the method that Cypress was claiming and that we had standardized, but we also investigated alternatives, and ultimately we did adopt an alternative which – which was somewhat painful but not significantly so, fortunately, in that case, but we did adopt an alternative."); Kellogg, Tr. 5047-5048 (Kentron presentations not included)). There is also evidence of an instance where JEDEC suspected a technology it was discussing (looped back clocking) might be covered by Rambus patents and JEDEC ultimately chose not to pursue the technology. (CCFF 2435-2440)). Finally, Mr. Kelley testified that on two occasions Mr. Crisp asked to make presentations of the Rambus DRAM at JEDEC. On both occasions Rambus refused to give a RAND assurance and Rambus was not permitted to even present as a result. (G. Kelley, Tr. 2486-2489)

This proposed finding is also misleading because it implies that all technologies that have potential patent issues will be accompanied by royalties. This ignores substantial evidence that the DRAM industry is characterized by broad cross licenses. (CCRF 1206). As a consequence, including some patented technologies would not increase the costs of manufacturing JEDEC-compliant DRAMs. The weight of the evidence is that JEDEC avoids technologies where royalty payments are involved. (CCFF 107-111, 300-304, 3029-3033).

The importance of cross licensing is that the absence of cross licenses with a potential intellectual property holder led to the incentive for DRAM manufacturers to attempt to determine licensing costs before getting locked into a standard. (McAfee, Tr. 7493-7494 ("Many of the companies in this industry cross-license with each other; that is to say, they're manufacturers and they each own licenses that have bearing on the behavior of the other and they have cross-license

agreements. The effect of that is that if one of them tries to charge a lot for its patented technology, it has to fear that the others will respond with equal increased charges. Rambus is not in that position in the sense that by virtue of not being a manufacturer, Rambus faces no such risk, no such symmetric risk. And the effect of that is to make it more likely -- from an economic perspective, it makes it more likely that the firms in the industry, ... would have incentive to seek out and find out what Rambus had in mind when it agreed to charge reasonable royalties."); G. Kelley, Tr. 2640-2641 ("I believe that IBM was concerned, and that might be a better choice than 'feared,' concerned with licensing the royalties for companies that it was not cross-licensed with."); Tabrizi, Tr. 9122).

For example, if Rambus had disclosed its intellectual property at JEDEC one reason why that technology would not have been incorporated into the standard was that JEDEC members feared what Rambus's royalty demands would have been in the absence of cross licenses with Rambus. (Lee, Tr. 6717 ("We have a responsibility in JEDEC to try to avoid the use of patents whenever possible in creating a standard, and also our company has a similar policy, as we try to avoid the use of patents whenever possible. Particularly I'd have to say in the case where Rambus is not a manufacturer, it wouldn't have even been a situation where we could have cross-licensed. So, we would have been strongly opposed [to using the technology in the standard].")).

1222. Similarly, James McGrath, the JEDEC representative for Molex, could not recall a single instance between 1992 and 1996 in which a JEDEC committee changed its course with regard to a standard upon learning of a patent or patent application. (McGrath, Tr. 9243, 9255).

Response to Finding No. 1222: This proposed finding is misleading and contrary to substantial evidence for the reasons described in CCRF 1221.

Further, the proposed finding is unreliable. Mr. McGrath testified that from 1992 through 1996 he did not make an effort to attend JC-42.3 meetings. (McGrath, Tr. 9269). He obviously could therefore not be expected to have any knowledge of the JC-42.3 committee changing its

course with regard to a standard upon learning of a patent or patent application. He simply was not there. (McGrath, Tr. 9263 ('[A] lot of these meetings, especially JC 42.3, I am in and out of those meetings, because a lot of those discussions don't apply to me."); McGrath, Tr. 9265 ("And, again, I didn't pay any attention to the ballots in JC 42.3.")).

1223. During the period when Rambus attended JEDEC, Desi Rhoden could not recall any example of a JEDEC committee trying to find an alternative technology after a JEDEC member disclosed a patent application that in someway related to the technology being standardized and stated that it would license on RAND terms. (Rhoden, Tr. 628-29).

Response to Finding No. 1223: This proposed finding is not supported by the cited testimony as Mr. Rhoden was not asked whether he could recall "any example of a JEDEC committee trying to find an alternative *technology* after a JEDEC member disclosed a patent application that in someway related to the technology being standardized ...." Instead, Mr. Rhoden was asked whether he could recall whether the committee tried to "figure out an *alternative patent* that would not use whatever it was that the patent application related to." (Rhoden, Tr. 629, *emphasis added*).

In any event this proposed finding conflicts with substantial evidence in the record as described in CCRF 1221.

1224. In fact, the meeting minutes show that the JC 42.3 routinely adopted technologies that had patent issues.

Response to Finding No. 1224: RPF 1224 lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to substantial record evidence that JEDEC sought to avoid technologies if royalties might attach to those technologies. (CCRF 1221).

1225. At the May 1990 meeting, JC 42.3 sent a ballot to Council to standardize the 256K x4 MPDRAM technology (JC-42.3-89-48) after receiving a RAND assurance from Digital Equipment Corporation. The minutes state, "This ballot passed but was on hold concerning the patent issue. A patent release letter (see Attachment M) was circulated during the meeting resolving that issue. The ballot will now go to Council." (JX 1 at 6). The "patent release letter" indicated that Digital Equipment Corporation was willing to license the relevant patent for a 1% royalty on sales. (JX 1 at 24).

Response to Finding No. 1225: This finding does not support Respondent's contention that JEDEC would have adopted Rambus's technologies with a RAND assurance. There is no testimony in the record that pertains to the presentation cited in the finding. It is unclear what the patent issue was that is mentioned in the minutes, what MPDRAM technology is, and whether it relates at all to SDRAM. Further, it is impossible to determine from the minutes whether there were alternative technologies for the committee to consider. Also, it is not apparent whether the patented technology was necessary to the standard. There is no evidence as to whether Digital Equipment Corporation had cross-licensing agreements with other JEDEC members.

1226. At the December 1991 JC 42.3 meeting, Siemens disclosed at the time of balloting that it had an issued patent that may cover Extended Data Out for MPDRAM (JC-42.3-91-157). (JX 10 at 9). The committee responded that it was aware of prior art on this patent and unanimously moved to send the ballot to Council assuming the patent issue could be resolved. (JX 10 at 9).

Response to Finding No. 1226: This finding does not support Respondent's contention that JEDEC would have adopted Rambus's technologies with a RAND assurance. There is no testimony in the record that pertains to the presentation cited in the finding. Furthermore, Rambus called no one to testify as to this proposal, and did not ask any witness to testify about the proposal despite the fact that a number of witnesses at the hearing may have had knowledge. (*See e.g.*, Rhoden, Tr. 416; Williams, Tr. 778; Sussman, Tr. 1372; G. Kelley, Tr. 2437-2438; Kellogg, Tr. 599-5100). It is unclear how the Committee believed that the patent issue could be resolved and whether it was in fact resolved. Further, it is impossible to determine from the

minutes whether there were alternative technologies for the committee to consider. Also, it is not apparent whether the patented technology was necessary to the standard.

Furthermore, there is no evidence cited as to whether Siemens had cross-licensing agreements with other JEDEC members that would have minimized the royalty impact of this patent if it applied. The existence of cross-licensing agreements is important to whether members are willing to agree to patented technologies. (Lee, Tr. 6717 ("We have a responsibility in JEDEC to try to avoid the use of patents whenever possible in creating a standard, and also our company has a similar policy, as we try to avoid the use of patents whenever possible. Particularly I'd have to say in the case where Rambus is not a manufacturer, it wouldn't have even been a situation where we could have cross-licensed. So, we would have been strongly opposed."))

1227. At the July 1992 JC 42.3 meeting, the committee considered a ballot for 2M x8/x9 Sync DRAM in TSOP II (JC 42.3-92-83). (JX 13 at 9). At the meeting, Motorola disclosed an issued patent and provided a letter assuring that Motorola would license the patent on a non-discriminatory basis for a reasonable fee. (JX 13 at 9, 136). The committee agreed that the letter met the EIA requirements, and the committee voted to pass the ballot. (JX 13 at 9-10). The item was given Council ballot number 93-13. (JX 16 at 38). At the May 1993 JEDEC Council meeting, the Council passed the ballot and standardized the technology. (CX 54 at 8).

Response to Finding No. 1227: This finding does not support Respondent's contention that JEDEC would have adopted Rambus's technologies with a RAND assurance. Rambus called no one to testify as to this proposal, and did not ask any witness to testify about the proposal despite the fact that a number of witnesses at the hearing may have had knowledge. (*See e.g.*, Rhoden, Tr. 450; Williams, Tr. 816, 898 (examination by Respondent); Sussman, Tr. 1392-1393; Crisp, Tr. 3081; Peisl, Tr. 4519 (examination by Respondent); Grossmeier, Tr. 10968). Consequently, Respondent does not cite to any testimony to support the finding. Therefore, it is impossible to determine from the minutes whether there were alternative technologies for the committee to consider. Also, it is not apparent whether the patented technology was necessary to the standard, and, if so, whether JEDEC members had an understanding of what fee Motorola had

agreed to. There is no evidence cited as to whether Motorola had cross-licensing agreements with other JEDEC members.

1228. At the March 1993 JC 42.3 meeting, the committee voted to pass a ballot on Mode Register Timing (JC-42.3-92-129-1A) for the SDRAM draft specification even though Hitachi commented "patent alert." (JX 15 at 5). At that meeting, the committee voted unanimously to send all SDRAM ballots to JEDEC Council for standardization. (JX 15 at 14). The item was given Council ballot number 93-19. (JX 16 at 39). At the May 1993 JEDEC Council meeting, the Council passed the ballot to standardize this technology. (CX 54 at 9).

Response to Finding No. 1228: This finding does not support Respondent's contention that JEDEC would have adopted Rambus's technologies with a RAND assurance. Rambus called no one to testify as to this proposal, and did not ask any witness to testify about what they understood by the term "patent alert" despite the fact that at least one witness at the hearing may have had knowledge. (G. Kelley, Tr. 2448). Consequently, Respondent does not cite to any testimony to support the finding. Therefore, it is also impossible to determine from the minutes what "patent alert" means, whether there were alternative technologies for the committee to consider or whether the patented technology was necessary to the standard. There is also no evidence cited as to whether Hitachi had cross-licensing agreements with other JEDEC members.

1229. At the March 1993 JC 42.3 meeting, the committee considered a ballot for Write Latency (JC-42.3-92-130A) for the SDRAM draft specification. With regard to this ballot, the minutes state that Mosaid raised a patent issue. (JX 15 at 5-6). The minutes also state, "The Committee is aware of the Hitachi patent. It was noted that Motorola has already noted they have a patent. IBM noted that their view has been to ignore patent disclosure rule because their attorneys have advised them that if they do then a listing maybe construed as complete." (JX 15 at 6). The committee voted unanimously to pass this ballot. (JX 15 at 6). At that meeting, the committee voted unanimously to send all SDRAM ballots to JEDEC Council for standardization. (JX 15 at 14). The item was given Council ballot number 93-20. (JX 16 at 38). At the May 1993 JEDEC Council meeting, the Council passed the ballot to standardize this technology. (CX 54 at 9).

Response to Finding No. 1229: This finding does not support Respondent's contention that JEDEC would have adopted Rambus's technologies with a RAND assurance.

Despite the fact that at least one witness at the hearing was in attendance at the meeting (G. Kelley, Tr. 2448), Respondent did not ask him about his impressions regarding the ballot in

question or any questions regarding the potentially applicable Motorola and Hitachi patents. Consequently, Respondent does not cite to any testimony to support the finding. It is, therefore, impossible to determine from the record what the patent issues were, whether there were alternative technologies to the Motorola and Hitachi technologies for the committee to consider, whether the patented technologies were necessary to the standard, or whether Motorola and Hitachi had cross-licensing agreements with other JEDEC members that might have provided rights to any potential Motorola or Hitachi patents.

The statement in the proposed finding that "IBM noted that their view has been to ignore patent disclosure rule because their attorneys have advised them that if they do then a listing maybe construed as complete" is incomplete and misleading. Mr. Kelley testified that the entry in the minutes was wrong and in fact what he had indicated to the committee was that it was impossible for him to guarantee that no IBM patents related but that he would inform the committee of any intellectual property that he was aware of and would seek further information if requested. (G. Kelley, Tr. 2449-2451 ("I think that probably the issue came up because people were aware that IBM was using some of these features at many levels within many computers, and so therefore they were asking me to provide the committee with a list of all issued patents and patent applications, and I was warning the committee that that was not something that I could do. It was just not a possible task for me to know what was going on all over the world for the IBM Corporation. I then went on to promise the committee that I would alert the committee to any information that I had that applied to the JEDEC task at hand and if a question came up, I would get them information on any patent that they could describe to me.")).

1230. At the March 1993 JC 42.3 meeting, the committee considered a ballot for Self-Refresh Entry/Exit (Item 487.09) for the SDRAM draft specification. (JX 15 at 8). The minutes state that both Hitachi and Mosaid raised a "patent alert." (JX 15 at 8). The committee voted unanimously to pass this ballot. (JX 15 at 8). At that meeting, the committee voted unanimously to send all SDRAM ballots to JEDEC Council for standardization. (JX 15 at 14). At the May

1993 JEDEC Council meeting, the Council passed the ballot to standardize this technology. (CX 54 at 10).

Response to Finding No. 1230: This finding does not support Respondent's contention that JEDEC would have adopted Rambus's technologies with a RAND assurance. Despite the fact that at least one witness at the hearing was in attendance at the meeting (G. Kelley, Tr. 2448), Respondent did not ask him about his impressions regarding the ballot in question or any questions regarding the potentially applicable patents. Consequently, Respondent does not cite to any testimony to support the finding. It is, therefore, impossible to determine from the record what the patent issues were, whether there were alternative technologies to the technologies for the committee to consider, whether the patented technologies were necessary to the standard, or whether the company that might have owned the patent had cross-licensing agreements with other JEDEC members that might have provided rights to any potential patents.

1231. At the March 1993 JC 42.3 meeting, the committee considered a ballot for Auto-Refresh (JC-42.3-92-134A) for the SDRAM draft specification. (JX 15 at 8). The minutes state that both Hitachi and Mosaid raised a patent issue. (JX 15 at 8). The committee voted unanimously to pass this ballot. (JX 15 at 9). At that meeting, the committee voted unanimously to send all SDRAM ballots to JEDEC Council for standardization. (JX 15 at 14). The item was given Council ballot number 93-24. (JX 16 at 38). At the May 1993 JEDEC Council meeting, the Council passed the ballot to standardize this technology. (CX 54 at 10).

Response to Finding No. 1231: This finding does not support Respondent's contention that JEDEC would have adopted Rambus's technologies with a RAND assurance. Despite the fact that at least one witness at the hearing was in attendance at the meeting (G. Kelley, Tr. 2448), Respondent did not ask him about his impressions regarding the ballot in question or any questions regarding the potentially applicable patents. Consequently, Respondent does not cite to any testimony to support the finding. It is, therefore, impossible to determine from the record what the patent issues were, whether there were alternative technologies to the technologies for the committee to consider, whether the patented technologies were necessary to the standard, or

whether the company that might have owned the patent had cross-licensing agreements with other JEDEC members that might have provided rights to any potential patents.

1232. At the March 1993 JC 42.3 meeting, the committee considered a ballot for DQM Latency Reads/Writes (JC-42.3-92-136A) for the SDRAM draft specification. (JX 15 at 9). The minutes state that both Hitachi and Mosaid raised a "patent concern." (JX 15 at 9). The committee voted unanimously to pass this ballot. (JX 15 at 9). At that meeting, the committee voted unanimously to send all SDRAM ballots to JEDEC Council for standardization. (JX 15 at 14). This item was given Council ballot number 93-26. (JX 16 at 38). At the May 1993 JEDEC Council meeting, the Council passed the ballot to standardize this technology. (CX 54 at 10).

Response to Finding No. 1232: This finding does not support Respondent's contention that JEDEC would have adopted Rambus's technologies with a RAND assurance. Despite the fact that at least one witness at the hearing was in attendance at the meeting (G. Kelley, Tr. 2448), Respondent did not ask him about his impressions regarding the ballot in question or any questions regarding the potentially applicable patents. Consequently, Respondent does not cite to any testimony to support the finding. It is, therefore, impossible to determine from the record what the patent issues were, whether there were alternative technologies to the technologies for the committee to consider, whether the patented technologies were necessary to the standard, or whether the company that might have owned the patent had cross-licensing agreements with other JEDEC members that might have provided rights to any potential patents.

1233. At the March 1994 JC 42.3 meeting, the committee considered a ballot for SGRAM and SVRAM Special Mode. (JX 19 at 12). Micron voted against the ballot, citing three issued patents held by Texas Instruments that could cover the technology. (JX 19 at 12). Hitachi moved to pass the ballot to Council "provided that TI gives some assurance on the patent." (JX 19 at 12). The committee passed the ballot unanimously. (JX 19 at 12).

Response to Finding No. 1233: This finding does not support Respondent's contention that JEDEC would have adopted Rambus's technologies with a RAND assurance.

Furthermore, this proposed finding appears to be misleading and inaccurate. The statement in this proposed finding that "the committee passed the ballot unanimously" does not appear to be accurate. Instead, it appears that there was a unanimous vote on the *motion* by Hitachi to "send it

[to] Council providing TI gives some assurance on the patent." (JX 19 at 12). Alternatively, the minutes could show that, in fact TI agreed to provide the assurances that Micron requested. The minutes show that after Micron voted against the ballot, Hitachi asked TI to comment on the minutes and TI responded that it had checked the patents and saw no reason to respond. (JX0019 at 12). TI may have suggested that there was no patent problem because Micron, according to the minutes, then stated that it would only change its vote if TI would give a written statement saying that their patents did not apply to the standard. (JX0019 at 12). The statement then cited in the finding "provided that TI gives some assurance on the patent" appears to be an assurance that it won't enforce the patent because the vote passed unanimously indicating either that the vote was on the separate motion by Hitachi, or that it was on the ballot and that Micron had withdrawn its 'no' votes. (JX0019 at 12).

In any event, despite the fact that a number of witnesses at the hearing were in attendance at the meeting (G. Kelley, Tr. 2477; Crisp, Tr. 2972; Kellogg, Tr. 5027-5028; Grossmeier, Tr. 10977), Respondent did not ask anyone about this incident. Consequently, Respondent does not cite to any testimony to support the finding. It is, therefore, impossible to determine precisely what the vote described in JX0019 at 12 resolved.

It is, furthermore, impossible to determine from the minutes whether there were alternative technologies to the TI technologies for the committee to consider. Also, it is not apparent whether the patented technology was necessary to the standard. There is no evidence as to whether TI had cross-licensing agreements with other JEDEC members.

1234. At the March 1995 JC 42.3 meeting, the committee considered ballot JC-42.3-95-14 Item 637. (JX 25 at 10). TI raised patent concerns. (JX 25 at 10). The committee nonetheless passed a motion to send the ballot to JEDEC Council. (JX 15 at 10).

Response to Finding No. 1234: This finding does not support Respondent's contention that JEDEC would have adopted Rambus's technologies with a RAND assurance.

Despite the fact that at least two witnesses at the hearing were in attendance at the meeting (G. Kelley, Tr. 2484-2485; Crisp, Tr. 3243), Respondent did not ask anyone about this incident. Consequently, Respondent does not cite to any testimony to support the finding and there is no record evidence of this event beyond the fact that "TI raised patent concerns"regarding this proposal but did not vote against it. Those patent concerns may have been addressed at the meeting. It is, furthermore, impossible to determine from the minutes whether there were alternative technologies to the technologies at issue for the committee to consider. Also, it is not apparent whether the technologies at issue were necessary to the standard.

1235. At the September 1995 JC 42.3 meeting, the committee considered a ballot for 4M/8M x8 DRAM in 32-pin SOP Item 660. (JX 27 at 7). The minutes state, "The Stacktek patent was discussed. Motion by HP to pass to Council the ballot conditionally on resolution of Stacktek's patent position. . . . Unanimous." (JX 27 at 8). The Council later passed this ballot. (JX 34 at 18).

Response to Finding No. 1235: This finding does not support Respondent's contention that JEDEC would have adopted Rambus's technologies with a RAND assurance. Despite the fact that a number of witnesses at the hearing were in attendance at the meeting (Sussman, Tr. 1410; G. Kelley, Tr. 2577; Crisp, Tr. 3306; Kellogg, Tr. 5092), Respondent did not ask anyone about this incident. Consequently, Respondent does not cite to any testimony to support the finding. It is, therefore, impossible to determine from the minutes what actual discussion on the Stacktek patent took place or how the patent related to the proposal. There is also no evidence as to whether there were alternative technologies to the technologies for the committee to consider. Also, it is not apparent whether the patented technologies were necessary to the standard. There is no evidence as to whether Stacktek had cross-licensing agreements with JEDEC members.

1236. When TI gave a RAND letter for its Quad-CAS technology (RX 562 at 13), the debate within JEDEC about TI's patents instantly subsided, the issue was resolved, and the JEDEC

committee voted unanimously to remove the hold on the Quad CAS standards and to revoke the ballot to rescind the standard. (JX 25 at 5).

Response to Finding No. 1236: The statement in this proposed finding that "When TI gave a RAND letter for its Quad-CAS technology (RX 562 at 13), the debate within JEDEC about TI's patents instantly subsided" is not supported by the cited evidence.

Furthermore, this proposed finding is misleading because it ignores substantial evidence in the record that notwithstanding the eventual agreement to revoke the ballot rescinding the standard, that the committee had developed an alternative to the Quad CAS technology and that Quad CAS technology is not used anymore. (Sussman, Tr. 1344 ("We took a vote. The result of the vote was to rescind it. We used an alternate technical implementation. Quad CAS doesn't exist anymore, at least as a standard part."); Kellogg, Tr. 5046 (Once IBM became aware of the patents or of the patent that read on quad CAS, from a JEDEC perspective, we were obligated to request all activity be stopped. We were obligated to consider work-arounds."); Kellogg, Tr. 5211-5212 ("I don't believe quad CAS is in use today or produced today.")).

1237. During the period from May 1990 through the end of 1995, patented technology, or potentially patented technology was proposed to JC 42.3 for standardization on at least a dozen occasions, as described above, and in each instance the technology was balloted and the ballot passed. On at least seven of these occasions, this occurred without any request for or receipt of a RAND assurance letter.

Response to Finding No. 1237: RPF 1224 lacks any reference to the record and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is misleading and contrary to substantial evidence in the record for the reasons discussed in CCRF 1219-1236.

1238. JEDEC's behavior, as described for example in the JEDEC 42.3 meeting minutes, shows that JEDEC repeatedly adopted technologies despite patent issues, especially after receiving

a RAND letter. In accordance with this behavior, had Rambus provided a RAND assurance, JEDEC would have adopted the Rambus technologies. (Teece, Tr. 10379-80, 10382-84).

Response to Finding No. 1238: The statement in this proposed finding that "JEDEC's behavior, as described for example in the JEDEC 42.3 meeting minutes, shows that JEDEC repeatedly adopted technologies despite patent issues, especially after receiving a RAND letter" is misleading and contrary to substantial evidence in the record for the reasons discussed in CCRF 1219-1236. (*See also* CCFF 2433-2440).

As a consequence, Professor Teece's opinion that "had Rambus provided a RAND assurance, JEDEC would have adopted the Rambus technologies" is unreliable because it is premised on his assumption that JEDEC does adopt technologies when a RAND letter is issued.

1239. EIA General Counsel, John Kelly, agreed that there is no objection to having features and standards that are protected by valid patents as long as they are available to all comers on reasonable and nondiscriminatory terms. (Kelly, Tr. 2072).

Response to Finding No. 1239: The proposed finding is incomplete. While, JEDEC rules will allow technologies in standards that are covered by intellectual property as long as they are available on a RAND basis, the preference is always to have standards free of patents at all (including RAND assured patents) and the ensuing royalties. (J. Kelly, Tr. 2073-2074 ("JEDEC, however, is concerned and I said before that JEDEC and EIA do not have a preference for including intellectual property in standards because of the fact that there may be a royalty that may increase the cost. The goal is always to try to produce a standard which is going to gain marketplace acceptance, and if the cost of the product is going to -- is likely to be increased by intellectual property, that's a general concern. That doesn't go to the licensing terms, however. That goes to the basic question of whether to include the IP at all or not."); *See also* G. Kelley, Tr. 2566 ("the consideration of anything on patents required as a first consideration avoidance and as a next consideration a RAND statement. The ideal RAND statement would be free. The next ideal

RAND requirement would be that it would meet the requirements of reasonable and nondiscriminatory.")).

1240. The chair of JC 42.3 admitted that if Rambus had agreed to give a RAND assurance, "I would have had to consider accepting their intellectual property." (Kelley, Tr. 2564-66).

Response to Finding No. 1240: The proposed finding is incomplete. Mr. Kelley went on to testify that consideration of accepting technologies along with RAND assurances was a second resort at JEDEC. (G. Kelley, Tr. 2566 ("the consideration of anything on patents required as a first consideration avoidance and as a next consideration a RAND statement. The ideal RAND statement would be free. The next ideal RAND requirement would be that it would meet the requirements of reasonable and nondiscriminatory.")

1241. Similarly, HP's JEDEC representative, Tom Landgraf, testified that if Rambus had disclosed the existence of patent applications on the DDR technologies, he would have still voted to incorporate those technologies if Rambus had indicated a willingness to comply with the JEDEC patent policy. (Landgraf, Tr. 1714).

Response to Finding No. 1241: The proposed finding is inaccurate. Mr. Landgraf testified that such a disclosure *would* affect his vote and that the impact of that disclosure depended on a number of factors, including: the identity of the owner of the patent application, the willingness to comply with the JEDEC patent policy, and how much the owner of the patent application was willing to tell the committee. (Landgraf, Tr.1714 ("QUESTION: Now, at this time that you were voting on DDR standards on behalf of Hewlett Packard, if Rambus had disclosed the existence of patent applications, would that have affected your vote as Hewlett Packard's representative? THE WITNESS: It would have affected our vote depending on the owner of the patented technology, their willingness to comply with the JEDEC policy. If we knew in advance that they were not going to comply with the JEDEC patent policy, we would have voted against it. If we didn't know that, knew it, you know, later on, we would have voted for it. So, it

depends on how much the owner was willing to tell the committee at the time and when they told us.")).

1242. The evidence therefore supports the conclusion that JEDEC would have adopted Rambus's technologies.

Response to Finding No. 1242: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is misleading because it implies that JEDEC consideration of technologies that have intellectual property issues is the same thing as JEDEC adopting technologies that are burdened by royalty or potential royalty payments. (*See* CCRF 1221).

1243. This conclusion is not undermined by testimony about "price constraining" alternatives. Even if alternatives were "price constraining" with respect to Rambus's technologies, they could not have been chosen by JEDEC. (Teece, Tr. 10366-67). A technology that is price constraining is not the same as an economic substitute. (Teece, Tr. 10370-71). An economic substitute must be equivalent in terms of cost-performance features. (Teece, Tr. 10371). Technologies that are not equivalent may still be price constraining, but that does not make them a viable alternative for JEDEC. (Teece, Tr. 10371). What is important to compare is the overall attractiveness of the alternatives on a quality/cost-adjusted basis. (Teece, Tr. 10976-97).

Response to Finding No. 1243: This proposal is misleading because it implies that Professor McAfee meant by "price constraining alternatives" something other than alternatives that could have been chosen by JEDEC. (McAfee, Tr. 7316 ("These are other -- if we're talking about technologies, these would be other technologies which are potential substitutes for the technology ....")). The alternatives described by Professor McAfee are "price constraining" *because* they could be chosen in response to a small but significant, non-transitory increase in price. (McAfee, Tr. 7332 ("And you increase the price, and if you get substitution away significant enough that the hypothetical monopolist would not like to increase the price, then in that case you have not found a

market and must add products. And so that's parallel in the sense that the commercially viable technologies are exactly those that don't survive the SSNIP -- that would be included or would be price-constraining under a SSNIP test.")). Professor McAfee testified that in looking for alternatives, he was specifically looking at the substitution behavior of the buyers. (McAfee, Tr. 7319-7324).

1244. The conclusion that JEDEC would have adopted Rambus's technologies in SDRAM and DDR once it received a RAND assurance from Rambus is not undermined by the possibility that JEDEC might have been "satisficing." (Teece, Tr. 10414-15). If JEDEC had avoided patented technologies in favor of alternative technologies without a lot of analysis, it would not have been satisficing; such conduct is merely biased behavior. (Teece, Tr. 10414). If JEDEC were satisficing, it would be willing to go forward with patented technology upon the receipt of a RAND letter. (Teece, Tr. 10414-15).

Response to Finding No. 1244: This proposed finding is misleading because it implies that JEDEC satisfices with respect to the inclusion of royalty-bearing technologies. The weight of the evidence, including the testimony of Professor McAfee, is that JEDEC avoids royalty-bearing technologies. (CCFF 107-111, 300-304, 2446-2454, 3029-3033).

3. Conclusion About The But-For World.

1245. The most likely scenario is the one in which JEDEC asks for and receives a RAND assurance from Rambus, no *ex ante* negotiations take place, and JEDEC adopts Rambus's technologies in both SDRAM and DDR. (Teece, Tr. 10415-16). Accounting for that scenario and the possibility that JEDEC might proceed without asking for a RAND letter, it is a virtual certainty that, had Rambus made the additional disclosures that Complaint Counsel allege should have been made, JEDEC would have adopted the same standards in the but-for world that it adopted in the actual world. (Teece, Tr. 10416).

Response to Finding No. 1245: The statement in this proposed finding that the most likely scenario is that Rambus provides a RAND letter is contrary to the weight of the evidence. (CCRF 1183-1203). The statement in this proposed finding that the most likely scenario is that no *ex ante* negotiations take place, and yet JEDEC includes the technologies in the standards is also contrary to the weight of the evidence. (CCRF 1204-1244).

E. Summary Of Findings On Alternatives.

1246. JEDEC repeatedly adopted for its standards the Rambus technologies at issue. It adopted two of the technologies in the SDRAM standard over several alleged alternatives. It adopted all four of the technologies in the DDR standard over alleged alternatives. And it adopted all four of the technologies in the DDR2 standard over alleged alternatives.

Response to Finding No. 1246: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is misleading because it omits the weight of the evidence in the record that indicates that the reason why JEDEC repeatedly adopted the Rambus technologies at issue was because Rambus failed to disclose to JEDEC that it was adopting Rambus technologies for use in emerging standards, and by the time that JEDEC members learned that Rambus had patents over technologies were included in the standard, "lock-in" prevented JEDEC members from switching to alternative technologies. (*See* CCFF 2101 (citing testimony from Howard Sussman, Betty Prince, Terry Lee, Mark Kellogg, Dr. Oh, and Willibald Meyer, in support of the proposition that had Rambus disclosed the scope of its patent applications while JEDEC was still working on the standards, some JEDEC members testified that they would have adopted alternative technologies; CCFF 2683-2756 (proposed findings that support the proposition that the DRAM industry is characterized by lock-in)).

1247. This repeated adopted shows that the Rambus technologies were superior to any alternatives considered by JEDEC.

Response to Finding No. 1247: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

This proposed finding is contrary to the weight of the evidence which indicates that lock-in explains why JEDEC continued to use Rambus technologies in subsequent generations of the SDRAM standard. (*See* CCRF 1246).

Furthermore, this proposed finding ignores the weight of the evidence that indicates that there were viable alternatives to Rambus's technologies. (*See generally* CCFF 2130-2432). There are almost always multiple ideas about what features JEDEC should and should not include in a particular device. (Rhoden, Tr. 414-15; *see also* CCFF 2102). Some fact witnesses testified that they would have preferred the use of an alternative technology at the time. (*See* CCFF 2107 (citing the testimony of Mark Kellogg, Mr. Bechtelsheim, Howard Sussman, and Mr. Polzin in support of the proposition that JEDEC members viewed the alternatives as viable, and many members preferred one or more of the alternatives to the technologies that were actually selected)).

1248. There were no technological restraints that required JEDEC to continue to use the four Rambus technologies in DDR2.

Response to Finding No. 1248: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

This proposed finding of fact is misleading as evidence to support that JEDEC preferred Rambus's technologies to alternatives. To the contrary, the weight of the evidence indicates that JEDEC members viewed the alternatives as viable, and many members preferred one or more of the alternatives to the technologies that were actually selected. (*See* CCFF 2107). Economic restraints (i.e., lock-in) explain why JEDEC continued to use the four Rambus technologies in DDR II SDRAM. (*See* CCFF 2683-2756).

1249. At the time of formulating the DDR2 standard, JEDEC explored using alternatives for each of the four Rambus technologies.

Response to Finding No. 1249: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1250. JEDEC adopted the four Rambus technologies in the DDR2 standard with knowledge of Rambus's issued patents and knowledge of Rambus's demands for royalties.

Response to Finding No. 1250: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is incomplete because it ignores the weight of the evidence that indicates that JEDEC could not switch to alternative technologies in the DDR II SDRAM standard out of a need to keep on schedule or risk substantial financial loss, and the need to maintain backwards compatibility between standards. (*See* CCFF 3227-3261).

1251. JEDEC members have continued standardization efforts in other contexts despite warnings that the standards being developed would violate Rambus's patents.

Response to Finding No. 1251: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, it is not clear that this proposed finding is relevant to this case because it does not indicate what other contexts it is referring to and whether those contexts involve Rambus technologies.

1252. There is substantial evidence that JEDEC members believed throughout the 1990's that Rambus's patents would not be val*id.* This evidence helps to explain their conduct.

Response to Finding No. 1252: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

In particular, Respondent does not cite any support in the record for the statement that JEDEC members believed throughout the 1990s that Rambus's patents would not be val*id.* Furthermore, that statement is incomplete because it ignores the weight of the evidence that indicates that JEDEC members had no knowledge that Rambus patents could cover JEDEC work. During the time that Rambus was a member of JEDEC, it was promoting its proprietary RDRAM technology and concealed its claims to JEDEC standard technology. (*See* CCFF 1238-1259 (outlining the evidence in the record supporting the latter proposition).

1253. Each of the alternatives proposed by Complaint Counsel's experts is either covered by Rambus's patents or inferior in cost-performance terms.

Response to Finding No. 1253: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

This proposed finding is contrary to the weight of the evidence which indicates that there were commercially and technically viable alternatives to Rambus's technologies. (*See* CCRF 809-902 (responding to RPFs drafted to challenge the viability of the CAS latency alternatives), CCRF 903-988 (responding to RPFs drafted to challenge the viability of the burst length alternatives), CCRF 990-1077 (responding to RPFs drafted to challenge the viability of the dual edged clocking alternatives), CCRF 1078-1124 (responding to RPFs drafted to challenge the viability of the on-chip DLL alternatives)).

In addition, the statement in this proposed finding that refers to Rambus patents covering alternative technologies is unreliable, unsupported by the evidence and contrary to the weight of the evidence for the reasons previously set forth in CCRF 964-969 (for alternatives to programmable CAS latency and burst length) and CCRF 1121-1124 (for alternatives to dual edged clocking and on-chip DLL). Rambus does not even allege that most of the alternatives identified by Complain Counsel are covered by Rambus patents. Furthermore, with respect to the small number of technologies that Respondent contends are covered by Rambus patents, there is no reliable evidence in the record to support those contentions for the reasons set forth in CCRF 964-965, 1121-1122.

1254. No combination of non-infringing alternatives identified by Complaint Counsel's experts is less costly than Rambus's royalties for SDRAM or DDR.

Response to Finding No. 1254: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

This proposed finding is contrary to the weight of the evidence that indicates that there were commercially and technically viable alternatives to Rambus's technologies for SDRAM and DDR SDRAM. (*See generally* CCFF 2130-2414). There are almost always multiple ideas about what features JEDEC should and should not include in a particular device. (Rhoden, Tr. 414-15; *see also* CCFF 2102). Some fact witnesses testified that they would have preferred the use of an alternative technology at the time. (*See* CCFF 2107 (citing the testimony of Mark Kellogg, Mr. Bechtelsheim, Howard Sussman, and Mr. Polzin in support of the proposition that JEDEC members viewed the alternatives as viable, and many members preferred one or more of the alternatives to the technologies that were actually selected)).

1255. A rational manufacturer or group of manufacturers would have adopted the Rambus technologies and paid the Rambus royalties for SDRAM and for DDR rather than adopt the alternatives proposed by Complaint Counsel's experts.

Response to Finding No. 1255: This proposed finding is unreliable because Respondent cites no evidence in the record as support to make such a statement. It is incomplete because it ignores the weight of the evidence in the record that indicates that there were viable alternatives to the Rambus technologies, which means that, at a minimum, it is equally likely that a rational manufacturer or group of manufacturers would have adopted alternative technologies rather than pay Rambus royalties. There is substantial evidence in the record that indicates that JEDEC members would have adopted alternative technologies had Rambus disclosed the scope of its patents while it was a member of JEDEC. (*See* CCFF 2101).

Furthermore, Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Brief.

1256. Manufacturers and consumers are better off using Rambus's technologies and paying the Rambus royalties for SDRAM and for DDR than they would be if JEDEC had adopted the alternatives proposed by Complaint Counsel's experts.

Response to Finding No. 1256: This proposed finding is unreliable because Respondent cites no evidence as support to make such a proposition. Given that the weight of the evidence indicates that there were viable alternatives to Rambus's technologies (CCFF 2130-2414), and that Rambus acquired monopoly power as a result of patenting standardized technologies (CCFF 2706, 2710-2756), Respondent's proposed finding that manufacturers and consumers would be better off using Rambus's technologies and paying Rambus royalties for SDRAM and DDR SDRAM would seems unlikely.

Furthermore, Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1257. Complaint Counsel have failed to meet their burden to show that there existed viable, non-infringing alternatives that JEDEC would have adopted in place of the Rambus technologies.

Response to Finding No. 1257: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Furthermore, it is contrary to the weight of the evidence. (*See* CCFF 2130-2414).

1258. Complaint Counsel have failed to meet their burden to prove that JEDEC would have adopted alternative technologies had Rambus made the additional disclosures that Complaint Counsel allege should have been made.

Response to Finding No. 1258: This proposed finding lacks any reference in the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this proposed finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

X. THE DRAM INDUSTRY IS NOT, AND HAS NOT BEEN, "LOCKED IN" TO USING THE RAMBUS TECHNOLOGIES.

1259. While Complaint Counsel contend that the DRAM industry was locked in to using the Rambus technologies once they were adopted into the JEDEC standards and the industry began producing compliant products, the evidence discussed above refutes this notion.

Response to Finding No. 1259: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1260. Specifically, the evidence shows that, even as late as 2000, JEDEC considered changing its standards and switching to alternatives to Rambus's technologies. For instance, in March 2000, Micron proposed eliminating programmable latency in SDRAM and DDR devices. (CX 154A at 25-29). In response, Bob Fusco at Hitachi wrote that it was *not* too late to make these changes in DDR. (RX 1626 at 4).

Response to Finding No. 1260: Complaint Counsel agrees that in March of 2000, JEDEC considered changing its standards and switching to alternatives to the disputed technologies. The weight of the evidence is that JEDEC did not switch because it was locked in to the current standard. (CCFF 2500-2584, 2914-2961).

The cited language in RPF 1260 from Mr. Fusco is not reliable evidence regarding whether the industry is locked into the JEDEC standards. (*See* CCRF 750).

Furthermore, this proposed finding is incomplete because it mischaracterizes the cited document. Mr. Fusco, who was not called to testify on this document by Rambus, wrote: "For DDR it's not too late for minor, carefully considered changes, so I am open to either proposal." (RX1626 at 4). Because Mr. Fusco was never called to testify, there is no record evidence as to whether Mr. Fusco meant what Respondent claims, or simply that he was willing to consider changes and would be willing to look to *see* if the changes proposed by Micron were, in fact, "minor, carefully considered changes." There is substantial evidence in the record that the changes needed to avoid Rambus patents were so extensive that companies outside of the DRAM industry became concerned that the industry would attempt to change the standard to avoid the patents, because, if that happened, their own products might not be compatible with the new DRAMs. (CCFF 2505, 2542, 2547).

1261. Steve Polzin testified that in 2000 he discussed alternatives to Rambus's technologies with DRAM manufacturers. (Polzin, Tr. 3988, 3996, 4044).

Response to Finding No. 1261: This proposed finding is incomplete because Mr. Polzin also testified that Rambus patents were "pretty simple things to work around if we had

known about them a long time ago. This was just when we were trying to get our [DDR-based chipset] and the first DDR motherboards out the door. They were pretty trivial to work around, but we were in the middle of ramping and they're pretty tough to change things.... The work-arounds that were obvious required some big changes to the device, to the chipsets, to the motherboards, et cetera." (Polzin, Tr. 3989-90).

1262. Also in this time period, JEDEC's Future DRAM Task Group considered alternatives for each of Rambus's technologies, but ended up adopting the Rambus technologies with full knowledge of Rambus's issued patents and demands for royalties.

Response to Finding No. 1262: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Complaint Counsel agrees that JEDEC considered changing its standards and switching to alternatives to the disputed technologies. The weight of the evidence is that JEDEC did not switch because it was locked in to the current standard. (CCFF 2500-2584, 2914-2961). The changes required to avoid the Rambus patents were so disruptive that they were not adopted by JEDEC for the DDR-2 standard. (CCFF 3252-3261).

Furthermore, this proposed finding is unreliable because the statement in this proposed finding that JEDEC acted "with full knowledge of Rambus's issued patents and demands for royalties" is vague as to the time frame involved and as to the meaning of the phrase "full knowledge."

1263. As Complaint Counsel's own expert testified, JEDEC members would not be discussing alternatives to Rambus's technologies in 2000 unless they thought that the alternatives could be adopted. (McAfee, Tr. 7571).

Response to Finding No. 1263: This proposed finding is inaccurate because Professor McAfee simply agreed that JEDEC would not spend "a lot of time discussing

technologies in the year 2000 if there was not a sense among at least some significant number of members that those technologies were commercially viable at that point in time." (McAfee, Tr. 7571). Professor McAfee did not testify about what JEDEC members believed based on less than "serious consideration" of alternatives by JEDEC. (McAfee, Tr. 7571).

1264. Complaint Counsel has failed to produce a single contemporaneous document that states these considerations were fruitless because the industry was locked in. In fact, while they have elicited the testimony of interested parties on this issue, Complaint Counsel has failed to produce a single document that states DRAM manufacturers or the industry could not have switched to alternatives to Rambus's technologies.

Response to Finding No. 1264: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposal is misleading because it implies that the industry is only locked in to the current standards if "DRAM manufacturers or the industry could not have switched to alternatives to Rambus's technologies." For the purpose of this case, the industry, and firms in the industry are "locked in" to the standard if the costs of switching are such that the industry is better off paying the Rambus royalties than switching. (CCFF 2659). If that is the case, then Rambus can charge its royalties without fear of firms switching to alternative technologies, and so Rambus's ability to control the prices of the technologies is caused by its patents on the SDRAM standards. (CCFF 2665-2666).

Furthermore, this proposed finding ignores substantial evidence in the record. In addition to the documents cited in support of lock-in (*see* CCFF 2500-2584), some documents that show the time and expense of changing the standard to avoid the Rambus patents include a pair of July 1997 emails from Rambus's former board chairman, William Davidow, to its current board chairman and CEO, Geoffrey Tate. First, Mr. Davidow, forwards an email that he sent to an Intel executive

saying "We are hoping that [the DRAM companies] will either drop their competitive efforts or discover for themselves that they have violated Rambus patents and will conclude that getting around them will be either extremely difficult or impossible and will take a lot of time." (CX0939 at 1). On the same day, Mr. Davidow sent another email to Mr. Tate saying: "At any rate, we are fairly confident that if Synclinc [sic] goes forward, they will have to do a lot of re-engineering to get around issued and soon to be issued patents. My guess is that this will delay their efforts from two to five years." (CX0936 at 1).

1265. Nonetheless, Complaint Counsel contend that the DRAM industry is locked in to using the Rambus technologies in SDRAM and DDR because the cost to transition to alternative technologies is allegedly too high and it is allegedly too difficult for the DRAM industry to coordinate a transition away from using Rambus's technologies. The evidence at trial, however, demonstrates that (1) DRAM manufacturers concurrently produce multiple types of DRAM in their factories and routinely change their manufacturing lines to incorporate new technologies, (2) that the industry routinely coordinates changes in technology, and (3) that switching costs are not prohibitive. The evidence therefore shows that the DRAM industry has not been and is not locked in to using Rambus's technologies.

Response to Finding No. 1265: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

A. The DRAM Industry Transitions To New Technologies All The Time.

1266. The evidence shows that the DRAM industry not only frequently and rapidly transitions to new technologies, but that it uses multiple DRAM standards at any given time.

Response to Finding No. 1266: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1. The Statistical Evidence Of DRAM Purchases Shows Multiple Co-Existing DRAM Standards And Frequent Transitions.

1267. The statistical evidence regarding DRAM purchases over time shows multiple DRAM standards coexisting and regular transitions.

Response to Finding No. 1267: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1268. In 1994, fast page mode ("FPM") DRAM accounted for 96.7% of the revenue for DRAM. (Rapp, Tr. 10100, 10248). The remaining 3% of DRAM revenue was accounted for by other DRAM technologies. (Rapp, Tr. 10248).

Response to Finding No. 1268: Complaint Counsel does not disagree.

1269. In 1995, FPM accounted for 87.2%, EDO DRAM for 9.9%, and other DRAM for 2.9% of DRAM revenue. (Rapp, Tr. 10100-01, 10248).

Response to Finding No. 1269: Complaint Counsel does not disagree.

1270. In 1996, FPM accounted for 39.4%, EDO for 52.7%, SDRAM for 4.3%, RDRAM for 0.5%, and other DRAM for 3.1% of DRAM revenue. (Rapp, Tr.10101, 10248).

Response to Finding No. 1270: Complaint Counsel does not disagree.

1271. In 1997, FPM accounted for 8.1%, EDO for 55.2%, SDRAM for 33.5%, DRAM for 1.3%, and other DRAM for 1.8% of DRAM revenue. (Rapp, Tr. 10101, 10248).

Response to Finding No. 1271: Complaint Counsel does not disagree.

1272. In 1998, FPM accounted for 8.8%, EDO for 27.6%, SDRAM for 60.8%, RDRAM for 1.6%, and other DRAM for 1.3% of DRAM revenue. (Rapp, Tr. 10101, 10249).

Response to Finding No. 1272: Complaint Counsel does not disagree.

1273. In 1999, FPM accounted for 10.5%, EDO for 17.5%, SDRAM for 69.3%, RDRAM for 1.1%, and other DRAM for 1.5% of DRAM revenue. (Rapp, Tr. 10102, 10249).

Response to Finding No. 1273: Complaint Counsel does not disagree.

1274. In 2000, FPM accounted for 5.2%, EDO for 11.1%, SDRAM for 78.4%, RDRAM for 3%, DDR for 0.4%, and other DRAM for 1.9% of DRAM revenue. (Rapp, Tr. 10101, 10249).

Response to Finding No. 1274: Complaint Counsel does not disagree.

1275. In 2001, FPM accounted for 4%, EDO for 7.7%, SDRAM for 69.7%, RDRAM for 12.5%, DDR for 5.3%, and other DRAM for 0.8% of DRAM revenue. (Rapp, Tr. 10101, 10249).

Response to Finding No. 1275: Complaint Counsel does not disagree.

1276. Within each of these categories, there were different speeds (e.g, for SDRAM, PC66, PC100, PC133; for DDR, DDR200, DDR266, DDR333, DDR400). (Rapp, Tr. 10249-50; Gross, Tr. 2348-56; Polzin, Tr. 3998-4005).

Response to Finding No. 1276: Complaint Counsel does not disagree that within some of these categories there were different speeds.

1277. These figures show that in any given year the DRAM market is divided among multiple incompatible standards (Rapp, Tr. 10103-04), and it demonstrates that there is no technological or economic force mandating a single standard in the DRAM industry. (Rapp, Tr. 10103-04).

Response to Finding No. 1277: This proposed finding is not supported by the referenced testimony. Dr. Rapp was not qualified as a technical expert and is not competent to testify as to whether the standards existing at any given time are "incompatible." Furthermore, this assumption is not supported by substantial record evidence rendering, Dr. Rapp's opinion that "there is no technological or economic force mandating a single standard in the DRAM industry" unreliable.

Furthermore, the statement in this proposed finding that there are "multiple incompatible standards" is misleading because it implies that the industry is capable of switching from the dominant DRAM standard to another, already existing standard. That implication ignores substantial evidence in the record that the DRAM industry is dominated by a single DRAM standard, and that the other DRAMs on the market are generally only appropriate for niche products. (McAfee, Tr. 11228). The market-share evidence gives the appearance of multiple co-existing standards because the industry transitions from one dominant DRAM standard to another over time. (McAfee, Tr. 11227-11228). When the industry transitions, the market share of the old dominant standard declines and the market share of the new dominant standard increases, so there

is a "transition period." (McAfee, Tr. 11227). As a result, at any given time, there might be DRAMs sold in the market for (1) long life cycle products that use older DRAMs; (2) PCs that use the dominant DRAM; and (3) high performance products, like video cards, that use low volume, next-generation DRAMs. (McAfee, Tr. 11227-11229).

Because some products that use DRAMs have long product lives, they cannot switch to the new dominant DRAM standard, and instead continue to use the old DRAM standard. (McAfee, Tr. 11228). For example, network switches made by Cisco have long product lives and generally use older standard DRAM. (Bechtelsheim, Tr. 5851 ("[S]ome of Cisco's products have life cycles that are coming close to ten years and others are well on their way there, so a ten-year life cycle is not unusual for a Cisco switch or router.")). Other products that place a high value on performance and a lower value on price than the dominant PC applications use DRAMs corresponding to next generation standards. (McAfee, Tr. 11228-11229). For example, video card manufacturers often use DRAMs corresponding to standards that have not yet even been completed by JEDEC in order to take advantage of the greater performance they provide. (Wagner, Tr. 3836 ("We try to make them as close as possible to whatever the next standard in JEDEC is going to be, or we predict it's going to be.")).

Furthermore, the statement in this proposed finding that the standards in existence at any given time in the industry are "incompatible" is vague and, depending on the meaning of the term, contrary to the weight of the evidence. There is substantial evidence in the record that the industry transitions from one standard to evolutionary improvements of that standard. (CCFF 127). The importance of evolutionary change is that it minimizes the costs of transition between standards. (CCFF 128, 2570, 2648-2649). For example, some of the technologies at issue in this case are in the current standards because they were evolutionary changes from the previous standard. (CCFF 534, 2571-2573). One aspect of evolutionary change is that new DRAM standards are "backwards

compatible" with the previous standard, which eases the transition from the old standard to the new standard. (CCFF 3249-3250).

Finally, this proposed finding ignores substantial evidence that there are "economic force[s] mandating a single standard in the DRAM industry." (CCFF 2541-2562, 2600-2624).

2. DRAM Manufacturers Are Constantly Redesigning DRAM.

1278. The evidence shows that DRAM manufacturers are constantly coming out with new and redesigned DRAM products.

Response to Finding No. 1278: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

This proposed finding is also misleading as it implies that DRAM manufacturers can quickly "com[e] out with new and redesigned DRAM products." The weight of the evidence is that it takes years for DRAM companies to design and mass produce new DRAMs. (CCFF 46-77; 2528-2540).

Furthermore, this proposed finding is misleading because it implies that DRAM manufacturers can change their production without coordinating with their customers or with other firms that manufacture inter-operating components like chipsets. The weight of the evidence is that individual firms cannot change the type of DRAM they manufacture without such coordination. (CCFF 2541-2562).

1279. Brian Shirley, Design Operations Manager for the Computing and Consumer group at Micron Technology (Shirley, Tr. 4133), testified that Micron "taped out," or gone through the entire design process, for numerous different DRAM each year.

Response to Finding No. 1279: This proposed finding is misleading for the reasons described in CCRF 1278.

Furthermore, this proposed finding is misleading because it implies that the tape-out stage of the design process is the "entire design process." In fact, the tape-out process is only one stage of the design process. (CCFF 46). There is substantial evidence in the record that depending on the type of design change involved, it can take up to a year and a half for a DRAM design to proceed to tape-out. (CCFF 55). Furthermore, this proposed finding is incomplete because it omits testimony by Mr. Shirley that once a DRAM is taped out, it can take between 10 months and a year and a half for that DRAM to proceed to high volume production. (CCFF 58-59).

1280. Mr. Shirley testified that

(Shirley, Tr. 4218 (in camera)).

Response to Finding No. 1280: This proposed finding is misleading for the reasons described in CCRF 1278 and 1279. This proposed finding is also misleading because it implies that the "different new" products were in fact different from each other rather than derivatives from the same basic part. (Appleton, Tr. 6264-6265 ("[T]he majority of the product is today synchronous DRAM and DDR, and there's just a whole variety of configurations that -- around those two devices, but essentially those are all derivatives of kind of the same basic part.")).

1281. In 1998,

(Shirley, Tr. 4218-19, 4226 (in camera)).

Response to Finding No. 1281: This proposed finding is misleading for the reasons described in CCRF 1278-1280.

1282. In 1999,

(Shirley, Tr. 4220-23, 4225-26 (in camera)).

Response to Finding No. 1282: This proposed finding is misleading for the reasons described in CCRF 1278-1280.

1283. In 2000,

(Shirley, Tr. 4223-25 (in camera)).

Response to Finding No. 1283: This proposed finding is misleading for the reasons described in CCRF 1278-1280.

1284. In 2001,
(Shirley, Tr. 4227 (in camera)).

Response to Finding No. 1284: This proposed finding is misleading for the reasons described in CCRF 1278-1280.

1285. In 2002,
(Shirley, Tr. 4228-29 (in camera)).

Response to Finding No. 1285: This proposed finding is misleading for the reasons described in CCRF 1278-1280.

1286. According to Mr. Shirley,

(Shirley, Tr. 4282 (in camera)).

Response to Finding No. 1286: This proposed finding is misleading for the reasons described in CCRF 1278-1280.

3. DRAM Manufacturers Manufacture Multiple Types Of DRAM Contemporaneously And Routinely Change Their Manufacturing Lines To Incorporate New Technologies.

1287. The evidence also shows that DRAM manufacturers not only produce multiple types of DRAM at any given time, but also frequently transition their manufacturing lines to incorporate new technologies.

Response to Finding No. 1287: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is misleading for the reasons described in CCRF 1278.

1288. Micron CEO Steven Appleton testified that Micron currently manufactures a wide variety of DRAMs, including EDO, SDRAM, DDR, DDR2 and various specialty DRAMs, such as pseudostatic RAMs. (Appleton, Tr. 6264).

Response to Finding No. 1288: This proposed finding is misleading for the reasons described in CCRF 1277-1278.

1289. In a "response script" prepared by Micron in December 1996 for use in discussions with customers, Micron described its ability to manufacture various different kinds of DRAMs. (RX 836 at 2-4).

Response to Finding No. 1289: Complaint Counsel does not disagree.

1290. The December 1996 "response script" was prepared by Micron in connection with Intel's announcement that it intended to design its next generation of chipsets to work with Rambus memory devices, then denominated "nDRAM." (RX 836 at 2; Lee, Tr. 6853-54). At the time, Micron did not have a license to manufacture the Rambus device. (*Id.*).

Response to Finding No. 1290: Complaint Counsel does not disagree.

1291. The December 1996 "response script" includes possible questions and proposed answers. One such question is "What would having to make 'nDRAM' or SyncLink mean to Micron?" (RX 836 at 3). Micron's answer to this question is instructive:

> "Keep in mind that ALL of these DRAM technologies use the same DRAM process, the same DRAM cell, and virtually the same DRAM array.
>
> . . .
>
> Switching from one product to another, while still using the same core technology, involves only changing priorities in design and product engineering and may mean some differences in our assembly and test equipment purchases. SDRAM, SLDRAM, nDRAM all use the same fab equipment and core DRAM technology. *In short, while the flavors might change, it's still a DRAM*."

(RX 836 at 3) (emphasis added).

Response to Finding No. 1291: This proposed finding is misleading for the reasons described in CCRF 1278-1279.

1292. Henry Becker, Vice President and Managing Director for the Infineon Technologies Richmond factory (Becker, Tr. 1093), testified that, since the first silicon came out of the Infineon Richmond plant in January 1998, that plant manufactured four different types of 64MB SDRAM (through 2001); three different types of the 256 SDRAM (2000-present); the 128MB SDRAM (2001-2002); and two different types of the 256MB DDR (2000-present). (Becker, Tr. 1167-69, 1179-83).

Response to Finding No. 1292: This proposed finding is misleading for the reasons described in CCRF 1278-1279.

This proposed finding also is misleading. The changes resulting in the "different types" of DRAMs manufactured at the Richmond plant were simple die shrinks, which are not comparable to the amount of time and expense needed required to change DRAM standards. (CCFF 46-77, 2564-2584).

1293. Mr. Becker further testified that every "shrink" (i.e., reduction in the feature size of the DRAM) and redesign requires a new "mask set" for the product. (Becker, Tr. 1170-73). In the 2.5-3 years in which the Infineon Richmond plant manufactured 64MB SDRAMs, it had to make at least 20 different mask sets. (Becker, Tr. 1170-73).

Response to Finding No. 1293: This proposed finding is misleading for the reasons described in CCRF 1279 and 1292.

1294. Mr. Becker also testified that, when the Infineon Richmond plant transitioned some of its lines from SDRAM to DDR, Infineon had to purchase additional equipment because DDR requires additional manufacturing processes. (Becker, Tr. 1182-83). Nonetheless, DDR and SDRAM were made in the same processing facility, and except for the additional equipment, its manufacture used the same processing equipment. (Becker, Tr. 1182-83).

Response to Finding No. 1294: This proposed finding is misleading for the reasons described in CCRF 1278.

1295. In fact, of the DRAM currently produced by the Infineon Richmond plant, approximately two-thirds are DDR and one-third are SDRAM. (Becker, Tr. 1139).

Response to Finding No. 1295: Complaint Counsel does not disagree.

1296. Infineon's 2002 product information guide lists three Infineon manufacturing plants, which produce the following product categories: DDR SDRAM, SDR SDRAM, Graphics RAM, Mobile-RAM, and RLDRAM. (CX 2466 at 2-3).

Response to Finding No. 1296: This proposed finding is misleading for the reasons described in CCRF 1277-1278.

1297. The Infineon 2002 product information guide lists the following densities for DDR products as either being currently in production by Infineon or planned for production in 2002: 128 Mb DDR, 256 Mb DDR, 256 Mb FBGA DDR, and 512 Mb DDR. (CX 2466 at 5). Each of

these different density products is produced in three different organizations (e.g., for the 128Mb DDR - 32Mx4, 16Mx8, and 8Mx16). (CX 2466 at 5). Each of these different organizations is produced in several speeds (e.g., for the 512Mb DDR in the 128Mx4 organization - DDR200, DDR266A, and DDR333). (CX 2466 at 5). In all, according to the product guide, Infineon had in production 34 different DDR products in 2002.

Response to Finding No. 1297: This proposed finding is misleading for the reasons described in CCRF 1277-1278. This proposed finding is further misleading because it implies that the amount of time and expense needed to change the density of a DRAM is similar to the amount of time and expense required to change DRAM standards. This implication is contrary to the evidence. (CCRF 1279; CCFF 46-77, 2564-2584).

1298. The Infineon 2002 product information guide lists the following densities for SDRAM products as either being currently in production by Infineon or would be in production in 2002: 256Mb SDRAM, 256Mb FBGA SDRAM, and 512Mb SDRAM. (CX 2466 at 6-7). Each of these different density products is produced in three different organizations (e.g., for the 256Mb SDRAM - 64Mx4, 32Mx8, and 16Mx16). (CX 2466 at 6). Each of these different organizations is produced in several speeds (e.g., for the 512Mb SDRAM in the 128Mx4 organization - PC100 and PC133). (CX 2466 at 7). In all, according to the product guide, in 2002 Infineon had in production in 27 different SDRAM products.

Response to Finding No. 1298: This proposed finding is misleading for the reasons described in CCRF 1277-1278 and 1297.

1299. In addition, the Infineon product guide shows that Infineon produced 7 different types of Graphics RAM, 20 different types of Mobile DRAM, and 6 different types of RLDRAM (according to the part numbers). (CX 2466 at 8-9).

Response to Finding No. 1299: This proposed finding is misleading for the reasons described in CCRF 1277-1278.

1300. According to Mr. Becker, Infineon's Richmond plant currently manufactures all 12 of the different types, organizations and speeds of 256-megabit SDRAMs listed in the Infineon 2002 product information guide (CX 2466), as well as DDR products. (Becker, Tr. 1143)

Response to Finding No. 1300: This proposed finding is misleading for the reasons described in CCRF 1277-1278.

1301. Infineon is able to shift its production of DRAM to a different density within in 14 months. (Becker, Tr. 1146-1148). According to Mr. Becker, die shrinks require new equipment,

new processes, putting in the capability to run the wafers, electrical performance testing of wafers and process tweaking, design tweaking and "some redesigns", reliability testing, customer qualification and feedback. All this takes only 14 months. (Becker, Tr. 1158).

Response to Finding No. 1301: This proposed finding is misleading for the reasons described in CCRF 1278-1279.

1302. Infineon is able to shift its production of DRAM to increased speeds in as little as 3 to 4 months. (Becker, Tr. 1148-49).

Response to Finding No. 1302: This proposed finding is misleading for the reasons described in CCRF 1278-1279.

1303. When Infineon shifted some of its manufacturing lines from producing SDRAM to producing DDR, the shift took 16-17 months. (Becker, Tr. 1149-50).

Response to Finding No. 1303: This proposed finding is misleading for the reasons described in CCRF 1278-1279.

1304. If technically feasible, the alternatives proposed by Professor Jacob could each have been implemented in a 6-12 month time frame. (Geilhufe, Tr. 9674-75).

Response to Finding No. 1304: This proposed finding is unreliable because it is based solely on the *ipse dixit* of Mr. Geilhufe, who provided no supporting evidence. Mr. Geilhufe's opinion that each of the alternatives that he reviewed could have been implemented in a six to twelve-month time frame was based solely on his statement of "the industry experience of how often a DRAM normally gets revised during its manufacturing cycle." (Geilhufe, Tr. 9675).

Furthermore, this proposed finding is misleading because in stating his opinion that each of the alternatives that he reviewed could have been implemented in a six to twelve-month time frame, Mr. Geilhufe did not include any consideration of how long it would take JEDEC to determine which alternatives to put in the standard. (Geilhufe, Tr. 9675). The weight of the evidence is that it takes two to three years for JEDEC to agree to a new DRAM standard. (CCFF 2564-2573).

Furthermore, this proposed finding is contrary to the weight of the evidence that from the time a manufacturer receives a completed specification from JEDEC, it can take more than two years to complete a new DRAM for production. (CCFF 46-65).

1305. These facts show that scale economies are not so powerful that they drive the industry necessarily to a single standard technology at any one time. (Rapp, Tr. 9894-95).

Response to Finding No. 1305: This proposed finding is unreliable because Dr. Rapp's opinion that scale economies are not "so powerful that they drive the industry necessarily to a single standard technology at any one time," is based on his understanding that there is not one dominant standard at any given time. That understanding ignores substantial evidence in the record that scale economies do drive a single dominant industry standard. (CCRF 1277; CCFF 112-121, 2600-2609).

1306. Economies of scale occur at the plant level. (Rapp, Tr. 9893). Plants in the industry often produce at the same time a variety of DRAM (using different technologies, DRAM of different speeds, etc.). (Rapp, Tr. 9893). For example, RDRAM, SDRAM, and DDR have coexisted in the marketplace. (Rapp, Tr. 9893-94). Similarly, different subgenerations of DRAM - e.g., PC66, PC100, PC133 - have coexisted in the marketplace. (Rapp, Tr. 9893-94). This shows that the economics of the industry does not require a single standard. (Rapp, Tr. 9893).

Response to Finding No. 1306: This proposed finding is unreliable for the reasons described in CCRF 1305.

1307. The coexistence of multiple standards also shows that network effects in the DRAM industry are not so high as to make it impractical to switch to an alternative technology. (Rapp, Tr. 9895).

Response to Finding No. 1307: This proposed finding is unreliable for the reasons described in CCRF 1305.

Furthermore, this proposed finding ignores the weight of the evidence that interoperability between DRAMs and other components is important in the DRAM industry. (CCFF 2610). The need for interoperability between DRAMs and other components creates a type of network effect

known as an "indirect network effect." (CCFF 2611). This indirect network effect reinforces the need in the industry for a single dominant DRAM. (CCFF 2611-2612).

4. The DRAM Industry Routinely Coordinates Transitions To New Standards.

1308. Complaint Counsel contend that the DRAM industry cannot switch to alternatives to Rambus's technologies because of the difficulties of coordinating the necessary changes among DRAM manufacturers and manufacturers of complementary products (which manufacture the so-called "infrastructure" of the memory subsystem). The evidence shows, however, the DRAM industry routinely coordinates transitions to new DRAM technology without impediment.

Response to Finding No. 1308: This proposed finding lacks any reference to the record , constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is misleading because it implies that since the DRAM industry transitions from one type of DRAM to another, it could or would do so easily in response to Rambus lawsuits on the DRAM standards. The weight of the evidence is that individual DRAM manufacturers cannot change their DRAM production unless there is also a change in a number of other products like chipsets and motherboards. (CCFF 2547-2562). Historically, this coordination problem has been solved in the DRAM industry by JEDEC. (CCFF 2563). The weight of the evidence is that it takes years to change the JEDEC standards. (CCFF 2564-2573).

Furthermore, this proposed finding ignores substantial evidence in the record that the transitions that occur "routinely" in the industry only occur when it is in the interests of all of the firms to make that transition, and that changes to improve DRAM technology is not the same as changes to avoid a patent. (Heye, Tr. 3811-3812 ("And, you know, there's no lost opportunity cost here because this is real -- this is bringing real value to the customer. ... So, when we spent all those 18 months, that wasn't to me lost opportunity cost, that was good old-fashioned business

acumen and engineering. Opportunity costs would have said, we've done this for let's say 15 months and then three months before you ship, now I have...three months before I ship now you've made a change which has no real end user benefits but to get around these patents we had to make these changes and that slips everything out.")). Similarly, the firms that make interoperable components with DRAMs only change their products when it is in their interest to do so, such as when the new DRAM is faster than the old DRAM. (CCFF 2561-2562). In addition, PC-OEMs only make changes to the type of DRAM they procure if it is in their interest. (CCFF 2554-2555).

Furthermore, this proposed finding ignores substantial evidence in the record that the "routine" transitions that occur in the DRAM industry are only routine because of the extensive planning that was required to implement them, and that is not comparable to the types of changes that would have to occur to avoid the Rambus patents. (Heye, Tr. 3804-3805 ("The trick is to work with all of your partners in lining it all up such that you put a lot of engineering effort and validation effort such that when you do make that transition, it is not a major disruption to the supply chains to your customer, i.e. the ones manufacturing PCs. That's your goal. And if you manage it and properly communicate with all your partners, the plans, you can manage change, because change does occur. The trick is all of the sudden when you're almost ready to launch and then you change something unexpectedly, then you have to go back and redo those plans and that's the adversity that I was referring to would occur.")).

1309. That the industry can coordinate changes in technology, even radical changes, is evidenced by AMD's experience. Prior to its K7 microprocessor, AMD produced microprocessors that were "pin compatible" with Intel processors. (Heye, Tr. 3653). That is, AMD processors could be plugged into sockets designed for Intel processors and could use the entire Intel-based infrastructure. (Heye, Tr. 3653). An infrastructure in a computer consists of a north bridge (also called a chipset), which connects the microprocessor via a bus to the memory, graphics, and the south bridge. (Heye, Tr. 3655-58). The south bridge communicates with peripheral devices, such as the keyboard and mouse, and the BIOS, which communicates with the microprocessor. (Heye, Tr. 3655-58).

Response to Finding No. 1309: The statement in this proposed finding that AMD's "experience" evidences that "the industry can coordinate changes in technology, even redical changes..." is misleading. The "transitions" described in RPF 1309 through RPF 1320 were the changes by one company, AMD, and its partners. A DRAM industry transition of the type that might be required to avoid the Rambus patents include these companies as well as the DRAM manufacturers and DRAM customers like PC-OEMs, server-OEMs and manufacturers of other products that use DRAMs. (CCFF 2547-2562).

1310. Richard Heye, Vice President and General Manager of the Microprocessor Business Unit at AMD (Heye, Tr. 3615), joined AMD in June 1997 to construct the infrastructure for the K7 processor, which did not exist. (Heye, Tr. 3652-54). AMD was able to coordinate with vendors for each part of the infrastructure and to launch complete systems by 1999. (Heye, Tr. 3646-47).

Response to Finding No. 1310: This proposed finding is incomplete because it omits testimony that development of the K7 began at AMD in the 1995-1996 time frame, up to two years prior to Mr. Heye joining AMD. (Heye, Tr. 3646-3647).

1311. During this time, AMD took no more than 15-18 months to design and produce a K7 north bridge, starting from scratch. (Heye, Tr. 3767-69). In June 1999, AMD launched the first AMD K7 processor, which used the AMD750 chipset with a 200MHz front side bus (FSB) and was compatible with PC100 SDRAM. (Polzin, Tr. 3998-4005).

Response to Finding No. 1311: This proposed finding is incomplete for the reasons described in CCRF 1310.

1312. Soon thereafter, third party vendors such as VIA designed and launched chipsets for the K7 processor that were compatible with PC133 SDRAM. (Polzin, Tr. 3998-4005; Heye, Tr. 3769-70). This change required the development of a different north bridge and a new motherboard. (Heye, Tr. 3769-70).

Response to Finding No. 1312: Complaint Counsel does not disagree.

1313. In September 2000, AMD launched a new version of the K7 processor using a 266 MHz FSB and the newly designed AMD760 chipset, which was compatible with DDR200 and DDR266. (Polzin, Tr. 3998-4005). The design of the new chipset took only 15-18 months, and the resulting chipset was not backward compatible with SDRAM. (Heye, Tr. 3767-69).

Response to Finding No. 1313: This proposed finding is incomplete as it omits testimony from Mr. Polzin that AMD chose not to make a backward compatible DDR chipset solely in order to get that chipset to market quickly. (Polzin, Tr. 3980 ("When we started the design of that, we decided to focus on getting the DDR infrastructure going with our IGD4 device, get it out there as soon as possible with the lowest risk. Adding an SDR certainly would be possible, maybe even straightforward, but it added risk, but it added not trivial schedule. We decided to go out and get DDR going, get the infrastructure going, get the industry going.")).

Furthermore, this proposed finding is incomplete because Mr. Polzin also testified that DDR was backward compatible with SDRAM and that many of AMD's chipset partners chose to make their DDR chipsets backward compatible as well. (Polzin, Tr. 3978-3979 ("DDR technology allowed both DRAM components and memory controller components to have -- to implement both the old single data rate or a PC100/PC133 spec and with the same component also implement the DDR spec, which would allow backwards compatibility, and in fact I believe most of the first DDR DRAM devices were in fact dual mode. They could work in single data rate mode and become a PC100 product or they could work in DDR mode and be a DDR product. Similarly, a number of our chipset partners did the same thing with their chipsets. They made memory controllers that could work with either a single data rate or double data rate.")).

1314. To transition from using SDRAM to DDR, the newly established AMD infrastructure needed newly designed motherboards, newly designed DIMMs, and a new BIOS. (Heye, Tr. 3767-69).

Response to Finding No. 1314: Complaint Counsel does not disagree.

1315. As part of this transition to DDR, AMD gave motherboard samples to manufacturers in March 2000, and those manufactures were able to produce the DDR compatible motherboards in volume by September 2000. (Polzin, Tr. 4017-18).

Response to Finding No. 1315: Complaint Counsel does not disagree.

1316. In fact, according to an internal memorandum, AMD decided to transition to DDR in early 1999, was able to power up a complete system by December 1999, and was shipping units by October 2000. (CX 2158 at 2; Heye, Tr. 3805-10).

Response to Finding No. 1316: Complaint Counsel does not disagree.

1317. In October 2002, AMD launched a new version of the K7 processor with a 333MHz FSB. Third party chipsets made for this version were compatible with DDR333. (Polzin, Tr. 3998-4005).

Response to Finding No. 1317: Complaint Counsel does not disagree.

1318. During these changes, portions of the infrastructure other than the chipset changed as well. For example, DDR333 had different DIMM specification from those of previous generations of DDR. (Polzin, Tr. 4006-07).

Response to Finding No. 1318: This proposed finding is misleading because it implies that changes in the DDR333 DIMM specification were accomplished by AMD rather than the DRAM manufacturers. (Heye, Tr. 3807-3808).

1319. In May 2003, AMD launched the K7 processor with a 400MHz FSB. (Polzin, Tr. 3998-4005). Matched with newly designed third party chipsets, this system uses DDR400. (Polzin, Tr. 3998-4005).

Response to Finding No. 1319: Complaint Counsel does not disagree.

1320. In sum, the AMD K7 systems went from using PC100 to PC133 to DDR200 and 266 to DDR333 to DDR400 - 5 transitions - all in the time period from June 1999 to May 2003. These transitions are illustrated in DX 31.

Response to Finding No. 1320: Complaint Counsel does not disagree.

1321. Compaq, an OEM that produced personal computers, servers, and workstations and is now part of HP (Gross, Tr. 2265), has gone through similar transitions.

Response to Finding No. 1321: The statement in this proposed finding that HP "has gone through similar transitions" as AMD is vague, and, depending on the definition of the phrase "similar transitions," contrary to the weight of the evidence. AMD is a CPU manufacturer that must generate a "virtual system" of components into an infrastructure so that it can sell its

CPUs. (CCFF 2558-2559). In contrast, HP is a PC-OEM that relies on the infrastructure generated by firms like Intel and AMD and the firms in the DRAM industry. (Gross, Tr. 2317).

1322. Compaq started using EDO DRAM in its products in 1995. (Gross, Tr. 2348-56).

Response to Finding No. 1322: Complaint Counsel does not disagree.

1323. In 1997, Compaq shifted to using PC66 SDRAM in its computers, which required different chipsets and different motherboards. (Gross, Tr. 2348-50). PC66 SDRAM was an Intel standard. (Gross, Tr. 2348-9).

Response to Finding No. 1323: The statement in this proposed finding that PC66 was an Intel standard is unreliable because Ms. Gross testified that she did not know who generated the DRAM standards. (Gross, Tr. 2361 ("I personally don't get involved in who establishes the standards as much as the fact that there is a standard, and I believe that JEDEC and Intel are the only two sources of DRAM standards historically.")).

Furthermore, that statement is contrary to the weight of the evidence that PC66/PC100 was simply a modified version of the JEDEC SDRAM standard, and that the technologies in dispute here are in the PC66/PC100 specification because they were already in use and in the SDRAM standard. (MacWilliams, Tr. 4910-4911 ("[B]ecause it was already there in the SDRAM parts. That was a previous feature that was balloted in JEDEC and approved.")). Pete MacWilliams was an Intel employee involved in the generation of the PC100 standard. (MacWilliams, Tr. 4907). PC66 was in fact PC100. (MacWilliams, Tr. 4908).

1324. In 1998, Compaq shifted to using PC100 SDRAM in its computers. (Gross, Tr. 2348-56). The PC100 SDRAM was an Intel standard. (Gross, Tr. 2348-56). It was not backward compatible with PC66 SDRAM. (Gross, Tr. 2348-56).

Response to Finding No. 1324: This proposed finding is unreliable and contrary to the weight of the evidence for the reasons described in CCRF 1323.

1325. In 1999, Compaq shifted to using PC133 SDRAM in its products. (Gross, Tr. 2348-56). The PC133 SDRAM was an Intel standard. (Gross, Tr. 2348-56).

Response to Finding No. 1325: The statement in this proposed finding that "PC133 SDRAM was an Intel standard" is unreliable Ms. Gross testified that she did not know who generated the DRAM standards. (Gross, Tr. 2361 ("I personally don't get involved in who establishes the standards as much as the fact that there is a standard, and I believe that JEDEC and Intel are the only two sources of DRAM standards historically.")).

Furthermore, this proposed finding is contrary to the weight of the evidence. The weight of the evidence is that Intel was not at all involved in the generation of the PC133 specification. By the time it standardized PC-133 SDRAM, JEDEC had recognized the need for a specification and provided the needed updates to the PC-100 specification to ensure that there would be full compatibility between the DRAMs manufactured by different DRAM manufacturers. (CX2560 at 1 ("PC133 specs were driven without us."); MacWilliams, Tr. 4912-13 ("[T]here was [sic] other people in the industry that proposed the spec changes from PC100 to make PC133 . . . specs and those were adopted and we weren't part of the loop initially.")).

1326. In 2001, Compaq/HP shifted to using DDR 266 in its products. (Gross, Tr. 2348-56). DDR requires a different chipset than does DRAM. (Bechtelsheim, Tr. 5938). DDR is not backward compatible with SDRAM; a DDR device cannot be used in an SDRAM socket (Bechtelsheim, Tr. 5958).

Response to Finding No. 1326: This proposed finding is misleading because it uses a definition of "backwards compatible" that is different than the definition used by others in the industry. This finding relies on testimony to the effect that a DRAM standard is backward compatible with a previous standard if a DRAM from the new standard can be used in a the "socket" for the old standard. Under that definition, DDR SDRAM might not be "backward compatible" with SDRAM. However, the weight of the evidence is that the term "backward compatible" means that a DRAM can be designed and manufactured that is compatible with both standards and a chipset can be designed that can be used with DRAMs from both standards. (CCFF

3245-3246). Under that definition of backward compatibility, DDR SDRAM was backward compatible with SDRAM. (Polzin, Tr. 3978-3979 ("DDR technology allowed both DRAM components and memory controller components to have -- to implement both the old single data rate or a PC100/PC133 spec and with the same component also implement the DDR spec, which would allow backwards compatibility, and in fact I believe most of the first DDR DRAM devices were in fact dual mode. They could work in single data rate mode and become a PC100 product or they could work in DDR mode and be a DDR product. Similarly, a number of our chipset partners did the same thing with their chipsets. They made memory controllers that could work with either a single data rate or double data rate.")).

1327. In late 2002, Compaq/HP shifted to using DDR 333 in its products. (Gross, Tr. 2348-56).

Response to Finding No. 1327: Complaint Counsel does not disagree.

1328. From 1995 to 2002, therefore, Compaq shifted from using EDO DRAM to PC66 SDRAM to PC100 SDRAM to PC133 SDRAM to DDR266 to DDR333 in its products.

Response to Finding No. 1328: Complaint Counsel does not disagree.

1329. There are of course other examples of the rapid product changes in the computer industry. For instance, Barry Wagner, the manager of technical marketing at nVidia, a company that produces graphics processors (Wagner, Tr. 3820), testified that nVidia launched 14 new products in the space of 6 years. (Wagner, Tr. 3875-76).

Response to Finding No. 1329: This proposed finding is incomplete because it omits testimony by Mr. Wagner that Nvidia only launches products in order to serve its markets. (Wagner, Tr. 3824 ("nVidia produces a lot of different graphics chips, each one of them is a different level of complexity, different cost structure, we sell them into different segments of the market.")).

Furthermore, this proposed finding is misleading since it implies that product launched by Nvidia were "rapid changes." There is substantial evidence in the record that it took Nvidia up to

two years to develop the graphics processors described in this proposed finding. (Wagner, Tr. 3838-3839, 3841). There is also substantial evidence in the record that changes to the DRAM standards could cause changes in the Nvidia graphics processors that could take nearly two years to complete. (CX2829 at 1; Wagner Tr. 3852-3853).

1330. In short, technological changes occur all the time within DRAM and the DRAM industry routinely coordinates the changes in complementary products.

Response to Finding No. 1330: This proposed finding lacks any reference to the record , constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is misleading and contrary to the weight of the evidence for the reasons described in CCRF 1308.

1331. If there were a change in the existing standards to incorporate alternatives to Rambus's technologies, only a small portion of the overall infrastructure would need to be changed - the chipset, the DIMM, the motherboard, and possibly the BIOS. (Heye, Tr. 3742-43).

Response to Finding No. 1331: This proposed finding is incomplete and not supported by the cited testimony. Mr. Heye never testified that "only a small portion of the overall infrastructure would need to be changed." Instead Mr. Heye testified that the changes to the standards would implicate important parts of the infrastructure that might take a lot of effort to design and implement. (Heye, Tr. 3733-3734 ("So, the concerns around [potential changes to the SDRAM standards in response to the Rambus lawsuits] would have been first, it would have taken time to establish the new standards; depending upon what they were, you would have had to change the memory component, the north bridge, possibly both, you would possibly have to change the motherboard. You may possibly have to change the [DIMM], once you've made all those changes, you would have to implement them, of course, then you would have to test – well, you

have to debug them, because again, now you're talking about multiple vendors with multiple different components. That would take time. You would have to revalidate all those modified DIMMs, and again, by DIMMs, I mean both the actual PCB and the memory chips against the north bridge, and by the way, that is a really big deal. We spent a lot of time and effort trying to get that right in the first go-round. And you certainly had potential inventory issues. You had opportunity cost issues.")).

1332. A shift to alternative technologies would thus incur no additional costs or coordination difficulties beyond those that would be incurred when the industry was in transition to a new standard. (Polzin, Tr. 4040-42).

Response to Finding No. 1332: This proposed finding is not supported by the cited testimony. Instead, the cited testimony is about a transition by AMD. Mr. Polzin testified that it would have been difficult for AMD to change its products at the time it was approached by Rambus because it was in the middle of launching its DDR-based product. (Polzin, Tr. 4041-4042 ("We had enabled a number of DRAM manufacturers, motherboard manufacturers, our own manufacturing of our chipset assuming one standard, one spec. To change that, we'd have to stop all that production, reengineer, redeploy, start production again. It would be detriment -- seriously detrimental to our business.")). Had AMD known about the patents earlier, it would have been able to avoid them. (Polzin, Tr. 4042 ("Q. So if I understand what you're saying, if you're starting at a zero base you can implement these alternatives? A. Yes. Q. Costlessly? A. Yes.")).

B. The Industry Is Not Locked In.

1333. Complaint Counsel contend that the DRAM industry is "locked in" to using the four Rambus technologies because it would be too difficult and expensive to switch to an alternative. The evidence, when evaluated from an economic perspective, contradicts this assertion.

Response to Finding No. 1333: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel

submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1. Switching Costs Are Not Prohibitive.

1334. Lock-in is a term used in economics to identify a situation where switching costs prohibit consumers from changing to another product or technology. (Rapp, Tr. 9873-74). Switching costs are the costs incurred to transition to an alternative product or technology. (Rapp, Tr. 9873-74).

Response to Finding No. 1334: Complaint Counsel does not disagree with this finding.

1335. Specific investments and switching costs are not identical. (Rapp, Tr. 9875-77). For instance, a company may make a specific investment of $100 million in building a coal-burning plant located near a particular coal mine. If, in response to an increase in the price of coal from the coal mine, the only way to avoid the paying the price increase is to shut down the plant and build a new plant in another location for $100 million, the switching costs and the specific investment of $100 million are the same. (Rapp, Tr. 9875-77). If, however, the coal plant can be converted to a gas burning plant for a cost of $5 million, the switching costs are $5 million, not the $100 million to build a new plant. (Rapp, Tr. 9875-77).

Response to Finding No. 1335: Complaint Counsel does not disagree with this finding.

1336. With respect to DRAM, the cost of constructing and equipping a fabrication facility is not relevant to switching costs. (Rapp, Tr. 9877-78). This is because a DRAM facility may produce several types of DRAM; there is no need to build a new DRAM facility to produce a new type of DRAM. (Rapp, Tr. 9877-78).

Response to Finding No. 1336: This proposed finding is unreliable because it is based on an assumption by Dr. Rapp that DRAM fabrication facilities can switch production to other DRAM technologies. (Rapp, Tr. 9878). Dr. Rapp is not competent to testify to the facts asserted. Consequently, this testimony can only be treated as an assumption by Dr. Rapp. Furthermore, as described below, this assumption is contrary to substantial record evidence, rendering unreliable Dr. Rapp's opinion that "the cost of constructing and equipping a fabrication facility is not relevant to switching costs."

Dr. Rapp's assumption that DRAM fabrication facilities can switch production to other DRAM technologies is contrary to substantial record evidence. Given the size of the investments made in DRAM production facilities, it is required that they produce DRAM non-stop. (CCFF 29-31, 101). In order for the DRAM manufacturers to be able to sell those DRAM chips, a number of complementary components are also required. (CCFF 26-28, 2550-2562). It takes a number of years for the DRAM industry to change the DRAM standard that it uses. (CCFF 2564-2565). In addition, once the DRAM manufacturer decides to switch, it can take two years or more to complete a new DRAM for production. (CCFF 65). As a result, a DRAM manufacturer cannot simply switch to another DRAM technology in response to an increase in the price of the DRAM technologies.

1337. The fact that an industry has high fixed costs and low marginal costs does not have any bearing on switching costs unless the fixed costs have to be replicated in their entirety in order to switch to a new technology. (Rapp, Tr. 9880).

Response to Finding No. 1337: Complaint Counsel does not disagree that this is Dr. Rapp's testimony.

1338. Complaint Counsel's economic expert admitted on cross-examination that he did not quantify any switching costs. (McAfee, Tr. 7716-17, 11356).

Response to Finding No. 1338: This proposed finding is incomplete because it omits testimony by Professor McAfee that he has seen switching costs but has not added them up. (McAfee, Tr. 7716-7717 ("Well, I haven't added them up. I mean, I have seen – I have certainly seen numbers in the record, but I haven't added them up.")).

Furthermore, this proposed finding is incomplete because it omits testimony by Professor McAfee that it is not practical to attempt to quantify the coordination costs, though in principal it might be possible to do so. (McAfee, Tr. 11296-11297 ("Well, in principle they could be quantified. It would be a massive challenge to actually characterize the quantity, the magnitude of

these costs. I mean, in principle you could say, well, what amount of money would it take to overcome the coordination costs, so in principle there's a quantification. It's just I don't know of any practical way to actually answer that question.")).

1339. It is not possible for an economist to make a sound judgment about whether switching costs are high enough to create lock-in without quantifying those costs. (Rapp, Tr. 9881).

Response to Finding No. 1339: This proposed finding is inaccurate and unreliable. Indeed, Dr. Rapp himself was able to give an opinion on the extent of the coordination costs required to change technologies without providing any quantification of those costs. (CCFF 2923-2926). In addition, Dr. Rapp was able to give an opinion on the extent of switching costs in the industry without quantifying the costs associated with the period of time it would take the DRAM industry to either agree upon an approach for working around the Rambus patents or to implement that approach. (CCFF 2935).

Professor McAfee disagrees that quantification is required "to make a sound judgement." (McAfee, Tr. 11297).

1340. The switching costs for a DRAM manufacturer to shift from using the Rambus technologies to alternative technologies may be calculated by summing the additional one-time-only fixed costs associated with switching to the alternative technologies. (Rapp, Tr. 9883-85). Mr. Geilhufe testified regarding his estimates of these costs. (Rapp, Tr. 9884, 10122-24).

Response to Finding No. 1340: This proposed finding is misleading and contrary to substantial evidence in the record. This proposal is misleading because it describes the switching costs for a single DRAM manufacturer without including the coordination costs that would be necessary to allow that DRAM manufacturer to sell that DRAM. (*See* CCFF 25-28, 2541-2562 regarding the need for coordination in the DRAM industry).

The statement in this proposed finding that "[t]he switching costs for a DRAM manufacturer to shift from using the Rambus technologies to alternative technologies may be

calculated by summing the additional one-time-only fixed costs associated with switching to the alternative technologies" is not supported by the cited testimony. Dr. Rapp, who was not qualified as an expert on DRAM manufacturing or the DRAM industry is not competent to testify to what the categories of costs are of switching DRAM production. Consequently, this testimony can only be treated as an assumption by Dr. Rapp. Furthermore, as described below, this assumption is contrary to substantial record evidence, rendering unreliable Dr. Rapp's opinion regarding the size of switching costs in the DRAM industry.

This proposed finding is contrary to substantial evidence in the record that there are other switching costs beside those considered by Dr. Rapp. In particular, a major switching cost is the cost of inventory that would be lost if the DRAM manufacturer did not license the technologies from Rambus. Mr. Geilhufe included inventory costs as part of his cost analysis of the alternative technologies. (Geilhufe, Tr. 9570-9571). Mr. Geilhufe defined two types of inventory: "work-in-progress" inventory and finished products inventory. (Geilhufe, Tr. 9571). Work in process inventory includes the value of the DRAM chips that are at some stage of the manufacturing process. (Geilhufe, Tr. 9571 ("There are two elements in inventory. One is the work in process element; that is, in a factory, it may take six weeks or eight weeks to complete all the 400 processing steps to create a finished wafer. That means you have work in process inventory sitting in that factory. If it's six weeks worth, you have six weeks worth of inventory.")).

1341. This calculation shows that switching costs associated with shifting to alternatives to Rambus's technologies were relatively low in comparison with the expenses associated with manufacturing DRAMs in general and that DRAM manufacturers could therefore have switched at any point. (Rapp, Tr. 9878).

Response to Finding No. 1341: This proposed finding is misleading and contrary to substantial evidence in the record for the reasons described in CCRF 1340.

1342. For example, to maintain the functionality provided by programmable CAS latency and programmable burst length when switching to fixed CAS latency and fixed burst length

requires 12 different parts (3 different CAS latencies and 4 different burst lengths). (Rapp, Tr. 9885). The additional fixed costs associated with switching to fixed CAS latency and fixed burst length are: $300,000 in additional design costs for the 3 CAS latencies; $400,000 in additional design costs for the 4 different burst types; $250,000 per part in additional qualification costs times 12 different parts; and $50,000 in additional photo-tooling costs times 12 different parts - this totals $4.3 million. (Rapp, Tr. 9885). These costs are illustrated in DX317.

Response to Finding No. 1342: This proposed finding is misleading and contrary to substantial evidence in the record for the reasons described in CCRF 1340.

Furthermore, this proposed finding is unreliable because Dr. Rapp's calculation of the costs of switching depends on the cost estimates of Mr. Geilhufe, which are themselves unreliable and contrary to substantial evidence in the record. This proposed finding is unreliable because Mr. Geilhufe's cost estimates are based solely on the *ipse dixit* of Mr. Geilhufe, who provided no supporting evidence.

Furthermore, Mr. Geilhufe's measurement of the fixed costs for photo tooling is contrary to substantial evidence in the record. Mr. Geilhufe testified that the photo-tooling cost (which consists of the costs of the photo-masks or "reticles" that are used to project the image of the circuit designs onto the wafers) for fixing the CAS latency or burst length was $50,000 for each fixed CAS latency or fixed burst length DRAM chip.

(Shirley, Tr. 4247-4248, *in camera*). Mr. Shirley further testified that, as of 2002, the replacement cost of mask sets required to fabricate SDRAM and DDR SDRAM at Micron was . (CCFF 2532-2533).

Furthermore, this proposed finding is misleading because the cost estimate for the switching cost does not include the cost of lost inventory. (*See* CCRF 1340). The total inventory cost for a DRAM manufacturer can be estimated from the testimony of Brian Shirley. (CCFF 2535). Mr. Shirley testified that for Micron the number of SDRAM chips produced per day in the

fourth quarter of 2002 was and the number of DDR SDRAM chips produced per day in that same period was . (CCFF 2535). Because it takes between 45 and 55 days for a DRAM to go through the entire fabrication process, Micron has between 45 and 55 days worth of work-in-progress inventory. (CCFF 2535). As a result, the amount of work-in-progress inventory for Micron as of the fourth quarter of 2002 was between (45 days times the number of SDRAM chips produced per day) and (55 days times the number of SDRAM chips produced per day) SDRAM chips and (45 days times the number of DDR SDRAM chips produced per day) and (55 days times the number of DDR SDRAM chips produced per day) for DDR SDRAM chips. In addition, Mr. Shirley testified that Micron maintains an average of of finished products inventory. (CCFF 2535). Assuming that the finished product inventory is kept in the same proportion as the daily production, Micron maintained SDRAM chips and DDR SDRAM chips in finished products inventory in the fourth quarter of 2002. Therefore, Micron's total inventory (work-in-progress plus finished goods) at any time in the fourth quarter of 2002 was between and SDRAM chips and and DDR SDRAM chips. Using the average selling prices constructed by Dr. Rapp of $4.87 for SDRAM and $5.13 for DDR SDRAM, the value of the total inventory for Micron of JEDEC-compliant DRAMs in the fourth quarter of 2002 was between and . (RPF 970, 1126). This is the value of inventory that Micron would not be able to sell if it did not agree to a license with Rambus but instead switched to an alternative. The total switching cost for Micron in the fourth quarter of 2002 would include at least the inventory cost and the replacement cost of the mask sets, so the total switching cost for Micron in the fourth quarter of 2002 was between and .

1343. The total of these costs – $4.3 million - is modest relative to DRAM production costs in general (Rapp, Tr. 9886), and less than the royalties paid to Rambus to license the use of programmable CAS latency and programmable burst length in SDRAM. (Rapp, Tr. 9886-87). If fixed CAS latency and fixed burst length were truly viable non-infringing alternatives, a manufacturer could profitably switch to those alternatives. (Rapp, Tr. 9886-87).

Response to Finding No. 1343: This proposed finding is unreliable, misleading and contrary to substantial evidence in the record for the reasons described in CCRF 1342.

1344. The evidence shows assuming that the alternatives were preferable in cost performance terms, it would have been relatively easy to implement certain of the proposed alternatives to programmable latency when manufacturers were going through technology upgrades or at the time of the transition from SDRAM to DDR SDRAM. (Soderman, Tr. 9418). Such regular redesigns happened on the order of every 6 to 12 or 18 months. (Soderman, Tr. 9418; Geilhufe, Tr. 9615). In particular, the fixed CAS latency alternative or the alternative or adding pins could easily have been implemented at these times.

Response to Finding No. 1344: This proposed finding ignores substantial evidence in the record that DRAM manufacturers do not implement interface design changes at the same time they implement die shrinks or density increases. (CCFF 2538-2540).

Furthermore, this proposed finding is misleading because it does not include the costs that would be incurred by the DRAM manufacturers and others to assure that the new DRAM could be used with the necessary complementary components like chipsets and motherboards. (CCFF CCFF 25-28, 2541-2562). Unless these other costs are also incurred, the DRAM manufacturers would not be able to sell the new DRAMs. (*See* CCFF 26-28).

1345. The switching costs for any combination of alternatives for Rambus's four technologies may be calculated by summing the design, qualification, and photo-tooling costs associated with those alternatives as provided by Mr. Geilhufe. (Rapp, Tr. 10124). The switching costs for the fixed CAS latency and fixed burst length alternatives are typical, if not higher than, the switching costs for the other alternatives. (Rapp, Tr. 10124).

Response to Finding No. 1345: This proposed finding is unreliable, misleading and contrary to substantial evidence in the record for the reasons described in CCRF 1340 and 1342.

Furthermore, the statement in this proposed finding that "the switching costs for the fixed CAS latency and fixed burst length alternatives are typical, if not higher than, the switching costs for the other alternatives" is not supported by the cited testimony. Dr. Rapp is not qualified as a DRAM industry expert and so is not competent to testify to what switching costs are "typical" for a DRAM manufacturer. Consequently, this testimony can only be treated as an assumption by Dr. Rapp. Furthermore, this assumption is contrary to substantial record evidence as described in CCRF 1340, rendering unreliable Dr. Rapp's opinion regarding the size of switching costs in the DRAM industry.

1346. Complaint Counsel's economic expert admitted that he did not quantify any switching costs. (McAfee, Tr. 7716-7; 11356). He also admitted that switching from Rambus's technologies to alternative technologies would be less costly than the switch from SDRAM to RDRAM. (McAfee, Tr. 7717-8).

Response to Finding No. 1346: This proposed finding is vague because the term "quantification" is undefined. Depending on the meaning of the term, this proposed finding is also incomplete because it omits testimony by Professor McAfee, that he has seen evidence of the switching costs in the record, but that he has not added the costs together. (McAfee, Tr. 7717).

2. Coordination Issues Do Not Prevent Switching.

1347. Because the DRAM industry routinely coordinates changes in DRAM technology with the various complementary manufacturers, one can infer that the switching costs to shift away from the Rambus technologies would be on the same order of magnitude as those for switching to fixed CAS latency and fixed burst length. (Rapp, Tr. 10127-28).

Response to Finding No. 1347: This proposed finding is unreliable because the sole basis for this "inference" is Dr. Rapp's unsupported statement that "switching costs are, generally speaking, relatively low when there is – when change is routine, in the same way as in the DRAM industry." (Rapp, Tr. 10128). Dr. Rapp, who was not qualified as an expert in the DRAM industry or in DRAM manufacturing, is not competent to testify to either whether change is "routine" in the DRAM industry or whether "switching costs are, generally speaking, relatively

low" in the DRAM industry. Consequently, this testimony can only be treated as assumptions by Dr. Rapp. Furthermore, these assumptions are contrary to the weight of the evidence that, in this industry, switching costs are high (CCRF 1342; CCFF 2527-2584), rendering unreliable Dr. Rapp's opinion that "one can infer that the switching costs to shift away from the Rambus technologies would be on the same order of magnitude as those for switching to fixed CAS latency and fixed burst length."

1348. Complaint Counsel's economic expert admitted that switching away from Rambus's technologies to alternative technologies would involve the same categories of costs that were incurred when the industry went from SDRAM to DDR, and from PC100 SDRAM to another grade of PC SDRAM. (McAfee, Tr. 7714-15, 11357).

Response to Finding No. 1348: This proposed finding is incomplete because it omits testimony by Professor McAfee that while the "category" of costs is the same between each transition, it is part of the process of designing the DRAM standards that they attempt to minimize those costs. (McAfee, Tr. 7715). The weight of the evidence is that it is the case that the DRAM industry attempts to minimize switching costs in the design of new standards by developing evolutionary changes. (CCFF 127-128, 2570, 2648-2649). One aspect of evolutionary change is that new DRAM standards are "backwards compatible" with the previous standard, which eases the transition from the old standard to the new standard. (CCFF 3249-3250).

1349. Coordination issues with producers of complementary goods would not prevent switching away from the Rambus technologies. (Rapp, Tr. 9889). Coordination of this sort happens all of the time in the industry; there is no evidence that suggests that any coordination issues with switching away from Rambus's technologies could not be resolved in the ordinary course of business. (Rapp, Tr. 9889-90).

Response to Finding No. 1349: This proposed finding is misleading because it implies that changes to the DRAM standards could happen quicky enough that DRAM manufacturers could switch from the disputed technologies to alternatives. However, this

implication is contrary to the weight of the evidence that switching costs are high in this industry. (CCRF 1342; CCFF 2527-2584).

The statement in this proposed finding that "[c]oordination of this sort happens all of the time in the industry; there is no evidence that suggests that any coordination issues with switching away from Rambus's technologies could not be resolved in the ordinary course of business" is not supported by the cited testimony. Dr. Rapp is not competent to testify whether "[c]oordination of this sort happens all of the time in the industry." Consequently, this testimony can only be treated as an assumption by Dr. Rapp. Furthermore, as described below, this assumption is contrary to substantial record evidence, rendering unreliable Dr. Rapp's opinion that "[c]oordination issues with producers of complementary goods would not prevent switching away from the Rambus technologies."

The statement in this proposed finding that "[c]oordination of this sort happens all of the time in the industry; there is no evidence that suggests that any coordination issues with switching away from Rambus's technologies could not be resolved in the ordinary course of business" is contrary to the weight of the evidence. DRAM manufacturers, manufacturers of complementary components like chipsets and DRAM customers all switch only when it is in their interest to switch. For example, DRAM manufacturers only do die shrinks or density increases if it will reduce the cost per bit of the DRAM or the DRAM manufacturer's customers want the change in density. (Becker, Tr. 1155-57; *see*, DX0007 at 18 ("probably the biggest thing we do to influence or decrease our costs on a regular basis is we shrink the technology, and the reason that works so well is that we're able to produce the same part with the same function,... but we can produce it on a smaller chip.... So if you have a smaller chip, you can fit more of those chips on a wafer, your cost per chip is greatly reduced..."); Becker, Tr. 1153-54). In addition, in order for the industry to

switch, companies that have not been subject to Rambus lawsuits will also have to switch even though they have no incentive to do so. (CCFF 2554-2555, 2561-2562).

1350. Coordination for a switch away from Rambus's technologies would not be difficult even if the DRAM industry has made investments in using the Rambus technologies. (Rapp, Tr. 9890). If there were truly viable non-infringing alternatives, the coordination issues faced by the industry would not be any more difficult than those that the industry faces routinely in other situations. (Rapp, Tr. 9890-91).

Response to Finding No. 1350: This proposed finding is misleading, unreliable, and contrary to the weight of the evidence for the reasons described in CCRF 1347-1349.

Furthermore, the statement in this proposed finding that "[i]f there were truly viable non-infringing alternatives, the coordination issues faced by the industry would not be any more difficult than those that the industry faces routinely in other situations" is not supported by the cited testimony. Dr. Rapp is not competent to testify to whether "the coordination issues faced by the industry would not be any more difficult than those that the industry faces routinely in other situations." Consequently, this testimony can only be treated as an assumption by Dr. Rapp. Furthermore, this assumption is contrary to substantial record evidence (*see* CCRF 1347-1349), rendering unreliable Dr. Rapp's opinion that "[c]oordination for a switch away from Rambus's technologies would not be difficult even if the DRAM industry has made investments in using the Rambus technologies."

1351. Complaint Counsel contend that coordination would be difficult because some DRAM manufacturers are licensed under Rambus's patents, but others are not. But the fact that some DRAM manufacturers are licensed to use Rambus's technologies and others are not would not affect the ability of the industry to coordinate switching (Rapp, Tr. 9891-92), because all manufacturers have an interest in using alternatives that are best in cost-performance terms. (Rapp, Tr. 9801-92).

Response to Finding No. 1351: This proposed finding is unreliable because it is based on an assumption that "all manufacturers have an interest in using alternatives that are best in cost-performance terms," and ignores the interest that licensed DRAM manufacturers might

have in ensuring that their competitors who are not licensed are either excluded from the DRAM market by the Rambus patents, or are paying higher royalties because they chose to litigate. McAfee, Tr. 7447-7450). Furthermore, there is substantial evidence in the record that Rambus planed to pursue the strategy of either charging higher royalty rates to those firms that choose to litigate, or not licensing some of those firms at all. (CCFF 1990-1993).

The statement in this proposed finding that "all manufacturers have an interest in using alternatives that are best in cost-performance terms" is not supported by the cited testimony. Dr. Rapp is not competent to testify to the facts asserted. Consequently, this testimony can only be treated as an assumption by Dr. Rapp. Furthermore, this assumption is contrary to substantial record evidence, as described above, rendering unreliable Dr. Rapp's opinion that "the fact that some DRAM manufacturers are licensed to use Rambus's technologies and others are not would not affect the ability of the industry to coordinate switching."

1352. Complaint Counsel's economic expert admitted that he did not reach a conclusion as to whether the interests of the 50% who have licensed from Rambus have interests regarding a standard that eliminates the patented technologies that are different from the 50% who have not taken a license. (McAfee, Tr. 7723).

Response to Finding No. 1352: This proposed finding is inaccurate. Professor McAfee testified that he studied but not come to a conclusion on the question of "whether the interests of the 50 percent that are licensed and the 50 percent that are not licensed are all consistently in favor of adopting a standard that eliminates the patented technologies." (McAfee, Tr. 7723).

1353. DRAM manufacturers were not locked in to using the Rambus's technologies at any point in time from 1990 to today. (Rapp, Tr. 9896). Their continued used of the Rambus technologies is due to the fact that the four Rambus technologies are superior in cost-performance terms to any alternatives. (Rapp, Tr. 9896-99). This is true for the two Rambus technologies used in SDRAM, the four used in DDR, and the four used in DDR2. (Rapp, Tr. 9896-99).

Response to Finding No. 1353: The statement in this proposed finding that "DRAM manufacturers were not locked in to using the Rambus's technologies at any point in time from 1990 to today" is contrary to the weight of the evidence. (CCFF 2500-2585, 2659-2756, 2914-2937; CCRF 1259-1352).

The statement in this proposed finding that "continued used of the Rambus technologies [by the DRAM manufacturers] is due to the fact that the four Rambus technologies are superior in cost-performance terms to any alternatives" is contrary to the weight of the evidence. (CCFF 2102-2414; CCRF 969-988, 1125-1140).

The statement in this proposed finding that "[t]his is true for the two Rambus technologies used in SDRAM, the four used in DDR, and the four used in DDR2," is contrary to the weight of the evidence. (CCFF 2102-2414, 3229-3261; CCRF 969-988, 1125-1140).

1354. The fact that the DRAM industry continues to use the four Rambus technologies in DDR2 when that standard was developed after Rambus's issued patents and their claimed scope were well known in the industry demonstrates that Rambus's technologies were superior in cost-performance terms even taking into account Rambus's royalty rates. (Rapp, Tr. 9898-99).

Response to Finding No. 1354: This proposed finding is contrary to the weight of the evidence that the DRAM industry was locked in to the technologies in the DDR-2 SDRAM standard, and continued to use the technologies claimed by Rambus because changing the DDR-2 SDRAM standard to avoid the Rambus patents would cause disruption and delay to the development and implementation of the standard. (CCFF 3229-3261).

C. Summary Of Findings On The Issue Of Lock In.

1355. Multiple standards have coexisted in the DRAM industry for the entire relevant period.

Response to Finding No. 1355: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel

submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1356. Manufacturers have produced multiple types of DRAM at any given time.

Response to Finding No. 1356: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1357. Manufacturers routinely redesign DRAM products.

Response to Finding No. 1357: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1358. The industry routinely coordinates switching to new types of DRAM.

Response to Finding No. 1358: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1359. Complaint Counsel has failed to show that the costs for a DRAM manufacturer to switch to alternatives for the Rambus technologies in SDRAM and DDR are prohibitive.

Response to Finding No. 1359: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1360. Complaint Counsel has failed to show that coordination issues prohibit the industry from adopting alternatives to Rambus's technologies.

Response to Finding No. 1360: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

XI. RAMBUS'S ROYALTIES ARE IN FACT REASONABLE AND NON-DISCRIMINATORY.

1361. Because JEDEC would have adopted in the but-for world the Rambus technologies incorporated in SDRAM and DDR had Rambus made the additional disclosures that Complaint Counsel contend should have been made without any *ex ante* negotiation of the royalty rates, Rambus and the DRAM manufacturers would have negotiated licenses for Rambus's patents *ex post*, as they did in the real world.

Response to Finding No. 1361: RPF 1361 lacks any reference to the record, constitutes legal argument and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Moreover, the statement in RPF 1361 that Rambus and DRAM manufacturers would have negotiated Rambus's licenses ex post as they did in the real world is contrary to the weight of the evidence. If Rambus had disclosed that it had pending patent applications containing claims, or could have amended its pending applications to add claims JEDEC would not have adopted Rambus's technologies into its SDRAM and DDR SDRAM standards. (CCFF 2415; G. Kelley, Tr. 2575, 2564-65; Rhoden, Tr. 350; Landgraf, Tr. 1714 ("If we knew in advance that they were not going to comply with the JEDEC patent policy, we would have voted against it.")).

1362. The only difference between the but-for world and the actual world would be that, in the but-for world, Rambus would have given a commitment to license on reasonable terms and conditions that are demonstrably free from unfair discrimination. If Rambus's actual royalty rates are in fact reasonable and nondiscriminatory, there is no difference between the but-for world and the real world.

Response to Finding No. 1362: RPF 1362 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Moreover, the statements in RPF 1362 contrary are to the weight of the evidence. First, the evidence shows that even if Rambus had issued a RAND letter, JEDEC would have adopted alternative royalty-free technologies. (CCFF 3029-30). Second, the weight of the evidence shows that Rambus would not have committed to a license on reasonable and non-discriminatory terms. (CCFF 2418-32). The notion that Rambus would have offered to license its intellectual property on reasonable and nondiscriminatory terms is inconsistent with Rambus's statements, business model, and its licensing strategy for RDRAM. (McAfee, Tr. 7489-90).

1363. As discussed below, Rambus's royalty rates for its SDRAM and DDR technologies are reasonable and non-discriminatory. This means that, not only would JEDEC have adopted the same technologies in the but-for world, but the licensing rates in the but-for world and the real world are identical.

Response to Finding No. 1363: The statement in RPF 1363 that "Rambus's royalty rates for its SDRAM and DDR technologies are reasonable and non-discriminatory" lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Moreover, the statements in RPF 1363 are contrary to the weight of the evidence. First, the weight of the evidence shows that Rambus's royalty rates for SDRAM and DDR are unreasonable and discriminatory. (CCRF 1371, 1384, 1405). Second, the evidence shows that if Rambus had disclosed its patents and patent applications, regardless of any RAND assurances, JEDEC would

have adopted alternative royalty-free technologies. (CCFF 3029-30). Finally, the statement in RFP 1363 that licensing rates in the but-for world and real world are identical is contrary to the weight of the evidence. (CCFF 2441-64).

1364. Rambus offered the expert testimony of Professor Teece on the issue of whether Rambus's royalties were reasonable and nondiscriminatory. Professor Teece is well qualified to opine on this issue.

Response to Finding No. 1364: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Professor Teece's testimony regarding the reasonableness and discriminatory nature of Rambus's royalty rates is unreliable because Professor Teece lacked sufficient basis to offer opinions regarding royalty rates for patents or innovations in the DRAM industry. Professor Teece based his opinions on his understanding of licensing negotiations in a collection of diverse industries. (Teece, Tr. 10463-10466). The statement in this proposed finding that Professor Teece is "well qualified to opine" on the issue of whether Rambus's royalties were reasonable and nondiscriminatory ignores substantial evidence in the record that Professor Teece has no knowledge of royalty rates for similar innovations in the DRAM industry. (Teece, Tr. 10465 ("Q. Did you, as part of your reasonable royalty analysis, consider -- did you have any particular data point or data points relating to royalty rates paid for patents covering a DRAM interface technology? A. Well, you know, I considered that inasmuch as I looked for every piece of evidence that was in the record in this case and in the public domain, but the situation is such that we don't have data at that level of granularity available to us, nor is it particularly a problem given the way that license negotiations typically take place.")). Furthermore, there is no record evidence

that Professor Teece was aware of any licensing agreements for technologies incorporated into the JEDEC DRAM standards. (Teece, Tr. 10463-10466).

Furthermore, despite the fact that Professor Teece was attempting to determine the "benchmark" that might be used by negotiators in determining the appropriate royalty rate for SDRAM and DDR SDRAM licenses (Teece, Tr. 10653-10654), Professor Teece could not recall conducting any review of the evidence regarding what *Rambus* actually considered to be a reasonable benchmark for its SDRAM and DDR SDRAM related intellectual property. (Teece, Tr. 10654-10655). As a result of the fact that he did not do such a review, Professor Teece did not review testimony by Geoffrey Tate, the Rambus CEO who testified as follows "Q Was the .75 royalty rate based on other licenses for semiconductors that you were aware of?

Q. So I mean that wasn't a consideration as far as arriving at the royalty percentages under the SDRAM and DDR licensing agreements, that other license agreements in the semiconductor industry weren't a consideration?...

((CX2060 at 157-158 (Tate, Dep.), *in camera status requested*; Teece, Tr. 10659).

1365. Professor Teece has studied the semiconductor industry for many years; he has consulted in the industry; and he has focused on understanding patents, licensing and cross-licensing in the semiconductor industry. (Teece, Tr. 10301-02).

Response to Finding No. 1365: This proposed finding is vague and potentially misleading to the extent that it implies that Professor Teece has similar knowledge in the DRAM

industry specifically, or has done an analysis capable of determining the results of negotiations between Rambus and potential licensees, for the reasons described in CCRF 1364.

1366. Professor Teece is frequently called to advise companies on their licensing policies and the design of licensing arrangements and agreements. (Teece, Tr. 10303). He is also frequently asked to testify on antitrust and patent damages issues. (Teece, Tr. 10303). Much of his consulting work involves the semiconductor industry. (Teece, Tr. 10303). Over the last 20 years, he has advised at least a dozen companies on licensing and licensing strategy. (Teece, Tr. 10417). In addition, as the member of the board of directors of several companies, he has approved licensing agreements and on some occasions actually negotiated them. (Teece, Tr. 10419).

Response to Finding No. 1366: This proposed finding is misleading to the extent that it implies that Professor Teece has done an analysis capable of determining the results of negotiations between Rambus and potential licensees for the reasons described in CCRF 1364.

1367. More recently, he published a paper on licensing and cross-licensing in the semiconductor industry that was published in the California Management Review. (Teece, Tr. 10302). He has written a number of times on the issue of licensing, including one of the first studies on technology transfer and technology licensing (for which he interviewed over one hundred licensing executives). (Teece, Tr. 10418). In the mid-1990's, Professor Teece did a study on cross-licensing during which he interviewed more licensing executives. (Teece, Tr. 10418).

Response to Finding No. 1367: Professor Teece conducted his major licensing study over a quarter century ago. (Teece, Tr. 10418). Moreover, the study Professor Teece conducted in the mid-1990's was not specific to the semiconductor industry. (*Id.*) This proposed finding is misleading to the extent that it implies that Professor Teece has done an analysis capable of determining the results of negotiations between Rambus and potential licensees for the reasons described in CCRF 1364.

1368. Professor Teece has been a member of the Licensing Executives Society for about 20 years. (Teece, Tr. 10417). He has addressed licensing executives at the annual meeting of the Licensing Executives Society and he has published two papers in the journal of that society. (Teece, Tr. 10418).

Response to Finding No. 1368: The Licensing Executives Society is not specific to the DRAM or semiconductor industry. This proposed finding is misleading to the extent that it

implies that Professor Teece has done an analysis capable of determining the results of negotiations between Rambus and potential licensees for the reasons described in CCRF 1364.

1369. Professor Teece has been qualified as an expert in a number of courts to testify on the issue of reasonable royalties. (Teece, Tr. 10419).

Response to Finding No. 1369: To the extent that it implies that Professor Teece has done an analysis capable of determining the results of negotiations between Rambus and potential licensees, this proposed finding is misleading for the reasons described in CCRF 1364.

1370. Complaint Counsel's economic expert, on the other hand, admitted that he had no expertise determining a reasonable royalty rate. (McAfee, Tr. 7737). Nor does he have any expertise in the areas of licensing or technology transfer. (McAfee, Tr. 11245).

Response to Finding No. 1370: Professor McAfee has looked at the question of how he would determine what a reasonable royalty rate would be based on a hypothetical negotiation. (McAfee, Tr. 7737). More importantly, Professor McAfee has extensive expertise in the DRAM industry and the factors that make that industry unique, and reviewed extensive portions of the record including the entire trial transcript up to the week of his testimony. (McAfee, Tr. 7154).

A. Rambus's Royalty Rates Are Reasonable.

1371. Rambus's royalty rates for its SDRAM and DDR technologies are "reasonable" within the meaning of the EIA/JEDEC patent policy.

Response to Finding No. 1371: RPF 1371 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Moreover, the statement in RFP 1371 that Rambus's royalty rates for SDRAM and DDR are "reasonable" within the meaning of the EIA/JEDEC patent policy is incomplete and misleading. First, EIA and JEDEC do not determine what consitutes a "reasonable" royalty rate.

(CCFF 355-56). As Rambus noted, JEDEC lets parties to a negotiation determine whether a royalty rate is reasonable. (RPF 1372; CCFF 356). At least one of the parties involved in licensing negotiations with Rambus believed that Rambus's proposed 3.5% royalty rate for DDR was "exorbitant" and refused to pay. (Appleton, Tr. 6390 ("We thought [the rates] were exorbitant. We didn't think they were reasonable at all."); *see also* RX 0855 at 1 ("0.1% royalty okay, 1-2% ridiculous)).

Second, while JEDEC does not take a position on the reasonableness of individual royalty rates, it does demand that members abide by JEDEC's rules and regulations. (RX 1461 a 1). JEDEC's rules, as set forth clearly in the EIA Legal Guides, demand that members act in good faith. (CCFF 310-312). Because Rambus subverted the JEDEC process, its royalty rates do not comply with the RAND requirement expressed in the JEDEC rules.

1. The JEDEC Rules Defined "Reasonable" As The Rate Determined By The Market.

1372. Mr. Kelly, the EIA General Counsel, testified that EIA does not get involved in the determination whether terms are reasonable and non-discriminatory; rather, EIA leaves this determination to the "marketplace," i.e., a willing licensee and licensor engaged in arms-length negotiation. (J. Kelly, Tr. 1882-83). As he explained, "We don't get into the definition, the further definition of reasonable and nondiscriminatory at all. We leave that to the parties to work out or the courts." (J. Kelly, Tr. 2073-74).

Response to Finding No. 1372: Complaint Counsel has no specific response.

1373. Mr. Kelly also admitted that it is not one of the goals of EIA or JEDEC to get the lowest possible royalty rate if there is intellectual property in the standards. (J. Kelly, Tr. 2073).

Response to Finding No. 1373: The statement in RPF 1373 that it is not one of JEDEC's goals to obtain the lowest possible royalty rate if there is intellectual property in the standard is incomplete. Mr. Kelly further testified that a more important goal of JEDEC is "produc[ing] a standard which is going to gain marketplace acceptance" and, therefore, JEDEC is hesitant to include intellectual property in a standard at all "because of the fact that there may be a

royalty that may increase the cost." (Kelly, Tr. 2073-74). If a technology covered by intellectual property is included in the standard, JEDEC does not get involved in determining whether royalty rates are reasonable. RPF 1372. JEDEC members, however, are concerned about negotiating the lowest possible royalty. CCFF 741, 2441-54.

1374. Robert Goodman of Kentron testified that he understood a reasonable rate to be what the market will agree to pay. (Goodman, Tr. 6088).

Response to Finding No. 1374: Mr. Goodman's testimony should be understood to apply to a royalty rate that the market agreed to pay before industry members become locked in to using a technology incorporated in a standard. *See, e.g.*, CCFF 2962-75.

1375. Similarly, according to Desi Rhoden, whether licensing terms for patents covering JEDEC compliant products were "fair and reasonable" is to be determined by the courts. (Rhoden, Tr. 658, 663; RX-1461 at 1).

Response to Finding No. 1375: While JEDEC does not take a position on the reasonableness of individual royalty rates, it does demand that members abide by the spirit of JEDEC's rules and regulations. The document Rambus cites in this finding, RX-1461, illustrates this point. In 1999, Mosaid told Jim Townsend that it would conform to the JEDEC policy by offering "non-discriminate licensing at 'reasonable rates.'" Mosaid's representative asked Mr. Townsend to interpret JEDEC's RAND policy, and specifically the term "non-discriminatory." Mr. Townsend replied that JEDEC does not comment on individual negotiations and "is only interested in the broader picture that you abide by the bylaws." (RX1461 at 1). Since Rambus subverted the JEDEC process and did not abide by JEDEC's bylaws, its royalty rates are not reasonable under EIA and JEDEC rules.

2. Rambus's Royalties Are Comparable To Other Licensing Rates In The Industry And Are "Reasonable" Under The JEDEC Rules.

1376. The evidence shows that Rambus's royalty rates for its SDRAM and for DDR licenses are reasonable. First, as shown below, Rambus's royalty rates are low relative to industry rates in the semiconductor industry.

Response to Finding No. 1376: RPF 1376 lacks reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Moreover, the statement in RFP 1376 that Rambus's royalty rates are low compared to other licensing rates in the seminconductor industry is inaccurate and misleading. First, license rates charged by companies that are not pure play technology companies are not entirely comparable to license rates charged by pure play technology companies such as Rambus. (Teece, Tr. 10622-23; CCFF 2985). Second, Rambus's examples of industry royalty rates do not necessarily involve technologies comparable to Rambus's technologies. (Teece, Tr. 10624-25 (Rambus's expert admitted that he was not qualified to testify about whether the royalty rates he used to form his opinion involved technologies comparable to Rambus's technologies)). Third, some of the documents Rambus cited to support its conclusions are unreliable. (CCRF 1390, 1391). Fourth, Rambus's examples are distinguishable from Rambus's situation and are not a reasonable benchmark in assessing the value of Rambus's patents. (CCRF 1378-84, 1388-89).

1377. Rambus's royalty rate for its SDRAM licenses is .75%. (Rapp, Tr. 9832). Its royalty rate for its DDR licenses (with the exception of its license to Hitachi) is 3.5%. (Rapp, Tr. 9853-53). These rates are low compared to other licensing rates in the semiconductor industry.

Response to Finding No. 1377: It is impossible to state what the Rambus royalty is. A number of agreements provide for royalty rates of for SDRAM and for DDR SDRAM. One agreement provides for royalty rates of for SDRAM and for DDR SDRAM. (CCFF 1999-2000 (*in camera*). More significantly, DRAM manufacturers accounting for a significant portion of DRAM sales are in litigation with Rambus, and Rambus has stated that

it plans to charge higher royalty rates to companies that litigate, and might not license them at all. CCFF 2035-37.

1378. The IBM Worldwide Licensing Policy sets forth royalty rates from 1-5% of selling price: "The royalty for use of IBM's patents may be based on the licensee's selling price of each product covered by one or more licensed patents or on the royalty portion selling price of such product, the choice being left to the licensee. . . . The royalty rates are 1% of the selling price if the product is covered by one Category I patent and 2% of the selling price if the product is covered by two or more Category I patents . . . . If the product is covered by one, two or three or more Category II patents, the royalty will be, respectively, 1%, 2% or 3% of the selling price added to any royalty incurred for Category I patents." (JX 9 at p.24).

Response to Finding No. 1378: IBM's patent policies are irrelevant to the reasonableness analysis of Rambus's royalty rates for several reasons. First, Rambus's economic expert could not identify a particular license by IBM in which a company paid a royalty rate between 1 and 5 percent for a DRAM technology. (Teece, Tr. 10640). Second, the IBM Worldwide Licensing Practices is a generic document and does not reflect any JEDEC activity or "the results of any negotiations on a specific patent activity" (Kellogg, Tr. 5038). Third, it did not represent IBM's position with respect to its licensing policy vis-a-vis JEDEC members. (Kellogg, Tr. 5038; *see also* CCRF 1376). Fourth, Rambus's expert could not identify any specific IBM technology that was adopted into a JEDEC DRAM standard to which this document related. In short, there is no record evidence that any company, let alone a JEDEC member, is paying IBM any royalty rate, let alone a rate between 1% and 5%, for any technology, let alone a technology incorporated in a JEDEC standard.

1379. Mark Kellogg presented this IBM Worldwide Licensing policy to JEDEC at a meeting of J42.5 on December 2, 1991. (JX 9 at 24; Kellogg, Tr. 5232, 5238-39). No one, to his memory, suggested that IBM's license rates were unreasonable. (Kellogg, Tr. 5238-39). Mr. Kellogg was not authorized by IBM to discuss royalty rates; he therefore could not tell anyone at JEDEC that IBM would license on other than IBM's standard rates. (Kellogg, Tr. 5236-37).

Response to Finding No. 1379: JEDEC did not take any position with respect to whether royalty rates were reasonable; any negotiation of rates took place outside of JEDEC

between individuals responsible for licensing. *See* RPF 1372. Thus, it is not surprising that Mr. Kellogg does not recall anybody saying anything about the royalty rates. There is no evidence in the record of any JEDEC member paying royalties of between 1% and 5% for any IBM technology used in any JEDEC standard. *See also* CCRF 1378.

1380. Gordon Kelley agreed that the IBM Worldwide Licensing Policy shown at the December 1991 JEDEC meeting shows royalty rates of 1-5%, and he too did not recall anyone saying that these rates were unreasonable. (Kelley, Tr. 2618-20).

Response to Finding No. 1380: *See* CCRF 1378-79.

1381. The IBM Standards Practice Manual that was in effect in 1996 states, "The normal royalty rate for a license to IBM patents ranges from 1% to 5% of the selling price for the apparatus that practices the patents. This is a very reasonable rate in our industry and generally meets the requirement of standards organizations that licenses be made available on reasonable and nondiscriminatory terms and conditions." (RX 653 at IBM/2 128124).

Response to Finding No. 1381: This proposed finding is incomplete. The same page of this document contemplates that IBM will be requested to grant rights to patents on terms other than royalty rates of 1% to 5%, and sets forth the procedure for approval of such terms. RX 0653 at IBM/2 128124; *see also* CCRF 1378.

1382. Similarly, the IBM Standards Program, which superseded the IBM Standards Practice Manual, states, "The normal royalty rate for a license to IBM patents ranges from 1 percent to 5 percent of the selling price for the apparatus that practices the patents. This is a very reasonable rate in our industry and generally meets the requirement of standards organizations that licenses be made available on reasonable and nondiscriminatory terms and conditions." (RX 653 at IBM/2 153802).

Response to Finding No. 1382: This proposed finding is incomplete. The same page of this document contemplates that IBM will be requested to grant rights to patents on terms other than royalty rates of 1% to 5%, and sets forth the procedure for approval of such terms. RX 0653 at IBM/2 153802; *see also* CCRF 1378.

1383. The IBM website contains IBM's Standards Practices and states that IBM's royalty rates for patent licenses granted to members of standard-setting organizations is 1-5%. (RX 2105-07 at 1).

Response to Finding No. 1383: *See* CCRF 1378.

1384. AMD

(Heye, Tr. 3919-20 (*in camera*); CX 1420 at 8 (*in camera*)).

Response to Finding No. 1384: The statement in RFP 1384 that

is misleading and based on incomplete evidence Mr Heye stated that

(Heye, Tr. 3918, *in camera*). Indeed, Mr. Heye's testimony establishes that {the other company's patent on core technology was more valuable than Rambus's patent on the interface, and that

(Heye, Tr. 3918, *in camera*) (

).

1385. In February 1990, Digital Equipment Corporation wrote to JEDEC to inform its members that Digital would agree to license its U.S. Patent No. 4,851,834 and corresponding foreign patents for a royalty rate of 1% of sales. (JX 1 at 24).

Response to Finding No. 1385: The finding is unreliable. No fact witness testified about this document. Rambus's economics expert, Professor Teece, could not recall (1) whether the DEC technology at issue was a DRAM technology; (2) what JEDEC committee or standard, if any, the technology related to; (3) whether JEDEC ever adopted a standard using that technology; (4) whether the DEC technology was ever widely used or adopted; and (4) whether DEC ever collected royalties from any company at the 1% rate. (Teece, Tr. 10637-38). RPF 1385 is also

contrary to the weight of the evidence. The V-PACK episode establishes that, almorst two years after the document cited by Rambus and when Rambus was in attendance at a JEDEC meeting, JEDEC members balked at adopting a technology subject to 1% royalty. (CCFF 873-75).

1386. After DRAM manufacturers complained of administrative burdens associated with royalty agreements, Kentron changed from charging 5% royalties for Kentron's FEMMA technology to pricing its patented flex tabs, which are a necessary input for the FEMMA technology, so as to receive the equivalent of the 5% royalty. (Goodman, Tr. 6020-22, 6078-80). Kentron has also set the price of its patented switches, used in its QBM technology, such that for a QBM product priced around $200, the purchaser would pay an additional $18 included within that price for the Kentron patented QBM technology (approximately 9%). (Goodman, Tr. 6087). As a matter of economics, a higher price built into a product that is a necessary input is the equivalent of the same amount charges as a royalty. (Teece, Tr. 10432).

Response to Finding No. 1386: Finding No. 1386 is misleading and incomplete. First, only two small companies ever paid Kentron royalties in the 5% range, and both companies did not have access to alternative technologies. (Goodman, Tr. 6021-23, 6025). In other words, a 5% royalty rate reflects a monopoly royalty rate, not a reasonable royalty rate. Second, the record contains no evidence that Kentron technology was adopted by JEDEC as a standard. (Teece, Tr. 10437, 10635). Finally, because Kentron is selling finished products, its prices are not comparable to license rates of pure-play technology companies such as Rambus. (Teece, Tr. 10622-23).

1387. Mr. W.R. Griffin, the DRAM product line manager for IBM, wrote in an August 11, 2000 email that Rambus's SDRAM royalty rate produced only a relatively small exposure for IBM: "If we were faced with a fee for 2001 then I believe our exposure is relatively small. This year 99% of our sales are SDR." (RX 1695 at 2; Kellogg, Tr. 5248).

Response to Finding No. 1387: This finding is irrelevant to Rambus's argument that its royalty rates are low relative to industry rates. Furthermore, RAmbus has misinterpreted this document. Rambus failed to call Mr. Griffin to testify about the document and clarify what he meant in the quoted passage. Mr. Kellogg flatly disagreed with Rambus's interpretation of the document. (Kellogg, Tr. 5249 ("And did you understand that one of the questions was what was

IBM's exposure in connection with the Rambus patents? A. No. That's not what this was saying.")).

1388. Published judicial decisions show that in 1993, Hyundai entered into a semiconductor cross-license with Texas Instruments and agreed to pay a royalty of 8% on all its sales of semiconductor products, including DRAM. *Texas Instruments, Inc. v. Hyundai Electronics Indus.*, 42 F. Supp. 2d 660, 663-64, 671, 676-77 & n.39 (E.D. Tex. 1999); *Texas Instruments, Inc. v. Hyundai Electronics Indus.*, 49 F. Supp. 893, 897 (E.D. Tex. 1999).

Response to Finding No. 1388: The terms of broad cross-licencing agreements, such as the agreement between Hyundai and Texas Instruments, are not comparable to the discrete licensing agreements at issue in this case. As the court in *Texas Instruments v. Hyundai Electronics* explained, mammoth companies "like Texas Instruments and Hyundai turn to broad, portfolio-like cross-license agreements . . . [to] avoid the costly and inefficient endeavor of a patent-by-patent licensing scheme." *Texas Instruments, Inc. v. Hyundai Electronics Indus.*, 42 F. Supp. 2d 660, 664 (E.D. Tex. 1999). The technologies being licensed in the Texas Instruments agreements are inclusive and relate to all aspects of DRAMs, including design, production, and the manufacturing process. (Teece, Tr. 10461-63). Rambus's expert Professor Teece admitted that the patent portfolio Texas Instruments licensed to Hyundai was "very large" and could well include more than one thousand patents. (Teece, Tr. 10462). In contrast, Rambus is licensing a discrete number of patents that relate only to specific, limited features in DRAM interfaces.

In sum, Rambus has failed to establish that a royalty rate involving two companies relating to an entire patent portfolio that relate to all aspects of DRAMs, including design, production and the manufacturing process, in all semiconductor products, that was negotiated in unexplained circumstances, and that in any event was apparently unrelated to any industry standard, has any bearing on what JEDEC members would have considered to be a reasonable royalty rate in connection with a decision of whether to incorporate Rambus's technologies, rather than the available alternatives, into the JEDEC standards.

1389. Samsung entered into a similar cross-license with Texas Instruments in which it agreed to pay 9% on the sales of DRAMs in the United States and 3% on the sales of DRAMs in Japan. *Texas Instruments, Inc.*, 49 F. Supp. at 902. Texas Instruments offered Hyundai similar terms on DRAM sales. *Id.*

Response to Finding No. 1389: The terms of broad cross-licencing agreements, such as agreements between Texas Instruments and DRAM manufacturers, are not comparable to the discrete licensing agreements at issue in this case. The technologies being licensed in the Texas Instruments agreements are inclusive and relate to all aspects of DRAMs, including design, production, and the manuacturing process. (Teece, Tr. 10461-62). The patent portfolio Texas Instruments licensed to Samsung and Hyundai was "very large" and could well include more than one thousand patents. (Teece, Tr. 10462). In contrast, Rambus is licensing a small number of patents that relate only to DRAM interface technology. Indeed, Rambus's own economics expert testified that the 9% royalty rate Samsung paid to Texas Instruments was not a reasonable benchmark for the value of the Rambus technologies at issue in this case. (Teece, Tr. 10611).

1390. The Licensing Economics Review conducted a survey of semiconductor licenses that was published 2001. (Teece, Tr. 10444-45; RX 2105-05). This survey found 78 licenses for semiconductors with an average royalty rate of 4.6% and a median rate of 3.2%. (Teece, Tr. 10444-45; RX 2105-05 at 5). The royalty rates ranged from 0% to 30%. (RX 2105-05 at 5).

Response to Finding No. 1390: Your Honor stated that Professor Teece could use the 2001 Licensing Economics Review only to the extent it helped him from his opinion on the issue of semiconductor licenses, not for its truth independently. (Teece, Tr. 10443-44). Because Rambus now cites this document for the truth of the matter asserted, Complaint Counsel submits that this finding should be disregarded pursuant to this Court's July 10, 2003 Order on Post Trial Briefs.

If Your Honor does not strike this finding, then it should be given little weight. First, because Professor Teece did not author the document, Complaint Counsel was denied the opportunity to cross-examine him about the data set, how the charts were developed, and what

criteria was used. (Teece, Tr. 10443). Second, the chart purports to illustrate royalty rates in 15 industries ranging from "entertainment" to "food" and is not specific to the semiconductor or DRAM industry. Third, the survey calculated its median royalty rate based on royalties as high as 30%. (Teece, Tr. 10643). Indeed, You Honor stated that you would not give evidence such as this a great deal of weight. (Teece, Tr. 10450).

1391. PLX Systems Survey conducted a commissioned study of licenses in the category of Semiconductors and Related Devices (SIC code 3674) in an Ernst & Young database, which was published in January 2003. (Teece, Tr. 10446-47; RX 2105-03). This survey found 238 license agreements with payment terms. (RX 2105-03 at 2). Of those, 106 agreements had royalty rates based on net sales and 5 were based on gross sales. (RX 2105-03 at 3). The average royalty rate for the agreements based on net sales was 4.54% and the median rate was 4%. (RX 2105-03 at 3; Teece, Tr. 10448).

Response to Finding No. 1391: Your Honor stated that Professor Teece could use the PLX Systems Survey only to the extent it helped him from his opinion on the issue of semiconductor licenses, not for its truth independently. (Teece, Tr. 10446-47). Because Rambus now cites this document for the truth of the matter asserted, the truth of the statistics presented on the slide, Complaint Counsel submits that this finding should be disregarded pursuant to this Court's July 10, 2003 Order on Post Trial Briefs.

If Your Honor does not strike this finding, then it should be given little weight. Because Professor Teece did not author the document, Complaint Counsel was denied the opportunity to cross-examine him about the methodology used to create the charts. (Teece, Tr. 10449-50). Moreover, of the over 700 agreements used in the survey, only six specifically involved DRAMs. (Teece, Tr. 10650). Indeed, You Honor stated, "I am not going to give this evidence a great deal of weight." (Teece, Tr. 10450).

In sum, Rambus has failed to establish that royalty rates negotiated between miscellaneous companies relating to an unknown number of patents covering an unknown number of technologies that perform unexplained functions in unidentified semiconductor products, that were negotiated in unexplained circumstances, and that in any event were apparently unrelated to any industry standard, has any bearing on what JEDEC members would have considered to be a

reasonable royalty rate in connection with a decision of whether to incorporate Rambus's technologies, rather than the available alternatives, into the JEDEC standards.

1392. In Rambus's 1992 business plan, Rambus recognized that its royalty rates were in line with semiconductor "traditional royalty levels of 1-5%." (CX 543A at 14).

Response to Finding No. 1392: The statement "traditional royalty levels" in Rambus's 1992 business plan is unclear. According to Mr. Tate, all of Rambus's executives offered input into the plan. (CCFF 911). However, Rambus did not call Mr. Tate, or any other senior Rambus executive, to testify about how Rambus determined the industry's "traditional royalty levels."

Furthermore, Rambus has presented as evidence that this was of any relevance to a reasonable royalty in the context of a disclosure to JEDEC. Of much greater relevance are Lester Vincent's notes of his discussion with Allen Roberts regarding the consequence of participating in JEDEC. Mr. Vincent's notes state, "would license at 1% royalty." CX1941.

1393. Based on these industry rates, as Professor Teece concluded, Rambus's royalty rates are reasonable. (Teece, Tr. 10429-51). The industry royalty rates cluster around 4 to 5%. The Rambus SDRAM royalty rate of 0.75% is low end of what comparable technologies command. (Teece, Tr. 10451). Rambus's DDR royalty rate is near the low end of the middle of comparable rates. (Teece, Tr. 10451).

Response to Finding No. 1393: The statement in RPF 1393 that based on industry rates Rambus's royalty rates are reasonable is inaccurate, misleading, contrary to the weight of the evidence, and based on unreliable evidence. *See* CCRF 1376. Indeed, Rambus's own economic expert admitted that his method of determining an average industry royalty rate was "imperfect." (Teece, Tr. 10612 (I'm trying to "give you as much information as I can find through survey research. Imperfect as it is . . . .")).

Moreover, Rambus executives did not consider external benchmarks, such as the kind Professor Teece testified about, when negotiating license agreements for technologies used in SDRAM and DDR. Rambus CEO Geoffrey Tate testified that "it's apples and oranges. The

royalty rate for one patent and the royalty rate for another patent, even in the industry, can vary tremendously based on the value of the patent and the applications involved." (Teece, Tr. 10658). Professor Teece admitted that he was not aware of this statement by Mr. Tate when he conducted his analysis and arrived at his conclusions on the reasonableness of Rambus's royalty rates. (Teece, Tr. 10658-59).

In sum, Rambus has failed to establish that royalty rates negotiated between miscellaneous companies relating to an unknown number of patents covering an unknown number of technologies that perform unexplained functions in unidentified semiconductor products, that were negotiated in unexplained circumstances, and that in any event were apparently unrelated to any industry standard, has any bearing on what JEDEC members would have considered to be a reasonable royalty rate in connection with a decision of whether to incorporate Rambus's technologies, rather than the available alternatives, into the JEDEC standards.

1394. Complaint Counsel's economic expert, on the other hand, admitted that he had no expertise in how to determine a reasonable royalty rate. (McAfee, Tr. 7737).

Response to Finding No. 1394: Professor McAfee has looked at the question of how he would determine what a reasonable royalty rate would be based on a hypothetical negotiation. (McAfee, Tr. 7737). More importantly, Professor McAfee has extensive expertise in the DRAM industry and the factors that make that industry unique.

1395. In fact, the industry rates used in this comparison underestimated actual rates because the semiconductor industry rates tend to reflect balancing payments on cross-licenses rather than rates for a straight license like Rambus's. (Teece, Tr. 10423-24). A royalty rate that is paid as a balancing payment (e.g., where two companies cross-license, the company with the smaller or weaker patents must pay the other party a balancing payment) reflects a much higher implied royalty rate for the underlying intellectual property rights. (Teece, Tr. 10424). Published royalty rates, particularly in the semiconductor industry, therefore show only the tip of the iceberg of what the royalty rates for a straight patent license would be worth in the industry. (Teece, Tr. 10424).

Response to Finding No. 1395: The proposition in RFP 1395 that the industry rates Professor Teece used in his comparison underestimated the actual rates because cross-licenses skew the royalty rates downward is incomplete and misleading. First, most of the agreements in the surveys Professor Teece relied on to calculate his average royalty rates were not cross-license

agreements. (Teece, Tr. 10647 (only 47 of the 705 agreements in the PLX survey were cross-licensing agreements)). Second, Mr. Teece's results were artificially *inflated* by his exclusion of licensing agreements with a zero percent royalty rate. (Teece, Tr. 10662-63).

In any event, Rambus has failed to establish that royalty rates negotiated between miscellaneous companies relating to an unknown number of patents covering an unknown number of technologies that perform unexplained functions in unidentified semiconductor products, that were negotiated in unexplained circumstances, and that in any event were apparently unrelated to any industry standard, has any bearing on what JEDEC members would have considered to be a reasonable royalty rate in connection with a decision of whether to incorporate Rambus's technologies, rather than the available alternatives, into the JEDEC standards.

1396. Complaint Counsel's economic expert recognized this when he admitted that companies can get economic value from internally developed patented technology because it gives the company a benefit in cross-licensing negotiations. (McAfee, Tr. 7698). For example, Micron has been able to reduce its overall royalty payments from approximately 10% to a negligible amount by increasing the number of patents it is able to include in its end of cross-licenses. (Appleton, Tr. 6299-300).

Response to Finding No. 1396: The statement in RPF 1396 that Micron has been able to reduce its overall royalty payments by increasing the number of patents it includes in its cross-licenses is incomplete, misleading, and does not support Rambus's conclusion. Rambus mischaracterizes testimony from Professor McAfee and Mr. Appleton to suggest that certain published royalty rates "show only the tip of the iceberg" of what a straight patent license would be worth. Professor McAfee simply testified that companies can gain value from internally developed technology by using it in their own operations. (McAfee, Tr. 7697). Likewise, Mr. Appleton simply testified that Micron decreased the amount of revenue it paid in royalty rates by devoting more resources to its own research and development projects. (Appleton, Tr. 6299-6300). Most fundamentally, Rambus confuses a per-patent reasonable royalty rate with a royalty rate for the

entire patent portfolio of a Fortune 500 company. Thus, Rambus establishes that Micron's patent portfolio as a whole has permitted it to reduce its royalty payments from approximately 10% to almost zero. In other words, Micron's entire patent portfolio generates the equivalent value of 10% royalties. Micron currently holds approximately 10,000 patents. Appleton, Tr. 6293-94. Thus, on a per-patent basis, each Micron patent carries an implied royalty of approximately 0.001%.

1397. Second, Rambus's royalty rates are low relative to the cost-performance of Rambus's technologies versus alternatives technologies. As discussed above, even with Rambus's royalties, the cost of Rambus's technologies is less than that of alternatives.

Response to Finding No. 1397: Complaint Counsel agrees with the basic premise that the reasonableness of a royalty for a patent must be determined with regard to the value of the specific technology at issue and whether alternatives are available, and not based on industry-wide surveys of royalty rates for unknown numbers of patents covering different technologies used in various products, the negotiation of which likely were affected by myriad specific considerations.

The statement in RPF 1397 that the cost of Rambus's technologies is less than that of alternatives lacks any reference to the record and is contrary to the weight of the evidence. (CCRF 969-988, 1125-1140). Indeed, the evidence shows that the industry thought that even Rambus's lower royalty rates for the far more extensive set of technologies in RDRAM was far too high for more interfere technologies for commanding DRAMs. RX 0855 at 1 ("0.1% royalty okay, 1-2% ridiculous"); Lee, Tr. 7047-48 (Rambus's demands for 2% royalties were "larger than anything we'd ever heard of for an interface technology and certainly the largest thing we ever heard of for some sort of fee we'd have to pay to produce main memory"); CX0952 at 2 (Intel wanted to have Rambus's long-term royalty rates for the industry as a whole at less than ½%); CCFF 1825-37, 2450-54).

1398. Third, Rambus's royalty rates for SDRAM and DDR SDRAM were agreed to in arms-length negotiations with major industry players. (Teece, Tr. 10425).

Response to Finding No. 1398: The statement in RPF 1398 that Rambus's royalty rates for SDRAM and DDR SDRAM were agreed to in arms-length negotiations with large companies is inaccurate and misleading. The fundamental issue is not whether negotiations were at arms-length, but whether negotiations occurred in the absence of monopoly power. Professor Teece did not contest the evidence that these negotiations in fact occurred after Rambus had obtained monopoly power. CCFF 2898-2985. Indeed, the license agreements themselves illustrate Rambus's use of its monopoly power. First, Rambus coerced companies into signing license agreements by threatening to unilaterally raise royalty rates. (CCFF 1983). Second, Rambus forced companies to sign license agreements by threatening to refuse to license any company that sued Rambus. (CCFF 1992-94). Finally,

(CCFF 1989).

1399.

(Teece, Tr. 10534 (*in camera*)).

Response to Finding No. 1399: Complaint Counsel agrees that Rambus's RDRAM licenses incorporated an entire memory interface and bus architecture, whereas its SDRAM and DDR SDRAM licenses incorporated only a small number of teachnologies that formed a very small part of the memory interface. Thus, one would expect the license rates for RDRAM to be higher than those for DDR SDRAM. The evidence also overwhelmingly shows that members of the DRAM industry believed Rambus's RDRAM royalty rates, , were extremely high. (CCFF 1816-22). JEDEC members viewed royalty rates of between 0.1% and 0.5% as reasonable. RX 0855 ("0.1% okay" 1; CX0952 (less than ½%); *see also* CX1941 ("would license at 1% royalty").

1400. First,

(Teece, Tr. 10534-35 (*in camera*); MacWilliams, Tr. 4824-25).

Response to Finding No. 1400: The statement in RPF 1400 that

is contrary to the weight of the evidence. First, Rambus does not define the vague term Second, the evidence shows that Rambus took advantage of its relationship with Intel to charge even higher royalty rates than it otherwise could have obtained. (CCFF 1829). Indeed, the evidence overwhelmingly shows that members of the DRAM industry believed Rambus's RDRAM royalty rates, , were extremely high. (CCFF 1816-22). Third,

(McAfee, Tr. 7863-64, *in camera*).

1401. Second,

(Teece, Tr. 10535 (*in camera*)).

Response to Finding No. 1401: RDRAM license agreements were not comparable to joint ventures because companies paid separately for Rambus's technical services. (CX1646 at 10 (Micron's RDRAM license agreement included a $3 million dollar "engineering fee"); CX1609 at 10 (Mitsubishi's RDRAM license agreement included a $3.5 million dollar "engineering fee"); CX1617 at 11 (Siemens's RDRAM license agreement included a $4 million dollar "engineering fee").

1402.

(Teece, Tr. 10535-36 (*in camera*)). Rambus was able to "participate in future design improvements," obtain information about the partner's customers, and be "part of the process going forward." (Farmwald, Tr. 8179-80).

Response to Finding No. 1402: The identical consideration would have applied to Rambus seeking to persuade JEDEC members to incorporated Rambus's technologies rather than

competing technologies into the JEDEC standards, so that it could then be part of the process in setting future JEDEC standards.

1403. Rambus's RDRAM licenses form a partnership; Rambus works with the licensee, and receives valuable feedback and information. (Farmwald, Tr. 8241). For non-DDR by contrast, there is no partnership, and Rambus receives no additional benefits. (Farmwald, Tr. 8241).

(Teece, Tr. 10535 (*in camera*)).

Response to Finding No. 1403: *See* CCRF 1402.

1404. Complaint Counsel's economic expert admitted that although Rambus's RDRAM licenses have benefits to Rambus that its DDR licenses do not, he did not quantify those benefits when comparing the DDR and RDRAM license rates. (McAfee, Tr. 7835).

Response to Finding No. 1404: The statement in RPF 1404 that Professor McAfee did not quantify possible benefits Rambus received from RDRAM licenses is misleading and incomplete. Professor McAfee testified that

(McAfee, Tr. 7863-64, *in camera*).

B. Rambus's Licenses Are Not Discriminatory.

1405. Rambus's licenses are non-discriminatory.

Response to Finding No. 1405: RPF 1405 lacks any reference to the record, constitutes legal argument and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Moreover, the statement in RFP 1405 that Rambus's licenses are non-discriminatory is inaccurate. Complaint Counsel has shown that Rambus's licenses are discriminatory for several reasons. First,

(CCFF 2000, 2978, McAfee, Tr. 7634-36, *in camera*). Second,

(CCFF 2018). Third, Rambus plans to charge companies that chose to litigate higher royalty rates. (CCFF 1990, 2037, 2980). Most importantly, Rambus had a strategy that it might not license at all to companies that chose to litigate against Rambus and lost. (CCFF 1992-93, 2980-81).

(Teece, Tr. 10567, *in camera* (

)).

Indeed, a major reason Rambus refused to agree to RAND terms was so that it would preserve its ability to charge discriminatory royalties. (CX1405 at 235 (Vincent, Dep.) ("Q: What was it about the terms of Rambus's standard license agreement that was not consistent or may not be consistent where the JEDEC policy? A: . . . Rambus would not be under an obligation to license somebody if they didn't want to."); CCFF 1091, 1535-39).

1. <u>JEDEC Has Left the Definition of "Non-Discriminatory" to the Market and the Courts</u>.

1406. As Mr. Rhoden testified, JEDEC takes no position on the definition of questions regarding "non-discriminatory." (Rhoden, Tr. 665). Rather, JEDEC leaves the determination of what terms are nondiscriminatory to the market and, if that fails, to the courts. (Kelly, Tr. 1882-83).

<u>Response to Finding No. 1406</u>: While JEDEC does not take a position on the discriminatory nature of individual royalty rates, it does require that members abide by JEDEC rules. (RX-1461 at 1 (when Mosaid asked Mr. Townsend to interpret the term "non-discriminatory," Townsend relied, "JEDEC is only interested in the broader picture that you abide by the bylaws.")). JEDEC's rules, as set forth clearly in the EIA Legal Guides, demand that members act in good faith. (CCFF 310-312).

1407. For instance, when Dick Foss of Mosaid wrote to JEDEC to ask whether the RAND requirement means that Mosaid had to license its DLL patent on the same terms to licensees currently under a broad patent license from Mosaid as to those who just licensed the DLL technology, Mr. Townsend responded that the details of the license terms were left to Mosaid's negotiations with individual companies. (RX 1461 at 1-2). Desi Rhoden also replied that the interpretation of RAND is left to the courts. (RX 1461 at 1).

Response to Finding No. 1407: While JEDEC does not take a position on the discriminatory nature of individual royalty rates, it does demand that members abide by JEDEC's rules and regulations. The situation Rambus cites in this finding illustrates this point. In 1999, Mosaid told Jim Townsend that it would conform to the JEDEC policy by offering "non-discriminate licensing at 'reasonable rates.'" When Mosaid's representative asked Mr. Townsend to interpret JEDEC's RAND policy, and specifically the term "non-discriminatory," Mr. Townsend replied that JEDEC does not comment on individual negotiations and "is only interested in the broader picture that you abide by the bylaws." (RX1461 at 1). JEDEC's rules, as set forth clearly in the EIA Legal Guides, demand that members act in good faith. (CCFF 310-312).

1408. Similarly, JEDEC did not object when Mosaid indicated that there would be differences in its licenses for its DLL patent depending on whether the licensee licensed only the DLL patent or multiple patents from Mosa*id.* In May 1999, Dick Foss wrote to JEDEC stating, "There is inevitably a difference between someone who gets a DLL license thrown in as part of a multi-million settlement on multiple patents and someone who just wants a license for DLL usage." (CX 400 at 2). He also wrote, "There will be differences in terms if company 'a' is a general licensee (and is automatically licensed anyway) and company 'b' is not and so will be expected to take a 'reasonable' license if wanting to use our IP on the item." (CX 400 at 1). Jim Townsend responded that he would presume that this arrangement was acceptable, though he thought Mosaid should ask counsel. (CX 400 at 1). Joe Macri did not recall any objection to Mosaid's two tiered licenses and never raised the issue with Dick Foss. (Macri, Tr. 4714-16; RX 1457).

Response to Finding No. 1408: The statement in RPF 1408 that Mr. Townsend told Mosaid that he presumed their licensing arrangement was acceptable is incomplete. Mr. Townsend stated that he presumed the arrangement was reasonable "based on demonstrable differences in value added; and that within each tier all licensees are offered in a non-discriminatory way." (CX0400 at 1). *See also* CCRF 1406.

1409. Robert Goodman of Kentron testified that he understood that a nondiscriminatory rate should be measured at a particular point in time; at different points in time, charging different rates is not discriminatory if there is some reason to charge a different rate. (Goodman, Tr. 6088).

Response to Finding No. 1409:

(McAfee, Tr. 7861, *in camera*).

1410. JEDEC has also indicated that whether a patentee can charge a higher rate for a party that chooses to litigate rather than license is left to the market and the courts. In a September 6, 2001 letter from Christopher Pickett, General Counsel of Tessera, Inc., to John Kelley, EIA's President and General Counsel, Mr. Pickett recounted his discussion with Mr. Kelley to the effect that either the parties or the courts must resolve whether JEDEC's RAND policy allowed Tessera to charge a higher rate to litigating parties: "As we discussed on the phone and as is set forth in your letters, this JEDEC policy is intentionally broad in order to allow the parties to negotiate terms and come to their own decision on what the words mean in the particular circumstances. The JEDEC patent policy does not negate the context of what is commercially reasonable in determining license terms with a particular licensee. Whether a patent owner may consider a company's adverse action in negotiating licensing terms is a matter that must be resolved, in the first instance, by the negotiating parties themselves. If the parties cannot reach agreement, they may submit the question to the courts for resolution." (RX 1885 at 1).

Response to Finding No. 1410: The letter from Mr. Pickett to John Kelly that Rambus cites in RPF 1410 is unreliable for several reasons. First, although Rambus tries to cast Mr. Pickett's language as JEDEC policy, the letter is not from JEDEC and does not reflect Mr. Kelly's understanding of the patent policy. Mr. Pickett is not a JEDEC participant and the record contains no evidence that he ever attended a JEDEC meeting. Other evidence shows that Mr. Kelly believed a patent owner would be violating the non-discrimination provision of the JEDEC patent policy if it refused to license a company that had taken adverse action against the patent holder. (J. Kelly, Tr. 1873, 1883-84). Rambus did not ask Mr. Kelly, who testified for two whole days, whether Mr. Pickett's letter accurately reflected JEDEC policy. Mr. Pickett is not a JEDEC participant and the record contains no evidence that he ever attended a JEDEC meeting.

2. Rambus's Licenses are Non-Discriminatory.

1411.

(Teece, Tr. 10538 (*in camera*)).

Response to Finding No. 1411: Complaint Counsel agrees that

The statement in RPF 1411 that a

is irrelevant and misleading.

(McAfee, Tr. 7861, *in camera*).

1412. Rambus offered its SDRAM and DDR licenses to everybody on more or less the same terms. (Farmwald, Tr. 8242).

Response to Finding No. 1412: The statement in RPF 1412 that Rambus offered its SDRAM and DDR licenses to everybody on more or less the same terms is inaccurate for several reasons. First, Mr. Farmwald was not involved in Rambus's licensing negotiations for SDRAM and DDR. Second,

(CCFF 2000) (

).

(CCFF 2018, McAfee, Tr. 7855, *in camera*).

(Appleton, Tr. 6390

(Rambus offered Micron 1.0% royalty on SDRAM compared to .75% offered to other companies)).

1413. Complaint Counsel contend that Rambus's DDR license rates are discriminatory because Rambus charges a higher rate to Hitachi, which is the only licensee that litigated with Rambus before signing a license.

Response to Finding No. 1413: RPF 1413 lacks any reference to the record, constitutes legal argument and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Moreover, the statement in RPF 1413 that "Complaint Counsel contend that Rambus's DDR rates are discriminatory because Rambus charges a higher rate to " is incomplete. Complaint Counsel has shown that Rambus's DDR license rates are discriminatory for several reasons, only one of which is the fact that Rambus charges a higher up front licensing fee and higher royalty rate compared to the fees paid by other DRAM manufacturers. (CCFF 2000, 2978). Rambus's rates are also discriminatory because

(CCFF 2018). In addition, Rambus plans to charge companies that chose to litigate higher royalty rates. (CCFF 1990, 2037, 2980). Most importantly, Rambus had a strategy that it might not license at all to companies that chose to litigate against Rambus and lost. (CCFF 1992-94, 2980-81).

(Teece, Tr. 10567, *in camera* (

)).

1414. In fact, however, before litigation, Rambus offered Hitachi a license on essentially the same terms it offered to others. (CX 2059, Karp Depo. at 251). Complaint Counsel's economic expert understood that in 2000, Rambus was prepared to offer a license for DDR to any interested company at 3.5%. (McAfee, Tr. 7845). He therefore admitted that, in the economic sense of nondiscriminatory, Rambus was prepared to offer nondiscriminatory licenses. (McAfee, Tr. 7848).

Response to Finding No. 1414: Because Rambus cites to *in camera* evidence in RPF 1414 without properly identifying it as *in camera*, Complaint Counsel submits that this finding should be disregarded pursuant to 16 C.F.R. § 3.45(e) and this Court's July 10, 2003 Order on Post Trial Briefs.

Moreover, the statement in RPF 1414 that Rambus offered Hitachi a license on essentially the same terms as it offered to others is unsupported by record evidence. First, the page Rambus cites from Mr. Karp's deposition does not support the proposition that "Rambus offered Hitachi a license on essentially the same terms it offered to others." Mr. Karp later testified that Rambus offered Hitachi a license, but did not specify the terms of the proposed agreement. Karp did speculate that Hitachi could have obtained the same deal as other companies, but commented, "It's all hypothetical, of course." (CX2059, Karp Dep. at 252). Second, Rambus can not cite to Professor McAfee for the proposition that "Rambus was prepared to offer DDR to any interested company at " because Professor McAfee is not a fact witness and has no actual knowledge of the royalty rates Rambus offered to charge companies. Finally, the record contains no proof that Rambus actually offered Hitachi the same terms as other companies.

1415. Higher royalties for litigating parties are not discriminatory in an economic sense for a number of reasons. First,
(Teece, Tr. 10541 (*in camera*)). Second,
(Teece, Tr. 10541 (*in camera*)).

Response to Finding No. 1415: The statement in RPF 1415 that litigation costs justify charging litigating parties higher royalties is inaccurate and contrary to Professor Teece's own testimony. (CCFF 2982; Teece, Tr. 10556-58, *in camera*).

(Teece, Tr. 10556, *in camera*).

(Teece, Tr. 10552, *in camera*).

1416. Third,

(Teece, Tr. 10540 (*in camera*)). In other words, the fact that Rambus charged a higher rate after litigation may be justified by changed perceptions regarding the strength of the patents.

Response to Finding No. 1416: Rambus's theoretical assertion that patents increase in value following litigation is inapplicable here and is contradicted by the actual behavior of the parties in this case. First,

(Teece, Tr. 10561-62, *in camera*). Second,

(CCFF 1999, 2005-2011).

1417. Fourth,

(Teece, Tr. 10542 (*in camera*)). This creates

(Teece, Tr. 10542-43 (*in camera*)).

Response to Finding No. 1417: Regardless of the reason, price discrimination proves a firm has market power. As Professor McAfee testified,

(McAfee, Tr. 7636, *in camera*).

1418.

(Teece, Tr. 10542, 10551 (*in camera*)).

Response to Finding No. 1418: The statement in RPF 1418 that

(CCFF 2982; Teece, Tr. 10556-58, *in camera*).

(Teece, Tr. 10556, *in camera*).

1419. Complaint Counsel's economic expert did not challenge this point. Rather he used an analysis based on production costs to conclude that Rambus's DDR royalty rate to Hitachi was discriminatory. (McAfee, Tr. 7827). But for purposes of determining whether patent licenses are discriminatory,

(Teece, Tr. 10545 (*in camera*)).

Response to Finding No. 1419: *See* CCRF 1420.

1420. Moreover, Complaint Counsel's economic expert effectively admitted that litigation imposes costs on Rambus and that it is economically rational to develop a strategy to avoid those costs. (McAfee, Tr. 7829). He went on to admit that it would be consistent with economic theory to charge a higher royalty rate to licensees that require the patent holder to incur costs before taking a license. (McAfee, Tr. 7829). Further, he recognized that Hitachi's litigation with Rambus imposed risks on Rambus (McAfee, Tr. 7830), and that a licensing strategy of charging more to companies that choose to litigate would maximize Rambus's profits by reducing its future costs. (McAfee, Tr. 7831).

Response to Finding No. 1420: Rambus's characterization of Professor McAfee's testimony is incomplete because it omits Professor McAfee's testimony that Rambus's licensing practices are discriminatory. Professor McAfee testified that

(CCFF 2979, McAfee, Tr. 7633-36, *in camera* (

).

1421. Complaint Counsel's economic expert did not make any assumption as to whether charging a higher rate to companies that choose to litigate violates the JEDEC nondiscrimination policy. (McAfee, Tr. 7832).

Response to Finding No. 1421: Although Professor McAfee did not attempt to interpret JEDEC policies, he did testify that charging a company that chooses to litigate a higher royalty rate is discriminatory. (McAfee, Tr. 7832, 7635-37, *in camera*; CCFF 2978).

1422. Therefore,

(Teece, Tr. 10537-38, 10545-46 (*in camera*)). For the same reasons,

(Teece, Tr. 10547 (*in camera*)).

Response to Finding No. 1422: RPF 1422 constitutes legal argument and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Moreover, Rambus's assertions in RPF 1422 are unconvincing and contrary to the weight of the evidence. First, the weight of the evidence shows that Rambus was not willing to offer companies that chose to litigate licenses on the same terms as other companies. (CCFF 2014-32). Second, Rambus's assertion that it is justified in charging higher royalty rates to parties that chose to litigate is not justified by litigation costs. Rambus charged Hitachi higher rates even though the actual cost of litigation was minimal compared to the increased royalty rate. (CCFF 2982). Finally, Rambus's own argument demonstrates that is has monopoly power. As Rambus's co-founder Mike Farmwald testified, the real reason Rambus charged Hitachi a higher royalty rate was to penalize Hitachi for "fighting." (Farmwald, Tr. 8242 (Hitachi paid a higher royalty rate "as sort of a penalty for fighting basically.")). The ability to punish parties by charging discriminatory rates shows that Rambus has market power. (CCFF 2979, 2982).

XII. THE ECONOMIC IMPLICATIONS OF THE EVIDENCE.

1423. Assuming, contrary to the facts, that: (1) JEDEC rules obligated Rambus to disclose information about its patent interests; (2) Rambus failed to disclose information to JEDEC that these rules required be disclosed; and (3) JEDEC members were misled by this alleged conduct on the part of Rambus, the evidence still shows that the alleged conduct did not harm competition.

Response to Finding No. 1423: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1424. First, the facts show that Rambus's alleged conduct was not "exclusionary" as that term is used in economics. Conduct that is not exclusionary, though it may be disliked by or even harmful to competitors, is not anticompetitive.

Response to Finding No. 1424: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1425. Second, the facts show that Rambus's alleged conduct did not increase or add to its market power.

Response to Finding No. 1425: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

A. Rambus's Alleged Failure to Disclose Was Not Exclusionary.

1426. Complaint Counsel contend that Rambus's alleged conduct was "exclusionary." As explained below, this contention fails for a number of reasons.

Response to Finding No. 1426: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1. The Alleged Conduct Was Not Exclusionary Because There Is a Valid Business Justification For Not Disclosing Information About Patent Applications.

1427. Exclusionary conduct can be characterized as an investment in the destruction of a rival. It is defined in economics by a two-part test. (Rapp, Tr. 9909-11). First, the conduct must consist of short-run actions that do not make sense except in terms of their adverse impact on competition. (Rapp, Tr. 9911). That is, the actions cannot have an independent business justification. (Rapp, Tr. 9911). Second, after competition is excluded or weakened, the conduct must be likely to lead to recoupment through the exercise of market or monopoly power that would not exist but for the conduct. (Rapp, Tr. 9911).

Response to Finding No. 1427: Complaint Counsel does not disagree that this proposed finding describes Dr. Rapp's characterization of exclusionary conduct.

1428. An example of exclusionary conduct is pricing below average variable cost. (Rapp, Tr. 9911-12). In that example, the conduct leads to greater losses every time another sale is made. (Rapp, Tr. 9912). There is therefore no business justification for pricing below average variable cost. (Rapp, Tr. 9912).

Response to Finding No. 1428: Complaint Counsel does not disagree.

1429. An example of conduct that might have an adverse effect on competitors but is not exclusionary is pricing below total cost but above variable cost, such conduct might reduce margins but does not increase losses with every transaction. (Rapp, Tr. 9912). There are good business reasons for this type of pricing. (Rapp, Tr. 9912). Thus, even though pricing below total cost might hurt competitors, especially if they are less efficient, it benefits consumers and is not exclusionary. (Rapp, Tr. 9912-13).

Response to Finding No. 1429: Complaint Counsel does not disagree that there may be valid business reasons for the type of pricing described and so it might not be exclusionary.

1430. An example of conduct involving intellectual property that is not exclusionary even though it adversely affects competitors is where a firm develops a cost-saving technology, protects the technology through trade secrets or patents, and drives its rivals out of business by being the low cost competitor. (Rapp, Tr. 9913). There is nothing exclusionary about this conduct even though, in the normal sense of the word, competitors are excluded. (Rapp, Tr. 9913-14).

Response to Finding No. 1430: Complaint Counsel does not disagree.

1431. Even conduct that may violate an extrinsic duty, and is therefore illegal or unethical, is not necessarily exclusionary even if that conduct affects competition. For instance, Complaint Counsel's economic expert admitted that a misrepresentation, even if it has an impact on competition, is not always exclusionary. (McAfee, Tr. 7535-36).

Response to Finding No. 1431: This proposed finding is vague because the phrases "affects competition" and "impacts competition" are undefined. Depending on the meaning of these phrases this proposed finding may be misleading.

Furthermore, this proposed finding is incomplete because it omits testimony from Professor McAfee that exclusionary behavior in the economic sense is behavior that eliminates equal or superior competitors and that has no efficiency rationale. (CCFF 2896-2898). Professor McAfee testified that one type of exclusionary behavior that has been alleged in this case is that Rambus provided false or misleading information to JEDEC. (CCFF 2989). This type of behavior can be exclusionary because it prevents competition on the merits and, in this case could have distorted the JEDEC standardization process. (CCFF 2990-2991, 3003). Professor McAfee testified that a second type of exclusionary behavior that has been alleged in this case is that Rambus made an intentional decision to jeopardize the enforceability of its patents in the hopes of being able to gain the ability to monopolize the relevant markets. (CCFF 3006-3009).

1432. Even if conduct excludes superior alternatives, excludes commercially viable alternatives, raises the perceived relative cost of alternatives, and adversely affects competition, these fact alone are not sufficient to define exclusionary conduct in an economic sense. (Rapp, Tr. 9927-28). Each of these is an effect of conduct rather than a characterization of conduct and is therefore insufficient itself, or together with the others, to define exclusionary conduct. (Rapp, Tr. 9927-28).

Response to Finding No. 1432: This proposed finding is incomplete because it omits testimony by Dr. Rapp that these facts alone are not "sufficient to define exclusionary or predatory conduct" in an economic sense because this is an analysis based solely on the result of the conduct and not on a characterization of the conduct itself. (Rapp, Tr. 9928 ("They're all result-related. The way that antitrust economics goes about analyzing predation or exclusion is by means of assessing the conduct, and if you take those four together – I have to – either three of the four or all four of them speak to the outcome, so there is a circularity about them that disqualifies

them as an adequate test by themselves for predation or exclusion.")). Professor McAfee identified two types of conduct that qualify as exclusionary conduct in an economic sense. (CCRF 1431).

1433. Incurring risk does not make conduct exclusionary. (Rapp, Tr. 9930-31). Businesses take risks all the time, most often to achieve some sort of gain. (Rapp, Tr. 9931). Conduct cannot be deemed exclusionary on the ground that it entails risks without assessing the possible gains from the conduct. (Rapp, Tr. 9931). Thus, the fact that risk was taken says nothing about whether conduct is exclusionary. (Rapp, Tr. 9931).

Response to Finding No. 1433: This proposed finding is incomplete because Dr. Rapp testified that one essential element for determining whether conduct is exclusionary is whether the firm "invests" in obtaining monopoly power. (Rapp, Tr. 9910-9911 ("it is the key off the word 'investment.' If you think about the way investment works, you disgorge a certain amount of money up front and then you have to wait until the investment pays off, and that is in the nature of predation or exclusion as well.")).

Furthermore, Professor McAfee testified that part of the reason that Rambus's willingness to risk equitable estoppel was exclusionary was because it constituted an investment in monopolizing the relevant markets. (McAfee, Tr. 7502-7503 ("So that is to say, the future gains, the recoupment of the investment in monopolizing the market by way of running losses currently makes up for the losses in the near term. And so if you succeed in monopolizing a market, that actually provides a rational account of why a firm might engage in predatory pricing. And there's an exact parallel here. The risk, which is a very serious risk, of having your patents found unenforceable might be compensated by the gain associated with actually ultimately monopolizing the markets.")).

1434. Rather, if there is a valid efficiency rationale for conduct, it is not exclusionary. (Rapp, Tr. 9914). In examining Rambus's conduct in this case, therefore, part of the economic test is to determine whether there exists a valid business justification for the alleged conduct. (Rapp, Tr. 9914).

Response to Finding No. 1434: Complaint Counsel does not disagree with the statement in this proposed finding that part of the economic test is to determine whether there exists a valid business justification for the alleged conduct.

1435. From an economic perspective, the protection of trade secrets is a valid business justification for not disclosing information regarding pending patent applications as well as for not disclosing intentions to file applications in the future (including intentions about amending pending claims). (Rapp, Tr. 9915-16).

Response to Finding No. 1435: This proposed finding is misleading because it implies that the business justification of "protection of trade secrets" was a motivation for the behavior at issue in this case. Dr. Rapp could not point to any specific evidence that he has seen that during the time Rambus was a member of JEDEC that anybody at Rambus actually had that concern. (Rapp, Tr. 10167). Furthermore, the proposed finding cites no evidence that this potential business justification was a motivation for the behavior at issue in this case.

Furthermore, this proposed finding ignores substantial record evidence that Rambus deliberately decided not to disclose its relevant intellectual property so that JEDEC members would not have the opportunity to design around that intellectual property. CX0783 at 2 (Crisp e-mail, 2/26/95: "I certainly do not want to bring this intellectual property issue up without careful consideration. I especially do not want it all over JEDEC."); CX0711 at 68, 73 (Crisp e-mail, 5/24/95: "[I]t makes no sense to alert them to a potential [patent] problem they can easily work around."); CX1277A at 1, 2 (Presentation, 3/96: "200Mhz SDRAM Myth:" "Challenges (do not tell them :-)"); CX0919 (Tate e-mail, 2/10/97: "do NOT tell customers/partners that we feel DDR may infringe – our leverage is better to wait"); CX0942 (Tate e-mail, 8/4/97: "our policy so far has been NOT to publicize our patents and i think we should continue with this"); CX0960 (Tate e-mail, 10/1/97: "when joel [karp] starts we need to have our spin control ready for partners/etc as to why we are hiring him and what he will be doing."); CX0987 at 4 (Tate e-mail, 1/19/98: "ddr

infringes our patents (question: when do we start saying this publicly?)"); CX1089 (Tate e-mail, 12/9/99: "it's important NOT to indicate/hint/wink/etc what we expect the results of our infringement analysis to be!!!").

1436. There is a valid business justification for not disclosing such information because: (1) disclosure may jeopardize the issuance of pending claims by enabling competitors to file patent interferences or to race to be first-to-file in certain foreign jurisdictions; and (2) disclosure may result in a loss of competitive advantage by informing competitors of the firm's R&D focus or by inducing competitors to begin work around efforts earlier. (Rapp, Tr. 9916-18).

Response to Finding No. 1436: This proposed finding is misleading for the reasons described in CCRF 1435. (Rapp, Tr. 10170).

1437. These business justifications apply to pending applications and intentions to file or amend future applications, even after a parent patent application becomes public. (Rapp, Tr. 9926). Thus, in Rambus's situation, even after the '898 application had been disclosed (in the form of the PCT application), Rambus still had trade secrets (additional pending applications and intentions to file additional applications) that it could legitimately protect from disclosure. (Rapp, Tr. 9926).

Response to Finding No. 1437: This proposed finding is misleading for the reasons described in CCRF 1435. (Rapp, Tr. 10176-10177).

1438. Not only is not disclosing information about pending or future patent applications rational and profit maximizing for the firm, it is procompetitive for the same reasons that preserving trade secrets is procompetitive. (Rapp, Tr. 9918). This type of nondisclosure preserves incentives to innovate because innovation depends on the ability to control intellectual property. (Rapp, Tr. 9918-19). It thus enhances consumer welfare by leading to better competitors, which leads to enhanced competition, increased output, and lower prices. (Rapp, Tr. 9918).

Response to Finding No. 1438: This proposed finding is misleading for the reasons described in CCRF 1435.

1439. Similarly, exercising intellectual property rights to exclude competitors and protecting trade secrets from use by other companies are not exclusionary conduct. (Rapp, Tr. 9229-30). Nor is exercising intellectual property rights to charge royalties that might raise a rival's costs is not exclusionary conduct. (Rapp, Tr. 9229). To the contrary, all of these actions may be procompetitive. (Rapp, Tr. 9929-30).

Response to Finding No. 1439: This proposed finding is misleading for the reasons described in CCRF 1435.

1440. These conclusions apply in the standard-setting context as in any other. A company that is the member of a standard-setting body may benefit from not disclosing information regarding its pending patent applications or its intentions to file future patent applications regardless what standards are developed. (Rapp, Tr. 9919-20). The benefits to a company keeping control of its business and intellectual property strategies do not depend on which standard is chosen by the standard-setting body. (Rapp, Tr. 9919-20). These benefits have to do with maximizing the ability to operate competitively, not standardization. (Rapp, Tr. 9920).

Response to Finding No. 1440: This proposed finding is misleading for the reasons described in CCRF 1435.

1441. From the standpoint of antitrust economics, if Rambus had failed to disclose information to JEDEC about its pending or future patent applications, its conduct would not have been exclusionary because there was a legitimate business justification for such nondisclosure. (Rapp, Tr. 9921). Keeping that information confidential did *not* impose on Rambus costs or risks that were compensable only by excluding rivals and thereby gaining market power. (Rapp, Tr. 9924).

Response to Finding No. 1441: This proposed finding is misleading for the reasons described in CCRF 1435.

Furthermore, the statement in this proposed finding that "if Rambus had failed to disclose information to JEDEC about its pending or future patent applications, its conduct would not have been exclusionary because there was a legitimate business justification for such nondisclosure" is incomplete because it omits that the testimony was provided in response to a question that requested that Dr. Rapp "[set] aside whatever JEDEC or other groups might do in response to that failure to disclose...." Consequently, this proposed finding omits that this testimony does not take into account that JEDEC might adopt standards using technology that Rambus claims to own in response to Rambus's failure to disclose.

Furthermore, the statement in this proposed finding that "[k]eeping that information confidential did *not* impose on Rambus costs or risks that were compensable only by excluding rivals and thereby gaining market power" is unreliable because it is based on testimony by Dr. Rapp that he could not identify any risk that Rambus took in not disclosing its intellectual property.

(Rapp, Tr. 9924 ("I was unable to find evidence that Rambus expended costs or took risks that were -- that were only compensable by the exclusion of another technology , that, in other words, did not have a proper business justification. And my finding was that no such risks were borne.")). However, there is substantial evidence in the record that Rambus employees, including Rambus's JEDEC representative, Richard Crisp, were aware of the potential equitable estoppel risk of Rambus's behavior at JEDEC. (CCFF 422, 821, 849-852, 889-891, 956-957, 1056-1061, 1083-1090).

1442. Rambus's economic expert, Dr. Rapp, testified that Rambus's alleged conduct was not exclusionary in an economic sense. (Rapp, Tr. 9921). Dr. Rapp is well qualified to give this type of economic opinion. He holds a bachelor's degree in economics from Brooklyn College in 1965, a master's degree in economic history from the University of Pennsylvania in 1966, and a Ph.D. in economic history from the University of Pennsylvania in 1970. (Rapp, Tr. 9766). He is the president of NERA, which is an economics consulting firm with 500 employees that specializes in the economics of competition, including industrial economics, antitrust, intellectual property. (Rapp, Tr. 9764). He has been an economic consultant with NERA since 1977 and the president of NERA since 1988. (Rapp, Tr. 9764). Prior to his joining NERA, Dr. Rapp was a tenured professor at the State University of New York at Stony Brook. (Rapp, Tr. 9766).

Response to Finding No. 1442: Complaint Counsel does not disagree that "Dr. Rapp, testified that Rambus's alleged conduct was not exclusionary in an economic sense." The statement in this proposed finding that "Dr. Rapp is well qualified to give this type of economic opinion," lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

This proposed finding si also misleading because it does not reflect that Dr. Rapp failed to consider critical evidence in this case. Dr. Rapp reviewed no Rambus business records other than Toshiba license agreement and a license term synopsis prepared by his staff. (Rapp, Tr. 9991; *see* DX0324). Dr. Rapp reviewed no third-party business records. (Rapp, Tr. 9992; *see* DX0324). Dr.

Rapp reviewed no deposition testimony. (Rapp, Tr. 9993; *see* DX0324). Dr. Rapp reviewed no JEDEC materials/minutes other than two technical specifications. (Rapp, Tr. 9994; *see* DX0324). Dr. Rapp reviewed no notes/reports on JEDEC activities. (Rapp, Tr. 9995; *see* DX0324). Dr. Rapp reviewed none of the Rambus / JEDEC / third-party records cited in McAfee's report. (Rapp, Tr. 9999; *see* DX0324).

1443. In addition, Dr. Rapp has published articles on predatory pricing, intellectual property economics, and innovation in high-technology markets. (Rapp, Tr. 9768-69). In the past 15 years, a great deal of his consulting work has been in the area of high-technology antitrust and intellectual property, typically in the computer and semiconductor industries. (Rapp, Tr. 9769-70).

Response to Finding No. 1443: Complaint Counsel does not disagree. However, this proposed finding does not support the conclusion that Dr. Rapp is well qualified to give this type of economic opinion for the reasons set forth in CCRF 1442.

1444. Dr. Rapp has been qualified as an expert on numerous occasions. Since the early 1980's, Dr. Rapp has testified in hearing or trials as an antitrust economics expert, on average, about once per year. (Rapp, Tr. 9771). He has testified at least five times as an expert on the economic aspects of intellectual property issues. (Rapp, Tr. 9771-72).

Response to Finding No. 1444: Complaint Counsel does not disagree. However, this proposed finding does not support the conclusion that Dr. Rapp is well qualified to give this type of economic opinion for the reasons set forth in CCRF 1442.

1445. Although he did not explicitly acknowledge that a decision not to disclose information regarding pending patent applications would not be exclusionary in the presence of valid business justifications, Complaint Counsel's expert conceded the underlying rationale for this conclusion.

Response to Finding No. 1445: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

To the extent that this proposed finding implies that Professor McAfee testified that the presence of valid efficiency justifications means that it is unlikely that the behavior in question is exclusionary, Complaint Counsel does not disagree. (McAfee, Tr. 7477 ("[T]the purpose of defining exclusionary conduct to be the exclusion of superior competitors or products is to ensure that exclusionary conduct is bad for the functioning of marketplaces and hence does not have a valid efficiency rationale."); *see* DX0229). However, Professor McAfee also concluded that if a number of factual assumptions are valid, then, on economic grounds, he was able to conclude that Rambus's conduct was exclusionary. (CCFF 2992-2996, 3006-3009).

1446. Complaint Counsel's economic expert did not criticize or rebut Dr. Rapp's opinion that Rambus's conduct was not exclusionary because of the presence of a legitimate business justification. To the contrary, he admitted that concealing information, even if it discourages competitors from entering a market, is not exclusionary. (McAfee, Tr. 7525-27). Complaint Counsel's economic expert also admitted that it is not exclusionary to conceal an invention from competitors in order to take advantage of the invention while others cannot. (McAfee, Tr. 7527-28).

Response to Finding No. 1446: This proposed finding is misleading because it implies that Professor McAfee agreed with Dr. Rapp that there were valid efficiency rationales for Rambus's conduct at JEDEC. However, while Professor McAfee agreed that the presence of valid efficiency rationales could mean that conduct is not exclusionary, he further testified that, if the facts turn out as Complaint Counsel allege, then Rambus's conduct was exclusionary. (CCFF 2986-3011).

Furthermore, the statement in this proposed finding that Professor McAfee "admitted that concealing information, even if it discourages competitors from entering a market, is not exclusionary," is incomplete and misleading. This statement is incomplete because it omits testimony from Professor McAfee that he only agreed that a company that is concealing the extent of its *profitability* is not behaving in an exclusionary manner. (McAfee, Tr. 7526 ("A. That a company doesn't disclose the profits that they make?... [that is] not exclusionary.")). This

statement is misleading because it implies that Professor McAfee agreed, in a general sense, that concealing information cannot be exclusionary even if it discourages competitors from entering a market. Professor McAfee made clear in his direct testimony that providing false or misleading information can be exclusionary. (CCFF 2989-2991).

Furthermore, the statement in this proposed finding that Professor McAfee "admitted that it is not exclusionary to conceal an invention from competitors in order to take advantage of the invention while others cannot," is incomplete and misleading. This statement is incomplete because it omits testimony from Professor McAfee that he only agreed that it is not exclusionary for a company to conceal an innovation that would allow it to produce products at a lower cost than its competitors, where there was no mention of any duty to disclose in the hypothetical. (McAfee, Tr. 7527-7528 ("Q. And let's further assume that that company would like to build a factory to employ that process and not let anybody know that it has a new factory using a cheaper process until they actually start producing product. Can we add that to the assumption? A. So just to make sure I'm clear, the hypothesis is they've invented what's known as a process innovation and it lowers their cost of manufacturing and they haven't told anybody about the process innovation because they want to wait until they've actually built the factory. Q. Yes...."). This statement is misleading because it implies that Professor McAfee agreed that in a general sense concealing an innovation from competitors cannot be exclusionary. Professor McAfee made clear in his direct testimony that providing false or misleading information regarding an innovation can be exclusionary in some circumstances. (CCFF 2992-2996, 3002-3004).

1447. Yet Complaint Counsel's economic expert admitted that the only "candidate purpose" he considered for Rambus's withholding information about its patent applications was monopolization, i.e., he did not consider other purposes that might have led Rambus to take the risk that he identified. (McAfee, Tr. 7539). In other words, he did not consider whether Rambus did not disclose information about its patent applications for a valid reason.

Response to Finding No. 1447: This proposed finding is inaccurate because Professor McAfee testified that he did consider other potential purposes for Rambus's behavior. (McAfee, Tr. 7539 ("Q. Okay. Did you consider other purposes that might lead someone to take such a risk? A. I d*id.* But the reason for my phrasing as it was was I didn't find that -- this could be a failure of imagination on my part. I didn't consider the other alternatives that I -- of which I was aware, but admitting the possibility using the phrase that I used that there might be some other explanation which you might give me now.")).

2. Even Under The Definition Proposed By Complaint Counsel's Economic Expert, Rambus's Conduct Was Not Exclusionary.

1448. The evidence shows that Rambus's conduct was not exclusionary even as that term was defined by Complaint Counsel's economic expert. The exclusion of inferior products from the market is not exclusionary in an economic sense. (McAfee, Tr. 7536).

Response to Finding No. 1448: The statement in this proposed finding that the "evidence shows that Rambus's conduct was not exclusionary even as that term was defined by Complaint Counsel's economic expert" lacks any reference to the record.

Furthermore, this proposed finding vague because the phrase "inferior products" is undefined. Depending on the definition of that phrase, this proposed finding might also be misleading.

Professor McAfee testified that "inferior" technologies should be distinguished from "equal or superior" technologies in the context of this case by the fact that equal or superior technologies are the technologies that could have been chosen by JEDEC had Rambus disclosed. (McAfee, Tr. 7312-7315, 7554-7556; CCFF 2764-2821). As a consequence of the fact that the equal or superior technologies could have been chosen, they constrained the prices of the Rambus-claimed technologies *ex ante.* (McAfee, Tr. 7476 ("[C]onduct that eliminates equal or superior competitors

is generally going to harm consumers by reducing their choice and eliminating competition in the marketplace."), 7577-7579; CCFF 2963-2967).

1449. According to Complaint Counsel's economic expert, in order for conduct to be exclusionary, it must impact equal or superior alternatives. (McAfee, Tr. 7537).

Response to Finding No. 1449: This proposed finding is vague because the phrase "equal or superior alternatives" is undefined. Depending on how this phrase is defined, this proposed finding may also be misleading.

Professor McAfee defined the phrase equal or superior alternatives to include the commercially viable alternatives that could have been chosen had Rambus disclosed. (CCRF 1448; McAfee, Tr. 7762-7763 ("So, commercially viable alternatives are price-constraining alternatives; that is to say, from the buyer's perspective, if the price of a given alternative is increased, if it's too high, the buyers can substitute one of the other alternatives, and so – I should say equal or superior from an economic perspective always includes prices. It's not – you can't actually assess whether it's equal or superior without prices. And so, ... the relationship between the price-constraining alternatives and equal or superior products is that at reasonable prices or at nearly similar prices, similar prices, the commercially viable alternatives are ... equal or superior.")).

1450. The evidence shows that there were no equal or superior alternatives in cost-performance terms. Dr. Rapp testified that the cost differences that he quantified and the performance advantages of the Rambus technologies made them superior to the alternatives in cost-performance terms. (Rapp, Tr. 9861-62).

Response to Finding No. 1450: This proposed finding is misleading because it confuses the use of the phrase "equal or superior" as used by Professor McAfee to indicate alternatives that could have been chosen, with Dr. Rapp's cost analysis.

Furthermore, the statement in this proposed finding that the "evidence shows that there were no equal or superior alternatives in cost-performance terms" is contrary to the weight of the evidence. (CCRF 969-988, 1125-1140; CCFF 2100-2414).

1451. Complaint Counsel's economic expert did not provide testimony to refute this conclusion.

Response to Finding No. 1451: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is not accurate as Professor McAfee pointed out a number of flaws in Dr. Rapp's cost analysis. (McAfee, Tr. 11229-11281; *see* DX0361-DX0370).

1452. Complaint Counsel's economic expert admitted that he did not quantify any cost differences between Rambus's technologies and the alternative technologies. (McAfee, Tr. 11340).

Response to Finding No. 1452: This proposed finding is vague because the term "quantify" is undefined. If this proposed finding is meant to imply that Professor McAfee did not consider cost differences between Rambus-claimed technologies and the alternative technologies, then this proposed finding is not accurate. Professor McAfee relied largely on the contemporaneous cost evaluations of DRAM industry participants as well as the evaluation of Professor Jacob. (CCFF 2765-2821). Furthermore, Professor McAfee evaluated the cost differences between Rambus-claimed technologies and the alternative technologies using the data relied upon by Dr. Rapp and found that evaluation led to the conclusion that there were commercially viable alternatives. (McAfee, Tr. 11229-11281).

1453. Although Complaint Counsel's economic expert admitted that JEDEC members would consider the performance of alternatives in deciding whether to pursue the alternatives (McAfee, Tr. 11340), he did not quantify the performance differences between Rambus's technologies and any of the alternatives he claimed were commercially viable. (McAfee, Tr. 7581-82, 11340). The evidence shows that Rambus's technologies were superior to the alternatives in performance terms.

Response to Finding No. 1453: This proposed finding is vague because the phrase "quantify performance differences" is undefined. If this proposed finding is meant to imply that

Professor McAfee did not consider performance differences between Rambus-claimed technologies and the alternative technologies, then this proposed finding is not accurate. Professor McAfee relied largely on the contemporaneous evaluations of DRAM industry participants, as well as the evaluation of Professor Jacob. (CCFF 2765-2821).

Furthermore, the statement in this proposed finding that the "evidence shows that Rambus's technologies were superior to the alternatives in performance terms" is contrary to the weight of the evidence. (CCRF 969-988, 1125-1140; CCFF 2100-2414).

1454. Complaint Counsel's economic expert also admitted that JEDEC members would consider the "headroom" or future flexibility of alternatives in deciding whether to pursue the alternatives. (McAfee, Tr. 11340). He did not, however, compare the headroom or future flexibility of Rambus's technologies with any of the alternatives he said were commercially viable. (McAfee, Tr. 11340-41). The evidence shows that Rambus's technologies were superior to the alternative in terms of headroom and flexibility.

Response to Finding No. 1454: This proposed finding is misleading because it implies that Professor McAfee, as an economist, was the appropriate witness to compare the technical properties of the alternative technologies, rather than Complaint Counsel's technical expert. For example, the "headroom" of asynchronous DRAM is potentially an issue regarding whether Burst EDO was a technically viable alternative. Professor Jacob, Complaint Counsel's technical expert, explicitly evaluated the headroom of asynchronous DRAM. (Jacob, Tr. 5396 ("[T]he general view is that moving to synchronous allows you to scale to higher speeds more easily and so it's a faster upgrade path. It's a simpler design mechanism for achieving higher rates of speed, but at some point it also tops out, because if you have a synchronous system with a global clock, at some point that global clock mechanism starts getting in the way of data transmission, so at some point you start moving back to mechanisms that look like asynchronous designs as well.")).

Furthermore, to the extent that this proposed finding implies that Professor McAfee did not *consider* the differences in headroom between alternatives, this proposed finding is not accurate. When the issue of the "headroom" of alternative technologies was raised, Professor McAfee evaluated the economic implications of that argument. For example, Dr. Soderman, one of Respondent's technical experts asserted that asynchronous DRAM did not have the headroom to "achieve high speeds in a general purpose environment." (Soderman, Tr. 9365-9366). Professor McAfee noted that type of argument implicitly depends on the fact that since the synchronous alternative was chosen in the early 1990s, the DRAM industry expended effort to improve that technology, and had the industry chosen the asynchronous alternative instead then the industry would have supported that alternative instead. (McAfee, Tr. 7388 ("The asynchronous designs of 1992 and 1993 are slow relative to, say, modern DDR designs, and that's because a great deal of investment has been applied to SDRAM and its successor DDR. Had the industry stayed with asynchronous designs, it's economically reasonable that those designs would have progressed. Generally in this industry I find that the application of engineering effort actually improves the product, and so the fact that they went to a synchronous design diverted resources away from asynchronous designs and made those designs less successful than they would have otherwise been.")).

1455. For example, Complaint Counsel's economic expert admitted that JEDEC behavior and JEDEC discussions show that JEDEC members valued multiple latencies and multiple burst lengths, yet he did not quantify that value. (McAfee, Tr. 11351).

Response to Finding No. 1455: This proposed finding is vague and potentially misleading for the reasons described in CCRF 1452.

The statement in this proposed finding that "JEDEC behavior and JEDEC discussions show that JEDEC members valued multiple latencies and multiple burst lengths" is not supported by the cited evidence because the testimony is cited for the truth of the matter asserted although it could

only have been admitted for the limited purpose of showing the assumptions of Professor McAfee on that subject. Citation to such testimony violates Part II of the Order on Post-Trial Briefs, July 10, 2003.

1456. Complaint Counsel's economic expert also testified that, although he had made no effort to determine if any intellectual property covered any of the alternatives that he considered commercially viable other than Kentron's technology, the presence of intellectual property *could* render a technology not commercially viable in his opinion, because JEDEC attached a "penalty" to the presence of intellectual property. (McAfee, Tr. 7582-85). As discussed above, there is evidence that several of the alternatives that he said were commercially viable are covered by patents.

Response to Finding No. 1456: This proposed finding is incomplete because it omits testimony by Professor McAfee that he understood that the presence of royalty-bearing intellectual property could render a technology not commercially viable in comparison to a technology that was not potentially burdened by a royalty. (McAfee, Tr.7584-7585 ("So it remains – it's my understanding it remains commercially viable against a technology with royalties. Against a technology without royalties, it may not be commercially viable.")).

1457. In short, Complaint Counsel's economic expert did not refute the cost-performance quantification provided by Dr. Rapp or his conclusion that Rambus's alternatives were superior to the alternatives.

Response to Finding No. 1457: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, the statement in this proposed finding that " Rambus's alternatives were superior to the alternatives" is contrary to the weight of the evidence. (CCRF 969-988, 1125-1140; CCFF 2100-2414).

1458. Because Rambus's conduct could have excluded only inferior technologies, it cannot be exclusionary even as that term is defined by Complaint Counsel's economic expert.

Response to Finding No. 1458: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

This proposed finding is also misleading and contrary to the weight of the evidence for the reasons described in CCRF 1219.

3. The Definition Of Equal Or Superior Alternatives Proposed By Complaint Counsel's Economic Expert Is Flawed.

1459. Complaint Counsel's economic expert testified that he believed that equal or superior alternatives were excluded by Rambus's alleged conduct. His definition of "equal or superior" was, however, flawed. To determine whether equal or superior alternatives were excluded, Complaint Counsel's expert developed a "commercial viability" test. (McAfee, Tr. 7330-31).

Response to Finding No. 1459: This proposed finding is vague because the phrase "'commercial viability' test" is undefined. Depending on the meaning of that phrase, this proposed finding may also be misleading. In that respect, Professor McAfee testified that he attempted to determine the existence of price-constraining alternatives by evaluating the actions of JEDEC members, in particular the serious consideration of those alternatives at JEDEC in the relevant time frame. (McAfee, Tr. 7331-7345). Furthermore, Professor McAfee testified that the term "commercially viable" was simply the name that he gave to the technologies that ended up in the relevant market. (McAfee, Tr. 7566-7567).

1460. Although he claimed that his methodology was "parallel" to standard economic tests, Complaint Counsel's economic expert admitted that he was aware of no economic literature that describes the use of a "commercial viability" test to determine market substitutability of alternatives. (McAfee, Tr. 7567).

Response to Finding No. 1460: This proposed finding is vague and potentially misleading for the reasons described in CCRF 1459.

1461. According to Complaint Counsel, an alternative was "commercially viable" if it constrained the price of Rambus's technologies. (McAfee, Tr. 7330-31). But defined that way, the concept of "commercially viable" does not mean that the technology is "equal or superior." Even weak substitutes can constrain the price of a technology. (Rapp, Tr. 9860). An alternative can therefore be "commercially viable" in this sense without being equal or superior or even a viable alternative in any practical sense (Teece, Tr. 10368, 10370-71).

Response to Finding No. 1461: This proposed finding is inaccurate because Professor McAfee's use of the term "commercially viable" in reference to a technology meant that the technology was a price constraining alternative to the technology chosen for the standard, and that in order for an alternative to be price constraining in any economic sense, it had to be an equal or superior technology as evaluated by JEDEC. (McAfee, Tr. 7762-7763 ("So, commercially viable alternatives are price-constraining alternatives; that is to say, from the buyer's perspective, if the price of a given alternative is increased, ... the buyers can substitute one of the other alternatives, and so – I should say equal or superior from an economic perspective always includes prices. It's not – you can't actually assess whether it's equal or superior without prices. And so, ... the relationship between the price-constraining alternatives and equal or superior products is that at reasonable prices or at ... similar prices, the commercially viable alternatives are ... equal or superior.")).

1462. What is more, when determining whether an alternative was price constraining, Complaint Counsel's economic expert provided no analysis of price elasticity. In other words, he did not consider the price level required before the alternatives would actually constrain the price. Instead, he simply looked for evidence that the alternative was considered as a possible alternative by members of JEDEC and that knowledgeable engineers now claimed that the alternative was viable. (McAfee, Tr. 7333-34).

Response to Finding No. 1462: This proposed finding is incomplete because it omits testimony by Professor McAfee that in markets where the products or technologies in question are not widely traded, there is not generally sufficient price information to determine the price elasticity of demand, and as a consequence, in those circumstances, economists analyze buyer substitution by looking at what buyers have actually done in response to changes in relative prices.

(CCFF 2762, 2767-2771). This proposed finding is incomplete for the additional reason that it omits testimony by Professor McAfee that one accepted approach to understanding buyer substitution in the absence of historical pricing data is to interview relevant purchasers in the marketplace. (CCFF 2762).

1463. Further, Complaint Counsel's economic expert tied his notion of commercial viability to subjective judgments of JEDEC members. (McAfee, Tr. 7335). This had several consequences for his analysis.

Response to Finding No. 1463: This proposed finding is vague because the term "tied" and the phrase "subjective judgments of JEDEC members" are undefined.

To the extent the term "tied" is intended to imply that Professor McAfee considered only the subjective judgements of JEDEC members, this proposed finding is inaccurate. For example, Professor McAfee considered the opinions of Professor Jacob. (*See e.g.*, McAfee, Tr. 7360). Professor McAfee also considered the cost information provided by Mr. Geilhufe. (McAfee, Tr. 11249-11278).

To the extent the phrase "subjective judgments of JEDEC members" means the testimony of current or former JEDEC members, this proposed finding is inaccurate. Professor McAfee, also considered that the technologies in question were given serious consideration by JEDEC in the relevant time period as reflected in the JEDEC minutes. (McAfee, Tr. 7566; *see* DX0176).

1464. First, Complaint Counsel's economic expert judged patented technologies to be "hobbling" because the JEDEC rules put a "penalty" on technologies that were covered by intellectual property. (McAfee, Tr. 7337,7582-83). He thus regarded patented technologies, such as Rambus's, as inferior merely because of the presence of intellectual property and without regard to the level of royalties sought for that technology.

Response to Finding No. 1464: This proposed finding is inaccurate because Professor McAfee specifically testified that his determination of what technologies were equal or superior and therefore commercially viable depends on prices. (McAfee, Tr. 7763 ("I should say

equal or superior from an economic perspective always includes prices. It's not -- you can't actually assess whether it's equal or superior without prices.")).

1465. Determining whether an alternative is "equal or superior" cannot turn on such subjective judgments. In a competitive market, if the best solution in cost-performance terms is patented and involves the payment of royalties, competition will dictate that the royalties be paid and that the patented solution is adopted. (Rapp, Tr. 9939). While individual executives in an industry may dislike paying royalties, just as they may dislike paying health care costs for workers or a competitive wage, they will have no choice because competition will mandate that these costs be incurred. (Rapp, Tr. 9938-39).

Response to Finding No. 1465: The statement in this proposed finding that in a competitive market, "if the best solution in cost-performance terms is patented and involves the payment of royalties, competition will dictate that the royalties be paid and that the patented solution is adopted," is unsupported by the cited testimony. Dr. Rapp testified that it was his opinion that "in a competitive market, if the best solution *taking account of licensing arrangements* is one that involves payments of royalties, then competition dictates that royalties will be pa*id*." (Rapp, Tr. 9939, *emphasis added*).

Furthermore, this proposed finding ignores substantial evidence in the record that firms in the DRAM industry might want to avoid including potentially royalty-bearing technologies in JEDEC standards because of the threat of hold-up. The weight of the evidence is that the DRAM industry and other firms that make components that are interoperable with DRAM have been concerned about being locked in to a standardized technology that is covered by hidden intellectual property. (CCFF 2682-2756).

1466. Second, Complaint Counsel's economic expert also considered "a perception of the magnitude of those problems" associated with that technology as "relevant to the determination of which technologies should be selected." (McAfee, Tr. 7586). In other words, he based his determination of whether a technology was "equal or superior" on the subjective perceptions of JEDEC members at the time, regardless of whether these perceptions were ultimately correct. While this factor may go to whether JEDEC would have selected the technology, it does not go to whether the alternative is equal or superior in objective terms.

Response to Finding No. 1466: Complaint Counsel agrees that Professor McAfee considered that other factors, as well as cost and performance, were relevant to his determination of what technologies could have been chosen by JEDEC had Rambus disclosed. Complaint Counsel also agrees that the understandings of JEDEC members regarding the relevant technologies during the relevant period, goes to the question of whether JEDEC would have selected a particular technology had Rambus disclosed. It is not clear from this finding what the relevance is of whether an "alternative is equal or superior in objective terms" to some other technology.

1467. Third, Complaint Counsel's economic expert considered each company's strategic interests in which technology would be selected because of differences in technical ability. (McAfee, Tr. 7338-39). In other words, in determining whether a technology was commercially viable, he factored in whether some JEDEC members might prefer the technology because they were better equipped to produce it. Again, while this factor may go to whether JEDEC would have selected the technology, it does not go to whether the alternative is equal or superior in objective terms.

Response to Finding No. 1467: Complaint Counsel agrees that the factors that Professor McAfee considered in determining commercial viability, including the strategic interests and different technical abilities of the voting members of JEDEC goes to the question of whether JEDEC would have selected a particular technology had Rambus disclosed. It is not clear from this finding what the relevance is of whether an "alternative is equal or superior in objective terms" to some other technology.

1468. Fourth, Complaint Counsel's economic expert relied on his notion of "satisficing" to conclude, in effect, that a product that has lesser performance is nonetheless "equal" to one with better performance. (McAfee, Tr. 7335-36). In other words, because he believed that JEDEC was "satisficing," Complaint Counsel's economic expert essentially defined "equal" to include technologies that were *inferior* to Rambus's technologies.

Response to Finding No. 1468: This proposed finding is misleading because it implies that Professor McAfee testified that JEDEC would determine what is the best technology and then choose an inferior technology. Instead, Professor McAfee testified that he understood that

because of the time to market concerns of the JEDEC members, JEDEC would not spend a lot of time trying to find the best alternative, but would find something that was good enough and then move on to the next problem. (McAfee, Tr. 7335-7336 ("[The concept of satisficing] arose out of the time-to-market issues, and what that ... entails is that for commercial viability is that several products can easily be commercially viable in that they aren't trying to make it perfect. They're trying to get a workable product that everybody or most of the companies can manufacture and that the buyers can use in their installations in a rapid and expedient manner.")).

1469. Fifth, when it came to cost and performance, as explained above, Complaint Counsel's economic expert offered no quantitative data.

Response to Finding No. 1469: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is vague and potentially misleading for the reasons described in CCRF 1452-1453.

1470. Not only were the factors considered by Complaint Counsel's economic expert subjective, his methodology was as well. Rather than examining the actual cost differences between the Rambus technologies and the alternatives, Complaint Counsel's economic expert simply opined that he had considered an amalgam of factors and determined that certain alternatives were "commercially viable" based "on the information [he] analyzed." (See, e.g., McAfee, Tr. 7363).

Response to Finding No. 1470: This proposed finding is misleading because it implies that Dr. Rapp examined the actual cost differences between the Rambus technologies and the alternatives. However, there is no evidence that Dr. Rapp did evaluate any "actual costs differences," given that the only cost information he relied upon were the cost estimates provided by Mr. Geilhufe. (CCFF 2828). Mr. Geilhufe testified that his cost estimates were not the actual costs of any DRAM manufacturer but a series of rough estimates based on his own experience.

(2123-2125). Mr. Geilhufe also testified that he had never designed an SDRAM or a DDR SDRAM, and that he had never designed a JEDEC-compliant DRAM of any sort. (CCFF 2113). Finally, even Dr. Rapp testified that he understood that Mr. Geilhufe did not testify as to what cost information JEDEC or JEDEC participants had in the *ex ante* period. (CCFF 2831).

Furthermore, this proposed finding is inaccurate because Professor McAfee did evaluate the alternatives using the cost information provided by Mr. Geilhufe and found that, using those cost estimates, there were a number of commercially viable alternatives to the technologies claimed by Rambus. (McAfee, Tr. 11249-11278).

1471. While Complaint Counsel's economic expert testified that it was likely that at least one of the technologies he deemed commercially viable alternatives to Rambus's technology was equally efficient or superior to Rambus's technology, he admitted that he could not identify any particular technology as equal or superior to Rambus's technologies. (McAfee, Tr. 7578-79).

Response to Finding No. 1471: This proposed finding is not accurate. Professor McAfee testified that he was not able to determine *which technology would have been chosen* had Rambus disclosed. (McAfee, Tr. 7578-7579 ("So my understanding of these technologies and also of the meaning of commercial viability is such that given intellectual property, the others – one of the others, not – I'm not sure I know which one – but that one of the others would have been selected over the Rambus technology. I think we went through that logic today. And the implication of that was that for JEDEC, given the disclosure, the others were – actually I need to say likely. I left out the word "likely" in that. At least one of them was – of the excluded technologies was equally efficient or superior, but I don't know necessarily which one.")).

4. Complaint Counsel's Economic Expert Admitted That Complaint Counsel's Theory of Exclusionary Conduct Requires Economically Irrational Behavior.

1472. The theory of exclusion put forth by Complaint Counsel's economic expert requires an assumption that Rambus behaved irrationally.

Response to Finding No. 1472: This proposed finding lacks any reference to the record. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is inaccurate because Professor McAfee had two reasons why Rambus's conduct was exclusionary, neither of which required that Rambus act irrationally. (CCFF 2986-3011).

1473. In determining that Rambus's conduct was exclusionary, Complaint Counsel's economic expert assumed that Rambus *knowingly* took a risk that it might lose the ability to enforce its patents by not disclosing patent interests that it should have disclosed. (McAfee, Tr. 7538-40). Complaint Counsel's economic expert believed that Rambus did so solely to dupe JEDEC into incorporating its technologies into the JEDEC standards.

Response to Finding No. 1473: This proposed finding is inaccurate because Professor McAfee had two reasons why Rambus's conduct was exclusionary, only one of which required that Rambus knowingly took a risk that it might lose the ability to enforce its patents by not disclosing patent interests that it should have disclosed. (CCFF 2986-3011).

1474. But Complaint Counsel's economic expert admitted that Rambus would have understood that if it withheld information about its patent applications that it should have disclosed, any effort to enforce its patents once they issued, would have triggered an inquiry into whether Rambus should have disclosed its patent interests. In addition, Complaint Counsel's economic expert admitted that if a JEDEC member failed to disclose patent interests that should have been disclosed and revealed knowledge of that patent interest, e.g., in a written document, the risk of a challenge that would render the patents invalid would increase substantially. (McAfee, Tr. 7550).

Response to Finding No. 1474: The statement in this proposed finding that Professor McAfee "admitted that Rambus would have understood that if it withheld information about its patent applications that it should have disclosed, any effort to enforce its patents once they issued, would have triggered an inquiry into whether Rambus should have disclosed its patent interests," is incomplete because it omits testimony by Professor McAfee that he thought of that

possibility merely as a matter of human nature and not as a part of his opinion as an economist. (McAfee, Tr. 7547 ("As a -- as human nature, so sort of somewhat outside of my economic reasoning, although human nature is actually part of the domain of economics, but it would be consistent with my understanding of human nature that people would at least be curious not so much when the patents issued but at the point that Rambus started suing them.")).

Furthermore, the statement in this proposed finding that Professor McAfee "admitted that if a JEDEC member failed to disclose patent interests that should have been disclosed and revealed knowledge of that patent interest, e.g., in a written document, the risk of a challenge that would render the patents invalid would increase substantially," is misleading. Professor McAfee agreed that if Rambus's JEDEC representative, Richard Crisp, had revealed specific knowledge of Rambus's patents in a written document which could later be used against Rambus, where Rambus later attempted to enforce its patents, that would increase the risk of an investigation. (McAfee, Tr. 7550 ("I think "at some level of knowledge" is an inadequate description. I would describe this as being on a continuum. That is to say, if he revealed specific knowledge in a written document which could later be used against Rambus, that would actually enhance the risks very substantially. On the other hand, vague generalities are not going to be much revelation at all. So I would describe this as on a continuum and it would matter the specific nature of the revelations.")).

1475. In other words, the theory of Complaint Counsel's economic expert assumed that Rambus's conduct was irrational because it would have known that its scheme would fail. He theorizes that Rambus withheld information about its patent applications to be able to enforce its patents against JEDEC members while knowing that the result of that conduct might be that it would be unable to enforce those patents.

Response to Finding No. 1475: The statement in this proposed finding that Professor McAfee assumed that Rambus's conduct was irrational is not accurate. (CCRF 1472).

Furthermore, Professor McAfee made no assumptions and came to no economic conclusions regarding the likelihood that Rambus's scheme would fail, only that Rambus's conduct risked that outcome. (CCFF 3006-3011; CCRF 1474).

Furthermore, this proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

5. Complaint Counsel's Economic Expert's Opinion Rests On An Assumption Of That A "Violation Of A Rule Or Process" Caused JEDEC To Adopt The Rambus Technologies.

1476. Complaint Counsel's economic expert explained that Rambus's concealing of information about its patent applications would, in his opinion, be exclusionary only if it violated a rule or process. (McAfee, Tr. 7530-31, 7546).

Response to Finding No. 1476: This proposed finding is inaccurate. Professor McAfee *assumed* that Rambus's conduct included a violation of a JEDEC rule or process. (McAfee, Tr. 7530 ("Well, I considered that I was very explicit about the assumptions that I was making in this, and I agree that I'm assuming that there was a material – that material information, relevant information, should have been revealed and was not and – but that's an assumption on my part, not a finding.")). An alternate assumption was that Rambus made misrepresentations to JEDEC. (McAfee, Tr. 7478, *see* DX0231).

1477. He assumed that Rambus "should have disclosed patents or patent applications with reference to all four of the technologies challenged in the case." (McAfee, Tr. 7546). But he admitted that, "If they shouldn't have disclosed on one of the technologies, then my finding of exclusionary conduct on that technology is no longer -- on that particular technology would no longer be reliable because I've assumed that they should have disclosed on that technology." (McAfee, Tr. 7546).

Response to Finding No. 1477: Complaint Counsel does not disagree.

1478. Yet Complaint Counsel's economic expert admitted that he did his analysis with no assumptions about the specific claims of any patent application that Rambus should have allegedly disclosed. (McAfee, Tr. 7669-70).

Response to Finding No. 1478: Complaint Counsel does not disagree.

1479. Complaint Counsel's economic expert also admitted that he did his analysis with no assumptions about the specific date that Rambus allegedly should have made the disclosures that Complaint Counsel allege should have been made. (McAfee, Tr. 7671).

Response to Finding No. 1479: Complaint Counsel does not disagree.

1480. Complaint Counsel's economic expert also admitted that he did his analysis with no assumed specific triggering event that would have caused Rambus to be obligated to make disclosures to JEDEC. (McAfee, Tr. 7671).

Response to Finding No. 1480: Complaint Counsel does not disagree.

1481. The premise of Complaint Counsel's economic expert is false because as discussed above, Rambus did not have, and in any event was not obligated to disclose, patent applications covering any of the four technologies while it was a JEDEC member.

Response to Finding No. 1481: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (CCFF 310-348, 500-1237).

1482. Complaint Counsel's economic expert admitted that if work on DDR had not begun by the time Rambus had left JEDEC and if there was no duty to disclose absent such work, the conclusions that he drew from assuming that Rambus failed to disclose with regard to DDR would fall away. (McAfee, Tr. 7575). As discussed above, no duty to disclose regarding DDR technologies was triggered while Rambus was attending JEDEC.

Response to Finding No. 1482: This proposed finding is misleading because Professor McAfee did not come to any conclusions regarding whether Rambus violated the JEDEC patent disclosure rules. (McAfee, Tr. 7574-7575 ("I haven't concerned myself with the determination of did they have a duty to disclose other than I read a fair number of documents just

so that I was comfortable that there was actually a reasonable assumption to be made. But that is still an assumption as opposed to a conclusion that I'm testifying to.")).

Furthermore, the statement in this proposed finding that "no duty to disclose regarding DDR technologies was triggered while Rambus was attending JEDEC," is contrary to the weight of the evidence. (CCFF 578-648).

1483. Complaint Counsel's economic expert admitted that if Rambus made the additional disclosures that Complaint Counsel allege should have been made, JEDEC ignored the disclosure, and JEDEC incorporated the Rambus technology nonetheless, Rambus would not have engaged in exclusionary conduct. (McAfee, Tr. 7682). As discussed above, this is a likely outcome had the additional disclosures been made.

Response to Finding No. 1483: This proposed finding is not accurate as Professor McAfee agreed that if Rambus made a disclosure, JEDEC made a determination that it did not think patents would issue that covered the Rambus technology they sought to incorporate into the standard and for that reason did not request a RAND assurance or RAND letter, and if the disclosure had occurred in good faith, then the Rambus conduct would not have been exclusionary. (McAfee, Tr. 7682).

Furthermore, the statement in this proposed finding that "this is a likely outcome had the additional disclosures been made" is contrary to the weight of the evidence. (CCFF 318, 347-348; CCRF 1159-1182).

1484. Complaint Counsel's economic expert also admitted that there are situations in which JEDEC could become aware of Rambus' potential patents other than through Rambus' disclosure of that information to JEDEC, such that Rambus' failure to disclose would not, as a matter of economics, constitute exclusionary conduct. (McAfee, Tr. 7686). As discussed above, JEDEC members were in fact aware of the risk that Rambus could obtain patents on the four technologies.

Response to Finding No. 1484: This proposed finding is vague because the phrase "situations in which JEDEC could become aware of Rambus' potential patents other than through Rambus' disclosure of that information to JEDEC" is undefined as to what situations could lead to

that result. Depending on the meaning of that phrase this proposed finding may also be misleading.

Furthermore, the statement in this proposed finding that "JEDEC members were in fact aware of the risk that Rambus could obtain patents on the four technologies" is contrary to the weight of the evidence. (CCFF 1238-1357).

1485. Complaint Counsel's economic expert further admitted that it is both plausible and consistent with his assumptions that if Rambus never joined JEDEC, JEDEC would have selected the four Rambus technologies for inclusion in its standards. (McAfee, Tr. 7688). In other words, Complaint Counsel's economic expert conceded that Rambus's conduct did not cause JEDEC to select the four technologies at issue in this case over others.

Response to Finding No. 1485: This proposed finding is incomplete because it omits testimony from Professor McAfee that he made no assumption regarding what would have happened had Rambus never joined JEDEC. (McAfee, Tr. 7688).

Furthermore, Professor McAfee's but-for world analysis, like the but-for world analysis of Professor Teece, required that the only thing that was different between the real world and the but-for world was the conduct that Complaint Counsel alleges should not have occurred. (CCFF 3018-3019). There is no allegation in this case that Rambus should not have joined JEDEC.

In addition, the statement in this proposed finding that "Complaint Counsel's economic expert conceded that Rambus's conduct did not cause JEDEC to select the four technologies at issue in this case over others" is not accurate. Professor McAfee testified that the most likely result in the but-for world was that JEDEC would have avoided the technologies claimed by Rambus. (McAfee, Tr. 11314-11315 ("Professor Teece has ruled out adopting alternative standards, and I would not rule out adopting alternative standards. In fact, I think that's what would in fact happen. So that is, I would put no probability/weight on adopting the existing standards, but instead I would actually expect because of the existence of commercially viable alternatives that one of those alternatives is in fact adopted."); *see* DX0375 ("Most likely outcome is JEDEC work-around")).

1486. In sum, even applying Complaint Counsel's economic expert's reasoning, Rambus's alleged conduct was not exclusionary.

Response to Finding No. 1486: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

6. Complaint Counsel Has Not Shown That Enforcing JEDEC's Rules Furthers The Objective Of Antitrust Law.

1487. Complaint Counsel's economic expert based his entire analysis on the assumption that Rambus's conduct violated a JEDEC rule or process. (McAfee, Tr. 7530-31).

Response to Finding No. 1487: This proposed finding is inaccurate, because the cited testimony does not indicate that Professor McAfee based his "entire analysis" on the assumption that Rambus's conduct violated a JEDEC rule or process but, rather that one of the assumptions for one of his reasons why Rambus's conduct was exclusionary in the economic sense was that Rambus's conduct violated a JEDEC rule or process. (CCFF 2992-3011).

1488. Yet Complaint Counsel's economic expert admitted that he had done no analysis to determine whether JEDEC's rules and processes advanced the interests of antitrust law. (McAfee, Tr. 7532-33).

Response to Finding No. 1488: This proposed finding is incomplete because it omits testimony by Professor McAfee that JEDEC's patent disclosure rules can be seen as an expression on the part of JEDEC of an interest to avoid the hold-up problem. (CCFF 2682-2690).

Furthermore, this proposed finding is incomplete because it omits testimony by Professor McAfee that there is substantial potential for lock-in and hold-up in the DRAM industry and that could lead to dominance of a particular technology in the marketplace. (CCFF 2703-2709).

1489. Nor did Complaint Counsel's economic expert perform any analysis of the JEDEC's costs and benefits in order to determine the economically efficient disclosure rules for it to impose. (McAfee, Tr. 7727). In fact, he admitted that he has not investigated the economic efficiency of JEDEC's rules. (McAfee, Tr. 7727-28).

Response to Finding No. 1489: Complaint Counsel does not disagree.

1490. Complaint Counsel's economic expert did, however, opine that the "preferred" time for disclosure of information regarding intellectual property is as early as possible. (McAfee, Tr. 7301). As an economic matter, however, it is not correct that the optimal time for disclosure of information regarding patent interests is as early in the standardization process as possible. (Teece, Tr. 10385).

Response to Finding No. 1490: Complaint Counsel does not disagree with the statement in this proposed finding that Professor McAfee gave an opinion that "the 'preferred' time for disclosure of information regarding intellectual property is as early as possible."

Complaint Counsel does not disagree that Professor Teece stated that he believed that it is not correct that the optimal time for disclosure of information regarding patent interests is as early in the standardization process as possible.

However, while Professor Teece might believe, as a matter of economics that it is not correct that the optimal time for disclosure of information regarding patent interests is as early in the standardization process as possible, the weight of the evidence is that JEDEC and JEDEC members believed that the rule at JEDEC was that disclosures should occur as soon as possible. (CCFF 339-345).

1491. Comments provided by the Institute of Electrical and Electronics Engineers Standards Association ("IEEE-SA") to the FTC in April 2002 speak to this issue. The IEEE is a professional society of engineers with over 370,000 members, whose standards arm has more than 870 active standards. (RX 2011 at 1).

Response to Finding No. 1491: It is unclear how this proposed finding is relevant to the issues in this case. It has been a consistent evidentiary ruling in this case that the rules and conduct of other standard setting organizations are not relevant to the issues in this case. (Bechtelsheim, Tr. 5887-5888 ("MR. STONE: Your Honor, I move to strike on the grounds that this testimony goes directly to the area which we have proffered Mr. Keefauver as an expert witness on and which complaint counsel made a motion, which was granted, in limine preventing

him from testifying as to the conduct and understanding that would come from other standards-setting organizations, and this is based on the witness – JUDGE McGUIRE: Sustained. I will not entertain the answer regarding his understanding of other organizations, the IEEE I believe he mentioned ...."); Tabrizi, Tr. 9122-9123 ("MR. PERRY: Your Honor, excuse me. There was a motion to exclude Mr. Keefauver, who we wanted to testify before this hearing about patent policies of other standard organizations. We would move to strike that testimony or we would move to have the right to bring in Mr. Keefauver. JUDGE McGUIRE: You do not have the right to bring in Mr. Keefauver because I've already ruled against that, so you do not have that right. MR. PERRY: I'm sorry. I didn't mean to get hot on that. It's just that motion was hard-fought. We lost an expert. They said other patent policies of other organizations are completely irrelevant. JUDGE McGUIRE: And that's going to apply here as well, Mr. Oliver.")). The rules of the IEEE are not part of the record of this proceeding. *See* Order on Motions in Limine at 5 (April 21, 2003). Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, RPF 1491 does not support the conclusion that disclosure of intellectual property as early as possible is not the preferred time for *JEDEC* to require disclosure. Members of the SyncLink Consortium formed their organization outside of the IEEE precisely because the IEEE's patent policy was unsatisfactory. CCFF 1558. Rambus itself clearly recognized that the IEEE patent policy was different and less stringent than the JEDEC policy. When Mr. Crisp refused to properly disclose intellectual property relating to SyncLink in September 1995, he noted that "SyncLink is being sponsored by an organization [the IEEE] <u>with a less stringent patent policy than JEDEC</u>." (JX0027 at 26) (emphasis added).

1492. The IEEE-SA informed the FTC in April 2002, in connection with the FTC/DOJ hearings regarding competition and intellectual property, that:

> "[i]f disclosure of issued patents is expected too early in the process - i.e., before the draft standard has reached a level of stability – more patents may be disclosed than those that are essential, since it may be too early to determine exactly those that will be required for implementation. This problem would become even larger if, as some have suggested, patent applications were to be treated in the same manner as issued patents. A 'one size fits all' solution cannot be applied to disclosure."

(RX 2011 at 5).

Response to Finding No. 1492: This proposed finding is irrelevant for the reasons described in CCRF 1491.

Furthermore, this proposed finding is irrelevant because Rambus clearly understood that the IEEE patent policy was different and less stringent than the JEDEC policy. When Mr. Crisp refused to properly disclose intellectual property relating to SyncLink in September 1995, he noted that "SyncLink is being sponsored by an organization [the IEEE] with a less stringent patent policy than JEDEC." (JX0027 at 26) (emphasis added). Reliance on the purported views of the IEEE to gain an understanding of JEDEC's rules is questionable given that the SyncLink Consortium formed precisely because its members viewed the IEEE's patent disclosure policies as inadequate. *See* CCFF 1558.

Furthermore, RPF 1492 does not support the conclusion that disclosure of intellectual property as early as possible is not the preferred time for JEDEC to require disclosure. As the IEEE letter confirms, a "one size fits all" approach may be inappropriate given the wide variety of standard setting organizations that exist. The IEEE provided these comments to the Federal Trade Commission and the Department of Justice in the context of arguing against the government issuing specific regulatory requirements that would apply to all standard setting organizations. (RX2011 at 1-2).

1493. As Professor Teece testified, disclosure involves costs, so the optimal time for disclosure must consider those costs. (Teece, Tr. 10385). Depending on the costs and benefits, later disclosure may be optimal. (Teece, Tr. 10402).

Response to Finding No. 1493: Complaint Counsel does not disagree that this proposed finding reflects Professor Teece's opinions of the hypothetical costs and benefits for the timing of disclosure of intellectual property to standards setting bodies. However, this proposed finding is incomplete because it omits testimony from Professor Teece that he could not, as a matter of economics, determine the preferred time for intellectual property disclosure to standards setting organizations. (Teece, Tr. 10453).

1494. The costs involved include the cost to the patent applicant of losing trade secrets and confidentiality. (Teece, Tr. 10453). The costs to the standard-setting organization are that it must try to evaluate and assess the highly preliminary information regarding the patent application. (Teece, Tr. 10453-54).

Response to Finding No. 1494: This proposed finding is incomplete for the reasons described in CCRF 1493.

1495. Since patents are not going to change and are public, the costs associated with disclosing patents are less than those associated with disclosing patent applications. (Teece, Tr. 10454-55).

Response to Finding No. 1495: This proposed finding is incomplete for the reasons described in CCRF 1493.

1496. As the IEEE-SA explained in its April 2002 comments,

> "[s]tandards committees realize that until a patent has been issued there is very little value to disclosure since the scope of valid patent claims has not been determined. This is why it is not appropriate to group issued patents and applications togehter, especially in the context of antitrust policy where government action could have a significant impact on standards-setting procedures."

(RX 2011 at 5).

Response to Finding No. 1496: This proposed finding is irrelevant for the reasons described in CCRF 1491-1492.

RPF 1496 does not support the conclusion that disclosure of intellectual property as early as possible is not the preferred time for JEDEC to require disclosure. As the IEEE letter confirms, a "one size fits all" approach may be inappropriate given the wide variety of standard setting organizations that exist. The IEEE provided these comments to the Federal Trade Commission and the Department of Justice in the context of arguing against the government issuing specific regulatory requirements that would apply to all standard setting organizations. (RX2011 at 1-2).

1497. The narrower the scope of disclosure regarding patent applications, the lower the costs and burdens of disclosure. (Teece, Tr. 10454, 10547-58). If intellectual property issues are put aside once a RAND assurance is given, there is less need for disclosure. (Teece, Tr. 10548).

Response to Finding No. 1497: This proposed finding is incomplete for the reasons described in CCRF 1493.

1498. Complaint Counsel's economic expert also opined that disclosure rules mitigate the risk of hold up. (McAfee, Tr. 7272-74). But he admitted that JEDEC's disclosure rules do little to mitigate risk because the disclosure obligation applies only to the knowledge of the representative at the meeting, rather than that of the member company (McAfee, Tr. 7724); and because in large companies, the representative might not have a lot of knowledge about the company's patents. (McAfee, Tr. 7724-25). He also admitted that a JEDEC disclosure requirement does not mitigate the risk that the standard might involve technology covered by patents held by nonmembers. (McAfee, Tr. 7725).

Response to Finding No. 1498: Complaint Counsel does not disagree that Professor McAfee testified that it was his opinion that disclosure rules mitigate the risk of hold up.

However, the statement in this proposed finding that Professor McAfee " admitted that JEDEC's disclosure rules do little to mitigate risk" is not accurate, and is unsupported by the cited testimony.

1499. In short, Complaint Counsel have not shown that enforcing JEDEC's rule and procedures – as Complaint Counsel have depicted those rules and procedures – furthers the interests of antitrust law.

Response to Finding No. 1499: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel

submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

B. Rambus's Alleged Failure To Disclose Did Not Increase Or Add To Its Market Power.

1500. A critical question in this case is whether the alleged conduct enhanced Rambus's market power.

Response to Finding No. 1500: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1501. Because technologies may have market power simply by virtue of their technological superiority, it is important to distinguish the source of any market power Rambus may have.

Response to Finding No. 1501: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1502. Assuming that (1) JEDEC rules obligated Rambus to disclose additional information about its patent applications, (2) Rambus knowingly and intentionally violated that obligation in order to mislead JEDEC members, and (3) JEDEC members were actually misled, the question remains whether the alleged conduct caused Rambus to gain additional market power. The evidence shows that it did not.

Response to Finding No. 1502: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (CCFF 2600-3060).

1. JEDEC's Standardization Of Rambus's Technologies Did Not Enhance Rambus's Market Power.

1503. The evidence shows that JEDEC's standardization of Rambus's technologies did not enhance Rambus's market power. Any market power that Rambus has is attributable to the fact that its technologies were and are superior to any alternatives. If they were not, the DRAM industry could switch to alternatives.

Response to Finding No. 1503: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

The statement in this proposed finding that "JEDEC's standardization of Rambus's technologies did not enhance Rambus's market power" is contrary to the weight of the evidence. (CCFF 2500-2584, 2901-2904, 2914-2958; CCRF 1259-1360).

The statement in this proposed finding that "[a]ny market power that Rambus has is attributable to the fact that its technologies were and are superior to any alternatives" is contrary to the weight of the evidence. (CCFF 2102-2414, 2763-2821, 2856-2884; CCRF 969-988, 1125-1140).

The statement in this proposed finding that " the DRAM industry could switch to alternatives" is contrary to the weight of the evidence. (CCFF 2500-2584, 2901-2904, 2914-2958; CCRF 1259-1360).

1504. On this issue, Rambus offered the testimony of Dr. Rapp, who has expertise in the area of standard setting. As an example, he recently presented a paper on the economics of standard setting at a session of the Antitrust Section of the American Bar Association, which Dr. Rapp proposed and helped to organize. (Rapp, Tr. 9770-71).

Response to Finding No. 1504: Complaint Counsel does not disagree. However, this proposed finding does not support the conclusion that Dr. Rapp is well qualified to give this type of economic opinion for the reasons set forth in CCRF 1442.

1505. Last year, Dr. Rapp presented a paper and testified about the issue of standard setting and market power at the joint hearings of the Federal Trade Commission and the Department of Justice on intellectual property and the knowledge based economy. (Rapp, Tr. 9771).

Response to Finding No. 1505: Complaint Counsel does not disagree. However, this proposed finding does not support the conclusion that Dr. Rapp is well qualified to give this type of economic opinion for the reasons set forth in CCRF 1442.

1506. In contrast, Complaint Counsel's economic expert has no expertise in the area of standard setting. (McAfee, Tr. 11345).

Response to Finding No. 1506: This proposed finding is not accurate. Professor McAfee testified that he was familiar with the economics literature in the area of standard setting. (McAfee, Tr. 7532 ("I have good familiarity with the standard-setting literature generally")). Professor McAfee, included a discussion of that literature in his book on business strategy and industrial organization. (McAfee, Tr. 11345).

1507. According to the economic literature, a standard is a specification of a product design intended to achieve engineering compatibility, either between parts of a product or system or between components of a network. (Rapp, Tr. 9783). Economists recognize that standards are necessary when compatibility requirements are high and when either products, systems, or networks will fail unless engineering compatibility is maintained. (Rapp, Tr. 9783). From an economist's point of view, standard setting does not entail specifying every detail of a product; rather, standard setting is economically efficient when it achieves compatibility but does not over-determine product characteristics. (Rapp, Tr. 9785).

Response to Finding No. 1507: Complaint Counsel does not disagree.

1508. Economist refer to standards that are set through formal means, i.e., through a standard-setting body or the government, as *de jure* standards. (Rapp, Tr. 9788-89). Standards that emerge through market forces are referred to as de facto standards. (Rapp, Tr. 9789).

Response to Finding No. 1508: Complaint Counsel does not disagree.

1509. In a market where compatibility requirements are exceedingly high, the market might permit only a single standard. (Rapp, Tr. 9791). This may occur in a network industry, which require a special kind of complementarity where systems must be able to communicate. (Rapp, Tr. 9792). The typical example of this type of network effect is the fax machine. A fax machine is worthless if it cannot communicate with other fax machines; the more fax machines that it is able to communicate with, the more valuable it is. (Rapp, Tr. 9792-93).

Response to Finding No. 1509: Complaint Counsel does not disagree.

1510. Where compatibility requirements are less than extreme, which is more common, multiple standards may coexist. (Rapp, Tr. 9791). For example, there are several standards for cellular telephones, but each type of cellular telephone can communicate with the other types. (Rapp, Tr. 9791).

Response to Finding No. 1510: Complaint Counsel does not disagree.

1511. Compatibility requirements in the DRAM industry are not high. (Rapp, Tr. 9793). Although DRAM must be compatible with other components in a particular computer, a computer with one type of DRAM can communicate with a computer with another type of DRAM. (Rapp, Tr. 9793-94). This means that network effects in the DRAM industry are weak. (Rapp, Tr. 9794).

Response to Finding No. 1511: The statement in this proposed finding that "compatibility requirements in the DRAM industry are not high" is contrary to the weight of the evidence. (CCFF 25-28, 2541-2562, 2719-2723, 3243-3249).

Furthermore, the statement in this proposed finding that "network effects in the DRAM industry are weak" is misleading because it implies that the only way compatibility requirements can be high is if a computer with one type of DRAM cannot communicate with a computer with another type of DRAM. There is substantial evidence in the record that instead network effects can take place because of the need for complementary products like chip sets. (McAfee, Tr. 11212 ("Parts compatibility plus significant complementary products can lead to high compatibility requirements."); CCFF 2610-2612).

1512. Because of the weakness of network effects, different DRAM standards can coexist in the market. (Rapp, Tr. 9794).

Response to Finding No. 1512: This proposed finding is contrary to the weight of the evidence for the reasons discussed in CCRF 1511.

1513. Multiple standards in fact exists in the DRAM market.

Response to Finding No. 1513: This proposed finding lacks any reference to the record. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago*

Bridge and Iron Co., Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence for the reasons discussed in CCRF 1511.

1514. Moreover, history has shown that standardization by JEDEC is neither necessary nor sufficient to ensure success in the DRAM marketplace.

Response to Finding No. 1514: This proposed finding lacks any reference to the record. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence for the reasons discussed in CCRF 1511.

1515. Standardization by JEDEC is not necessary for marketplace success. For instance, the latest generation of Video RAM was not standardized by JEDEC yet gained market success. Samsung actually brought the technology to JEDEC for standardization, but JEDEC refused to consider it. (Prince, Tr. 9021). Samsung produced the product anyway, and it became a high volume DRAM product. (Prince, Tr. 9021-22).

Response to Finding No. 1515: The statement in this proposed finding that "the latest generation of Video RAM was not standardized by JEDEC yet gained market success" ignores substantial evidence in the record that it is not a high volume DRAM product. Video RAM has never obtained a significant percentage of the DRAM market. (RPF 1268-1275).

Furthermore, this proposed finding is incomplete because it omits testimony by Dr. Prince that de facto standards rarely succeed in the DRAM market. (Prince, Tr. 9022 ("So if you provide the user community what it wants, periodically a de facto standard happens, not very often.").

This proposed finding also ignores substantial evidence in the record that every high volume DRAM commodity DRAM other than RDRAM in the past 10 to 15 years has resulted from JEDEC standard-setting work. (Prince, Tr. 9020-9021; CCFF 259, 2904).

1516. Similarly, reduced latency DRAM ("RLDRAM") was developed and produced by Infineon and Micron without any involvement by JEDEC. (Bechtelsheim, Tr. 5965-66).

Response to Finding No. 1516: This proposed finding ignores substantial evidence in the record for the reasons described in CCRF 1515.

Furthermore, the statement in this proposed finding that RLDRAM was developed and produced by Infineon and Micron without any involvement by JEDEC is not supported by the cited testimony.

This proposed finding also ignores substantial evidence in the record that every high volume DRAM commodity DRAM other than RDRAM in the past 10 to 15 years has resulted from JEDEC standard-setting work. (Prince, Tr. 9020-9021; CCFF 259, 2904).

1517. Standardization by JEDEC is also insufficient for marketplace success. For example, JEDEC standardized Burst EDO, a technology brought to JEDEC by Micron (JX 23 at 68), yet it failed in the marketplace. (Williams, Tr. 873). Failure occurred despite the fact that Micron rigorously promoted the technology. (Williams, Tr. 822-24).

Response to Finding No. 1517: This proposed finding ignores substantial evidence that other JEDEC-compliant DRAMs succeeded in the DRAM market over Burst EDO. Burst EDO was introduced in the mid-1990s. (Williams, Tr. 824). The weight of the evidence is that EDO, the DRAM standard that came before Burst EDO was a JEDEC standard. (Prince, Tr. 9021). The DRAM standard that followed EDO rather than Burst EDO was JEDEC-compliant SDRAM. (Prince, Tr. 9020-9021).

1518. The publication of JEDEC's SDRAM standard was insufficient to ensure market success or even interoperability. The JEDEC SDRAM standard was not sufficiently comprehensive; because of this, SDRAM products made by one DRAM manufacturer were not compatible with those produced by another. (MacWilliams, Tr. 4908).

Response to Finding No. 1518: Complaint Counsel does not disagree

1519. Prompted by these incompatibilities, Intel - not JEDEC - developed the "PC SDRAM" standard in 1996. (MacWilliams, Tr. 407-09). As stated in that standard, "The objective of this document is to define a *new Synchronous DRAM specification* ('PC SDRAM') which will remove extra functionality from the current JEDEC standard SDRAM specification, so that it will be a 'fully compatible' device among all vendor designed parts." (RX 2104-14 at 9) (emphasis added).

Response to Finding No. 1519: This proposed finding is misleading because it omits testimony that since 1996, the DRAM specifications were developed by JEDEC - not Intel. (MacWilliams, Tr. 4914).

Furthermore, the statement in this proposed finding that "Intel - not JEDEC - developed the "PC SDRAM" standard in 1996" ignores substantial evidence in the record that Intel did not develop the PC-100 specification by itself, but instead did so based on the JEDEC SDRAM standard and in partnership with the DRAM industry. (RX0805 at 8 ("Intel is working with DRAM leaders to develop specification for 100 MHz DRAM part and DIMM to support 440BX chipset.")).

1520. The Intel PC SDRAM specification set forth what would become the industry standard for PC100 SDRAM. (MacWilliams, Tr. 4908). For instance, Compaq used Intel PC100 SDRAM compliant parts for its products. (Gross, Tr. 2350-51). Similarly, AMD referred to the Intel PC SDRAM specification when designing its chipsets. (Polzin, Tr. 4010-11).

Response to Finding No. 1520: The statement in this proposed finding that the "Intel PC SDRAM specification set forth what would become the industry standard for PC100 SDRAM" is not supported by the cited testimony. The PC-100 specification was not a DRAM standard, but a specification. The technologies used in the standard were set by JEDEC. (MacWilliams, Tr. 4910-4911).

Furthermore, this proposed finding is incomplete because it omits testimony by Mr. Polzin that the PC-100 specification was only one of the specifications that AMD used to develop its

chipsets. (Polzin, Tr. 4010 ("Probably among others we used this, yeah, among other specifications this is probably one we looked at, yeah.")).

1521. The Intel PC SDRAM specification later set forth the industry standard for PC66 SDRAM. (MacWilliams, Tr. 4908; RX 2104-14 at 60-61). Compaq, for example, used Intel PC66 SDRAM compliant parts for its products. (Gross, Tr. 2348-49).

Response to Finding No. 1521: The statement in this proposed finding that the "Intel PC SDRAM specification later set forth the industry standard for PC66 SDRAM" is not supported by the cited testimony or document.

Furthermore, the statement in this proposed finding that "Compaq, for example, used Intel PC66 SDRAM compliant parts for its products" is incomplete because it omits testimony by Ms. Gross that she is unaware of who developed the specifications that Compaq uses. (Gross, Tr. 2361 ("I believe that JEDEC was involved in SDRAM standards, but frankly, I personally don't get involved in who establishes the standards as much as the fact that there is a standard, and I believe that JEDEC and Intel are the only two sources of DRAM standards historically.")).

1522. The PC133 SDRAM standard was developed by yet another route. In that case, DRAM manufacturers and PC OEMs developed the specification. (MacWilliams, Tr. 4912-13; CX 2560 at 1). The PC133 SDRAM standard was later incorporated into the Intel PC SDRAM standard. (RX 2104-14 at 7 (document revision history shows addition of standards for 133MHz SDRAM); MacWilliams, Tr. 4908). Again, Compaq used the Intel PC133 SDRAM compliant DRAM for its products. (Gross, Tr. 2353).

Response to Finding No. 1522: The statement in this proposed finding that "Compaq used the Intel PC133 SDRAM compliant DRAM for its products" is incomplete for the reasons described in CCRF 1521.

1523. Intel's setting of the PC SDRAM standard demonstrates that there are powerful forces in the DRAM industry that affect DRAM standards in a de facto rather than de jure sense. From an economic perspective, Intel can, outside of a standard setting body, create specifications or specification addendums that become the industry standard. (Rapp, Tr. 9797). Formal standard setting is therefore not the only way in which an iteration of DRAM can become prominent. (Rapp, Tr. 9798).

Response to Finding No. 1523: This proposed finding is misleading because the statements that "Intel's setting of the PC SDRAM standard..." and "Intel can, outside of a standard setting body, create specifications or specification addendums that become the industry standard" are not accurate. The weight of the evidence is that Intel had not set the DRAM standards but rather has occasionally added specifications to that standard. Furthermore, the weight of the evidence is that each of the technologies at issue in this case is part of the SDRAM or DDR SDRAM standards because they were adopted by JEDEC. (MacWilliams, Tr. 4910 ("Q. Why is programmable CAS latency specified as part of the PC100 specification? A. Because it was already there in the SDRAM parts. That was a previous feature that was balloted in JEDEC and approved.")).

1524. It is sometimes the case, but not always, that formal standard setting may create market power. (Rapp, Tr. 9798-99). Formal standard setting may create market power when (1) there are high compatibility requirements, (2) the standard setting body is faced with several technologies that are more or less equivalent in cost-performance terms, and (3) standard setting elevates one of those technologies above the others. (Rapp, Tr. 9799-800). Where compatibility requirements are not high and there may exist more than one standard, then little or no market power is gained through standard setting. (Rapp, Tr. 9800).

Response to Finding No. 1524: Complaint Counsel does not disagree that this proposed finding describes the opinions of Dr. Rapp.

However, this proposed finding is vague and potentially misleading because the phrase "high compatibility requirements" is undefined. Depending on the meaning of that phrase, this proposed finding may also be misleading.

1525. In contrast, where one technology is superior to the alternatives then that technology would have been selected and become the *de facto* standard had the market been allowed to operate. Under these circumstances, formal standard setting does not add any market power. (Rapp, Tr. 9800-01). The market power of the technology is due to its superiority. (Rapp, Tr. 9801).

Response to Finding No. 1525: This proposed finding is unreliable because it is based on the assumption that had the market been allowed to operate then "where one technology

is superior to the alternatives then that technology would have been selected." This assumption is not supported by any record evidence. Furthermore, there is substantial evidence in the record that the DRAM industry does not work this way (CX2315 at 2 ("[H]istory has shown time and time again technical superiority does not win.")).

1526. Rambus did not obtain any additional market power due to any alleged failure to disclose its intellectual property interests before standardization by JEDEC (i.e., *ex ante*) because the Rambus technologies were superior in cost-performance terms and compatibility requirements were not so strong that alternatives could not have been employed. (Rapp, Tr. 9901-02). Standardization of the Rambus technologies by JEDEC, therefore, did not reduce the substitution possibilities of alternatives, and Rambus's market power was unchanged by formal standard setting by JEDEC. (Rapp, Tr. 9902).

Response to Finding No. 1526: The statement in this proposed finding that "Rambus did not obtain any additional market power due to any alleged failure to disclose its intellectual property interests before standardization by JEDEC (i.e., *ex ante*) because the Rambus technologies were superior in cost-performance terms and compatibility requirements were not so strong that alternatives could not have been employed" is contrary to the weight of the evidence. (CCFF 2102-2414, 2763-2821, 2856-2884; CCRF 969-988, 1125-1140, *see* RX0868 at 7 (The Value of an Interface: compatibility across vendors, innovation within the bounds of compatibility is the best value-added opportunity, proven model in the industry.)).

The statement in this proposed finding that "[s]tandardization of the Rambus technologies by JEDEC, therefore, did not reduce the substitution possibilities of alternatives, and Rambus's market power was unchanged by formal standard setting by JEDEC" is contrary to the weight of the evidence. (CCFF 2500-2584, 2901-2904, 2914-2958; CCRF 1259-1360).

1527. Rambus did not obtain or retain any additional market power due to any alleged failure to disclose its intellectual property interests after standardization by JEDEC (i.e., ex post) because, even after standardization, switching costs would not have prevented a shift to an available technology that was as good or better than Rambus's technology. (Rapp, Tr. 9902-03).

Response to Finding No. 1527: This proposed finding is contrary to the weight of the evidence. (CCFF 2500-2584, 2901-2904, 2914-2958; CCRF 1259-1360).

1528. From an economic point of view, both consumers and manufacturers were better off by selecting the four Rambus features incorporated in DDR and paying royalties to Rambus rather than selecting any combination of the "commercially viable" alternatives identified by Complaint Counsel's economic expert. (Rapp, Tr. 9858-59).

Response to Finding No. 1528: This proposed finding is contrary to the weight of the evidence. (CCFF 2102-2414, 2763-2821, 2856-2884; CCRF 969-988, 1125-1140).

1529. Complaint Counsel's economic expert did not offer testimony that refuted these conclusions. While he claimed that Rambus's market power was increased because "commercially viable" alternatives were eliminated, the alternatives to Rambus's technologies that Complaint Counsel's economic expert identified as "commercially viable" are not close economic substitutes because of the cost-performance distance between those alternatives and Rambus's technologies. (Rapp, Tr. 9861-62).

Response to Finding No. 1529: This proposed finding is not accurate because Professor McAfee did offer testimony to refute these conclusions. (CCFF 2763-2821, 2856-2884, 2901-2904, 2914-2958).

1530. JEDEC's inclusion within its standards of the four technologies at issue here did not, therefore, enhance Rambus's market power.

Response to Finding No. 1530: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence as described in CCRF 1527-1529.

2. The Alleged Conduct Did Not Enhance Rambus's Market Power Because JEDEC Would Have Selected Rambus's Technologies Even With The Additional Disclosure.

1531. The evidence shows that even if Rambus had made the additional disclosures that Complaint Counsel allege should have been made, JEDEC still would have included the four

technologies in its standards, and JEDEC members would have ended up paying the same royalties. This shows that the alleged conduct did not enhance Rambus's market power or cause harm to competition.

Response to Finding No. 1531: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.,* Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (CCRF 720-763, 1147-1182).

1532. First, the evidence shows that the four Rambus technologies were the technologies of choice throughout the relevant time period and that a rational manufacturer or a rational JEDEC would have selected the Rambus technologies. (Rapp, Tr. 9903). The additional disclosures that Complaint Counsel allege Rambus should have made would not have affected the outcome because there were no cost-performance equivalent technologies to the two Rambus technologies incorporated in SDRAM or to the four Rambus technologies incorporated in DDR. (Rapp, Tr. 9907-08). Had the allegedly required additional disclosures occurred, rational manufacturers and a rational standard setting organization would have adopted the Rambus technologies for both SDRAM and DDR. (Rapp, Tr. 9908-09).

Response to Finding No. 1532: This proposed finding is contrary to the weight of the evidence. (CCFF 2102-2414, 2763-2821, 2856-2884; CCRF 969-988, 1125-1140, 1219).

1533. It therefore follows that competition has not been adversely affected by Rambus's alleged failure to disclose. (Rapp, Tr. 9908-09). It is worth noting on this issue that Complaint Counsel's economic expert testified that the alleged conduct of Rambus has had no impact on DRAM prices, no effect on consumers, and no effect on the final PC market as of the time of trial (over three and one-half years after Rambus began asserting its patents). (McAfee, Tr. 7565-66)).

Response to Finding No. 1533: The statement in this proposed finding that it "therefore follows that competition has not been adversely affected by Rambus's alleged failure to disclose" is contrary to the weight of the evidence for the reasons described in CCRF 1152.

Furthermore, the statement in this proposed finding that Professor McAfee testified that "[T]he alleged conduct of Rambus has had no impact on DRAM prices, no effect on consumers, and no effect on the final PC market as of the time of trial (over three and one-half years after

Rambus began asserting its patents)" is incomplete. Professor McAfee testified that the effect of the Rambus lawsuits on final consumers could only happen in the long-run because of the effect of the lawsuits on supply. (McAfee, Tr. 7175-7176 ("As an economist, I expect [the Rambus assertions of patent infringement] to have a long-run effect. The nature of DRAM production is such that even a 5 percent royalty would not typically cause them to reduce their current production, and as a result you wouldn't expect to see the current prices of DRAM rise even in the face of a 5 percent royalty. On the other hand, that such a royalty does produce a disincentive to further plant building, to going to a larger wafer size and other means of producing more output in the future, and as a result you would expect in the long run that those royalty costs would be passed on to consumers and hence have the effect of lowering output in the downstream DRAM market.")).

Professor McAfee's opinion that the price of DRAMs is likely to eventually reflect royalty payments made to Rambus is supported by substantial record evidence. (CX0839 at 2 ("[Farhad Tabrizi] told me that they pass on license fees and royalties to their customers, and they worry that Rambus is too greedy and that will make RDRAMs too expensive."); CX2107 at 140-141 (Oh, Tr.)).

1534. The conclusion that competition has not been adversely affected by Rambus's alleged failure to disclose is bolstered by the likelihood that JEDEC would have selected Rambus's four technologies had Rambus never joined JEDEC. This demonstrates that JEDEC members, acting as rational manufacturers, would have selected Ramubus's technologies, so that standardization by JEDEC did not increase Rambus's market power. (Rapp, Tr. 9863).

Response to Finding No. 1534: This proposed finding is misleading and unreliable because it rests on the hypothesis that Rambus does not attend JEDEC. Both Professor McAfee and Professor Teece agreed that from the standpoint of economic theory and methodology, in formulating a but-for world, the standard methodology is to conceptualize a world in which nothing changes except the challenged conduct does not occur. That is, the defendant, conforms its

conduct in the but-for world with what it is challenged for not having done in the real world. (Teece, Tr. 10676-10677; *see also* CCFF 3018-3019 for similar testimony by Professor McAfee).

1535. Second, a decision analysis considering both JEDEC's and Rambus's economic incentives shows that JEDEC would have adopted Rambus's technologies. The analysis also shows that once JEDEC selected Rambus's technologies, there would not have been any *ex ante* negotiations. That being the case, licenses to Rambus's technologies would have been negotiated *after* the SDRAM and DDR standards were set and *after* Rambus's patents issued. In other words, the license negotiations would have occurred in the but-for world at the same point in time that they occurred in the real world.

Response to Finding No. 1535: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore this proposed finding is contrary to the weight of the evidence. (CCFF 2441-2464, 3012-3044; CCRF 1147-1182).

1536. Finally, the evidence shows that Rambus's royalties are reasonable and nondiscriminatory. The royalty rates are those that would have been agreed to by a willing licensee and a willing licensor.

Response to Finding No. 1536: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. (CCFF 2441-2464; CCRF 1361-1422).

1537. Because the but-for-world outcome is the same as the actual world outcome, Rambus's alleged conduct caused it to gain no additional market power. (Teece, Tr. 10312-13).

Response to Finding No. 1537: This proposed finding is contrary to the weight of the evidence. (CCFF 3012-3044; CCRF 1147-1182).

3. Rambus's Alleged Failure To Disclose Did Not Enhance Rambus's Market Power Because Intel, Not JEDEC, Chose The Memory Device Currently In Widespread Use.

1538. Complaint Counsel theorize that JEDEC standardization of the four technologies at issue gave them market power. In fact, the evidence shows that it was Intel, not JEDEC, that chose the memory device currently in widespread use.

Response to Finding No. 1538: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is contrary to the weight of the evidence. The current SDRAM and DDR SDRAM standards were set by JEDEC. (CCFF 500-658). Intel did choose RDRAM as its next generation DRAM standard in the mid-1990s. However, the market share of RDRAM never exceeded 13% of the market according to Dr. Rapp's own testimony. (RPF 1268-1275).

1539. In the 1995-1996 time period, Intel spent about a year exploring various alternatives for the next generation DRAM. (MacWilliams, Tr. 4800-01). Intel looked at EDO, SDRAM, DDR, SyncLink, and Rambus. (MacWilliams, Tr. 4800-01). Other than these alternatives, "the memory vendors didn't have any other good ideas." (MacWilliams, Tr. 4800-01).

Response to Finding No. 1539: Complaint Counsel does not disagree.

1540. An internal Intel document written by Peter MacWilliams explained that the DRAM manufacturers were not focused on improving DRAM technology: "Up to this point in time [(Q395)], memory vendors were stric[t]ly focus[]ing on lowering costs and increasing density; Intel felt the memory vendors needed to get more focused on increasing access speed." (RX 1532 at 1).

Response to Finding No. 1540: The statement in this proposed finding that "[a]n internal Intel document written by Peter MacWilliams explained that the DRAM manufacturers were not focused on improving DRAM technology" is misleading. The cited evidence states that

the DRAM vendors in 1995 were focused on lowering costs and increasing densities but were not sufficiently focused on improving access speed to suit Intel's needs. (RX1532 at 1).

1541. Intel saw a growing performance gap in the mid-1990's between CPU performance and DRAM performance. (RX 868 at 3). After examining the alternatives for a year, Intel chose RDRAM to be its next generation DRAM technology. (MacWilliams, Tr. 4800-01).

Response to Finding No. 1541: Complaint Counsel does not disagree.

1542. Intel chose RDRAM because of the need for higher bandwidth for use with faster CPUs and the need to satisfy memory needs driven by more I/O demands and new applications. (RX 904 at 5-6; *see also* RX 805 at 2 (December 1996 Intel document reciting need for increased bandwidth driven by memory intensive applications such as visual computing and noting that Intel was looking for technology beyond 100 MHz SDRAM)).

Response to Finding No. 1542: Complaint Counsel does not disagree.

1543. Intel's choice of RDRAM was significant. As Richard Heye of AMD - Intel's competitor in the microprocessor market - explained, in the late 1990's AMD believed that RDRAM would become the next volume memory product (even though the technology was "revolutionary") because it had been chosen by Intel: "And given that, you know, Intel, who owns 80 percent of the market, really put his wood behind the arrow, so to speak, on Rambus, you know, they had talked about the customers, well our customers were saying, hey, you ought to use Rambus, and we talked to the memory vendors. And the memory vendors were saying, you know what, Rambus, it's a revolutionary change, not evolutionary, but, you know, that's the way the industry is going, that's the way we're going to go, and Rambus is it." (Heye, Tr. 3685).

Response to Finding No. 1543: This proposed finding is incomplete because it omits testimony by Mr. Heye that he believed that, notwithstanding the support of Intel, RDRAM was never going to become the commodity DRAM, but instead JEDEC's DDR SDRAM was going to become the next commodity DRAM. (Heye, Tr. 3704 ("Through all the information I was collecting throughout the industry, it was my personal belief that Rambus was going to fail as a commodity part, and that ultimately even Intel would have to go DDR, and that AMD should be the first – should drive the DDR standard and not get tied up with the Rambus memory.")).

1544. Steve Polzin of AMD concurred. He testified that it was important to AMD that Intel chose RDRAM because Intel's selection would make RDRAM a *de facto* standard: "[Intel]drove the volume, and if the volume DRAM was Rambus, that would become the commodity part, and we had to remain competitive in terms of both performance and cost, and if

the indications were most of the DRAMs to be built in the world were going to be Rambus DRAMs, we better be compatible with them." (Polzin, Tr. 3941-42).

Response to Finding No. 1544: This proposed finding is misleading to the extent it is intended to convey that RDRAM became the dominant DRAM standard. (CCRF 1538).

1545. Intel's selection of RDRAM was also significant to the PC OEMs. For example, Compaq, one of the largest producer of personal computers in the world stated in a November 1998 Compaq Memory Update states that Compaq was planning to incorporate RDRAM into all Compaq products. (RX 1302 at 8). Jacquelyn Gross, the Director of Memory Procurement at Compaq (Gross, Tr. 2265), testified that Compaq was planning to transition all of its products - desktops, workstations, etc. - to RDRAM at rate higher than it had ever changed memory technologies before. (Gross, Tr. 2324-27). As described in Compaq's documents, this was the "[m]ost aggressive, cross divisional memory technology shift ever planned at Compaq." (RX 1302 at 8). This was planned, even though Compaq considered RDRAM to be "revolutionary." (Gross, Tr. 2327).

Response to Finding No. 1545: This proposed finding is misleading to the extent it is intended to convey that RDRAM became the dominant DRAM standard. (CCRF 1538).

Furthermore, the statement in this proposed finding that "Compaq, one of the largest producer of personal computers in the world stated in a November 1998 Compaq Memory Update states that Compaq was planning to incorporate RDRAM into all Compaq products" is not supported by the cited evidence.

Furthermore, the statement in this proposed finding that "Jacquelyn Gross, the Director of Memory Procurement at Compaq ..., testified that Compaq was planning to transition all of its products - desktops, workstations, etc. - to RDRAM at rate higher than it had ever changed memory technologies before..." is not supported by the cited testimony (Gross, Tr. 2326 ("Q. And finally, in the fifth bullet point, you refer to 'all other product lines looking at implementation in 2000.' Does that mean you were planning to introduce RDRAM in all of your other product lines in 2000? A. Based on the consideration that it would become the standard, yes, it was considered that that was a possibility.")).

1546. Similarly, an October 1998 internal presentation reflects Compaq's sentiment at the time that "Rambus is the clear next generation memory." (RX 1287 at 4). As Ms. Gross explained, the reason for this belief was that Intel had told Compaq that it was going to produce chip sets for RDRAM. (Gross, Tr. 2317-18). This was important to Compaq because 90% of Compaq's PC applications used Intel chipsets. (Gross, Tr. 2317-18).

Response to Finding No. 1546: This proposed finding is misleading to the extent it is intended to convey that RDRAM became the dominant DRAM standard. (CCRF 1538).

1547. Both Intel and the OEMs recognized that in order for RDRAM to gain widespread market acceptance, the DRAM manufacturers needed to produce RDRAM in high volumes, which would drive down the price. As Peter MacWilliams of Intel explained, it was very important to the success of RDRAM that it be produced in volume so that its price be reduced:

> "Q. Okay. And how important was the price of RDRAM to its success during the time period of 1998 through 2001?
> A. It was very important. The price of RDRAM needed to come down to be very close to what the volume memory technology was in order for it to transition to be the mainstream technology, and it can be higher priced at introduction, it can be higher priced for the first part of the ramp, but OEMs had to have confidence that it was going to come down in order to make a larger commitment to it. So it became the determining factor as to how big the volume could be."
>
> Q. And one of the factors going into the price of RDRAM was the number of manufacturers who would produce it; is that right?
> A. Yes.
>
> Q. And one of the factors also would be whether the volume of the RDRAM being produced was sufficient to meet all of the demand?
> A. Yes."

(MacWilliams, Tr. 4933-34).

Response to Finding No. 1547: This proposed finding is misleading because it omits other factors that were necessary for RDRAM to gain widespread market acceptance. These factors included the need for reasonable royalties on RDRAM, the cost of manufacture of RDRAM being within 5% of the cost to manufacture SDRAM, and RDRAM technology being sufficiently stable and robust to permit design and manufacture of supporting chipsets. In fact, RDRAM failed to gain widespread acceptance in the marketplace because Rambus's royalty rates were perceived

to be too high, (CCFF 1814-1837), the cost to manufacture RDRAM was too high, (CCFF 1838-1866), and technical problems caused the failure of Intel's Camino chipset. (CCFF 1877-1910).

4. The DRAM Manufacturers Acknowledged – By Undertaking Extraordinary Efforts To Slow Or Block RDRAM's Market Acceptance – That It Is Intel's Decisionmaking, Not JEDEC Standardization, That Most Strongly Influences Marketplace Success.

1548. The DRAM manufacturers were well aware of Intel's power to create a *de facto* industry standard in selecting the RDRAM device. They also recognized that JEDEC standardization of a competing device would mean nothing if Intel did not change its course, and they knew that "Intel will not change course unless Rambus fails." (RX 870 at 1). Finally, the manufacturers recognized that they could not affect Intel's decision without concerted action; they "need[ed] some united strategy." (RX 808 at 2). As a result, both before and after Intel announced its selection of RDRAM, Intel faced resistance – organized, concerted resistance -- from the DRAM manufacturers.

Response to Finding No. 1548: RPF 1548 is misleading. Intel does play a significant role in the selection of future architectures. (CCFF 1576). Intel does not, however, "create" standards in the sense of selecting the technologies to be included in those architectures, except to the extent that Intel itself is a member and participates actively in JEDEC. Furthermore, Intel's influence is limited to the PC space. Even after Intel's decision to exclusively promote RDRAM in the PC space, JEDEC and SyncLink continued to develop technologies that could serve applications in which RDRAM was not an option, such as servers and graphics applications. *See* CCFF 1556. Finally, RPF 1548 is contrary to the weight of the evidence because Rambus has failed to prove the existence on any illegal conspiracy amongst DRAM manufacturers. In this regard, it also is important to note that witnesses from a cross-section of the industry, including customers, chipset vendors, and even Intel itself, testified during the hearing concerning the development and importance of JEDEC standards (*see* CCFF 258-67), the application of JEDEC's patent disclosure policy (*see* CCFF 318-434), and the reasons why Rambus's technology was not preferred. (*see* CCFF 1814-94). These witnesses confirmed the importance of JEDEC standards in

the industry, the high cost of manufacturing RDRAM and the failure of RDRAM being caused by its technical problems and the failure of Intel's Camino chipset. CCFF 1800-1924.

1549. There has been substantial disagreement among the parties about the relevance in this case of evidence of concerted action by DRAM manufacturers that was intended to limit or prevent the marketplace success of RDRAM. While such evidence may not be *dispositive* of any material issue, it is *relevant* for at least four reasons.

Response to Finding No. 1549: RPF 1549 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1550. First, as noted above, it tends to show that it is Intel's selection, not JEDEC's standardization, that influences marketplace success for a DRAM device or technology.

Response to Finding No. 1550: RPF 1550 is contrary to the weight of the evidence because there is no evidence that Intel or anyone else has ever created a *de facto* commodity DRAM standard outside of JEDEC. *See* CCFF 258-67. Indeed, JEDEC standards have dominated the industry for at least the past ten years. *See* CCFF 267.

1551. Second, it tends to rebut Complaint Counsel's argument that Rambus's motivation in asserting its patents in 1999 and 2000 should be viewed with suspicion because the assertion of those patents came after RDRAM had supposedly failed to compete on the merits because of its (allegedly) inherently high manufacturing costs.

Response to Finding No. 1551: RPF 1551 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Complaint Counsel submits that RDRAM's failure was due to Rambus's royalties, the high cost of producing RDRAM, and technical problems leading to the failure of Intel's Camino chipset. CCFF 1800-

1924. None of the reasons relate to any alleged conspiracy by DRAM manufacturers. Further, Rambus's reasons for playing its "IP card" are well documented. *See* CCFF 1911-24.

1552. Third, it tends to place in context the testimony of the executives and employees of DRAM manufacturers whose words and deeds are reflected in the evidence in question. Their interest in a finding that RDRAM failed on its merits, rather than as a result of collusive action, is likely to be affected by their participation in such action.

Response to Finding No. 1552: RPF 1552 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, to the extent the credibility of testimony is based on financial interest in the outcome of this case, Complaint Counsel submits that there is no company that has a larger stake in the outcome of the case than Rambus. Moreover, the employees of large DRAM manufacturers have little (if any) stake in the outcome, whereas many Rambus officers and employees have large shareholdings in Rambus and thus have a direct financial interest in the outcome of this case. The credibility of Rambus witnesses, therefore, should be viewed accordingly.

1553. Finally, while Complaint Counsel necessarily have focused their efforts on advancing the allegations made in the Complaint, this Court has a broader responsibility to the Commission and the public. If this Court receives evidence of collusive action by competitors that may have had the effect of reducing consumer choice, raising prices, or eliminating a superior technology, it is appropriate to bring that evidence to light. *See* FTC Act, 15 U.S.C. §§ 43, 45.

Response to Finding No. 1553: RPF 1553 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1554. With these points in mind, the Court has considered the evidence presented and finds reason to believe that the DRAM manufacturers: (1) were alarmed by the possibility that Intel's selection of the RDRAM would lower their profits and cause them to lose control of future DRAM design and implementation; (2) joined together in various consortia with the intention of

impairing or blocking the successful marketplace launch of RDRAM; and (3) agreed to steps that resulted in lower production and higher prices of RDRAM, thus limiting and ultimately preventing RDRAM's success.

Response to Finding No. 1554: RPF 1554 is contrary to the weight of the evidence because Rambus has not proven that the "various consortia" were not legitimate joint ventures created to share resources and expertise with the goal of developing new products. In addition, these consortia typically involved a very limited segment of each DRAM supplier's memory resources. Nevertheless, because RDRAM lacked functionality for certain applications, *e.g.*, servers and graphics, DRAM manufacturers and their customers required a different solution. Meanwhile, during the entire relevant time, DRAM manufacturers continued to devote significantly greater resources to developing RDRAM for the Intel PC market. *See* CCFF 1581,1800-13. Further, Respondent has not proven that there was any agreement between DRAM manufacturers with respect to the production of RDRAM. Respondent has not cited any evidence indicating that any manufacturer refused to produce RDRAM or otherwise altered its production plans in response to any agreement.

1555. In September 1996, for example, Hyundai executive and SyncLink Consortium chairman Farhad Tabrizi wrote an e-mail entitled "Emergency request for help!" that expressed a concern that "the real motive of Intel is to control DRAM manufacturers . . . ." (RX 778 at 1). According to Mr. Tabrizi, Intel's actions would give it "control of DRAMs and other CPU makers. We will become a foundry for all Intel activities and if Intel would like and desires to do business with us then we may get a small share of the their total demand." (RX 778 at 1).

Response to Finding No. 1555: RPF 1555 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. There is no evidence that DRAM manufacturers limited the production of RDRAM. Indeed, the evidence shows that notwithstanding the high costs of production, (*see* CCFF 1838-61), unprecedented royalty structure, (*see* CCFF 1814-24) and continuous technical difficulties in bringing RDRAM to market (*see* CCFF 1877-94), DRAM manufacturers continued to prepare for volume production of

RDRAM until Intel withdrew its support. (CCFF 1895-1910). For example, Mr. Tabrizi testified that it was his responsibility to combine the post-merger DRAM operations of Hyundai and Lucky Goldstar. (Tabrizi, Tr. 9112). His recommendations to the head of Hyundai's research and development department, Dr. Kim, was to combine the merged firm's RDRAM operations in one location and put the best of both companies engineers to work on RDRAM using the most advanced process technology then available. (RX1487 at 6; Tabrizi, Tr. 9112-15). Furthermore, notwithstanding Mr. Tabrizi's personal efforts to lobby for a role for SyncLink, Hyundai's president, Sang Park, ordered Hyundai to give Rambus the highest priority. (Tabrizi, Tr. 9108 ("JUDGE McGUIRE: Now, what are you talking about when you say Sang Park, our new president, had joined our company and put Rambus as the highest priority and allocated many dollars to Rambus? What context are you talking about? What was he doing in that time period? THE WITNESS: So we get together for a product planning meeting and we decide the priority of the product, and at that time Samsung was one of the main suppliers for Rambus and Sang Park wanted to compete with Samsung head to head . . . So he'd ordered our factory to load all of our factory with Rambus and he wanted to compete with Samsung. He said if Samsung is enjoying Rambus prices are high, I want to share that.")).

Finally, the cited document relates to Mr. Tabrizi's efforts on behalf of the SyncLink Consortium. The SyncLink Consortium was a joint venture created to share resources and expertise with the goal of developing the SyncLink DRAM. *See* CCFF 1554-66; *see also* Antitrust Guidelines for Collaborations Among Competitors Issued by The Federal Trade Commission and The U.S. Department of Justice, Section 1.2 at 4 (April 2000) (collaborations involving "an efficiency enhancing integration of economic activity" are accorded rule of reason analysis). The SyncLink Consortium was an outgrowth of the RamLink project which had been sponsored by the IEEE. *See* CCFF 1501-20.

1556. Mr. Tabrizi concluded his September 1996 e-mail by writing, "I urge you to please educate others and get their agreement to say 'NO TO RAMBUS AND NO TO INTEL DOMINATION.'" (RX 778 at 1).

Response to Finding No. 1556: RPF 1556 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. *See* CCRF 1555.

1557. Mr. Tabrizi sent this email to one of his competitors, Jim Sogas at Hitachi, for comments. (Tabrizi, Tr. 9035). Prior to trial, he had testified that he was trying to get agreement from other DRAM manufacturers to say "no" to Rambus and "no" to Intel domination. (Tabrizi, Tr. 9038). At trial, however, he claimed that he could not recall sending the e-mail to other DRAM companies. (Tabrizi, Tr. 9037-38).

Response to Finding No. 1557: RPF 1557 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. With respect to Hitachi, there is no evidence that it said "No" to Intel or to Rambus. Instead, the evidence demonstrates that Hitachi considered itself a newcomer to SyncLink and "an equal distance from [SyncLink] and Rambus II." (CX2250 at 1) With respect to Hyundai, as late as June 2000, Hyundai's CEO was ordering the company to load all of Hyundai's DRAM production lines with RDRAM in order to compete head-to-head with Samsung. (Tabrizi, Tr. 9107-08 (discussing June 8, 2000, email exchange with Sang Park)). *See also* CCRF 1555.

1558. In December 1996, at a SyncLink Consortium meeting attended by various manufacturers, Mr. Tabrizi stated that "[m]any suppliers are paranoid over the prospect of a single customer, e.g., Intel, having control of market. We can't resist such a possibility individually. We need some united strategy." (RX 808 at 2).

Response to Finding No. 1558: RPF 1558 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. As the DRAM industry learned of Intel's decision to exclusively support RDRAM for PC main memory, customers and manufacturers decided to continue development of alternatives that could be used in

certain applications in which RDRAM was inadequate, including servers and graphics. *See* CCFF 1573-75.

Finally, the cited document relates to Mr. Tabrizi's efforts on behalf of the SyncLink Consortium. The SyncLink Consortium was a joint venture created to share resources and expertise with the goal of developing the SyncLink DRAM. *See* CCFF 1554-66; *see also* Antitrust Guidelines for Collaborations Among Competitors Issued by The Federal Trade Commission and The U.S. Department of Justice, Section 1.2 at 4 (April 2000) (collaborations involving "an efficiency enhancing integration of economic activity" are accorded rule of reason analysis). The SyncLink Consortium was an outgrowth of the RamLink project which had been sponsored by the IEEE. *See* CCFF 1501-20.

1559. At that same meeting, the assembled manufacturers agreed to hold a meeting of DRAM manufacturer executives in Japan in January 1997. (Tabrizi, Tr. 9041). Prior to the January 1997 meeting of executives, Mr. Tabrizi sent an email to other DRAM manufacturers that stated that the "Intel decision to go on a Rambus route was pure political and domination and control over the DRAM suppliers and not technical." (RX 802 at 3; Tabrizi, Tr. 9041-42). He then urged a unified effort to prevent Intel from gaining "control": "As I have mentioned many times before, Intel does not make DRAMs, we do. And if all of us put our resources together, we do not have to go on this undesirable path. The path of control and domination by Intel." (RX 802 at 3). He pleaded with the DRAM manufacturers to "stick together on this matter." (RX 802 at 3; Tabrizi, Tr. 9042-43).

Response to Finding No. 1559: RPF 1559 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. The purpose of holding a meeting of DRAM executives in after Intel's decision to exclusively support RDRAM for PC main memory was to try to persuade the executives to continue providing some level of support for SyncLink. (Tabrizi, Tr. 9138 ("After the Intel announcement, I had to decide either to stop the efforts or to get some level of support from the DRAM companies to continue at least our development activity, standard activity.")). During that period of time Hyundai, for

example, had only one or two engineers devoted to SyncLink projects compared to at least 50 devoted to developing Rambus. (Tabrizi, Tr. 9136-37).

Finally, the cited document and testimony relates to Mr. Tabrizi's efforts on behalf of the SyncLink Consortium. The SyncLink Consortium was a joint venture created to share resources and expertise with the goal of developing the SyncLink DRAM. *See* CCFF 1554-66; *see also* Antitrust Guidelines for Collaborations Among Competitors Issued by The Federal Trade Commission and The U.S. Department of Justice, Section 1.2 at 4 (April 2000) (collaborations involving "an efficiency enhancing integration of economic activity" are accorded rule of reason analysis). The SyncLink Consortium was an outgrowth of the RamLink project which had been sponsored by the IEEE. *See* CCFF 1501-20.

1560. At the January 1997 meeting of DRAM executives, Mr. Tabrizi warned the assembled executives that if Intel succeeded in making RDRAM the next generation memory device, "DRAM manufacturers would loose control of specification and the gross margins will decline." (RX 849 at 44). Mr. Tabrizi conceded at trial that it was his view at the time that if Intel's selection of Rambus did not change, the gross margins of DRAM manufacturers would decline. (Tabrizi, Tr. 9048).

Response to Finding No. 1560: RPF 1560 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. *See* CCRF 1559. As the record demonstrates, Intel's decision did not change until June 1999. *See* CCFF 1895. Notwithstanding Mr. Tabrizi's perception of the market, DRAM manufacturers continued to expend vast resources on developing RDRAM for the Intel PC market. *See* CCFF 1581, 1838-66.

Finally, the cited document and testimony relates to Mr. Tabrizi's efforts on behalf of the SyncLink Consortium. The SyncLink Consortium was a joint venture created to share resources and expertise with the goal of developing the SyncLink DRAM. *See* CCFF 1554-66; *see also* Antitrust Guidelines for Collaborations Among Competitors Issued by The Federal Trade

Commission and The U.S. Department of Justice, Section 1.2 at 4 (April 2000) (collaborations involving "an efficiency enhancing integration of economic activity" are accorded rule of reason analysis). The SyncLink Consortium was an outgrowth of the RamLink project which had been sponsored by the IEEE. *See* CCFF 1501-20.

1561. Tabrizi's January 1997 presentation also warned that if Rambus became the next generation memory solution, "ALL DRAM COMPANIES WILL BECOME FOUNDRIES for a single source CPU manufacturer." (RX 849 at 44). The phrase "single source CPU manufacturer" was a reference to Intel. (Tabrizi, Tr. 9046).

Response to Finding No. 1561: RPF 1561 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. *See* CCRF 1559. As the record demonstrates, Intel's decision did not change until June 1999. *See* CCFF 1895. Notwithstanding Mr. Tabrizi's perception of the market, DRAM manufacturers continued to expend vast resources on developing RDRAM for the Intel PC market. *See* CCFF 1581, 1838-66.

Finally, the cited document and testimony relates to Mr. Tabrizi's efforts on behalf of the SyncLink Consortium. The SyncLink Consortium was a joint venture created to share resources and expertise with the goal of developing the SyncLink DRAM. *See* CCFF 1554-66; *see also* Antitrust Guidelines for Collaborations Among Competitors Issued by The Federal Trade Commission and The U.S. Department of Justice, Section 1.2 at 4 (April 2000) (collaborations involving "an efficiency enhancing integration of economic activity" are accorded rule of reason analysis). The SyncLink Consortium was an outgrowth of the RamLink project which had been sponsored by the IEEE. *See* CCFF 1501-20.

1562. Micron engineer Terry Lee participated in the January 1997 DRAM executive meeting; his notes reflect that Siemens executive Dr. von Zitzewitz stated that Tabrizi's "[c]ontrol concerns are realistic." (CX 2250 at 2; Tabrizi, Tr. 9047-48). The notes also state that Dr. von Zitzewitz was "[d]isappointed with some statements accepting Rambus II. 0.1% royalty would have been OK. . . . The bottleneck of a small company is bad. Rambus is not acceptable." (CX 2250 at 2). Mr. Lee's notes were later made available to all members of the SyncLink

Consortium (which was renamed the "SLDRAM Consortium" around this time). (Tabrizi, Tr. 9050; RX 855 at 1).

Response to Finding No. 1562: RPF 1562 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. Indeed, the statement attributed to Dr. Von Zitzewitz establishes that the various manufacturers continued to pursue strategies that were in their respective unilateral best interests. Throughout Mr. Lee's notes the vast differences of opinion are readily apparent. For example, NEC "Supports Rambus . . .[and was] not in position to develop [SyncLink] yet." (CX2250 at 1). Fujitsu believed that the market for SyncLink was "unclear" and that it needed "a market in order to develop" SyncLink. (CX2250 at 1). Hitachi, a newcomer to SyncLink, considered itself to be "at an equal distance from [SyncLink] and Rambus II." (CX2250 at 1). Toshiba was very clear that they believed that three alternatives would exist in 2000, but that "development should be left up the the individual companies." (CX2250 at 2).

Finally, the cited document and testimony relates to the efforts of the SyncLink Consortium. The SyncLink Consortium was a joint venture created to share resources and expertise with the goal of developing the SyncLink DRAM. *See* CCFF 1554-66; *see also* Antitrust Guidelines for Collaborations Among Competitors Issued by The Federal Trade Commission and The U.S. Department of Justice, Section 1.2 at 4 (April 2000) (collaborations involving "an efficiency enhancing integration of economic activity" are accorded rule of reason analysis). The SyncLink Consortium was an outgrowth of the RamLink project which had been sponsored by the IEEE. *See* CCFF 1501-20.

1563. After the January 1997 DRAM executive meeting, Mr. Tabrizi set up an e-mail "reflector" so that the DRAM supplier executives – ostensibly fierce competitors – could communicate among themselves via private e-mail. (Tabrizi, Tr. 9052; RX 938 at 1).

Response to Finding No. 1563: RPF 1563 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. First, the purpose of the reflector was to provide a means for Mr. Tabrizi or other "member[s] of the consortium [to] communicate or transfer e-mails to the executive. I don't recall a single executive sending e-mails to each other. It was for me and other members to send important information to executives, not just every information." (Tabrizi, Tr. 9052).

Finally, the cited document and testimony relates to the efforts of the SyncLink Consortium. The SyncLink Consortium was a joint venture created to share resources and expertise with the goal of developing the SyncLink DRAM. *See* CCFF 1554-66; *see also* Antitrust Guidelines for Collaborations Among Competitors Issued by The Federal Trade Commission and The U.S. Department of Justice, Section 1.2 at 4 (April 2000) (collaborations involving "an efficiency enhancing integration of economic activity" are accorded rule of reason analysis). The SyncLink Consortium was an outgrowth of the RamLink project which had been sponsored by the IEEE. *See* CCFF 1501-20.

1564. Throughout 1997, 1998 and 1999, Mr. Tabrizi and others kept up regular communications about Rambus with their competitors, often sharing cost, production and planning information ordinarily maintained in confidence by true competitors. (Tabrizi, Tr. 9053; RX 916 at 1; RX 1181 at 1; RX 1155 at 1; RX 2191 at 1-2; RX 2192 at 2-3; RX 1105 at 1; RX 1386 at 1; RX 1487 at 4).

Response to Finding No. 1564: RPF 1564 is misleading and does not support the conclusion that DRAM manufacturers exchanged competitively sensitive information. RPF 1564 certainly does not support Respondent's proposed conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. *See* CCRF 1565-1602.

1565. In February 1998, for example, Jeff Mailloux of Micron wrote an email to Mr. Tabrizi stating that Mr. Mailloux had spoken to a reporter for an industry publication called EE Times. (RX 1105 at 1). Mr. Mailloux stated that "I told him that at any density and any process that is available in 1999, RDRAM is at least 30 percent cost adder for Micron," and then

encouraged Mr. Tabrizi to call the reporter with Hyundai's views. (RX 1105 at 1). Mr. Mailloux asked Mr. Tabrizi to "please visit me if I end up in jail. . . ." (*Id.*).

Response to Finding No. 1565: RPF 1565 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. First, the forwarded article obviously contained only public information. Second, there is no evidence that Mr. Mailloux shared any company confidential information with a competitor. Relative costs often are a factor in the selection of the next generation memory technology. (Rhoden, Tr. 599-600). When discussing relative cost, the DRAM industry typically uses the then-current commodity product as the baseline. (*See, e.g.,* CCFF 2641). In 1998, the baseline product would have been SDRAM. (*See, e.g.*, Lee, Tr. 6732-33). There is no evidence of any discussion of Micron's actual cost to make either SDRAM or RDRAM. RPF 1565 does not support Respondent's proposed inference that Micron discussed competitively sensitive information with its competitors.

1566. Two months later, Mr. Mailloux sent another email to Mr. Tabrizi, attaching an article in an industry publication that had been written by Mr. Tabrizi's boss at Hyundai, Mark Ellsberry. (RX 1155 at 1; Tabrizi, Tr. 9055-56). Mr. Mailloux appears to have been concerned that the article by Mr. Ellsberry was pro-Rambus. (*Id.*). His e-mail states, "Mark seems to give a message at the end here, he only refers to DDR as a 'long shot' and does not even mention SLDRAM. Hope Hyundai has not caved in to the 'dark side.'" (RX 1155 at 1).

Response to Finding No. 1566: RPF 1566 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. First, the forwarded article obviously contained only public information. Second, there is no evidence that Mr. Mailloux shared any confidential Micron information with a competitor. Third, there is no evidence that Mr. Tabrizi ever responded to this email. Finally, the substance of the public article forwarded by the email highlights the fact that manufacturers continued to act in their unilateral best interests. As RPF 1566 readily points out, Mr. Ellsberry was Mr. Tabrizi's *boss*. Notwithstanding any of Mr. Tabrizi's efforts on behalf of SyncLink, more senior executives at

Hyundai continued to pour resources behind RDRAM. Thus, Mr. Ellsberry's and Hyundai's public and internal support of RDRAM is consistent with Mr. Tabrizi's testimony concerning the disparate levels of support given RDRAM and SyncLink. *See* CCRF 1559.

Finally, the cited document and testimony relates to the efforts of the SyncLink Consortium. The SyncLink Consortium was a joint venture created to share resources and expertise with the goal of developing the SyncLink DRAM. *See* CCFF 1554-66; *see also* Antitrust Guidelines for Collaborations Among Competitors Issued by The Federal Trade Commission and The U.S. Department of Justice, Section 1.2 at 4 (April 2000) (collaborations involving "an efficiency enhancing integration of economic activity" are accorded rule of reason analysis). The SyncLink Consortium was an outgrowth of the RamLink project which had been sponsored by the IEEE. *See* CCFF 1501-20.

1567. In April 1998, Bert McComas, an industry consultant, gave an "exclusive" seminar for DRAM manufacturers about Intel's selection of RDRAM. (RX 1138 at 1; Tabrizi, Tr. 9061-62). Mr. McComas pre-cleared his seminar invitation and list of topics with Mr. Tabrizi. (Tabrizi, Tr. 9064).

Response to Finding No. 1567: RPF 1567 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. There is no evidence that any confidential information was shared amongst the attendees of Mr. McComas's seminar and there is no evidence that any agreement between competitors was reached during or otherwise in connection with Mr. McComas's seminar. In addition, Mr. Tabrizi had no input into the substance of the seminar. He reviewed the list of topics only to approve its distribution to members of the SyncLink Consortium. (Tabrizi, Tr. 9064). In addition, although Mr. Tabrizi had no control over the list of attendees, he did undertake efforts to convince Mr. McComas to broaden the list. (RX1153 at 1).

1568. Mr. McComas's invitation asked its recipients not to forward the invitation to Rambus or Intel. (RX 1138 at 1). A few days later, Desi Rhoden (now Chairman of the Board of

JEDEC) sent an email to Mr. Tabrizi about the attendance restrictions. (RX 1149; Tabrizi, Tr. 9064-65). Mr. Rhoden's e-mail stated that he knew McComas and that his "main focus appears to make sure that Rambus and Intel do not attend and therefore has been very restrictive on who can attend. If he says everyone except Rambus and Intel, then it is restraint of trade; while if he says only suppliers, then most of who he wants can attend without there being a charge of restraint of trade." (RX 1149 at 1).

Response to Finding No. 1568: RPF 1568 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. Mr. McComas was an independent industry analyst. (*See* Tabrizi, Tr. 9060). The selection of the agenda and the audience was within his complete discretion and there is no evidence that any aspect of Mr. McComas's seminar violated the antitrust laws. *See also* CCRF 1567. In addition, Mr. Rhoden is not an attorney. Thus, while his sensitivity to steer clear of violations of the antitrust laws is admirable, his statement that a decision to not allow Rambus and Intel to attend would be a restraint of trade must be read in the context of a layman attempting to provide legal advice.

1569. During his April 1998 seminar presentation to the DRAM manufacturers, Mr. McComas stated that a manufacturer that chose to build RDRAMs was making a "guaranteed bad bet for margin enhancement" (RX 1482 at 12), and he stated that RDRAM "deepens [the manufacturer's] financial dilemma." (RX 1482 at 26). As a "possible strateg[y]," Mr. McComas suggested that DRAM manufacturers "tape out but do not fully productize or cost reduce" the RDRAM device, in the hopes of "resist[ing] popular deployment" of RDRAM. (RX 1482 at 34-35).

Response to Finding No. 1569: RPF 1569 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. There is no evidence that DRAM manufacturers reached any agreement to follow Mr. McComas's suggested strategy. In fact, the evidence demonstrates that DRAM manufacturers continued to act in their respective unilateral best interests. *See* CCRF 1562; CCFF 1581.

1570. After the seminar, Mr. McComas accepted an invitation to speak at the next SLDRAM Consortium Executive Meeting, so-called because company executives attend in addition to engineers and marketing personnel. (Tabrizi, Tr. 9066-8). In an April 17, 1998 email extending the invitation, Roberto Cartelli of Texas Instruments wrote to Mr. McComas, "I

personally believe that your story on Intel and its relationship to Rambus is an excellent 'case for action' story to stimulate discussion among industry executives." (RX 1166 at 1; Tabrizi, Tr. 9068).

Response to Finding No. 1570: RPF 1570 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. There is no evidence that DRAM manufacturers reached any agreement to follow Mr. McComas's suggested strategy. In fact, the evidence demonstrates that DRAM manufacturers continued to act in their respective unilateral best interests. *See* CCRF 1562; CCFF 1581.

Finally, the cited document and testimony relates to the efforts of the SyncLink Consortium. The SyncLink Consortium was a joint venture created to share resources and expertise with the goal of developing the SyncLink DRAM. *See* CCFF 1554-66. The SyncLink Consortium was an outgrowth of the RamLink project which had been sponsored by the IEEE. *See* CCFF 1501-20.

1571. Mr. McComas spoke at the June 25, 1998 SLDRAM Executive Summit about the problems faced by DRAM manufacturers. One of the "tactical" problems he identified was how to "Manage Price Competition, Profitability." (RX 1188 at 1). He also talked about how manufacturers could "Respond to the Strategic Threat of Intel/Rambus," and he asked the question, "Who will control the DRAM industry?" (RX 1188 at 1). McComas warned that "Intel/Rambus are using your money to take control of the DRAM industry" and that Intel would "[o]rchestrate early oversupply situation," and he emphasized that "[f]ragmented competition undermines all DRAM manufacturers." (RX 1188 at 26).

Response to Finding No. 1571: RPF 1571 is inaccurate because it misstates the evidence. RX1188 is a seven page document and, therefore, page 26 does not exist. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Further, RPF 1571 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. The statements cited at page 1 of the document represent the work of Mr. McComas, an independent DRAM industry analyst. *See* (Tabrizi, Tr. 9060).

Moreover, there is no evidence concerning what Mr. McComas intended by the cited statements. Although Mr. McComas was on Respondent's final witness list, Respondent did not call him to testify.

1572. Another industry consultant, Victor De Dios, also gave a presentation at the June 25, 1998 SLDRAM Executive Summit. (Tabrizi, Tr. 9071-72). Mr. De Dios told the assembled executives that "Many of the problems are industry problems, not company problems. Competition will not solve them." (RX 1204 at 4).

Response to Finding No. 1572: RPF 1572 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. The statements cited represent the work of Mr. De Dios, an independent DRAM industry analyst. Moreover, there is no evidence concerning what Mr. De Dios intended by the cited statements.

1573. During his presentation at the June 1998 "Executive Summit," Mr. McComas suggested that the DRAM manufacturers share their RDRAM production plans to determine whether there would be a demand-supply imbalance. (Tabrizi, Tr. 9073-74).

Response to Finding No. 1573: RPF 1573 is misleading to the extent that it suggests that Mr. McComas suggested that DRAM manufacturers share production information with each other. Mr. McComas sought to earn income from DRAM manufacturers by providing a service by which DRAM manufacturers could provide certain information to him alone. (Tabrizi, Tr. 9073-74). Mr. McComas's efforts to earn a living by attempting to garner interest in his services from DRAM manufacturers is not evidence of a conspiracy between DRAM manufacturers. There is no evidence that Mr. McComas intended to or did provide DRAM manufacturers with confidential information. Further, the evidence demonstrates that Mr. McComas's suggestion garnered no support whatsoever. (Tabrizi, Tr. 9073-74 ("I don't think anybody went with this suggestion",) 9078-79 ("I don't think his service can be valuable"); RX1251 at 1 ("this research could be interesting, but not very sure how important that can be. . . Intel will limit the production of Camino chipsets just enough to oversupply Rambus parts. It

won't matter how many or how few RDRAMs the industry produces.") (emphasis added)). Thus, RPF 1573 also does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM, because, according to Mr. Tabrizi, any such agreement would have been a waste of effort.

1574. After the meeting, Mr. McComas sought Mr. Tabrizi's advice on how to implement the project of collecting RDRAM production information. (Tabrizi, Tr. 9076). In an August 1998 email to Mr. Tabrizi, Mr. McComas sent a draft message to DRAM manufacturers which stated that "[d]uring the critical production ramp-up phase of Direct Rambus, DRAM vendors will need a constant flow of information to help make wise decisions and to walk the fine line between a pleasant shortage and a disastrous oversupply." (RX 1232 at 1).

Response to Finding No. 1574: RPF 1574 is incomplete and does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. *See* CCRF 1573. In short, Mr. Tabrizi's advice to Mr. McComas was that the project was unlikely to be of any use to the DRAM industry and was not likely to have any impact on the production of RDRAM because Intel would determine the need for RDRAM through its production of chipsets. (RX1251 at 1; Tabrizi, Tr. 9078-79).

1575. Mr. Tabrizi agreed that a shortage of RDRAM would please DRAM manufacturers because "[p]rices go up." (Tabrizi, Tr. 9077).

Response to Finding No. 1575: RPF 1575 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. Throughout the late 1990s, DRAM manufacturers consistently made efforts to reduce the cost of manufacturing RDRAM. Indeed, Hyundai made solving the remaining problems with RDRAM a "High Priority." (CX2334 at 27; CCFF 1862). Intel acknowledged the problems with producing RDRAM. *See* CCFF 1851-54. Even Rambus itself acknowledged the problems with producing RDRAM were related to testing, packaging, and die size. *See* CCFF 1854.

1576. The shortage of RDRAM was not pleasant to the PC OEMs, however, who recognized that for RDRAM to succeed, output of RDRAM had to increase. This led them to try to influence the DRAM manufacturers to increase RDRAM output. (RX 1287 at 4 ("Intel and

major users have been trying to influence improved RDRAM output"). As Ms. Gross testified, Intel, Compaq, and other PC OEMs were trying to influence DRAM manufacturers to increase output of RDRAM and to align roadmaps with Intel's roadmap. These OEMs wanted an RDRAM production ramp-up so that they would have sufficient availability and lower RDRAM prices. (Gross, Tr. 2318-20).

Response to Finding No. 1576: RPF 1576 is misleading because it assumes that DRAM suppliers were the sole basis for RDRAM production estimates. In fact, OEM's were getting unrealistically high projections of RDRAM supply from Intel. These projections were based on the availability of the Camino chipset and consistently proved to be wrong by orders of magnitude. Intel continuously had problems getting the Camino chipset to work. *See* CCFF 1879-94. Intel's own estimates of RDRAM volume plummeted quarter after quarter. *See* CCFF 1898–1905 (Intel's total estimate dropped from 600 million pieces to 250 million pieces during 1999 and 2000). In addition to the delays in the Camino chipset, Intel frequently changed the design of the Rambus system. *See* CCFF 1891. These changes delayed the ramp and increased the cost to DRAM manufacturers. Because of the delays with the Camino chipset, changes in the design of the Rambus system, and the universal inaccuracy of Intel's forecasts, DRAM suppliers were reluctant to commit to full ramp or to meet Intel's forecasts. *See* CCFF 1891. Thus, OEM efforts to influence DRAM manufacturers to commit to Intel's forecast of RDRAM production should be considered in the context of the lack of confidence that Rambus and Intel would actually get a working product to market on time. In spite of this lack of confidence in Intel's forecasts, some DRAM suppliers unilaterally continued to make commitments to produce large volumes of RDRAM *when* it was ready for production. (Tabrizi, Tr. 9107-08, 9165 (discussing CX2303 at 7) ("what we are trying to show to Dell is we are ready to support you in Q299 with our 64-meg, and as your need increases, we will support you with 128-meg and 256-meg Rambus product."); RX1302 at 6 (showing increases in RDRAM supply to Compaq from various manufacturers)).

1577. It was critical to Intel and to the PC OEMs that the DRAM vendors increase the volume of RDRAM because DRAM manufactures will shrink the highest volume parts first. (MacWilliams, Tr. 3837-38). The highest volume parts therefore have a cost advantage. (MacWilliams, Tr. 3837-38; RX 1532 at 1).

Response to Finding No. 1577: Complaint Counsel does not disagree with the basic statements that DRAM manufacturers tend to shrink the highest volume parts first and that the highest volume parts tend to have a cost advantage. *See* CCFF 104-06. RPF 1577 is misleading, however, to the extent it suggests that RDRAM would ever approach the cost of SDRAM. Even Intel was concerned that RDRAM would never be comparable to SDRAM. *See* CCFF 1852-53. Notwithstanding the foregoing, DRAM manufacturers were prepared to ramp RDRAM in volume if the technical problems were fixed on time. *See* CCFF 1800-13, 1862. In fact, Mr. Tabrizi recommended to his superiors at Hyundai that the soon to be combined Hyundai/Lucky Goldstar put its best engineers to work on Rambus using the next generation process technology. (RX1487 at 6). By using the next generation process technology, Hyundai would be able to produce RDRAM at lower relative cost than other dram architectures. *See* CCFF 104-06 (smaller process technology reduces cost).

1578. In response, DRAM manufacturers agreed to manufacture RDRAM in larger volume. For example, in 1998, Hyundai committed to produce 30,000 RDRAM units for Compaq. (RX 1302 at 6). Similarly, Micron committed to produce 15,000 RDRAM units for Compaq. (RX 1302 at 6). Neither company, however, met these commitments. (Gross, Tr. 2327-29). According to Ms. Gross of Compaq, the DRAM manufacturers would not "increase their output at the rate at which we needed to support our systems." (Gross, Tr. 2345-46).

Response to Finding No. 1578: RPF 1578 is misleading to the extent that it suggests that DRAM manufacturers did not follow through on their RDRAM commitments because of an agreement amongst competitors. Ms. Gross's projections of RDRAM volume were based on information obtained from Intel. (Gross, Tr. 2317). As noted, the Intel projections proved to be universally and substantially inaccurate. *See* CCRF 1576. Because of the continual technical problems between Intel and Rambus, there was never any need for DRAM manufacturers

to produce RDRAM in the volumes that Ms. Gross had anticipated. For example, in her testimony Ms. Gross cites to documents that anticipate high volumes of RDRAM in 1999. (Gross, Tr. 2324-29 (discussing RX1302)). In November 1998, Compaq projected worldwide RDRAM demand for calendar year 1999 to be 244 million pieces. (RX1302 at 4). The Camino chipset did not launch until November 1999. *See* CCFF 1887. There was no other chipset that could work with RDRAM. (Tabrizi, Tr. 9186). By the third quarter of 2000, after all of the technical delays, Intel's estimate for the projected demand for RDRAM for the calendar year 2001 was less than 200 million pieces. (CX2338 at 79). Thus, comparing an estimate taken in November 1998 with actual production three years later will provide misleading results. Had Intel and Rambus been able to produce working parts in a timely fashion, then the likely result would have been an aggressive ramp of RDRAM chips.

1579. There is evidence that Mr. Tabrizi took steps in 1998 to ensure that RDRAM production stayed low so that the price difference between RDRAM and SDRAM stayed high. Tabrizi believed at the time that Intel would not change course unless RDRAM failed to get market penetration. (Tabrizi, Tr. 9082). He admitted that one way to cause RDRAM to fail to get market acceptance was if the OEMs were convinced that even if volumes went up, prices would not fall. (Tabrizi, Tr. 9083). If the OEMs were convinced of this, they would not adopt RDRAM. (Tabrizi, Tr. 9083).

Response to Finding No. 1579: RPF 1579 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. As explained previously, the failure of RDRAM was due to the significant delays and system changes caused by technical problems between Rambus and Intel. *See* CCRF 1576, 1578.

1580. In the fall of 1998, Hyundai gave RDRAM price projections to its customers that were on the order of 50% to 60% higher than those reflected in its internal pricing documents. (Tabrizi, Tr. 9085-90; RX 1280; RX 1293A). Mr. Tabrizi encouraged Hyundai's sales force to distribute these higher prices to key accounts that were deciding whether to use RDRAM, DDR, or PC100 because "Intel was telling everybody that [RDRAM is] only going to be a 5 percent premium . . . . I wanted to make sure my OEM knows it's going to cost them more than 5 percent . . ." (Tabrizi, Tr. 9091).

Response to Finding No. 1580: RPF 1580 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. First, as explained previously, the failure of RDRAM was due to the significant delays and system changes caused by technical problems between Rambus and Intel. *See* CCRF 1576, 1578. Second, as Mr. Tabrizi explained, initial projections provided to customers were a starting point for negotiations. (Tabrizi, Tr. 9087-89 (noting that initial prices given to customers was subject to negotiation and dependent on actual yield)). Third, Respondent does not even suggest that Mr. Tabrizi's statements to Hyundai's own sales force was provided to or followed by any other DRAM manufacturer. Hyundai's unilateral business strategy cannot be the basis for a finding of concerted action.

1581. Mr. Tabrizi also admitted at trial that in October 1998, Hyundai gave RDRAM production forecasts to Intel that were deliberately inflated. (Tabrizi, Tr. 9092). (*See also* RX 1295 at 1 (internal Hyundai e-mail, copied to Tabrizi, that states that from the perspective of the Hyundai America marketing group, "we can overstate our direct Rambus production so Intel can feel we are more aggressive on the ramp up.”))

Response to Finding No. 1581: RPF 1581 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. First, as explained previously, the failure of RDRAM was due to the significant delays and system changes caused by technical problems between Rambus and Intel. *See* CCRF 1576, 1578. Second, as Mr. Tabrizi explained, Hyundai unilaterally inflated its RDRAM production to Intel because it wanted to be viewed by Intel as a leader in RDRAM production and remain on Intel's "good side." (Tabrizi, Tr. 9092-93). Moreover, the logical impact of providing Intel with an inflated forecast is to convince Intel that RDRAM prices actually would be *lower* than they would with less production. Thus, such action is not consistent with an effort to convince Intel or OEM's to alter course.

1582. Although Mr. Tabrizi would not admit it at trial, it is likely that when combined with Hyundai's inflated price forecasts, the inflated production numbers that Hyundai provided were intended to convince Intel that RDRAM prices would not come down *even if* production increased.

Response to Finding No. 1582: RPF 1582 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1583. Mr. Tabrizi also urged his fellow DRAM manufacturers to lie to Intel about production and pricing. A report prepared by an Infineon engineer about an October 1998 meeting attended by Mr. Tabrizi along with engineers from Micron and Infineon, states that "[a]ccording to Farhad Tabrizi, Hyundai has given Rambus ASP projections for end of next year of two to three times of todays SDRAM prices; they also gave to Intel a production projection of three times their actual plans => *They encourage every DRAM manufacturer to do the same in order to let Intel not generate a Rambus oversupply*." (RX 2192 at 2) (emphasis added). Mr. Tabrizi denied at trial that he had made the statements attributed to him in the Infineon trip report. (Tabrizi, Tr. 9097). Mr. Lee similarly denied being present when any such statements were made, although the Infineon trip report places him at the meeting. (Lee, Tr. 7028; RX 2192 at 1, 3)

Response to Finding No. 1583: RPF 1583 is misleading to the extent that it suggests that Mr. Tabrizi made the statement attributed to him to a group of competitors. Mr. Tabrizi did not even attend this meeting. (Tabrizi, Tr. 9095). Nor does he have any recollection of making such a comment to other DRAM manufacturers. (Tabrizi, Tr. 9097 ("This is absolutely not correct.")). *See also* (Lee, Tr. 7028-29 (present at the meeting, but did not recall this statement being made)). The evidence is unclear concerning the source and the context of the alleged statement. More importantly, however, the statement, even if made by Mr. Tabrizi, does not support the conclusion that DRAM manufacturers reached an agreement with respect to the production of RDRAM. Indeed, the logical impact of providing Intel with an inflated forecast is to convince Intel that RDRAM prices actually would be *lower* than they would with less production. Thus, such action is not consistent with an effort to convince Intel or OEM's to alter course.

1584. The DRAM manufacturers also met in October 1998 to discuss a proposal by Micron's Terry Lee that they agree to "a common roadmap" that the manufacturers would provide

to chipset companies and PC OEMs. (RX 2191 at 1; RX 2192 at 3). Such a "roadmap" would be "'signed' by all or most of the DRAM companies" and would show a joint commitment by the manufacturers to support DDR or SLDRAM instead of RDRAM. (*Id.*). The "main target" of such a joint roadmap would be to remove the "current uncertainty about the supply situation" among the chipset companies and PC OEMs. (RX 2191 at 1). A proposed joint roadmap was later circulated to numerous DRAM manufacturers by Micron. (RX 1423 at 1-2).

Response to Finding No. 1584: RPF 1584 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. There is no evidence that the forecast contained in that email was ever adopted by any DRAM manufacturer. For example, the email referenced at RX1423 is dated March 30, 1999. After receiving the email, Mr. Tabrizi caused others at Hyundai to determine if the information was consistent with Hyundai's own internal forecasts. (RX1423 at 1). Apparently, it was not, because in April 1999, Hyundai still anticipated that RDRAM would be the next dominant architecture in PC main memory. (CX2334 at 23). Even later, in July 1999, while preparing for Hyundai's merger with Lucky Goldstar, Mr. Tabrizi advised his superiors at Hyundai to put the combined company's best engineers to work on developing RDRAM using the next generation process technology. (RX1487 at 6). In June 2000, after the technical problems with RDRAM seemed to be resolved, the combined Hyundai/Luck Goldstar was ordered by its CEO to make RDRAM the highest priority and load Hyundai's production lines with RDRAM chips. (Tabrizi, Tr. 9108 (discussing RX1661) ("JUDGE McGUIRE: Now, what are you talking about when you say Sang Park, our new president, had joined our company and put Rambus as the highest priority and allocated many dollars to Rambus? What context are you talking about? What was he doing in that time period? THE WITNESS: So we get together for a product planning meeting and we decide the priority of the product, and at that time Samsung was one of the main suppliers for Rambus and Sang Park wanted to compete with Samsung head to head . . . So he'd ordered our factory to load all of our factory with Rambus and he wanted to compete with Samsung. He said if

Samsung is enjoying Rambus prices are high, I want to share that.")). Thus, there is no evidence that any manufacturer's made any agreement with respect to RDRAM production or that RDRAM production was affected by the forecast of consumer demand found at RX1423. As Mr. Tabrizi had predicted, RDRAM production would be dictated by Intel's supply of chipsets. (RX1251 at 1 ("this research could be interesting, but not very sure how important that can be. . . Intel will limit the production of Camino chipsets just enough to oversupply Rambus parts. It won't matter how many or how few RDRAMs the industry produces.") (emphasis added)). Thus, the reduction in expected RDRAM production fell when Intel began to make substantial reductions in its forecast for RDRAM penetration. *See* CCFF 1898-1905 (During 1999 and 2000, Intel's total estimate of RDRAM dropped from 600 million pieces to 250 million pieces).

1585. Communications about RDRAM production between and among the DRAM manufacturers continued in 1999. In January 1999, Desi Rhoden sent a proposal to all of the major DRAM manufacturers regarding the transformation of the former SyncLink Consortium (by then called "SLDRAM Inc.") into a marketing-oriented organization to be called "Advanced Memory Inc." (RX 1373 at 1-3). "Advanced Memory Inc." was ultimately called "AMI2"; Mr. Rhoden became its President and Chief Executive Officer. (Rhoden, Tr. 260, 696-97, 1235). Mr. Rhoden stated that the focus of the new organization would be to "*co-ordinate* instead of developing new technology." (RX 1377 at 3) (emphasis added). He also stated that "[i]n the DRAM industry, we are clearly stronger together than we are individually." (RX 1373 at 1).

Response to Finding No. 1585: RPF 1585 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. AMI2 "follows the contract that was originally drawn up by SLDRAM, and there is a series of bylaws, and those bylaws were inherited as modified from the SLDRAM consortium." (Rhoden, Tr. 603). *See also* CCRF 1554. As with the SyncLink Consortium, AMI2 members included not only DRAM manufacturers, but also infrastructure providers such as chipset companies. (Rhoden, Tr. 673-74). AMI2 attempts to take the industry a few steps beyond the standardization process that takes place at JEDEC. For example, "before you can have a full [computer] system. . . that actually utilizes that standard. . . many other chips, motherboards, memory modules, clock devices,

memory controllers" must be developed. (Rhoden, Tr. 690). The effort to coordinate the implementation of a full computer system entails significant costs which, as in SyncLink, was shared among the members. (Rhoden, Tr. 689-90).

1586. Mr. Rhoden was obviously aware of the antitrust problems that arise when competitors "co-ordinate" their activities in an effort to be "stronger" market participants. (*Id.*). In Mr. Rhoden's view, however, the corporate form for the new organization would "indemnify member companies from antitrust while still providing a close working environment for all." (RX 1373). He also suggested that an existing consortium of DRAM manufacturers called "M12" should "be folded under the corporation for anti-trust protection." (RX 1373 at 8).

Response to Finding No. 1586: RPF 1586 is misleading to the extent it suggests anything nefarious in Mr. Rhoden's sensitivity to abiding by the antitrust laws. Joint ventures, standard setting organization, trade associations, etc., must be careful to avoid competitors from sharing confidential information that is not necessary to accomplish the procompetitive purposes of the organization. As with the SyncLink Consortium (*see* CCFF 1554-66), AMI members shared technical information and resources for the purpose of promoting a new technology. *See* CCRF 1585. In particular, AMI2 focuses on the steps that must take place after standardization by JEDEC in order to facilitate broad acceptance of new technologies. For example, "before you can have a full [computer] system. . . that actually utilizes that standard. . . many other chips, motherboards, memory modules, clock devices, memory controllers" must be developed. (Rhoden, Tr. 690). The effort to coordinate the implementation of a full computer system entails significant costs which, as in SyncLink, was shared among the members. (Rhoden, Tr. 689-90). JEDEC has rules that regulate information shared between its members. *See* (CX0204 at 3 "Improper Activities and Programs"). Likewise, Mr. Rhoden, as chairman of AMI2, took care to ensure that members of AMI2 conducted their activities in accordance with the law. Moreover, the record demonstrates that Mr. Rhoden spoke on the topic of antitrust concerns on other occasions. For example, Mr. Rhoden's presentation promoting JEDEC specifically cites "Uphold the

principles of Anti-trust" as on of the guiding principles of JEDEC. (CX0302 at 9; Rhoden, Tr. 302-03). Thus, it should come as no surprise that Mr. Rhoden, in particular, would seek to ensure that AMI2 followed suit. Finally, there is no testimony concerning RX1373 because Respondent did not ask Mr. Rhoden any questions concerning the document.

1587. In a follow-up proposal to DRAM manufacturers by Mr. Rhoden, he again emphasized the need to provide antitrust protection for the "M12" consortium, although that organization had expanded and was now called "M14":

> "Marketing coordination has been the function of the M14 group and that group should be folded into the corporation, if for no other reason than to provide antitrust proteciton."

(RX 2284 at 2).

Response to Finding No. 1587: RPF 1587 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. *See* CCRF 1586. As with RPF 1586, Respondent did not ask Mr. Rhoden any questions concerning the cited document.

1588. While it is not clear whether the "M12" consortium was ever formally "folded under" Mr. Rhoden's company for "antitrust protection," and while it is not clear why anyone would believe that competitors could avoid antitrust liability for market coordination or other collusive activity simply by engaging in joint action within a corporate shell, it is clear from the activities of AMI2 and "M14" why Mr. Rhoden thought that "antitrust protection" was needed.

Response to Finding No. 1588: RPF 1588 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. In any event, the reasons why members of AMI2 might be entitled to antitrust protection for joint action are set forth in the Antitrust Guidelines for Collaborations Among Competitors Issued by The Federal Trade Commission and The U.S. Department of Justice, Section 1.2 at 4 (April 2000) (an agreement, even if it might otherwise be *per se* unlawful, is analyzed under the rule of reason provided that it

is "reasonable related to, and reasonably necessary to achieve procompetitive benefits from, an efficiency-enhancing integration of economic activity.").

1589. In a March 1, 1999 meeting of the "M14" consortium, the DRAM manufacturers in attendance agreed to visit customers "as a group" to persuade them to utilize DDR instead of RDRAM. (RX 1390 at 2-3). The manufacturers also agreed to provide production "volume projections" of memory devices to Mr. Rhoden to allow him to produce a joint production forecast. (*Id.*). In addition, "a decision was made" that "benchmarking" be "done for DDR SDRAM" on the issues of "Price-Cost-Availability." (RX 1390 at 2).

Response to Finding No. 1589: RPF 1589 does not support the conclusion that DRAM manufacturers reached any agreement with respect to the production of RDRAM. Further, RPF 1589 is misleading to the extent it suggests that the goal was to convince OEM's to use DDR *instead* of RDRAM. Because of Intel's dominance of microprocessors and chipsets, DRAM manufacturers and OEM's were committed to producing and using RDRAM in the PC space. *See* CCFF 1581 (citing roadmaps showing that RDRAM was anticipated as the main memory for the PC space). As with SyncLink, the effort of AMI at this time was to finding a role for a competitive technology outside of the PC main memory space. *See* CCFF 1573-81. Once again, however, manufacturers continued to act in accordance with their own unilateral best interest. For example, Luck Goldstar and Toshiba decided that they would not visit customers with the other members of AMI2. (RX1390 at 2).

Generally, joint ventures, standard setting organization, trade associations, etc., must be careful to avoid competitors from sharing confidential information that is not necessary to accomplish the procompetitive purposes of the organization. As with the SyncLink Consortium (*see* CCFF 1554-66), AMI members shared technical information and resources for the purpose of promoting a new technology. *See* CCRF 1585; *see also* Antitrust Guidelines for Collaborations Among Competitors Issued by The Federal Trade Commission and The U.S. Department of Justice, Section 1.2 at 4 (April 2000) (an agreement, even if it might otherwise be *per se* unlawful,

is analyzed under the rule of reason provided that it is "reasonable related to, and reasonably necessary to achieve procompetitive benefits from, an efficiency-enhancing integration of economic activity."). In particular, AMI2 focuses on the steps that must take place after standardization by JEDEC in order to facilitate broad acceptance of new technologies. For example, "before you can have a full [computer] system. . . that actually utilizes that standard. . . many other chips, motherboards, memory modules, clock devices, memory controllers" must be developed. (Rhoden, Tr. 690). The effort to coordinate the implementation of a full computer system entails significant costs which, as in SyncLink, was shared among the members. (Rhoden, Tr. 689-90). JEDEC has rules that regulate to information shared between its members. *See* (CX0204 at 3 "Improper Activities and Programs"). Likewise, the members of AMI2 took care to ensure that they conducted their activities in accordance with the law. Moreover, the record demonstrates that Mr. Rhoden, the chairman of AMI2, spoke on the topic of antitrust concerns on other occasions. For example, Mr. Rhoden's presentation promoting JEDEC specifically cites "Uphold the principles of Anti-trust" as on of the guiding principles of JEDEC. (CX0302 at 9; Rhoden, Tr. 302-03). Thus, it should come as no surprise that Mr. Rhoden, who was present at this meeting, would seek to ensure that AMI2 followed suit. Complaint Counsel also notes that the only witness questioned concerning this meeting was Mr. Kellogg of IBM, who was not present at the meeting. Respondent once again shied away from directing any questions to Mr. Rhoden (or any other witness present at the meeting) concerning the cited document.

1590. It is likely that the requirement for "benchmarking" of the price of DDR SDRAM related to the manufacturers' need to introduce the new DDR SDRAM device at little or no premium over existing SDRAM prices, in an effort to convince the OEMs to abandon RDRAM in favor of SDRAM. (RX 1713 at 1). By June 2001, Mr. Rhoden was able to report to the DRAM manufacturers that comprised the AMI2 board that their efforts in this regard had been successful, for their Taiwanese customers had told Mr. Rhoden that the "DDR price is low enough." (RX 1848 at 2).

Response to Finding No. 1590: RPF 1590 is misleading to the extent it suggests that the benchmarking of DDR SDRAM related to actual prices in the market. In addition to relative cost and availability, the DDR SDRAM benchmarking performed by members of AMI2 also concerned power and performance. (RX1390 at 2). As noted previously, relative measures, including cost, performance, availability, power usage, etc. are often discussed in the context of new standards. (Rhoden, Tr. 599-600). This is because such information is useful to both customers and manufacturers in evaluating various alternatives. Thus, customers would have the benefit of full information when deciding whether to purchase DDR for uses outside of PC main memory. Further, DDR was "evolutionary" with respect to SDRAM (*see* CCFF 653, 2569, 2572, 2649) because it was able to use the same testers, other infrastructure, and the die size is not much larger than SDRAM. Thus, there should be no surprise that the relative cost of SDRAM and DDR was close.

Finally, the cited document and testimony relates to the efforts of AMI2. AMI2 was a joint venture created to share resources and expertise with the goal of marketing new memory technologies. *See* CCRF 1585.

1591. "Benchmarking" the DDR price in an effort to avoid a price premium between DDR and SDRAM would only be a successful strategy, and would only lure OEM customers away from RDRAM, if the RDRAM price premium over SDRAM simultaneously stayed high. There is substantial evidence that DRAM manufacturers were *very* concerned in 1999 about the possibility that Samsung, in particular, might produce too much RDRAM, thus driving prices down.

Response to Finding No. 1591: RPF 1591 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1592. In April 1999, Micron's Kevin Ryan sent an e-mail to Terry Lee, Jeff Mailloux, Vice-President Bob Donnelly and others at Micron that attached an article describing Samsung's plans to produce as much as 40 million Rambus devices in 1999. (RX 1444 at 2). Mr. Ryan

complained that Samsung had "broken ranks with the other suppliers" and had "sold their soul to the devil." (RX 1444 at 1). One of the recipients of the e-mail, Mike Seibert, responded that "[t]hese guys are big trouble for us all. *If this thing gets into an oversupply mode with RDRAM things could get really ugly.*" (RX 1444 at 1) (emphasis added). Mr. Seibert then asked Micron Vice-President Bob Donnelly if Samsung understood "what the Rambus/Intel biz model will do to our autonomy?" (*Id.*). Vice-President Donnelly responded that he had "certainly made the point with the officers that Intel . . . ultimately could control the DRAM industry." (*Id.*).

Response to Finding No. 1592: RPF 1592 does not support the conclusion that DRAM manufacturers reached any agreement on the production of RDRAM. Indeed, Samsung's leadership in RDRAM production shows that DRAM manufacturers continued to act in their respective unilateral best interests. In the very same email, Mr. Donnelly pointed out that "I don't think everyone considers it as much of a threat as I do" further illustrating the fact that DRAM manufacturers continued to pursue their unilateral interests. (RX1444 at 1). In fact, even as late at 2000, Hyundai decided to "compete with Samsung head to head" by putting all their dram wafers into Rambus development. (Tabrizi, Tr. 9107-08). Significantly, this action was taken *after* Mr. Tabrizi had recommended that the combined Hyundai/Lucky Goldstar put its best engineers to work on RDRAM using the next generation process technology. (RX1487 at 6).

1593. Hyundai was also anxious to make Samsung understand the dangers of high volume RDRAM production. In a July 1999 email, Mario Martinez of Hyundai recommended to Mr. Tabrizi and others at Hyundai that "[w]ith Samsung building significant amounts of product, *we need to work with them to limit the supply in the market*, otherwise we both will be competing for market share which will result in an oversupply. We have to meet with Samsung and discuss our and their production plan, TAM analysis and targeted market share." (RX 1487 at 4 (emphasis added); Tabrizi, Tr. 9103). Mr. H.S. Ahn responded in the same email: "I have connection in Samsung. If I know what time you are available, I will try set up meeting with key person in Samsung in Seoul, Korea and I will try persuade them. [A]ctually they also have same idea for Rambus business compare with you." (RX 1487 at 4; Tabrizi, Tr. 9104).

Response to Finding No. 1593: RPF 1593 does not support the conclusion that DRAM manufacturers reached any agreement on the production of RDRAM and ignores substantial evidence of Mr. Tabrizi's and Hyundai's efforts to be a leader in RDRAM production. In fact, even as late at 2000, Hyundai decided to "compete with Samsung head to head" by putting

all their dram wafers into Rambus development. (Tabrizi, Tr. 9107-08). In the very same email that RPF 1593 cites, Mr. Tabrizi recommends to his superiors that the combined Hyundai/Lucky Goldstar put its best engineers to work on Rambus using the next generation process technology. (RX1487 at 6).

1594. Hyundai marketing executive Farhad Tabrizi admitted at trial that he had told Sang Park, then the President and Chief Operating Officer of Hyundai, that he wanted to "kill" Rambus and force RDRAM from the market. (Tabrizi, Tr. 9105-07). Tabrizi subsequently testified that what he meant by "killing" Rambus was really just "Rambus suicide, [with] me watching on the sideline." (Tabrizi, Tr. 9109). In his June 2000 email to Mr. Park, however, Mr. Tabrizi had written only of killing: "[i]f Intel does not invest in us, I really want to ask you to let me go back to my old mode of RDRAM killing. I think we were very close to achieving our goal until you said we are absolutely committed to this baby." (RX 1661 at 2).

Response to Finding No. 1594: RPF 1594 does not support the conclusion that DRAM manufacturers reached any agreement on the production of RDRAM. Moreover, RPF 1594 demonstrates that notwithstanding Mr. Tabrizi's efforts to find support to SyncLink, the highest levels of Hyundai continued to devote substantial resources to RDRAM. Even in June 2000, after all of the Rambus failures and delays, Hyundai still had two RDRAM projects among its top ten priorities. (RX1661 at 1). Further, the two RDRAM projects still were priorities for Hyundai even after Rambus began filing lawsuits against manufacturers for royalties related to SDRAM. (RX1661 at 2).

1595. The "baby" was indeed killed. Jacquelyn Gross of Compaq testified that because the price of RDRAM did not decrease and because Compaq did not believe that it would decrease in the future, Compaq decided to abandon its plans and to shift to DDR. (Gross, Tr. 2339).

Response to Finding No. 1595: RPF 1595 is misleading because it mischaracterizes Ms. Gross's testimony. Ms. Gross testified that, to her understanding, the reason why RDRAM prices would not fall to the levels necessary for Compaq to adopt it was due to the availability of test equipment, packaging issues, and some supply materials. (Gross, Tr. 2362). These are the same concerns that Rambus itself acknowledged as problems that inhibited the

widespread adoption of RDRAM. *See* CCFF 1584. Ms. Gross also testified that her belief that RDRAM prices would not decrease was only one of the reasons that Compaq abandoned RDRAM. (Gross, Tr. 2339). Moreover, as noted previously, the failure a RDRAM was due to the high royalty rates on RDRAM, the high cot of manufacturing RDRAM (due to large die size, testing costs, etc.), and the inability of Intel and Rambus to produce a working chipset to support RDRAM within the time frame they had promised. *See* CCFF 1800-1924.

1596. Similarly, AMD abandoned plans to adopt RDRAM because, based on what they were told by DRAM manufacturers, it was clear that DDR, not RDRAM would become a commodity product. (Polzin, Tr. 4013).

Response to Finding No. 1596: RPF 1596 is misleading because it mischaracterizes the testimony of the witness. Mr. Polzin did not testify that AMD abandoned plans for RDRAM. Instead, he testified that plans were "shelved" in such a manner that they could be restarted because RDRAM would not become a commodity product in the time frame that AMD had anticipated. (Polzin, Tr. 4013). Indeed, Mr. Polzin specifically attributed the decision to put its RDRAM chipset "on the shelf" to "resource constraints and continuing bad news about RDRAM (i820 delayed launch, low RDRAM yields)." (CX2158 at 2) (emphasis added). Thus, had Intel and Rambus continued with their efforts to timely develop working parts, AMD likely would have taken the project "off the shelf."

Moreover, as noted previously, the failure a RDRAM was due to the inability of Intel and Rambus to produce the Camino chipset (*i.e.*, the i820 chipset) within the time frame they had promised. *See* CCFF 1877-1910 (technical difficulties lead to Intel revising downward its projections for RDRAM during 1999 and 2000). Mr. Polzin's testimony is consistent with the facts of the continual delays and technical problems associated with getting RDRAM to market.

1597. The Dell story is the same. In a February 2000 e-mail asking Micron to supply it with RDRAM, Dell stated that it was "committed to Rambus" but that its ability to incorporate Rambus devices in its PC's was "clearly limited by supply." (RX 1560 at 1). Looking ahead to the

second half of 2000, Dell projected that with lower pricing, fully 40% of its market demand would be satisfied with RDRAM technology. (RX 1560 at 1).

Response to Finding No. 1597: RPF is misleading to the extent it suggests that DRAM manufacturers were not attempting to produce RDRAM to meet demand. As Dell indicated in its email, supply in the second half of 2000 was estimated to be better than in the first half, (RX1560 at 1) suggesting the DRAM suppliers were in the process of ramping RDRAM. As previously noted, the Camino chipset launched only a few months earlier in November 1999. *See* CCFF 1887. However, in May 2000, Intel was forced to recall its Camino chipsets. CCFF 1893. The following month, in June 2000, Intel was forced to delay the launch of its Timna chipset. CCFF 1894. As a result, Intel revised its projections for the volume of RDRAM to be shipped in 2000 downward sharply. CCFF 1895-1910.

Moreover, as noted previously, the failure a RDRAM was due to the inability of Intel and Rambus to produce a working product within the time frame working parts in the time frame they had promised. *See* CCFF 1877-1910 (technical difficulties lead to Intel revising downward its projections for RDRAM during 1999 and 2000).

1598. By May 2000, however, the situation had not improved, and Dell was considering moving into "a low key Rambus mode." (RX 1636 at 1). The Dell "message" was "pretty straightforward:"

> "Dell has booked our products over the last year around the assumption that RDRAM prices would decline and close on SDRAM. This would help us create demand . . . the memory vendors have shown no desire to drop prices, therefore we are reevaluating out strategies . . . so the message to them is drop prices or we will continue to decrease our RDRAM forecasts and we will architect next generation systems around DDR . . . we will give the memory vendors till the end of May to reply to our request . . . if they still have no desire to drop prices, we should push ahead rearchitecting chipsets around DDR."

(RX 1636 at 1). Prices did not come down, however, and Dell too shifted its roadmap to DDR.

Response to Finding No. 1598: RPF 1598 does not support the conclusion that DRAM manufacturers reached any agreement with respect to production of RDRAM. In fact, by the second quarter of 2000, Intel had reduced its year 2000 forecast of RDRAM penetration from approximately 600 million pieces to little more than 100 million pieces. *See* (CX2338 at 79) (comparing Intel year 200 forecast given in 1Q99 with Intel year 200 forecast given in 2Q00). As noted previously, DRAM suppliers were not the sole basis for RDRAM production and cost estimates. In fact, OEM's like Dell were getting unrealistically high projections of RDRAM supply from Intel. These projections were based on the availability of the Camino chipset and consistently proved to be wrong by orders of magnitude. Intel continuously had problems getting the Camino chipset to work. *See* CCFF 1879-94. Intel's own estimates of RDRAM volume plummeted quarter after quarter. *See* CCFF 1898–1905 (Intel's total estimate dropped from 600 million pieces to 250 million pieces during 1999 and 2000). In addition to the delays in the Camino chipset, Intel frequently changed the design of the Rambus system. *See* CCFF 1891. These changes delayed the ramp and increased the cost to DRAM manufacturers. Because of the delays with the Camino chipset, changes in the design of the Rambus system, and the universal inaccuracy of Intel's forecasts, DRAM suppliers were reluctant to commit to full ramp or to meet Intel's forecasts. *See* CCFF 1891. Thus, OEM efforts to influence DRAM manufacturers to commit to Intel's forecast of RDRAM production should be considered in the context of the lack of confidence that Rambus and Intel would actually get a working product to market on time. In spite of this lack of confidence in Intel's forecasts, some DRAM suppliers unilaterally continued to make commitments to produce large volumes of RDRAM *when* it was ready for production. (Tabrizi, Tr. 9107-08, 9165 (discussing CX2303 at 7) ("what we are trying to show to Dell is we are ready to support you in Q299 with our 64-meg, and as your need increases, we will support you

with 128-meg and 256-meg Rambus product."); RX1302 at 6 (showing increases in RDRAM supply to Compaq from various manufacturers)).

1599. RDRAM failed to command significant market share despite the fact that it was the "best solution." (RX 1762 at 5; MacWilliams, Tr. 4931-32). As Peter MacWilliams of Intel put it:

(MacWilliams, Tr. 5075 (in camera)).

Response to Finding No. 1599: RPF 1599 is misleading, incomplete, and ignores substantial evidence that RDRAM was not the "best" solution for most applications. In fact, Intel's opinion is strictly limited to the Intel Pentium 4 processor platform. (RX1762 at 5). Given the tremendous resources devoted to getting RDRAM to work as the exclusive memory for the Pentium 4, it should not be surprising that Intel would believe that it was the "best" technology for the platform. But there is no evidence that this opinion extended beyond the Pentium 4 platform. Even Mr. MacWilliams acknowledged that RDRAM was only

(MacWilliams, Tr. 5075 (*in camera*)). Moreover, "best" is a relative term. DRAM customers tend to consider the "best" choice to be the choice that offers them the best price/performance benefit. To that end, many customers are willing to forego the small performance advantages that Rambus offered in exchange for lower prices, particularly in cost price sensitive products. *See* CCFF 93, 99, 125, 525. Thus, despite the fact that manufacturers were expending great effort in an attempt

to reduce the cost of RDRAM, (*see* RX1762 at 5) RDRAM continued to be higher cost due to its larger die size, its packaging issues, and its testing cost. CCFF 1838-66. DRAM customers required the next generation DRAM to be within 5% of the cost of the then-current commodity DRAM, which was SDRAM. CCFF 126. RDRAM missed the mark by a wide margin. *See* (CX0974 at 1 (Tate December 1997 email discussing Rambus-Intel meeting: "COST – biggest issue"; "rdram price premiums of 20-30%!!"; "die size premium"; "royalty reduction"). *See also* CCFF 1852-58.

1600. There is also evidence that *after* RDRAM failed to achieve marketplace success, the DRAM manufacturers felt able to *raise* DDR prices substantially, and that they did so through concerted action. In a November 26, 2001 e-mail entitled "OEM meeting update," a Micron manager named Kathy Radford described the efforts of Infineon and Samsung to raise DDR prices, and stated that Micron intended to try to raise its prices to "all of the OEM customers." (RX 1922A at 1). Ms. Radford then reported that "[t]he consensus from all suppliers is that if Micron makes the move, *all of them will do the same and make it stick*." (RX 1922A at 1) (emphasis added).

Response to Finding No. 1600: RPF 1600 does not support the conclusion that DRAM manufacturers reached any agreement with respect to production of RDRAM. As an initial matter, RPF 1600 is irrelevant because it relates to Micron's internal pricing strategy for SDRAM and DDR SDRAM and contains no discussion of RDRAM. Thus, even if DRAM manufacturers did conspire to raise the price of SDRAM and DDR SDRAM (and there is no evidence that they did), such a conspiracy has nothing to do with the raising the price or reducing the volume of RDRAM. Further, the logical impact of higher prices for SDRAM and DDR SDRAM would be to increase demand for royalty-generating RDRAM. As Mr. Polzin testified, AMD's RDRAM projects were not "killed", but only "shelved." (Polzin, Tr. 4013). Thus any effort to raise the prices of SDRAM and DDR SDRAM had the potential of making RDRAM more attractive. In addition, long before November 2001, the major OEM's were making products that contained RDRAM. (Gross, Tr. 2276 (Compaq began using RDRAM in products in 1999)). Increases in the

prices of SDRAM and DDR SDRAM likely would lead to reduced sales of products that included those memories and an increase in the sales of products containing RDRAM.

1601. Prices did, in fact, increase substantially in the months after Mr. Radford's e-mail. On March 1, 2002,

(RX 1991 at 1) (in camera).

Response to Finding No. 1601: RPF 1601 does not support the conclusion that DRAM manufacturers reached any agreement with respect to production of RDRAM.

(RX1991 at 1, *in camera*).

1602. The evidence that was introduced during trial regarding concerted action by DRAM manufacturers to manipulate memory production and pricing in order to block RDRAM's market success and protect the manufacturers' "autonomy" is not summarized here in order to excuse any of Rambus's alleged conduct. The evidence is instead relevant for four reasons:

(1) it shows that Intel's choices, not GATWICK's standard-setting, tend to determine marketplace success in the DRAM industry;
(2) it rebuts Complaint Counsel's assertion that the RDRAM device failed on its merits because of what the DRAM manufacturers claimed were its inherently high manufacturing costs;
(3) it affects the credibility of the trial witnesses whose words and deeds are reflected in the cited exhibits; and
(4) evidence that manufacturers have engaged in collusive action with the intent and effect of reducing consumer choice, raising prices, or eliminating a superior technology from the marketplace is always of interest to the Federal Trade Commission.

Response to Finding No. 1602: RPF 1602 lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits

that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs. Furthermore, the proposed findings are irrelevant for the reasons stated in Complaint Counsel's Motion *In Limine* to Bar Presentation of Testimony and Arguments Regarding Purported Collusion Among DRAM Manufacturers (March 26, 2003).

C. Summary Of Findings Regarding Economic Implications Of The Evidence.

1603. Complaint Counsel has failed to meet its burden to prove that Rambus's alleged conduct was exclusionary.

Response to Finding No. 1603: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1604. To be exclusionary, conduct must not make economic sense absent some gain from an adverse impact on competition.

Response to Finding No. 1604: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1605. Conduct that has a legitimate business justification is not exclusionary.

Response to Finding No. 1605: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1606. Legitimate business justifications exist for not disclosing information about pending patent applications. In fact, not disclosing information about pending patent applications may be procompetitive and enhance consumer welfare.

Response to Finding No. 1606: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1607. These legitimate business justifications continue to be valid for firms that involved in standard-setting bodies. A firm that is involved in a standard-setting body may benefit from not disclosing information about pending patent applications for reasons that are independent of what standards are adopted by the standard-setting body.

Response to Finding No. 1607: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1608. If Rambus did not disclose information to JEDEC about its pending patent applications, this conduct cannot be considered exclusionary because there is a legitimate business justification for such conduct.

Response to Finding No. 1608: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is misleading to the extent it implies that any legitimate business justification was in fact the motivation for Rambus's conduct in this case.

1609. Further, applying the definition of exclusionary used by Complaint Counsel's economic expert, Complaint Counsel have not proven that Rambus's alleged conduct excluded equal or superior technologies.

Response to Finding No. 1609: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel

submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1610. Although he concluded that equal or superior alternatives were excluded, Complaint Counsel's economic expert's definition of "equal or superior" was flawed and could not support a finding that such alternatives were excluded.

Response to Finding No. 1610: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1611. Complaint Counsel's theory of exclusionary behavior in this case requires that Rambus acted in an irrational manner. The theory posits that knowingly Rambus withheld information about its pending patents in hopes of later being able to enforce its patents against JEDEC-compliant products. But the theory also requires that Rambus do so knowing that its enforcement of its patents would trigger inquiries into its JEDEC-related conduct, leading to the discovery of its purposeful and knowing withholding of information, and thus to the inability to enforce its patents.

Response to Finding No. 1611: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

Furthermore, this proposed finding is inaccurate. There is no requirement, in either of Professor McAfee's reasons why Rambus's behavior is exclusionary, for that behavior to be irrational.

1612. Further, Complaint Counsel's economic expert made inadequate assumptions in forming his opinions. Although he assumed that Rambus violated JEDEC's rules by failing to disclose certain information, he made no assumptions as to what information should have been disclosed or when that disclosure should have occurred. Further, Complaint Counsel's economic expert's opinions have been undermined by the evidence.

Response to Finding No. 1612: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel

submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1613. Complaint Counsel's economic expert premises his opinion that Rambus's conduct was exclusionary on the assumption that Rambus's conduct violated JEDEC's rules, but Complaint Counsel have not shown that enforcing JEDEC's rules would promote the purposes of the antitrust laws.

Response to Finding No. 1613: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1614. Complaint Counsel have failed to meet their burden to show that Rambus's alleged conduct enhanced its market power.

Response to Finding No. 1614: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1615. Complaint Counsel have failed to show that JEDEC's standardization of Rambus's technologies enhanced Rambus's market power.

Response to Finding No. 1615: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1616. Rambus's technologies were superior to any of the alternatives, even accounting for Rambus's royalties. If they were acting rationally, JEDEC members would have adopted those technologies with full knowledge of Rambus's patents and royalty payments.

Response to Finding No. 1616: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel

submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1617. Complaint Counsel have failed to show that JEDEC would have adopted alternative technologies had Rambus made the additional disclosures Complaint Counsel allege should have been made.

Response to Finding No. 1617: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

1618. Because JEDEC would have adopted the same standards had Rambus made the additional disclosures Complaint Counsel allege should have been made, and because Rambus's royalty rates are reasonable and non-discriminatory, Rambus's alleged conduct has not increased its market power.

Response to Finding No. 1618: This proposed finding lacks any reference to the record, constitutes legal argument, and is inappropriate for findings of fact. Complaint Counsel submits that this finding should be disregarded pursuant to *Chicago Bridge and Iron Co.*, Docket 9300 (June 12, 2003) and this Court's July 10, 2003 Order on Post Trial Briefs.

CERTIFICATE OF SERVICE

I, Jessica Rash, hereby certify that on October 10, 2003, I caused a copy of the following materials:

1. Public Version Complain Counsel's Reply to Respondent's Proposed Findings of Fact

to be served upon the following persons:

by hand delivery to:

Hon. Stephen J. McGuire
Chief Administrative Law Judge
Federal Trade Commission
600 Pennsylvania Avenue, NW
Washington, DC 20580

and by electronic transmission and overnight courier to:

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_____
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