PUBLIC

UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

In the matter of **RAMBUS INC.,** **a corporation.**	**Docket No. 9302**

RESPONDENT RAMBUS INC.'S PROPOSED FINDINGS OF FACT AND CONCLUSIONS OF LAW

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Pursuant to Your Honor's July 10, 2003 Order on Post Trial Briefs, Respondent Rambus Inc. ("Rambus") submits these Proposed Findings of Fact and Conclusions of Law.[1]

FINDINGS OF FACT

I. INTRODUCTION.

1. There exists a standard-setting organization called the JEDEC Solid State Technology Association ("JEDEC"), which was throughout most of the 1990's an unincorporated activity within the engineering department of the Electronic Industries Association ("EIA"). (Rhoden, Tr. 289). JEDEC undertakes to adopt standards for semiconductor devices and related technologies. (Complaint, ¶ 14).

2. The particular JEDEC committee most relevant to this case is the "JC 42" committee, which has responsibility within JEDEC for many computer memory devices. (Complaint, ¶ 25). The members of JC 42 have included such computer memory manufacturers and users as Siemens (now Infineon), Micron, NEC, Samsung, Toshiba, IBM, Texas Instruments and Hewlett-Packard. (JX 10 at 1). The particular subcommittee most involved in this case is the "JC 42.3" subcommittee, whose focus throughout the 1990's was dynamic random access memory devices, or "DRAMs." (Complaint, ¶ 26).

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[1] Some of the testimony and other evidence cited herein was afforded *in camera* treatment prior to or during the trial in this matter. Accordingly, and pursuant to 16 C.F.R. § 3.45(e), this version of Rambus's Proposed Findings of Fact and Conclusions of Law is filed under seal. A public version will be filed shortly.

3. A DRAM differs from other types of memory devices in part because it is "dynamic," that is, the memory cells it contains must be refreshed periodically in order to retain their values. (Rhoden, Tr. 266-7, 279).

4. Respondent Rambus Inc. ("Rambus") is a company that, among other things, develops and licenses memory technologies to companies that manufacture semiconductor memory devices. (First Set of Stipulations, April 24, 2003, p. 1, item 1).

5. Rambus attended its first JEDEC 42.3 meeting as a guest in December 1991. (JX 10 at 2; CX 2054, Mooring Depo. Tr., 44). Rambus formally joined JEDEC in early 1992. (CX 601 at 1).

6. Rambus attended its last JEDEC 42.3 meeting in December 1995. (Crisp 8/10/01 Micron Depo. Tr., 853:18-854:1).

7. After receiving a bill for 1996 dues, Rambus sent a letter confirming its withdrawal from JEDEC in June 1996. (CX 887 at 1).

8. The Complaint in this matter asserted that, while a member of JEDEC, Rambus representatives observed efforts at JEDEC to promulgate an industry standard for a synchronous DRAM device called "SDRAM." (Complaint, ¶ 40). The Complaint asserted that Rambus should have disclosed to JEDEC that it had filed or intended to file or amend patent applications relating to certain features of the SDRAM device standardized by JEDEC. (Complaint, ¶¶ 55-56).

9. After discovery had closed, and shortly before trial began, the parties stipulated that "[p]rior to the adoption of the JEDEC SDRAM standard in 1993, Rambus

had no claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard." (First Set of Stipulations, April 24, 2003, p. 2, item 9).

10. The Complaint also alleged that JEDEC considered improvements to the SDRAM standard in the early and mid-1990s, and that these discussions ripened into the formal development of a new standard, called "DDR SDRAM," in the 1996-1999 time period. (Complaint, ¶¶ 27-28).

11. The Complaint asserted that Rambus should have disclosed to JEDEC that it had filed or intended to file or amend patent applications relating to certain features of the DDR SDRAM device standardized by JEDEC. (Complaint, ¶¶ 64-70).

12. The Complaint alleged that while it was a JEDEC member, Rambus had misled JEDEC members into believing that it had no actual or potential intellectual property claims in the technologies being considered for standardization by JEDEC. (Complaint, ¶ 71).

13. The Complaint alleged that had Rambus disclosed to JEDEC that it had filed or intended to file patent applications relating to technologies being considered for standardization, JEDEC would have incorporated alternative technologies into its standards that avoided Rambus's intellectual property claims. (Complaint, ¶¶ 62, 65, 69).

14. The Complaint asserted that by the use of "anticompetitive and exclusionary acts and practices," Rambus has obtained monopoly power in various markets and submarkets in violation of section 5 of the FTC Act, 15 U.S.C. § 45. The Complaint also

asserted that Rambus has engaged in the aforementioned acts and practices with the specific intent to monopolize various markets and submarkets, in violation of section 5 of the FTC Act. (Complaint, ¶¶ 122-3).

15. Rambus's Answer denied the material allegations of the Complaint and asserted that the evidence would show that JEDEC's rules and policies did not impose, and were not commonly understood to impose, the disclosure obligations set out in the Complaint. (Answer, pp. 1-2).

16. Rambus also asserted in its Answer that the evidence would show that it did not have, until after it had left JEDEC, any undisclosed patents or patent applications that contained claims reading on devices manufactured in accordance with any JEDEC standard. (Answer, p. 2).

17. Rambus also asserted in its Answer that the evidence would show that JEDEC did not rely on any purported silence on Rambus's part at JEDEC meetings and instead chose to adopt certain technologies because of the cost/performance advantages of those technologies and the absence of reasonable alternatives. (Answer, p. 2).

18. Rambus's Answer asserted that in light of the absence of a duty to disclose, in light of the absence of pending claims reading on JEDEC standards, and in light of the other evidence to be considered at trial, it would be clear by the close of trial that Rambus's alleged failure to disclose its potential intellectual property claims had no anticompetitive effect in any market and that Rambus had not violated section 5. (Answer, pp. 1-3).

II. PROCEDURAL BACKGROUND

19. The Complaint in this matter issued on June 18, 2002. (Complaint, p. 37, available at www.ftc.gov/os/adjpro/d9302/020618admincmp.pdf).

20. Rambus filed its Answer on July 29, 2002. (Answer, p. 49, available at www.ftc.gov/os/adjpro/d9302/020729arri.pdf).

21. An initial scheduling order was issued by Chief Administrative Law Judge James P. Timony on August 6, 2002. (Available at www.ftc.gov/os/adjpro/d9302/020806so.pdf). The Scheduling Order was subsequently amended by stipulation and order on October 31, 2002. (Available at www.ftc.gov/os/adjpro/d9302/02103aljrevisedschedulinorder.pdf).

22. After Judge Timony retired as of January 29, 2003, the matter was assigned to Chief Administrative Law Judge Stephen J. McGuire on February 28, 2003. (Available at www.ftc.gov/os/adjpro/d9302/030228ordreassigncase.pdf).

23. Trial commenced on April 30, 2003.

24. The last day on which testimony was received was August 1, 2003. The parties subsequently submitted a substantial volume of deposition designations. The trial transcript exceeded 11,000 pages.

25. The parties filed and served Proposed Findings of Fact and Conclusions of Law on September 5, 2003.

26. The parties filed and served Reply Findings of Fact and Conclusions of Law on September 26, 2003.

III. RAMBUS AND ITS INVENTIONS

A. The Computer Industry Faced A Memory Bottleneck

27. Dr. Michael Farmwald, one of the two founders of Rambus, received his bachelor's degree in mathematics from Purdue University in 1974. (Farmwald, Tr. 8058). He then went on to earn a Ph.D. in computer science from Stanford University in 1981. (Farmwald, Tr. 8059). While a graduate student at Stanford, Dr. Farmwald was in charge of a supercomputer project at Lawrence Livermore National Labs. (Farmwald, Tr. 8059). After obtaining his Ph.D, he continued to work at Livermore for four years and then founded a company called FTL (which stood for "Faster Than Light"), whose goal was to build very fast computers. (Farmwald, Tr. 8060-61). In 1988, Dr. Farmwald went to the University of Illinois to teach in the computer science department. (Farmwald, Tr. 8063-64).

28. While working as a professor at the University of Illinois, Dr. Farmwald realized that developments in microprocessor technology would lead to significant speed increases in microprocessors while memory chip performance would not keep up. (Farmwald, Tr. 8063, 8067). He recognized that the result of these trends would be a "bottleneck" – memory technology would limit computer system performance. (Farmwald, Tr. 8068-69).

29. "Moore's law," named after Intel founder Gordon Moore, predicts that processor speeds will increase by a factor of four every three years. (Farmwald, Tr. 8068). This "law" has held true for over the last two decades. (Farmwald, Tr. 8068). The

performance of DRAMs, however, was increasing at a lesser rate; while DRAMs were fast in comparison to microprocessors in the early 1980s, as an historical matter, DRAM performance had increased very slowly over time. (Farmwald, Tr. 8072).

30. Graphing predicted microprocessor speeds against memory performance, Dr. Farmwald predicted an ever increasing gap between microprocessor performance and DRAM performance. (Farmwald, Tr. 8071-73). To meet the memory needs of future microprocessors, computer designers would either have to use a large number of DRAM working in parallel or obtain faster DRAM.

31. Assuming that the predicted DRAM speeds were not improved, Dr. Farmwald projected that the number of DRAMs needed to support future microprocessors would become extremely large over time. (Farmwald, Tr. 8073).

32. The increasing number of DRAMs needed to support faster computers was also consistent with Dr. Farmwald's experience that microprocessors were demanding higher and higher bandwidth memory systems ("bandwidth" being the amount of information that can be transferred over a specific period of time). (Farmwald, Tr. 8076-79).

33. Dr. Farmwald also plotted the projected price for computers, which showed that the cost for computer systems was dropping over time. (Farmwald, Tr. 8074-75 (illustrated by DX 251)). Comparing these projected costs with the number of DRAMs that would be required to support the bandwidth needs of faster microprocessors, Dr. Farmwald knew that "there was something broken" – the costs of the thousands of

DRAMs needed at higher microprocessor speeds would prevent the decline of computer system prices. (Farmwald, Tr. 8075-76). Later, a 1992 Rambus "Corporate Backgrounder" described the issue: "One of the most serious problems is the chronic speed mismatch between processors and main memory. Designers refer to this as the memory bottleneck. The data transfer rates of memory ICs lag far behind a processor's ability to handle the data." (RX 81 at 4).

34. To meet the higher bandwidth needs of microprocessors without the overwhelming cost of thousands of DRAMs, DRAM performance had to increase at a higher rate. (Farmwald, Tr. 8076).

35. Years later, Dr. Farmwald's 1988 observations were recognized by others in the industry. For example, an April 1992 Siemens internal memorandum states that "[a]s a result of the trend toward increasingly faster RISC and CISC processors, the DRAM interface has become more and more of a problem for system developers. In order to eliminate this data transmission rate bottleneck, various competing concepts regarding the design of newer DRAMS have emerged . . . ." (RX 285A at 1).

36. Similarly, an October 1992 article published in IEEE Spectrum warned, "If the price-to-performance ratio of computer systems is to keep improving, the gap in speed between processors and memory must be closed." (RX 329 at 1). IEEE Spectrum is the overall general magazine for the IEEE, a professional organization of electronic and electrical engineers. (Prince, Tr. 8972-3). The article went on to explain that "the accepted dynamic RAM (DRAM) architectures and solutions have been pushed to their limits. A

basic change in architecture seems the only way to obtain an urgently needed increase in memory speed." (RX 329 at 1). This article reflected a general discussion within the industry in 1992 that computer companies needed faster DRAMs. (Prince, Tr. 8977-78).

37. Another article in the October 1992 IEEE Spectrum flatly stated, "If dynamic RAMs and processors are to trade data at close to top speed, the interface between them must be re-engineered. . . . None of the types of interfaces now popular can do this while conserving power and cost to the desired degree." (RX 333 at 1).

38. In February 1994, Dr. Betty Prince, a long-time consultant in the DRAM industry and the author of five books on DRAM technologies (Prince, Tr. 8970-72), wrote in an article published in IEEE Spectrum that "[t]he mismatched bandwidths of fast processors and the slower memory chips they must employ are a problem of long standing. Processors now as always require more data per unit time than many standard memory chips have been designed to provide." (RX 465 at 1). She also provided a graph showing that this performance gap was increasing over time. (RX 465 at 1). Dr. Prince agreed that the performance gap she wrote about created a bottleneck. (Prince, Tr. 8990-91).

39. Intel saw the memory bottleneck coming at least as early as 1995, and the recognition of this bottleneck prompted Intel to investigate various memory technologies in an effort to remedy the situation. (MacWilliams, Tr. 4929-30).

40. Richard Heye, the Vice President and General Manager of the Microprocessor Business Unit at AMD (Heye, Tr. 3615), analogized how the continued improvements in microprocessor performance mandate faster memory and improvements

of other parts of a computer system to placing a high-performance engine into an ill-fitting frame:

> "The best way to describe it is by analogy. Another way to look at the microprocessor, if that's your high performance of the car, and as you continue to improve and improve your engine on the car, you've got to improve the rest of the car to take advantage of that engine. So, for example, you take a Porsche engine, drop it into a Ford pick-up truck, that Ford pick-up truck is just not going to perform like a Porsche that has the exact same engine. So, all the other stuff that Porsche does to make that car run really well, Ford pick-up trucks don't have that.
>
> So, it's to the same extent, is that if the performance of my processor keeps getting better and better and better, that the components of the system which feed the microprocessor need to also get better and better and better to take advantage of the technology of the microprocessor."

(Heye, Tr. 3651-52).

B. <u>The Farmwald and Horowitz Inventions Solved the Problem</u>.

1. <u>Dr. Farmwald Enlists Dr. Horowitz</u>.

41. Determined to solve the memory bottleneck problem, in 1988, Dr. Farmwald conceived the general idea of a new memory interface and protocol (an organization of the bits and timing of bits transferred by a memory chip) that would allow a single DRAM chip to have higher performance than a board Dr. Farmwald had designed containing 320 existing DRAM chips. (Farmwald, Tr. 8086-88).

42. In order to progress beyond his initial ideas, however, Dr. Farmwald realized that he needed the assistance of an expert in circuit design. (Farmwald, Tr. 8089).

Dr. Farmwald sought the help of a former colleague – Dr. Mark Horowitz (a professor at Stanford). (Farmwald, Tr. 8089-90).

43. Dr. Horowitz had completed both his bachelors and masters degrees in electrical engineering from MIT in four years, receiving the degrees in 1978. (Horowitz, Tr. 8477). He then went on to earn a Ph.D. in integrated circuit design from Stanford University in 1983. (Horowitz, Tr. 8480). Aside from a year's leave of absence to work on what became Rambus, Dr. Horowitz has been a professor in the electrical engineering and computer science departments at Stanford University since the mid-1980s. (Horowitz, Tr. 8476). Dr. Horowitz currently holds two endowed chairs at Stanford. (Horowitz, Tr. 8482).

44. Dr. Farmwald convinced Dr. Horowitz to take a year's leave from Stanford to further explore their ideas. (Farmwald, Tr. 8092-93). Starting in the spring of 1989, the two worked from Dr. Horowitz's Palo Alto home. (Farmwald, Tr. 8093-94).

45. Dr. Horowitz's goal in working on what was to become Rambus was to build the fastest possible DRAM interface. (Horowitz, Tr. 8486). Drs. Horowitz and Farmwald determined that 500 megahertz DRAM operation might be possible, and they worked toward that goal. (Horowitz, Tr. 8505-06).

C. Farmwald And Horowitz Formed Rambus To Promote Their Inventions As An Open Standard.

46. Early on, Dr. Farmwald and Professor Horowitz recognized that any company they formed would not be able to actually manufacture the DRAM parts that they

were designing; a DRAM manufacturing facility costs a half a billion dollars. (Farmwald, Tr. 8095). Given this limitation, in order to commercialize their inventions, "the only possible business model that made any sense was to patent it, convince others to build it, and charge them royalties." (Farmwald, Tr. 8095). They formed Rambus with that limitation in mind. (Farmwald, Tr. 8247-48).

47. Rambus's "Business Strategy," as reflected in a revised business plan prepared in November 1990 by Geoff Tate, was to develop its technology and "[p]rotect the intellectual property rights to the technology through a basic, broad patent filed in all major industrial nations and follow up with additional patents on inventions created during the development of the technology. Further protect the intellectual property through signing nondisclosures with all parties exposed to the technology." (RX 1091 at 1). As that same business plan reflects, Rambus implemented this strategy by filing its original patent application in 1990. (RX 1091 at 4). The original application had "been reviewed by all partners who've signed and several others and found to be a strong, broad patent with high odds of being issued largely as filed." (RX 1091 at 4; *see also* Farmwald, Tr. 8175-76).

48. An early slide presentation that Drs. Farmwald and Horowitz used with venture capitalists set forth the business model. (RX 82 at 18; Farmwald, Tr. 8141, 8149-50). Rambus would sell its technology directly to semiconductor companies and computer companies, and it would earn revenue from consulting (working with the DRAM

companies to implement the technology) and royalties (payment for the use of Rambus's intellectual property in the resulting products). (RX 82 at 18; Farmwald, Tr. 8150).

49. Rambus's strategy was to make its technology a *de facto* standard. As Andreas Bechtelsheim, one of the founders of Sun Microsystems testified, a DRAM that is manufactured by multiple companies is a "standard" regardless of whether or not it has been officially standardized by JEDEC or some similar body. (Bechtelsheim, Tr. 5757-58). Rambus planned for its technology to be widely used throughout the industry: "It was the part everybody used. There was a specification. Everybody would implement that specification and they would all be compatible with each other, so they're standard parts you could interchange one for the other." (Farmwald, Tr. 8163).

50. To accomplish this, Rambus intended to "license it to everybody " so that every DRAM manufacturer could manufacture the part. (Farmwald, Tr. 8097). As a 1989 draft business plan explained, Rambus hoped to establish a *de facto* standard "by offering all interested DRAM and CPU vendors a sufficiently low licensing fee (2%) that it will not be worth their time and effort to attempt to circumvent or violate the patents." (RX 15 at 9). Dr. Farmwald explained, "We were going to try and find customers for our parts, big customers, and we were going to try and license all the DRAM makers to build our part to supply those customers," which would lead to *de facto* standardization. (Farmwald, Tr. 8124-25).

51. Rambus's plan was for its technology to be an "open standard"; it refused to license its technology on exclusive terms. (Farmwald, Tr. 8185; RX 25 at 16 ("Second

sources are important for all concerned")). An "open standard" in the DRAM industry is a standard for which any patents that apply to it are available on reasonable and non-discriminatory terms. (Bechtelsheim, Tr. 5897; CX 2112, Mooring Depo. at 190-91; Kelly, Tr. 1778; Rhoden, Tr. 301). Rambus wanted to avoid what happened to the Sony Betamax, which was hampered in the market by restrictive licensing. (Farmwald, Tr. 8165). Instead, Rambus's goal was to license its technology "openly and fairly to everybody so everyone is on equal footing with a relatively low royalty." (Farmwald, Tr. 8165-66).

52. To ensure that the Rambus technology was standardized, i.e., that parts from one manufacturer were interchangeable with parts from another manufacturer, Rambus planned to cooperate with its partners (i.e., the licensees who would manufacture the devices) to ensure that feedback was propagated to all partners so that everyone would use the same good ideas instead of creating customized parts. (Farmwald, Tr. 8148; RX 82 at 17).

53. Rambus and its founders believed that they had compelling, revolutionary ideas, that their patents would be significant, and that a small royalty would be palatable given the performance leap of the technology. (Farmwald, Tr. 8112-13).

54. Rambus hoped that success would come through the strength of the technology and the patents. (Farmwald, Tr. 8121-22). As the 1989 draft business plan stated, "Rambus technology provides several strong barriers to entry for potential competitors, the strongest of which are its patents and the overwhelming 'unfair' advantage its technology enjoys." (RX 15 at 9). In other words, after thoroughly considering the

technology, Drs. Farmwald and Horowitz concluded that some of their inventions were "absolutely necessary" to create fast DRAMs. (Farmwald, Tr. 8123).

55. Drs. Farmwald and Horowitz also realized that the keystone of their company would be the strength and depth of their patents. They recognized that even with a low royalty rate of 2 to 3%, manufacturers might try to get out of paying for the technology if they could. (Farmwald, Tr. 8129). Whether their patents would be "enforceable and broad enough to stop imitators" was a risk from the very beginning. (RX 15 at 19).

56. After they had fleshed out their ideas, Drs. Farmwald and Horowitz proceeded to seek funding from three prominent and well-respected Silicon Valley venture capital firms – Kleiner Perkins; Merrill, Pickard, Anderson and Eyre; and Mohr Davidow. (Farmwald, Tr. 8098-99). Kleiner Perkins hired a well-known patent attorney, Roger Borovoy, to investigate how strong Rambus's patents could be. (Farmwald, Tr. 8133-34). As Dr. Farmwald's August 28, 1989 notes show, Mr. Borovoy concluded that the Farmwald and Horowitz ideas were very significant and that potentially a lot of patents could derive from them. (CX 1702 at 3; Farmwald, Tr. 8135). Kleiner Perkins also told Rambus that the key to success was that they "had to find a number of high-volume customers and high-volume producers to produce the part so that it became the part that everybody was using" in order for Rambus to become a *de facto* standard. (Farmwald, Tr. 8140; CX 1750 at 1).

57. To this end, the Rambus inventions were designed to be produced using existing DRAM manufacturing technology. (Farmwald, Tr. 8142-43; RX 82 at 6).

58. Even early on, Rambus believed that to succeed, it needed Intel to buy into the Rambus technology. (Farmwald, Tr. 8153). Bill Davidow of Mohr Davidow arranged for Drs. Farmwald and Horowitz to present their ideas to Gordon Moore, the founder of Intel, who was very excited by their ideas and wanted Intel to work with Rambus. (Farmwald, Tr. 8154-55). All three venture capital firms saw the value of the Rambus inventions and chose to invest funds in the company. (Farmwald, Tr. 8155-56).

1. Drs. Farmwald And Horowitz Developed Numerous Inventions In Solving The Memory Bottleneck Problem.

59. In working toward their goal, Drs. Farmwald and Horowitz had to solve numerous problems. (Horowitz, Tr. 8487). They realized that current memory interfaces could not run at high speeds as a result of electrical issues, clocking issues, and issues relating to the protocol, and that they would need innovations in each of these areas in order to meet their goal. (Horowitz, Tr. 8487-88).

a. Inventions Related to Electrical Issues.

60. With respect to electrical issues, Drs. Farmwald and Horowitz needed to develop driver and receiver circuitry that could generate very high-speed signals, and they also needed to develop a bus that would allow the signals to propagate. (Farmwald, Tr. 8118-20; Horowitz, Tr. 8488).

61. Drs. Farmwald and Horowitz developed a number of solutions to the electrical issues that arose. First, they realized that reflected signals from the end of the

bus lines would be a serious problem at high speeds and conceived the idea of introducing resistors to "terminate" the bus lines and reduce reflections. (Horowitz, Tr. 8492-93).

62. Second, Drs. Farmwald and Horowitz realized that the high voltage signaling then in use would generate too much power at high speeds, and they developed low voltage signaling using a particular kind of driver called a "current mode" driver. (Farmwald, Tr. 8119, 8144-45; Horowitz, Tr. 8494-95; RX 82 at 9).

63. Third, Drs. Farmwald and Horowitz realized that they could not build a 500 MHz DRAM with current technology and so, to transmit data at the highest possible speed, they conceived the idea of transmitting and receiving data on both edges of a 250 MHz clock. (Farmwald, Tr. 8118; Horowitz, Tr. 8495-97).

b. <u>Inventions Related to Clocking Issues</u>.

64. With respect to clocking issues, Drs. Farmwald and Horowitz realized that, although current memory chips were asynchronous, they would have to develop a synchronous device with mechanisms for exercising very tight control over timing with respect to the clock to make sure that each bit of data – traveling at a very high speed – was sampled at the right time. (Horowitz, Tr. 8488-89).

65. Drs. Farmwald and Horowitz decided to design a synchronous system since the timing reference provided by a clock could be used to limit timing uncertainties in the system and allow for high speed performance. (Horowitz, Tr. 8499-8502).

66. Even in a synchronous system, however, there remain some timing uncertainties; for example, expected delays of the buffers may vary from DRAM to DRAM due to differences in their fabrication. (Horowitz, Tr. 8503-04). In order to have the highest speed possible, Drs. Farmwald and Horowitz wanted to minimize this remaining uncertainty to the extent possible; they therefore came up with the idea of using a delay locked loop (DLL) or a phase locked loop (PLL) on-chip. (Farmwald, Tr. 8118; Horowitz, Tr. 8504). Dr. Horowitz believed that a DLL or PLL circuit on the DRAM was necessary for 500 megahertz operation. (Horowitz, Tr. 8506).

c. Inventions Related to the Memory Interface Protocol.

67. With respect to the design of the protocol, additional optimizations developed for high speed operation included returning a variable amount of data in response to a request rather than a single bit of data and by putting registers and associated control circuitry directly on the DRAM. (Farmwald, Tr. 8115; Horowitz, Tr. 8489-90).

68. With respect to the protocol, Drs. Farmwald and Horowitz again came up with various innovations. As one example, they decided to put registers on the DRAM to make the interface more efficient. (Farmwald, Tr. 8115-16; Horowitz, Tr. 8506). These registers would be programmed with parameters such as the address range that a particular DRAM would respond to, or the access time of the DRAM. (Horowitz, Tr. 8507, 8509-10).

69. Drs. Farmwald and Horowitz wanted to make the access time variable for two reasons. First, if the bus were improved so that it could operate at a faster clock frequency, the access time of the DRAM could be adjusted so that it would operate with that faster clock. Second, a variable access time would allow the access times of all the DRAMs in a system to be adjusted to have the same access time. (Horowitz, Tr. 8510-11). As noted above, they conceived the idea of using a register on the DRAM to store the variable access time value. *See* Findings, ¶ 68. "Access time" and "latency" are synonymous, so variable access time includes programmable latency. (Horowitz, Tr. 8511).

70. As another example of an innovation related to the protocol, Drs. Farmwald and Horowitz allowed the response to a request to include a variable amount of data, a feature known as "variable block size" or "variable burst length." (Farmwald, Tr. 8116-17, 8146; Horowitz, Tr. 8512; RX 82 at 9).

71. In addition to the various innovations described above, Drs. Farmwald and Horowitz had to solve many other problems with other innovative solutions. (Horowitz, Tr. 8513).

2. <u>The '898 Application</u>.

72. By early 1990, Drs. Farmwald and Horowitz had put together a set of their ideas that they proceeded to describe in a patent application. (Horowitz, Tr. 8514). This patent application, serial number 07/510,898 (the "'898 application"), named

Drs. Farmwald and Horowitz as inventors and was filed on April 18, 1990. (CX 1451 at 2).

73. After the filing of the '898 application, Rambus received an 11-way restriction requirement from the PTO – that is, the Patent Examiner determined that Rambus was claiming 11 distinct categories of inventions in the '898 application. (Nusbaum, Tr. 1510).

74. After receiving the restriction requirement, Rambus elected one group of claims to prosecute in its original application and filed 10 divisional applications to pursue the other groups of claims identified in the restriction requirement. (Nusbaum, Tr. 1511).

3. The Patent Application Process

75. The main parts of a patent application are the written description, the drawings, and the claims. (Nusbaum, Tr. 1496-97). Together, these are sometimes called the patent "specification."

76. The function of a claim in a patent application is to define the boundaries of the applicant's right to exclude others from making, using, or selling the claimed invention in the event that the claim is allowed by the United States Patent and Trademark Office ("PTO"). (Nusbaum, Tr. 1497).

77. When a patent application is filed, the patent examiner reads the disclosure in the application, including the claims, to make sure that the disclosure requirements of the patent laws are satisfied and to gain an understanding of the claimed invention. (Nusbaum, Tr. 1498).

78. As discussed further below, one of these disclosure requirements, the "written description requirement" of patent law, provides that the specification must "support" the claims; that is, the specification must clearly disclose to one of ordinary skill in the art that the applicant is in possession of the inventions being claimed. *See* Findings, ¶¶ 86-87. The applicant need not claim every invention disclosed in the specification when the application is first filed. Rather, claims can be added through amendments and follow-on applications known as "continuations" and "divisionals," discussed below, so long as those later-added claims are supported by the specification as originally filed. *See* Findings ¶¶ 83-85.

79. The patent examiner then does a search of prior art to determine whether there is prior art that may invalidate the proposed claims of the application. (Nusbaum, Tr. 1498).

80. The patent examiner next compiles the various objections to or rejections of the claims in the application, if any, and sends them to the applicant in what is called an "office action." (Nusbaum, Tr. 1498).

81. The patent applicant must respond to each and every objection and rejection raised by the patent examiner in an office action. The applicant may either argue that the examiner was incorrect for legal or technical reasons, or the applicant may choose to amend the claims. (Nusbaum, Tr. 1498-9).

82. After the examiner receives the response, he may be convinced by the arguments or amendments and choose to allow the claims. If the examiner rejects the

claims again, however, that is typically a final rejection of the claims. (Nusbaum, Tr. 1499).

a. Continuation and Divisional Applications.

83. Patent applicants may file so-called "continuation" applications not only to continue the prosecution of a patent application that has received a final rejection, but also in order to obtain claims that are supported by the written description but different in scope from those in the prior application. (Nusbaum, Tr. 1513).

84. A continuation application names one or more of the inventors of an identified prior application and adds no "new matter" (*i.e.,* no subject matter not in the parent application) to the disclosure of the parent application. (Nusbaum, Tr. 1508-9).

85. A divisional application is much like a continuation application, and likewise adds no new matter to the disclosure, but typically arises when a patent examiner determines that the original or "parent" application is claiming multiple distinct inventions. (Nusbaum, Tr. 1509-10). In such a circumstance, the examiner will impose a so-called "restriction requirement," requiring that the applicant elect one group of claims, corresponding to one of the distinct inventions, to prosecute in the original application. (Nusbaum, Tr. 1510). The applicant may choose to file divisional applications directed to the groups of claims that were not elected. (*Id*.).

b. Adequacy of a Patent Application's Disclosure

86. With respect to adequacy of disclosure of a patent application, patent examiners consider three requirements that the specification must satisfy: the "written

description" requirement, the "enablement" requirement, and the "best mode" requirement.

87. The "written description" requirement provides, with respect to later added claims, that the originally filed application has to clearly disclose to one of ordinary skill in the art to which the patent pertains that the applicant was in possession of the later claimed invention as of the original filing date. (Nusbaum, Tr. 1502, 1613-14; Fliesler, Tr. 8806-09).

88. The "enablement" requirement provides that the patent application must be set forth in such full, clear, concise and exact language that a person of ordinary skill in the art is enabled to make and use the claimed invention without having to resort to undue experimentation. (Nusbaum, Tr. 1501-02).

89. The "best mode" requirement provides that an applicant must disclose the best way that he has contemplated of implementing a claimed invention. (Nusbaum, Tr. 1502).

c. Definiteness of Claims.

90. Patent examiners also consider the "definiteness" of the claims in an application. A claim in an application must particularly point out and distinctly claim the invention, that is, the words of the claim must circumscribe a particular subject matter with a reasonable degree of precision and particularity such that the bounds of the invention being claimed are reasonably precise. If the examiner determines that a claim does not satisfy this requirement, the claim will be rejected as indefinite. (Nusbaum, Tr. 1502-03).

d. The Need to Maintain the Confidentiality of Information Regarding Patent Applications.

91. Prior to 1999, patent applications were kept strictly confidential by the PTO until patent issuance. (Fliesler, Tr. 8830).

92. Patent applications are generally kept confidential by applicants for as long as possible. (Fliesler, Tr. 8829-30). Applicants have no enforceable rights until a patent issues and generally do not want to have their technology disclosed to competitors until such time as they do have enforceable patent rights. (*Id.*). In the 1990 to 1996 time frame, if a patent ultimately did not issue from an application, the application would remain secret and the applicant could retain trade secret protection over the material in the application. (Fliesler, Tr. 8836-37).

93. Companies often are wary of disclosing patent applications because to do so would be to disclose to competitors the areas of technology that the company is developing and the areas of technology for which the company is seeking patent protection. (Fliesler, Tr. 8840).

94. Even when a patent has issued from an original application – which results in disclosure of the drawings and written description – the applicant would still have reasons to keep confidential other applications claiming priority back to that original application. (Fliesler, Tr. 8837-38). It would be very valuable to a competitor to know what claims the applicant is actually pursuing in those other applications from the entirety of inventions that could be claimed based on the written description. (Fliesler, Tr. 8838, 8900-02).

95. Similarly, even if a corresponding international patent application is published, there remain business reasons for not disclosing a United States patent application, because information about the particular claims being pursued constitutes strategic business and technical information that a company would want to keep from its competitors. (Fliesler, Tr. 8840-41, 8894-96).

96. In addition, if information about pending applications were disclosed by a company to a competitor, the competitor could potentially slow down or interfere with the prosecution of the application. (Fliesler, Tr. 8841). The competitor could disclose prior art to the company, for example. Even if it is not relevant prior art, it could cause a dilemma for the company about whether the information triggered a duty to disclose prior art to the PTO, potentially confusing or delaying the patent prosecution. (Fliesler, Tr. 8841-42).

97. The competitor could also try to provoke an "interference" at the patent office – that is, a proceeding to determine which of two applicants claiming the same invention was actually the first to invent and entitled to a patent – by claiming the same invention in one of the competitor's applications. (Fliesler, Tr. 8834-35, 8842).

98. Also, disclosing information about pending applications could jeopardize an applicant's ability to get foreign patents.

99. In the United States, patents are generally awarded to the applicant who was the first to invent a given invention. (Fliesler, Tr. 8834-35). Most foreign jurisdictions, however, have a first to file rule: The first applicant to file an application that is otherwise entitled to a patent will be awarded the patent. (Fliesler, Tr. 8838-39).

100. If a competitor learned of an application before the applicant had filed all of its foreign applications, the competitor could claim to be an independent inventor and race to the foreign patent office ahead of the original applicant.

101. Martin Fliesler, a patent attorney with over 30 years of experience prosecuting patent applications, advises his clients that they should not disclose patent applications but should, instead, keep them confidential. (Fliesler, Tr. 8765-72, 8842-43).

102. If a client wants to disclose an application in the context of negotiations over an agreement (such as a license agreement or joint venture agreement) with a competitor, Mr. Fliesler advises it to follow a "tiered system" of disclosure: first, the client should disclose only the general area of the application without details, and even that level of disclosure should be done pursuant to a nondisclosure agreement; if the talks proceed, the specification of the application might be disclosed pursuant to a tighter nondisclosure agreement, but the claims would still be held back; finally, if the talks are moving forward well, the client might disclose the claims and all of the applications in the chain subject to an even tighter nondisclosure agreement. (Fliesler, Tr. 8843-45).

103. The need to keep patent applications confidential was well recognized in the semiconductor industry. JEDEC members were informed in 1992 of potential negative consequences flowing from premature disclosure of inventions. In October 1992, JC 42 Chairman Jim Townsend circulated an article entitled "Don't Lose Your Patent Rights" to members of the JC 42 committee. (CX 342 at 8). The article advises inventors to "Keep It Under Your Hat" because disclosure of an invention may waive any rights to obtain a

patent. The article states that in the United States, a disclosure made one year before filing an application can bar a patent, while in some foreign jurisdictions, any disclosure before filing an application will bar a patent. (CX 342 at 8).

104. Similarly, Robert Goodman, the CEO of Kentron, testified that Kentron's policy is to treat patent applications as trade secrets and to preserve their confidence. (Goodman, Tr. 6072). Mr. Goodman testified that when his company was asked by members of a JEDEC committee to disclose a pending patent application, Kentron resisted the request. (Goodman, Tr. 6059-60, 6067-68). Mr. Goodman viewed the request as inappropriate, and Kentron never disclosed its actual pending claims. (Goodman, Tr. 6059-60, 6070).

105. Richard Crisp was informed in 1992 of the importance of keeping patent applications confidential by Rambus's outside patent counsel, Lester Vincent. (Crisp, Tr. 3495-96). Mr. Crisp testified that he also obtained from Mr. Vincent an understanding of the potential negative consequences of disclosing patent applications:

> "I understood that companies could potentially file interference actions on our patent applications in the patent office; that in certain countries where the rules are first to file, somebody could potentially file a claim before we actually did; and that we basically would be disclosing trade secrets that could work against us in terms of our competitive position in the marketplace."

(Crisp, Tr. 3496).

106. In his letters transmitting copies of Rambus's patent applications, Mr. Vincent repeatedly reminded Mr. Crisp to "keep in mind that this information is

confidential." (CX 1951 at 2; CX 1945 at 2).

107. Mr. Crisp followed Mr. Vincent's advice and did not disclose Rambus's patent applications to third parties. (Crisp, Tr. 3496-97).

IV. THE EIA/JEDEC PATENT POLICY.

A. Introduction.

108. During much of the 1990's, JEDEC was an unincorporated standards-setting activity within the engineering department of a trade association known as the Electronic Industries Association ("EIA"). (Rhoden, Tr. 289).

109. Rambus joined JEDEC at the beginning of 1992, and it attended its last JEDEC meeting in December 1995. (CX 601 at 1; Crisp 8/10/01 Micron Depo. Tr., 853:18-854:1). Rambus did not pay its 1996 membership dues and formally notified JEDEC in June 1996 that it had withdrawn from the organization. (CX 887 at 1).

110. The Complaint asserts that Rambus was obligated by certain policies in effect while Rambus was a JEDEC member to disclose that it had filed or intended to file or amend patent applications relating to certain features of the SDRAM or DDR SDRAM devices standardized by JEDEC. (Complaint, ¶¶ 55-56).

111. Rambus asserted in its Answer that the applicable policies did not impose the disclosure obligations set out in the Complaint. (Answer, pp. 1-2).

B. The Governing (And Other) Manuals And Policies.

112. The patent disclosure policy or policies that governed JEDEC's standardization activities while Rambus was a JEDEC member were contained in various

EIA manuals, including: (1) the EIA "Legal Guides," published in March 1983 (CX 204); (2) the *Manual for Committee, Subcommittee, and Working Group Chairmen and Secretaries*, Engineering Publication EP-3-F ("EP-3-F"), published in October 1981 (RX 9); (3) the *Style Manual for Standards and Publications of EIA, TIA, and JEDEC*, EIA Engineering Publication EP-7-A ("EP-7-A"), published in August 1990 (JX 54); and (4) a revised version of EP-7-A, published in October 1995, called EP-7-B (RX 616). (Kelly, Tr. 1824-5; 1905-6; 2082-3).

113. During the time period when Rambus was a JEDEC member, EIA policies governed the conduct of JEDEC meetings and the obligations of its members. (Kelly, Tr. 1918).

114. Between 1990 (or earlier) and 1998, "JEDEC was a subpart" of the EIA that "existed inside the engineering department" of the EIA. (Rhoden, Tr. 289). *See also* EIA Manual of Organization and Procedure EP-1-J, published in June 1989 (CX 206 at 30) (organizational chart showing JEDEC's position within EIA Engineering Department).

115. JEDEC's relationship with EIA changed in 1999, when JEDEC became a more autonomous entity. (Rhoden, Tr. 667; Kelly, Tr. 1752). Prior to that time, JEDEC "fell completely under the umbrella of the EIA for legal guides." (RX 1179 at 1).

116. In addition to policy manuals published by the EIA, the Complaint cites a "Manual of Organization and Procedure" published in 1993 not by EIA but by JEDEC, which was referred to as "JEP 21-I" or simply as "21-I." (Complaint, ¶ 21).

117. EIA General Counsel John Kelly testified at trial that in the event of a conflict, the JEDEC manual was subordinate to the EIA manual. (Kelly, Tr. 1915-6).

118. Mr. Kelly also testified that to be effective, JEDEC Manual 21-I needed approval by the EIA's Engineering Department Executive Council ("EDEC"). (Kelly, Tr. 2105).

119. Mr. Kelly testified that he did not know whether JEDEC Manual 21-I had ever received EDEC approval. (Kelly, Tr. 2105).

120. No witness testified at trial that JEDEC Manual 21-I had received EDEC approval.

121. Complaint Counsel did not meet their burden of proof to show that JEDEC Manual 21-I ever became effective.

122. An earlier version of JEP 21-I, called JEP 21-H, was in effect when Rambus joined JEDEC. (CX 205 at 1; Kelly, Tr. 1914).

123. Another manual was issued in 1994 called the "JC 42 Members' Manual." (RX 507 at 1). The JC 42 Members' Manual was intended to "assist new (and established) members [of the JC 42 committee] in achieving full effectiveness in the standards making process." (RX 507 at 2).

124. Another policy in effect during the time that Rambus was a JEDEC member was called the "ANSI Patent Policy." The American National Standards Institute ("ANSI") was and is an umbrella organization that accredits standards-setting organizations, including EIA. (Kelly, Tr. 1947-8; 2074-5).

125. ANSI published "Guidelines" regarding its Patent Policy. The ANSI Patent Policy Guidelines were circulated to JEDEC 42.3 members in 1994 at the request of EIA General Counsel John Kelly. (CX 353 at 1). The ANSI Guidelines were also attached to the May 1992 JC 42.3 meeting minutes. (CX 34 at 19).

126. EIA General Counsel John Kelly caused the ANSI Patent Policy Guidelines to be circulated to JC 42.3 members in 1994 because he "thought they provided insight into the proper interpretation of the EIA and JEDEC patent policy." (Kelly, Tr. 1950).

127. EIA Manual EP-7-B, published in October 1995, provided that "[s]tandards and publications are adopted by EIA in accordance with the American National Standards Institute (ANSI) patent policy." (RX 616 at 2).

C. The Manuals And Policies That Governed JEDEC's Standardization Activities While Rambus Was A Member Encouraged, But Did Not Require, Disclosure Of Intellectual Property Interests.

128. One of the issues addressed at trial was whether the manuals and policies governing EIA/JEDEC standardization activities while Rambus was a JEDEC member *encouraged*, or instead *required*, the disclosure at certain times and in certain circumstances of a member's intellectual property interests.

1. The EIA Legal Guides Do Not Require The Disclosure Of Intellectual Property Interests.

129. The EIA Legal Guides state that they govern "all EIA engineering standardization and related programs." (CX 204 at 4).

130. The EIA Legal Guides were required to be followed by JEDEC members. (Kelly, Tr. 1829-30; CX 206 at 6).

131. The EIA Legal Guides provide that a "basic objective" of EIA standardization activity was that "[s]tandards are proposed or adopted by EIA without regard to whether their proposal or adoption may in any way involve patents on articles, materials, or processes." (CX 204 at 4). The EIA Legal Guides state that this "basic objective" applies to "all EIA engineering standardization and related programs." (CX 204 at 4).

132. The EIA Legal Guides do not contain any reference to any disclosure obligation in connection with a member's intellectual property interests. (CX 204).

2. <u>The EIA Manuals That Were In Effect When Rambus Joined JEDEC Did Not Contain Any Reference To Any Disclosure Obligation</u>.

133. The EP-3-F manual and the EP-7-A manual were in effect when Rambus joined JEDEC. (Kelly, Tr. 1824-5; 1905-6; 2082-3). Neither the EP-3-F manual nor the EP-7-A manual makes any explicit reference to an obligation on the part of EIA members or others to disclose patents or patent applications. (CX 203A; JX 54).

134. The October 1981 EIA manual known as "EP-3-F" provides in part:

> "8.3 Reference to Patented Products In EIA Standards
>
> Requirements in EIA Standards which call for the use of patented items should be avoided. No program of standardization shall refer to a product on which there is a known patent unless all the technical information covered by the patent is known to the Formulating committee,

> subcommittee or working group. The Committee Chairman must have also received a written expression from the patent holder that he is willing to license applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination. Additionally, when a known patented item is referred to in an EIA Standard, a Caution Notice, as outlined in the Style Manual, EP-7, shall appear in the EIA Standard."

(CX 203A at 11).

135. The language used in paragraph 8.3 of EP-3-F does not call for disclosure of intellectual property interests by anyone. It instead describes the approach to be implemented if a standard refers to, or calls for the use of, "known patents." (CX 203A at 11).

136. EP-3-F clearly states that *if* a standard calls for the use of a "known patent," the Committee Chairman "must" have received an assurance from the patent holder that it is willing to license the patent on reasonable and nondiscriminatory terms.

137. It is reasonable to assume that if this section of EIA Manual EP-3-F was intended to impose a mandatory obligation of patent disclosure upon a standards participant, it would have: (1) mentioned disclosure; and (2) used mandatory language such as "must." (CX 203A at 11).

138. The 1990 EIA manual known as "EP-7-A" provides in part:

> 3.4 Patented Items or Processes
>
> Avoid requirements in EIA standards that call for the exclusive use of a patented item or process. No program [of] standardization shall refer to a patented item or process unless all of the technical information covered by the patent is known to the formulating committee or working group, and the

committee chairman has received a written expression from the patent holder that one of the following conditions prevails:

(1) a license shall be made available without charge to applicants desiring to utilize the patent for the purpose of implementing the standard, or

(2) a license shall be made available to applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination.

. . . An appropriate footnote shall be included in the standard identifying the patented item and describing the conditions under which the patent holder will grant a license (see 6.5.2).

(JX 54 at 9-10).

139. The language used in paragraph 3.4 of EP-7-A does not call for disclosure of intellectual property interests by anyone. It instead describes the approach to be implemented if a standard is to refer to, or call for the exclusive use of, a patented item or process.

140. It is reasonable to assume that like EP-3-F, EIA Manual EP-7-A would have used mandatory language such as "must" if its framers had intended it to communicate to readers the existence of a mandatory disclosure obligation.

3. The ANSI Patent Policy, Which Was Officially Adopted By The EIA At Least As Early As October 1995, Does Not RequireThe Disclosure Of Intellectual Property Interests. The EIA Informed The FTC In 1996 That Its Patent Policy Did Not Require Such Disclosure.

141. The ANSI Patent Policy was officially adopted by the EIA at least as early as October 1995, when EIA Manual EP-7-B was published. (RX 616 at 2). The EP-7-B

manual provides that "[s]tandards and publications are adopted by EIA in accordance with the American National Standards Institute (ANSI) patent policy." (RX 616 at 2).

142. In a January 1996 letter to the Federal Trade Commission, the EIA stated that it "endorse[d] and follow[ed] the ANSI intellectual property rights (IPR) policy as it relates to essential patents." (RX 669 at 2). The EIA's January 1996 letter to the FTC, and its statement that the EIA "endorse[d] and follow[ed] the ANSI intellectual property rights (IPR) policy," are consistent with EIA's formal adoption of the ANSI Patent Policy in October 1995, when EP-7-B was published. (RX 616 at 2; RX 669 at 2).

143. The EIA's January 1996 letter to the FTC states that the "EIA and TIA encourage the early, voluntary disclosure of patents that relate to the standards in work." (RX 669 at 3).

144. The ANSI Patent Policy encourages, but does not require, disclosure of intellectual property interests by participants in standards-setting organizations. (Kelly, Tr. 1961).

145. The EIA's statement in the January 1996 letter to the FTC that it "encourage[d]" the "voluntary" disclosure of patents is consistent with the EIA's formal adoption of the ANSI Patent Policy in EIA Manual EP-7-B. (RX 616 at 2).

146. The EIA's statement in the January 1996 letter to the FTC that disclosure of patents by EIA members was "encouraged" and "voluntary" is wholly inconsistent with the proposition that the EIA manuals then in effect required disclosure of patents by EIA members. (RX 669 at 2).

147. By 1990, the EIA had selected Webster's Third New International Dictionary, Unabridged as the official reference guide for the language used in EIA publications and standards. (JX 54 at 3).

148. The Administrative Law Judge may and does take official notice that the definitions of "voluntary" in Webster's Third New International Dictionary include an act "performed, made, or given of one's own free will" and an act performed "without any present legal obligation to do the thing done or any such obligation that can accrue from the existing state of affairs. . . ." Webster's Third New International Dictionary, Unabridged (1986), p. 2564.

149. The January 1996 letter to the FTC was submitted on behalf of EIA and its unincorporated divisions and departments (including JEDEC), as well as on behalf of the Telecommunications Industries Association ("TIA"). (RX 669 at 5; Kelly, Tr. 2094).

150. The EIA's January 1996 letter to the FTC was reviewed and approved by EIA General Counsel John Kelly before it was sent to the FTC. (Kelly, Tr. 2092-3). Mr. Kelly's name appears in the signature block, along with the name of Mr. Dan Bart, the Vice President for Standards and Technology for both the EIA and the TIA, and the name of Mr. Paul Vishny, outside counsel for the TIA. (RX 669 at 5).

151. In July 1996, the FTC responded to the EIA's January 1996 letter in a letter signed by FTC Secretary Donald Clark. The FTC's letter states in part that:

> "EIA and TIA, following ANSI procedures, encourage the early, voluntary disclosure of patents, but do not require a certification by

> participating companies regarding potentially conflicting patent interests."

(RX 740 at 1).

152. The FTC's July 10, 1996 letter points out that the EIA's patent policy was different from the policy of the standard-setting organization involved in the *Dell* case, where the policy *did* require a certification regarding "potentially conflicting patent interests." (RX 740 at 2).

153. The FTC's statement distinguishing the EIA's patent policy from the policy at issue in the *Dell* matter, and the FTC's explanation that the differences in the two patent policies meant that the "expectations of participants in the two standard-setting processes differ," show that the FTC staff and Secretary Clark interpreted the EIA's January 1996 letter to mean what it says – that the EIA encouraged, but did not require, the disclosure by members of intellectual property interests. (RX 740 at 2; RX 669 at 2).

154. No evidence was submitted at trial that the FTC staff or Secretary Clark in fact understood from the EIA's January 1996 letter that the EIA's policies required mandatory disclosure of any intellectual property interests.

155. No evidence was submitted at trial that any EIA official had informed the FTC in 1996 that the FTC had misunderstood the "voluntary" nature of patent disclosure under the EIA's policies.

156. Complaint Counsel did not call Secretary Clark to testify at trial about the July 10, 1996 letter to the EIA and TIA.

157. On July 10, 1996, JEDEC Secretary Kenneth McGhee sent a memorandum to "JEDEC Council Members and Alternates" regarding the FTC's Final Consent Order in the *Dell* case, which memorandum stated in part that:

> "ANSI and EIA do however, encourage early, voluntary disclosure of any known essential patents."

(RX 742 at 1).

158. Mr. McGhee's July 10, 1996 memorandum is dated the same day as the FTC's July 10, 1996 letter to the EIA and TIA. (RX 742 at 1; RX 740 at 1).

159. Mr. McGhee's July 10, 1996 memorandum stating in part that the EIA "encourage[s] early, voluntary disclosure of any known essential patents" was subsequently shown to JEDEC 42.3 members. (RX 742 at 1; Calvin, Tr. 1076).

4. JEDEC Manual 21-H, Which Was In Effect When Rambus Joined JEDEC, Contains No Reference To A Disclosure Obligation.

160. JEDEC Manual of Organization and Procedure 21-H, which was in effect when Rambus joined JEDEC in 1992, provided that "JEDEC standards are adopted without regard to whether or not their adoption may involve patents on articles, materials or processes." (CX 205A at 11).

161. JEDEC manual 21-H contains no other reference to intellectual property. (CX 205A; Kelley, Tr. 2685).

5. The Application Form Used By Rambus When Joining JEDEC Contains No Reference To A Disclosure Obligation.

162. The application form that Rambus filled out when it applied to join JEDEC

says nothing about intellectual property or about its disclosure by JEDEC members. (CX 601 at 1-2).

6. JEDEC Manual 21-I, Published In October 1993, Does Refer To A Disclosure Obligation. The Record Contains No Evidence, However, That The 21-I Manual Received The Necessary EDEC Approval.

163. JEDEC Manual of Organization and Procedure 21-I, also known as "JEP 21-I," bears an October 1993 publication date. (CX 208 at 1).

164. JEP 21-I refers to an obligation on the part of committee chairpersons to "call attention to the obligation of all participants to inform the meeting of any knowledge they may have of any patents, or pending patents, that might be involved in the work they are undertaking." (CX 208 at 19).

165. JEP 21-I needed approval by the EIA's Engineering Department Executive Council ("EDEC") in order to be effective. (Kelly, Tr. 2105).

166. EIA General Counsel John Kelly testified that JEP 21-I needed a "final stamp of approval" from EDEC. (Kelly, Tr. 2105).

167. Mr. Kelly testified that he did not know one way or the other if JEP 21-I had ever received EDEC's approval. (Kelly, Tr. 2105).

168. Mr. Kelly testified that he had not intended, in responding to questions posed by Complaint Counsel, to testify that JEP 21-I had been formally approved by EDEC. (Kelly, Tr. 2105).

169. No witness testified at trial that EDEC approval of the JEP 21-I manual was ever obtained.

170. Complaint Counsel did not meet their burden to show that the JEP 21-I manual ever became effective.

171. The JEP 21-I manual states that committee chairpersons would satisfy the requirement that they call attention to a member's obligations under 21-I by showing, at committee meetings, "viewgraphs" that were contained in Appendix E of JEP 21-I. (CX 208 at 19).

172. The viewgraphs in Appendix E to the JEP 21-I manual contain no reference to the disclosure of intellectual property interests. (CX 208 at 19).

173. At the September 1993 42.3 meeting, the committee chairman showed a viewgraph containing proposed language from an appendix to the not-yet-published JEP 21-I manual. This viewgraph was expressly marked "DRAFT" and contained a footnote stating that the "material is a proposed revision" that "has not been approved by JEDEC." (JX 17 at 12). In any event, this "draft" viewgraph does not contain language requiring intellectual property disclosures by JEDEC members. (*Id*.).

174. The JEP 21-I manual also includes an "Appendix F" that is entitled "Patent Policy Application Guidelines." These guidelines state that the discussion of "pending or existing patents" is "a permissible activity." (CX 208 at 29).

175. JEP 21-I also states, in Appendix D, that JEDEC standards "are adopted without regard to whether or not their adoption may involve patents [on] articles, materials,

or processes." (CX 208 at 25).

7. The JC 42 Members' Manual Refers To A Disclosure Obligation On The Part Of Presenters.

176. Another manual that was published while Rambus was a JEDEC member was the "JC 42 Members' Manual," which bears a publication date of September 1994. (RX 507 at 1).

177. The introduction to the JC 42 Members' Manual is signed by Jim Townsend, Chair of the JC 42 Executive Committee, and states in part that "[t]his manual was compiled to assist new (and established) members in achieving full effectiveness in the standards-making process." (RX 507 at 2).

178. The JC 42 Members' Manual contains no reference to JEP 21-I. (RX 507). Instead, the JC 42 Members' Manual refers to EP-7-A and EP-3-F in reference to the "patent policy." (RX 507 at 15).

179. No witness testified at trial that the JC 42 Members' Manual had received EDEC approval.

180. According to the version of the JC 42 Members' Manual that was published in 1994, a member that was *presenting* a technology to JEDEC for standardization "must reveal any known or expected patents, *within his company*, on the material presented." (RX 507 at 15) (emphasis in original).

181. There is no evidence, and Complaint Counsel do not allege, that Rambus ever proposed or advocated the adoption of any standard or technology while a JEDEC

member. In fact, Rambus made no presentations at all, and it voted at only one meeting, when it voted *against* four proposals. (Calvin, Tr. 1071; Crisp., Tr. 3083-4; JX 13 at 9-11; Wiggers, Tr. 10590). There was also testimony by Gordon Kelley, 42.3 committee chair, that he had twice *barred* Rambus from presenting its technology for standardization at JEDEC. (Kelley, Tr. 2649-58). Kelley also testified that he had never barred any other company from making a presentation (*id.*), and that he was only empowered to do so with respect to Rambus by virtue of a completely undocumented "hand vote" at the May 1991 JC 42.3 meeting. (*Id.*).

8. JEDEC's Ballots Encouraged, But Did Not Require, Disclosure By Members Of Relevant Patents.

182. The ballots used by JEDEC to record votes on standardization proposals during the time that Rambus attended JEDEC meetings contained the phrase "If anyone receiving this ballot is aware of patents involving this ballot, please alert the committee accordingly during your voting response." (CX 252A at 2).

183. When the ballot language regarding patents was first added to JEDEC ballots, a JEDEC member asked during a JEDEC meeting about the purpose of the new language. The minutes of the JC 42.1 meeting held on September 13, 1989 state that:

> "Council discussed patent issue at their June meeting at the request of JC-42.3. The result was not to change EIA legal requirements as outlined in document EP-7, but to add some wording on JEDEC ballot voting sheets about informing the Committee if any patent covers the balloted material.
>
> TI was concerned that Committee members could be held liable if they didn't inform Committee members correctly on patent

> matters. Committee responded that the question was added on ballot voting sheets for information only and was not going to be checked to see who said what."

(CX 3 at 6).

184. The statements in the official JEDEC meeting minutes that the patent-related question on the ballot was added "for information only" and that the ballots were "not going to be checked to see who said what" are inconsistent with the proposition that the ballot language was intended to, or did, express any mandatory disclosure obligation. (CX 3 at 6).

185. Desi Rhoden, the current JEDEC Chairman and President of AMI2, testified that he understood the phrase "please alert the committee" on the ballot form to mean that a member "must" alert the Committee. (Rhoden, Tr. 582). Mr. Rhoden's testimony on this issue is not credible in light of the express statement in the JEDEC meeting minutes that the language had been added to the ballots for "information only and was not going to be checked to see who said what" and in light of the fact that the ballot form uses the term "Mandatory" to refer to *other* information sought by the ballot (CX 252a at 2), but does not use that term or any similar term with respect to patent-related information.

D. There Is Substantial Evidence That JEDEC Members And The JEDEC Leadership Understood During The Time That Rambus Was A JEDEC Member That Members Were *Encouraged*, But Not *Required*, To Make A Disclosure Of Their Intellectual Property In Certain Circumstances.

186. EIA officials stated in writing in January 1996 that the EIA "encourage[d]" the "voluntary" disclosure of patents relating to standardization efforts. (RX 669 at 2).

187. In addition, on March 29, 1994, JEDEC Secretary Ken McGhee sent a memorandum to JC 42 Chairman Jim Townsend that stated that JEDEC's "legal counsel" had said that "he didn't think it was a good idea to require people at JEDEC standards meetings to sign a document assuring anything about their company's patent rights. . . ." (RX 486 at 1).

188. Secretary McGhee's March 29, 1994 memorandum to Mr. Townsend states that legal counsel had given the "following reasons" why he did not believe that it would be a good idea to require JEDEC representatives to sign an assurance regarding their company's patent rights:

> "(1) It would have a chilling effect at future meetings.
>
> (2) A general assurance wouldn't be worth that much anyway.
>
> (3) It needs to come from a VP or higher within the company – engineers can't sign such documents.
>
> (4) It would need to be done at each meeting slowing down the business at hand."

(RX 486 at 1).

189. The statement in Secretary McGhee's March 29, 1994 memorandum that requiring a written assurance about a company's patent rights "would have a chilling effect" is inconsistent with the proposition that as of March 1994, a member's mere presence or silence at JEDEC meetings was understood by JEDEC members to constitute such an assurance.

190. The statements in Secretary McGhee's March 29, 1994 memorandum that an assurance would need to be obtained "from a VP or higher within the company" and that "engineers can't sign such documents" are inconsistent with the proposition that the engineers present at JEDEC meetings were obligated to make disclosures on behalf of their companies.

191. In a similar e-mail sent in February 2000, JEDEC Secretary Ken McGhee informed JEDEC 42.4 members that "[t]he JEDEC patent policy concerns items that are known to be patented that are included in JEDEC Standards. *Disclosure of patents is a very big issue for Committee members and cannot be required of members at meetings*." (RX 1582 at 1) (emphasis added).

192. IBM informed JEDEC members and JEDEC leaders on several occasions between 1992 and 1996 that it would not disclose its intellectual property position at JEDEC meetings. (JX 15 at 6; RX 420 at 1; JX 18 at 8; JX 19 at 4).

193. The minutes of the March 1993 meeting of JEDEC 42.3 state in part that "IBM noted that their view has been to ignore [the] patent disclosure rule because their attorneys have advised them that if they do then a listing may be construed as complete." (JX 15 at 6).

194. In an August 1993 memo to JEDEC leaders entitled "BGA Patent/License Rights," IBM JEDEC representative (and JEDEC 42.3 subcommittee chair) Gordon Kelley stated that:

> "IBM Intellectual Property Law attorneys have informed me that we will not use JEDEC as a forum for discussing this subject. It is the responsibility of the producer to evaluate the subject and to work out the proper use of rights. So, I can not confirm or deny any IPL rights."

(RX 420 at 1).

195. The December 1993 JEDEC 42.3 minutes state in part that "[a]s a side issue, IBM noted that in the future they will not come to the committee with a list of applicable patents on standards proposals. It is up to the user of the standard to discover which patents apply." (JX 18 at 8).

196. Between December 1993 and December 1995 (Rambus's last meeting), no IBM patent or patent application was added to the "patent tracking list" maintained by JC 42 Chairman Jim Townsend. (JX 18 at 14-21; JX 19 at 17-23; JX 20 at 15-18; JX 21 at 14-18; JX 22 at 12-17; JX 25 at 18-26; JX 26 at 15-24; JX 27 at 20-25; JX 28 at 12-23).

197. Several JEDEC participants testified that they had heard Gordon Kelley state that IBM would not disclose its intellectual property interests at JEDEC meetings. (Calvin, Tr. 1074-5; Rhoden, Tr. 590; Crisp, Tr. 3503-4). No witness testified that IBM was criticized for its position.

198. Rambus itself declined to comment on two separate occasions, in 1992 and 1995, when asked about its intellectual property. (Crisp, Tr. 3490; JX 27 at 26; Calvin, Tr. 1068-70; RX 297 at 1; CX 673 at 1; RX 290 at 3). There is no evidence that anyone informed Rambus on these occasions that disclosure was mandatory rather than voluntary. (*Id*.).

E. Some JEDEC Representatives Believed That No Disclosure Was Required As Long As The Member Company Ultimately Licensed Its Relevant Patents To All Comers On Reasonable Terms.

199. Hans Wiggers, a JEDEC representative from Hewlett-Packard in the early to mid 90's, testified that it was his understanding of the JEDEC patent policy that as long as a company licensed its patents after they issued on reasonable and non-discriminatory terms to all interested parties, it had no obligation under the patent policy to disclose its intellectual property. (Wiggers, Tr. 10591).

200. Gordon Kelley, a JEDEC representative from IBM who served as the chair of the 42.3 subcommittee in the early and mid-1990's, testified that he did not disclose IBM patents relating to "toggle mode" in 1990 in part because IBM was "prepared to meet the requirements of the JEDEC committee" to license the patents on reasonable and non-discriminatory terms. (Kelley, Tr. 2715-16).

201. Desi Rhoden, who is currently the Chairman of the Board of JEDEC and President of AMI2, gave similar testimony about whether intellectual property disclosures made to JEDEC by AMI2's corporate predecessor had complied with JEDEC's patent policy. Rhoden testified that a statement by AMI2's predecessor that it "might have IP relating" to its presentation and would license it "under the JEDEC patent policy" was a sufficient disclosure of the intellectual property under the policy. (Rhoden, Tr. 1304-5).

202. The January 1996 letter by EIA and TIA to the FTC also points out that "[e]ven if knowledge of a patent comes later in time due to the pending status of the patent

while the standard was being created, the important issue is the license availability to all parties on reasonable, non-discriminatory terms." (RX 669 at 4).

203. EIA General Counsel John Kelly similarly testified that there is no objection to having standards that incorporate patented technologies as long as the patents are available to all comers on reasonable and nondiscriminatory terms. (Kelly, Tr. 2072).

F. If There Were A Disclosure Requirement, It Extended Only To Issued Patents And Not To Patent Applications.

204. Assuming that JEDEC members were obligated to disclose some intellectual property interests at JEDEC meetings while Rambus was a member, Complaint Counsel did not meet their burden of proving that that obligation extended to patent applications.

1. The ANSI Patent Policy, Which Was Formally Adopted By The EIA At Least By October 1995, Does Not Require The Disclosure Of Patent Applications.

205. It was undisputed at trial that the ANSI Patent Policy does not require the disclosure of patent applications by standards participants. (Kelly, Tr. 1958; 2074).

206. The EIA officially adopted the ANSI Patent Policy at least as early as October 1995, when it published EIA Manual EP-7-B. (RX 616 at 2). The EP-7-B manual, which would have been generally available to JEDEC members after its publication (Kelly, Tr. 2082), provides that "[s]tandards and publications are adopted by EIA in accordance with the [ANSI] patent policy." (RX 616 at 2).

207. During the time that Rambus was a JEDEC member, EIA manuals and policies governed JEDEC standardization activities. (Kelly, Tr. 1918; RX 1179 at 1). In

the event of a conflict, the EIA manual would control over the JEDEC manual. (Kelly, Tr. 1915-16).

208. ANSI published "Guidelines" regarding its patent policy. The ANSI patent policy guidelines were circulated to JC 42.3 members in 1994 at the request of EIA General Counsel John Kelly. (CX 353 at 1; Kelly, Tr. 1950).

209. Mr. Kelly caused the ANSI Guidelines to be circulated to JC 42.3 members in 1994 because he "thought they provided insight into the proper interpretation of the EIA and JEDEC patent policy." (Kelly, Tr. 1950).

210. At the time that he caused the ANSI Guidelines to be circulated to JC 42.3 members, Mr. Kelly understood that the ANSI Patent Policy did not require the disclosure of patent applications. (Kelly, Tr. 2075).

211. The ANSI Guidelines themselves were one basis for Mr. Kelly's view, at the time he circulated the ANSI Guidelines to JC 42.3 members, that the ANSI Patent Policy did not require the disclosure of patent applications. (Kelly, Tr. 2077).

212. At the time that the ANSI Guidelines were circulated to JC 42.3 members in 1994, the language of the EIA patent policy and the ANSI patent policy was essentially identical. (Kelly, Tr. 2077-78).

213. The cover memorandum that accompanied the ANSI Guidelines when they were circulated to JC 42.3 members in 1994 said nothing that would have alerted recipients that the EIA, unlike ANSI, supposedly required disclosure of patent applications. (CX 353 at 1).

2. The EIA's January 1996 Comment Letter To The FTC Refers Only To Voluntary Disclosure Of Patents, Not Patent Applications.

214. The EIA's January 1996 comment letter to the FTC states that the EIA "endorse[s] and follow[s] the ANSI Intellectual Property Rights ("IPR") policy . . . ." (RX 669 at 2).

215. EIA General Counsel John Kelly reviewed and approved the EIA's January 1996 comment letter to the FTC before it was submitted, and Mr. Kelly's name and title appear in the signature block. (RX 669 at 5; Kelly, Tr. 2092-3).

216. The EIA's January 1996 comment letter to the FTC states that the "EIA and TIA encourage the early, voluntary disclosure of patents that relate to the standards in work." (RX 669 at 3). The letter does not state that the EIA requires (or even encourages) the disclosure of patent applications. (*Id.*).

217. The EIA's January 1996 comment letter to the FTC also states that ". . . if knowledge of a patent comes later in time due to the pending status of the patent while the standard was being created, the important issue is the license availability to all parties on reasonable, non-discriminatory terms." (RX 669 at 4).

218. On July 10, 1996, JEDEC Secretary Ken McGhee sent a memorandum to all JEDEC Council members and alternates that stated in part that ANSI and the EIA "encourage early, voluntary disclosure of any known essential patents." (RX 742 at 1). Mr. McGhee's memorandum does not state that ANSI or the EIA requires (or even encourages) disclosure of patent applications. (*Id.*).

3. Gordon Kelley's Testimony About The So-Called "Hand Vote" Is Not A Credible Basis For Finding A Disclosure Obligation.

219. Gordon Kelley, the IBM representative who chaired the 42.3 subcommittee and who later chaired the JEDEC Council as well, testified that he understood that the word "patent" as used in EIA manuals meant only "issued patents," not "patents and patent applications." (Kelley, Tr. 2686-7; 2696-7).

220. Mr. Kelley testified that he did not believe at any time prior to Rambus's departure from JEDEC that the EIA had changed its interpretation of the word "patents" to include "patents *and* patent applications." (Kelley, Tr. 2695; 2697).

221. Mr. Kelley testified that prior to May 1991, he did not understand that JEDEC members had any obligation to disclose patent applications relating to the work of JEDEC. (Kelley, Tr. 2686-7; 2692).

222. Mr. Kelley testified that at the May 1991 meeting of the JC 42.3 subcommittee, a "hand vote" was supposedly taken at which the subcommittee agreed to adopt a "new definition of patents" within JC 42.3. According to Mr. Kelley, the JC 42.3 members voted to include "patent applications" within the definition of "patents" and to require disclosure of both. (Kelley, Tr. 2669; 2691).

223. While Mr. Kelley initially testified that the "hand vote" occurred at the May 1992 JC 42.3 meeting, he later changed his testimony to say that it had occurred at the May 1991 meeting. (Kelley, Tr. 2669; 2691).

224. There is no reference to the "hand vote" in the May 1991 or May 1992 JC 42.3 meeting minutes. (Kelley, Tr. 2670; JX 5; CX 34).

225. Mr. Kelley agreed that it was "important" that the meeting minutes reflect that this policy change had occurred. He stated that he did not know why the "hand vote" was not mentioned in the minutes. (Kelley, Tr. 2670).

226. Mr. Kelley did not mention the "hand vote" in his IBM trip report for the May 1991 JEDEC meeting. (Kelley, Tr. 2675-6).

227. Mr. Kelley testified that there was a separate "hand vote" on the same issue at the JC 16 meeting in May 1991, although he later qualified this to say that he "believe[d]" there was a separate vote in the JC 16 meeting. (Kelley, Tr. 2670, 2676).

228. There was no written evidence presented at trial that a "hand vote" relating to the disclosure of patent applications ever occurred in a JC 42.3 or JC 16 meeting.

229. No witness other than Mr. Kelley testified that a "hand vote" relating to the disclosure of patent applications had ever occurred in a JC 42.3 or JC 16 meeting.

230. The complete absence of corroborating evidence of a "hand vote" regarding the disclosure of patent applications renders Mr. Kelley's testimony on that issue not credible.

231. There was also no evidence presented at trial that anyone ever mentioned the alleged "hand vote" to Rambus or in its presence. Rambus was not a JEDEC member when the "hand vote" supposedly occurred.

4. Complaint Counsel Did Not Prove That JEDEC Manual 21-I Ever Became Effective.

232. Although JEDEC manual 21-I refers, indirectly, to an obligation to disclose information regarding both patents and "pending patents," Complaint Counsel did not meet their burden of showing that the 21-I manual had ever become effective. (CX 208 at 19; Kelley, Tr. 2105). *See* Findings, ¶¶ 165-169.

5. The February 2000 Meeting Of The JEDEC Board Of Directors Shows That Disclosure Of Patent Applications Was Not Required.

233. Substantial evidence that JEDEC did not, in fact, require the disclosure of patent applications is found in the official minutes of the February 2000 meeting of the JEDEC Board of Directors. (RX 1570 at 13).

234. The minutes of the February 2000 meeting of the JEDEC Board of Directors state as follows:

> "D. Disclosure on Patents Pending
>
> Mr. Walther noted that Micron had sent a letter indicating they have patents pending on items that may affect committee standards. The issue was whether companies should make public that a patent is pending. The BoD discussed it and noted they encourage companies to make this kind of disclosures even though they were not required by JEDEC bylaws."

(RX 1570 at 13).

235. The February 2000 Board minutes state unambiguously that a disclosure by a JEDEC member "that a patent is pending" is "not required by JEDEC bylaws." (RX 1570 at 13). Such a disclosure is instead "encouraged." (*Id.*).

236. Although this JEDEC Board meeting occurred in 2000, no witness testified that JEDEC had *lessened* the disclosure obligations contained in the JEDEC patent policy after Rambus left JEDEC. These Board minutes are, therefore, substantial evidence that JEDEC encouraged, but did not require, the disclosure of patent applications while Rambus was a member.

237. In an e-mail written a few days after the February 2000 board meeting, JEDEC Secretary Ken McGhee, who had been present at the meeting (RX 1570 at 2), reported to a JEDEC subcommittee that the JEDEC Board had discussed Micron's "patent pending" disclosure "at their February 8 meeting." (RX 1585 at 1). Secretary McGhee stated that:

> "The JEDEC patent policy concerns items that are known to be patented that are included in JEDEC standards. Disclosure of patents is a very big issue for Committee members and cannot be required of members at meetings. However, if a company gives early disclosure on a patent they are working on, it definitely gives a lot of assurance to the Committee members regarding development of any standards affecting it.
>
> Therefore, in Micron's letter, *by giving early disclosure, they have gone one step beyond the patent policy and have complied with the spirit of the law. JEDEC encourages this type of activity from any member*."

(RX 1585 at 1) (emphasis added).

238. Secretary McGhee's February 11, 2000 e-mail corroborates the minutes of the February 2000 JEDEC Board meeting and provides further evidence that disclosure of patent applications was encouraged but not required.

6. The Disclosures That Were *Not* Made By JEDEC Members In The Early And Mid-1990s Are Further Evidence That JEDEC Members Did Not Understand That Patent Applications Had To Be Disclosed.

239. The behavior of JEDEC members also makes clear that many members did not understand that they were obligated to disclose patent applications that were related to JEDEC standard-setting work.

240. For example, a Hewlett-Packard representative to JEDEC, Mr. Hans Wiggers, testified that he had attended a JEDEC meeting where IBM representative Gordon Kelley:

> "said 'Look, I cannot disclose – my company would not let me disclose all the patents that IBM is working on because, you know, I just can't do that. The only thing we will do is we will follow the JEDEC guidelines and – or rules on whatever and we will make them available.'"

(Wiggers, Tr. 10592-93).

241. Mr. Wiggers testified that when Mr. Kelley stated his position at the JEDEC meeting regarding IBM's non-disclosure of patent applications, Mr. Wiggers told the meeting attendees that HP took the same position. (Wiggers, Tr. 10593-4).

242. In numerous other instances, although named inventors on patent applications were present at JEDEC meetings while standards relating to those applications were being discussed, the inventors did not disclose their patent applications.

a. Members of the SyncLink Consortium Did Not Disclose Pending Patent Applications.

243. On May 24, 1995, Hyundai and Mitsubishi made presentations at a meeting of the JC-42.3 subcommittee regarding a type of DRAM known as SLDRAM. (JX 26 at 10-11; Rhoden, Tr. 469-71). The minutes note that "[t]he proposal was brought to JEDEC for a pinout standard." (JX 26 at 10). The Mitsubishi presentation showed the pinout for an SLDRAM. (JC 26 at 111; Rhoden, Tr. 471).

244. At a JEDEC meeting on December 9-10, 1997, the SLDRAM pinout standard ballot was approved by the JC-42.3 subcommittee. (JX 41 at 22, 24; RX 1114 at 1; Rhoden, Tr. 1206-08).

245. United States Patent No. 6,442,644 issued on August 27, 2002. (RX 2086 at 1). Among the inventors named on the patent were JEDEC representatives Hans Wiggers of Hewlett-Packard, Kevin Ryan and Terry Lee of Micron, and Desi Rhoden, formerly of VLSI. (RX 2086 at 1). Claim 3 of the patent claims the precise SLDRAM pinout that had been standardized by JEDEC. (RX 2086 at 41; Rhoden, Tr. 1211).

246. The '644 patent claims priority to a number of provisional applications, including provisional application 60/069,092 which was filed on December 10, 1997, the very same day that the JEDEC meeting approving the SLDRAM patent was being held. (RX 2086 at 1; RX 2099-43). The '092 provisional application discloses the SLDRAM pinout claimed in the '644 patent. (RX 2099-43 at 250).

247. Messrs. Wiggers, Ryan and Rhoden were all present at the December 1997

JC-42.3 subcommittee meeting where the SLDRAM pinout standard was balloted and approved. (JX 41 at 2). They were each involved in or affiliated with the "SLDRAM Consortium" or SLDRAM Inc., which became AMI2, to whom the '644 patent has been assigned. (RX 870 at 1; Rhoden, Tr. 696-97, 1235; RX 2086 at 1). The minutes of the meeting do not indicate that any of the three disclosed the '092 provisional application. (JX 41 at 22, 24).

b. Fujitsu Did Not Disclose Pending Patent Applications.

248. The Complaint in this matter alleges that Rambus should have disclosed pending patent claims to "on-chip PLL/DLL technology" and that such technology was ultimately incorporated into the DDR SDRAM standard that was adopted in August 1999. (Complaint at 64).

249. The Court has taken official notice of United States Patent No. 6,028,816, which issued on February 22, 2000 and is assigned to Fujitsu. The application for the '816 patent was filed on September 5, 1997 (although the patent claims priority back to a number of Japanese patent applications filed earlier in 1997 and in 1996). ('816 patent at 1). The '816 patent has claims directed to a semiconductor device, such as a DRAM, with "an input timing adjusting circuit" for receiving an external clock signal and outputting and adjusting the phase of an internal clock signal. ('816 patent at 101).

250. As Complaint Counsel's technical expert, Professor Bruce Jacob explained in the context of describing an NEC presentation, a PLL is a timing adjustment circuit that "can be used to synchronize an external clock and an internal clock." (Jacob, Tr. 5533-34).

251. One of the inventors of the '816 patent, Masao Nakano, was present at meetings 81-85, spanning December 11, 1996 through December 9, 1997, of the JEDEC 42.3 Subcommittee. (JX 35 at 2; JX 36 at 2; JX 38 at 2; JX 40 at 2; JX 41 at 2). On-chip PLLs or DLLs were discussed at these meetings. For example, at the December 1996 meeting, Fujitsu made a presentation on DDR SDRAMs including an "internal DLL circuit." (JX 35 at 34). However, the minutes do not reflect that Mr. Nakano disclosed his pending patent application.

c. IBM Did Not Disclose Pending Patent Applications.

252. The Court has taken official notice of United States Patent No. 6,289,413, which issued on September 11, 2001 and is assigned to IBM. The '413 patent claims priority to an application filed on October 18, 1996. ('413 patent at 1). Claim 1 of the '413 patent claims a "cached SDRAM" device including means for programming the device to operate in "Write Transfer mode" or "No Write Transfer mode" during a write cycle. ('413 patent at 21).

253. At meeting No. 86 of the JEDEC JC-42.3 Subcommittee on March 3, 1998, a "No Write Transfer mode" for a cached SDRAM known as ESDRAM was balloted. (JX 42 at 10). The "No Write Transfer mode" was ultimately incorporated into the JEDEC

standard for ESDRAM – Section 3.11.5.3.5 of standard 21-C provides for a programming such a mode in which write data is not written to the cache. (CX 234 at 180).

254. Jim Rogers, one of the inventors of the '413 patent, was present during meeting No. 86, but the minutes do not reflect that he disclosed his pending application. (JX 42 at 2, 10).

d. Micron Did Not Disclose Pending Patent Applications.

255. The Court has taken official notice of United States Patent No. 5,526,320, entitled "Burst EDO Memory Device," which issued on June 11, 1996 and is assigned to Micron. The application for the '320 patent, application serial no. 370,761, was filed on December 23, 1994. ('320 patent at 1). Approximately 20 patents have issued that claim priority to the '761 application. (Williams, Tr. 934).

256. In connection with the prosecution of the '320 patent, Micron submitted to the Patent and Trademark Office a JEDEC presentation by OKI Electronics Industries in September 1994 and another JEDEC presentation by Toshiba in December 1994 as material to the application. (Williams, Tr. 926–928).

257. Brett Williams of Micron put together a presentation on Burst EDO that was presented at a January 1995 JEDEC DRAM Task Group Meeting. (JX 23 at 68-77; Williams, Tr. 825-26). Mr. Williams is an inventor on the '320 patent and was present at the January 1995 meeting. (JX 23 at 1; '320 patent at 1). Mr. Williams was aware that Micron's Burst EDO patent application was not listed on the patent tracking list shown at

the January 1995 meeting. (Williams, Tr. 963-64). Nevertheless, Mr. Williams did not disclose his pending application. (Williams, Tr. 964-65).

258. Burst EDO was passed unanimously as a JEDEC standard in March 1995. (RX 585 at 1; Williams, Tr. 929-31). Micron did not disclose its pending patent application on Burst EDO in connection with that vote. (RX 585 at 3-4; Williams, Tr. 936-37).

e. Mitsubishi Did Not Disclose Pending Patent Applications.

259. The Court has taken official notice of United States Patent No. 6,356,484, which issued on March 12, 2002 and is assigned to Mitsubishi. The '484 patent claims priority to an application filed on April 15, 1992. ('484 patent at 1). The '484 patent claims a synchronous memory device that takes "an external signal in response to rising and falling edges of the single clock signal." ('484 patent at 276).

260. One of the inventors of the '917 application, Hisashi Iwamoto, attended meeting no. 90 of JEDEC's 42.3 Subcommittee in March 1999. (JX 46 at 2). Although there were numerous presentations related to DDR SDRAMs at that meeting, Mr. Iwamoto did not disclose his pending application. (JX 46 at 9-13, 17-18).

f. Samsung Did Not Disclose Pending Patent Applications.

261. United States Patent No. 5,835,956 issued on November 10, 1998 and is assigned to Samsung. (RX 1308). The '956 patent claims priority to a United States application filed on October 4, 1993, and earlier Korean applications dating to October 2,

1992. (RX 1308 at 1). The '956 patent has claims directed at "[a] synchronous memory device capable of receiving latency mode information to select one of a plurality of latency modes." (RX 1308 at 90).

262. The Court has taken official notice of U.S. Patent No. 5,838,990 which claims priority to the same United States and Korean applications as the '956 patent. ('956 patent at 1). Claim 1 of the '990 patent claims a semiconductor memory containing "code registers" which "store a code in response to the mode set signal, wherein the codes determine the operation modes of the semiconductor memory. ('990 patent at 90). Dependent claim 2 of the '990 patent specifies that the codes in the code registers determine "a burst length mode." (*Id.*). Dependent claim 4 of the '990 patent specifies that the codes in the code registers determine "a latency mode." (*Id.*).

263. SDRAMs have a "mode register" containing binary codes that determine burst length and CAS latency. (JX 56 at 114).

264. One of the inventors of the '956 and '990 patents, Yun Ho Choi, attended JC-42.3 meetings at which SDRAMs were discussed in December 1991, February 1992, December 1992, September 1993 and December 1995. (JX 10 at 2; JX 12 at 2; JX 14 at 2; JX 17 at 2; JX 28 at 2). Yet, the minutes do not reflect that Mr. Choi disclosed the existence of his patent applications. As of December 1995, there were no Samsung patents or patent applications listed on the patent tracking list. (JX 28 at 15-18).

g. Texas Instruments Did Not Disclose Pending Patent Applications.

265. The Court has taken official notice of United States Patent No. 5,808,958 which issued on September 15, 1998 and is assigned to Texas Instruments. The '958 application claims priority to an application filed on April 23, 1991. ('958 patent at 1). The '958 patent has claims directed to a synchronous random access memory with an "output circuit for producing a predetermined number of data bits from the storage cells." ('958 patent at 22).

266. SDRAMs have a programmable burst length feature that results in the production of a predetermined number of data bits from the storage cells depending on the value stored in a mode register. (Rhoden, Tr. 380, 392; CX 234 at 150).

267. The Court has taken official notice of United States Patent No. 5,982,694, which lists the same inventors as the '958 patent and claims priority to an application filed on October 21, 1994. (RX 2310 at 1). The '694 patent has claims directed to a synchronous random access memory that outputs data on both "the positive-going edge of the system clock signal" and "the negative-going edge of the system clock signal." (RX 2310 at 21-22).

268. DDR SDRAMs output data on both the positive-going, or rising, edge of the system clock signal and the negative-going, or falling, edge of the system clock signal. (Rhoden, Tr. 389).

269. Four of the inventors of the '958 and '694 patents, Wilbur Vogley, Anthony

Balistreri, Joseph Hartigan, and Roger Norwood, were regular attendees of JC 42.3 subcommittee meetings. For example, Mr. Hartigan, who became Texas Instruments' JEDEC representative, was at various meetings between July 1992 and September 1997. (JX 13 at 2; JX 40 at 1) Mr. Vogley was at a number of meetings including March 1995 and March 1996. (JX 25 at 2; JX 31 at 2). Neither the various meeting minutes nor the patent tracking list reflect the disclosure of the applications that led to the '958 and '964 patents. (JX 28 at 15-18).

h. Toshiba Did Not Disclose Pending Patent Applications.

270. The Court has taken official notice of United States Patent No. 5,986,968, which issued on November 16, 1999 and is assigned to Toshiba. The '968 patent claims priority to a United States application filed on March 16, 1993 and an earlier Japanese application filed on March 19, 1992. ('968 patent at 1). Claim 42 of U.S. Patent No. 5,986,968 claims a semiconductor device comprising a "memory array," "control means" for outputting data N clock cycles ("latency N") after receiving a read command, and "programming means for variably programming the latency N." ('968 patent at 18).

271. SDRAMs contain a programmable latency feature whereby latency is programmed in the mode register. (CX 234 at 150; Rhoden, Tr. 393-94).

272. One of the inventors of the '968 patent, Hitoshi Kuyama, attended the May 1992 meeting of the JC-42.3 subcommittee. (CX 34 at 2). Presentations relating to programmable latency were made at that meeting, but the minutes do not reflect that

Mr. Kuyama disclosed his pending application and the application does not appear on the patent tracking list. (CX 34 at 59; JX 28 at 15-18).

i. Summary.

273. The evidence thus shows that numerous JEDEC attendees who were aware of patent applications (because they were named inventors on those applications) that were related to JEDEC's standard-setting work did not disclose those applications. This evidence supports the conclusion that JEDEC members did not understand that they were required to disclose such applications before they became issued patents.

G. The EIA/JEDEC Patent Policy At Most Required Disclosure Of "Essential" Patents.

274. Assuming that JEDEC members were obligated to disclose some intellectual property interests at JEDEC meetings while Rambus was a member, the evidence shows that that obligation could have extended only to patents that were "essential" to a standard, *i.e.*, those patents that were necessary for the manufacture or use of a product that complied with the standard.

275. EIA Manual EP-3-F refers only to standards that "*call for the use* of patented items." (CX 203A at 11) (emphasis added).

276. EIA Manual EP-7-A refers only to standards "that *call for the exclusive use* of a patented item or process." (JX 54 at 9) (emphasis added).

277. The EIA's January 1996 letter to the FTC states that the EIA "follows the

ANSI intellectual property rights (IPR) policy as it relates to *essential* patents." (RX 669 at 2) (emphasis added).

278. JEDEC Secretary Ken McGhee's July 10, 1996 memorandum to JEDEC Council members and alternates states that the EIA encourages disclosure of "known *essential* patents." (RX 742 at 1) (emphasis added).

279. JEDEC's policy manual JEP 21-I similarly refers only to standards that "*require the use* of patented items." (CX 208 at 19) (emphasis added).

280. When writing on behalf of the EIA in August 1995 to an EIA member called Echelon, EIA General Counsel John Kelly explained that the "ANSI and EIA patent policy . . . requires an SDO to secure a commitment to license a patented item or process from a patent holder when a standard refers to a patented technology *or, as a practical matter, conformance to a standard requires use of the patented technology*." (RX 2299 at 2) (emphasis added).

281. Infineon's JEDEC representative Willi Meyer testified that it was his understanding the disclosure duty applied only to patents "related to the work at JEDEC in the sense that it described features that were *necessary to meet the standard*." (Meyer, 5/7/01 *Infineon* Trial Tr. at 117:12-14) (emphasis added).

282. A Hewlett-Packard JEDEC representative, Thomas Landgraf, testified that he understood the patent policy to involve disclosure if "the standard required someone else's idea to be used . . . in order for it to operate." (Landgraf, Tr. 1693-5).

283. Another Hewlett-Packard JEDEC representative, Ilan Krashinsky, testified that he had not disclosed any Hewlett-Packard patents to JEDEC because he did not think that they were "infringed" by any JEDEC standards proposals. (Krashinsky, Tr. 2848-9).

284. JEDEC 42.3 subcommittee chairman and IBM representative Gordon Kelley testified that the disclosure duty was triggered by a patent claim that "reads on or applies" to the standard, meaning that "if you exercise the design or production of the component that was being standardized [it] would require use of the patent." (Kelley, Tr. 2706-7).

285. Another IBM JEDEC representative, Mark Kellogg, testified that his understanding was that "you have to disclose intellectual property that reads on the standard." (Kellogg, Tr. 5310-1). Mr. Kellogg also stated that "[s]ometimes we disclose intellectual property that doesn't [read on the standard] and one would question why. It adds confusion." (Kellogg, Tr. 5311).

H. JEDEC Members Were Not Required To Disclose Foreign Patents Or Foreign Patent Applications.

286. It is undisputed in this case that JEDEC "does not require its members to disclose foreign patents." (Complaint Counsel's Pre-Trial Brief, p. 259).

287. Siemens' JEDEC representative Willi Meyer testified that "[n]obody disclosed European patents" at JEDEC meetings. (Meyer, 5/7/01 Infineon Trial Tr., p. 119:3).

I. If Disclosure Of Intellectual Property Interests Was Required, It Was Required Only When JEDEC Participants Had "Actual Knowledge" Of The Intellectual Property And Its Relationship To JEDEC Standardization.

288. Assuming that JEDEC members were obligated to disclose some intellectual property interests at JEDEC meetings while Rambus was a member, the evidence shows that that obligation was triggered by the "actual knowledge" of the JEDEC representative of the intellectual property and its relationship to a standard.

289. JEDEC Board Chairman Desi Rhoden testified that the disclosure obligations under the JEDEC patent policy were "triggered by the actual knowledge of the people that were involved. . . ." (Rhoden, Tr. 624).

290. EIA General Counsel John Kelly testified that the disclosure obligations applied "to all participants with actual knowledge." (Kelly, Tr. 1970).

291. Mr. Kelly explained some of the reasons for the "actual knowledge" requirement:

> "Q. . . . you'd agree with me that EIA doesn't want people giving false information in patent disclosures?
> A. Absolutely.
>
> Q. And they want the information that comes in to be true and accurate?
> A. And open and honest and good faith, yes.
>
> Q. And that's one of the reasons that you've talked before about actual knowledge on the part of the representative?
> A. That's correct.

Q. And that the representative needs to have that actual knowledge so that they can make a truthful and accurate disclosure of IP to the committee?
A. That is correct."

(Kelly, Tr. 2171-2).

292. Mr. Rhoden did not know what obligation might exist where a representative had a *question* about whether his company might have intellectual property interests relating to a particular feature under discussion, but did not know if those interests existed. (Rhoden, Tr. 625).

293. No witness testified that a JEDEC representative who had a question about whether his company might have intellectual property interests relating to a feature under discussion at JEDEC meetings had an obligation to disclose that he had that question.

294. It was undisputed at trial that JEDEC representatives had no obligation to do any investigation, research or inquiry of their company or its lawyers regarding possible intellectual property interests relating to JEDEC work. (Rhoden, Tr. 623-4; Kelley, Tr. 2451, 2700; Kelly, Tr. 1966-68; Meyer 12/13/00 Depo. Tr., 188:24-189:18).

295. The EIA's January 10, 1996 comment letter to the FTC also spoke to the "actual knowledge" requirement and noted the "chilling effect" that a broader disclosure obligation would have:

> "EIA and TIA strongly agree that the FTC must limit the application of the *Dell* rule to cases involving *actual knowledge* of the existence of a patent and intentional failure to disclose the patent interest. Extending *Dell* to situations involving negligent failure to disclose or imputed knowledge

> ('should have known') of the existence of a patent interest would have a profound chilling effect on companies that participate in the process of voluntary standard development."

(RX 669 at 3) (emphasis added).

J. If Disclosure Of Intellectual Property Interests Was Required, It Was Required Only At The Time Of Balloting.

296. Assuming that JEDEC members were obligated to disclose some intellectual property interests at JEDEC meetings while Rambus was a member, the evidence shows that that obligation was not triggered until the time that a proposal was balloted for approval.

297. JC 42.3 Committee Chairman Gordon Kelley testified that as he understood the JEDEC patent policy, disclosure was required only at the time of balloting, although it was encouraged earlier in the process. (Kelley, Tr. 2707).

298. Siemens JEDEC representative Willi Meyer testified (via deposition) that although it was "good practice" to notify the committee before balloting, "the ballot was considered the deadline when it should have been done." (CX 2057, Meyer 12/13/00 Depo. Tr., p. 211). Cray's JEDEC representative, Alan Grossmeier, agreed. (Grossmeier, Tr. 10945). The viewgraphs that were routinely shown at JC 42.3 meetings reinforced this view, since they ask the committee chair to "resolve patent status prior to (choose one)," followed by a list of events, almost all of which relate to balloting. (*See, e.g.*, JX 20 at 15-18; JX 21 at 14-18; JX 22 at 12-17).

299. EIA General Counsel John Kelly testified that ". . . the participant needs to

exercise some judgment" on the question of when a disclosure requirement was triggered. (Kelly, Tr. 1981). According to Mr. Kelly,

> "[T]here's a gray area there where, to put it this way, the standard is evolving, their IP may be evolving, and the question is, is there a sufficient relationship between the IP – if this is what you're driving at – the IP and the work on the committee to trigger that duty to disclose? So, there's a – there's an area of judgment, and the area of judgment is probably more apparent earlier in the process and less apparent later in the process, and in theory – again, if this is what you're driving at, and I thought it was where you were going – at some point when there's an issued patent and the work on the committee is complete, the judgmental area becomes much narrower, and there may, in fact, be very little judgment involved by the participant in whether they are sufficient knowledge to trigger the duty to disclose."

(Kelly, Tr. 1981).

300. As Kelly's testimony points out, even assuming that there is a disclosure requirement for patent applications, its implementation involves "gray area[s]" and the exercise of "judgment" on the part of the participant, especially where the standard is still "evolving." (Kelly, Tr. 1981).

K. <u>Summary Of Findings Regarding Patent Policy Issues</u>.

301. The manuals and policies that governed JEDEC's standardization activities while Rambus was a member encouraged, but did not require, disclosure of intellectual property interests.

302. The EIA legal guides do not require the disclosure of intellectual property interests.

303. The EIA manuals in effect prior to June 1996 contained no reference to any disclosure obligation.

304. The ANSI patent policy, which was officially adopted by the EIA at least as early as October 1995, encouraged but did not require the disclosure of intellectual property interests.

305. JEDEC manual 21-H, which was in effect when Rambus joined JEDEC and when the SDRAM standard was adopted in 1993, contains no reference to a disclosure obligation.

306. JEDEC manual 21-H, which was in effect when Rambus joined JEDEC in 1992 and when the SDRAM standard was adopted in 1993, states that JEDEC standards "are adopted without regard to whether or not their adoption may involve patents on articles, materials or processes."

307. The application form used by Rambus when joining JEDEC contains no reference to a disclosure obligation.

308. JEDEC manual 21-I, published in October 1993, does refer – indirectly – to a disclosure obligation. Complaint Counsel did not show, however, that the 21-I manual had ever received the necessary EDEC approval.

309. The appendices contained in the 21-I manual that relate to intellectual property state only that discussion of patent applications is "permissible," and do not state that any such discussion is required.

310. The JC 42 members' manual refers to a disclosure obligation on the part of presenters. Rambus made no presentations to JEDEC.

311. JEDEC's ballot forms encouraged, but did not require, disclosure by members of relevant patents.

312. There is substantial evidence that JEDEC members and the JEDEC leadership understood during the time that Rambus was a JEDEC member that members were encouraged, but not required, to make a disclosure of their intellectual property.

313. Some JEDEC representatives believed that no disclosure was required as long as the member company ultimately licensed its relevant patents to all comers on reasonable terms.

314. If there were a disclosure requirement, it extended only to issued patents and not to patent applications.

315. If there were a disclosure requirement, it was only triggered by the "actual knowledge" of the JEDEC representative himself.

316. The EIA/JEDEC patent policy at most required disclosure of "essential" patents.

317. If disclosure of intellectual property interests was required, it was required only at the time of balloting.

V. RAMBUS DID NOT VIOLATE ANY EIA/JEDEC RULES.

A. Introduction And Summary Of Findings.

318. Because the EIA/JEDEC patent policies in effect while Rambus was a JEDEC member encouraged, but did not require, a member to disclose its intellectual property interests, Rambus's alleged non-disclosure violated no policies or rules.

319. If the EIA/JEDEC patent policies in effect while Rambus was a JEDEC member did require disclosure of intellectual property interests, but required such disclosure only by *presenters* who were trying to encourage JEDEC's adoption of a particular technology, Rambus violated no policies or rules, for Complaint Counsel have not proved that Rambus made any such presentations.

320. If the EIA/JEDEC patent policies in effect while Rambus was a member required disclosure of intellectual property interests only by members who did not license their patents on reasonable and non-discriminatory terms, then Rambus violated no policies or rules, for Complaint Counsel have not proved that Rambus's license terms are unreasonable or discriminatory. *See* Findings ¶¶ 1359-1420.

321. If the EIA/JEDEC patent policies in effect while Rambus was a member required disclosure only of issued patents (and not patent applications) that read on or were "essential" to the use of technology proposed for standardization, then Rambus violated no policies or rules, for Complaint Counsel have not proved that Rambus had any such patents. *See* Findings ¶¶ 327-360.

322. If the EIA/JEDEC patent policies in effect while Rambus was a member required disclosure of both patents *and* patent applications that read on or were "essential" to the use of a technology proposed for standardization, then Rambus violated no policies or rules, for Complaint Counsel have not proved that Rambus had any such patents or patent applications. *See* Findings ¶¶ 361-396.

323. If the EIA/JEDEC patent policies in effect while Rambus was a member required disclosure of patents and/or patent applications where the JEDEC representative had "actual knowledge" that the claims of the patent or application covered the technology proposed for standardization, then Rambus violated no policies or rules, for Complaint Counsel have not proved that Rambus's representatives had any such knowledge. *See* Findings ¶¶ 417-431.

324. If the EIA/JEDEC patent policies in effect while Rambus was a member required disclosure of intellectual property interests at the time of balloting, as JC 42.3 Chairman Gordon Kelley testified, then Rambus could not have violated any policy or rule except as to programmable latency and programmable burst, for those are the only two features complained of by Complaint Counsel that were balloted while Rambus was a JEDEC member. *See* Findings ¶¶ 397-416.

325. Rambus did not violate any JEDEC rule or policy simply by seeking or obtaining patent protection for inventions that related to JEDEC standards, for no rule or policy prohibited such patents. *See* Findings ¶¶ 432-443.

326. Complaint Counsel have not met their burden of showing that Rambus intentionally sought to violate any patent policy governing its conduct as a JEDEC member. *See* Findings, ¶¶ 417-431, 444-463.

B. While It Was A JEDEC Member, Rambus Never Had Any Intellectual Property Interests That It Was Required To Disclose To JEDEC.

1. Rambus Had No Undisclosed Patents That It Was Required To Disclose To JEDEC.

327. The parties stipulated that as of January 1996, Rambus held no issued U.S. patents that were essential to the manufacture or use of any device manufactured in compliance with any JEDEC standard. (The Parties' First Set of Stipulations, Stipulation 10).

328. The only patent that Complaint Counsel allege should have been disclosed to JEDEC by Rambus is U.S. Patent 5,513,327 (the '327 patent). Complaint Counsel allege that disclosure of the '327 patent was required because, they say, claims 1 and 7 of the patent could have been reasonably construed by an engineer to cover a JEDEC-compliant SDRAM that also incorporated certain dual-edged clocking proposals and because those claims would, they say, read on the JEDEC DDR SDRAM standard. (Jacob, Tr. 5541-49, 5551-60). The proposals or presentations that Complaint Counsel raise in this regard are: (1) a presentation by William Hardell of IBM referenced in the May 1992 minutes of the JEDEC 42.3 subcommittee (the "Hardell presentation") (CX 34 at 32; Jacob, Tr. 5542), (2) a "Future SDRAM Features Survey Ballot" referenced in the

December 1995 minutes of the JEDEC 42.3 subcommittee (the "Survey Ballot") (JX 28 at 34-35; Jacob, Tr. 5543-44), and (3) a presentation by Samsung entitled "Future SDRAM," referenced in the March 1996 minutes of the JEDEC 42.3 subcommittee (the "Samsung presentation") (JX 31 at 71; Jacob, Tr. 5544).

329. The '327 patent issued on April 30, 1996 and was publicly available as of that date. (CX 1494 at 1). All of the proposals or presentations referenced by Complaint Counsel as supposedly triggering a disclosure obligation with respect to the '327 patent were made *before* the '327 patent issued.

330. None of the proposals or presentations referenced by Complaint Counsel as triggering a disclosure obligation with respect to the '327 patent were balloted for approval at JEDEC while Rambus was a member.

331. Complaint Counsel did not show that Rambus's JEDEC representative had actual knowledge of the claim of the '327 patent at the time of the proposals or presentations that supposedly triggered a disclosure obligation with respect to the '327 patent.

332. Complaint Counsel's patent law expert, Mark Nusbaum, did not testify as to whether claims of the '327 related to JEDEC work.

333. Professor Jacob, who did testify regarding the alleged relationship between the '327 patent and JEDEC work, has no patents to his name and has never previously done any claims analysis of the type he presented in this matter with respect to the '327

patent. (Jacob, Tr. 5624, 5650).

334. In order to show that a claim of a patent would cover a JEDEC-compliant device, it is necessary to show that all of the elements or "limitations" in the claim are found in that device. (Nusbaum, Tr. 1565-66). If there are limitations in the claim that are not found in a JEDEC-compliant device, then there would be no infringement of the claim. (Nusbaum, Tr. 1625).

a. The Relevant Claims of the '327 Patent Contain Various Limitations.

335. As Professor Jacob concedes, Claim 1 of the '327 patent "describes a specific implementation" of dual edge clocking, including the "implementation detail" that the DRAM contains two input receivers with one receiver latching information in response to the rising edge of a clock signal and the other receiver latching information in response to the falling edge of the clock signal. (CX 1494 at 23; Jacob, Tr. 5546-47).

336. Professor Jacob also concedes that claim 7 of the '327 patent describes a specific implementation of dual edged clocking where the DRAM "toggle[s] between two output drivers through a multiplexer." (CX 1494 at 23; Jacob, Tr. 5548).

b. The Hardell Presentation Triggered No Disclosure Obligation With Respect To The '327 Patent.

337. The Hardell presentation related to IBM's "toggle mode" DRAM. (Kelley, Tr. 2514). IBM's toggle mode was an asynchronous design. (Jacob, Tr. 5608; Soderman, Tr. 9398; Sussman, Tr. 1472).

338. The Hardell presentation noted that it has "A-Synchronous RAS/CAS." (CX 34 at 32). This makes it an asynchronous DRAM, according to Professor Jacob's definition of asynchronous DRAMs as "those who are driven off the RAS and CAS signals where the RAS and CAS actually control the operation of the DRAM rather than a clock." (Jacob, Tr. 5394).

339. Claims 1 and 7 of the '327 patent cannot be construed as covering a JEDEC-compliant SDRAM that also incorporated dual-edge clocking as described in the Hardell presentation because such a device cannot exist. JEDEC-compliant SDRAMs are synchronous DRAMs with synchronous RAS and CAS signals; the Hardell presentation described an asynchronous DRAM with an asynchronous RAS/CAS interface. (CX 34 at 30-32).

340. The Hardell presentation gave no details about implementation of the dual-edged clocking feature, stating simply: "dual clock edge." (CX 34 at 32).

341. The Hardell presentation was referenced in a memorandum discussing presentations at a meeting of a task group in Dallas in April 1992. (CX 34 at 4, 30). There was no evidence at trial that the Hardell presentation was ever balloted at JEDEC.

342. Complaint Counsel did not show that a Rambus JEDEC representative had actual knowledge of the claims of the '327 patent (or any related application that led to the issuance of the '327 patent) at the time of the Hardell presentation.

c. The Survey Ballot.

343. The Survey Ballot was presented to JEDEC members as a survey to determine what features JEDEC members might want to include in future DRAMs. (JX 28 at 34-48).

344. The Survey Ballot was circulated on or about October 30, 1995. (CX 260; Lee, Tr. 6636).

345. The Survey Ballot was circulated shortly *after* the September 1995 JEDEC meeting, at which Rambus made the statement that: "Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property." (RX 602 at 1; JX 27 at 4, 26).

346. Several witnesses testified that in their understanding, survey ballots were for information only and triggered no patent disclosure obligations of any kind. (Rhoden, Tr. 480, 587; Kelley, Tr. 2701; Crisp, Tr. 3517).

347. With respect to dual-edge clocking, the result of the Survey Ballot was that there was "mixed support" for "using both edges of the clock for sampling inputs." (JX 28 at 35). The Survey Ballot provided no further details of the implementation of dual-edge clocking.

348. Complaint Counsel did not show that a Rambus JEDEC representative had actual knowledge of the claims of the '327 patent (or any related application that led to

the issuance of the '327 patent) at the time of the Survey Ballot.

d. The Samsung Presentation.

349. With respect to dual-edge clocking, the Samsung presentation stated only that "Data in sampled at both edge of Clock into memory." (JX 31 at 71). No further details of the implementation of dual edge clocking were provided.

350. There was no evidence at trial that the Samsung presentation was ever balloted at JEDEC.

351. Complaint Counsel did not show that a Rambus JEDEC representative had actual knowledge of the claims of the '327 patent (or any related application that led to the issuance of the '327 patent) at the time of the Samsung presentation.

e. Claims 1 and 7 of the '327 Patent Do Not Cover the Presentations Raised by Complaint Counsel.

352. Claim 1 of the '327 patent cannot be construed as covering a JEDEC-compliant SDRAM that also incorporated dual-edge clocking as described in the Hardell presentation, the Survey Ballot, or the Samsung presentation, because none of those presentations provided any implementation details and because none included the implementation details required by claim 1.

353. Claim 7 of the '327 patent cannot be construed as covering a JEDEC-compliant SDRAM that also incorporated dual-edge clocking as described in the Hardell presentation, the Survey Ballot, or the Samsung presentation, because none of those presentations provided any implementation details and because none included the

implementation details required by claim 7.

f. Claims 1 and 7 of the '327 Patent Do Not Cover the JEDEC DDR SDRAM Standard.

354. Devices could be built to the JEDEC DDR SDRAM standard without infringing Claim 1 of the '327 patent. (Fliesler, Tr. 8860-61). Claim 1 calls for the use of a clock signal to write data to the DRAM, while the DDR SDRAM standard uses a different signal, the DQS strobe signal, for that purpose. (CX 1494 at 23; CX 234 at 164; JX 57 at 5; Fliesler, Tr. at 8861; Jacob, Tr. 5641-42). A clock signal and a strobe signal are different: a clock is a "free-running" signal, that is running all the time, while the strobe in DDR SDRAMs is not free-running. (Macri, Tr. 4634).

355. Devices could be built to the JEDEC DDR SDRAM standard without infringing Claim 7 of the '327 patent. (Fliesler, Tr. 8861-2). Claim 7 calls for a multiplexer in the DRAM output path while the DDR SDRAM standard does not require the use of a multiplexer. (CX 1494 at 23; CX 234; Fliesler, Tr. 8863; Jacob, Tr. 5642-43).

356. Rambus has not asserted the '327 patent against any SDRAM or DDR SDRAM devices. (Patent tree attached to the Parties' First Set of Stipulations).

g. Summary of Findings Regarding Undisclosed Patents.

357. Complaint Counsel did not meet their burden of proving that Rambus had any undisclosed patents while it was a JEDEC member that were required to be disclosed under EIA/JEDEC policies.

358. Complaint Counsel did not meet their burden of proving that Rambus's JEDEC representative, Richard Crisp, had actual knowledge of the claims contained in the '327 patent during the time that Rambus was a JEDEC member.

359. Complaint Counsel did not meet their burden of proving that the claims of the '327 patent were "essential" to or "read on" any technology described in any presentation made while Rambus was a JEDEC member.

360. Complaint Counsel did not meet their burden of proving that the claims of the '327 patent were "essential" to or "read on" any technology that was balloted while Rambus was a JEDEC member.

2. Rambus Had No Undisclosed Patent Applications That It Was Required To Disclose To JEDEC.

361. The parties have stipulated that prior to the adoption of the JEDEC SDRAM standard in 1993, Rambus had no undisclosed claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard. (The Parties' First Set of Stipulations, Stipulation 9).

362. Complaint Counsel allege that the following claims of Rambus patent applications should have been disclosed to JEDEC:

(1) Claims 151, 159, 160, 164, 165 and 168 of application serial no. 07/847,961 (the "'961 application"), because they allegedly cover JEDEC-compliant SDRAMs (Nusbaum, Tr. 1544-45; Jacob, Tr. 5507, 5523-28);

(2) Claims 183, 184, and 185 of application serial no. 08/469,490 (the "'490 application"), because they allegedly cover JEDEC-compliant SDRAMs (Nusbaum, Tr. 1572-3; Jacob, Tr. 5528-32);

(3) Claims 151, 152, 166 and 167 of application serial no. 07/847,692 (the "'692 application"), because they allegedly cover a presentation made by NEC that is contained in the September 1994 minutes of the JEDEC 42.3 subcommittee (JX 21 at 91; Nusbaum, Tr. 1584; Jacob, Tr. 5535, 5540); and

(4) Claim 151 of application serial no. 08/222,646 (the "'646 application), because it allegedly covers the Hardell presentation, the Survey Ballot, and the Samsung presentation (Nusbaum, Tr. 1597-98; Jacob, Tr. 5550).

a. <u>The '961 Application Does Not Cover JEDEC-Compliant SDRAMs</u>.

363. The claims of the '961 application that Complaint Counsel allege covered JEDEC-compliant SDRAMs, claims 151, 159, 160, 164, 165 and 168, were added in an amendment filed on January 6, 1995, well after the SDRAM standard was adopted. (CX 1504 at 216-26; Nusbaum, Tr. 1544-45; Fliesler, Tr. 8847). In an office action dated April 16, 1995, the patent examiner rejected all of the claims pending in the '961 application. (CX 1504 at 227-39). Among other grounds, claims 151-165 were rejected as indefinite. (CX 1504 at 229). All of the claims in the '961 application that allegedly

covered JEDEC-compliant SDRAMs were cancelled by Rambus on June 23, 1995. (CX 1504 at 258; Fliesler, Tr. 8847-48).

364. The Federal Circuit has concluded that claims 151, 159, 160, 164, 165 and 168 of the '961 application would not read on a device built to the JEDEC SDRAM standard. (Fliesler, Tr. 8848-51). The Federal Circuit stated:

> "This court has examined the claims of the cited applications [which includes the '961 application] as well as the relevant portions of the SDRAM standard. Based on this review, this court has determined that substantial evidence does not support the finding that these applications had claims that read on the SDRAM standard."

Rambus Inc. v. Infineon Technologies AG, 318 F.3d 1081, 1103 (Fed. Cir. 2003). The Court further held that "claims in the '961 application were limited to the device identifier feature" that is not "present in the SDRAM standard." (*Id.*).

365. Complaint Counsel did not show that Rambus's JEDEC representative had actual knowledge of claims 151, 159, 160, 164, 165 or 168 of the '961 application while Rambus was a JEDEC member.

b. <u>The '490 Application Does Not Cover JEDEC-Compliant SDRAMs</u>.

366. The claims of the '490 application that Complaint Counsel allege covered JEDEC-compliant SDRAMs, claims 183, 184 and 185, were added in a preliminary amendment filed on June 23, 1995, well after the SDRAM standard was adopted in 1993. (CX 1504 at 258, 264-66; Nusbaum, Tr. 1572-73; Fliesler, Tr. 8852). After a restriction

requirement from the patent office, Rambus elected to pursue other claims. Claims 183, 184 and 185 were withdrawn from further consideration as of November 27, 1995. (CX 1504 at 274-75; Fliesler, Tr. 8852-54).

367. Claims 183, 184 and 185 of the '490 application are substantially similar to the claims raised by Complaint Counsel in the '961 application, which the Federal Circuit has held do not read on SDRAMs. (Nusbaum, Tr. 1572, 1629-30).

368. Claims 183 and 184 contain the limitation that the semiconductor device be operative to wait for the access time "in response to a request specifying the semiconductor device." (CX 1504 at 264-65). Claim 185 contains the similar limitation that the semiconductor device wait the access time before responding "to transaction requests specifying the semiconductor device." (CX 1504 at 265-66).

369. Claims 183, 184 and 185 of the '490 application would not cover a device built to the JEDEC SDRAM standard. (Fliesler, Tr. 8855). The limitation that the request "specify[] the semiconductor device" is specific language calling for a device identifier feature that is not a part of the JEDEC SDRAM standard. (Fliesler, Tr. 8943-44). Because this limitation is not found in JEDEC-compliant SDRAMs, the claims do not cover devices built to the JEDEC SDRAM standard

370. Complaint Counsel did not show that Rambus's JEDEC representative had actual knowledge of claims 183, 184 or 185 of the '490 application while Rambus was a JEDEC member.

c. The '692 Application Does Not Cover the September 1994 NEC Presentation.

371. Claims 151 and 152 of the '692 application were filed in a preliminary amendment on June 28, 1993. (CX 1502 at 205, 208; Fliesler, Tr. 8864-65). In an amendment filed on October 23, 1995, claims 151 and 152 were amended and claims 166 and 167 were added. (CX 1502 at 233-35; Fliesler, Tr. 8864-65).

372. The claims raised by Complaint Counsel, namely claims 151 and 152 of the '692 application (whether before or after the October 23, 1995 amendment) and claims 166 and 167, would not cover devices built according to the September 1994 NEC presentation "because the claims contain limitations that would not be found in such devices." (JX 21 at 91; Fliesler, Tr. at 8866-67).

373. All of the claims raised by Complaint Counsel call for the generation of a local clock signal for "performing" or "controlling" memory operations with respect to the memory array. (CX 1502 at 208, 233-35). In the 1994 NEC presentation, however, the internal clock signal (designated as "ICLK") controls the timing of an output buffer but does not perform or control operations with respect to the memory array. (JX 21 at 91; Nusbaum, Tr. 1632-34; Fliesler, Tr. 8870-75). In fact, the ICLK signal generated by the PLL in the NEC presentation cannot affect the timing of *anything* within the memory array. (Fliesler, Tr. 8959).

374. All of the claims raised by Complaint Counsel call for a "phase locked loop" that is coupled to the memory array. (CX 1502 at 208, 233-35). In the 1994 NEC

presentation, however, the box designated as the "PLL" is coupled to the output buffer, not the memory array. (JX 21 at 91; Fliesler, Tr. 8870-75).

375. As the terms are generally understood by persons of ordinary skill in the art, a DLL uses variable delay circuitry and a feedback loop to delay one signal so that it is in sync with another signal, while a PLL uses a voltage-controlled oscillator instead of variable delay circuitry. (Nusbaum, Tr. 1637; Jacob, Tr. 5443, 5617; Soderman, Tr. 9401, 9411).

376. Although the claims of the '692 application refer to a "phase locked loop" or "PLL," the claims describe this circuit as providing "a variable delay to the local signal." As a result, the circuit is actually a delay locked loop or DLL. (Jacob, Tr. 5633-34).

377. There was no evidence at trial that the 1994 NEC presentation was ever balloted at JEDEC.

378. Complaint Counsel did not show that Rambus's JEDEC representative had actual knowledge of claims 151, 152, 166 or 167 of the '692 application while Rambus was a JEDEC member.

d. The '646 Application Does Not Cover the Presentations Raised By Complaint Counsel or the DDR SDRAM Standard.

379. Claim 151 of the '646 application was filed on September 6, 1994. (CX 1493 at 183-85; Fliesler, Tr. 8856). In an office action dated January 24, 1995, the patent examiner rejected claim 151 for, among other reasons, being indefinite. (CX 1493

at 212, 215). Claim 151 was canceled in an amendment filed on September 14, 1995. (CX 1493 at 243; Fliesler, Tr. 8856-57). The '327 patent, which issued from the '646 application, did not contain claim 151. (CX 1494; Nusbaum, Tr. 1617).

380. Claim 151 was filed over two years after the Hardell presentation, and before the Samsung presentation or the issuance of the Survey Ballot. (CX 1493 at 183-85; Fleisler, Tr. 8856; CX 34 at 32; JX 28 at 34-35; JX 31 at 71). Thus, claim 151 was not pending at the time of any of the presentations that allegedly triggered its disclosure.

381. The presentations raised by Complaint Counsel contain no implementation details, thus, they do not contain the implementation details that are *required* by claim 151 of the '646 application. (CX 1493 at 184-85).

382. Claim 151 of the '646 application would not read on a device built to the JEDEC DDR SDRAM standard. (Fliesler, Tr. 8857). Claim 151 calls for writing data to the DRAM in response to the rising edge of a clock signal and the falling edge of a clock signal, while the JEDEC DDR SDRAM standard discusses using a different signal called the DQS or data strobe signal to write the data to the DRAM. (CX 1493 at 184-85; CX 234 at 164; JX 57 at 5; Fliesler, Tr. at 8857-58).

383. Complaint Counsel did not show that Rambus's JEDEC representative had actual knowledge of claim 151 of the '646 application while Rambus was a JEDEC member.

e. Summary of Findings Regarding Undisclosed Patent Applications.

384. Complaint Counsel have not met their burden of proving that Rambus had any undisclosed patent applications while it was a JEDEC member that were required to be disclosed under EIA/JEDEC policies.

385. Complaint Counsel have not met their burden of proving that Rambus's JEDEC representative, Richard Crisp, had actual knowledge of claims 151, 159, 160, 164, 165 and/or 168 of the '961 application during the time that Rambus was a JEDEC member.

386. Complaint Counsel have not met their burden of proving that claims 151, 159, 160, 164, 165 and/or 168 of the '961 application were "essential to" or "read on" any technology described in any presentation made while Rambus was a JEDEC member.

387. Complaint Counsel have not met their burden of proving that claims 151, 159, 160, 164, 165 and/or 168 of the '961 application were "essential to" or "read on" any technology that was balloted while Rambus was a JEDEC member.

388. Complaint Counsel have not met their burden of proving that Rambus's JEDEC representative, Richard Crisp, had actual knowledge of claims 183, 184 and/or 185 of the '490 application during the time that Rambus was a JEDEC member.

389. Complaint Counsel have not met their burden of proving that claims 183, 184 and/or 185 of the '490 application were "essential to" or "read on" any technology described in any presentation made while Rambus was a JEDEC member.

390. Complaint Counsel have not met their burden of proving that claims 183, 184 and/or 185 of the '490 application were "essential to" or "read on" any technology that was balloted while Rambus was a JEDEC member.

391. Complaint Counsel have not met their burden of proving that Rambus's JEDEC representative, Richard Crisp, had actual knowledge of claims 151, 152, 166 and/or 167 of the '692 application during the time that Rambus was a JEDEC member.

392. Complaint Counsel have not met their burden of proving that claims 151, 152, 166 and/or 167 of the '692 application were "essential to" or "read on" any technology described in any presentation made while Rambus was a JEDEC member.

393. Complaint Counsel have not met their burden of proving that claims 151, 152, 166 and/or 167 of the '692 application were "essential to" or "read on" any technology that was balloted while Rambus was a JEDEC member.

394. Complaint Counsel have not met their burden of proving that Rambus's JEDEC representative, Richard Crisp, had actual knowledge of claim 151 of the '646 application during the time that Rambus was a JEDEC member.

395. Complaint Counsel have not met their burden of proving that claim 151 of the '646 application was "essential to" or "read on" any technology described in any presentation made while Rambus was a JEDEC member.

396. Complaint Counsel have not met their burden of proving that claim 151 of the '646 application was "essential to" or "read on" any technology that was balloted while

Rambus was a JEDEC member.

C. Rambus Withdrew From JEDEC Before The Standardization Of The DDR SDRAM Began.

397. An additional reason why Rambus had no disclosure obligation with respect to dual edge clocking and on-chip PLL/DLL is that it withdrew from JEDEC before the standardization process of the DDR SDRAM, which incorporated those features, began.

398. Rambus attended its last JEDEC meetings as of December 1995. In June 1996, Rambus notified the JEDEC office that it would not pay its dues for 1996 and that it would no longer be a JEDEC member. (CX 2104, Crisp 8/10/01 Micron Depo. Tr. 853:18-854:1; CX 887 at 1).

399. The DDR SDRAM standard received JC 42.3 committee approval in March 1998, but was not published until 2000. (CX 375 at 1; JX 57).

400. The DDR SDRAM standard received JEDEC Board of Director approval in 1999. (Rhoden, Tr. 743).

401. The first time that a balloted item was approved as part of the JEDEC DDR SDRAM standard was June 1997. (CX 375 at 2).

402. As described below, an e-mail authored by JEDEC Board Chairman Desi Rhoden in March 1998 shows that the first *presentation* leading to the DDR SDRAM standard occurred in December 1996, after Rambus had left JEDEC. (CX 375 at 1-2).

403. On March 9, 1998, Mr. Rhoden sent an e-mail to Ken McGhee, the JEDEC Secretary, for forwarding to all JC 42 members. (Rhoden, Tr. 1192-93; CX 375). The

e-mail was an effort by Rhoden to recap what had transpired in the DDR SDRAM standardization process. (Rhoden, Tr. 1195).

404. Mr. Rhoden's March 9, 1998 e-mail states in part:

> "[W]e could have finished the DDR standard sooner if only we had started earlier. Let us recap what has transpired with DDR:
>
> 1. A lot of private and independent work *outside of JEDEC* for most of 1996 (here is where we missed a good opportunity to start early).
> 2. December 96 – A single overview presentation of a DDR proposal at a JC 42 meeting.
> 3. March 97 – Many (5 as I remember) presentations of very different proposals at JEDEC (no where near the consensus that was supposedly built outside of the committee). None of these were compatible with each other. At this meeting the decision was made to finally get serious and set up a special meeting for April 97.
> 4. April 97 – Real, focused, dedicated work begins at a special meeting. Many very good ideas and a lot of truly animated discussion.
> 5. June 97 – First ballots on DDR pass committee.
> 6. July 1997 – A second special meeting where the last of the basic concepts were articulated and send out for ballot.
> 7. Sept 97 – The diamond in the rough took its basic shape (there were 2 very similar, but still different forms.)"

(CX 375 at 1-2).

405. Mr. Rhoden's March 1998 e-mail thus dates the first presentation to JEDEC of a DDR SDRAM proposal to December 1996. (CX 375 at 1).

406. Mr. Rhoden's email states that the DDR device was being developed "outside of JEDEC" in 1996. (CX 375 at 1).

407. In an April 1997 presentation, Mr. Rhoden stated: "DDR & SLDRAM were Introduced In JEDEC in Dec 1996." (RX 911 at 3).

408. The initial DDR SDRAM presentation that Mr. Rhoden referred to in his March 1998 e-mail and his April 1997 presentation was made by Fujitsu in December 1996. (Rhoden, Tr. 1198; RX 911 at 3; CX 375 at 1). This presentation, identified in the minutes of the JC 42.3 subcommittee as "Fujitsu Double Data Rate SDRAM," was designated as a "first showing." (JX 35 at 6, 34-42).

409. Mr. Rhoden's March 1998 e-mail also states that the decision to "finally get serious" about DDR SDRAM was not made until March 1997. (Rhoden, Tr. 1201). "Real, focused, dedicated work" on the DDR SDRAM standard did not take place until April 1997. (Rhoden, Tr. 1202). The DDR SDRAM standard did not take "its basic shape" until September 1997. (Rhoden, Tr. 1202).

410. Desi Rhoden was in a position to know about the dates described in his March 1998 e-mail. He has played a leadership role at JEDEC for quite some time. (Rhoden, Tr. 1191). He is currently chairman of the JC 42 committee, which contains the JC 42.3 subcommittee. (Rhoden, Tr. 1191). He has also been chairman of the 42.3 subcommittee and is currently chairman of the JEDEC Board of Directors. (Rhoden, Tr. 1190). In 1998, Mr. Rhoden was very actively involved in the DDR SDRAM standardization process within the JEDEC 42 committee. (Rhoden, Tr. 1191-92).

411. There is other contemporaneous evidence that work on the DDR SDRAM device did not begin, even outside of JEDEC, until the summer of 1996. An IBM presentation on DDR SDRAM dated March 17, 1997 notes that "Industry has been working on DDR definition for 6-9 months," that is, beginning at some point between approximately mid-June and mid-September 1996. (RX 892 at 1). Initially, this work consisted of "small supplier consortiums and individual supplier/user meetings." (*Id*.). Like Mr. Rhoden, the IBM document dates the first "Official DDR presentations" at JEDEC to December 1996, referring (again) to the first showing by Fujitsu. (*Id*.).

412. A March 10, 1997 Mitsubishi memorandum regarding "DDR SDRAM Specification Planning History and Recent Trends" confirms that DDR efforts began outside of JEDEC in the summer of 1996, with "eight companies . . . meeting once every 2 weeks to quickly plan DDR specifications." (RX 885A at 1). The Mitsubishi memorandum's first mention of JEDEC work relating to DDR SDRAM is the first showing by Fujitsu in December 1996. (*Id*.).

413. A July 1997 official JEDEC ballot form regarding a proposed DDR SDRAM pinout states: "DDR SDRAMs has been under discussion within JEDEC since September 1996." (RX 967 at 1).

414. As noted above, Rambus attended its last JC 42.3 meeting in December 1995, and it sent a letter confirming its withdrawal from JEDEC in June 1996. (CX 2104, Crisp 8/10/01 Micron Depo. Tr. 853:18-854:1; CX 887 at 1).

415. As Gordon Kelley, Chairman of the JC 42.3 subcommittee, explained, after a company left JEDEC, it had no duty to disclose anything to JEDEC. (Kelley, Tr. 2700).

416. The district court in the *Infineon* case granted judgment in Rambus's favor on the question of whether it had committed fraud with respect to the DDR SDRAM standard. The district judge held that "substantial evidence did not support the jury's verdict *because Rambus withdrew from JEDEC before formal consideration of the DDR SDRAM standard*." *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1105 (Fed. Cir. 2003) (emphasis added). The Federal Circuit agreed (and the panel was unanimous on this point), finding that:

> "[T]he disclosure duty, as defined by the EIA/JEDEC policy, did not arise before legitimate proposals were directed to and formal consideration began on the DDR-SDRAM standard. None of the evidence relied on by Infineon (e.g., survey ballot, technology proposals on the SDRAM standard) provides substantial evidence for the implicit jury finding that Rambus had patents or applications 'related to' the DDR-SDRAM standard that should have been disclosed before the standard came under formal consideration."

(*Id.*).

D. Rambus Had No Reasoned And Considered Belief Before Late 1998 That It Had Pending Claims That Could Potentially Be Asserted Against JEDEC-Compliant SDRAM Or DDR SDRAM Products.

417. Complaint Counsel have asserted that a JEDEC member was obligated to disclose its *beliefs* that it had sought or could seek intellectual property protection over features or technologies under discussion at JEDEC meetings. (Opening Statement, Tr. 17).

418. There is substantial evidence that it was a JEDEC representative's "actual *knowledge*," not his *beliefs*, that triggered whether disclosure obligations might exist. (Rhoden, Tr. 624; Kelly, Tr. 1970, 2171-2; RX 669 at 3). The Federal Circuit agreed, stating:

> The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard. Otherwise the standard would exempt a member from disclosure, if it truly, but unreasonably, believes its claims do not cover the standard. As discussed above, the JEDEC test in fact depends on whether claims reasonably might read on the standard. A member's subjective beliefs, hopes, and desires are irrelevant.

(*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003).)

419. Assuming, however, that a representative's beliefs did trigger a disclosure obligation, Complaint Counsel nevertheless did not meet their burden of proving that Rambus's JEDEC representative, Richard Crisp, held such a belief at any relevant time.

420. Complaint Counsel rely upon a draft of a Rambus business plan, prepared in June of 1992, that states that "we believe that Sync DRAMs infringe on some claims in our filed patents." (CX 543A at 17).

421. Mr. Crisp is not among the individuals listed as receiving the draft plan. (CX 543A at 1).

422. Complaint Counsel did not show that Mr. Crisp had received a copy of the June 1992 draft business plan.

423. Rambus CEO Geoff Tate testified that the statement in the June 1992 draft plan that "we believe that Sync DRAMs infringe on some claims in our filed patents"was based on a "feeling" that "synchronous DRAMs sure looked like they stem[med] from [our] inventions." (CX 2073, Tate Micron Depo. at 221-22). Mr. Tate had "assumed" that broad patent applications had been filed to protect all of Rambus's inventions. (CX 2073, Tate Micron Depo. at 222; CX 2088, Tate Infineon Trial Testimony at 57). At the time that he wrote the 1992 Business Plan, Mr. Tate did not know of any particular claim that might be infringed by SDRAMs. (*Id*.).

424. After the 1992 Business Plan was prepared, a Rambus employee was assigned the task of determining what filed claims would be infringed by SDRAMs. (CX 2073, Tate Micron Depo. at 222-3). The employee subsequently informed Mr. Tate that the filed claims were not as broad as previously thought and did not cover the full range of what had been invented and disclosed in the '898 application. (CX 2073, Tate Micron Depo. at 222-24; CX 2088, Tate Infineon Trial Testimony at 57-58).

425. Complaint Counsel also point to a June 1993 e-mail by Rambus engineer Fred Ware that states that a claim in a Rambus patent application was "directed against SDRAMs." (CX 1959 at 1). Complaint Counsel did *not* contend at trial, however, that in June 1993 Rambus had *any* claim in a pending application that covered *any* feature of SDRAMs. To the contrary, as noted above, the only Rambus patent claims that are even

alleged by Complaint Counsel to cover SDRAMs are claims in the '961 and '490 applications; these claims were not filed until 1995. *See* Findings ¶ 362.

426. In their opening statement, Complaint Counsel asserted that Mr. Ware's June 1993 e-mail referred to a May 1993 "amendment to Rambus's pending '651 application [application serial no. 07/847,651] related to the concept of programmable CAS latency and that this amendment was intended to cover programmable CAS latency when used in DRAMs generally, including SDRAMs that were the subject of JEDEC work." (Opening Statement, Tr. 84-85). However, all the claims in the May 1993 amendment to the '651 application contained the limitation that data, address, and control information be "in the form of packets," a feature that, according to Complaint Counsel, is not found in SDRAMs. (CX 1458 at 5-8). Complaint Counsel elicited testimony from numerous witnesses that SDRAMs, unlike RDRAMs, do not receive information in the form of packets. (Rhoden, Tr. 402; Sussman, Tr. 1431-32; Kelley, Tr. 2573-74; Kellogg, Tr. 5298; Jacob, Tr. 5466-67). Complaint Counsel did *not* contend at trial that the claims contained in the May 1993 amendment to the '651 application covered programmable latency as used in JEDEC-compliant SDRAMs.

427. Rambus's JEDEC representative, Richard Crisp, testified that during the time that Rambus was a JEDEC member, he: (1) had not seen any Rambus patent application with claims over an SDRAM that used any of the four features at issue here; and (2) did not know one way or the other whether Rambus's pending patent applications

covered JEDEC-compliant SDRAMs using any of those features. (Crisp, Tr. 3540-43; 3461-66).

428. During the time Rambus was attending JEDEC, Dr. Farmwald did not believe that Rambus's patents were infringed by SDRAMs. (CX 2106, Farmwald FTC Depo at 70).

429. In March 1998, Joel Karp informed Rambus's board of directors that Rambus's existing patent claims were narrowly framed. (Farmwald, Tr. 8231-34; CX 615 at 2). Mr. Karp also informed the board that he believed that he could improve the strength of the patent portfolio, but that it would take a year or two to do so. (Farmwald, Tr. 8231-32).

430. By July 1999, Mr. Karp had done a thorough review of Rambus's patent portfolio, observed a number of weaknesses that could be repaired, recognized new patent applications or amendments that could be filed, and was actively working on these projects. (Farmwald, Tr. 8237-38; CX 622 at p.2 (July 14, 1999 board minutes referring to Karp presentation)).

431. It was not until mid-1999 that a Rambus patent issued with claims that were infringed by JEDEC-compliant SDRAMs or DDR SDRAMs. (Farmwald, Tr. 8239-40; CX 623 (October 14, 1999 board minutes referring to strategic IP issues)).

E. Rambus Did Not Violate Any JEDEC Rule Or Policy Simply By Seeking Patent Protection For Inventions That Related To JEDEC Standards, For There Was No Such Rule Or Policy.

432. Complaint Counsel have suggested at times that JEDEC's rules or policies discourage or even preclude members from seeking patent coverage for inventions that relate to JEDEC standards. The evidence does not support such a view.

433. The EIA Legal Guides, which governed JEDEC standardization activities while Rambus was a JEDEC member, state explicitly that "[s]tandards are proposed or adopted by EIA without regard to whether their proposal or adoption may in any way involve patents on articles, materials, or processes." (CX 204 at 4).

434. The EIA's January 22, 1996 comment letter to the FTC states in part that "[a]llowing patented technology in standards is procompetitive." (RX 669 at 2). The letter explains that "[b]y allowing standards based on patents, American consumers are assured of standards that reflect the latest innovation and high technology the great technical minds can deliver." (RX 669 at 2-3).

435. The EIA's January 22, 1996 comment letter to the FTC also states that "[s]tandards in these high-tech industries must be based on the leading edge technologies. Consumers will not buy second-best products that are based only on publicly available information. They demand and deserve the best technology these industries can offer." (RX 669 at 4).

436. The EIA's January 22, 1996 comment letter to the FTC also states that

"[e]ven if knowledge of a patent comes later in time due to the pending status of the patent while the standard was being created, the important issue is the licensing availability to all parties on reasonable, non-discriminatory terms." (RX 669 at 4).

437. EIA General Counsel John Kelly testified that there is no objection to having standards that incorporate patented technologies as long as the patents are available to all potential licensees on reasonable and nondiscriminatory terms. (Kelly, Tr. 2072).

438. It is also clear that throughout the time period that Rambus was a member, JC 42.3 routinely passed ballots to adopt technology as part of its standards despite its awareness of patent-related issues.

439. At the March 1993 JC 42.3 meeting, for example, the committee voted to pass a ballot on Mode Register Timing for the SDRAM draft specification even though Hitachi raised a "patent alert." (JX 15 at 5).

440. At the March 1993 JC 42.3 meeting, the committee also considered ballots for Self-Refresh Entry/Exit, DQM Latency Reads/Writes, and Auto-Refresh for the SDRAM draft specification. (JX 15 at 8). The minutes state that both Hitachi and Mosaid raised a "patent alert" or a "patent concern" with respect to each of these features. (JX 15 at 8, 9). The committee voted unanimously to pass these ballots. (JX 15 at 8, 9).

441. At the March 1993 JC 42.3 meeting, the committee also considered a ballot for a Write Latency = 0 for the SDRAM draft specification. With regard to this ballot, the minutes state that Mosaid raised a patent issue. (JX 15 at 5-6). The minutes also state,

"The Committee is aware of the Hitachi patent. It was noted that Motorola has already noted they have a patent. IBM noted that their view has been to ignore patent disclosure rule because their attorneys have advised them that if they do then a listing maybe construed as complete." (JX 15 at 6). The committee voted unanimously to pass this ballot. (JX 15 at 6). At that meeting, the committee also voted unanimously to send all SDRAM ballots to the JEDEC Council for standardization. (JX 15 at 14).

442. At the very next JC 42.3 meeting, which was held *before* the SDRAM ballots had been voted on by the JEDEC Council, the 42.3 Committee reviewed an analysis of patents relating to SDRAMs. The analysis, which was prepared by Chipworks, included a discussion of several Hitachi patents related to SDRAMs that were described as "powerful" (CX 53A at 13), as well as SDRAM-related patents held by Motorola and other JEDEC members. (CX 53A at 14).

443. No witness who was present at the March and May 1993 JC 42.3 meetings testified that any criticism was leveled against JEDEC members who had obtained patents relating to SDRAMs.

F. Rambus Had No Intent To Violate the Rules Or To Mislead Other JEDEC Members.

444. Complaint Counsel have asserted that Rambus "acted with knowledge that it was violating" JEDEC's rules relating to intellectual property disclosures. (Complaint Counsel's Pre-Trial Brief, p. 196).

445. Complaint Counsel did not meet their burden of showing that Rambus

intended to violate the patent policies that governed JEDEC standardization activities while Rambus was a member.

1. Rambus Sought And Followed Legal Advice Upon Joining JEDEC To Assist It In Understanding And Complying With Its Legal Obligations.

446. Rambus attended its first JEDEC meeting, in December 1991, at Toshiba's recommendation and as Toshiba's guest. (CX 2054, Mooring 11/15/00 Depo. Tr., 43-44).

447. Rambus decided to join JEDEC because of the prospect of standardizing the RDRAM device, because it seemed to be a useful place to learn marketplace and competitive information, and because it was a good place for "meeting and greeting" potential customers. (CX 2101, Horowitz Depo. Tr., 279; CX 2099, Tate Depo. Tr., 739; CX 2054, Mooring 11/15/00 Depo. Tr., 44).

448. Shortly after it joined JEDEC, Rambus sought the legal advice of its outside patent counsel, Mr. Lester Vincent, in connection with its participation in JEDEC.

449. In March 1992, Richard Crisp and his supervisor, Allen Roberts, talked to Mr. Vincent about JEDEC-related issues. (CX 3125, Vincent 4/11/01 Depo. Tr., 310-315). After discussing JEDEC with Mr. Vincent, "the two key things that [Mr. Crisp] walked away from the meeting understanding was that Rambus should not go and promote a standard, and we should not mislead JEDEC into thinking that we wouldn't enforce our property rights." (Crisp, Tr. 3470-71).

450. Mr. Vincent's time sheets show that at around the time he gave Mr. Crisp

this advice, he reviewed one or more "JEDEC publications." (CX 1937 at 12). At that time, JEDEC manual 21-H was in effect, and the only language in it relating to intellectual property was the following:

> "JEDEC standards are adopted without regard to whether or not their adoption may involve patents or articles, materials or processes."

(CX 205A at 11).

451. Mr. Crisp testified that he followed Mr. Vincent's advice and did not promote a technology for standardization. (Crisp, Tr. 3470).

452. An e-mail that Mr. Crisp wrote in December 1995, almost four years later, shows that he was still mindful of Mr. Vincent's advice at that time. He wrote that he understood that Rambus should not "intentionally propose something as a standard and quietly have a patent in our back pocket. . . ." (CX 711 at 188). As he also stated at the time, he was "unaware of us doing any of this or of any plans to do this." (*Id.*). Mr. Crisp testified that this December 1995 passage referred to "what we would have to do and what we should not do in the event that we were to propose the R-module as a standard." (Crisp, Tr. 3485).

453. Rambus did not propose the Rambus module, or "R-module," for JEDEC standardization after Mr. Crisp wrote his December 1995 e-mail. In fact, *no* witness testified that Mr. Crisp promoted *any* technology for standardization at JEDEC at any time during Rambus's membership.

454. Mr. Crisp also followed Mr. Vincent's 1992 advice not to mislead JEDEC members into thinking that Rambus would not enforce its intellectual property. When Mr. Crisp was asked at JEDEC meetings on two occasions to comment about Rambus's intellectual property, he *declined* to comment each time, and the JEDEC members who testified at trial uniformly understood that he had declined to comment. *See* Findings of Fact 492-514, *infra*, and citations contained therein. Mr. Crisp also testified that no one had informed him that his refusal to comment violated any JEDEC rule or policy. (Crisp, Tr. 3490-91).

455. Mr. Crisp's refusal to comment at the September 1995 JEDEC meeting could not have been clearer:

> "At this time, Rambus elects to not make a specific comment on our intellectual property position relative to the Synclink proposal. Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property."

(RX 602 at 1; JX 27 at 4, 26).

456. Mr. Crisp was also advised by Mr. Vincent, in the 1992 time frame, about the importance of keeping patent applications confidential. Mr. Crisp testified as follows:

> "Q: Did [Vincent] at any time give you any legal advice with respect to the disclosure of patent applications?
> A: Yes, he did.
>
> Q: What was that advice?

A: He told us to not disclose our patent applications. They were confidential.

Q: Did you have an understanding in that time period of any consequences that might result from disclosure of applications?
A: Yes, I did.

Q: What was your understanding at the time?
A: I understood that companies could potentially file interference actions on our patent applications in the patent office; that in certain countries where the rules are first to file, somebody could potentially file a claim before we actually did; and that we basically would be disclosing trade secrets that could work against us in terms of our competitive position in the marketplace.

Q: Did you do anything with this advice from Mr. Vincent?
A: Yes, I did.

Q: What did you do?
A: I followed it."

(Crisp, Tr. 3496).

457. In addition, in his letters transmitting copies of Rambus's patent applications, Mr. Vincent reminded Rambus employees to "keep in mind that this information is confidential." (CX 1951 at 2; CX 1945 at 2).

458. Mr. Crisp described his thinking about Rambus's reasons not to disclose patent applications in a September 23, 1995 e-mail:

"[w]e decided that we really could not be expected to talk about potential infringement for patents that had not issued both from the perspective of not knowing what would wind up being acceptable to the examiner, and from the perspective of

> not disclosing our trade secrets any earlier than we are forced to."

(CX 387 at 2).

459. Mr. Crisp testified that this e-mail passage reflects the advice he had received from Mr. Vincent. (Crisp, Tr. 3473).

460. Mr. Crisp was present at a JEDEC meeting when an IBM representative stated that he would not disclose intellectual property at JEDEC meetings. Mr. Crisp understood from that statement that such disclosures were not required. (Crisp, Tr. 3505-07).

461. In sum, Complaint Counsel failed to meet their burden of proving that Rambus knew of and intentionally violated a JEDEC disclosure requirement.

462. Complaint Counsel also failed to meet their burden of showing that any JEDEC disclosure obligation that is based on the "actual knowledge" of a JEDEC representative was ever triggered with respect to Mr. Crisp. (Crisp, Tr. 3540-43; 3461-66). *See also* Findings ¶¶ 342, 348, 351, 358, 365, 370, 378, 383. Instead, the unrebutted evidence is that while Mr. Crisp may have *hoped* that Rambus might have rights to certain technologies, he did not, while attending JEDEC meetings, know "one way or the other" whether Rambus had pending patent applications that would cover SDRAMs that incorporated or made use of those technologies. (*Id.*). Indeed, after a review in June or July 1995 of Rambus patents and patent applications, he "didn't see that we had anything that applied to SDRAM" or to the SyncLink device. (Crisp, Tr. 3540-43).

463. It is thus apparent that even if a mandatory disclosure obligation applied to JEDEC members when they had "actual knowledge" of patents (or applications) that covered a proposed standard, those disclosure obligations were not triggered as to Mr. Crisp or Rambus.

VI. RAMBUS DID NOT LULL ANY JEDEC MEMBER INTO BELIEVING THAT RAMBUS WOULD NOT HAVE OR WOULD NOT ENFORCE INTELLECTUAL PROPERTY WITH RESPECT TO FEATURES INCORPORATED WITHIN THE SDRAM OR DDR SDRAM STANDARDS.

464. The Complaint alleges that Rambus intentionally gave the members of JEDEC 42.3 the "materially false and misleading impression . . . that JEDEC, by incorporating into its SDRAM standards technologies openly discussed and considered during Rambus's tenure in the organization, was not at risk of adopting standards that Rambus could later claim to infringe upon its patents." (Complaint, ¶ 71).

465. The evidence demonstrates, however, that Rambus said nothing and did nothing to mislead JEDEC 42.3 members into believing that Rambus would not seek or enforce intellectual property rights over features incorporated in JEDEC standards.

A. JEDEC Members And JEDEC Committee Leaders Were Aware As Early As 1992 That Rambus Might Obtain Patent Rights With Respect To Features Being Considered For Incorporation Into JEDEC Standards, And Rambus Did Nothing To Dispel Or Alleviate Those Concerns.

1. Rambus's Conduct At The May 1992 JEDEC Meeting Did Not Mislead JEDEC Members Or Leaders On Issues Relating To Rambus's Intellectual Property.

466. Several witnesses testified at trial about an exchange at the May 1992 JEDEC meeting that involved the JEDEC representatives from IBM, Siemens and Rambus, respectively, during which issues relating to Rambus's intellectual property were raised.

467. In order to understand fully the significance of this May 1992 exchange involving Siemens, IBM and Rambus representatives, it is useful to examine Siemens' and IBM's DRAM development efforts in the spring of 1992.

468. In the spring of 1992, IBM and Siemens (whose former semiconductor division is now called Infineon Technologies) were cooperating on a joint venture to develop and produce a new DRAM design. (Kelley, Tr. 2532; Meyer, Infineon Trial Tr. 4/25/01, 277:18-23, 310:6-11).

469. Both the Siemens JEDEC representative, Willi Meyer, and the IBM JEDEC representative, Gordon Kelley, were involved in the Siemens/IBM DRAM development efforts in the spring of 1992. (Kelley, Tr. 2620-21). The efforts included a consideration of the Rambus technology. (Kelley, Tr. 2627).

470. In March 1992, Mr. Kelley prepared a memorandum regarding Rambus. (RX 240 at 1). Mr. Kelley's March 19, 1992 memorandum refers to "a unique (and probably patented) Rambus protocol" and "a special Microprocessor and DRAM interface (other than industry standard)." (RX 240 at 1). Mr. Kelley's memorandum also states that he had asked an IBM in-house lawyer "to get me a copy of Rambus patents." (*Id.*).

471. On April 23, 1992, Mr. Kelley attended a presentation at IBM by Rambus founder Mike Farmwald and Rambus executive David Mooring. (Kelley, Tr. 2631; RX 273 at 1).

472. According to handwritten notes of the April 23, 1992 Rambus/IBM meeting that were produced in discovery by IBM, a Rambus representative stated at the meeting that Rambus intended to obtain "license fees + royalties from IC company." (CX 2355 at 1). The notes also state that Rambus "want to set industry std." (CX 2355 at 1).

473. In April 1992, Gordon Kelley prepared a "Rambus Assessment" along with two other IBM employees, Dr. Beilstein and Michael Clinton. (RX 279 at 1). The "Rambus Assessment" is dated April 24, 1992, the day after Mr. Kelley had attended the presentation by Rambus. (RX 279 at 1; Kelley, Tr. at 2635).

474. The April 1992 "Rambus Assessment" that Mr. Kelley co-authored refers to "Unique Rambus Features/Attributes." (RX 279 at 1). The "Rambus Assessment" also states that "Intel is Rambus licensee" and notes a "potential future Intel memory strategy

to marry . . . 586/686 processor with Rambus protocol to corner PC/notebook market with state of the art performance." (RX 279 at 4).

475. The "Rambus Assessment" co-authored by Gordon Kelley states that "Rambus can work technically" and notes "the risk is whether it becomes a standard for the low end-bulk of DRAM bit volume – and that it provides a simple low end solution for anyone to get into the PC business." (RX 279 at 8).

476. The "Rambus Assessment" co-authored by Gordon Kelley states that "[i]f Rambus fails to become standard, then it is business as usual for BTV [the acronym for IBM's Burlington, Vermont operations] and the SDRAM has a significant chance of being standard." (RX 279 at 7).

477. It is apparent from Mr. Kelley's March and April 1992 analyses of Rambus that he was aware of and focused on Rambus, its technology, and its prospects for success in the spring of 1992. (RX 279; RX 273; RX 240; CX 2355).

478. One week after Mr. Kelley finalized the April 24, 1992 "Rambus Assessment," he participated in a conference call with Siemens JEDEC representative Willi Meyer. The call included a discussion of Rambus. (RX 286A at 1).

479. Trial exhibit RX 286A is a memorandum dated April 30, 1992 prepared by Mr. Meyer about a telephone conference involving Meyer, Siemens executive Dr. Martin Peisl, and IBM's Gordon Kelley. (RX 286A; Meyer, Infineon Trial Tr. 4/25/01, 317-319).

480. Meyer's April 30, 1992 memorandum states in part: "Rambus: Visited key in-house IBM users. IBM is still keeping its eye on Rambus. Rambus has announced a claim against Samsung for USD 10 million due to the similarity of the SDRAM with the Rambus storage device architecture. For that reason, IBM is seriously considering to preemptively obtain a license as soon as possible (at an introductory price)." (RX 286A at 2).

481. Mr. Meyer testified that during the conference call, Gordon Kelley had provided the Rambus-related information contained in Meyer's April 30, 1992 memorandum. (RX 286A; Meyer, Infineon Trial Tr. 4/25/01, 317:5-319:9).

482. Siemens executive Martin Peisl similarly testified that the information regarding Rambus that is contained in Meyer's April 30, 1992 memorandum "seems to be information coming from IBM or Gordon Kelley." (Peisl, Tr. 4517).

483. Gordon Kelley testified at trial, however, that he did *not* provide the information regarding Rambus that is contained in Meyer's April 30, 1992 memorandum. (RX 286A; Kelley, Tr. 2643). Kelley testified that *Meyer* had provided the information. (Kelley, Tr. 2643).

484. Regardless of whether it was Mr. Kelley or Mr. Meyer who provided the Rambus-related information contained in Mr. Meyer's April 30, 1992 memorandum, it is clear that the IBM JEDEC representative (who was also the JC 42.3 chair) and the Siemens JEDEC representative were aware as of April 30, 1992 of a possibility that

Rambus might assert intellectual property claims "due to the similarity of the SDRAM with the Rambus storage device architecture." (RX 286A at 2).

485. The privilege log provided by IBM in this matter reflects that on May 1, 1992, there was a presentation about Rambus patents by an in-house lawyer named J. Walter, although Mr. Kelley does not recall whether he attended. (Kelley, Tr. 2647-8). An April 16, 1992 IBM memorandum referenced the fact that Mr. Walter had been asked to review and comment upon Rambus-related intellectual property issues. (RX 272 at 2).

486. Mr. Meyer also wrote a separate memorandum dated April 30, 1992 that stated in part that "[t]he original idea behind the SDRAM is based on the basic principle of a simple pulse input (IBM toggle pin) and the complex RAMBUS structure." (RX 285A at 5). This memorandum also demonstrates Mr. Meyer's awareness of similarities between the SDRAM device and the "Rambus structure." (RX 285A at 5).

487. On May 6, 1992, Mr. Meyer prepared a chart showing the "Pros" and "Cons" of "Sync DRAM," "Rambus DRAM," and "Cached DRAM." (RX 289 at 1).

488. In his May 6, 1992 "Pros" and "Cons" chart, Mr. Meyer states that the "2-bank" synchronous DRAM "may fall under Rambus patents." (RX 289 at 1).

489. Mr. Meyer testified that at the time, he thought there was a potential that Rambus would obtain patents that would cover synchronous DRAMs. (CX 2088, Meyer, Infineon Trial Tr. 4/26/01, 44:3-23).

490. Mr. Meyer also testified that in 1992, "we were absolutely sure that Rambus was trying to get patents." (CX 2088, Meyer, Infineon Trial Tr. 4/26/01, 75:4-14).

491. On May 6, 1992, the same date as on Mr. Meyer's "Pros" and "Cons" chart, Mr. Meyer and Mr. Kelley attended a JC 42.3 subcommittee meeting in New Orleans, Louisiana. (CX 34).

492. The May 1992 meeting was Richard Crisp's first JC 42.3 subcommittee meeting as Rambus's JEDEC representative. (CX 34 at 1; Crisp, Tr. 2929).

493. Complaint Counsel predicted in his opening statement that the evidence would show that at the May 1992 JEDEC meeting, JEDEC 42.3 subcommittee chairman Gordon Kelley had asked Rambus representative Richard Crisp "point blank": "Do you have anything to disclose relating to two-bank design" of an SDRAM? (Opening Statement, Tr. 66). Complaint Counsel also predicted that "some" witnesses would testify "that Mr. Crisp shook his head no" in response to this question, suggesting that Rambus had no intellectual property claims in the area. (Opening Statement, Tr. 66).

494. The evidence at trial did not show that Mr. Crisp had stated or suggested at the May 1992 JC 42.3 meeting, by word or by movement, that Rambus did not have or would not seek intellectual property rights relating to a two-bank design or any other feature of an SDRAM.

495. No witness who testified at trial about the May 1992 exchange between Mr. Kelley and Mr. Crisp testified that he or she had understood Mr. Crisp to be stating or

suggesting that Rambus did not have or would not seek intellectual property rights with respect to a two-bank design or any other feature of an SDRAM.

496. Instead, every witness who testified at trial about the May 1992 exchange between Mr. Kelley and Mr. Crisp testified that Mr. Crisp had *declined to comment* in response to the question asked of him.

497. The witnesses who testified about the May 1992 exchange between Mr. Kelley and Mr. Crisp were Mr. Kelley, Mr. Crisp, Siemens representative Willi Meyer, IBM representative Mark Kellogg and Intel representative Samuel Calvin. (Kelley, Tr. 2662; Crisp, Tr. 3066; Kellogg, Tr. 5055-6; Calvin, Tr. 1066-9; CX 2088, Meyer, Infineon Trial Tr. 4/26/01, 164:6-23, 136:3-5).

498. Mr. Calvin, the Intel representative, testified that he recalls that at a JEDEC meeting (whose date he could not remember), Mr. Crisp was asked if he cared to comment about whether Rambus had patents or intellectual property that covered a particular subject. (Calvin, Tr. 1068-9). Mr. Calvin recalls that Mr. Crisp declined to comment. (Calvin, Tr. 1068-70).

499. Mr. Meyer, who was Siemens' primary JEDEC representative between 1992 and 1996, testified that at the May 1992 meeting, he asked Mr. Kelley to ask Mr. Crisp "whether [he] would like to comment" about whether Rambus had patents relating to the use of two banks in a DRAM. (CX 2088, Meyer, Infineon Trial Tr. 4/26/01, 133:1-

134:13; Meyer, Infineon Trial Tr. 5/7/01 87:12-19); CX 2057, 12/13/00 Infineon Meyer Depo. Tr., 66:7-11).

500. Mr. Meyer testified that "[t]he way how Mr. Kelley formulated the question was: Do you want to give a comment on this?" (CX 2088, Meyer, Infineon Trial Tr.4/26/01, 136:3-5, 164:21-23 ("Q. The question Mr. Kelley asked was did Rambus care to comment, right? A. Right.")). Mr. Meyer testified that Mr. Crisp "just shook his head." (*Id*.).

501. Mr. Meyer's trip report of the May 1992 meeting states in part that:

> "Siemens and Philips concerned about patent situation with regard to Rambus and Motorola. No comments given."

(RX 297 at 5).

502. Mr. Crisp testified that Mr. Meyer had raised a concern during the May 1992 meeting about potential Rambus patents relating to the two bank design of the SDRAM. (Crisp, Tr. 2993-4; 3490-1). Mr. Crisp testified that Mr. Kelley then asked Mr. Crisp if he would comment, and that he declined to do so. (Crisp, Tr. 2994; 3490).

503. Mr. Crisp sent an e-mail on May 6, 1992 that described his exchange with Mr. Kelley in this manner:

> "Siemens expressed concern over potential Rambus Patents covering designs. Gordon Kelley of IBM asked me if we would comment which I declined."

(CX 673 at 1).

504. Gordon Kelley testified that Siemens representative Willi Meyer had raised an "issue of concern with Rambus and Rambus patents" at the May 1992 meeting. (Kelley, Tr. 2662). Mr. Kelley recalls that Mr. Meyer had asked Mr. Crisp if he knew whether Rambus "had patentable material on the concept of the synchronous DRAM." (Kelley, Tr. 2543). Mr. Kelley recalls that Mr. Crisp declined to comment in response to that question. (Kelley, Tr. 2662).

505. Mr. Kelley testified that he could not recall whether he had said anything at the May 1992 JEDEC meeting about possible Rambus patent claims. (Kelley, Tr. 2544).

506. Mr. Kelley also testified that a "no comment" from a JEDEC member in response to a question about intellectual property is "unusual" and "surprising" and "is notification to the committee that there should be a concern. . . ." (Kelley, Tr. 2579).

507. IBM representative Mark Kellogg prepared contemporaneous handwritten notes at the May 1992 JEDEC meeting that refer to the concerns Mr. Meyer had raised. (RX 290 at 3). Mr. Kellogg's notes state:

> "Siemens: Kernel of chip similar to Rambus. Patent concerns?
> (No Rambus comments)."

(RX 290 at 3).

508. Mr. Kellogg testified that when he used the phrase "kernel of the chip" in his notes, he was referring to Mr. Meyer's concern that "the fundamental architecture of the SDRAM device" was "similar to Rambus." (Kellogg, Tr. 5324).

509. Mr. Kellogg testified that he took his notes at the May 1992 meeting in part to act as "a log of events" and "also to initiate action on my part or the part of others." He said that this discussion "would have been a flag, which is why I wrote it down." (Kellogg, Tr. 5322 (quoting deposition testimony, which Mr. Kellogg agreed was truthful)).

510. Mr. Kellogg testified that he considered the discussion a "flag" because JEDEC members were "describing possible intellectual property concerns which may affect our decision process for synchronous DRAM." He testified that "[t]hat is a concern" and that "[t]he lack of response by Rambus is also a concern." (Kellogg, Tr. 5323 (quoting deposition testimony, which Mr. Kellogg agreed was truthful)).

511. In sum, the evidence shows that: (1) Mr. Crisp was asked at the May 1992 JC 42.3 meeting if he would care to comment about whether Rambus had intellectual property with respect to the SDRAM device; (2) Mr. Crisp declined to comment; and (3) JEDEC leaders and members were aware that Mr. Crisp had declined to comment.

512. Three conclusions are evident from the May 1992 JEDEC meeting and the events leading up to it.

513. First, it is clear that the chairman of the JC 42.3 committee was aware in April and May 1992 that Rambus might have intellectual property claims relating to one or more technologies being considered for JEDEC standardization.

514. Second, it is clear that Rambus did nothing and said nothing at the May 1992 JEDEC meeting to suggest that Rambus did not have or would not obtain intellectual property claims relating to the SDRAM device.

515. Third, it is apparent that Rambus's refusal to comment about its intellectual property at the May 1992 meeting occurred in the presence of, and was a concern to, JEDEC leaders and members.

516. There was an additional discussion of Rambus's potential intellectual property claims at the May 1992 JEDEC meeting. After the exchange between Mr. Kelley and Mr. Crisp, NEC representative Howard Sussman stated that he had reviewed Rambus's "PCT" patent application. (RX 290 at 3; CX 673 at 1).

517. A "PCT" application is an international patent application filed pursuant to the Patent Cooperation Treaty. (CX 1454 at 1). Rambus had filed a PCT application on April 16, 1991 that was identical in all material respects to the '898 application it had filed at the same time in the U.S. (CX 1451; CX 1454; Fliesler, Tr. 8811).

518. Pursuant to the procedures governing applications filed under the Patent Cooperation Treaty, Rambus's PCT application became publicly available as of October 31, 1991. (CX 1454 at 1; First Set of Stipulations, April 24, 2003, p. 2, item 8).

519. At the May 1992 JEDEC meeting, NEC representative Howard Sussman stated that he had reviewed Rambus's PCT application, that it contained 150 claims, and

that many of the claims were, in Mr. Sussman's opinion, barred by prior art. (RX 290 at 3; CX 673 at 1).

520. Mr. Crisp's May 6, 1992 e-mail states that:

> In response to the patent issue, Sussman stated that our patent application is available from foreign patent offices, that he has a copy, and noted many, many claims that we make that are anticipated by prior art. He also stated the Motorola patent predated ours (not the filing date!) and it too was anticipated by prior art."

(CX 673 at 1).

521. The handwritten notes taken contemporaneously at the May 1992 meeting by IBM representative Mark Kellogg similarly state that:

> "NEC: Rambus International Patent 150 pages, Motorola patents/Rambus patents – suspect claims won't hold."

(RX 290 at 3).

522. Roughly one week after the May 1992 meeting, Siemens' JEDEC representative Willi Meyer also reported that: "Siemens and Philips concerned about patent situation with regard to Rambus and Motorola. No comments given. Motorola patents have priority over Rambus'. Rambus patents filed but pending." (RX 297 at 5).

523. In June 1992, Gordon Kelley gave a presentation about Rambus to a group of about 30 engineers. Half of the engineers were from IBM; half were from Siemens. (Kelley, Tr. 2658-9).

524. Any question about whether JC 42.3 Chairman Kelley had been misled or "lulled" by Mr. Crisp's refusal to comment at the May 1992 meeting is resolved by Mr. Kelley's testimony about his June 1992 presentation. (Kelley, Tr. 2545; 2658-9).

525. In connection with his June 1992 presentation, Mr. Kelley prepared a chart entitled "COMPARE ALTERNATIVES for Future High Performance, High Volume DRAM Designs." The chart listed "Pros" and "Cons" of Sync DRAMs and Rambus DRAMs. One of the two "cons" listed for Sync DRAMs was "Patent Problems? (Motorola/Rambus)." (RX 303 at 1; Kelley, Tr. 2544).

526. Mr. Kelley testified that he included the reference to possible "patent problems" involving Motorola and Rambus in his June 1992 "Pros" and "Cons" chart because he "was notifying the people involved in the design of the joint work that was going on between IBM and Siemens that there was concern about potential patent problems as I had heard at the JEDEC meeting about Motorola and Rambus intellectual property, and I wanted the group to recognize that there was this concern." (Kelley, Tr. 2545).

527. Mr. Meyer testified that in September 1992, he had prepared a presentation entitled "What Is Rambus?" (RX 321 at 1; CX 2088, Meyer Infineon Trial Tr. 4/26/01, 66-67). Meyer delivered this presentation to, among others, Dr. Schumacher, the current CEO of Infineon. (*Id.*).

528. In his September 1992 presentation, Mr. Meyer referred to Rambus as a "deadly menace to the established computer industry." (RX 321 at 2). He also suggested that to "protect" the computer industry, someone could "buy Rambus and dump it." (RX 321 at 3). Mr. Meyer testified that he thought that some of his competitors were so worried about Rambus that they might purchase the entire company and "bury the technology." (CX 2088, Meyer Infineon Trial Tr. 4/26/01, 89-90).

529. Mr. Kelley testified, in a 2001 deposition, that he had had conversations with Mr. Meyer *after* 1992 that related to the potential applicability of Rambus patents to SDRAM devices. He could not recall the substance of these conversations. (Kelley, Tr. 2664-5).

2. Rambus Did Not Mislead JEDEC Members Or Leaders After The May 1992 Meeting With Respect To Its Intellectual Property. The Evidence Shows Instead That JEDEC Members Believed That If Rambus Did Obtain Patents Relating To SDRAMs, The Patents Would Be Invalid Because Of Prior Art.

530. There was an additional discussion of Rambus's PCT application at a JEDEC meeting in September 1993, after Rambus representative Richard Crisp disclosed that Rambus had obtained its first U.S. patent (the '703 patent). According to Siemens' JEDEC representative Willi Meyer:

> "During the meeting, which was the same meeting in which the Rambus '703 patent was disclosed with its full patent number, and a participant, I'm not quite sure, either the participant or the chairman or the JEDEC official, somebody at the meeting said by the way, there is also something called like

> a WIPO, World Intellectual Property, and he offered to anybody who was interested in it to get the number from him, the reference number, and to step up to him after the meeting to do so."

(CX 2057, Meyer, 12/13/00 Infineon Depo. Tr., 298:10-20).

531. A PCT application is sometimes referred to as a "WIPO" application because it is filed with the World Intellectual Property Organization. (CX 1454 at 1; Vincent, Tr. 7883).

532. Mr. Meyer testified that this statement about the "WIPO" application was made "during the official meeting session," and he testified that whoever had brought up the application described it as "a collection of prior art:"

> "He said everything else regarding the Rambus intellectual property is stuck in the patent office and is not proceeding right now. Other comments from this person were it's basically because they are checking for prior art and that it seems to be that what Rambus has submitted is mainly a collection of prior art, this is what I recall very specifically, and then he brought up this WIPO, saying maybe this is because everything else is stuck, this is a way around that, and Rambus has chosen to document all that which they could not get through the U.S. Patent Office through this World Intellectual Property Organization, whatever it is. And then came the mentioning, I have the number and reference number of that WIPO and if you want to step up after the meeting, you can get it from me, the number."

(CX 2057, Meyer 12/13/00 Infineon Depo. Tr., 300:7-23).

533. Mr. Meyer also testified that he obtained the serial number for Rambus's "WIPO" application at the JEDEC meeting and "sent it back to the [Siemens] patent department." (CX 2088, Meyer Infineon Trial Tr., 4/26/01, 112:13-24).

534. A few months later, in March 1994, Mr. Meyer prepared a memorandum about Rambus to a Siemens engineering manager named Penzel. The memorandum stated in part that "[a]ll computers will (have to be) built like this some day, but hopefully without royalties to Rambus." (RX 488A at 1; CX 2088, Meyer Infineon Trial Tr., 4/26/01, 124).

535. As noted in findings 659-706, below, and as demonstrated by the Mitsubishi documents and other evidence cited in support of those findings, a patent lawyer or person of ordinary engineering skill would understand from reviewing the PCT application that Rambus might seek broad patent claims covering the use in memory devices of programmable CAS latency, programmable burst length, dual-edge clocking and on-chip DLL.

536. Rambus was also asked at a May 1995 JEDEC meeting to respond to questions about its intellectual property. At the May 24, 1995 JEDEC meeting, presentations were made by several JEDEC members regarding a "next generation" memory technology called "SyncLink." (JX 26 at 10-11). Rambus representative Richard Crisp was asked at the meeting to "get a statement from his company on the issue of whether they held patents on the concepts of the SyncLink DRAM. . . ." (Kelley,

Tr. 2578). Mr. Crisp provided a statement at the next JEDEC meeting. *See* Findings ¶¶ 544-548.

537. A few days after the May 1995 meeting, Mr. Crisp sent an e-mail to Reese Brown, a JEDEC consultant, that included a reference to "Ramlink," the foundation for the proposed SyncLink device. (CX 711 at 80-81; Gustavson, Tr. 9281-3). Mr. Crisp's e-mail stated in part that Ramlink "has numerous patent issues associated with it." (CX 711 at 80-81).

538. Mr. Brown forwarded Mr. Crisp's e-mail to Hans Wiggers, the JEDEC representative for Hewlett-Packard, who was chairing the Ramlink/SyncLink working group. (CX 711 at 88-91; Gustavson, Tr. 9282-3).

539. On June 10, 1995, Mr. Wiggers forwarded Mr. Crisp's comments to, among others, Gordon Kelley, the Chairman of the JC 42.3 subcommittee, along with a request that Mr. Crisp clarify his comments about patents relating to Ramlink. (CX 711 at 90-1). On June 12, 1995, Mr. Kelley prepared an internal IBM memorandum that stated with respect to the SyncLink device that "the Rambus patents should be closely reviewed." (RX 575 at 7).

540. On June 13, 1995, Mr. Crisp sent an e-mail to Mr. Wiggers that stated:

> "[R]egarding patents, I have stated to several persons that my personal opinion is that the Ramlink/SyncLink proposals will have a number of problems with Rambus intellectual property. We were the first out there with high bandwidth, low pincount, DRAMs, our founders were busily at work on their original concept before the first Ramlink meeting was held, and their

> work was documented, dated and filed properly with the US patent office. *Much of what was filed has not yet issued, and I cannot comment on specifics as these filings are confidential.*"

(RX 576 at 2) (emphasis added).

541. Mr. Crisp's e-mail to Mr. Wiggers also stated that:

> "I was asked at the last JEDEC 42.3 meeting to report on our patent coverage relative to SyncLink as proposed at JEDEC 42.3 at the next meeting in Crystal City in September. Our attorneys are currently working on this, so I think I will be in a position to make some sort of official statement at that time and plan to do so. In the meantime, I have nothing else to say to you or the rest of the committee about our patent position. If you want to search for issued patents held by Rambus, then you may learn something about what we clearly have covered and what we do not. *But I must caution you that there is a lot of material that is currently pending and we will not make any comment at all about it until it issues*."

(RX 576 at 2) (emphasis added).

542. In August 1995, Rambus warned the SyncLink working group that its work might infringe Rambus's intellectual property. The minutes of the August 21, 1995, meeting of the SyncLink working group state in part as follows:

> "Richard Crisp, of RamBus, informed us that in their opinion both RamLink and SyncLink may violate RamBus patents that date back as far as 1989. Others commented that the RamLink work was public early enough to avoid problems, and thus might invalidate such patents to the same extent that they appear to be violated. However, the resolution of these questions is not a feasible task for this committee, so it must continue with the technical work at hand."

(RX 592 at 2).

543. Although the August 22, 1995 SyncLink meeting was held under the auspices of a standards-setting body called the IEEE, not JEDEC, each of the seven companies represented at the SyncLink meeting was also a JEDEC member company, and at least five of the engineers present at the SyncLink meeting were JEDEC representatives who attended the next JEDEC 42.3 meeting on September 11, 1995. (First Set of Stipulations, April 24, 2003, p. 3, item 21).

544. At the September 1995 JEDEC meeting, Mr. Crisp presented a written response to the questions about intellectual property that had been raised at the May 1995 meeting. The statement included this passage:

> "At this time, Rambus elects to not make a specific comment on our intellectual property position relative to the Synclink proposal. *Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property*."

(JX 27 at 26) (emphasis added). Rambus's statement was published in full in the official JEDEC minutes of the September 1995 meeting. (JX 27 at 26).

545. JC 42.3 chair Gordon Kelley testified that Rambus's "comment of no comment" was "unusual on the committee and is surprising. . . ." Kelley, Tr. 2579.

546. Kelley explained that "[a] comment of no comment is notification to the committee that there should be a concern" about intellectual property issues. Kelley, Tr. 2579.

547. A September 1995 meeting report prepared by Motorola JEDEC representative Mark Farley noted that Mr. Crisp had:

> "[m]ade a non-statement statement to the committee saying that Rambus has been developing this technology for five+ years and has a substantial number of patents relating to high bandwidth DRAMs." (RX 615 at 1).

Mr. Farley also reported that "SyncLink told Motorola confidentially that there were very likely patents violated by their proposal." (RX 615 at 1).

548. Intel representative Samuel Calvin testified that he understood from Rambus's September 11, 1995 statement that any silence by Rambus at JEDEC meetings should not be taken as an indication that it did not have intellectual property relating to JEDEC's work. (Calvin, Tr. 1070).

549. In this same time period – the fall of 1995 – Rambus CEO Geoff Tate and Rambus Vice President Allen Roberts held a series of meetings with DRAM manufacturers in Asia in an effort to convince the manufacturers to become Rambus licensees. As set out below, Mr. Tate's notes of those meetings reflect that he told DRAM manufacturers LG Semicon, Samsung, NEC, and Oki that Rambus expected to have intellectual property that would read on the SyncLink architecture and on devices manufactured in compliance with the SDRAM standard.

550. During a meeting in Korea in October 1995, Rambus informed LG Semiconductor that Rambus had or might obtain intellectual property rights that might apply to SDRAMs. (CX 2111, Tate Depo. at 314-15; CX 1729 at 96).

551. During a meeting in Korea in October 1995, Rambus informed Samsung that SyncLink and fast SDRAMs were heading in the direction where they might infringe future Rambus patents. (CX 2111, Tate Depo. at 316-18; CX 1729 at 109).

552. During a meeting in Japan in October 1995, Rambus informed NEC that SyncLink and new SDRAMS (SDRAMs using a PLL or dual-edge clock) might end up in a position where they infringed future Rambus patents. (CX 2111, Tate Depo. at 319-20; CX 1729 at 119).

553. During a meeting in Japan in October 1995, Rambus informed OKI of the possibility that there would be Rambus intellectual property that might apply to SyncLink and new SDRAMs. (CX 2111, Tate Depo. at 320-21; CX 1729 at 123).

554. During a meeting with Intel in October 1995, Rambus informed Intel that it did not see how future memory chips could meet performance goals without using some or all of Rambus's inventions. (CX 2111, Tate Depo. at 322-24; CX 1729 at 134-36).

555. DRAM manufacturer Micron Technology demonstrated its concern about Rambus's patents in 1995 and 1996. On November 7, 1995, Micron executive Jeff Mailloux sent a memo entitled "Rambus Inc. Patents" to several other Micron employees, including JEDEC representative Terry Walther. (RX 629; RX 630). Mr. Mailloux's memorandum stated in part as follows:

> "Attached are abstracts for the patents that have been granted to RAMBUS Inc. so far . . . . Please consider both the quality (is there prior art?) and the breadth (apply to more than just RAMBUS?) of the patents."

(RX 629 at 1; RX 630 at 1).

556. Mitsubishi's Japanese patent department was also busy looking for prior art to Rambus's patents in November 1995. (RX 1041A at 1) ("[W]e have obtained Cray Corporation's patents to investigate the prior art for the patents owned by Rambus Inc. . . .").

557. In January 1996, the concerns of Micron and others about Rambus's intellectual property were reflected in the minutes of the SyncLink Consortium:

> "Rambus has 16 patents already with more pending. Rambus says their patents may cover our SyncLink approach even though our method came out of early RamLink work. Micron is particularly concerned to avoid the Rambus patents, though all of us share this concern."

(RX 663 at 2).

558. Others who took a close look at Rambus's intellectual property in this time period included Dr. David Gustavson, the Secretary of the SyncLink Consortium, who reviewed several European patent applications that Rambus had filed. (Gustavson, Tr. 9286). Dr. Gustavson has testified that he recognized immediately upon reviewing the Rambus patent applications that they had a broad scope that would apply to virtually any memory device, but that he believed the applications would never be allowed in light of their breadth. (Gustavson, Tr. 9287).

559. Dr. Gustavson testified that two Apple engineers, David James and Glen Stone, reviewed the Rambus patent applications along with him. (Gustavson, Tr. 9286).

560. Rambus's separation from JEDEC was formalized on June 17, 1996, when Rambus sent a letter to the JEDEC office that stated:

> "I am writing to inform you that Rambus Inc. is not renewing its membership in JEDEC.
>
> Recently at JEDEC meetings the subject of Rambus patents has been raised. Rambus plans to continue to license its proprietary technology on terms that are consistent with the business plan of Rambus, and those terms may not be consistent with the terms set by standards bodies, including JEDEC. A number of major companies are already licensees of Rambus technology. We trust that you will understand that Rambus reserves all rights regarding its intellectual property. Rambus does, however, encourage companies to contact Dave Mooring of Rambus to discuss licensing terms and to sign up as licensees.
>
> To the extent that anyone is interested in the patents of Rambus, I have enclosed a list of Rambus U.S. and foreign patents. *Rambus has also applied for a number of additional patents in order to protect Rambus technology.*"

(CX 887 (emphasis added)).

561. Complaint Counsel have contended that Rambus deliberately omitted its newly issued '327 patent from the list of patents attached to its June 17, 1996 letter to JEDEC, and that the claims of the '327 patent would have alerted JEDEC members to the breadth of Rambus's potential patent claims. Complaint Counsel have pointed to the

omission of the '327 patent as evidence of an intent to mislead. There was no evidence at trial, however, to support this contention. Instead, the only evidence presented on the issue showed that the '327 patent was left off the list of Rambus's patents by mistake. It was Lester Vincent's responsibility to compile the list of patents sent to JEDEC with the letter confirming Rambus's withdrawal. (CX 3129, Vincent Micron Depo. at 538.) Mr. Vincent did not purposely leave the '327 patent off the list. (*Id*.). The list was compiled in connection with an earlier draft of the letter in late March 1996 and was not updated when the letter was sent in June 1996. (CX 879 at 3; CX 3129, Vincent Micron Depo. at 490-91.) There was also no evidence at trial that any JEDEC member had reviewed or relied upon the list of patents. In any event, as discussed at Findings 591-3, the '327 patent was on a list of Rambus patents circulated in 1998 by Hyundai to a large group of DRAM manufacturers, putting them in the same position as if the '327 patent had been identified by Rambus.

B. There Is Substantial Evidence That After Rambus Left JEDEC, JEDEC Leaders and Members Were Aware Of Possible Rambus Intellectual Property Claims.

562. The evidence shows that after Rambus confirmed its departure from JEDEC in June 1996, JEDEC members and leaders were aware of possible Rambus intellectual property claims and even investigated the prior art that might defeat those claims.

563. In October 1996, for example, **{IN CAMERA MATERIAL REDACTED}** (RX 781 at 2) (*in camera*).

564. In December 1996, Micron executive Jeff Mailloux wrote a memorandum to Micron CEO Steve Appleton that stated in part that:

> "We have been investigating high speed DRAMs and the intellectual property associated with them for some time now. . . . We have also been investigating the prior art related to the area of high-speed DRAMs. From our research, we think many Rambus patents read on prior art or other patents."

(RX 829 at 2).

565. Micron has also withheld several documents from this time period that relate to Rambus patent claims. For example, a May 28, 1997 e-mail from a Micron employee to a Micron attorney is described on Micron's privilege log as a "[c]onfidential communication regarding persons knowledgeable about Rambus patents." (RX 1920 at 422). Two months earlier, on March 26, 1997, a Micron lawyer sent an e-mail to Micron JEDEC representatives Terry Lee and Kevin Ryan that is described on the Micron privilege log as a "[c]onfidential communication regarding Rambus patents." (RX 1920 at 152). In April 1997, Mr. Ryan sent an e-mail to Mr. Lee and to attorney David Westergard that is again described as a "[c]onfidential communication regarding Rambus patents." (RX 1920 at 153).

566. These latter two e-mails coincide with the March 1997 JEDEC meeting, where Micron's JEDEC representatives demonstrated that they were well aware that Rambus's intellectual property reached *beyond* the RDRAM architecture and its so-called "packetized" and "narrow bus" features.

567. The minutes of the March 1997 JC 42.3 meeting reflect that during a presentation regarding an NEC proposal involving DDR SDRAM, a representative stated that "[s]ome on the committee felt that Rambus had a patent on that type of clock design." (JX 36 at 7).

568. Micron representative Terry Lee was present at the March 1997 JC 42.3 meeting. He testified that he had raised the concern about a possible Rambus patent at the meeting that is reflected in the minutes. (Lee, Tr. 6957-8; JX 36 at 7).

569. The NEC representative's trip report for the March 1997 JEDEC meeting supports Mr. Lee's recollection, for it includes the following summary of the discussion regrading the NEC DDR proposal:

"Company	Comments
Micron	This technique is patented by Rambus and they will not agree to the JEDEC patent policy.
Mosaid/VLSI	This may be a future bus concept. Future bus was invented before Rambus became a company, so this may not be a valid patent."

(RX 880 at 25).

570. Mr. Lee also sent an e-mail on April 17, 1997 to Micron attorney David Westergard "regarding meeting summary and DDR." (RX 1920 at 421). This e-mail has been withheld by Micron on privilege grounds. (*Id*.).

571. Complaint Counsel have contended that JEDEC members had long believed that Rambus's intellectual property claims would reach only to the "packetized," "narrow bus" RDRAM architecture. As Mr. Lee testified, however, the NEC DDR proposal did *not* involve a "narrow bus" and was *not* "packetized." (Lee, Tr. 6961).

572. Mr. Lee agreed that by March 1997, he thought that Rambus might have intellectual property claims relating not just to RDRAMs but to the work of the JC 42.3 committee as well. (Lee, Tr. 6962-2).

573. In April 1997 – two years *before* the DDR SDRAM device was standardized by JEDEC – Mr. Lee and other Micron JEDEC representatives learned that Rambus intended to seek intellectual property rights with respect to the use of dual edge clocking in *all* memory devices.

574. On April 16, 1997, a Micron employee named Keith Weinstock sent an e-mail to various Micron employees that stated in part that "Rambus plans legal action to request royalties on all DDR memory efforts." (RX 920 at 2).

575. At the time he prepared his April 16, 1997 e-mail, Mr. Weinstock was a Micron account representative with responsibility for Intel. (Lee, Tr. 6700, 6968).

576. Mr. Weinstock sent his April 16, 1997 e-mail, and its statement that "Rambus plans legal action to request royalties on all DDR memory efforts," to Jon Biggs, with a copy to Terry Walther, Jeff Mailloux, Terry Lee, Kevin Ryan, Gary Welch and Steve Trick. (RX 920 at 1).

577. At the time, Mr. Biggs was Mr. Weinstock's predecessor as the Micron account representative for Intel. (Lee, Tr. 6967). Mr. Mailloux was Micron's DRAM Marketing Manager at the time. (CX 3133, Mailloux Micron Depo. Tr. 4/5/01, 44:20-45:6). Mr. Walther was a JEDEC representative for Micron. (Lee, Tr. 6594, 6953). Mr. Welch was in Product Marketing at Micron, with responsibility for Rambus product. (Lee, Tr. 6967). Mr. Trick was a Micron employee responsible for module development. (Lee, Tr. 6973). Mr. Lee was in the Strategic Marketing department at Micron, reporting to Mr. Mailloux. He also attended JEDEC meetings frequently in the 1997-2000 time period. (Lee, Tr. 6591-95). Mr. Ryan was in a similar position as Mr. Lee and also attended JEDEC meetings in this time period. (Lee, Tr. 6601; JX 37 at 2; JX 39 at 2; JX 41 at 2; JX 43 at 1; JX 46 at 2, JX 49 at 1).

578. On April 17, 1997, Micron JEDEC representative Terry Walther responded to Mr. Weinstock's e-mail and asked him to confirm the report about Rambus's intellectual property claims:

> "Does Rambus believe they have a patent on changing data on both edges of the clock? . . . I think that is old technology. Can you find out what they think they have?"

(RX 920 at 1).

579. Mr. Weinstock responded to Mr. Walther's question:

> "*Yes, Rambus feels DDR for any memory is under their patent coverage.* James [Akiyama, an Intel employee] said that Rambus has more IP than Intel has seen. He further stated the determining factor would be whether the courts take a broad or a narrow view of the patents."

(RX 920 at 1) (emphasis added).

580. The April 17, 1997 response by Mr. Weinstock was copied to Mr. Mailloux, Mr. Lee and all of the other recipients of Mr. Weinstock's original e-mail. (RX 920 at 1).

581. Mr. Lee testified that he understood Mr. Weinstock's statement about Rambus's intellectual property claims over "DDR for any memory" to be a reference to the DDR SDRAM device that was then being discussed at JEDEC. (Lee, Tr. 6968).

582. Mr. Lee also understood that Mr. Weinstock was referring to possible patent infringement lawsuits by Rambus when Mr. Weinstock wrote:

> "Rambus plans legal action to request royalties on all DDR memory efforts."

(Lee, Tr. 6971-2; RX 920 at 2).

583. Mr. Lee testified that he did nothing at all to follow up on the reference to Rambus's intellectual property claims regarding "DDR for any memory." (Lee, Tr. 6702, 6972; RX 920 at 1).

584. Mr. Lee testified that as far as he knows, none of the other recipients of Mr. Weinstock's April 17, 1997 e-mail did anything to follow up on the reference to Rambus's intellectual property claims. (Lee, Tr. 6972-3).

585. Mr. Lee explained that he had not followed up with respect to the information regarding Rambus's possible intellectual property claims, and did not consider asking JEDEC to request "RAND" assurances from Rambus, because he "didn't believe this was true." (Lee, Tr. 6981).

586. After reviewing the April 16 and 17, 1997 Micron e-mails during trial, 42.3 chairman Gordon Kelley testified that he believed that the Micron JEDEC representatives who received the e-mails were obligated under the JEDEC patent policy to tell the JC 42.3 committee the information about Rambus's claims that is contained in the e-mails. (Kelley, Tr. 2748-9).

587. In May 1997, Rambus engineer Richard Crisp met with the Vice President of Engineering for VIA Technologies, a chipset manufacturer based in Taiwan. (RX 924 at 1).

588. Mr. Crisp's e-mail regarding the May 1997 meeting states in part that the VIA executive had:

> ". . . told me that he thinks that SyncLink is going to be stepping all over Rambus patents. I told him that no one can know for sure about any of that until chips exist, but that since we were first and have a lot of fundamental patents, it would not be a surprise to find that to be the case, and if it were, that I felt quite sure we would pursue protection of our IP rights."

(RX 924 at 1).

589. In July 1997, the official SyncLink Consortium minutes reflect a concern that the Consortium should "collect information relevant to prior art and Rambus filings" in anticipation that "Rambus will sue individual companies" for patent infringement. (RX 966

at 3).

590. At the next SyncLink Consortium meeting, some attendees were re-thinking their desire to obtain information relating to Rambus patents. As one attendee pointed out, "you may not want to know because that multiplies the damages," an apparent reference to the treble damages available from willful infringers. (RX 1001 at 5).

591. In January 1998, Micron JEDEC representative Terry Lee **{IN CAMERA MATERIAL REDACTED}** (RX 1095 at 4). **[IN CAMERA]**.

592. In July 1998, a Hynix executive sent an e-mail containing "a list of Rambus patents" to a large group of DRAM engineers and JEDEC representatives from such companies as Micron, Texas Instruments, IBM, VLSI, Compaq, Mosaid and Siemens. (RX 1214 at 1).

593. The list of patents provided by the Hynix executive included the '327 patent that Rambus had left off the list of patents submitted with its JEDEC resignation letter. (RX 1214 at 1).

594. Complaint Counsel's technical expert, Dr. Bruce Jacob, who has testified (contrary to Rambus's expert) that claims contained in the '327 patent are infringed by memory devices that comply with the DDR SDRAM standard, has *also* testified that if the engineers who received the July 1998 e-mail (RX 1214), were reasonable engineers, *they would have known* from looking at the '327 patent that it covered the DDR SDRAM device

they were working on at the time. (Jacob, Tr. 5675).

595. In light of the foregoing, it is clear that after Rambus left JEDEC, various JEDEC members were aware of possible Rambus patent claims relating to the work of the JC 42.3 committee. There is no record evidence that any of these members contacted Rambus to make any further inquiry regarding those possible claims or to ask Rambus for "RAND" assurances.

VII. RAMBUS INFORMED THE INDUSTRY AND THE WORLD OF ITS INTENT TO OBTAIN BROAD PATENT PROTECTION FOR ALL OF ITS INVENTIONS.

A. Introduction.

596. It is not surprising that JEDEC leaders and JEDEC members were aware of and concerned about the possibility that Rambus could obtain patent protection that extended beyond the RDRAM architecture. As discussed below, Rambus informed the public and the DRAM industry throughout the early 1990's that it was seeking broad intellectual property protection. Moreover, as discussed below, a review of any of Rambus's published patents or patent applications would have made it clear to a reasonably experienced engineer or patent lawyer that Rambus's patents could cover the use of various features in any synchronous DRAM.

B. Rambus's Public Disclosures In 1992 Told The World Of Rambus's Desire To Obtain Broad Patent Coverage.

597. On March 9, 1992, Rambus held simultaneous events in the Silicon Valley and in Tokyo to publicly announce its technology and its business plan. (Farmwald, Tr. 8182-84;

RX 67 at 1). Prior to this date, Rambus had presented its technology to companies on an individual basis and had secured licenses from three of the top five DRAM manufacturers: Fujitsu, NEC, and Toshiba. (RX 67 at 2).

598. The press release announcing these events stated that Rambus's revolutionary technology would offer a tenfold improvement over traditional DRAMs and would solve the memory bottleneck. (RX 67 at 1). The press release also described Rambus's business plan as licensing its technology in return for license fees and royalties. (RX 67 at 2). By controlling the Rambus interface standard, Rambus would ensure compatibility. (RX 67 at 2). The press release also made it clear that Rambus's "open standard" would be "available for license by any IC company." (RX 67 at 2; *see also* Farmwald, Tr. 8185).

599. At the events, Rambus made available a "Corporate Backgrounder" that provided an overview of Rambus's business strategy and its technology. (RX 81; Farmwald, Tr. 8186). The Backgrounder explicitly detailed Rambus's intellectual property strategy: "Rambus Inc. is fully protecting the intellectual property rights of its technology by filing basic, broad patents in all major industrial nations around the world." (RX 81 at 3). This statement reflected Rambus's patent application activity. (Farmwald, Tr. 8186-87).

600. Later in this same public document, there are descriptions of Rambus's technology. (RX 81 at 8-11). The Backgrounder states that Rambus's "dramatic performance improvements were achieved through numerous technical breakthroughs" and then proceeds to describe "[s]ome of the major technical highlights of the Rambus solution" (RX 81 at 8).

The technology descriptions included the use of dual-edge clocking: "An innovative electrical interface permits the Rambus Channel to operate at 500 Megabytes/second by using both edges of a 250 MHz clock." (RX 81 at 8). Moreover, the technology descriptions explicitly state that Rambus used the on-chip PLL/DLL technology: "Clock skew and capacitance loading are minimized by a phase lock loop circuit on board both the master and the RDRAM." (RX 81 at 8).

601. The Backgrounder also made it clear that Rambus's technology was divided into three distinct elements of the memory system: the Rambus Channel (the high-speed bus); the Rambus Interface (the circuitry that connects a device, such as a controller or DRAM, to the bus); and the Rambus DRAM (the memory itself). (RX 81 at 7; Farmwald, Tr. 8188-8190).

602. The Backgrounder also informed every reader that Rambus's business strategy was to license its technology, work with the licensee to help implement the technology, and to receive fees and royalties in return. (RX 81 at 3; see also Farmwald, Tr. 8187). Moreover, it stated that "Rambus technology is an open standard that Rambus Inc. will license to any IC company." (RX 81 at 3).

603. Later that year, at the invitation of Betty Prince (Prince, Tr. 8986-87), Dr. Farmwald and David Mooring of Rambus published an article in the October 1992 issue of IEEE Spectrum, which gave a brief description of the Rambus technology and stated that the "technology behind the architecture can be licensed for a royalty fee comparable to that for other patented technologies." (RX 332 at 1).

604. Testimony at trial confirms that Rambus's business model was well known in the industry during the time Rambus attended JEDEC meetings. Brett Williams, a JEDEC representative for Micron testified that in 1992, "I knew it was [Rambus's] business model to patent their technology, and that's how they would gain their revenues." (Williams, Tr. 857). Similarly, Martin Peisl of Infineon stated that he was aware of Rambus's business model in the early 1990's and expected Rambus to get patents to cover their technology. (Peisl, Tr. 4505).

605. According to Andreas Bechtelsheim, formerly of Sun Microsystems, Rambus made very clear to Sun that it intended to seek patent coverage for all of its inventions and developments, and Rambus explained to various companies, including Sun, that it was seeking patent coverage for its inventions because it intended to obtain revenue or earn revenue through licensing its technology to both memory manufacturers and system manufacturers. (Bechtelsheim, Tr. 5819).

C. Rambus Disclosed Its Inventions To The DRAM Industry.

1. Rambus Disclosed Its Inventions During Visits To DRAM Manufacturers And Systems Companies.

606. In 1989-90, Drs. Farmwald and Horowitz made visits to many DRAM manufacturers and systems companies to try to convince them about the benefits of their approach and to get feedback from them. (Horowitz, Tr. 8515).

607. Among the DRAM manufacturers that Drs. Farmwald and Horowitz visited in 1989-90 were Texas Instruments, IBM, Toshiba, Fujitsu, Mitsubishi, NEC, Matsushita, Micron and Siemens. (Horowitz, Tr. 8515; Farmwald, Tr. 8166).

608. Among the systems companies that Drs. Farmwald and Horowitz visited in 1989-90 were IBM (both a DRAM manufacturer and a systems company), Sun Microsystems, Motorola, Apple, SGI and Tandem. (Horowitz, Tr. 8515-16; Farmwald, Tr. 8166-7).

609. The response to the early presentations in 1989-90 was "just disbelief" that Drs. Farmwald and Horowitz would be able to achieve a 500 megabit per second DRAM data rate. (Horowitz, Tr. 8516). People who listened to these presentations were also skeptical about many of the specific features of the technology. For example, it was felt that putting registers on a DRAM was too expensive for a commodity part and that one could not put a phase locked loop or a delay locked loop on the DRAM itself. (Horowitz, Tr. 8517).

610. The four inventions at issue in this case were described in these early presentations. For example, one of the early presentations that Dr. Horowitz gave, with slides dated January 31, 1990, states that the Rambus interface "allows 'block mode' transfer from an individual DRAM" with "1-1024 byte long blocks supported." (RX 29 at 9; Horowitz, Tr. 8518-20). This describes variable block size or variable burst length. (Horowitz, Tr. 8520).

611. The January 31, 1990 presentation also describes the use of a delay locked loop on the DRAM to reduce clock skew. (RX 29 at 33-34; Horowitz, Tr. 8521-22).

612. The January 31, 1990 presentation also refers to the dual-edge clocked or double data rate technique. (RX 29 at 34; Horowitz, Tr. 8522-23).

2. Rambus Disclosed Its Inventions In Technical Descriptions Of The Rambus Technology.

613. In the 1990-91 period, Dr. Horowitz prepared detailed technical descriptions of the Rambus technology. (Horowitz, Tr. 8523). These documents were for Rambus's internal use and were also used with customers and potential customers to convince them of the merits of Rambus technology and to help them build it. (Horowitz, Tr. 8523-24).

a. The May 1990 Technical Description Discloses the Rambus Inventions.

614. One of these technical descriptions is dated May 7, 1990 and was generated at about that time. (RX 63; Farmwald, Tr. 8168-69; Horowitz, Tr. 8524-25).

615. The fax line on the May 7, 1990 technical description indicates that it was sent to Siemens. (Farmwald, Tr. 8168).

616. The May 7, 1990 technical description discloses all four of the technological features at issue here. (Horowitz, Tr. 8525). For example, the technical description disclosed dual-edge clocking in a figure with two input receivers, one clocked by a signal designated "CLK" (clock) and the other clocked by the complement of CLK (clock bar), a signal that is zero when clock is one and vice versa. (RX 63 at 10; Horowitz, Tr. 8525-

26). This means that one receiver samples an input when the clock goes high (the rising edge of the clock) and the other when the clock goes low (the falling edge). (Horowitz, Tr. 8526). This is the dual-edge clocking feature.

617. The May 7, 1990 technical description also discloses a delay-locked loop on the DRAM. (Horowitz, Tr. 8527-28). A figure in the technical description shows two delay locked loops generating the internal clocks for Rambus design. (RX 63 at 14; Horowitz, Tr. 8527). This is the on-chip DLL feature.

618. The May 7, 1990 technical description also discloses programmable latency. (Horowitz, Tr. 8528). In the "device registers" section of the document an "access time" or latency register is listed. (RX 63 at 18; Horowitz, Tr. 8528). "Latency" refers to the time between request and response. (Horowitz, Tr. 8530). The document explains that a fixed value for latency "does not allow for technology improvements," and, consequently, the Rambus system "set[s] the time between request and response during system reset." (RX 63 at 5; Horowitz, Tr. 8530-31). In other words, the value in the access time or latency register would be fixed when the system was started up and probably would not be changed after that time. (Horowitz, Tr. 8531). This is the programmable latency feature.

619. The May 7, 1990 technical description also discloses variable burst length. (Horowitz, Tr. 8528-29). The document contains a table showing a variable number of bytes in the block size or burst length depending on the value in the "BlockType" field. (RX 63 at 21; Horowitz, Tr. 8528-29). This is the variable burst feature.

b. The November 1990 Technical Description Discloses The Rambus Inventions.

620. A later Rambus technical description, dated November 5, 1990, was generated at around that time. (RX 94; Farmwald, Tr. 8169; Horowitz, Tr. 8535).

621. The November 5, 1990 technical description was sent to Siemens. (RX 99; Farmwald, Tr. 8169-70).

622. The November 5, 1990 technical description disclosed dual-edged clocking. First, the document contains the same figure relating to inputting data on both edges of the clock as in the May 7, 1990 description. (RX 63 at 10; RX 94 at 15; Horowitz, Tr. at 8535). Second, the document shows that the output data is also being transmitted on both edges of the clock. (RX 94 at 19; Horowitz, Tr. 8536).

623. The November 5, 1990 technical description disclosed two alternatives for the DRAM clock circuitry. One alternative was to use a phase locked loop. (RX 94 at 45; Horowitz, Tr. 8536-37). The other alternative was to use delay locked loops. (RX 94 at 46; Horowitz, Tr. 8537).

624. The November 5, 1990 technical description disclosed variable latency using a data delay field in the request packet. (RX 94 at 59; Horowitz, Tr. 8537-38).

625. The November 5, 1990 technical description disclosed variable block size or burst length with a table similar to that in the May 7, 1990 technical description. (RX 63 at 21; RX 94 at 60; Horowitz, Tr. at 8538).

c. Siemens Responded to the Technical Descriptions with a List of Questions about Rambus's Inventions.

626. Both Dr. Farmwald and Dr. Horowitz received feedback from Siemens regarding the November 5, 1990 technical description. (RX 102; RX 117; Farmwald, Tr. 8171-72; Horowitz, Tr. 8541-42).

627. A fax from K. Horninger of Siemens to Dr. Farmwald, dated December 7, 1990, contained a detailed list of questions relating to the November 5, 1990 technical description. (RX 102; Farmwald, Tr. 8171-73).

628. A fax from H.J. Neubauer of Siemens to Dr. Horowitz, dated January 29, 1991, stated "Dear Dr. Horowitz, concerning the RAMBUS Technical Description some basic items remained open. In the following we present a list of detailed questions to you which we would like to get answered." (RX 117 at 2; Horowitz, Tr. 8542).

629. A number of the questions in the fax that Siemens sent to Dr. Horowitz related to the four features of Rambus technology at issue in this case. Question number one in the Siemens fax asked about the details of how eight bits of data would be transmitted by the DRAM and relates to Rambus's variable block size feature. (RX 117 at 2; Horowitz, Tr. 8543-44).

630. Question number two in the Siemens fax asked about the implementation of variable latency in the Rambus technology. (RX 117 at 2; Horowitz, Tr. 8544).

631. Another question in the Siemens fax referenced Figure 13 on internal page 14 of the November 5, 1990 technical description. (RX 117 at 4). That figure showed

dual-edge clocking or double data rate on the output. Dr. Horowitz's understanding was that Siemens' question related to the implementation of the double data rate drivers as shown in the November 5, 1990 technical description. (RX 94 at 19; RX 117 at 4; Horowitz, Tr. 8546).

632. Another question in the Siemens fax referenced Figure 28 on internal page 41 of the November 5, 1990 technical description. (RX 117 at 4). That figure shows a delay locked loop and Siemens' question was about the delay locked loop. (RX 94 at 46; RX 117 at 4; Horowitz, Tr. 8546).

d. <u>The April 1991 Technical Description Discloses the Rambus Inventions</u>.

633. A still later Rambus technical description was released on April 1, 1991 and was a more complete version with many more technical details. (RX 130; Farmwald, Tr. 8171; Horowitz, Tr. 8538).

634. The April 1, 1991 technical description disclosed dual-edged clocking. The document contains the same figure relating to inputting data on both edges of the clock as in the May 7, 1990 and November 5, 1990 descriptions. (RX 63 at 10; RX 94 at 15; RX 130 at 36; Horowitz, Tr. at 8539).

635. The April 1, 1991 technical description disclosed using a phase locked loop on the DRAM. (RX 130 at 56; Horowitz, Tr. 8539).

636. The April 1, 1991 technical description disclosed programmable latency through the use of a "read delay" or latency register. (RX 130 at 94; Horowitz, Tr. 8539-40).

637. The April 1, 1991 technical description disclosed variable block size or burst length, with the value in a "count" field representing the number of bytes to be transferred. (RX 130 at 64; Horowitz, Tr. at 8539).

3. Rambus Disclosed Its Inventions In A Series Of Public Documents.

a. Rambus Disclosed Its Inventions In A Marketing Brochure.

638. In early 1992, Rambus produced and distributed its first marketing brochure about Rambus technology. (RX 2183; Horowitz, Tr. 8547). The 1992 marketing brochure disclosed the four features of Rambus technology at issue here. (Horowitz, Tr. 8547-48).

639. The 1992 marketing brochure states that the "heart of [the Rambus] Interface is high performance PLL (phase-locked-loop) circuitry which provides the clocks for transmitting and receiving Rambus Channel data." (RX 2183 at 6).

640. The 1992 marketing brochure also states that there can be "Transfers of 1 to 256 Bytes per Request . . . ." (RX 2183 at 7). This discloses variable burst length, because data transfers could involve a variable amount of data.

641. The 1992 marketing brochure also states that "Data is effectively transferred on both edges of the clock." (RX 2183 at 9). This discloses dual-edge clocking.

642. The 1992 marketing brochure also states that "the Read Data Packet is returned a time ReadDelay after the Request Packet" and that this delay value is "programmed into the configuration registers of all devices during system initialization." (RX 2183 at 11). This discloses programmable latency.

b. Rambus Disclosed Its Inventions In Publications Describing The First Rambus DRAM

643. The first Rambus DRAM was a 4.5 megabit Rambus DRAM produced by Toshiba in the 1991-92 time frame. (Horowitz, Tr. 8548-49).

644. A paper about the Toshiba 4.5 megabit Rambus DRAM was presented at the 1992 International Symposium on VLSI Circuits (VLSI Circuits Symposium) and published in the proceedings of that symposium. (RX 301 at 76-77; Horowitz, Tr. 8552-54).

645. The VLSI Circuits Symposium is held annually and is one of the top two conferences in the world for circuit designers (Horowitz, Tr. 8552). The "technical program committees" of the Symposium read all the papers submitted and choose the better ones for publication at the conference. (Horowitz, Tr. 8552-53). The technical program committees for the 1992 VLSI Circuits Symposium that selected the paper about the Toshiba 4.5 megabit Rambus DRAM included representatives from IBM, Texas Instruments, Siemens, Sun Microsystems, Intel, Hitachi, Samsung, Matsushita, Mitsubishi, Fujitsu, Sanyo, Oki, and NEC. (RX 301 at 5).

646. The paper published in the proceedings of the 1992 VLSI Circuits Symposium about the Toshiba 4.5 megabit Rambus DRAM discusses the four features of Rambus technology at issue in this case. (Horowitz, Tr. 8554). Figure 2 of the paper shows a block size transfer and read latency. (RX 301 at 77; Horowitz, Tr. 8555). Figure 3 of the paper shows double data rate input receivers. (*Id*.). The paper also states that "[t]o eliminate skew caused by the internal circuitry, the DRAM contains two PLLs." (RX 301 at 76; Horowitz, Tr. 8555).

647. At the end of the 1992 VLSI Circuits Symposium, the authors of the top papers were invited to provide a longer version to be published in the Journal of Solid State Circuits. (Horowitz, Tr. 8555-56). The Journal of Solid State Circuits is the most widely read journal for circuit designers. (*Id*.). The paper about the Toshiba 4.5 megabit Rambus DRAM was selected, and a longer version of that paper was published in the Journal of Solid State Circuits in April 1993. (RX 385; Horowitz, Tr. 8556).

D. Rambus's Inventions Were Discussed In The Press In Early 1992.

648. In connection with the public announcement of Rambus's technology and its business plan in March 1992, Rambus provided information to the press regarding Rambus's inventions, and numerous articles about Rambus appeared. (RX 1446).

649. Many of these articles provided a significant amount of technical detail. For example, an article entitled "Rambus Unveils Revolutionary Memory Interface" in the March 4, 1992 Microprocessor Report describes Rambus's technology in some depth.

(RX 1446 at 22-26).

650. The March 4, 1992 Microprocessor Report article discloses three of the four features of Rambus technology at issue here, as well as aspects of the fourth.

651. The article states: "The Rambus Channel is a 500-Mbyte/s interface operating with a 250-MHz clock and transferring a byte of data on each clock edge." (RX 1446 at 22). This discloses dual-edged clocking.

652. The article states: "A phase-locked loop on each Rambus device limits clock skew within the chip." (RX 1446 at 23). This discloses on-chip PLL.

653. The article states: "The six-byte request packet encodes a 36-bit address, a 4-bit operation code, an 8-bit transfer length count (in bytes). Byte addressing and block sizes of up to 256 bytes are supported." (RX 1446 at 24). This discloses variable burst length.

654. The article also notes that "control registers" on the DRAM can be used to specify certain parameters. (RX 1446 at 23). This is related to programmable CAS latency which, in SDRAMs, is programmed in a control register called a "mode register" on the DRAM.

1. Rambus's Early Patent Disclosures Gave Notice That Rambus Could Obtain Patents On The Four Technologies.

a. The History of the '898 Application.

655. After the filing of the '898 application, Rambus received an 11-way restriction requirement from the PTO – that is, the Patent Examiner determined that

Rambus was claiming 11 distinct categories of inventions in the '898 application. (Nusbaum, Tr. 1510).

656. After receiving the restriction requirement, Rambus elected one group of claims to prosecute in its original application and filed 10 divisional applications to pursue the other groups of claims identified in the restriction requirement. (Nusbaum, Tr. 1511).

657. The patents that Rambus has asserted against DRAM manufacturers have all issued from applications that are continuations or divisionals stemming from the original '898 application and all share a specification with that original application. (Stipulated Patent Tree, attached to Parties' First Set of Stipulations; Nusbaum, Tr. 1513-14).

658. Pursuant to the "written description" requirement for a patent's validity, the PTO determined that the claims of this patents were supported by the specification of the original '898 application, that is, that a person of ordinary skill in the art who was reviewing the '898 application would have understood that Rambus was in possession of the inventions claimed in the later patents as of the April 1990 filing date of the '898 application. *See* Findings ¶¶ 78, 87. Complaint Counsel have not challenged the validity of Rambus's issued patents.

b. <u>The PCT Application</u>.

659. On April 16, 1991, Rambus filed an international patent application pursuant to the Patent Cooperation Treaty (the "PCT application"). (CX 1454 at 1).

660. The PCT application is identical in all material respects to the '898

application. In particular, the PCT application contains the same written description, drawings, and 150 claims as the '898 application. (CX 1451; CX 1454; Fliesler, Tr. 8811).

661. The PCT application was published and made publicly available as of October 31, 1991. (CX 1454 at 1; The Parties First Set of Stipulations, Stipulation 8). Several JEDEC members obtained the PCT application in the early 1990's, including Mitsubishi and IBM. (RX 379A at 1; RX 201 at 1).

c. <u>The '898 and PCT Applications Disclose Numerous Inventions</u>.

662. The '898 and PCT applications each contain a lengthy disclosure consisting of a 62-page written description, 15 drawings, and 150 claims. (CX 1451, CX 1454).

663. The written description of the '898 and PCT applications contain numerous headings and subheadings, such as "Device Address Mapping," "Bus," "Protocol and Bus Operation," "Retry Format," "Bus Arbitration," "System Configuration/Reset," "ECC," "Low Power 3-D Packaging," "Bus Electrical Description," "Clocking," "Device Interface," "Electrical Interface - Input/Output Circuitry," and "DRAM Column Access Modification." (CX 1451 at 18, 20, 21, 30, 32, 37, 40, 43, 45, 47, 54; CX 1454 at 18, 20, 21, 30, 32, 37, 41, 44, 46, 48, 55).

664. A person of ordinary skill in the art to which the '898 and PCT applications pertain would have an electrical engineering degree and at least two to three years of

experience in designing computer memory circuits. (Nusbaum, Tr. 1613; Fliesler, Tr. 8779-80).

665. A person of ordinary skill in the art, an experienced DRAM designer, or a patent lawyer reviewing the '898 application or PCT application would not have thought that the inventions described in them were limited to a particular bus architecture. (Fliesler, Tr. 8788, 8811; Geilhufe, Tr. 9559). Instead, such individuals would recognize that although the applications describe how an entire system is to be put together, they also describe numerous technical features that can be used independently of one another and of the system. (Fliesler, Tr. 8788-89).

666. Indeed, as discussed further below, Mitsubishi engineers reviewed the PCT application in 1993 and did, in fact, recognize that the various innovations described therein were not limited to a particular bus architecture and could be used independently of one another. *See* Findings ¶¶ 669-671.

667. The '898 and PCT applications themselves note that, although a preferred implementation of the invention contains 8 bus data lines, "[p]ersons skilled in the art will recognize that 16 bus data lines or other numbers of bus data lines can be used to implement the teaching of this invention." (CX 1451 at 10; CX 1454 at 10). A person of ordinary skill in the art would recognize from this clear statement alone that the Rambus inventions were not limited to a particular "narrow" bus.

668. It was Dr. Horowitz's understanding when the patent application was filed that the various solutions to problems described in the application could be used independently of one another. Thus, if one did not want quite the level of performance that Drs. Farmwald and Horowitz envisioned, one could use only a subset of the techniques described in the patent application. (Horowitz, Tr. 8514-15).

669. Dr. Farmwald never thought of his ideas as implementing a "narrow" bus. (Farmwald, Tr. 8143). Rambus originally used a 9-bit wide bus because that corresponded to the number of pins that could fit on the edges of the chips that existed at the time; later Rambus used wider buses because more pins could be placed on the chip. (Farmwald, Tr. 8143-44). While some of the inventions of Drs. Farmwald and Horowitz might enable narrower busses to work better, the inventions are not specific to a particular bus width. (Farmwald, Tr. 8144).

670. As discussed below, Mitsubishi engineers who reviewed the PCT application came to the conclusion that the various technologies disclosed therein could be used independently of one another and independently of the bus architectures described in the application.

671. A March 12, 1993 Mitsubishi memorandum begins by stating that "A need has arisen to evaluate in detail all of the claims in a patent being applied for by Rambus (1 patent, a total number of claims is 150)." (RX 2214A at 1). The memorandum goes on to list guidelines for this evaluation, including "1) Do not discuss Rambus interface.

2) Determine whether or not any other areas contain technologies that will be important in increasing memory speed in the future." (RX 2214A at 1).

672. A June 10, 1993 Mitsubishi document with the heading "RAMBUS Patent (summary of responses)" states: "In addition to the technologies of narrower bus width and communication by protocol that are described above, the RAMBUS patent includes a variety of requirements such as memory system configuration, packaging method, and device configuration, and it can be achieved through a combination of these factors." (RX 406 at 4). The document continues: "The individual technologies that appear in the RAMBUS patent will be used independently in the future." (RX 406 at 4).

d. <u>The '898 and PCT Applications Disclose Programmable Latency</u>.

673. The '898 application and the PCT application describe access time registers that store latency, that is the amount of time between receiving a request and driving data onto the bus in response to that request. (CX 1451 at 16, 23; CX 1454 at 16, 23; Jacob, Tr. 5481). The applications state that "Each slave may have one or several access-time registers," where "slave" can refer to a DRAM. (CX 1451 at 16; CX 1454 at 16; Jacob, Tr. 5649).

674. In common use, programmable CAS latency in the mode register of an SDRAM is set at initialization. (Jacob, Tr. 5648-49). Likewise, the '898 application and PCT application state with respect to the access time registers (and other registers): "Most

of these registers can be modified and preferably are set as part of an initialization sequence . . . ." (CX 1451 at 16; CX 1454 at 16).

675. A person of ordinary skill in the art reviewing the '898 application or PCT application would understand that CAS latency on an SDRAM could be programmed using access time registers like those described therein. (Fliesler, Tr. 8784-85, 8791-93, 8811, 8904).

676. Indeed, Mitsubishi engineers who reviewed the PCT application recognized the correspondence between the access time registers in the PCT application and programmable CAS latency in SDRAMs. Thus, a Mitsubishi document headed "Assessment of Rambus Patents (Second Half) states next to the numbers 95, 97 and 103: "Modifiable Access Time Register (Similar to SDRAM latency control)." (RX 2213A at 25, 27). Claim 103 of the PCT application (and '898 application) is directed at a "modifiable access-time register." (CX 1454 at 105). Thus, Mitsubishi recognized that the PCT application and, in particular, Claim 103 of that application, related to the sort of mode register used to store a latency value in SDRAMs.

677. In a claim-by-claim analysis of the PCT application produced by Mitsubishi, a marginal note identifies claim 103 of the application as relating to "latency" and "SDRAM." (RX 2213A at 7). The analysis further indicates that Mitsubishi determined that this claim relating to latency in SDRAMs was particularly important, for Claim 103 was given a grade of "A." (*Id.*). A later page of the document explains that an "A" grade

means that a technology is "important for increasing DRAM speed. . . ." (RX 2213A at 27).

e. <u>The '898 and PCT Applications Disclose Variable Burst Length</u>.

678. The '898 application and the PCT application describe varying the "block size," that is the amount of data transmitted in response or received in response to a request. (CX 1451 at 29-30; CX 1454 at 29-30; Jacob, Tr. 5477-78). The applications each state that "BlockSize [0:3] specifies the size of the data block transfer." (CX 1451 at 29; CX 1454 at 29). The applications each contain a table showing the "Number of Bytes in Block" corresponding to the value in the "BlockSize" field. (CX 1451 at 30; CX 1454 at 30).

679. "Burst length" as the term is used in SDRAMs, refers to the amount of data to be transferred per read or write transaction. (Rhoden, Tr. 379-80; Jacob, Tr. 5396-97.) Likewise, "block size," as used in Rambus's patents encodes the amount of data to be transferred per read or write transaction. (Jacob, Tr. 5477.) The two terms describe the same function and are used interchangably. (Horowitz, Tr. 8661-62; Geilhufe, Tr. 9643.)

680. A person of ordinary skill in the art reviewing the '898 application or PCT application would understand that variable burst length is disclosed in it. (Fliesler, Tr. 8784-85, 8794-95, 8811, 8904-05).

f. The '898 and PCT Applications Disclose Dual-Edge Clocking.

681. The '898 and PCT applications state: "Clock distribution problems can be further reduced by using a bus clock and device clock rate equal to the bus cycle data rate divided by two, that is, the bus clock period is twice the bus cycle period. Thus a 500 MHz bus preferably uses a 250 MHz clock rate." (CX 1451 at 49; CX 1454 at 50). Since the clock rate is half the data rate on the bus, both edges of the clock are used to transmit data. (Fliesler, Tr. 8801-02).

682. Figure 10 in the '898 and PCT applications shows two input receivers clocked by "clock" and "clock bar" as in the Rambus technical descriptions. (CX 1451 at 147; CX 1454 at 148; Fliesler, Tr. 8799). Since "clock bar" is high when "clock" is low, and vice versa, data is input on both the rising and falling edges of clock. (Fliesler, Tr. 8799-8800).

683. Figure 13 in the '898 and PCT applications shows a timing diagram with data being input, as indicated by the arrows along the bottom of the figure, on both the rising and falling edges of the clock. (CX 1451 at 149; CX 1454 at 150). Howard Sussman, the JEDEC representative for Sanyo and formerly the JEDEC representative of NEC, testified that Figure 13 of the PCT application shows "input being sampled on the high and low edge of the clock" and that is "double data rate input." (Sussman, Tr. 1322, 1467-68).

684. A person of ordinary skill in the art reviewing the '898 application or PCT application would understand that dual edge clocking is disclosed in it. (CX 1451 at 49, 147, 149; CX 1454 at 50, 148, 150; Sussman, Tr. 1465-68; Fliesler, Tr. 8784-85, 8795, 8798-802, 8811, 8905).

g. The '898 and PCT Applications Disclose On-Chip DLL.

685. Figure 12 of the applications shows variable delay circuitry and a feedback loop. (CX 1451 at 148; CX 1454 at 149; Jacob, Tr. 5649-50). The figure would be recognized by an electrical engineer as containing a DLL. (Geilhufe, Tr. 9656).

686. A person of ordinary skill in the art or patent lawyer reviewing the '898 application or PCT application would understand that on-chip DLL is disclosed therein. (CX 1451 at 58-60, 148; CX 1454 at 59-61, 149; Fliesler, Tr. 8805, 8811, 8905).

687. When Joel Karp, then of Samsung, reviewed Rambus's PCT application in 1991, Figure 12 "jumped out" at him as evidencing a DLL. (CX 2078, Karp Micron Depo. at 119; CX 2114, Karp FTC Depo. at 276-77).

688. In its license negotiations with Rambus in 1994, Samsung was motivated to seek a non-assertion provision for non-Rambus-compatible uses of Rambus's inventions because of the on-chip DLL shown in Rambus's PCT application. (CX 2078, Karp Micron Depo. at 107-08, 119-20).

h. Review of the '898 or PCT Applications Would Raise Concerns that Rambus Might Be Able to Get Claims Over the Four Inventions.

689. A person of ordinary skill in the art or patent lawyer reviewing the '898 application or PCT application would have realized that Rambus might have claims broad enough to cover programmable CAS latency, programmable burst length, dual-edge clocking, and on-chip DLL. (Fliesler, Tr. 8784-85, 8810-11).

690. An experienced DRAM designer reviewing the PCT application would reach the conclusion that there is considerable similarity in form and function between programmable latency, variable burst length, dual-edge clocking, and on-chip DLL as disclosed in the PCT application and the corresponding features in SDRAMs or DDR SDRAMs. (Geilhufe, Tr. 9556-57).

691. If an experienced DRAM designer working on designing an SDRAM incorporating programmable latency and burst length in the early 1990s had reviewed the PCT application, he likely would have become concerned that Rambus might have claims to those features and would have raised the issue with management. (Geilhufe, Tr. 9558). Indeed, the evidence shows that experienced DRAM designers at IBM and Siemens reviewed Rambus's patent applications and did become concerned that Rambus might obtain patents that would cover SDRAMs. *See* Findings ¶¶ 468-482.

692. A manager faced with this issue, in light of the potential for substantial economic consequences if a DRAM design infringes a patent, would likely have gathered

additional technical analysis from specialists and, if there remained a concern, would have taken the issue to corporate counsel for a careful review. (Geilhufe, Tr. 9558-59). This conclusion is supported by the Mitsubishi documents, discussed below, that demonstrate a detailed analysis of Rambus's PCT application. It is further supported by the privilege logs and other documents produced by Micron and IBM which indicate that attorneys at those companies reviewed certain Rambus patents or applications. *See* Findings ¶¶ 485, 565-566.

693. When Mitsubishi reviewed the PCT application, it quickly undertook an in-depth study. A March 3, 1993 Mitsubishi memorandum has the subject line "Request for cooperation on evaluating Rambus (U.S.)'s patent application" and states in part:

> "Rambus Inc. of the U.S. has been approaching various Japanese companies to sell its high-speed data transfer technology . . . . Recently, we found a patent application (PCT International application) that appears to be related to [said technology] and began evaluating it, and realized that the technology is related not only to stand-alone semiconductor devices but also to systems. . . . [W]e would like to request the cooperation of your specialists in evaluating the contents of Rambus Inc.'s patent application. Please let us know which technology departments will be able to help us."

(RX 379A at 1).

694. A June 10, 1993 Mitsubishi document again stressed the need for expert analysis of Rambus's patent application to determine the scope of the claims, particularly as to individual technologies disclosed in the patent application: "There is a need to examine the specifications of the patent claims to determine whether individual

technologies used independently will infringe on the RAMBUS patent, and for that we will have to obtain the views and interpretations of experts." (RX 406 at 4).

695. On July 17, 1993, a Mitsubishi manager wrote:

> "The claims regarding the DRAM part expand in a variety of ways upon the specifications for DRAM on a Rambus, and, as a reference, *I translated and looked at those parts that looked the most like they could be investigated separately from the bus*. I would like to have a thorough search and investigation of the validity of these patents. . . ."

(RX 416A at 1) (emphasis added).

696. An August 16, 1993 Mitsubishi document again raised the issue of whether Rambus could have claims on features separate from any particular bus architecture:

> "[B]ecause there is the possibility that the claims will be narrowed to become a patent wherein the bus part is removed when Rambus itself is rejected, the DRAM folks will continuously perform detailed investigations into the applicability and into prior art." (RX 419A at 1).

697. Mitsubishi continued to keep a close watch on Rambus's patent portfolio. A January 11, 1996 memorandum indicates that Mitsubishi conducted an "investigation of the US patents owned by Rambus" that were granted by the end of October 1995 and that 18 patents met that criteria. (RX 528A at 1).

698. Mitsubishi also maintained a chart tracking all of Rambus's issued U.S. patents. For example, one version of this chart begins with Rambus's first issued U.S. Patent, 5,243,703, at number 1 and concludes with U.S. Patent no. 5,578,940 which

issued on November 26, 1996 at number 27. (RX 2216 at 2, 4). Rambus's '327 patent is listed at number 23 on the chart. (RX 2216 at 3).

699. A later version of the Mitsubishi chart contains 37 Rambus patents and includes patents that issued in early 1998. (RX 2218 at 3-6).

700. In its analyses of Rambus's patents, Mitsubishi focused on some of the four features at issue here. For example, as noted above, a Mitsubishi analysis of the claims of the PCT application specifically calls out the "modifiable access time register" and note its similarity to "SDRAM latency control." (RX 2213A at 27).

701. Mitsubishi also was clearly aware of potential Rambus patent claims over dual edged clocking. An August 24, 1996 report on a "Rambus meeting" states: "Rambus' patents. Issued: 16, filed: 80. For example, data is transferred at both edges." (RX 756A at 1).

702. A set of undated notes produced by Mitsubishi has the heading Rambus and picks out, among other features, "PLL," clock and clock-bar, and "modifiable register . . . Access Time (~ SDRAM @ Latency)." (RX 2211 at 1). "Clock" and "clock-bar" relate to the dual-edge clocking implementation disclosed in Rambus's '898 and PCT applications.

i. The Patent Office Has Determined That a Person of Ordinary Skill in the Art Would Understand from A Review of the '898 Application That Rambus Was in Possession of the Four Inventions.

703. As Complaint Counsel concede, Rambus has obtained patent claims that cover programmable CAS latency, variable burst length, dual-edge clocking, and on-chip

DLL as those features are used in SDRAMs and/or DDR SDRAMs. (Complaint, ¶ 91). Rambus has asserted claims covering these four features against SDRAMs and DDR SDRAMs. (Complaint, ¶ 92).

704. For example, claim 1 of Rambus's U.S. Patent 5,953,263, which issued on September 14, 1999, claims:

> "A synchronous semiconductor memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises:
> a programmable register to store a value which is representative of a delay time after which the memory device responds to a read request."

(CX 1517 at 29). This claim reads on an SDRAM or DDR SDRAM device containing a mode register to store a CAS latency value.

705. When examining claims, patent examiners use the broadest reasonable interpretation of the claim terms consistent with the patent specification. (Nusbaum, Tr. 1517-18). As Complaint Counsel's patent law expert explained:

> "This claim interpretation approach is used in the Patent & Trademark Office because it's very important that once a patent issues, and is asserted in a litigation, that a patentee doesn't assert an interpretation of a claim that's actually broader than what the patent examiner was using when he was searching for the prior art in determining patentability with respect to the prior art."

(Nusbaum, Tr. 1518-19).

706. Thus, the PTO has issued claims to Rambus that the PTO interpreted as broad enough to cover programmable CAS latency, variable burst length, dual-edge

clocking and on-chip DLL as those features are used in SDRAMs and/or DDR SDRAMs. It follows from the written description requirement that, in issuing those claims, the PTO has determined that the '898 application would clearly disclose to one of ordinary skill in the art that Rambus was in possession of these inventions as of the filing date of the '898 application. *See* Findings ¶¶ 78, 87. In other words, a person of ordinary skill in the art would, from reviewing the '898 application, identify broad inventions covering programmable CAS latency, variable burst length, dual edge clocking, and on-chip DLL, as those features are used in SDRAMs and DDR SDRAMs.

j. Professor Jacob's Testimony Regarding What an Engineer Reading the '898 Application Would Have Understood Is Entitled to Little Weight.

707. Professor Jacob has no patents to his name. (Jacob, Tr. 5650). There is no evidence in the record that he has ever applied for a patent or testified about patent issues, nor does he appear to have any patent-related experience at all. By contrast, many DRAM engineers, including many JEDEC representatives, are named inventors on patents or applications. For example, Desi Rhoden, formerly VLSI's JEDEC representative, testified that he was a named inventor on 15-20 patents. (Rhoden, Tr. 633). Mark Kellogg of IBM testified that he was an inventor on several patents. (Kellogg, Tr. 5307). Terry Lee of Micron testified that he was an inventor on many patents. (Lee, Tr. 6833). Brett Williams of Micron and Martin Peisl of Infineon also have patents to their names. (Williams, Tr. 960; Peisl, Tr. 4505-06).

708. As an academic who has never worked in the DRAM industry, Professor Jacob does not deal with intellectual property issues that arise in the industry. Professor Jacob is poorly equipped to opine as to what an engineer with patent experience would have understood from reading a patent application.

709. Given Professor Jacob's background, Rambus challenged his qualifications to render an opinion as to what a reasonable engineer in the early to mid-1990s would have understood from Rambus's '898 patent application. Complaint Counsel responded that "what we are doing is looking at the Rambus '898 application in order to determine the understanding that can be drawn out of that application." (Jacob, Tr. 5461). In other words, Complaint Counsel suggested that they were engaging in an objective inquiry, presumably based on Professor Jacob's current understanding from reviewing the '898 application. Complaint Counsel made no showing, however, that Professor Jacob's current understanding is relevant to the understanding of DRAM engineers in the early to mid-1990s.

710. Professor Jacob's testimony regarding what an engineer would have understood from reviewing the '898 application is also internally inconsistent. Professor Jacob testified that an engineer reading the '898 application during the 1990s would not have realized that Rambus could obtain patent rights over the dual-edge clocking feature as it was proposed for use or used in DDR SDRAMs because, in his opinion, the implementation described in the patent specification is different from that in DDR

SDRAMs. (Jacob, Tr. 5493). Professor Jacob also testified that the claims of the '327 patent would read on DDR SDRAMs. (Jacob, Tr. 5660). But, the specification of the '327 patent is identical in all material respects to the specification of the '898 application and, in particular, the two documents describe the same implementation of dual-edge clocking. Professor Jacob's opinion is, therefore, inconsistent with the legal determination made by the PTO in issuing the patent that the claims of the '327 patent are supported by its specification (and thus by the specification of the '898 application) from the point of view of a person of ordinary skill in the art.

711. In reaching his opinions about what an engineer in the 1990s would have realized from reviewing the '898 application, Professor Jacob did not consider the evidence in the record regarding what engineers in the 1990s actually did realize from reviewing the '898 application or the corresponding PCT application. In particular, Professor Jacob did not consider documents indicating that IBM and Mitsubishi had reviewed Rambus's PCT application and had concerns about the scope of Rambus's intellectual property coverage. (Jacob, Tr. 5661-67).

712. Although Professor Jacob spoke to various JEDEC members in connection with his work in this case, he did not ask any of them whether they had read the PCT application and, if so, what conclusions they had drawn. (Jacob, Tr. 5666-67).

713. The evidence of what engineers actually *did* realize when they reviewed the PCT application is more persuasive than Professor Jacob's opinion of what an engineer "would have" realized.

k. Rambus's '703 Patent Gave Notice that Rambus Could Obtain Patents Over the Four Inventions.

714. Rambus's first United States patent, U.S. patent no. 5,243,703 ("the '703 patent"), issued on September 7, 1993. (RX 425). Rambus disclosed the '703 patent to JEDEC during a committee meeting in September 1993. (The Parties' First Set of Stipulations, Stipulation 11). The '703 patent was subsequently added to the "patent tracking list" maintained by JEDEC, where it was described as involving a "Sync Clock." (JX 18 at 18).

715. The '703 patent can be traced back to a divisional application of the original '898 application. (RX 425 at 1; Fliesler, Tr. 8812).

716. The written description and drawings of the '703 patent, like all the issued patents that claim priority to the '898 application, are substantially the same as the written description and drawings in the '898 application. (RX 425 at 1; CX 1451 at 1; Fliesler, Tr. 8812, 8817). Thus, the '703 patent contains the same descriptions of programmable latency, variable burst length, dual-edge clocking, and on-chip DLL as in the '898 application and PCT application. (RX 425 at 7, 8, 9, 14-17, 21; Fliesler, Tr. 8819-20).

717. In addition to listing the original '898 application, the '703 patent's written description also contains a list of the nine other divisional applications stemming from the

'898 application that were pending at the time. (RX 425 at 11; Fliesler, Tr. 8813-14). An engineer with some familiarity with the patent system or a patent attorney would understand that the PTO had determined that the original '898 application disclosed multiple inventions and that Rambus was pursuing at least ten other inventions in related applications.

718. The subheadings in the "Detailed Description" section of the '703 patent would be one indication to a person of ordinary skill in the art that the inventors had worked not only on a whole system, but also on individual components and subcomponents of that system (RX 425 at 13-25; Fliesler, Tr. 8818).

719. A person of ordinary skill in the art or patent attorney reviewing the '703 patent would have understood that Rambus was claiming a number of different inventions claiming priority to the '898 application. (RX 425 at 24-25; Fliesler, Tr. 8818-19).

IX. JEDEC WOULD NOT HAVE ADOPTED DIFFERENT STANDARDS HAD RAMBUS MADE ADDITIONAL DISCLOSURES.

720. Even if Rambus made the additional disclosures Complaint Counsel allege should have been made, JEDEC would have adopted the same Rambus technologies into the SDRAM and DDR standards. This conclusion is supported by three distinct lines of evidence. Any one of these lines of evidence is sufficient to show that JEDEC would not have adopted alternative technologies.

721. First, what technologies JEDEC would have adopted had Rambus made the additional disclosures can be inferred from JEDEC's technology choices in the real world.

As discussed below, the doctrine of revealed preference shows that JEDEC would have adopted Rambus's technologies because JEDEC adopted them in the real world - even after Rambus began asserting its patents against DRAM manufacturers.

722. Second, a comparison of the alleged alternative technologies with the Rambus technologies in cost-performance terms demonstrates that the alternatives were inferior - even accounting for the royalties that Rambus is paid for the use of its technologies. This demonstrates two things: (1) JEDEC would have adopted the Rambus technologies because they are the best choice in terms of cost-performance characteristics and (2) both DRAM manufacturers and consumers are better off licensing the Rambus technologies than they would be using alternative technologies.

723. Third, a decision analysis examining both JEDEC's and Rambus's economic incentives and past behavior shows that had Rambus made the additional disclosures that Complaint Counsel allege should been made, JEDEC would have adopted the very same standard that it did in the real world, and JEDEC members would have negotiated with Rambus for licenses in the same circumstances that they did in the real world. In other words, assuming that Rambus had made the additional disclosures that Complaint Counsel allege should have been made, the outcome in this "but-for" world is the same as in the real world - nothing would have changed.

A. JEDEC Repeatedly Chose Rambus's Technologies, Even When Warned Of Rambus's Potential Patents, And Even After Rambus Began To Assert Its Patents.

724. The economic theory of revealed preference teaches that one should not look to what people say but at what they actually do. (Teece, Tr. 10366).

725. In simple terms, the theory of revealed preference is that you draw inferences about people's preferences by observing their choices. (Rapp, Tr. 9804). For example, if a person purchases $70 worth of groceries, the inference is that there is no combination of goods that could be purchased for $69 that is worth as much to that person as the bundle of goods actually purchased. (Rapp, Tr. 9804).

726. According to the theory of revealed preference, the choices of JEDEC and DRAM manufacturers to use the Rambus technologies when there were opportunities to use other technologies, shows that the Rambus technologies were superior to any alternatives in cost-performance terms. (Rapp, Tr. 9803-05).

727. JEDEC selected Rambus's technologies over all others in the real world. For SDRAM, JEDEC selected two Rambus technologies: programmable CAS latency and programmable burst length over all available alternatives. As Gordon Kelley testified, JEDEC considered the available technologies and selected what was considered to be the best. (Kelley, Tr. 2707-09).

728. In the process of developing the SDRAM standard, JEDEC considered and rejected many of the alternatives that Complaint Counsel now assert JEDEC could have

adopted in place of the Rambus technologies. Instead of Rambus's programmable CAS latency technology, JEDEC considered the alternatives of fixed latency and the use of fuses to set the latency. (Kellogg, Tr. 5136). With regard to Rambus's programmable burst length technology, JEDEC considered the alternatives of fixed burst length, the use of pins to set the burst length, and the use of fuses to set the burst length. (Kellogg, Tr. 5111-12).

729. For DDR, JEDEC selected four Rambus technologies over all others: programmable CAS latency, programmable burst length, dual-edge clocking, and on-chip PLL/DLL.

730. Just as with the SDRAM standard, for the DDR standard JEDEC considered and rejected several alternatives for Rambus's technologies that Complaint Counsel now assert JEDEC could have adopted in place of the Rambus technologies. In the place of Rambus's dual-edge clocking technology, JEDEC considered increasing the speed of the clock and interleaving banks on a module. (Kellogg, Tr. 5178). Instead of Rambus's on-chip PLL/DLL technology, JEDEC considered using verniers and relying only on data strobes. (Kellogg, Tr. 5156).

731. Instead of these alternatives, JEDEC selected Rambus's technologies. Applying the theory of revealed preference shows that none of these alternatives met JEDEC's needs as well as the Rambus technologies.

732. Complaint Counsel allege that JEDEC members were unaware at the time of the selection of the Rambus technologies for SDRAM and DDR that Rambus could possibly obtain patents that covered these technologies. This allegation is refuted by the evidence discussed above. But even if the allegation were correct, it would not undermine the application of the theory of revealed preference. JEDEC demonstrated that it would choose Rambus's technologies even if patented when it adopted the four Rambus technologies in the DDR2 standard even after Rambus began asserting its patents against DRAM manufacturers.

733. The development of the DDR2 standard began in April 1998. (Macri, Tr. 4598). From that date through June 2000, JEDEC specified many of the architectural attributes for DDR2. (Macri, Tr. 4598-99).

734. In late 1999, well prior to the close of the DDR2 specification period, Rambus began asserting its patents against JEDEC-compliant SDRAM and DDR products that incorporated the technologies at issue in this case. (Complaint, ¶ 92). This assertion of patent rights was widely publicized and well-known in the industry. (CX 1864 at 1; Macri, Tr. 4667-8). JEDEC's development of the DDR2 standard continued in the face of this knowledge.

735. From June 2000 to June 2001, even as more companies announced licenses for Rambus's technologies in SDRAM and DDR, JEDEC continued to flesh out the DDR2 specification. According to Mr. Macri, "Well, once you have kind of a -- you know, a list

of attributes, major attributes, to create a, you know, a real standard which is in the end a specification, you must add an infinite amount of detail to those attributes. So, this was – during June of 2000 to June of 2001, we were adding the meat, you know, the real description that an engineer would need to truly understand these -- these concepts." (Macri, Tr. 4598-99).

736. All of this JEDEC work from June 2000 to June 2001 was done in full view of Rambus's patents and in full view of Rambus's assertion – accepted by the over one-half of the industry that had licensed the technologies -- that SDRAM and DDR SDRAM devices infringed certain claims of those patents. **{IN CAMERA MATERIAL REDACTED}** (Macri, Tr. 4753-56 (*in camera*)).

737. Even after this fleshing out period described by Mr. Macri, JEDEC still made architectural changes to the DDR2 standard. From June 2001 through September 2001, JEDEC made further architectural changes to the DDR2 standard. (Macri, Tr. 4599). Again, these changes were made with knowledge of Rambus's patents and demands for royalties.

738. Even as of May 2003, the DDR2 specification had not been finalized. (Rhoden, Tr. 411-12).

739. Although JEDEC's design philosophy for DDR2 was to borrow as much as possible from other technologies (CX 140 at 3; Macri, Tr. 4709-10; RX 2234 at 3 (intent

of DDR2 design to borrow as many features as possible from other designs); Macri, Tr. 4693)), it is plain from the record that JEDEC did not have to use the Rambus technologies in DDR2 merely because they were used in SDRAM and DDR.

740. The April 1998 meeting minutes of the Future DRAM Task Group (the JEDEC subcommittee that developed DDR2) reveal that JEDEC considered entirely different architectures for the next generation DRAM, including architectures based on SLDRAM, Rambus and DDR, as well as packetized and non-packetized architectures. (CX 379A at 9). About one-third of the Task Group voted to base the next generation DRAM on the SLDRAM architecture and one-third voted to use a packetized architecture. (CX 379A at 9).

741. Similarly, a few months later, in September and October of 1998, Joe Macri, the Task Group Chair, presented four possible choices on how to proceed with DDR2 definition, from simply tightening the DDR specifications to a complete change of the logic interface, I/O, and core architecture. (RX 1306 at 9; Macri, Tr. 4621-22).

1. JEDEC Considered Foregoing Rambus's On-chip PLL/DLL Technology, But Chose to Adopt It Instead of Alternatives.

742. It is plain from the record that JEDEC explored alternatives to the use of Rambus technologies in DDR2. In late 1998, the Future DRAM Task Group wanted to explore eliminating both on-chip DLL and programmable burst length. (RX 1306 at 10; Macri, Tr. 4705). HP was assigned the first task, and IBM the second. (RX 1306 at 10; Macri, Tr. 4705).

743. The December 1998 Future DRAM Task Group Minutes record that HP proposed to eliminate the on-chip PLL in DDR2. (CX 137 at 3, 27). Those minutes also show that IBM proposed to use a vernier mechanism in place of on-chip PLL. (CX 137 at 4).

744. Despite this investigation, and despite Rambus's assertion of its patents in 1999, no alternative to on-chip PLL/DLL was adopted. (RX 1854 at 12-14 (preliminary DDR2 specification showing mode register and extended mode register using DLL Reset, and DLL Enable/Disable, "passed committee ballots and went to council at June 2001 meeting")).

745. IBM's Mark Kellogg testified that he would, today, support going to an alternative for on-chip DLL or PLL if there were "predatory IP," that is, intellectual property that is not licensed on reasonable and nondiscriminatory terms. Kellogg also testified that he has no knowledge of Rambus's royalty rates. (Kellogg, Tr. 5245-47).

2. JEDEC Selected Rambus's Technologies With Knowledge Of Rambus's Issued Patents.

746. Even knowing of Rambus's issued patents, JEDEC insisted on choosing Rambus's technologies. While JEDEC considered alternatives, it rejected them and decided to use the Rambus technologies.

747. Steve Polzin of AMD testifed that he had discussions with DRAM manufacturers in 2000 about alternatives for programmable CAS latency, programmable burst length and dual-edge clocking. (Polzin, Tr. 3988, 3996, 4044). At the time, the

DDR2 standard was still winding its way through JEDEC. (Polzin, Tr. 4044-45). Mr. Polzin understood at the time of these discussions that Rambus patents cover these technologies. (Polzin, Tr. 4047-48). The DDR2 standard, however, still specifies programmable CAS latency, programmable burst length, and dual-edge clocking. (Polzin, Tr. 4046-48).

748. Complaint Counsel's economic expert conceded that it is unlikely that JEDEC would discuss alternatives in the year 2000 unless at least some significant number of JEDEC members thought that the adoption of the alternatives was feasible at that point in time. (McAfee, Tr. 7571).

a. JEDEC Chose Rambus's Programmable CAS Latency Technology Despite Rambus's Issued Patents.

749. In March and April 2000, JEDEC considered alternatives for programmable CAS latency in SDRAM, DDR, and DDR2, including fixed latency, scaling latency with clock frequency, and using pins or additional commands in DDR2. (RX 1626 at 6). At the March 2000 meeting of JC42.3, Micron made a proposal entitled, "Simplifying Read Latency for DDRII." (CX 154A at 27; CX 2758 at 1; Lee, Tr. 6779-80). The proposal included a section on "Avoiding Programmable Latency in SDR/DDR SDRAMs." (CX 154A at 29) The presentation also included a proposed alternative for programmable CAS latency in DDR2. (CX 154A at 30-31; Lee, Tr. 6779-80).

750. In response to these proposals, Bob Fusco at Hitachi wrote, "For DDR-2, we have no legacy to live with, so I like the Micron proposal. For DDR-1 it's not too late for minor, carefully considered changes, so I'm open to either proposal." (RX 1626 at 4). This response demonstrates that JEDEC could have adopted alternatives if doing so were preferable.

751. Bill Hovis of IBM rejected the proposals regarding alternatives to programmable CAS latency because of cost concerns: "What are we really saving here? . . . Any cost savings has to be off-set with the additional component costs associated with adding new part numbers to satisfy CL=2 and CL=3 demands." (RX 1626 at 3). For DDR, Mr. Hovis still supported programmable CAS latency because "ultimately the flexibility of supporting multiple CAS latencies in one device can result in benefits to the customers that end up buying the memory." (RX 1626 at 3). Mr. Hovis similarly insisted that DDR2 retain programmable CAS latency, even though he was "not currently locked in": "On DDR II devices, I still want multiple CAS latencies supported for the same reasons. Obviously here, the situation with the system is that I am not currently locked in, so the ability to deal with an additional limitation is not as compelling . . . . However, the same arguments given above apply here. One part number is a benefit to system users, not a deficit. Unless the cost delta is significant (DRAM cost difference >2%, 5%???), I suggest we drop this as an issue." (RX 1626 at 3-4).

752. In July 2000, Micron made a presentation entitled, "Pin Selectable Posted CAS for DDR II (JEDEC- July 2000- Kevin Ryan)." (CX 2766 at 1). The proposal included using multiple pins "to select specific latency values," which had the trade off of "higher overhead for pins/traces, lower overhead associated with mode register." (CX 2766 at 3). The proposal also stated, "Latency select pin(s) on DRAM can be: hardwired (directly or through jumpers) to the appropriate voltage levels on the module PCB; brought out to pins on the module (requires new/additional latency selection pins on the DIMM); driven by modified SPD device." (CX 2766 at 4).

753. JEDEC ultimately opted to use Rambus's programmable CAS latency technology in DDR2. (Polzin, Tr. 4046; RX 1854 at 12-14 (preliminary DDR2 specification showing mode register and extended mode register using programmable CAS latency has passed committee ballots and went to the JEDEC council in June 2001)).

b. JEDEC Chose Rambus's Programmable Burst Length Technology Despite Rambus's Issued Patents.

754. JEDEC also decided to adopt Rambus's programmable burst length technology even though it was well aware that Rambus's patents covered the technology.

755. The preliminary DDR2 specification, published in July 2001, specified a fixed burst length of 4. (RX 1854 at 20; Macri, Tr. 4733-34; Krashinsky, Tr. 2834 (JEDEC based preliminary DDR2 specification on single (fixed) burst length)).

756. After that specification was published, both AMD and Intel proposed to

change the DDR2 specification to add programmable burst length. (Macri, Tr. 4675). At the September 2001 JC42.3 meeting, Intel proposed that DDR2 have burst length of 8 in addition to 4. (CX 174 at 7-8). At that same meeting, AMD also proposed the addition of a burst length of 8. (CX 174 at 8). According to Intel, adding a burst length of 8 would result in a "[p]otential improvement of 4-10% on high-bandwidth applications." (CX 174 at 37). The vote to ballot this proposal was unanimous. (CX 174 at 7-8).

757. Joe Macri, the Future DRAM Task Group chairman, admitted that he was aware when adding programmable burst length to DDR2 that Rambus would believe it infringes its patents. (Macri, Tr. 4679-83).

758. JEDEC adopted Rambus's programmable burst length technology in DDR2 despite complete awareness of Rambus's issued patents and demands for royalties. (Polzin, Tr. 4046-47). It is also clear that there was no technological force other than the superiority of Rambus's technology that required JEDEC to adopt Rambus's programmable burst length technology.

c. JEDEC Chose Rambus's Dual-Edge Clocking Technology Despite Rambus's Issued Patents.

759. JEDEC also tried to find viable alternatives to Rambus's dual-edge clocking technology. The reason the JEDEC committee was looking at alternative clocking schemes was to avoid Rambus patents. (Krashinsky, Tr. 2828). JEDEC failed to find an acceptable alternative and adopted Rambus's dual-edge clocking technology. (Polzin, Tr. 4047).

760. At the September 2000 JEDEC meeting, Micron made a proposal that DDR2 incorporate single data rate technology instead of dual-edge clocking. (CX 2769 at 13). Micron made this proposal to convince the committee that they had a better clocking scheme. (Macri, Tr. 4719-20).

761. In a November 2000 conference call, committee members discussed going to a single data rate ("SDR") technology. (Macri, Tr. 4639-42). The minutes of that meeting reflect a consensus to try to adopt SDR if it would work. Those minutes state, "HP – prefers SDR" and indicate that for IBM, "Single data rate clocks are acceptable provided that it works." (CX 426 at 2). The minutes also indicate that IBM agreed "with the need to avoid I.P. issues." (CX 426 at 3). The minutes continue, "Majority of companies prefers single data rate clocks but not all of them." (CX 426 at 3). "Discussion on single data rate clock vs. doble [sic] data rate clock . . . . Fundamentally question is that is single data rate clock possible? Micron believes that SDR has some advantages as it gets [rid] of duty cycle issue, it has old prior art, and the inherent bandwidth is better with write than with read. . . . In general, everyone agreed that SDR
clock is ok provided that it works." (CX 426 at 4). The overall consensus of the group was: "Single data rate clock is preferred provided we can make it work." (CX 426 at 4).

762. Mr. Macri, the chair of the Task Group, believed that everyone knew about Rambus IP at this time; therefore, there was no need to discuss the issue and the JEDEC

rules were satisfied even though he did not disclose his knowledge of Rambus patents. (Macri, Tr. 4639-42).

763. Despite the consensus to use SDR in place of dual-edge clocking "provided we can make it work," JEDEC incorporated dual-edge clocking into DDR2. (Polzin, Tr. 4047).

d. JEDEC Members' Views on the Likely Invalidity of Rambus's Patents Have Influenced Their Design Choices.

764. Complaint Counsel have contended that JEDEC chose the Rambus technologies in DDR2 because the industry was "locked in" to those technologies. As discussed above, however, JEDEC members knew of Rambus's patents while the DDR2 design phase was still ongoing, and they chose the Rambus technologies even though they acknowledged that "[f]or DDR-2, we have no legacy to live with" and are "not currently locked in . . . ." (RX 1626 at 3-4).

765. There is also substantial evidence that JEDEC members have based their adoption of the Rambus technologies in part on their view that any Rambus patents covering those technologies are, or are likely to be held to be, invalid because of prior art.

766. Mark Kellogg of IBM testified, for example, that he examined Rambus's patents in 2001. (Kellogg, Tr. 5301). With respect to the technologies in SDRAM and DDR, Mr. Kellogg testified that he believed that there was prior art to Rambus's patents, and he said that he had conveyed his opinion to other DRAM manufacturers. (Kellogg,

Tr. 5301-02). According to Mr. Kellogg, the DRAM manufacturers "were considering the fact that some of the Rambus patents might be overturned" when making decisions about whether to try to design around Rambus patents. (Kellogg, Tr. 5303-04).

767. JEDEC members have on many occasions expressed the view that any Rambus patents would be barred by prior art.

768. On the very first occasion that Rambus's potential patents were discussed at JEDEC, one or more members asserted that any such patents would likely not issue or be held invalid because of prior art.

769. At the May 1992 JEDEC meeting, NEC representative Howard Sussman stated that he had reviewed the claims in Rambus's PCT application and that, in his opinion, many of the 150 claims were barred by prior art. (RX 290 at 3; CX 673 at 1).

770. Notes taken at the May 1992 JC 42.3 meeting by IBM representative Mark Kellogg state: "NEC: Rambus International Patent 150 pages, Motorola patents/Rambus patent – suspect claims won't hold." (RX 290 at 3; Kellogg, Tr. 5319).

771. In an email recounting the meeting, Richard Crisp wrote, "Siemens expressed concern over potential Rambus Patents covering 2 bank designs. . . . In response to the patent issue, Sussman stated that our patent application is available from foreign patent offices, that he has a copy, and has noted many, many claims that we make that are anticipated by prior art. He also stated the Motorola patent predated ours (not the filing date!) and it too was anticipated by prior art." (RX 673 at 1). Mr. Crisp understood the

gist of Mr. Sussman's statement to be that "everything that he thought Rambus had invented, somebody else had invented first." (Crisp, Tr. 3492-93).

772. Siemens' JEDEC representative Willi Meyer prepared a trip report from the May 1992 JC 42.3 meeting that states, "Siemens and Philips concerned about patent situation with regard to Rambus and Motorola. No comments given. *Motorola patents have priority over Rambus'.* Rambus patents filed but pending." (RX 297 at 5) (emphasis added).

773. Mr. Meyer also testified that sixteen months later, at the September 1993 JC 42 meeting, there was an additional discussion of Rambus's patent applications in which someone said that the applications were "stuck in the patent office" and not proceeding right now." (CX 2057 12/13/00 Depo., 300:7-23). The speaker then referred to Rambus's patent applications as "a collection of prior art." (*Id.*).

774. In 1994, during a presentation to Samsung, Dr. Betty Prince summarized the sentiment in the industry that Rambus's patents were anticipated by prior art. Dr. Prince's presentation stated that "[m]any of the large systems houses believe that Rambus patents are challengeable by previous internal work and/or patents." (RX 153 at 10). This was public information that Dr. Prince had gathered for Samsung. (Prince, Tr. 9003). The presentation went on to state, "The early concern about the impact of the Rambus patents on the major systems houses seems to have diminished considerably." (RX 2153 at 10).

775. As Dr. Prince explained at trial, industry participants believed that Rambus's patents would be invalid due to prior art: "When Rambus first started talking about their product, they were very secretive and nobody really knew what they had. After it was clear what they had, then many of the big companies reviewed the patents that they had already – prior work that they had already had and there was discussion various places in the industry that much of this seemed to have prior art." (Prince, Tr. 9004). Dr. Prince testified that this information was from public sources. (Prince, Tr. 9004).

776. A November 6, 1995 Mitsubishi memorandum regarding "Request for Cray Patent Investigation as a Countermeasure for the Rambus Patent" states: "In response to the directive from the U Memory Department, we did a prior art search regarding the patents owned by Rambus, emphasizing the patents by Cray Corporation, and have found at least three issues that are potentially prior art for the Rambus patent." (RX 660A at 3).

777. Mitsubishi followed up with Cray Corporation, and received some additional reassurance. In a November 28, 1995 e-mail, Alan Grossmeier of Cray wrote to Kazutami Ariomoto in Mitsubishi's Memory Devices Department that, based on Cray work, "[w]e have not been concerned about infringing on Rambus patent since if dispute would occur we believe we have sufficient *prior art* to show." (RX 660 at 1).

778. A 1996 Micron email also shows that Micron believed Rambus's patents would be invalid due to prior art: "We have also been investigating the prior art related to

the area of high-speed DRAMs. From our research, we think many RAMBUS patents read on prior art or other patents." (RX 829 at 2).

779. It is clear that JEDEC engineers were confident of their ability to detect the existence of prior art in the DRAM arena. As Howard Sussman, who represented NEC and then Sanyo at JEDEC meetings, explained, although the engineers who attended JEDEC meetings were "not really the experts" on construing patent claims, "[f]or prior art, we most likely have knowledge." (Sussman, Tr. 1344).

780. It is also clear that in the face of explicit warnings that the Ramlink and SyncLink devices may violate Rambus's intellectual property rights, the DRAM manufacturers developing these devices continued to do so. For example, although there was no assurance that Ramlink did not infringe Rambus's patents, the Ramlink standard was issued by the IEEE. (Gustavson, Tr. 9300-01). The SyncLink work also proceeded, despite warnings by Rambus that the device might violate Rambus's patents. As Mr. Wiggers explained at trial, "the SyncLink work went forward, yes, based on the fact that we still felt we were in the public domain, that everything we had done was, you know, based on things that had been done in the public domain. . ." (Wiggers, Tr. 10604). Mr. Wiggers testified that he did not take Rambus's patent position very seriously. (Wiggers, Tr. 10604).

781. Also in 1997, Craig Hampel of Rambus was informed that Desi Rhoden, currently JEDEC's Chairman of the Board, "was commenting that it looked like there was

going to be prior art on Rambus, that would make our patents difficult to defend." (RX 908 at 1).

782. Mr. Rhoden testified that he recalls hearing discussions at dinner parties in the 1997 time period about there being prior art with respect to the Rambus patents. (Rhoden, Tr. 712).

783. Hans Wiggers of HP testified that if Richard Crisp had claimed at a JEDEC meeting that Rambus had invented dual-edge clocking, he would have said that Rambus could not patent that technology because it was a known technology. (Wiggers, Tr. 10588). This is understandable; Mr. Wiggers thought he had a patent on that technology. (Wiggers, Tr. 10607).

784. Given these views, it is not surprising that the DRAM manufacturers have continued to use Rambus's technologies despite knowing of Rambus's patents.

B. There Were No Viable Non-Infringing Alternatives To Rambus's Technologies.

785. Though JEDEC continued to adopt Rambus's technologies into new standards despite knowledge of Rambus's issued patents and demands for royalties, Complaint Counsel nonetheless contend that there were several alternatives that JEDEC would have adopted had Rambus made the additional disclosures Complaint Counsel allege should have been made. Complaint Counsel's technical expert, Professor Jacob, testified that several alternatives were "technically viable." Complaint Counsel's economic expert, Professor McAfee, testified that certain of these "technically viable"

alternatives were "commercially viable." The evidence shows, however, that each of the alternatives identified by Complaint Counsel's experts are either covered by Rambus's patents or are inferior to the Rambus technologies in cost-performance terms.

1. The Testimony Of Professor Jacob Regarding Allegedly Viable Alternatives Is Entitled To Little Weight.

a. Professor Jacob Does Not Have Sufficient Experience In Circuit Design.

786. Complaint Counsel's expert witness regarding viable alternatives, Professor Jacob, has never done DRAM circuit design. (Jacob, Tr. 5588). Indeed, Professor Jacob had never designed any circuits for computer chips (even apart from DRAMs) that were to be fabricated prior to 2002. (*Id.*). Aside from looking at some DRAM data sheets, Professor Jacob, who was a student at the time, had no particular DRAM-related experience in the mid-1990s. (Jacob, Tr. 11148).

787. By contrast, Respondent's technical experts have a wealth of relevant experience in the DRAM and semiconductor industries. Dr. Soderman was employed in the semiconductor industry for over 30 years during which time he designed DRAMs as well as various other types of integrated circuits. (Soderman, Tr. 9329-36).

788. Likewise, Mr. Geilhufe worked in the semiconductor industry for over 30 years. (Geilhufe, Tr. 9543-52). Mr. Geilhufe holds four patents for DRAM design, and managed Intel's international manufacturing operations which involved working closely with DRAM manufacturers such as Samsung. (Gelhufe, Tr. 9549-50, 9553).

789. Professor Jacob's relatively recent experience also pales beside that of Drs. Farmwald and Horowitz. When Drs. Farmwald and Horowitz made their inventions in the late 1980s and early 1990s, Dr. Farmwald had already founded a computer company, while Dr. Horowitz had been a professor of electrical engineering for a number of years. *See* Findings ¶¶ 27, 43). Professor Jacob did not obtain his graduate degree and begin to teach electrical engineering until 1997. (Jacob, Tr. 5357).

b. Professor Jacob's Analysis of His Proposed Alternatives Was Inadequate.

790. By contrast to his publications comparing certain DRAM architectures, in which Professor Jacob tried to model their performance as precisely as possible using software simulation, Professor Jacob did no such software simulation with respect to the alternatives that he proposed to Rambus's technology. (Jacob, Tr. 5589).

791. With the exception of three of his alternatives (using a burst terminate command, increasing the number of pins on the DRAM, and increasing the number of pins on the module), Professor Jacob did no simulation or modeling of any kind to try to assess the alternative's performance. (Jacob, Tr. 5590-91).

792. Professor Jacob's proposed alternatives were not sufficiently detailed to enable an actual circuit design. (Geilhufe, Tr. 9673).

793. Professor Jacob did not do any investigation to determine whether any of his proposed alternatives was covered by patents owned by Rambus or others. (Jacob, Tr. 5601).

2. To Understand Whether A Particular Alternative Is Viable, The Relevant Cost Factors Must Be Considered.

794. The primary cost factors to be considered in evaluating an alternative DRAM technology are costs relating to: (1) process and storage cell/array; (2) product design; (3) wafer plant; (4) photo tooling; (5) wafer sort; (6) good die yield; (7) packaging; (8) final test and good unit yield; (9) inventory; (10) qualification; and (11) board complexity. (Geilhufe, Tr. 9564-74).

795. The largest part of a DRAM, approximately 90 percent of the active area, consists of the memory array, that is the memory cells and related circuitry. (Geilhufe, Tr. 9560). The remaining 10 percent consists of peripheral circuitry. (*Id.*). Circuitry for implementing the four features at issue here – programmable CAS latency, programmable burst length, dual edge clocking, and on-chip DLL – would be found in the peripheral circuitry. (Geilhufe, Tr. 9559).

796. The vast majority of DRAM development costs is spent on the memory array portion of the DRAM, including the manufacturing process and equipment development. (Geilhufe, Tr. 9560-61). Development costs for the peripheral circuitry is much lower. (*Id.*).

797. The "process and storage cell/array" cost factor relates to the development of processes to reduce the size of memory cells or to increase the density of the memory array. (Geilhufe, Tr. 9565). This is a fixed, or one-time, cost. (Geilhufe, Tr. 9565-66).

798. The "product design" cost factor relates to the manpower, computer time,

and simulations to create the design for a particular alternative. (Geilhufe, Tr. 9566). This is a fixed cost. (*Id.*).

799. The "wafer plant" cost factor relates to new equipment in the wafer factory that may be required to support a particular alternative. (Geilhufe, Tr. 9566-67). This is a fixed cost. (Geilhufe, Tr. 9567).

800. The "photo tooling" cost factor relates to the "reticles," also known as "masks," required to process a silicon wafer. (Geilhufe, Tr. 9567). This is a fixed cost. (*Id.*).

801. The "wafer sort" cost factor relates to the electrical test operation that separates the good from the bad die on a wafer. (Geilhufe, Tr. 9568). This is a variable cost, i.e., one that increases with the number of units produced. (*Id.*).

802. The "good die yield" cost factor relates to the percentage of total die that are good die. (Geilhufe, Tr. 9569). This is a variable cost.

803. The "packaging" cost factor relates to the packages that potentially good die are placed in so that they can be attached to a circuit board. (Geilhufe, Tr. 9569). This is a variable cost. (Geilhufe, Tr. 9570).

804. The "final test and good unit yield" cost factor relates to post-packaging testing that results in some further units that are rejected. (Geilhufe, Tr. 9570). This is a variable cost. (*Id.*).

805. The "inventory" cost factor has two elements: First, the "work-in-process"

inventory in the fabrication and assembly plants relating to the time period, approximately six to eight weeks, required to complete all of the processing steps to create a finished wafer. Second, the "finished product" inventory, at the DRAM manufacturer, distribution channel and user, after a product passes final test and is determined to be a good unit (Geilhufe, Tr. 9571). Inventory is a variable cost. (*Id.*).

806. The "qualification" cost factor relates to the reliability and specification qualification that is done for a particular product. (Geilhufe, Tr. 9572). This is a fixed cost. (Geilhufe Tr. 9572-73).

807. The "board complexity" cost factor relates to the motherboard and the possibility that a change to the DRAM may require a larger board area or more traces or other circuitry on the board. (Geilhufe, Tr. 9573). This is a variable cost. (*Id.*).

808. In estimating the costs of various alternative technologies proposed by Professor Jacob, Respondent's expert, Michael Geilhufe, tried to be conservative, that is, to err on the low end with respect to cost increases. (Geilhufe, Tr. 9746).

3. There Were No Viable Non-Infringing Alternatives To The Rambus Technologies Adopted In The SDRAM.

a. Programmable Latency.

809. Complaint Counsel have suggested, through their technical expert, Professor Jacob, the following possible alternatives to programmable CAS latency in SDRAMs:

(1) Use fixed CAS latency parts;

(2) Program CAS latency by blowing fuses on the DRAM;

(3) Scale CAS latency with clock frequency;

(4) Use dedicated pins to transmit latency information from the controller to the DRAM;

(5) Explicitly identify CAS latency in the read command;

(6) Stay with an asynchronous-style DRAM.

(Jacob, Tr. 5370-96).

(1) <u>The Use of Fixed CAS Latency Parts Was Not a Viable Alternative</u>.

810. One of the alternatives proposed by Professor Jacob for programmable CAS latency was to fix the CAS latency at the design stage, the manufacturing stage, or the packaging stage. (Jacob, Tr. 5371). Fixing CAS latency at the design stage would result in a single part with only one CAS latency. (Jacob, Tr. 5373). Fixing CAS latency at the processing stage would involve a "metal mask option" that would fix the CAS latency to one value or another. (Jacob, Tr. 5373-75). Fixing CAS latency during packaging would require a multiplexer that would be hardwired to either power or ground during the packaging process to select one of two latency values. (Jacob, Tr. 5375-76).

811. Complaint Counsel did not meet their burden of showing that the use of fixed CAS latency parts was a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs.

812. To the contrary, the evidence in the record shows that the use of fixed CAS latency parts was not a viable alternative to programmable CAS latency in SDRAMs and

DDR SDRAMs because multiple fixed CAS latency parts would have been required, leading to higher costs and logistical difficulties for DRAM manufacturers and users.

813. Multiple CAS latency values are required for SDRAMs because users of DRAMs would prefer to buy parts that they can insert in a variety of systems with different bus speeds. (RX 1626 at 3-4; Soderman, Tr. 9346-47). The appropriate CAS latency for a part will depend on the bus speed and the access time of the DRAM. (Soderman, Tr. 9347-48). Therefore, using fixed latency parts would require multiple fixed latency parts, as opposed to a single, programmable latency part. (*Id*.).

814. Mark Kellogg of IBM testified that, in the 1992 time frame, "we weren't convinced that we knew the right latency and we did expect that the DRAM frequency would go up over time -- that we knew the correct latency if we were to select one and we expected that the DRAM frequency would increase over time, which meant we might wish to change the CAS latency." (Kellogg, Tr. 5139).

815. The mode register in SDRAMs and DDR SDRAMs reserves three bits for CAS latency, allowing for up to eight different CAS latency values. (CX 234 at 150).

816. Release 4 of JEDEC Standard 21-C (November 1993), which contains the first published SDRAM standard, specified three required CAS latency values (1, 2, and 3) and one optional CAS latency value (4). (JX 56 at 114; Lee, Tr. 11003-04). Release 9 of JEDEC Standard 21-C (August 1999), which contains the first published DDR SDRAM standard, specified two required CAS latency values for SDRAMs (2 and 3) and one

optional value (4); it also specified two required CAS latency values for DDR SDRAMs (2 and 2.5) and three optional values (1.5, 3, and 3.5). (CX 234 at 150; Lee, Tr. 11068-72).

817. Although not all of the eight possible values of CAS latency are used in SDRAMs and DDR SDRAMs, the other possibilities were reserved to preserve flexibility for future additions. (Lee, Tr. 11072-73).

818. Desi Rhoden gave a presentation on "Future SDRAM" at the March 1996 meeting of the JEDEC 42.3 subcommittee. (JX 31 at 64; Rhoden, Tr. 489-90). The presentation indicates that CAS latencies of 2, 3, 4, 5 and 6 would be required for different generations of SDRAMs. (JX 31 at 64; Rhoden, Tr. 490-91).

819. JEDEC's DDR2 SDRAM standard intends to expand the use of programmable latency. (Soderman, Tr. 9351-53). Preliminary DDR2 SDRAM data sheets from both Hynix and Samsung indicate that DDR2 SDRAMs will continue to have three bits in the mode register reserved for CAS latency, allowing for up to eight different CAS latency values. (RX 2099-14 at 21; RX 2099-39 at 20; Soderman, Tr. 9351). Hynix's part provides three different CAS latency values (3, 4, 5), while Samsung's part provides four different CAS latency values (3, 4, 5 and 6). (*Id.*). DDR2 SDRAMs also reserve three bits in an "extended mode register" for "additive latency," allowing for up to eight different additive latency values. (RX 2099-14 at 24; RX 2099-39 at 22; Soderman, Tr. 9351-53; Lee, Tr. 11068). Hynix's part provides six different additive latency values (0, 1, 2, 3, 4,

and 5), while Samsung's part provides five different additive latency values (0, 1, 2, 3 and 4). (*Id.*). The "read latency" in DDR2 SDRAMs (that is, the number of clock cycles from receipt of a CAS command until data is output onto the bus) is the sum of the CAS latency and the additive latency. (RX 2099-14 at 32; RX 2099-39 at 37).

820. In 1993, Micron's first SDRAM design allowed for four different CAS latencies (1, 2, 3, and 4). (Lee, Tr. 11063-64).

821. Micron currently sells an SDRAM for the graphics market allowing for three different CAS latencies (1, 2, and 3). (Lee, Tr. 11064-67).

822. The total unit cost for a mature product built by a first tier DRAM manufacturer in the mid-1990s was approximately $2.00. (Geilhufe, Tr. 9564). Multiple fixed latency parts would have been an expensive alternative, for several reasons. (Soderman, Tr. 9348-49).

823. First, manufacturing multiple fixed latency parts would decrease a DRAM manufacturer's yield due to speed distribution. (Soderman, Tr. 9348; Geilhufe, Tr. 9577). DRAMs cannot be accurately tested for speed until after packaging; fixing the CAS latency prior to that time would result in some parts that are not capable of performing at the CAS latency that has been fixed and, therefore, would not be usable. (Soderman, Tr. 9347-49; Geilhufe, Tr. 9577-8). If CAS latency were programmable, those slower parts would be usable at a higher CAS latency value. (*Id.*).

824. Second, fixing CAS latency would result in DRAM manufacturers losing some of the price premium associated with their fastest (i.e. lowest CAS latency) parts which can sell for 50 percent or more over their standard parts. (Soderman, Tr. 9348-50; Lee, Tr. 11074-75). This is again because the latency would be fixed prior to accurate speed testing and, consequently, some parts that would be capable of faster performance (i.e. operating at a low CAS latency) will be set to a CAS latency higher than necessary. (*Id*.).

825. Steve Polzin of AMD testified that "Fixed CAS latency would have been pretty onerous for the DRAM manufacturers." (Polzin, Tr. 3992). Mr. Polzin explained:

> Probably [fixed CAS latency] had -- would have a significant cost impact for the DRAM manufacturers. One of the advantages of programmable CAS latency is that DRAM manufacturers can bin their devices. They can have fast devices with a short CAS latency and sell them for more money, and parts that were perhaps yielding slower, they could be programmed with a longer CAS latency and sold for less cost.

(*Id*.).

826. Joe Macri of ATI testified that **{IN CAMERA MATERIAL REDACTED}**

(Macri, Tr. 4762-63, **in camera**).

827. Third, there would have been an increase in design, photo tooling and qualification costs because multiple products would have had to be designed and manufactured, rather than just one. (Geilhufe, Tr. 9679, 9682-83, 9690).

828. Some design effort would have been required for each different CAS latency; one mask would have had to be changed for each different CAS latency; and each different CAS latency part would have had to be qualified before it could be sold. (Geilhufe, Tr. 9575-76, 9578-79).

829. Fourth, multiple fixed latency parts in place of a single programmable latency part would result in substantial inventory costs. (Soderman, Tr. 9349-50).

830. Gordon Kelley of IBM testified about the benefits of programmability as follows: "One of the advantages of that is that that drives low cost. The producer does not have to maintain multiple part numbers. One part number fits many applications. That's one of the drivers to low cost." (Kelley, Tr. 2550-51).

831. When first developing the Rambus technology, Drs. Farmwald and Horowitz considered having a fixed latency. (Horowitz, Tr. 8532). Dr. Horowitz learned from an early visit to a DRAM manufacturer the importance of having a single, as opposed to multiple, parts. At that time, there were two different packages for DRAMs, and the DRAM manufacturer was making a single die that could fit into either package even

though this entailed 10 percent additional die area. (Horowitz, Tr. 8532-33). Dr. Horowitz's understanding at the time was that the reason for making a single part despite the die size penalty was that inventory costs from having two different designs during the manufacturing process would be too expensive. (Horowitz, Tr. 8533-34).

832. Multiple fixed latency parts would also be inferior from the user's standpoint. Because the part could no longer be programmed to operate in various systems, a user would have to pay attention to the part's detailed specifications to determine whether it would work in its system. (Soderman, Tr. 9350-51).

833. In an April 11, 2000 e-mail responding to a proposal to fix CAS latency in DDR2, Bill Hovis of IBM rejected the idea both because of cost concerns and because of the benefits to DRAM users from programmable CAS latency. With respect to cost concerns, Mr. Hovis stated: "What are we really saving here? . . . . Any cost savings has to be off-set with the additional component costs associated with adding new part numbers to satisfy CL=2 and CL=3 demands." (RX 1626 at 3). With respect to user benefits from programmable CAS latency, Mr. Hovis stated that "ultimately the flexibility of supporting multiple CAS latencies in one device can result in benefits to the customers that end up buying the memory." (RX 1626 at 3).

834. Using fixed latency would not allow for the elimination of the mode register in SDRAMs and DDR SDRAMs because the mode register is used for purposes other than programming CAS latency. In the JEDEC SDRAM standard, the mode register is used for

storing CAS latency, burst length and burst type. (CX 234 at 150). Certain SDRAMs being manufactured use the mode register for additional purposes as well, such as for programming operating mode and write burst mode. (RX 2100-13 at 3). The DDR SDRAM standard adds an extended mode register used to enable or disable a DLL. (CX 234 at 176). The DDR2 SDRAM standard expands the use of the mode register even further, with the mode register being used to program burst length, burst type, CAS latency, test mode, DLL reset, and tWR, and the extended mode register being used to program DLL enable, output driver impedance control, RTT, additive latency, OCD, /DQS enable and RDQS enable. (RX 2099-14 at 21, 24; RX 2099-39 at 20, 22).

835. Although there would have been a decrease in testing costs because each part would have had to be tested for a single CAS latency, rather than for multiple CAS latencies (Geilhufe, Tr. 9576), this cost saving would have been far outweighed by the cost increases due to other factors.

836. The fixed CAS latency alternative would have resulted in the following approximate net costs compared to the cost of SDRAM in the mid-1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: $100,000 increase in product design costs per latency; $50,000 increase in photo tooling costs per latency; one cent decrease per unit in testing costs at wafer sort; three cents per unit cost increase due to reduced good die yield; two cents per unit increase

in inventory costs; and $250,000 increase in qualification costs per latency. (Geilhufe, Tr. 9562-64, 9575-79).

837. The net increase in variable costs for the fixed CAS latency alternative is, therefore, approximately 4 cents per unit. The total cost increase is approximately 6 cents per unit, calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9579).

838. The additional inventory cost estimate is based on three different fixed latency parts being manufactured, the number of required CAS latencies in the original SDRAM standard, instead of a single programmable latency part. (Geilhufe, Tr. 9578; JX 56 at 114). The estimate of three parts is conservative given the number of CAS latencies in use and projected to be in use in the future in SDRAMs, DDR SDRAMs and DDR2 SDRAMs. *See* Findings ¶¶ 815-821.

839. The estimate for increased inventory costs is very conservative, because inventory costs due to multiple products can be much larger. For example, in 1989, Apple Computer reported $27 million quarterly loss attributed entirely to purchasing a DRAM part that they could no longer use in their systems. (Geilhufe, Tr. 9587). This amounted to a loss of about five to six dollars per unit. (Geilhufe, Tr. 9588).

(2) Programming CAS Latency with Fuses Was Not a Viable Alternative.

840. Professor Jacob's proposed alternative of programming CAS latency with fuses is similar to his fixed CAS latency alternative because, once the fuse is blown, the part has a fixed CAS latency. (Jacob, Tr. 5378-79).

841. Complaint Counsel did not meet their burden of showing that programming CAS latency with fuses was a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs.

842. To the contrary, the evidence in the record shows that programming CAS latency with fuses was not a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs because, as with the fixed CAS latency alternative, multiple parts with different CAS latencies would have been required, leading to higher costs and logistical difficulties for DRAM manufacturers and users.

843. Fuses can be blown by lasers or electrically. (Jacob, Tr. 5380).

844. Laser-blown fuses are more reliable than electrically-blown fuses. (Soderman, Tr. 9356-57). Certain products using electrically blown fuses were discontinued at Intel for reliability reasons. (Geilhufe, Tr. 9581-82).

845. In the 1995 time frame, the dominant fuse technology used by major DRAM manufacturers was laser fuse technology. (Geilhufe, Tr. 9581-82). There are DRAM manufacturers who do not have the technology to blow fuses electrically and did not have such technology in the 1995-2000 time frame. (Jacob, Tr. 5596; Geilhufe, Tr. 9740-41).

846. Fixing the CAS latency with laser-blown fuses prior to packaging would lead to the same logistical difficulties as Professor Jacob's fixed CAS latency alternative. (Soderman, Tr. 9354).

847. Another disadvantage of using fuses is that the manufacturer would have to blow the fuses after receiving orders for parts, leading to a "time lag from request to delivery of parts." (Kellogg, Tr. 5131).

848. Laser blown fuses could not be blown by OEMs (original equipment manufacturers) because they cannot be blown after packaging. (Jacob, Tr. 5378-80; Soderman, Tr. 9354-56). Electrically-blown fuses can be blown after packaging, but they still could not be blown by OEMs because the part must be tested after the fuse is blown to make sure it is operating correctly. (Soderman, Tr. 9517). OEMs do not have the capability to perform such testing. (Jacob, Tr. 5597-98; Soderman, Tr. 9354-56).

849. Programming CAS latency with fuses would have resulted in increased costs.

850. There would have been an increase in design costs due to the design effort to provide the fuses required. (Geilhufe, Tr. 9575, 9584-85).

851. There would have been an increase in testing costs due to the time required to blow a fuse and perform certain additional steps. (Geilhufe, Tr. 9585).

852. There would have been reduced good die yield, inventory, and qualification costs of the same magnitude as the corresponding increases for the fixed CAS latency

alternative because, once the fuse is blown, the part is a fixed latency part. (Geilhufe, Tr. 9585-89).

853. Programming CAS latency by blowing fuses would have resulted in the following approximate net costs compared to SDRAM in the mid-1990s, assuming a first-tier DRAM manufacturer using existing laser fuse technology and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: $100,000 increase in product design costs per latency; one cent increase per unit in testing costs at wafer sort; three cents per unit cost increase due to reduced good die yield; two cents per unit increase in inventory costs; and $250,000 increase in qualification costs per latency. (Geilhufe, Tr. 9562-64, 9584-86, 9589).

854. The net increase in variable costs for the alternative of programming CAS latency by blowing fuses is, therefore, approximately 6 cents per unit. The total cost increase is approximately 7 cents per unit, calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9589).

855. If the DRAM manufacturer did not have antifuse or electrically blown fuse technology available and wished to use that technology, adding it to the manufacturing process would entail several million dollars in additional development costs. (Geilhufe, Tr. 9583-84).

(3) Scaling CAS Latency with Clock Frequency Was Not a Viable Alternative.

856. Professor Jacob's proposed alternative of scaling CAS latency with clock frequency involves having the DRAM either being informed of the frequency by the memory controller or using some sort of internal circuitry to sense the frequency. The DRAM would then calculate the appropriate CAS latency to use based upon its own inherent latency. (Jacob, Tr. 5383).

857. Complaint Counsel did not meet their burden of showing that scaling CAS latency with a clock frequency was a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs.

858. To the contrary, the evidence in the record shows that scaling CAS latency with clock frequency was not a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs. First, implementation of scaling CAS latency with clock frequency would have resulted in higher costs. Second, scaling CAS latency with clock frequency is not an "alternative" at all because it would still infringe Rambus's patents.

859. Professor McAfee did not testify that this alternative was commercially viable. (McAfee, Tr. 7363).

860. Having the controller send the bus speed information to the DRAM would require extra pins and circuitry on the controller and, potentially, extra pins on the DRAM, adding manufacturing expense. (Soderman, Tr. 9359-60).

861. Having the DRAM sense the bus speed would require complex and costly circuitry on the DRAM. (Soderman, Tr. 9358).

862. In any event, scaling CAS latency with clock frequency is not an alternative to using a register to store a latency value because the latency value would still have to be stored in a register, violating Rambus's patents to the same extent as current SDRAMs do. (RX 1626 at 2; Soderman, Tr. 9359).

863. For example, this alternative would be covered by claim 1 of U.S. Patent 5,953,263, assigned to Rambus, which claims:

> "A synchronous semiconductor memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises:
> a programmable register to store a value which is representative of a delay time after which the memory device responds to a read request."

(CX 1517 at 29).

864. A claim covers a device if each and every claim element or "limitation" is found in that device. (Nusbaum, Tr. 1565-66). SDRAMs are synchronous memory devices that have memory sections containing a plurality of memory cells. (Rhoden, Tr. 359-60, 369-70). Moreover, "CAS latency" in SDRAMs refers to the delay time after which the SDRAM responds to a read request. (Rhoden, Tr. 382). As noted above, if CAS latency is scaled with clock frequency, CAS latency information would still have to be stored in a programmable register. Thus, each and every element of claim 1 of the '263

patent would be found in SDRAMs that implemented scaling CAS latency with clock frequency.

865. Scaling CAS latency with clock frequency was actually proposed by Micron as an alternative to programmable CAS latency for DDR2. At the March 2000 meeting of the JEDEC JC-42.3 subcommittee, Micron made a first showing entitled "Simplifying Read Latency for DDRII." (CX 154A at 9, 25-32). In its presentation, Micron noted that one approach would be to "offer devices with a fixed read latency." (CX 154A at 26). Under this approach, "[v]endors can offer different speed devices, each with a different fixed latency," but there would be the "[d]isadvantage" that "[u]sers may need to order different parts to cover different applications." (*Id*.).

866. Micron went on to present a second approach: "offer devices with a programmable operating frequency; each operating frequency has a fixed read latency associated with it." (CX 154A at 27). In other words, Micron proposed to scale CAS latency with clock frequency.

867. In an e-mail dated April 13, 2000 from Mark Kellogg of IBM to Art Kilmer of IBM, Mr. Kellogg discussed the proposals made by Micron at the March 2000 JEDEC meeting in the context of "the Rambus patents." (RX 1626 at 2). Mr. Kellogg noted that "[i]n the last JEDEC meeting, the option of a single latency device was pooh-poohed." (*Id*.). Mr. Kellogg went on to discuss Micron's alternative proposal of scaling CAS latency with clock frequency. Mr. Kellogg stated:

> "[T]he alternate proposal from Micron (programming the frequency range instead of CAS Latency) was better received. The problem with the latter proposal (in my mind), was that nothing changed except the name assigned to the command register bits (originally defined as CAS Latency, now to be defined as frequency range or something similar). As such, I felt they were walking a fine line and that this change would not hold up in court as being anything other than an attempt to circumvent possible patent infringement via a term redefinition."

(*Id*.).

(4) Using Dedicated Pins to Identify the Latency Was Not a Viable Alternative.

868. Professor Jacob's proposed alternative of using an existing or dedicated pin to identify the latency involves a pin on the DRAM that would select one CAS latency if it received a high voltage and a different CAS latency if it received a low voltage. (Jacob, Tr. 5386-87).

869. Complaint Counsel did not meet their burden of showing that using dedicated pins on the DRAM to select CAS latency was a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs.

870. To the contrary, the evidence in the record shows that using dedicated pins on the DRAM to select CAS latency was not a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs, because it would be costlier and less reliable.

871. This alternative would require additional wiring in the DIMM and from the DIMM to the memory controller. These additional wires can have a "noise glitch" – that is, the signals could be perturbed by adjacent signals – that would upset the CAS latency

value and lead to improper operation of the DRAM. (Soderman, Tr. 9361-62).

872. Certain configurations of SDRAMs had no "no-connect" pins. (CX 234 at 84; Geilhufe, Tr. 9741-42). Certain others had only a single "no-connect" pin. (RX 2100-13 at 1; Polzin, Tr. 4026-28).

873. Moreover, pins designated as "no connect" are not necessarily available for other uses because they may be used in testing. (Soderman, Tr. 9463-65).

874. Pins designated as "no connect" also may be unavailable because they are reserved for uses in other configurations. For example, if a manufacturer used the same mask for x4, x8 and x16 configurations, and if a pin designated "no connect" in the x4 and x8 configurations was used as a data pin in the x16 configuration, that pin could not be used for other purposes in the x4 and x8 configurations; in other words, the pin would need to remain a "no connect" pin in the x4 and x8 configurations. (Lee, Tr. 11084-87).

875. Pins designated as "no connect" may also be valuable for use in future, higher density generations of the product. As Gordon Kelley of IBM testified, using up a pin is not something that was done "easily, because once you use that pin up for a function, you don't have it available to you in the future for generation advance. As the memory densities increase, we need pins for more addressing of more address locations and those pins are very valuable for that feature, so this would have limited the number of generations of DRAM design that we could have used if we were to use up this pin." (Kelly, Tr. 2552-53).

876. To achieve the same level of flexibility as SDRAMs and DDR SDRAMs which have three bits in the mode register for storing a CAS latency value, a manufacturer would have to add three pins to a DRAM with no pins available. (Soderman, Tr. 9362; Geilhufe, Tr. 9589-90). Moreover, since the packages in use in the 1990s were all rectangular and required pins to be added in multiples of two, four pins would have to be added. (Soderman, Tr. 9362-63; Geilhufe, Tr. 9590; Lee, Tr. 11082).

877. In its license negotiations with Rambus in 1994, Samsung was motivated to seek a non-assertion provision for non-Rambus-compatible uses of Rambus's inventions because of the on-chip DLL shown in Rambus's PCT application. (CX 2078, Karp Micron Depo. at 107-08, 119-20).

878. The number of pins required could not be reduced by having more than two voltage levels per pin. Although Professor Jacob has suggested that this could be done, he has never designed a circuit that would detect more than two voltage levels at high frequency. (Jacob, Tr. 11126). No SDRAM or DDR SDRAM parts support more than two voltage levels per pin in normal operation. (Jacob, Tr. 11125-26). Having more than two voltage levels on a pin would require sophisticated circuitry that would be easily perturbed by noise. (Soderman, Tr. 9363-64).

879. The first Rambus DRAM, the 4.5 megabit part built by Toshiba in the early 1990s, had a pin with three voltage levels. (Horowitz, Tr. 8549). Rambus did not want to use an extra pin for entering test mode and, instead, created an extra voltage level on one

of the existing pins for that purpose. (*Id.*). Although Rambus, believed that the part had been built and designed with enough separation between the voltage levels to prevent confusion, in fact the part sometimes failed because it entered test mode accidentally. (Horowitz, Tr. 8550-51). Rambus never used a pin with more than two voltage levels on subsequent Rambus DRAMs. (Horowitz, Tr. 8551).

880. Assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement, programming CAS latency by using dedicated pins would have resulted in approximately 4 cents in increased packaging costs per unit, compared to the cost of SDRAMs in the mid-1990s, because of the need for additional four pins. (Geilhufe, Tr. 9562-64, 9589-91). This 4-cent increase is a variable cost.

881. The four cent increase cost estimate for this alternative is very conservative. First, standard packages generally add more than four pins – for example, the JEDEC SDRAM standards move from a 44-pin package to a 54-pin package, adding 10 pins, and then to a 66-pin package, adding 12 pins. (Geilhufe, Tr. 9590; CX 234 at 99-106). Thus, if there were not enough pins available on a certain standard package, one might have to move up to the next standard package, adding many more than the bare minimum of four pins.

882. Second, in addition to the four pins on the DRAM, more pins would also be required on the memory controller; however, every pin on controllers is fully utilized, so

pins would have to be added there. (Soderman, Tr. 9363; Geilhufe, Tr. 9591).

883. Third, both a new, more expensive connector may be required to connect the DIMM to the motherboard, and more lines on the bus. (Geilhufe, Tr. 9590-91).

(5) Identifying CAS Latency in the Read Command Was Not a Viable Alternative.

884. Professor Jacob's proposed alternative of identifying CAS latency in the read command would involve a different command sent from the controller to the DRAM for each desired CAS latency. (Jacob, Tr. 5389).

885. Complaint Counsel did not meet their burden of showing that identifying CAS latency in the read command was a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs.

886. To the contrary, the evidence in the record shows that, as with the alternative of scaling CAS latency with clock frequency, this is not really an alternative because it would still require storing latency information in a programmable register like the mode register in SDRAMs. (Soderman, Tr. 9365).

887. For example, this alternative would be covered by claim 1 of U.S. Patent 5,953,263, assigned to Rambus, which claims:

> A synchronous semiconductor memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises:
> a programmable register to store a value which is representative of a delay time after which the memory device responds to a read request.

(CX 1517 at 29).

888. A claim covers a device if each and every claim element or "limitation" is found in that device. (Nusbaum, Tr. 1565-66). SDRAMs are synchronous memory devices that have memory sections containing a plurality of memory cells. (Rhoden, Tr. 359-60, 369-70). Moreover, "CAS latency" in SDRAMs refers to the delay time after which the SDRAM responds to a read request. (Rhoden, Tr. 382). As noted above, if CAS latency is identified in the read command, CAS latency information would still have to be stored in a programmable register. Thus, each and every element of claim 1 of the '263 patent would be found in SDRAMs that implemented identifying CAS latency in the read command.

889. Professor Jacob testified that this alternative would not require a register because a "latch" could be used to store the latency information instead. (Jacob, Tr. 5393). This distinction is of no consequence because a register is a generic class of storage (Soderman, Tr. 9450-51), and one type of register is a latch. (*Id.*; Horowitz, Tr. 8508-09).

890. Professor Jacob concedes that "a register might be built out of latches." (Jacob, Tr. 5393). He testified that: "A latch is a specific implementation. A register implies how a piece of storage is being used." (*Id.*). In this case, if latches were used to store latency information, they would be used for precisely the same purpose as the mode register in an SDRAM.

891. Identifying CAS latency in the command would have the negative side effect

of limiting the simultaneous issuing of independent commands that is possible with the current command set. (Jacob, Tr. 5599).

892. This alternative may also be covered by U.S. Patent No. 5,835,956, which is assigned to Samsung and was not considered by Professor Jacob. (RX 1308; Jacob, Tr. 5599-601). Claim 1 of that patent claims a synchronous memory device that is capable of receiving latency mode information and selecting one of a plurality of latency modes in response to the information. (RX 1308 at 90).

(6) Staying with Asynchronous Technology Was Not a Viable Alternative.

893. Complaint Counsel did not meet their burden of showing that staying with asynchronous technology was a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs.

894. To the contrary, the evidence in the record shows that staying with asynchronous technology was not a viable alternative to programmable CAS latency in SDRAMs and DDR SDRAMs because asynchronous technology was not capable of achieving the performance necessary for high speed operation.

895. SDRAM, SLDRAM and RDRAM are all synchronous designs. (Jacob, Tr. 5601-02).

896. Despite the success of SDRAM, a substantial amount of work on asynchronous technology has continued during the last decade at both the academic and commercial levels. (Jacob, Tr. 5602; Horowitz, Tr. 8560-61).

897. When Dr. Horowitz began working on what was to become RDRAM, he had substantial experience in asynchronous designs. Some of Dr. Horowitz's Ph.D. students had done their dissertations in asynchronous design, and Dr. Horowitz had himself done studies comparing asynchronous to synchronous designs. (Horowitz, Tr. 8559).

898. Dr. Horowitz decided that a synchronous design would be necessary for RDRAM because he did not believe that one could build a very high-performance asynchronous interface. (Horowitz, Tr. 8498). As a circuit designer, Dr. Horowitz realized that when a signal passes through a block of circuitry, the amount by which it is delayed is subject to some uncertainty because of fluctuations in certain parameters such as temperature and voltage. (Horowitz, Tr. 8499-500). In the absence of a timing reference, like the clock in a synchronous system, as the signal continues to travel through more and more blocks, the amount of uncertainty will grow so that it will not be possible to predict with any accuracy when data will arrive. (*Id.*). For high performance, the amount of uncertainty must be kept to a small, predictable amount; this requires a synchronous system. (Horowitz, Tr. 8501-02).

899. Asynchronous memories are very dependent on loading on the bus – that is, how many other chips are on the bus. In a general purpose environment, the loading of the bus can vary; consequently, asynchronous memories do not perform well in a bus environment at high frequencies. (Soderman, Tr. 9366).

900. It was generally understood in the 1990s that asynchronous memories were not capable of reaching the speeds that would be required for future DRAMs. For example, an article by a Fujitsu engineer published in 1996 states that "[a]synchronous DRAMs, be that EDO or Burst EDO, can not keep up with bus speeds of over 66 MHz." (RX 2099-4 at 4). Jacquelyn Gross of Hewlett-Packard, formerly of Compaq, testified that it was Compaq's view in the 1996-97 time frame that asynchronous technology was limited in the bandwidth it could achieve and that synchronous technology "provided higher benefits." (Gross, Tr. 2347). Steve Polzin of AMD testified that in the 1996-97 time frame it was his opinion that, due to inherent limitations, asynchronous technology had less "headroom," that is less of an ability to offer improved performance over time, than synchronous technology. (Polzin, Tr. 4033-35).

901. Burst EDO was an asynchronous type of DRAM that Micron was "strongly pushing" in the mid-1990s. (Williams, Tr. 822-823, 879). A 1995 Micron publication entitled "The Burst EDO DRAM Advantage" raises a question about the viability of Burst EDO ("BEDO") at bus speeds greater than 75 MHz and states that "BEDO will probably reach its limit somewhere around 100 MHz." (CX 2632 at 5).

902. Burst EDO was standardized by JEDEC in March 1995. (Williams, Tr. 873, 879-80; RX 585 at 1). However, Burst EDO failed in the marketplace in competition with SDRAM. (Williams, Tr. 829).

b. Programmable Burst Length.

903. Complaint Counsel, through Professor Jacob, have suggested the following possible alternatives to programmable burst length in SDRAMs:

(1) Use fixed burst length parts;

(2) Program burst length by blowing fuses on the DRAM;

(3) Use dedicated pins to transmit burst length information from the controller to the DRAM;

(4) Explicitly identify burst length in the read command;

(5) Use a burst terminate command;

(6) Use a CAS pulse to control data output.

(Jacob, Tr. 5397-5412).

(1) Use of Fixed Burst Length Parts Was Not a Viable Alternative.

904. Professor Jacob's proposed alternative of using fixed burst length parts, similar to his fixed CAS latency alternative, involves fixing the burst length of the DRAM during the design phase, manufacturing phase or packaging phase.

905. Complaint Counsel did not meet their burden of showing that the use of fixed burst length parts was a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs.

906. To the contrary, the evidence in the record shows that the use of fixed burst length parts was not a viable alternative to programmable burst length in SDRAMs and

DDR SDRAMs because multiple fixed burst length parts would have been required, leading to higher costs and logistical difficulties for DRAM manufacturers and users.

907. Different burst lengths are required for different applications, so multiple fixed burst length parts would be required for this alternative. (Soderman, Tr. 9368-69). As Gordon Kelley of IBM testified with respect to programmable burst length:

> "The programmable feature allowing you to make that selection when the PC or the computer powered up was a nice feature because it allowed you to use devices that were common from multiple suppliers, put them into many different types of machines. Some of them would be a burst length of one, some would be a burst length of four, with the same part that was programmed at power-up. One of the advantages of that is that that drives low cost. The producer does not have to maintain multiple part numbers. One part number fits many applications. That's one of the drives to low cost."

(Kelley, Tr. 2550-51).

908. The mode register in SDRAMs and DDR SDRAMs reserves three bits for burst length, allowing for up to eight different burst length values. (CX 234 at 150).

909. Release 4 of JEDEC Standard 21-C (November 1993), which contains the first published SDRAM standard, provided specified two required burst length values (4 and 8) and three optional burst length values (1, 2, and full page). (JX 56 at 114). Release 9 of JEDEC Standard 21-C (August 1999), which contains the first published DDR SDRAM standard, specified three required burst length values for SDRAMs (2, 4, and 8) and two optional values (1 and full page); it also specified three required burst length values for DDR SDRAMs (2, 4, and 8). (CX 234 at 150).

910. Burst lengths of one are used in graphics applications. (Lee, Tr. 11076).

911. Micron sells SDRAMs that allow for five different burst lengths (1, 2, 4, 8 and full page). (RX 2100-13 at 1; Lee, Tr. 11078-80).

912. Mark Kellogg of IBM noted that a disadvantage of fixing burst length in the manufacturing process would be that if a manufacturer did not have enough parts of the right burst length in stock, there could be a time lag of two weeks to one month before parts could be delivered. (Kellogg, Tr. 5119). Mr. Kellogg recommended to his company in 1992 that they support the programmable burst length feature because "[i]t offered us the greatest flexibility. We had a lot of applications." (Kellogg, Tr. 5132).

913. A fixed burst length would have been "very, very bad for AMD." (Polzin, Tr. 3994). AMD designed processors to use a burst length of eight "for performance reasons," but because Intel processors use a burst length of four, fixing burst length would have meant that manufacturers would most likely produce burst length four parts. (*Id*.).

914. JEDEC originally intended to fix the burst length at four in the DDR2 SDRAM standard . (Soderman, Tr. 9369; Macri, Tr. 4673-74). After further review by the DRAM manufacturers and the user community, it was determined that programmable burst length needed to be retained. (Soderman, Tr. 9369). DDR2 SDRAMs continue to have three bits in the mode register reserved for burst length, allowing for up to eight different burst length values. (RX 2099-14 at 21; RX 2099-39 at 20; Soderman, Tr. 9370). DDR2 SDRAMs currently require burst lengths of four and eight. (RX 2099-14 at 21;

RX 2099-20 at 22; Soderman, Tr. 9369). This may change in the future; thus, the flexibility provided by the mode register is very important. (Soderman, Tr. 9370).

915. The fixed burst length alternative would have resulted in increased costs.

916. There would have been an increase in design, photo tooling and qualification costs because multiple products would have had to be designed and manufactured rather than just one. (Geilhufe, Tr. 9679, 9682-83, 9690). As in the fixed CAS latency alternative, a minimal design effort would have been required for each different burst length; one mask would have had to be changed for each different burst length; and each different burst length part would have had to be qualified before it could have been sold. (Geilhufe, Tr. 959).

917. There would have been a decrease in testing costs due to the fact that each part would have had to be tested for a single burst length rather than multiple burst lengths. (Geilhufe, Tr. 9594).

918. There would have been additional inventory cost due to four different burst lengths parts being manufactured, one less than the number of required and optional burst lengths in the original SDRAM standard, instead of a single programmable burst length part. (Geilhufe, Tr. 9595; JX 56 at 114). Mark Kellogg of IBM testified that there would be an "economic disadvantage" from having multiple part numbers corresponding to different burst lengths. (Kellogg, Tr. 5119).

919. The fixed burst length alternative would have resulted in the following approximate net costs compared to SDRAM in the mid-1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: $100,000 increase in product design costs per latency; $50,000 increase in photo tooling costs per latency; one cent decrease per unit in testing costs at wafer sort; three cents per unit increase in inventory costs; and $250,000 increase in qualification costs per latency. (Geilhufe, Tr. 9562-64, 9594-95).

920. The net increase in variable costs for the fixed burst length alternative is, therefore, approximately 2 cents per unit. The total cost increase is approximately 4 cents per unit, calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9595-96).

921. If both CAS latency and burst length were fixed, one would need to multiply the number of latencies by the number of burst lengths to calculate the total number of parts required. For example, if there were three latencies and four burst lengths, 12 parts would be required. (Geilhufe, Tr. 9601). Fixing both CAS latency and burst length would thus increase inventory costs by far more than the increase that woudl result from fixing CAS latency or burst length, but not both. (*Id.*).

(2) Programming Burst Length with Fuses Was Not a Viable Alternative.

922. Professor Jacob's proposed alternative of setting burst length with fuses is similar to his corresponding proposed alternative for programming CAS latency with fuses. (Jacob, Tr. 5403).

923. Complaint Counsel did not meet their burden of showing that setting burst length with fuses was a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs.

924. To the contrary, the evidence in the record shows that setting burst length with fuses was not a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs because multiple parts with different burst lengths would have been required, leading to higher costs and logistical difficulties for DRAM manufacturers and users.

925. Professor McAfee did not testify that this alternative was commercially viable. (McAfee, Tr. 7372).

926. Once the fuse is blown, the DRAM becomes a fixed burst length part under this alternative. (Jacob, Tr. 5404; Soderman, Tr. 9370). As with fixing the CAS latency, having multiple fixed burst length parts would lead to logistical difficulties exacerbated by the fact that the fuse could not be blown by OEMs. (Soderman, Tr. 9370-71; Kellogg, Tr. 5142).

927. Setting burst length with fuses would have resulted in increased costs.

928. There would have been an increase in design costs due to the design effort to provide the fuses required. (Geilhufe, Tr. 9575, 9584-85).

929. There would have been increased inventory and qualification costs of the same magnitude as the corresponding costs for the fixed burst length alternative because, once the fuse is blown, the part would be a fixed burst length part. (Geilhufe, Tr. 9585-89).

930. Setting burst length by blowing fuses would have resulted in the following approximate net costs compared to SDRAM in the mid-1990s, assuming a first-tier DRAM manufacturer using existing laser fuse technology and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: $100,000 increase in product design costs per latency; three cents per unit increase in inventory costs; and $250,000 increase in qualification costs per latency. (Geilhufe, Tr. 9562-64, 9596-98).

931. The net increase in variable costs for the alternative of setting burst length by blowing fuses is, therefore, approximately 3 cents per unit. The total cost increase is approximately 5 cents per unit calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9598).

932. If the DRAM manufacturer did not have antifuse or electrically blown fuse technology available and wished to use that technology, adding it to the manufacturing

process would entail several million dollars in development costs in addition to the costs above. (Geilhufe, Tr. 9583-84).

(3) Using Dedicated Pins to Identify Burst Length Was Not a Viable Alternative.

933. Professor Jacob's proposed alternative of using an existing or a new, dedicated pin to identify burst length is similar to his corresponding proposed alternative for using pins to identify CAS latency. (Jacob, Tr. 5405).

934. Complaint Counsel did not meet their burden of showing that using dedicated pins on the DRAM to identify burst length was a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs.

935. To the contrary, the evidence in the record shows that using dedicated pins on the DRAM to identify burst length was not a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs, because it would be significantly costlier. Moreover, using dedicated pins to identify burst length is not an "alternative" at all because it is covered by Rambus's patents.

936. As with the use of pins to set CAS latency, this alternative would lead to additional costs associated with adding pins to the DRAM, wiring to the module and the motherboard, and adding pins to the controller. (Soderman, Tr. 9371).

937. When asked about the advantages of using pins to set burst length, Gordon Kelley of IBM responded:

"I can't think of a lot of advantages compared to the

> programmable feature, which did not require a pin. I can think of the disadvantage that having a pin or using up a pin to do burst length selection was not a thing that we did easily, because once you use that pin up for a function, you don't have it available to you in the future for generation advance. As the memory densities increase, we need pins for more addressing of more address locations and those pins are very valuable for that feature, so this would have limited the number of generations of DRAM design that we could have used if we were to use up this pin."

(Kelley, Tr. 2552-53).

938. This "alternative" is not really an alternative at all since it is covered by the same Rambus patents that cover SDRAMs and DDR SDRAMs. For example, this alternative would be covered by claim 1 of U.S. Patent 6,324,120, assigned to Rambus, which claims:

> "A method of operation of a synchronous memory device, wherein the memory device includes an array of memory cells, the method of operation comprises:
> receiving an external clock signal;
> receiving block size information, wherein the block size information defines an amount of data to be output by the memory device in response to a first operation code;
> sampling the first operation code synchronously with respect to the external clock signal wherein the first operation code instructs the memory device to perform a read operation; and
> outputting the amount of data in response to the first operation code."

(RX 2099-52 at 31-32; Soderman, Tr. 9371-72).

939. A claim covers a device if each and every claim element or "limitation" is found in that device. (Nusbaum, Tr. 1565-66). SDRAMs are synchronous memory

devices that contain an array of memory cells. (Rhoden, Tr. 359-60, 369-70). Moreover, the claim's reference to "receiving block size information" includes receiving burst length information using a pin. (Soderman, Tr. 9372-73). Thus, each and every element of claim 1 of the '120 patent would be found in SDRAMs that implemented the use of dedicated pins to identify burst length.

940. Programming burst length by using dedicated pins would have resulted in the following approximate net costs compared to SDRAM in the mid-1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: 2 cents in increased packaging costs per unit due to an additional two pins. (Geilhufe, Tr. 9562-64, 9599). This 2-cent increase is a variable cost.

941. Although SDRAMs use three bits to program burst length, the cost calculation above involves the addition of only two pins based on the assumption that if pins were being used to set burst length, they would also be used to set CAS latency. (Geilhufe, Tr. 9599). Because pins have to be added in even increments, four pins were added to program CAS latency although only three were required. That extra pin, plus two additional pins, are sufficient to set burst length. (Id). If burst length were being set using pins, but not CAS latency, then an additional four pins would be required to achieve the same degree of flexibility as provided in the SDRAM standard. (Geilhufe, Tr. 9599-9600).

942. As in the case of using dedicated pins for CAS latency, the estimated two cent increase cost for this alternative is very conservative. (Geilhufe, Tr. 9599).

(4) Explicitly Identifying Burst Length in the Read Command Was Not a Viable Alternative.

943. Professor Jacob's proposed alternative of identifying burst length in the read command is similar to his corresponding proposed alternative for identify CAS latency in the read command. (Jacob, Tr. 5407).

944. Complaint Counsel did not meet their burden of showing that identifying burst length in the read command was a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs.

945. To the contrary, the evidence in the record shows that, as with the alternative of using dedicated pins to identify burst length, this is not really an alternative because it would be covered by the same Rambus patents that read on SDRAMs and DDR SDRAMs.

946. For example, claim 1 of the '120 patent, reproduced above, would cover this alternative because it covers "receiving block size information" including when the block size (equivalently, burst length) information is embedded in a read command. (RX 2099-52 at 31-32; Soderman, Tr. 9373-74).

(5) Using a Burst Terminate Command Was Not a Viable Alternative.

947. Professor Jacob's proposed alternative of using a burst terminate command rather than programming burst length through the mode register would involve defining all

parts to have a fixed, long burst length and then sending a command to terminate the burst if a shorter burst length were desired. (Jacob, Tr. 5409).

948. Complaint Counsel did not meet their burden of showing that using a burst terminate command was a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs.

949. To the contrary, the evidence in the record shows that using a burst terminate command was not a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs, because it would result in significantly lower performance.

950. A burst terminate command is an optional feature in SDRAMs. (CX 234 at 161). The burst terminate command is required in DDR SDRAMs, but can be used only to terminate "read" bursts, not "write" bursts. (CX 234 at 174). Although DDR SDRAMs have this burst terminate command available, DDR SDRAMs program burst length in the mode register. (CX 234 at 150).

951. A burst length of one would not have been possible with a burst terminate command because when a read command is issued it takes one cycle to execute before a burst terminate command could be encountered and, but that point, there are already two bits of data coming out. (Geilhufe, Tr. 9598-99).

952. Professor Jacob's proposed alternative of using a burst terminate command would lead to inefficiencies on the bus. (Jacob, Tr. 5411. For example, terminating a read burst when the next command is a write leads to inefficient bus utilization because data

already in the pipeline to be read out must be cleared before data can be written to the DRAM. (Soderman, Tr. 9374-76). Moreover, when the burst terminate command was on the bus, the controller would not be able to send a command to another bank. (Jacob, Tr. 11126).

953. In fact, according to a study performed by Professor Jacob and a graduate student, this alternative could lead to a 10-15 percent decrease in the efficiency of the system. (Jacob, Tr. 5604-06).

954. JEDEC participants considered "burst terminate" an "internal device timing nightmare." (CX 415 at 10).

955. Steve Polzin of AMD testified that use of a burst terminate command would interfere with pipelining and make the system less efficient overall. (Polzin, Tr. 4038-40).

956. The JEDEC Future DRAM Task Group considered eliminating the burst terminate command, also known as "burst interrupt," from DDR2 because at "high data rates burst interrupt commands are of less value, and are more difficult to engineer." (CX 392 at 5). The Task Group also noted that elimination of burst terminate would "reduce[] test costs" and "increase[] yield due to elimination of speed critical path." (RX 2234 at 10).

957. Although JEDEC retained some form of burst terminate in DDR2 SDRAM, the timing difficulties led JEDEC to limit its use. (Soderman, Tr. 9376-77). As Joe Macri, chairman of the JEDEC Future DRAM Task Group focusing on DDR2, testified:

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(Macri, Tr. at 4774, **in camera**). Thus, in the DDR2 standard, burst terminate can be used only to truncate a burst of eight to four, and it can be used only when reads are followed by reads or writes are followed by writes, not when a read is followed by a write or a write is followed by a read. (RX 2099-39 at 63; Soderman, Tr. 9376-77). Despite including this limited form of a burst terminate command in the DDR2 standard, JEDEC also included the programmable burst length feature. (RX 2099-39 at 20).

(6) Using CAS Pulse to Control Data Output Was Not a Viable Alternative.

958. Professor Jacob's proposed alternative of using a CAS pulse to control data output involves toggling the CAS line to the DRAM once for each bit of data desired – thus, if a burst of four were required, the CAS line would be toggled four times. (Jacob, Tr. 5411-12).

959. Complaint Counsel did not meet their burden of showing that using a CAS pulse to control data output was a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs.

960. To the contrary, the evidence in the record shows that using a CAS pulse to control data output was not a viable alternative to programmable burst length in SDRAMs and DDR SDRAMs, because it would lead to cost, testing and performance problems.

961. Professor McAfee did not testify that this was a commercially viable alternative.

962. This alternative would not work as Professor Jacob described it because it is not clear how the DRAM would be able to determine whether a signal on the CAS line were intended to be a "toggle" that was part of a burst of data or a new command. (Soderman, Tr. 9378-79). Sophisticated additional circuitry would have to be added to allow the DRAM to recognize the toggling of the CAS line, and that would add cost and create testing problems. (Soderman, Tr. 9379).

963. In addition, this alternative would not allow efficient interleaving between banks without adding more CAS lines. (Soderman, Tr. 9379-80). Currently, while one bank of an SDRAM is reading out data, the CAS line can be used to send a command to a second bank, a process known as interleaving. Under the proposed CAS pulse alternative, the CAS line would be toggling in connection with the burst and additional CAS lines would have to be added to the other banks to enable this sort of operation. (*Id.*). Because there are four banks on each DRAM, three CAS lines would have to be added requiring additional pins on the DRAM and the controller, as well as additional circuitry on the DIMMs and the motherboard. (Soderman, Tr. 9380).

c. There Is Evidence That Some Of Complaint Counsel's Proposed Alternatives To Programmable CAS Latency and Programmable Burst Length Would Infringe Rambus Patents.

964. Rambus has come forward with a number of patents that it contends cover certain of the alternatives to programmable CAS latency and programmable burst length proposed by Complaint Counsel through their technical expert, Professor Jacob. In particular, as set forth above, there is evidence to support Rambus's contention that the alternatives of scaling CAS latency with clock frequency and identifying CAS latency in the read command are covered by Rambus's '263 patent. *See* Findings ¶¶ 862-864, 886-890. The latter alternative also may be covered by Samsung's '956 patent. *See* Findings ¶ 892.

965. Likewise, there is evidence to support Rambus's contention that the proposed alternatives of using dedicated pins to set burst length and identifying burst length in the read command are covered by Rambus's '120 patent. *See* Findings ¶¶ 938-939, 945-946.

966. Professor Jacob did not consider any of the patents raised by Rambus in his analysis of proposed alternatives; indeed, Professor Jacob did no investigation at all as to whether his proposed alternatives were encumbered by patents. *See* Findings ¶¶ 793, 892.

967. Professor McAfee has testified that one of the alternatives proposed by Professor Jacob to dual-edge clocking, interleaving on-module ranks, would require royalty payments to Kentron. (McAfee, Tr. 7404). In considering whether the other

alternatives proposed by Professor Jacob were commercially viable, he assumed that they were unencumbered by patents. (McAfee, Tr. 7582-84). Professor McAfee admitted that, if this assumption was incorrect and there were patents attached to alternatives that he had concluded were commercially viable, "it could be in principle upset my conclusion that they were commercially viable." (McAfee, Tr. 7584).

968. Complaint Counsel has introduced no evidence that the patents raised by Rambus do not cover certain of the proposed alternatives. Even with his assumption of no patent coverage, Professor McAfee could not testify that the alternative of scaling CAS latency with clock frequency was commercially viable. As for Professor McAfee's opinions that identifying CAS latency in the read command, using dedicated pins to set burst length, and identifying burst length in the read command were each commercially viable, these opinions are based on the incorrect assumption that these alternatives are not encumbered by patents. It follows that Professor McAfee's opinions in this regard are entitled to no weight.

d. Given The Cost-Performance Differences, An Economically Rational DRAM Manufacturer Would Have Adopted And Licensed The Rambus Technologies Incorporated In SDRAM If It Had Known Of Rambus's Royalty Rates In Advance.

969. JEDEC-compliant SDRAM parts use two of the four Rambus technologies at issue: programmable CAS latency and programmable burst length. In order to determine whether the use of alternatives to the Rambus technologies used in SDRAM is

more costly than paying the Rambus royalties, one can determine the additional variable costs associated with the alternatives and compare them to the Rambus royalties that would be paid under the a license from Rambus. (Rapp, Tr. 9830-33). Costs for alternatives to different features are additive; that is, to calculate the costs associated with implementing alternatives to more than one feature simultaneously, one would simply add the costs associated with the individual alternatives. (Geilhufe, Tr. 9614).

970. To make this comparison, the total additional cost of each alternative is divided by the weighted average of the selling price ("ASP") of SDRAM for the period 1996 to 2006. (Rapp, Tr. 9816-17, 9830-33). For SDRAM, the ASP is $4.87. (Rapp, Tr. 9816-17). This calculation shows the additional cost of the alternative as a percentage of selling price.

971. The Rambus royalty rate for the use of its technologies in SDRAM is 0.75%. (Rapp, Tr. 9832).

972. The alternatives for programmable CAS latency identified as "commercially viable" by Complaint Counsel's economic expert were: fixed CAS latency, explicitly identify latency in the read command, programming latency with fuses, and using multiple pins to set a latency value. (Rapp, Tr. 9810-11; McAfee, Tr. 7354-63).

973. The total additional incremental costs associated with the use of the fixed latency alternative is $0.04 per part. (Rapp, Tr. 9814). This total consists of the following additional incremental costs per part: a $0.01 wafer sort cost savings, a $0.03 good die

yield cost increase, and a $0.02 inventory cost increase. (Rapp, Tr. 9814). As a percentage of ASP, this total additional incremental cost is 0.82%. (Rapp, Tr. 9817). (These numbers are illustrated in DX307.)

974. The total additional incremental costs associated with the use of the alternative of explicitly identifying latency in the read command is $0.01 per part, which is the additional incremental costs associated with packaging. (Rapp, Tr. 9814-15). As a percentage of ASP, this total additional incremental cost is 0.21%. (Rapp, Tr. 9817). (These numbers are illustrated in DX307.) As discussed above, this alternative is covered by Rambus's patents.

975. The total additional incremental cost associated with the use of the alternative of programming latency with fuses is $0.06 per part. (Rapp, Tr. 9815). This total consists of the following additional incremental costs per part: a $0.01 wafer sort cost increase, a $0.03 good die yield cost increase, and a $0.02 inventory cost increase. (Rapp, Tr. 9815). As a percentage of ASP, this total additional incremental cost is 1.23%. (Rapp, Tr. 9817-18). (These numbers are illustrated in DX307.)

976. The total additional incremental costs associated with the use of the alternative of using multiple pins to set latency is $0.04 per part, which is the additional incremental costs associated with packaging. (Rapp, Tr. 9815). As a percentage of ASP, this total additional incremental cost is .82%. (Rapp, Tr. 9818). (These numbers are illustrated in DX 307).

977. In addition to the additional incremental costs, each of the alternatives for programmable CAS latency either has performance disadvantages when compared to Rambus's technology or is covered by Rambus's patents. (Rapp, Tr. 9819-23). (These disadvantages are illustrated in DX308.)

978. The alternatives for programmable burst length identified as "commercially viable" by Complaint Counsel's economic expert were: fixed burst length, explicitly identify burst length in the read command, using a burst terminate command, and using multiple pins to set the burst length. (Rapp, Tr. 9810-11; McAfee, Tr. 7366-72).

979. The total additional incremental costs associated with the use of the fixed burst length alternative is $0.02 per part. (Rapp, Tr. 9824-25). This total consists of the following additional incremental costs per part: a $0.01 wafer sort cost savings and a $0.03 inventory cost increase. (Rapp, Tr. 9825). As a percentage of ASP, this total additional incremental cost is 0.41%. (Rapp, Tr. 9825). (These numbers are illustrated in DX309.)

980. The total additional incremental costs associated with the use of the alternative of explicitly identifying burst length in the read command is $0.01 per part, which is the additional incremental costs associated with packaging. (Rapp, Tr. 9825-26). As a percentage of ASP, this total additional incremental cost is 0.21%. (Rapp, Tr. 9826). (These numbers are illustrated in DX309.) As discussed above, this alternative is covered by Rambus's patents.

981. There is no additional incremental cost associated with the use of the alternative of using a burst terminate command to set burst length. (Rapp, Tr. 9826). As discussed above, this alternative suffers from performance drawbacks.

982. The total additional incremental costs associated with the use of the alternative of using multiple pins to set latency is $0.02 per part, which is the additional incremental costs associated with packaging. (Rapp, Tr. 9826). As a percentage of ASP, this total additional incremental cost is .41%. (Rapp, Tr. 9826). (These numbers are illustrated in DX 309.) As discussed above, this alternative is covered by Rambus's patents.

983. In addition to the additional incremental costs, each of the alternatives for programmable burst length either has performance disadvantages when compared to Rambus's technology or is covered by Rambus's patents. (Rapp, Tr. 9828-30). (These disadvantages are summarized in DX 310.)

984. The most costly alternatives to the two identified Rambus technologies that are used in JEDEC-compliant SDRAM that are not covered by Rambus's patents are the use of fuses to set latency and the use of fixed burst length. (Rapp, Tr. 9832). The total additional incremental cost of using these two alternatives is $0.08 per part. (Rapp, Tr. 9832). As a percentage of ASP, this additional incremental cost is 1.64%, which exceeds the 0.75% Rambus royalty rate. (Rapp, Tr. 9832). (These numbers are illustrated in DX 311.)

985. The least costly alternatives to the two Rambus technologies that are used in JEDEC-compliant SDRAM that are not covered by Rambus's patents are the use of fixed CAS latency and the use of a burst terminate command to set burst length. (Rapp, Tr. 9831). The total additional cost of using these two alternatives is $0.04 per part. (Rapp, Tr. 9831-32). As a percentage of ASP, this additional incremental cost is 0.82%, which exceeds the 0.75% Rambus royalty rate. (Rapp, Tr. 9832). (These numbers are illustrated in DX 311.)

986. In order to determine what royalty a rational decision-maker would have expected Rambus to charge (in the absence of direct knowledge), the standard assumption and methodology in economics is to assume that the royalty rate actually charged is the best estimate of the royalty rate a decision-maker would have expected at an earlier time. (Rapp, Tr. 10207-09). Similarly, the standard assumption and methodology in economics is to assume that the actual weighted average selling price over the product life cycle is the best estimate of an ASP that a decision-maker would have predicted in advance. (Rapp, Tr. 10212-13). Using the standard assumptions and methodology in economics, a rational DRAM manufacturer or group of manufacturers would have expected the additional costs of any alternatives to outweigh the costs of Rambus's royalties.

987. Even without any reference to performance penalties, a rational manufacturer or group of manufacturers in JEDEC would have chosen to take a license from Rambus at 0.75% for SDRAM rather than use any combination of the alternatives

identified by Complaint Counsel's economic expert as "commercially viable" that are not covered by Rambus's patents because all of those alternatives are more costly than licensing the Rambus technologies for SDRAM. (Rapp, Tr. 9833). Taking performance issues into account would have reinforced the decision to license rather than to substitute any of these alternatives because most of the alternatives have performance problems as well. (Rapp, Tr. 9833).

988. Accordingly, a rational standard-setting organization that knew that Rambus had patent interests on those two technologies but did not know precisely what Rambus's royalty rates would be to license the technologies would have selected the Rambus technologies. (Rapp, Tr. 9838-39). That is true even if the standard-setting body were acting in a satisficing manner. (Rapp, Tr. 9839-40). If satisficing means that small cost differences are overlooked, then a satisficing standard-setting body would be indifferent to the prospect of paying royalties; therefore, the theory of satisficing does not contribute to the analysis. (Rapp, Tr. 9839-40).

4. There Were No Viable Non-Infringing Alternatives To The Specified Rambus Technologies Adopted In DDR SDRAM.

989. The discussion above applies to the two specified Rambus technologies that were carried over from SDRAM to DDR SDRAM, namely programmable CAS latency and programmable burst length.

a. Dual-Edge Clocking.

990. Complaint counsel, through Professor Jacob, have suggested the following possible alternatives to dual-edge clocking in DDR SDRAMs:

(1) Interleave on-chip banks;

(2) Interleave on-module ranks;

(3) Increase the number of pins on the DRAM;

(4) Increase the number of pins on the module;

(5) Double the clock frequency;

(6) Use simultaneous bidirectional input/output;

(7) Use toggle mode.

(Jacob, Tr. 5415-5438).

(1) Interleaving On-Chip Banks Was Not a Viable Alternative.

991. Professor Jacob's alternative of interleaving on-chip banks involves sending a clock signal to one bank on the DRAM and a second clock signal, a delayed version of the first, to another bank. (Jacob, Tr. 5419-20, 5614). Data would then be output or input on only a single edge of each clock signal, alternating between the two banks. (*Id.*).

992. Complaint Counsel did not meet their burden of showing that interleaving on-chip banks was a viable alternative to dual-edge clocking in DDR SDRAMs.

993. To the contrary, the evidence in the record shows that interleaving on-chip banks was not a viable alternative to dual-edge clocking in DDR SDRAMs, because it

suffers from performance and cost disadvantages. Moreover, interleaving on-chip banks is not an alternative because it is covered by Rambus patents.

994. Professor McAfee did not testify that interleaving on-chip banks was a commercially viable alternative. (McAfee, Tr. 7376-81).

995. Efficient implementation of interleaving on-chip banks would still require dual-edge clocking and, therefore, is not an alternative. (Soderman, Tr. 9366). That is because the successive data signals from each bank should be given equal amounts of time on the bus. If one bank were given a shorter time window for detection of data signals than the other, the data given the shorter time window might not be detected accurately; if, the data could be detected accurately in such a short time window, then it would be more efficient to restrict both banks to such a time window and run the bus at a faster speed. (Soderman, Tr. 9384-85). Also, a multiplexer would be used to select which bank is outputting data onto the bus at a given time. (Soderman, Tr. 9384). But the multiplexer must have a timing reference to tell it when to switch from one bank to the other. If one of the two clocks required by Professor Jacob's alternative is used for this reference, then data will be output onto the bus on both the rising and falling edge of this clock (since the falling edge of one of these clocks corresponds to the rising edge of the other); if, on the other hand, a third clock (not specified by Professor Jacob) is used to time the multiplexer, data would have to be output on the rising and falling edges of that clock. (Soderman, Tr. 9384-86).

996. Even if interleaving on-chip banks did not require dual-edge clocking, it would still not be an alternative to Rambus's technology because it is covered by U.S. Patent No. 5,915,105, assigned to Rambus. (RX 1472).

997. For example, claim 27 of the '105 patent claims:

> A memory device having at least one memory section which includes a plurality of memory cells, the memory device comprises:
>
> a first clock receiver to receive a first external clock signal;
>
> a second clock receiver to receive a second external clock signal; and
>
> input receiver circuitry, coupled to the first and second clock receivers, to sample information on a bus synchronously with respect to the first and second external clock signals.

998. A claim covers a device if each and every claim element or "limitation" is found in that device. (Nusbaum, Tr. 1565-66). SDRAMs are memory devices that have memory sections containing a plurality of memory cells. (Rhoden, Tr. 359-60, 369-70). Interleaving on-chip banks involves two external clock signals, with the first going to one bank on the DRAM and the second to another bank. (Jacob, Tr. 5419-20, 5614). Data would then be input or "sampled" synchronously with respect to the first and second external clock signals. (*Id*.). Thus, each and every element of claim 27 of the '105 patent would be found in DDR SDRAMs that implemented interleaving on-chip banks.

999. Professor Jacob did not consider the '105 patent when he proposed interleaving on-chip banks as an alternative. (Jacob, Tr. 5615-16).

1000. Performance disadvantages of interleaving on-chip banks include significant increased power dissipation because of the power consumed by the additional clocks and

the fact that two banks are being accessed alternately. Keeping both banks active doubles the number of precharge cycles, and the precharge operation may be the most power consuming part of the whole DRAM operation. (Soderman, Tr. 9387).

1001. The alternative of interleaving on-chip banks would also have resulted in increased costs.

1002. There would have had to be a significant design effort for this alternative. (Geilhufe, Tr. 9602-03).

1003. There would have been a reduction in good die yield due to additional critical die area. (Geilhufe, Tr. 9603-04). So-called "redundancy technology" can be used to replace a defective part of the memory array on a DRAM, but the peripheral circuitry is "critical" in the sense that a defect in that circuitry will cause the unit to fail. (Geilhufe, Tr. 9603). The additional peripheral circuitry that would have been required to implement this alternative – such as multiplexing circuitry and timing circuitry – is critical in nature and defects in this circuitry would have reduced the good die yield. (Geilhufe, Tr. 9603-04).

1004. This alternative would have also complicated final testing and led to a slightly higher fall-out at that stage due to the necessity to activate two banks and to test the additional clocking circuitry. (Geilhufe, Tr. 9604).

1005. The alternative of interleaving on-chip banks would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990s, assuming a

first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: $250,000 increase in product design costs; three cents per unit cost increase due to reduced good die yield; two cents per unit increase in final testing and good unit yield costs. (Geilhufe, Tr. 9562-64, 9602-04).

1006. The net increase in variable costs for the alternative of interleaving on-chip banks is, therefore, approximately 5 cents per unit. The total costs increase is approximately 6 cents per unit, calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9604-05).

(2) Interleaving On-Module Ranks Was Not a Viable Alternative.

1007. Professor Jacob's proposed alternative of interleaving banks on the DIMM or memory module is similar to his proposed alternative of interleaving on-chip banks except that data from different chips in a module, rather than data from different banks on the same chip, would be interleaved. (Jacob, Tr. 5426).

1008. Complaint Counsel did not meet their burden of showing that interleaving on-module ranks was a viable alternative to dual-edge clocking in DDR SDRAMs.

1009. To the contrary, the evidence in the record shows that interleaving on-module ranks was not a viable alternative to dual-edge clocking in DDR SDRAMs, because it would be significantly costlier, in addition to having performance problems.

Moreover, interleaving on-module ranks would provide less flexibility than dual-edge clocking and would not be available for all applications.

1010. Implementing this technology would require high speed bidirectional switches or multiplexers. (Soderman, Tr. 9389). Such bidirectional switches would require sophisticated engineering and would add appreciable cost. (*Id*.). Moreover, additional hardware would be required to drive the switches. (*Id*.).

1011. Professor Jacob testified that this alternative would have significant advantages and that the only disadvantage would be a slight complication of the memory module because of an extra clock line. (Jacob, Tr. 5427-28). Professor Jacob did not testify about any need for expensive high speed switches. (*Id*.). Unlike most of Professor Jacob's proposed alternatives, his opinion about this alternative can be tested because a company, Kentron Technologies, has actually tried to implement the alternative of interleaving on module ranks. (Soderman, Tr. 9388).

1012. Kentron's "QBM" technology involves interleaving between chips on the module. (Goodman, Tr. 5997, 6002-03). Robert Goodman, Kentron's Chief Executive Officer, testified that the QBM technology requires the use of advanced switches. (Goodman, Tr. 6082). Mr. Goodman further testified that each module would require eight switches at a dollar apiece in high-volume production, for a total of eight dollars per module. (Goodman, Tr. 6046-47, 6083). Additional circuitry, such as a PLL on the module is also required. (Goodman, Tr. 6048).

1013. Although Kentron now uses DDR SDRAM chips in its QBM technology, it initially called the technology "DBR" for "double bus rate" and used SDRAM chips. (CX 409 at 2). Kentron asserted that it could achieve the "same performance as 'DDR' using standard SDRAM single data rate." (*Id*.).

1014. **{IN CAMERA MATERIAL REDACTED}**

(RX 1976 at 49) **[In Camera]** .

1015. AMD's preliminary evaluation of the Kentron QBM technology concluded that it would have signal integrity problems. (Polzin, Tr. 4035-36).

1016. At the September 2000 JEDEC meeting, Kentron's motion to ballot QBM technology failed for lack of a second. (CX 160 at 1).

1017. Kentron has no customers for its QBM technology. (Goodman, Tr. 6008).

1018. Interleaving on-module ranks suffers from additional disadvantages. First, it would lead to a less flexible memory increment: Because high bandwidth is achieved by interleaving between DRAMs, twice as many DRAMs would be required on the DIMM to achieve the same bandwidth as is available using dual-edge clocking. (Soderman, Tr. 9389-90).

1019. Moreover, this alternative would not be available in all applications since many applications do not use modules at all but, rather, have the DRAM soldered directly onto the motherboard. (Soderman, Tr. 9390-91; Wagner, Tr. 3871-72).

1020. The alternative of interleaving on-module ranks would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: four dollars per module for multiplex and driver circuitry. (Geilhufe, Tr. 9562-64, 9605-06).

1021. This four dollar per module cost translates into a 25 cent per DRAM cost for DIMMs, which are memory modules containing 16 DRAMs each.(Geilhufe, Tr. 9606). This 25-cent increase is a variable cost.

(3) Increasing the Number of Pins on the DRAM Was Not a Viable Alternative.

1022. Professor Jacob's proposed alternative of increasing the number of pins per DRAM involves achieving high bandwidth by using only a single edge of a clock but doubling the number of data pins. (Jacob, Tr. 5429).

1023. Complaint Counsel did not meet their burden of showing that increasing the number of pins on the DRAM was a viable alternative to dual-edge clocking in DDR SDRAMs.

1024. To the contrary, the evidence in the record shows that increasing the number of pins on the DRAM was not a viable alternative to dual-edge clocking in DDR SDRAMs, because it would be significantly costlier, in addition to having performance problems.

1025. Professor McAfee did not testify that this alternative is commercially viable. (McAfee, Tr. 7376-81).

1026. In addition to doubling the number of data pins, this alternative would require increasing the number of power and ground pins in order to support the added data pins. (Jacob, Tr. 5429-30). The number of pads and receivers on the DRAM would also have to be increased, leading to an increase in the size of the DRAM die and the size of the package. (Jacob, Tr. 5430-31).

1027. The additional data signals would toggle very fast and cause noise that could perturb the DRAM or other circuitry on the board. (*Id.*).

1028. Tom Landgraf of Hewlett-Packard testified that his company was in favor of including dual-edged clocking in the DDR standard because of cost concerns. (Landgraf, Tr. 1709). Mr. Landgraf explained:

> "In DDR, double data rate memory, you need -- you're essentially transitioning data twice as fast as at a single data rate, and since memory systems tend to be very cost-competitive, one of our goals was to minimize the number of new pins we had to add to the next generation of memory. So, by using the double edged clock to transfer data, we were using the package and the pins more efficiently."

(Landgraf, Tr. 1709-10).

1029. The alternative of increasing the number of pins on the DRAM would be very expensive because of the number of additional pins required. (Soderman, Tr. 9391-92). For example, DRAMs with 16 data pins would have to have 16 additional data pins, plus additional power and ground pins. (*Id*.). Moreover, the pins would need to be interconnected through the DIMM to the motherboard, increasing the cost of the whole system. (Soderman, Tr. 9392).

1030. There would have been additional product design costs because of the significant design effort associated with adding 16 input/output drivers and related multiplexing circuitry. (Geilhufe, Tr. 9607).

1031. There would have been a reduction in good die yield because of the considerable amount of critical die area added by the additional input/output circuitry. (Geilhufe, Tr. 9607).

1032. There would have been additional packaging costs associated with a more sophisticated and packaging technology known as a "ball grid array," which would have been required by the addition of 16 input/outputs. (Geilhufe, Tr. 9607-08).

1033. The alternative of increasing the number of pins on the DRAM, assuming that the data width would be doubled from 16 to 32, would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a

volume of 20 million unit volume, that is, a product that has already realized its cost improvement: $250,000 increase in product design costs; five cent per unit cost increase due to reduced good die yield; 25 cent per unit increase in packaging costs. (Geilhufe, Tr. 9562-64, 9607-08).

1034. The net increase in variable costs for the alternative of increasing the number of pins on the DRAM is, therefore, approximately 30 cents per unit. The total cost increase is approximately 31 cents per unit, calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9579).

(4) Increasing the Number of Pins on the Module Was Not a Viable Alternative.

1035. Professor Jacob's proposed alternative of increasing the number of pins per module would not change the single data rate DRAM at all but would achieve the desired bandwidth by adding data pins to the module. (Jacob, Tr. 5431).

1036. Complaint Counsel did not meet their burden of showing that increasing the number of pins per module was a viable alternative to dual-edge clocking in DDR SDRAMs.

1037. To the contrary, the evidence in the record shows that increasing the number of pins per module was not a viable alternative to dual-edge clocking in DDR SDRAMs, because it would be significantly costlier and would be unavailable in certain applications.

1038. Professor McAfee testified that this alternative is *not* commercially viable. (McAfee, Tr. 7378).

1039. This alternative would require 128 wires on the motherboard and 128 pins on the memory controller. (Jacob, Tr. 5432-33).

1040. This alternative would be expensive because of the extra pins and wires required. (Soderman, Tr. 9392-93).

1041. This alternative would not be available in all applications because many applications do not use modules at all but, rather, have the DRAM soldered directly onto the motherboard. (Soderman, Tr. 9390-91; CX 2833; Wagner, Tr 3871-72).

(5) Doubling the Clock Frequency Was Not a Viable Alternative.

1042. In Professor Jacob's proposed alternative of doubling the clock frequency, rather than using both the rising and falling edges of a clock, only a single edge of a clock running at twice the frequency would be used to achieve the same bandwidth. (Jacob, Tr. 5433-34).

1043. Complaint Counsel did not meet their burden of showing that doubling the clock frequency was a viable alternative to dual-edge clocking in DDR SDRAMs.

1044. To the contrary, the evidence in the record shows that doubling the clock frequency was not a viable alternative to dual-edge clocking in DDR SDRAMs, because it would be significantly costlier, in addition to being difficult to implement and having performance problems.

1045. This alternative would require a clock signal that transitions at twice the rate of present systems and would, therefore, burn twice as much power as present systems. (Jacob, Tr. 5434-35).

1046. This alternative would cause clock distribution problems, because routing the clock signal through the DIMM to the various DRAMs is a critical task that becomes much more difficult at higher frequencies. (Soderman, Tr. 9393-94).

1047. This alternative would also lead to increased electromagnetic radiation from the higher frequency clock. (Soderman, Tr. 9395). Both DRAM manufacturers and systems companies are very careful about the amount of electromagnetic radiation generated because it can interfere with other circuitry and because there are strict FCC guidelines as to how much such radiation is permissible. (*Id*.).

1048. Mark Kellogg of IBM testified that at the time that JEDEC was considering using dual-edged clocking in DDR SDRAMs, the "predominant disadvantage" of using a higher frequency clock was "electromagnetic interference, radiation, the fact that fast pulses tend to radiate. And we've constantly been concerned, and at that time was no different, about our ability to distribute very high-speed signals throughout a system." (Kellogg, Tr. 5182).

1049. In July 1997, Texas Instruments made a proposal involving a high speed single-edge clock (CX 371 at 2-3; Lee, Tr. 6710-12). Terry Lee of Micron wrote the following in an e-mail about the Texas Instruments proposal: "A single frequency clock is

not practical. There is no real support yet for the higher frequency clock idea yet." (Lee, Tr. 11039, 11087-89).

1050. In September 2000, Micron proposed using a double frequency, single-edge clock in DDR2. (CX 2769 at 13; Lee, Tr. 6795-98).

1051. As late as November 2000, JEDEC was considering using a single data rate clock in DDR2. In an e-mail dated November 29, 2000, Terry Lee of Micron circulated a summary of a conference call regarding "clocking issues" in DDR2. (CX 426). The conference call included representatives of ATI, Micron, Hewlett-Packard, IBM, Intel, Mitsubishi, AMD, Texas Instruments, and others. (CX 426 at 2-4). The summary of the conference call includes the following statement:

> "Discussion on single data rate clock vs. double data rate clock
> Fundamentally question is that is single data rate clock possible?
> Micron believes that SDR has some advantages as it gets ride [sic] of duty cycle issue, it has old prior art, and the inherent bandwidth is better with write than read . . . .
> In general, everybody agreed that SDR clock is ok provided that it works."

(CX 426 at 4). The conference call participants ultimately concluded that "single data rate clock is preferred provided that we can make it work." (*Id.*).

1052. DDR2 SDRAMs use dual edge clocking. (RX 2099-14 at 3; RX 2099-39 at 5-6).

1053. The alternative of doubling the clock frequency would have resulted in increased costs.

1054. There would have been additional design costs associated with additional circuitry required for the faster clock. (Geilhufe, Tr. 9608-9).

1055. There would have been additional final testing costs associated with testing involving a clock that is running at the speed of current technology. This would have been a significant step up in testing that would have required changes in the test equipment and would have lowered yield. (Geilhufe, Tr. 9609).

1056. To distribute a double frequency clock on the DIMM would have required an on-DIMM clock. (Geilhufe, Tr. 9609). At the required frequency, that clock would have cost approximately $3.80. Because the cost of a clock is a function of frequency, such a clock could cost as much as $7 to $8 dollar for the highest frequency parts and much less for lower frequencies. (Geilhufe, Tr. 9609-10).

1057. The alternative of doubling the clock frequency would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million unit volume, that is, a product that has already realized its cost improvement: $100,000 increase in product design costs; four cent per unit cost increase due to higher speed final testing; $3.80 per module for an on-module clock. (Geilhufe, Tr. 9562-64, 9608-10).

1058. The net increase in variable costs for the alternative of doubling the clock frequency is approximately 28 cents per unit, obtained by dividing the “per module” costs

by 16 corresponding to the number of DRAMs on a DIMM and adding this to the other variable costs. (Geilhufe, Tr. 9610). Since the increase in fixed costs is relatively small, the total cost increase, calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs, is also approximately 28 cents per unit.

(6) Using Simultaneous Bidirectional I/O Drivers Was Not a Viable Alternative.

1059. Professor Jacob's proposed alternative of using simultaneous bidirectional input/output drivers involves a signaling scheme that allows read data and write data to exist on the bus simultaneously, potentially increasing bandwidth. (Jacob, Tr. 5435-36).

1060. Complaint Counsel did not meet their burden of showing that using simultaneous bidirectional I/O drivers was a viable alternative to dual-edge clocking in DDR SDRAMs.

1061. To the contrary, the evidence in the record shows that using simultaneous bidirectional I/O drivers was not a viable alternative to dual-edge clocking in DDR SDRAMs, because it would be very costly and difficult, if not impossible, to implement and would, in any event, not provide the performance of dual-edge clocking.

1062. Professor McAfee did not testify that simultaneous bidirectional I/O drivers was a commercially viable alternative. (McAfee, Tr. 7376-81).

1063. Simultaneous bidirectional input/output drivers involve a more complex driver design. (Jacob, Tr. 5437).

1064. This complex technology has been used in point-to-point systems in which there is only a single transmitter and receiver sending data back and forth and the time it takes to get from one to the other is known and built into the design parameters of the system. (Soderman, Tr. 9396-97). It would not work in a high-speed, bus-based system, such as used in general purpose computers, where there might be differing numbers of DRAMs connected to the bus and the components do not know precisely when signals being sent will arrive at other components. (*Id.*).

1065. Even if this alternative could be made to work, the amount of additional bandwidth that would result from the ability to read from and write to the DRAM simultaneously would depend on the application and on whether the read and write operations are balanced. (Jacob, Tr. 5437). For most systems, which require a burst of data to be read from the DRAM prior to writing to the DRAM and for which the read and write operations are thus not balanced, this alternative would not achieve the same high bandwidth as DDR SDRAMs. (Soderman, Tr. 9397-98). In the extreme case of an application that only read data from the DRAM but never wrote data to the DRAM, no benefit whatsoever would be obtained. (*Id.*).

1066. Rambus has considered using simultaneous bidirectional input/output for high speed signaling. (Horowitz, Tr. 8563). It has never been used, however, because Rambus could not implement it in a way that was not likely to cause errors. (Horowitz, Tr. 8563-64).

(7) Using Toggle Mode Was Not a Viable Alternative.

1067. By his proposed "toggle mode" alternative, Professor Jacob meant a DRAM like IBM's toggle mode DRAM. (Jacob, Tr. 5417).

1068. Complaint Counsel did not meet their burden of showing that toggle mode was a viable alternative to dual-edge clocking in DDR SDRAMs.

1069. To the contrary, the evidence in the record shows that toggle mode was not a viable alternative to dual-edge clocking in DDR SDRAMs, because it would be significantly costlier and could not achieve the performance of DDR SDRAMs with dual-edge clocking.

1070. IBM's "toggle mode" DRAM was an asynchronous design. (Jacob, Tr. 5608; Soderman, Tr. 9398; Sussman, Tr. 1472). Asynchronous technology could not achieve the same performance in a general purpose, bus type architecture as could synchronous technology. (Soderman, Tr. 9398-99)

1071. An IBM researcher described IBM's toggle mode DRAM as "very big, very hot, and very nonstandard." (RX 2099-7 at 16; Soderman, Tr. 9399-9400). The researcher went on to conclude that "in the commodity market, these attributes are disastrous." (*Id*.).

1072. The toggle mode alternative would have resulted in increased costs.

1073. The toggle mode alternative would have required signficant additional design costs. (Geilhufe, Tr. 9611).

1074. The good die yield would have been reduced due to additional critical die area. (Geilhufe, Tr. 9611).

1075. The toggle mode alternative would also have required an additional pin for the data toggle signal. Because pins must be added in pairs, two additional pins would have to be added. (Geilhufe, Tr. 9611).

1076. The toggle mode alternative would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million units, that is, a product that has already realized its cost improvement: $250,000 increase in product design costs; 10 cents cost increase per unit due to reduced good die yield; one cent cost increase per unit for an additional pin. (Geilhufe, Tr. 9562-64, 9610-11).

1077. The net increase in variable costs for the toggle mode alternative is, therefore, approximately 12 cents per unit. The total cost increase is approximately 13 cents per unit, calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run) and adding the resulting per unit fixed costs to the per unit variable costs. (Geilhufe, Tr. 9611-12).

b. <u>On-chip DLL</u>.

1078. Complaint Counsel has suggested, through Professor Jacob, the following possible alternatives to on-chip DLL in DDR SDRAMs:

(1) Put a DLL on the memory controller;

(2) Put a DLL on the module;

(3) Use a vernier method;

(4) Increase the number of pins on the DRAM;

(6) Rely on the DQS data strobe for timing.

(Jacob, Tr. 5443-5458).

1079. The purpose of the on-chip DLL in DDR SDRAMs is to compensate for internal delays on the DRAM and thereby to remove uncertainty in the timing of the system. (Jacob, Tr. 5442-43; Soderman, Tr. 9404).

1080. This timing uncertainty varies from DRAM to DRAM because of differences in process, temperature and voltage. (Soderman, Tr. 9402-03).

1081. The timing uncertainty compensated for by the DLL is more of a problem at high speeds because, as speeds increase, the window of time in which data is valid becomes smaller and the timing uncertainty reduces the size of the window even more. (Soderman, Tr. 9404-05).

1082. At high enough bus speeds, a DLL or PLL on the DRAM to compensate for individual timing uncertainties is required for correct operation. (Soderman, Tr. 9401-05).

1083. In the mid-1990s, DRAM engineers believed that a DLL or PLL on the DRAM would be necessary at future bus speeds. (RX 2099-29; RX 2099-13; Soderman, Tr. 9408-10).

1084. In a presentation on "Future SDRAM" at the March 1996 meeting of the JEDEC 42.3 subcommittee, Desi Rhoden presented a chart with columns representing clock speeds and rows representing certain features. (JX 31 at 64; Rhoden, Tr. 542-43). The chart indicates that "on-chip PLL/DLL" would be a "no" at 100 MHz, "maybe" at 150 MHz, and "yes" at 200 MHz and above. (*Id*.). Indeed, Mr. Rhoden testified that: "We discussed [on-chip PLL/DLL] at length inside of JEDEC, and I don't think we ever had any question whether we would use the technology. It was just a question of when." (Rhoden, Tr. 546).

1085. In an e-mail dated November 18, 1997, Bill Gervais of Transmeta wrote that "a DLL must be onchip and enabled for the Intel spec." (RX 1060). In other words, an on-chip DLL was required to meet Intel's timing requirements.

(1) Putting a DLL on the Memory Controller Was Not a Viable Alternative.

1086. Professor Jacob's proposed alternative of putting the DLL on the memory controller involves putting a DLL circuit on the memory controller rather than on each individual DRAM. (Jacob, Tr. 5445).

1087. Complaint Counsel did not meet their burden of showing that putting a DLL on the memory controller was a viable alternative to on-chip DLL in DDR SDRAMs.

1088. To the contrary, the evidence in the record shows that putting a DLL on the memory controller was not a viable alternative to on-chip DLL in DDR SDRAMs, because it would not be sufficient for high speed performance.

1089. This alternative is not sufficient for high speed performance because a DLL on the controller will broadcast the same delayed clock to all of the DRAMs and, therefore, cannot compensate for timing differences between DRAMs. (Soderman, Tr. 9405-06).

1090. Dr. Horowitz and other Rambus engineers have considered moving the DLLs off of the DRAMs and onto the memory controller on a number of occasions. (Horowitz, Tr. 8561-62). However, they determined that they were unable to meet the necessary timing requirements without a DLL on the DRAM. (*Id.*).

(2) Putting a DLL on the Module Was Not a Viable Alternative.

1091. Professor Jacob's proposed alternative of putting the DLL on the module involves putting an additional chip on the module containing either one or more DLL circuits rather than having a DLL on each individual DRAM. (Jacob, Tr. 5448-49).

1092. Complaint Counsel did not meet their burden of showing that putting a DLL on the module was a viable alternative to on-chip DLL in DDR SDRAMs.

1093. To the contrary, the evidence in the record shows that putting a DLL on the module was not a viable alternative to on-chip DLL in DDR SDRAMs, because it would be significantly costlier and difficult to implement.

1094. At high speeds, a single DLL would be insufficient and a separate DLL would be required for each DRAM on the module. (Jacob, Tr. 5449; Soderman, Tr. 9406-07).

1095. Professor Jacob's suggestion that multiple DLLs be put on a single chip would not solve the problem. A DLL on the DRAM could sense the DRAM's performance in order to compensate for timing uncertainties, while a DLL on a chip outside the DRAM would require significant extra circuitry on the DRAM to communicate with the DLL chip about the DRAMs performance. (Soderman, Tr. 9407). Such circuitry would be difficult and expensive to implement and would require extra traces on the module which would further increase the cost of the system. (Soderman, Tr. 9407-08).

1096. Tom Landgraf of Cisco, formerly at Hewlett-Packard, testified that Hewlett-Packard was in favor of including an on-chip PLL or DLL in the DDR SDRAM standard because putting a PLL on the motherboard or module would have led to lower performance at higher cost. Mr. Landgraf explained:

> "One way to implement PLL is to put it on a – on the system, on the motherboard or on the memory module, and what we were suggesting, what we were in favor of doing was any time you can take a function which is on the motherboard that is common to a memory system, if you can incorporate that in the memory system itself, it reduces the overall cost of the system and also improves the performance of the system."

(Landgraf, Tr. 1709).

1097. The alternative of putting a DLL on the module would have resulted in increased costs.

1098. The test time at wafer sort would have been decreased because the DLL on the DRAM would no longer have had to be tested. (Geilhufe, Tr. 9612-13).

1099. There would have been an increase in good die yield due to the decrease in critical die area resulting from removal of the DLL from the DRAM. (Geilhufe, Tr. 9613).

1100. The cost of an on-DIMM DLL is a function of the frequencies supported. For the DLL required for DDR SDRAMs, it would have cost approximately $3.80. (Geilhufe, Tr. 9613).

1101. The alternative of putting the DLL on the module would have resulted in the following approximate net costs compared to DDR SDRAM in the late 1990s, assuming a first-tier DRAM manufacturer and a product that is already well down the learning curve with a volume of 20 million units, that is, a product that has already realized its cost improvement: two cent cost decrease due to decreased test time at wafer sort; one cent cost decrease due to increased good die yield; $3.80 per module for an on-DIMM DLL. (Geilhufe, Tr. 9562-64, 9612-14).

1102. These costs would lead to an approximate 21 cent increase in the cost per unit, calculated by converting the fixed costs to per unit costs through division by 20 million (the unit production run), dividing the "per module" costs by 16 corresponding to the number of DRAMs on a DIMM, and adding the resulting per unit fixed costs and per unit variable costs to the other variable costs. (Geilhufe, Tr. 9614). This 21-cent cost increase is a variable cost.

(3) Using a Vernier Method to Account for Skew Was Not a Viable Alternative.

1103. Professor Jacob proposed using a "vernier method" to "account for skew," that is timing uncertainties. (Jacob, Tr. 5444). A "vernier" is a circuit that provides a static delay, that is, it is a variable delay circuit that does not contain a feedback loop like a DLL for changing the size of the delay. (Jacob, Tr. 5450; Soderman, Tr. 9411).

1104. Complaint Counsel did not meet their burden of showing that using a vernier method was a viable alternative to on-chip DLL in DDR SDRAMs.

1105. To the contrary, the evidence in the record shows that using a vernier method was not a viable alternative to on-chip DLL in DDR SDRAMs, because it would not be sufficient for high speed performance. Moreover, using a vernier method is not free of patent coverage.

1106. Unlike a DLL, Professor Jacob's proposed alternative of using a vernier method to account for skew would not account for dynamic changes in skew caused by, for example, fluctuations in temperature or voltage without recalibration, that is adjustment of the amount of the delay, by the memory controller. (Jacob, Tr. 5452-53).

1107. These temperature and voltage changes can occur on the order of milliseconds and microseconds, respectively, and without the DLL's feedback loop the vernier will not be able to take these fluctuations into account and minimize the timing uncertainty. (Soderman, Tr. 9411-12).

1108. Moreover, the recalibration necessary to make the vernier more precise would consume bus bandwidth, because the recalibration information would have to be transmitted over the bus from the controller to the DRAM, and would make the system less efficient. (Soderman, Tr. 9412).

1109. The SyncLink consortium tried to design a chip, called an "SLDRAM," using verniers alone without PLLs or DLLs on the DRAM. (RX 2099-43 at 158; Soderman, Tr. 9412-14).

1110. Ultimately, however, SyncLink's SLDRAM chip did use a DLL in each DRAM, in addition to the vernier, in order "to make that timing a little bit more accurate." (Jacob, Tr. 5620-21; RX 2099-11; Soderman, Tr. 9414-15).

1111. In addition, the use of verniers is covered by U.S. Patent no. 6,115,318, "Clock Vernier Adjustment" assigned to Micron Technology (RX 1701), and as used in SLDRAM by U.S. Patent no. 5,917,760, "Deskewing Data Signals in a Memory System, assigned to SLDRAM, Inc. (RX 1479). Professor Jacob did not consider these patents when he proposed the use of verniers as an alternative. (Jacob, Tr. 5622-23).

(4) Increasing the Number of Pins on the DRAM Was Not a Viable Alternative.

1112. Professor Jacob's proposed alternative of achieving high bandwidth using more DRAM pins and not clock frequency is the same as the alternative he proposed of using more pins per DRAM rather than using dual-edge clocking. (Jacob, Tr. 5453-54).

1113. This alternative suffers from the same infirmities and the same additional costs as the same alternative when it was proposed as an alternative for dual-edge clocking. (Geilhufe, Tr. 9612).

1114. Professor McAfee did not testify that this was a commercially viable alternative. (McAfee, Tr. 7385).

(5) Relying on the DQS Data Strobe Was Not a Viable Alternative.

1115. Professor Jacob's proposed alternative of relying on the DQS data strobe involves using the DQS signal that already exists in DDR SDRAMs to time the data which would no longer necessarily be aligned with the system clock. (Jacob, Tr. 5456-57).

1116. Complaint Counsel did not meet their burden of showing that relying on the DQS data strobe was a viable alternative to on-chip DLL in DDR SDRAMs.

1117. To the contrary, the evidence in the record shows that relying on the DQS data strobe was not a viable alternative to on-chip DLL in DDR SDRAMs, because it would not be sufficient for high speed performance.

1118. Using the DQS signal without the DLL is not sufficient for high speed performance. (Soderman, Tr. 9415-16).

1119. DDR SDRAMs already have the DQS signal available, but DDR SDRAMs also contain a DLL for accurate operation, even though DRAM manufacturers incur a cost to put the DLL on the DRAM. (Soderman, Tr. 9416-17).

1120. DDR2 SDRAMs have DQS data strobe signals as well as on-chip DLLs, even though DRAM manufacturers incur a cost to put the DLL on the DRAM. (RX 2099-14 at 3; RX 2099-39 at 5, 7).

c. There Is Evidence That Some of Complaint Counsel's Proposed Alternatives to Dual-Edge Clocking and On-Chip DLL Would Infringe Rambus Patents.

1121. Rambus has come forward with a number of patents that it contends cover certain of the alternatives to dual-edge clocking and on-chip DLL proposed by Complaint Counsel through their technical expert, Professor Jacob. In particular, as set forth above, there is evidence to support Rambus's contention that the alternative of interleaving on-chip banks is covered by Rambus's '105 patents. Findings ¶¶ 996-998.

1122. Likewise, there is evidence to support Rambus's contention that Professor Jacob's proposed alternative of using a vernier method to remove skew is covered by certain Micron and SLDRAM patents. *See* Findings ¶ 1111.

1123. As discussed above, Professor Jacob did not consider these, or any other, patents in his investigation of these proposed alternatives, but Professor McAfee based his conclusions of commercial viability on the assumption that the alternatives were unencumbered by patents. *See* Findings ¶¶ 999, 1111.

1124. Complaint Counsel has introduced no evidence that the patents raised by Rambus do not cover certain of the proposed alternatives. Even with his assumption of no patent coverage, Professor McAfee could not testify that the alternative of interleaving on-

chip banks was commercially viable. As for Professor McAfee's opinion that using a vernier method was commercially viable, this opinion is based on the incorrect assumption that this alternative is not encumbered by patents. It follows that Professor McAfee's opinions in this regard is entitled to no weight.

d. Given The Cost-Performance Differences, Economically Rational DRAM Manufacturers Would Have Adopted And Licensed The Rambus Technologies Incorporated In DDR.

1125. JEDEC-compliant DDR parts use all four of the Rambus technologies at issue: programmable CAS latency, programmable burst length, dual-edge clocking, and on-chip PLL/DLL. In order to determine whether the use of alternatives to these Rambus technologies used in DDR is more costly than paying the Rambus royalties, one can determine the additional incremental costs associated with the alternatives and compare that to the Rambus royalties that would be paid to Rambus under a license from Rambus. (Rapp, Tr. 9850-54). Costs for alternatives to different features are additive; that is, to calculate the costs associated with implementing alternatives to more than one feature simultaneously, one would simply add the costs associated with the individual alternatives. (Geilhufe, Tr. 9614).

1126. To make this comparison, the total additional incremental costs of alternatives are summed and divided by the weighted average of the actual and forecast selling price ("ASP") of DDR for the period 2000 to 2006. (Rapp, Tr. 9844-45, 9850-54). For DDR, the ASP is $5.13. (Rapp, Tr. 9844-45).

1127. The Rambus royalty rate for the use of its technologies in DDR is 3.5%. (Rapp, Tr. 9853).

1128. The same additional incremental costs and performance disadvantages that apply to the alternatives to programmable CAS latency and programmable burst length as used in SDRAM also apply to the use of those alternatives in DDR. (Rapp, Tr. 9842-43).

1129. The alternatives for dual-edge clocking identified as "commercially viable" by Complaint Counsel's economic expert were: interleaving banks on the module, doubling the clock frequency, and the use of toggle mode. (Rapp, Tr. 9841; McAfee, Tr. 7380-81).

1130. The total additional incremental cost associated with the use of the alternative of interleaving banks on a module is $0.25 per part, which is the additional incremental cost associated with board complexity. (Rapp, Tr. 9844). As a percentage of ASP, this total additional incremental cost is 4.88%. (Rapp, Tr. 9844-45). These numbers are illustrated in DX313.

1131. The total additional incremental cost associated with the use of the alternative of doubling the clock frequency is $0.28 per part. (Rapp, Tr. 9845-46). This total consists of the following additional incremental costs per part: a $0.04 final test and good yield cost increase and a $0.24 circuit board area cost increase. (Rapp, Tr. 9845-46). As a percentage of ASP, this total additional incremental cost is 5.46%%. (Rapp, Tr. 9846). These numbers are illustrated in DX313.

1132. These two technologies also have performance disadvantages when compared to Rambus's dual-edge clocking technology. (Rapp, Tr. 9846-48). These disadvantages are summarized in DX314.

1133. The final alternative, toggle mode, is an asynchronous technology that is not technically viable. (Rapp, Tr. 9841, 9856-57).

1134. The alternatives for on-chip PLL/DLL identified as "commercially viable" by Complaint Counsel's economic expert were: the use of a vernier mechanism, placing the DLL on the module, and relying on the DQS data strobe. (Rapp, Tr. 9841-42). Each of these alternative has performance disadvantages when compared to Rambus's on-chip PLL/DLL technology. (Rapp, Tr. 9848-50). (These disadvantages are summarized in DX 315).

1135. The most costly alternatives to the four specified Rambus technologies that are used in JEDEC-compliant DDR that are not covered by Rambus's patents are the use of fuses to set latency, the use of fixed burst length, any on-chip PLL/DLL alternative, and doubling the clock frequency. (Rapp, Tr. 9850-52). The total additional cost of using these four alternatives is $0.36 per part. (Rapp, Tr. 9852). As a percentage of ASP, this additional cost is 7.02%, which exceeds the 3.5% Rambus royalty rate by a substantial margin. (Rapp, Tr. 9853). (These numbers are illustrated in DX 316).

1136. The least costly alternatives to the four specified Rambus technologies that are used in JEDEC-compliant DDR that are not covered by Rambus's patents are the use

of fixed latency, the use of a burst terminate command, any on-chip PLL/DLL alternative, and interleaving banks on a module. (Rapp, Tr. 9850-52). The total additional cost of using these four alternatives is $0.29 per part. (Rapp, Tr. 9852). As a percentage of ASP, this additional cost is 5.65%, which exceeds the 3.5% Rambus royalty rate by a substantial margin. (Rapp, Tr. 9853). (These numbers are illustrated in DX 316).

1137. In order to determine what royalty a rational decision-maker would have expected Rambus to charge (in the absence of direct knowledge), the standard assumption and methodology in economics is to assume that the royalty rate actually charged is the best estimate of the royalty rate a decision-maker would have expected at an earlier time. (Rapp, Tr. 10207-09). Similarly, the standard assumption and methodology in economics is to assume that the actual weighted average selling price over the product life cycle is the best estimate of an ASP that a decision-maker would have predicted in advance. (Rapp, Tr. 10212-13). Using the standard assumptions and methodology in economics, a rational DRAM manufacturer or group of manufacturers would have expected the additional costs of any alternatives to outweigh the costs of Rambus's royalties.

1138. Based on these cost calculations and in consideration of the performance advantages of the four Rambus technologies incorporated in DDR, it is clear that Rambus's technologies were superior in cost-performance terms. (Rapp, Tr. 9857-58). A rational manufacturer or group of manufacturers in JEDEC would have chosen to take a license from Rambus at 3.5% for DDR rather than use any combination of the alternatives

identified by Complaint Counsel's economic expert as "commercially viable" that are not covered by Rambus's patents. (Rapp, Tr. 9857-59).

1139. Although DRAM manufacturing costs decline over time, this does not affect the additional incremental costs used for purposes of the calculations with regard to alternative technologies for either SDRAM or DDR because these costs were estimated for a mature product. (Rapp, Tr. 9854). Moreover, some of the estimated costs, such as inventory costs, are not subject to a decline over time because the decline in costs in the DRAM industry come from improvements in manufacturing technology and increased yields. (Rapp, Tr. 9854-55).

1140. Complaint Counsel's technical expert did not provide any cost information that was useful for economic analysis because he provided no cost numbers. (Rapp, Tr. 9855-56). Economists cannot make useful statements about cost comparisons without some sort of a numerical calculation or comparison. (Rapp, Tr. 9856).

5. Rambus Also Has Patents Outside the '898 Family That Cover DDR SDRAMs.

1141. Even if Rambus were unable to enforce patents in the '898 family, it would still have patents, outside the '898 family, that cover DDR SDRAMs.

a. Rambus's '405 Patent Covers DDR SDRAMs.

1142. The '405 patent issued on October 22, 2002 and claims priority to an application filed on October 19, 1995. (RX 2122-15 at 1; Fliesler, Tr. 8877-78). However, Claim 1 of the patent was not filed until May 29, 2001. (Fliesler, Tr. 8880).

1143. Claim 1 of the '405 patent reads on the JEDEC DDR SDRAM standard. (RX 2122-15 at 45; Fliesler, Tr. 8879). Claim 1 of the patent contains precharge and strobe signal limitations that correspond to features of the DDR SDRAM standard. (RX 2122-15 at 45; CX 234 at 151, 164; JX 57 at 30; Fliesler, Tr. 8879).

b. Rambus's '353 Patent Covers DDR SDRAM.

1144. The Court has taken official notice of United States Patent No. 6,591,353 which issued on July 8, 2003 and is assigned to Rambus.

1145. Claim 1 of the '353 patent claims:

> "A method of operations of in a memory device that includes a plurality of memory cells, the method comprising:
>
> receiving a command to sample data;
>
> deferring sampling a first portion of the data until an external strobe signal is detected; and
>
> sampling the first portion of the data from an external signal line in response to detecting the external strobe signal."

1146. DDR SDRAMs are memory devices that include a plurality of memory cells. DDR SDRAMs receive commands to sample data (namely, write commands). DDR SDRAMs sample data from an external signal line (the bus) only when an external strobe signal (the DQS data strobe) is detected. (CX 234 at 164; JX 57 at 30). As JEDEC standard JESD79 for DDR SDRAMs states: "WRITE bursts are initiated with a WRITE command. . . . During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS." (JX 57 at 30).

D. Even Assuming That Alternatives Did Exist, JEDEC Would Not Have Rejected The Rambus Technologies.

1147. A wholly independent means to determine whether JEDEC would have adopted alternatives to Rambus's SDRAM and DDR technologies had Rambus made the additional disclosures that Complaint Counsel allege should have been made is to examine JEDEC's and Rambus's likely behavior in a but-for world.

1148. Rambus offered the testimony of Professor David Teece regarding this decision analysis. He is very well qualified to opine on this issue.

1149. Professor Teece has a Master's degree in economics from the University of Canterbury, a Master's degree in economics from the University of Pennsylvania, and a Ph.D. in economics from the University of Pennsylvania. (Teece, Tr. 10297). The subject of his Ph.D. thesis was the resource costs of transferring technology between nations and amongst firms. (Teece, Tr. 10297). The thesis was published as a book, and two peer-reviewed articles came from it. (Teece, Tr. 10297). Professor Teece has over 150 publications and over a dozen books. (Teece, Tr. 10298).

1150. Professor Teece is a chaired professor in the School of Business at the University of California at Berkeley. (Teece, Tr. 10295). He is also the Director of the Institute for Management, Innovation, and Organization at the University of California at Berkeley. (Teece, Tr. 10295). The Institute conducts research into questions of innovation, technology policy, and technology strategy. (Teece, Tr. 10295). The Institute has conducted a lengthy multi-country study of the global semiconductor industry. (Teece,

Tr. 10295-96).

1151. Professor Teece has taught a number of courses over the years, including (with regularity) a Master's level course on management innovation and a Ph.D. seminar on technology strategy and related public policy issues. (Teece, Tr. 10296-97). In addition to teaching at Berkeley, Professor Teece has taught at the University of Pennsylvania, Stanford University, and Oxford University. (Teece, Tr. 10296). He was recently invited to give the Clarendon Lectures in the Business Economics at Oxford University. (Teece, Tr. 10296).

1152. Professor Teece has received the first international prize in technology strategy and he has been named one of the 50 most important business thinkers of our time. (Teece, Tr. 10298-99).

1153. Professor Teece co-founded a journal entitled Industrial and Corporate Change, published by Oxford University Press, which focuses on technology management, technology policy, and the economics of innovation. (Teece, Tr. 10299). He has also refereed several peer-reviewed journals. (Teece, Tr. 10299-300).

1154. Professor Teece's specialization within the field of industrial organization is in technology policy and particularly antitrust policy as it relates to high technology industries. (Teece, Tr. 10300). In the last 15 to 20 years, he has written numerous articles on technology strategy and on the interface of technology policy and antitrust policy. (Teece, Tr. 10300).

1155. Professor Teece also has substantial expertise in the area of the economics of standard-setting. He began to study the economics of standard-setting organizations about a decade ago. (Teece, Tr. 10300-01). He was invited to speak twice at the joint FTC/DOJ hearings on the subject of standard-setting and antitrust. (Teece, Tr. 10301).

1156. In contrast, Complaint Counsel's economic expert has never published a single paper on the issue of standard-setting. (McAfee, Tr. 11345). He was not invited to speak at the joint FTC and DOJ hearings. (McAfee, Tr. 11345). He has never been invited to speak on the issue of standard-setting. (McAfee, Tr. 11345).

1157. The but-for world may be analyzed by the use of a decision tree, which is a device commonly used in economics to understand the different possible scenarios and outcomes in a "but-for" world. (Teece, Tr. 10315-16). In this case, the decision tree starts with the but-for world assumption that Rambus made the additional disclosures that Compliant Counsel allege it should have made. (Teece, Tr. 10316). (A demonstrative exhibit that shows the decision tree – for illustration purposes, not as evidence – was marked as DX 332).

1158. The decision tree may be described as follows. Had Rambus made these additional disclosures, JEDEC would have a choice; it could either proceed without seeking a RAND letter from Rambus, or it could ask Rambus to provide a RAND letter. (Teece, Tr. 10316). Had JEDEC proceeded without asking for a RAND letter, the same outcome would have occurred in the but-for world as in the actual world – JEDEC would

have adopted standards incorporating Rambus's technologies. (Teece, Tr. 10329-30). If JEDEC had asked for a RAND letter, Rambus would have to decide whether to give a RAND letter. (Teece, Tr. 10317). If Rambus agreed to give a RAND letter, JEDEC members would (as a theoretical matter) have sought to negotiate licenses from Rambus before the standard was adopted and before any relevant patents issued (*ex ante*) or it could have proceeded without such negotiations. (Teece, Tr. 10317-18). If there were no *ex ante* negotiations, JEDEC could have adopted the standards incorporating Rambus's technologies or it could have adopted different standards. (Teece, Tr. 10319). Had JEDEC adopted the same standards as it actually adopted, the same outcome would have occurred in the but-for world as in the actual world. (Teece, Tr. 10319).

1. Had Rambus Made The Disclosures Described By Complaint Counsel, JEDEC Might Have Proceeded Without Seeking a RAND Assurance from Rambus.

1159. As a matter of economic analysis, there are a number of considerations that suggest JEDEC might not have asked Rambus for a RAND letter, even if Rambus had made all of the disclosures described by Complaint Counsel. First, JEDEC might have perceived that Rambus was trying to derail the standard-setting process by gaming the system. (Teece, Tr. 10320-22). That is, JEDEC might have believed that Rambus was asserting that it had patent rights in order to provoke JEDEC into seeking a RAND letter so that Rambus could refuse to give the letter and thereby stopping or slowing the standardization process. (Teece, Tr. 10320-22).

1160. Second, JEDEC might not have asked for a RAND letter because it might have believed that Rambus would not obtain patents that would cover products complying with the JEDEC standard. (Teece, Tr. 10323). For example, JEDEC might have believed that Rambus's patent applications would not result in issued patents or that, if they did, the patents might not be valid because of prior art. (Teece, Tr. 10323).

1161. Third, JEDEC might not have asked for a RAND letter from Rambus because, in the real world, JEDEC did not seek, and to this day has not sought, a RAND assurance from Rambus regarding SDRAM, DDR or DDR2 despite JEDEC's knowledge of and concerns about Rambus's patent coverage. (Teece, Tr. 10323-27).

1162. JEDEC's failure to seek a RAND letter from Rambus is not explained by speculation that JEDEC *may* have chosen not to ask for a RAND letter -- after Rambus began asserting its issued patents against DRAM manufacturers -- because of litigation between Rambus and the DRAM manufacturers. (Teece, Tr. 10328-29). This argument is inconsistent with JEDEC's real world behavior. In the real world, JEDEC sought a RAND letter from Texas Instruments regarding the Quad-CAS technology even though TI was in litigation with Micron at the time. (Teece, Tr. 10329; CX 348 at 2, 4).

1163. Had Rambus made the additional disclosures that Complaint Counsel contend it should have made and had JEDEC not sought a RAND letter, economic analysis shows that JEDEC would have adopted the same standards that it did in the real world - the standards incorporating Rambus's technology. (Teece, Tr. 10329-30). Complaint

Counsel's economic expert conceded this to be true; he testified that had JEDEC not sought a RAND letter, "it would lead to the same outcome as the actual world." (McAfee, Tr. 11308). In that event, the alleged failure to disclose had no anticompetitive effect. (Teece, Tr. 10320).

1164. While Complaint Counsel's economic expert testified that JEDEC would not have adopted Rambus's technologies, he based his opinions on the assumption that if JEDEC were informed of a patented technology, it would not proceed to adopt that technology into a standard without first requesting a RAND assurance. (McAfee, Tr. 7672). Complaint Counsel's economic expert made no study of JEDEC behavior in arriving at this assumption.

1165. Complaint Counsel's economic expert also admitted that if JEDEC was aware of patents that applied to SDRAM and not to previous generations of DRAM, and if JEDEC went forward with SDRAM without requesting a RAND letter, that would impact his assumption that JEDEC requires a RAND letter and therefore impact his opinions that rely on that assumption. (McAfee, Tr. 7708). As discussed above, JEDEC did go forward with the SDRAM standard despite knowing of applicable patents and without seeking RAND letters. As Complaint Counsel's expert testified it would, this evidence casts doubt on the validity of his assumption that a RAND letter was required in all circumstances.

1166. There was, in addition, an example in the 1995-1996 time frame where a RAND letter was *not* requested by an EIA standards body despite an assertion by an EIA

member that it possessed a patent relating to the standard. In that case, an EIA member called Echelon gave notice to an EIA standards body, the Consumer Electronics Association ("CEA") that it had an issued patent that might cover a technology included in a CEA standards proposal. As discussed below, the EIA body chose not to ask for RAND assurances. (Kelly, Tr. 2122-3).

1167. Echelon was a participant in the standards-setting process that had voted against the proposed standard. Echelon was promoting its own technology in competition with certain technology included in the standard. (Kelly, Tr. 2122).

1168. EIA General Counsel John Kelly was personally involved in the Echelon situation. He testified that RAND assurances were not sought from Echelon because "it appeared to us at the time . . . that Echelon was deliberately trying to impede the process, to stall it out for its own purposes . . . ." (Kelly, Tr. 2135).

1169. Mr. Kelly testified that after Echelon asserted that it had a patent related to the standard, it tried to insist that the EIA request a RAND assurance from it under the EIA Patent Policy. (Kelly, Tr. 2166-7).

1170. Mr. Kelly believed that Echelon was asserting its intellectual property claims, and insisting upon receiving a request for RAND assurances, in a bad faith effort "to block the process" of standardization. (Kelly, Tr. 2167). Mr. Kelly also believed that it was "reasonably clear" that "we weren't going to get those licensing assurances" from Echelon. (Kelly, Tr. 2166-7). Mr. Kelly believed that if a request for RAND assurances

was made to Echelon, Echelon would refuse to give those assurances, and the standardization process would necessarily come to a stop. (Kelly, Tr. 2165-7).

1171. The Echelon case thus provides useful insights into how JEDEC may have reacted if Rambus had announced that its patent applications might relate to features under consideration for inclusion in the SDRAM or subsequent standards. The evidence shows that: (1) Rambus, like Echelon, was promoting its own memory device in competition with the JEDEC standard device; (2) on the three occasions when Rambus's potential intellectual property interests were explicitly discussed at JEDEC meetings while Rambus was a member, JEDEC representatives expressed the view that Rambus's patents, if they issued, would be barred by prior art; (3) similar views about prior art were aired on the occasions when Rambus's potential intellectual property interests were raised at SyncLink meetings and at JEDEC meetings after Rambus left JEDEC; and (4) the chair of the SyncLink standards committee believed that Rambus was trying to "torpedo" the SyncLink standard by asserting invalid IP claims. In light of this evidence, there is a strong possibility that the JC 42.3 committee would have believed that Rambus, like Echelon, was trying to trigger a request for RAND assurances, which assurances it would then decline to give, in the hopes of using its intellectual property disclosures to bring the SDRAM or DDR SDRAM standardization process to a halt.

1172. The concern that standard-setting organizations could be gamed in this manner was shared by others in the industry. For example, SyncLink Consortium Secretary David Gustavson testified that he was concerned about the issue:

> "My concern was that any person who wished to block a standard could simply assert that they had patents applied for which would interfere with that standard, and if they refused to say that they would make their patents available on a nondiscriminatory basis to others it would be impossible for the standard to complete. In my view it would make it possible for every standard in the IEEE to be blocked by a single individual."

(Gustavson, Tr. 9296). Dr. Gustavson expressed this same concern in an email to the IEEE. (RX 675 at 1 (complaining that the IEEE patent policy would allow a party to assert that it has a patent claim that would be infringed, block the standard, and the policy does not allow the IEEE to ensure the validity of the claim)). In fact, Dr. Gustavson believed that this situation occurred when Rambus claimed it had patent applications covering RamLink. (Gustavson, Tr. 9297).

1173. Additional evidence on this point comes from the reactions of Micron's JEDEC representatives in April 1997, when they learned from Micron's Intel account representative that "Rambus plans legal action to request royalties on all DDR memory efforts." (RX 920 at 2).

1174. It appears that neither Mr. Ryan, Mr. Lee nor Mr. Walther, each of whom received this e-mail and each of whom attended JEDEC meetings on behalf of Micron,

ever notified JEDEC about the information they had learned regarding Rambus's plans. (Lee, Tr. 6972-3).

1175. Mr. Walther responded to the information in part by saying that he thought that "changing data on both edges of the clock" was "old technology." (RX 920 at 1).

1176. Mr. Lee testified that he ignored the information about Rambus's plans "to request royalties on all DDR memory efforts" because he did not "believe this was true." (Lee, Tr. 6981). Instead, he believed that Rambus was trying to spread "misinformation." (Lee, Tr. 6983). As Lee explained, his "thought process was that they were trying to get Intel locked into designing RDRAM in on everything, direct RDRAM, and to try to tell [Intel] they had no other alternative, that they've eliminated all of their competition. . . ." (Lee, Tr. 6982-3).

1177. Mr. Lee testified that "it was consistent with [Rambus's] prior behavior that they might tell Intel, 'Oh, we have patents on that, so you can't use DDR. . . .'" (Lee, Tr. 6983).

1178. In other words, Mr. Lee believed that Rambus was doing exactly what Mr. Kelly thought Echelon had been doing – asserting intellectual property claims over a competing technology in the hopes of slowing or preventing its marketplace acceptance.

1179. Complaint Counsel's economic expert did not refute the evidence that JEDEC might have proceeded without seeking a RAND letter. In fact, he testified that if JEDEC determines that the technology is not patented, JEDEC may proceed without

requesting a RAND letter or RAND assurance even if someone asserts that the technology is covered by a valid patent. (McAfee, Tr. 7676-77).

1180. Complaint Counsel's economic expert further conceded that if, in the but for world in which Rambus made the additional disclosures that Complaint Counsel allege should have been made, JEDEC had determined that the Rambus technology it sought to include into a standard would not be patented, JEDEC might not have requested a RAND letter. (McAfee, Tr. 7678).

1181. Complaint Counsel's economic expert also admitted that he did not consider the possibility that had Rambus made the additional disclosures that Complaint Counsel allege should have been made, JEDEC might have proceeded to incorporate the technology without requiring a RAND letter. (McAfee, Tr. 7680-81). Although Professor McAfee said in his rebuttal testimony that he did not think that there was a significant possibility that JEDEC would not have asked for a RAND letter (McAfee, Tr. 11308), he *also* testified that if JEDEC thought that it was being "gamed" by Rambus, and if JEDEC thought that Rambus was unlikely to obtain patent coverage, it was a "logical possibility" that JEDEC would *not* ask for a RAND letter and would proceed to incorporate in its standards the technologies at issue. (McAfee, Tr. 11331).

1182. As noted above, the Echelon case, and the reactions by Mr. Lee, Mr. Wiggers and others when they learned of Rambus's intellectual property claims, make this scenario far more than just a "logical possibility."

2. If JEDEC Had Sought A RAND Assurance, It Would Still Have Adopted Rambus's Technologies.

1183. If JEDEC would have requested a RAND letter from Rambus, Rambus would have given the RAND assurance and JEDEC would have proceeded to adopt Rambus's SDRAM and DDR technologies.

a. Rambus Would Have Given a RAND Assurance.

1184. A RAND letter must state that the patent holder will license its patent either royalty free or on reasonable terms and conditions that are demonstrably free of any unfair competition; in the latter case the royalty rate is not specified in the letter. (Teece, Tr. 10331-32; JX 54 at 9; CX 203A at 11). In this case, given Rambus's business model, an economist would not expect Rambus to agree to license its technology royalty free. (Teece, Tr. 10314, 10331-32; McAfee, Tr.7492-93).

1185. To determine whether Rambus would have provided a RAND letter, it is useful to examine the economic implications of that action.

1186. A RAND assurance has three key provisions, each of which has economic implications for the patent holder. (Teece, Tr. 10333).

1187. The first provision is that the patent holder must make licenses available to all interested parties. (Teece, Tr. 10333). This provision means that the patent holder gives up the right to pick and choose to whom it will license. (Teece, Tr. 10334). There is, however, a substantial economic motivation for a patent holder to agree to this provision. Agreeing to the provision makes it likely that firms will be willing to

incorporate the patented technology because they are assured of not being frozen out. (Teece, Tr. 10334). The patent holder is therefore likely to receive royalties that it otherwise would not receive. (Teece, Tr. 10334-35). The economic literature teaches that patent holders may be willing to agree to this type of restriction because doing so gives confidence to the licensees that they can use the patent holder's technology and be competitive in the marketplace. (Teece, Tr. 10335).

1188. The second provision of a RAND assurance is that the licensor agrees to license on reasonable terms and conditions. (Teece, Tr. 10336). This provision prevents the patent holder from charging unreasonable terms. (Teece, Tr. 10336). This commitment assures the licensees that royalties will not be unreasonable, again making them more likely to adopt the patentee's technology. (Teece, Tr. 10336). A patentee therefore has an economic incentive to agree to this provision. (Teece, Tr. 10337-38).

1189. In economic terms, reasonable terms and conditions means that the royalty rates are not so high as to negate the offer to license. (Teece, Tr. 10336-37). For example, if the rate is so high that it would put the licensee out of business, the rate is not reasonable. (Teece, Tr. 10337).

1190. Reasonable terms and conditions are understood to mean, as they are in the *Georgia Pacific* analysis in patent damages cases, terms to which a willing buyer and a willing seller would agree. (Teece, Tr. 10337).

1191. The third provision of a RAND assurance is that the license be demonstrably free of any unfair discrimination. (Teece, Tr. 10338). This provision prevents arbitrary pricing differences among different licensees; it is designed to create a level playing field. (Teece, Tr. 10338). Again, this commitment is often attractive for a patent holder because it makes it more likely that licensees will adopt the patented technology, leading to royalties for the patentee. (Teece, Tr. 10338).

1192. From an economic perspective, licensees would be most concerned about the third provision - that licenses be demonstrably free of any unfair discrimination. (Teece, Tr. 10339). A level playing field is more important to firms than the level of royalties because non-discriminatory licenses mean that the firm is not competitively disadvantaged. (Teece, Tr. 10320).

1193. Economic analysis leads to the conclusion that if JEDEC had asked Rambus to provide a RAND letter, Rambus would have provided such a commitment. (Teece, Tr. 10340-41). First, in the but-for world in which Rambus makes the additional disclosures Complaint Counsel contends should have been made, Rambus would have already lost any benefits of keeping that information confidential. (Teece, Tr. 10344). Agreeing to give a RAND assurance at that point therefore involves less of a sacrifice. (Teece, Tr. 10344).

1194. Second, in Complaint Counsel's "but-for world," where commercially feasible alternatives to Rambus's technologies exist, Rambus would have been confronted

with the choice of giving a RAND letter and obtaining royalties or potentially seeing its technologies excluded from the standard and not receiving royalties. (Teece, Tr. 10344-45). Rambus never had to make that choice in the real world. Rambus is a pure-play licensing company. That is, Rambus does not manufacture DRAM, but rather uses research and development to invent new DRAM technologies and makes its money by licensing its technology to others. (Teece, Tr. 10350-51). If Rambus does not license, it goes out of business. (Teece, Tr. 10341). Rambus therefore has an economic incentive to agree to terms that make it possible for it to license its technology. (Teece, Tr. 10341). If it does not give a RAND assurance, it forces JEDEC to look at alternative technologies. (Teece, Tr. 10345). But given Rambus's business model, it does not want JEDEC to look at alternatives; it wants JEDEC to adopt its technologies so that it can obtain royalties. (Teece, Tr. 10345).

1195. This incentive is especially great if there are in fact alternatives to Rambus's technologies. (Teece, Tr. 10341-42). If there were good alternatives to Rambus's technologies, Rambus would clearly have given a RAND assurance because refusing to do so would have cost it the opportunity to get significant revenue from licensing. (Teece, Tr. 10343). In that situation, it would have been economically irrational for Rambus to refuse to give a RAND letter. (Teece, Tr. 10345).

1196. This conclusion is consistent with the views of Complaint Counsel's economic expert. First, he admitted that his starting point would be that whatever

information was known to JEDEC about alternative would be known to Rambus. (McAfee, Tr. 7729). Second, he admitted that one of the risks that Rambus would face if it chose not to give a RAND letter in the but-for world would have been that JEDEC would adopt a non-infringing alternative. (McAfee, Tr. 7729).

1197. The conclusion that Rambus would have given a RAND letter is not affected by speculation that Rambus might have gained some marketplace benefit for RDRAM by refusing to give a RAND assurance. (Teece, Tr. 10345-46). Especially if there were alternatives to Rambus's technologies, any benefit to Rambus's goal of increasing the acceptance and sales of RDRAM that might flow from a refusal to give a RAND assurance for SDRAM and/or DDR would be minimal or nonexistent. (Teece, Tr. 10346). Moreover, giving a RAND assurance would lead to royalties in hand for Rambus rather than a mere potential benefit to RDRAM. (Teece, Tr. 10739-40).

1198. Finally, the conclusion that Rambus would have issued a RAND letter if asked is bolstered by the fact that the DRAM industry exhibits fairly rapid technological change. (Teece, Tr. 10346-47). Rambus is a "repeat player"; that is, its business model is such that it will often be engaging in licensing in the DRAM industry as it develops new technologies. (Teece, Tr. 10346-47). Rambus therefore has an incentive to behave in a reasonable and cooperative manner because it is building an ongoing technology company (Teece, Tr. 10347), and it therefore has incentive to give a RAND letter because it wants to build relationships with the licensees for the future. (Teece, Tr. 10740-41).

1199. Evidence that Rambus was concerned about agreeing to a RAND policy does not change this conclusion. First, in the but-for world, unlike the real world, Rambus has already disclosed its trade secrets. (Teece, Tr. 10716).

1200. Second, evidence that Rambus might have been reluctant in the actual world to give a RAND letter is affected by the fact that Rambus had apparently misunderstood what a JEDEC RAND assurance required. Had Rambus been confronted with a request from JEDEC to provide a RAND letter, it would have had an incentive to seek to determine what that commitment entailed. (Teece, Tr. 10716-17).

1201. This conclusion is supported by Rambus's conduct in December 1995 – just before Rambus left JEDEC – when Rambus was considering proposing the R-Module technology for standardization at JEDEC. Because Rambus realized that *proposing* a technology at JEDEC might require it to agree to license on RAND terms, Richard Crisp made inquiries about what RAND entailed. (Crisp, Tr. 3479-82). When he did so, Mr. Crisp learned from Mr. Sussman that "reasonable" terms and conditions meant "almost anything we wanted it to mean." (Crisp, Tr. 3480-81; CX 711 at 188). After learning this, Mr. Crisp wrote an e-mail to others at Rambus explaining, "So the conclusion I reach here is that we can abide by the patent policy on a case-by-case basis, are free to set the terms of our license arrangements to what we like (as long as we agree to license all-comers to build our modules), and we give up nothing else in the process." (CX 711 at 188; Crisp,

Tr. 3483). He then concluded that with regard to RAND, the JEDEC policy was not "nearly as onerous as some of us had earlier believed." (CX 711 at 188; Crisp, Tr. 3483).

1202. This evidence shows that (1) Rambus mistakenly believed that the RAND requirements were "onerous" and (2) when motivated to understand the RAND requirement, Rambus made inquiries in that regard. In the but-for analysis, therefore, it is reasonable to conclude that had Rambus been confronted with a request from JEDEC for a RAND letter concerning the technologies incorporated in SDRAM or DDR, it would have sought to understand the details of that commitment and would have dispelled its misunderstandings.

1203. In contrast to this analysis, Complaint Counsel's economic expert admitted that he was unable to determine whether or not Rambus would have given a RAND letter in the but-for world (McAfee, Tr. 7730, 11333), and he admitted that he could not say "one way or the other" if it would have been in Rambus's economic interest to issue a RAND letter in the but-for world. (McAfee, Tr. 7733).

b. <u>There Would Not Have Been Any *Ex Ante* Negotiations</u>.

1204. Complaint Counsel's economic expert testified that once Rambus issued a RAND letter, JEDEC members would have an "incentive" to engage in *ex ante* negotiations, i.e., to negotiate with Rambus prior to the adoption of Rambus's technologies into the SDRAM and DDR standards. (McAfee, Tr. 7493-94). Complaint Counsel's economic expert also testified that if one firm engaged in *ex ante* negotiations with

Rambus, that firm would "report" the royalty rates back to other JEDEC members. (McAfee, Tr. 7494). This analysis, however, is flawed. Firms have incentives to do lots of things that they do not actually do; a proper analysis must take into account all the pertinent factors, including those that would have prevented JEDEC members from asking on any incentive to negotiate *ex ante*. (Teece, Tr. 10353-54). Moreover, any such licensing negotiations would be done under confidentiality agreements (Teece, Tr. 10352-53), and companies would, or should, avoid such an exchange of pricing information because of antitrust concerns.

1205. Here, *ex ante* negotiations would have to have occurred before Rambus's patents issued. Rambus's first patents that covered JEDEC-compliant products issued in mid-1999. *See* Findings ¶ 431.

1206. Despite the opinion expressed by Complaint Counsel's economic expert regarding the likelihood of *ex ante* negotiations involving JEDEC members, there is no evidence of any *ex ante* negotiations occurring in the DRAM industry.

1207. There is also no evidence of *ex ante* negotiations for naked licenses for patent applications outside of the DRAM industry. (Teece, Tr. 10354). Professor Teece, who has studied licensing for over 20 years, did not know of a single example of a negotiation of a naked license for a patent application. (Teece, Tr. 10356, 10360).

1208. There are several economic reasons for the absence of negotiations before patents issue. First, because patent applications are a bundle of rights that has not matured,

the parties do not know for what they are bargaining. (Teece, Tr. 10357). Patent applications often change during the course of prosecution - claims get amended, claims get withdrawn, claims are abandoned - and it is not clear what claims will ultimately issue. (Teece, Tr. 10357-59). There is therefore great uncertainty about the rights that would be negotiated before a patent issues. (Teece, Tr. 10357). In essence, the licensee would buy a "pig in a poke." (Teece, Tr. 10357).

1209. Uncertainty is the foundation for disagreements. (Teece, Tr. 10358-59). Because of the uncertainty about what if any claims in an application will issue, negotiations before patents issue are extraordinarily complex, extraordinarily costly, and in the real world, firms do not engage in this type of negotiations with any frequency. (Teece, Tr. 10357).

1210. Moreover, *ex ante* negotiations for a license regarding patent applications involve confidentiality concerns - the negotiations may be an avenue for the parties to discover each other's intellectual property strategies or information about future inventions. (Teece, Tr. 10359). This provides a disincentive to *ex ante* negotiations of this sort. (Teece, Tr. 10358-59).

1211. Finally, *ex ante* negotiations for a naked license involving patent applications may require claim contingent licensing – agreements on different royalty rates depending on which claims in the application issue – which adds to the complexity and costs. (Teece, Tr. 10359).

1212. The fact that Rambus entered into licenses for RDRAM does not undermine this conclusion. The licenses for RDRAM were not naked patent licenses (licenses that do not include rights other than a right to use the intellectual property). (*See, e.g.,* CX 1592 at 19-21; Teece, Tr. 10355-56) The RDRAM licenses included other provisions such as a technology transfer. *(See, e.g.,* CX 1592 at 19-21; Heye, Tr. 3689-90 (describing circuit design given by Rambus to its licensees that the licensee could "literally drop into our design")).

1213. Because of these costs and disincentives, *ex ante* negotiations for a naked license involving patent applications do not take place either inside or outside the DRAM industry. (Teece, Tr. 10354-10360).

1214. Complaint Counsel's economic expert agreed that *ex ante* negotiations are less likely with respect to a patent application than an issued patent. (McAfee, Tr. 11335). He also agreed that the less certainty there is about the exact scope of a claim and whether or not it would issue, the lower the probability of *ex ante* negotiations. (McAfee, Tr. 11336).

1215. Complaint Counsel's economic expert also admitted that if the potential licensee believed that the pending claims would be invalid or would not issue, it would be less likely to engage in *ex ante* negotiations. (McAfee, Tr. 11336). Here, the evidence shows that JEDEC members believed that Rambus's patents would be invalid or would not issue.

1216. Moreover, according to Complaint Counsel's economic expert, the likelihood of *ex ante* negotiations would be less if Rambus did not have pending claims that actually covered the relevant technologies at the time it gave the RAND letter because, "[i]f nothing else, it makes it harder to describe precisely what is being negotiated about." (McAfee, Tr. 11334-35). As described herein, Rambus did not have any pending claims that actually read on any of the four technologies during the time it was at JEDEC.

1217. In the but-for world, JEDEC members and Rambus would have recognized the costs of negotiating a license regarding patent applications as opposed to patents. (Teece, Tr. 10396). Complaint Counsel's economic expert agreed that JEDEC members might rationally conclude that the costs of *ex ante* negotiations exceed the costs of waiting to negotiate ex post. (McAfee, Tr. 11337).

1218. Complaint Counsel did not meet their burden of establishing that *ex ante* negotiations would have taken place in the but-for world. (Teece, Tr. 10360-61).

c. JEDEC Would Have Adopted Rambus's Inventions With Rambus's RAND Assurance.

1219. Given that Rambus would have given a RAND assurance if asked, there are a number of reasons why JEDEC would have adopted the Rambus technologies. First, as demonstrated above, the alternatives were inferior, even when taking into account Rambus's royalties. (Teece, Tr. 10363, 10365. Second, the theory of revealed preference shows that JEDEC preferred Rambus's technologies. (Teece, Tr. 10365-66). These two

points alone are sufficient to show that JEDEC would have adopted Rambus's technologies for both SDRAM and DDR. (Teece, Tr. 10366).

1220. Third, JEDEC is willing to adopt patented technologies, and it would likely do the same thing with Rambus's technologies. (Teece, Tr. 10371-72). For example, JEDEC adopted the on-chip PLL/DLL technology for DDR knowing that Mosaid had a patent on the technology. (CX 400 at 2).

1221. JEDEC has repeatedly adopted patented technologies so long as it received a RAND letter. Gordon Kelley, a long time chair of JC42.3 testified that he could not recall any instance in which JEDEC pursued alternatives after receiving a RAND commitment on what the committee thought was the best alternative. (Kelley, Tr. 2707-09). By contrast, Mr. Kelley did recall several instances in which all consideration of alternatives was dropped as soon as a RAND assurance was received. (Kelley, Tr. 2707-09).

1222. Similarly, James McGrath, the JEDEC representative for Molex, could not recall a single instance between 1992 and 1996 in which a JEDEC committee changed its course with regard to a standard upon learning of a patent or patent application. (McGrath, Tr. 9243, 9255).

1223. During the period when Rambus attended JEDEC, Desi Rhoden could not recall any example of a JEDEC committee trying to find an alternative technology after a JEDEC member disclosed a patent application that in someway related to the technology being standardized and stated that it would license on RAND terms. (Rhoden, Tr. 628-29).

1224. In fact, the meeting minutes show that the JC 42.3 routinely adopted technologies that had patent issues.

1225. At the May 1990 meeting, JC 42.3 sent a ballot to Council to standardize the 256K x4 MPDRAM technology (JC-42.3-89-48) after receiving a RAND assurance from Digital Equipment Corporation. The minutes state, "This ballot passed but was on hold concerning the patent issue. A patent release letter (see Attachment M) was circulated during the meeting resolving that issue. The ballot will now go to Council." (JX 1 at 6). The "patent release letter" indicated that Digital Equipment Corporation was willing to license the relevant patent for a 1% royalty on sales. (JX 1 at 24).

1226. At the December 1991 JC 42.3 meeting, Siemens disclosed at the time of balloting that it had an issued patent that may cover Extended Data Out for MPDRAM (JC-42.3-91-157). (JX 10 at 9). The committee responded that it was aware of prior art on this patent and unanimously moved to send the ballot to Council assuming the patent issue could be resolved. (JX 10 at 9).

1227. At the July 1992 JC 42.3 meeting, the committee considered a ballot for 2M x8/x9 Sync DRAM in TSOP II (JC 42.3-92-83). (JX 13 at 9). At the meeting, Motorola disclosed an issued patent and provided a letter assuring that Motorola would license the patent on a non-discriminatory basis for a reasonable fee. (JX 13 at 9, 136). The committee agreed that the letter met the EIA requirements, and the committee voted to pass the ballot. (JX 13 at 9-10). The item was given Council ballot number 93-13. (JX 16 at 38). At the

May 1993 JEDEC Council meeting, the Council passed the ballot and standardized the technology. (CX 54 at 8).

1228. At the March 1993 JC 42.3 meeting, the committee voted to pass a ballot on Mode Register Timing (JC-42.3-92-129-1A) for the SDRAM draft specification even though Hitachi commented "patent alert." (JX 15 at 5). At that meeting, the committee voted unanimously to send all SDRAM ballots to JEDEC Council for standardization. (JX 15 at 14). The item was given Council ballot number 93-19. (JX 16 at 39). At the May 1993 JEDEC Council meeting, the Council passed the ballot to standardize this technology. (CX 54 at 9).

1229. At the March 1993 JC 42.3 meeting, the committee considered a ballot for Write Latency (JC-42.3-92-130A) for the SDRAM draft specification. With regard to this ballot, the minutes state that Mosaid raised a patent issue. (JX 15 at 5-6). The minutes also state, "The Committee is aware of the Hitachi patent. It was noted that Motorola has already noted they have a patent. IBM noted that their view has been to ignore patent disclosure rule because their attorneys have advised them that if they do then a listing maybe construed as complete." (JX 15 at 6). The committee voted unanimously to pass this ballot. (JX 15 at 6). At that meeting, the committee voted unanimously to send all SDRAM ballots to JEDEC Council for standardization. (JX 15 at 14). The item was given Council ballot number 93-20. (JX 16 at 38). At the May 1993 JEDEC Council meeting, the Council passed the ballot to standardize this technology. (CX 54 at 9).

1230. At the March 1993 JC 42.3 meeting, the committee considered a ballot for Self-Refresh Entry/Exit (Item 487.09) for the SDRAM draft specification. (JX 15 at 8). The minutes state that both Hitachi and Mosaid raised a "patent alert." (JX 15 at 8). The committee voted unanimously to pass this ballot. (JX 15 at 8). At that meeting, the committee voted unanimously to send all SDRAM ballots to JEDEC Council for standardization. (JX 15 at 14). At the May 1993 JEDEC Council meeting, the Council passed the ballot to standardize this technology. (CX 54 at 10).

1231. At the March 1993 JC 42.3 meeting, the committee considered a ballot for Auto-Refresh (JC-42.3-92-134A) for the SDRAM draft specification. (JX 15 at 8). The minutes state that both Hitachi and Mosaid raised a patent issue. (JX 15 at 8). The committee voted unanimously to pass this ballot. (JX 15 at 9). At that meeting, the committee voted unanimously to send all SDRAM ballots to JEDEC Council for standardization. (JX 15 at 14). The item was given Council ballot number 93-24. (JX 16 at 38). At the May 1993 JEDEC Council meeting, the Council passed the ballot to standardize this technology. (CX 54 at 10).

1232. At the March 1993 JC 42.3 meeting, the committee considered a ballot for DQM Latency Reads/Writes (JC-42.3-92-136A) for the SDRAM draft specification. (JX 15 at 9). The minutes state that both Hitachi and Mosaid raised a "patent concern." (JX 15 at 9). The committee voted unanimously to pass this ballot. (JX 15 at 9). At that meeting, the committee voted unanimously to send all SDRAM ballots to JEDEC Council

for standardization. (JX 15 at 14). This item was given Council ballot number 93-26. (JX 16 at 38). At the May 1993 JEDEC Council meeting, the Council passed the ballot to standardize this technology. (CX 54 at 10).

1233. At the March 1994 JC 42.3 meeting, the committee considered a ballot for SGRAM and SVRAM Special Mode. (JX 19 at 12). Micron voted against the ballot, citing three issued patents held by Texas Instruments that could cover the technology. (JX 19 at 12). Hitachi moved to pass the ballot to Council "provided that TI gives some assurance on the patent." (JX 19 at 12). The committee passed the ballot unanimously. (JX 19 at 12).

1234. At the March 1995 JC 42.3 meeting, the committee considered ballot JC-42.3-95-14 Item 637. (JX 25 at 10). TI raised patent concerns. (JX 25 at 10). The committee nonetheless passed a motion to send the ballot to JEDEC Council. (JX 15 at 10).

1235. At the September 1995 JC 42.3 meeting, the committee considered a ballot for 4M/8M x8 DRAM in 32-pin SOP Item 660. (JX 27 at 7). The minutes state, "The Stacktek patent was discussed. Motion by HP to pass to Council the ballot conditionally on resolution of Stacktek's patent position. . . . Unanimous." (JX 27 at 8). The Council later passed this ballot. (JX 34 at 18).

1236. When TI gave a RAND letter for its Quad-CAS technology (RX 562 at 13), the debate within JEDEC about TI's patents instantly subsided, the issue was resolved, and

the JEDEC committee voted unanimously to remove the hold on the Quad CAS standards and to revoke the ballot to rescind the standard. (JX 25 at 5).

1237. During the period from May 1990 through the end of 1995, patented technology, or potentially patented technology was proposed to JC 42.3 for standardization on at least a dozen occasions, as described above, and in each instance the technology was balloted and the ballot passed. On at least seven of these occasions, this occurred without any request for or receipt of a RAND assurance letter.

1238. JEDEC's behavior, as described for example in the JEDEC 42.3 meeting minutes, shows that JEDEC repeatedly adopted technologies despite patent issues, especially after receiving a RAND letter. In accordance with this behavior, had Rambus provided a RAND assurance, JEDEC would have adopted the Rambus technologies. (Teece, Tr. 10379-80, 10382-84).

1239. EIA General Counsel, John Kelly, agreed that there is no objection to having features and standards that are protected by valid patents as long as they are available to all comers on reasonable and nondiscriminatory terms. (Kelly, Tr. 2072).

1240. The chair of JC 42.3 admitted that if Rambus had agreed to give a RAND assurance, "I would have had to consider accepting their intellectual property." (Kelley, Tr. 2564-66).

1241. Similarly, HP's JEDEC representative, Tom Landgraf, testified that if Rambus had disclosed the existence of patent applications on the DDR technologies, he

would have still voted to incorporate those technologies if Rambus had indicated a willingness to comply with the JEDEC patent policy. (Landgraf, Tr. 1714).

1242. The evidence therefore supports the conclusion that JEDEC would have adopted Rambus's technologies.

1243. This conclusion is not undermined by testimony about "price constraining" alternatives. Even if alternatives were "price constraining" with respect to Rambus's technologies, they could not have been chosen by JEDEC. (Teece, Tr. 10366-67). A technology that is price constraining is not the same as an economic substitute. (Teece, Tr. 10370-71). An economic substitute must be equivalent in terms of cost-performance features. (Teece, Tr. 10371). Technologies that are not equivalent may still be price constraining, but that does not make them a viable alternative for JEDEC. (Teece, Tr. 10371). What is important to compare is the overall attractiveness of the alternatives on a quality/cost-adjusted basis. (Teece, Tr. 10976-97).

1244. The conclusion that JEDEC would have adopted Rambus's technologies in SDRAM and DDR once it received a RAND assurance from Rambus is not undermined by the possibility that JEDEC might have been "satisficing." (Teece, Tr. 10414-15). If JEDEC had avoided patented technologies in favor of alternative technologies without a lot of analysis, it would not have been satisficing; such conduct is merely biased behavior. (Teece, Tr. 10414). If JEDEC were satisficing, it would be willing to go forward with patented technology upon the receipt of a RAND letter. (Teece, Tr. 10414-15).

3. Conclusion About The But-For World.

1245. The most likely scenario is the one in which JEDEC asks for and receives a RAND assurance from Rambus, no *ex ante* negotiations take place, and JEDEC adopts Rambus's technologies in both SDRAM and DDR. (Teece, Tr. 10415-16). Accounting for that scenario and the possibility that JEDEC might proceed without asking for a RAND letter, it is a virtual certainty that, had Rambus made the additional disclosures that Complaint Counsel allege should have been made, JEDEC would have adopted the same standards in the but-for world that it adopted in the actual world. (Teece, Tr. 10416).

E. Summary Of Findings On Alternatives.

1246. JEDEC repeatedly adopted for its standards the Rambus technologies at issue. It adopted two of the technologies in the SDRAM standard over several alleged alternatives. It adopted all four of the technologies in the DDR standard over alleged alternatives. And it adopted all four of the technologies in the DDR2 standard over alleged alternatives.

1247. This repeated adopted shows that the Rambus technologies were superior to any alternatives considered by JEDEC.

1248. There were no technological restraints that required JEDEC to continue to use the four Rambus technologies in DDR2.

1249. At the time of formulating the DDR2 standard, JEDEC explored using alternatives for each of the four Rambus technologies.

1250. JEDEC adopted the four Rambus technologies in the DDR2 standard with knowledge of Rambus's issued patents and knowledge of Rambus's demands for royalties.

1251. JEDEC members have continued standardization efforts in other contexts despite warnings that the standards being developed would violate Rambus's patents.

1252. There is substantial evidence that JEDEC members believed throughout the 1990's that Rambus's patents would not be valid. This evidence helps to explain their conduct.

1253. Each of the alternatives proposed by Complaint Counsel's experts is either covered by Rambus's patents or inferior in cost-performance terms.

1254. No combination of non-infringing alternatives identified by Complaint Counsel's experts is less costly than Rambus's royalties for SDRAM or DDR.

1255. A rational manufacturer or group of manufacturers would have adopted the Rambus technologies and paid the Rambus royalties for SDRAM and for DDR rather than adopt the alternatives proposed by Complaint Counsel's experts.

1256. Manufacturers and consumers are better off using Rambus's technologies and paying the Rambus royalties for SDRAM and for DDR than they would be if JEDEC had adopted the alternatives proposed by Complaint Counsel's experts.

1257. Complaint Counsel have failed to meet their burden to show that there existed viable, non-infringing alternatives that JEDEC would have adopted in place of the Rambus technologies.

1258. Complaint Counsel have failed to meet their burden to prove that JEDEC would have adopted alternative technologies had Rambus made the additional disclosures that Complaint Counsel allege should have been made.

X. THE DRAM INDUSTRY IS NOT, AND HAS NOT BEEN, "LOCKED IN" TO USING THE RAMBUS TECHNOLOGIES.

1259. While Complaint Counsel contend that the DRAM industry was locked in to using the Rambus technologies once they were adopted into the JEDEC standards and the industry began producing compliant products, the evidence discussed above refutes this notion.

1260. Specifically, the evidence shows that, even as late as 2000, JEDEC considered changing its standards and switching to alternatives to Rambus's technologies. For instance, in March 2000, Micron proposed eliminating programmable latency in SDRAM and DDR devices. (CX 154A at 25-29). In response, Bob Fusco at Hitachi wrote that it was *not* too late to make these changes in DDR. (RX 1626 at 4).

1261. Steve Polzin testified that in 2000 he discussed alternatives to Rambus's technologies with DRAM manufacturers. (Polzin, Tr. 3988, 3996, 4044).

1262. Also in this time period, JEDEC's Future DRAM Task Group considered alternatives for each of Rambus's technologies, but ended up adopting the Rambus technologies with full knowledge of Rambus's issued patents and demands for royalties.

1263. As Complaint Counsel's own expert testified, JEDEC members would not be discussing alternatives to Rambus's technologies in 2000 unless they thought that the

alternatives could be adopted. (McAfee, Tr. 7571).

1264. Complaint Counsel has failed to produce a single contemporaneous document that states these considerations were fruitless because the industry was locked in. In fact, while they have elicited the testimony of interested parties on this issue, Complaint Counsel has failed to produce a single document that states DRAM manufacturers or the industry could not have switched to alternatives to Rambus's technologies.

1265. Nonetheless, Complaint Counsel contend that the DRAM industry is locked in to using the Rambus technologies in SDRAM and DDR because the cost to transition to alternative technologies is allegedly too high and it is allegedly too difficult for the DRAM industry to coordinate a transition away from using Rambus's technologies. The evidence at trial, however, demonstrates that (1) DRAM manufacturers concurrently produce multiple types of DRAM in their factories and routinely change their manufacturing lines to incorporate new technologies, (2) that the industry routinely coordinates changes in technology, and (3) that switching costs are not prohibitive. The evidence therefore shows that the DRAM industry has not been and is not locked in to using Rambus's technologies.

A. The DRAM Industry Transitions To New Technologies All The Time.

1266. The evidence shows that the DRAM industry not only frequently and rapidly transitions to new technologies, but that it uses multiple DRAM standards at any given time.

1. The Statistical Evidence Of DRAM Purchases Shows Multiple Co-Existing DRAM Standards And Frequent Transitions.

1267. The statistical evidence regarding DRAM purchases over time shows multiple DRAM standards coexisting and regular transitions.

1268. In 1994, fast page mode ("FPM") DRAM accounted for 96.7% of the revenue for DRAM. (Rapp, Tr. 10100, 10248). The remaining 3% of DRAM revenue was accounted for by other DRAM technologies. (Rapp, Tr. 10248).

1269. In 1995, FPM accounted for 87.2%, EDO DRAM for 9.9%, and other DRAM for 2.9% of DRAM revenue. (Rapp, Tr. 10100-01, 10248).

1270. In 1996, FPM accounted for 39.4%, EDO for 52.7%, SDRAM for 4.3%, RDRAM for 0.5%, and other DRAM for 3.1% of DRAM revenue. (Rapp, Tr.10101, 10248).

1271. In 1997, FPM accounted for 8.1%, EDO for 55.2%, SDRAM for 33.5%, DRAM for 1.3%, and other DRAM for 1.8% of DRAM revenue. (Rapp, Tr. 10101, 10248).

1272. In 1998, FPM accounted for 8.8%, EDO for 27.6%, SDRAM for 60.8%, RDRAM for 1.6%, and other DRAM for 1.3% of DRAM revenue. (Rapp, Tr. 10101, 10249).

1273. In 1999, FPM accounted for 10.5%, EDO for 17.5%, SDRAM for 69.3%, RDRAM for 1.1%, and other DRAM for 1.5% of DRAM revenue. (Rapp, Tr. 10102, 10249).

1274. In 2000, FPM accounted for 5.2%, EDO for 11.1%, SDRAM for 78.4%, RDRAM for 3%, DDR for 0.4%, and other DRAM for 1.9% of DRAM revenue. (Rapp, Tr. 10101, 10249).

1275. In 2001, FPM accounted for 4%, EDO for 7.7%, SDRAM for 69.7%, RDRAM for 12.5%, DDR for 5.3%, and other DRAM for 0.8% of DRAM revenue. (Rapp, Tr. 10101, 10249).

1276. Within each of these categories, there were different speeds (e.g, for SDRAM, PC66, PC100, PC133; for DDR, DDR200, DDR266, DDR333, DDR400). (Rapp, Tr. 10249-50; Gross, Tr. 2348-56; Polzin, Tr. 3998-4005).

1277. These figures show that in any given year the DRAM market is divided among multiple incompatible standards (Rapp, Tr. 10103-04), and it demonstrates that there is no technological or economic force mandating a single standard in the DRAM industry. (Rapp, Tr. 10103-04).

2. DRAM Manufacturers Are Constantly Redesigning DRAM.

1278. The evidence shows that DRAM manufacturers are constantly coming out with new and redesigned DRAM products.

1279. Brian Shirley, Design Operations Manager for the Computing and Consumer group at Micron Technology (Shirley, Tr. 4133), testified that Micron "taped out," or gone through the entire design process, for numerous different DRAM each year.

1280. Mr. Shirley testified that **{IN CAMERA MATERIAL**

REDACTED} (Shirley, Tr. 4218 (in camera)).

1281. In 1998, **{IN CAMERA MATERIAL REDACTED}** (Shirley, Tr. 4218-19, 4226 (in camera)).

1282. In 1999, **{IN CAMERA MATERIAL REDACTED}** (Shirley, Tr. 4220-23, 4225-26 (in camera)).

1283. In 2000, **{IN CAMERA MATERIAL REDACTED}** (Shirley, Tr. 4223-25 (in camera)).

1284. In 2001, **{IN CAMERA MATERIAL REDACTED}** (Shirley, Tr. 4227 (in camera)).

1285. In 2002, **{IN CAMERA MATERIAL REDACTED}** (Shirley, Tr. 4228-29 (in camera)).

1286. According to Mr. Shirley, **{IN CAMERA MATERIAL REDACTED}** (Shirley, Tr. 4282 (in camera)).

3. DRAM Manufacturers Manufacture Multiple Types Of DRAM Contemporaneously And Routinely Change Their Manufacturing Lines To Incorporate New Technologies.

1287. The evidence also shows that DRAM manufacturers not only produce multiple types of DRAM at any given time, but also frequently transition their manufacturing lines to incorporate new technologies.

1288. Micron CEO Steven Appleton testified that Micron currently manufactures a wide variety of DRAMs, including EDO, SDRAM, DDR, DDR2 and various specialty DRAMs, such as pseudostatic RAMs. (Appleton, Tr. 6264).

1289. In a "response script" prepared by Micron in December 1996 for use in discussions with customers, Micron described its ability to manufacture various different kinds of DRAMs. (RX 836 at 2-4).

1290. The December 1996 "response script" was prepared by Micron in connection with Intel's announcement that it intended to design its next generation of chipsets to work with Rambus memory devices, then denominated "nDRAM." (RX 836 at 2; Lee, Tr. 6853-54). At the time, Micron did not have a license to manufacture the Rambus device. (*Id.*).

1291. The December 1996 "response script" includes possible questions and proposed answers. One such question is "What would having to make 'nDRAM' or SyncLink mean to Micron?" (RX 836 at 3). Micron's answer to this question is instructive:

"Keep in mind that ALL of these DRAM technologies use the

> same DRAM process, the same DRAM cell, and virtually the same DRAM array.
>
> . . .
>
> Switching from one product to another, while still using the same core technology, involves only changing priorities in design and product engineering and may mean some differences in our assembly and test equipment purchases. SDRAM, SLDRAM, nDRAM all use the same fab equipment and core DRAM technology. *In short, while the flavors might change, it's still a DRAM*."

(RX 836 at 3) (emphasis added).

1292. Henry Becker, Vice President and Managing Director for the Infineon Technologies Richmond factory (Becker, Tr. 1093), testified that, since the first silicon came out of the Infineon Richmond plant in January 1998, that plant manufactured four different types of 64MB SDRAM (through 2001); three different types of the 256 SDRAM (2000-present); the 128MB SDRAM (2001-2002); and two different types of the 256MB DDR (2000-present). (Becker, Tr. 1167-69, 1179-83).

1293. Mr. Becker further testified that every "shrink" (i.e., reduction in the feature size of the DRAM) and redesign requires a new "mask set" for the product. (Becker, Tr. 1170-73). In the 2.5-3 years in which the Infineon Richmond plant manufactured 64MB SDRAMs, it had to make at least 20 different mask sets. (Becker, Tr. 1170-73).

1294. Mr. Becker also testified that, when the Infineon Richmond plant transitioned some of its lines from SDRAM to DDR, Infineon had to purchase additional equipment because DDR requires additional manufacturing processes. (Becker, Tr. 1182-83). Nonetheless, DDR and SDRAM were made in the same processing facility, and except for

the additional equipment, its manufacture used the same processing equipment. (Becker, Tr. 1182-83).

1295. In fact, of the DRAM currently produced by the Infineon Richmond plant, approximately two-thirds are DDR and one-third are SDRAM. (Becker, Tr. 1139).

1296. Infineon's 2002 product information guide lists three Infineon manufacturing plants, which produce the following product categories: DDR SDRAM, SDR SDRAM, Graphics RAM, Mobile-RAM, and RLDRAM. (CX 2466 at 2-3).

1297. The Infineon 2002 product information guide lists the following densities for DDR products as either being currently in production by Infineon or planned for production in 2002: 128 Mb DDR, 256 Mb DDR, 256 Mb FBGA DDR, and 512 Mb DDR. (CX 2466 at 5). Each of these different density products is produced in three different organizations (e.g., for the 128Mb DDR - 32Mx4, 16Mx8, and 8Mx16). (CX 2466 at 5). Each of these different organizations is produced in several speeds (e.g., for the 512Mb DDR in the 128Mx4 organization - DDR200, DDR266A, and DDR333). (CX 2466 at 5). In all, according to the product guide, Infineon had in production 34 different DDR products in 2002.

1298. The Infineon 2002 product information guide lists the following densities for SDRAM products as either being currently in production by Infineon or would be in production in 2002: 256Mb SDRAM, 256Mb FBGA SDRAM, and 512Mb SDRAM. (CX 2466 at 6-7). Each of these different density products is produced in three different

organizations (e.g., for the 256Mb SDRAM - 64Mx4, 32Mx8, and 16Mx16). (CX 2466 at 6). Each of these different organizations is produced in several speeds (e.g., for the 512Mb SDRAM in the 128Mx4 organization - PC100 and PC133). (CX 2466 at 7). In all, according to the product guide, in 2002 Infineon had in production in 27 different SDRAM products.

1299. In addition, the Infineon product guide shows that Infineon produced 7 different types of Graphics RAM, 20 different types of Mobile DRAM, and 6 different types of RLDRAM (according to the part numbers). (CX 2466 at 8-9).

1300. According to Mr. Becker, Infineon's Richmond plant currently manufactures all 12 of the different types, organizations and speeds of 256-megabit SDRAMs listed in the Infineon 2002 product information guide (CX 2466), as well as DDR products. (Becker, Tr. 1143)

1301. Infineon is able to shift its production of DRAM to a different density within in 14 months. (Becker, Tr. 1146-1148). According to Mr. Becker, die shrinks require new equipment, new processes, putting in the capability to run the wafers, electrical performance testing of wafers and process tweaking, design tweaking and "some redesigns", reliability testing, customer qualification and feedback. All this takes only 14 months. (Becker, Tr. 1158).

1302. Infineon is able to shift its production of DRAM to increased speeds in as little as 3 to 4 months. (Becker, Tr. 1148-49).

1303. When Infineon shifted some of its manufacturing lines from producing SDRAM to producing DDR, the shift took 16-17 months. (Becker, Tr. 1149-50).

1304. If technically feasible, the alternatives proposed by Professor Jacob could each have been implemented in a 6-12 month time frame. (Geilhufe, Tr. 9674-75).

1305. These facts show that scale economies are not so powerful that they drive the industry necessarily to a single standard technology at any one time. (Rapp, Tr. 9894-95).

1306. Economies of scale occur at the plant level. (Rapp, Tr. 9893). Plants in the industry often produce at the same time a variety of DRAM (using different technologies, DRAM of different speeds, etc.). (Rapp, Tr. 9893). For example, RDRAM, SDRAM, and DDR have coexisted in the marketplace. (Rapp, Tr. 9893-94). Similarly, different subgenerations of DRAM - e.g., PC66, PC100, PC133 - have coexisted in the marketplace. (Rapp, Tr. 9893-94). This shows that the economics of the industry does not require a single standard. (Rapp, Tr. 9893).

1307. The coexistence of multiple standards also shows that network effects in the DRAM industry are not so high as to make it impractical to switch to an alternative technology. (Rapp, Tr. 9895).

4. The DRAM Industry Routinely Coordinates Transitions To New Standards.

1308. Complaint Counsel contend that the DRAM industry cannot switch to alternatives to Rambus's technologies because of the difficulties of coordinating the necessary changes among DRAM manufacturers and manufacturers of complementary

products (which manufacture the so-called "infrastructure" of the memory subsystem). The evidence shows, however, the DRAM industry routinely coordinates transitions to new DRAM technology without impediment.

1309. That the industry can coordinate changes in technology, even radical changes, is evidenced by AMD's experience. Prior to its K7 microprocessor, AMD produced microprocessors that were "pin compatible" with Intel processors. (Heye, Tr. 3653). That is, AMD processors could be plugged into sockets designed for Intel processors and could use the entire Intel-based infrastructure. (Heye, Tr. 3653). An infrastructure in a computer consists of a north bridge (also called a chipset), which connects the microprocessor via a bus to the memory, graphics, and the south bridge. (Heye, Tr. 3655-58). The south bridge communicates with peripheral devices, such as the keyboard and mouse, and the BIOS, which communicates with the microprocessor. (Heye, Tr. 3655-58).

1310. Richard Heye, Vice President and General Manager of the Microprocessor Business Unit at AMD (Heye, Tr. 3615), joined AMD in June 1997 to construct the infrastructure for the K7 processor, which did not exist. (Heye, Tr. 3652-54). AMD was able to coordinate with vendors for each part of the infrastructure and to launch complete systems by 1999. (Heye, Tr. 3646-47).

1311. During this time, AMD took no more than 15-18 months to design and produce a K7 north bridge, starting from scratch. (Heye, Tr. 3767-69). In June 1999, AMD launched the first AMD K7 processor, which used the AMD750 chipset with a

200MHz front side bus (FSB) and was compatible with PC100 SDRAM. (Polzin, Tr. 3998-4005).

1312. Soon thereafter, third party vendors such as VIA designed and launched chipsets for the K7 processor that were compatible with PC133 SDRAM. (Polzin, Tr. 3998-4005; Heye, Tr. 3769-70). This change required the development of a different north bridge and a new motherboard. (Heye, Tr. 3769-70).

1313. In September 2000, AMD launched a new version of the K7 processor using a 266 MHz FSB and the newly designed AMD760 chipset, which was compatible with DDR200 and DDR266. (Polzin, Tr. 3998-4005). The design of the new chipset took only 15-18 months, and the resulting chipset was not backward compatible with SDRAM. (Heye, Tr. 3767-69).

1314. To transition from using SDRAM to DDR, the newly established AMD infrastructure needed newly designed motherboards, newly designed DIMMs, and a new BIOS. (Heye, Tr. 3767-69).

1315. As part of this transition to DDR, AMD gave motherboard samples to manufacturers in March 2000, and those manufactures were able to produce the DDR compatible motherboards in volume by September 2000. (Polzin, Tr. 4017-18).

1316. In fact, according to an internal memorandum, AMD decided to transition to DDR in early 1999, was able to power up a complete system by December 1999, and was shipping units by October 2000. (CX 2158 at 2; Heye, Tr. 3805-10).

1317. In October 2002, AMD launched a new version of the K7 processor with a 333MHz FSB. Third party chipsets made for this version were compatible with DDR333. (Polzin, Tr. 3998-4005).

1318. During these changes, portions of the infrastructure other than the chipset changed as well. For example, DDR333 had different DIMM specification from those of previous generations of DDR. (Polzin, Tr. 4006-07).

1319. In May 2003, AMD launched the K7 processor with a 400MHz FSB. (Polzin, Tr. 3998-4005). Matched with newly designed third party chipsets, this system uses DDR400. (Polzin, Tr. 3998-4005).

1320. In sum, the AMD K7 systems went from using PC100 to PC133 to DDR200 and 266 to DDR333 to DDR400 - 5 transitions - all in the time period from June 1999 to May 2003. These transitions are illustrated in DX 31.

1321. Compaq, an OEM that produced personal computers, servers, and workstations and is now part of HP (Gross, Tr. 2265), has gone through similar transitions.

1322. Compaq started using EDO DRAM in its products in 1995. (Gross, Tr. 2348-56).

1323. In 1997, Compaq shifted to using PC66 SDRAM in its computers, which required different chipsets and different motherboards. (Gross, Tr. 2348-50). PC66 SDRAM was an Intel standard. (Gross, Tr. 2348-9).

1324. In 1998, Compaq shifted to using PC100 SDRAM in its computers. (Gross, Tr. 2348-56). The PC100 SDRAM was an Intel standard. (Gross, Tr. 2348-56). It was not backward compatible with PC66 SDRAM. (Gross, Tr. 2348-56).

1325. In 1999, Compaq shifted to using PC133 SDRAM in its products. (Gross, Tr. 2348-56). The PC133 SDRAM was an Intel standard. (Gross, Tr. 2348-56).

1326. In 2001, Compaq/HP shifted to using DDR 266 in its products. (Gross, Tr. 2348-56). DDR requires a different chipset than does DRAM. (Bechtelsheim, Tr. 5938). DDR is not backward compatible with SDRAM; a DDR device cannot be used in an SDRAM socket (Bechtelsheim, Tr. 5958).

1327. In late 2002, Compaq/HP shifted to using DDR 333 in its products. (Gross, Tr. 2348-56).

1328. From 1995 to 2002, therefore, Compaq shifted from using EDO DRAM to PC66 SDRAM to PC100 SDRAM to PC133 SDRAM to DDR266 to DDR333 in its products.

1329. There are of course other examples of the rapid product changes in the computer industry. For instance, Barry Wagner, the manager of technical marketing at nVidia, a company that produces graphics processors (Wagner, Tr. 3820), testified that nVidia launched 14 new products in the space of 6 years. (Wagner, Tr. 3875-76).

1330. In short, technological changes occur all the time within DRAM and the DRAM industry routinely coordinates the changes in complementary products.

1331. If there were a change in the existing standards to incorporate alternatives to Rambus's technologies, only a small portion of the overall infrastructure would need to be changed - the chipset, the DIMM, the motherboard, and possibly the BIOS. (Heye, Tr. 3742-43).

1332. A shift to alternative technologies would thus incur no additional costs or coordination difficulties beyond those that would be incurred when the industry was in transition to a new standard. (Polzin, Tr. 4040-42).

B. The Industry Is Not Locked In.

1333. Complaint Counsel contend that the DRAM industry is "locked in" to using the four Rambus technologies because it would be too difficult and expensive to switch to an alternative. The evidence, when evaluated from an economic perspective, contradicts this assertion.

1. Switching Costs Are Not Prohibitive.

1334. Lock-in is a term used in economics to identify a situation where switching costs prohibit consumers from changing to another product or technology. (Rapp, Tr. 9873-74). Switching costs are the costs incurred to transition to an alternative product or technology. (Rapp, Tr. 9873-74).

1335. Specific investments and switching costs are not identical. (Rapp, Tr. 9875-77). For instance, a company may make a specific investment of $100 million in building a coal-burning plant located near a particular coal mine. If, in response to an increase in the

price of coal from the coal mine, the only way to avoid the paying the price increase is to shut down the plant and build a new plant in another location for $100 million, the switching costs and the specific investment of $100 million are the same. (Rapp, Tr. 9875-77). If, however, the coal plant can be converted to a gas burning plant for a cost of $5 million, the switching costs are $5 million, not the $100 million to build a new plant. (Rapp, Tr. 9875-77).

1336. With respect to DRAM, the cost of constructing and equipping a fabrication facility is not relevant to switching costs. (Rapp, Tr. 9877-78). This is because a DRAM facility may produce several types of DRAM; there is no need to build a new DRAM facility to produce a new type of DRAM. (Rapp, Tr. 9877-78).

1337. The fact that an industry has high fixed costs and low marginal costs does not have any bearing on switching costs unless the fixed costs have to be replicated in their entirety in order to switch to a new technology. (Rapp, Tr. 9880).

1338. Complaint Counsel's economic expert admitted on cross-examination that he did not quantify any switching costs. (McAfee, Tr. 7716-17, 11356).

1339. It is not possible for an economist to make a sound judgment about whether switching costs are high enough to create lock-in without quantifying those costs. (Rapp, Tr. 9881).

1340. The switching costs for a DRAM manufacturer to shift from using the Rambus technologies to alternative technologies may be calculated by summing the

additional one-time-only fixed costs associated with switching to the alternative technologies. (Rapp, Tr. 9883-85). Mr. Geilhufe testified regarding his estimates of these costs. (Rapp, Tr. 9884, 10122-24).

1341. This calculation shows that switching costs associated with shifting to alternatives to Rambus's technologies were relatively low in comparison with the expenses associated with manufacturing DRAMs in general and that DRAM manufacturers could therefore have switched at any point. (Rapp, Tr. 9878).

1342. For example, to maintain the functionality provided by programmable CAS latency and programmable burst length when switching to fixed CAS latency and fixed burst length requires 12 different parts (3 different CAS latencies and 4 different burst lengths). (Rapp, Tr. 9885). The additional fixed costs associated with switching to fixed CAS latency and fixed burst length are: $300,000 in additional design costs for the 3 CAS latencies; $400,000 in additional design costs for the 4 different burst types; $250,000 per part in additional qualification costs times 12 different parts; and $50,000 in additional photo-tooling costs times 12 different parts - this totals $4.3 million. (Rapp, Tr. 9885). These costs are illustrated in DX317.

1343. The total of these costs – $4.3 million - is modest relative to DRAM production costs in general (Rapp, Tr. 9886), and less than the royalties paid to Rambus to license the use of programmable CAS latency and programmable burst length in SDRAM. (Rapp, Tr. 9886-87). If fixed CAS latency and fixed burst length were truly viable non-

infringing alternatives, a manufacturer could profitably switch to those alternatives. (Rapp, Tr. 9886-87).

1344. The evidence shows assuming that the alternatives were preferable in cost performance terms, it would have been relatively easy to implement certain of the proposed alternatives to programmable latency when manufacturers were going through technology upgrades or at the time of the transition from SDRAM to DDR SDRAM. (Soderman, Tr. 9418). Such regular redesigns happened on the order of every 6 to 12 or 18 months. (Soderman, Tr. 9418; Geilhufe, Tr. 9615). In particular, the fixed CAS latency alternative or the alternative or adding pins could easily have been implemented at these times.

1345. The switching costs for any combination of alternatives for Rambus's four technologies may be calculated by summing the design, qualification, and photo-tooling costs associated with those alternatives as provided by Mr. Geilhufe. (Rapp, Tr. 10124). The switching costs for the fixed CAS latency and fixed burst length alternatives are typical, if not higher than, the switching costs for the other alternatives. (Rapp, Tr. 10124).

1346. Complaint Counsel's economic expert admitted that he did not quantify any switching costs. (McAfee, Tr. 7716-7; 11356). He also admitted that switching from Rambus's technologies to alternative technologies would be less costly than the switch from SDRAM to RDRAM. (McAfee, Tr. 7717-8).

2. <u>Coordination Issues Do Not Prevent Switching</u>.

1347. Because the DRAM industry routinely coordinates changes in DRAM

technology with the various complementary manufacturers, one can infer that the switching costs to shift away from the Rambus technologies would be on the same order of magnitude as those for switching to fixed CAS latency and fixed burst length. (Rapp, Tr. 10127-28).

1348. Complaint Counsel's economic expert admitted that switching away from Rambus's technologies to alternative technologies would involve the same categories of costs that were incurred when the industry went from SDRAM to DDR, and from PC100 SDRAM to another grade of PC SDRAM. (McAfee, Tr. 7714-15, 11357).

1349. Coordination issues with producers of complementary goods would not prevent switching away from the Rambus technologies. (Rapp, Tr. 9889). Coordination of this sort happens all of the time in the industry; there is no evidence that suggests that any coordination issues with switching away from Rambus's technologies could not be resolved in the ordinary course of business. (Rapp, Tr. 9889-90).

1350. Coordination for a switch away from Rambus's technologies would not be difficult even if the DRAM industry has made investments in using the Rambus technologies. (Rapp, Tr. 9890). If there were truly viable non-infringing alternatives, the coordination issues faced by the industry would not be any more difficult than those that the industry faces routinely in other situations. (Rapp, Tr. 9890-91).

1351. Complaint Counsel contend that coordination would be difficult because some DRAM manufacturers are licensed under Rambus's patents, but others are not. But the fact that some DRAM manufacturers are licensed to use Rambus's technologies and

others are not would not affect the ability of the industry to coordinate switching (Rapp, Tr. 9891-92), because all manufacturers have an interest in using alternatives that are best in cost-performance terms. (Rapp, Tr. 9801-92).

1352. Complaint Counsel's economic expert admitted that he did not reach a conclusion as to whether the interests of the 50% who have licensed from Rambus have interests regarding a standard that eliminates the patented technologies that are different from the 50% who have not taken a license. (McAfee, Tr. 7723).

1353. DRAM manufacturers were not locked in to using the Rambus's technologies at any point in time from 1990 to today. (Rapp, Tr. 9896). Their continued used of the Rambus technologies is due to the fact that the four Rambus technologies are superior in cost-performance terms to any alternatives. (Rapp, Tr. 9896-99). This is true for the two Rambus technologies used in SDRAM, the four used in DDR, and the four used in DDR2. (Rapp, Tr. 9896-99).

1354. The fact that the DRAM industry continues to use the four Rambus technologies in DDR2 when that standard was developed after Rambus's issued patents and their claimed scope were well known in the industry demonstrates that Rambus's technologies were superior in cost-performance terms even taking into account Rambus's royalty rates. (Rapp, Tr. 9898-99).

C. Summary Of Findings On The Issue Of Lock In.

1355. Multiple standards have coexisted in the DRAM industry for the entire

relevant period.

1356. Manufacturers have produced multiple types of DRAM at any given time.

1357. Manufacturers routinely redesign DRAM products.

1358. The industry routinely coordinates switching to new types of DRAM.

1359. Complaint Counsel has failed to show that the costs for a DRAM manufacturer to switch to alternatives for the Rambus technologies in SDRAM and DDR are prohibitive.

1360. Complaint Counsel has failed to show that coordination issues prohibit the industry from adopting alternatives to Rambus's technologies.

XI. RAMBUS'S ROYALTIES ARE IN FACT REASONABLE AND NON-DISCRIMINATORY.

1361. Because JEDEC would have adopted in the but-for world the Rambus technologies incorporated in SDRAM and DDR had Rambus made the additional disclosures that Complaint Counsel contend should have been made without any *ex ante* negotiation of the royalty rates, Rambus and the DRAM manufacturers would have negotiated licenses for Rambus's patents *ex post*, as they did in the real world.

1362. The only difference between the but-for world and the actual world would be that, in the but-for world, Rambus would have given a commitment to license on reasonable terms and conditions that are demonstrably free from unfair discrimination. If Rambus's actual royalty rates are in fact reasonable and nondiscriminatory, there is no difference between the but-for world and the real world.

1363. As discussed below, Rambus's royalty rates for its SDRAM and DDR technologies are reasonable and non-discriminatory. This means that, not only would JEDEC have adopted the same technologies in the but-for world, but the licensing rates in the but-for world and the real world are identical.

1364. Rambus offered the expert testimony of Professor Teece on the issue of whether Rambus's royalties were reasonable and nondiscriminatory. Professor Teece is well qualified to opine on this issue.

1365. Professor Teece has studied the semiconductor industry for many years; he has consulted in the industry; and he has focused on understanding patents, licensing and cross-licensing in the semiconductor industry. (Teece, Tr. 10301-02).

1366. Professor Teece is frequently called to advise companies on their licensing policies and the design of licensing arrangements and agreements. (Teece, Tr. 10303). He is also frequently asked to testify on antitrust and patent damages issues. (Teece, Tr. 10303). Much of his consulting work involves the semiconductor industry. (Teece, Tr. 10303). Over the last 20 years, he has advised at least a dozen companies on licensing and licensing strategy. (Teece, Tr. 10417). In addition, as the member of the board of directors of several companies, he has approved licensing agreements and on some occasions actually negotiated them. (Teece, Tr. 10419).

1367. More recently, he published a paper on licensing and cross-licensing in the semiconductor industry that was published in the California Management Review. (Teece,

Tr. 10302). He has written a number of times on the issue of licensing, including one of the first studies on technology transfer and technology licensing (for which he interviewed over one hundred licensing executives). (Teece, Tr. 10418). In the mid-1990's, Professor Teece did a study on cross-licensing during which he interviewed more licensing executives. (Teece, Tr. 10418).

1368. Professor Teece has been a member of the Licensing Executives Society for about 20 years. (Teece, Tr. 10417). He has addressed licensing executives at the annual meeting of the Licensing Executives Society and he has published two papers in the journal of that society. (Teece, Tr. 10418).

1369. Professor Teece has been qualified as an expert in a number of courts to testify on the issue of reasonable royalties. (Teece, Tr. 10419).

1370. Complaint Counsel's economic expert, on the other hand, admitted that he had no expertise determining a reasonable royalty rate. (McAfee, Tr. 7737). Nor does he have any expertise in the areas of licensing or technology transfer. (McAfee, Tr. 11245).

A. Rambus's Royalty Rates Are Reasonable.

1371. Rambus's royalty rates for its SDRAM and DDR technologies are "reasonable" within the meaning of the EIA/JEDEC patent policy.

1. The JEDEC Rules Defined "Reasonable" As The Rate Determined By The Market.

1372. Mr. Kelly, the EIA General Counsel, testified that EIA does not get involved in the determination whether terms are reasonable and non-discriminatory; rather, EIA

leaves this determination to the "marketplace," i.e., a willing licensee and licensor engaged in arms-length negotiation. (J. Kelly, Tr. 1882-83). As he explained, "We don't get into the definition, the further definition of reasonable and nondiscriminatory at all. We leave that to the parties to work out or the courts." (J. Kelly, Tr. 2073-74).

1373. Mr. Kelly also admitted that it is not one of the goals of EIA or JEDEC to get the lowest possible royalty rate if there is intellectual property in the standards. (J. Kelly, Tr. 2073).

1374. Robert Goodman of Kentron testified that he understood a reasonable rate to be what the market will agree to pay. (Goodman, Tr. 6088).

1375. Similarly, according to Desi Rhoden, whether licensing terms for patents covering JEDEC compliant products were "fair and reasonable" is to be determined by the courts. (Rhoden, Tr. 658, 663; RX-1461 at 1).

2. Rambus's Royalties Are Comparable To Other Licensing Rates In The Industry And Are "Reasonable" Under The JEDEC Rules.

1376. The evidence shows that Rambus's royalty rates for its SDRAM and for DDR licenses are reasonable. First, as shown below, Rambus's royalty rates are low relative to industry rates in the semiconductor industry.

1377. Rambus's royalty rate for its SDRAM licenses is .75%. (Rapp, Tr. 9832). Its royalty rate for its DDR licenses (with the exception of its license to Hitachi) is 3.5%. (Rapp, Tr. 9853-53). These rates are low compared to other licensing rates in the

semiconductor industry.

1378. The IBM Worldwide Licensing Policy sets forth royalty rates from 1-5% of selling price: "The royalty for use of IBM's patents may be based on the licensee's selling price of each product covered by one or more licensed patents or on the royalty portion selling price of such product, the choice being left to the licensee. . . . The royalty rates are 1% of the selling price if the product is covered by one Category I patent and 2% of the selling price if the product is covered by two or more Category I patents . . . . If the product is covered by one, two or three or more Category II patents, the royalty will be, respectively, 1%, 2% or 3% of the selling price added to any royalty incurred for Category I patents." (JX 9 at p.24).

1379. Mark Kellogg presented this IBM Worldwide Licensing policy to JEDEC at a meeting of J42.5 on December 2, 1991. (JX 9 at 24; Kellogg, Tr. 5232, 5238-39). No one, to his memory, suggested that IBM's license rates were unreasonable. (Kellogg, Tr. 5238-39). Mr. Kellogg was not authorized by IBM to discuss royalty rates; he therefore could not tell anyone at JEDEC that IBM would license on other than IBM's standard rates. (Kellogg, Tr. 5236-37).

1380. Gordon Kelley agreed that the IBM Worldwide Licensing Policy shown at the December 1991 JEDEC meeting shows royalty rates of 1-5%, and he too did not recall anyone saying that these rates were unreasonable. (Kelley, Tr. 2618-20).

1381. The IBM Standards Practice Manual that was in effect in 1996 states, "The

normal royalty rate for a license to IBM patents ranges from 1% to 5% of the selling price for the apparatus that practices the patents. This is a very reasonable rate in our industry and generally meets the requirement of standards organizations that licenses be made available on reasonable and nondiscriminatory terms and conditions." (RX 653 at IBM/2 128124).

1382. Similarly, the IBM Standards Program, which superseded the IBM Standards Practice Manual, states, "The normal royalty rate for a license to IBM patents ranges from 1 percent to 5 percent of the selling price for the apparatus that practices the patents. This is a very reasonable rate in our industry and generally meets the requirement of standards organizations that licenses be made available on reasonable and nondiscriminatory terms and conditions." (RX 653 at IBM/2 153802).

1383. The IBM website contains IBM's Standards Practices and states that IBM's royalty rates for patent licenses granted to members of standard-setting organizations is 1-5%. (RX 2105-07 at 1).

1384. AMD **{IN CAMERA MATERIAL REDACTED}** (Heye, Tr. 3919-20 (*in camera*); CX 1420 at 8 (*in camera*)).

1385. In February 1990, Digital Equipment Corporation wrote to JEDEC to inform

its members that Digital would agree to license its U.S. Patent No. 4,851,834 and corresponding foreign patents for a royalty rate of 1% of sales. (JX 1 at 24).

1386. After DRAM manufacturers complained of administrative burdens associated with royalty agreements, Kentron changed from charging 5% royalties for Kentron's FEMMA technology to pricing its patented flex tabs, which are a necessary input for the FEMMA technology, so as to receive the equivalent of the 5% royalty. (Goodman, Tr. 6020-22, 6078-80). Kentron has also set the price of its patented switches, used in its QBM technology, such that for a QBM product priced around $200, the purchaser would pay an additional $18 included within that price for the Kentron patented QBM technology (approximately 9%). (Goodman, Tr. 6087). As a matter of economics, a higher price built into a product that is a necessary input is the equivalent of the same amount charges as a royalty. (Teece, Tr. 10432).

1387. Mr. W.R. Griffin, the DRAM product line manager for IBM, wrote in an August 11, 2000 email that Rambus's SDRAM royalty rate produced only a relatively small exposure for IBM: "If we were faced with a fee for 2001 then I believe our exposure is relatively small. This year 99% of our sales are SDR." (RX 1695 at 2; Kellogg, Tr. 5248).

1388. Published judicial decisions show that in 1993, Hyundai entered into a semiconductor cross-license with Texas Instruments and agreed to pay a royalty of 8% on all its sales of semiconductor products, including DRAM. *Texas Instruments, Inc. v. Hyundai Electronics Indus.*, 42 F. Supp. 2d 660, 663-64, 671, 676-77 & n.39 (E.D. Tex.

1999); *Texas Instruments, Inc. v. Hyundai Electronics Indus.*, 49 F. Supp. 893, 897 (E.D. Tex. 1999).

1389. Samsung entered into a similar cross-license with Texas Instruments in which it agreed to pay 9% on the sales of DRAMs in the United States and 3% on the sales of DRAMs in Japan. *Texas Instruments, Inc.*, 49 F. Supp. at 902. Texas Instruments offered Hyundai similar terms on DRAM sales. *Id.*

1390. The Licensing Economics Review conducted a survey of semiconductor licenses that was published 2001. (Teece, Tr. 10444-45; RX 2105-05). This survey found 78 licenses for semiconductors with an average royalty rate of 4.6% and a median rate of 3.2%. (Teece, Tr. 10444-45; RX 2105-05 at 5). The royalty rates ranged from 0% to 30%. (RX 2105-05 at 5).

1391. PLX Systems Survey conducted a commissioned study of licenses in the category of Semiconductors and Related Devices (SIC code 3674) in an Ernst & Young database, which was published in January 2003. (Teece, Tr. 10446-47; RX 2105-03). This survey found 238 license agreements with payment terms. (RX 2105-03 at 2). Of those, 106 agreements had royalty rates based on net sales and 5 were based on gross sales. (RX 2105-03 at 3). The average royalty rate for the agreements based on net sales was 4.54% and the median rate was 4%. (RX 2105-03 at 3; Teece, Tr. 10448).

1392. In Rambus's 1992 business plan, Rambus recognized that its royalty rates were in line with semiconductor "traditional royalty levels of 1-5%." (CX 543A at 14).

1393. Based on these industry rates, as Professor Teece concluded, Rambus's royalty rates are reasonable. (Teece, Tr. 10429-51). The industry royalty rates cluster around 4 to 5%. The Rambus SDRAM royalty rate of 0.75% is low end of what comparable technologies command. (Teece, Tr. 10451). Rambus's DDR royalty rate is near the low end of the middle of comparable rates. (Teece, Tr. 10451).

1394. Complaint Counsel's economic expert, on the other hand, admitted that he had no expertise in how to determine a reasonable royalty rate. (McAfee, Tr. 7737).

1395. In fact, the industry rates used in this comparison underestimated actual rates because the semiconductor industry rates tend to reflect balancing payments on cross-licenses rather than rates for a straight license like Rambus's. (Teece, Tr. 10423-24). A royalty rate that is paid as a balancing payment (e.g., where two companies cross-license, the company with the smaller or weaker patents must pay the other party a balancing payment) reflects a much higher implied royalty rate for the underlying intellectual property rights. (Teece, Tr. 10424). Published royalty rates, particularly in the semiconductor industry, therefore show only the tip of the iceberg of what the royalty rates for a straight patent license would be worth in the industry. (Teece, Tr. 10424).

1396. Complaint Counsel's economic expert recognized this when he admitted that companies can get economic value from internally developed patented technology because it gives the company a benefit in cross-licensing negotiations. (McAfee, Tr. 7698). For example, Micron has been able to reduce its overall royalty payments from approximately

10% to a negligible amount by increasing the number of patents it is able to include in its end of cross-licenses. (Appleton, Tr. 6299-300).

1397. Second, Rambus's royalty rates are low relative to the cost-performance of Rambus's technologies versus alternatives technologies. As discussed above, even with Rambus's royalties, the cost of Rambus's technologies is less than that of alternatives.

1398. Third, Rambus's royalty rates for SDRAM and DDR SDRAM were agreed to in arms-length negotiations with major industry players. (Teece, Tr. 10425).

1399. **{IN CAMERA MATERIAL REDACTED}** (Teece, Tr. 10534 (*in camera*)).

1400. First, **{IN CAMERA MATERIAL REDACTED}** (Teece, Tr. 10534-35 (*in camera*); MacWilliams, Tr. 4824-25).

1401. Second, **{IN CAMERA MATERIAL REDACTED}**

1402. **{IN CAMERA MATERIAL REDACTED}**

(Teece, Tr. 10535-36 (*in camera*)). Rambus was able to "participate in future design improvements," obtain information about the partner's customers, and be "part of the process going forward." (Farmwald, Tr. 8179-80).

1403. Rambus's RDRAM licenses form a partnership; Rambus works with the licensee, and receives valuable feedback and information. (Farmwald, Tr. 8241). For non-DDR by contrast, there is no partnership, and Rambus receives no additional benefits. (Farmwald, Tr. 8241). **{IN CAMERA MATERIAL REDACTED}** (Teece, Tr. 10535 (*in camera*)).

1404. Complaint Counsel's economic expert admitted that although Rambus's RDRAM licenses have benefits to Rambus that its DDR licenses do not, he did not quantify those benefits when comparing the DDR and RDRAM license rates. (McAfee, Tr. 7835).

B. Rambus's Licenses Are Not Discriminatory.

1405. Rambus's licenses are non-discriminatory.

1. JEDEC Has Left the Definition of "Non-Discriminatory" to the Market and the Courts.

1406. As Mr. Rhoden testified, JEDEC takes no position on the definition of questions regarding "non-discriminatory." (Rhoden, Tr. 665). Rather, JEDEC leaves the determination of what terms are nondiscriminatory to the market and, if that fails, to the courts. (Kelly, Tr. 1882-83).

1407. For instance, when Dick Foss of Mosaid wrote to JEDEC to ask whether the RAND requirement means that Mosaid had to license its DLL patent on the same terms to licensees currently under a broad patent license from Mosaid as to those who just licensed the DLL technology, Mr. Townsend responded that the details of the license terms were left to Mosaid's negotiations with individual companies. (RX 1461 at 1-2). Desi Rhoden also replied that the interpretation of RAND is left to the courts. (RX 1461 at 1).

1408. Similarly, JEDEC did not object when Mosaid indicated that there would be differences in its licenses for its DLL patent depending on whether the licensee licensed only the DLL patent or multiple patents from Mosaid. In May 1999, Dick Foss wrote to JEDEC stating, "There is inevitably a difference between someone who gets a DLL license thrown in as part of a multi-million settlement on multiple patents and someone who just wants a license for DLL usage." (CX 400 at 2). He also wrote, "There will be differences in terms if company 'a' is a general licensee (and is automatically licensed anyway) and company 'b' is not and so will be expected to take a 'reasonable' license if wanting to use our IP on the item." (CX 400 at 1). Jim Townsend responded that he would presume that this arrangement was acceptable, though he thought Mosaid should ask counsel. (CX 400 at 1). Joe Macri did not recall any objection to Mosaid's two tiered licenses and never raised the issue with Dick Foss. (Macri, Tr. 4714-16; RX 1457).

1409. Robert Goodman of Kentron testified that he understood that a nondiscriminatory rate should be measured at a particular point in time; at different points

in time, charging different rates is not discriminatory if there is some reason to charge a different rate. (Goodman, Tr. 6088).

1410. JEDEC has also indicated that whether a patentee can charge a higher rate for a party that chooses to litigate rather than license is left to the market and the courts. In a September 6, 2001 letter from Christopher Pickett, General Counsel of Tessera, Inc., to John Kelley, EIA's President and General Counsel, Mr. Pickett recounted his discussion with Mr. Kelley to the effect that either the parties or the courts must resolve whether JEDEC's RAND policy allowed Tessera to charge a higher rate to litigating parties: "As we discussed on the phone and as is set forth in your letters, this JEDEC policy is intentionally broad in order to allow the parties to negotiate terms and come to their own decision on what the words mean in the particular circumstances. The JEDEC patent policy does not negate the context of what is commercially reasonable in determining license terms with a particular licensee. Whether a patent owner may consider a company's adverse action in negotiating licensing terms is a matter that must be resolved, in the first instance, by the negotiating parties themselves. If the parties cannot reach agreement, they may submit the question to the courts for resolution." (RX 1885 at 1).

2. <u>Rambus's Licenses are Non-Discriminatory</u>.

1411. **{IN CAMERA MATERIAL REDACTED}** (Teece,

Tr. 10538 (*in camera*)).

1412. Rambus offered its SDRAM and DDR licenses to everybody on more or less the same terms. (Farmwald, Tr. 8242).

1413. Complaint Counsel contend that Rambus's DDR license rates are discriminatory because Rambus charges a higher rate to Hitachi, which is the only licensee that litigated with Rambus before signing a license.

1414. In fact, however, before litigation, Rambus offered Hitachi a license on essentially the same terms it offered to others. (CX 2059, Karp Depo. at 251). Complaint Counsel's economic expert understood that in 2000, Rambus was prepared to offer a license for DDR to any interested company at 3.5%. (McAfee, Tr. 7845). He therefore admitted that, in the economic sense of nondiscriminatory, Rambus was prepared to offer nondiscriminatory licenses. (McAfee, Tr. 7848).

1415. Higher royalties for litigating parties are not discriminatory in an economic sense for a number of reasons. First, **{IN CAMERA MATERIAL REDACTED}** (Teece, Tr. 10541 (*in camera*)). Second, **{IN CAMERA MATERIAL REDACTED}** (Teece, Tr. 10541 (*in camera*)).

1416. Third, **{IN CAMERA MATERIAL REDACTED}** (Teece, Tr. 10540 (*in camera*)). In other words, the fact that

Rambus charged a higher rate after litigation may be justified by changed perceptions regarding the strength of the patents.

1417. Fourth, **{IN CAMERA MATERIAL REDACTED}** (Teece, Tr. 10542 (*in camera*)). This creates **{IN CAMERA MATERIAL REDACTED}** (Teece, Tr. 10542-43 (*in camera*)).

1418. **{IN CAMERA MATERIAL REDACTED}** (Teece, Tr. 10542, 10551 (*in camera*)).

1419. Complaint Counsel's economic expert did not challenge this point. Rather he used an analysis based on production costs to conclude that Rambus's DDR royalty rate to Hitachi was discriminatory. (McAfee, Tr. 7827). But for purposes of determining whether patent licenses are discriminatory, **{IN CAMERA MATERIAL REDACTED}** (Teece, Tr. 10545 (*in camera*)).

1420. Moreover, Complaint Counsel's economic expert effectively admitted that litigation imposes costs on Rambus and that it is economically rational to develop a strategy to avoid those costs. (McAfee, Tr. 7829). He went on to admit that it would be consistent

with economic theory to charge a higher royalty rate to licensees that require the patent holder to incur costs before taking a license. (McAfee, Tr. 7829). Further, he recognized that Hitachi's litigation with Rambus imposed risks on Rambus (McAfee, Tr. 7830), and that a licensing strategy of charging more to companies that choose to litigate would maximize Rambus's profits by reducing its future costs. (McAfee, Tr. 7831).

1421. Complaint Counsel's economic expert did not make any assumption as to whether charging a higher rate to companies that choose to litigate violates the JEDEC nondiscrimination policy. (McAfee, Tr. 7832).

1422. Therefore, **{IN CAMERA MATERIAL REDACTED}** (Teece, Tr. 10537-38, 10545-46 (*in camera*)). For the same reasons, **{IN CAMERA MATERIAL REDACTED}** (Teece, Tr. 10547 (*in camera*)).

XII. THE ECONOMIC IMPLICATIONS OF THE EVIDENCE.

1423. Assuming, contrary to the facts, that: (1) JEDEC rules obligated Rambus to disclose information about its patent interests; (2) Rambus failed to disclose information to JEDEC that these rules required be disclosed; and (3) JEDEC members were misled by this

alleged conduct on the part of Rambus, the evidence still shows that the alleged conduct did not harm competition.

1424. First, the facts show that Rambus's alleged conduct was not "exclusionary" as that term is used in economics. Conduct that is not exclusionary, though it may be disliked by or even harmful to competitors, is not anticompetitive.

1425. Second, the facts show that Rambus's alleged conduct did not increase or add to its market power.

A. Rambus's Alleged Failure to Disclose Was Not Exclusionary.

1426. Complaint Counsel contend that Rambus's alleged conduct was "exclusionary." As explained below, this contention fails for a number of reasons.

1. The Alleged Conduct Was Not Exclusionary Because There Is a Valid Business Justification For Not Disclosing Information About Patent Applications.

1427. Exclusionary conduct can be characterized as an investment in the destruction of a rival. It is defined in economics by a two-part test. (Rapp, Tr. 9909-11). First, the conduct must consist of short-run actions that do not make sense except in terms of their adverse impact on competition. (Rapp, Tr. 9911). That is, the actions cannot have an independent business justification. (Rapp, Tr. 9911). Second, after competition is excluded or weakened, the conduct must be likely to lead to recoupment through the exercise of market or monopoly power that would not exist but for the conduct. (Rapp, Tr. 9911).

1428. An example of exclusionary conduct is pricing below average variable cost. (Rapp, Tr. 9911-12). In that example, the conduct leads to greater losses every time another sale is made. (Rapp, Tr. 9912). There is therefore no business justification for pricing below average variable cost. (Rapp, Tr. 9912).

1429. An example of conduct that might have an adverse effect on competitors but is not exclusionary is pricing below total cost but above variable cost, such conduct might reduce margins but does not increase losses with every transaction. (Rapp, Tr. 9912). There are good business reasons for this type of pricing. (Rapp, Tr. 9912). Thus, even though pricing below total cost might hurt competitors, especially if they are less efficient, it benefits consumers and is not exclusionary. (Rapp, Tr. 9912-13).

1430. An example of conduct involving intellectual property that is not exclusionary even though it adversely affects competitors is where a firm develops a cost-saving technology, protects the technology through trade secrets or patents, and drives its rivals out of business by being the low cost competitor. (Rapp, Tr. 9913). There is nothing exclusionary about this conduct even though, in the normal sense of the word, competitors are excluded. (Rapp, Tr. 9913-14).

1431. Even conduct that may violate an extrinsic duty, and is therefore illegal or unethical, is not necessarily exclusionary even if that conduct affects competition. For instance, Complaint Counsel's economic expert admitted that a misrepresentation, even if it has an impact on competition, is not always exclusionary. (McAfee, Tr. 7535-36).

1432. Even if conduct excludes superior alternatives, excludes commercially viable alternatives, raises the perceived relative cost of alternatives, and adversely affects competition, these fact alone are not sufficient to define exclusionary conduct in an economic sense. (Rapp, Tr. 9927-28). Each of these is an effect of conduct rather than a characterization of conduct and is therefore insufficient itself, or together with the others, to define exclusionary conduct. (Rapp, Tr. 9927-28).

1433. Incurring risk does not make conduct exclusionary. (Rapp, Tr. 9930-31). Businesses take risks all the time, most often to achieve some sort of gain. (Rapp, Tr. 9931). Conduct cannot be deemed exclusionary on the ground that it entails risks without assessing the possible gains from the conduct. (Rapp, Tr. 9931). Thus, the fact that risk was taken says nothing about whether conduct is exclusionary. (Rapp, Tr. 9931).

1434. Rather, if there is a valid efficiency rationale for conduct, it is not exclusionary. (Rapp, Tr. 9914). In examining Rambus's conduct in this case, therefore, part of the economic test is to determine whether there exists a valid business justification for the alleged conduct. (Rapp, Tr. 9914).

1435. From an economic perspective, the protection of trade secrets is a valid business justification for not disclosing information regarding pending patent applications as well as for not disclosing intentions to file applications in the future (including intentions about amending pending claims). (Rapp, Tr. 9915-16).

1436. There is a valid business justification for not disclosing such information

because: (1) disclosure may jeopardize the issuance of pending claims by enabling competitors to file patent interferences or to race to be first-to-file in certain foreign jurisdictions; and (2) disclosure may result in a loss of competitive advantage by informing competitors of the firm's R&D focus or by inducing competitors to begin work around efforts earlier. (Rapp, Tr. 9916-18).

1437. These business justifications apply to pending applications and intentions to file or amend future applications, even after a parent patent application becomes public. (Rapp, Tr. 9926). Thus, in Rambus's situation, even after the '898 application had been disclosed (in the form of the PCT application), Rambus still had trade secrets (additional pending applications and intentions to file additional applications) that it could legitimately protect from disclosure. (Rapp, Tr. 9926).

1438. Not only is not disclosing information about pending or future patent applications rational and profit maximizing for the firm, it is procompetitive for the same reasons that preserving trade secrets is procompetitive. (Rapp, Tr. 9918). This type of nondisclosure preserves incentives to innovate because innovation depends on the ability to control intellectual property. (Rapp, Tr. 9918-19). It thus enhances consumer welfare by leading to better competitors, which leads to enhanced competition, increased output, and lower prices. (Rapp, Tr. 9918).

1439. Similarly, exercising intellectual property rights to exclude competitors and protecting trade secrets from use by other companies are not exclusionary conduct. (Rapp,

Tr. 9229-30). Nor is exercising intellectual property rights to charge royalties that might raise a rival's costs is not exclusionary conduct. (Rapp, Tr. 9229). To the contrary, all of these actions may be procompetitive. (Rapp, Tr. 9929-30).

1440. These conclusions apply in the standard-setting context as in any other. A company that is the member of a standard-setting body may benefit from not disclosing information regarding its pending patent applications or its intentions to file future patent applications regardless what standards are developed. (Rapp, Tr. 9919-20). The benefits to a company keeping control of its business and intellectual property strategies do not depend on which standard is chosen by the standard-setting body. (Rapp, Tr. 9919-20). These benefits have to do with maximizing the ability to operate competitively, not standardization. (Rapp, Tr. 9920).

1441. From the standpoint of antitrust economics, if Rambus had failed to disclose information to JEDEC about its pending or future patent applications, its conduct would not have been exclusionary because there was a legitimate business justification for such nondisclosure. (Rapp, Tr. 9921). Keeping that information confidential did *not* impose on Rambus costs or risks that were compensable only by excluding rivals and thereby gaining market power. (Rapp, Tr. 9924).

1442. Rambus's economic expert, Dr. Rapp, testified that Rambus's alleged conduct was not exclusionary in an economic sense. (Rapp, Tr. 9921). Dr. Rapp is well qualified to give this type of economic opinion. He holds a bachelor's degree in economics

from Brooklyn College in 1965, a master's degree in economic history from the University of Pennsylvania in 1966, and a Ph.D. in economic history from the University of Pennsylvania in 1970. (Rapp, Tr. 9766). He is the president of NERA, which is an economics consulting firm with 500 employees that specializes in the economics of competition, including industrial economics, antitrust, intellectual property. (Rapp, Tr. 9764). He has been an economic consultant with NERA since 1977 and the president of NERA since 1988. (Rapp, Tr. 9764). Prior to his joining NERA, Dr. Rapp was a tenured professor at the State University of New York at Stony Brook. (Rapp, Tr. 9766).

1443. In addition, Dr. Rapp has published articles on predatory pricing, intellectual property economics, and innovation in high-technology markets. (Rapp, Tr. 9768-69). In the past 15 years, a great deal of his consulting work has been in the area of high-technology antitrust and intellectual property, typically in the computer and semiconductor industries. (Rapp, Tr. 9769-70).

1444. Dr. Rapp has been qualified as an expert on numerous occasions. Since the early 1980's, Dr. Rapp has testified in hearing or trials as an antitrust economics expert, on average, about once per year. (Rapp, Tr. 9771). He has testified at least five times as an expert on the economic aspects of intellectual property issues. (Rapp, Tr. 9771-72).

1445. Although he did not explicitly acknowledge that a decision not to disclose information regarding pending patent applications would not be exclusionary in the

presence of valid business justifications, Complaint Counsel's expert conceded the underlying rationale for this conclusion.

1446. Complaint Counsel's economic expert did not criticize or rebut Dr. Rapp's opinion that Rambus's conduct was not exclusionary because of the presence of a legitimate business justification. To the contrary, he admitted that concealing information, even if it discourages competitors from entering a market, is not exclusionary. (McAfee, Tr. 7525-27). Complaint Counsel's economic expert also admitted that it is not exclusionary to conceal an invention from competitors in order to take advantage of the invention while others cannot. (McAfee, Tr. 7527-28).

1447. Yet Complaint Counsel's economic expert admitted that the only "candidate purpose" he considered for Rambus's withholding information about its patent applications was monopolization, i.e., he did not consider other purposes that might have led Rambus to take the risk that he identified. (McAfee, Tr. 7539). In other words, he did not consider whether Rambus did not disclose information about its patent applications for a valid reason.

2. Even Under The Definition Proposed By Complaint Counsel's Economic Expert, Rambus's Conduct Was Not Exclusionary.

1448. The evidence shows that Rambus's conduct was not exclusionary even as that term was defined byComplaint Counsel's economic expert. The exclusion of inferior products from the market is not exclusionary in an economic sense. (McAfee, Tr. 7536).

1449. According to Complaint Counsel's economic expert, in order for conduct to be exclusionary, it must impact equal or superior alternatives. (McAfee, Tr. 7537).

1450. The evidence shows that there were no equal or superior alternatives in cost-performance terms. Dr. Rapp testified that the cost differences that he quantified and the performance advantages of the Rambus technologies made them superior to the alternatives in cost-performance terms. (Rapp, Tr. 9861-62).

1451. Complaint Counsel's economic expert did not provide testimony to refute this conclusion.

1452. Complaint Counsel's economic expert admitted that he did not quantify any cost differences between Rambus's technologies and the alternative technologies. (McAfee, Tr. 11340).

1453. Although Complaint Counsel's economic expert admitted that JEDEC members would consider the performance of alternatives in deciding whether to pursue the alternatives (McAfee, Tr. 11340), he did not quantify the performance differences between Rambus's technologies and any of the alternatives he claimed were commercially viable. (McAfee, Tr. 7581-82, 11340). The evidence shows that Rambus's technologies were superior to the alternatives in performance terms.

1454. Complaint Counsel's economic expert also admitted that JEDEC members would consider the "headroom" or future flexibility of alternatives in deciding whether to pursue the alternatives. (McAfee, Tr. 11340). He did not, however, compare the headroom

or future flexibility of Rambus's technologies with any of the alternatives he said were commercially viable. (McAfee, Tr. 11340-41). The evidence shows that Rambus's technologies were superior to the alternative in terms of headroom and flexibility.

1455. For example, Complaint Counsel's economic expert admitted that JEDEC behavior and JEDEC discussions show that JEDEC members valued multiple latencies and multiple burst lengths, yet he did not quantify that value. (McAfee, Tr. 11351).

1456. Complaint Counsel's economic expert also testified that, although he had made no effort to determine if any intellectual property covered any of the alternatives that he considered commercially viable other than Kentron's technology, the presence of intellectual property *could* render a technology not commercially viable in his opinion, because JEDEC attached a "penalty" to the presence of intellectual property. (McAfee, Tr. 7582-85). As discussed above, there is evidence that several of the alternatives that he said were commercially viable are covered by patents.

1457. In short, Complaint Counsel's economic expert did not refute the cost-performance quantification provided by Dr. Rapp or his conclusion that Rambus's alternatives were superior to the alternatives.

1458. Because Rambus's conduct could have excluded only inferior technologies, it cannot be exclusionary even as that term is defined by Complaint Counsel's economic expert.

3. The Definition Of Equal Or Superior Alternatives Proposed By Complaint Counsel's Economic Expert Is Flawed.

1459. Complaint Counsel's economic expert testified that he believed that equal or superior alternatives were excluded by Rambus's alleged conduct. His definition of "equal or superior" was, however, flawed. To determine whether equal or superior alternatives were excluded, Complaint Counsel's expert developed a "commercial viability" test. (McAfee, Tr. 7330-31).

1460. Although he claimed that his methodology was "parallel" to standard economic tests, Complaint Counsel's economic expert admitted that he was aware of no economic literature that describes the use of a "commercial viability" test to determine market substitutability of alternatives. (McAfee, Tr. 7567).

1461. According to Complaint Counsel, an alternative was "commercially viable" if it constrained the price of Rambus's technologies. (McAfee, Tr. 7330-31). But defined that way, the concept of "commercially viable" does not mean that the technology is "equal or superior." Even weak substitutes can constrain the price of a technology. (Rapp, Tr. 9860). An alternative can therefore be "commercially viable" in this sense without being equal or superior or even a viable alternative in any practical sense (Teece, Tr. 10368, 10370-71).

1462. What is more, when determining whether an alternative was price constraining, Complaint Counsel's economic expert provided no analysis of price elasticity. In other words, he did not consider the price level required before the alternatives would

actually constrain the price. Instead, he simply looked for evidence that the alternative was considered as a possible alternative by members of JEDEC and that knowledgeable engineers now claimed that the alternative was viable. (McAfee, Tr. 7333-34).

1463. Further, Complaint Counsel's economic expert tied his notion of commercial viability to subjective judgments of JEDEC members. (McAfee, Tr. 7335). This had several consequences for his analysis.

1464. First, Complaint Counsel's economic expert judged patented technologies to be "hobbling" because the JEDEC rules put a "penalty" on technologies that were covered by intellectual property. (McAfee, Tr. 7337,7582-83). He thus regarded patented technologies, such as Rambus's, as inferior merely because of the presence of intellectual property and without regard to the level of royalties sought for that technology.

1465. Determining whether an alternative is "equal or superior" cannot turn on such subjective judgments. In a competitive market, if the best solution in cost-performance terms is patented and involves the payment of royalties, competition will dictate that the royalties be paid and that the patented solution is adopted. (Rapp, Tr. 9939). While individual executives in an industry may dislike paying royalties, just as they may dislike paying health care costs for workers or a competitive wage, they will have no choice because competition will mandate that these costs be incurred. (Rapp, Tr. 9938-39).

1466. Second, Complaint Counsel's economic expert also considered "a perception of the magnitude of those problems" associated with that technology as "relevant to the

determination of which technologies should be selected." (McAfee, Tr. 7586). In other words, he based his determination of whether a technology was "equal or superior" on the subjective perceptions of JEDEC members at the time, regardless of whether these perceptions were ultimately correct. While this factor may go to whether JEDEC would have selected the technology, it does not go to whether the alternative is equal or superior in objective terms.

1467. Third, Complaint Counsel's economic expert considered each company's strategic interests in which technology would be selected because of differences in technical ability. (McAfee, Tr. 7338-39). In other words, in determining whether a technology was commercially viable, he factored in whether some JEDEC members might prefer the technology because they were better equipped to produce it. Again, while this factor may go to whether JEDEC would have selected the technology, it does not go to whether the alternative is equal or superior in objective terms.

1468. Fourth, Complaint Counsel's economic expert relied on his notion of "satisficing" to conclude, in effect, that a product that has lesser performance is nonetheless "equal" to one with better performance. (McAfee, Tr. 7335-36). In other words, because he believed that JEDEC was "satisficing," Complaint Counsel's economic expert essentially defined "equal" to include technologies that were *inferior* to Rambus's technologies.

1469. Fifth, when it came to cost and performance, as explained above, Complaint Counsel's economic expert offered no quantitative data.

1470. Not only were the factors considered by Complaint Counsel's economic expert subjective, his methodology was as well. Rather than examining the actual cost differences between the Rambus technologies and the alternatives, Complaint Counsel's economic expert simply opined that he had considered an amalgam of factors and determined that certain alternatives were "commercially viable" based "on the information [he] analyzed." (See, e.g., McAfee, Tr. 7363).

1471. While Complaint Counsel's economic expert testified that it was likely that at least one of the technologies he deemed commercially viable alternatives to Rambus's technology was equally efficient or superior to Rambus's technology, he admitted that he could not identify any particular technology as equal or superior to Rambus's technologies. (McAfee, Tr. 7578-79).

4. Complaint Counsel's Economic Expert Admitted That Complaint Counsel's Theory of Exclusionary Conduct Requires Economically Irrational Behavior.

1472. The theory of exclusion put forth by Complaint Counsel's economic expert requires an assumption that Rambus behaved irrationally.

1473. In determining that Rambus's conduct was exclusionary, Complaint Counsel's economic expert assumed that Rambus *knowingly* took a risk that it might lose the ability to enforce its patents by not disclosing patent interests that it should have

disclosed. (McAfee, Tr. 7538-40). Complaint Counsel's economic expert believed that Rambus did so solely to dupe JEDEC into incorporating its technologies into the JEDEC standards.

1474. But Complaint Counsel's economic expert admitted that Rambus would have understood that if it withheld information about its patent applications that it should have disclosed, any effort to enforce its patents once they issued, would have triggered an inquiry into whether Rambus should have disclosed its patent interests. In addition, Complaint Counsel's economic expert admitted that if a JEDEC member failed to disclose patent interests that should have been disclosed and revealed knowledge of that patent interest, e.g., in a written document, the risk of a challenge that would render the patents invalid would increase substantially. (McAfee, Tr. 7550).

1475. In other words, the theory of Complaint Counsel's economic expert assumed that Rambus's conduct was irrational because it would have known that its scheme would fail. He theorizes that Rambus withheld information about its patent applications to be able to enforce its patents against JEDEC members while knowing that the result of that conduct might be that it would be unable to enforce those patents.

5. Complaint Counsel's Economic Expert's Opinion Rests On An Assumption Of That A "Violation Of A Rule Or Process" Caused JEDEC To Adopt The Rambus Technologies.

1476. Complaint Counsel's economic expert explained that Rambus's concealing of information about its patent applications would, in his opinion, be exclusionary only if it

violated a rule or process. (McAfee, Tr. 7530-31, 7546).

1477. He assumed that Rambus "should have disclosed patents or patent applications with reference to all four of the technologies challenged in the case." (McAfee, Tr. 7546). But he admitted that, "If they shouldn't have disclosed on one of the technologies, then my finding of exclusionary conduct on that technology is no longer -- on that particular technology would no longer be reliable because I've assumed that they should have disclosed on that technology." (McAfee, Tr. 7546).

1478. Yet Complaint Counsel's economic expert admitted that he did his analysis with no assumptions about the specific claims of any patent application that Rambus should have allegedly disclosed. (McAfee, Tr. 7669-70).

1479. Complaint Counsel's economic expert also admitted that he did his analysis with no assumptions about the specific date that Rambus allegedly should have made the disclosures that Complaint Counsel allege should have been made. (McAfee, Tr. 7671).

1480. Complaint Counsel's economic expert also admitted that he did his analysis with no assumed specific triggering event that would have caused Rambus to be obligated to make disclosures to JEDEC. (McAfee, Tr. 7671).

1481. The premise of Complaint Counsel's economic expert is false because as discussed above, Rambus did not have, and in any event was not obligated to disclose, patent applications covering any of the four technologies while it was a JEDEC member.

1482. Complaint Counsel's economic expert admitted that if work on DDR had not

begun by the time Rambus had left JEDEC and if there was no duty to disclose absent such work, the conclusions that he drew from assuming that Rambus failed to disclose with regard to DDR would fall away. (McAfee, Tr. 7575). As discussed above, no duty to disclose regarding DDR technologies was triggered while Rambus was attending JEDEC.

1483. Complaint Counsel's economic expert admitted that if Rambus made the additional disclosures that Complaint Counsel allege should have been made, JEDEC ignored the disclosure, and JEDEC incorporated the Rambus technology nonetheless, Rambus would not have engaged in exclusionary conduct. (McAfee, Tr. 7682). As discussed above, this is a likely outcome had the additional disclosures been made.

1484. Complaint Counsel's economic expert also admitted that there are situations in which JEDEC could become aware of Rambus' potential patents other than through Rambus' disclosure of that information to JEDEC, such that Rambus' failure to disclose would not, as a matter of economics, constitute exclusionary conduct. (McAfee, Tr. 7686). As discussed above, JEDEC members were in fact aware of the risk that Rambus could obtain patents on the four technologies.

1485. Complaint Counsel's economic expert further admitted that it is both plausible and consistent with his assumptions that if Rambus never joined JEDEC, JEDEC would have selected the four Rambus technologies for inclusion in its standards. (McAfee, Tr. 7688). In other words, Complaint Counsel's economic expert conceded that Rambus's

conduct did not cause JEDEC to select the four technologies at issue in this case over others.

1486. In sum, even applying Complaint Counsel's economic expert's reasoning, Rambus's alleged conduct was not exclusionary.

6. Complaint Counsel Has Not Shown That Enforcing JEDEC's Rules Furthers The Objective Of Antitrust Law.

1487. Complaint Counsel's economic expert based his entire analysis on the assumption that Rambus's conduct violated a JEDEC rule or process. (McAfee, Tr. 7530-31).

1488. Yet Complaint Counsel's economic expert admitted that he had done no analysis to determine whether JEDEC's rules and processes advanced the interests of antitrust law. (McAfee, Tr. 7532-33).

1489. Nor did Complaint Counsel's economic expert perform any analysis of the JEDEC's costs and benefits in order to determine the economically efficient disclosure rules for it to impose. (McAfee, Tr. 7727). In fact, he admitted that he has not investigated the economic efficiency of JEDEC's rules. (McAfee, Tr. 7727-28).

1490. Complaint Counsel's economic expert did, however, opine that the "preferred" time for disclosure of information regarding intellectual property is as early as possible. (McAfee, Tr. 7301). As an economic matter, however, it is not correct that the optimal time for disclosure of information regarding patent interests is as early in the standardization process as possible. (Teece, Tr. 10385).

1491. Comments provided by the Institute of Electrical and Electronics Engineers Standards Association ("IEEE-SA") to the FTC in April 2002 speak to this issue. The IEEE is a professional society of engineers with over 370,000 members, whose standards arm has more than 870 active standards. (RX 2011 at 1).

1492. The IEEE-SA informed the FTC in April 2002, in connection with the FTC/DOJ hearings regarding competition and intellectual property, that:

> "[i]f disclosure of issued patents is expected too early in the process - i.e., before the draft standard has reached a level of stability – more patents may be disclosed than those that are essential, since it may be too early to determine exactly those that will be required for implementation. This problem would become even larger if, as some have suggested, patent applications were to be treated in the same manner as issued patents. A 'one size fits all' solution cannot be applied to disclosure."

(RX 2011 at 5).

1493. As Professor Teece testified, disclosure involves costs, so the optimal time for disclosure must consider those costs. (Teece, Tr. 10385). Depending on the costs and benefits, later disclosure may be optimal. (Teece, Tr. 10402).

1494. The costs involved include the cost to the patent applicant of losing trade secrets and confidentiality. (Teece, Tr. 10453). The costs to the standard-setting organization are that it must try to evaluate and assess the highly preliminary information regarding the patent application. (Teece, Tr. 10453-54).

1495. Since patents are not going to change and are public, the costs associated with disclosing patents are less than those associated with disclosing patent applications. (Teece, Tr. 10454-55).

1496. As the IEEE-SA explained in its April 2002 comments,

> "[s]tandards committees realize that until a patent has been issued there is very little value to disclosure since the scope of valid patent claims has not been determined. This is why it is not appropriate to group issued patents and applications togehter, especially in the context of antitrust policy where government action could have a significant impact on standards-setting procedures."

(RX 2011 at 5).

1497. The narrower the scope of disclosure regarding patent applications, the lower the costs and burdens of disclosure. (Teece, Tr. 10454, 10547-58). If intellectual property issues are put aside once a RAND assurance is given, there is less need for disclosure. (Teece, Tr. 10548).

1498. Complaint Counsel's economic expert also opined that disclosure rules mitigate the risk of hold up. (McAfee, Tr. 7272-74). But he admitted that JEDEC's disclosure rules do little to mitigate risk because the disclosure obligation applies only to the knowledge of the representative at the meeting, rather than that of the member company (McAfee, Tr. 7724); and because in large companies, the representative might not have a lot of knowledge about the company's patents. (McAfee, Tr. 7724-25). He also admitted

that a JEDEC disclosure requirement does not mitigate the risk that the standard might involve technology covered by patents held by nonmembers. (McAfee, Tr. 7725).

1499. In short, Complaint Counsel have not shown that enforcing JEDEC's rule and procedures – as Complaint Counsel have depicted those rules and procedures – furthers the interests of antitrust law.

B. Rambus's Alleged Failure To Disclose Did Not Increase Or Add To Its Market Power.

1500. A critical question in this case is whether the alleged conduct enhanced Rambus's market power.

1501. Because technologies may have market power simply by virtue of their technological superiority, it is important to distinguish the source of any market power Rambus may have.

1502. Assuming that (1) JEDEC rules obligated Rambus to disclose additional information about its patent applications, (2) Rambus knowingly and intentionally violated that obligation in order to mislead JEDEC members, and (3) JEDEC members were actually misled, the question remains whether the alleged conduct caused Rambus to gain additional market power. The evidence shows that it did not.

1. JEDEC's Standardization Of Rambus's Technologies Did Not Enhance Rambus's Market Power.

1503. The evidence shows that JEDEC's standardization of Rambus's technologies did not enhance Rambus's market power. Any market power that Rambus has is

attributable to the fact that its technologies were and are superior to any alternatives. If they were not, the DRAM industry could switch to alternatives.

1504. On this issue, Rambus offered the testimony of Dr. Rapp, who has expertise in the area of standard setting. As an example, he recently presented a paper on the economics of standard setting at a session of the Antitrust Section of the American Bar Association, which Dr. Rapp proposed and helped to organize. (Rapp, Tr. 9770-71).

1505. Last year, Dr. Rapp presented a paper and testified about the issue of standard setting and market power at the joint hearings of the Federal Trade Commission and the Department of Justice on intellectual property and the knowledge based economy. (Rapp, Tr. 9771).

1506. In contrast, Complaint Counsel's economic expert has no expertise in the area of standard setting. (McAfee, Tr. 11345).

1507. According to the economic literature, a standard is a specification of a product design intended to achieve engineering compatibility, either between parts of a product or system or between components of a network. (Rapp, Tr. 9783). Economists recognize that standards are necessary when compatibility requirements are high and when either products, systems, or networks will fail unless engineering compatibility is maintained. (Rapp, Tr. 9783). From an economist's point of view, standard setting does not entail specifying every detail of a product; rather, standard setting is economically efficient when it achieves compatibility but does not over-determine product

characteristics. (Rapp, Tr. 9785).

1508. Economist refer to standards that are set through formal means, i.e., through a standard-setting body or the government, as *de jure* standards. (Rapp, Tr. 9788-89). Standards that emerge through market forces are referred to as de facto standards. (Rapp, Tr. 9789).

1509. In a market where compatibility requirements are exceedingly high, the market might permit only a single standard. (Rapp, Tr. 9791). This may occur in a network industry, which require a special kind of complementarity where systems must be able to communicate. (Rapp, Tr. 9792). The typical example of this type of network effect is the fax machine. A fax machine is worthless if it cannot communicate with other fax machines; the more fax machines that it is able to communicate with, the more valuable it is. (Rapp, Tr. 9792-93).

1510. Where compatibility requirements are less than extreme, which is more common, multiple standards may coexist. (Rapp, Tr. 9791). For example, there are several standards for cellular telephones, but each type of cellular telephone can communicate with the other types. (Rapp, Tr. 9791).

1511. Compatibility requirements in the DRAM industry are not high. (Rapp, Tr. 9793). Although DRAM must be compatible with other components in a particular computer, a computer with one type of DRAM can communicate with a computer with another type of DRAM. (Rapp, Tr. 9793-94). This means that network effects in the

DRAM industry are weak. (Rapp, Tr. 9794).

1512. Because of the weakness of network effects, different DRAM standards can coexist in the market. (Rapp, Tr. 9794).

1513. Multiple standards in fact exists in the DRAM market.

1514. Moreover, history has shown that standardization by JEDEC is neither necessary nor sufficient to ensure success in the DRAM marketplace.

1515. Standardization by JEDEC is not necessary for marketplace success. For instance, the latest generation of Video RAM was not standardized by JEDEC yet gained market success. Samsung actually brought the technology to JEDEC for standardization, but JEDEC refused to consider it. (Prince, Tr. 9021). Samsung produced the product anyway, and it became a high volume DRAM product. (Prince, Tr. 9021-22).

1516. Similarly, reduced latency DRAM ("RLDRAM") was developed and produced by Infineon and Micron without any involvement by JEDEC. (Bechtelsheim, Tr. 5965-66).

1517. Standardization by JEDEC is also insufficient for marketplace success. For example, JEDEC standardized Burst EDO, a technology brought to JEDEC by Micron (JX 23 at 68), yet it failed in the marketplace. (Williams, Tr. 873). Failure occurred despite the fact that Micron rigorously promoted the technology. (Williams, Tr. 822-24).

1518. The publication of JEDEC's SDRAM standard was insufficient to ensure market success or even interoperability. The JEDEC SDRAM standard was not sufficiently

comprehensive; because of this, SDRAM products made by one DRAM manufacturer were not compatible with those produced by another. (MacWilliams, Tr. 4908).

1519. Prompted by these incompatibilities, Intel - not JEDEC - developed the "PC SDRAM" standard in 1996. (MacWilliams, Tr. 407-09). As stated in that standard, "The objective of this document is to define a *new Synchronous DRAM specification* ('PC SDRAM') which will remove extra functionality from the current JEDEC standard SDRAM specification, so that it will be a 'fully compatible' device among all vendor designed parts." (RX 2104-14 at 9) (emphasis added).

1520. The Intel PC SDRAM specification set forth what would become the industry standard for PC100 SDRAM. (MacWilliams, Tr. 4908). For instance, Compaq used Intel PC100 SDRAM compliant parts for its products. (Gross, Tr. 2350-51). Similarly, AMD referred to the Intel PC SDRAM specification when designing its chipsets. (Polzin, Tr. 4010-11).

1521. The Intel PC SDRAM specification later set forth the industry standard for PC66 SDRAM. (MacWilliams, Tr. 4908; RX 2104-14 at 60-61). Compaq, for example, used Intel PC66 SDRAM compliant parts for its products. (Gross, Tr. 2348-49).

1522. The PC133 SDRAM standard was developed by yet another route. In that case, DRAM manufacturers and PC OEMs developed the specification. (MacWilliams, Tr. 4912-13; CX 2560 at 1). The PC133 SDRAM standard was later incorporated into the Intel PC SDRAM standard. (RX 2104-14 at 7 (document revision history shows addition

of standards for 133MHz SDRAM); MacWilliams, Tr. 4908). Again, Compaq used the Intel PC133 SDRAM compliant DRAM for its products. (Gross, Tr. 2353).

1523. Intel's setting of the PC SDRAM standard demonstrates that there are powerful forces in the DRAM industry that affect DRAM standards in a de facto rather than de jure sense. From an economic perspective, Intel can, outside of a standard setting body, create specifications or specification addendums that become the industry standard. (Rapp, Tr. 9797). Formal standard setting is therefore not the only way in which an iteration of DRAM can become prominent. (Rapp, Tr. 9798).

1524. It is sometimes the case, but not always, that formal standard setting may create market power. (Rapp, Tr. 9798-99). Formal standard setting may create market power when (1) there are high compatibility requirements, (2) the standard setting body is faced with several technologies that are more or less equivalent in cost-performance terms, and (3) standard setting elevates one of those technologies above the others. (Rapp, Tr. 9799-800). Where compatibility requirements are not high and there may exist more than one standard, then little or no market power is gained through standard setting. (Rapp, Tr. 9800).

1525. In contrast, where one technology is superior to the alternatives then that technology would have been selected and become the *de facto* standard had the market been allowed to operate. Under these circumstances, formal standard setting does not add

any market power. (Rapp, Tr. 9800-01). The market power of the technology is due to its superiority. (Rapp, Tr. 9801).

1526. Rambus did not obtain any additional market power due to any alleged failure to disclose its intellectual property interests before standardization by JEDEC (i.e., *ex ante*) because the Rambus technologies were superior in cost-performance terms and compatibility requirements were not so strong that alternatives could not have been employed. (Rapp, Tr. 9901-02). Standardization of the Rambus technologies by JEDEC, therefore, did not reduce the substitution possibilities of alternatives, and Rambus's market power was unchanged by formal standard setting by JEDEC. (Rapp, Tr. 9902).

1527. Rambus did not obtain or retain any additional market power due to any alleged failure to disclose its intellectual property interests after standardization by JEDEC (i.e., ex post) because, even after standardization, switching costs would not have prevented a shift to an available technology that was as good or better than Rambus's technology. (Rapp, Tr. 9902-03).

1528. From an economic point of view, both consumers and manufacturers were better off by selecting the four Rambus features incorporated in DDR and paying royalties to Rambus rather than selecting any combination of the "commercially viable" alternatives identified by Complaint Counsel's economic expert. (Rapp, Tr. 9858-59).

1529. Complaint Counsel's economic expert did not offer testimony that refuted these conclusions. While he claimed that Rambus's market power was increased because

"commercially viable" alternatives were eliminated, the alternatives to Rambus's technologies that Complaint Counsel's economic expert identified as "commercially viable" are not close economic substitutes because of the cost-performance distance between those alternatives and Rambus's technologies. (Rapp, Tr. 9861-62).

1530. JEDEC's inclusion within its standards of the four technologies at issue here did not, therefore, enhance Rambus's market power.

2. The Alleged Conduct Did Not Enhance Rambus's Market Power Because JEDEC Would Have Selected Rambus's Technologies Even With The Additional Disclosure.

1531. The evidence shows that even if Rambus had made the additional disclosures that Complaint Counsel allege should have been made, JEDEC still would have included the four technologies in its standards, and JEDEC members would have ended up paying the same royalties. This shows that the alleged conduct did not enhance Rambus's market power or cause harm to competition.

1532. First, the evidence shows that the four Rambus technologies were the technologies of choice throughout the relevant time period and that a rational manufacturer or a rational JEDEC would have selected the Rambus technologies. (Rapp, Tr. 9903). The additional disclosures that Complaint Counsel allege Rambus should have made would not have affected the outcome because there were no cost-performance equivalent technologies to the two Rambus technologies incorporated in SDRAM or to the four Rambus technologies incorporated in DDR. (Rapp, Tr. 9907-08). Had the allegedly required

additional disclosures occurred, rational manufacturers and a rational standard setting organization would have adopted the Rambus technologies for both SDRAM and DDR. (Rapp, Tr. 9908-09).

1533. It therefore follows that competition has not been adversely affected by Rambus's alleged failure to disclose. (Rapp, Tr. 9908-09). It is worth noting on this issue that Complaint Counsel's economic expert testified that the alleged conduct of Rambus has had no impact on DRAM prices, no effect on consumers, and no effect on the final PC market as of the time of trial (over three and one-half years after Rambus began asserting its patents). (McAfee, Tr. 7565-66)).

1534. The conclusion that competition has not been adversely affected by Rambus's alleged failure to disclose is bolstered by the likelihood that JEDEC would have selected Rambus's four technologies had Rambus never joined JEDEC. This demonstrates that JEDEC members, acting as rational manufacturers, would have selected Ramubus's technologies, so that standardization by JEDEC did not increase Rambus's market power. (Rapp, Tr. 9863).

1535. Second, a decision analysis considering both JEDEC's and Rambus's economic incentives shows that JEDEC would have adopted Rambus's technologies. The analysis also shows that once JEDEC selected Rambus's technologies, there would not have been any *ex ante* negotiations. That being the case, licenses to Rambus's technologies would have been negotiated *after* the SDRAM and DDR standards were set and *after*

Rambus's patents issued. In other words, the license negotiations would have occurred in the but-for world at the same point in time that they occurred in the real world.

1536. Finally, the evidence shows that Rambus's royalties are reasonable and nondiscriminatory. The royalty rates are those that would have been agreed to by a willing licensee and a willing licensor.

1537. Because the but-for-world outcome is the same as the actual world outcome, Rambus's alleged conduct caused it to gain no additional market power. (Teece, Tr. 10312-13).

3. Rambus's Alleged Failure To Disclose Did Not Enhance Rambus's Market Power Because Intel, Not JEDEC, Chose The Memory Device Currently In Widespread Use.

1538. Complaint Counsel theorize that JEDEC standardization of the four technologies at issue gave them market power. In fact, the evidence shows that it was Intel, not JEDEC, that chose the memory device currently in widespread use.

1539. In the 1995-1996 time period, Intel spent about a year exploring various alternatives for the next generation DRAM. (MacWilliams, Tr. 4800-01). Intel looked at EDO, SDRAM, DDR, SyncLink, and Rambus. (MacWilliams, Tr. 4800-01). Other than these alternatives, "the memory vendors didn't have any other good ideas." (MacWilliams, Tr. 4800-01).

1540. An internal Intel document written by Peter MacWilliams explained that the DRAM manufacturers were not focused on improving DRAM technology: "Up to this

point in time [(Q395)], memory vendors were stric[t]ly focus[]ing on lowering costs and increasing density; Intel felt the memory vendors needed to get more focused on increasing access speed." (RX 1532 at 1).

1541. Intel saw a growing performance gap in the mid-1990's between CPU performance and DRAM performance. (RX 868 at 3). After examining the alternatives for a year, Intel chose RDRAM to be its next generation DRAM technology. (MacWilliams, Tr. 4800-01).

1542. Intel chose RDRAM because of the need for higher bandwidth for use with faster CPUs and the need to satisfy memory needs driven by more I/O demands and new applications. (RX 904 at 5-6; *see also* RX 805 at 2 (December 1996 Intel document reciting need for increased bandwidth driven by memory intensive applications such as visual computing and noting that Intel was looking for technology beyond 100 MHz SDRAM)).

1543. Intel's choice of RDRAM was significant. As Richard Heye of AMD - Intel's competitor in the microprocessor market - explained, in the late 1990's AMD believed that RDRAM would become the next volume memory product (even though the technology was "revolutionary") because it had been chosen by Intel: "And given that, you know, Intel, who owns 80 percent of the market, really put his wood behind the arrow, so to speak, on Rambus, you know, they had talked about the customers, well our customers were saying, hey, you ought to use Rambus, and we talked to the memory vendors. And the

memory vendors were saying, you know what, Rambus, it's a revolutionary change, not evolutionary, but, you know, that's the way the industry is going, that's the way we're going to go, and Rambus is it." (Heye, Tr. 3685).

1544. Steve Polzin of AMD concurred. He testified that it was important to AMD that Intel chose RDRAM because Intel's selection would make RDRAM a *de facto* standard: "[Intel]drove the volume, and if the volume DRAM was Rambus, that would become the commodity part, and we had to remain competitive in terms of both performance and cost, and if the indications were most of the DRAMs to be built in the world were going to be Rambus DRAMs, we better be compatible with them." (Polzin, Tr. 3941-42).

1545. Intel's selection of RDRAM was also significant to the PC OEMs. For example, Compaq, one of the largest producer of personal computers in the world stated in a November 1998 Compaq Memory Update states that Compaq was planning to incorporate RDRAM into all Compaq products. (RX 1302 at 8). Jacquelyn Gross, the Director of Memory Procurement at Compaq (Gross, Tr. 2265), testified that Compaq was planning to transition all of its products - desktops, workstations, etc. - to RDRAM at rate higher than it had ever changed memory technologies before. (Gross, Tr. 2324-27). As described in Compaq's documents, this was the "[m]ost aggressive, cross divisional memory technology shift ever planned at Compaq." (RX 1302 at 8). This was planned, even though Compaq considered RDRAM to be "revolutionary." (Gross, Tr. 2327).

1546. Similarly, an October 1998 internal presentation reflects Compaq's sentiment at the time that "Rambus is the clear next generation memory." (RX 1287 at 4). As Ms. Gross explained, the reason for this belief was that Intel had told Compaq that it was going to produce chip sets for RDRAM. (Gross, Tr. 2317-18). This was important to Compaq because 90% of Compaq's PC applications used Intel chipsets. (Gross, Tr. 2317-18).

1547. Both Intel and the OEMs recognized that in order for RDRAM to gain widespread market acceptance, the DRAM manufacturers needed to produce RDRAM in high volumes, which would drive down the price. As Peter MacWilliams of Intel explained, it was very important to the success of RDRAM that it be produced in volume so that its price be reduced:

> "Q. Okay. And how important was the price of RDRAM to its success during the time period of 1998 through 2001?
> A. It was very important. The price of RDRAM needed to come down to be very close to what the volume memory technology was in order for it to transition to be the mainstream technology, and it can be higher priced at introduction, it can be higher priced for the first part of the ramp, but OEMs had to have confidence that it was going to come down in order to make a larger commitment to it. So it became the determining factor as to how big the volume could be."
>
> Q. And one of the factors going into the price of RDRAM was the number of manufacturers who would produce it; is that right?
> A. Yes.
>
> Q. And one of the factors also would be whether the volume of the RDRAM being produced was sufficient to meet all of the demand?
> A. Yes."

(MacWilliams, Tr. 4933-34).

4. The DRAM Manufacturers Acknowledged – By Undertaking Extraordinary Efforts To Slow Or Block RDRAM's Market Acceptance – That It Is Intel's Decisionmaking, Not JEDEC Standardization, That Most Strongly Influences Marketplace Success.

1548. The DRAM manufacturers were well aware of Intel's power to create a *de facto* industry standard in selecting the RDRAM device. They also recognized that JEDEC standardization of a competing device would mean nothing if Intel did not change its course, and they knew that "Intel will not change course unless Rambus fails." (RX 870 at 1). Finally, the manufacturers recognized that they could not affect Intel's decision without concerted action; they "need[ed] some united strategy." (RX 808 at 2). As a result, both before and after Intel announced its selection of RDRAM, Intel faced resistance – organized, concerted resistance -- from the DRAM manufacturers.

1549. There has been substantial disagreement among the parties about the relevance in this case of evidence of concerted action by DRAM manufacturers that was intended to limit or prevent the marketplace success of RDRAM. While such evidence may not be *dispositive* of any material issue, it is *relevant* for at least four reasons.

1550. First, as noted above, it tends to show that it is Intel's selection, not JEDEC's standardization, that influences marketplace success for a DRAM device or technology.

1551. Second, it tends to rebut Complaint Counsel's argument that Rambus's motivation in asserting its patents in 1999 and 2000 should be viewed with suspicion

because the assertion of those patents came after RDRAM had supposedly failed to compete on the merits because of its (allegedly) inherently high manufacturing costs.

1552. Third, it tends to place in context the testimony of the executives and employees of DRAM manufacturers whose words and deeds are reflected in the evidence in question. Their interest in a finding that RDRAM failed on its merits, rather than as a result of collusive action, is likely to be affected by their participation in such action.

1553. Finally, while Complaint Counsel necessarily have focused their efforts on advancing the allegations made in the Complaint, this Court has a broader responsibility to the Commission and the public. If this Court receives evidence of collusive action by competitors that may have had the effect of reducing consumer choice, raising prices, or eliminating a superior technology, it is appropriate to bring that evidence to light. *See* FTC Act, 15 U.S.C. §§ 43, 45.

1554. With these points in mind, the Court has considered the evidence presented and finds reason to believe that the DRAM manufacturers: (1) were alarmed by the possibility that Intel's selection of the RDRAM would lower their profits and cause them to lose control of future DRAM design and implementation; (2) joined together in various consortia with the intention of impairing or blocking the successful marketplace launch of RDRAM; and (3) agreed to steps that resulted in lower production and higher prices of RDRAM, thus limiting and ultimately preventing RDRAM's success.

1555. In September 1996, for example, Hyundai executive and SyncLink Consortium chairman Farhad Tabrizi wrote an e-mail entitled "Emergency request for help!" that expressed a concern that "the real motive of Intel is to control DRAM manufacturers . . . ." (RX 778 at 1). According to Mr. Tabrizi, Intel's actions would give it "control of DRAMs and other CPU makers. We will become a foundry for all Intel activities and if Intel would like and desires to do business with us then we may get a small share of the their total demand." (RX 778 at 1).

1556. Mr. Tabrizi concluded his September 1996 e-mail by writing, "I urge you to please educate others and get their agreement to say 'NO TO RAMBUS AND NO TO INTEL DOMINATION.'" (RX 778 at 1).

1557. Mr. Tabrizi sent this email to one of his competitors, Jim Sogas at Hitachi, for comments. (Tabrizi, Tr. 9035). Prior to trial, he had testified that he was trying to get agreement from other DRAM manufacturers to say "no" to Rambus and "no" to Intel domination. (Tabrizi, Tr. 9038). At trial, however, he claimed that he could not recall sending the e-mail to other DRAM companies. (Tabrizi, Tr. 9037-38).

1558. In December 1996, at a SyncLink Consortium meeting attended by various manufacturers, Mr. Tabrizi stated that "[m]any suppliers are paranoid over the prospect of a single customer, e.g., Intel, having control of market. We can't resist such a possibility individually. We need some united strategy." (RX 808 at 2).

1559. At that same meeting, the assembled manufacturers agreed to hold a meeting of DRAM manufacturer executives in Japan in January 1997. (Tabrizi, Tr. 9041). Prior to the January 1997 meeting of executives, Mr. Tabrizi sent an email to other DRAM manufacturers that stated that the "Intel decision to go on a Rambus route was pure political and domination and control over the DRAM suppliers and not technical." (RX 802 at 3; Tabrizi, Tr. 9041-42). He then urged a unified effort to prevent Intel from gaining "control": "As I have mentioned many times before, Intel does not make DRAMs, we do. And if all of us put our resources together, we do not have to go on this undesirable path. The path of control and domination by Intel." (RX 802 at 3). He pleaded with the DRAM manufacturers to "stick together on this matter." (RX 802 at 3; Tabrizi, Tr. 9042-43).

1560. At the January 1997 meeting of DRAM executives, Mr. Tabrizi warned the assembled executives that if Intel succeeded in making RDRAM the next generation memory device, "DRAM manufacturers would loose control of specification and the gross margins will decline." (RX 849 at 44). Mr. Tabrizi conceded at trial that it was his view at the time that if Intel's selection of Rambus did not change, the gross margins of DRAM manufacturers would decline. (Tabrizi, Tr. 9048).

1561. Tabrizi's January 1997 presentation also warned that if Rambus became the next generation memory solution, "ALL DRAM COMPANIES WILL BECOME FOUNDRIES for a single source CPU manufacturer." (RX 849 at 44). The phrase "single source CPU manufacturer" was a reference to Intel. (Tabrizi, Tr. 9046).

1562. Micron engineer Terry Lee participated in the January 1997 DRAM executive meeting; his notes reflect that Siemens executive Dr. von Zitzewitz stated that Tabrizi's "[c]ontrol concerns are realistic." (CX 2250 at 2; Tabrizi, Tr. 9047-48). The notes also state that Dr. von Zitzewitz was "[d]isappointed with some statements accepting Rambus II. 0.1% royalty would have been OK. . . . The bottleneck of a small company is bad. Rambus is not acceptable." (CX 2250 at 2). Mr. Lee's notes were later made available to all members of the SyncLink Consortium (which was renamed the "SLDRAM Consortium" around this time). (Tabrizi, Tr. 9050; RX 855 at 1).

1563. After the January 1997 DRAM executive meeting, Mr. Tabrizi set up an e-mail "reflector" so that the DRAM supplier executives – ostensibly fierce competitors – could communicate among themselves via private e-mail. (Tabrizi, Tr. 9052; RX 938 at 1).

1564. Throughout 1997, 1998 and 1999, Mr. Tabrizi and others kept up regular communications about Rambus with their competitors, often sharing cost, production and planning information ordinarily maintained in confidence by true competitors. (Tabrizi, Tr. 9053; RX 916 at 1; RX 1181 at 1; RX 1155 at 1; RX 2191 at 1-2; RX 2192 at 2-3; RX 1105 at 1; RX 1386 at 1; RX 1487 at 4).

1565. In February 1998, for example, Jeff Mailloux of Micron wrote an email to Mr. Tabrizi stating that Mr. Mailloux had spoken to a reporter for an industry publication called EE Times. (RX 1105 at 1). Mr. Mailloux stated that "I told him that at any density and any process that is available in 1999, RDRAM is at least 30 percent cost adder for

Micron," and then encouraged Mr. Tabrizi to call the reporter with Hyundai's views. (RX 1105 at 1). Mr. Mailloux asked Mr. Tabrizi to "please visit me if I end up in jail. . . ." (*Id*.).

1566. Two months later, Mr. Mailloux sent another email to Mr. Tabrizi, attaching an article in an industry publication that had been written by Mr. Tabrizi's boss at Hyundai, Mark Ellsberry. (RX 1155 at 1; Tabrizi, Tr. 9055-56). Mr. Mailloux appears to have been concerned that the article by Mr. Ellsberry was pro-Rambus. (*Id*.). His e-mail states, "Mark seems to give a message at the end here, he only refers to DDR as a 'long shot' and does not even mention SLDRAM. Hope Hyundai has not caved in to the 'dark side.'" (RX 1155 at 1).

1567. In April 1998, Bert McComas, an industry consultant, gave an "exclusive" seminar for DRAM manufacturers about Intel's selection of RDRAM. (RX 1138 at 1; Tabrizi, Tr. 9061-62). Mr. McComas pre-cleared his seminar invitation and list of topics with Mr. Tabrizi. (Tabrizi, Tr. 9064).

1568. Mr. McComas's invitation asked its recipients not to forward the invitation to Rambus or Intel. (RX 1138 at 1). A few days later, Desi Rhoden (now Chairman of the Board of JEDEC) sent an email to Mr. Tabrizi about the attendance restrictions. (RX 1149; Tabrizi, Tr. 9064-65). Mr. Rhoden's e-mail stated that he knew McComas and that his "main focus appears to make sure that Rambus and Intel do not attend and therefore has been very restrictive on who can attend. If he says everyone except Rambus and Intel, then

it is restraint of trade; while if he says only suppliers, then most of who he wants can attend without there being a charge of restraint of trade." (RX 1149 at 1).

1569. During his April 1998 seminar presentation to the DRAM manufacturers, Mr. McComas stated that a manufacturer that chose to build RDRAMs was making a "guaranteed bad bet for margin enhancement" (RX 1482 at 12), and he stated that RDRAM "deepens [the manufacturer's] financial dilemma." (RX 1482 at 26). As a "possible strateg[y]," Mr. McComas suggested that DRAM manufacturers "tape out but do not fully productize or cost reduce" the RDRAM device, in the hopes of "resist[ing] popular deployment" of RDRAM. (RX 1482 at 34-35).

1570. After the seminar, Mr. McComas accepted an invitation to speak at the next SLDRAM Consortium Executive Meeting, so-called because company executives attend in addition to engineers and marketing personnel. (Tabrizi, Tr. 9066-8). In an April 17, 1998 email extending the invitation, Roberto Cartelli of Texas Instruments wrote to Mr. McComas, "I personally believe that your story on Intel and its relationship to Rambus is an excellent 'case for action' story to stimulate discussion among industry executives." (RX 1166 at 1; Tabrizi, Tr. 9068).

1571. Mr. McComas spoke at the June 25, 1998 SLDRAM Executive Summit about the problems faced by DRAM manufacturers. One of the "tactical" problems he identified was how to "Manage Price Competition, Profitability." (RX 1188 at 1). He also talked about how manufacturers could "Respond to the Strategic Threat of Intel/Rambus,"

and he asked the question, "Who will control the DRAM industry?" (RX 1188 at 1). McComas warned that "Intel/Rambus are using your money to take control of the DRAM industry" and that Intel would "[o]rchestrate early oversupply situation," and he emphasized that "[f]ragmented competition undermines all DRAM manufacturers." (RX 1188 at 26).

1572. Another industry consultant, Victor De Dios, also gave a presentation at the June 25, 1998 SLDRAM Executive Summit. (Tabrizi, Tr. 9071-72). Mr. De Dios told the assembled executives that "Many of the problems are industry problems, not company problems. Competition will not solve them." (RX 1204 at 4).

1573. During his presentation at the June 1998 "Executive Summit," Mr. McComas suggested that the DRAM manufacturers share their RDRAM production plans to determine whether there would be a demand-supply imbalance. (Tabrizi, Tr. 9073-74).

1574. After the meeting, Mr. McComas sought Mr. Tabrizi's advice on how to implement the project of collecting RDRAM production information. (Tabrizi, Tr. 9076). In an August 1998 email to Mr. Tabrizi, Mr. McComas sent a draft message to DRAM manufacturers which stated that "[d]uring the critical production ramp-up phase of Direct Rambus, DRAM vendors will need a constant flow of information to help make wise decisions and to walk the fine line between a pleasant shortage and a disastrous oversupply." (RX 1232 at 1).

1575. Mr. Tabrizi agreed that a shortage of RDRAM would please DRAM manufacturers because "[p]rices go up." (Tabrizi, Tr. 9077).

1576. The shortage of RDRAM was not pleasant to the PC OEMs, however, who recognized that for RDRAM to succeed, output of RDRAM had to increase. This led them to try to influence the DRAM manufacturers to increase RDRAM output. (RX 1287 at 4 ("Intel and major users have been trying to influence improved RDRAM output"). As Ms. Gross testified, Intel, Compaq, and other PC OEMs were trying to influence DRAM manufacturers to increase output of RDRAM and to align roadmaps with Intel's roadmap. These OEMs wanted an RDRAM production ramp-up so that they would have sufficient availability and lower RDRAM prices. (Gross, Tr. 2318-20).

1577. It was critical to Intel and to the PC OEMs that the DRAM vendors increase the volume of RDRAM because DRAM manufactures will shrink the highest volume parts first. (MacWilliams, Tr. 3837-38). The highest volume parts therefore have a cost advantage. (MacWilliams, Tr. 3837-38; RX 1532 at 1).

1578. In response, DRAM manufacturers agreed to manufacture RDRAM in larger volume. For example, in 1998, Hyundai committed to produce 30,000 RDRAM units for Compaq. (RX 1302 at 6). Similarly, Micron committed to produce 15,000 RDRAM units for Compaq. (RX 1302 at 6). Neither company, however, met these commitments. (Gross, Tr. 2327-29). According to Ms. Gross of Compaq, the DRAM manufacturers would not

"increase their output at the rate at which we needed to support our systems." (Gross, Tr. 2345-46).

1579. There is evidence that Mr. Tabrizi took steps in 1998 to ensure that RDRAM production stayed low so that the price difference between RDRAM and SDRAM stayed high. Tabrizi believed at the time that Intel would not change course unless RDRAM failed to get market penetration. (Tabrizi, Tr. 9082). He admitted that one way to cause RDRAM to fail to get market acceptance was if the OEMs were convinced that even if volumes went up, prices would not fall. (Tabrizi, Tr. 9083). If the OEMs were convinced of this, they would not adopt RDRAM. (Tabrizi, Tr. 9083).

1580. In the fall of 1998, Hyundai gave RDRAM price projections to its customers that were on the order of 50% to 60% higher than those reflected in its internal pricing documents. (Tabrizi, Tr. 9085-90; RX 1280; RX 1293A). Mr. Tabrizi encouraged Hyundai's sales force to distribute these higher prices to key accounts that were deciding whether to use RDRAM, DDR, or PC100 because "Intel was telling everybody that [RDRAM is] only going to be a 5 percent premium . . . . I wanted to make sure my OEM knows it's going to cost them more than 5 percent . . ." (Tabrizi, Tr. 9091).

1581. Mr. Tabrizi also admitted at trial that in October 1998, Hyundai gave RDRAM production forecasts to Intel that were deliberately inflated. (Tabrizi, Tr. 9092). (*See also* RX 1295 at 1 (internal Hyundai e-mail, copied to Tabrizi, that states that from the

perspective of the Hyundai America marketing group, "we can overstate our direct Rambus production so Intel can feel we are more aggressive on the ramp up."))

1582. Although Mr. Tabrizi would not admit it at trial, it is likely that when combined with Hyundai's inflated price forecasts, the inflated production numbers that Hyundai provided were intended to convince Intel that RDRAM prices would not come down *even if* production increased.

1583. Mr. Tabrizi also urged his fellow DRAM manufacturers to lie to Intel about production and pricing. A report prepared by an Infineon engineer about an October 1998 meeting attended by Mr. Tabrizi along with engineers from Micron and Infineon, states that "[a]ccording to Farhad Tabrizi, Hyundai has given Rambus ASP projections for end of next year of two to three times of todays SDRAM prices; they also gave to Intel a production projection of three times their actual plans => *They encourage every DRAM manufacturer to do the same in order to let Intel not generate a Rambus oversupply*." (RX 2192 at 2) (emphasis added). Mr. Tabrizi denied at trial that he had made the statements attributed to him in the Infineon trip report. (Tabrizi, Tr. 9097). Mr. Lee similarly denied being present when any such statements were made, although the Infineon trip report places him at the meeting. (Lee, Tr. 7028; RX 2192 at 1, 3)

1584. The DRAM manufacturers also met in October 1998 to discuss a proposal by Micron's Terry Lee that they agree to "a common roadmap" that the manufacturers would provide to chipset companies and PC OEMs. (RX 2191 at 1; RX 2192 at 3). Such a

"roadmap" would be "'signed' by all or most of the DRAM companies" and would show a joint commitment by the manufacturers to support DDR or SLDRAM instead of RDRAM. (*Id.*). The "main target" of such a joint roadmap would be to remove the "current uncertainty about the supply situation" among the chipset companies and PC OEMs. (RX 2191 at 1). A proposed joint roadmap was later circulated to numerous DRAM manufacturers by Micron. (RX 1423 at 1-2).

1585. Communications about RDRAM production between and among the DRAM manufacturers continued in 1999. In January 1999, Desi Rhoden sent a proposal to all of the major DRAM manufacturers regarding the transformation of the former SyncLink Consortium (by then called "SLDRAM Inc.") into a marketing-oriented organization to be called "Advanced Memory Inc." (RX 1373 at 1-3). "Advanced Memory Inc." was ultimately called "AMI2"; Mr. Rhoden became its President and Chief Executive Officer. (Rhoden, Tr. 260, 696-97, 1235). Mr. Rhoden stated that the focus of the new organization would be to "*co-ordinate* instead of developing new technology." (RX 1377 at 3) (emphasis added). He also stated that "[i]n the DRAM industry, we are clearly stronger together than we are individually." (RX 1373 at 1).

1586. Mr. Rhoden was obviously aware of the antitrust problems that arise when competitors "co-ordinate" their activities in an effort to be "stronger" market participants. (*Id.*). In Mr. Rhoden's view, however, the corporate form for the new organization would "indemnify member companies from antitrust while still providing a close working

environment for all." (RX 1373). He also suggested that an existing consortium of DRAM manufacturers called "M12" should "be folded under the corporation for anti-trust protection." (RX 1373 at 8).

1587. In a follow-up proposal to DRAM manufacturers by Mr. Rhoden, he again emphasized the need to provide antitrust protection for the "M12" consortium, although that organization had expanded and was now called "M14":

> "Marketing coordination has been the function of the M14 group and that group should be folded into the corporation, if for no other reason than to provide antitrust proteciton."

(RX 2284 at 2).

1588. While it is not clear whether the "M12" consortium was ever formally "folded under" Mr. Rhoden's company for "antitrust protection," and while it is not clear why anyone would believe that competitors could avoid antitrust liability for market coordination or other collusive activity simply by engaging in joint action within a corporate shell, it is clear from the activities of AMI2 and "M14" why Mr. Rhoden thought that "antitrust protection" was needed.

1589. In a March 1, 1999 meeting of the "M14" consortium, the DRAM manufacturers in attendance agreed to visit customers "as a group" to persuade them to utilize DDR instead of RDRAM. (RX 1390 at 2-3). The manufacturers also agreed to provide production "volume projections" of memory devices to Mr. Rhoden to allow him to produce a joint production forecast. (*Id.*). In addition, "a decision was made" that

"benchmarking" be "done for DDR SDRAM" on the issues of "Price-Cost-Availability." (RX 1390 at 2).

1590. It is likely that the requirement for "benchmarking" of the price of DDR SDRAM related to the manufacturers' need to introduce the new DDR SDRAM device at little or no premium over existing SDRAM prices, in an effort to convince the OEMs to abandon RDRAM in favor of SDRAM. (RX 1713 at 1). By June 2001, Mr. Rhoden was able to report to the DRAM manufacturers that comprised the AMI2 board that their efforts in this regard had been successful, for their Taiwanese customers had told Mr. Rhoden that the "DDR price is low enough." (RX 1848 at 2).

1591. "Benchmarking" the DDR price in an effort to avoid a price premium between DDR and SDRAM would only be a successful strategy, and would only lure OEM customers away from RDRAM, if the RDRAM price premium over SDRAM simultaneously stayed high. There is substantial evidence that DRAM manufacturers were *very* concerned in 1999 about the possibility that Samsung, in particular, might produce too much RDRAM, thus driving prices down.

1592. In April 1999, Micron's Kevin Ryan sent an e-mail to Terry Lee, Jeff Mailloux, Vice-President Bob Donnelly and others at Micron that attached an article describing Samsung's plans to produce as much as 40 million Rambus devices in 1999. (RX 1444 at 2). Mr. Ryan complained that Samsung had "broken ranks with the other suppliers" and had "sold their soul to the devil." (RX 1444 at 1). One of the recipients of

the e-mail, Mike Seibert, responded that "[t]hese guys are big trouble for us all. *If this thing gets into an oversupply mode with RDRAM things could get really ugly*." (RX 1444 at 1) (emphasis added). Mr. Seibert then asked Micron Vice-President Bob Donnelly if Samsung understood "what the Rambus/Intel biz model will do to our autonomy?" (*Id*.). Vice-President Donnelly responded that he had "certainly made the point with the officers that Intel . . . ultimately could control the DRAM industry." (*Id*.).

1593. Hyundai was also anxious to make Samsung understand the dangers of high volume RDRAM production. In a July 1999 email, Mario Martinez of Hyundai recommended to Mr. Tabrizi and others at Hyundai that "[w]ith Samsung building significant amounts of product, *we need to work with them to limit the supply in the market*, otherwise we both will be competing for market share which will result in an oversupply. We have to meet with Samsung and discuss our and their production plan, TAM analysis and targeted market share." (RX 1487 at 4 (emphasis added); Tabrizi, Tr. 9103). Mr. H.S. Ahn responded in the same email: "I have connection in Samsung. If I know what time you are available, I will try set up meeting with key person in Samsung in Seoul, Korea and I will try persuade them. [A]ctually they also have same idea for Rambus business compare with you." (RX 1487 at 4; Tabrizi, Tr. 9104).

1594. Hyundai marketing executive Farhad Tabrizi admitted at trial that he had told Sang Park, then the President and Chief Operating Officer of Hyundai, that he wanted to "kill" Rambus and force RDRAM from the market. (Tabrizi, Tr. 9105-07). Tabrizi

subsequently testified that what he meant by "killing" Rambus was really just "Rambus suicide, [with] me watching on the sideline." (Tabrizi, Tr. 9109). In his June 2000 email to Mr. Park, however, Mr. Tabrizi had written only of killing: "[i]f Intel does not invest in us, I really want to ask you to let me go back to my old mode of RDRAM killing. I think we were very close to achieving our goal until you said we are absolutely committed to this baby." (RX 1661 at 2).

1595. The "baby" was indeed killed. Jacquelyn Gross of Compaq testified that because the price of RDRAM did not decrease and because Compaq did not believe that it would decrease in the future, Compaq decided to abandon its plans and to shift to DDR. (Gross, Tr. 2339).

1596. Similarly, AMD abandoned plans to adopt RDRAM because, based on what they were told by DRAM manufacturers, it was clear that DDR, not RDRAM would become a commodity product. (Polzin, Tr. 4013).

1597. The Dell story is the same. In a February 2000 e-mail asking Micron to supply it with RDRAM, Dell stated that it was "committed to Rambus" but that its ability to incorporate Rambus devices in its PC's was "clearly limited by supply." (RX 1560 at 1). Looking ahead to the second half of 2000, Dell projected that with lower pricing, fully 40% of its market demand would be satisfied with RDRAM technology. (RX 1560 at 1).

1598. By May 2000, however, the situation had not improved, and Dell was considering moving into "a low key Rambus mode." (RX 1636 at 1). The Dell "message" was "pretty straightforward:"

> "Dell has booked our products over the last year around the assumption that RDRAM prices would decline and close on SDRAM. This would help us create demand . . . the memory vendors have shown no desire to drop prices, therefore we are reevaluating out strategies . . . so the message to them is drop prices or we will continue to decrease our RDRAM forecasts and we will architect next generation systems around DDR . . . we will give the memory vendors till the end of May to reply to our request . . . if they still have no desire to drop prices, we should push ahead rearchitecting chipsets around DDR."

(RX 1636 at 1). Prices did not come down, however, and Dell too shifted its roadmap to DDR.

1599. RDRAM failed to command significant market share despite the fact that it was the "best solution." (RX 1762 at 5; MacWilliams, Tr. 4931-32). As Peter MacWilliams of Intel put it:

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(MacWilliams, Tr. 5075 (in camera)).

1600. There is also evidence that *after* RDRAM failed to achieve marketplace success, the DRAM manufacturers felt able to *raise* DDR prices substantially, and that they did so through concerted action. In a November 26, 2001 e-mail entitled "OEM meeting update," a Micron manager named Kathy Radford described the efforts of Infineon and Samsung to raise DDR prices, and stated that Micron intended to try to raise its prices to "all of the OEM customers." (RX 1922A at 1). Ms. Radford then reported that "[t]he consensus from all suppliers is that if Micron makes the move, *all of them will do the same and make it stick*." (RX 1922A at 1) (emphasis added).

1601. Prices did, in fact, increase substantially in the months after Mr. Radford's e-mail. On March 1, 2002, **{IN CAMERA MATERIAL REDACTED}**

(RX 1991 at 1) (in camera).

1602. The evidence that was introduced during trial regarding concerted action by DRAM manufacturers to manipulate memory production and pricing in order to block RDRAM's market success and protect the manufacturers' "autonomy" is not summarized here in order to excuse any of Rambus's alleged conduct. The evidence is instead relevant for four reasons:

(1) it shows that Intel's choices, not JEDEC's standard-setting, tend to determine marketplace success in the DRAM industry;

(2) it rebuts Complaint Counsel's assertion that the RDRAM device failed on its merits because of what the DRAM manufacturers claimed were its inherently high manufacturing costs;

(3) it affects the credibility of the trial witnesses whose words and deeds are reflected in the cited exhibits; and

(4) evidence that manufacturers have engaged in collusive action with the intent and effect of reducing consumer choice, raising prices, or eliminating a superior technology from the marketplace is always of interest to the Federal Trade Commission.

C. Summary Of Findings Regarding Economic Implications Of The Evidence.

1603. Complaint Counsel has failed to meet its burden to prove that Rambus's alleged conduct was exclusionary.

1604. To be exclusionary, conduct must not make economic sense absent some gain from an adverse impact on competition.

1605. Conduct that has a legitimate business justification is not exclusionary.

1606. Legitimate business justifications exist for not disclosing information about pending patent applications. In fact, not disclosing information about pending patent applications may be procompetitive and enhance consumer welfare.

1607. These legitimate business justifications continue to be valid for firms that involved in standard-setting bodies. A firm that is involved in a standard-setting body may benefit from not disclosing information about pending patent applications for reasons that are independent of what standards are adopted by the standard-setting body.

1608. If Rambus did not disclose information to JEDEC about its pending patent applications, this conduct cannot be considered exclusionary because there is a legitimate business justification for such conduct.

1609. Further, applying the definition of exclusionary used by Complaint Counsel's economic expert, Complaint Counsel have not proven that Rambus's alleged conduct excluded equal or superior technologies.

1610. Although he concluded that equal or superior alternatives were excluded, Complaint Counsel's economic expert's definition of "equal or superior" was flawed and could not support a finding that such alternatives were excluded.

1611. Complaint Counsel's theory of exclusionary behavior in this case requires that Rambus acted in an irrational manner. The theory posits that knowingly Rambus withheld information about its pending patents in hopes of later being able to enforce its patents against JEDEC-compliant products. But the theory also requires that Rambus do so

knowing that its enforcement of its patents would trigger inquiries into its JEDEC-related conduct, leading to the discovery of its purposeful and knowing withholding of information, and thus to the inability to enforce its patents.

1612. Further, Complaint Counsel's economic expert made inadequate assumptions in forming his opinions. Although he assumed that Rambus violated JEDEC's rules by failing to disclose certain information, he made no assumptions as to what information should have been disclosed or when that disclosure should have occurred. Further, Complaint Counsel's economic expert's opinions have been undermined by the evidence.

1613. Complaint Counsel's economic expert premises his opinion that Rambus's conduct was exclusionary on the assumption that Rambus's conduct violated JEDEC's rules, but Complaint Counsel have not shown that enforcing JEDEC's rules would promote the purposes of the antitrust laws.

1614. Complaint Counsel have failed to meet their burden to show that Rambus's alleged conduct enhanced its market power.

1615. Complaint Counsel have failed to show that JEDEC's standardization of Rambus's technologies enhanced Rambus's market power.

1616. Rambus's technologies were superior to any of the alternatives, even accounting for Rambus's royalties. If they were acting rationally, JEDEC members would have adopted those technologies with full knowledge of Rambus's patents and royalty payments.

1617. Complaint Counsel have failed to show that JEDEC would have adopted alternative technologies had Rambus made the additional disclosures Complaint Counsel allege should have been made.

1618. Because JEDEC would have adopted the same standards had Rambus made the additional disclosures Complaint Counsel allege should have been made, and because Rambus's royalty rates are reasonable and non-discriminatory, Rambus's alleged conduct has not increased its market power.

CONCLUSIONS OF LAW

I. THE ALLEGED VIOLATIONS

1. The Complaint in this matter alleges that during the time Rambus was a member of JEDEC, JEDEC engaged in efforts to promulgate an industry standard for SDRAM and considered improvements to the SDRAM standard that ripened into the DDR SDRAM standard in the 1996-1999 time period. (Complaint, ¶¶ 27-28, 40). According to the Complaint, Rambus should have disclosed to JEDEC that it had filed or intended to file or amend patent applications relating to certain features of the SDRAM and DDR devices. (Complaint, ¶¶ 55-56, 64-70). The Complaint also asserts that Rambus misled JEDEC members into believing that Rambus had no actual or potential patent claims for the technologies being considered for standardization by JEDEC. (Complaint, ¶ 71). Finally, the Complaint asserts that if Rambus had disclosed to JEDEC that it had filed or intended to file patent applications relating to technologies being considered for standardization, JEDEC would have incorporated alternative technologies into its standards that avoided Rambus's intellectual property claims. (Complaint, ¶¶ 62, 65, 69).

2. Based on these allegations, the Complaint alleges three violations of Section 5 of the FTC Act. 15 U.S.C. § 45(a)(1). The first alleges that Rambus "has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices . . . whereby it has obtained monopoly power" in certain markets. (Complaint ¶ 122). The second alleges that Rambus "has willfully engaged in a pattern of anticompetitive and exclusionary acts

and practices . . . with a specific intent to monopolize" certain markets. (Complaint ¶ 123). The third alleges that Rambus "has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices . . . whereby it has unreasonably restrained trade" in certain markets. (Complaint ¶ 124).

3. Complaint Counsel represented to the Court that the first two alleged violations "are based on principles emanating from Section 2 of the Sherman Act – *i.e.*, the monopolization and attempted monopolization claims." (Complaint Counsel's Memorandum in Opposition to Respondent Rambus Inc.'s Motion for Summary Decision, filed Mar. 25, 2003 (Summary Decision Opp.), p. 33). Complaint Counsel represented that the third alleged violation is "one entailing proof falling somewhere in between that which would be required to establish, on the one hand monopolization, or on the other, attempted monopolization, under Section 2 of the Sherman Act." (*Id.* at 35). Complaint Counsel have thus represented that the third alleged violation requires proof of anticompetitive effects "more than the threatened effect that might suffice for attempted monopolization." (*Id.* at 36).

II. THE ELEMENTS OF THE ALLEGED VIOLATIONS

4. To prove monopolization, Complaint Counsel "must show that 1) the defendant possessed monopoly power in the relevant market and 2) the defendant willfully acquired or maintained this monopoly power by anticompetitive conduct as opposed to gaining that power as a result 'of a superior product, business acumen, or historical

accident.'" *Concord Boat Corp. v. Brunswick Corp.*, 207 F.3d 1039, 1060 (8th Cir. 2000) (quoting *United States v. Grinnell Corp.*, 384 U.S. 563, 570-71 (1966)).

5. To prove attempted monopolization, Complaint Counsel must prove "(1) that the defendant has engaged in predatory or anticompetitive conduct with (2) a specific intent to monopolize and (3) a dangerous probability of achieving monopoly power." *Spectrum Sports v. McQuillan*, 506 U.S. 447, 456 (1993).

III. THE BURDEN OF PROOF

6. In this case, Complaint Counsel allege that a patentee (Rambus) failed to make disclosures about its patent interests in the face of a duty to disclose and that through this conduct Rambus gained market power. Complaint Counsel seek an order barring Rambus from access to the courts to enforce its patents against certain products. Given the nature of these allegations and the nature of the remedy sought, precedent compels this Court to hold that Complaint Counsel must prove the essential elements of their claims by clear and convincing evidence. *See, e.g., Loctite Corp. v. Ultraseal, Ltd.*, 781 F.2d 861, 876-77 (Fed. Cir. 1985); Initial Decision, *In the Matter of VISX, Inc.*, Dkt. No. 9286 (filed May 27, 1999) (available at www.ftc.gov/os/adjpro/d9286/index.htm) ("*VISX* Initial Decision"), pp. 111, 139; *In the Matter of American Cyanamid Co.*, 72 F.T.C. 623, 1967 FTC Lexis 43 at *138-*145; *In the Matter of American Cyanamid Co.*, 63 F.T.C. 1747, 1963 FTC Lexis 77 at *224-5. *See also* Complaint Counsel's Post-Hearing Brief, *In the Matter of VISX, Inc.*, Dkt.. No. 9286 (filed April 7, 1999), p. 9 n.26 (noting that to find

either fraud or inequitable conduct, "[m]ateriality, intent and 'but for' all must be proved by clear and convincing evidence, evidence 'which proves in the mind of the trier of fact an abiding conviction that the truth of [the] factual contentions [is] highly probable.'") (citations omitted) (available in Commission file).

7. Although Complaint Counsel bears this heightened standard of proof, the Court finds that they have not met their burden even under a lesser, preponderance of the evidence standard.

IV. CONCLUSIONS OF LAW RELATED TO PATENT ISSUES

A. The Written Description Requirement

8. A patent application must include a specification. 35 U.S.C. § 111. According to the first paragraph of 35 U.S.C. § 112, the specification "shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention." 35 U.S.C. §§ 111, 112 ¶ 1. The first paragraph of § 112 contains three distinct disclosure requirements: written description, enablement, and best mode. *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1562 (Fed. Cir. 1991).

9. The written description requirement is satisfied if the specification as originally filed "describe[s] the claimed invention in sufficient detail that one skilled in the

art can reasonably conclude that the inventor had possession of the claimed invention." (MPEP § 2163(I) (citing *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563 (Fed. Cir. 1991)).

10. As part of the normal examination process of a patent application, patent examiners follow the guidelines set forth in the Manual of Patent Examining Procedure to check for compliance with the written description requirement. (MPEP § 2163). Patent examiners are instructed that "[a]n applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention." (MPEP § 2163(I) (citing *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997)). Patent examiners check for compliance with the written description requirement "from the standpoint of one of skill in the art at the time the application was filed." (MPEP § 2163(II)(A)(2) (citing *Wang v. Toshiba Corp.*, 993 F.2d 858, 865 (Fed. Cir. 1993).) In checking compliance with the written description requirement, patent examiners give claims their "broadest reasonable interpretation." (MPEP § 2163(II)(A)(1)). Patent examiners are instructed to reject any claim in a patent application that lacks written description support. (MPEP, § 2163(III)).

11. Patent examiners are instructed that written description issues often arise when determining whether new or amended claims in an application are supported by the specification or when determining whether claims in a continuation or divisional

application are entitled to the filing date of the original application. (MPEP §§ 2163(I), 2163.03). Patent examiners are further instructed that the purpose of the written description requirement is to "prevent an applicant from claiming subject matter that was not adequately described in the specification as filed." (MPEP § 2163(I)(B)).

12. Patent examiners are instructed that "[u]nder certain circumstances, omission of a limitation can raise an issue regarding whether the inventor had possession of a broader, more generic invention." (MPEP § 2163(I)(B) (citing *Gentry Gallery, Inc. v. Berkline Corp.*, 134 F.3d 1473 (Fed. Cir. 1998)). Patent examiners are further instructed that "[a] claim that omits an element which an applicant describes as an essential or critical feature of the invention originally disclosed does not comply with the written description requirement." (*Id.*). The determination of whether an element is "essential or critical" to the invention as originally disclosed is made from the point of view of a person of ordinary skill in the art. (*Id.*)

B. <u>The Definiteness Requirement</u>

13. The specification of a patent "shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention." 35 U.S.C. § 112, ¶ 2. Patent examiners are instructed to reject claims under this "definiteness" requirement if "the scope of the invention sought to be patented cannot be determined from the language of the claims with a reasonable degree of certainty." (MPEP § 2173.02).

C. Amendments, Continuation Applications And Divisional Applications

14. An amendment to a patent application may introduce new or amended claims, but such an amendment may not introduce new matter into the application's disclosure. 35 U.S.C. § 132. If an amendment adds new matter to the claims of an application, the patent examiner is instructed to reject the claims pursuant to the written description requirement. (MPEP § 2163.06(I)).

15. A "continuation" application that claims an invention disclosed in a prior application will have the same effect as though filed on the date of the prior application so long as (1) the prior application is still pending at the time the continuation application is filed, (2) the prior application names at least one inventor named in the continuation application, and (3) the disclosure of the invention claimed in the continuation application meets the requirements of the first paragraph of 35 U.S.C. § 112, including the written description requirement. 35 U.S.C. § 120.

16. "If two or more independent and distinct inventions are claimed in one application, the [PTO] may require the application to be restricted to one of the inventions." 35 U.S.C. § 121.

17. If the PTO restricts an application to one inventions, other inventions that had been claimed in that application may be made the subject of "divisional" application. A divisional application is entitled to the benefit of the filing date of the original application

only if the same requirements are satisfied as for a continuation application. (35 U.S.C. § 121).

18. There is no requirement that a divisional application disclose other divisional applications stemming from the same parent application.

D. Amending Pending Applications To Cover Competitor's Products Is Legitimate

19. "There is nothing improper, illegal or inequitable in filing a patent application for the purpose of obtaining a right to exclude a known competitor's product from the market; nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application." *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988).

20. Amending a pending patent application to cover a competing product is not acting in bad faith. *See Multiform Desiccants, Inc. v. Medzam, Ltd.*, 133 F.3d 1473, 1482 (Fed. Cir. 1998).

21. Broadening pending patent claims to cover a competitor's product does not indicate any intent to deceive. *See Emerson Elec. Co. v. Spartan Tool, LLC*, 223 F. Supp. 2d 856, 921 (N.D. Ohio 2002).

22. Amending a pending patent application to cover "a product containing a variant of the inventor's brainstorm" is "standard practice and has been for a long time."

MERGES, MENELL & LEMLEY, INTELLECTUAL PROPERTY IN THE NEW TECHNOLOGICAL AGE 225 (2d ed. 2000).

23. These principles apply in the DRAM industry as they do in any other. *See Texas Instruments, Inc. v. U.S. Int'l. Trade Comm'n*, 871 F.2d 1054, 1064-65 (Fed. Cir. 1989).

24. The patent laws ensure that the inventor can only claim inventions that were disclosed in the original written description: "While it is legitimate to amend claims or add claims to a patent application purposefully to encompass devices or processes of others, there must be support for such amendments or additions in the originally filed application." *PIN/NIP, Inc. v. Platte Chem. Co.*, 304 F.3d 1235, 1247 (Fed. Cir. 2002).

25. Rambus was entitled under the patent laws to attempt to amend its pending patent applications to cover technologies being incorporated in JEDEC standards.

E. The Claims In Rambus Applications And Patents Raised By Complaint Counsel Did Not Read On The Standards Or Presentations Alleged

26. It is "well settled that each element of a claim is material and essential, and that in order for a court to find infringement, the plaintiff must show the presence of every element or its substantial equivalent in the accused device." *Wolverine World Wide v. Nike, Inc.*, 38 F.3d 1192, 1199 (Fed. Cir. 1994) (internal quotation marks omitted).

27. The PTO determined that, among the claims raised by Complaint Counsel, claims 151, 159, 160, 164, and 165 of Rambus's '961 application and claim 151 of Rambus's '646 application were indefinite. Thus the PTO has determined that the scope of

the invention sought to be patented in those claims cannot be determined with a reasonable degree of certainty.

28. As the Federal Circuit has held, claims of Rambus's '961 application did not read on the JEDEC SDRAM standard. *Rambus Inc. v. Infineon Techs. AG*, 318 F. 3d 1081, 1103 (Fed. Cir. 2003). Claims in the '961 application were limited to the device identifier feature, which is not present in the SDRAM standard. (*Id.*). A license under the claims of the '961 application would not be necessary to practice the SDRAM standard. (*Id.*).

29. Likewise, claims 183, 184 and 185 of Rambus's '490 application did not read on the JEDEC SDRAM standard.

30. Claims 151, 152, 166 and 167 of Rambus's '692 application did not read on NEC's September 1994 presentation regarding "PLL enable mode."

31. Claim 151 of Rambus's '646 application did not read on the Hardell presentation, the Survey Ballot, or the Samsung presentation.

32. Claims 1 and 7 of the '327 patent do not read on the Hardell presentation, the Survey Ballot, the Samsung presentation, or the JEDEC DDR SDRAM standard.

F. A DRAM Engineer Reviewing Rambus's '898 Application Would Have Recognized That The Application Could Support Broad Claims Not Limited to Any Particular Bus Architecture

33. The patents that Rambus has asserted against DRAM manufacturers all issued in or after June 1999 and claim priority to the '898 application. (Stipulated Patent Tree).

34. The specification of the '898 application describes a preferred embodiment of Rambus's inventions. Complaint Counsel have referred to the preferred embodiment as including a "narrow, multiplexed, packetized bus." This does not mean, however, that Rambus's potential claims from the '898 application would be limited to such a bus architecture, for "it is well established . . . that broad claims supported by the written description should not be limited in their interpretation to a preferred embodiment." *Gart v. Logitech*, 254 F.3d 1334, 1343 (Fed. Cir. 2001).

35. As the Federal Circuit has held, "a multiplexing bus is only one of many inventions disclosed in the '898 application." *Rambus Inc. v. Infineon Techs. AG*, 318 F.3d 1081, 1095 (Fed. Cir. 2003). The Court further held that, in the prosecution history of the Rambus patents, the PTO "demonstrated an understanding of 'bus' that is not limited to a multiplexing bus." *Id.*

36. The claims that Rambus has asserted against the DRAM manufacturers are not limited to a narrow, multiplexed, packetized bus architecture structure. Indeed, the Federal Circuit unanimously reversed the district court that had construed "bus," for purposes of Rambus's asserted claims, as meaning a "multiplexed" bus. *Id.* at 1094. Interpreting "bus" as "what one of ordinary skill in the art at the time of the invention would have understood the term to mean," *id.* at 1088, the Federal Circuit held that "bus" as used in the claims of Rambus's asserted patents is simply "a set of signal lines to which a

number of devices are connected, and over which information is transferred between devices," *id*. at 1095, without any "multiplexed" or "narrow" or "packetized" limitation.

37. In issuing the asserted patents, the PTO determined that the claims in those patents are supported by the specification of the '898 application as originally filed, that is, the written description requirement is satisfied with respect to those claims.

38. Each claim of the patents issued to Rambus, including the asserted patents, is presumed valid. 35 U.S.C. § 282. In particular, there is a presumption that the written description requirement is satisfied for each of the issued claims. This includes a presumption that, from the point of view of a person of ordinary skill in the art, there is no essential element of Rambus's invention, as disclosed in the original '898 application omitted from the issued claims.

39. Complaint Counsel have not rebutted the presumption that the written description requirement is satisfied for each claim issued to Rambus. Therefore, the Court finds that a person of ordinary skill in the art, such as a DRAM engineer, would recognize from a review of the '898 application that Rambus was in possession of each of the inventions claimed in the patents Rambus has asserted against DRAM manufacturers as of the April 1990 filing date of the '898 application. A person of ordinary skill in the art would not have thought from reviewing the '898 application that any element omitted from the issued claims, such as a particular bus architecture, was an essential element of Rambus's inventions.

V. ANTICOMPETITIVE CONDUCT

40. The Complaint alleges that, through omissions, Rambus intentionally misled the members of JEDEC with regard to the possible scope of Rambus's pending or future patent applications, in violation of the purported JEDEC patent disclosure policy. (Complaint at ¶¶ 2, 47-55, 70-80). Complaint Counsel contend that this amounts to anticompetitive conduct.

A. There Was No Clear Duty To Disclose

41. To find a violation of the antitrust laws premised on a failure to disclose requires that the obligation to disclose be clear. *See VISX* Initial Decision at pp. 141-42 (finding no violation of Section 5 under antitrust theory based on failure to disclose because of an absence a clear duty to do so); *see also Infineon*, 318 F.3d at 1102 ("When direct competitors participate in an open standards committee, their work necessitates a written patent policy with clear guidance on the committee's intellectual property position. A policy that does not define clearly what, when, how, and to whom the members must disclose does not provide a firm basis for the disclosure duty necessary for a fraud verdict."); *A.C. Aukerman Co. v. R.L. Chaides Cons. Co.*, 960 F.2d 1020, 1043-44 (Fed. Cir. 1992) (holding that in a patent-law equitable estoppel case, silence alone will not create an estoppel unless there was a *clear duty to speak*, or somehow the patentee's continued silence reinforces the defendant's inference from the plaintiff's *known acquiescence* that the defendant will be unmolested") (emphasis added); *OddzOn Prods.,*

Inc. v. Just Toys, 122 F.3d 1396, 1404 (Fed. Cir. 1997) (holding that where the duty to disclose particular references to the Patent Office was "ambiguous" and "unclear," patentee could not, as a matter of law, have acted "with deceptive intent" when it failed to disclose references).

42. As summarized below and as set forth in detail in the Court's Findings of Fact, Complaint Counsel have not met their burden to prove that Rambus was under a clear duty to disclose to JEDEC or its members any information about its patent interests.

43. The manuals and policies that governed JEDEC's standardization activities while Rambus was a member encouraged, but did not require, disclosure of intellectual property interests.

44. The EIA legal guides do not require the disclosure of intellectual property interests.

45. The EIA manuals in effect prior to June 1996 contained no reference to any disclosure obligation.

46. The ANSI patent policy, which was officially adopted by the EIA at least as early as October 1995, encouraged but did not require the disclosure of intellectual property interests.

47. JEDEC manual 21-H, which was in effect when Rambus joined JEDEC and when the SDRAM standard was adopted, contains no reference to a disclosure obligation

and instead states that JEDEC standards "are adopted without regard to whether or not their adoption may involve patents on articles, materials or processes."

48. The application form used by Rambus when joining JEDEC contains no reference to a disclosure obligation.

49. JEDEC manual 21-I, published in October 1993, does refer – at least indirectly – to a disclosure obligation. Complaint Counsel did not show, however, that the 21-I manual had ever received the necessary EDEC approval.

50. JEDEC's ballot forms encouraged, but did not require, disclosure by members of relevant patents.

51. There is substantial evidence that JEDEC members and the JEDEC leadership understood during the time that Rambus was a JEDEC member that members were encouraged, but not required, to make a disclosure of their intellectual property.

52. Some JEDEC representatives believed that no disclosure was required as long as the member company ultimately licensed its relevant patents to all comers on reasonable terms.

53. The EIA/JEDEC patent policy at most required disclosure of "essential" patents.

54. In light of the Court's Findings in this matter, the evidence does not support a finding that Rambus was under *any* duty to disclose to JEDEC or its members any information about its patent interests.

B. The Evidence Does Not Show Anticompetitive Intent

55. To prevail on the monopolization claim, Complaint Counsel must prove that Rambus "willfully acquired or maintained this monopoly power by anticompetitive conduct." *Concord Boat*, 207 F.3d at 1060. That is, Complaint Counsel must prove that Rambus intentionally engaged in anticompetitive conduct. *See, e.g., United States Football League v. National Football League*, 842 F.2d 1335, 1359 (2d Cir. 1988) ("The willfulness element certainly requires proof of intent").

56. To prevail on the attempted monopolization claim, Complaint Counsel must prove that Rambus engaged in exclusionary conduct with "a specific intent to monopolize." *Spectrum Sports*, 506 U.S. at 456.

57. For either claim, the intent necessary is an intent to achieve or maintain a monopoly through anticompetitive as opposed to lawful means. *Illinois, ex rel. Burris v. Panhandle E. Pipe Line Co.*, 935 F.2d 1469, 1481 (7th Cir. 1991). Complaint Counsel must therefore prove that Rambus intended through its actions or omissions to mislead JEDEC, *i.e.*, that Rambus knowingly violated a JEDEC disclosure obligation in order to mislead JEDEC members. *See MCI Communications Corp. v. American Tel. & Tel. Co.*, 708 F.2d 1081, 1149 (7th Cir. 1983) (holding that representations about product must be "knowingly false or misleading before it can amount to an exclusionary practice"); *ILC Peripherals Leasing Corp. v. International Business Machines Corp.*, 458 F. Supp. 423, 442 (C.D. Cal. 1978) (granting directed verdict on monopolization and attempted

monopolization claims based on allegedly misleading statements where there was "nothing knowingly false" about the representations).

58. In light of the Court's findings in this matter, Complaint Counsel have failed to prove that Rambus knowingly violated a JEDEC disclosure obligation in order to mislead JEDEC members.

59. Complaint Counsel have also failed to prove that Rambus acted with anticompetitive intent.

C. The Evidence Does Not Show That Rambus Violated Any Duty To JEDEC Or That Such A Violation Would Be Exclusionary

60. Given their claims, Complaint Counsel must prove that Rambus violated a duty to disclose. Complaint Counsel must also prove that such conduct was "exclusionary." *See, e.g, Concord Boat Corp. v. Brunswick Corp.*, 207 F.3d 1039, 1060 (8th Cir. 2000).

1. Complaint Counsel Did Not Meet Their Burden To Prove That Rambus Breached A Duty To Disclose

61. Because the EIA/JEDEC patent policies in effect while Rambus was a JEDEC member encouraged, but did not require, a member to disclose its intellectual property interests, Rambus's alleged non-disclosure violated no policies or rules.

62. If the EIA/JEDEC patent policies in effect while Rambus was a JEDEC member did require disclosure of intellectual property interests, but required such disclosure only by *presenters* who were trying to encourage JEDEC's adoption of a

particular technology, Rambus violated no policies or rules, for Complaint Counsel have not proved that Rambus made any such presentations.

63. If the EIA/JEDEC patent policies in effect while Rambus was a member required disclosure of intellectual property interests only by members who did not license their patents on reasonable and non-discriminatory terms, then Rambus violated no policies or rules, for Complaint Counsel have not proved that Rambus's license terms are unreasonable or discriminatory.

64. If the EIA/JEDEC patent policies in effect while Rambus was a member required disclosure only of issued patents (and not patent applications) that read on or were "essential" to the use of technology proposed for standardization, then Rambus violated no policies or rules, for Complaint Counsel have not proved that Rambus had any such patents.

65. If the EIA/JEDEC patent policies in effect while Rambus was a member required disclosure of both patents *and* patent applications that read on or were "essential" to the use of a technology proposed for standardization, then Rambus violated no policies or rules, for Complaint Counsel have not proved that Rambus had any such patents *or* patent applications.

66. If the EIA/JEDEC patent policies in effect while Rambus was a member required disclosure of patents and/or patent applications where the JEDEC representative had "actual knowledge" that the claims of the patent or application covered the technology

proposed for standardization, then Rambus violated no policies or rules, for Complaint Counsel have not proved that Rambus's representatives had any such knowledge.

67. If the EIA/JEDEC patent policies in effect while Rambus was a member required disclosure of intellectual property interests at the time of balloting, as JC 42.3 Chairman Gordon Kelley testified, then Rambus could not have violated any policy or rule except as to programmable latency and programmable burst, for those are the only two features complained of by Complaint Counsel that were balloted while Rambus was a JEDEC member.

68. Rambus did not violate any JEDEC rule or policy simply by seeking or obtaining patent protection for inventions that related to JEDEC standards, for no rule or policy prohibited such patents.

69. Rambus did not have any undisclosed patents during the time that it was a JEDEC member that it was obligated to disclose.

70. Rambus did not have any undisclosed patent applications during the time that it was a JEDEC member that it was obligated to disclose.

71. Rambus had no duty to make any disclosure with respect to the DDR standard, because Rambus withdrew from JEDEC before work began on that standard.

72. In light of the Court's findings in this matter, Complaint Counsel have not met their burden of showing that Rambus violated any patent policy governing its conduct as a JEDEC member.

2. Complaint Counsel Have Not Proven That The Challenged Conduct Is Exclusionary

73. Exclusionary conduct must have "'no rational business purpose other than its adverse effects on competitors.'" *Concord Boat Corp. v. Brunswick Corp.*, 207 F.3d at1062 (quoting *Stearns Airport Equip. Co. v. FMC Corp.*, 170 F.3d 518, 522 (5th Cir. 1999)); *Neumann v. Reinforced Earth Co.*, 786 F.2d 424, 427 (D.C. Cir. 1986) ("predation involves aggression against . . . rivals through the use of business practices that would not be considered profit maximizing except for the expectation that (1) actual rivals will be driven from the market, or the entry of potential rivals blocked or delayed, so that the predator will gain or retain a market share sufficient to command monopoly profits, or (2) rivals will be chastened sufficiently to abandon competitive behavior the predator finds threatening to its realization of monopoly profits"); *see also Aspen Skiing Co. v. Aspen Highlands Skiing Corp.*, 472 U.S. 585, 609-11 (1985) (holding that conduct was exclusionary where the defendant failed to offer "any efficiency justification whatever" for its pattern of conduct, and where it was instead "willing to sacrifice short-run benefits and consumer goodwill in exchange for a perceived long-run impact on its smaller rival").

74. Where conduct has a legitimate business justification, it is not exclusionary and cannot be the basis for a monopolization or attempted monopolization claim. *See Technical Resource Servs. v. Dornier Med. Sys., Inc.*, 134 F.3d 1458, 1466 (11th Cir. 1998) (holding that there can be no Section 2 liability "if defendant's actions can be explained by legitimate business justifications"); *High Tech. Careers v. San Jose Mercury News*, 996

F.2d 987, 990 (9th Cir. 1993) ("If there is a valid business justification for [defendants'] conduct, there is no antitrust liability"); *Trace X Chemical, Inc. v. Canadian Industries, Ltd.*, 738 F.2d 261, 266 (8th Cir.1984) ("Acts which are ordinary business practices typical of those used in a competitive market do not constitute anti-competitive conduct violative of Section 2.").

75. The fact the alleged conduct violates JEDEC's rules or processes does not mean that it is exclusionary. *See Taylor Publ'g. Co. v. Jostens, Inc.*, 216 F.3d 465, 476 (5th Cir. 2000) ("Antitrust law is rife with . . . examples of what competitors find to be disreputable business practices that do not qualify as predatory behavior"); *Goldwasser v. Ameritech Corp.*, 222 F.3d 390, 400-01 (7th Cir. 2000) (plaintiff must state "freestanding antitrust claim" and cannot base its antitrust claim simply on violations of the 1996 Telecommunications Act, even though that Act was intended to promote "the development of competitive local markets"); *Olympia Equipment Leasing Co. v. Western Union Tel. Co.*, 797 F.2d 370, 376 (7th Cir. 1986) (exclusionary conduct cannot be determined by liability "in tort or contract law, under theories of promissory estoppel or implied contract . . . or by analogy to the common law tort" rules). Even if it did violate JEDEC's rules, the presence of a legitimate business justification would render the conduct not exclusionary. *See Conoco, Inc. v. Inman Oil Co.*, 774 F.2d 895, 905-06, 908-09 (8th Cir. 1985) (holding that legitimate business reasons rendered certain conduct not exclusionary but that same conduct did violate common law duty of good faith and fair dealings).

76. Prior to a 1999 amendment which allows patent applications to be published under certain circumstances 18 months after filing, 35 U.S.C. § 122 provided: "Applications for patents shall be kept in confidence by the Patent and Trademark Office and no information concerning the same given without authority of the applicant or owner unless necessary to carry out the provisions of any Act of Congress or in such special circumstances as may be determined by the Commissioner."

77. Not disclosing information about pending or future patent applications is an ordinary business practice typical of the semiconductor industry.

78. There are rational business reasons for not disclosing information about pending or future patent applications, and these reasons are unrelated to any adverse effects on competition.

79. Not disclosing information about pending or future patent applications enhances consumer welfare.

80. There were legitimate business justifications for Rambus not to disclose to JEDEC information about its pending patent applications or its intentions with regard to amending those applications or filing future patent applications.

81. Because of these legitimate business justifications, Rambus's alleged failure to disclose to JEDEC information about its pending patent applications or its intentions with regard to amending those applications or filing future patent applications was not exclusionary.

82. The goal of antitrust law is to protect economic efficiency. *See, e.g., Olympia Equipment*, 797 F.2d at 375. (stating that the emphasis of antitrust policy is "the protection of competition as a means of promoting economic efficiency"). The enforcement of certain private agreements, understandings, or rules may not advance those goals. *See, e.g., Madison Fund, Inc. v. Charter Co.*, 406 F. Supp. 749, 751 (S.D.N.Y. 1975) (antitrust law, "framed to preserve normal competitive forces," does not "police the performance of private contracts"). Complaint Counsel therefore bear the burden of proving that enforcement of JEDEC's rules and policies would promote economic efficiency.

83. Complaint Counsel have failed to prove that enforcing a JEDEC rule requiring disclosure to JEDEC information about a member's pending patent applications or its intentions with regard to amending those applications or filing future patent applications would further the goals of antitrust law.

84. A violation of a JEDEC rule requiring disclosure to JEDEC of information about a company's pending patent applications or its intentions with regard to amending those applications or filing future patent applications cannot be the basis for an antitrust violation.

VI. CAUSATION

85. Complaint Counsel must prove that Rambus engaged in anticompetitive conduct that caused or threatens to cause anticompetitive harm. *See, e.g., Dickson v. Microsoft Corp.*, 309 F.3d 193, 211 (4th Cir. 2002) ("The offense of monopolization

requires a showing of 'anticompetitive effect.'"); *United States v. Microsoft Corp.*, 253 F.3d 34, 58 (D.C. Cir. 2001) ("to be condemned as exclusionary, a monopolist's act must have an 'anticompetitive effect' . . . . "the plaintiff, on whom the burden of proof of course rests must demonstrate that the monopolist's conduct indeed has the requisite anticompetitive effect" (internal citations omitted)); *Taylor Publ'g. Co. v. Jostens, Inc.*, 216 F.3d 465, 474 (5th Cir. 2000) (in attempted monopolization case court looks at threatened effects "in light of the state of the market").

A. JEDEC Members Did Not Rely (At Least Not Reasonably) On The Alleged Failure To Disclose

86. To show causation, Complaint Counsel must prove that JEDEC members relied on the alleged failure to disclose. *See, e.g., Nobelpharma AB v. Implant Innovations*, 141 F.3d 1059, 1070-71 (Fed. Cir. 1998) (holding that to prove monopolization based on a patent allegedly procure by fraud on the Patent Office, the plaintiff must make a "clear showing of reliance, i.e., that the patent would not have issued but for the misrepresentation or omission" that "cause[d] [the] PTO to grant [an] invalid patent"); *American Professional Testing Serv. v. Harcourt Brace Jovanovich Legal & Professional Publs.*, 108 F.3d 1147, 1152 (9th Cir. 1997) (affirming judgment as a matter of law for monopolization claim based on false advertising because of lack of reliance evidence); 2 H. HOVENKAMP, ET. AL., IP AND ANTITRUST § 35.5, at 35-40 (2002) (stating that an antitrust plaintiff "must establish that the standard-setting organization adopted the standard in question, and would not have done so but for the misrepresentation or omission"); 3 P. AREEDA, ET. AL., ANTITRUST

LAW ¶ 782b (2002) (antitrust allegation based on a misrepresentation "implicates the usual tort issues with respect to nondisclosure (when is there a duty to speak?), the distinction between fact and opinion, the knowledge or due care of the speaker, the actual degree of reliance by those allegedly deceived, and the reasonableness of any such reliance").

87. Complaint Counsel must also prove that reliance was reasonable. *See, e.g., Grubb v. Federal Deposit Ins. Corp.*, 868 F.2d 1151, 1162 (10th Cir. 1989) ("The 'justifiable reliance' requirement ensures that a causal connection exists between the misrepresentation and the plaintiff's injury."); *American Professional Testing Serv.*, 108 F.3d at 1151 (monopolization case requiring evidence that reliance would be reasonable); *In re Indep. Serv. Orgs. Antitrust Litig.*, 85 F. Supp. 2d 1130, 1158 (D. Kan. 2000) (same).

88. JEDEC and its members were aware that Rambus was seeking broad patent protection for its inventions.

89. JEDEC and its members were aware that Rambus might obtain patent claims covering features being considered for standardization at JEDEC.

90. JEDEC members believed that Rambus would not be able to obtain or enforce broad patent claims because of prior art.

91. Rambus's early disclosures of inventions and technology gave notice that Rambus might succeed in obtaining patent protection for the four technologies in issue.

92. In light of the Court's Findings in this matter, Complaint Counsel have failed to prove that JEDEC members relied on Rambus's alleged failure to disclose.

93. In light of the Court's Findings in this matter, Complaint Counsel have failed to prove that any reliance by JEDEC members on Rambus's alleged failure to disclose was reasonable.

B. Rambus Did Not Acquire Any Market Power Through The Challenged Conduct

94. Complaint Counsel must prove that Rambus gained market power through the challenged conduct rather than from the superiority of its technologies. *See, e.g., United States v. Grinnell Corp*., 384 U.S. 563, 570-71 (1966) (requiring proof that defendant acquired monopoly power through anticompetitive conduct rather than a superior product).

95. In light of the Court's Findings in this matter, Complaint Counsel have failed to prove that Rambus gained market power through the challenged conduct rather than from the superiority of its technologies.

1. Complaint Counsel Have Not Proven That Standardization By JEDEC Enhanced Rambus's Market Power

96. Complaint Counsel must prove that standardization of Rambus's technologies enhanced Rambus's market power.

97. In light of the Court's Findings in this matter, Complaint Counsel have failed to prove that JEDEC's standardization of Rambus's technologies in the SDRAM standard enhanced Rambus's market power.

98. In light of the Court's Findings in this matter, Complaint Counsel have failed to prove that JEDEC's standardization of Rambus's technologies in the DDR standard enhanced Rambus's market power.

2. Complaint Counsel Have Not Proven There Were Acceptable Non-Infringing Alternatives

99. Complaint Counsel must prove the existence of acceptable, noninfringing alternatives for each of the two Rambus technologies incorporated in the SDRAM standard and for each of the four Rambus technologies in the DDR standard. *See, e.g.,* H. HOVENKAMP, ET. AL., IP AND ANTITRUST § 35.5, at 35-42 ("if the patent is one that actually confers an economic monopoly because of the absence of feasible noninfringing alternatives, it is the patent itself – not the patentee's failure to disclose it to the standard-setting organization – that restricts competition in the market").

100. Complaint Counsel must prove that an alternative is equal or superior to Rambus's technologies in cost-performance terms.

101. In light of the Court's Findings in this matter, Complaint Counsel have failed to prove that there were equal or superior alternatives to any of the four Rambus technologies.

102. Complaint Counsel bears the burden to show that alternatives are not covered by either Rambus's patents or third party patents. *See, e.g.,* Complaint Counsel's Memorandum in Support of Motion to Dismiss the Complaint, *In the matter of VISX, Inc.*, Dkt. No. 9286 ("Complaint Counsel *VISX* Br."), pp. 6-7 (requesting dismissal of complaint

seeking to enjoin enforcement of patent allegedly procured by fraud because Respondent received a new patent "that will give [Respondent] monopoly power in the technology market and market power in the apparatus market to the same extent as the old one").

103. In light of the Court's Findings in this matter, Complaint Counsel have failed to prove that any of their proposed alternatives were noninfringing.

104. In light of the Court's Findings in this matter, Complaint Counsel have failed to prove that there were acceptable, noninfringing alternatives that JEDEC could have adopted instead of the Rambus technologies.

105. Complaint Counsel have therefore failed to prove that the challenged conduct enhanced Rambus's market power.

3. Complaint Counsel Have Not Proven That JEDEC Would Have Selected Alternatives If They Existed

106. If acceptable, noninfringing alternatives existed, Complaint Counsel must prove that JEDEC would have adopted alternatives to Rambus's technologies had Rambus made the additional disclosures that Complaint Counsel contend should have been made.

107. In light of the Court's Findings in this matter, Complaint Counsel have failed to prove that JEDEC would have selected alternative technologies had Rambus made the additional disclosures that Complaint Counsel contend should have been made.

4. Complaint Counsel Have Not Proven That Rambus's Royalty Rates Were Not Reasonable And Non-Discriminatory

108. Since JEDEC would have adopted Rambus's technologies had Rambus made

the additional disclosures, Complaint Counsel must prove that Rambus's royalty rates were not reasonable and nondiscriminatory.

109. In light of the evidence above, Complaint Counsel have failed to prove that Rambus's royalty rates are not reasonable and nondiscriminatory.

5. Complaint Counsel Have Not Proven That The DRAM Industry Is Locked In

110. Complaint Counsel must prove that industry members are locked in to using the Rambus technologies because switching costs prohibit turning to alternatives. *See, e.g., Alcatel USA, Inc. v. DGI Techs., Inc.*, 166 F.3d 772, 783-84 (5th Cir. 1999) (rejecting monopolization claim because plaintiff failed to prove significant switching costs); *United Farmers Agents Ass'n, Inc. v. Farmers Ins. Exchange*, 89 F.3d 233, 237-39 (5th Cir. 1996) (affirming summary judgment because antitrust plaintiff failed to show market power (even though defendant held 100% of relevant market) because switching costs were low).

111. In light of the Court's Findings in this matter, Complaint Counsel have failed to prove that the DRAM industry is locked in to using the Rambus technologies. Accordingly, Complaint Counsel have failed to prove that the challenged conduct enhanced Rambus's market power.

VII. CONCLUSION

112. Complaint Counsel have failed to prove the essential elements of monopolization.

113. Complaint Counsel have failed to prove the essential elements of attempted monopolization.

114. Complaint Counsel have failed to prove that Rambus violated Section 5 of the FTC Act.

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