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1. it is reasonable to assume that a first-tier manufacturer would run only 20 million units of a product iteration (Geilhufe, Tr. 9562:10-9563:4; 9725:1-9726:23)	Tr. 1139:12-24 (Becker) Q. And how many chips do you actually produce at the fab a week? A. Given the product mix we're producing today and the production volumes, we produce about 3 and a half million chips a week. Q. And what type of chips are you producing? A. We're producing 256-megabit SDRAM and 256-megabit double data rate. Q. Of those 3 and a half million that you're putting out a week, how many of those would be SDRAM and how many at the double data rate? A. Current production quantities; it's about one-third SDRAM and two-third double data rate.
2. use of fixed CAS latency parts is difficult and costly because (a) based on all options contained in the JEDEC standard as adopted (and not on industry usage or practice), 3 separate parts would be required (Geilhufe, Tr. 9578:10-23, Tr. 9682:20-9683:2); (b) it would cost approximately $100,000 more than programmable CAS latency in design costs (Geilhufe, Tr. 9575:9-21); (c) it would require assumptions about the speed grade of the parts	Trial vol 33 (Lee) page 6626 Q. When you say a reduced set of features, do you recall any particular features that were reduced in SDRAM-Lite? A. Yes. They were proposing to go to a single fixed burst length and a single fixed CAS latency. Q. Now, based on your understanding in the late 1995 and early 1996 time frame, what, if any, were the advantages of an SDRAM-Lite? A. The advantages would be it would be faster to design and it would be cheaper to produce and test. Q. Can you please explain your understanding at that time of why SDRAM-Lite would be faster to design? A. It was simpler for us. We didn't have to design in different modes and consider all the combinations of burst lengths and CAS latencies for the timing data path. Q. And can you please explain your understanding at that time of why SDRAM-Lite would be cheaper to

EXHIBIT B

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(Soderman, Tr. 9347:8-9348:11); (d) it would interfere with a manufacturer's ability to speed grade parts (Soderman, Tr, 9348:12-9349:15); (e) it would add expense due to decreased die yield (Geilhufe, Tr. 9577:1-9578:9)	23 produce? 24 A. Yes, our test times would be reduced for 25 similar reasons. We would not have to test against page 6627 1 different burst lengths and CAS latencies and repeat 2 the entire test for them. 3 Q. Based on your understanding at that time, what, 4 if any, were the disadvantages of SDRAM-Lite? 5 A. I don't think there were any fundamental 6 disadvantages other than at that time there was still 7 some discussion as to which was the best burst length 8 and which was the best CAS latency. Trial vol 33 (Lee) page 6633 14 Q. Now, based on your assessment at that time, was 15 use of a fixed CAS latency acceptable from a technical 16 point of view? 17 A. Yes. 18 Q. Again, based on your assessment at that time, 19 was use of fixed CAS latency acceptable from a cost 20 perspective? 21 A. Yes. 22 Q. Based on your assessment at that time, was use 23 of fixed burst length acceptable from a technical point 24 of view? 25 A. Yes. page 6634 1 Q. And based on your assessment at the time, was 2 use of fixed burst length acceptable from a cost 3 perspective? 4 A. Yes. Trial vol 33 (Lee) page 6781 21 Q. And then if I could ask you to look at the 22 fourth bullet point, it reads, "Vendor testing at 23 multiple latencies for a given operating frequency adds

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	24 unnecessary cost." 25 Again, could you please explain your page 6782 1 understanding as of the March 2000 time frame of what 2 was conveyed by that bullet point? 3 A. Sure. What he was conveying was that as a 4 manufacturer, we had to test all combinations of 5 frequency and latency, a similar concern we had all the 6 way back to the SDRAM-Lite days, and I testified to 7 that earlier. So, he was saying this adds costs for us 8 to test this if it's not being used and that, 9 therefore, it would be unnecessary. 10 Q. If I could ask you to turn to the next page, 11 page 4, again with a caption Avoiding Programmable 12 Latency in SDR/DDR SDRAMs, and the top bullet point 13 reads, "One approach: offer devices with a fixed read 14 latency." 15 Do you see that? 16 A. Yes. 17 Q. Can you please explain your understanding at 18 the time of what was being proposed here? 19 A. Yes. What was being proposed was that there 20 would be one latency but not be programmable. 21 Q. So, in other words, that would be a fixed 22 latency? 23 A. Correct. 24 Q. If I could ask you to turn, please, to page 6 25 of CX-2758. Again, under the caption Avoiding page 6783 1 Programmable Latency in SDR/DDR SDRAMs, the first 2 bullet point on page 6 reads, "Another approach: offer 3 devices with programmable operating frequency; each 4 operating frequency range has a fixed read latency 5 associated with it."

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	6 Can you please explain your understanding at 7 the time of what was meant by that paragraph? 8 A. Yes. My understanding was that the proposal 9 was to have a programmable frequency instead of a 10 programmable latency, and for a given operating 11 frequency it would -- it would have a latency 12 associated with it.
3. use of fixed burst length parts is difficult and costly because (a) based on all options in the JEDEC standard as adopted (and not on industry usage or practice), it would require 4 separate parts (Geilhufe, Tr. 9594:25-9595:3); (b) it would involve extra photo tool costs of $50,000; (c) it would cost approximately $100,000 more than programmable burst length in design costs (Geilhufe, Tr. 9594:5-12)	See above.
4. based on all options in the JEDEC standard as adopted (and not on industry usage or practice), use of both fixed CAS latency and fixed burst length would require 12-15	See above.

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separate parts (Geilhufe, Tr. 9601:7-16)	
5. use of fixed CAS latency would not permit the mode register to be removed from the DRAM (Geilhufe, Tr. 9736:24-9737:19)	Trial vol 33 (Lee) page 6637 23 Q. Based on your understanding at the time that 24 you were reviewing and discussing this document in late 25 1995, did you understand that page 9 of CX-260 page 6638 1 explicitly explained how CAS latency would be 2 determined in a future SDRAM standard? 3 A. Yes. 4 Q. And what was your understanding of how page 9 5 proposed to determine the CAS latency of the future 6 SDRAM standard? 7 A. The last sentence of the paragraph discusses 8 the mode register, so it would be programmable through 9 the mode register just like the SDRAM device, and 10 specifically called out that there were fields 11 available for that. Trial vol 33 (Lee) page 6640 21 Q. If I could ask you, please, to turn to page 7 22 of JX-40, and I'd like to direct your attention to the 23 paragraph appearing underneath heading 8.1 towards the 24 bottom of page 7. It's the paragraph that carries over 25 to the top of page 8. The caption reads, page 6641 1 "JC-42.3-97-62B, DDR Mode Register Modification Item 2 815.02C." 3 Do you see that paragraph? 4 A. Yes. 5 Q. Is this one of the paragraphs that you reviewed

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	6 in late 1997 when you reviewed these minutes? 7 A. Yes. 8 Q. At the time you reviewed them, did you have an 9 understanding of this paragraph? 10 A. Yes. 11 Q. Could you please explain your understanding as 12 of late 1997 of what was reflected in this paragraph? 13 A. Sure. They voted to approve the DDR mode 14 register settings, and this aspect of the mode register 15 settings was centered around CAS latency. 16 Q. And based on this proposal, how was CAS latency 17 to be determined in the DDR SDRAM standard? 18 A. It was to be determined through mode register 19 setting, it was programmable through the mode register, 20 and the specific values in the mode register were 21 agreed upon at this time. 22 Q. Did this represent adoption of programmable CAS 23 latency in the DDR SDRAM standard? 24 A. Yes. Trial vol 33 (Lee) page 6787 13 Q. And if I could also ask you to look at the last 14 sub-bullet point on this page, "Multi-pin: Could be 15 used to select specific latency values as well as 16 whether to use Posted or normal CAS operation. 17 Trade-off: Higher overhead for pins/traces; lower 18 overhead associated with the mode register." 19 Do you see that? 20 A. Yes. 21 Q. I'm interested in the aspect of this related to 22 select specific latency values. Now, could you please 23 explain in a little bit more detail how this proposal 24 would select specific latency values? 25 A. Sure. The idea was instead of using -- in the

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	page 6788 1 multipin case, instead of using the mode register, the 2 DC level of a pin coming into the device could be used 3 to detect which latency to operate at, and also in one 4 form of the proposal, whether to use posted or normal 5 CAS operation.
6. (a) electrically blown fuses and anti-fuses are not reliable (Soderman, Tr. 9356:18-9357:2); (b) based on a survey of "maybe 50" out of "hundreds" of data sheets, only about 2 out of 50 SDRAMs appear to incorporate electrically blown fuses (Soderman, Tr. 9357:3-9358:1); (c) anti-fuse technology is not generally available in DRAMs (Geilhufe, Tr. 9582:20-9583:19; Tr. 9732:11-9734:21); (d) the use of laser blown fuses would lead to reduced yield due to speed distribution (Geilhufe, Tr. 9585:21-9586:9)	Trial vol 2 (Rhoden) page 427 14 Q. If I could direct your attention to the next 15 page, the bottom of page 71, and the last line of that 16 slide reads, "Fuse option for serial and interleaved 17 wrap mode." 18 Do you see that? 19 A. Yes, at the bottom of the page, I see. 20 Q. What was Samsung proposing with respect to the 21 fuse option for serial and interleaved wrap mode? 22 A. Samsung was proposing using a fuse option to 23 actually select between the type of burst mode, whether 24 it was interleaved burst mode or whether it was 25 sequential burst mode, and it's not important, but page 428 1 the -- which one is which, just that they were two 2 different modes of operation of the device, and they 3 were proposing for selecting between those two 4 different burst options. They were proposing using a 5 fuse to do that. 6 Q. How would a manufacturer use a fuse to select 7 between those options? 8 A. Well, a fuse is a pretty common -- 9 MR. DETRE: Objection, Your Honor. We have had 10 no foundation that the witness is expert in any kind of 11 manufacturing. It's not clear to me whether he's still 12 recalling now or -- 13 JUDGE McGUIRE: Overruled. I'll entertain

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	the answer if you have one. THE WITNESS: Thank you. The -- fuses are very common in DRAM, and fuses are common in perhaps many devices, but certainly in DRAM. Fuses are a common element that's used to select particular functions. Inside DRAMs that are shipped today, they use fuses to select bad bits or good bits. When they're testing a device, if they find a block that's bad, they would use a fuse to actually block that bad one out, and they always build the devices with some extra hanging around, and they will then program it such that they can replace the bad one for page 429 the good one. So, fuses were pretty common at this time, still are very common, and they were proposing using a fuse similar to the ones that were in common use at the time and still today to actually select this option. BY MR. OLIVER: Q. In late 1991 and early 1992, did you have an understanding as to whether it would have been possible to use fuses to determine the CAS latency and the burst length? A. I -- MR. DETRE: Objection, Your Honor. I think that Mr. Oliver is now getting into expert testimony from the witness and his opinion on what might have been possible, and Mr. Rhoden hasn't been designated as an expert. JUDGE McGUIRE: Overruled. THE WITNESS: As I said, fuses were a very common function that existed in all the memory at

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	that 20 time, so fuses would have been an easy selection, and 21 Samsung was very much in favor of it, because it would 22 be -- it would provide a simple device. 23 BY MR. OLIVER: 24 Q. Do you recall whether any JC-42.3 subcommittee 25 members proposed to use fuses to determine either CAS page 430 1 latency or burst length? 2 A. The discussion certainly took place. I was the 3 discussion leader for most of the SDRAM throughout its 4 development, and a fuse was one of the options that was 5 considered for a very long time, until we finally 6 settled on the register. So, yes, indeed, many people 7 did. 8 Q. By the way, would -- in terms of how use of 9 fuses was being discussed within 42.3 at the time, was 10 that being discussed as an alternative to programming 11 CAS latency or burst length through the mode register? 12 A. Certainly it would be, yes. Trial vol 27 (Kellogg) page 5130 10 Q. If we could move on to the fourth item that 11 we've listed here, use of fuses, could you please 12 explain briefly your understanding in the 1992 time 13 period of how fuses could be used to determine burst 14 length. 15 A. Yes, I can. 16 Fuses were a common method we had of doing 17 things such as replacing bad segments of the memory 18 already, and we could use what we called E-fuses or

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	19 electrical fuses blown at test or we could use a fuse 20 that was, say, a laser fuse, something that was broken 21 by some other means. The fuse would establish the 22 operating mode either at the very end of the 23 manufacturing process or during the test process. 24 Q. Would it be fair to say then that two or more 25 burst lengths would be designed into the part? page 5131 1 A. Yes, it would. 2 Q. And then how would the ultimate burst length 3 then be determined? 4 A. We would set an operating mode via the fuses 5 and that operating mode would be fixed. 6 Q. In other words, by blowing one or more fuses, 7 that would determine which of the designs you would 8 actually use in the feature? 9 A. That is correct. Trial vol 25 (in camera) (Macri) page 4763

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7. (a) based on the number of bits provided for in the JEDEC standard as adopted (and not on industry usage or practice), setting CAS latency and burst length via pins each would require three bits of information (Geilhufe, Tr. 9589:22-9590:6; 9599:8-9600:1)	Trial vol 33 (Lee) page 6787 6 Q. If I could ask you to turn to page 3, please, 7 under the caption DDR Proposal, the first bullet point, 8 "Use a dedicated pin (or pins) on DDR II SDRAMs to 9 select read latency (and therefore write latency as 10 well)." 11 Do you see that? 12 A. Yes. 13 Q. And if I could also ask you to look at the last 14 sub-bullet point on this page, "Multi-pin: Could be 15 used to select specific latency values as well as 16 whether to use Posted or normal CAS operation. 17 Trade-off: Higher overhead for pins/traces; lower 18 overhead associated with the mode register." 19 Do you see that? 20 A. Yes. 21 Q. I'm interested in the aspect of this related to 22 select specific latency values. Now, could you please 23 explain in a little bit more detail how this proposal 24 would select specific latency values? 25 A. Sure. The idea was instead of using -- in the page 6788

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	multipin case, instead of using the mode register, the DC level of a pin coming into the device could be used to detect which latency to operate at, and also in one form of the proposal, whether to use posted or normal CAS operation. Q. Now, how, if at all, did this proposal differ from the proposal of March 2000, CX-2758, that we looked at a moment ago? A. In this proposal, he's suggesting using an external pin to control it with a level. In the prior proposal, there was -- there was really two proposals. There was just have a fixed latency, and then the other one was to program frequency.
(b) it would be necessary to add pins (Geilhufe, Tr. 9724:16-21;9741:8-9742:1; Soderman, Tr. 9362:12-9363:3)	Trial vol. [7] (Sussman). Pages 1378-9 Q. Okay, based on your experience in the industry, did anyone ever propose using a no-connect pin to program CAS latency or burst length or any additional feature? A. There were a number of presentations on using the no-connect pin for other functions. Q. And specifically with respect to the presentations made at this meeting or the discussion of this concept at this meeting, were there any alternatives being proposed by others at the meeting, without necessarily going through each and every presentation? A. The answer to that one is yes.
8. running a single edge clock at a higher frequency (a) would cause significant clock distribution problems (Soderman, Tr. 9393:20-9394:8)	Trial vol 33 (Lee) page 6796 Q. What is this document? A. This is a JEDEC proposal for a clocking scheme for DDR2. Q. Is this a presentation that you made? A. Yes. Q. If I could ask you to turn, please, to page 13, and on that page, under the caption Single Data Rate

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	13 May Be Possible, the first bullet point reads, 14 "Pre-fetch and data rate is the same as DDR, but with a 15 full bandwidth single-edge clock." 16 Do you see that? 17 A. Yes. 18 Q. What did you intend to convey with that bullet 19 point? 20 A. I was proposing no change to the architecture 21 and data rate of the device. I was proposing to 22 increase the clock frequency. 23 Q. And with respect to the reference to the single 24 edge clock, what did you mean by that reference? 25 A. That the proposal was to use a single edge page 6797 1 clock as opposed to a double edge clock. 2 Q. If I could ask you to look at the next to the 3 last bullet point on that page, the bullet point reads, 4 "Today's silicon can handle single data rate 5 frequency." Underneath that, the last bullet point, 6 "400 megahertz clock chips are already available." 7 Do you see that? 8 A. Yes. 9 Q. Now, what did you mean by those two bullet 10 points? 11 A. At the time, the target for the design was 400 12 megabits per second, and in a DDR type of clocking, 13 that would correspond to a 200-megahertz clock used for 14 data capture, but in this proposal, I was proposing a 15 single data rate clock, which would be 400 megahertz, 16 and I was -- I was pointing out that the process 17 technology today could handle those kind of operating 18 frequencies for the clock, and there were also clock 19 chips available at those kind of speeds. 20 Q. Now, if I could ask you to turn, please, to 21 page 21, and under the caption Recommended Action, the 22 last bullet point reads, "Single data rate clocks."

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	23 Do you see that? 24 A. Yes. 25 Q. And again, what were you proposing here? page 6798 1 A. This was kind of the conclusion andy 2 recommendation based on the proposal that we eliminate 3 strobes and we go with single data rate clocks with a 4 different clocking scheme, which is described inside 5 the document. 6 MR. OLIVER: May I approach, Your Honor? 7 JUDGE McGUIRE: You may. 8 BY MR. OLIVER: 9 Q. Mr. Lee, I've handed you a document marked 10 CX-426. Do you recognize this document? 11 A. Yes. 12 Q. What is this document? 13 A. This is an email chain, but essentially it's 14 the meeting minutes from a conference call, a JEDEC 15 task group, to look at the clocking proposal that I had 16 proposed earlier. 17 Q. And did you participate in this conference 18 call? 19 A. Yes. 20 Q. And can you please explain in general terms the 21 results of this conference call? 22 A. Sure. We analyzed technical details of the 23 proposal, further explanation, discussed some concerns 24 and some analysis and tried to identify different 25 companies' preferences for this scheme and kind of what page 6799 1 to do next. 2 Q. Now, based on your recollection, do you recall 3 whether there was any consensus as to whether a single 4 data rate clock was technically feasible? 5 A. Yes, I recall.

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	6 Q. And what was your recollection? 7 A. It was generally considered feasible by most of 8 the companies but not all. 9 Q. Now, do you have a recollection as to whether 10 there was a consensus from the call in terms of what 11 should be done next? 12 A. Yes, I recall. 13 Q. And what is your recollection? 14 A. We felt there was still a little further work 15 that needed to be done, and we were going to try to 16 explore the idea a little bit further, and we were 17 going to prepare a summary at the next JEDEC meeting on 18 the progress of our call. Trial vol 33 (Lee) page 6802 12 Q. Now, based on your understanding at the time, 13 this would be the late 2000 to early 2001 time frame, 14 what was your understanding of the advantages of using 15 a single edge clock in the DDR2 standard at the time? 16 A. The advantages of a single edge clock? 17 Q. Yes. 18 A. For DDR2? There were several that were listed 19 in my original presentation, but they included -- we 20 felt it would have been easier to test using that and 21 not having a burst through strobe. We felt that we 22 would gain some benefits in the timing budget by not 23 having to worry about duty cycle control of the dual 24 edge clock. 25 Q. Now, focusing on the late 2000, early 2001 time page 6803 1 frame, what was your understanding at that time of the 2 potential disadvantages to using a single edge clock in 3 the DDR2 standard? 4 A. One of the challenges was to get adequate data

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	rate or get a high enough clock frequency using a single edge clock. Perhaps the biggest disadvantage was that it wasn't like DDR, and so it didn't have a direct migration path. That was fed back to us from some customers. Q. Can you please explain in more detail your understanding of why it was a disadvantage that using a single edge clock in DDR2 was not like DDR? A. Sure. There was concern that it would be difficult to design a controller that would support DDR and then this new scheme as well.
(b) would require on-DIMM clock circuitry and possibly an on-DIMM PLL/DLL, which would cost $3.80 (Geilhufe, Tr. 9609:17-9610:5)	Complaint Counsel has already introduced evidence anticipating, and attempting to rebut Mr. Geilhufe's cost figure relating to an on-DIMM PLL/DLL: <u>Tr. 6049:6 – 6050:19 (Goodman):</u> Q. Do you know how much a standard PLL costs? A. I believe it's generally around $1. Q. And in light of these modifications, would the PLL for Kentron be cheaper or more expensive? A. It's going to be more expensive, slightly more expensive, because it has more features. Q. Are these features complicated? A. No. Q. And the volume relationship that we described earlier would also be applicable to this situation? A. Yes. Q. Are you aware of what determines the cost of the PLL? A. No. Q. And who manufactures PLLs? A. There's several companies. The one that we're working with is called ICS. Q. So, that's the sole source for your PLL? A. Currently. Q. Are you currently in discussions with other

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	companies? A. Yes. Q. What is the purpose of the PLL in the QBM module? A. Again, it's a -- it provides the various clocks that are required in the technology, at 1x, 1x90 and 2x. Q. Is the $2 the initial cost? A. No, it will be slightly higher at launch, but we expect it to come down pretty rapidly in cost. Q. Do you have an expectation for at what volume that would occur? A. No, again, just we expect QBM to be in high volume fairly rapidly. Q. What do you mean by "high volume"? A. Again, the marketplace is very large, and we're looking at, you know, getting some type of market share that would immediately put us into a high-volume category.
9. moving the DLL to the module would cost $3.80 for the DLL (Geilhufe, Tr. 9613:13-25)	See above. Also, see Trial vol 33 (Lee) page 6646 23 Q. If I could direct your attention to the first 24 bullet point, Disadvantages of DLL, and then underneath 25 that, it reads, "Start-up time after power-up, after page 6647 1 exiting self-refresh, and after changing operating 2 frequency." 3 Do you see that? 4 A. Yes. 5 Q. Can you please explain your understanding at 6 the time that you reviewed this of that bullet point? 7 A. Sure. DLL, the way it works, it takes a 8 certain amount of time to lock, what we call lock. You 9 can consider it like a warm-up time for a car or 10 something. And after certain operations or upon 11 power-up, it took a certain amount of time before DLL 12 was guaranteed to be accurate.

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	13 Q. And if I could direct your attention to the 14 next bullet point, "Power-consumption," could you 15 please explain your understanding at the time you 16 reviewed this document of the disadvantage of DLL with 17 respect to power consumption? 18 A. Yes, the DLL circuitry used current and 19 therefore consumed power. 20 Q. The next bullet point reads, "Jitter." 21 Could you please explain your understanding at 22 the time you reviewed this of why that was a 23 disadvantage with respect to DLL? 24 A. Yes, I think the simple way to look at jitter 25 is it's the relative accuracy of the DLL, that it -- page 6648 1 rather than putting out something at a specific period 2 of time, it may meander about that time. 3 Q. The next bullet point reads, "Design 4 time/uncertainty." 5 Can you please explain your understanding at 6 that time of why that was a disadvantage of the DLL? 7 A. Yes, at that time there was concerns about the 8 amount of time it would take to get a DLL designed 9 right in the DRAM process, which was not really 10 optimized for this type of circuit, and some 11 uncertainty on the amount of time it would also take to 12 debug it and get it to where it's ready for production. 13 Q. And the then final bullet point under 14 Disadvantages of DLL reads, "Cost." 15 Could you please explain your understanding at 16 the time of that bullet point? 17 A. Yes, at that time our understanding is that, of 18 course, the DLL circuitry increased the die size and 19 had some increased die cost, but also there was concern 20 about how to test a part with a DLL at that time. Trial vol 33 (Lee) page 6663 13 Q. Now, if I could ask you to turn back to the

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	14 five components of the -- of variation of data valid 15 windows that Mr. Ryan outlined on page 20 of JX-29, and 16 focusing again on your understanding in the 1996 time 17 frame, what was your understanding of which, if any, of 18 these five components would be corrected for or 19 improved by an on-chip DLL? 20 A. The on-chip DLL would primarily improve 21 component number 3, which he's called chip-to-chip 22 skew. It would just improve the certainty of time in 23 which the data was output onto the bus from the DRAM 24 relative to the clock coming in. 25 Q. Now, again, based on your understanding in the page 6664 1 1996-1997 time frame, what, if any, effect would an 2 on-chip DLL have with respect to the -- to bullet 3 points 1, 2, 4 and 5 of Mr. Ryan's presentation? 4 A. It really wouldn't impact those. 5 Q. Now, in Mr. Ryan's presentation, what 6 technology, if any, was Micron proposing to help solve 7 the variation of the data valid window problem? 8 A. I think at this time he was primarily proposing 9 the use of echo clocks, which was a technique described 10 earlier where we're converting the problem of absolute 11 timing variance to relative timing variance.
10. SLDRAM was unable to design a high speed DRAM using Vernier circuitry, without an on-chip DLL (Soderman, Tr. 9412:22-9415:9)	Trial vol 33 (Lee) page 6622 5 Q. And I'd like to have you explain, if you could, 6 briefly your understanding of the SyncLink 7 architecture. 8 A. Okay, so can I assume that the architecture is 9 the same terminology used earlier?

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	10 Q. Yes, thank you, it would refer to the bus 11 structure, the devices and the interface. 12 A. Okay. SyncLink architecture was kind of a 13 combination between the narrow bus and wide bus. It 14 was in between the width of a DDR bus and that of a 15 Rambus, and it was a source-synchronous design that 16 used strobes. It used what we call verniers for a 17 thing we call leveling the bus by moving around timing 18 of the data onto the bus. 19 Is that the kind of information you want? 20 Q. Yes, thank you. Trial vol 33 (Lee) page 6623 9 Q. Now, you've discussed in general terms the -- 10 what I referred to as the SyncLink architecture. Based 11 on your understanding in the 1996 time frame, were 12 there any differences between the Rambus architecture, 13 as you understood it, and the SyncLink architecture? 14 A. Yes, there were many. 15 Q. Could you please explain your understanding of 16 those differences? 17 A. Sure. In the case of Rambus, they used this 18 loop back clock scheme and forwarded the clock with the 19 signal. SyncLink used, instead of a loop back clock, 20 they used a source-synchronous design, which used data 21 strobes, and the data strobes traveled in either 22 direction on the same signal, unlike the Rambus, which 23 always -- the clock moved in one direction. 24 SyncLink used a -- what we call an SL I/O, 25 which is -- I'm getting into some technical terms here, page 6624 1 but it's a push/pull driver scheme. Rambus used this

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	open drain driver. They're quite a bit different. SyncLink used these verniers for aligning when data would be put onto the bus. Rambus didn't do anything like that. They relied on the loop back clock for providing the timing of when to put the data on the bus. There were many differences in the protocol and the bank organization and things like that as well. Trial vol 33 (Lee) page 6667 In the 1996 or 1997 time period, were you familiar with the concept known as vernier? A. Yes. Q. Again, focusing on your understanding at that time, can you please explain what your understanding of the vernier method was? A. Sure. The vernier is -- you can consider it an adjustable delay element, so the way we would use it, it was one of the tools we liked to use to solve this timing uncertainty problem, is if the timing varied, you could use the vernier adjustable delay to compensate for that. So, if the timing increased, you could use less delay, and if the timing decreased, you page 6668 could use more delay, so the loop delay was constant. And so providing that constant loop delay created a less timing uncertainty and a larger data valid line back at the controller, and this was a technique we were looking at in SyncLink at the time. Trial vol 33 (Lee) page 6675 Q. Now, Mr. Lee, focusing on the 1996 and 1997 page 6676 time period, did you give any consideration during that time period as to whether a vernier method could be used to improve capture of data at the memory controller?

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	A. Yes. Q. And based on your understanding at that time, could a vernier circuit have been used in place of an on-chip DLL to facilitate capture of data at the memory controller? A. Yes. Q. Could you please explain your understanding at that time of how a vernier method could have been used to do that? A. Sure. There's really a couple places we could have put a vernier to solve the timing uncertainty of data coming out of the DRAM, which is what the DLL was trying to address. One is we could have put it in the DRAM itself, and as the delay started to increase, we could reduce the delay -- the number of delay elements in the vernier inside the DRAM to offset that so that there was a more constant output data time. The other thing we could do is we could put it in the controller itself, and as the delay coming -- of the data coming back from the DRAM started to increase, we could reduce the number of delay elements in the page 6677 controller to offset that, so that once again the loop time remains nearly constant. Q. Focusing again on the 1996 and 1997 time period, during that time period, did you ever consider the advantages of using vernier circuits rather than on-chip PLL or DLL to facilitate capture of data at the memory controller? A. Yes. Q. And based on your understanding at that time, what were the advantages of using a vernier circuit rather than on-chip PLL or DLL? A. They had some of the same advantages of the

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	13 DLL, that might be easy for me to contrast it. While 14 they both had the disadvantages of some power and die 15 size utilization, with the vernier, we didn't have this 16 lock time problem. We didn't have to wait for it to 17 lock. 18 And also, we felt that with the vernier, we 19 could put it on the controller so it didn't have to be 20 replicated on every DRAM, and by doing that we could 21 reduce the cost and complexity. 22 Q. Now, compared with using on-chip PLL or on-chip 23 DLL, based on your understanding at that time, did you 24 understand there to be any disadvantages with using 25 vernier rather than on-chip PLL or DLL? page 6678 1 A. I would say the disadvantages were similar, as 2 I mentioned, to the DLL with power and die size if it 3 was included on the DRAM. I think there was probably 4 more familiarity in the DRAM business with DLL than 5 vernier, but other than that, there's no disadvantage. 6 Q. Now, based on your understanding at that time, 7 did you regard use of the vernier method to be an 8 adequate substitute for use of an on-chip PLL or 9 on-chip DLL from a technical point of view? 10 A. Yes. 11 Q. And again, based on your understanding at the 12 time, did you regard use of the vernier method to be an 13 acceptable alternative to on-chip PLL or DLL from a 14 cost perspective? 15 A. Yes.
11. because the proposed alternatives didn't include circuit designs,	

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they were poorly thought out (Geilhufe, Tr. 9673:17-9674:5)	
12. DDR II (a) expands the use of programmable CAS latency (Soderman, Tr. 9351:7-9353:3)	Trial vol 33 (Lee) page 6785 5 Q. Mr. Lee, if I could ask you to turn, please, to 6 the next page, page 9, and here there's a -- the 7 caption The real problem: DDR II -- hold on just a 8 minute. 9 If we could please pull up CX-2758, page 9. 10 Mr. Lee, with respect to page 9, the caption 11 The real problem: DDR II, can you please explain just 12 in general terms your understanding at the time of what 13 the proposal meant on this page? 14 A. Yeah, he was trying to explain the CAS latency 15 issue as it related to DDR2, and he was providing some 16 discussion of the issues behind CAS latency as exists 17 for DDR2. 18 Q. Based on your understanding, what was the 19 reference to "the real problem" with DDR2 on this page? 20 A. My understanding, the reason Kevin worded it 21 this way, he was concerned about bringing -- trying to 22 bring changes for SDR and DDR and even DDR2 to the 23 committee at this point of the process. He was 24 concerned that the committee would -- would strongly 25 reject it, perhaps with some hostility. So, he was page 6786 1 trying to -- I believe in his words -- trying to ease 2 into it. Trial vol 33 (Lee) page 6792 18 Q. Okay. Now, again, excluding any discussions

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	19 you had with counsel or excluding any -- excluding any 20 discussions following instructions from counsel, did 21 you have any discussions between March and July of 2000 22 as to whether Micron should present a second time its 23 proposal to use a fixed CAS latency at JEDEC? 24 A. Not regarding fixed CAS latency. 25 Q. Did you have any discussions between March and page 6793 1 July of 2000 as to whether Micron should repeat the 2 proposal it made to JEDEC of March 2000? 3 A. I had a discussion with Kevin related to what 4 he felt should happen. 5 Q. Now, as part of that, did you also -- did you 6 provide a recommendation as to whether you thought 7 Micron should repeat its March of 2000 presentation? 8 A. I didn't make a recommendation. 9 Q. Did you have a belief at that time as to 10 whether Micron should repeat its March of 2000 11 presentation? 12 A. I did. 13 Q. What was your belief at that time? 14 A. Based on Kevin's report of how the first 15 showings went, my belief was that there was no 16 opportunity there to be able to change that at JEDEC.
(b) initially planned to use a single burst length, but subsequently reverted to programmable burst length (Soderman, Tr. 9369:12-23)	Trial vol 33 (Lee) page 6779 7 Q. Mr. Lee, if I could ask you to turn to page 2 8 of CX-2758, the first bullet point on page 2, "The 9 objective of this presentation is to propose an 10 approach for reducing the complexity and cost 11 associated with read latency operation described in the 12 current DDR II specification." 13 Do you see that? 14 A. Yes.

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	MR. OLIVER: Your Honor, and I will have a question after this. BY MR. OLIVER: Q. The second bullet point reads, "The first part of the presentation discusses possible methods for eliminating programmable read latency from existing SDR and DDR devices; this discussion serves as useful background for the DDR II proposal." Mr. Lee, what I'm trying to understand is that on the cover, it refers to DDR2, and yet here on page 2, it makes reference to SDR and DDR as well as DDR2, page 6780 and actually, let me ask one clarification question first. The reference to SDR on page 2, that refers to the SDRAM standard. Is that right? A. Yes. Q. And what I'm trying to understand is whether this presentation was directed at the SDRAM and DDR SDRAM standards as well as DDR2 or was it directed just at the DDR2 standard? A. It was directed at all three. Q. If I could ask you to turn, please, to page 3, and under the caption Avoiding Programmable Latency in SDR/DDR SDRAMs," the second bullet point reads, "Users typically operate a device at the lowest (fastest) read latency possible at a given operating frequency." Do you see that? A. Yes. Q. Can you please explain your understanding at the time of what was meant by that bullet point? A. Yes. It meant that for a given clock rate that they were using the device, they would try to operate at a CAS latency that was the lowest acceptable for that clock rate given the device capabilities.

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	24 Q. Now, what, if any, was the relevance at that 25 point to his presentation? page 6781 1 A. The relevance was that for a given clock rate, 2 they normally didn't change the latency. They worked 3 with a latency -- one common latency for that clock 4 rate. 5 Q. If I could direct your attention to the next 6 bullet point, it reads, "DIMMs are typically designated 7 as being for one combination of operating frequency and 8 read latency." 9 Do you see that? 10 A. Yes. 11 Q. Can you please explain your understanding of 12 that bullet point at that time? 13 A. Sure. What he's referring to is that there was 14 a trend for, say, a PC100 DIMM, there would be 15 typically say a CAS latency of two module, and that's 16 what we typically shipped, and then similar trend with 17 DDR. So, he's saying that typically, although these 18 things were programmable, there was really one 19 operating frequency and latency that was being used for 20 a given system. 21 Q. And then if I could ask you to look at the 22 fourth bullet point, it reads, "Vendor testing at 23 multiple latencies for a given operating frequency adds 24 unnecessary cost." 25 Again, could you please explain your page 6782 1 understanding as of the March 2000 time frame of what 2 was conveyed by that bullet point? 3 A. Sure. What he was conveying was that as a 4 manufacturer, we had to test all combinations of

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	frequency and latency, a similar concern we had all the way back to the SDRAM-Lite days, and I testified to that earlier. So, he was saying this adds costs for us to test this if it's not being used and that, therefore, it would be unnecessary. Q. If I could ask you to turn to the next page, page 4, again with a caption Avoiding Programmable Latency in SDR/DDR SDRAMs, and the top bullet point reads, "One approach: offer devices with a fixed read latency." Do you see that? A. Yes. Q. Can you please explain your understanding at the time of what was being proposed here? A. Yes. What was being proposed was that there would be one latency but not be programmable. Q. So, in other words, that would be a fixed latency? A. Correct. Q. If I could ask you to turn, please, to page 6 of CX-2758. Again, under the caption Avoiding page 6783 Programmable Latency in SDR/DDR SDRAMs, the first bullet point on page 6 reads, "Another approach: offer devices with programmable operating frequency; each operating frequency range has a fixed read latency associated with it." Can you please explain your understanding at the time of what was meant by that paragraph? A. Yes. My understanding was that the proposal was to have a programmable frequency instead of a programmable latency, and for a given operating frequency it would -- it would have a latency associated with it.

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(c) limits the use of the burst terminate command because of timing difficulties (Soderman, Tr. 9376:19-9377:20)	Mr. Macri, one of Complaint Counsel's witnesses, testified to this exact point during direct examination (prior to the testimony of both Professor Jacob and Mr. Lee). Complaint Counsel could have asked the later witnesses to address the issue. Tr. 4774:11 – 4775:6 (Macri) **[in camera]**