UNITED STATES OF AMERICA
BEFORE FEDERAL TRADE COMMISSION

PUBLIC

In the Matter of RAMBUS INCORPORATED, a corporation.	Docket No. 9302

COMPLAINT COUNSEL'S MOTION FOR ACCEPTANCE OF CORRECTED VERSION OF "ATTACHMENT A" TO COMPLAINT COUNSEL'S MOTION FOR ADDITIONAL ADVERSE INFERENCES AND OTHER APPROPRIATE RELIEF NECESSARY TO REMEDY RAMBUS INC.'S INTENTIONAL SPOLIATION OF EVIDENCE

On March 27, 2003, Complaint Counsel Filed a Motion for Additional Adverse Inferences and Other Appropriate Relief Necessary to Remedy Rambus Inc.'s Intentional Spoliation of Evidence ("Motion"). Upon reviewing "Attachment A" to the Motion, Complaint Counsel discovered typographical errors and one duplicate adverse inference. Accordingly, Complaint Counsel requests that Your Honor accept the corrected version of "Attachment A," filed herewith, as a substitute for the version filed initially.

Respectfully submitted,

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COUNSEL SUPPORTING THE COMPLAINT

Dated: March 27, 2003

ATTACHMENT A
Proposed Adverse Inferences

Rambus's Business Strategy

1. From its inception, Rambus's business strategy has been to obtain high royalties through licensing its technology for use in a widely adopted DRAM industry standard.

2. From its inception, Rambus knew that industry standards play a critically important role in the DRAM marketplace.

3. From its inception, Rambus knew that at any given time there is likely to be only one dominant industry standard for commodity (as opposed to specialized) DRAMs, and that all commodity DRAM producers are forced by market forces to produce products complying with the dominant industry standard.

4. From its inception, Rambus knew that the most valuable DRAM-related patents are ones that cover technologies that must be used to be in compliance with the dominant industry standard.

5. Through most of the 1990s, Rambus's primary business strategy was to establish its proprietary RDRAM architecture as the dominant industry standard for modern DRAM devices, and then to charge high royalties for the use of RDRAM technology.

6. In or around early 1992, Rambus developed an alternative plan for obtaining high royalties associated with DRAM industry standards – namely, a plan to secure patent rights over alternative standards that were emerging to compete with RDRAM, including but not limited to JEDEC's work on SDRAM standards.

7. From roughly mid-1992 through late 1999 or early 2000, Rambus simultaneously pursued two alternative strategies for obtaining patent rights over widely adopted DRAM industry standards: (1) its public strategy of achieving market success with its RDRAM proprietary technology; and (2) its private and secretive strategy of securing patent rights over JEDEC's RAM standards.

8. Rambus referred to the second strategy as "playing the IP card" against DRAM markers.

9. Rambus's central business objective throughout the 1990s was to work aggressively

toward achieving market success for RDRAM, with the understanding that if failed to succeed with RDRAM, it would "play the IP card" – i.e., assert patent claims over competing standards, principally including JEDEC's SDRAM and DDR SDRAM standards.

10. From roughly late 1996 through sometime in 1999, Rambus placed great hope and confidence in the potential for RDRAM – with the strong backing of Intel – to succeed as the dominant DRAM industry standard.

11. Rambus's strategy was to conceal its JEDEC-related patents and patent applications unless or until its relationship with Intel "blew up."

12. Rambus's relationship with Intel did "blow up" in 1999, and the same month that this occurred Rambus shifted aggressively to its alternative business strategy of "playing the IP card" – i.e., enforcing JEDEC-related patents – against DRAM makers, and others whose products interoperate with DRAMs (e.g., chipsets).

13. In enforcing its JEDEC-related patents against DRAM makers, Rambus was determined to charge royalties higher than the royalties that it charged for its proprietary RDRAM technology.

14. Rambus set its royalties for SDRAM and DDR SDRAM devices at levels (.75% and 3.5%, respectively) that it believed would cause these products to be less competitive vis-a-vis RDRAM.

15. Thus, in asserting JEDEC-related patents, Rambus sought to achieve two primary goals: (1) collecting massive revenues off of the production of DRAMs complying with the industry-dominant JEDEC standards, and (2) reducing competition for its proprietary DRAM architecture.

16. Through its assertion of JEDEC-related patents, Rambus also has sought to reduce or eliminate JEDEC's continuing influence over DRAM-related industry standards.

Rambus's Motives for Joining and Participating in JEDEC

17. Rambus joined JEDEC as part of its business strategy of obtaining high royalties for use of its technology in widely adopted DRAM industry standards.

18. Very early on in its JEDEC membership, Rambus considered the possibility of presenting its RDRAM technology to JEDEC as a proposed standard, but later concluded that this approach would be inconsistent with Rambus's licensing-based business model, inasmuch as having RDRAM standardized by JEDEC would restrict Rambus's flexibility in licensing to whomever it wished on whatever terms it wished.

19. Shortly after joining JEDEC, Rambus concluded that the organization's ongoing efforts to develop specifications for a new synchronous DRAM standard would involve use of technologies that Rambus believed to be covered by its existing patent applications, or which could be covered through amendments to such pending applications.

20. From mid-1992 through the present, Rambus has engaged in efforts, in conjunction with its patent attorneys, to amend existing patent applications to cover technology features that were being discussed within JEDEC for potential use in JEDEC's RAM standards.

21. Rambus chose to remain in JEDEC for over four years in part because of the benefits it derived from being present to observe JEDEC presentations, witness technology-related debates among JEDEC members, and glean information about the future direction of JEDEC's standardization efforts – such information helped Rambus in its efforts to write new and amended patent claims designed to cover technologies that it knew to be, or expected would be, encompassed by JEDEC's RAM standards.

22. Rambus also remained in JEDEC because it knew that its presence and participation, combined with its pattern of misleading conduct, substantially increased the likelihood that JEDEC would proceed to develop DRAM-related standards incorporating technologies over which Rambus could later assert patent rights.

Rambus's Knowledge of JEDEC's Purposes, Rules, and Procedures

23. Rambus knew that JEDEC was firmly committed to the principle of developing "open" standards, free to be used by anyone, and unencumbered – wherever possible – by proprietary patent claims.

24. Rambus knew that JEDEC and its members maintained a commitment to avoid the incorporation of patented technologies into its published standards.

25. Rambus knew that JEDEC's rules and procedures imposed upon all participants a duty to participate in good faith.

26. Rambus knew that JEDEC prohibited the incorporation of patented or patent-pending technology into a standard unless the patent owner, or applicant, committed in advance to license the technology on royalty-free or otherwise reasonable and non-discriminatory terms.

27. Rambus also knew that providing such assurances alone did not guarantee that the patented or patent-pending technology would be used in JEDEC's standards.

28. Rambus knew that JEDEC would not use any patented or patent-pending technology in its standards (even after securing such assurances) unless, after careful review and consideration, it was determined that use of the patented or patent-pending technology was well justified.

29. Rambus knew, throughout its membership in JEDEC, that the organization's rules and procedures required members to disclose any patents or patent applications that related to, or that might be involved in, the standard-setting work being undertaken by JEDEC.

30. Rambus knew, throughout its membership in JEDEC, that these patent disclosure rules and procedures were construed broadly so as to result in disclosure as early as possible in the JEDEC process.

31. Rambus knew that, throughout its membership in JEDEC, these patent disclosure rules and procedures were also construed consistently with the overriding duty of all members to participate in good faith, and thus not to take any action that was at odds with the fundamental purposes and principles of JEDEC, including the principle of developing "open" standards that avoid the use of proprietary patents wherever possible.

32. Rambus knew, throughout its membership in JEDEC, that JEDEC's patent disclosure rules included the duty to disclose both issued patents and patent applications.

33. Rambus knew, throughout its membership in JEDEC, that the failure to disclose pertinent patents and patent applications violated the integrity of JEDEC rules and procedures and subverted the standard-setting process at JEDEC.

34. Rambus knew, throughout its membership in JEDEC, that JEDEC's patent disclosure rules were mandatory (not voluntary) and that they applied to all members (not only those who made presentations).

35. Rambus knew, throughout its membership in JEDEC, that JEDEC's patent disclosure rules required disclosure of patents and applications whenever the holder of the patent, or patent applicant, believed that the patent (or application, if and when issued as a patent) might be infringed by products built in compliance with JEDEC's standards.

36. Rambus knew, throughout its membership in JEDEC, that JEDEC's patent disclosure rules required disclosure of patent applications whenever the applicant believed that the underlying content of the application was such that, even without adding any new technical matter to the application, the application's claims could be amended such that (if and when a patent issued containing such amended claims) they might be infringed by products built in compliance with JEDEC's standards.

37. Rambus knew, throughout its membership in JEDEC, that a JEDEC member's duty to

disclose patents or patent applications could not be avoided simply by withdrawing from the organization in lieu of disclosure.

38. Rambus knew, throughout its membership in JEDEC, that by voluntarily choosing to participate as a member of JEDEC, it was impliedly committing itself to be legally bound by JEDEC's rules and procedures and all other duties and expectations normally incumbent upon JEDEC members.

Rambus's Knowledge of the Activities at JEDEC

39. Between December 1991 and June 1996, Rambus knew that various members of the JC-42.3 Subcommittee made presentations proposing to incorporate the following technologies or features into JEDEC's DRAM standards:

- programmable latency via a control register;
- programmable access latency;
- a writable configuration register permitting programmable CAS latency;
- the use of control registers to contain values which control RAS and CAS access timing;
- the use of control registers to contain values;
- auto precharge;
- auto precharge options available during the column portion of any cycle;
- a proposal permitting the user to specify that the bank currently being accessed precharge itself as soon as the burst is completed;
- internally precharging a bank without first receiving a separate precharge command;
- data output occurring on both edges of an external clock;
- output of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal;
- input of a first portion of data in response to a rising edge of a data strobe and a second portion of data in response to a falling edge of a data strobe;

- output of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal;
- input of a first portion of data synchronously with respect to a first external data strobe and a second portion of data synchronously with respect to a second external data strobe;
- output a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal;
- use of a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock;
- sampling of data occurring on both edges of an external clock;
- data output occurring on the rising edge of an external clock and the falling edge of the external clock;
- clocking data on both edges of the clock;
- use of both edges of the clock for transmission of address, commands, or data;
- a receiver circuit for latching information in response to a rising edge of the clock signal to the falling edge of the clock signal;
- on-chip PLL or on-chip DLL circuitry;
- phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal;
- having phase lock loop on DRAM to control delays inside and outside DRAM;
- using a PLL/DLL circuit on a DRAM to reduce input buffer skews;
- DRAM with PLL clock generation;
- using PLL on an SDRAM; and

- using a DLL to compensate for the output delay.

40. Even after withdrawing from JEDEC, Rambus closely monitored JEDEC's ongoing work on SDRAM standards, including work involving specific technologies on which Rambus sought to perfect patent rights.

Rambus's Knowledge as to How its Patents or Patent Applications Related to JEDEC Work

41. From late 1991 to mid 1996, while participating in JEDEC's development of RAM standards, Rambus reasonably believed that the JEDEC RAM standards being developed at that time would require the use of patents held or applied for by Rambus.

42. From late 1991 to mid 1996, Rambus reasonably believed that the following technologies or ideas, proposed for inclusion in the JEDEC RAM standards during the period of Rambus's participation in JEDEC, were covered by Rambus's then-pending patent applications or could be covered through amendments to such applications:

- programmable burst length;
- programmable CAS latency;
- on-chip PLL or on-chip DLL circuitry;
- dual-edge clock;
- use of a programmable register operative to store information specifying a manner in which the semiconductor device is to respond to a read request or a write request;
- use of a register to store a value to determine CAS latency, where that value can be changed by programming the mode register;
- use of a programmable register to store a value that is representative of a delay time after which the device responds to a read request;
- use of a programmable register to store a value which is representative of a delay time, that value being a number of clock cycles of an external clock, after which the SDRAM responds to a read request;
- use of a programmable access-time register operative to store information

specifying a value indicative of an access time for the device, such that the device waits for the access time before responding to a read request;

- use of a register to store a value to determine burst length, where that value can be changed by programming the mode register;
- use of a register to store a value to determine block size, where that value can be changed by programming the mode register;
- use of a programmable register that receives information that defines an amount of data to be output by the memory device in response to a read request;
- programmable block size;
- use of a register to store a value that defines an amount of data to be output by the memory device in response to a read request, where that value can be changed by programming the mode register;
- use of a programmable register that receives information that defines an amount of data to be input by the memory device in response to a write request;
- use of a programmable register to store a value that defines an amount of data to be input by the memory device in response to a write request;
- outputting data on the rising and the falling edge of a clock signal;
- outputting a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal;
- inputting of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal;
- output of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal;
- data output occurring synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal;
- data input occurring synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal;

- output of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal;
- data output occurring synchronously with respect to both a first external clock signal and a second external clock signal;
- input of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal;
- data input occurring synchronously with respect to both a first and a second external clock signal;
- data input and output occurring synchronously with the rising and falling edge of an external clock, according to a dual edge clocking scheme;
- inputting a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal;
- outputting a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal;
- inputting a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal;
- data input occurs synchronously with respect to both the rising edge of the external clock and the falling edge of the external clock signal;
- outputting a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal;
- inputting a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal;
- use of phase locked loop circuitry or delay locked loop circuitry to generate an

internal clock signal using an external clock signal;

- having a phase lock loop on DRAM to control delays;
- using a PLL/DLL circuit on a DRAM to reduce input buffer skews;
- using a PLL clock generation;
- using a PLL on an SDRAM;
- using a DLL to compensate for the output delay in a DRAM; and
- using an on-chip PLL or DLL to ensure that the data strobe and data coming off of a DRAM chip are sufficiently synchronized to the system clock so that the memory controller can capture that data.

Rambus's Efforts to Broaden and Expand Its Patent Claims to Cover Technologies Incorporated into JEDEC Standards

43. During its participation at JEDEC, Rambus reasonably believed it could perfect its patent rights by amending pending claims of its '898 patent application and later-filed progeny to cover technologies proposed to be incorporated into JEDEC's DRAM-related standards.

44. Between December 1991 and June 1996, Rambus attempted to amend its patent claims to cover JEDEC work relating to the following technologies, so that if included in a JEDEC standard, use of such technologies in JEDEC-compliant devices would infringe Rambus patents:

- programmable CAS latency;
- programable burst length;
- dual edge clock;
- on-chip DLL or on-chip PLL circuitry;
- using a programmable register operative to store information specifying a manner in which the semiconductor device is to respond to a read request or a write request;
- use of a register to store a value to determine CAS latency, where that value can be changed by programming the mode register;

- use of a programmable register to store a value that is representative of a delay time after which the device responds to a read request;
- use of a register to store a value to determine CAS latency;
- use of a programmable register to store a value which is representative of a delay time, that value being a number of clock cycles of an external clock, after which the SDRAM responds to a read request;
- use of a programmable access-time register operative to store information specifying a value indicative of an access time for the device, such that the device waits for the access time before responding to a read request;
- use of a register to store a value to determine burst length, where that value can be changed by programming the mode register;
- use of a register to store a value to determine block size, where that value can be changed by programming the mode register;
- use of a programmable register that receives information that defines an amount of data to be output by the memory device in response to a read request;
- programmable block size;
- use of a register to store a value that defines an amount of data to be output by the memory device in response to a read request, where that value can be changed by programming the mode register;
- use of a programmable register that receives information that defines an amount of data to be input by the memory device in response to a write request;
- use of a programmable register to store a value that defines an amount of data to be input by the memory device in response to a write request;
- outputting a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal;
- inputting of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal;

- output of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal;
- data output occurring synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal;
- data input occurring synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal;
- output of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal;
- data output occurring synchronously with respect to both a first external clock signal and a second external clock signal;
- input of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal;
- data input occurring synchronously with respect to both a first and a second external clock signal;
- use of a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock;
- data input and output occurring synchronously with the rising and falling edge of an external clock, according to a dual edge clocking scheme;
- outputting a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal;
- inputting a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal;
- outputting a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal;
- data output occurring synchronously with respect to both the rising edge of the

external clock signal and the falling edge of the external clock signal;

- inputting a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal;
- data input occurring synchronously with respect to both the rising edge of the external clock and the falling edge of the external clock signal;
- outputting a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal;
- data output occurring synchronously with respect to both a first external clock signal and a second external clock signal;
- inputting a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal;
- using a dual edge clocking scheme which inputs and outputs synchronously with the rising and falling of an external clock;
- use of phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal;
- having a phase lock loop on DRAM to control delays;
- using a PLL/DLL circuit on a DRAM to reduce input buffer skews;
- using a PLL clock generation;
- using a PLL on an SDRAM;
- using a DLL to compensate for the output delay in a DRAM; and
- using an on-chip PLL or DLL to ensure that the data strobe and data coming off of a DRAM chip are sufficiently synchronized to the system clock so that the memory controller can capture that data.

Rambus's Intent to Enforce JEDEC-Related Patents

45. While a member of JEDEC, Rambus intended to enforce its JEDEC-related patents (and, once issued as patents, its JEDEC-related patent applications) against memory manufacturers who produced products compliant with the JEDEC RAM standards.

46. In enforcing such JEDEC-related patents, Rambus also intended to charge high royalties.

Rambus's Intent to Mislead JEDEC and JEDEC's Members about the Existence or Scope of Its Intellectual Property Claims

47. Rambus knew that its very participation in JEDEC, coupled with its failure to make required patent-related disclosures, conveyed a materially false and misleading impression that JEDEC was not at risk of adopting standards that Rambus could later claim to infringe upon its patents.

48. Rambus also knew that by engaging in various affirmatively misleading conduct, it was reinforcing the materially false and misleading impression that JEDEC was not at risk of adopting standards that Rambus could later claim to infringe upon its patents.

49. Rambus intended through its conduct – both its actions and omissions – to convey the materially false and misleading impression that JEDEC was not at risk of adopting standards that Rambus could later claim to infringe upon its patents.

50. Rambus's pattern of misleading conduct – both its actions and omissions – continued for a number of years after it withdrew from JEDEC.

51. During the time it was a JEDEC members and for a number of years thereafter, Rambus sought to conceal from JEDEC and its members both (1) the fact that it possessed patents and pending patents that would (or might) be infringed by devices built in accordance with JEDEC standards, and (2) the fact that Rambus in the future intended (or at a minimum, reserved the right) to enforce such patents and to demand high royalties.

Rambus's Knowledge That Its Limited and Misleading Disclosures Did Not Put JEDEC or its Members on Notice of the True Nature and Scope of its Patent Claims

52. Rambus knew that, before and during its membership in JEDEC, it never disclosed either to JEDEC or to individual JEDEC members information sufficient to place them (individually or collectively) on notice of the fact that Rambus possessed (or reasonably believed it possessed) patents and pending patents that would (or might) be infringed by devices built in accordance with JEDEC standards.

53. Rambus knew that, after withdrawing from JEDEC – up until the time it began to enforce its JEDEC-related patents – it never disclosed either to JEDEC or to individual JEDEC members information sufficient to place them (individually or collectively) on notice of the fact that Rambus possessed (or reasonably believed it possessed) patents and pending patents that would (or might) be infringed by devices built in accordance with JEDEC standards.

54. Rambus knew that, in the course of making disclosures to DRAM makers and others in the context of licensing-related discussions involving Rambus's RDRAM architecture, it never disclosed either to JEDEC or to individual JEDEC members information sufficient to place them (individually or collectively) on notice of the fact that Rambus possessed (or reasonably believed it possessed) patents and pending patents that would (or might) be infringed by devices built in accordance with JEDEC standards.

55. Rambus knew that, through availability of Rambus's foreign patents and patent applications, neither JEDEC nor individual JEDEC members could gather sufficient information to place them (individually or collectively) on notice of the fact that Rambus possessed (or reasonably believed it possessed) patents and pending patents that would (or might) be infringed by devices built in accordance with JEDEC standards.

56. Rambus knew that, through its disclosure of the '703 patent to JEDEC, it did not provide JEDEC or individual JEDEC members with sufficient information to place them (individually or collectively) on notice of the fact that Rambus possessed (or reasonably believed it possessed) patents and pending patents that would (or might) be infringed by devices built in accordance with JEDEC standards.

57. Rambus knew that, through its participation in JEDEC, it did nothing that would have served to place JEDEC or its members (individually or collectively) on notice of the fact that Rambus possessed (or reasonably believed it possessed) patents and pending patents that would (or might) be infringed by devices built in accordance with JEDEC standards.

58. Rambus knew that the limited disclosures it made to IEEE or the SynkLink Consortium, relating to Rambus patents, would not have served to place JEDEC or its members (individually or collectively) on notice of the fact that Rambus possessed (or reasonably believed it possessed) patents and pending patents that would (or might) be infringed by devices built in accordance with JEDEC standards.

59. Rambus knew that the limited disclosures it made to JEDEC in a letter concerning the SynkLink technology would not have served to place JEDEC or its members (individually or collectively) on notice of the fact that Rambus possessed (or reasonably believed it possessed) patents and pending patents that would (or might) be infringed by devices built in accordance with JEDEC standards.

60. Rambus knew that nothing contained in its June 1996 JEDEC withdrawal letter would have served to place JEDEC or its members (individually or collectively) on notice of the fact that Rambus possessed (or reasonably believed it possessed) patents and pending patents that would (or might) be infringed by devices built in accordance with JEDEC standards.

Rambus's Knowledge That JEDEC Would Seek to – and Would Be Able to – Work Around Rambus's Patented Technology, Had Rambus Made Proper Patent-Related Disclosures

61. Rambus knew that, if it had made proper patent-related disclosures to JEDEC (including but not limited to disclosures relating to CAS latency, programable burst length, on-chip PLL/DLL, and dual-edge clock), JEDEC and its members would seek to work around Rambus's patented or patent-pending technologies.

62. Rambus knew that, if it had made proper patent-related disclosures to JEDEC (including but not limited to disclosures relating to CAS latency, programable burst length, on-chip PLL/DLL, and dual-edge clock), JEDEC and its members would have been able to revise JEDEC's DRAM-related standards to work around or avoid Rambus's patented or patent-pending technologies.

63. Rambus knew that, if it had made proper patent-related disclosures to JEDEC (including but not limited to disclosures relating to CAS latency, programable burst length, on-chip PLL/DLL, and dual-edge clock), the most likely result is that JEDEC's DRAM-related standards would have excluded or omitted any technologies covered by Rambus's patented or patent-pending technologies.

64. Rambus knew that, if it had made proper patent-related disclosures to JEDEC (including but not limited to disclosures relating to CAS latency, programable burst length, on-chip PLL/DLL, and dual-edge clock), Rambus's patents in the future would derive no value by virtue of any association with the contents of JEDEC's DRAM standards.

Rambus's Knowledge That Commercially Viable Alternatives to Its Technology Existed

65. During its participation at JEDEC, Rambus knew that there were a variety of commercially viable alternatives to the use of its proprietary technologies in JEDEC's DRAM-related standards.

66. Rambus knew that the design objectives served by inclusion of programmable CAS latency, programmable burst length, on-chip PLL/DLL, and dual-edge clock technologies in JEDEC standards likely could have been accomplished through use of alternative DRAM-related technologies available at the time these standards were being developed.

67. During its participation at JEDEC, Rambus knew that JEDEC and its members would be capable of developing commercially viable alternative standards that avoided Rambus's patents and patent applications.

68. Rambus knew that the following technologies, among others, were commercially viable alternatives to various Rambus patented or patent-pending technologies:

- permanently fixing the CAS latency at a single value;
- having the memory controller signal the CAS latency through separate pins on each DRAM device;
- setting the CAS latency through the command structure of the read command;
- using fixed latency parts;
- explicitly identifying the CAS latency in the read or write command;
- programming CAS latency by blowing fuses on the DRAM;
- scaling CAS latency with clock frequency;
- using an existing pin or a new, dedicated pin to identify the latency via two or more different voltage levels asserted by the memory controller;
- using asynchronous DRAM;
- fixing the burst length at a single value;
- having the memory controller signal the burst length through separate pins on each DRAM device;
- setting the burst length through the command structure of the read command;
- setting the burst length through the use of a burst interrupt feature;
- using a short fixed burst length;
- explicitly identifying the burst length in the read or write command;
- using a long fixed burst length coupled with the burst-terminate command;

- using a burst-EDO style protocol where each CAS pulse toggles out a single column of data;
- using an existing pin or a new, dedicated pin to identify the burst length via multiple voltage levels;
- moving the PLL/DLL circuitry to the memory controller;
- moving the PLL/DLL circuitry to each DIMM;
- using a periodic calibration technique;
- using a vernier method to measure and account for dynamic changes in skew;
- putting the DLL on the memory controller;
- use of off-chip (on-module) DLLs;
- increasing the speed at which DRAM's could operate;
- interleaving data between different DIMM's onto the same data bus;
- interleaving data between different banks on each DRAM onto the same data bus;
- increasing the width of the data bus;
- use of two or more interleaving memory banks on-chip and assigning a different clock signal to each bank;
- keeping each DRAM single data rate and interleaving banks on the module;
- increasing the number of pins per DRAM;
- increasing the number of pins per module;
- doubling the clock frequency;
- use of simultaneous bidirectional I/O drivers; and

- use of toggle mode.

Rambus's Strategic Reasons for Delaying Any Disclosure of Pertinent Patents or Patent Applications

69. Rambus consciously chose not to disclose to JEDEC or to JEDEC's members the fact that Rambus possessed (or reasonably believed it possessed) patents and pending patents that would (or might) be infringed by devices built in accordance with JEDEC standards, for a variety of strategic reasons, including

- a desire to avoid JEDEC developing alternative standards that worked around Rambus's technology;
- a desire to place Rambus in a position to charge high royalties in the future based on use of Rambus technologies in JEDEC-compliant devices;
- a desire to avoid any limitation on its freedom to license its patents to whomever it wished on whatever terms it wished; and
- a desire to use its patent leverage over the JEDEC standards to limit competition between RDRAM and JEDEC-compliant DRAM.

Rambus's Knowledge That JEDEC Members Were Unlikely to Accept Rambus's Desired Royalty Rates

70. Rambus knew that, were it to disclose patents or patent applications to JEDEC, its claimed intellectual property would be used by JEDEC only subject to advance commitments by Rambus that it would license such intellectual property either on royalty-free or other terms unfavorable to Rambus.

71. Rambus knew that the DRAM industry, including JEDEC member companies, would not consider the royalty rates it intended to and later did charge for SDRAM and DDR SDRAM licenses (.75% and 3.5%, respectively) to be fair and reasonable.

Rambus's Knowledge That It Faced Equitable Estoppel and Antitrust Risks by Participating in JEDEC

72. Throughout most of the time it participated in JEDEC, Rambus knew that the misleading nature of its participation created significant legal risks to the enforceability of Rambus's JEDEC-related patents.

73. Throughout most of the time it participated in JEDEC, Rambus knew that the misleading nature of its participation created significant risks that Rambus's JEDEC-related patents could be held unenforceable on grounds of equitable estoppel.

74. Throughout most of the time it participated in JEDEC, Rambus knew that the misleading nature of its participation created significant risks that Rambus's JEDEC-related patents also could be held unenforceable on antitrust grounds.

75. At least as of December 1995, when Rambus learned of the FTC's proposed consent order in *In re Dell Computer Corporation*, Rambus knew that its conduct at JEDEC violated antitrust laws.

76. Throughout most of the time it participated in JEDEC, Rambus's attorneys encouraged the company to withdraw from JEDEC, because of the legal risks associated with participation.

77. Until early 1996, Rambus consciously chose to ignore legal advice to withdraw from JEDEC.

Rambus's Knowledge That Its Actions Violated and Subverted the Purposes, Rules, and/or Procedures of JEDEC

78. Rambus knew that joining JEDEC as part of its business strategy of obtaining high royalties for use of its technology in widely adopted DRAM industry standards violated and subverted the purposes, rules, and/or procedures of JEDEC.

79. Rambus knew that its efforts to amend existing patent applications to cover technology features that were being discussed within JEDEC for potential use within JEDEC RAM standards violated and subverted the purposes, rules, and/or procedures of JEDEC.

80. Rambus knew that its intentions, while a member of JEDEC, to enforce **its JEDEC-related patents in the future against memory manufacturers who produced products compliant with JEDEC RAM standards violated and subverted the purposes, rules, and/or procedures of JEDEC**.

81. Rambus knew that its plans to license its intellectual property on terms it knew the industry would not consider to be fair and reasonable violated and subverted the purposes, rules, and/or procedures of JEDEC.

82. **Rambus knew that, by conveying a materially false and misleading impression that JEDEC was not at risk of adopting standards that Rambus could later claim to infringe upon its patents,** it was violating and subverting the purposes, rules, and/or procedures of JEDEC.

83. Rambus knew that its failure to make sufficient disclosures to JEDEC that would have alerted JEDEC and its members to the true nature and scope of its patent claims violated and subverted the purposes, rules, and/or procedures of JEDEC.

84. Rambus knew that its purpose to substantially enhance the value of its patents by not making proper patent-related disclosures violated and subverted the purposes, rules, and/or procedures of JEDEC.

85. Rambus knew that, by remaining in JEDEC for over four years in order to glean information that would enable it to write new and amended patent claims designed to cover technologies that it knew to be, or expected would be, encompassed by JEDEC's RAM standards, it was violating and subverting the purposes, rules, and/or procedures of JEDEC.

86. Rambus knew that, by withdrawing from JEDEC without revealing its relevant patents and patent applications, it was violating and subverting the purposes, rules, and/or procedures of JEDEC.

Rambus's Reasons for Withdrawing from JEDEC

87. Rambus ultimately withdrew from JEDEC in part because it feared its conduct at JEDEC could render its patents unenforceable on and antitrust and/or equitable estoppel grounds.

88. Rambus ultimately withdrew from JEDEC in part because it feared its conduct at JEDEC could lead to an FTC antitrust enforcement action.

89. Rambus ultimately withdrew from JEDEC in part because it feared that continued participation could result in limitations being imposed on Rambus's freedom to licenses its patents to whomever it wished on whatever terms it wished.

Rambus's Knowledge of Significant Lock-in Effects Relating to JEDEC

90. Rambus knew that once the DRAM industry (and related industries) had adopted the JEDEC DRAM standards, the industry would become locked into those standards, rendering it economically infeasible for the industry to attempt to alter or work around the standards in order to avoid paying royalties to Rambus.

91. Rambus knew that manufacturers who might attempt to work around the JEDEC RAM standards could be forced to absorb potentially massive revenue losses if, as a result of modifying the JEDEC standards, their introduction of new products were delayed.

92. Rambus knew that purchasers and other users of JEDEC-compliant DRAM technology – including manufacturers of computers, chipsets, graphics cards, and motherboards – would themselves become locked into the JEDEC standards.

93. Rambus knew that any effort to work around the JEDEC standard would face innumerable practical and economic impediments, including but not limited to the out-of-pocket costs associated with redesigning, validating, and qualifying DRAM products to conform with a revised set of standards.

94. Rambus knew that it was unclear whether downstream purchasers and other users of SDRAM technology would tolerate the delay in the introduction of new products that likely would result from the process of changing the standard.

95. Rambus knew that, by late 1999 or early 2000, when it first began to enforce its patents against memory manufacturers producing JEDEC-compliant DRAM, the DRAM manufacturers and their customers had become "locked in" to the JEDEC standards.

96. Rambus knew that due to the lock-in effect, it could succeed in extracting exorbitant royalty rates from DRAM makers.

97. Rambus knew that, once industry lock-in occurred, it had the power to exclude DRAM makers from the commodity memory marketplace by refusing to grant them a license.

Rambus's Document Destruction

98. Rambus knew that, by destroying massive amounts of internal business records, it could substantially increase the chances of its success in future JEDEC-related patent litigation.

99. Rambus knew that, by destroying massive amounts of internal business records, it could substantially increase the chances of its success in future JEDEC-related antitrust litigation.

100. Rambus knew that, by destroying massive amounts of internal business records, it could substantially increase the chances of its success in any future JEDEC-related FTC enforcement action.