# Program at a Glance

| | Morning | AM Session | PM Session | Evening |
|---|---|---|---|---|
| **Monday** May 23rd | | | Check-in at hotel<br>**15:00 – 17:00** MINATEC Facility Tour (advanced registration required) | **17:00 – 20:00** Reception and registration at MINATEC Facility |
| **Tuesday** May 24th | **07:30** Registration Attendee Check-in<br>**08:00** Breakfast | **08:45** Conference Opening<br>**09:00 Session 1** Keynote Talks<br>**10:30** Coffee Break and Poster Viewing<br>**11:00 Session 2** Technology Overview for Nanoelectronics and Metrology | **12:00 Session 3** Metrology for Beyond CMOS<br>**12:30** Lunch<br>**14:00 Session 3** (continued)<br>**15:00 Session 4** Theory, Modeling and Simulation<br>**15:30** Coffee Break and Poster Viewing<br>**16:00 Session 4** (continued)<br>**16:30 Session 5 part 1** Microscopy for Nanoelectronics<br>**17:00** Poster Session | |
| **Wednesday** May 25th | **08:00** Registration Attendee Check-in and Breakfast | **08:30 Session 5 part 2** Microscopy for Nanoelectronics<br>**10:00** Coffee Break and PosterViewing<br>**10:30 Session 5** (continued)<br>**11:00 Session 6** Novel Characterization Methods | **12:30** Lunch<br>**14:00 Session 6** (continued)<br>**15:00 Session 7** CMOS Metrology<br>**15:30** Coffee Break and Dedicated Poster Viewing Session<br>**17:00 Session 7** CMOS Metrology (continued) | **18:45** Depart MINATEC for Banquet |
| **Thursday** May 26th | **08:00** Registration Attendee Check-in and Breakfast | **08:30 Session 8** Interconnect Metrology<br>**10:00** Coffee Break and Poster Viewing<br>**10:30 Session 9** Metrology for Patterning | **12:30** Lunch<br>**14:00 Session 10** Next-Generation Defect Inspection<br>**15:00 Session 11** Characterization Needs and Methods for "More than Moore"<br>**15:30** Coffee Break and Poster Viewing<br>**16:00 Session 11** (continued)<br>**17:30** Poster Session | |

design: www.lafabriquestudio.fr - photos: P. Joyet - P. Conche - impression: Les deux ponts

IC-FCMN 2011 / MINATEC Campus - Grenoble / May 23-26

# 2011 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics

## >May 23-26

MINATEC Campus Grenoble

> http://www.nist.gov/pml/semiconductor/conference

Cover caption : Lower part - Electron Tomography of organometallic (Gd) clusters embedded in 50nm porous silica balls. © P. Cherns and W. L. Ling. Upper part - Source for analysis by Medium Energy Ion Scattering. © P. Morel

## Committee Co-Chairs

**David Seiler**
National Institute of Standards and Technology (NIST)

**Alain Diebold**
College of Nanoscale Science and Engineering, SUNY Albany

**Bob McDonald**
formerly of Intel (Treasurer)

**Dan Herr**
Semiconductor Research Corporation (SRC)

**George Thompson**
Intel

**Amal Chabli**
CEA-Leti

## Committee Members

- **Alexander Braun**, formerly of Semiconductor Intl
- **Michael Current**, Current Scientific
- **Dick Hockett**, Evans Analytical Group Ltd
- **Toshihiko Kanayama**, National Institute of Advanced Industrial Science and Technology (AIST)
- **Rajinder Khosla**, National Science Foundation (NSF)
- **David Kyser**, Applied Materials
- **Shifeng Lu**, Micron
- **Ulrich Mantz**, Zeiss
- **Lori S. Nye**, Brewer Science, Inc.
- **Yaw Obeng**, NIST
- **Sandip Tiwari**, Cornell University
- **Victor Vartanian**, International SEMATECH Manufacturing Initiative (ISMI)
- **Wilfried Vandervorst**, Imec
- **Ehrenfried Zschech**, Fraunhofer Institute for Non-Destructive Testing

**Banquet, may 25th,**
**How to reach La Bastille...**


Get off the tram at the « **Victor Hugo** » station
Go straight on 'Felix Poulat' street and take a look around Grenoble downtown!
Take a left on 'Bressieux' street, and go through the « **Jardin de ville** » (City garden),towards the cable car departure.
Give your gala pass and receive your roundtrip ticket.
**Keep your return ticket!**

Get on the tram at the « **Cité Internationale** » station (in front of the venue)

**Enjoy the ride, and the view !**

# 2011 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics

Welcome to the 2011 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics (FCMN)! Our goal is to bring together scientists and engineers interested in all aspects of the characterization and measurement technology needed for nanoelectronic materials and device research, development, and manufacturing. All approaches are covered in this conference: chemical, physical, electrical, optical, and in-situ. The conference summarizes major issues and provides critical reviews of important semiconductor techniques needed as the semiconductor industry continues its move in silicon nanoelectronics and beyond. New to the conference is a session dedicated to the emerging area of More than Moore. It is hoped that the invited talks, contributed poster papers, and informal discussions will be a stimulus to provide practical perspectives, breakthrough ideas for research and development, and a chance to explore collaborations and interactions on a world-wide basis.

We are pleased to have Michel Brillouet, Deputy Director, CEA-Leti; and Rudi Cartuyvels, VP Process Technology and General Manager, IMEC, as keynote speakers for the event. Over 30 other invited talks will offer overviews in the session that follow. Poster papers will supplement these overviews with the latest metrology-based research results. These poster papers represent significant contributions to the latest developments in characterization and metrology technology, especially at the nanoscale.

The 2011 FCMN is the eighth in a series that began in 1995. It emphasizes the frontiers and innovation in characterization and metrology of nanoelectronics. The proceedings for all seven previous conferences were published as hardcover volumes by the American Institute of Physics, New York.

For the first conference in this series to be held outside of the United States, the organizers have chosen to hold the conference at the MINATEC Campus in Grenoble, France. The campus is home to 2,400 researchers, 1,200 students, and 600 technology transfer experts on a state-of-the-art 20-hectare campus offering 10,000 square meters of clean room space. An international center for micro and nanotechnologies, the MINATEC campus is unlike any other research facility in Europe.

It is our sincere hope that you find this conference stimulating and enjoyable!

With best wishes from the Committee Co-Chairs,

**David Seiler**, NIST; **Alain Diebold,** College of Nanoscale Science and Engineering, SUNY Albany; **Bob McDonald**, formerly of Intel (Treasurer); **Dan Herr**, SRC; **George Thompson**, Intel; and **Amal Chabli**, CEA-Leti

## Purpose and Goals

We bring together scientists and engineers interested in all aspects of the characterization and measurement technology needed for nanoelectronic materials and device research, development, and manufacturing. All approaches are covered in this conference: chemical, physical, electrical, optical, and in-situ. The conference summarizes major issues and provides critical reviews of important semiconductor techniques needed as the semiconductor industry continues its move in silicon nanoelectronics and beyond.

## Contributed Poster Papers

One of the major emphases of this conference is on the contributed poster papers. The poster papers selected by the committee represent significant contributions to frontier, state-of-the-art materials and device characterization and metrology

Authors must be present at the conference for their papers to be accepted for publication in the conference proceedings. Specifically, authors are responsible for setting up their displays, being present for posters sessions, and removing their displays at the end of the day.

## Proceedings

After being formally reviewed, accepted manuscripts will be published in a hardback book by the American Institute of Physics. If your manuscript has not already been submitted, it must be submitted in the prescribed camera-ready format by e-mail (erik.secula@nist.gov) by Jun. 10, 2011, in order to be included in the proceedings. The book and CD-ROM are expected to be available in the fall of 2011.

## Banquet

A dinner banquet will be held on Wednesday, May 25th, at "restaurant du téléphérique" at the Bastille. A tramway in front of MINATEC will depart at 6:45 PM, followed by a 10 min walk through the "Jardin de Ville" and then a cable car to the restaurant.

## Poster Sessions

Poster sessions with complimentary wine and hors d'oeuvres are scheduled for the end of Tuesday and Thursday at the MINATEC Facility. Wednesday's session will be part of an extended afternoon coffee break.

# Gold Sponsors


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## About CEA-Leti

CEA is a French research and technology organisation, with activities in four main areas: energy, information technologies, healthcare technologies and defence and security. Within CEA, the Laboratory for Electronics & Information Technology (CEA-Leti) works with companies in order to increase their competitiveness through technological innovation and transfers. CEA-Leti is focused on micro and nanotechnologies and their applications, from wireless devices and systems, to biology and healthcare or photonics. Nanoelectronics and microsystems (MEMS) are at the core of its activities. As a major player in MINATEC campus, CEA-Leti operates 8,000-m$^2$ state-of-the-art clean rooms, on 24/7 mode, on 200mm and 300mm wafer standards. With 1,200 employees, CEA-Leti trains more than 190 Ph.D. students and hosts 200 assignees from partner companies. Strongly committed to the creation of value for the industry, CEA-Leti puts a strong emphasis on intellectual property and owns more than 1,700 patent families. For more information, visit : **www.leti.fr**

**Press Contacts**

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### About the National Institute of Standards and Technology (NIST)

Founded in 1901, NIST is a non-regulatory federal agency within the U.S. Department of Commerce. NIST's mission is to promote U.S. innovation and industrial competitiveness by advancing measurement science, standards, and technology in ways that enhance economic security and improve our quality of life.
NIST carries out its mission in four cooperative programs: the NIST Laboratories, the Baldrige Performance Excellence Program, the Hollings Manufacturing Extension Partnership, and the Technology Innovation Program. There are also two user facilities: the NIST Center for Neutron Research and the Center for Nanoscale Science and Technology.
NIST's Semiconductor Electronics Division is a key leader for this metrology conference. The Division provides technical leadership to industry, government, and academia in research and development of the semiconductor measurement needs essential to the silicon microelectronics industry, advanced semiconductor materials technologies, and advanced electronic devices based upon molecular or quantum structures. The Division's programs also respond to industry measurement needs related to MicroElectroMechanical Systems, power electronics, and various sub-areas of nanotechnology including nanoelectronics, nanocharacterization, nanobiotechnology, and plastic electronics.

**Contacts:**

Gail Porter (gail.porter@nist.gov), Director, Public and Business Affairs Office

David Seiler (david.seiler@nist.gov) Chief, Semiconductor Electronics Division

## Local authorities

## Silver Sponsors

## Sponsors

# Program at a Glance

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# Conference Program

## Monday, May 23

Tour of CEA-Leti facilities

**3:00 PM – 5:00 PM**

Advanced registration is required.  See conference website for details.

**5:00 PM – 8:00 PM**

Reception and Registration  MINATEC Campus

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# Tuesday, May 24



Registration

**7:30 AM – 8:45 AM**
Conference Opening

**8:45 AM**
Conference Opening
*David Seiler, NIST, Conference Chair*

Keynote Talks
Session Chair: *David Seiler, NIST*

**9:00 AM**
Nanocharacterization Challenges in a Changing Microelectronics Landscape
*Michel Brillouet, CEA-Leti* ----------P.16

**9:45 AM**
Nanoelectronics and More-than-Moore at IMEC
*Rudi Cartuyvels, IMEC* ----------P.17

**10:30 AM**
*Coffee Break and Poster Viewing*

Technology Overview for Nanoelectronics and Metrology
Session Chair: *Michel Brillouet, CEA-Leti*

**11:00 AM**
More than Moore or More Moore: a SWOT Analysis
*Dan Hutcheson, VLSI Research* ----------P.18

**11:30 PM**
ITRS Review in Relation to Future Metrology Needs
*Alain Diebold, College of Nanoscale Science and Engineering, SUNY Albany* --------P.19

Metrology for Beyond CMOS
Session Chair: *George Thompson, Intel*

**12:00 PM**
Metrology and Characterization Challenges for Emerging Research Materials and Devices
*Mike Garner, formerly of Intel, Dan Herr, SRC, and Yaw Obeng, NIST* ----------P.20

**12:30 PM**
Lunch and Poster Viewing

**2:00 PM**
Carbon Based Nanoelectronics, including CNT and Graphene Based Devices
*C.Y. Sung, Phaedon Avouris, IBM* ----------P.21

**2:30 PM**
Quantum Control and Engineering of Single Spins
*David Awschalom, UCSB* ----------P.22

Theory, Modeling, and Simulation
Session Chair: *Robert McDonald, formerly of Intel*

**3:00 PM**
Discrete Tomography in Materials Science
*K. Joost Batenburg, Centrum Wiskunde & Informatica* ----------P.23

**3:30 PM**
Coffee Break and Poster Viewing

**4:00 PM**
Materials Modeling and Metrology
*Sadas Shankar, Intel* ----------P.24

Microscopy for Nanoelectronics (part one)
Session Chair: *Amal Chabli, CEA-Leti*

**4:30 PM**
TSOM Method for Nanoelectronics Dimensional Metrology
*Ravikiran Attota, NIST* ----------P.25

**5:00 PM – 6:00 PM**
*Poster Session (with Wine and Cheese)*

**TU-01**, Origin Of Resistivity Change in NiO Thin Films Studied by Hard X-Ray Photoelectron Spectroscopy

P. Calka[1], E. Martinez[1], D. Lafond[1], S. Minoret[1], C. Guedj[1], S. Tirano[2], B. Detlefts[3], J. Roy[3], and J. Zegenhagen[3]
**[1]CEA-Leti, MINATEC Campus, Grenoble Cedex 9, France**
**[2]IM2NP, Université de Provence, Marseille, Cedex 20, France**
**[3]European Synchrotron Radiation Facility, Grenoble, France** *P.26*

**TU-02**, Nanoscale Chemical Characterization by Auger Electron Spectroscopy

E. Martinez[1], L. Borowik[1], L. You[1], N. Chevalier[1], C. Guedj[1], G. Auvert[2], A. Roussey[1], V. Jousseaume[1], R. Boujamaa[2], M. Gros-Jean[2], J. C. Barbé[1], G. Feuillet[1], F. Bertin[1], A. Chabli[1]
**[1]CEA-Leti, MINATEC Campus, Grenoble Cedex 9, France**
**[2]STMicroelectronics, Crolles, France** *P.27*

**TU-03**, Analytical Study of BAM (Al/GaAs) and Photovoltaic Samples Using State-of-The Art Auger Nanoprobes

P. Yadav[1,2], M. Bouttemy[1], E. Martinez[2], A. Etcheberry[1], O. Renault[2], P. Mur[2], A. Chabli[2], and N. Gambacorti[2]
**[1]Institut Lavoisier de Versailles, Versailles, Cedex, France**
**[2]CEA-Leti, MINATEC Campus, Grenoble Cedex 9, France** *P.28*

**TU-04,** Atom Probe Tomography and Nanoelectronics

D. Blavette, O. Mirédin-Cojocaru, T. Philippe, and S. Duguay
**Groupe de Physique des Matériaux (UMR CNRS 6634), UFR Sciences et Techniques, Rouvray, Cedex, France** *P.29*

**TU-05**, Characterization of Strain Induced by PECVD Silicon Nitride Films in Transistor Channel

R. Thomas[1], D. Benoit[1], L. Clement[1], P.Morin[1], D. Cooper[2], and F. Bertin[2]
**[1]STMicroelectronics, Crolles, France**
**[2]CEA-LETI, Minatec Campus, Grenoble, France** *P.30*

**TU-06**, AFM Analysis of High Temperature Dewetting under Ultra High Vacuum of Ultrathin Solid Silicon Films on Insulator

Ł. Borowik, N. Chevalier, D. Mariolle, F. Bertin, E. Martinez, A. Chabli, and J.C. Barbé
**CEA-Leti, MINATEC Campus, Grenoble, Cedex 9, France** *P.31*

**TU-07**, MOTIS: a Focused Ion Beam Source Based On Laser-Cooled Atoms

B. Knuffman[1], A.V. Steele[1], J. Orloff[2], M. Maazouz[2], and J.J. McClelland[1]
**[1]National Institute of Standards and Technology, Gaithersburg, MD**
**[2]FEI Company, Hillsboro, OR, USA** *P.32*

**TU-08**, Surface Imaging and Spectromicroscopy of Technological Materials: Complementarities Between Electron Spectroscopies, Scanning- and Ion Probes

O. Renault, E. Martinez, N. Chevalier, D. Mariolle, Ł. Borowik, J-C. Barbe, J. –P. Barnes, M. Veillerot, F. Bertin, and A. Chabli

**CEA-Leti, MINATEC Campus, Grenoble Cedex 9, France** *P.33*

**TU-09**, Effects of Roughness on Scatterometry Signatures

M. Foldyna[1], T.A. Germer[2], and B.C. Bergner[3]

**[1]Laboratory of Interfaces and Thin Films, CNRS, Ecole Polytechnique, Palaiseau, France**

**[2]Optical Technology Division, National Institute of Standards and Technology, Gaithersburg, MD**

**[3]Spectum Scientific, Inc., Irvine, CA** *P.34*

**TU-10**, Recent Advances in 2D-Band Structure Imaging by k-PEEM and Perspectives for Technological Materials

C. Mathieu[1], O. Renault[1], N. Barrett[2], and A. Chabli[1]

**[1] CEA-Leti, MINATEC Campus, Grenoble, Cedex 9, France**

**[2] CEA, DSM/IRAMIS/SPCSI, CEA Saclay, Cedex, France** *P.35*

**TU-11**, Characterization of Nanodevices by STEM Tomography

O. Richard, A. Vandooren, G. S. Kar, P. Van Marcke, and H. Bender

**IMEC, Leuven, Belgium** *P.36*

**TU-12**, Three Dimensional Investigation for the 22-nm-Node and Beyond: Surface Morphology of Gate-all-Around Transistors by Atom Probe and Electron Tomography

A. Grenier[1], D.Cooper[1], J.P. Barnes[1], K. Tachi[1], T.Ernst[1], S. Duguay[2], E. Cadel[2], F.Vurpillot[2], D. Blavette[2], A. Chabli[1], and F. Bertin[1]

**[1]CEA, CEA-Leti, MINATEC, Grenoble, France**

**[2]Groupe de Physique des Matériaux, Université de Rouen, Saint Etienne du Rouvray, Cedex, France** *P.37*

**TU-13**, Strain In Semiconductor Nanowires and Device Integration

J. Eymery[1], V. Favre-Nicolin[1,2], F. Mastropietro[1,3], F. Rieutord[1], L. Fröberg[4], T. Mårtensson[4], M. Borg[4], L. Samuelson[4], L.-E. Wernersson[4], S. Baudot[1,5], and F. Andrieu[5]

**[1]CEA, Grenoble, France**

**[2]Université Joseph Fourier, Grenoble, France**

**[3]ESRF, Grenoble, France**

**[4]Lund University, Physics Department, Sweeden**

**[5]CEA-Leti, Minatec Campus, France** *P.38*

**TU-14**, Physico-chemical and Electrical Characterization of Gate Stacks on GaAs and (In,Ga)As

M. El Kazzi, D.J. Webb, L. Czornomaz, C. Rossel, C. Gerl, M. Richter, M. Sousa, P. Maechler, J. Fompeyrine, and C. Marchiori

**IBM Research – Zurich, Switzerland** *P.39*

**TU-15**, Quantitative Strain Measurement Using Nanobeam Electron Diffraction and Dark Field Electron Holography

A. Béché[1], C. Bougerol[2], B. Daudin[2], J.L. Rouvière[2], and D. Cooper[3]
**[1]FEI Company, Eindhiven, The Netherlands**
**[2]CEA-Grenoble, INAC/SP2M, Grenoble, France**
**[3]CEA- Leti, MINATEC Campus, Grenoble, Cedex 9, France** *P.40*

**TU-16**, Investigation of Surface Potential on CdTe/CdS p-n Heterojunction with Kelvin Probe Force Microscopy

L.You[1,2], N.Chevalier[1], S.Bernardi[1], E. Martinez[1], D.Mariolle[1], G.Feuillet[1], M.Kogelschatz[2], G.Bremond[3], A.Chabli[1], and F.Bertin[1]
**[1]CEA- Leti, MINATEC Campus, Grenoble, Cedex 9, France**
**[2]LTM-CNRS, Grenoble Cedex 9, France**
**[3]Université de Lyon, Institut des Nanotechnologies de Lyon (INL), Villeurbanne, Cedex, France** *P.41*

**TU-17**, New Method of Electron Diffraction for Characterization of Nanomaterials Using the Scanning Electron Microscope

R.H. Geiss and R.R. Keller
**National Institute of Standards and Technology, Boulder, CO** *P.42*

**TU-18**, Status and Trends In 3D Nanodevices: Inspection by Electron Tomography

G. Haberfehlner, A. Grenier, D. Cooper, P.-H. Morel, T. Ernst, and P. Bleuet
**CEA-Leti, MINATEC Campus, Grenoble, Cedex 9, France** *P.43*

**TU-19**, Enhanced Spatial Resolution Electrical Scanning Probe Microscopy by Using Carbon Nanotube Terminated Tips

J.J. Kopanski[1], I. Sitnitsky[1], V. Vartanian[2], P. McClure[3], and V. Mancerski[3]
**[1]National Institute of Standards and Technology, Gaithersburg, MD**
**[2]International SEMATECH Manufacturing Initiative Albany, NY**
**[3]Xidex Corporation Austin, TX** *P.44*

**TU-20**, The Preparation with Argon Milling and Characterization with Cathodoluminescence of HB LED's

D. Erwin[1], M. Hassel Shearer[1], and D. Stowe[2]
**[1]Gatan Inc., Pleasanton, CA**
**[2]Gatan UK, Abingdon Oxon, UK** *P45*

**TU-21**, X-Ray Reflectometry Parameter Uncertainties for Thin $SiO_2$ Films

D. Windover[1], D.L. Gil[1], J.P. Cline[1], Y. Azuma[2], and T. Fujimoto[2]
**1National Institute of Standards and Technology, Gaithersburg, MD**
**[2]National Institute of Advanced Industrial Science and Technology, National Metrology Institute of Japan, Tsukuba, Japan** *P.46*

**TU-22**, C-MOS Gate Silicide Analysis by Atom Probe Tomography
F. Panciera[1,2], K. Hoummada[2], M. Gregoire[1], M. Juhel[1], N. Bicais[1], and D. Mangelinck[2]
[1]**STMicroelectronics, Crolles Cedex, France**
[2]**IM2NP, CNRS-Université Paul Cézanne, Marseille, Cedex 20, France** *P.47*

**TU-23**, Quantitative Characterization of Buried BxCy Nanolayers by Complementary Methodologies – a Round-Robin Study
B. Beckhoff[1], B. Pollakowski[1], R. Unterumsberger[1], S. Ladas[2], L. Sygellou[2], A. Schroeder-Heber[3], A. Nutsch[3], S. Gennaro[4], D. Giubertoni[4], and L. Vanzetti[4]
[1]**Physikalisch-Technische Bundesanstalt, Berlin, Germany**
[2]**Surface Science Laboratory, University of Patras, Greece**
[3]**Fraunhofer Institute for Integrated Systems and Device Technology, Erlangen, Germany**
[4]**Fondazione Bruno Kessler, Povo, Trento, Italy** *P.48*

**TU-24**, Atomic-Scale Modeling of Nanoelectronic Devices
A. Blom and K. Stokbro
**QuantumWise, Copenhagen, Denmark** *P.49*

**TU-25**, Localized Edge Vibrations and Edge Reconstruction by Joule Heating in Graphene Nanoflakes
M. Engelund
**DTU Nanotech, Department of Micro- and Nanotechnology, Technical University of Denmark, Lyngby, Denmark** *P.50*

**TU-26**, Atom Probe Tomography of Commercial Devices
D.J. Larson[1], P.H. Clifton[1], D. Lawrence[1], D. Olson[1], T.J. Prosa[1], D.A. Reinhard[1], R. M. Ulfig[1], L. Renaud[2], J.H. Bunton[1], D. Lenz[1], and T.F. Kelly[1]
[1]**Cameca Instruments Inc., Madison, WI**
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**TU-27**, Helium Ion Microscopy Characterization for Nano-Device Structures: SE Imaging and Ion Beam Luminescence Detection
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**TU-28**, Experimental Determination of Inelastic Mean Free Paths for Calculation of TEM Specimen Thickness
E. Verleysen[1,2,3], H. Bender[1], D. Schryvers[3], and W. Vandervorst[1,2]
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**TU-29**, Application of Scanning Transmission Electron Microscopy (STEM)-based Techniques for Development of Novel Si/SiGe on SOI FinFET Structures
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# Nanocharacterization Challenges in a Changing Microelectronics Landscape

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## ABSTRACT

As the microelectronics industry enters the "nano"-era new challenges emerge. Traditional scaling of the MOS transistor faces major obstacles in fulfilling "Moore's law". New features like strain and new materials (e.g. high k – metal gate stack) are introduced in order to sustain the performance increase. For a better electrostatic control devices use the 3rd dimension e.g. in gate-all-around nanowire structures. In this low dimensional regime a single atom can have a major impact in the performance and variability of the logic circuit: advanced measurement techniques are required to address this concern. Memories are probably the components where scaling is the most aggressively pursued. A slight shift in a row of atoms or the built-up of a nm-sized filament induces the bistability of the memory cell. In this paper we will show some examples of 2D and 3D characterization techniques at the nm-level which combine resolution, sensitivity and potentially throughput and in-line operation.

Due to the escalating cost and complexity of sub-28nm technologies fewer industrial players can afford the development and production of advanced CMOS processes. From a European perspective value in products can also be obtained in using more diversified non-digital technologies in the packaged devices (the so-called "More-than-Moore" domain, see Figure 1). Here also innovative measurement techniques are needed to characterize devices as diverse as image sensors, NEMS or biochips which will be eventually integrated with the logic chips through advanced packaging techniques including 3D integration and TSVs.

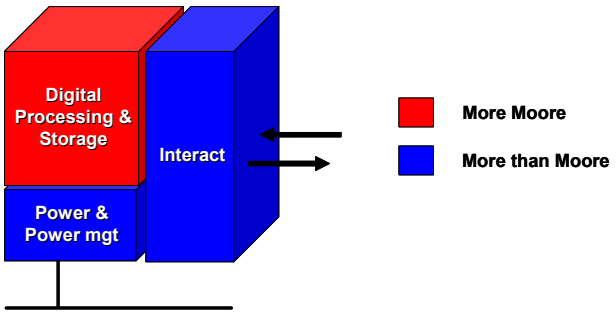


**FIGURE 1.** "More-than-Moore" devices complement the "More Moore" digital processing and storage elements in allowing the interaction of the packaged system with the outside world and in powering it. From [1]

Keywords: More Moore, More-than-Moore, heterogeneous integration, 3D integration, nanocharacterization

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On-line at http://www.itrs.net/Links/2010ITRS/IRC-ITRS-MtM-v2 3.pdf

# Nanoelectronics and More-than-Moore at IMEC

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## ABSTRACT

We are entering the 5th decade of CMOS technology scaling. It is slated to bring 22, 16, and 12 nm nodes to production. Geometric scaling will continue using computationally optimized multi patterning 193nm immersion lithography and next generation EUV lithography. For logic devices, the main challenges to be addressed are the transition from planar Si device architectures to FINFET device architectures to better control short channel effects. Engineering the high-k/metal gate and strain engineering solutions introduced in planar device architectures on these 3D topographies will be a non trivial R&D challenge. Overall system energy efficiency is the key challenge to be tackled. Power supply voltage has scaled poorly over the past decade leveling off about 1 Volt. Replacing the Si channel with III-V materials with intrinsic higher channel mobility than the Si channel holds the promise to operate future devices at supply voltages of 0.5 Volt. Tunnel FETS are believed to be a likely candidate to enable scaling beyond the 10 nm node. The TFET architecture potentially enables to combine a steeper sub-threshold slope (<60 mV/decade) with a high on-state current. It will bring us to the 6th decade of nanoelectronic scaling.

Innovations developed for logic devices have been further adapted to scale memory technology. High-k dielectrics for MIM capacitors in DRAM, development of vertical FETs access transistors, transition to Cu interconnect enable denser and faster DRAM chips. Floating Body RAM is being researched as next generation DRAM combining switch and memory functions in a single device. Similarly, high-k dielectrics as interpoly and tunnel barriers have enabled floating gate flash technology to continue scaling. Resistive RAM is being researched as next generation NVM technology.

3D TSV technology opens the 3rd dimension for system scaling. It allows to further increase system performance and functionality by enabling new system architectures taking advantage of stacking divergent technologies. Using 3D TSVs, technologies developed for chemical, optical, thermal sensing functionality can be integrated in compact form factors on energy efficient computational engines. Similarly, progress in MEMS and new functional materials will enable various systems innovations to alleviate challenges like efficient health care, sustainable energy consumption and an overall smarter environment.

The innovations in nanoelectronics and More-than-Moore technology pose tremendous challenges to physical and chemical analysis. Novel analysis techniques such as AtomProbe (Fig 1) enable to extract high resolution 3D dopant distributions. Defect characterisation of selectively grown III-V layers and characterisation of interface properties of III-V materials with dielectric materials in features sizes relevant for sub 22 nm nodes will be necessary to understand and optimize device operation.

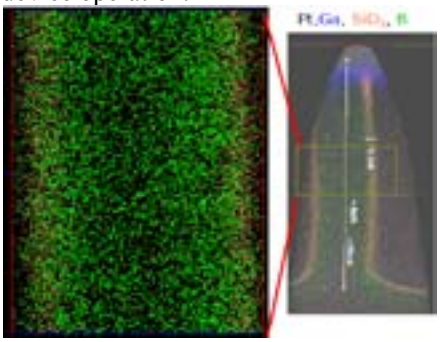

**FIGURE 1.** Elemental analysis (B) with spatial resolution of 0.4 nm in a 40 nm Si FIN using AtomProbe

**Keywords: CMOS scaling, 3D TSV, MEMS**

2-1



# More than Moore or More Moore: a SWOT Analysis

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## ABSTRACT

Over the last decade, the world of semiconductors has broadened its horizon from More Moore to More than Moore. Some first hypothesized the end of Moore's law and the beginning of a new era. They saw it as an OR gate while some saw it as a NOR gate. Since then it has been an AND gate as Moore's law has continued to move down it's persistent scaling path. Even if it fades, i.e. the end of More Moore, both will technologies will flourish. The reason is that More than Moore is complementary to More Moore semiconductor technology. More than Moore is largely made up of MEMS, which integrate microelectronics with micromechanical structures. Some include 3D packaging, LEDs, and Photovoltaic cells into the mix. In the future there are NEMS, or Nano-Electrical-Mechanical-Systems. In all cases the use manufacturing methods and metrology evolved from semiconductors. Metrology is critical to all these technologies, because to make something, you must be able to measure it, and to do that you must be able to see it.

This presentation examines the Strengths, Weaknesses, Opportunities and Threats (SWOT) for both classical semiconductor markets and these emergent technologies. It delves into how their technologies are evolving and the economic impact of this evolution. It addresses such questions as:

- Is scaling measurably slowing?
- Are design costs getting too high?
- What are the critical factors for a Moore's Wall scenario?
- As chips become an ever big-player game, will there be enough research centers to support metrology development.
- How fragmented is the More than Moore Market?
- Who are the leading players?
- Will they cross the valley of death from MEMS to Bioelectronics?

# The Status and Future of Metrology: Challenges from the ITRS Metrology Roadmap

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## ABSTRACT

The International Technology Roadmap for Semiconductors (ITRS) has provided a picture into the future technology requirements for integrated circuits for about twenty years. The ITRS continues to project these technology requirements for transistor, memories, interconnect, and lithography with a fifteen year horizon. New materials and structures are described as potential solutions to circuit based requirements for future transistors, capacitors, and interconnect. Since the inception of the ITRS, metrology has been challenged by these requirements and the Metrology Roadmap captured these requirements and potential solutions. Frequently, the Metrology Roadmap has indicated that the metrology community does not have a capability that meets key future measurement needs such as critical dimension, overlay, and film thickness. This presentation will cover the near and long term measurement requirements for metrology based on the ITRS and project potential solutions to these needs. The presentation will also discuss advances and gaps in measurement capability for the new materials and structures that the ITRS discusses for Beyond CMOS.

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# Metrology and Characterization Challenges for Emerging Research Materials and Devices[1]

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## ABSTRACT

The ITRS Emerging Research Materials (ERM) and Emerging Research Devices (ERD) Technology Workgroups have identified materials and devices that could enable continued increases in the density and performance of future integrated circuit(IC) technologies and the challenges that must be overcome; however, this will require significant advances in metrology and characterization to enable progress. New memory devices and beyond CMOS logic devices operate with new state variables (e.g. spin, redox state, etc.) and metrology and characterization techniques are needed to verify their switching mechanisms and scalability, and enable improvement of operation of these devices. Similarly, new materials and processes are needed to enable these new devices. Additionally, characterization is needed to verify that the materials and their interfaces have been fabricated with required quality and performance.

New materials and processes are also needed to extend lithography, interconnects, and assembly and packaging, and metrology is needed to verify and improve functional performance. While directed self assembly is a candidate for extending lithography, metrology is needed to characterize defect densities of these thin polymers over large areas to determine whether it will be possible to achieve ITRS defect densities of $<0.01 cm^{-2}$. For extending copper interconnects, metrology is needed to evaluate the effectiveness of ultrathin diffusion barriers to 1nm in thickness. For more advanced concepts, such as carbon nanotubes or graphene for interconnects and vias, metrology is needed to evaluate the contact resistance and quality of materials deposited into vias and interconnects. For carbon nanotubes(CNTs), metrology is needed to determine their density and determine whether growth factors will limit this density. Furthermore, as graphene or CNTs are deposited on other materials, it is important to determine whether their performance has been degraded by interfacing to these materials.

In assembly and packaging, materials are needed to enable a thermal hierarchy of assembly temperatures, low stress on the integrated circuits, and spreading of heat generated between the ICs. The challenge for assembly materials is to be able to simultaneously satisfy required thermal conductivity, modulus, hardness, adhesion, electrical resistivity, moisture resistance, and other functional properties. Nanosolders offer the possibility of establishing a thermal hierarchy for assembly, but the resulting structure and reliability of these solders must be verified when they are connecting multiple ICs.

The critical challenge is to develop characterization techniques that can determine whether it is possible for the emerging materials and devices to achieve their most important performance limitations and be viable candidates for progressing to process or circuit development.

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# Carbon Based Nanoelectronics

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## ABSTRACT

Carbon nanoelectronics are strong candidates in replacing or supplementing Si technology. Theoretical and experimental studies have shown that carbon based transistors perform well at nanoscale device dimensions. Significant progress has been made for graphenen radio-frequency (RF) applications where high on/off ratio is not necessarily required. IBM graphene FETs (GFET) yield the highest cut-off frequency ($f_T$) values reported: >200 GHz on epitaxially grown SiC wafer and >150 GHz on CVD-grown-transferred onto Si wafer, which are well above ITRS Si MOSFET $f_T$-$L_g$ trend. Device simulations show that transconductance can be greatly improved by further reducing the contact resistance and structure optimization. $f_T$ as high as 350 GHz is expected for 90-nm self-aligned gate GFET. A novel reconfigurable graphene p-n junction based logic device will be introduced. Its switching is accomplished by using co-planar split gates that modulate the properties that are unique to graphene including angular dependent carrier reflection which can dynamically change the device operation, leading to reconfigurable multi-functional logic. Epitaxy is to produce wafer-scale, high-quality graphene. A decomposition-based technique is implemented with in-situ monolayer control using a UHV growth chamber, equipped with low-energy electron diffraction microscopy (LEEM), which is capable of monolayer thickness precision and provides real-time electron reflection images from the graphene surface, allowing graphene formation via Si desorption from the SiC surface to be studied, optimized and controlled. 1-2 layers of graphene uniformly grown across Si-face SiC wafers with only monolayer variation exhibits high Hall mobility >4000 $cm^2V^{-1}s^{-1}$. It is an important advance in large scale graphene epitaxy. Chemical vapor deposition (CVD) is another promising way to produce large-scale graphene which hold great commercialization potential at low cost. IBM demonstrated large dimension, single layer high quality graphene sheets CVD grown on Cu foil and later transferred to any desired substrate (Si wafer).

IBM also demonstrated a wafer-scale fabrication of high performance CNFETs using an 8" Si-CMOS line. A novel embedded poly-Si gate structure is employed to provide excellent electrostatics, CMOS process compatibilities and threshold tuning ability through gate doping. The nanotube transistors maintain their performance as their channel length is scaled from 3 mm to 15 nm, with an absence of short channel effects. The 15-nm device has the shortest channel length and highest room-temperature conductance and transconductance of any nanotube transistor reported. Finally, we demonstrate the performance of a nanotube transistor with channel and contact lengths of 20 nm, an on-current of 10 mA, an on/off current ratio > 13000, and peak transconductance of 20 mS. These results provide an experimental forecast for carbon nanotube device performance at dimensions suitable for future transistor technology nodes through the next decade of the technology roadmap.

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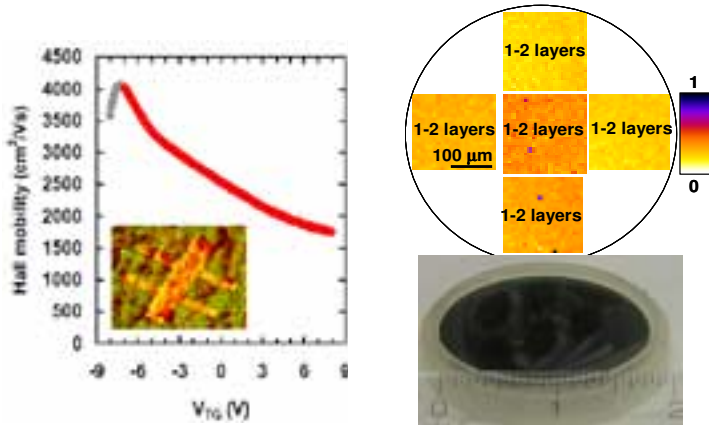


**Fig. 1.** Hall mobility and atomically smooth graphene of 1-2 layers with monolayer variation is uniformly grown on 2" SiC.

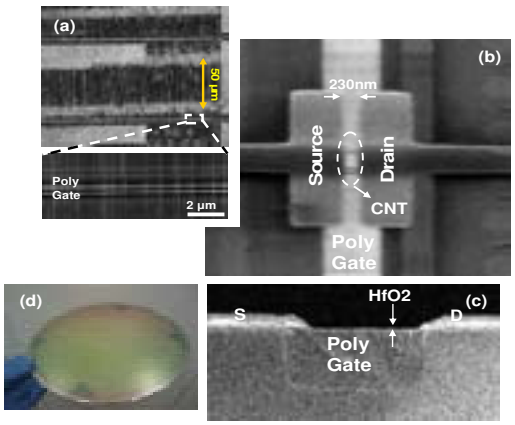


**Fig. 2** (a) Transferred aligned CNTs on the wafer with embedded poly gates. (b) Top, (c) cross-sectional view. (d) Fully-processed 8" wafer with CNFETs.

# Quantum control and engineering of single spins

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## ABSTRACT

Eighty years since Dirac developed the quantum theory of electron spin, contemporary information technology still relies largely on classical electronics: the charge of electrons for computation and the magnetic materials for permanent storage. There is a growing interest in exploiting spins in semiconductors for the manipulation and storage of information in emergent technologies based upon spintronics and quantum logic. Recently, localized electronic states of carbon-based materials have appeared as a unique solid state platform for fundamental measurements at the single spin level. In diamond, the spins of individual nitrogen-vacancy (NV) color centers can be imaged and manipulated at room temperature and have remarkably coherence times. We perform gigahertz coherent control of individual NV center spins in a new dynamical regime [1], including spin rotation on the same timescale as the Larmor precession. We find strong hyperfine coupling with the intrinsic N nuclear spin, thus offering a potential resource for both quantum information processing and atomic storage [2]. In addition, we present a technique to nanofabricate single spins based on broad-beam nitrogen implantation through apertures in electron beam lithography resist. This method enables high-throughput nanofabrication of large scale spin arrays with ~50nm spatial accuracy [3]. By combining coherent spin control with resonant optical excitation we demonstrate non-destructive spin measurement and coherent spin manipulation through the optical Stark effect [4]. In contrast to destructive readout methods traditionally employed to measure spin states, these interactions preserve coherence and enable the coherent exchange of quantum information between spins and light. These results may facilitate coherent measurement, control, and entanglement that is scalable over large distances.

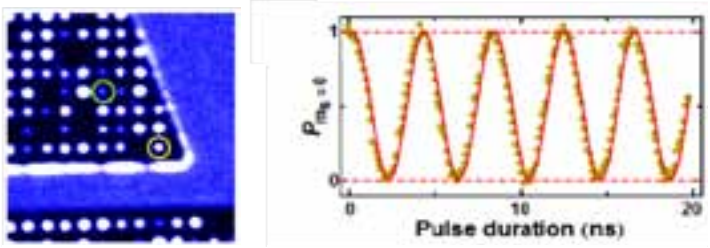


**FIGURE 1.** Section of implanted spin array with microwave control line; 300K measurement of single electron spin coherence.

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4-1

# Discrete Tomography in Materials Science

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## ABSTRACT

Over the last decade, electron tomography has become a powerful tool in the investigation of nanostructures in materials science. The possibility to obtain *qualitative* 3-dimensional (3D) information has already taken nanocharacterization to a new level, but gaining access to *quantitative* 3D information is the next step in the evolution of electron tomography. The increasing demand for quantitative results in 3D is not only driven by new developments in nanotechnology, but also by theoretical modeling studies that exactly require this type of information.

The so-called “missing wedge” has mostly been considered to be the main factor preventing reliable quantification of a 3D reconstruction. The missing wedge is related to the fact that it is often impossible to tilt a sample over 180°, due to the limited area for the sample holder in between the objective pole pieces of the microscope. The lack of 2-dimensional (2D) projection images for a certain range of angles will consequently result in a “missing wedge” of information in Fourier space, which will cause artifacts in the final 3D reconstruction. Although these artifacts may already hamper a qualitative interpretation of the 3D data, they will completely prevent quantification of 3D results. Therefore, several novel tomography holders and acquisition schemes have been developed [1-3]. However, despite these efforts, quantitative interpretation of a 3D reconstruction is still not straightforward. Here, we therefore evaluate the use of so-called "discrete tomography" for quantitative electron tomography in materials science.

Discrete tomography is an alternative reconstruction technique that uses prior knowledge on the object that has to be reconstructed [4,5]. More specifically, an estimate of the number of different gray levels (corresponding to different compositions) that can be expected in the original object serves as an input. One of the advantages of this approach is an improvement of the quality of the reconstructions in comparison to reconstructions based on the conventional reconstruction algorithms. Moreover, if the number of possible gray values is small, it is often possible to obtain very accurate reconstructions based on a few projections. Furthermore, missing wedge artifacts are strongly reduced, and segmentation is performed automatically during the reconstruction procedure, which will enable quantitative electron tomography. It will be shown that discrete tomography is therefore a very powerful tool to solve a broad range of materials science problems ranging from the 3D study of carbon nanotubes to semiconductor devices.

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# Materials Characterization in Nanodomains and Interfaces - Challenges and Opportunities

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## ABSTRACT

Over the past 3 decades the semiconductor industry has doubled the number of transistors on integrated circuits every 2 years, following an empirical law widely known as Moore's law. The ability of the semiconductor industry to stay on Moore's law has enabled the digital revolution and now the convergence of communications and computing. However, as the size of the smallest structures decrease, this has required the introduction of many new materials and the interactions of these heterogeneous materials and processing is increasing in complexity. With these decreasing dimensions, three factors become important; 1) Size to volume ratio is high leading to multi-material interactions, 2) sizes of nano-domains (such as grain boundaries) and devices become comparable, 3) interfaces or buried surfaces become dominant. The future of understanding these systems resides in modeling and metrology. This paper reviews some of the challenges in materials science and the opportunities for using fundamental characterization techniques to enable successful management of these heterogeneous interactions. As the industry evaluates new materials for future technologies, research is needed to develop new characterization techniques including modeling to evaluate nano-materials and materials with nano-scale dimensions and structure. Specific topics covered will include some technology problems, key metrology techniques such as NMR, nanoindentation, and modeling techniques such as quantum and atomistic methods.

5-1



# TSOM Method for Nanoelectronics Dimensional Metrology

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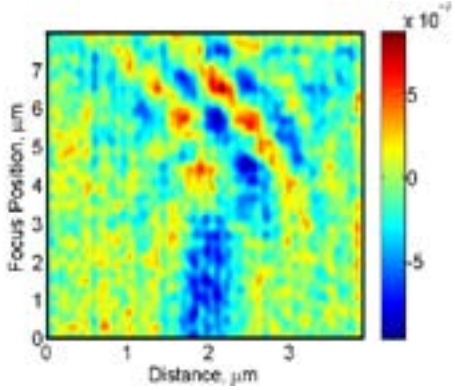
**Abstract**. A relatively new "through-focus scanning optical microscopy" (TSOM-pronounced as "tee-som") method [1-5] transforms conventional optical microscopes to truly 3D metrology tools for nanoscale to microscale dimensional analysis with potentially sub-nanometer scale resolution. The method can be used in both reflection and transmission modes of microscopes. It is applicable to a wide variety of target materials ranging from transparent to opaque, and shapes ranging from simple nanoparticles to complex semiconductor memory structures, including buried structures under transparent films. Potential applications of TSOM include defect analysis, inspection and process control, critical dimension (CD) metrology, photomask metrology, overlay registration metrology, nanoparticle metrology, film thickness metrology, quantum dots, 3D interconnect metrology (large range depth analysis such as TSVs), line-edge roughness measurement, and nanoscale movement of parts, e.g., in MEMS/NEMS [3]. Numerous industries could benefit from the TSOM method —such as the semiconductor industry, MEMS, NEMS, biotechnology, nanomanufacturing, nanometrology, data storage, and photonics. The method is relatively simple and inexpensive, has a high throughput, provides nanoscale sensitivity for 3D measurements and could enable significant savings and yield improvements in nano/microscale metrology and manufacturing. Potential applications are demonstrated using experiments and simulations.

TSOM is not a resolution enhancement method. However, it has a potential to provide lateral and vertical *measurement* sensitivity of less than a nanometer using a conventional optical microscope [3-5], comparable to the dimensional measurement resolution of typical scanning electron microscopes (SEMs) and atomic force microscopes (AFMs) and is expected to extend the limits of optical metrology. The TSOM method has the ability to decouple vertical, lateral or any other dimensional changes at the nanoscale with little or no ambiguity and has the potential to analyze target dimensions ranging from a few tens of nanometers to relatively large dimensions (tens or even hundreds of micrometers in the lateral and the vertical directions, beyond the reach of typical SEM and AFM) with similar nanometer scale sensitivity. This presentation will describe the method of constructing a TSOM image using a conventional optical microscope along with experimental and simulated results showing nanoscale sensitivity. An experimental measurement with about a nanometer difference in the linewidth of a 45 nm wide Si line on Si substrate is shown on the left (using 546 nm illumination wavelength).

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**Keywords:** TSOM, Nanometrology, Optical microscopy, Through focus scanning

# Origin Of Resistivity Change In NiO Thin Films Studied By Hard X-Ray Photoelectron Spectroscopy

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## ABSTRACT

The flash memory technology driving the market of portable electronic devices is rapidly approaching miniaturization limits. As the industry moves toward memory cells with 22-nm lateral features (1) charge trapping becomes increasingly difficult.

Therefore a new class of non-volatile memory devices rather based on resistivity change is being intensively investigated by the scientific community. OxRRAM (oxide resistive random access memory) are advantageous in terms of data retention, low power consumption, and 3-D architecture compatibility. The transition metal oxide compound surrounded by two metallic electrodes can be tuned between a high resistive state and a low resistive state by the application of a bias. However, the understanding of the resistive switching is critical for further device integration and optimization. Several models (2-4) have been proposed to explain the resistance change phenomenon but none confirmed experimentally.

We have investigated the origins of the resistivity change during the forming of NiO based resistive random access memories using hard X-ray photoelectron spectroscopy. This technique allows a non-destructive chemical analysis of the switch structure with information depth of about 30 nm. Energy shifts (Fig 1 left) and band gap states suggest that oxygen vacancies are created in the low resistive state. As a result the resistive switching could correlate with conduction via defects such as electrons traps and metallic nickel impurities. Transport of oxygen atoms could be facilitated by crystalline defects, such as those observed by high resolution cross-sectional TEM images (Fig 1 right). Our results provide concrete evidence of the major role played by oxygen defects in the resistance switching mechanism.

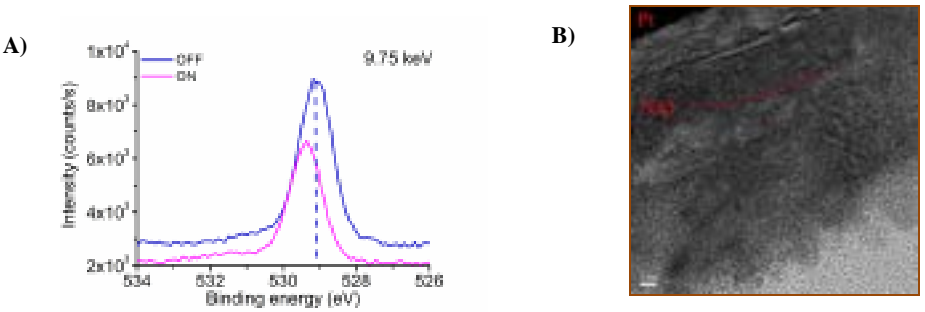


**FIGURE 1.** A) O 1*s* (b) core level spectra obtained by HAXPES at 9.75 keV. The OFF state represents the oxide high resistance state whereas the ON state represents the oxide in the low resistance state. Bands shift towards high binding energies in the ON state relatively to the Fermi level are probably due to *n*-doping induced by the creation of oxygen vacancies. B) Transmission electron microscopy image of the NiO/Pt stack. Defects were observed in the NiO layer.

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**KEY WORDS:** RRAM, synchrotron radiation, defects

# Nanoscale Chemical Characterization by Auger Electron Spectroscopy*

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## ABSTRACT

State of the art Auger nano-probes are more and more competitive to characterize the devices developed for nanotechnologies. Auger Electron Spectroscopy (AES) and Scanning Auger Microscopy (SAM) are gaining interest to investigate the surface chemical composition with high lateral resolution (< 10 nm). We will present the new capabilities of these techniques by the analysis of innovative nanostructures. In particular, the potential of the Auger nano-probe from Physical Electronics recently installed at the Minatec NanoCharacterization Platform will be illustrated.

The potential of SAM will be shown in terms of high lateral resolution, stability over time and sensitivity. From one hand, we investigate the chemical composition of nanodots (~10nm in height) formed during Si anneal at 900°C under UHV. These impurities, formed from surface contamination, are identified as SiC dots by Auger analyses. From the other hand, the interest of SAM is also demonstrated by the analysis of Si nanowires. The coaxial geometry prevents shadowing effects and enables uniform chemical mapping of these structures. Location of the Copper catalyst and investigation of the oxidation states are performed with high lateral and energy resolution.

In-depth chemical analysis is another interesting aspect of the technique. Results obtained by cross-section analysis and depth profiling will be compared. From one hand, tests performed on cross-sections of CdTe/CdS based solar-cells devices will be shown. These results also evidence the efficiency of charge neutralization for measurements on glass substrates. From the other hand, Auger depth profiles measured for high-k/metal gate stacks allow to clearly identify thin LaO layers (<1nm).

Auger microscopy can also bring information complementary to TEM based techniques. SAM is performed on Focused Ion Beam (FIB) cross-sections to obtain the surface chemical composition. A direct comparison between high resolution TEM images and Auger mapping will be presented. The advantages and specificity of each technique will be discussed.

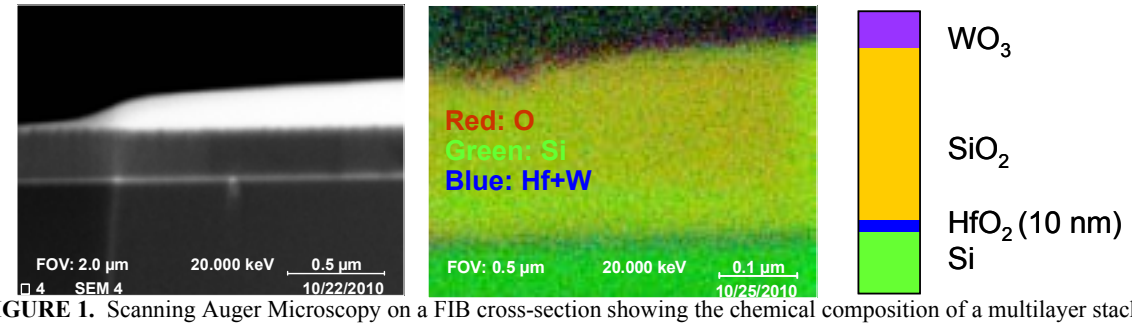


**FIGURE 1.** Scanning Auger Microscopy on a FIB cross-section showing the chemical composition of a multilayer stack. The thin (10 nm) $HfO_2$ layer is clearly identified.

**Keywords:** AES, SAM, Auger mapping, depth profiling, Si nanowires, SiC formation, TEM, cross-section

**This work was supported by the french "Recherche Technologique de Base" program.*

# Analytical Study of BAM (Al/GaAs) and Photovoltaic Samples Using State-of-The Art Auger Nanoprobes*

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## ABSTRACT

For the analysis of Bundesanstalt für Materialforschung und–prüfung, BAM, (Al/GaAs) and Photovoltaic samples, we used new generations JEOL JAMP-9500F Field emission Auger Microprobe[1] and PHI-700 Xi Nanoprobe. These nano-probes are generally used for the characterization of complex nano-structures. For the JEOL JAMP-9500F Field emission Auger Microprobe system, it uses an electrostatic hemispherical analyzer (HSA) with multi-channel detectors. The energy resolution (ΔE/E) can be varied from 0.05% to 0.6% and high lateral resolution of 8 nm (25 KV, 1 nA) for Auger analysis and 3 nm (25 KV, 10 pA) for secondary electron imaging can be reached. For the PHI-700 Xi Nanoprobe system, it uses a cylindrical mirror analyzer (CMA) with a coaxial electron gun. The energy resolution is 0.1% and lateral resolutions are 8 nm (20 KV, 1 nA) for Auger analysis and 6 nm (20 KV, 1 nA) for SEM. Firstly, we used the JEOL system for the determination of the surface composition of a BAM (Al/GaAs) reference sample (figure 1). In that, we studied the different thicknesses of Al/GaAs lines to show astonishing possibilities of the deeper detection and sensitivity with this newly designed system. Moreover, we investigated very precisely the point, line, depth profiling and Auger mapping on the sample with high energy resolution. Secondly, we used the PHI-700 Xi Nanoprobe system for Photo voltaic samples. Here, we used the nano-probe system to find the different interfaces like a-Si:H (n)/ZnO/Al interface and ITO/a-Si:H (p) interface. However, limitations such as image drift due to acoustic vibration and heating effects due to continuous bombardment of energetic electron at the same point are still a big challenge for both the systems.

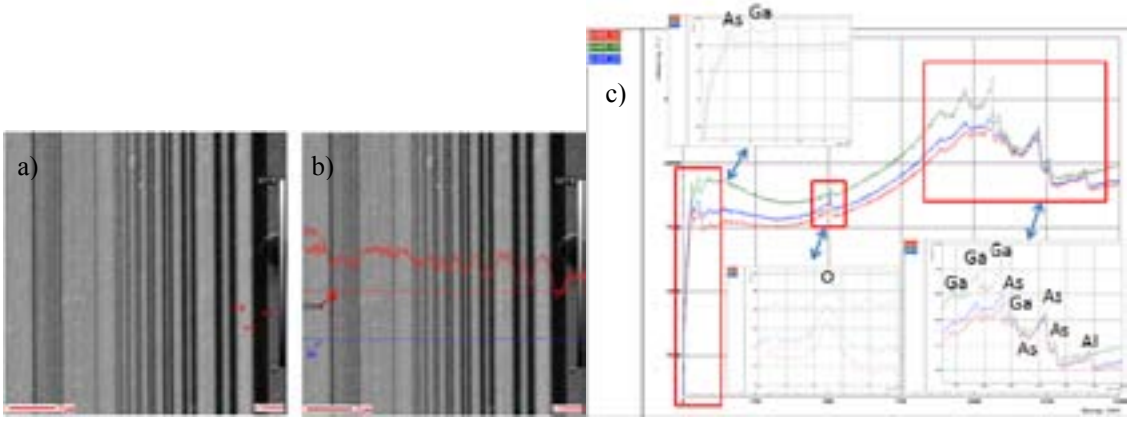


**FIGURE 1.** JEOL JAMP-9500F Field Emission Auger Microprobe (20kV, 10 nA, 30° tilt): a) point analysis, b) line analysis, c) corresponding Auger spectra.

**Keywords:** AES, SAM, SEM, Auger mapping, Photovoltaic, cross-section

**References:** [1] D. Karpuzov, A. He, S. Xu, *Surf. Interface Anal.* 2006; **38**: 287-291

**This work was supported by the European EuroTalent program and french "Recherche Technologique de Base" program.*

# Atom Probe Tomography and Nanoelectronics

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## ABSTRACT

The design of Atom probe tomography (APT) 20 years ago has been an outstanding event. The first prototypes were developed at Oxford, GB and Rouen, France (1,2). For the first time it has been possible to map out the distribution of chemical species at the atomic scale in 3D (3). With the recent implementation of ultra-fast pulsed laser to the instrument, a new breakthrough has been achieved. Previously limited to metals, semiconductors as well oxides can now be analysed. This challenging innovation has made APT a unique approach for atomic-scale investigations in nanoelectronics (4,5,6,7). The two versions of this instrument developed in the lab (4) and in USA (5) are now both marketed by CAMECA–AMETEK. Unique capabilities of APT will be highlighted on the basis of some selected salient illustrations (clustering of boron or arsenic in implanted silicon, segregation of dopants (B, As) to grain boundaries in polycrystalline silicon, as well as to interfaces, extended defects and dislocation loops (figure), reactive diffusion Ni-Si (contacts in microelectronics), bipolar transistors…).

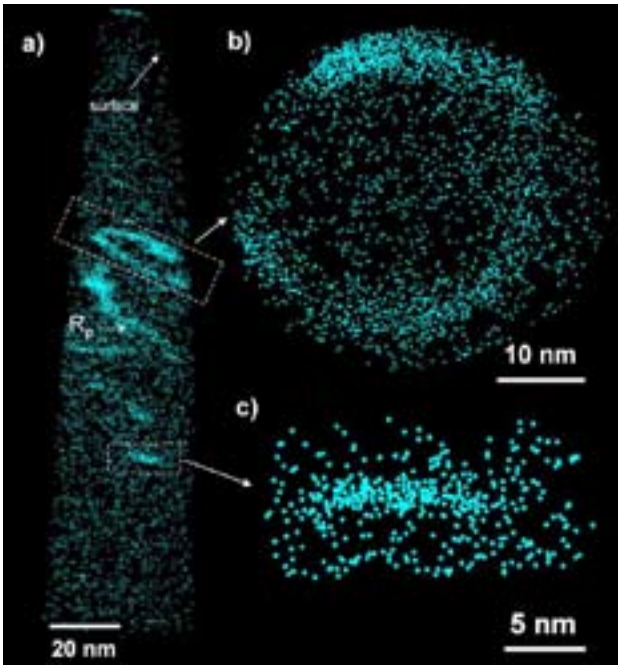


**FIGURE 1.** 3D reconstruction of boron-enriched Cottrell atmospheres in implanted silicon (7)

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*Key words: silicon, dopants, atomic-scale distribution*

# Characterization of Strain Induced by PECVD Silicon Nitride Films in Transistor Channel

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In order to reach high level of transistor performances, it is desirable to increase electrical conductivity of the device. An efficient way to enhance carrier mobility in conduction channel is to generate strain in the structure induced by process. To achieve that, stress engineering of the contact etch stop layer (CESL), an amorphous hydrogenated silicon nitride film deposited by plasma enhanced chemical vapour deposition on top of the metal oxide semiconductor assembly, is widely used since it is a low-cost technique. Indeed, this film possesses an intrinsic stress that can be set from tensile (σ=1.6GPa) to compressive (σ=-3.0GPa) depending on deposition conditions.

From an electrical point of view, strain induced in silicon channel can lead to an increase of carrier mobility as high as 8-10% which in turn increases Ion/Ioff and decreases switching time of the transistor. Usually, strain induced in the channel is very low (0.1 – 0.3%), making quantitative measurements challenging. Moreover, stress transmission mechanisms are not fully understood at a nano-metric scale.

To evaluate stress transmission to silicon channel, we are using dark-field electron holography characterization technique operating on both Titan and Tecnai F20 transmission electron microscopes. Strain maps with nanometre spatial resolution, high sensitivity ($\Delta\varepsilon \approx 10^{-3}$%) and large field of view (400 – 500nm²) have been obtained on CESL strained devices. To understand stress transfer mechanisms, we have analysed structures with varying parameters such as film thickness, stoichiometry, film stress, structure density. The experimental results are compared to those obtained by simulation.

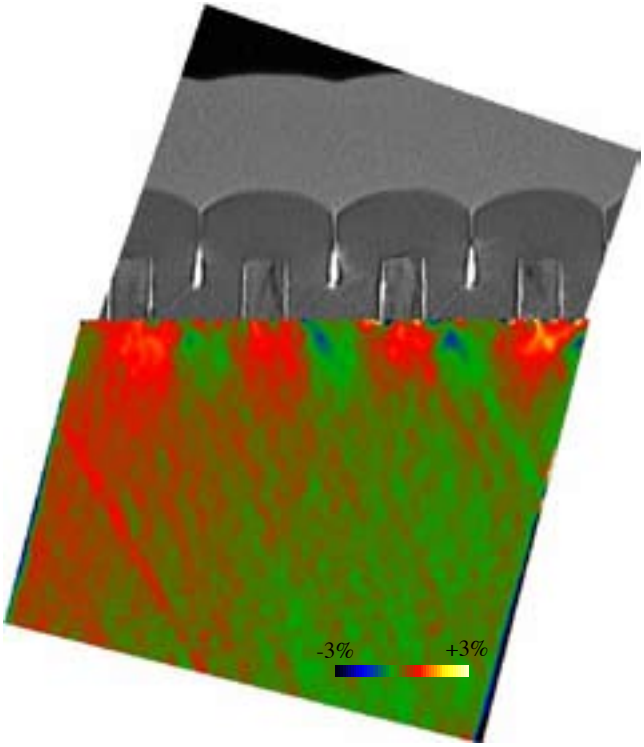


Figure 1: Strain map of a MOS structure with tensile (σ=1.6GPa) CESL stressor

*Keywords: holography, transistor, stress*

# AFM analysis of high temperature dewetting under ultra high vacuum of ultrathin solid silicon films on insulator

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## ABSTRACT

The dewetting of ultrathin silicon layers, induced by the thermal budget, is an issue to develop SOI-based technology. This study aims at demonstrating the effect of the strain on the dewetting mechanism [1] (Figure 1). For that purpose, we present the results obtained on (001) oriented ultrathin (<11 nm) silicon layers on silicon dioxide (SOI). Both stress-free and strained (s-SOI) films fabricated using the "Smart-cut®" [2] process have been studied. We used two s-SOI samples, with respectively 0.8% and 1.6% in-plane strain in the top silicon film.

In order to understand the dewetting mechanism, samples were heated up to ~800°C under ultra high vacuum ($1\times10^{-9}$ mBar) during 10 minutes. The dewetted area topography was characterised by both non-contact and tapping-mode AFM. In addition the chemical composition of these areas was analysed by nano-Auger electron spectroscopy.

AFM results show that Si agglomerates are always present during the dewetting. We will present clear evidences of the influence of strain on the size and density of these Si agglomerates. Moreover, we will show the importance of surface contamination. It is well known that, when heated in ultra high vacuum, carbon contamination can result in silicon carbide (SiC) nanodots [3]. These nanodots induce instabilities at the silicon film surface. Thus, it affects the dewetting mechanism.

To summarize: (i) the level of strain in the silicon films impacts the size and the density of Si agglomerates (ii) silicon carbide nanodots induced by surface contamination influence the dewetting.

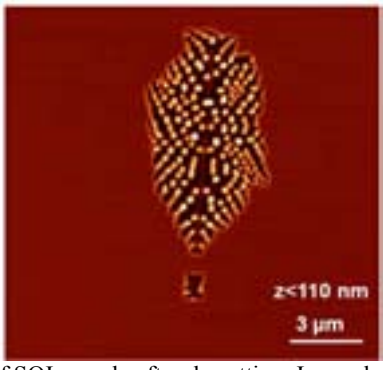


**Figure 1.** Topography of SOI sample after dewetting. Image by AFM in tapping mode.

Keywords: dewetting, strained silicon, surface contamination.

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# MOTIS: A Focused Ion Beam Source Based On Laser-Cooled Atoms

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## ABSTRACT

Focused ion beams (FIBs) are an invaluable tool for the creation and observation of materials with nanoscale feature sizes, providing key capabilities in integrated circuit sectioning, critical dimension measurement, and circuit repair. However, ion sources capable of both high brightness and low emittance operation are difficult to realize, with practical sources limited to very few atomic species. Recently, we have developed a new type of low-emittance, high-brightness ion source based on the ionization of magneto-optically trapped atoms[1]. Using this source, known as a magneto-optical trip ion source (MOTIS), we have demonstrated nanoscale-focused ion beams of both lithium and chromium.

The MOTIS uses laser-cooled neutral atoms that are photoionized to create an isotopically pure beam of ions whose ion optical properties are comparable to or better than those of liquid metal ion sources. The MOTIS paradigm can be extended to create ion sources from any atomic species that can be laser-cooled, i.e., Li, Na, K, Rb, Cs, Fr, Mg, Ca, Sr, He, Ne, Ar, Kr, Xe, Al, Ag, Cr, Er, Cd, Hg, and Yb. This flexibility allows the atomic species of the source to be tailored to the specific application, e.g., microscopy with light ions, milling with heavy ions, and nanoscale implantation of a variety of elements. In addition, the inherently low energy spread enables the creation of high-resolution focused ion beams at low energy.

We report on the construction and performance of MOTIS-technology-based lithium and chromium FIBs. Each FIB platform consists of a chromium or lithium MOTIS that is integrated with a conventional ion optical column. We will present results of microscopy using chromium and lithium beams and a characterization of focal spot sizes. We will also examine applications of this technology, such as beam-activated surface chemistry, direct deposition and removal of materials, and deterministic single ion implantation.

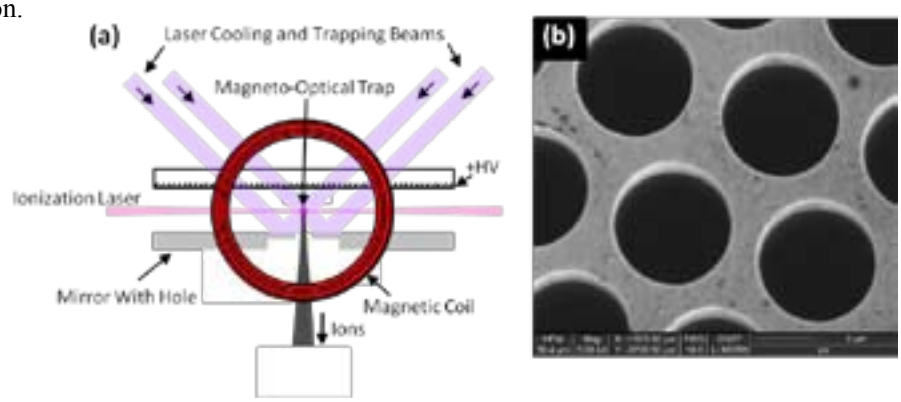


**FIGURE 1.** (a) Schematic of Magneto-Optical Trap Ion Source. (b) Image of microchannelplate pores acquired with a 2 kV, 2 pA $Li^+$ beam.

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# Surface Imaging and Spectromicroscopy Of Technological Materials: Complementarities Between Electron Spectroscopies, Scanning- and Ion Probes

O. Renault, E. Martinez, N. Chevalier, D. Mariolle, Ł. Borowik, J-C. Barbe, J. –P. Barnes, M. Veillerot, F. Bertin, A. Chabli

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## ABSTRACT

Engineering of surfaces and interfaces is a key step in the integration of technological materials, which must now be addressed at a local level. Surface-sensitive microscopies are therefore becoming increasingly important. However, within the wide landscape of advanced devices, from sub-32 nm transistors to micro-systems, the diversity of both scales and type of information to be addressed prevents from using a unique method being used in a reliable way. Thus, it is necessary to implement different techniques in a complementary way. Proximity and ultra-high vacuum environment are additional requirements for extracting reliable, cross-checkable information.

In this contribution, we will highlight the specificities of two state-of-the-art electron spectroscopy-based imaging techniques and their complementarities with scanning- and ion probes. These two methods, high-resolution XPS spectromicroscopy (XPEEM) and Nano-Scanning Auger Microscopy (SAM), have made recently significant progress in terms of lateral and energy resolution [1]. More specifically, XPEEM with laboratory X-ray sources now provides spectromicroscopic information from decananometric to mesoscopic scales [1,2], whereas novel Nano-SAM systems now offer Auger nano-analysis at high lateral (10 nm) and energy resolutions ($\Delta E/E=0.1\%$ and less). The complementarities will be presented in terms of (1) accessible lateral scales, (2) acquisition speed (scanning or full-field imaging modes) and (3) type of information available. Particularly we will highlight the capabilities of a characterization approach combining all these techniques in terms of multi-scale analysis. Selected examples will be given to illustrate this point, from the formation of SiC nanodots at silicon surfaces (Fig1, right) to graphene domains on SiC(0001) (Fig. 1, left) and sealing technologies for NEMS packaging.

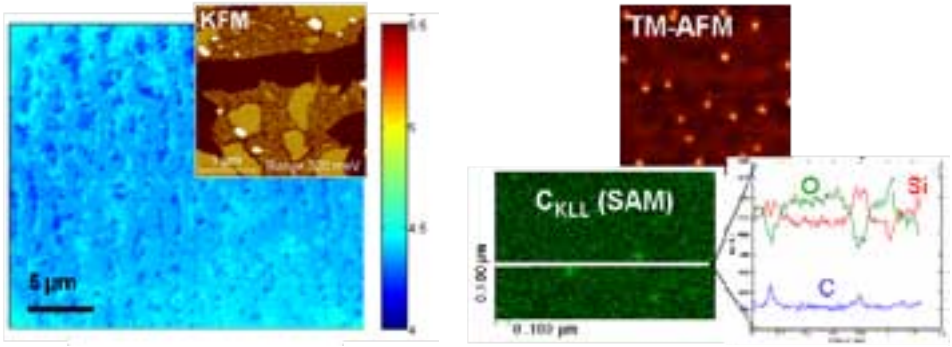


**FIGURE 1.** *Left:* Local work function maps by XPEEM and KFM of graphene domains on SiC(0001). *Right:* Nanodots identified by AFM at a silicon surface and corresponding analysis by nano-SAM.

**Keywords:** XPS spectromicroscopy, XPEEM, Auger mapping, SAM, work function, AFM, KFM, Tof-SIMS

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# Effects of Roughness on Scatterometry Signatures

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## ABSTRACT

Recent development in the optical characterization allows using more complex experimental methods in order to characterize periodic structures [1]. The new trend is to examine potential of the Mueller matrix and multi-configuration methods in order to access the most challenging problems of the optical metrology. In this work we are going to present results acquired on the artificially perturbed periodic line grating with significant line width roughness (LWR). The method used in this work is based on the generalized ellipsometry, which provides not only the spectrally resolved $\Delta$ and $\psi$, but also eleven elements of the Mueller matrices.

Application of the multi-azimuth method allows for the robust analysis of the perturbed and unperturbed gratings [2] with an estimation of the model parameters accuracy. Moreover, using Mueller matrices provides extra advantages including: the information in the block off-diagonal elements for different conical configurations; the estimation of the measured data accuracy by combining adequate configurations; the complete description of the depolarization effects. Our situation is slightly complicated by experimental conditions requiring significant focusing of the incident light beam into the small feature area. The focused incident beam leads to Mueller matrices with significant depolarization characteristics which have to be taken into account also in the optical model. The effect is more pronounced in spectral regions, where the signal changes very fast.

Recent theoretical works on the sensitivity of angularly resolved data to the LWR [3,4] demonstrated significance of the problem and explored limits of effective medium approximations for the purpose of LWR modeling. In this work, we are more focused on modeling of perturbed periodic structures (see Fig. 1) using the rigorous coupled-wave method and evaluating of the sensitivity of the experimental spectrally resolved data to the dimensional parameters of LWR.

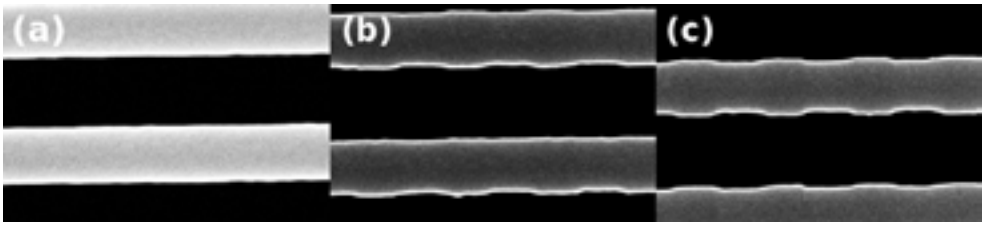


**FIGURE 1.** Scanning electron microscopy images of diffraction gratings with artificially manufactured line-width roughness. The amplitudes of modulation as a fraction of the unperturbed line-width are: (a) unperturbed; (b) 2%; and (c) 5%.

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# Recent Advances in 2D-Band Structure Imaging by *k*-PEEM and Perspectives for Technological Materials

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## ABSTRACT

The imaging of surfaces using the PhotoElectron Emission Microscopy (PEEM) technique has recently received considerable interest, mainly thanks to the use of high brilliance synchrotron radiation which facilitates the study of surface properties and chemical selectivity [1, 2]. By placing a transfer lens in the optical column of a high transmission and full energy-filtering PEEM, it is possible to image the focal plane, instead of the image plane. Hence, the corresponding image shows the angular distribution of the emitted photoelectrons, for a given kinetic energy. By varying the kinetic energy, the complete energy filtering provides full 2D cuts of the band structure in reciprocal space, called k-PEEM [3]. This approach has two advantages over classical ARPES measurements. No uncertainty is introduced due to sample rotation and the images obtained are directly $I(k_x, k_y)$. Therefore, full 2D band mapping is possible, with potential acquisition times considerably shorter than in a classical ARPES set-up.

The k-PEEM technique has been successfully used to study the band structure of metals and alloys, such as Ag(111) and Ag(001) [3], Cu(111) [4], and Au(111), as shown in figure 1 (left). The 2D mapping of these samples enabled us to achieve high momentum resolution and to clearly observe surface features, demonstrating the performances of this technique [5]. We have already performed some studies on epitaxial graphene on SiC, which had reveal the potential of this technique, by presenting numerous information on a selected area, providing chemical and work function mapping along with its band structure. By these very promising results on the performance of this technique, we report here the recent advances of band structure imaging on technological samples of high interest.

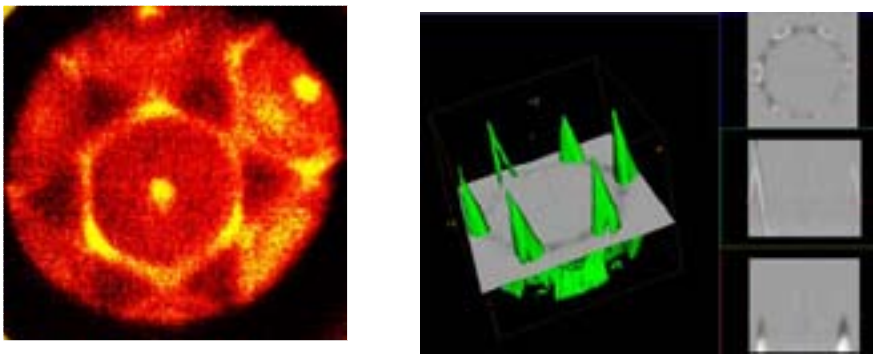

FIGURE 1: (left) *k*-space image of Au(111) taken at the Fermi energy, excited at 90 eV, with an exposure time of 100 seconds. (right) Experimental 3D image [$I(k_x, k_y, E)$] obtained on epitaxial graphene on SiC(0001), excited with He I

**Keywords:** X-PEEM, *k*-PEEM, band structure imaging.

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TU-11



# Characterization Of Nanodevices By STEM Tomography

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## ABSTRACT

In order to overcome the limitations encountered by the further scaling of the metal-oxide-semiconductor field effect transistors (MOSFETs) and of the flash memories, new device architectures are introduced. The vertical nanowire tunnel field effect transistor (TFET), with good short channel characteristic (low leakage current) and a subthreshold slope smaller than 60mV/decade (physical limit for the MOSFETs), and the bit cost scalable (BICS) flash memory are among the considered structures for further miniaturization.

The vertical nanowire TFET device consists of a cylindrical single crystalline silicon wire perpendicular to the silicon substrate with the gate layers stack wrapped around it. The BICS flash memory device consists of a cylindrical plug in the polysilicon control gate (CG) in which the memory layers stack (silicon oxide/silicon nitride/ silicon oxide) is deposited. The plug is subsequently filled with the polysilicon channel. Both the nanowire of the TFET device and the plug of the BICS flash memory have a diameter of about 70nm for the studied devices.

Due to the cylindrical symmetry and to the dimensions of these structures, smaller than the typical thickness of the TEM specimens, the overlap of different materials along the electron beam direction renders the interpretation of the conventional TEM and STEM images difficult. Tomographic 3D reconstruction from high angle annular dark field scanning (HAADFS) TEM images series overcomes this problem and is therefore likely the most suited technique to characterize the structure of such nanodevices.

Frontal tomographic slices coming from the center of the TFET and of the flash memory are presented in figure 1 and 2, respectively. Due to the presence of materials with a wide range of atomic numbers for the TFET device, the difference of contrast exhibited by the low-Z materials is small limiting the clear distinction of these layers. The different low-Z materials composing the BICS flash memory however are more clearly observed in tomography than on the conventional TEM and STEM images.

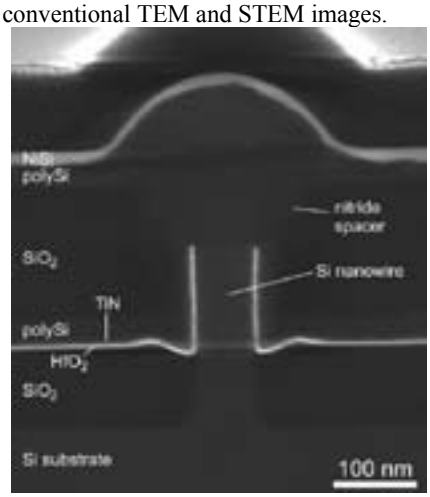


**FIGURE 1.** Frontal tomographic slice of the center of the TFET device

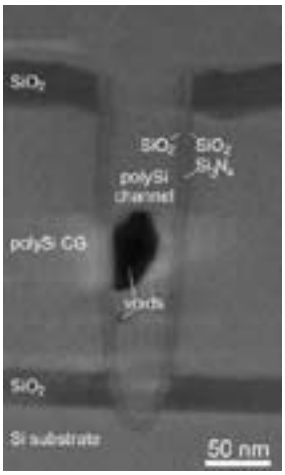


**FIGURE 2.** Frontal slice of the center of the BICS flash memory

Keywords: nanodevices, electron tomography

# Three dimensional investigation for the 22-nm-node and beyond: surface morphology of gate-all-around transistors by atom probe and electron tomography.

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## ABSTRACT

Gate-all-around (GAA) Si nanowire transistors are promising candidates for future CMOS devices [1]. They present a low off-state leakage current and offer high performance for sub-22 nm technologies [2]. The fabrication of such devices involves the conformal deposition of the gate stack directly around etched semiconductor Si nanowires. It is known that electrical properties of these devices are directly linked to the morphology and roughness of nanowires [3]. In this poster, we will show that the combination of electron tomography and atom probe tomography allows a fully 3D morphological characterization of the GAA devices, as it shows on the figure 1. Atom probe tomography, based on the field effect evaporation, is the only technique capable of chemically quantifying at the atomic-scale resolution in three dimensions, as it has recently demonstrated in semiconductors [4].

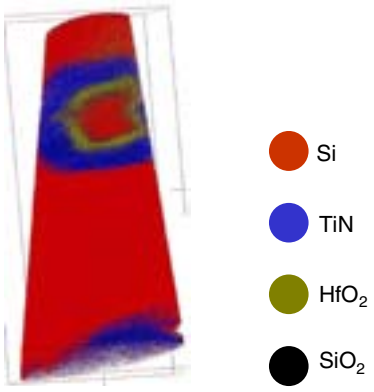


Fig.6: 3D reconstruction of GAA device by atom probe tomography.

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[4]: E. Cadel et al. J. Appl. Phys. 106, (2009), 044908.
[5]: This work was performed as part of the IBM – STMicroelectronics – CEA/LETI-MINATEC Development Alliance.
[6]: This study has been done in the frame of the french RTB program.

Keywords : Gate-All-Around, morphology, electron tomography, atom probe tomography.

# Strain In Semiconductor Nanowires And Device Integration

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One-dimensional nanowires (NWs) are promising materials for future nanodevices owing to their small dimensions and novel properties. After ten years of materials optimization [1], it is now possible with the help of X-rays and synchrotron radiation to draw some preliminary conclusions about the structural requirements necessary to tune the physical properties of demanding devices in terms of strain control and size distribution. The frontiers of information given by diffraction experiments performed at the European Synchrotron Facility will be illustrated by III-V and IV-IV semiconductor devices.

Quantitative structural information about epitaxial arrays of Au-catalyzed NWs will be reported for InAs/InP longitudinal [2] and core/shell [3] heterostructures grown by MOCVD on InAs $(111)_B$ substrates (see Fig. 1 (a-b)). *Grazing incidence X-ray diffraction* (GIXRD) and *crystal truncation rod* measurements allow separating the NW contribution from the substrate overgrowth and give averaged information about crystallographic phases, epitaxial relationships with orientation distribution, and strain. Wrap gate InAs NWs have been also studied after $HfO_2$ dielectric coating and Cr metallic deposition necessary for transistor integration. X-ray diffraction allows determining the strain tensor and shows a longitudinal contraction increasing with $HfO_2$ and Cr shell depositions. The measurement of grazing incidence X-ray scattering [2, 3] for different azimuths with respect to the nanowire edges has shown the signature of the initial hexagonal shape and of the coating thicknesses of the wires.
Longitudinal InP/InAs/InSb NW heterostructures with different InAs insertion thicknesses will be also presented. *Anomalous scattering* measurements and *reciprocal space mapping* close to the As and Sb absorption edges (11.8 and 30.5 keV) allows estimating the InAs interdiffusion inside the wires and separating the structural and chemical part of the strain relaxation occurring in complex heterostructures.

Mechanical relaxations of strained Silicon On Insulator (sSOI) nanostructures will be discussed from the point of view of isolation and implantation processes used in transistor technology (see Fig. 1 (c)). The strain in long etched sSOI lines of different widths and 2D sSi samples implanted by As/Xe ions with the same stripe geometry (the gate stack acting as an implantation mask) is measured by GIXRD [4]. Then, Fully Depleted Silicon-On-Insulator (FDSOI) n and pMOSFETs (Metal-Oxide-Semiconductor-Field-Effect-Transistors) integrated with a TiN/$HfO_2$ gate stack on 1.55 GPa strained SOI (sSOI) and 2.1 GPa eXtremely strained SOI (XsSOI) substrates will be analyzed. The performance improvement in terms of effective mobility as well as the threshold voltage has been systematically extracted as a function of the gate width and the channel orientation for long and narrow n and pMOSFETs and correlated to strain properties [5].

Recent results corresponding to the use of micro-beam *coherent Bragg diffraction* on single and buried wires will also be presented. Size requirement (sample and beam) and reconstruction of strain distribution in single wires will be illustrated with the previous samples (see Fig. 1 (d)).

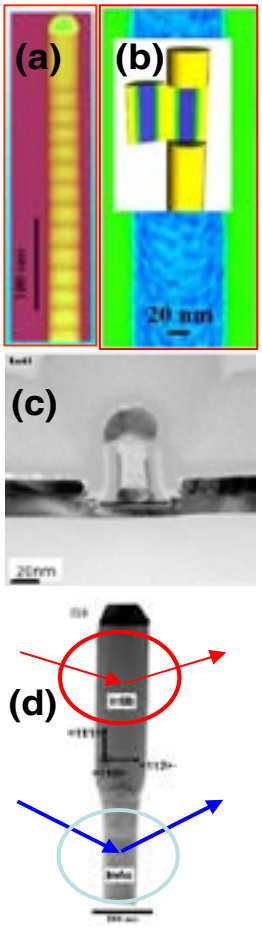


**Figure 1.** Examples of NWs studied by X-ray: (a) assembly of longitudinal InAs/InP NWs, (b) Core/shell Cr/$HfO_2$/InAs assembly, (c) Si active layer in n-MOSFET on SOI (arrays of transistors), (d) single InSb/InAs NW with a micro-beam.

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**Keywords:** X-ray diffraction, assembly and single objects, nanowire devices.

TU-14



# Physico-chemical and Electrical Characterization of Gate Stacks on GaAs and (In,Ga)As

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Due to their higher carrier injection velocity, III-V compound semiconductors are being studied as potential candidates to replace Si as active channel material in C-MOS technology. However, the integration of a suitable gate stack on III-V channels may be even more challenging than the integration of high-k-based gate stacks on Si. The following issues must be addressed: I) efficient cleaning methods leading to clean, stoichiometric and ordered III-V surfaces have to be developed; II) efficient passivating methods to minimize the amount of electrically active defects at the III-V/dielectric interface need to be defined; III) the gate stack must be thermodynamically stable against the temperatures used for gate stack deposition and post-deposition processing like source/drain formation. In particular, substrate oxidation has to be *totally* avoided; IV) gate stack composition must be optimized to achieve high gate capacitance and low defect density in the dielectrics and at their interfaces.

*In-situ* X-ray photoelectron spectroscopy (XPS) is a powerful characterization tool which allows one to address all these issues, providing an excellent feedback for the adjustment of the growth parameters and the post-deposition thermal treatments. This will be shown by discussing the case of GaAs and $In_{0.53}Ga_{0.47}As$ channels cleaned by remote RF H-plasma in UHV and passivated by a thin layer of amorphous Si before deposition of the high-k oxides [1]. XPS gives a comprehensive picture of the gate stack, ranging from the properties of the cleaned surface (removal of contaminants, stoichiometry, band bending, Fermi level (FL) pinning), to the effect of the passivating layer on the III-V surface (interfacial chemistry, thickness of the passivating layer, valence band offset, FL de-pinning) and to the interaction between the different layers [Figure 1(a)]. Electrical properties of gate stacks on GaAs and $In_{0.53}Ga_{0.47}As$ channels [Figure 1(b)] will be presented and correlated to the gate stack properties determined by XPS. Finally, we will show how XPS analysis is decisive in determining a gate stack deposition procedure which leads to *scaled* devices with outstanding electrical characteristics.

**Key words : III-V CMOS, Passivation, XPS**

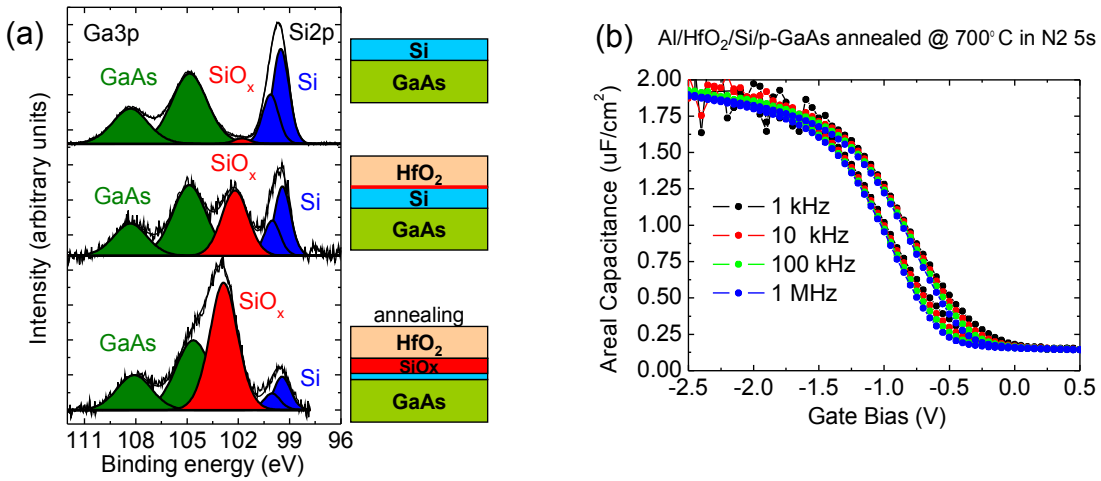


**FIGURE 1.** (a) XPS spectra showing the evolution of the Si passivating layer upon $HfO_2$ deposition and post-deposition anneal at 700°C in $N_2$ for 5s. (b) Capacitance vs voltage characteristic for an Al/$HfO_2$/Si/GaAs MOS capacitor.

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# Quantitative Strain Measurement Using Nanobeam Electron Diffraction and Dark Field Electron Holography

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## ABSTRACT

Nanobeam Electron Diffraction (NBED or NBD) [1] and Dark Field Electron Holography (DFEH) [2,3] are recently developed transmission electron microscopy (TEM) based techniques that are able to quantitatively measure the strain with a spatial resolution of a few nanometers and a strain sensitivity of respectively $6.10^{-3}$ [4] and $2.10^{-4}$ [5].

We will compare both techniques applied to different samples like SiGe multilayers on Si (Fig. 1.a), nanowires (Fig 1.b and 1.c) and SOI devices. We will discuss the advantages and disadvantages of each technique when applied to these different samples. Criteria like sample preparation, spatial resolution, processing time, required TEM competences and reliability of strain measurement will be used to classify NBED and DFEH. Finally, it will appear that these two techniques are complementary and should both be applied on the same sample Severy time it is possible.

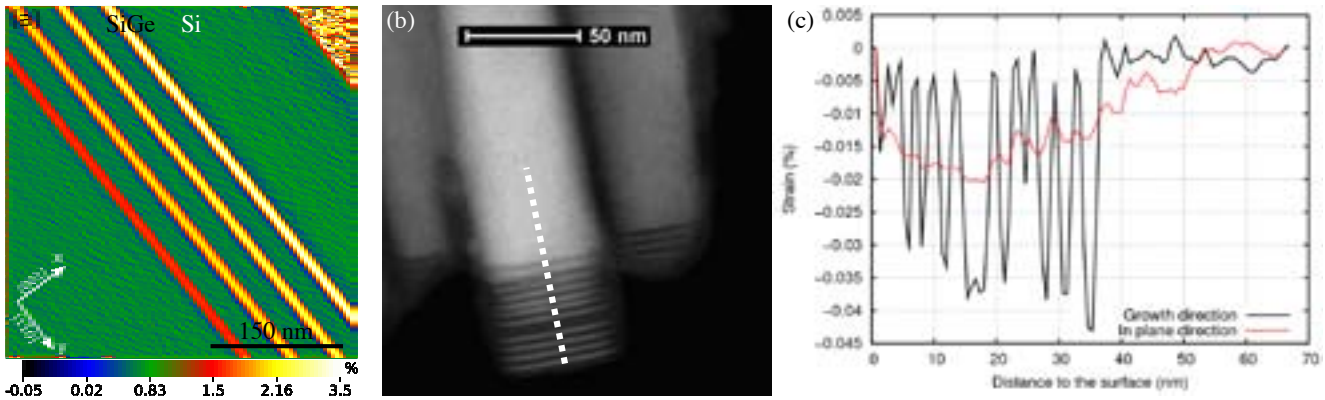


**FIGURE 1.** (a) Strain map obtained by DFEH on SiGe multi-layers embedded in a Si matrix. (b) GaN nanowire presenting AlN insertion barriers. (c) NBED strain profile of the GaN/AlN nanowire presented in (b).

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# Investigation of Surface Potential on CdTe/CdS p-n Heterojunction with Kelvin Probe Force Microscopy

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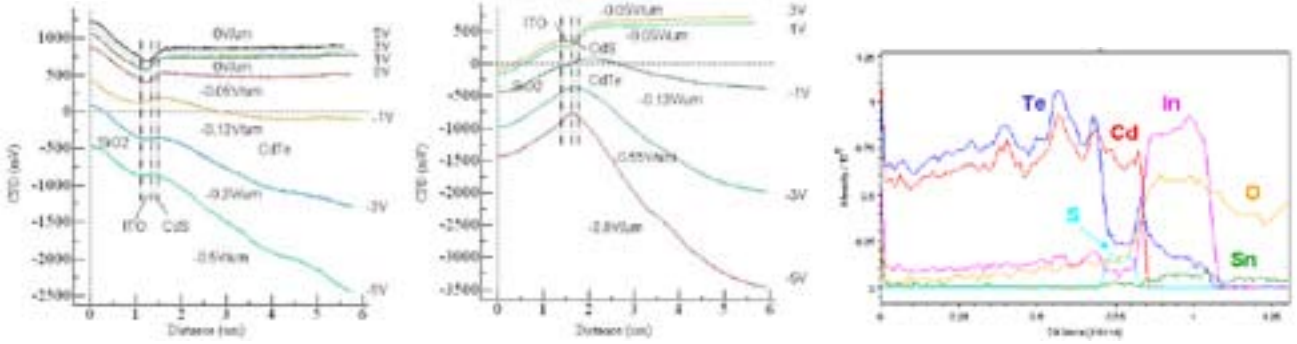
## ABSTRACT

CdTe/CdS photovoltaic (PV) modules have become the lowest-cost producer of solar electricity, despite working at lower efficiency (up to 16.5%) than crystalline silicon cells [1]. Polycrystalline CdTe cells are more efficient comparing to their single crystalline counterparts. However, the charge transport mechanisms responsible of this effect are not clear [2].

In this communication, we report a series of Kelvin probe Force Microscopy (KFM) measurements, suitable to observe the topography and the distribution of the Contact Potential Difference (CPD) inside the structure of the device: CdTe/CdS/ITO/Glass. The sample is prepared by mechanical polishing in order to decrease the roughness after the cleaving process. In order to have a better understanding of the charge transport inside the solar cell and to vary the Fermi level pinning effect[3], different bias are applied to the sample. The CPD variations with different bias on cross-section in the dark and under illumination condition are presented on figure 1(a) and (b) respectively. In both cases, we observe the reverse bias widens the CdTe/CdS depletion region. Under illumination, electron-hole pairs are generated at the interface and modify the electric field inside the material at the same position. Moreover, the surface chemical composition has been investigated by Nano-Auger Electron Spectroscopy (AES) to confirm the boundary line of different layers as shown in figure 1(a)(b), which are assumed from the corresponding topography measurement. All the detailed results will be discussed in this presentation.




(a) (b) (c)

**FIGURE 1.** Cross section characterization on CdTe/CdS solar cell (a) CPD as measured by KFM with different bias under dark condition, electric field between the distance of 2um and 3um are indicated (b) under illumination (c) Nano-Auger analysis on surface chemical composites.

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**Key words: thin-film solar cell, KFM, Auger Electron Spectroscopy.**

# New Method of Electron Diffraction for Characterization of Nanomaterials using the Scanning Electron Microscope

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## ABSTRACT

A new method is described for obtaining and analyzing the crystallographic structure and orientation of nanoparticles and ultrathin films using conventional electron backscatter diffraction (EBSD) equipment in the scanning electron microscope (SEM). Electron-transparent samples of nanoparticles, thin films or nanowires, which can be suspended on transparent carbon film substrates, were positioned immediately below the pole piece of the SEM by use of a custom made holder. This allowed electron diffraction patterns to be captured in transmission from nanometer-scale areas on the samples using a conventional EBSD camera. Such an arrangement obviates the need for a transmission electron microscope (TEM). The resulting diffraction patterns were displayed with EBSD software on a computer screen. In this fashion, we obtained diffraction patterns from nanoparticles as small as 20 nm in diameter and from nanowires with widths as small as 30 nm, as shown in figure 1. Patterns were also obtained from free-standing thin film metal samples sandwiched in copper grids and from thin metal samples deposited on silicon nitride window substrates. When coupled with an energy dispersive spectrometer (EDS) for elemental analysis, this diffraction technique provides a tool for phase ID of nanometer-sized particles. In thin film samples, orientation mapping was facilitated by scanning the electron beam in the same manner that is used in reflection EBSD. With this mode of transmitted electron diffraction we observed improvements in pattern contrast, signal to noise ratio, and lateral spatial resolution compared to the same factors observed with conventional EBSD. These improvements are thought to be due in part to a strongly reduced contribution from diffuse scattering and can be qualitatively explained using Monte Carlo scattering simulations.

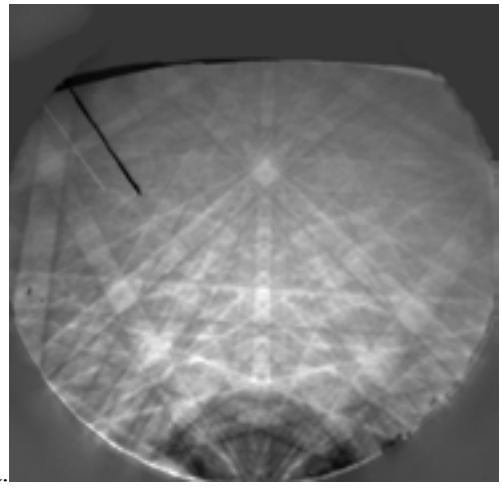
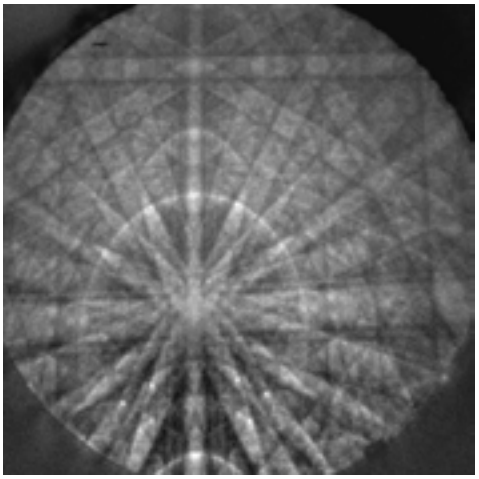
a.  b. 

**FIGURE 1.** Electron diffraction patterns taken in transmission using a standard EBSD camera in an SEM. Figure 1a is from a 20 nm diameter particle of $Al_2O_3$ and figure 1b is from a 30 nm diameter GaN nanowire. Both patterns were taken at 20 kV.

# Status And Trends In 3D Nanodevices: Inspection By Electron Tomography

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## ABSTRACT

The reduction of the size of modern semiconductor devices has lead to the requirement of characterisation techniques with nanometer resolution, and more recently these requirements have been extended to all three dimensions. Most classical characterisation methods provide only 2-dimensional projections and are therefore unable to reproduce the complex structure of 3D nanoelectronic devices. To perform 3D nanocharacterization, electron tomography must be implemented. In electron tomography, a sample illuminated by an electron beam is tilted while a series of TEM images are recorded. The images are then used as an input for 3D reconstruction algorithms. The process leads to a 3D image of the nanodevice with a depth-resolution almost equal to the lateral resolution.

The spatial resolution can reach few nanometers for a sample with a cross-section as large as 200nm. These dimensions correspond well to the needs of the nanoelectronics industry which makes electron tomography an ideal method for advanced device characterization. For crystalline samples High-Angle Annular Dark Field Scanning TEM (HAADF STEM) is especially well suited for image acquisition since the diffraction contrast becomes negligible. Therefore the projection requirement is fulfilled and 3D reconstruction algorithms can be used. HAADF STEM can provide chemical contrast as the signal of the projections is proportional to the mass-thickness product [1].

In this study we present the technique of electron tomography and discuss advantages and limitations. We report some recent HAADF STEM results for the characterization of nanowires and nanowire-based devices. In particular tomography allows the characterization of interface morphology in three dimensions which is frequently a critical parameter for device performance. The potential of energy-filtered TEM (EFTEM) tomography for quantitative chemical imaging of nanodevices is also highlighted [2].

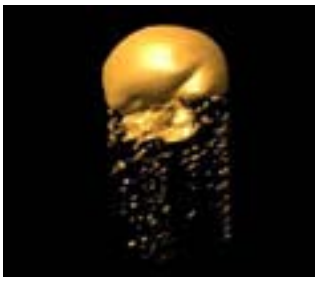

**FIGURE 1.** 3D reconstruction of gold catalyst particle on a silicon nanowire.

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Keywords: electron tomography, nanowires, morphology

# Enhanced Spatial Resolution Electrical Scanning Probe Microscopy Using Carbon Nanotube-Terminated Tips

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## ABSTRACT

Electrical scanning probe microscopes, such as the scanning capacitance microscope (SCM) for two dimensional dopant profiling, scanning Kelvin force microscope (SKFM) for surface potential measurements, and tunneling atomic force microscope (TUNA) for dielectric integrity measurements, are important tools for characterizing CMOS and nanoelectronic devices. A significant limitation of all these techniques is the terminal tip radius and the cone angle of the shank of the tip, which contribute substantial stray capacitance to the signal resulting in signal averaging over an area much wider than the terminal tip. To overcome this limitation, we have used conventional SPM tips terminated with a welded carbon nanotube (CNT). We have examined ultra-shallow junctions, high-κ gate stacks, low-κ intermetal dielectrics, and FinFET devices in cross-section with SCM and SKFM, using both conventional and CNT-terminated tips. We have also measured the electrical properties of the CNT-terminated tips. Spatial resolution improved substantially with the CNT-terminated tips compared to the conventional tips, but the CNT tips can introduce additional artifacts. We will present detailed comparisons of the two types of tips used for various SPM-based electrical characterization measurements that are useful for nanoelectronics.

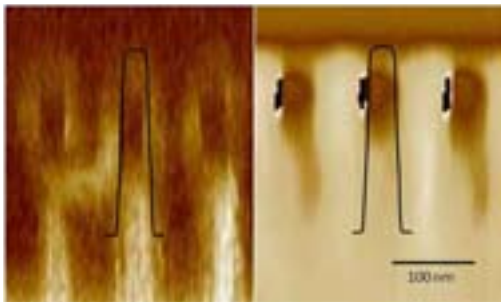

**FIGURE 1.** SCM images of 65 nm FINS measured with conventional (left) and CNT-terminated (right) tips.

# The Preparation with Argon Milling and Characterization with Cathodoluminescence of HB LED's

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## ABSTRACT

High Brightness LED's (HB LED's) are emerging as a viable lighting alternative for industrial, commercial as well as home use. The competitive advantage of HB LED's over alternative light sources are; their low power consumption and longer life-times. These market advantages must be balanced by their high production costs resulting in a much higher selling price. This high price mandates finding failure modes and increasing the reliability and lifetime of these devices for them to succeed in the market.

A key factor affecting the lifetimes of HB LED's is heat induced degradation of the LED at one of the many interfaces in a completed device. These interfaces occur between materials with widely different thermal, electrical and hardness characteristics. Therefore, making cross sections while preserving the interfacial structure is extremely difficult using either FIB, cleaving or mechanical polishing. An alternative method will be demonstrated using a collimated Argon beam with a shielding blade to produce an undamaged interface suitable for high resolution SEM imaging and analytical characterization. This paper will describe results using this Argon Beam cross sectioning technique along with Cathodoluminescence to characterize the LED layer structure as well as the phosphor for commercially produced HB LED's.

KEY WORDS: Argon Milling, Cathodoluminescence, HB LED's

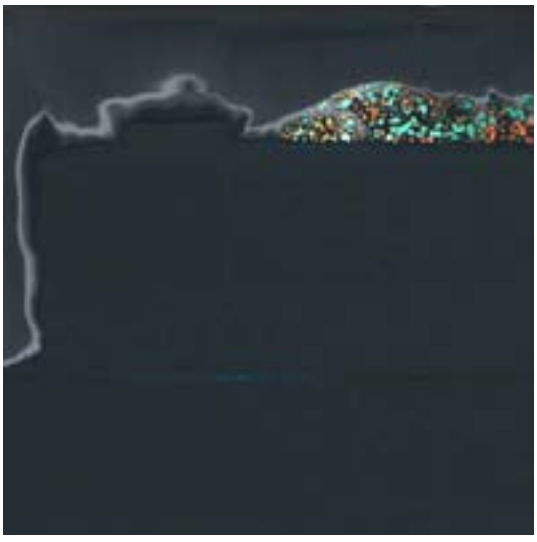

**FIGURE 1.** Cathodoluminescence from a Commercial HB LED Device

# X-Ray Reflectometry Parameter Uncertainties for Thin $SiO_2$ Films

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## ABSTRACT

The X-ray reflectometry measurement method provides researchers with a powerful tool for determining physical model parameters in thin film stacks. This data analysis is often performed using various optimization-based schemes to generate model refinement. Questions often arise as to the nature of the uncertainty for these optimization solutions. In this work, we apply in-house and collaboration-developed statistical methods for determining uncertainties for structural model solutions on measurements of thin films of $SiO_2$ on Si. The XRR measurements analyzed were performed at AIST. Our approach is to use Markov Chain Monte Carlo sampling of a Bayesian statistical model of XRR data using a well-established Parratt recursion model with Gaussian roughness and the simplest structural models which can adequately describe the data. Through careful analysis of posterior probability distributions and two-dimensional histograms of structural model parameters, one can establish uncertainties for each structural model parameter. One can also study the absence or presence of solution-space multi-modalities over allowed parameter ranges. The presence of such ranges may indicate the need for more prior information of a given structure, which is required before a single set of parameters can be determined. The figure below shows an example where two sets of solutions are evident in the analysis. The conclusion of this analysis are uncertainty estimates providing the contribution to uncertainty inherent within the XRR modeling method - an uncertainty rarely incorporated in parameter estimations.

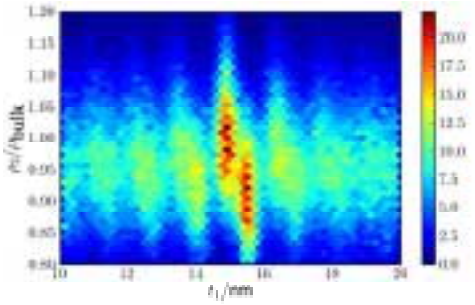

**FIGURE 1.** Two-dimensional histogram of Markov Chain Monte Carlo sampling frequency for a thin $SiO_2$ film thickness (horizontal axes) versus Si substrate density (vertical axis) showing a bimodal distribution in XRR model/solution space.

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# C-MOS Gate Silicide Analysis by Atom Probe Tomography

F. Panciera [a,b], K. Hoummada[b], M. Gregoire[a], M. Juhel[a], N. Bicais[a], D. Mangelinck[b]

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## ABSTRACT

Metal silicides are widely used as contacts and interconnections to source and drain in microelectronics devices. The Nickel monosilicide (NiSi) is integrated in advanced technologies because of the following advantages : low resistivity and low Si consumption, formation controlled by Ni diffusion, adequate work function for metal gates[i,ii]. It has been shown that the addition of Pt in the Ni film increases the nucleation temperature of $NiSi_2$ by approximately 150 °C, stabilizes the NiSi films[iii] and increases the temperature of NiSi agglomeration [iv]. Despite the large number of study about Ni silicide the chemical analysis of transistor silicide remains a great challenge.

In this paper, the gate silicides of n-type metal-oxide-semiconductor field effect transistor (MOSFET) were analyzed by atom probe tomography (APT). The sample analyzed is a 28 nm transistor from S-RAM produced by STMicroelectronics. The transistor has been extracted from the wafer (Fig.1a) by focused- ion-beam (FIB) site-selective lift-out and then prepared for APT analysis employing a serie of FIB annular millings (Fig.1b). APT analysis allows to measure the Pt and As concentration profile with sub-nanometric spatial resolution (Fig. 1c and d), evidencing a gradient in Pt concentration within NiSi and an As accumulation at NiSi/Si interface (Fig.1e). Moreover statistical distribution analysis and the detection of PtAs molecular ions in the mass spectrum suggest the formation of PtAs precipitates in NiSi phase.

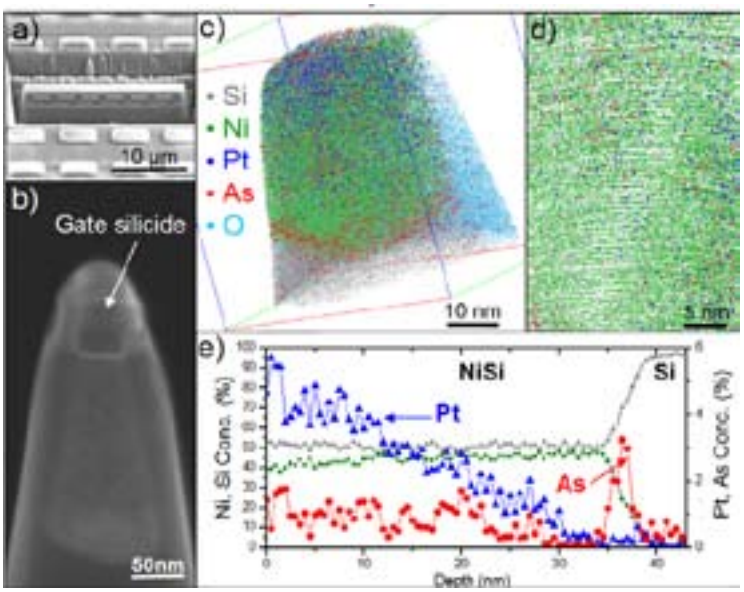


**FIGURE 1.** (a) Scanning electron microscopy image of FiB cut S-RAM lamella (b)Focused ion beam prepared APT specimen containing a transistor; (c) APT reconstruction of C-MOS gate silicate; (d) Details of analyzed volume showing NiSi atomic planes; (e) Concentration profile along tip axis direction.

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[iii] D. Mangelinck, J. Y. Dai, J. Pan, and S. K. Lahiri, Appl. Phys. Lett. **75** (1999) 1736.
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# Quantitative characterization of buried $B_xC_y$ nanolayers by complementary methodologies – a round-robin study

Burkhard Beckhoff[1], Beatrix Pollakowski[1], Rainer Unterumsberger[1], Spyros Ladas[2], Labrini Sygellou[2], Annemarie Schroeder-Heber[3], Andreas Nutsch[3], Salvatore Gennaro[4], Damiano Giubertoni[4] and Lia Vanzetti[4]

1. *Physikalisch-Technische Bundesanstalt (PTB), Abbestr. 2-12, 10587 Berlin, Germany*
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3. *Fraunhofer Institute for Integrated Systems and Device Technology (IISB), 91058 Erlangen, Germany*
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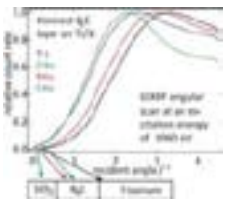
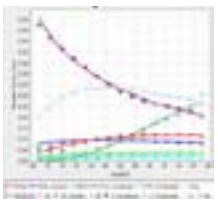
Improved metrology and characterization techniques for nano- and micro-electronics are required by both novel materials and shrinking dimensions. Providing complementary analytical methodologies [1] through cross-comparison, round-robin, and benchmarking was an objective of the European Integrated Activity of Excellence and Networking for Nano- and Micro-Electronics Analysis (ANNA). A corresponding ANNA round Robin addressed the quantitative characterization of buried nanolayers consisting of the light elements B and C. A set of different samples was to be analyzed by complementary methodologies. The sample structure was SiO2 cap layer / *t* nm thick BxCy / Ti, Ni or SiO2 on a Si wafer where the buried layer thickness *t* ranged between 1 nm and 50 nm.

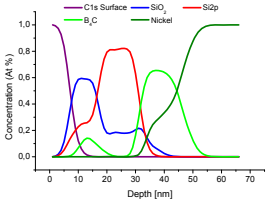
XRF and GIXRF investigations were performed with synchrotron radiation and calibrated instrumentation [2] in the PTB laboratory at BESSY II. The elemental sensitivity and penetration depth could be varied. XRF analytical results for B are well in line with the nominal layer values. GIXRF results (fig.) depend on the x-ray standing wave field. NEXFAS investigations were performed for the speciation of the buried layers. Samples with overlayers thinner than 10nm, were studied at SSL by standard XPS. Binding energies were referenced to the main C1s component at 284.8 eV. Buried $B_xC_y$ gave a C1s component near 282 eV (fig.) and a single B1s peak near 188.0 eV. Using data from the substrate, the $Si/SiO_2$ cap layer and $B_xC_y$, empirical sensitivity factors and a SSL procedure based on ISO18118(2004):E [3], atomic composition and layer thicknesses were sequentially determined, along with the respective estimated uncertainty. Non-destructive depth profiling is possible with angle resolved XPS (ARXPS) which was employed at IISB without any sample tilt or analyzer turning. The analyzer has a lens system, which collects the electrons from a solid angle of 60° being displayed on a detector array so that a specific angle interval can be related to particular detector channels. B4C depth information for a buried layer was obtained from modeling (fig.). At FBK, XPS investigations were replicated to match SSL findings, and SIMS (by magnetic sector and Time of Flight) was applied to assess the thickness of the BxCy films and to attempt a relative quantification of the stoichiometry of the probed layers. The results show a good agreement on the thickness evaluated using the two different techniques, whilst a clear assessment of the exact film composition resulted to be challenging.



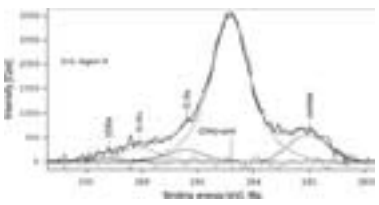
Figures: GIXRF scan



XPS angular probe




XPS depth profiling



Fitted XP spectrum in the C1s region

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2. B. Beckhoff, *J. Anal. At. Spectrom.* **23**, 845-853 (2008).

# Atomic-Scale Modeling of Nanoelectronic Devices

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## ABSTRACT

As device features near atomic dimensions, simulations of electrical currents need to be based on a quantum-mechanical description of the system rather than a classical one. New phenomena appear which can be exploited for novel device characteristics, but also fundamental challenges arise when the influence of single defects can have devastating effects. From a metrological perspective, the very definition of electrical current should be based on the quantum conductance, but in order to compare measurements and calculations accurately, a realistic atomistic description of the device configuration is required in order to properly describe impurities and defects.

Although atomic-scale calculations of ballistic tunneling currents have become rather mainstream over the last decade, many challenges remain. Tight-binding models may work for some systems, but fail to capture the electronic structure of metallic systems, or interfaces combining metals and semiconducting materials, in which cases first-principles [1] or semi-empirical [2] approaches becomes necessary. For transistor applications it is necessary to include gates and dielectric screening regions, and in other cases we may need to consider sequential tunneling in the weak coupling limit [3], rather than the more common coherent tunneling picture. Moreover, all of the above needs to be carried out for large-scale systems that might involve thousands of atoms.

We will provide an overview of these and other aspects of state-of-the-art atomic-scale modeling techniques, and show examples of how our software Atomistix ToolKit® is used used to study a wide variety of nanoelectronic device structures, such as graphene field-effect transistors, conductance of nanowires, molecular junction diodes, contact resistance of metal-semiconductor interfaces, leakage currents in ultrathin oxide layers, and so on.

**Keywords:** Atomic-scale modeling, electronic transport, software

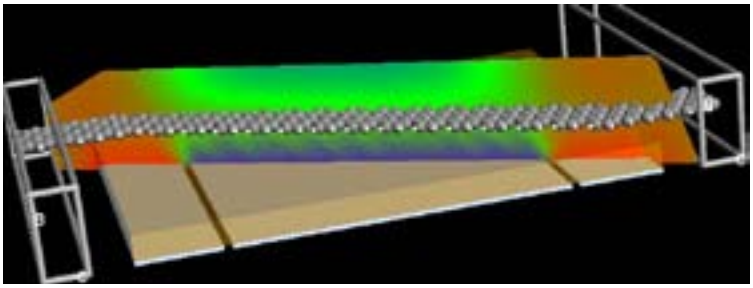

**FIGURE 1.** A field-effect transistor structure made from a Z-shaped metal-semiconductor-metal graphene nanoribbon junction. The blue bottom plate is a metallic gate electrode, and between it and the graphene is a dielectric screening region. The figure displays the effective potential, and shows how the gate influences the potential landscape in the ribbon. [2]

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3. Kurt Stokbro, arXiv:1006.0082v1

TU-25



# Localized Edge Vibrations And Edge Reconstruction By Joule Heating In Graphene Nanoflakes

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## ABSTRACT

Vibrations are often treated by very simple methods compared to electrons, but the precise atomic configuration becomes important for the stability of conductors when their size approaches nanometer scales. Graphene flakes are an example of a system, where atomically precise calculations are needed.

Control of the edge topology of graphene nanostructures is critical to graphene-based electronics. A means of producing atomically smooth zigzag edges using electronic current has recently been demonstrated in experiments [1]. We develop a microscopic theory for current-induced edge reconstruction using density functional theory. Our calculations[2] provide evidence for localized vibrations at edge-interfaces involving unpassivated armchair edges. We demonstrate that these vibrations couple to the current, estimate their excitation by Joule heating, and argue that they are the likely cause of the reconstructions observed in the experiments

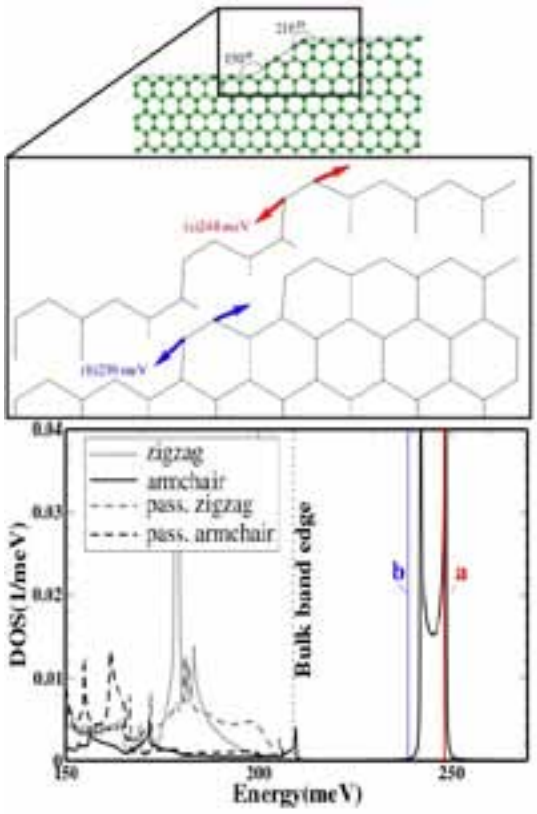


**FIGURE 1.** [Top] A graphene structure. [Middle] Two vibrational modes that accumulate energy at the edge. [Bottom] Vibratioanl density of states of the two modes compared to various edge structures.

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2. Engelund *et al.*, Physical Review Letters, **104**, 036807, 2010.

# Atom Probe Tomography of Commercial Devices

D.J. Larson[1], P.H. Clifton[1], D. Lawrence[1], D. Olson[1], T.J. Prosa[1], D.A. Reinhard[1], R. M. Ulfig[1], L. Renaud[2], J.H. Bunton[1], D. Lenz[1], and T.F. Kelly[1]

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For the nanoelectronics industries, atom probe tomography (APT) looms large for the unique capabilities it offers for device characterization. The advantages of APT for analysis of a 3D device include; a) atomic-scale three-dimensional compositional mapping of a relevant volume (>$10^6$ $nm^3$), b) high detection efficiency (>50%), and c) high sensitivity (down to single atoms) for device analysis. These advances in applications have been made possible by major developments in instrumentation [1], specimen preparation [2], and often by methods correlation with TEM [3] or SIMS [4] or both [5].

Nonetheless, the cost of ownership and the spatial fidelity of complex structures have been cited as topics with the potential to impede widespread adoption. The cost depends on ease of specimen preparation of site-specific structures and the yield of quality analyses from these specimens. We will report on progress made in making routine analyses from off-the-shelf die structures of individual transistors. FIB deprocessing and preparation is used to create quality specimens in a few hours (Figures 1 and 2). Recent advances in laser instrumentation have improved the yield of quality data from these specimens (Figures 3 and 4). Recent developments in reconstruction algorithms have demonstrated fundamental improvements for multiphase nanoelectronic device structures. This presentation will highlight these results for generating cost-effective analyses for devices. The results demonstrate that APT is maturing for product research and development, process development, and failure analysis of device structures.

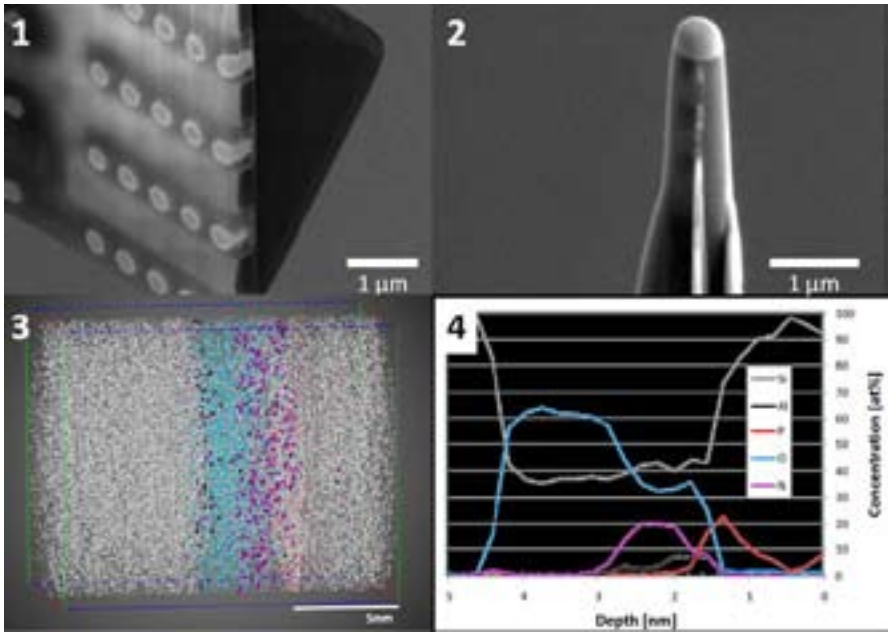


**FIGURE 1.** Device structure being deprocessed in FIB. **2.** APT specimen near final form. **3.** APT image of $SiON_x$ dielectric film. **4.** Composition profile through $SiON_x$ film of **3.**

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# Helium Ion Microscope (HIM) Characterization for Nano-Device Structures - SE Imaging and Ion Beam Luminescence Detection -

Shinichi Ogawa, Tomohiko Iijima, Shogo Awata*, Shigeru Kakinuma*, Shintaro Komatani*, and Toshihiko Kanayama
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## Abstract

This paper discusses the several imaging modes that may make HIM [1] a tool of particular value to soft materials such as low-k dielectrics with less transformation and copper interconnect buried in dielectrics, and shows possibility of detection of luminescence induced by the focused helium ion beam using the HIM for the first time.

The imaging of fine line features patterned in low-k materials is important for ULSI Cu/low-k interconnect validation of the dry etch, wet clean, e.g., in back end process steps, while conventional secondary electron microscope (SEM) imaging of low-k materials often results in changes to the low-k material line width, edge roughness, and shape by damage during the SEM electron beam irradiation. The HIM could provide low-k dielectric secondary electron (SE) image with nm order resolution, deeper focus depth, less transformation because of lower thermal energy transfer into a unit volume of the low-k material (three order magnitude) than the SEM under an appropriate operation condition [2), 3)]. The helium ion / sample interaction was also investigated. A new imaging mode, through the inter-level dielectric, of the underlying copper, was explored as well. Cu interconnect was seen through a 130 nm thick low-k dielectrics (Fig.1). It might be because the incident helium ions generated secondary electrons at the buried Cu surface and the secondary electrons of 1-2 eV energy passed through the dielectric of a few eV band gap without any energy transfer, and then the image was obtained. Helium ion channeling at the Cu surface area varied the secondary electron quantity, and it resulted in a crystal orientation contrast information of the buried Cu interconnect surface.

Luminescence induced by the focused helium ion beam was studied using the HIM for the first time for characterization of the dielectrics properties. Helium ion beam of a few pA current was irradiated onto a SiO2 film surface, and peaks in a spectrum were observed at around 281 nm, 447 nm, and 672 nm (Fig. 2) ; these positions were different from those by a conventional cathode luminescence using a SEM [4)]. In a case of the SiO2 film, intensity of the peaks increased with a number of irradiations, on the other hand, in a case of the low-k film, intensity of a broad peak at 300–480 nm decreased. This presumably is because the materials were modified or damaged during the helium ion beam irradiation. The phenomena have not been well understood so far, and further study will be presented.

We would like to acknowledge W. Thompson, L. Stern and J. Nottte of Carl Zeiss Inc. for their assistance in the Cu / low-k works, and M. Matsuura, and K. Goto of Renesas Electronics Corp. for supplying dielectric film samples.

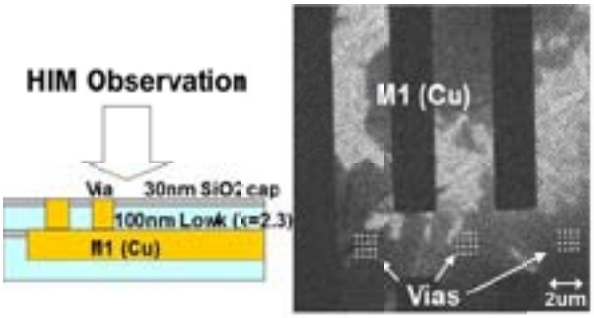


Fig.1 Side view of a Cu/low-k structure (Left) and M1 (Cu) seen through a 130 nm thick low-k dielectric material (Right)

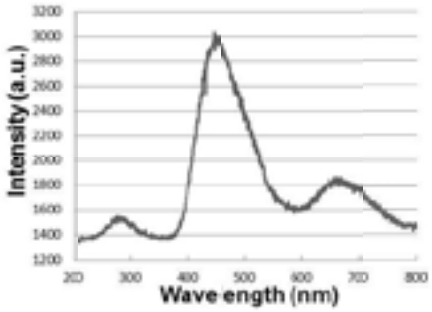


Fig.2 Spectrum of the HIM helium ion beam induced luminescence from SiO2 film

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**Key words : Helium ion microscope, Cu/low-k interconnect, Luminescence**

# Experimental Determination of Inelastic Mean Free Paths for Calculation of TEM Specimen Thickness

E. Verleysen[1,2,3], H. Bender[1], D. Schryvers[3] and W. Vandervorst[1,2]

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## ABSTRACT

The continuous scaling in semiconductor technology has made accurate characterization of transistor components more challenging. In this context, accurate determination of TEM specimen thickness is gaining importance. The aim of this work is to develop an experimental methodology to determine the electron mean free path for inelastic scattering, which in turn can be used to determine the thickness of TEM specimens by Electron Energy Loss Spectroscopy (EELS). The methodology is based on the study of cone shaped specimens which are prepared with focused ion beam (FIB) by milling ring shaped patterns with gradually decreasing diameter. The investigated specimens contain nickel silicides with different compositions on top of a Si substrate. Figure 1 shows a TEM and an HAADF-STEM image of such a cone shaped specimen with a $NiSi_2$ layer on a Si substrate. Since the intersection of the cones is circular, the width of the cones equals the maximum specimen thickness. The ratio of the specimen thickness to the electron mean free path for inelastic scattering can be determined by EELS, since this ratio is related to the total intensity of the spectrum scaled by the intensity of the zero loss peak [1]. EELS profiles are measured along the full width of the cone shaped specimens and the ratio of specimen thickness to the mean free path is determined at each point of the profile. Since for the cone shaped specimens the specimen thickness along the profile is known, the mean free path can be determined. The dependence on the experimental conditions and material composition is studied. The experimental mean free paths are compared to calculated values obtained with the formulae available in literature [1]. It is shown that the calculated values significantly underestimate the true specimen thickness for high accelerating voltages. The experimentally determined mean free paths are used to determine the thickness of TEM specimen of device structures containing nickel silicides.

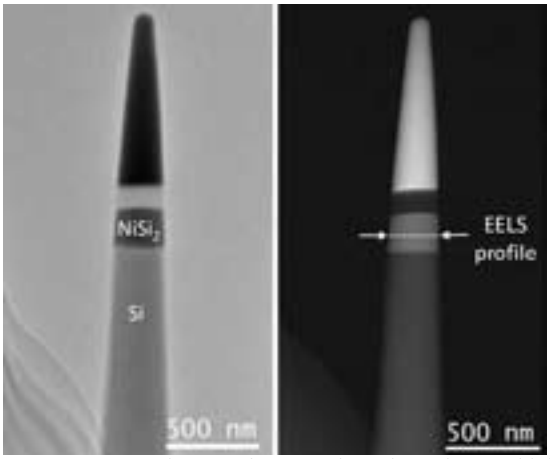


**FIGURE 1.** TEM and HAADF-STEM image of a cone shaped specimen which contains a $NiSi_2$ layer

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# Application of scanning transmission electron microscopy (STEM)-based techniques for development of novel Si/SiGe on SOI FinFET structures

James Nadeau, Chris Deeb[1], PY Hung[1], Injo Ok[1], Chris Hobbs[1],

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## ABSTRACT

This work illustrates the application of scanning transmission electron microscopy (STEM)-based techniques to enhance the process control of Si/SiGe FinFETs on SOI. A high angle annular dark field (HAADF) STEM together with nanobeam diffraction (NBD) was used to monitor the SiGe thickness and strain inside the fin and between the Si/SiGe layers. The results show that the Si/SiGe underwent asymmetric relaxation with greater strain along the length of the fin and less strain perpendicular to the fin, which agrees with previous publications (1-2). In addition, the strain gradient on both sides of the Si/SiGe interface can be measured; the degree of gradient is a measure of the compliance in each material. These results illustrate the application of STEM-related techniques to monitor complex FinFET structures. Similar applications can be used for novel 3D structures like III-V FinFETs and nanowires.

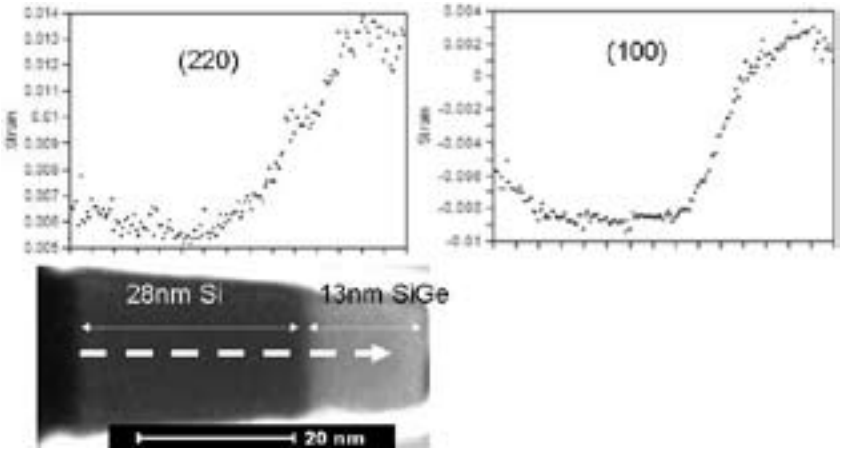


**FIGURE 2**. NBD strain profiles in the (220) and (100) Si plane taken from fin with target structure of 30 nm Si/10 nm SiGe. Strain profile was taken along the dotted white line in reference from the HAADF TEM (bottom)

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| | Morning | AM Session | PM Session | Evening |
|---|---|---|---|---|
| **Monday** May 23rd | | | Check-in at hotel<br>**15:00 – 17:00** MINATEC Facility Tour (advanced registration required) | **17:00 – 20:00** Reception and registration at MINATEC Facility |
| **Tuesday** May 24th | **07:30** Registration Attendee Check-in<br>**08:00** Breakfast | **08:45** Conference Opening<br>**09:00 Session 1** Keynote Talks<br>**10:30** Coffee Break and Poster Viewing<br>**11:00 Session 2** Technology Overview for Nanoelectronics and Metrology | **12:00 Session 3** Metrology for Beyond CMOS<br>**12:30** Lunch<br>**14:00 Session 3** (continued)<br>**15:00 Session 4** Theory, Modeling and Simulation<br>**15:30** Coffee Break and Poster Viewing<br>**16:00 Session 4** (continued)<br>**16:30 Session 5 part 1** Microscopy for Nanoelectronics<br>**17:00** Poster Session | |
| **Wednesday** May 25th | **08:00** Registration Attendee Check-in and Breakfast | **08:30 Session 5 part 2** Microscopy for Nanoelectronics<br>**10:00** Coffee Break and PosterViewing<br>**10:30 Session 5** (continued)<br>**11:00 Session 6** Novel Characterization Methods | **12:30** Lunch<br>**14:00 Session 6** (continued)<br>**15:00 Session 7** CMOS Metrology<br>**15:30** Coffee Break and Dedicated Poster Viewing Session<br>**17:00 Session 7** CMOS Metrology (continued) | **18:45** Depart MINATEC for Banquet |
| **Thursday** May 26th | **08:00** Registration Attendee Check-in and Breakfast | **08:30 Session 8** Interconnect Metrology<br>**10:00** Coffee Break and Poster Viewing<br>**10:30 Session 9** Metrology for Patterning | **12:30** Lunch<br>**14:00 Session 10** Next-Generation Defect Inspection<br>**15:00 Session 11** Characterization Needs and Methods for "More than Moore"<br>**15:30** Coffee Break and Poster Viewing<br>**16:00 Session 11** (continued)<br>**17:30** Poster Session | |

# Wednesday, May 25

Registration
**8:00 AM – 8:30 AM**

Microscopy for Nanoelectronics (part two)
Session Chair: Amal Chabli, CEA-Leti

**8:30 AM**
State-of-the-art TEM for the Semiconductor Industry
*David Cooper, CEA-Leti* ---------- P.62

**9:00 AM**
SPM-Microscopy for Nanoelectronics
*P. De Wolf, Veeco* ---------- P.63

**9:30 AM**
Atom Probe Tomography of Semiconducting Materials
Ahmed Shariq, Fraunhofer CNT, Dresden, Germany ---------- P.64

**10:00 AM**
Coffee Break and Poster Viewing

**10:30 AM**
Scanning He Ion Beam Microscopy and Metrology
*David Joy, Univ. Tenn and ORNL* ---------- P.65

Novel Characterization Methods
Session Chair: Lori Nye, Brewer Science, Inc.

**11:00 AM**
A Novel SPM System for Determining the Quantum Electrical Structure of Nanometer-scale Systems such as Graphene
*Joseph Stroscio, NIST* ---------- P.66

**11:30 AM**
Metrology for 3D Devices:  Plasma-based FIB for High-throughput Sectioning of Large Dimensions
*Noel Smith, Oregon Physics, US*---------- P.67

**12:00 PM**
Time Resolved Cathodoluminescence
*Jean-Daniel Ganiere, EPFL* ---------- P.68

**12:30 PM**
Lunch and Poster Viewing

**2:00 PM**
Quantitative High-resolution Depth Profiling of Light and Heavy Elements with Low-energy High-resolution ERDA
*Timo Sajavaara. University of Jyväskylä, Finland* ---------- P.69

**2:30 PM**
Inelastic Electron Tunneling Spectroscopy for Measuring Microscopic Bonding Structures, Impurities, and Traps
*T.P. Ma, Yale*---------- P.70

CMOS Metrology
Session Chair: Yaw Obeng, NIST

**3:00 PM**
Metrology at IMEC: a Center of Excellence Enabling Fundamental Understanding of Process and Materials Development
*Wilfried Vandervorst, IMEC*---------- P.71

**3:30 PM**
Coffee Break and Dedicated Poster Viewing Session

**5:00 PM**
Strain Analysis in Scaled Si Transistors by Simulation-Hybrid UV Raman Microscopy
*Toshihiko Kanayama, AIST*---------- P.72

**5:30 PM**
Overview of Optical Metrology of Advanced Semiconductor Materials
*Vimal Kamineni, CNSE* ---------- P.73

**6:00 PM**
Metrology Challenges for the Ultra-thin SOI
*Oleg Kononchuk, SOITEC*---------- P.74

**6:45 PM**
Depart MINATEC for Banquet

# Poster Presentation

**WE-16,** Comparison Between Spectroscopic Ellipsometry and HRTEM-VEELS Analyses of $HfO_2$-based Stacks

C. Guedj[1], C. Licitra[1], G. Auvert[2], G. Audoit[1], D. Lafond[1], E. Martinez[1], F. de la Peña[1], P. Bayle-Guillemaud[3], N. Gambacorti[1], A. Chabli[1], and F. Bertin[1]
**[1]CEA-Leti, MINATEC Campus, Grenoble, Cedex 9, France**
**[2]STMicroelectronics, Crolles, France**
**[3]CEA, INAC, Grenoble, France** P.90

**WE-17**, Development of a High Brilliance X-ray Source for Advanced Thin Film Characterization

I. Kieffer[1], P. Gergaud[1], P. Dova[2], P. Panine[2], and S. Rodrigues[2]
**[1]CEA - CEA-Leti, MINATEC Campus, Grenoble, Cedex 9, France**
**[2]Xenocs SA, Sassenage, France** P.91

**WE-18**, Synchrotron Radiation X-Ray Photoelectron Spectroscopy Applied to Advanced High-k Metal Gate Stacks

R. Boujamaa[1,2,3], O. Renault[2], E. Martinez[2], B. Detlefs[4], J. Zegenhagen[4], M. El Kazzi[5], F. Sirotti[5], S. Baudot[1], M. Gros-Jean[1], F. Bertin[2], and C. Dubourdieu[3]
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**[3]LMGP, CNRS, Grenoble, France**
**[4]European Synchrotron Radiation Facility, Grenoble, France**
**[5]Synchroctron SOLEIL, Gif-sur-Yvette, France** P.92

**WE-19**, A High Depth Resolution MEIS Analysis of Ultra Thin STO/TiN Layers on Si for DRAM MIM Capacitors

J.A. van den Berg[1], M.A. Reading[1], P.C. Zalm[1], P. Bailey[2], T.C.Q. Noakes[2], C. Adelmann[3], and H. Tielens[3]
**[1]University of Salford, Salford, UK**
**[2]STFC Daresbury Laboratory, Daresbury, UK**
**[3]IMEC, Leuven, Belgium** P.93

**WE-20**, Multi-technique Approach for the Evaluation of the Crystal Phase of Ultrathin High-k Gate Oxide Films

E. Bersch[1], J. LaRose[1], I. Wells[1], S. Consiglio[2], R.D. Clark[2], G.J. Leusink[2], R.J. Matyi[1], and A.C. Diebold[1]
**[1]College of Nanoscale Science and Engineering, University at Albany, Albany, NY**
**[2]TEL Technology Center, America, LLC, Albany, NY** P.94

**WE-21**, High Frequency Acoustics for Probing at Nanometer Scale in SOI-based Stacks

J. Groenen[1], S. Schamm-Chardon[1], L. Lamagna[2], L. Yaacoub[1], M. Fondevilla[1], A. Zwick[1], and M. Fanciulli[2,3]
**[1]CNRS,CEMES,Université de Toulouse, Toulouse, France**
**[2]Laboratorio Nazionale MDM, CNR-INFM, Agrate, Brianza (MI), Italy**
**[3]Dipartimento di Scienza dei Materiali, Università degli Studi di Milano-Bicocca, Milano, Italy** P.95

**WE-22,** SiC Resistivity Monitoring: a look at Novel Methods

E. Tsidilkovski and R.J. Hillard
**Semilab USA, Billerica, MA** P.96

# State-of-the-art semiconductor characterisation in an aberration-corrected transmission electron microscope.

D. Cooper[1], A. Béché[2], J-L. Rouvière[3], and A. Chabli[1].

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## ABSTRACT

In September 2005, CEA-LETI received the first FEI Probe Corrected Titan TEM that was delivered. In this presentation we will show how this state-of-the-art TEM has been successfully used to develop and apply new techniques in order to characterise the latest generations of nm-scale semiconductor devices.

We will critically discuss the advantages of having a probe corrector installed in our TEM and show examples of how it has been applied to diverse applications from the imaging of single dopants in quantum dots to STEM-EELS applied to high-k metal gates. In addition we will discuss how an ultra-stable modern TEM can be used to perform multiple techniques on the same TEM specimen, for example structural information by HAADF STEM, chemical mapping by STEM EELS and dopant and strain mapping by electron holography. Figure 1(a) shows a dopant map of a 40-nm gate n-MOS device with 1-nm-resolution acquired by electron holography. Figure 1(b) and (c) shows a TEM image and an in-plane strain map of a 27-nm recessed source and drain device. The strain profiles are shown in (d) and these are consistent with the strain profiles shown in (e) that were acquired from the same sample but by using Nanobeam Electron Diffraction (NBED).

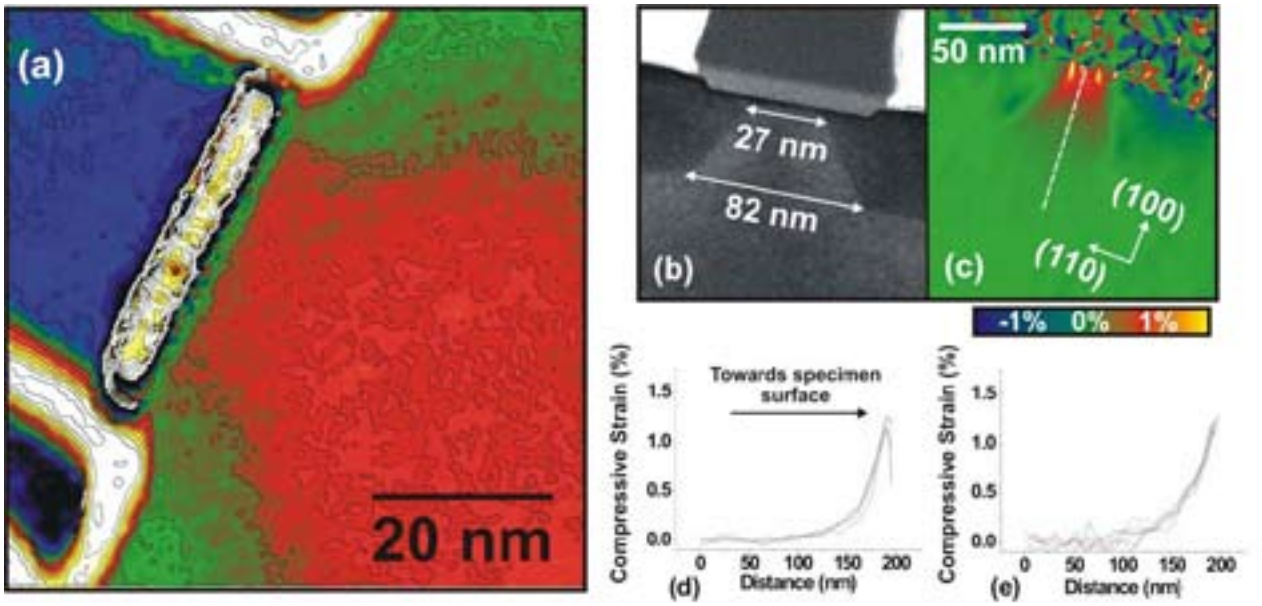


**FIGURE 1.** (a) Dopant map with 1 nm spatial resolution. (b) TEM image and (c) Strain Map of a 27 nm gate SiGe device. (d) and (e) show strain profiles that have been acquired by dark-field electron holography and NBED from the same sample.

Keywords: Transmission Electron Microscopy, Aberration Correction, Electron Holography

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5-3

# Scanning Probe Microscopy For Nanoelectronics

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## ABSTRACT

Recent focus of Scanning Probe Microscopy (SPM) developments has been to further push the technology closer to its physical limits. We will present a few aspects of these developments relevant to nanoelectronics. This includes: high resolution structural imaging at lower forces or higher throughput, quantitative nanomechanical characterization, and advances in electrical and chemical property measurements.

High resolution structural imaging at lower forces & higher throughput:

Compared to more conventional imaging modes (for example: contact mode and Tapping mode), Peak Force Tapping provides improved tip-sample force control and the possibility to operate at lower forces (down to tens of pN). This enables longer tip lifetime, improved resolution, and more accurate imaging of delicate sample structures. The Peak Force Tapping method is explained and illustrated with various examples, including deep trench structures as well as soft, fragile materials. Imaging speed is the second aspect of structural imaging addressed here. SPM throughput increase is illustrated by both automated parameter optimization techniques as well as improved scanning hardware.

Nanomechanical characterization:

The lack of quantitative measurements of mechanical properties at the nanoscale has been identified as a bottleneck for the development of new materials. To achieve reliable mechanical measurements with temporal resolution of nanoseconds and spatial resolution of nanometers, we have explored and optimized several approaches, namely, tapping harmonics, contact resonance and Peak Force Tapping. These methods now allow us to achieve highly consistent modulus, adhesion, deformation & dissipation measurements that are scalable for materials from a few MPa to tens of GPa. Examples are shown of simultaneous mapping of these mechanical properties with morphology at the nanometer scale.

Advances in electrical & chemical property characterization:

Today, a wide range of SPM-based electrical characterization methods is routinely applied in the study of nanoelectronics materials and devices. This application range has been further expanded with the availability of new methods. An example is the combination of Peak Force Tapping with Conductive (or Tunneling) AFM, allowing one to measure soft or fragile samples, previously not accessible with contact-based methods. Other improvements focus on environmental control (higher repeatability & reliability) and the elimination of the effect of the AFM laser light (eliminate light-induced artifacts).

The combination of a Raman spectrometer with SPM methods allows one to correlate chemical information with SPM-generated nanoscale information. Two approaches are rapidly gaining interest and application ranges: (i) Co-localized measurements in which SPM and Raman measurements are sequentially performed at the exact same sample location, providing correlated material information, and (ii) Tip-Enhanced Raman Scattering (TERS): By holding a specially-prepared SPM tip a few nanometer from the sample's surface, highly-localised enhanced Raman signals can be generated by increasing the strength of the electromagnetic field through surface plasmons supported at the apex of the tip. This can result in Raman maps with resolution beyond the diffraction limit, again correlated with other SPM-generated material information.

# Atom Probe Tomography of Semiconducting Materials

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## ABSTRACT

Metrology has been an important infrastructure enabling the exponential increase of device density and exponential decrease of device dimensions leading to a continued miniaturization in the microelectronics industry. Performance of such devices relies on the extreme sensitivity of the electronic characteristics to their nanoscale physical properties. Introduction of new exotic materials combined with innovative design to sustain these technological revolution present significant challenges to metrology. These high demands persuade the usage of new analytic techniques or improvements to the established methods to answer the questions regarding physical phenomenona at a scale which are approaching the resolution limits of most of the conventional metrological techniques. In the present contribution Atom probe tomography (APT) is utilized in quest for establishing a relatively new characterization technique for analyzing semiconducting materials for the quantitative compositional analysis with sub-nm resolution. In the ITRS roadmap the atom probe tomography (APT) is mentioned as one of the promising methods for the quantitative compositional analysis on the required scale. APT is based on the laser assisted field evaporation of atoms from a sharp needlelike specimen. A position sensitive detector provides the spatial information of the ion hits, while, the elemental information is obtained by measuring the time of flight of these ionized atoms. The APT analyses on dopant distribution in source/drain, contact materials, high-κ dielectrics and metal interconnects will be discussed.

Two-dimensional dopant profiling of advanced silicon transistors has become an important technique for obtaining requisite electrical characteristics. The resulting p-n-junctions exhibit high dopant concentration values very close to the surface limiting the junction depth. Knowledge of the spatial distribution of these dopants after annealing is critical for the performance of such devices. The APT study reveals temperature dependent dopant redistribution explaining respective electronic behavior. Another application of the APT is to characterize multilayer stacks such as Ti based silicides. Traditionally, SIMS has been utilized to provide information about the boron redistribution during the formation of Ti silicide. However, APT provides additional information about nano-scale $TiB_2$ precipitate formation at the TiN/TiSi interface. The achievement of the required reliability of on-chip interconnects is one of the key issues for current and future technology nodes.

The continued reduction of interconnect dimensions and the introduction of new materials and processes create new challenges for the long-term reliability of semiconductor chips. Electromigration is one of the major reliability issues in Cu interconnects therefore Al-alloyed Cu interconnects has been introduced. APT has been utilized to study out-diffusion of Al and to envisage the grain size increase after applying the requisite thermal budget. The performance of the capacitor in DRAM application is quite sensitive to the post deposition annealing. The effect of post deposition annealing on embedded thin film of a $Zr_{(1-x)}Al_xO_2$ based high-κ material is also studied using APT. The data obtained from APT is compared with other characterization techniques such as SIMS and TEM.

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5-5

# Scanning He Ion Beam Microscopy and Metrology

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## ABSTRACT

Although the CD-SEM remains a powerful tool for metrology there is little scope for further enhancements in its performance. In contrast the scanning Helium Ion Microscope (HIM) offers a comparable or better level of imaging resolution as compared to the SEM, a much superior depth of field, and strong and interpretable topographic contrast [1]. The HIM gun is a high brightness field ionization source, utilizing helium gas, with a single atom effective source size, producing emission currents of several hundred pico-amps for energies between about 20 and 40keV. The column optics of the gun and lenses is similar to those of an SEM but all the elements are electrostatic rather than electromagnetic. The ultra-short ion wavelength (~ 100 femptometers at 30keV) eliminates diffraction limiting so the focused beam can be collimated to an angle $\alpha$ of the order of 100μrads. As a result spherical aberration - which varies as $\alpha^3$ - is absent and chromatic aberration – which varies as $\alpha$ - is insignificant while the imaging depth of field, which varies as $1/\alpha$ is greatly enhanced. Consequently sub-nanometer resolution (0.7nm) can be achieved at 40keV even at working distances of 5mm or more.

The principal imaging mode of the HIM uses ion induced secondary electrons (iSE). The stopping power of ions in materials is much larger than that of electron beams of the same energy so the iSE yield is typically an order of magnitude higher than the comparable electron yield [2]. The increased stopping power also limits the range of the ion beam. In any given material the range of a He+ ion beam of some energy E(keV) is only about 1/E times the range for an electron beam of the same energy in the same material.. The iSE signal is therefore inherently richer in surface information at all beam energies than that from the SEM, and also provides strong chemical and crystallographic contrast. Topographic contrast – the variation of the iSE signal as a function of the angle of incidence $\theta$ of the incident beam to the specimen surface - is similar to but not identical with that observed in an SEM because both the magnitude and the form of the yield curve with incident angle depend on the chemistry of the sample. Modeling signal profiles for device metrology will therefore be more challenging than in the SEM case.

Helium ion beams do pose some special problems. Sample charging in the HIM is both more serious than in an SEM, and is always positive in polarity at all beam energies, with the result that the emission and collection of the iSE signal from insulators, oxides, etc is greatly affected. The best current solution is to periodically flood the specimen surface with a low energy electron beam to achieve neutralization although it is probable that operation in a "variable pressure" mode, as in the VPSEM, would be more satisfactory. The nature and severity of beam damage is also a consideration. Ions are more massive than electrons and so could cause significant damage through both sputtering and radiolysis. However sputter rates from He+ beams are only of the order of 0.1 events per ion and fall steadily with increasing beam energy. Radiolytic damage in typical resist materials with a 40keV He+ beam results in a few percent shrinkage a dose of about 10 ions/$A^2$ which is no worse than the corresponding damage from electrons. Because the iSE yield from the ion beam is both significantly larger than from an equivalent electron beam and rises with increasing incident energy the shrinkage for a given signal to noise ratio could be significantly lower than from an e-beam if ion energies in excess of 100keV were to be employed.

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KEY WORDS Helium ion microscopy, metrology, high resolution imaging

6-1

# A Novel SPM System for Determining Quantum Electronic Structure at the Nanometer-scale

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## ABSTRACT

Since the beginning of the last century new frontiers in physics have emerged when advances in instrumentation achieved lower experimental operating temperatures. Notable examples include the discovery of superconductivity and the integer and fractional quantum Hall effects. New experimental techniques are continually adapted in order to meet new experimental challenges. A case in point is scanning probe microscopy (SPM) which has seen a wealth of new measurements emerge as cryogenic SPM instruments have been developed in the last two decades. In this talk I describe the design, development and performance of a scanning probe microscopy facility operating at a base temperature of 10 mK in magnetic fields up to 15 T [1]. The microscope is cooled by a custom designed, fully ultra-high vacuum (UHV) compatible dilution refrigerator (DR) and is capable of in-situ tip and sample exchange. Sub-picometer stability at the tip-sample junction is achieved through three independent vibration isolation stages and careful design of the dilution refrigerator. The system can be connected to a network of interconnected auxiliary UHV chambers used for sample and probe tip preparation. I will describe results from current measurements which are focusing on Dirac fermions in graphene [2] and in topological insulators.



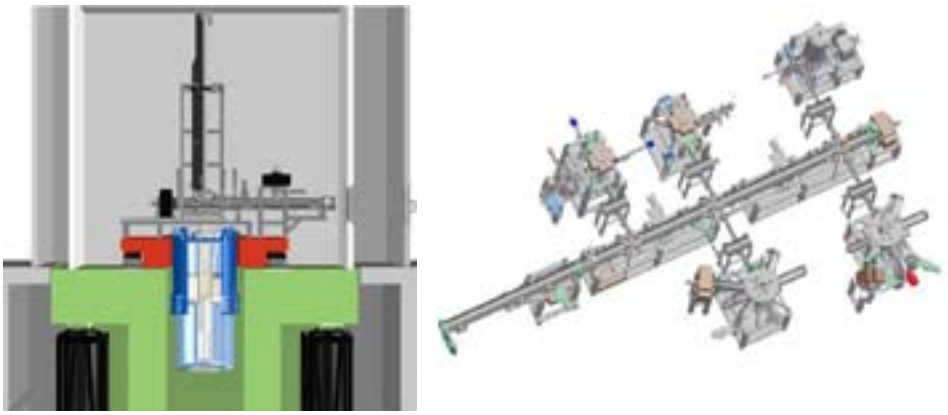

**FIGURE 1.** 3D CAD model cross section of the double shielded SPM laboratory (left), and the suite of auxiliary systems for sample and probe tip fabrication in the adjoining laboratory (right) which can be connected to the SPM system [1].

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6-2

# Metrology for 3D Devices: Plasma-FIB for High-throughput Sectioning of Large Dimensions

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## ABSTRACT

Milling speeds with a gallium focused ion beam (FIB) are often much too slow for many sample preparation and surface engineering applications. For example, cross-sectioning stacked-die semiconductor devices and prototyping micro-mechanical structures are growing applications that require milling rates that far exceed those provided by the gallium FIB.

The high brightness of the gallium liquid metal ion source (LMIS) can be fully exploited to form beam diameters of nominally 5-50nm with beam currents of 1pA-1nA. However, above 10nA the LMIS-FIB spot size tends to increase rapidly as a function of current, with the geometric aberrations of the condenser lens becoming dominant. A 100nA gallium LMIS-FIB can only be focused into a nominal spot size of 5-10um, with the column aberrations causing the beam brightness at the target to be attenuated by a factor of $10^3$, compared to the source brightness. In this high current regime, an ion source not only requires high brightness, but also a high enough angular intensity to prevent condenser lens aberrations from influencing the final beam diameter.

Here we review a focused ion beam that employs an inductively coupled plasma (ICP) ion source (Hyperion™). This ICP-FIB is able to focus a 2000nA, 30keV xenon beam into a 3um spot and provide an imaging resolution of <20nm with 1pA. The same ion source is also readily operated as a high brightness source of oxygen, hydrogen and any inert ions.

The ICP ion source operates by transferring energy to plasma electrons via a radio frequency induction field, creating a plasma state without a cathodic electrode. This method of plasma creation can create high plasma densities (>$1x10^{13}$ ion $cm^{-3}$), coupled with very low mean thermal ion energies (<0.05eV), providing the conditions required for energy normalized beam brightness values that exceed $1x10^4$ $Am^{-2}sr^{-1}V^{-1}$ and an angular intensity of several mA/sr. This high brightness can be attained with long lifetimes (>>2000 hours), stable beam current (<±0.5% drift per 30 minutes), an axial energy spread for the extracted ion beam of 5-6eV and for a broad array of ion species.

The Hyperion™ ion source is already capable of generating smaller probe diameters than the liquid metal ion source (LMIS) FIB at beam currents in excess of 20nA, and the future for this technology promises to be even brighter. This paper discusses the principles of the ICP-FIB and presents an array data from that exemplifies the capability for creating large area cross-sections of next generation 3D semiconductor devices.

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# Time Resolved Cathodoluminescence

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## ABSTRACT

Cathodoluminescence (CL) has, in comparison to photoluminescence (PL), the advantage of a much higher lateral resolution due to the small spot size of the exciting electron beam. This makes CL an unique tool for luminescence mapping and for selected investigation of nanometer-sized structures such as pyramids or nanowires. With the multimode imaging capabilities of the electron microscope we gain access to spectroscopic information within a single nano-object and correlation with the surface morphology is thus straightforward.
We present an original time-resolved cathodoluminescence set-up to study carrier dynamics with a time resolution of 10 picoseconds and a spatial resolution better than 50 nm.
To add temporal resolution to cathodoluminescence, we use an optically driven electron gun. The electron source is a gold photocathode illuminated by the third harmonic of a Ti-Saph laser (80 MHz - 100 fs - 266 nm). A streak camera (Hamamatsu 5680), mounted behind a monochromator is used as temporal detector. To illustrate the capabilities of the set-up, we will discuss briefly two examples:
- The relaxation and recombination mechanisms in a-plane GaN.
- Non-radiative recombinations on basal stacking fault in ZnO nanobelts.

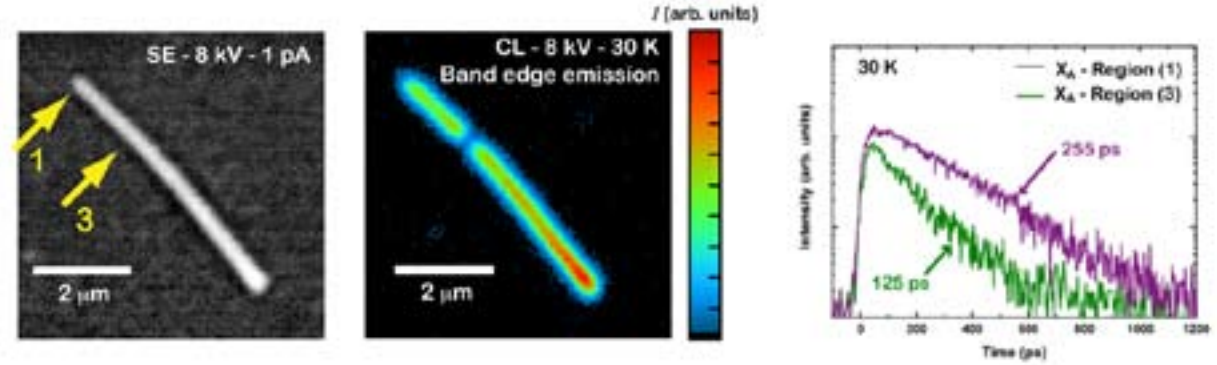


**FIGURE 1.** Intensity CL mapping and time resolved spectra on a single ZnO nanobelt

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# Quantitative High-resolution Depth Profiling Of Light And Heavy Elements With Low-energy High-resolution ERDA

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## ABSTRACT

Ion beam modification and ion beam analysis techniques have had a central role in the CMOS development over the last decades, and for instance Rutherford Backscattering Spectrometry (RBS) is still extensively used by the research institutes and industry. The main reason for this is clear: It can provide quantitative information on the elemental distributions in the sample with a modest, typically 10–20 nm, depth resolution. New materials, devices and structures have, however, sizes near atomic dimensions and here, in many cases, the performance of the traditional RBS does not meet the requirements of the community. However, the detector development in the form of a high resolution magnetic spectrometer [1] and especially a toroidal electrostatic analyzer [2] for Medium Energy Ion Scattering has brought the depth resolution of the backscattering techniques to the sub-nm range.

New possibilities open if, instead of using light ions like H and He, heavy incident ions are used and recoiled sample atoms are detected at the forward direction. With element or mass dispersive energy detector telescope Elastic Recoil Detection Analysis (ERDA) becomes a very powerful tool for materials characterization. In principle all elements, including hydrogen, can be separated and depth profiled by measuring time of flight and energy for each recoil atom in coincidence. If gas ionization detector with thin $Si_3N_4$ window [3] is used for energy detection, the good mass resolution will remain even if low energy incident ions are used. As an example in Fig. 1 TOF-E histogram and elemental depth profiles of 8.6 nm thick atomic layer deposited $Al_2O_3$ film on silicon are shown.

This paper summarizes the latest developments in the low-energy high-resolution ERDA and demonstrates the high performance of the technique via high-k, low-k, and light element shallow implantation analysis examples.

*Keywords: TOF-ERDA, high resolution depth profiling*

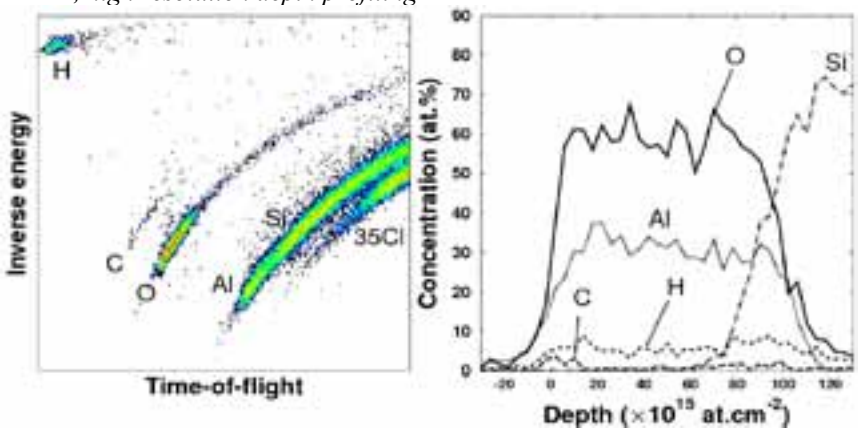


**FIGURE 1.** A raw TOF-E histogram (left) and corresponding elemental depth profiles (right) from an 8.6 nm thick ALD $A_2O_3$ film on silicon measured with 3 MeV $^{35}Cl^{1+}$ beam from 1.7 MV Pelletron accelerator. In the measurement, gas ionization detector was used as an energy detector.

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6-5



# Inelastic Electron Tunneling Spectroscopy for Measuring Microscopic Bonding Structures, Impurities, and Traps

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## ABSTRACT

As the thickness (EOT) of the gate dielectric in a CMOS transistor continues to shrink in each new generation of integrated circuits in order to meet the targeted gains in performance and circuit density, it becomes increasingly difficult for some conventional dielectric characterization tools, such as infrared spectroscopy, Raman spectroscopy, neutron scattering, and Rutherford scattering, to reveal their structural and compositional information. In contrast, the Inelastic Electron Tunneling Spectroscopy (IETS) technique, which relies on tunneling current to probe the ultra-thin gate dielectric in a metal-insulator-semiconductor (MIS) sandwich [1-5], becomes more sensitive when the tunneling current increases, which is in the direction of the CMOS scaling trend. It has been shown that a wealth of information about an MIS sample may be obtained by IETS, with excellent sensitivity and resolution [1-5]. An IETS spectrum is essentially a $d^2I/dV^2$ *vs* $V$ plot, where $V$ is the applied voltage, which equals the Fermi level separation between the two electrodes. Thus, the voltage at which a feature appears in the IETS spectrum corresponds to the characteristic energy (in eV) of a specific inelastic interaction, such as energy loss to phonons, bonding vibrations, impurity bonds, and traps, where the intensity of the interaction is also reflected in the feature size. Figure 1 shows an example of IETS spectra, measured in both polarities, for an Al/$HfO_2$/SiOx/Si MOS capacitor structure, where the data for the positive polarity (i.e., reverse bias) preferentially probes the interactions near the gate/dielectric interface while the data for the negative polarity(i.e., forward bias) preferentially probes those near the dielectric/Si interface. Traps have been shown to exhibit distinctly different IETS features [4,5], and have been measured and analyzed in numerous gate stacks. Trap energies and spatial locations can be extracted from IETS spectra [4,5]. Many examples will be shown in the presentation to illustrate the capabilities and limitations of the IETS technique.

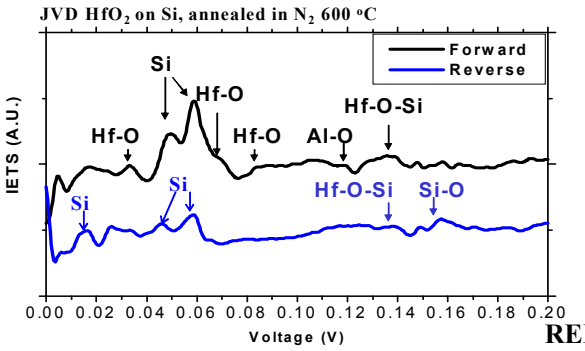


**FIGURE 1.** Reverse-bias (gate negative) IETS spectrum reveals information near Si/$HfO_2$ interface, while forward-bias (gate positive) IETS reveals information near gate/$HfO_2$ interface.

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7-1

# Metrology at IMEC: a Center of Excellence Enabling Fundamental Understanding of Process and Materials Development

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## ABSTRACT

Enabling the development of advanced nanoscale structures and technologies requires the ability to gain insight in the technological processes and material interactions on the atomic scale. The challenges "metrology suppliers" are faced with, is hence to provide a detailed characterization of structure, compositional and bonding distribution and electrical properties on the nm scale. Characteristic dimensions of the relevant structures may range from solely one-dimensional layer structures, over 2D-confined devices and even 3D-structures like FINFET's and nanowires etc.. Obviously with increasing degree of dimensional restrictions, the metrology requirements increase dramatically from "simple" depth resolution problems to metrology with high 2D-spatial resolution to the need to probe in an extremely small confined volume (3D-devices, nanowires,..) and/or at buried interfaces. Along this technological spectrum, the problems linked with resolution, sample preparation, sample localization and finite signal intensity (limited to limited statistics) increase tremendously and a focused effort on improving various metrology approaches and their fundamental understanding is required to meet future expectations. Moreover a close link to process engineers is required to optimize sample structure for high resolution, high quality analysis and to enable fundamental insight in the materials and their interations.

A number of cases will be presented illustrating this concept with an overview of the recent evolution in 1D, 2D, and 3D analysis at Imec. Topics to be discussed will include : optical probes (PMOR) to reconstruct carrier profiles from non-destructive, localised (in-line) measurements; EXLE-SIMS targeting ultra high resolution depth profiles such as the analysis of surface passivation of Ge-materials with monolayers of Si, quantitative interfacial dopant profiles; SSRM to identify size-effects in dopant activation in nanowires, the connectivity of CNT's and 3D-Dopant profiles in FINFETS; backside preparation techniques to probe high k- metal gate interactions with XPS and C-AFM; Atomprobe for FINFET doping metrology and ultra high resolution depth profiles; EDX for void detection in narrow interconnect lines; micro-sheet resistance measurements for III-V carrier depth profiling; ...

# Strain Analysis in Scaled Si Transistors by Simulation-Hybrid UV Raman Microscopy

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## ABSTRACT

Recent aggressive scaling of transistors imposes severe demand on material characterization. Material properties must be measured with high spatial resolution in complicated device structures composed of multiple materials. A typical example is mechanical strain in the channel region. It is preferable to measure the local strain quantitatively in a nondestructive manner after completion of transistor structure. To meet this demand, we are developing a hybrid technique of simulation and polarized UV Raman measurements. [1]

In this technique, the strain distribution in a transistor is estimated by a simulator, for which the Raman measurement plays two essential roles, calibration and verification. Strain simulation needs mechanical properties of constituent materials such as elastic constants and internal stress but these values are usually difficult to measure. Thus, these parameter values in strain simulation are calibrated by comparing the calculated Raman shift mapping with actual measurement results in a μm-scale transistor structure. The polarization dependence of Raman spectra enables detailed quantitative comparison.[2,3] Finally, the simulated strain distribution in actual scaled transistor is verified by the polarized Raman measurement. The fact that the light polarized normal to the gate side wall can penetrate through the side wall spacer enables this comparison.[4] Figure 1 shows that after the calibration the simulation reproduces the measured dependence of Raman shift on S/D width for pMOSFETs of 45-nm gate length.

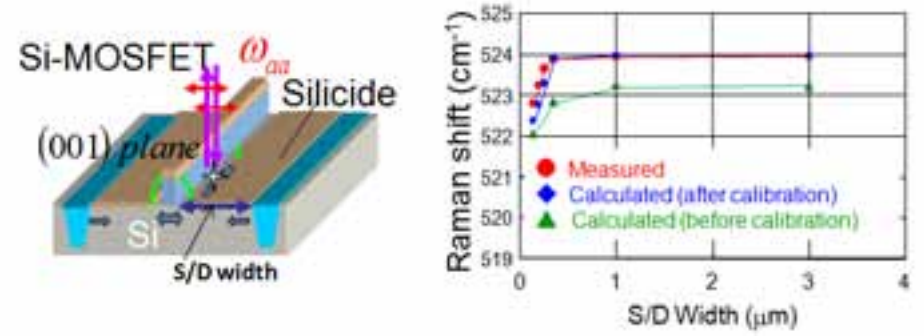


**FIGURE 1.** Simulation-hybrid Raman measurement of mechanical strain in p-MOSFET with 45-nm gate length. Dependence of Raman shift on S/D width is calculated and compared with actual measurements for vertical illumination/observation conditions. It is verified that the compressive strain due to stress liner decreases when the S/D width is reduced.

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7-3

# Overview of Optical Metrology of Advanced Semiconductor Materials

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## ABSTRACT

As novel materials are being investigated for semiconductor applications, it becomes imperative to advance the characterization techniques to meet the metrology requirements for these next generation materials. Spectroscopic ellipsometry (SE) is a rapid optical metrology technique capable of characterizing advanced materials. In this overview, SE was utilized to measure various other properties beyond conventional parameters (optical constants and thickness). In the case of very thin metal films, the correlation between thickness dependent optical properties and the free electron relaxation time is traced to the change in grain size. Low-κ dielectric materials were characterized to extract the chemical (molecular bond vibration and carbon content), porous (pore volume fraction and pore size), and mechanical (coefficient of thermal expansion and Young's modulus) properties. SE was also employed to measure the bandgap of high-κ dielectric thin films and the glass transition temperature of EUV photoresists and under layers. The percentage of curing in adhesive bonding layers used in 3D interconnects and the stress in strain engineered III-nitride thin films were measured via infrared SE. SE is also an excellent method of measuring thin Silicon on Insulator materials. The shift in transition energies of the critical points in extremely thin silicon-on-insulators (ETSOI) were measured using reciprocal analysis of the optical response. This talk will also describe other optical methods that are complementary to SE. Photoreflectance can measure the energy of the E1 critical point and thus strain in Si and SiGe and changes in band structure while low temperature photoluminescence can measure changes in the band gap of nanomaterials and identify the electron-hole (e-h) phase due to 2D quantum confinement.

**Keywords:** Ellipsometry, photoluminescence, photoreflectance.

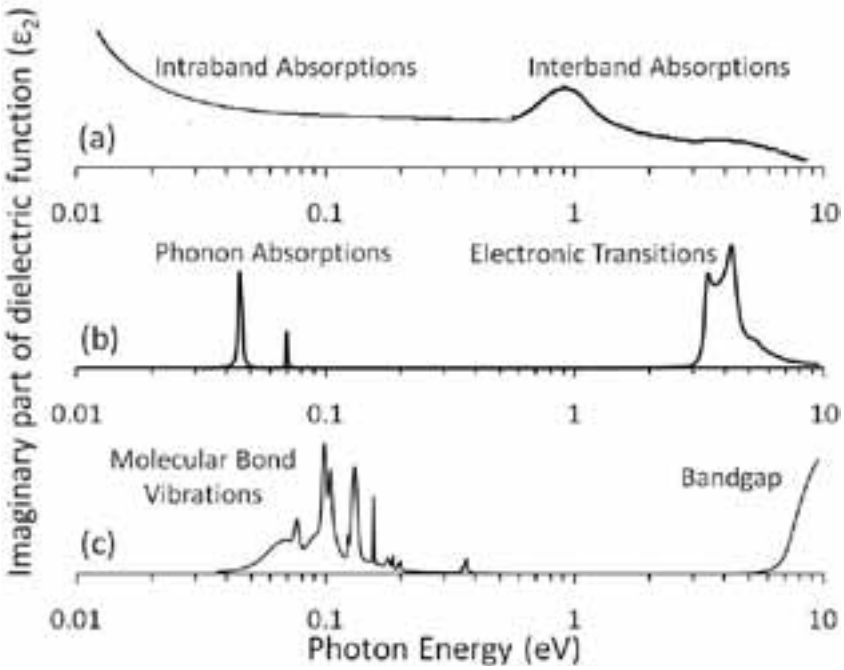


**FIGURE 1.** Imaginary part of dielectric function ($\varepsilon_2$) of (a) metals, (b) semiconductors and (c) dielectrics

# Metrology Challenges for the Ultra-thin SOI

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## ABSTRACT

Silicon on insulator (SOI) wafers have become today one of the standard substrate choices for high-end CMOS applications. Current quality of SOI wafers is approaching to the quality of high end bulk Si products. The manufacturing process requires monitoring of tens of parameters, both on-line during wafer processing and off-line on the finished product. Among those parameters the most important require SOI specific metrology. Recent development of technology based on planar fully depleted MOSFET architecture drives thickness of Si and buried oxide layer (BOX) of SOI wafers in sub 10nm range [1]. This new transistor design reduces significantly Vt variation due to random doping fluctuation but imposes additional tight requirements on Si thickness uniformity. It becomes the critical parameter for fully depleted MOSFETs and has to be controlled in the wide range of spatial frequencies, covering frequencies from wafer scale to tens of nanometers. Traditional spectroscopic ellipsometry has to be expanded into submicron lateral resolution domain and complemented by surface roughness techniques. Difficulties of correlation and calibration of multiple techniques will be highlighted.

Big challenge of particle measurements on SOI wafers is the inspection limitations of conventional LPD measurement tools [2]. Introduction of SP2 scanner allowed significantly decrease threshold of LPD inspection on SOI wafers together with quantitative measurement of surface roughness. Limitations and possible extensions of this technique for thin (10 – 20nm) SOI layers will be discussed.

Another specific feature of SOI wafers is reduced tolerance to metal contamination and structural defects in top Si layer as compared with standard bulk Si technology. Oxygen precipitates or agglomerations of Si vacancies with size superior to the top Si layer thickness will result in killer defects due to underetching of the BOX during wet cleaning steps used in CMOS processing. Interesting application of well known HF etching technique became possible due to very high quality of modern SOI process. HF defect densities in standard SOI wafers typically fall below 0.05 defects per $cm^2$. It allows mapping of the HF defects by LPD inspection tools. Combination of these techniques with non-preferential chemical thinning of top Si layer is a powerful method which allows quantitative measurements of density and size of oxygen precipitates in incoming Si wafers used as donor wafers for SOI production. Detection limits of < 10nm in precipitate size and < $10^5 cm^{-3}$ in precipitate density are demonstrated, which are superior to those of conventional techniques, such as LST. It will be shown that this technique also is very sensitive to traces of metal contamination in the $10^8 cm^{-2}$ levels.

Quality of BOX/Si interface is a result of BOX formation method as well as SOI manufacturing steps. Various techniques assessing quality of the interfacial layer can be used for statistical process control. One of the techniques is electrical characterization of the interface using pseudo-MOS method. Examples of sensitivity of this technique to metal contamination and interface defectivity will be shown. Overview of different variations of the technique will be presented and challenges associated with decreasing of the thickness of the layers are discussed.

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# Determination of SiGe Optical Properties for Accurate Ellipsometry Measurement

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## ABSTRACT

For mobility enhancement through local stress SiGe films are very attractive candidates for the 28nm CMOS technology node. In a production environment the in-line measurements of the SiGe thickness and Ge content become key parameters. Although techniques such as XRD and SIMS are traditionally adopted as reference technique for Ge thickness and concentration there is a clear need for rapid and non-destructive inline measurements such as spectroscopic ellipsometry.

One of the key requirements for ellipsometry measurement is a very accurate determination of the optical properties of SiGe[1] versus Ge%. As it stands, the experimental determination of the n & k dispersions curves is inherently affected by experimental errors that can spoil the correctness of the measurements. The SiGe dispersion curves are indeed usually determined independently for each percentage of Ge. This kind of approach can lead to discrepancies between the curves for different Ge percentage. We present in this article an original technique that recalculate the experimental values by ensuring that for each wavelength the relation between n and k versus Ge% is regular and free of scattered points (Figure 1). The resulting set of n & k functions, as defined in the bidimentional domain of the wavelength and the Ge%, are smooth and free of irregularities. This is clearly better adapted for a non-linear search of the optimal fit solution of ellipsometric data. In this paper we show that an improvement in SiGe thickness and Ge% measurement can be achieved by the implementation of this technique both for monitor and production wafers.

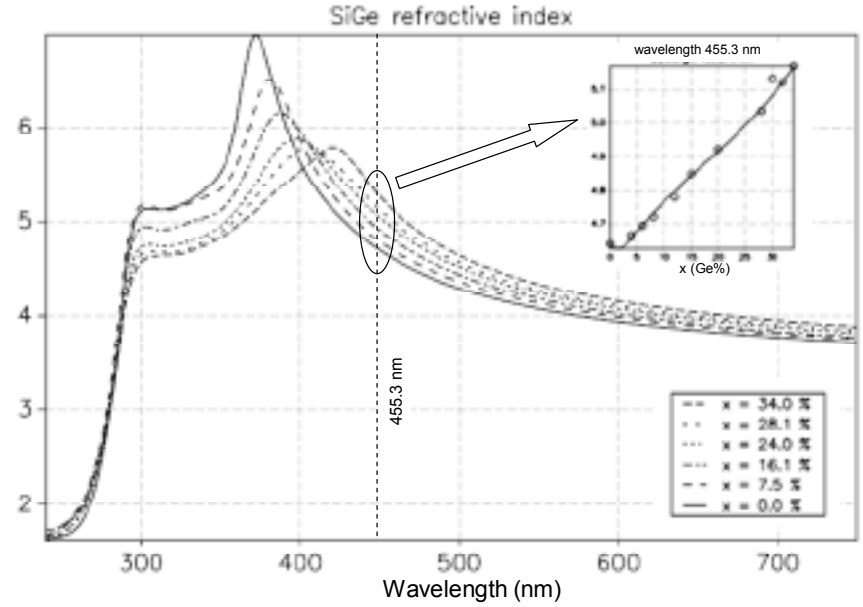


**FIGURE 1.** SiGe refractive index versus wavelength for different Ge%. In the insert n vs Ge% (λ=455.3 nm).

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Keywords: ellipsometry, epitaxy, SiGe

# High Resolution Multiwavelength μ-Raman Spectroscopy for Nanoelectronic Material Characterization Applications

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## ABSTRACT

Micro-Raman spectroscopy is a non-destructive, in-line characterization technique that is desirable for semiconductor manufacturing due to its sub-micron spatial resolution, and short measurement time, requiring no sample preparation [1]. With its high spectral resolution, micro-Raman spectroscopy is especially useful for characterizing and monitoring advanced materials used in nanoelectronics applications. Spectra peak intensity, shift, full width at half maximum (FWHM) and shape asymmetry provide insight into lattice stress/strain, dopant concentration and activation, lattice defects, and several other parameters critical to semiconductor performance.

A polychromator-based, high resolution, multi-wavelength Raman spectroscopy system (WaferMasters MRS-300) [2] was used as an in-line stress/strain and crystallinity monitoring system for Si, epitaxial $Si_{1-x}Ge_x$/Si and implanted Si before and after annealing. Three major spectral lines at 457.9, 488.0 and 514.5 nm from a multi-wavelength Ar ion laser are used as the excitation source. Multi-wavelength excitation permits virtual depth profiling of various material parameters. The system has three thermoelectrically-cooled charge-coupled device (CCD) cameras, one for each excitation wavelength. Raman peaks from three different excitation wavelengths can be acquired without any disruption in the optical path (i.e., without scanning the monochromator or switching the excitation laser), making the system particularly stable.

Figure 1 shows the schematic illustration of MRS-300 system and Raman signals from blanket pads of five $Si_{1-x}Ge_x$/Si(100) device wafers with different Ge content under 457.9 nm excitation. All five $Si_{1-x}Ge_x$/Si (100) wafers exhibited two spectral peaks corresponding to bulk Si around 520.3 $cm^{-1}$ and Si-Si peaks from $Si_{1-x}Ge_x$, in the range of ~500-515 $cm^{-1}$, depending on Ge content. As the Ge content increases, the Si-Si peak from $Si_{1-x}Ge_x$ shifts to the lower wavenumber. This shift and peak shape can be used to periodically monitor the stress as the manufacturing process proceeds.

**Keywords:** Raman Spectroscopy, Stress, Strain, SiGe, Ge Content, Depth Profiling

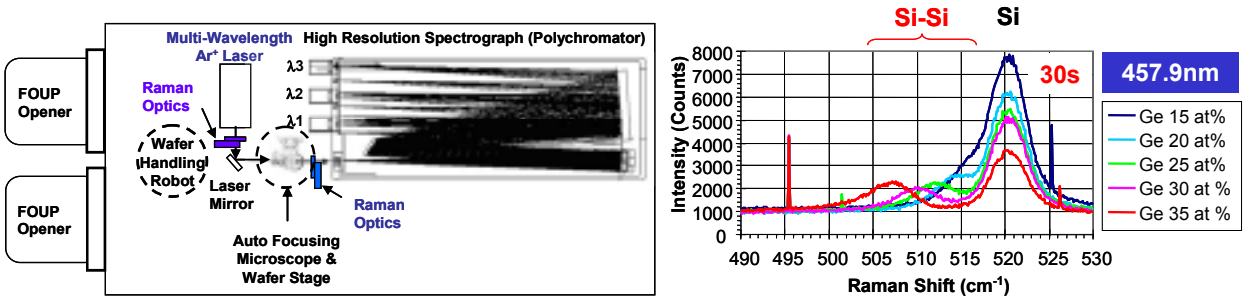


**FIGURE 1.** Schematic illustration of MRS-300 system and Raman signals from blanket pads of five $Si_{1-x}Ge_x$/Si(100) wafers.

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# Current Voltage Characteristics through Grains and Grain Boundaries Of $HfSi_xO_y$ Thin Films Measured By Tunneling Atomic Force Microscopy

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## ABSTRACT

High-k dielectric films are of interest as alternative gate insulators for metal-oxide semiconductor devices. In our previous study, surface morphology and leakage current distribution of high-k dielectric films ($HfSi_xO_y$ and $ZrO_2$) have been simultaneously investigated at the nanoscale by tunneling atomic force microscopy (TUNA) [1]. It was found that the dominant leakage current paths of high-k dielectric films were located at the grain boundaries. Probable reasons for the larger leakage current through grain boundaries are different current conduction mechanisms for grains and grain boundaries or the minor thickness of grain boundaries compared to that of grains. Figure 1 shows the typical topography and corresponding current map of an 8.0 nm thick $HfSi_xO_y$ film measured by TUNA. Crystalline grains can clearly be observed in the topography map. In the TUNA current map, the conductive structures (dark color), corresponding to the grain boundaries in the topography map, are clearly visible which indicate larger currents. Figure 2 shows local I-V curves for different grains and grain boundaries of the $HfSi_xO_y$ film. The difference between I-V curves through grains and grain boundaries can clearly be observed. The distribution of the local I-V curves through grains has a wide spread, while that through grain boundaries shows two groups (i.e., group A and B) with rather narrow spread. The reason for the two I-V groups for the grain boundaries will be discussed. Most important, leakage currents through grain boundaries are found to increase above the noise level at lower voltages for group A. The I-V curves will be evaluated by conventional and advanced evaluation methods (e.g., Fowler-Nordheim, Poole-Frenkel and α-V plot [2]) and discussed in detail to identify the physical reasons for the differences. In order to analyze the relationship between local I-V curves and the thickness of grains and grain boundaries transmission electron microscopy characterization of the films will be performed.

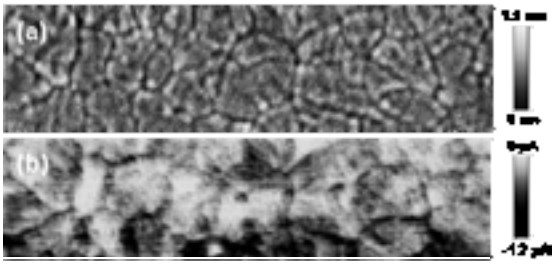


**FIGURE 1.** (a) TUNA topography map and (b) corresponding TUNA current map of the $HfSi_xO_y$ film. Scan size: 2x1 $\mu m^2$, applied bias voltage: -9.3 V.

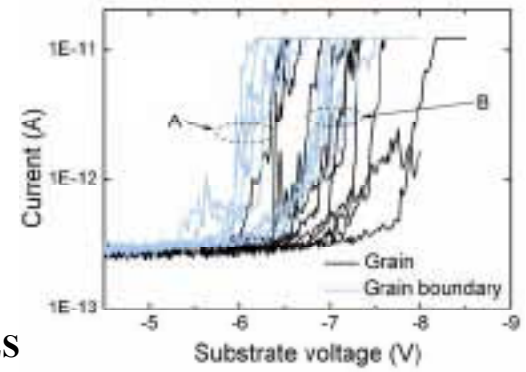


**FIGURE 2.** Local I-V curves through grains and grain boundaries of the $HfSi_xO_y$ film measured by TUNA.

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Keyword: TUNA, high-k, grain and grain boundary

# A New Type Of Detector For Dynamic XPS Measurements

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## ABSTRACT

**Abstract:** Real time observation of fast processes occurring in a time window of a few milliseconds to a few minutes have been always difficult to observe by x-ray excited photoemission (XPS) studies under laboratory conditions. However the demand to understand the chemistry of surface processes e.g. during heating processes, electro migration and diffusion is of high relevance in various research fields.

In this contribution we will report on first results of a new multi-anode detector concept with 128 individual anodes, preamplifiers and counters. It has the capability to allow of quantitative XPS studies on fast time scales with good signal to noise ratio excited with a monochromated Al Kα laboratory source. The detector can be operated in snapshot XPS mode. This mode allows recording an energy window in the spectrum versus time with high repetition-rates and good energy resolution, e.g. a 15 eV detectable energy window with an approximate energy resolution of 0.5 eV.

As an early application we report on results of removing an in-situ grown $SiO_2$ layer on a Si substrate. The measurement was made during a sample temperature ramp from room temperature to 900° Celsius within a time frame of one hour. The target of the experiment was to analyze the time window in which the oxide was removed.

Snapshot spectra have been recorded with an acquisition time of 0.5 seconds per spectrum to follow the evolution of the subcomponents of Si 2p from $Si^{4+}$ to $Si^{0}$ during the heating process of the Silicon, see Fig.1. The snapshot series with >5000 spectra shows the evolution of the peak versus time. The complete removal of the oxide occurred at a very small temperature window around 850°C. A closer look into the data revealed that the removal of the oxide from the silicon took place in about 2.5 minutes. Within this transition time 300 spectra have been recorded.

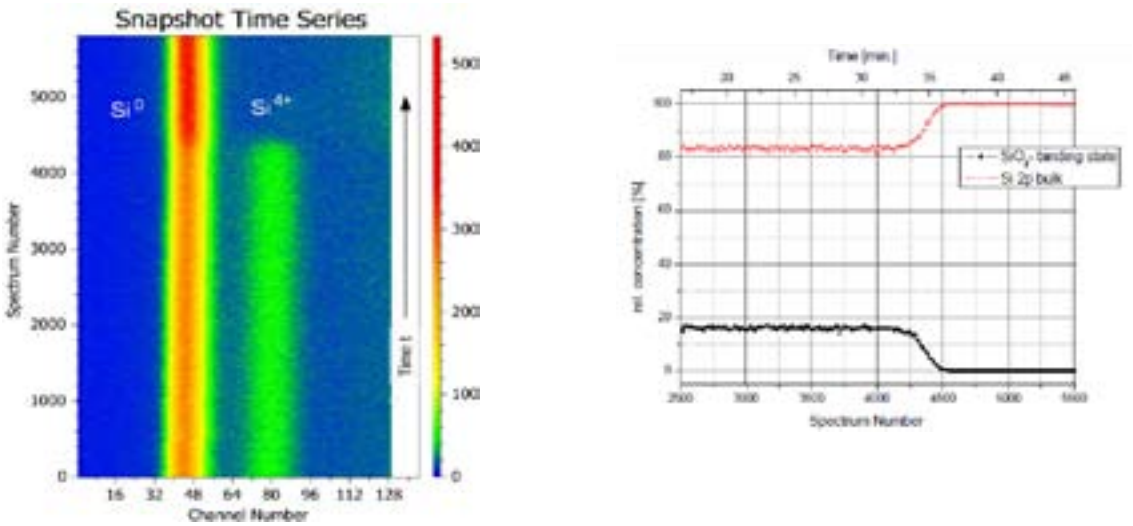


**FIGURE 1.** a) XPS snapshot series of about 6000 spectra recorded with a 128 channel detector on the Si 2p peak with a time span of one hour. Sample: $SiO_2$/Si. b) Relative concentration of the $SiO_2$-binding state and Si 2p bulk component vs. time.

# Electrical Characterization of Resistive Switching Memories

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## ABSTRACT

Metal oxide based resistive switching memories, also known as resistive-RAM (RRAM), have shown promising characteristics for next-generation nonvolatile memory and reconfigurable logic applications. These devices can be electrically switched between a low-resistance-state (LRS) and high-resistance-state (HRS) over many cycles. Fig. 1(a) illustrates the resistive switching terminologies and the operation parameters. A typical unipolar switching I-V curve is shown in Fig. 1(b) where key switching parameters are defined. Various metal oxides have demonstrated resistive switching properties. However, the measured switching parameters vary in a wide range, which calls for more consistent and uniform characterization methodologies. Although standard nonvolatile memory measurement methods are applicable to RRAMs, some unique features of RRAMs require carefully designed characterization approaches and not all the commonly used memory criteria can be simply extended to RRAMs. As an example, Fig. 1(c) shows a temperature-accelerated retention measurement of RRAMs [1]. A barrier-controlled retention model derived from the analogy to other nonvolatile memories (e.g., Flash memory) enables accurate retention measurement; however, the physical interpretation of the retention parameters is still debatable. Variability presents a major challenge for not only RRAM performance but also the characterization methodology. Phenomenological failure analysis has shown some abnormal failure modes during RRAM cycling, which needs to be addressed with rigorous testing algorithms [2]. Realistic RRAM evaluation and benchmark based on electrical characterization also needs to consider tradeoffs among key switching parameters.

This paper will discuss characterization methodologies for RRAMs in the following four categories: (1) standard measurement methods and RRAM parameters including switching voltage/current, speed, cycling endurance, retention, *etc*.; (2) characterization methods to explore the transport and switching mechanisms; (3) unique issues of RRAMs including switching polarity effects, switching control, reliability, variability, *etc*.; (4) tradeoffs among key switching parameters and failure modes important for RRAM evaluation and benchmark. Fig. 1(d) illustrates the four levels of RRAM characterization methodologies discussed in this paper.

**Keywords**: Resistive switching, RRAM, memory characterization, failure modes, variability

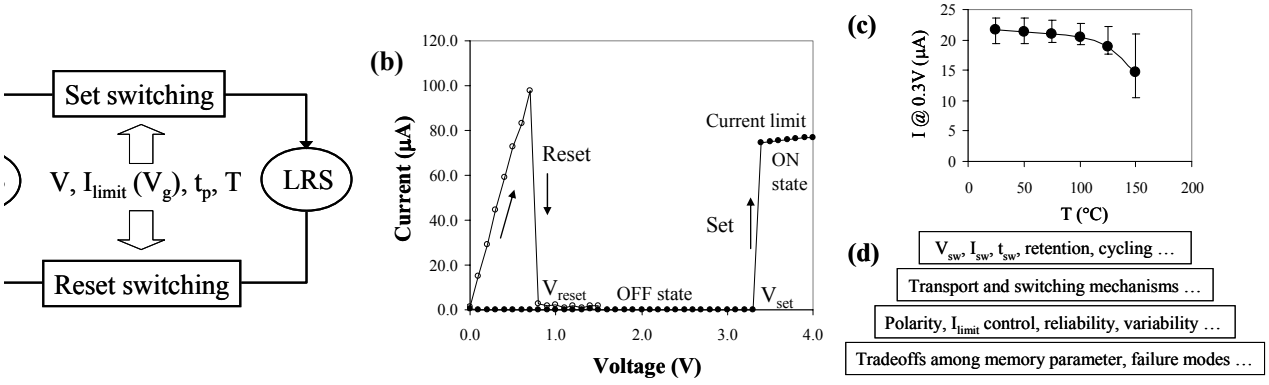


**FIGURE 1.** (a) Controllable operation parameters for resistive switching; (b) a typical unipolar resistive switching I-V curve; (c) temperature-accelerated retention measurement; (d) four levels of electrical characterization discussed in this paper.

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# Ellipsometric Porosimetry: from Thin Films to Patterned Structures Characterization

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## ABSTRACT

For the sub-32 nm nodes, porous SiCOH dielectrics (p-SiCOH) are integrated using dual damascene patterning by etching trenches and vias directly into the porous material. Since p-SiCOH dielectrics exhibit a poor resistance to plasma treatments one challenge is to control the process conditions to minimize the plasma-induced damage. Until now Ellipsometric Porosimetry (EP) on blanket test wafers has been used to investigate the impact of plasma treatments on porous materials and demonstrated possible surface densification and hydrophobicity loss after the process steps [1]. Unfortunately the properties of vertically patterned structures, i.e. real circuits, may differ from the bottom of the trench region. Few studies have been performed on patterned structures to determine the sidewall modification while this information is critical for device performance. In this study quantitative measurements of vertically patterned porous materials will be demonstrated using the recently developed Scatterometric Porosimetry (SP) technique [2]. It consists in coupling EP measurements of periodic structures with a scatterometric analysis (Fig. 1). A comparison between EP and SP will be detailed on different plasma-treated samples showing that material modifications strongly depend on the sample geometry.

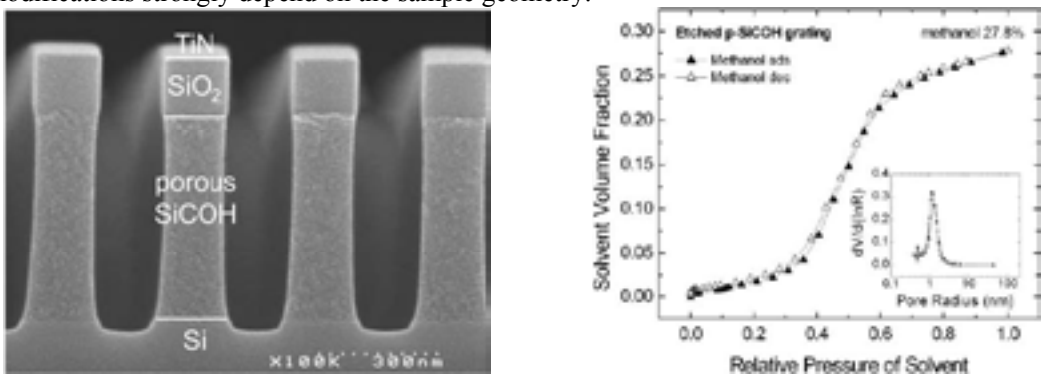


**FIGURE 1.** Left: Test structure for Scatterometric Porosimetry with critical dimension CD=180 nm and pitch=340 nm. Right: methanol isotherms and pore size distribution measured on an etched p-SiCOH grating.

**Keywords**: ellipsometric porosimetry, porous ultra low-k dielectrics, scatterometry

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# Reliable In-Line Metrology Based On The Combination Of X-Ray Reflectometry And Spectroscopic Ellipsometry

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## ABSTRACT

The demand for accurate and highly reliable in-fab characterization of thin layers included in advanced CMOS and MEMS stacks has placed stringent requests on in-line optical metrology methodology and protocols. This paper will report on the interest of a lab-to-fab characterization protocol based on the combination of X-ray reflectometry (XRR), variable-angle spectroscopic ellispometry (VASE) and in-line micro-spot ellipsometry (μ-SE). First, X-ray reflectometry (XRR) provides unambiguous thickness information of the thin layers of interest. Then, VASE analysis is run based on XRR-deduced thickness, which permits to determine the dispersion laws of the materials of interest will low correlation concern when compared with SE-only analysis. Finally, these dispersion laws are implemented on μ-SE tool so as to run automated measurements on product wafers. Based on numerous examples (semiconductors, dielectrics, transparent conductive oxides, anisotropic materials), we will evaluate the performances and limitations of this characterization protocol. We will demonstrate that, as far as key parameters (e.g. interfacial and top oxide layers, airborne molecular contamination, surface and interfacial roughnesses, etc) are taken into account, systematic combination of XRR and SE permits to accelerate the development of new processes and to increase the reliability of in-fab process monitoring.

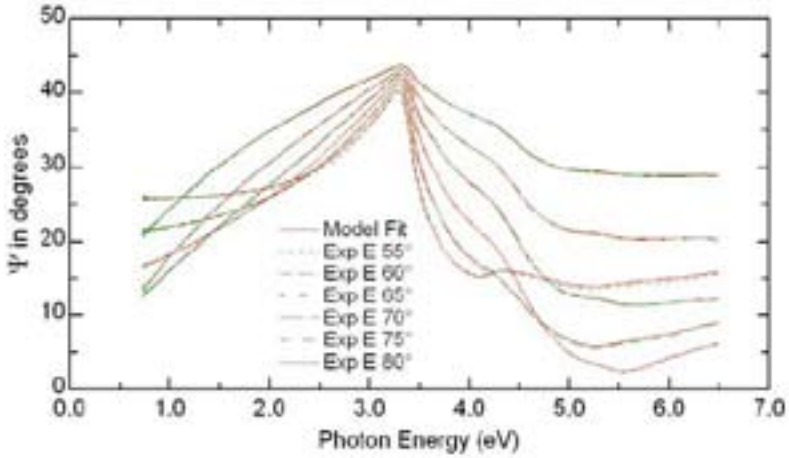


**FIGURE 1.** VASE raw data and best-model calculation based on isotropic assumption relating to a sample made of 63nm-thick hydrogenated amorphous carbon layer grown by PECVD at 400°C on a silicon wafer. Though the isotropic model appears to properly depict the raw data, it leads to a thickness error in the 10% range. Appropriate lab-to-fab protocol, based on XRR-deduced thickness revealed the slight uniaxial anisotropy of the a-C:H layer and improved the fitting quality.

# Observation of Work Function, Metallicity, Band Bending, Dipole by EUPS for Characterizing High-k/Metal Interface

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## ABSTRACT

For characterizing high-k/metal gate interfaces, EUPS is being employed to evaluate work function and metallicity of various material surfaces, band-bending of Si with high-k films, and dipole at the interface.

EUPS is a novel photoelectron spectroscopy (refs.1,2), in which a sample is excited with a 4.86nm (255eV) 3-ns pulse EUV light emitted from a laser-produced plasma and an electron spectrum is analyzed with a time-of-flight (TOF) analyzer. EUPS gives information of the topmost atoms because the escape depth of photo-electrons excited by the 4.86nm light is 0.5nm. EUPS can evaluate band-bending because the peak density of the excitation light on sample is extremely high so that bended electronic bands in semiconductors can be flattened. Secondary electron spectra, which give a vacuum level of the material surface, are obtained very quickly owing to the TOF analyzer.

Metal gate is introduced in nano-electronic devices to avoid depletion effect in a poly-Si gate electrode, but nobody knew metallicity of nm films. We are evaluating metallicity of the material surface by the 2ndary electron intensity. Figure 1 shows 2ndary electron spectra for TaN films deposited on 100nm-W on Si wafer, which indicates that a TaN film thicker than 2nm has large enough metallicity. Figure 1 also indicates that work function is lower for a thinner film. These two indications have been confirmed by C-V measurements.

Figure 2, the kinetic energy of Hf $4f_{7/2}$ photo-electrons as a function of the signal intensity, is an example of the band-bending observation, showing that band bending of 0.2eV is independent on thickness of a TiN film on $HfO_2$.

Having the depth resolution of 0.5nm or below of photo-electrons in EUPS and 2ndary electrons, we can also characterize buried interfaces by ion-sputtering covering layers. We confirmed that our sputtering has the depth resolution well better than 1-nm. We plan to directly observe dipoles at various interfaces of nm thick layers.

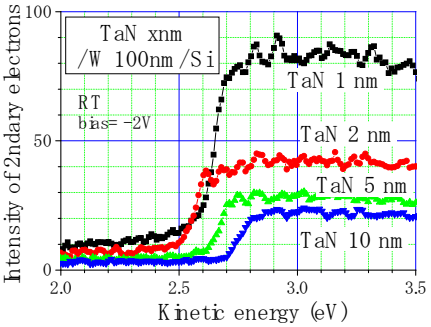


**FIGURE 1.** Secondary Electron Spectra for TaN xnm/W/Si.

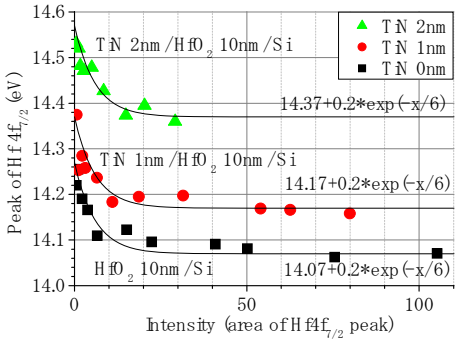


**FIGURE 2.** Band Bending of TiN xnm/$HfO_2$ 10nm/Si.

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**Key words:** EUPS, Work Function, Metallicity, Band Bending

# High-*k* Thin Film Thickness Variation Under Post-Deposition Annealing Investigated By X-ray Reflectivity and X-ray Photoelectron Spectroscopy

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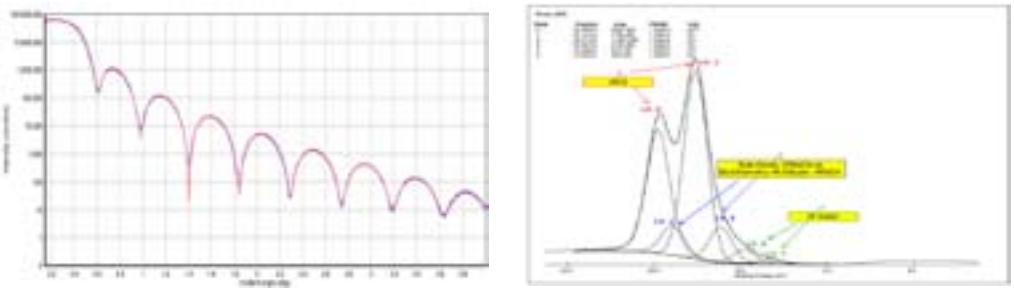
## ABSTRACT

The film structure changes and interface stability induced by thermal treatment were significant issues when $HfO_2$ films were used to replace SiO2 for the gate dielectric [1-2]. In this work, different material models were studied to fit GIXRR measurements for the 10 nm HfO2 film, which consists of a top layer $HfO_2$ (by atomic layer deposition, ALD), a native $SiO_2$ as an interfacial layer, and a silicon substrate. At first, a four-layer material model of $HfO_2$(low-density)/$HfO_2$/$SiO_2$/Si-sub was constructed to improve X-ray Reflectivity (XRR) fitting by using genetic algorithm (GA) analysis, as shown in Figure 1(a), for the as-deposited (ASD) $HfO_2$ samples.. Moreover, $HfO_2$ films were also annealed using furnaces at 550 C, 850 C and 1000 C under Ar atmosphere, respectively. X-ray photoelectron Spectroscopy (XPS) was used for investigating inter-diffusion phenomenon of oxides as shown in Figure 1(b), in order to confirm the structure changes and interface thermal stability of the HfO2 films for building accurate material model in XRR fitting analysis. The curve fittings for individual element at several annealing temperatures have showed the composition changes of oxides, which attributes to formation of Hf-silicate induced by layer inter-diffusions. According to the XPS chemical analysis, a better layer structure for material model can be constructed for the XRR fitting analysis, which gives more accurate HfO2 film thicknesses.

Keywords : Thickness, HfO2, SiO2, XRR, XPS



(a) (b)

**FIGURE 1.** (a) XRR fitting spectrum with a four-layer model, and
(b) XPS composition analysis (surface scan) of as-deposited HfO2 10 nm films.

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# Wafer Bonding Interface X-Ray Characterization

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## ABSTRACT

The wafer direct bonding technique has found many applications ranging from mass production of SOI substrates to 3D and heterogeneous integration. Understanding the effects of the bonding process parameters and the physical and chemical mechanisms operating during bonding requires the possibility to study the structure of the bonding interface. This is a challenging task as the vertical extension of the interface is in the nanometer range while it is often buried under bulk materials of millimeter thickness, sidelining most surface sensitive probes. We will show that X-ray interfacial reflection (and scattering) using high energy synchrotron radiation meets the seemingly contradictory requirements of a high penetration to access the interface and a high sensitivity to the ultra-thin interfacial layers[1]. Examples will be given of interface studies from silicon oxide to silicon oxide direct bonding[2] and metal/metal bonding[3]. In the case of silicon oxide to oxide hydrophilic bonding, we will show that the technique allows a detailed balance of the different species present at the interface, allowing a detailed mechanism for interface closure to be given. Adhesion energy evolution, behavior upon annealing and strain and defect formation can then be explained. The inversion of scattering data will be discussed.

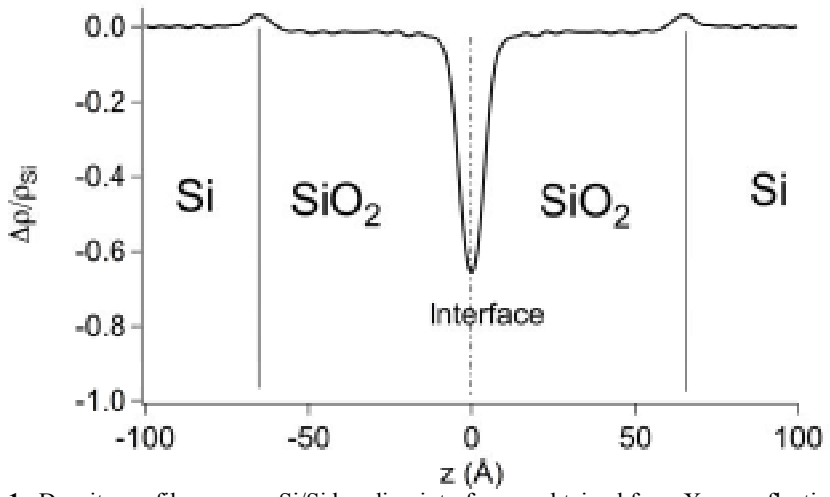


**FIGURE 1.** Density profile across a Si/Si bonding interface as obtained from X-ray reflection experiments

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# Laue MicroDiffraction on French Beamline BM32 at ESRF

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## ABSTRACT

X-ray scattering experiments on polycrystals at micrometer scale have shed new light on structure and mechanical behavior of unique or assembly of small systems such as semiconductors devices, metal interconnects, MEMS. Conventional scattering on single crystal is a powerful and advanced structural technique but is generally difficult to set up at this scale needing time-consuming data collection procedures. Laue diffraction corresponding to the scattering of a white (polychromatic) beam overcomes this limitation: A large number of Bragg reflections is collected on a 2D detector from a single x-ray shot. This Laue pattern is analysed in two steps: orientation recognition (indexation) and strain refinement for each crystal grain. Laue MicroDiffraction allows a fast and non destructive 2D mapping of grain to grain orientation and strain with a submicrometer spatial resolution. Only few beamlines on 3rd generation synchrotron facilities offer an intense white micron-sized beam dedicated to materials science. French CRG-IF-BM32 beamline located at ESRF has operated since 2006 a microdiffraction setup unique in Europe, running complementary Laue and monochromatic diffraction techniques. It is delivering a stable narrow x-ray probe (beamsize: <1X1 $\mu m^2$) to determine the local full strain tensor in various *in situ* loading environments (e.g. temperature, electromigration and mechanical stress). Developments aiming at increasing the instrument throughput are underway: improved automation to fit increasing characterization needs from microtechnologies and extension towards 3D resolution allowed from the larger penetration capability of x-rays.

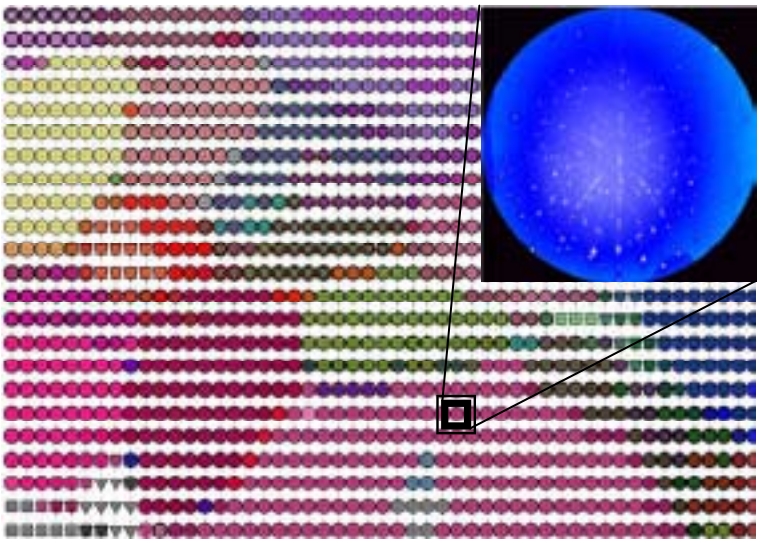

**FIGURE 1.** Determination of local orientation and strain of several grains at each mapping step (1 micron) from the analysis of of the Laue microdiffraction pattern (insert).

# Fluorescence yield XAFS spectrometer for light elements (B, C, N, O) in semiconductor materials

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## ABSTRACT

Light elements such as boron, carbon, nitrogen, and oxygen play important roles for silicon and compound semiconductor devices. They influence electronic properties as dopants or impurities. The measurement of the structural and electronic properties of those light elements is challenging. Atom probe and TEM provide atomic-scale distribution and lattice images, but we normally cannot analyze the lattice location of the light elements. X-ray absorption fine structure (XAFS) spectroscopy complements atom probe and TEM data, although spatial resolution is not in nanometer scale. XAFS measurements for impurities in matrices are frequently performed by using fluorescence x-rays at synchrotron radiation beam lines. However, the light elements in semiconductor materials are difficult to detect with energy dispersive x-ray (EDX) detectors, because of the low energies of fluorescence x-rays in a range of 183 – 525 eV. The situation gets worse when the matrices are wide band gap semiconductors such as SiC, ZnO, and diamond. Spectral overlap between the impurities and the matrix elements obscures the information of the target impurities.

Our solution to realized fluorescence yield XAFS for the light elements is to use a superconducting EDX spectrometer, which has a high energy resolution of better than 20 eV@ N Kα: 392 eV and an expected counting rate of over 1 Mcps.[1] The prototype XAFS spectrometer is shown in Fig. 1.

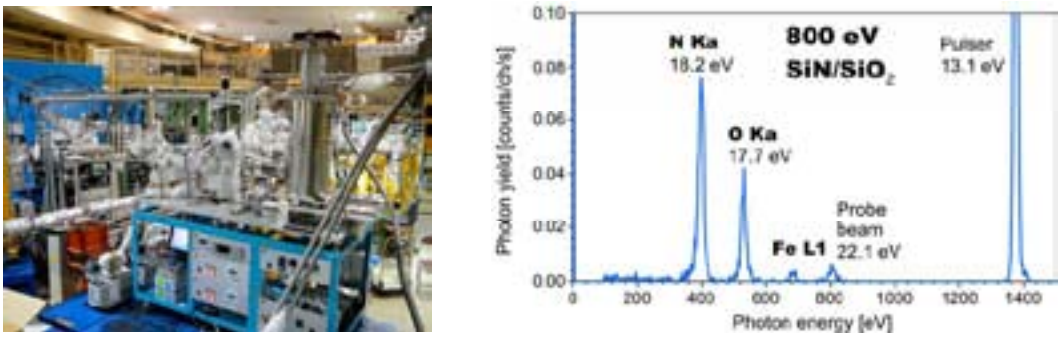


**FIGURE 1.** XAFS spectrometer equipped with a superconducting EDX detector system and energy resolution for the light elements at a KEK PF beam line.

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**Light element, Impurity, XAFS, Energy-dispersive x-ray spectroscopy, Superconducting detector**

# The Reduction of Substitutional C in Annealed Si/SiGeC Superlattices Studied by Dark-Field Electron Holography

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## ABSTRACT

SiGeC is an attractive material in microelectronics because carbon doping offers flexibility for the control of the strain, the composition and the electronic properties of epitaxial layers grown on silicon. A small content of C in substitutional position can compensate the strain induced by a relatively large proportion of germanium. However, the reduction of substitutional C under $\beta$-SiC precipitation during annealing at high temperature limits the processability of the material[1]. Here, we have estimated the substitutional C content in annealed $Si/Si_{0.744}Ge_{0.244}C_{0.012}$ superlattices grown by reduced pressure - chemical vapor deposition (RP-CVD), by comparing dark-field electron holography[2] (DFEH) and finite element simulations. As DFEH is a TEM-based imaging technique, it provides a visual interpretation which is helpful for the decorrelation of the different relaxation mechanisms: Si and Ge interdiffusion, dislocation and cluster formation. Practically, the Ge and C distributions were first established by SIMS. The strain distribution was then mapped by DFEH (cf. Figure 1). Supposing that the interstitial C has a negligible influence on the SiGeC lattice parameter, the strain in the lamellas was simulated for different substitutional C content until a good fit was obtained with the experiment. It was found that the substitutional C content is equal to 0.75% in the as-grown samples and decreases to 0.6% after annealing at 950°C during two minutes. After annealing at 1050°C, it was concluded that all the C content has moved to a non-substitutional position and does not contribute anymore to the strain state.

**Key-words:** *Strain, Holography, SiGeC.*

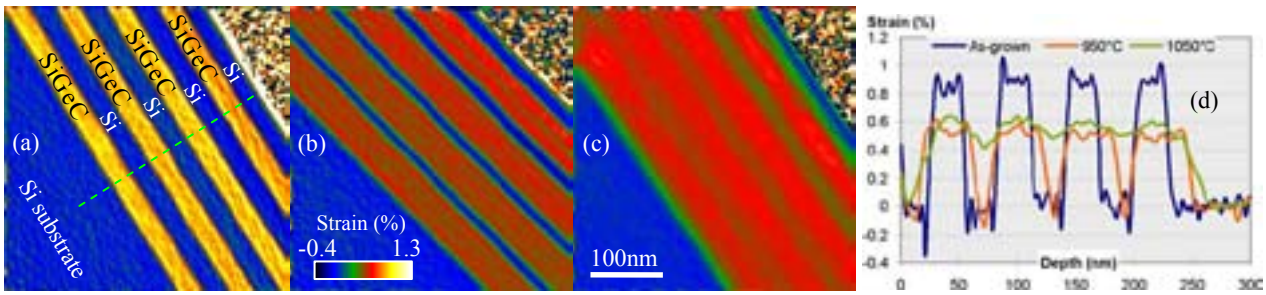


**FIGURE 1.** Strain maps of the Si/SiGeC superlattices reconstructed from dark-field electron holograms: (a) as-grown sample, (b) sample annealed at 950°C and (c) sample annealed at 1050°C. (d) Strain profiles extracted from the maps.

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# Atomic Layer Deposited $Al_20_3$ as Characterized Reference Samples for Nanolayer Metrology

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## ABSTRACT

The continuous reduction of device dimensions for nano- and microelectronics but also for nanotechnologies drives the development of metrology, analysis and characterization. The comparison and benchmarking of metrology require well-designed calibration and reference materials [1]. Due to the interaction of the probe with the studied sample, and in particular the specific probing conditions at the sample, reference samples have to be adapted to the measurement task. Furthermore, the specific modelling of both the sample and the metrology are required for obtaining comparable and reliable results. In this paper thin $Al_2O_3$ films produced by Plasma Assisted Atomic layer Deposition (PA ALD) were characterized by a complementary metrology approach using Spectroscopic Ellipsometry (SE) and Total Reflection X- Ray Fluorescence (TXRF).

The instruments were a Woollam M-2000DI rotating compensator ellipsometer and an Atomika 8300 W using WLβ excitation, respectively. SE was used to determine the thickness and the optical properties of the samples. TXRF was used to perform elemental depth profiling and surface contamination analysis. The linearity of the layer thickness with the number of cycles is given in Figure 1 (left). The linearity of the Al fluorescence signal as a function of the number of cycles is given in Figure 1 (right). The Figure 1 (middle) shows the angular resolved TXRF analysis of Al in the layer. Such results require modelling of the according metrology and the samples e.g. the elemental distribution on the surface. Sulphur and chlorine profiles on surface and in the depth were detected and analyzed, too. These characterized samples sustain development of analytical techniques. Furthermore, they are suitable for calibration and benchmarking of optical and X-ray metrology.

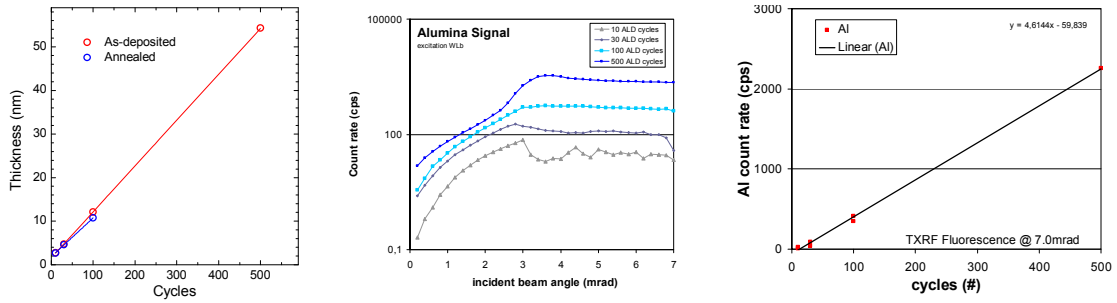


**FIGURE 1:** left: Results of ellipsometry showing the thickness vs. ALD cycles. The interception with the y axis is 1.61 and 1.86 for the as-deposited and annealed cases, respectively.
middle: TXRF Al signal as a function of the incident beam angle, showing an increase of the critical angle.
right: Result of the TXRF analysis showing the a linear Al signal increase with the number of cycle at 7.0 mrad incident beam angle

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# A Novel X-ray Diffraction and Reflectivity Tool for Front-End of Line Metrology

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## ABSTRACT

At the 32 nm technology node and beyond, strain engineering remains a critical approach for enhancing the performance of advanced logic devices. Selective epitaxial growth of SiGe into the source/drain regions of pMOS transistors is used to introduce uniaxial compressive strain the Si channel in order to improve the hole mobility. A similar approach using Si:C is being investigated to introduce uniaxial tensile strain for future nMOS transistors, which should improve the electron mobility beyond what is possible using SiN stress-liners alone. The increased complexity and use of selective epitaxial processes is challenging conventional in-line metrology.

High-resolution X-ray diffraction (HRXRD) is an established technique for the characterization and metrology of epitaxial thin-films. However, its use by the silicon semiconductor industry for in-line process control has been limited due to the stringent reliability, throughput and spot-size requirements for product wafer measurements. We have developed a novel X-ray metrology tool (JVX 7200) that meets these demands. The tool features an HRXRD channel that provides composition, relaxation and thickness information for SiGe and Si:C epitaxial films. It also combines an X-ray reflectivity (XRR) channel to provide complimentary thickness, density and roughness information on SiGe as well as other front-end of line (FEOL) films, such as those found in high-*k* gate stacks.

We will describe the JVX 7200 tool, its capabilities and will also provide a comparison with more traditional X-ray metrology tools. We will demonstrate that reliable measurements can be obtained on small test pads that are compatible with current design rules. Representative data will be presented for several FEOL film stacks.

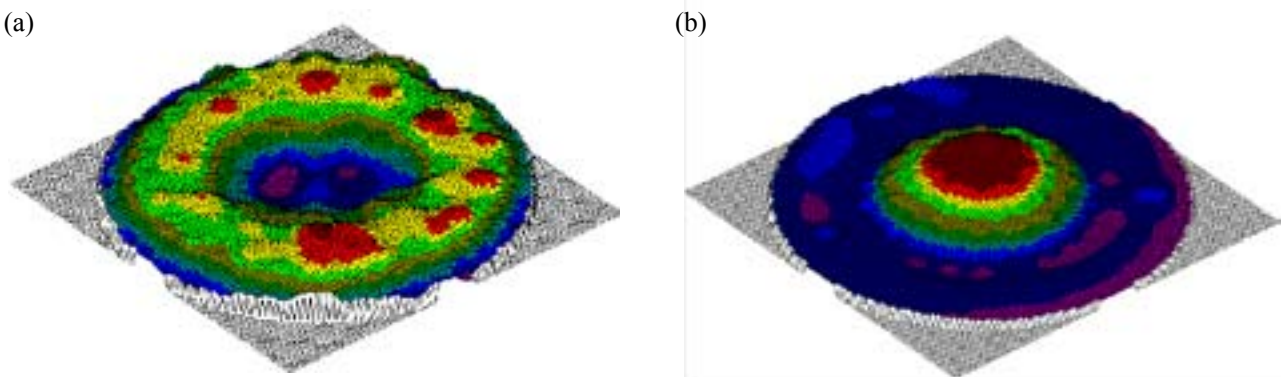


**FIGURE 1.** Rapid uniformity maps from a blanket SiGe epilayer on a 300 mm Si(001) wafer using (a) HRXRD for composition and (b) XRR for thickness. Thickness mapping is also possible with the HRXRD channel in the case of fully-strained epitaxial films.

# Comparison between spectroscopic ellipsometry and HRTEM-VEELS analyses of $HfO_2$-based stacks.

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## ABSTRACT

HfO2-based materials are interesting candidates for advanced CMOS gate dielectrics and for advanced devices such as non volatile memories. The downscaling trends driven by the industry induce drastic requirements in terms of nanocharacterization of the structural, optical and electronic properties. Among the various characterization tools for high-k materials, optical methods such as spectroscopic ellipsometry has been proved to be efficient for the determination of thicknesses and optical properties of thin films with nanometric resolution[1], however these methods are usually not applicable to a site-specific nm-area analysis of the dielectric characteristics of nanometric devices. One of the most prominent alternative is the valence electron loss spectroscopy (VEELS) inside a high-resolution transmission electron microscope[2]. This technique, combined with conventional EELS, may provide interband transitions energies (bandgap), plasmons frequencies, and chemical composition analysis with nanometric spatial resolution[3]. In this presentation, we will compare the results obtained by spectroscopic ellipsometry and HRTEM-VEELS on the same sample. We will demonstrate that a good agreement is obtained between the two methods for the bandgap, the optical indexes and the layer thicknesses.

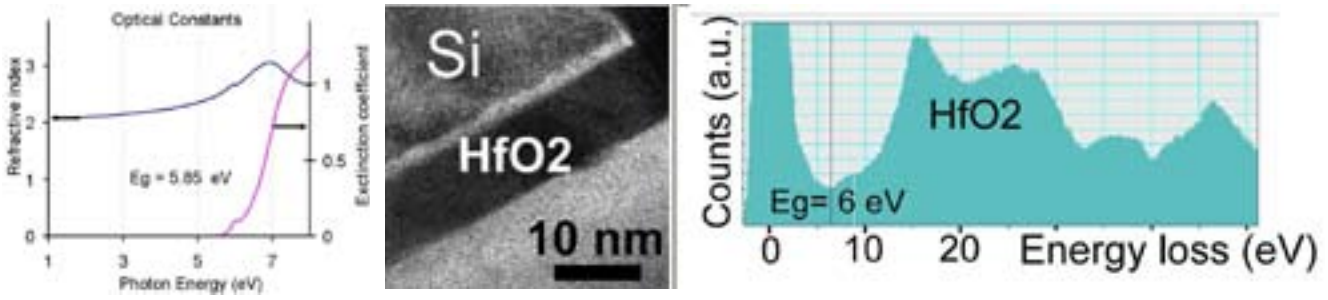


**FIGURE 1** : Optical indexes obtained by spectroscopic ellipsometry (left), for a 10 nm thick HfO2 stack (center). The bandgap of 6 eVobtained by HRTEM-VEELS (right) is very close to the value obtained by ellipsometry (5.85 eV).

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# Development Of A High Brilliance X-ray Source For Advanced Thin Film Characterization

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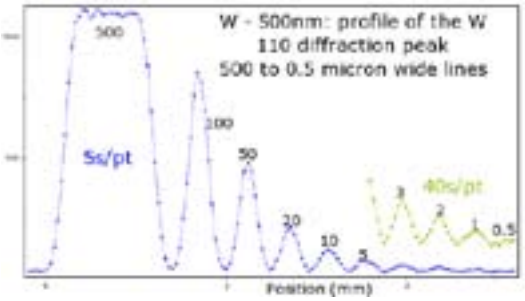
## ABSTRACT

X-ray based metrology techniques have demonstrated their capabilities for the measurement of critical process parameters on complex microelectronic thin film structures such as layer crystallinity or texture analysis (X-ray Diffraction, XRD), multilayer thickness (X-ray Reflectivity, XRR), material composition (X-ray Fluorescence, XRF) [1]. Achieving the X-ray beam spatial resolution and photon density for fast, high precision data acquisition on small test structures is a real challenge. This requirement is being addressed by various equipment suppliers integrating microfocus sealed tubes X-ray sources with moderate brilliance coupled with advanced X-ray optics [2]. However the further increasing requirements of future technology nodes are increasing the challenge and higher brilliance solutions are required.

In the framework of a French collaborative project (HIBRIX), we have been investigating a new X-ray beam delivery concept. This solution is based on a relatively medium power micro-focus source (using rotating anode technology) coupled with a high efficiency multilayer optics to provide an intense high brilliance X-ray beam optimally shaped for the required application. A prototype has been installed at the CEA-LETI in France on a multi application diffractometer platform (XRD/XRR/XRF) consisting of a 4-circle goniometer and various detector configurations.

Performances of the setup (in terms of brilliance, spatial resolution, detection limits) have been demonstrated and compared with those of commercial diffractometers, highlighting the impact of increased photon density and high spatial resolution for process diagnostic on polycrystalline materials. Combined XRD and XRF measurements have been carried out on various samples with pattern sizes between 0.5 and 500 microns: W and TiN lines, back-end T-boxes, patterned SOI. Tilt and stress of patterned SOI layers have been measured.



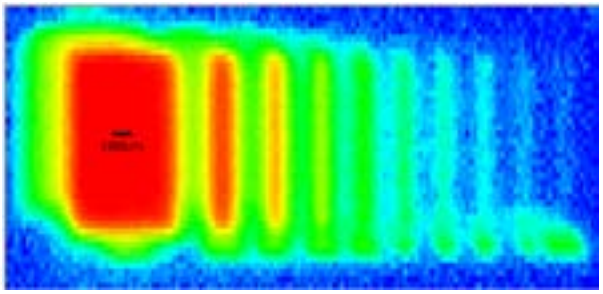



**FIGURE 1 (left).** Profile of a 500 nm thick W patterned layer on Si measured by X-ray diffraction.
**FIGURE 2 (right).** Mapping of a 60 nm thick TiN patterned layer on Si measured by X-ray fluorescence.

The multi-application diffractometer has been funded by the French National Research Agency (ANR) through the "Recherche Technologique de Base" Program. The HIBRIX project has been supported by FUI-Minalogic.

**Keywords : X-ray micro-focus source, mapping metrology, combined X-ray analysis**

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# Synchrotron Radiation X-Ray Photoelectron Spectroscopy Applied to Advanced High-k Metal Gate Stacks

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## ABSTRACT

The integration of metal gate/high-k dielectric structures for the 32 nm-generation of CMOS devices and beyond requires a thorough physico-chemical characterization of the stacks with appropriate experimental techniques in order to help further optimizations. X-ray photoelectron spectroscopy (XPS) is widely used for this purpose. Laboratory XPS instruments, which typically use Al $K\alpha$ (1486.6 eV) or Mg $K\alpha$ (1253.6 eV) lines for excitation, give very useful information. However the capabilities of laboratory systems are typically limited by their energy resolution and surface sensitivity. The use of synchrotron radiation overcomes these obstacles thanks to: an improved spectral width ranging from hard to soft x-ray domain, a tunable energy and high brightness source. Then, synchrotron radiation allows the non-destructive in-depth analysis of nanoscale buried layers and interfaces typically present in CMOS structures.

Using both soft (S-XPS) and hard (HAXPES) x-ray photoelectron spectroscopy, a detailed analysis of the chemical and electronic properties of technologically relevant TiN/HfSiON/SiON/Si gate stacks (i.e. processed in "integration like" conditions) will be presented. In these structures, an ultra-thin LaOx or AlOx capping layer is inserted in between the TiN gate and the HfSiON dielectric. Measurements were performed at the Soleil synchrotron facility on beamline TEMPO for S-XPS and at the ESRF on beamline ID32 for HAXPES. The combination of these techniques enables us to successfully probe the targeted interfaces, without deprocessing the top TiN metal gate layer keeping the integrity of the full stack. These analyses not only have confirmed the formation of interfacial silicate layers but, they have also assessed their thermal stability. In addition, based on the core level energy shifts, we highlight band offsets, which strongly indicate the presence of an interfacial dipole and/or a fixed charge effect. The results of the different analyses will be discussed and related to the electrical properties of the devices.

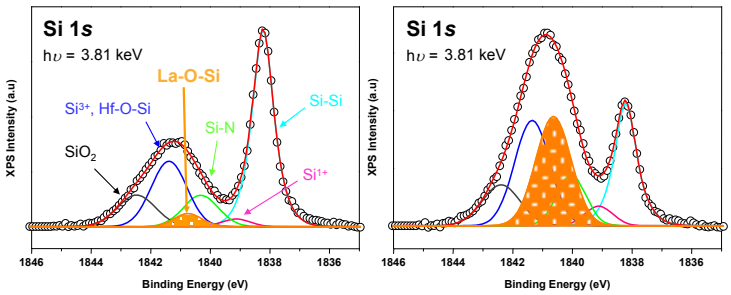


**FIGURE 1.** Si 1*s* core-level spectra obtained with HAXPES on TiN/LaOx/HfSiON/SiON/Si gate stacks before (left) and after (right) high-temperature activation annealing

**Keywords:** Synchrotron radiation, S-XPS, HAXPES, High-k, CMOS

# A High Depth Resolution MEIS Analysis Of Ultra Thin STO/TiN Layers On Si For DRAM MIM Capacitors

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## ABSTRACT

The physical characterisation of atomic layer deposited (ALD) $Sr_xT_{1-x}O_y$ (STO) dielectric material films, a few nm thick, for application in metal-insulator-metal capacitors (MIMcap) in the form of high aspect rather than planar geometries in Dynamic Random Access Memory (DRAM) devices [1], represents a considerable metrology challenge. The analysis is important since there is currently a renewed interest in the behaviour of such layers, especially when combined with TiN electrodes, which is a low cost alternative to Pt or Ru metal ones [2]. Medium energy ion scattering (MEIS) in conjunction with energy spectrum simulation has been demonstrated to possess the capability of yielding quantitative information on the structure and composition of shallow planar layers with sub-nm depth resolution at the surface in a comparison with other techniques in an analysis of $HfO_2$ and $Hf_xSi_yO_2$ gate dielectric nanofilms [3]. Important factors that affect the quantification of MEIS information such as neutralization, Andersen correction and the changing energy bin width across the energy spectrum will be briefly discussed.

Sample structures investigated were a full MIMcap structure comprising of a 2 nm TiN top electrode, a 3 nm STO (Sr-rich or stoichiometric) insulator layer and a 3 nm TiN bottom electrode, both before and after annealing at 650°C in $N_2$ and these were preceded by subsets of this structure. MEIS conditions used were 100 keV He ions in the double alignment configuration, [-1-11] in, [111] or [221] out, yielding scattering angles of 70.5 or 90°.

Further to the determination of the composition and thickness of the layers investigated, MEIS studies have enabled the monitoring of interface behaviour, providing information on processing and interface issues such as the effect of the TiN sputter deposition process, the near-surface Sr enrichment of an uncapped Sr rich STO layer, Ti interdiffusion into the Sr rich STO upon annealing and the apparent higher thermal stability of the stoichiometric STO/TiN system against Ti diffusion.

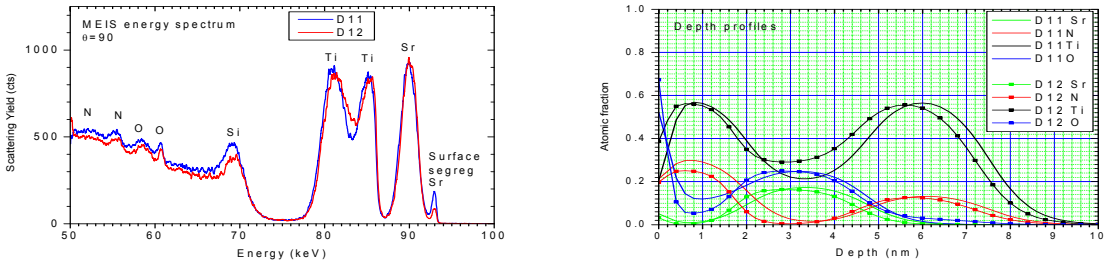


**FIGURE 1.** MEIS spectra and profiles of a TiN/STO/TiN MIMcap structure before and after annealing to 650°C in $N_2$.

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# Multi-technique Approach for the Evaluation of the Crystal Phase of Ultrathin High-*k* Gate Oxide Films

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## ABSTRACT

High-*k* $HfO_2$ based gate oxides have recently been put into production in CMOS based integrated circuits, and their use in future integrated circuits depends on how well they can continue to be downscaled. To this end, efforts to increase the dielectric constant (*k*) of $HfO_2$ based gate oxides have been ongoing..[1] Higher-*k* values (k>30) for $HfO_2$ occur for the metastable tetragonal/cubic crystal phases, while the thermodynamically preferred monoclinic phase has a lower *k* value (~20).[2] Recent work has shown that by tailoring annealing procedures the higher-k phase can be stabilized.[3] Much of this work, however, has been done on films that are significantly thicker than those used in devices (< 30 Å). In this regard, to evaluate the crystal structure of such thin $HfO_2$ films which have undergone various annealing treatments, we used a multitude of techniques including grazing incidence X-ray diffraction (GIXRD) in both in-plane and out of plane configurations, spectroscopic ellipsometry (SE), and UV photoelectron spectroscopy (UPS) measurements. SE has shown that the extinction coefficient of the $HfO_2$ film has a sub-band-gap feature that is associated with crystallinity.[4] UPS measurements of the valence band of $HfO_2$ have shown a characteristic two peak structure that is also associated with crystallinity.[5] We have analyzed the extinction coefficient and valence band spectra from SE and UPS measurements, respectively, and correlated them with the XRD measurements in an effort to find additional methods to distinguish the crystal phases of the $HfO_2$ films. **(Keywords: high-κ, higher-κ, crystal phase, grazing incidence X-ray diffraction, spectroscopic ellipsometry, UV photoemission spectroscopy)**



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# High Frequency Acoustics For Probing At Nanometer Scale in SOI-based stacks

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As dimensions in devices continuously shrink, available tools have to be refined and novel schemes explored. Here we do show that high frequency acoustics provides interesting opportunities when dimensions come in the nm range. We present Raman-Brillouin scattering (R-BS) involving high frequency acoustic phonons from stacks based on SOI structures (i.e. a thin silicon layer separated from a silicon substrate by a buried oxide layer) having additional inserted or deposited $SiO_2$, $Si_3N_4$ or $Al_2O_3$ layers with thicknesses in the nm range. We have shown recently that thin Silicon On Insulator (SOI) layers can be used as internal probes, providing simultaneously the generation and detection of THz acoustic phonons [1] and avoiding the deposition of transducers (which are required in conventional optical pump-probe experiments). We demonstrate that the R-BS from the SOI layer is very sensitive to its environment, i.e. the other layers in the stack. As an example, Figure 1 shows how the SOI R-BS depends on the thickness of an $Al_2O_3$ capping layer.

Comparing experiment and simulations allows one to perform a quantitative analysis of the actual stack characteristics, regarding layer thicknesses, elastic properties and the presence of interfacial layers. Interestingly, high frequency acoustic phonons are particularly sensitive to the interface quality. The correlation between R-BS and Electron Energy Loss Spectroscopy is presented. We demonstrate that the R-BS from a ultra-thin SOI layer provides a means of probing properties of surrounding layers and materials at nm-scale.

Keywords : acoustic, phonon, SOI

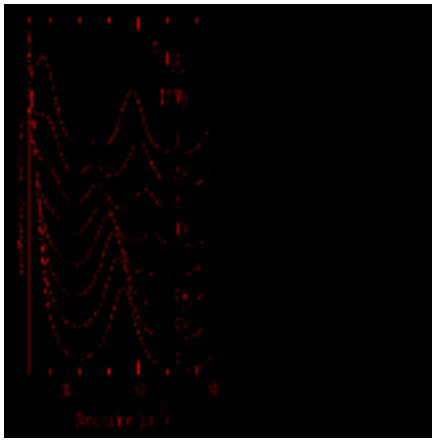

**FIGURE 1.** Calculated R-BS from a 20 nm thick SOI capped with $Al_2O_3$, as a function of cap layer thickness.

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# SiC Resistivity Monitoring; A look at Novel Methods

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## ABSTRACT

The market for SiC devices is growing rapidly in Asia, US and Europe. Applications include heterojunction transistors where SiC emitters allow forming high gain, high speed, and radiation hardened devices. SiC is particularly attractive for the power device manufacturers due to its wide band gap and high thermal conductivity.

For all applications, the electrical properties of the SiC epitaxial layer, such as doping density or resistivity are mostly critical. Conventionally, Mercury Probe Schottky CV has been used for SiC resistivity measurement. Hg probe CV is a well developed method but often requires a surface treatment and is contaminating. This paper presents several novel methods for determining the carrier density in SiC. One method involves the use of a non-destructive and non-contaminating Elastic Material probe (EM-probe) [1]. MOS CV measurements, both equilibrium and non-equilibrium, can be made with this probe. The small area and probe oxide layer reduce the need for surface treatment and, statistically reduce the chance of forming a contact on a defect site. Additional parasitic effects, such as dissipation factor and leakage are reduced significantly, as well. Another presented alternative method that allows carrier density profiling in SiC utilizes conductive rubber probe with the contact diameter about 0.5 mm.

An example of EM-probe MOS CV measurement of a SiC Epitaxial layer is shown in Figure 1. Figure 2 shows a correlation plot between Hg probe and EM-probe for several samples. Samples 4 and 5 could not be measured with the standard Hg probe due to the surface issues, while EM-probe MOS CV measured these samples readily.

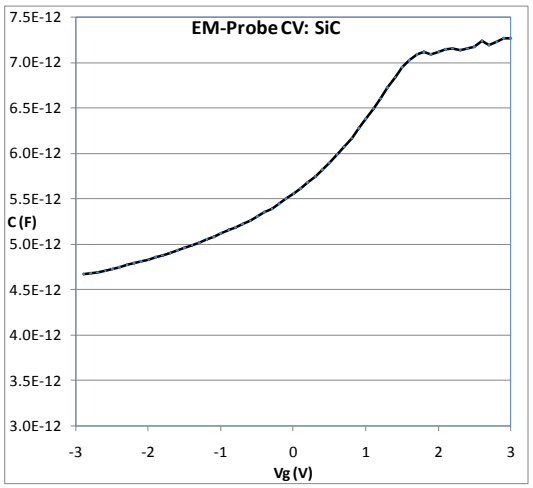


FIGURE 1. EM-probe MOS CV on SiC Epi.

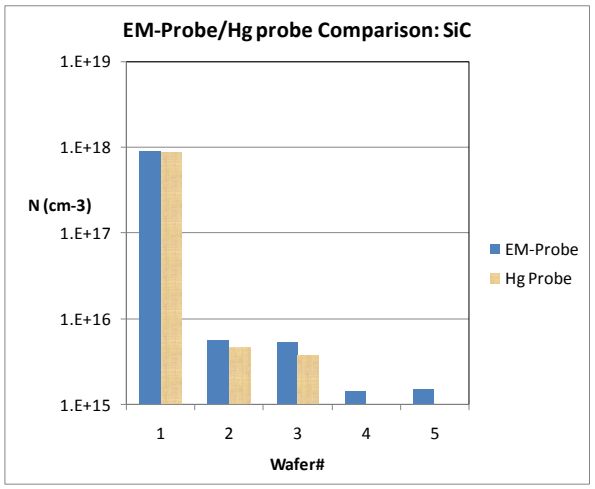


FIGURE 2. EM-probe vs. Hg probe comparison

*Key words: Nano-electronics Materials and Devices; Novel Measurement Methods, SiC*

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# A Method for USJ Process Control

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## ABSTRACT

Ultra-Shallow Junction formation is one of the most challenging areas of semiconductor processing to monitor. Most of the dopant characterization techniques, both electrical and optical, are primarily designed to monitor only one step of doping process: they can be used either to monitor implant induced defect density or to measure activated doping. The presented Surface Photo-Voltage (SPV) - based method [1] is a non-contact mapping technique capable of measuring implanted silicon wafers both before and after electrical activation of doping atoms.

Presented method has been developed for ion implant characterization process and was outlined in several publications [1, 2]. The technique operates in low injection mode and is high frequency modulated. Analysis of the signal allows correlation of the response to critical implant process parameters, such as implant dose, implant energy, beam angle, etc. For annealed wafers, the technique allows calculation of activated doping density averaged over all depletion layers, within the light absorption region.

The important advantage of the method is the capability to measure the multilayer structures. Commonly, to achieve high quality Ultra-Shallow Junction layer IC manufacturers use various pre-conditioning implants, such as Halo or PAI. In the paper we demonstrate the sensitivity of the method to the dopant/implant dose variations in both the source-drain and halo implant regions. The sensitivity of the developed technique to multiple doping layers is due to the electrical connection of these layers and it can be tuned by modifying the excitation light properties. We report measurement results of the single USJ and double implants, including Halo. The measured sensitivity to $As^{75}$, $B^{11}$ and $BF_2$ implant doses in Halo and USJ layers varied from 0.8 to 1.2 with the signal repeatability < 0.25% (see Figures 1 and 2).

*Key words: Ultra-Shallow Junctions; In-Situ, Real-Time Control and Monitoring; Novel Measurement Methods*

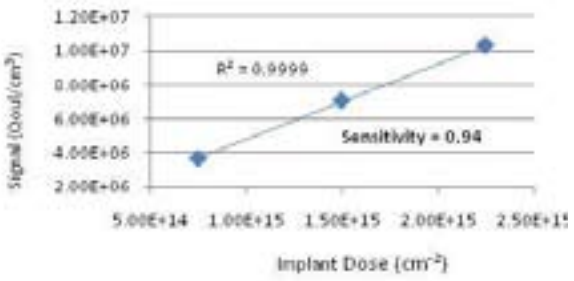


FIGURE 1. Dose Sensitivity to the USJ double implant

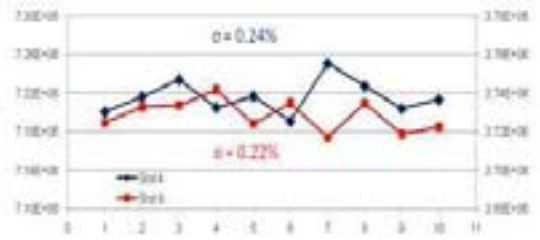


FIGURE 2. USJ Measurement repeatability: As + B

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# Soft X-Ray Induced Characterization Of Ultra Shallow Junction Depth Profiles and Activation

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## ABSTRACT

Soft X-ray induced characterization methods including Grazing Incidence and Grazing Exit X-Ray Fluorescence Analysis (GIXRF and GEXRF respectively) as well as Near Edge X-ray Absorption Fine Structure (NEXAFS) have been adopted to the characterization of ultra shallow junction implantations into silicon.

To determine implantation depth profiles, GIXRF uses the in depth changes of the X-ray standing wave field intensity dependent on the angle between the sample surface and the primary beam [1]. Additionally, implantation depth profiles were derived from GEXRF measurements, where the exit angle of the excited fluorescence radiation was selected with a von Hamos type spectrometer [2].

For the evaluation of the suitability of NEXAFS on the characterization of electrical activation of thermally treated ultra shallow junction implantations, measurements at the boron K-edge have been conducted. The results obtained are in line with sheet resistance measurements.

Arsenic, Boron and Aluminum implanted Si wafers with nominal fluences between $1x10^{14}$ $cm^{-2}$ and $1x10^{16}$ $cm^{-2}$ and implantation energies between 0.5 keV and 50 keV have been used to compare SIMS analysis with synchrotron radiation induced GIXRF and GEXRF analysis in the soft X-Ray range. The GIXRF measurements have been carried out at the laboratory of the Physikalisch-Technische Bundesanstalt at the electron storage ring BESSY II using monochromatized undulator radiation of well-know radiant power and spectral purity [3]. The GEXRF measurements were obtained at the ID21 beamline of the ESRF in Grenoble.

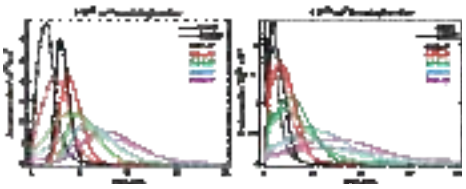

**FIGURE 1.** Comparison of the As and B depth distributions for implantation energies between 0.2 keV and 5 keV as determined by GIXRF and SIMS.

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# Single Wavelength Photoreflectance Characterization of Strain Relaxation in Silicon on Silicon-Germanium

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## ABSTRACT

Photoreflectance (PR) provides an optical means to measure the electronic properties of semiconductor nanostructures. Single wavelength PR has been suggested for process control measurements of strain and active dopants in silicon IC manufacturing if a probe beam with a suitable wavelength is chosen [1]. Recently, such an approach has proven effective for characterizing milli-second anneal processes used in ultra-shallow junction formation [2]. This paper reports the use of single wavelength PR to characterize strain in silicon on silicon-germanium films. Silicon films ~1.5 to ~17.5 nm thick were deposited on graded silicon-germanium layers formed by chemical vapor deposition (CVD). The silicon film thicknesses were designed to achieve a progression of physical strain values, ranging from fully strained for thinner films to fully relaxed for thicker films. Reference metrology was performed using X-ray diffraction (XRD), Raman spectroscopy, and spectroscopic ellipsometry (SE). Methods to calibrate PR signals to physical strain in strained silicon on silicon-germanium layers are detailed. Single wavelength PR is shown to exhibit excellent sensitivity to physical strain in silicon on silicon-germanium films.

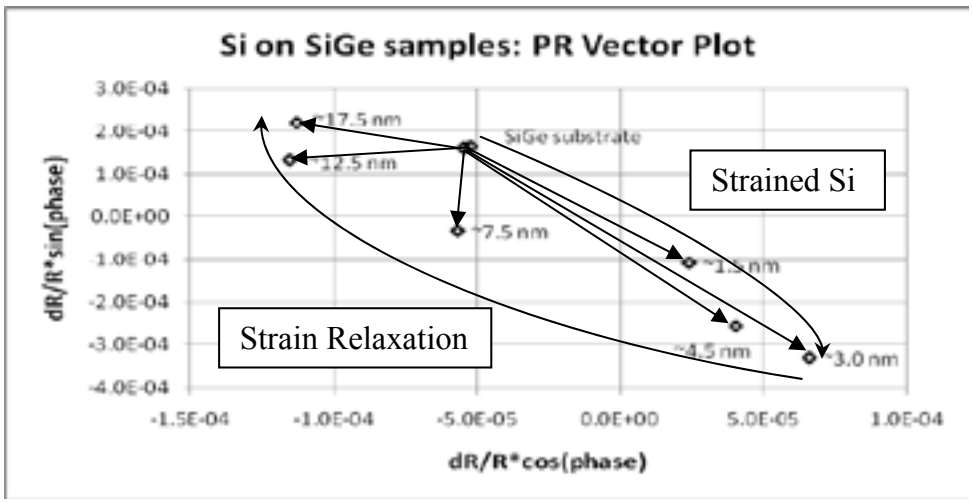


**FIGURE 1.** Measured photoreflectance vector for silicon films on silicon-germanium. Si thickness is indicated for each film.

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# Advanced SIMS Quantification in the first few nm of B , P and As Ultra Shallow Implants

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*Keywords* : Shallow Implants, SIMS, In-depth profiles, Quantification.

## ABSTRACT

Newest semiconductor chip manufacturing and further scaling of CMOS devices push to junction depths below the 10nm range with profile steepness of 1-2 nm/dec. At such scale, the SIMS technique can be used to monitor in-depth distributions of dopants, provided that SIMS profiles can be measured with depth resolution better than 1 nm/dec. This can only be achieved by using very low energy primary ion bombardment (<150 eV). The use of Extreme Low Impact Energy (EXLIE) sputtering conditions can be limited by a dramatic drop in sputter yield observed below 250eV impact energy. Therefore, SIMS tool primary ion columns must deliver high current densities at low impact energies to maintain erosion speeds consistent with reasonable analysis throughput. New $Cs^+$ and $O_2^+$ ion source designs on the CAMECA IMS Wf tool have improved source brightness, thereby giving access to sputter rates of 1 and 2nm/min for the $Cs^+$ and $O_2^+$ primary beams, respectively.

Analytical value of EXLEI sputtering conditions have been evaluated for B, P, and As ultra shallow implant profiles. The preferred protocol for As shallow profiles is $Cs^+$ 150eV in combination with $O_2$ oxygen backfilling. For B & P profiles, $O_2^+$ 150eV experimental conditions offer the best profile shape accuracy at the near surface. The overall results confirm that the use of EXLIE conditions minimizes near surface profiles artifacts. At the same time data quantification requires dedicated post-analysis data treatment to take into account transient sputtering at the near surface and matrix effects between Si and $SiO_2$. The capabilities of EXLIE conditions are further challenged when analyzing a structure with small lateral dimension such as test patterns. At very low energies, primary ion beam focusing on the surface is limited. High dynamic range depth profiles could suffer from crater edge effects during small-area analysis. However, sample preparation using the so-called MESA technique significantly improves the dynamic range in small pattern depth profiles. A trench around the pattern is removed using a higher energy for better throughput. A new software option enables fully automated MESA preparation prior EXLIE profiling on the CAMECA IMS Wf. Application examples of the use of EXLIE SIMS will be presented.

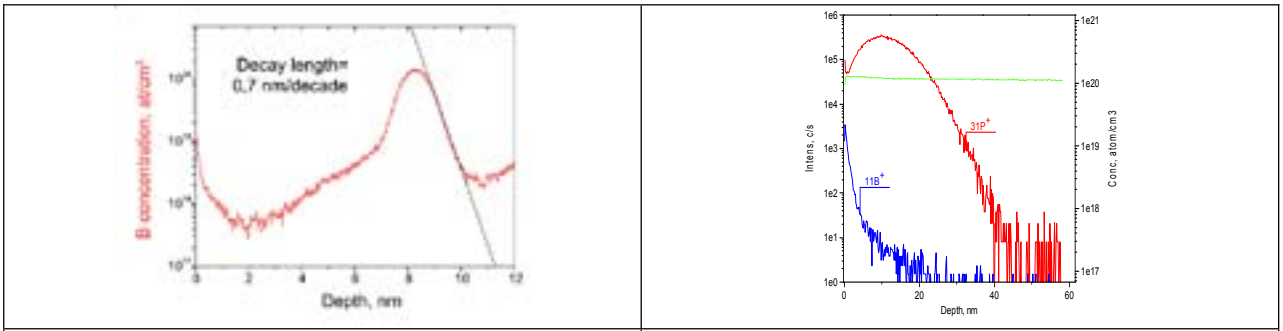


**FIGURE 1.** B delta layer profile measured under $O_2^+$ bombardment with 150eV impact energy




**FIGURE 2.** Phosphorous profile measured under $O_2^+$ bombardment with 150eV impact energy.

# The Use of LEXES to Measure the Chemical Composition of In-situ Doped Epitaxial SiGe for High Performance CMOS Technology

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N. Morel, M. Schuhmacher

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*Keywords* : SiGe, Boron, LEXES, Composition, Thickness.

## ABSTRACT

For the past few technology nodes, high performance CMOS logic designs have utilized so-called "Strained-Si" techniques to enhance device performance. In one of the most widely used embodiments, the source/drain regions of the device are etched away and epitaxial embedded SiGe or SiC is regrown in the S/D cavity. Several process integration adjustments are required to support these performance enhancement techniques and therefore new metrology needs are also required. Ideally the chosen monitoring technique needs to offer speed and flexibility to quickly define and adjust recipes for various integration / mask / design choices. The characterization of the structural properties (lattice spacing and layer thickness) of epitaxial SiGe is typically done by HRXRD. But the chemical composition also needs to be measured and controlled. LEXES (Low energy Electron X-ray induced Spectrometry), a non-destructive technique integrated into the fully fab-compatible tool CAMECA Shallow Probe, allows measurement of the Ge at.%, the SiGe film thickness, and the Boron concentration in the film.

The long term LEXES measurement stability for a SiGe:B film is shown in Figure 1. Across more than 3 months, the measured values of the Ge at.% and film thickness vary by less than 0.65% 1σ. Similarly the measured B concentration (on the order of 1E20 at/cm3) varies by less than 1% over the 3 months. For process development it is useful to have full wafer mapping as well as detailed local analysis. Figure 2 shows an example of a linescan in x and y across the diameter of a 300mm SiGeB blanket wafer showing the across-wafer non uniformity of that epitaxy process. The accuracy of the metrology data has been compared to the reference technique SIMS for composition and profile. A direct agreement better than +/-7 % is found.

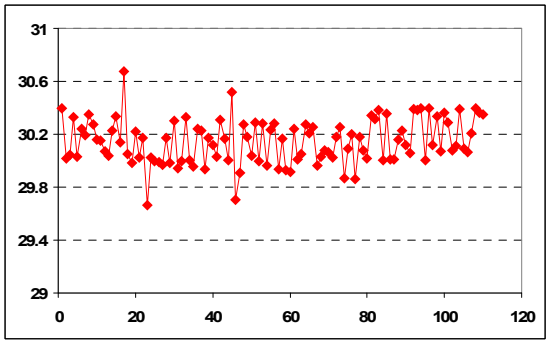


**FIGURE 1.** Ge at% monitored by LEXES for more than 3 months

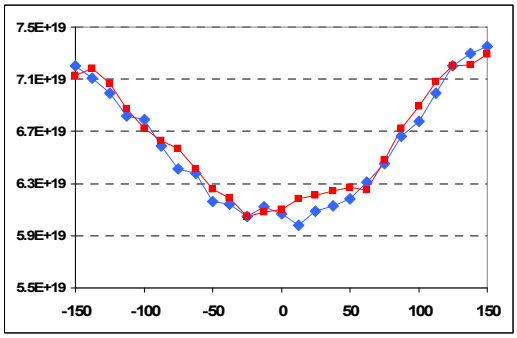


**FIGURE 2.** Line scan in X (blue ♦) and Y (red ■) directions of a 300 mm blanket wafer for [B] (at/cm$^3$).

# Advanced Use of Therma-Probe for Ultra-Shallow Junction Monitoring

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## ABSTRACT

Therma-Probe® (TP) is widely used in the semiconductor industry for the SPC monitoring of the various ion implantation steps included in the Complementary Metal Oxide Semiconductor process. This fully optical, hence non-destructive and fast, pump-probe technique measures the probe laser reflectance (DC reflectance) as well as the pump-laser-induced changes in probe reflectance (AC reflectance, also called TW signal). Interestingly, this technique uses tightly focused laser beams (radius=0.5 µm) allowing for very local measurements.

The physical origin of the commonly used signal, the AC reflectance, lies both in the pump-induced heating (*thermal* component) and in the presence of pump-generated excess carriers (*plasma* component), leading to two different and complementary measurement regimes and therefore two types of applications. On the one hand, if the *thermal* component is dominant (e.g. as-implanted layers, preamorphized substrates,...), the AC reflectance is a measure of the sample damage and, consequently, of implant dose[1,2]. On the other hand, if the *plasma* component is dominant (e.g. annealed implanted layers), the AC reflectance is sensitive to the carrier profile[3,4,5].

In this paper, we report on the latest advances in the use of TP for the monitoring of Ultra-Shallow Junctions both before and after annealing of the implanted layers. First, we discuss the sensitivity of TP to implant dose prior to anneal. Second, after annealing, we look at the capabilities of TP to map, over a whole wafer area, the local variations in sheet resistance (using the DC reflectance) simultaneously with the variations in junction depth (using the AC reflectance). Finally, we show that, by combining the DC and AC reflectances, TP offers a very powerful carrier profiling potential.

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# A Multi Techniques Approach to Characterize Ultra Shallow Junctions For sub 45 nm CMOS Devices

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## ABSTRACT

In order to achieve the requirements for P+/N junctions for <45nm ITRS nodes, ultra low energy and high dose implantations are needed. Different challenges have then to be faced. Plasma Immersion Ion Implantation (PIII) [1] efficiency is no more to proove for the realization of Ultra Shallow Junctions (USJ) in semiconductor applications: this technique allows getting ultimate shallow profiles (as implanted) due to no lower limitation of energy and high dose rate. But as the junction depth decreases and the ion implanted dose increase new characterization methods need to be developed to achieve real concentration in the first nanometer of the junction.

This paper presents physico-chemical characterizations of junctions realized with B2H6, BF3 or AsH3 PIII as implanted or followed by different annealing processes, with aim to obtain ultra shallow junctions.

In order to fully characterize these junctions, different Dynamical SIMS ([2-5] and figure 1) and TOF SIMS methodologies have been investigated and compared to ARXPS, TEM and Atom Probe experiments.

This full characterization allows evidencing the features that need to be taken into account in order to choose the best and fastest characterization mean. The features pointed out are the high concentration level (above the dilute limit), the etching and oxidation effects, the contamination effect. Moreover it allows to better understand the properties of the shallow junctions investigated.

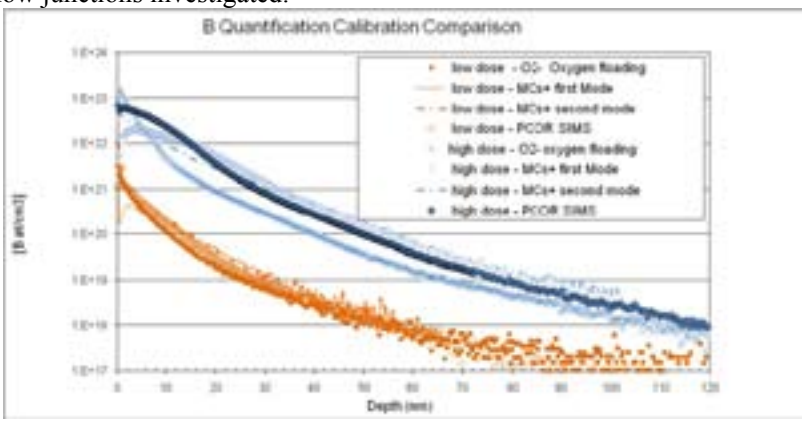


**FIGURE 1.** Boron PIII implant : D SIMS profile comparison.

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key words: Ultra Shallow Junction, SIMS, Atom Probe

# Advanced metrologies for topography and thickness measurements

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## ABSTRACT

Atomic force microscopy (AFM) is in common use in the semiconductor industry for surface geometry characterization. Despite the wide range of applications addressed by AFM, the technique is speed limited and contacts the surface. Because the probe contact with the surface may be destructive and the long time required for measurements, most AFM users limit the surface characterization to a few measurement locations.

Optical profilometry typically uses the interference between coherent light scattered from the test surface and from a reference surface to produce fringes. Of particular interest, the Scanning White Light Interferometry (SWLI) [1,2] combines the strengths of both Phase Shift Interferometry (PSI) and Vertical Scanning Interferometry (VSI) modes since the fringe coherence peak and the phase are used for the raw data processing. Similar to AFM images, the height map allows defect identification of features on a surface. However, conventional optical profilometry, contrary to the AFM, is limited to measurement of substrates or opaque surfaces.

A new data processing approach, proposed by ZYGO/Nanometrics, further expands the technique by analysis of the collected interferograms (ICT: Index Corrected Topography) to extract films parameters (thickness, for instance) and surface topography. This model based technique delivers literally complete information (*e.g.* topography, roughness, filmstack properties) of measured structure with sub-micron lateral resolution and angstrom vertical resolution. The approach is a strong asset since it allows contact less topography measurement of wafer surfaces in the low spatial wavelength range (i.e.: 0.599 – 5 μm).

In this paper we will show how this specific metrology can meet the aforementioned stringent requirements. The measurement stability and its accuracy will be discussed, and comparison with both the AFM and the spectroscopic ellipsometry will be presented.

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2. Peter de Groot and Leslie Deck, Proc. SPIE 2248; pp. 101-104 (1994)

| | Morning | AM Session | PM Session | Evening |
|---|---|---|---|---|
| **Monday** May 23rd | | | Check-in at hotel<br>**15:00 – 17:00** MINATEC Facility Tour (advanced registration required) | **17:00 – 20:00** Reception and registration at MINATEC Facility |
| **Tuesday** May 24th | **07:30** Registration Attendee Check-in<br>**08:00** Breakfast | **08:45** Conference Opening<br>**09:00 Session 1** Keynote Talks<br>**10:30** Coffee Break and Poster Viewing<br>**11:00 Session 2** Technology Overview for Nanoelectronics and Metrology | **12:00 Session 3** Metrology for Beyond CMOS<br>**12:30** Lunch<br>**14:00 Session 3** (continued)<br>**15:00 Session 4** Theory, Modeling and Simulation<br>**15:30** Coffee Break and Poster Viewing<br>**16:00 Session 4** (continued)<br>**16:30 Session 5 part 1** Microscopy for Nanoelectronics<br>**17:00** Poster Session | |
| **Wednesday** May 25th | **08:00** Registration Attendee Check-in and Breakfast | **08:30 Session 5 part 2** Microscopy for Nanoelectronics<br>**10:00** Coffee Break and PosterViewing<br>**10:30 Session 5** (continued)<br>**11:00 Session 6** Novel Characterization Methods | **12:30** Lunch<br>**14:00 Session 6** (continued)<br>**15:00 Session 7** CMOS Metrology<br>**15:30** Coffee Break and Dedicated Poster Viewing Session<br>**17:00 Session 7** CMOS Metrology (continued) | **18:45** Depart MINATEC for Banquet |
| **Thursday** May 26th | **08:00** Registration Attendee Check-in and Breakfast | **08:30 Session 8** Interconnect Metrology<br>**10:00** Coffee Break and Poster Viewing<br>**10:30 Session 9** Metrology for Patterning | **12:30** Lunch<br>**14:00 Session 10** Next-Generation Defect Inspection<br>**15:00 Session 11** Characterization Needs and Methods for "More than Moore"<br>**15:30** Coffee Break and Poster Viewing<br>**16:00 Session 11** (continued)<br>**17:30** Poster Session | |

Registration
**8:00 AM – 8:30 AM**

Interconnect Metrology
Session Chair: Scott List, Intel

**8:30 AM**
Metrology for 3D IC Integration (including TSV)
Ehrenfried Zschech, Fraunhofer Institute for Non-Destructive Testing ---------- P.112

**9:00 AM**
Nanomechanical Characterization and Metrology for Low- / ULK Materials
*Ude Hangen, Hysitron* ---------- P.113

**9:30 PM**
Stress-induced Effects Caused by 3D IC TSV Packaging on Advanced Semiconductor Processes
*Valeriy Sukharev, Mentor Graphics, San Jose/CA`* ---------- P.114

**10:00 AM**
Coffee Break and Poster Viewing

Metrology for Patterning
Session Chair: Victor Vartanian, ISMI

**10:30 AM**
Overview of EUV Mask Metrology
*Bryan Rice, SEMATECH* ---------- P.115

**11:00 AM**
3D-AFM Enhancement for CD Metrology Dedicated to 28 nm Node and Below
*Johann Foucher, CEA-Leti* ---------- P.116

**11:30 AM**
Advances in CD-Metrology (CD-SAXS, Muller Matrix based Scatterometry, and SEM)
*Brad Thiel, CNSE* ---------- P.117

**12:00 PM**
Line Edge Roughness of Directed Self Assembled PS-PMMA Block Copolymers – A Candidate for Future Lithography
*Wen-li Wu, NIST* ---------- P.118

**12:30 PM**
Lunch and Poster Viewing

Next-Generation Defect Inspection
Session Chair: Dick Hockett, Evans Analytical Group Ltd.

**2:00 PM**
Fundamental Limits of Optical Defect Metrology
*Richard Silver, NIST* ---------- P.119

**2:30 PM**
Wafer Inspection for Sub 20 nm Patterning
*Wolf Staud, Applied Materials Inc., Israel* ---------- P.120

Characterization Needs and Methods for "More than Moore"
Session Chair: Herbert Bennett, NIST

**3:00 PM**
Positioning More Than Moore Characterization Needs and Methods Within the 2011 ITRS
*Mart Graef, Delft Univ, Netherlands* ---------- P.121

**3:30 PM**
Coffee Break and Poster Viewing

**4:00 PM**
Measurements and Standards to Characterize More than Moore Applications of Electronics: Perspectives from KIT and IEC
*Norbert Fabricius, Karlsruher Institut für Technologie (KIT)* ---------- P.122

**4:30 PM**
Thermal Properties Characterization of Advanced Materials for Nanoelectronics
*Stefan Dilhaire, CNRS-CPMOH*---------- P.123

**5:00 PM**
Frontiers of More than Moore in Bioelectronics and the Required Metrology Needs
*Anthony Guiseppi-Elie, Clemson*---------- P.124

**5:30 PM – 6:30 PM**
Poster Session (with Wine and Cheese)

# Poster Presentations

**TH-15,** Joint Research on Scatterometry and AFM Wafer Metrology

B. Bodermann[1], E. Buhr[1], P. Klapetek[2], P.-E. Hansen[3], V. Korpelainen[4], F. Scholze[1], M. van Veghel[5], and A. Yacoot[6]
**[1]Physikalisch-Technische Bundesanstalt, Braunschweig**
**[2]Cesky Metrologicky Institut Brno, Brno**
**[3]Dansk Fundamental Metrolog, Matematiktorvet, Kongens Lyngby**
**[4]Mittatekniikan Keskus, Espoo**
**[5]VSL B.V., JA Delft**
**[6]NPL Management Limited, Teddington, Middlesex** ---------- P.139

**TH-16**, Possible Methods for Measuring the Impact of Bubbles in Temporary Bonding Materials for 3D Integration

S. Bernard[1], R.A. Miller[2], V. Pepper[3], J. Braggin[4], and F.F.C. Duval[2]
**[1]Entegris, GmbH., Dresden, Germany**
**[2]Imec, Kapeldreef 75, Leuven, Belgium**
**[3]Nanda Technologies GmbH, Unterschleissheim, Germany**
**[4]Entegris, Inc., Billerica, MA** ---------- P.140

**TH-17**, Studies of Impurity Redistribution in Copper Ultrafine Lines in BEOL Structures

H. Parvaneh[1], S. Novak[2], K. Dunn[2], M. Rizzolo[2], and E. Lifshin[2]
**[1]Department of Materials Science and Engineering, Rensselaer Polytechnic Institute, Troy NY**
**[2]College of Nanoscale Science and Engineering, University at Albany, Albany, NY** ------- P.141

**TH-18**, ToF-SIMS Analysis of the Effect of Bath Modulation on Impurity Incorporation into Damascene Copper

M. Rizzolo, H. Parvaneh, S. Novak, E. Lifshin, and K. A. Dunn
**College of Nanoscale Science and Engineering, University at Albany, Albany, NY** --------- P.142

**TH-19**, Multi-scale Resolution 3D X-ray Imaging for 3D IC Process Development and Failure Analysis

W. Yun, M. Feser, J. Gelb, and L. Hunter
**Xradia, Inc., Concord, CA** ---------- P.143

**TH-20**, Void Detection In Copper Interconnects Using Energy Dispersive X-Ray Spectroscopy

M. Tsigkourakos[1,2], T. Hantschel[1], A. Franquet[1], T. Conard[1], L. Carbonell[1], and W. Vandervorst[1,2]
**[1]IMEC, 3001 Leuven, Belgium**
**[2]K.U. Leuven, Department of Physics and Astronomy, Leuven, Belgium** ---------- P.144

**TH-21,** Fourier Scatterometry for Characterization of Sub-wavelength Periodic Two Photon Polymerization Structures

K. Frenner[1], V. Ferreras Paz[1], S. Peterhänsel[1], W. Osten[1], A. Ovsianikov[2], K. Obata[2], and B. Chichkov[2]
**[1]Institute of Applied Optics, Stuttgart University, Stuttgart, Germany**
**[2]Nanotechnology Department, Laser Zentrum Hannover e.V., Hannover, Germany** ------ P.145

**TH-22**, Robust, High Aspect Ratio Columnar Diamond Atomic Force Microscope Probes for High Relief Imaging

S.K. Tripathi[1], N. O'Hara[1], G. Fois[1], D. Scanlan[2], and G.L.W. Cross[1,2]
**[1]CRANN Nanoscience Institute, School of Physics, Trinity College, Dublin 2, Ireland**
**[2]Adama Innovations, Galway, Ireland** ---------- P.146

**TH-23**, Thin Film Mechanical Characterization Using Colored Picosecond Acoustics

P. Emery and A. Devos
**MENAPiC, Lille, Cedex, France** ---------- P.147

8-1

# Metrology for 3D IC Integration

Ehrenfried Zschech[1] and Alain Diebold[2]

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## ABSTRACT

Performance and functionality of microelectronic devices have increased continuously by increasing transistor integration densities ("More Moore") over more then four decades. However, today it has become questionable if this development alone will be able to overcome the predicted performance and cost issues as well as time to market for new product generations. The ITRS roadmap predicts 3D integration as a key technology to overcome this so-called "wiring crisis". The corresponding solution will most probably be based on through silicon via (TSV) technology. Many companies and research organizations are working currently in the area of 3D integration. A large percentage of this process flows are usually feasible but are still not commercially viable. Others are already part of products based on TSV technologies and actually present in the market. There are 3 ways to use TSVs to electrically connect multiple chips in a single package: die-to-die, die-to-wafer or wafer-to-wafer. This paper covers several process and materials approaches as well as analytical techniques for process and quality control.

At the same time that research in 3D stacking technology is advancing quickly, new requirements to microscopy techniques are coming up, and the analytical techniques have to be developed further. Void inspection after copper plating, defect detection and overlay measurements after wafer bonding are challenging. Microscopy techniques for which silicon is opaque such as scanning acoustic microscopy (SAM) and confocal infrared microscope (IR) are capable of inspecting the interface between bonded wafer pairs, while high-resolution X-Ray microcopy is used to detect voids in TSVs. This paper discusses the current status of SAM, IR microscopy and X-ray tomography, complemented by Focused Ion Beam analysis, in terms of their application to process metrology and failure analysis for 3D IC integration.

# Nanomechanical Characterization and Metrology for Low-k / ULK Materials

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## ABSTRACT

Low-k and ULK films are used in microelectronic products. These films have become an important material to develop next-generation integrated circuits that allow higher current densities by reducing the interconnect resistive capacitive delay. These films are designed for low dielectric constants by the choice of material and by increasing the volume of embedded pores. At the same time the low-k materials must exhibit enough structural support to be compatible with the demands of modern semiconductor processing. The damascene type processing may include chemical-mechanical polishing (CMP), lithography, etching etc. The dielectric and mechanical properties should not be affected.

For porous dielectric films the porosity is directly related to the dielectric constant [1]. Nanomechanical tests are therefore a suitable method of characterizing both – the structural stability and the expected dielectric performance. Force–displacement curves of an indentation experiment represent a fingerprint of the material and allow to directly characterizing the corresponding change in the process. Therefore an increasing demand for determining mechanical properties as a part of the process control is expected. More sophisticated methods of mechanical testing and the combination of methods allow to fully characterizing the structural change inside a low-k film.

Examples of different applications for nanomechanical testing in this area will be shown that allow characterizing the thin film adhesion to the substrate. The interfacial failure of a three layer film stack is shown as well as the effect of an unwanted collapse of porosity close to the surface that can be easily identified in the force-displacement curve of an indentation experiment. Overall monitoring hardness and modulus vs. depth allows studying substrate effects as well as stiffer materials regions. The profile of this property vs. depth curve will change with varying film thickness or structure variations. The meaning of "not producing a good film" becomes measurable.

## REFERENCES

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# Stress-Induced Effects Caused by 3D IC TSV Packaging on Advanced Semiconductor Processes

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## ABSTRACT

Mechanical stress management is a challenge for leading edge semiconductor technology, both in terms of achieving the desired device performance through strain engineering, and in terms of managing chip-package interactions. Starting from the 45 nm CMOS technology node, the mechanical stress has comparable impact on layout-driven variability of intra-channel charge carrier mobility and threshold voltage as the lithography-caused effects. The process steps employed by 3D IC technology such as wafer/die thinning, through silicon via (TSV) etching and filling, wafer bumping, high-temperature solder reflow, and chip stacking, etc. act as additional stress sources that can affect the chip-stack performance. It is a very challenging task to get an entire picture of the modification of the stress distribution across device layers caused by this technology. Hence, it is important to have a capability to assess the stress generated during 3D IC stacking accurately. Clearly, any such methodology has to be based on multi-scale simulation. This paper describes a recently developed physics-based stress simulation flow that includes an interface to layout formats (GDS, OASIS, etc) and can be linked with finite-element analysis-based package-scale models. A set of physics-based compact models for a multi-scale simulation to assess the mechanical stress and the consequent effects on device performance across the device layers in silicon chips stacked and packaged with the 3D TSV technology is proposed (Fig, 1). Analogously to multi-scale simulation, a multi-scale materials characterization is critical as an input for the predictive simulation of stress distribution across the device layout. A calibration technique based on fitting to measured stress components and electrical characteristics of the test-chip devices is presented.

Keywords: 3D IC, TSV, stress, simulation.

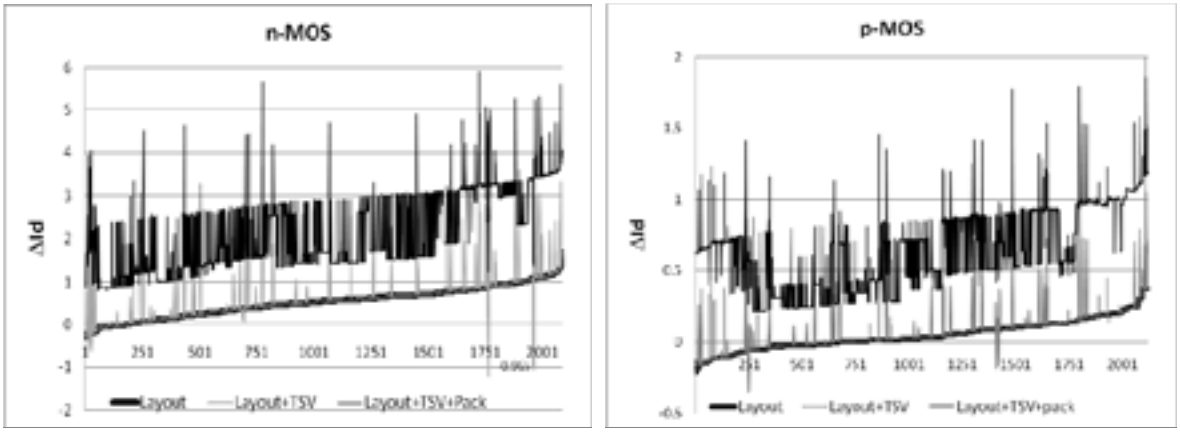


**FIGURE 1.** Sorted distributions of $I_{dlin}$ for NMOS (a) and PMOS (b) when layout-induced stress sources were accounted (thick black lines); TSV-induced stress was added (light grey lines); TSV and package-induced stresses were added (thin blak lines).

9-1

# Overview of EUV Mask Metrology

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*[1] Intel Assignee to SEMATECH*

## ABSTRACT

Extreme ultraviolet (EUV) lithography is the successor to optical lithography and will enable advanced patterning in semiconductor manufacturing processes down to the 8nm half pitch technology node and beyond. However, before EUV can successfully be inserted into high volume manufacturing a few challenges must be overcome. Central among these remaining challenges is the requirement to produce "defect free" EUV masks.

Since 2003, EUV mask blank defects have been reduced from 10000 of size greater than 100nm to about a few tens at size 70nm. Unfortunately, today's state of the art defect levels are still about 10 to 100 times higher than needed. Closing this gap requires progress in the various processes associated with glass substrate creation and multilayer deposition. That process development improvement in turn relies upon the availability of metrology equipment that can resolve and chemically characterize defects as small as 30 nm.

SEMATECH's Mask Blank Development Center has been working since 2003 to develop the technology to support defect free EUV mask blanks. Since 2009 the defect reduction efforts have included an intense focus on inspection and characterization. The facility boasts nearly $100M of metrology hardware, including an FEI Titan TEM, Lasertec M1350 and M7360 tools, an actinic inspection tool (AIT, see Figure 1 for an image), AFM, SPM, and scanning auger capabilities.

This paper will describe SEMATECH's efforts to develop robust inspection of EUV mask defects. We will discuss the development of hardware and procedures for inspecting particles 70nm and smaller. Chemical characterization techniques will be described, including approaches to TEM imaging of mask lamella (see Figure 1) that have high yield as well as scanning auger analysis of 30nm defects. The talk will conclude by describing efforts to develop future hardware, including novel approaches to fund such infrastructure development.

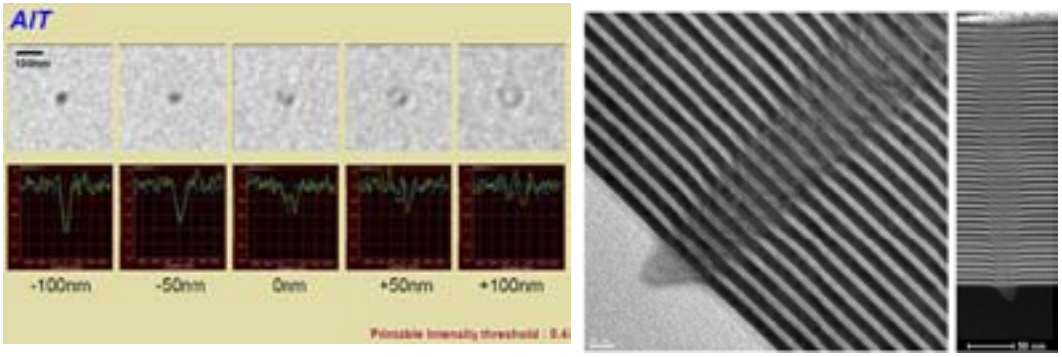


**FIGURE 1.** Shown here are images from SEMATECH Actinic Inspection Tool at Lawrence Berkeley National Laboratory (left) and TEM images from SEMATECH's FEI Titan installed at the College of Nanoscale Science and Engineering at the University at Albany.

# Hybrid Metrology & 3D-AFM Enhancement For CD Metrology Dedicated To 28 nm Node And Below Requirements

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## ABSTRACT

The measurement uncertainty is becoming one of the major components that have to be controlled in order to guarantee sufficient process quality and enough production yields for advanced technological nodes. Already at the R&D level, we have to cope up with the accurate measurements of sub-40nm dense trenches and contact holes coming from 193 immersion lithography or E-Beam lithography. Current production CD metrology techniques such as CD-SEM and OCD are limited in accuracy for various reasons (i.e electron proximity effect, outputs parameters correlation, stack influence, electron interaction with materials…). Therefore, time for R&D is increasing, process windows degrade and finally production yield can decrease. A new high volume manufacturing (HVM) CD metrology solution has to be found in order to improve the relative accuracy of production environment.

In this paper, we will present and discuss a new potential CD metrology solution so-called Hybrid CD metrology (HCDM) that smartly tuned various morphological data coming from different CD Metrology techniques. The final is to create added values to CD Metrology since we are at a time where if you can measure you can not manufacture. The final goal for "chipmakers" is to improve yield and save R&D and production costs through real-time feedback loop implementation on CD metrology routines. We will discuss in details one potential hybrid metrology solution through the 3D-AFM/CD-SEM couple. We will discuss about measurement uncertainty, new 3D-AFM tip design compatible with HVM, CD-SEM threshold algorithm optimization through reference metrology feedback loop. Example of applications will be shown with typical sub-40nm trenches measurements dedicated to advanced lithography process development that will demonstrate that we have succeed to push ahead the limit of the 3D-AFM and CD-SEM technologies in measuring the tight dimensions that would allow to continue its use for current and upcoming technology nodes.

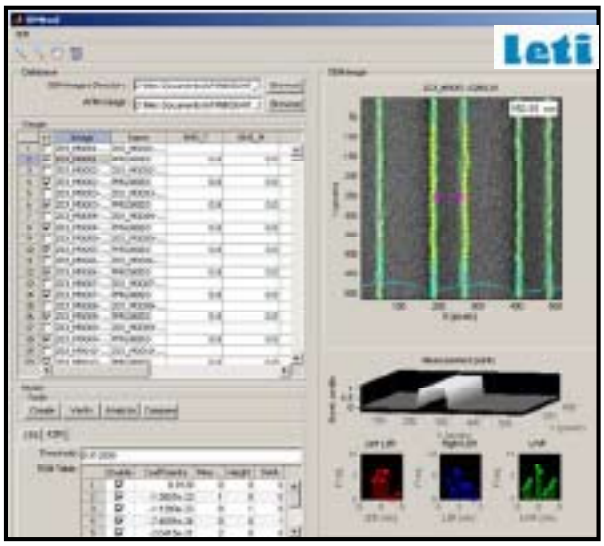


**FIGURE 1.** First LETI demonstrator of hybrid metrology software

Keywords: Hybrid metrology, reference metrology, 3DAFM, accuracy, precision, tip, carbon, CD-SEM

This work has been done in the frame of the Joint Development Program between ST/LETI/IBM

9-3

# Advances in CD-Metrology (CD-SAXS, Mueller Matrix based Scatterometry, and SEM)

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## ABSTRACT

Scanning Electron Microscopy (SEM) has been a mainstay of critical dimension (CD) metrology since the inception of integrated microelectronics, due to its inherent high resolution capability and relative ease of interpretation. However, as device dimensions continue to shrink, and non-planar devices become integrated into process flows (e.g., finFETs), the need to identify and develop successor technologies becomes essential. Here, we report progress on the development of two innovative technologies proposed for CD measurement, and assess their viability for high volume manufacturing applications. Finally, we describe recent efforts to extend the life of conventional CD-SEM.

Small Angle X-ray Scattering (SAXS) also offers Angstron-level resolution, is non-destructive, and requires no additional preparation steps. Performed in either transmission or reflection mode, this method is particularly suitable for arrayed structures and non-planar devices. Whereas direct imaging methods provide a complete description of a single measurement site, SAXS probes a comparatively large area containing many sites, and effectively provides information on feature dimensions and the statistical variations within the sampled. The chief limitation to implementing CD-SAXS is throughput, gated by x-ray source brilliance. Conventional x-ray tube and rotating anode sources do not have the correct combination of brightness and stability required to obtain rapid, consistent measurements. Recent innovations in x-ray source technology, including plasma and liquid metal based sources, have shown promise for making CD-SAXS a viable HVM method.

Scatterometry methods offer yet another attractive approach. Advances in the optical components and simulation software enable one to obtain most of the sixteen components of the Mueller Matrix for each wavelength of light instead of the typical $\Psi$ and $\Delta$. This is great importance when measuring highly anisotropic 3D scatterometry test structures.

Finally, it is worth considering the efforts to extend the life of CD-SEM. A series of advances such as drift correct frame averaging and 3D Monte Carlo models that improve metrology for nanoscale features are all under consideration. These improvements push CD-SEM resolution closer to its theoretical limits. Additionally, the use of contrast transfer functions (CTFs) as an improved means for achieving tool matching and assessing tool performance is considered. When an image is collected from an ideal test specimen, such as a high resolution Fresnel Zone Plate or a pseudo-random dot array, the CTF can be used as a measure of the fidelity with which specimen topography is represented in the recorded signal, as a function of spatial frequency. Tuning SEM parameters to manipulate the CTF provides a richer feedback mechanism than simply using nominal resolution and signal-to-noise ratio.

# Line Edge Roughness of Directed Self Assembled PS-PMMA Block Copolymers – A Candidate for Future Lithography

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## ABSTRACT

Directed self-assembled (DSA) block co-polymer (BCP) is a technology that combines lithographically defined features to guide self-assembled polymers by physical or chemical properties to create features smaller than those possible with conventional lithography. To semiconductor industry DSA presents a possible lithography solution beyond 22-16nm node where the targeted line edge roughness (LER) is 1.3nm or less. For DSA to become a viable solution the intrinsic LER of BCP has to be less than 1.3nm. Hitherto the LER of DSA block copolymers was measured mostly using SEM and AFM, hence the results represent only the top surface characteristics. In addition, the observed LER using SEM or AFM is often inferior to 1.3nm. The purpose of this work is to demonstrate the use of transmission X-ray scattering to quantify LER as well as the critical dimensions in BCP patterns created with DSA technique. Experimental results from polystyrene/ poly methyl methacrylate copolymer line gratings at 23nm half pitch will be preseted and the theoretical developments needed to extract LER from X-ray scattering will also be discussed.

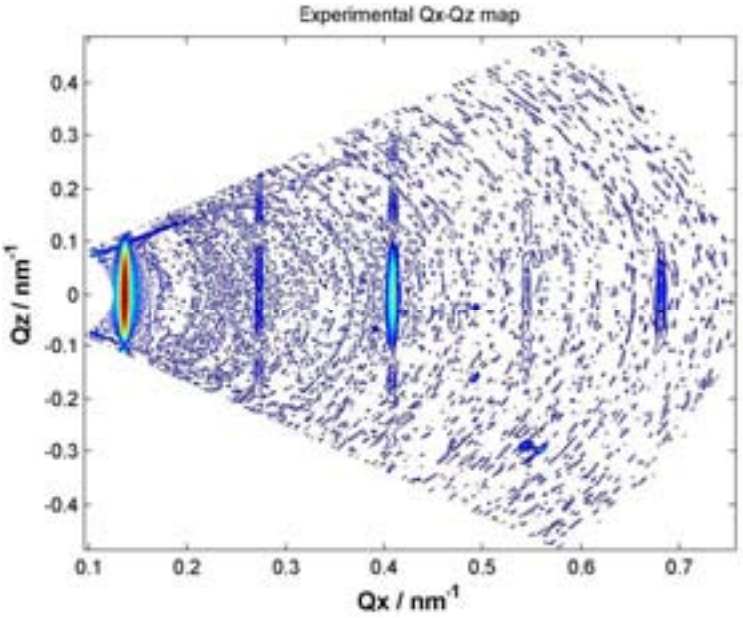


**FIGURE 1.** X-ray scattering results of a PS/PMMA line grating created with DSA technique with a half pitch of 23nm. The X-axis is perpendicular to the lines and the Z-axis is along the thickness direction.

10-1

# Fundamental Limits of Optical Patterned Defect Metrology

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## ABSTRACT

This presentation will explore different optical technologies for extending high throughput defect inspection beyond the 22 nm node. The semiconductor manufacturing industry is now facing serious challenges in achieving defect detection rates with acceptable throughput and accuracy. With conventional bright field and dark field inspection methods now at their limits, metrology tool developers are exploring alternative optical methods such as angle-resolved scatterfield microscopy, 193 nm short wavelength solutions and coherent illumination. In this paper we will explore angle and polarization resolved illumination, measurement wavelengths down to 193 nm and interference microscopy using electromagnetic simulations and laboratory apparatus.

We will evaluate performance gains using scatterfield microscopy techniques for die-to-die defect metrology on 22 nm node layouts. Scatterfield microscopy enables design-specific bright field optical tools for use in signal-based defect analysis of features with dimensions well below the measurement wavelength. Central to this approach is engineering the illumination as a function of angle and analysis of the entire scattered field. This methodology has been applied to defect inspection for various defect types on intentional defect array (IDA) wafers.

Theoretical simulations will be reported using a fully three-dimensional finite difference time domain (FDTD) electromagnetic simulation package. Comprehensive modeling was completed investigating angle-resolved and polarization-resolved illumination to enhance defect detection for a 13 nm linewidth logic-poly stack. Oblique incidence is compared against more conventional illumination. Angle and polarization resolved enhancements and defect sensitivity gains are identified and presented.

Comprehensive modeling to investigate a range of illumination wavelengths to enhance defect detection for several defect types has also been completed. Simulation results will be shown that evaluate performance gains obtained at wavelengths ranging from 193 nm to 450 nm. The data show that many defects are more detectable when using the shorter 193 nm or 266 nm illumination wavelength. However, an optimum wavelength between $\lambda = 193$ nm and $\lambda = 266$ nm cannot be identified without consideration of the process stack, materials, defect type and directionality, incident angle, and polarization. We will present 193 nm Scatterfield Microscope imaging results on an IDA 65 nm logic-poly stack. Experimental efforts are focused toward the validation of simulation results, essential for confirming and optimizing shorter measurement wavelength and oblique illumination performance gains for some process stacks and to provide direction for the extensibility of optical defect detectability.

This paper will also look at emerging approaches using interference microscopy. Recent results show that using optical interference techniques may be another avenue to improve sensitivity to defects. An FDTD model has been modified to allow rigorous simulation of interference microscopy applied to defects.

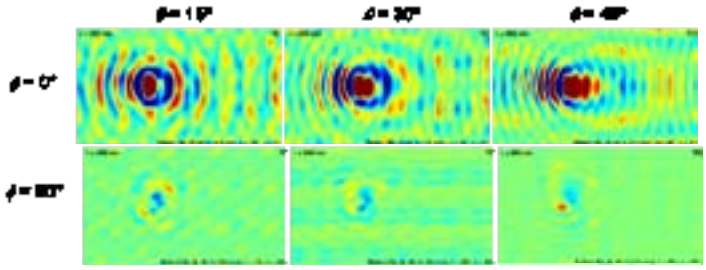

FIGURE 1. Simulated differential images for a 13 nm bridge defect as a function of incident angle for $\lambda = 266$ nm.

10-2

# Pattern Verification for the Sub-20nm Era

Wolf Staud

*Applied Materials*

## ABSTRACT

The industry has converged on EUV lithography as the most promising candidate to replace ArF for the 22nm half-pitch node and beyond. Alternatively, ML2 is being pursued as a more cost-effective solution, especially for smaller wafer volumes and prototyping.

Both technologies have their individual approaches and problems when it comes to mask and wafer inspection. ML2 however has the added complexity, that the ultimate pattern verification step, patterned mask inspection in D:Db mode is not possible.

A new approach and flow is needed.

At the same time, optical/DUV based Wafer Inspection is running out of resolution, just like DUV based lithography.

A promising new candidate is Electron Beam based Wafer Inspection. While it certainly has the resolution, and is a long proven technology, throughput is in general considered an issue.

In this talk we will summarize the studies and present results of developing solutions to EB based Wafer and Mask Inspection. We will take a special look at the requirements for pattern verification, the resolution and throughput needs, and the technological answers to these challenges. We will investigate the options for EB2M applications, and the sensitivities that can be achieved. The various configuration options for multi-beam approaches will be discussed.

In a final assessment we will look at the economics of MBEBI for wafer and masks, and the possible transparency of these inspections in both EUV and ML2.

# Positioning More Than Moore Characterization Needs and Methods Within the 2011 ITRS

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## ABSTRACT

The concept "More than Moore" was introduced in the 2005 edition of the International Technology Roadmap for Semiconductors (ITRS)[1], with the purpose to describe technology features that do not fit the miniaturization trends as implied by Moore's Law. These features typically enable non-digital functionalities, such as wireless communication, power management, sensing and actuation. As these new functionalities are progressively being incorporated into system-in-package (SiP) and system-on-chip (SoC) formats, the complexity of the resulting microsystems is rapidly increasing (Fig. 1.). Consequently, there is a need for new sets of physical parameters and figures of merit for the characterization of emerging technology options in the More than Moore domain. Recently, the International Roadmap Committee (IRC) of the ITRS has proposed a methodology to address this subject[2].

The paper will discuss the characterization requirements in the More than Moore domain, as they are identified in the 2011 edition of the ITRS. The analysis starts with the system needs emanating from the various application fields, which have to be translated into functional requirements and device characteristics. This enterprise is by nature multi-disciplinary, involving expertise from the industrial as well as the scientific communities. The technological and scientific challenges that have to be explored include heterogeneous process integration, multi-scale device engineering and design for reliability. All these require new approaches in characterization.

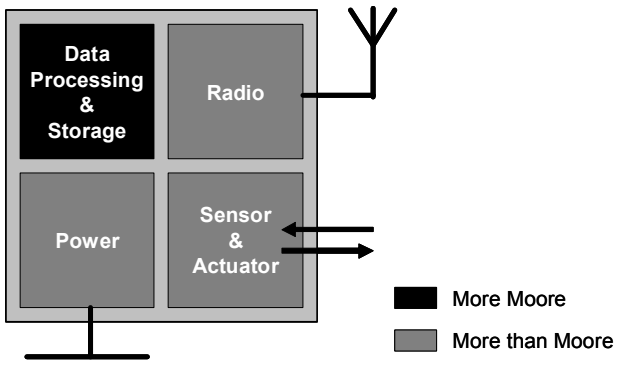


**FIGURE 1.** A typical microsystem incorporates "More Moore" and "More than Moore" subsystems.

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# Measurements and Standards to Characterize More than Moore Applications of Electronics: Perspectives from IEC

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## ABSTRACT

It is a common understanding that nanotechnology is one of the key technologies of the 21st century. Therefore governments and companies are investing an enormous amount of money in research and development to participate on the expected commercial success with nano-enabled products. Within the electrotechnical industry nanotechnology became important due to the miniaturizing of microelectronic devices driven by Moores Law. Typical structures have been reached dimensions well below 100 nm coming closer and closer to the physical and technical limit which is somewhere slightly below 20 nm. Nevertheless there are only a limited number of electrotechnical products in the market where the functionality of the product is based and inherently coupled to the use of nanomaterials and nanoprocesses. The lesson learned especially from the microelectronic industry is that standards play a critical role for the utilization of research results for commercial purposes. Therefore the International Electrotechnical Commission (IEC) has established the cross sectional technical committee IEC/TC 113 "Nanotechnology standardization for electrotechnical and electronic products and systems". Within the scope of this committee are the nanotechnology aspects within the broad range of technical areas where IEC is the responsible Standards Development Organization (SDO). IEC/TC 113 develops standards along the whole fabrication value adding chain and covers the complete life cycle of the product from fabrication to its end-of-life. Actually the main focus is on nanofabrication including standards on Key Control Characteristics (KCC), material specifications, nanomanufacturing processes and equipment as shown in figure 1. Examples of product groups addressed are nanoenabled batteries, photovoltaic cells, lightning devices and printed electronics.

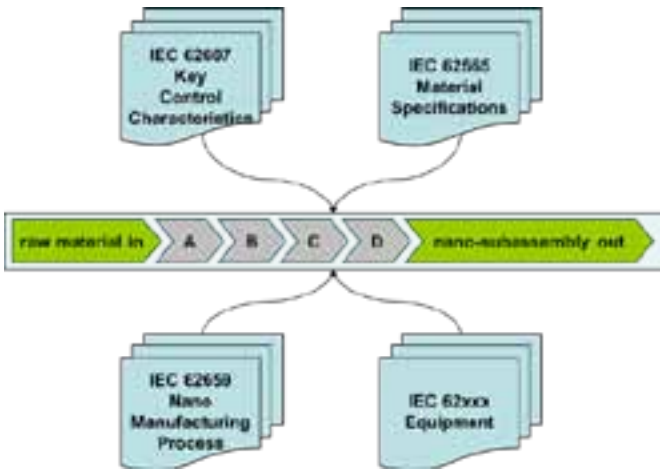


**FIGURE 1.** Standards regarding nanomanufacturing processes and equipment, material specifications and key control characteristics supports high quality fabrication of nanoenabled electrotechnical products.

11-3

# Thermal Properties Characterization of Advanced Materials Application to Nanoelectronics

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## ABSTRACT

Energy transport is fundamental to both improving our understanding of basic material properties and advancing the intelligent design of new and more optimally functional materials. Energy transport is mediated by various particles and their subsequent interactions, including electrons, photons, phonons, plasmons, spinons, and excitons. The precise nature of any material determines which of these are most important. A more complete understanding of materials currently in development is of critical importance for a wide range of applications ranging from energy harvesting photovoltaics and thermoelectrics to next generation molecular electronics and mechanisms of material failure in nanoelectronics. Currently, there are a number of unanswered questions that are impeding the advancements of many important real-world applications, including the development of green technologies. Our research goal is to answer some of these questions. For example, how does nano-structuring --- such as changes in dimensionality, layering, and nano particle impregnation --- change energy transport characteristics? What effects do chemical and structural modifications on the near-field scale have on far field measurements of energy transport? Is it possible to decouple electronic and thermal transport in materials? What is the source of heat generation in nano electronics systems? The goal of this work deals with the design of materials with more precise and efficient control of energy transport by managing thermal properties of those systems or make them work to our advantage.

Currently, pump-probe spectroscopy is being successfully applied to energy transport measurements using techniques such as picosecond acoustics and time domain thermal reflectance with high temporal resolution [1]. These measurements, however, are limited by the diffraction to half the wavelength light. Quasiparticle excitations such as plasmon- [2] and phonon-polaritons [3,4l] dominate near field, sub-wavelength effects, and high spatial resolution is required to probe them. Scanning-probe microscopy offers high spatial resolution and local probing of near field effects, but is wanting of temporal resolution.

We will present different experimental approaches to measure thermal properties of nano structured materials taking example such as Nano-particles, nano wires, super-lattices, and thin films.

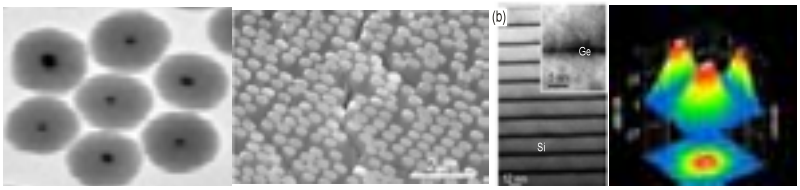


**FIGURE 1.** Different nano materials, from left to right: Nano particles, nanowires, super-lattice, picosecond snap shot of thermal field upon a nano layer.

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# Frontiers of More than Moore in Bioelectronics and the Required Metrology Needs

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## ABSTRACT

Silicon's intersection with biology is a premise inherent in Moore's prediction. However, to realize this prediction, two grand challenge problems must be addressed - the biocompatibility of synthetic materials within the human body and the interfacing of solid state micro- and nano-electronic devices with the electronics of biological systems. Our center has concerned itself with these two grand challenge issues. We have sought to address these challenges through the exampled development of an implantable biochip for the measurement of physiological stress markers during trauma induced hemorrhage [1]. A fully implantable and rapidly deployable biosensor system for the measurement of lactate, glucose, pH, and oxygen with telemetered reporting of physiologic status is under development. Such a device is relevant for battlefield casualty care and management, mass casualty triage decision making, and of course, civilian trauma. The device can be rapidly administered to the hemorrhaging patient by a first responder, medic or EMT, to allow accrual of critical physiologic data to be used by the far-forward or emergency room trauma surgeon.

To address the needs of the system, we have developed soft, condensed, biomimetic but otherwise inherently electronically conductive materials to address the challenge of interfacing solid state devices with the electronics of the body, which is predominantly ionic [2]. These electroconductive hydrogels offer the potential for biocompatibility while sustaining electrical fidelity across the biological-to-solid state interface. We have developed nano-templated interfaces via the oriented immobilization of single walled carbon nanotubes (SWCNTs) onto metallic electrodes to engender reagentless, direct electron transfer between biological redox entities and solid state electrodes [3]. We have developed processing techniques to alter the time scale of assembly of large biomolecules such as enzymes and nanomaterials such as SWCNTs [4].

In addressing these challenges, metrology needs and opportunities are found in such widely diverse areas as single molecule counting and addressing, sustainable power requirements such as the development of implantable biofuel cells for the deployment of implantable biochips, and new manufacturing paradigms to address plura-biology needs on solid state devices.

*Keywords:* bioelectronics, nanometrology, biosensors, biochips, biointerfaces

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TH-1

# Ultimate Backside Sample Preparation For Ultra Thin High-k/Metal Gate Stack Characterization

M. Py[1], M. Veillerot[1], E. Martinez[1], J.M. Fabbri[1], R. Boujamaa[1, 2], and J.P. Barnes[1]

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Over the past decade it has become increasingly common to resort to backside analysis to overcome weaknesses such as ion mixing and preferential sputtering in SIMS depth profiling,[1-3] and to bring the layer of interest as close as possible to the surface for XPS analysis. However backside analysis remains challenging since only a fraction (~20 nm) of the 750µm thick silicon substrate must remain while maintaining a smooth and flat surface suitable for analysis. Recent developments have used Silicon on Insulator (SOI) substrates where the buried thick (145nm) $SiO_2$ is used as an etch stop layer.[4]

Here we present a backside sample preparation method adapted to samples with an extremely thin etch stop layer. It consists in a two step preparation: a mechanical polishing up to a few remaining microns, followed by a dedicated TMAH etch. This method yields an extremely flat and smooth surface, without remaining silicon after preparation (see Figure 1). We therefore used it to prepare two samples consisting of a high-k/metal gate stack for 32 nm node CMOS devices, before and after activation anneal. On these samples the etch stop layer is materialized by a 1.5 nm thick SiON layer (structure on Figure 1). This preparation therefore allowed precise analysis of the behaviour of different elements in the stack upon annealing with ToF-SIMS and XPS. The results of the different analysis will be discussed and compared with conventional ones (i.e. frontside analysis). We will point out the improvements brought by the preparation as well as some typical features of the studied stacks upon annealing.

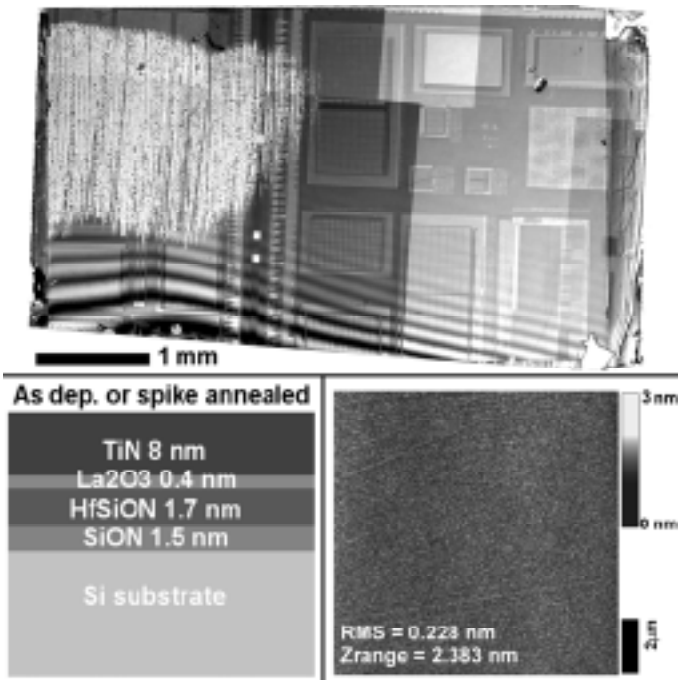


**FIGURE 1.** [Top] Optical image of a sample after backside preparation. Except on the top left corner of the sample, there is no silicon left. Patterns on the surface of the support wafer are seen by transparence through the layers of interest (~12 nm) and the glue (~1-2µm). [Bottom left] Schematic structure of the samples studied in this work. [Bottom right] Topography of the surface of the sample after preparation.

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**Acknowledgments**: This work was partially supported by the European EUREKA/CATRENE program in the frame of the CT206 UTTERMOST project.

*Keywords:Backside analysis, ToF-SIMS, XPS, High-k*

# Elemental Depth Profiling Of Ultra Thin High-k Material Stacks By Full Spectrum ToF-SIMS And LEIS

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[3]*ION-TOF GmbH, Heisenbergstr. 15, 48149 Münster, Germany*

The Microelectronics technological nodes at 32 nm and below require extreme dimensional scaling which is impossible to obtain with classical materials for CMOS integration. High-k materials, with their reduced EOT, are considered as one of the answers to this problem.[1] However, the electrical properties of the final High-K / Metal Gate devices greatly depend on the stoichiometry and on the in-depth distribution of the high-k layer constituent elements.[2] Accurate concentration depth profiling of these materials is thus essential. In this work we investigate the feasibility of a quantitative depth profiling with Time of Flight Secondary Ion Mass Spectrometry (ToF-SIMS) and Low Energy Ion Scattering (LEIS). SIMS or ToF-SIMS characterization of high-k material stacks is usually hampered by matrix effects.[3] Here, we use a Full Spectrum protocol for ToF-SIMS data acquisition and treatment which reduces matrix effects and allows simultaneous quantitative profiling for all matrix elements.[4-5]

Three samples were prepared on Si substrates and studied with the CEA-Leti TOF.SIMS 5 instrument, and with a Qtac LEIS instrument, both from ION-TOF GmbH. Each sample is representative of different steps in the elaboration of a typical high-k stack: first a thin SiON(1.5 nm) layer, then an HfSiON(1.7 nm)/$SiO_2$(1.2 nm) stack, and finally an HfSiON(1.7 nm)/SiON(1.5 nm) stack. $SiO_2$ is formed by oxidation of the silicon substrate with in-situ steam generation at 1025°C and hafnium silicate is deposited by MOCVD. Nitridation of both pedestal $SiO_2$ and hafnium silicate are carried out by a plasma nitridation followed by a 1000°C Rapid Thermal Anneal.

An example of complete high-k material stack quantitative profiling by ToF-SIMS is shown in figure 1. The ToF-SIMS profile seems accurate since it yields a material composition of $Hf_{0.6}Si_{0.38}O_{1.7}N_{0.31}$, in agreement with the nominal specifications. However, only the comparison of the results obtained with both instruments will allow us to draw conclusions on the accurate in-depth composition of these stacks. Profiles are thus compared and both instruments accuracy is assessed. The typical features of each technique in terms of depth resolution, sensitivity and depth of information are also investigated.

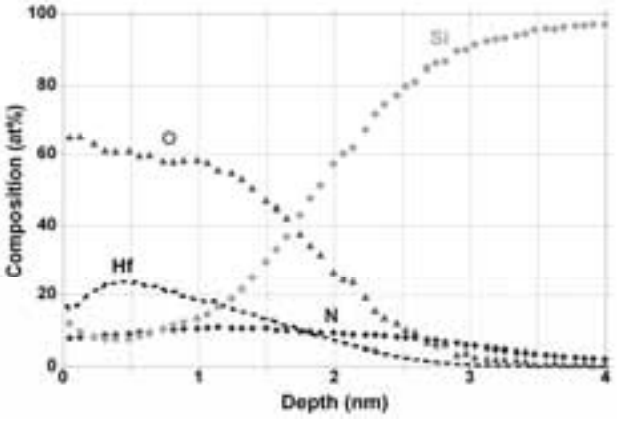


**FIGURE 1.** Full Spectrum ToF-SIMS profiles of an HfSiON(1.7 nm)/SiON(1.5 nm) stack deposited on Si.

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**Acknowledgments**: This work was partially supported by the European EUREKA/CATRENE program in the frame of the CT206 UTTERMOST project.
*Keywords: ToF-SIMS, LEIS, High-k*

TH-3

# Establishing SI Traceability for Scatterometry

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## ABSTRACT

Scatterometry, sometimes referred to as optical critical (CD) dimension metrology, combines reflectometry or ellipsometry with electromagnetic simulations to measure dimensions of features in periodic structures. Optical scatterometry has become an attractive tool for dimensional metrology in the semiconductor industry, due in large part to its inline potential for providing critical feedback information necessary for tight process control. Unlike atomic force microscopy (AFM), which measures the dimensions of a target by physically contacting it, scatterometry measures those dimensions by obtaining an optical signature and comparing that signature to a theoretical parametric model. Until recently, however, little attention has been given to establishing absolute accuracy for optical scatterometry.

I will discuss the development of an independent uncertainty budget for optical scatterometry, an important step toward establishing traceability to the International System (SI) meter. One of the key developments has been a methodology for propagating systematic uncertainties and signal noise through a regression analysis. The regression analysis optimizes a set of floating parameters (e.g., CD, side wall angle, and height) under a set of fixed assumptions (e.g., optical constants and instrument conditions). A scatterometry sensitivity analysis program, OCDSense, has been developed that implements this methodology for any grating structure and measurement scheme. OCDSense propagates the noise in the reflectance measurement and the uncertainties in the fixed parameters (assumptions) to the covariance matrix of the floating parameters. Uncertainties in incident angle, wavelength, finite target size, roughness, beam focusing, channel cross-talk, and radiometric accuracy also contribute to the measurement uncertainty, and to some extent, these uncertainties can be included in OCDSense as well. Ultimately, an uncertainty budget for line profile needs to specify not just uncertainties in a single number (such as CD or sidewall angle), but an uncertainty in the profile function. Figure 1, below, shows a set of profiles that are consistent with the uncertainty covariance for a virtual measurement. An uncertainty budget for a specific scatterometry measurement of a silicon trench grating will be presented.

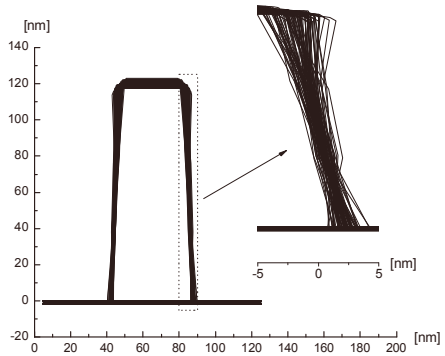


**FIGURE 1.** Example of a scatterometry uncertainty analysis yielding an ensemble of profiles consistent with measurement uncertainties. The inset expands the horizontal scale within the dashed rectangle to better view the various profiles.

Keywords: Scatterometry, Traceability, Optical Critical Dimension Metrology

# Evaluation of Metal Etches on Unpatterned Wafers Using Surface Haze Measurements

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## ABSTRACT

Laser light scattering is an extremely useful metrology tool for detecting process defects with both high sensitivity and high wafer throughput on unpatterned wafers[1]. In addition to capturing the higher spatial frequency components (i.e. defects), the low spatial frequency background scatter signal (i.e. haze) can also be leveraged for better yield learning about new processes. This background haze signal is sensitive to local changes in surface reflectance and roughness, thereby making haze useful for characterizing film properties such as composition, morphology or thickness over the entire wafer surface[2].

Here we describe a series of experiments aimed at optimizing a metal etch process on unpatterned wafers across a skew of process parameters. During the course of the investigation it was found that though the defect signal could discern some information about the etch residue removal efficiency, it could not be used to conclusively distinguish between non/partial/total etches of the metal. In contrast, by using surface haze data we were able to show a very clear distinction between the various wafer states, even when the defect signal was itself ambiguous (see Figure 1 below). Thus accurate and rapid characterization of etch skews was achieved by utilizing the surface haze signal (both within wafer and wafer-to-wafer) as a metric for etch quality, leading to an efficient optimization of the etch process in question.

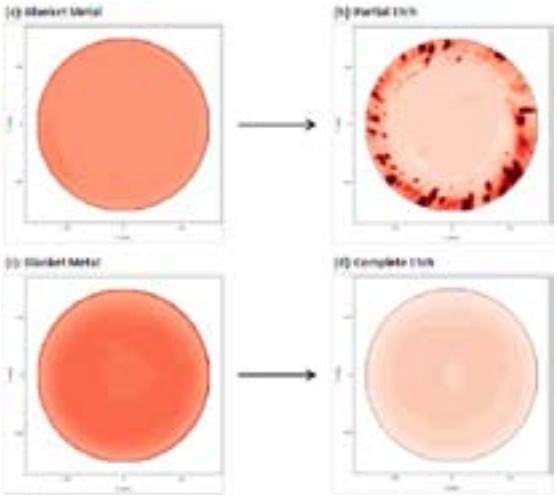

**FIGURE 1.** Example of (a-b) partial etch and (c-d) full etch surface haze maps showing high contrast on remaining residues. Areas of red correspond to regions of higher surface haze compared to the white regions.

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**Keywords: Surface Haze, Scattering, Etch**

# Microwave Characterization of Transparent Conducting Films

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## ABSTRACT

The high frequency conductivity of thin metallic and graphitic nano-films attracts interest due to many potential applications in spin electronics, electromagnetic shielding, flexible antennas, displays, and in solar cells. Surface morphology of thin conducting nano-films typically consists of an isolated clustering structure, which can evolve into a conducting percolated network [1]. The high frequency conductance of such materials is not well understood. We present measurements of microwave conductivity of thin optically transparent films in a coplanar waveguide (CPW) configuration [2]. Fig. 1 shows a signal flow graph of a two port microwave network representing a section of CPW with a conducting thin film specimen. The CPW outside the specimen section has a real characteristic impedance $Z_0$, while the material's properties in the specimen section are represented by the complex impedance $\boldsymbol{Z}_s$ that depends on the reflection ($\Gamma$) and transmission ($e^{-\gamma l}$) coefficients; propagation constant ($\gamma$) and propagation length ($l$). We determine the relation between the experimentally measured scattering parameters ($\boldsymbol{S}_{11}$) and ($\boldsymbol{S}_{21}$), complex impedance ($\boldsymbol{Z}_s$) and propagation constant ($\gamma$) for the CPW test structure through a signal flow graph method. Once the signal flow is solved for $\gamma$ and $\boldsymbol{Z}_s$ , then the conductance $G_s$ and the capacitance $C_s$ of the specimen can be determined from conventional transmission line relations.

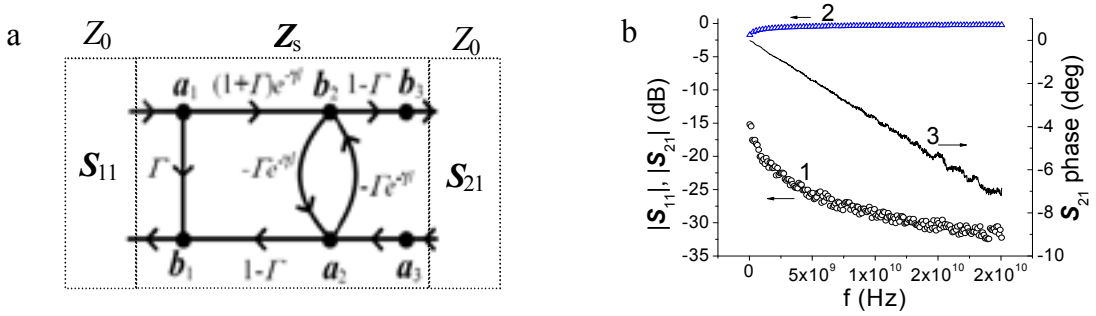


**FIGURE 1.** a- Signal flow graph of CPW. b- Scattering parameters for Au film. (1)-$|\boldsymbol{S}_{11}|$, (2)- $|\boldsymbol{S}_{21}|$ and (3) - phase of $\boldsymbol{S}_{21}$..

Measurements are carried out on CPWs with a characteristic impedance of 50 Ω and a propagation length ranging from 450 μm to 3600 μm, which are patterned on alumina substrates by lift off lithography.

The measured phase angle of $\boldsymbol{S}_{11}$ (not shown) oscillates between ± 180° in the corresponding frequency range. In comparison, $|\boldsymbol{S}_{11}|$ of the empty reference CPW was measured to be about –60 dB ($\Gamma \approx 0$), while $|\boldsymbol{S}_{21}|$ was in the range of 0 dB ($e^{-\gamma l} \approx 1$). The conductance of the film decreases considerably with increasing frequency from about 50 S/m at 1 GHz to about 10 S/m at 20 GHz. The presented results are general and applicable for characterization of electrical properties of thin nanostructured films at microwave frequencies.

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**Keywords:** Thin Films; Microwave Conductance; Coplanar Waveguides;

# The Impact Of Organic Contamination On The Oxide-Silicon Interface

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## ABSTRACT

In this work, we carried out a set of experiments to investigate the impact of organic contamination on the electrical properties of the oxide-silicon interface. Some wafers were contaminated by immersion in solution of diethylphthalate in solvent. The wafers were then oxidized to perform surface recombination velocity measurements by Elymat, and capacitors were fabricated for capacitance vs. voltage and capacitance vs time measurements. In addition, the interface state density was measured by the MOS-DLTS technique and the gate oxide integrity was evaluated by constant current stress.

Elymat measurements of surface recombination velocity show that surface recombination velocity is increased by organic contamination (see fig. 1). Strong non-homogeneities are observed in contaminated wafers.

Vice versa no impact of organic contamination could be detected on oxide charge and surface generation velocity by capacitance vs. voltage and capacitance vs. time measurements.

From the point-of-view of the intrinsic properties of the oxide-silicon interface, MOS-DLTS showed the most significant effects, in that these measurements allowed identifying a band of interface states located around $E_v$ +0.1 eV as related to organic contamination (see fig. 2). Large within-wafer variations were observed by MOS-DLTS, consistently with Elymat maps of surface recombination velocity.

However, the most relevant effects of organic contamination were observed by electrical stress of the oxide. Indeed, the fraction of capacitors with degraded breakdown voltage increased dramatically in contaminated wafers (see fig. 3).

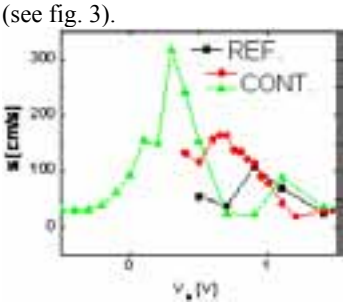



**FIGURE 1.** Surface recombination velocity s as a function of the surface voltage $V_s$ in reference and contaminated wafers.

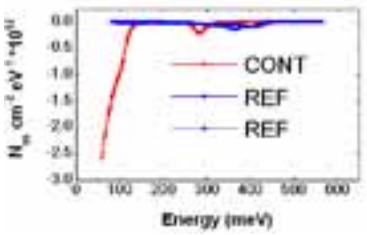
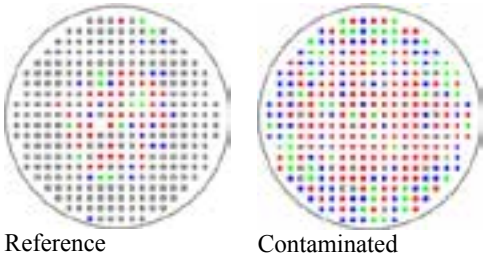



**FIGURE 2.** MOS-DLTS spectra of reference and contaminated samples.



Reference Contaminated

Failed at 9.5 MV/cm Failed at 10.6 MV/cm
Failed at 12 MV/cm

**FIGURE 3.** GOI maps of reference and contaminated samples.

**Keywords:** Organic Contamination, MOS-DLTS, GOI

**Acknowledgements.** This work was partially supported by the European Commission under the FP6 Program through the Integrated Infrastructure Initiative "ANNA" contract n. 026134-RII3.

# Reliability Testing of Advanced Interconnect Materials

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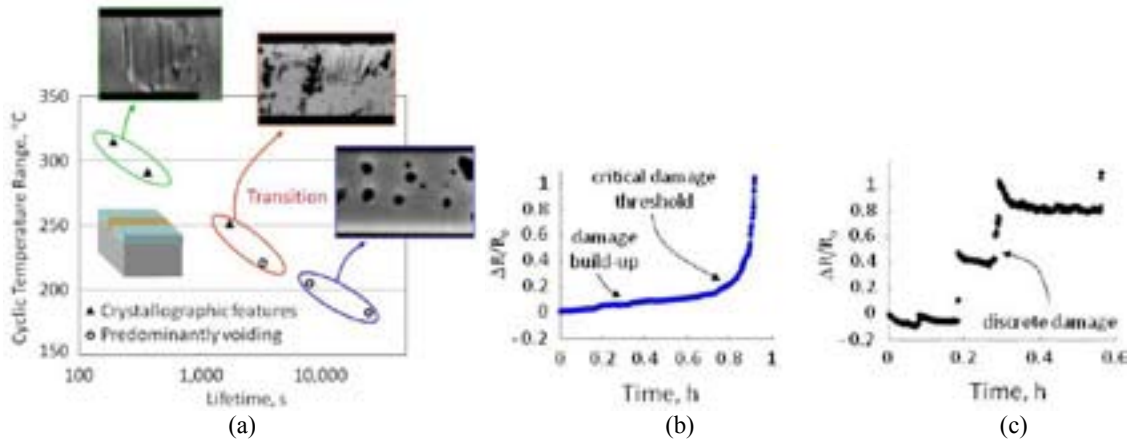
## ABSTRACT

We describe the development of electrical test methods to evaluate damage that determines reliability in advanced, small-scale conductors, including damascene copper and aligned carbon nanotube networks. Rapid thermal cycling induced during high-current AC stressing provides a means for measuring lifetimes associated with cyclic plasticity and/or diffusive damage in damascene copper. The specific type of damage that develops depends on the line geometry and the nature of the stress state induced within the lines during cycling. Voids form in both fully passivated and partially passivated lines under high levels of hydrostatic tension. Dislocation activity takes place in partially passivated lines in the presence of high shears, as shown in figure 1 (a). Effects of AC damage on subsequent electromigration tests will also be shown, including the observation that approximately 1/3 of voids created during AC stressing move under subsequent DC stressing conditions.

High-current DC stressing provides a means for evaluating the fabrication quality of aligned carbon nanotube (CNT) networks, in what we believe to be the first lifetime degradation tests of such materials. While classic electromigration is unlikely in nanocarbon, we observed through resistance changes two forms of degradation that we believe are tied to the nanotube packing and resulting conduction path density through the network, as shown by the resistance degradation plots in figures 1 (b) and 1 (c). The structure tested in figure 1 (b) shows a gradual build-up of damage, and that in figure 1 (c) shows a more discretized form of damage accumulation, which may tie to sudden changes in network morphology due to stressing. We also discuss the utility of measuring the initial rate of resistance change as an indicator of the ability of a CNT array to sustain DC stressing for an extended period.




(a) (b) (c)

**FIGURE 1.** (a) Lifetime plot for damascene copper subjected to rapid thermal cycling by high-current AC stressing. (b) Resistance degradation plot for CNT networks, showing gradual buildup of damage. (c) Resistance degradation plot for CNT networks, showing discretized buildup of damage.

# Measurement of Nanograin Orientations: Application to Cu Interconnects and Nanoparticle Phase Identification

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## ABSTRACT

Today, orientation maps of polycrystalline material are necessary for a better understanding of, for example, the formation of voids in the interconnects modern electronic devices. In this context, EBSD (Electron BackScattering Diffraction) has proved to be a powerful tool to measure grain orientation, but its spatial resolution is limited at the best to a diameter of about 10 nm. As new generations of devices have dramatically reduced in size, new tools are required to meet these spatial resolution specifications.

In this work the NanoBeam Electron Diffraction (NBED) coupled with the ASTAR system is used to obtain orientation maps. The ASTAR system is an automatic crystallographic orientation indexing tool developed for the transmission electron microscopes [1]. It can operate using the precession diffraction mode to provide quasi-kinematical patterns. Experiments were performed on two different microscopes: a JEOL 2010 FEF with a FEG (Field Emission Gun) and a JEOL 3010 equipped with a LaB6 filament. With these respective microscopes, diffraction patterns using a beam size of 3 nm (JEOL 2010 FEF) and 10 nm (JEOL 3010) can be achieved and indexation of grains or nanoparticles around 10-20 nm can be obtained.

Orientation maps obtained with different configurations (microscopes, voltage, camera length, with and without precession) will be compared. Two studies will be presented: the first one deals with polycrystalline copper interconnections as used in the 45nm technological node, the second one, illustrates the phase identification in nanoparticles.



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**Key words: TEM precession scanning, Cu interconnect, phase identification**

# Characterization and Failure Analysis of 3D Integrated Systems using a novel plasma-FIB system

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## ABSTRACT

Today 3D integration based on TSV's is a well accepted approach to further improve Integrated Circuits in terms of miniaturization, performance, power consumption and heterogeneous integration [1]. However, 3D integration comes with the introduction of many new processes and materials that may affect behavior and reliability of the overall system [2]. Therefore, there is a strong demand for physical characterization and failure analysis and more explicitly, also for tools and techniques that allow for easy chip access, navigation to the site of interest and that can provide physical information at the nm scale within a field of view of up to 100 x 100 $\mu m^2$.

In the framework of the European project JEMSIP-3D, a novel plasma-FIB (Focused Ion Beam) platform has been developed and evaluated by the project partners. This new platform has been characterized in terms of mill rates, resolution and ion assisted CVD kinetics and effective methods have been developed to suppress the curtaining that may appear on X-sections due to variations in material milling rates. The plasma-FIB platform has also been used to analyze failures of 3D integrated systems caused by TSV formation and the permanent bonding process. Figure 1 shows the application of the novel FIB analysis technique on a 3-layer stacked device with cross-sections of the areas of interest (IMC bond, TSV). Compared to classical FIB systems, the new equipment allows removing material significantly faster while maintaining good resolution at low beam currents, important for the subsequent analysis. The characteristics and merits of the novel plasma FIB platform and the resulting failure analysis will be discussed in detail.

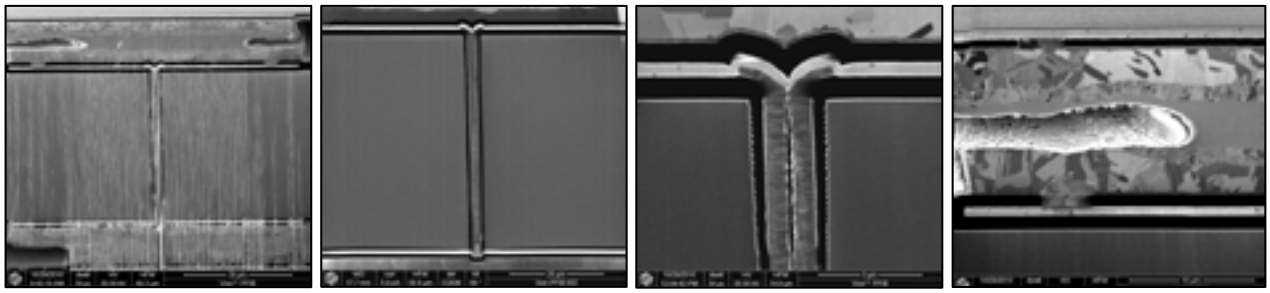

**FIGURE 1.** Plasma-FIB based analysis of the 3 level stacked device. Left to right: "curtaining", clean section, ICV, IMC bond.

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*A part of the work has been performed in the project JEMSiP-3D, which is funded by the Public Authorities in France, Germany, Hungary, the Netherlands, Norway and Sweden, as well as by the ENIAC Joint Undertaking.*

# FIB/SEM Structural Analysis Of Through-Silicon-Vias

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## ABSTRACT

3D integration of electronic circuits allows to overcome the interconnect performance limitations and to introduce heterogeneous integration of various device technologies. In the 3D stacked IC's the connection between the dies is made with Cu filled 'through silicon vias' (TSV's). Typical dimensions are 25-50 µm depth and 5 µm diameter. For the development of the TSV processing a control of the filling quality is necessary, while for stacked dies the major interest shifts to the study of the bonding quality. Dual beam focused ion beam / scanning electron microscopy is an important method for the structural characterization (Cu filling, Cu grain size, bonding) of TSVs. Due to the large dimensions, the analysis time is however very long.

Different milling strategies that can be applied to optimize the milling conditions will be discussed. To keep the total analysis time acceptable, relatively high beam currents need to be used, generally also in the final milling steps. Due to the large milling depth and the differences in milling rate of the various materials (Cu, Si, $SiO_2$ liner, TaN barrier, voids) curtaining artifacts can be severe under these conditions and in particular at the bottom of the TSVs the curtaining can complicate the interpretation of the images. Ways to minimize these artifacts or to move the artifacts to positions where they are less harmful for the interpretation of the images will be discussed.

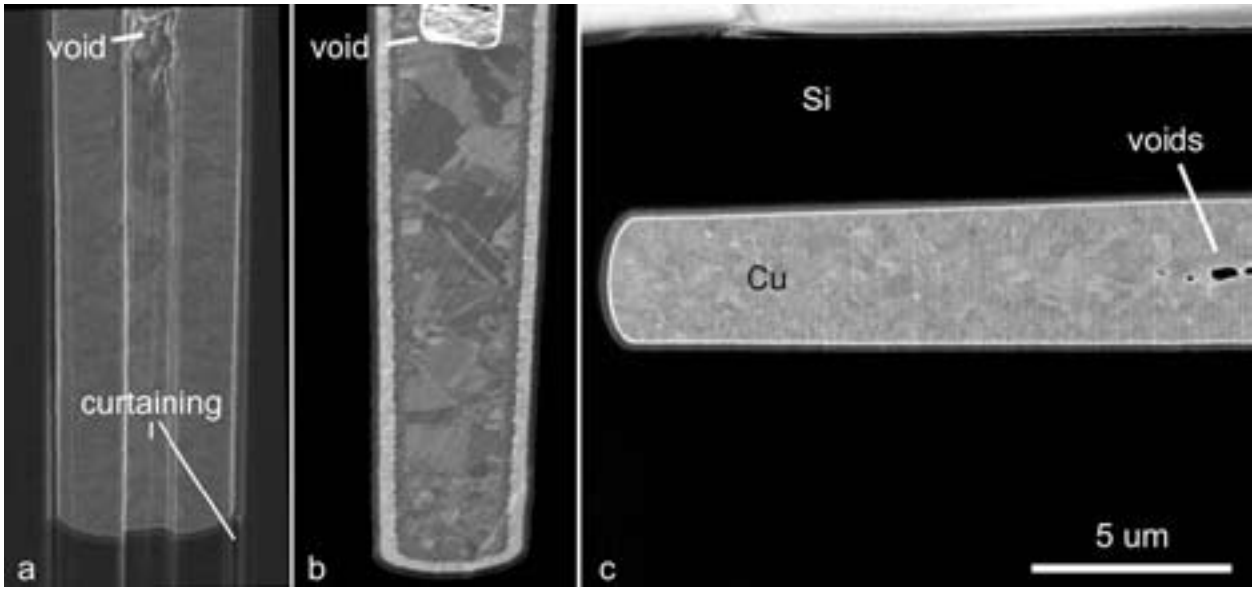


**FIGURE 1.** SEM images of the bottom of 50 µm deep TSVs a) milled with the standard procedure resulting in strong curtaining artifacts, b) final milled under an angle relative to the TSV axis, and c) milled orthogonal to the TSV axis so that the curtaining lines are strongly suppressed.

# Analysis of the Noble Metals on Silicon Wafers by Chemical Collection and ICPMS

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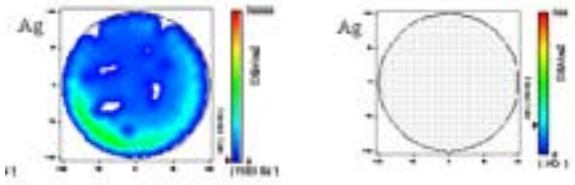
## ABSTRACT

Recent technological evolutions in advanced microelectronic, in heterogeneous integration or in MEMS technologies have led to an increase of materials present in manufacturing clean rooms leading to new risks of wafers contamination [1,2]. Among these new elements, noble metals (Pt, Au, Ag, Pd, Ru, Os, Rh, Ir) represent high detrimental impact risks for wafers which imply their mandatory control on the wafer surfaces at lower levels than 1E11 at/cm² [3].

Currently, only the TXRF technique allows the measurement of noble elements with a relative good sensitivity (up to few E10 at/cm² range) but also with significant uncertainties (15%-100% depending on levels). Usual sensitive (up to E7-E8 at/cm²) and accurate (~20%) analytical techniques of metallic contaminants based on a chemical collection followed by their analysis with Atomic Absorption Spectroscopy (AAS) or Inductively Coupled Plasma Mass spectrometer (ICPMS) are not applicable for noble metals due to their high oxido-reduction potentials. Indeed, HF Vapor Phase Decomposition-Droplet Collection (VPD-DC) is inefficient whatever their chemical form (metal as ionic) [4] whereas Liquid Phase Decomposition with diluted HF (LPD) can be applied only to the collection of ionic species on thick silicon oxide surfaces.

In this paper, we have addressed the measurement of noble metals by a chemical collection coupled to ICPMS analysis. To achieve this goal, chemistries have been selected depending on elements and implemented on wafer by a liquid phase collection. The technique development was focused on Au, Ag and Pt noble metals and, was evaluated in terms of collection efficiency, low limit of detection and repeatability from intentionally contaminated wafers. Both ionic and metal forms of the contaminants have been studied through different voluntary contamination modes of wafers: spin-coating method (ionic form), electroplating method and Physical Vapor Deposition processes (metal form). The liquid phase collection and ICPMS analysis method developed leads actually to reach low limits of detection close to 1E10 at/cm² and good collection efficiencies (>90% for Ag and Au; Pt on going) as illustrated by TXRF measurements presented in Fig.1 for silver




*Before: Ag at 7.6E13 at/cm²* *After: Ag <3E11 at/cm²*

**FIGURE 1.** TXRF mappings of an Ag intentionally contaminated wafer by a physical vapor deposition before (left) and after (right) the liquid phase collection step.

**Keywords:** VPD-DC-ICPMS, LPD-ICPMS, gold, silver, platinum.

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TH-12

# Mechanism of haze formation on 193 nm photolithographic reticules: $SO_2$ contamination on Cr

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## ABSTRACT

Haze contamination and crystal growth on 193 nm reticules is a widespread problem of advanced semiconductor manufacturing plants. This contamination leads to significant losses caused by wafer yield drop, shortened mask lifetime, etc. These progressive defects appear on all surfaces found on the mask, just as well on the Cr or MoSi pattern-side as on the quartz back-side [1,2]. Haze is created from surface contaminants (cleaning residues, airborne molecular contaminants, …) that photo-chemically evolve under deep UV light and water vapor to form crystals [3,4,5]. Ammonium sulfate haze represents the first concern and, since sulfate-free cleanings are used by mask manufacturers the major root causes is expected to come today from airborne dioxide sulfur ($SO_2$) and ammonia ($NH_3$). The growth mechanism as well as the thresholds of air concentration are still undetermined.

In this work an intentional contamination study of Cr surfaces with airborne $SO_2$ has been carried out. Surfaces were prepared by deposition of Cr metal layers (100nm) by DC-PVD on silicon wafers. XPS and XRR measurements were carried out to confirm that these films were representative of actual Cr mask surfaces. Contamination was performed by exposure of thermally Cr coated-wafers to controlled concentrations of $SO_2$ in the gas phase generated from dilution with clean wet air. Exposure concentration (from 10ppbv to several hundred ppbv) and time (up to 24h) were varied as experimental parameters. Amounts of $SO_2$ and other inorganic contaminants deposited on the surface were characterized by Ionic Chromatography. A typical kinetic curve of contamination is given in fig.1. XPS and ToF-SIMS analyses of contaminated Cr surfaces have also been performed in order to determine the chemical composition and spatial distribution of the contamination. Ionic images of Sulfur and co-contaminants are given in fig.2. From this work critical kinetic data and possible chemical mechanisms of $SO_2$ contamination of Cr surfaces have been identified.

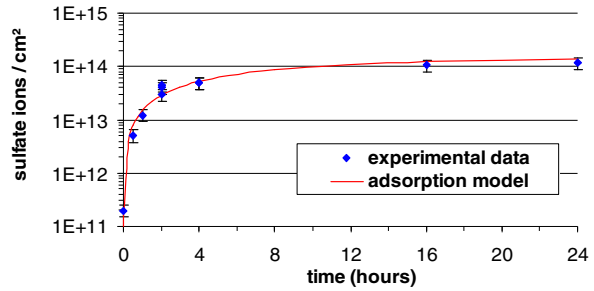


**FIG.1**: Adsorption kinetic of the $SO_2$ at 160ppbv on a Cr surface in clean room conditions (21°C -45% RH).

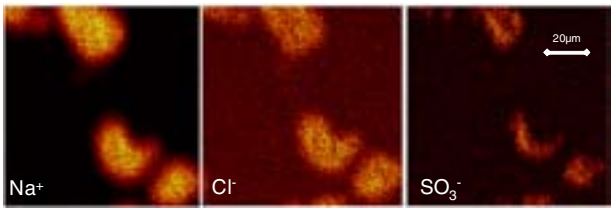


**FIG. 2**: ToF-SIMS ionic images of contamination crystal grown on the Cr after exposure to $SO_2$.

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**Keywords:** AMC, adsorption kinetic, mechanism, ToF-SIMS.

# Advanced monitoring of trace metals applied to contamination reduction of silicon device processing

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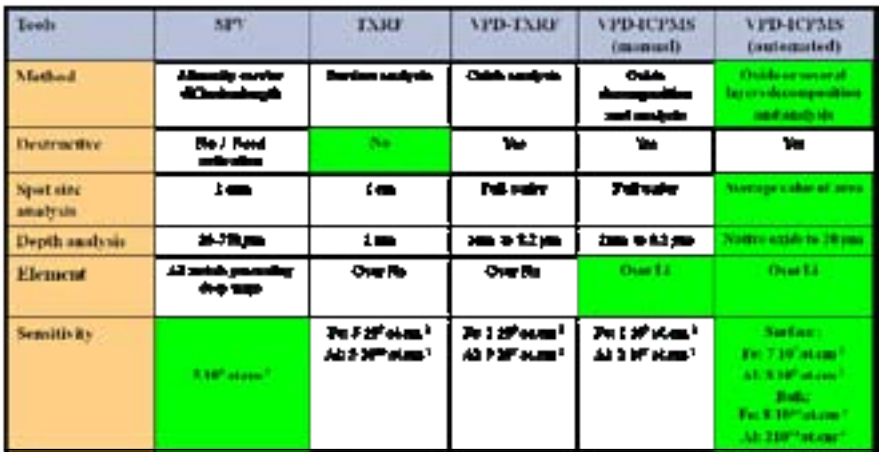
## ABSTRACT

Metallic contamination has long been known to be a key detrimental factor to device yield, causing degradation of various electrical parameters depending on technology, design and device type [1-4]. Thus, device manufacturing control plans systematically include monitoring of metal contamination and , historically, this has been commonly achieved in-line on monitor wafers through a combination of Total Reflectance X-Ray Fluorescence (TXRF) and post anneal Surface Photo Voltage (SPV). In addition, DLTS (Deep Level Transient Spectroscopy) can be extremely powerful for specie identification [5] but is inherently slow not suitable for usage as a process control tool. On the other hand, VPD (Vapor Phase Decomposition) combined with ICP-MS (Inductively Coupled Mass Spectrometry) or TXRF is known to provide both identification and quantification of surface trace metals at lower detection limits that TXRF alone[6, 8]. We have also shown that VPD ICP-MS on thick oxide could be used for control of ion implant induced contamination [7].
Going further in terms of capability improvement, we are moving to a clean room compatible, automated VPD / ICP-MS running in full automation mode from wafer loading to results data upload. Ultimate detection limits can be reached, down to a few $10^6$ at/cm² for certain species. In addition, the system is capable, through the use of adequate chemistries to allow monitoring of either surface or bulk contaminants on wafers. In this presentation we will show preliminary data which illustrate the strong capabilities of the system in a R&D and production environment in comparison with TXRF, SPV and manual VPD



| Tools | SPV | TXRF | VPD-TXRF | VPD-ICPMS (manual) | VPD-ICPMS (automated) |
|---|---|---|---|---|---|
| Method | | | | | |
| Destructive | | | | | |
| Spot size analysis | | | | | |
| Depth analysis | | | | | |
| Element | | | | | |
| Sensitivity | | | | | |

Fig 1 : Figures of merit of automated VPD ICP-MS in comparison with other techniques

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Key words : VDP, ICPMS, contamination, metallic

# Micro roughness determination of periodic microelectronics structures using optical far field measurements

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## ABSTRACT

Recently, a novel approach was proposed for the determination of micro roughness on periodic structures through optical far field characterization using an angle resolved scatterometry set up developed at Fresnel Institute [1]. The light source used in our experiment is a He-Ne Laser using a wavelength of 632.8 nm. The incidence angle equals to 0° and the measurements are performed in the incident plane at a scattering angle ranging from 10° to 90°. A somehow similar approach but at a single 90° collection angle has been reported recently [2].

The scattered intensity is the sum of that of a periodic structure and that of a rough surface. The exact numerical model allows treating the periodic part of the structure while the roughness is viewed as a perturbation and treated using a first order approximation.. Scattering intensity is extracted and is calculated in each direction of space. Theoretical simulation performed using a computer code developed at Fresnel Institute based on differential method [3] and results derived from measurement performed with the aforementioned optical set-up demonstrated the validity of the approach.

The weak point of our present set up is the relatively large size of the illumination beam limiting its use on large structures of test vehicles rather than scribe lines structures. Modification of the optical set-up to reduce the beam spot size is underway. We will describe the optical principle and the theoretical approach for data treatment and to show roughness data in good correlations with AFM values extracted from common part of power spectrums.

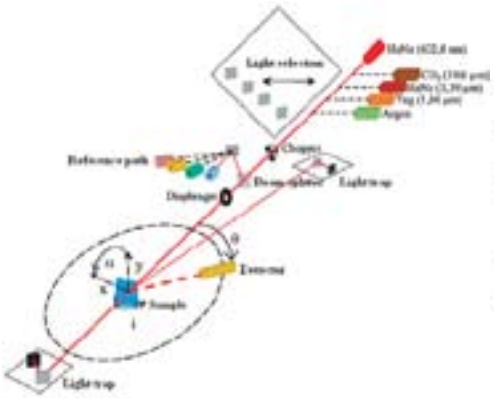

Figure 1: Optical set up

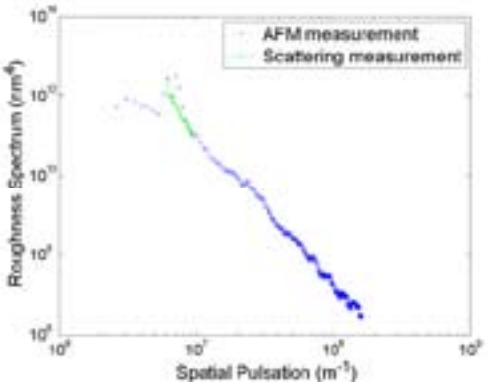


Figure 2: Roughness spectrum of grating: Optical versus AFM

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Key words : scattering, roughness, far field, AFM

# Joint Research on Scatterometry and AFM Wafer Metrology

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## ABSTRACT

The development of sophisticated dimensional metrology is essential to meet the metrology requirements for future technology nodes. CD-metrology in particular is identified by the ITRS as an essential challenge. For production measurements scatterometers and CD-SEMs are key metrology tools. However, universal product-related reference standards for the characterisation and calibration of scatterometers are currently unavailable.

Within the European Metrology Research Program [1] (EMRP) EURAMET [2] and the European Union are funding a joint research project (JRP) with 10 participants from European national metrology institutes, universities and companies. The aim of this project is to overcome current challenges in optical scatterometry. This JRP will significantly improve and extend scatterometry methodically and regarding application areas. These extensions include the application of short wavelengths down to X-rays, a stringent exploitation of the polarisation degree of freedom, using phase information of the scattered field by scanning with a focused coherent spot and new detection schemes together with the development of improved or new concepts for modelling and data analysis.

For further refinement of the scatterometric algorithms, the impact of the structure form and local deviations must be taken into account. The necessary input on structure details will be provided by high resolution SEM and AFM methods, which have to be expanded to provide comparability to scatterometric measurements.

Finally a scatterometry reference standard will be design, developed, characterised and calibrated to face the tough specifications demanded by the semiconductor industry for future technology nodes. As a first step towards a "golden reference standard" suitable for calibration of scatterometers as well as AFM and SEM metrology tools this standard will be designed and developed to be suitable also for testing of AFMs and SEMs, so that the matching of these different types of tools will be possible.

Thus not only a comparability of these methods is introduced but also a mutual support of the partly redundant and partly supplementing information obtained by the different methods is provided. The sophisticated data analysis schemes will be developed in this JRP to reach levels of measurement uncertainty for different measurands significantly beyond the uncertainty levels reachable for each individual metrology method.

Additionally this project combines and extends the current scatterometry application fields towards surface roughness, periodically structured surfaces and diffractive optics, so that the synergy between metrology for semiconductor industry and for optics industry will be exploited.

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# Possible Methods for Measuring the Impact of Bubbles in Temporary Bonding Materials for 3D Integration

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## ABSTRACT

The progresses observed in the microelectronic industry with an increase in applications based on thin wafers and thin microelectronic substrates have made the use of glues for permanent and temporary bonding an essential part in the processing and handling of thin substrates during manufacturing. The evolution of MEMS device technology into high volume production sees the need for materials which have consistent batch-to-batch performance, resulting in high quality coatings with low defect counts. Today's MEMS device manufacturers are focused on increasing yields and eliminating waste rendering the need of a good dispense system more and more necessary. One of the main concerns for integration is the presence of bubbles within the bonding material leading to potential yield degradation.

Because of their high viscosity, spin on glue materials used for permanent and temporary bonding applications are usually difficult to dispense and filter at the point of use and achieve high quality, uniform, bubble-free coatings. In this paper, we will first focus on investigating the use of the IntelliGen® HV dispense system to improve the temporary bonding material coating uniformity and reduce bubble defects. The second main focus will consist in finding a suitable, fast and robust inline metrology tool to detect and quantify defects in bonding materials. Different metrology methods were investigated to measure the effect of filtration on the coating performances. Coating uniformity data were collected by a Senduro reflectometer and bubble defectivity studies were performed using the NandaTech® SPARK inspection tool as shown in Figure 1. Nanda tool is a full wafer inspection system that have both scattered and reflected imaging channels in one. In order to address topology variations and defects for current experiment reflected light optical channel was used.

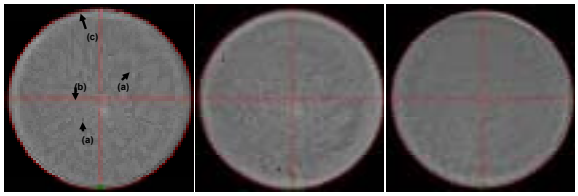


Figure 1. Comparison of the different coating techniques measured using the NandaTech SPARK inspection tool: (a) bubbles, (b) particles and (c) wafer edge bubbles

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TH-17

# Studies of Impurity Redistribution in Copper Ultrafine Lines in BEOL Structures

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*** Corresponding Author*

## *Abstract*

Ultrafine line interconnects in BEOL structures are currently formed by electroplating copper into narrow trenches with a width 40 nm or less. The plating is done over a PVD copper seed deposited on a thin layer of Ta/ TaN that makes contact with the dielectric above the FEOL structures. The total thickness of liner and seed must be as thin as possible to ensure that most of the trench is filled with high purity copper as free of defects and impurities as possible to maintain high conductivity as well as to minimize potential problems that could arise from electromigration. While it would be most desirable to have the copper consist of a single crystal, "bamboo" structure of large grained material whose grain boundaries are perpendicular to electric current flow is considered satisfactory. As deposited copper is usually fine grained, however, and an annealing step is required to promote grain growth needed to attain the bamboo structure. For lines greater than 100 nm in width such annealing procedures usually give satisfactory results, but once the lines are narrower, fine grain structures can persist leading to the possibility of degraded performance. In the current study a variety of analytic techniques have been used to determine the distribution of plating solution components in copper both as a function of solution composition and with and without annealing. Figure 1. Illustrates results obtained by time of flight secondary ion mass spectrometry (ToF-SIMS). Measurements were also made by an SEM/EDS x-ray analysis to obtain higher lateral resolution.

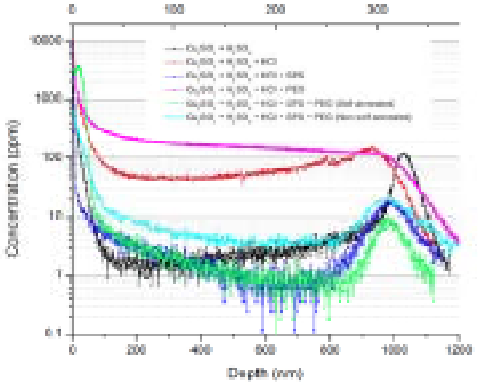


Figure 1. ToF-SIMS Depth Profiles for Chlorine for the Different Plating Conditions

TH-18

# ToF-SIMS Analysis of the Effect of Bath Modulation on Impurity Incorporation into Damascene Copper

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## ABSTRACT

Impurity pinning during self-annealing of damascene copper is often cited as a key inhibitor to the growth of grains. In this study, we examine the connection between the incorporation of bath additives into electrochemically deposited (ECD) copper and microstructural evolution using time of flight secondary ion mass spectrometry (ToF-SIMS), Focused Ion Beam (FIB) imaging, and Transmission Electron Microscopy (TEM).

In the first set of experiments, 450 nm-wide trenches in $SiO_2$ were prepared for ECD with 3 nm PVD TaN, 3 nm PVD Ta and 30 nm PVD Cu seed (nominal field values). A 3-component plating bath with an ATMI/Enthone Viaform additive package was used for beaker plating with a 2-stage current density profile: 5 mA/cm$^2$ for seed reinforcement and 10mA/cm$^2$ for trench fill and overburden deposition. TEM images comparing as-plated and self-annealed samples showed significant grain growth, but grains as small as 30 nm could still be observed (Fig. 1a). Sputter depth-profiling of 450 nm lines by ToF-SIMS revealed the concentration of impurities in the overburden was ~4 x $10^{18}$ atoms/cm$^3$ for sulfur and chlorine, while the trenches contained 4-10 times more (Fig. 1b).

The second set of experiments sought to determine the effect of changing the bath composition during plating as a means for reducing impurity incorporation. Finer lines (70 and 100 nm) were plated with the ATMI/Enthone Viaform additives using a 33 mA/cm$^2$ trench fill and overburden step. This initial study focused on tracing fragments containing sulfur. Two separate solutions were prepared, a standard 3-component and a 2-component bath lacking accelerator. Samples were then plated either by a manual transfer between the two beakers after trench fill or by swapping solutions during plating using a sealed microfluidic plating cell with individually programmable syringes of plating solution. FIB imaging confirmed superconformal, void-free filling of the trenches used for measurement. The ToF-SIMS sputter depth profiles were taken over 70nm or100nm lines. Results indicated a factor of 5 decrease in the average sulfur content relative to the control (single bath), from ~$10^{19}$ to 2x$10^{18}$, with a gradient of increasing sulfur with depth. These observations will be discussed in light of earlier results on blanket films showing impurity segregation through a quasi-zone refining process during recrytallization, and the transition from volumetric to 2D growth in films.

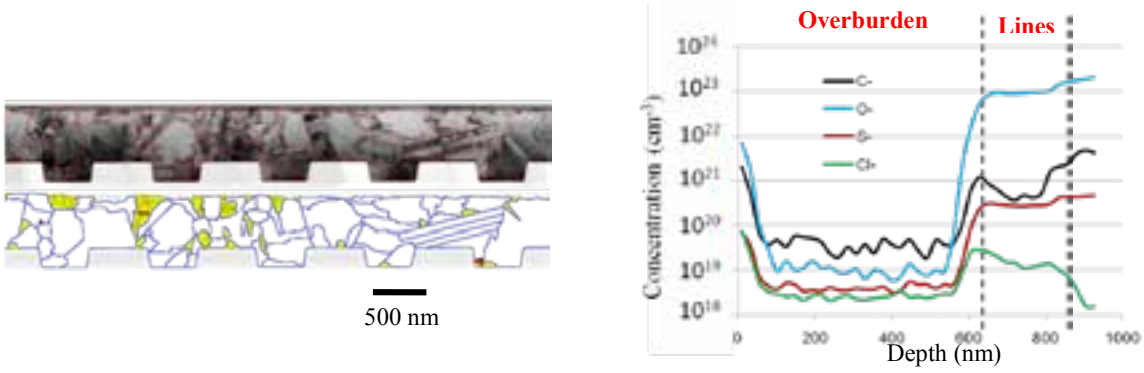


Figure 1. (a) TEM montage with grain tracing (upper) and extracted grain boundary map (lower). Yellow grains are less than 100 nm equivalent diameter, and red grains less than 30 nm. (b) SIMS depth profile showing impurity content from trenches shown in (a). The C, O, S and Cl are low and stable throughout the overburden. The oxygen content increases dramatically as the depth profile encounters the $SiO_2$ pattern. The carbon, sulfur, and chlorine content is 4-10 x greater in the trenches than the overburden.

Keywords: Damascene, grain growth, impurities

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TH-19

# Multi-scale Resolution 3D X-ray Imaging for 3D IC Process Development and Failure Analysis

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## ABSTRACT

Multi-scale resolution 3D x-ray imaging with 50 nm resolution offers unique capability to new process development, failure analysis, and production monitoring of 3D IC devices. Its nondestructive nature allows parts to be imaged without sample preparation induced artifacts or time lapse imaging (4D imaging) to study failure mechanism such as current or stress induced failures. It images a large number of features simultaneously and allows quick feedback on manufacturing processes to speedup process development. The spatial resolution of 3D x-ray imaging is been continuously improved and 30nm and 50nm resolution has been developed using synchrotron and laboratory x-ray sources, respectively. The performance and application examples of two major 3D x-ray imaging systems will be presented and discussed

# Void Detection In Copper Interconnects Using Energy Dispersive X-Ray Spectroscopy

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## ABSTRACT

Low-dimensional copper interconnects are prone to void formation which takes place during the Cu-filling of narrow interconnect lines. These voids increase the electrical resistance of the interconnects which in turn results in an increase of the RC delay of the integrated circuit. Therefore, a fast and non-destructive method is needed, which will allow the detection of the voids in copper interconnects at the early stages of their fabrication process.

In this work, we used Energy Dispersive X-ray Spectroscopy (EDS) on narrow copper lines (15-55 nm) as a non-destructive method to detect the presence of voids. The methodology used is based on the fact that within EDS, the intensity of the characteristic X-rays (for Cu) is proportional of the amount of Cu-atoms present within the interaction volume. Hence, for thin and polished Cu-lines where absorption effects can be ignored, a decrease of the copper signal during an EDS line-scan along the copper interconnect line can be translated into a reduced amount of Cu i.e. the presence of a void.

Using this methodology we have been able to identify the presence of <10 nm voids within 15-30 nm lines (see Fig. 1). A sensitivity analysis based on the S/N ratio of the system and the volume fraction of the void relative to the line width and height, demonstrates that the technique is primarily suited for void detection in narrow lines (>50 nm) whereas for larger dimensions the relative intensity variation due to the presence of the void, becomes too small.

a) b)

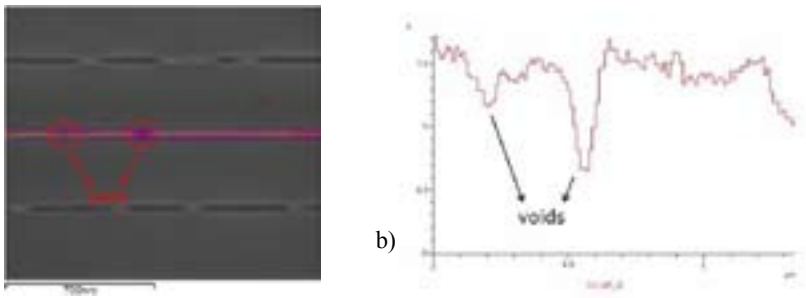


**FIGURE 1.** a) EDS mapping of the 15 nm Cu-line; Cu is illustrated with green color and $SiO_2$ with magenta. b) Line-scan of the Cu-line where the Cu signal is displayed. On both images, the two voids are clearly detected.

*Keywords*: Copper interconnects; EDS; Void detection

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# Fourier scatterometry for characterization of sub-wavelength periodic two photon polymerization structures

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## ABSTRACT

Scatterometry is an indirect method for a quantitative determination of the surface profile of micro and nanostructured surfaces by measuring and analyzing the light diffraction of those surfaces. Different measurement configurations are available in commercial measurement tools. The most frequent are normal incidence reflectometry, 2-θ scatterometry and spectroscopic ellipsometry [1,2]. In recent time angle resolved Fourier scatterometry has become of great interest as it allows an angle resolved measurement for a large incidence angle range in one shot without the need of mechanical scanning [3]. Not only in semiconductor industry but also in other fields the fast and precise optical characterization of periodical gratings of sub-wavelength size is of great interest. We present the application of Fourier scatterometry, extended by the use of white light for the characterization of sub-wavelength periodic gratings of photosensitive material structured by two-photon polymerization. First a simulation-based sensitivity comparison of Fourier scatterometry at one fixed wavelength, Fourier scatterometry using a white light light source and also additionally using a reference-branch for white-light-interference has been carried out. The investigated structures include gratings produced by two-photon polymerization of photosensitive material and typical semiconductor test gratings. The simulations were performed using the rigorous-coupled-wave-analysis included in our software package MICROSIM. The sample is illuminated with white light through a high-NA microscope objective (NA: 0.95) allowing an incoming illumination with wide illumination (0°-72°) and azimuthal angle ranges (0°-360°). Using white light instead of a fixed wavelength illumination gives a new dimension of freedom and finally using scanning white-light-interference allows increasing sensitivity towards structure height and shape. Based on the results of the sensitivity simulations the expected gain of information using Fourier scatterometry in combination with white-light-interferometry is verified. We also show our experimental implementation of the measurement setup using a white-light-laser with an broad intensity distribution in the used spectral range (400 – 700 nm) and a modified microscope with a high-NA (NA: 0.95) objective as well as a Linnik-type reference branch for the interferometry measurements. First measurements for the investigation of the performance of this measurement setup are presented for comparison with the simulation results.

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TH-22

# Robust, High Aspect Ratio Columnar Diamond Atomic Force Microscope Probes For High Relief Imaging

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## ABSTRACT

We report on the fabrication of a high resolution, high aspect ratio columnar diamond atomic force microscope probe using a simple two-step batch fabrication method [1-2]. The process utilizes a low energy gallium ion implant into the first few nanometers of the surface of diamond substrate using focused ion beam (FIB). The implanted regions form a hard mask against plasma etching allowing production of well controlled high relief structures over the exposed surface of the substrate. This technology has an advantage over the other conventional resist based lithographic techniques since it can write a mask pattern on any non planar surfaces viz., spheres, cones etc. and has the capability to form high aspect ratio, high resolution patterns in all varieties of diamond including natural, synthetic HPHT and CVD films, at various levels of doping.

For the fabrication of diamond columnar AFM probes, Ga ions were implanted at the apex of the tip of a commercially available diamond probe. Subsequently the probe was etched to achieve the columnar shape at the tip as shown in figure 1. Improved lateral resolution of the AFM images is demonstrated using these columnar probes as compared to the standard probes. A standard calibration grating with step height of 18±1 nm, width of 1.5 µm and pitch of 3µm, and a high resolution grating with step height of 35 nm, width of 35 nm and pitch of 70 nm is used in contact mode for resolution test. In addition, the diamond columnar probes are shown to exhibit low wear compared to the other commercially available columnar probes. These probes can be also utilized for video rate AFM imaging applications considering its low wear and high resolution qualities.

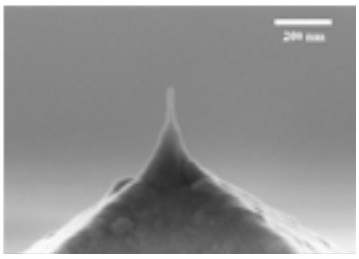

**FIGURE 1.** Columnar diamond AFM probe having a diameter of 23 nm and height 130 nm (aspect ratio ~ 6:1)

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TH-23

# Thin film mechanical characterization using Colored Picosecond Acoustics

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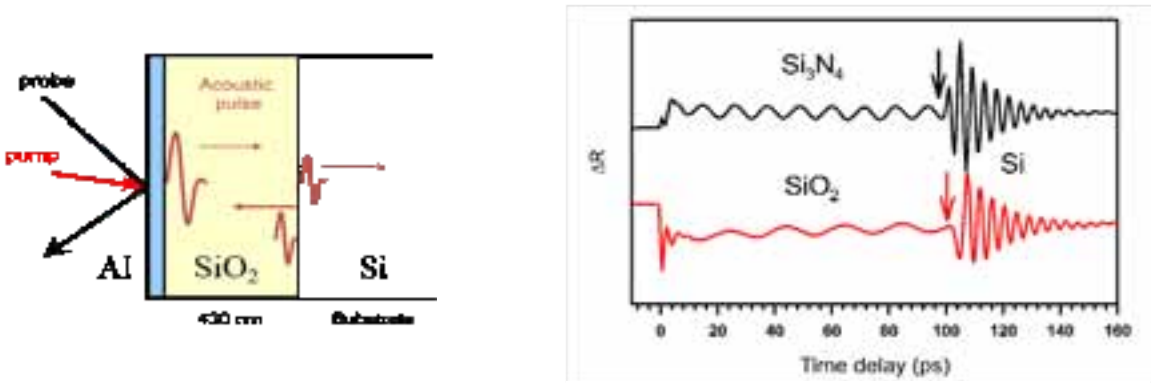
## ABSTRACT

The mechanical properties of materials currently used by the microelectronic industry are poorly known. Only a few measurement techniques are able to probe various materials deposited in submicron-thick films. Picosecond acoustics (PA) is an optical technique which uses a femtosecond laser to excite and detect longitudinal acoustic waves at very high frequencies (100 GHz to 1 THz). Such an optical setup offers a unique way of implementing a sonar at nanoscale. By measuring the time-delay between successive echoes it is basically possible to access to the thickness or to the longitudinal sound velocity.
For several years we have shown that the PU capabilities can be enhanced if one uses several laser wavelengths or colors. More parameters are measurable, for example thickness and sound velocity are simultaneously reachable and the measurement accuracy can be significantly enhanced using this so-called Colored Picosecond Acoustic technique (CPA).
As an optical technique, CPA is contactless and is a non-destructive technique. It can be applied to metals, dielectrics and semiconductors, crystalline or not, deposited in films as thin as a few nanometers. Beyond the sound velocity, the CPA technique can also access to the mass density, the acoustic losses or to the temperature dependence of the elastic constants. Recently we found a way of producing high-frequency surface acoustic waves using the same experimental setup. From that we are now able to perform complete elastic measurements namely measuring the Young modulus and the Poisson ratio of thin films.
In this presentation we will present the capabilities of the CPA and will focus on its application to the design and the control of some microelectronic devices.




Schematic view of the experimental setup and some data measured on thin films. CPA can access to film thickness and sound velocity in thin films thanks to an optical setup which implements a sonar at nanoscale

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Keywords: Picosecond Acoustics, Mechanical properties, Sound velocity, Mass density, Young modulus, Poisson ratio, Thickness

# FCMN - May 27th Post-conference tour

In the heart of the Alps sits France's flattest city. Find out about its history and famous figures in a 2 hour morning guided tour.

Then have lunch in a restaurant.

After lunch, a comfortable coach will transport you to visit two of the most famous places in Vercors.

The Choranche cave :

Let yourself drift... The waters of the underground lakes and rivers flood the crystal whiteness of the rock formations with emerald green reflections. Nature at its purest...

The stalactites, called soda straws are the great sights of this cave: they are very thin, very fragile. There are thousands of them in Choranche which is a unique scene in Europe.

http://www.grottes-de-choranche.com/ChorancheUK/indexChorancheUK.php

Pont en Royans village :

Classified as historical monuments in 1946, the sight of the houses suspended over the Bourne river had already impressed Stendhal. They should be admired from the left bank of the Bourne river.

http://www.ot-pont-en-royans.com/

Your one-day tour will finish by a stop in Meunier distillery.

Meunier Distillery :

Since 1809, Meunier distillery is specialized in the distillation of plants, especially Génépi. You will discover typical copper stills, still in use in the distillery and the visit ends with a tasting of liquors produced locally.

http://www.distilleriemeunier.fr/

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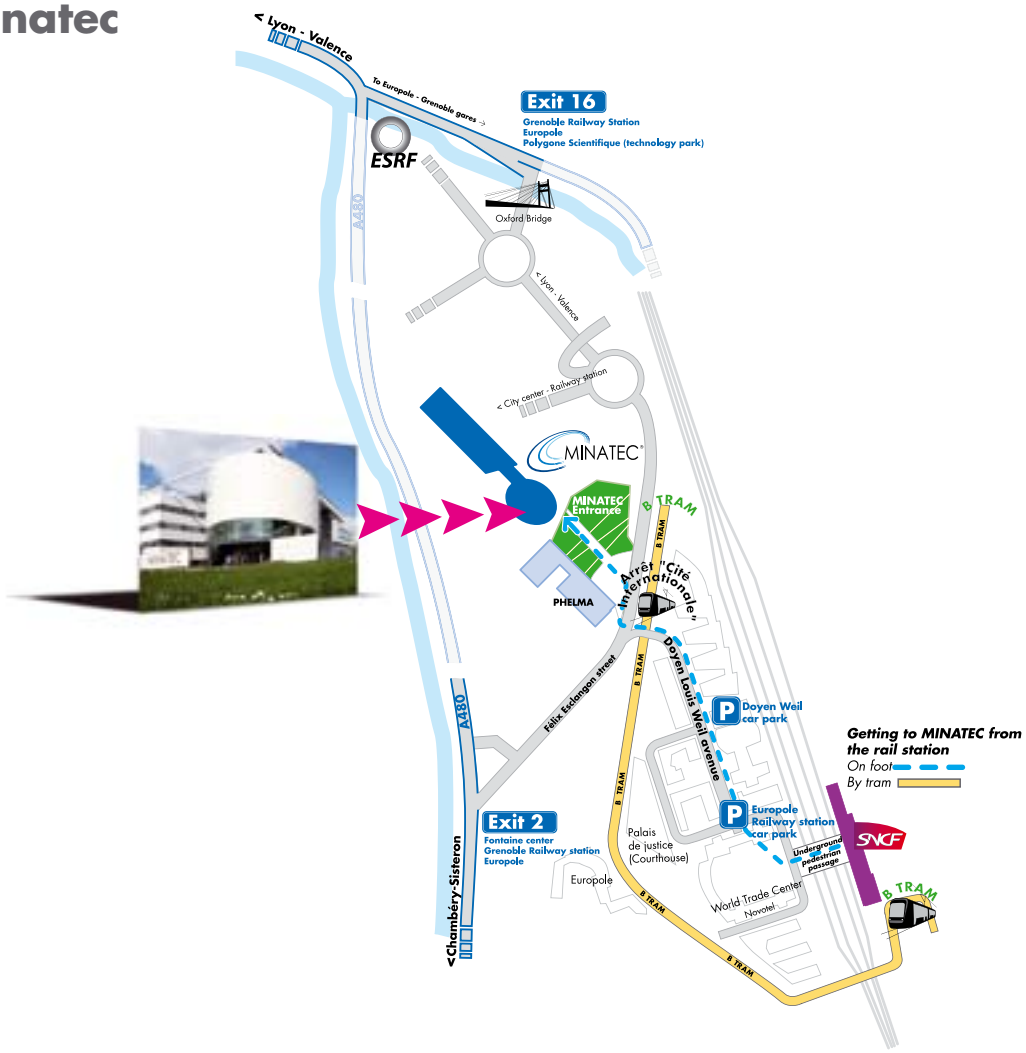


# May 25th : Banquet at « La Bastille » :

In the heart of Grenoble, La Bastille, is a small fortified mountain located at the crossroad of three valleys, served by the first urban cable-car in the world. In a few minutes, days and night, the famous "bubbles" of Grenoble take you in the air from the center of the town up to the Bastille fortress.
From the hilltop, you will discover the flattest town in France in its mountain setting! When the sun sets and the lights go down in the city, the view is outstanding.
Then you will have dinner at the "Restaurant du Téléférique" On its panoramic terrace overlooking the town with the Alps in the background, day and night, the view is magnificent...