Integrated DC-DC Conversion for Energy-Efficient Multicore Microprocessors

New power converters provide versatility in optimizing energy usage for processor chips.

Introduction

Current server systems utilize standard power-management architectures which use an off-chip voltage regulation module (VRM) downconverting to the required supply voltage for the processor. Achieving the highest energy efficiency for processors requires dynamic selection of the supply voltage depending on workload. Processors are increasingly operating at high current levels at low voltages, exacerbating power supply impedance requirements. At the same time, the advent of multicore processors to achieve additional performance through parallelism requires many individually scaled voltage domains to be supported. Conventional system architecture is not sustainable or scalable to these requirements.

The percentage of power consumed by a server's processor chip varies and can be as much as 50% of the server-wide power utilization. This project seeks to improve both the energy efficiency and scalability of voltage management for processor chips. In particular, the use of novel materials and designs will be applied to on-chip direct-current-to-direct-current (DC-DC) voltage converters which allow greater control of power distribution and reduce demand for power supplied to the processor chips.

Benefits for Our Industry and Our Nation

The nation's servers and data centers were estimated to use 61 billion kilowatt-hours (kWh)—or 1.5% of total U.S. electricity consumption. Of that, volume servers consumed 68% of the electricity used. Much of that electricity consumption is from non-productive dissipation that occurs during DC voltage regulation and conversion processes within the servers. This project will lead to novel multicore processors that integrate DC-DC converters to help meet growing server performance demands.

Applications in Our Nation's Industry

The advanced material and design work to create on-chip power conversion components will lead to a more energy-efficient multicore processor. This will contribute to large efficiency gains



High-efficiency, on-chip voltage regulation. Illustration courtesy of the U.S. Department of Energy's Industrial Technologies Program.

in the server and telecommunications market and increase the capacity for performance demands. The industries affected by this work include the following:

- · Data center and telecommunication facility owners
- Manufacturers and resellers of volume servers and other equipment requiring multicore processors
- Microelectronics, computer chip fabrication, and system board design manufacturing firms

Project Description

This project addresses the future scalability and energy efficiency of multicore processors that require high-power densities at low scalable voltages across multiple domains on a single chip. By developing on-chip DC-DC converters capable of delivering power densities exceeding 60 watts per square centimeter (W/ cm²) at a less than 1 volt (V) supply, the research team will maintain processor DC-DC power conversion efficiencies above 90%.

Conventional volume servers are designed with off-chip, boardlevel VRMs. Such architectures limit the number of available voltage domains and create unreasonable demands on powersupply network impedances to achieve target power densities and supply voltages.

The power management circuits that will be developed are based on improved magnetic energy storage techniques. These novel on-chip structures will utilize magnetic materials and be integrated with specific DC-DC converters in order to achieve more than the desired power densities. Passive magnetic devices will be used to improve the design of on-chip power management and energy delivery by allowing high-density, on-chip storage. The power to the chip will require less supply current than conventional designs and allow granular, dynamic, supplyvoltage scaling.

Barriers

The current supply chain for server components is governed by a limited set of fabricated designs and commodity pricing for materials. Without proof of new design and material performance, the computing industry will be slow to revise current inefficiencies in microelectronics design and materials.

This project will utilize newly identified materials and designs for on-chip power conversion, which will dramatically lower electrical current demand and increase the productive use of power to the processor. The resulting scalability of the architecture should make it attractive to further development and commercialization within the computing industry.

Pathways

This project is developing and testing various designs and materials for high-density, on-chip power supply management. Validating and evaluating a multicore processor at the end of the project will provide the impetus for developing of commercial components.

Milestones

- · Development of novel on-chip power management components
- · Production and evaluation of first-generation products
- Testing of multicore processors with integrated power management

Commercialization

This project will prove the technical feasibility of the new onchip inductors and capacitors. Based on partnership with IBM and expressed interest by Intel, there will be significant market expertise available to bring validated technology to the development and verification stages.

Project Partners

Columbia University New York, NY Principal Investigator: Kenneth Shepard E-mail: shepard@ee.columbia.edu

Cornell University Ithaca, NY

IBM Thomas J. Watson Research Center Yorktown Heights, NY

For additional information, please contact

Gideon Varga Technology Manager U.S. Department of Energy Industrial Technologies Program Phone: (202) 586-0082 E-mail: Gideon.Varga@ee.doe.gov

Information & Communications Technology

Power Supply Chain Research & Development

U.S. DEPARTMENT OF

Energy Efficiency & Renewable Energy

EERE Information Center 1-877-EERE-INFO (1-877-337-3463) eere.energy.gov/informationcenter

DOE/EE-0501 • May 2011 Printed with a renewable-source ink on paper containing at least 50% wastepaper, including 10% post consumer waste.