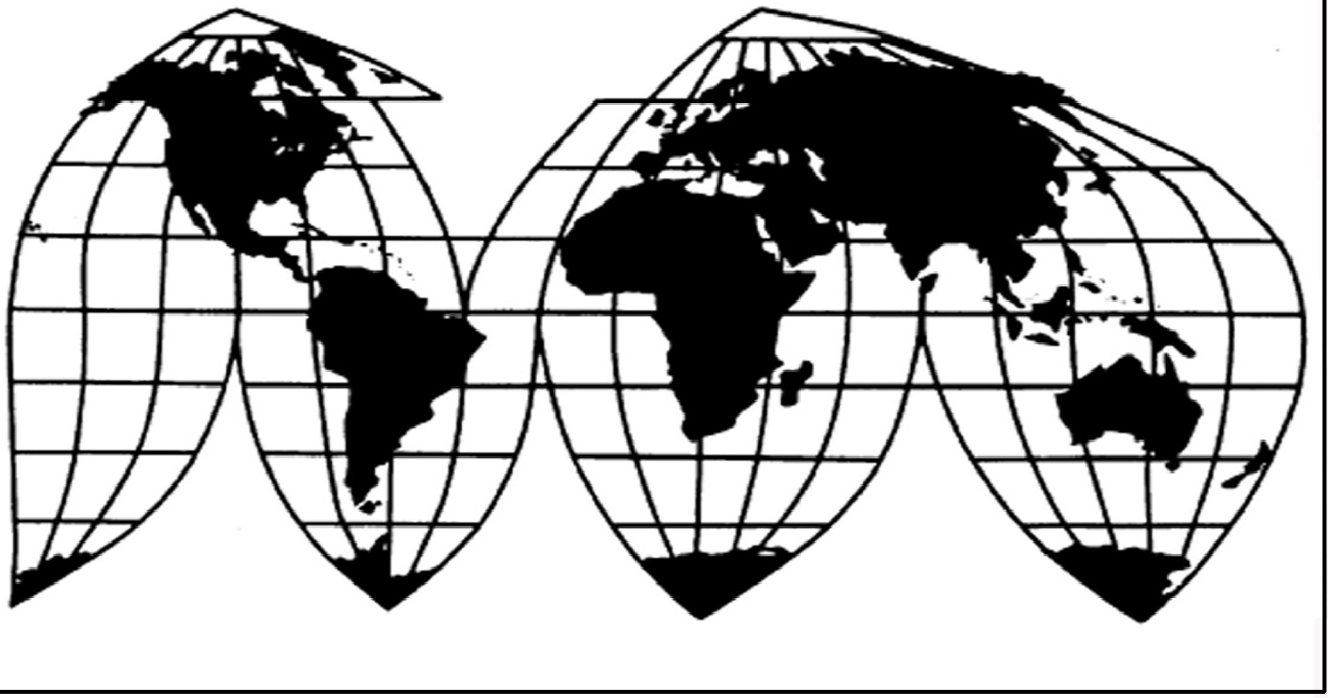
In the Matter of

Certain NAND Flash Memory Circuits and Products Containing Same

Investigation No. 337-TA-526

Publication 3970 **December 2007**

U.S. International Trade Commission



Washington, DC 20436

U.S. International Trade Commission

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Address all communications to
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Washington, DC 20436

U.S. International Trade Commission

Washington, DC 20436
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In the Matter of

Certain NAND Flash Memory Circuits and Products Containing Same

Investigation No. 337-TA-526

Publication 3970 **December 2007**

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of **CERTAIN NAND FLASH MEMORY CIRCUITS AND PRODUCTS CONTAINING SAME**	**Investigation No. 337-TA-526**

NOTICE OF COMMISSION DECISION TO REVIEW IN PART AN INITIAL DETERMINATION, AND ON REVIEW, TO TAKE NO POSITION CONCERNING CERTAIN VALIDITY ISSUES AND TO AFFIRM THE ADMINISTRATIVE LAW JUDGE'S DETERMINATION THAT THERE IS NO VIOLATION OF SECTION 337; TERMINATION OF INVESTIGATION

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the United States International Trade Commission has determined to review in part an initial determination ("ID") issued by the presiding administrative law judge ("ALJ") finding no violation of section 337 of the Tariff Act of 1930. Specifically, the Commission has determined to review the portion of the ALJ's determination relating to anticipation and obviousness. On review, the Commission has determined to take no position with respect to these issues, but to affirm the ALJ's determination of no violation of section 337 and to terminate the investigation.

FOR FURTHER INFORMATION CONTACT: Steven Crabb, Esq., Office of the General Counsel, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 708-5432. Copies of non-confidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 205-2000. General information concerning the Commission may also be obtained by accessing its Internet server at *http://www.usitc.gov*. The public record for this investigation may be viewed on the Commission's electronic docket (EDIS) at *http://edis.usitc.gov*. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on (202) 205-1810.

SUPPLEMENTARY INFORMATION: The Commission instituted this investigation on October 15, 2004, based on a complaint filed by SanDisk Corporation ("SanDisk") under section 337 of the Tariff Act of 1930 (19 U.S.C. § 1337) against respondents, STMicroelectronics N.V. of Geneva, Switzerland and STMicroelectronics, Inc. of Carrollton, Texas (collectively referred to as "ST").

SanDisk's complaint alleged violations of section 337 in the importation into the United States, the sale for importation, and the sale within the United States after importation of certain NAND Flash Memory circuits and products containing the same by reason of infringement of claims 27, 28, and 32 of United States Patent No. 5,172,338 (the "'338 patent").

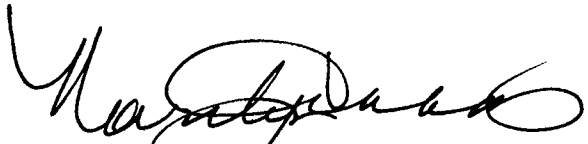
The ALJ held a hearing from August 1, 2005 to August 8, 2005, and on October 19, 2005, the ALJ issued his final ID, including his recommended determination on remedy and bonding. The ALJ determined that there was no violation of section 337, because respondents' products do not infringe the asserted claims of the '338 patent and because complainant failed to satisfy the technical prong of the domestic industry requirement. The ALJ rejected arguments by ST that the '338 patent is invalid as anticipated and as obvious. The ALJ further rejected arguments by ST and the Commission's investigative attorney ("IA") that the '338 patent is invalid for failing to meet the written description requirement and/or the indefiniteness requirement under 35 U.S.C. § 112, ¶¶ 1 and 2. The ALJ also rejected ST's arguments that the '338 patent is unenforceable based on inequitable conduct and improper inventorship.

On October 31, 2005, SanDisk filed a petition for review, arguing that the ALJ improperly construed the claims and concluded that there was no infringement and no domestic industry. On the same day, ST filed a contingent petition for review, requesting that the Commission review the ALJ's claim construction and determination that the patent was not invalid and not unenforceable, in the event that the Commission decided to grant SanDisk's petition . On November 7, 2005, SanDisk and the IA filed responses to the petitions, arguing that the invalidity and unenforceability issues do not warrant review. On the same day, ST filed a response, supported by the IA, arguing that the infringement and domestic industry issues should not be reviewed.

Having examined the record of this investigation, including the ALJ's final ID, the petitions for review, and the responses thereto, the Commission has determined to review in part the ALJ's ID. Specifically, the Commission has determined to review the portion of the ALJ's determination relating to anticipation and obviousness. On review, the Commission has determined to take no position with respect to those issues, but to affirm the ALJ's determination of no violation of section 337 based on his findings of no infringement and no domestic industry, thereby terminating the investigation.

The authority for the Commission's determination is contained in section 337 of the Tariff Act of 1930, as amended (19 U.S.C. § 1337), and in section 210.42 - 45 of the Commission's Rules of Practice and Procedure (19 C.F.R. § 210.42-45).

By order of the Commission.



Marilyn R. Abbott
Secretary to the Commission

Issued: December 5, 2005

CERTAIN NAND FLASH MEMORY CIRCUITS AND PRODUCTS CONTAINING SAME **337-TA-526**

CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the attached **NOTICE OF COMMISSION DECISION TO REVIEW IN PART AN INITIAL DETERMINATION, AND ON REVIEW, TO TAKE NO POSITION CONCERNING CERTAIN VALIDITY ISSUES AND TO AFFIRM THE ADMINISTRATIVE LAW JUDGE'S DETERMINATION THAT THERE IS NO VIOLATION OF SECTION 337; TERMINATION OF INVESTIGATION** was served upon the Commission Investigative Attorney, Juan Cockburn, Esq., and all parties via first class mail and air mail where necessary on December 6, 2004.

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PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	)	
	)	
CERTAIN NAND FLASH MEMORY CIRCUITS AND PRODUCTS CONTAINING SAME	)	Investigation No. 337-TA-526
	)	
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Final Initial and Recommended Determinations

This is the administrative law judge's Final Initial Determination under Commission rule 210.42. The administrative law judge, after a review of the record developed, finds no violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, has occurred.

This is also the administrative law judge's Recommended Determination on remedy and bonding, pursuant to Commission rules 210.36(a) and 210.42(a)(1)(ii). Should a violation of section 337 be found by the Commission, the administrative law judge recommends that the Commission issue a limited exclusion order and a cease and desist order. He further recommends that any bond during the Presidential review period be in the amount of 100 percent of the entered value for any importation involving infringing products.

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ABBREVIATIONS

CBr	Complainant's Post-hearing Brief
CDX	Complainant's Demonstrative Exhibit
CORFF	Complainant's Objection To Respondents' Proposed Finding
COSFF	Complainant's Objection To Staff's Proposed Finding
CFF	Complainant's Proposed Finding
CPHS	Complainant's Pre-hearing Statement
CPX	Complainant's Physical Exhibit
CRRBr	Complainant's Post-hearing Reply Brief to Respondents' Post-hearing Brief
CRSBr	Complainant's Post-hearing Reply Brief to Staff's Post-hearing Brief
CRRFF	Complainant's Rebuttal Finding to Respondents' Proposed Finding
CRSFF	Complainant's Rebuttal Finding To Staff's Proposed Finding
CX	Complainant's Exhibit
FF	Additional Findings Of Fact
JX	Joint Exhibit
RBr	Respondents' Post-hearing Brief
RDX	Respondents' Demonstrative Exhibit
RPHS	Respondents' Pre-hearing Statement
RPX	Respondents' Physical Exhibit
RRBr	Respondents' Post-hearing Reply Brief
RRX	Respondents' Rebuttal Exhibit
ROCFF	Respondents' Objection To Complainant's Proposed Finding

ROSFF	Respondents' Objection To Staff's Proposed Finding
RFF	Respondents' Proposed Finding
RRCFF	Respondents' Rebuttal Finding To Complainant's Proposed Finding
RRSFF	Respondents' Rebuttal Finding To Staff's Proposed Finding
RX	Respondents' Exhibit
SPBr	Staff's Pre-hearing Brief
SBr	Staff's Post-hearing Brief
SFF	Staff's Proposed Finding
SRBr	Staff's Post-hearing Reply Brief
SRRFF	Staff's Rebuttal Finding To Respondents' Proposed Finding
SRCFF	Staff's Rebuttal Finding To Complainant's Proposed Finding
Tr.	Transcript Of Pre-hearing Conference And Hearing

I. Procedural History

By notice, which issued on November 15, 2004, the Commission instituted an investigation, pursuant to subsection (b) of section 337 of the Tariff Act of 1930, as amended, to determine whether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation into the United States, or the sale within the United States after importation of certain NAND flash memory circuits and products containing same by reason of infringement of one or more of claims 27, 28 and 32 of U.S. Patent No. 5,172,338, (the '338 patent) and whether an industry in the United States exists as required by subsection (a)(2) of section 337. The Commission, in its notice, designated this administrative law judge as the presiding judge.

The complaint was filed with the Commission on October 15, 2004, under section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, on behalf of SanDisk Corporation (San Disk), 140 Caspian Court, Sunnyvale, Calif., 94089. A supplement was filed on October 29, 2004. The complaint requested that the Commission institute an investigation and, after the investigation, issue a permanent exclusion order and a permanent cease and desist order. Named in the notice of investigation as respondents were STMicroelectronics N.V., 39, Chemin du Champ des Filles, C.P. 21, CH 1228 Plan-Les-Oúates, Geneva, Switzerland and STMicroelectronics, Inc., 1310 Electronics Drive M/S 2308, Carrollton, Texas 75006 (ST).

In January 1996, complainant SanDisk had filed a complaint with the Commission which alleged infringement of the '338 patent and U.S. Patent No. 5,418,752 (the '752 patent) against NAND Flash memory devices sold by Samsung Electronics Co., Ltd. and Samsung Semiconductor Inc., (Samsung). The complaint led to the Commission's institution of Investigation No. 337-TA-382, In the Matter of Certain Flash Memory Circuits and Products

Containing Same (the Samsung investigation). On February 26, 1997, another administrative law judge issued an Initial Determination construing claim 27 of the '338 patent, which found that Samsung's Flash memory circuits infringed claim 27 of the '338 patent and that the claims of the '338 patent were valid and enforceable. (CX-39C.) Pursuant to Commission rule 210.66(f), the finding of infringement and validity of the '338 patent became the Commission's Final Determination on April 15, 1997.

On September 15, and 17, 1996, prior to the hearing in the Samsung investigation, requests for reexamination were filed in the Patent Office by both San Disk and Samsung. The Patent Office granted the requests. As a result of the reexamination, inter alia, the language "until all the addressed cells are verified" was included in the last means clause of claim 32 in issue.[1] The reexamination certificate on the '338 patent issued on July 8, 1997. (RX-6.)

Order No. 3, which issued on December 21, 2004, set a target date of January 19, 2006 (a fourteen (14) month target date[2]) which meant that any final initial determination on violation should be filed no later than October 19, 2005.

Order No. 17, which issued on July 12, 2005, required submissions from complainant, respondents and the staff with respect to issues in the investigation.

By notice dated August 23, 2005, the Commission determined to grant the administrative

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[1] The '338 patent initially issued on December 15, 1992 with named inventors Sanjay Mehrotra, Eliyahou Harari and Winston Lee. (CX-1). During prosecution SanDisk filed a petition with the Patent Office requesting the removal of Lee as an inventor. (RX-22.) Eventually Lee was removed as an inventor by a certificate of correction. (CX-1 at SDITC 056452).

[2] The notice of investigation was published in the Federal Register on November 19, 2004 (69 Fed. Reg. 67758).

law judge's request for judicial enforcement of a subpoena issued against Atmel Corporation (Atmel) (Order No. 19). The Commission also determined that Order No. 19 is not an initial determination, but rather a request issued pursuant to Commission rule 210.32(g). The district court ordered Atmel to respond to a petition for enforcement of the subpoena by September 30.

Order No. 24, which issued on August 19, 2005, denied respondents' Motion No. 526-18 to strike from the record certain hearing testimony and hearing exhibits of complainant SanDisk. Order No. 25, which issued on August 19, granted respondents' Motion No. 526-19 to withdraw certain exhibits from the evidentiary record.

A pre-hearing conference was conducted on August 1, 2005, with the hearing also commencing on that date and continuing to August 8. All parties participated in the hearing. Post-hearing submissions have been filed. The matter is now ready for a final decision.

The Final Initial and Recommended Determinations herein are based on the record compiled at the hearing and the exhibits admitted into evidence. The administrative law judge has also taken into account his observation of the witnesses who appeared before him during the hearing. Proposed findings of fact submitted by the parties not herein adopted, in the form submitted or in substance, are rejected as either not supported by the evidence or as involving immaterial matters and/or as irrelevant. Certain findings of fact included herein have references to supporting evidence in the record. Such references are intended to serve as guides to the testimony and exhibits supporting the finding of fact. They do not necessarily represent complete summaries of the evidence supporting said findings.

II. Parties

See FF 1-8.

III. Jurisdiction

The complaint and notice of investigation state a cause of action under section 337 of the Tariff Act of 1930, as amended. Also, in respondents' responses to the complaint, respondents admit that they have imported the accused chips into the United States and sold them in the United States. (Response to the Complaint, pp. 1-2, ¶¶ 16, 40 (December 9, 2005).) In addition, the parties have entered into a stipulation relating to importation of ST's accused products. (SX-3C). Thus, the Commission has jurisdiction over the subject matter of this investigation. See Amgen, Inc. v. U.S. Int'l Trade Comm'n, 902 F.2d 1531, 1536 (Fed. Cir. 1990). All parties appeared in the investigation. Hence, the Commission has in personam jurisdiction.

IV. Samsung Investigation

Referring to the Samsung investigation, complainant argued that the Commission is "bound by its own precedents, especially with respect to matters of law." (CBr at 26.) Complainant further asserted that "the doctrine of collateral estoppel" requires that the staff's post-hearing brief, as it relates to the proper construction of claim terms in dispute, be stricken because the staff participated in the Samsung investigation. (CBr at 13.)

It is not disputed that the respondents in this investigation are different from any respondent in the Samsung investigation, as complainant has recognized. (CBr at 20.) Moreover, an "agency is free to change prior rulings and decisions so long as such action is not done capriciously or arbitrarily." See 5 Jacob A. Stein, Administrative Law § 40.02 (2005); see also NLRB v. J. Weingarten Co., 420 U.S. 251, 265 (1975) ("We agree that earlier precedents do not impair the validity of the Board's construction [of a statutory provision]."); Memorandum from the General Counsel to the Commission, "The Status of An Unreviewed Initial Determination,"

GC-G-306, 1983 WL 2068656 (Nov. 28, 1983) ("It is [a] well-established principle of administrative law that while an agency may not depart from prior practice without explaining to the parties its reasons for the difference in treatment, an agency is not bound by its own prior determinations. There is no doctrine of stare decisis in administrative practice."). Hence the administrative law judge rejects any argument by complainant that respondents are bound by any result in the Samsung investigation.[3]

The administrative law judge further rejects any argument by complainant that any post hearing submission of the staff be stricken. The staff is not a party whose products will be excluded if SanDisk succeeds in this investigation. Rather the staff's role, as a third party, is to represent the public interest in a dispute otherwise between private parties. As a party in the investigation, the staff's duty is to provide the administrative law judge and the Commission with

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[3] At the January 18, 2005 preliminary conference in this investigation, all parties, including complainant, agreed that the prior claim construction in the Samsung investigation was not binding. (See Tr. at 9 (Complainant's counsel explaining that, assuming no material change in the underlying facts or law, regarding "claim construction, [] we would argue, and I think properly, that the prior decision would be persuasive, although ultimately not binding on Your Honor.") (emphasis added)).

In addition on June 15, 2005, complainant's counsel filed a Petition for Review of Final Initial and Recommended Determinations (Petition) on behalf of respondents in In the Matter of Certain Optical Disk Controller Chipsets and Products Containing Same, Including DVD Players and PC Optical Storage Devices, Inv. No. 337-TA-506. In the Petition, it argued that "[t]he prior decision of the Commission in the 409 investigation should have no effect in the present investigation." (Petition at 26 (emphasis added).) It further stated that both the respondents and the staff are in agreement that the prior decision of the Commission was "not in any sense binding." (Id. at 27.) Moreover complainant in its post-hearing brief recognized that "there is no res judicata or collateral estoppel" arising from the Samsung investigation. (CBr at 20.)

the viewpoint of a disinterested observer.[4]

V. Technology Involved

The technology at issue in this investigation relates to non-volatile memory, including EEprom and flash EEprom. (Banerjee, Tr. at 482.) A memory may be volatile or non-volatile. (Banerjee, Tr. at 479-480.) Volatile memories, such as static random access memories (SRAMs) or dynamic random access memories (DRAMs), require power. Volatile, in the context of a memory, means the power supply must be kept on. If one removes power even momentarily, the stored memory is lost. In contrast, non-volatile memories will maintain data even if power is removed. (Banerjee, Tr. at 479-481.) In 1989, the categories of non-volatile and volatile memories were well-known in the field. (Banerjee, Tr. at 481.)

EEprom and flash EEprom are based on metal oxide semiconductor field effect transistor, or MOSFET, technology. (Banerjee, Tr. at 482-85; CDX-72.) A MOSFET has a source, a drain, and, in between the source and drain, the channel or substrate. Above the substrate is the gate electrode or gate terminal, which is separated from the substrate by an insulator. (Banerjee, Tr. at 483-84; CDX-72.) The insulator in a MOSFET, between the substrate and the gate, is an oxide. (Banerjee, Tr. at 484; CDX-72.) In a MOSFET, applying a voltage to the gate develops an electric field across the insulator, which attracts electrons in the substrate to the surface region. That is why a MOSFET is called a "field effect" transistor. (Banerjee, Tr. at 484-86; CDX-72.)

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[4] In United States v. ITT Rayonier, Inc., 627 F2d 996 (9th Cir. 1980), cited by complainant, the Environmental Protection Agency was estopped from relitigating an enforcement action because of a prior judgment in a state court action brought by a party with which the EPA was found to be in privity. Here, in contrast, the staff is not seeking to enforce a regulation involving a general public utility.

In a MOSFET, the source voltage is also the voltage applied to the source terminal. The drain voltage is the voltage applied to the drain terminal. The gate voltage is the voltage that is applied to the gate terminal. (Banerjee, Tr. at 485-86; CDX-72.) A MOSFET further includes a fourth terminal, in addition to the source terminal, drain terminal, and gate terminal. (Banerjee, Tr. at 486; CDX-72.)

In general, the term "substrate" in the art refers to the silicon wafer or disk on which integrated circuits are formed. Tanks or wells are formed in the substrate, and then transistors are formed within the tanks or wells. The term "substrate" is often used to refer to the channel, or to the tank or well, and not necessarily to the overall wafer. (Banerjee, Tr. at 537-38.) If a voltage higher than the threshold voltage is applied to the gate of a MOSFET, it attracts electrons into the substrate region, forming a conductive path between the source and the drain. (Banerjee, Tr. at 483-84; CDX-72.) Also if the gate voltage is greater than the threshold voltage, a conductive connective path will be created between the source and the drain. Then, if a voltage (often referred to as VCC or VDD) is applied to the drain, current will flow from the drain to the source. (Banerjee, Tr. at 486-88; CDX-158.) However, if the gate voltage is less than the threshold voltage, no conductive connective path will be created between the source and the drain. Then, even if a voltage is applied to the drain, no current will flow from the drain to the source. (Banerjee, Tr. at 486-87; CDX-158.)

An EEprom cell is similar to a MOSFET, except that it includes a "floating" gate between the control gate and the substrate or channel. (Banerjee, Tr. at 488-89; CDX-73.) In the context of transistors and EEproms, people often refer to the channel region between the source and the drain as the "substrate." (Banerjee, Tr. at 537-38). In an EEprom cell, the floating gate is isolated

by oxide below and above the floating gate. (Banerjee, Tr. at 488-89; CDX-73.)

Electrons can be placed on the floating gate of an EEprom cell by applying appropriate voltages to different terminals. (Banerjee, Tr. at 488-89; CDX-73.) If electrons are placed on the floating gate of an EEprom cell, they will stay there, because the electrons are isolated by the oxides all around. (Banerjee, Tr. at 488-89; CDX-73). Electrons will stay on the floating gate of an EEprom cell, even if power is removed, for ten years or longer. (Banerjee, Tr. at 488-89; CDX-73.) In a programmed EEprom cell, electrons are trapped on the floating gate, and isolated by the insulators that surround the floating gate. (Banerjee, Tr. at 489-24; CDX-159.) Voltage cannot be applied directly to the floating gate in an EEprom, because the floating gate has no external connection. However, the voltage on the floating gate can be indirectly affected by the control gate voltage. (Banerjee, Tr. at 489-90; CDX-159.) The threshold voltage of an EEprom will be higher if electrons are placed on the floating gate. If there are no electrons trapped on the floating gate, the threshold voltage will be lower. (Banerjee, Tr. at 493-95; CDX-76.)

As for the basic structure and operation of an EEPROM, NOR and NAND are both ways of arranging EEprom memory cells in an array consisting of rows and columns. (Banerjee, Tr. at 479.) In a NOR flash array, the cells are arranged in rows and columns. The rows are connected with wordlines, and the columns with bitlines. NAND architectures similarly include wordlines for the rows, and bitlines for the columns. (Banerjee, Tr. at 493; CDX-98; CDX-99.) A NOR EEprom array has each memory cell at the intersection of a wordline and a bitline. The cells can therefore be accessed individually, rather than sequentially. NOR architecture is less dense than NAND architecture. (Banerjee, Tr. at 478-79; CDX-98.) A main distinction between NOR and NAND is that in NOR, any cell can be accessed randomly, while in NAND, cells must be

accessed sequentially. However, NOR is much less dense than NAND. (Banerjee, Tr. at 478-79; CDX-98; CDX-99.)

Programming EEPROMs refers to adding electrons to the floating gate of an EEprom cell. (Banerjee, Tr. at 490-91; CDX-160.) An EEprom cell can be programmed by applying suitable high voltages to various terminals, such as the drain or the control gate, to create high electric fields. These fields enable the electrons to go from the substrate to the floating gate. (Banerjee, Tr. at 490-91, 495; CDX-160.) When an EEprom cell is programmed, the threshold voltage is higher because there are electrons in the floating gate. When the EEprom cell is not programmed, the threshold voltage is lower. (Banerjee, Tr. at 493-95; CDX-76.) The threshold voltage is the minimum voltage required to turn the EEprom transistor on, so that it conducts. (Banerjee, Tr. at 495-96; CDX-75; CX-1 at 1.) Each threshold voltage level within the threshold window can be used to define a definite memory state within the cell. (Banerjee, Tr. at 495-96; CDX-75; CX-1 at 1.) Threshold voltages that can be changed in an EEprom can be used to represent memory states in an EEprom cell. (Banerjee, Tr. at 498-500; CDX-77; CX-1 at Figures 6 and 7A, and 8.) The more electrons added to the floating gate, the higher the threshold voltage. (Banerjee, Tr. at 500; CDX-77; CX-1 at Figures 6 and 7A, and 8.) Threshold voltages can be used to represent binary states in a non-volatile memory cell.

With reference to EEPROM programing mechanisms, both Fowler-Nordheim tunneling and hot electron injection were well known as of April 13, 1989,[5] and had in fact been known for decades prior to that time. (Banerjee, Tr. at 515; Subramanian, Tr. at 1494.) An EEprom will

[5] The application that issued as the '338 patent is a continuation-in-part of an abandoned application filed on April 13, 1989.

conduct if a control gate voltage, greater than some known fraction of the threshold voltage, is applied to the control gate. (Banerjee, Tr. at 493-95; CDX-76.) An EEprom will not conduct if a control gate voltage that is less than some known fraction of the threshold voltage is applied to the control gate. (Banerjee, Tr. at 493-95; CDX-76.) An EEprom cell is read by applying suitable voltage conditions to determine whether or not there are electrons trapped on the floating gate. (Banerjee, Tr. at 495-511; CDX-76.) During a read operation, a suitable control gate voltage is applied. If the applied voltage is lower than the threshold voltage programmed in the cell, the transistor will not conduct. If the applied voltage is greater than the threshold voltage, the cell will conduct. That is how the threshold voltage in the cell is inferred, and, therefore, how the different memory states are distinguished. (Banerjee, Tr. at 504-05; CDX-76.) Erasing an EEPROM cell is the opposite of programming: erasing involves removing electrons from the floating gate. (Banerjee, Tr. at 535-36.)

VI. Claims In Issue

Claims 27, 28, and 32 of the '338 patent are at issue. Claims 27 and 32 are independent claims. Claim 28 depends from claim 27. Claim 27 reads:

> In an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip, the memory cell being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltage conditions for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions, a system for programming data to EEprom cells including means for temporarily storing a chunk of data for programming a plurality of addressed cells, means for programing in parallel the stored chunk of data into the plurality of addressed cells, and means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data, wherein the improvement

comprises:

> means for inhibiting further programming of correctly verified cells among the plurality of addressed cells; and
>
> means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly.

(CX-1, '338 patent, col. 26, lns. 28-54.) Claim 28 reads:

> The system for programming the EEprom cells as in claim 27, wherein the system resides on the EEprom integrated circuit chip.

(CX-1, col. 26, lns. 55-57.) Claim 32, after re-examination, reads:

> In an array of addressable semiconductor electrically erasable and programmable memory (EEprom) cells on an integrated circuit chip, the memory cells being of the type having a source, a drain, a control gate and an erase electrode receptive to specific voltages for reading, programming and erasing of data in the cell, and having a floating gate capable of retaining a specific charge level corresponding to a specific memory state of the cell, such that a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions, a system residing on the EEprom integrated circuit chip for programming data to EEprom cells including means for temporarily storing a chunk of data for programming a plurality of addressed cells, means for programming in parallel the stored chunk of data into the plurality of addressed cells, and means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data, wherein the improvement comprises:
>
> means for enabling further programming and verifying in parallel to one or more of the addressed cells until all the plurality of addressed cells are verified; and
>
> means on chip for individually inhibiting programming of any addressed cell already verified until all of the addressed cells are verified, while enabling further programming in parallel to all other addressed cells not yet verified.

(CX-1, Re-exam certificate, col. 2, lns. 27-32.)

VII. Claim Interpretation

Claim interpretation is a question of law. Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), aff'd, 517 U.S. 370 (1996); see Cybor Corp. v. FAS Techs., Inc., 138 F.3d 1448, 1455 (Fed. Cir. 1998). In construing claims, the court should first look to intrinsic evidence consisting of the language of the claims, the specification and the prosecution history as it "is the most significant source of the legally operative meaning of disputed claim language." Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996); see Bell Atl. Network Servs., Inc. v. Covad Communications Group, Inc., 262 F.3d 1258, 1267 (Fed. Cir. 2001).

The claims themselves "provide substantial guidance as to the meaning of particular claim terms." Phillips v. AWH Corporation 415 F.3d 1303, 1314 (Fed. Cir. 2005), citing Vitronics, 90 F.3d at 1582. It is essential to consider the claim as whole when construing each term, because the context in which a term is used in a claim "can be highly instructive." Id. This requirement is consistent with the Federal Circuit's guidance that a claim term can only be understood "with a full understanding of what the inventors actually invented and intended to envelop with the claim." Phillips, 415 F.3d at 1316, citing Reneshaw PLC v. Marposs Societa' Per Azioni, 158 F.3d 1243, 1250 (Fed. Cir. 1998). Moreover, "the context in which a term is used in the asserted claim can be highly instructive." Phillips, 415 F.3d at 1314. Claim terms "are generally given their ordinary and accustomed meaning." Vitronics, 90 F.3d at 1582.

The ordinary meaning of a claim term may be determined by reviewing a variety of sources, which may include the claims themselves, dictionaries and treatises, and the written description, the drawings and the prosecution history. Ferguson Beauregard/Logic Controls v.

Mega Sys., LLC, 350 F.3d 1327, 1338 (Fed. Cir. 2003). However the use of a dictionary may extend patent protection beyond what should properly be afforded by an inventor's patent. Also there is no guarantee that a term is used in the same way in a treatise as it would be by a patentee. Phillips 415 F.3d at 1322. Moreover, the presumption of ordinary meaning will be "rebutted if the inventor has disavowed or disclaimed scope of coverage, by using words or expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope." ACTV, Inc. v. Walt Disney Co., 346 F.3d 1082, 1091 (Fed. Cir. 2003).

The specification of a patent "acts as a dictionary" both "when it expressly defines terms used in the claims" and "when it defines terms by implication." Vitronics, 90 F.3d at 1582. For example, the specification "may define claim terms by implication such that the meaning may be found in or ascertained by a reading of the patent documents." Phillips, 415 F.3d at 1323, quoting Iredto Access, Inc. v. Echostar Satellite Corp., 383 F.3d 1295, 1300 (Fed. Cir. 2004). Importantly, "the person of ordinary skill in the art is deemed to read the claim term not only in context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." Phillips, 415 F.3d at 1314. The Federal Circuit has explained that "although the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments." Phillips, 415 F.3d at 1323.

The prosecution history, including "the prior art cited," is "part of the 'intrinsic evidence.'" Phillips, 415.F3d at 1317. The prosecution history "provides evidence of how the inventor and the PTO understood the patent." Id. The prosecution history includes any reexamination of the patent. Intermatic Inc. v. Lamson & Sessions Co., 273 F.3d 1355, 1367

(Fed. Cir. 2001).

In addition to the intrinsic evidence, the administrative law judge may, but need not, consider extrinsic evidence when interpreting the claims. Extrinsic evidence consists of all evidence external to the patent and the prosecution history, including inventor testimony and expert testimony. This extrinsic evidence may be helpful in explaining scientific principles, the meaning of technical terms, and terms of art. See Vitronics Corp., 90 F.3d at 1583; Markman, 52 F.3d at 980. However, "[e]xtrinsic evidence is to be used for the court's understanding of the patent, not for the purpose of varying or contradicting the terms of the claims." Markman, 52 F.3d at 981. Moreover, the Federal Circuit has viewed extrinsic evidence in general as less reliable than the patent and its prosecution history in determining how to read claim terms. Phillips, 415 F.3d at 1318. Also, while extrinsic evidence may be useful, it is unlikely to result in a reliable interpretation of patent claim scope unless considered in the context of the intrinsic evidence. Phillips, 415 F.3d at 1319.

Patent claims should be construed so as to maintain their validity. However, that maxim is limited to cases in which a court concludes, after applying all the available tools of claim construction, that the claim is still ambiguous. Phillips, 415 F.3d at 1327. If the only reasonable interpretation renders the claim invalid, then the claim should be found invalid. See, e.g., Rhine v. Casio, Inc., 183 F.3d 1342, 1345 (Fed. Cir. 1999).

The parties have commented on many phrases in the claims in issue. The administrative law judge's interpretation of said phrases follows.

A. Claim phrase "erase electrode"

The phrase "erase electrode" appears in the preamble of claim 27 in issue. It does not

appear in the specification of the '338 patent. Complainant's proposed construction is "a terminal to which erase voltage conditions are applied to draw electrons off the floating gate." (See CBr at 34.) Respondents' proposed construction is "conductive strips surrounding the floating gate and serving as erase gates toward which electrons are attracted during erasure." (See RRBr at 16.) The staff's proposed construction is "a structure that is used to achieve the voltage conditions necessary to draw electrons off the floating gate (such as a terminal, plate, or other element) separate from the drain, source, or substrate." (See SBr at 17.)

The administrative law judge finds that although the claimed "erase electrode" was not a phrase in common use in 1989, each of the individual terms "erase" and "electrode" did have a plain meaning well known to a person of ordinary skill in the art.[6] An electrode in a semiconductor is a terminal that can emit or collect electrons. (CFF256, CFF 257, and CFF 259; none of which was objected to by respondents[7].) Also, a person of ordinary skill in the art was aware of what "erase" meant in the context of EEproms. (CFF 271 (undisputed).) It is uncontested that the '338 patent in issue is directed to EEproms. (CFF 115 (undisputed).) Hence, the administrative law judge finds that a person of ordinary skill in the art would interpret the phrase "erase electrode" in the context of the '338 patent in issue as an electrode that performs an

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[6] One of ordinary skill in the art relevant to the '338 patent in 1989 would have had the equivalent of a bachelor's degree in electrical engineering and a number of years of hands-on experience in nonvolatile memory. (Banerjee, Tr. at 510-11; Pathak, Tr. at 888-89; Subramanian, Tr. at 1485-86; Pricer, Tr. at 2423; Pashley, Tr. at 2147.)

[7] The administrative law judge notes that the staff has repeatedly objected to ranges of findings, without directing their objections to specific findings. For example, see pages 24-25 of SRCFF, where the staff uses a single paragraph to object to CFF 254 through CFF 270, inclusive. Such format is not in compliance with the ground rules governing the format of rebuttal findings. (See ground rules at 23-24.) Objections not directed to specific findings have little value in rebutting proposed findings.

erase of an EEprom, i.e., a terminal that attracts electrons from the floating gate in an EEprom cell. (CFF 276, 295 (undisputed).) He finds nothing in the patent specification which redefines either "electrode" or "erase." Moreover, the specification does not explicitly define or limit the phrase "erase electrode." It is further undisputed that at the time the '338 patent in issue was filed, it was known that a substrate or source of an EEprom could be used to erase the cell. (CFF 276, CFF 277, 280 (undisputed).) The fact that the specification of the '338 patent in issue uses the phrase "erase gate" and the asserted claims of the '338 patent use the phrase "erase electrode" further indicate that "erase electrode" should not be limited to only an erase gate. In addition, the '344 patent (incorporated by reference into the '338 patent in issue) discloses a way to electrically erase a cell without using a separate structure. (CX-47 at col. 1, ln. 64 to col. 2, ln. 3.)[8] Also, the '338 patent in issue was subject to two reexamination requests that were consolidated into a single reexamination. (CFF 1587, 1590, 1594 (undisputed).) One of those requests was brought by a party (Samsung) with adverse interests to those of complainant.[9] The Examiner had before him Samsung's argument that an "erase electrode" is a separate structure and could be neither a source nor a substrate, on how to interpret the claim term "erase electrode." (See CFF 301, 1592-93 (not objected to in relevant part by respondents; undisputed by staff).) Also, claim 58 of the '338 patent in issue uses the term "erase gate" as an example of an "erase electrode." (CX-1.) Claim 58 was allowed by the Examiner during the reexamination.

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[8] The '344 patent discloses that "[o]ne way in which the cell is erased electrically is by transfer of charge from the floating gate to the transistor drain through a very thin tunnel dielectric. This is accomplished by application of appropriate voltages to the transistor's source, drain and control gate. Other EEprom memory cells are provided with a separate, third gate for accomplishing the erasing." (CX-47 at col. 1, ln. 64 to col. 2, ln. 3.)

[9] See also Section X,A, infra.

(CFF 302 (undisputed).)

Based on the foregoing, the administrative law judge finds, that erase electrode is properly construed as (1) a terminal to which erase voltage conditions are applied to draw electrons off the floating gate, (2) can include the substrate, and (3) is not limited to the erase gate structure of the preferred embodiment.

Respondents argued that claim 58, added during a reexamination of the '338 patent in issue, impermissibly broadens claims 27 and 32 and should not be given weight as it was a "litigation induced" change. (See RRBr at 19.) The Examiner, however, allowed claim 58 during the reexamination. (CFF 302 (undisputed).) As indicated supra, the Examiner did have contrary arguments before him on how to interpret the claim term "erase electrode." (See CFF 301, 1592, 1593 (not objected to in relevant part by respondents; undisputed by staff).) Significantly, there is evidence in the '338 specification, through incorporation by reference of the '344 patent, that there is a way to electrically erase a cell without using an erase gate.

Respondents argued that the terms "erase gate" and "erase electrode" are synonyms, basing their analysis on Pickholtz v. Rainbow Techs., Inc., 284 F.3d 1365 (Fed. Cir. 2002). (See RRBr at 18.) In Pickholz, the Court found that computer and computer system were synonymous terms, based on the fact that one term was used in the specification and the other in the claims, and that "nothing in the patent itself explicates their relation or indicates any difference in meaning." (Pickholz, at 1373.) The administrative law judge finds that the facts of that case are different from those in the instant case. Thus the specification of the '338 patent incorporates by reference the '344 patent, and therefore discloses a way to electrically erase a cell without using an erase gate. (See footnote 8, supra.) Also, claim 58 of the '338 patent uses the phrase "erase

gate" as an example of an "erase electrode." As the specification of the '338 patent shows that "erase gate" and "erase electrode" cannot be synonyms, and the claims use both terms, the administrative law judge concludes that the logic of Pickholz does not apply.

Respondents and the staff argued that if "erase electrode" could be any structure that can erase a cell, then it would be a superfluous claim limitation. (See RBr at 37; SBr at 17.) If "erase electrode" were superfluous, however, then by the same logic, source, drain, and control gate would be superfluous as well, meaning that all four terms are simply being used to describe an EEprom, which is a valid claim limitation. Moreover, the administrative law judge finds that "erase electrode" is a valid claim limitation, either as a distinct term or as part of a description of an EEprom. Thus, the administrative law judge rejects said argument of the respondents and the staff.

The staff argued that the '338 patent in issue teaches away from using the substrate as an "erase electrode," arguing that endurance-related stress is increased when the substrate is used for both programming and erasing. (See SBr at 18-19.) The '338 patent in issue however does not suggest having a separate "erase electrode" as a solution to the endurance problem discussed in the section of the patent quoted by the staff. (CX-1, col. 9, ln. 52 - col. 10, ln. 3.) Indeed, the specification does not appear to discuss any advantage to having a separate "erase electrode." Hence, the staff's argument must fail.

B. Claim phrase "a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions"

The claim phrase "a specific memory state is achieved by increment or decrement of the charge level with successive applications of programming or erasing voltage conditions" appears

in the preamble of asserted claim 27 of the '338 patent in issue. (CX-1, col. 26, lns. 36-39; CX-1, B1, col. 1, lns. 35-37.) Programming and erasing are distinct operations. (CFF 314 (undisputed).) Erasing is disclosed by the specification as a process of applying voltage to a group of cells as many times as required to reach an erase state. (See CX-1, col. 16, lns. 18-25.) Programming is described in the specification as an operation consisting of applying a voltage pulse as often as required to reach a desired programmed state. (See CX-1, col. 19, ln. 63 - col. 20, ln. 16.) The administrative law judge finds that a person of ordinary skill in the art at the time the '338 patent was filed would understand said element to require that a "memory cell of the claim (i) achieves the desired programmed state by increment of the charge level with successive applications of programming voltage conditions; (ii) achieves the erased state by decrement of the charge level with successive applications of erasing voltage conditions; or (iii) performs both of these functions."[10]

C. Claim phrase "chunk of data"

The phrase "chunk of data" appears in the preamble of asserted claim 27 of the '338 patent. Complainant argued that a "chunk of data" is "the data (typically several bytes). . ." (CRRBr at 23.) Respondents argued that a "chunk of data" is "N*L[11] bits where N is the number of addressed cells and L is the number of bits per cell." (RRBr at 20.) The staff argued that "chunk of data" should be construed as "N* L where N is the number of cells and L is the number of bits in each cell." (SBr at 21.)

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[10] Said construction was argued by complainant. (CBr at 40.) It was not opposed by respondents or the staff.

[11] The parties agree that "N*L" means N multiplied by L.

The administrative law judge finds that the construction argued by both respondents and staff for "chunk of data" stems from a description of a single embodiment in the specification. (See CX-1, col. 19, lns. 42-56.) The specification, however, discloses using "chunk of cells" for the same function, and no specific size limit is placed on "chunk of cells". (See CX-1, col. 19, lns.10-26.) For example, the '338 specification states "the program verification is optimized by programming a chunk (typically several bytes) of cells. . ." (See CX-1, col. 19, lns. 10-12.) Cells contain data. (CFF 325 (undisputed in relevant part).) The claim language itself places no limitation on "chunk of data," in any of the claims in issue. Thus, the administrative law judge finds that a "chunk of data" is typically several bytes of data.

The staff argued that because "chunk of data" is recited in only one place in the specification, that must be the only interpretation of the claim term. While the staff does not explain why the language of the claims in issue should be ignored, the staff mentions, in a footnote, that "[t]he specification refers to a 'chunk of cells' in two places. (CX 1, col. 19, lns. 10-11, 27-32)." (SBr at 21, n.10.) The staff does not attempt to explain the significance, or lack thereof, of said language.

Respondents argued that "[a] single sentence referring to a 'chunk of cells' cannot inform the claims' reference to a 'chunk of data.'" (RBr at 42 (emphasis in original).) At least two sentences in the specification of the '338 patent in issue, however, specifically mention a "chunk of cells," and there are several sentences in the same paragraph that discuss the cells in the chunk. (See CX-1, col. 19, lns. 10-26.) The "chunk of cells" language appears immediately before the "chunk of data" language in the specification, and discloses performing the same function as "chunk of data." Also, the language in the specification that is used in interpreting

the claims is not restricted to language exactly replicating that of the claims.

D. Claim phrase "means for temporarily storing a chunk of data for programming a plurality of addressed cells"

The claim phrase "means for temporarily storing a chunk of data for programming a plurality of addressed cells" appears in the preamble of claim 27 of the '338 patent in issue. (CX-1, col. 27, lns. 40-42; CX-1, B1, col. 1, lns. 39-41.)

1. Function

Complainant argued that the function of the "means for temporarily storing" element is "the data for each of the addressed cells in the 'chunk' to be programmed is temporarily stored for a limited period of time, but at least long enough to complete the programming of that cell." (CBr at 42.) Respondents argued that the function is "storing N* L bits of data for programming a plurality of addressed cells for at least long enough for programming and verification to occur." (RBr at 21.) The staff argued that the function is "to store the entire chunk of data from the time it is loaded into the latches until the program cycle ends." (SBr at 27.)

The administrative law judge finds that the word "temporarily" means for a limited period of time, and that the data being stored are the final target memory states for the cells being programmed. (CFF 328, 329 (undisputed).) The plain language of claim 27 in issue shows that the "chunk of data" must be used for programming in parallel and verifying. (CX-1, col. 26, lns. 42-46.) The language of claim 27 in issue also shows that verification is done of individual cells. (CX-1, col. 26, lns. 44-46 ("means for verifying the programmed data in each of the plurality of addressed cells. . . ").) Furthermore, the language of claim 27 in issue indicates that once a cell is correctly verified, no further programming of that cell takes place. (CX-1, col. 26, lns. 48-54.)

The specification also supports this interpretation, stating that "an inhibit circuit within the program circuit 210 selectively blocks programming to those cells whose bits are correctly verified with the programmed data bits. Thus, only the unverified cells are programmed each time." (CX-1, col. 20, lns. 11-16.) Significantly, the data to be programmed into the particular cells is what is temporarily stored. Therefore, the administrative law judge finds that a person of ordinary skill in the art at the time the '338 patent was filed would conclude that while the chunk of data need not be stored, as a whole, for the entire programming process, the data related to an individual cell must be held until that particular cells is programmed and verified.

Based on the foregoing, the administrative law judge finds that the function of the "means for temporarily storing a chunk of data . . ." to be data for each of the addressed cells in the chunk to be programmed which is temporarily stored for a limited period of time but at least long enough to complete the programming of that cell.

2. Structure

Complainant's position on corresponding structure in its CPHS was:

> [t]he structure disclosed in the specification for performing this function is the block numbered 190 in Figure 5, labeled 'Read/Program Latches and Shift Registers.' These structures are described in the '338 patent at 19:27-20:36.[12]

(CPHS at 26.) Also in its CPHS, within the infringement section, complainant argued that:

> The temporary storage page buffer (sense amp) latch of the STMicro NAND flash memory chips is also structurally equivalent to the Read/Program Latches and Shift Registers block 190 of the '338 patent. Pathak Infringement Rpt. at 23. The latches of the STMicro NAND flash memory chips and the latches and shift register of the '338 patent perform the same temporary storage function, substantially the same way to achieve substantially the same storage result.

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[12] This portion of the '338 patent specification cited above teaches that "data bits are stored in latches and shift registers 190 . . . ." (CX-1, col. 19, lns. 51-52 (emphasis added).)

(CPHS at 74 (emphasis added).) Thus, as of the time complainant submitted its CPHS, complainant took the position that the structures corresponding to the means for temporarily storing function include the read/program latches and shift registers 190 of Figure 5 of the '338 patent. At the hearing (and consistent with complainant's position set forth in its CPHS) complainant's expert Pathak indicated that the corresponding structure includes latches and shift registers. (Pathak, Tr. at 952-53; CDX-183 (equating corresponding structure with "Read/Program Data Latches and Shift Registers (block 190, FIG. 5)").)

Complainant, in contrast to its CPHS, in its CBr argued that the structure corresponding to the "means for temporarily storing" is "latches 190, which is shown in Figure 5 of the '338 patent in the box labeled 'Read/Program Latches and Shift Registers.'" (See CBr at 45-46.) Thus complainant's shift in position from a corresponding structure of both latches and shift registers to latches was first demonstrated in complainant's post-hearing brief. For example, complainant, in its CBr in the claim construction section, argued:

> At the hearing, the parties generally agreed that structure disclosed in the '338 patent as corresponding to the 'temporarily storing' means was latches 190, which is shown in Figure 5 of the '338 patent in the box labeled 'Read/Program Latches and Shift Registers.' CFF 340-344.

(CBr at 45.) Complainant, in the infringement section of its CBr, argued that:

> The structure disclosed in the specification of the '338 patent as corresponding to the claimed function of temporarily storing is the latches of block 190 in Figure 5, labeled 'Read/Program Latches and Shift Registers.' *See supra* section IV.B.3.C. The page buffer latches of the accused STMicro NAND Flash memory chips are structurally equivalent to the block 190 latches. CFF 879.
>
> While STMicro claims that "temporarily store" function requires the "chunk of data" be stored for the entire program operation, there is no real dispute between the parties regarding the structural equivalence between latches 190 of the '338 patent and page buffer latches of the STMicro NAND Flash memory chip. It is

> undisputed that STMicro NAND Flash memory chips includes a plurality of page buffer latches to temporarily store information for the page (chunk) to be programmed. CFF 860, 877, 878, 882, 883.
>
> The evidence submitted at the hearing shows that the temporary storage page buffer latches (e.g., the QB latch or LSB latch) of the STMicro NAND Flash memory chips is structurally equivalent to the Read/Program Latches and Shift Registers block 190 of the '338 patent. CFF 857, 860, 865-866, 879, 884-886.

(CBr at 88-89 (emphasis added).) In complainant's reply to ST's RBr, within the claim construction section discussing structure corresponding to the means for temporarily storing limitation, complainant argued:

> As stated in STMicro's brief, there does not appear to any genuine dispute regarding the corresponding structure to the means for temporarily storing. STMicro Br. at 45. The parties agree that (1) "a latch is a structure that stores data" and (2) "shift registers converts bits input to the EEprom device in serial fashion (one at a time) into a chunk of data that is stored in latches." STMicro Br. at 45. The parties further agree that "the shift register directs one at a time to the appropriate latch" and, except for a disagreement regarding duration, "the latch holds the bit." Id.

(CRRBr at 21 n.5 (emphasis in original).) The portion of ST's RBr referenced above in complainant's reply brief sets forth ST's position that the corresponding structure "includes at least read/program latches and shift registers 190." (RBr at 45.) It was this very portion of ST's brief that complainant cited in its CRRBr when complainant commented that "[a]s stated in STMicro's brief, there does not appear to any genuine dispute regarding the corresponding structure to the means for temporarily storing. STMicro Br. at 45." (CRRBr at 21 n.5.) Yet complainant, in that same reply brief, argued that:

> STMicro asserts, without basis, that the claims require a 'shift register' to perform the claimed temporary storing function. . . . There is nothing in the specifications [sic] that suggest or require shift registers for performing the claimed temporarily storing function.

(CRRBr at 62-63 (emphasis added).) The administrative law judge finds no explanation by complainant as to why it changed its position on the structure corresponding to the means for temporarily storing limitation, from its initial latches and shift registers position to a latches only position.

Respondents argued that the structure in issue consists of "read/program latches and shift registers 190 shown in Fig. 5." (See RBr at 43.) The staff argued that said structure consists of the read/program latches and shift registers 190 in Figure 5 of the '338 patent in issue. (See SBr at 23.)

The specification of the '338 patent discloses that the "data bits are stored in latches and shift registers 190." (See CX-1, col. 19, lns. 51-52.) Also, each of the parties point to Figure 5 as structure for this claim term. (See CBr at 45-46; RBr at 43; SBr at 23.) Thus, the administrative law judge finds that the structure corresponding to the "means for temporarily storing" is the read/program latches and shift registers 190 shown in Fig. 5.

E. Claim phrase "means for programming in parallel the stored chunk of data into the plurality of addressed cells"

The claim phrase "means for programming in parallel the stored chunk of data into the plurality of addressed cells" appears in the preamble of asserted claim 27 of the '338 patent in issue.[13] (CX-1, col. 26, lns. 42-44.)

1. Function

Complainant argued that the function of the claim element "means for programming in parallel" requires "programming for the addressed cells to take place for more than one cell at a

[13] Comparable language also appear in the body of asserted claim 27.

time, such that all cells selected for programming in accordance with a chunk of stored data receive programming conditions at the same time." (CBr at 46.) Respondents argued that the function of this element is "programming N* L data bits into N addressed cells during the same programming cycle." (RBr at 24.) The staff argued that "[p]rogramming 'in parallel' should be construed to mean programming all of the data in the chunk into the addressed cells at the same time."

The plain meaning of the claim term "programming in parallel," in the context of EEprom cells, means programming multiple cells at the same time. (CX-1, col. 26, lns. 42-44; CX-1, B1, col. 1, lns. 41-42.) Thus the specification of the '338 patent states that "in order to program the N cells, a voltage V_{pd} must be applied to each of the N cells' drain and a voltage V_{pg} applied to the control gates." (col. 20, lns. 56-58.) That nothing in the specification changes the plain meaning is also supported by undisputed expert testimony. (CFF 354 (undisputed).) Accordingly, the administrative law judge finds that a person of ordinary skill in the art at the time the '338 patent was filed would conclude that the function of "means for programming in parallel" to be programming data into more than one of the addressed cells at the same time during the same programming cycle.[14]

2. Structure

Complainant argued that the structure of "means for programming in parallel" is "block 210, labeled 'Program Circuit with Inhibit,' with source multiplexer 107 and drain multiplexer 109 providing the data path." (CBr at 47.) Respondents argued that the corresponding structure

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[14] The administrative law judge notes that there appears to be no substantive dispute between the parties regarding the function of this element, with the only exception being the construction of "chunk of data," supra.

is "the program circuit with inhibit 210 shown in Figs. 5, 14, and 17, the source mux 107 and drain mux 109 shown in Figs. 4 and 14, the local power control 180 shown in Fig. 5, and the program algorithm of Fig. 15." (RBr at 24.) The staff argued that the structure for said claim term is a source mux 107 and a drain mux 109, program circuit with inhibit 210, and read circuits 220, while the algorithm in Figure 15 of the specification is also a structure. (SBr at 28.)

Figure 14 in the specification of the '338 patent is labeled "Read/Program data paths for n Cells in Parallel" and illustrates the operation of at least source mux 107, drain mux 109, program circuit with inhibit 210, and read circuits 220. (See CX-1, Figure 14.) The specification further describes said claim term stating:

> FIG.14 illustrates the program and verify paths for a chunk of n cells in parallel. The same numerals are used for corresponding modules in the system diagram of FIG. 5. . . . The source multiplexer 107 selectively connects the N sources of one addressed chunk of cells to the source voltage V_s in line 103. Similarly, the drain multiplexer 109 selectively makes the N drains of the chunk accessible through an N-channel data path 105. The data path 105 is accessed by the program circuit with inhibit 210 during programming and by read circuits 220 during reading, program verifying or erase verifying.

(CX-1, col. 19, lns. 27-41.) Hence, the administrative law judge finds that the required structure of the claim term "means for programming in parallel" is source mux 107, drain mux 109, and program circuit with inhibit 210 as structure for this claim term. (See CX-1, Figure 14; col. 19, lns. 27-41.)

Respondents argued that local power control 180 should be a required structure for this claim phrase because the claim language states "receptive to specific voltage conditions for reading, programming, and erasing of data in the cell . . ." (CX-1, col. 26, lns. 32-34.) The specification must, however, clearly associate a structure with the performance of the function,

for said structure to be corresponding structure to said function. Cardiac Pacemakers, Inc. v. St. Jude Medical, Inc., 296 F.3d 1106, 1113 (Fed. Cir. 2002). Nothing in the specification links power control 180 to be part of the structure for the "means for programming in parallel" function.

The staff argued that read circuits 220 should also be included as corresponding structure for the "means for programming in parallel" claim term. The specification shows, however, that read circuits 220 are used only during reading, program verifying or erase verifying, while inhibit circuit 210 is used for programming. Hence, the administrative law judge finds that read circuits 220 are not corresponding structure for the means for programming in parallel.

The staff also argued that the algorithm set forth in Figure 15 of the specification of the '338 patent, identified as "an on-chip program/verify algorithm according to the present invention," is a structure that corresponds to the parallel programming means. (SBr at 28.) Figure 15 however is not a corresponding structure because there are portions of Figure 15 unrelated to the claimed parallel programming means function. Reference is made, for example, to Figure 15's step (1) (apply sector erase and verify algorithm), step (4) (read algorithm for data stored in addressed cells), and step (5) (verify read data equals program data for all addressed cells). Thus there are steps in Figure 15 that do not relate to programming in parallel. In order to qualify as a corresponding structure, the structure must not only perform the claimed function, but the specification must clearly associate the structure with performance of the function. Cardiac, 296 F.3d at 1113. Moreover section 112, ¶ 6 does not permit incorporation of structure from the written description of the patent beyond that necessary to perform the claimed function. Micro Chemical v. Great Plains Chemical, 194 F.3d 1250, 1258 (Fed. Cir. 1999). The

administrative law judge finds that the specification of the '338 patent does not associate Figure 15 with the claimed parallel programming means function.

There is a special situation in which a structure corresponding to the means element is an algorithm executed by a computer. WMS Gaming, Inc. V. International Game Tech., 184 F.3d 1339, 1344 (Fed. Cir. 1999) (Gaming); see also Tehrani v. Hamilton Medical , Inc., 331 F.3d 1355, 1362 (Fed. Cir. 2003).[15] In Gaming, the Court stated that where a patent discloses a general purpose computer or microprocessor as the structure, "[t]he instructions of the software program that carry out the algorithm electrically change the general purpose computer by creating electrical paths within the device [that] create a special purpose machine for carrying out the particular algorithm." 184 F. 3d at 1348. Thus, computers, which can be programmed to carry out a myriad of functions, whereby the program itself changes the structure of the computer by affecting its electrical paths, create a special problem in means-plus-function claim construction. Since the disclosed structure cannot in those circumstances be identified as the general purpose computer, whose structure changes according to its programmed functions, the special purpose computer programmed to perform the disclosed algorithm however must be identified. See 184 F.3d at 1348-49. Even in this special case where the structure is altered by virtue of its

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[15] In Resqnet.Com, Inc. v. Lansa, Inc. 346 F. 3d 1374 (Fed. Cir. 2003), relied on by the staff (SBr at 29), the Court referenced a portion of claim 1 of the '961 patent, viz., "means for processing said information to generate a screen identification ("ID") from said first image, said ID being generated as a function of the number, location, and length of each field in said first image said ID uniquely identifying said first image" and indicated that the language immediately following the functional language of said portion of claim 1 shows that the "claimed algorithm evaluates attributes of each (and every) field in the information to be displayed, i.e., the first image." Id. at 1377, 1379. Significantly, the algorithm in the '961 patent was so described in the specification of the '961 patent. See 346 F.3d at 1379. The description of the algorithm in the '961 patent is in distinct contrast to how Figure 15 is described in the '338 patent.

programmable nature, the structural element is construed to include only the structure programmed to perform the particular disclosed function. Hence, in this special case, where the corresponding structure is a general programmable device such as a computer or microprocessor which requires an algorithm to differentiate the claimed structure from a general programmable device, the algorithm does describe a corresponding structure. The administrative law judge finds that Figure 15 does not fit into the special case exception.[16]

F. Claim phrase "means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data"

1. Function

Complainant argued that the function of the means for verifying limitation, recited in the preamble of asserted claim 27 (CX-1),[17] is determining on a cell-by-cell basis whether the data in an individual addressed cell matches the data (in the stored chunk of data) that is targeted to be

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[16] In Harris Corporation v. Ericsson, Inc., 417 F.3d 1241 (Fed. Cir. 2005), the patentee's claim 1 included a means-plus-function limitation implemented by a microprocessor. 417 F.3d at 1253. The district court had held that a corresponding structure of a "time domain processing means" was merely a "symbol processor." The Court, in reversing the district court, held that the "symbol processor" construction does not incorporate any disclosed algorithm and hence the "time domain processing means" was not a merely a "symbol processor." It further held that the corresponding structure was a microprocessor programmed to carry out a two-step algorithm in which the processor calculates generally nondiscrete estimates and then selects the discrete value closet to each estimate. In so holding, the Court made specific reference to the detailed disclosure relating to the processor 37 in the specification of the patent that was in issue. 417 F.3d at 1254. The Court did reject the patentee's argument that the disclosed algorithm was broad enough to literally encompass one-step processes. Significantly, it relied on specific language in the specification of the patent that was in issue that characterized the "two-step process as 'the invention,' not merely an implementation of the invention." Id. The administrative law judge finds no such comparable limiting language in the specification of the '338 patent.

[17] Comparable language, relating to verifying, also appears in the body of asserted claim 27.

written into the cell. (CBr at 50.) Complainant further argued "that the term 'with' in the means-for-verifying refers to the use or participation of the temporarily stored data in the verify process"; and that "[t]he term 'with' in the claimed verify means is used in the sense of 'repairing a car with a wrench' or 'calculating sales tax with a calculator.'" (CBr at 50 (emphasis in original).)

Respondents argued that the function of the means for verifying limitation requires testing the programmed data in each of the plurality of addressed cells by comparing it with the chunk of stored data, i.e., "a bit-by-bit comparison of the data read from the memory cells with the data stored in the read/program latches 190." (RBr at 48-49.)

The staff argued that the function of the verifying means requires using stored data from the stored chunk to verify, or indicate, that the target data has been properly programmed into a memory cell. (SBr at 33.)

The '338 patent specification contains disclosures describing the function of the "means for verifying" limitation in issue, which disclosures are all made within the context of the '338 patent's teachings about the "on chip program/verify" algorithm of Figure 15. Under the heading Summary of the Invention and describing an embodiment where programming operations begin with cells in the erased state, viz., the embodiment of the Figure 15 algorithm, the '338 specification teaches that:

> According to another aspect of the present invention, where a programmed state is obtained by repetitive steps of programming and verifying from the 'erased' state, a circuit verifies the programmed state after each programming step with the intended state and selectively inhibits further programming of any cells in the chunk that have been verified to have been programmed correctly.

(CX-1, col. 3, ln. 64 - col. 4, ln. 3.[18]) With reference to the algorithm of Figure 15 and its disclosures regarding the verifying function, the '338 patent specification teaches that:

> After each programming step, the cell under programming is read to verify if the desired state has been reached. If it has not further programming and verifying will continue until it is so verified.

(CX-1, col. 18, lns. 64-68.) Further describing the Figure 15 algorithm as it relates to the verifying function, the '338 patent discloses that "[i]n FIG. 15(5), the N*L bits are compared bit by bit with the N*L program data bits from latches 190 by compare circuit 200." (CX-1, col. 20, lns. 4-7.)

Respondents argued that the function of the means for verifying limitation should be limited to requiring "use of both the programmed data in the addressed memory cells and the chunk of N*L data bits" in "a bit-by-bit comparison of data read from the memory cells with the data stored in the read/program latches 190." (RBr at 48, 49.) The portion of the '338 specification teaching a "bit-by-bit" comparison, however, relates to a single embodiment that the administrative law judge has determined is not a limitation of the asserted claims, viz., the algorithm of Figure 15. Thus, the "bit-by-bit"recitation in the '338 specification relates to the Figure 15 embodiment in which "N*L bits are compared bit by bit with the N*L program data bits from latches 190 by compare circuit 200." (CX-1, col. 20, lns. 4-7.) As seen from the construction of the claim term "chunk of data," the administrative law judge did not limit the

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[18] Other portions of the '338 specification teach that the embodiment that requires a programming operation to begin with all cells in the erased state relates to the on chip program/verify algorithm of Figure 15. (See CX-1, '338 patent, col. 19, lns. 60-63 ("As mentioned in an earlier section, prior to programming the sector, the whole sector must be erased and all cells in it verified to be in the 'erased' state (FIG. 15(1)).."); col. 18, lns. 62-64 ("programming of an EEprom cell to a desired state is preferably programmed in small steps starting from the 'erase' state").)

term chunk of data to N*L bits of data. Moreover, there is nothing in the language of asserted claim 27 or claim 32 that would suggest to a person of ordinary skill in the art that any verifying function must be limited to being performed on a "bit-by-bit" basis and neither claim includes the "bit-by-bit" phrase. Accordingly, the administrative law judge finds that the means for verifying function is not limited to "a bit-by-bit comparison of data read from the memory cells with the data stored in the read/program latches 190."

Respondents argued that the verifying function requires a specific type of comparison, viz., "a bit-by-bit comparison of data read from the memory cells with the data stored in the read/program latches 190"; and that complainant's reliance on the doctrine of claim differentiation in connection with the addition of dependent claims 49 and 56 during the reexamination to prove that the "means for verifying" limitation does not require a comparison "is wrong as a matter of logic and as a matter of law." (RBr at 49.) Complainant, however, in its CRRBr and specifically discussing the verifying function, acknowledged that "[i]n order to determine whether an addressed cell has reached its desired state, some kind of comparison is required." (CRRBr at 33 (emphasis in original).) While complainant acknowledged that some kind of comparison is required, complainant argued that the verifying function of asserted claim 27 should be construed more broadly than the verifying limitations recited in dependent claims 49 and 56, rather than being limited to the specific bit-by-bit construction urged by respondents. (CRRBr at 33-34 (claim 49); CBr at 51-52.)

The '338 patent contains dependent claims 49 and 56, which depend from claim 27 and were added during the reexamination. (CFF 381-82 (undisputed); CX-1, col. B1, lns. 23-25.) Claim 49 adds the following limitations to the claim 27 means for verifying limitation in issue:

> wherein said means for verifying the programmed data includes means for detecting a parameter related to the charge levels of the individual programmed cells, and means for comparing the parameter detected from the individual programmed cells with at least one reference parameter related to corresponding individual bits of the chunk of data being programmed, wherein individual programmed cells are verified upon said comparison of parameters being achieved.

(CX-1, col. B2, lns. 14-22 (emphasis added).) Respondents' position on the scope of dependent claim 49 is that "[t]he specific comparison required by claim 49 is a comparison of a parameter detected from the individual programmed cells with at least one reference parameter related to corresponding individual bits of the chunk of data being programmed." (RRCFF 383A (emphasis added).) Dependent claim 56 adds the following limitation to the claim 27 means for verifying limitation in issue: "wherein said verifying means includes means for comparing the programmed data in each of the plurality of addressed cells with the chunk of stored data." (CX-1 at col. B2, lns. 51-54.) Respondents admit that claim 56 requires "a bit-by-bit comparison of the programmed data in each of the plurality of addressed cells with the chunk of stored data. . . ." (RRCFF 390.) Thus respondents' position on the scope of the means for verifying limitation contained in dependent claim 56 is identical to respondents' proposed construction of the means for verifying limitation in independent claim 27. However, "the presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim." Phillips, 415 F.3d at 1314-15. The administrative law judge finds that respondents have not established that the means for verifying limitation of independent claim 27 should be construed as narrowly as the means for verifying limitations of its dependent claims 49 and 56. Rather, the administrative law judge finds that the claimed "verifying" function recited in independent claim 27 is, necessarily, at least broad enough to encompass its

dependent claims 56 and 49.

Respondents further argued that "the addition of dependent claims [49 and 56] during reexamination was obviously a litigation-motivated strategy having nothing to do with the ostensible purpose of the reexamination and therefore is entitled to little, if any, weight in interpreting the asserted claims." (RBr at 50, citing Moleculon Research Corp. v. CBS, Inc., 793 F.2d 1261, 1270 (Fed. Cir. 1986) (a statement to the Patent Office made during litigation "might very well contain merely self-serving statements which likely would be accorded no more weight than testimony of an interested witness or argument of counsel"); Total Containment, Inc. v. Environ Products, Inc., 921 F. Supp. 1355, 1385 (E.D. Pa. 1995).) While determining the proper construction of the asserted claims in Moleculon, the Federal Circuit "ignored" statements the patentee made in a Citation of Prior Art to the PTO distinguishing the claimed invention from a prior art patent, which Citation the Federal Circuit recognized was "filed by Moleculon in the U.S. Patent and Trademark Office (PTO) . . . . one day before Moleculon filed the present suit" against defendant CBS. Moleculon, 793 F.2d at 1270-71. The Court found that the patentee's statements in the Citation shed "no additional light to our task of interpreting" the asserted claims. Id. In contrast to Moleculon, the administrative law judge has relied on issued patent claims, not any statements SanDisk submitted to the PTO during the reexam, in determining the scope of the means for verifying function. Moreover, dependent claims 49 and 56 are the result of a reexamination proceeding that was requested approximately eight years before the complaint was filed in this investigation. Cf. Moleculon, 793 F.2d at 1270-71 (Citation of Prior Art filed day before complaint filed).

In Total Containment, the district court did "not consider" a dependent claim 13 added

during reexamination "in construing the meaning of the term 'section' in claim 11," because applying the doctrine of claim differentiation and considering claim 13 the court would have found said claim 13 invalid for violation of 35 U.S.C. § 305.[19] 921 F. Supp. at 1386. The court also found that "[u]sing claim 13 to construe claim 11 would be especially inappropriate in this case, because claim 13 was added after this suit had been initiated and [defendant] EPI's products were well known to the plaintiff." 921 F. Supp. at 1385. In the present investigation, the reexamination requests for the '338 patent were filed some eight years before SanDisk filed its complaint against ST. Moreover, respondents have not demonstrated that ST's products were "well known to" SanDisk at the time the reexamination requests were filed or have respondents established any other facts supporting their allegation that the addition of dependent claims 49 and 56 "was obviously a litigation-motivated strategy." Accordingly, the administrative law judge finds that respondents have not established that dependent claims 49 and 56 are "entitled to little, if any, weight in interpreting the asserted claims" of the '338 patent.

Given that the '338 patent specification's disclosures relating to the means for verifying function are all made within the context of the Figure 15 embodiment, which the administrative law judge has found is not a limitation of the asserted claims, and that dependent claims 49 and 56 further limit the scope of the independent claim 27 means for verifying limitation in issue, the administrative law judge finds that the means for verifying function of asserted claims 27 and 32 requires determining on a cell-by-cell basis for each of the addressed cells in the chunk whether

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[19] With respect to patent claims added during reexamination, 35 U.S.C. § 305 provides that "[n]o proposed amendment . . . new claim enlarging the scope of a claim of the patent will be permitted in a reexamination proceeding under this chapter." 35 U.S.C. § 305; see Total Containment, 921 F. Supp. at 1381.

the data in an individual addressed cell matches the data that is targeted to be written into the cell, i.e., the chunk of stored data.

2. Structure

Complainant argued that the structure corresponding to the verifying function includes read circuits, e.g., sense amplifiers, for performing the claimed verifying function in the case of a binary implementation (CBr at 53; CRRBr at 36); that the '338 patent specification discloses various read circuits that can perform the claimed verifying function (Id. citing CX-1, col. 10, lns. 49-53; col. 18, lns. 18-21; Figure 5); that it is undisputed that a person of ordinary skill in the art in 1989 would understand that such read circuits include "voltage sensing sense amplifiers" and "current sensing sense amplifiers" (CBr at 54, citing CFF 400-19; see CFF 421-27); that "[a]s the Commission determined in the previous investigation, a person of ordinary skill in the art would understand that, for the binary case, the structure disclosed in Figure 11-E of the '344 patent [incorporated by reference into the '338 patent] could be reduced to a circuit with a single sense amplifier and no comparator for use in a binary device" (CBr at 55, citing CX-3 at 59032; see CFF 398-99, 411-13, 438-40); and that based on intrinsic evidence, a person of ordinary skill in the art would understand that a read circuit such as a sense amplifier without a comparator is sufficient structure to perform the recited verifying function. (CRRBr at 37; see CFF 379, 408, 411-13.)

With respect to the corresponding structure for the verifying function in a multi-state embodiment, complainant argued that the '338 patent discloses "various multi-state sense amplifiers for multi-state cells" (CBr at 63, citing CX-1, col. 12, lns. 39-59); that "[i]n addition, the '338 patent discloses a XOR comparator that can be used in conjunction with a sense

amplifier circuit" (CBr at 63, citing CX-1, col. 20, lns. 20-25; cf. CRBr at 35 (arguing that sense amplifier is a required structure, but that a comparator is optional)); and that "one example of verify circuits is the combination of the multistate sense amplifier 440 and K-L decoder 480 of Figure 9B and the compare circuitry (XOR gate 717 and NOR gate 711) of Figure 16 of the '338 patent." (CBr at 56, citing CFF 430-431; CX-1 at 20:17-36; Figure 9B; Figure 16; CDX-88.)

Respondents argued that the structure corresponding to the means for verifying limitation includes at least a read circuit to determine the state of the memory cells and a compare circuit to compare the chunk of stored data with the programmed data (RBr at 50); that the '338 patent specification makes clear that the verifying function cannot be accomplished without the read circuits 220 (as shown in Figures 5, 9A-B, 9D-I, 12A, 13C, and 14) used to read the memory cells (RBr at 51, citing CX-1, col. 8, lns. 31-36; col. 18, lns. 18-24); that Figures 9A-9I of the '338 patent disclose current-sensing sense amplifiers, not voltage-sensing read circuits (RRBr at 30); that SanDisk's argument that voltage-sensing read circuits are disclosed in the '344 patent is "meritless," as structure cannot be disclosed by reference (Id. citing Default Proof, 412 F.3d at 1298); that the '338 specification is "explicit that a compare circuit is also 'required' for a 'program verify'" (RBr at 51, citing CX-1, col. 19. lns. 51-56); that with respect to step 5 of the Figure 15 algorithm, "Verify Read Data = Program Data For All Addressed Cells," the '338 specification identifies compare circuit 200 as the structure required to perform such verify step (RBr at 51, citing CX-1, col. 20, lns. 5-7); that within compare circuit 200, XOR gates 711, 713, and 715 each perform a logical comparison of a read data bit against a write data bit; that the outputs of the individual XOR gates are then provided as inputs to NOR gate 717, which in turn indicates whether all L bits are read from a cell match all L bits from latches 190 (RBr at 52); and

that as compare circuit 200 is the only disclosed structure for performing the verify step of Figure 15, the structure corresponding to the means for verifying limitation must include a comparator to compare the programmed data from the memory cells to the programming data in temporary storage. (RBr at 52.)

Respondents further argued that SanDisk acknowledges that the '338 patent's only disclosed structure for performing a comparison in the multi-state case is a multi-state read circuit, such as that shown in Figure 9B, followed by the comparator shown in Figure 16; that nonetheless, SanDisk maintains that the compare circuit shown in Figure 16 is "optional" structure for performing the "verify" function; that neither Mehrotra's simplification of Figure 3 of CX-270 nor Banerjee's simplification thereof constitute equivalent structure to the Figure 16 compare circuit of the '338 patent; that while the "simplified" circuit shown in Figure 3 of CX-270 is directed to the binary case, SanDisk "has never even suggested that the 'verify' function could be performed in the multi-state case without a comparator" (RRBr at 34); and that the Figure 15 program algorithm is also corresponding structure for the function of verifying. (RRBr at 35.)

The staff argued that the '338 specification discloses: (1) the compare circuit 200 in Figures 5 and 16, (2) read circuit 220, and (3) latches/shift registers 190 in Figure 5 as structures associated with verifying function (SBr at 33-34); that the disclosed read circuits of the '338 patent alone, which are "current mirror read circuits" and not "voltage sense read circuits," are not capable of performing the verifying function; that while the '344 patent teaches that voltage level sensing circuits can be substituted for the current sensing circuits disclosed in the '338 specification (CX-67, col. 27, lns. 2-3), the '344 patent, like the '338 patent, discloses a

comparator that is used to determine whether a cell has reached its desired state by comparing the data obtained from the sense amplifiers with the desired reference levels (CX-67, col. 26, lns. 4-35) (SBr at 35 (noting that Default Proof held that corresponding structures cannot be incorporated by reference)); that the '338 specification discloses only verification accomplished by compare circuit 200 (Figure 16) having inputs from the read circuits 220 and read/program data latches 190 and then comparing the two inputs; and that the '338 specification expressly states that the verification function is accomplished by the XOR gates with at least one XOR gate required for binary implementation. (SBr at 37, citing CX-1, col. 20, lns. 18-10, 24-25.) The staff further argued that SanDisk's experts' "simplifications" or "hypothetical circuit" variations of the circuit depicted in Figure 16 would not work, which was agreed to by both SanDisk's and ST's experts (SBr at 39-40); that even if such "simplifications" would work, a person of ordinary skill in the art would consider the changes to the circuit of Figure 16 very substantial; that eliminating the data latches 190 removes the chunk of stored data from consideration; that eliminating the XOR gate would also be considered to be a substantial change to one of skill in the art; that the circuit depicted in Figure 16 would perform all of the requisite functions without any need for hypothetical circuits added by SanDisk's experts (SBr at 40-41); and that "the evidence of record demonstrates that the final [SanDisk] hypothetical circuit would not be considered to be 'equivalent' to Figure 16, irrespective of whether it would function or whether latch 721 were 'one-way' or 'two-way,' because that circuit would require significant changes in the layout of the circuit, leading to a decrease in space on the chip for memory cells." (SRBr at 16.)

The '338 patent specification's disclosures on the structures corresponding to the

verifying function begin under the heading "Read Circuits and Techniques Using Reference Cells" with the following:

> To accurately and reliably determine the memory state of a cell is essential for EEprom operations. This is because all the basic functions such as read, erase verify and program verify depend on it. Improved and novel read circuits 220 for the EEprom chip 130 and techniques of the present invention make multi-state EEprom feasible.

(CX-1, col. 8, lns. 30-36 (emphasis added).) In a disclosure on the use of read circuits, e.g., sense amplifiers, for determining the memory state of a cell, the '338 specification provides:

> The memory state of a cell may be determined by measuring the threshold voltageVT programmed therein. Alternatively, as set forth in co-pending patent application, Ser. No. 204,175[20], the memory state may be conveniently determined by measuring the differing conduction in the source-drain current IDS for the different states. . . . Associated with each amplifier is a corresponding reference conduction states IREF level (shown as broken curves in FIG. 8). Just as the breakpoint threshold levels (see FIGS. 6 and 7A) are used to demaracte the different regions in the threshold voltage window, the IREF levels are used to do the same in the corresponding source-drain current window. By comparing with the IREFs, the conduction state of the memory cell can be determined. Co-pending patent application, Ser. No. 204,175 proposes using the same sensing amplifiers and IREFs for both programming and reading.

(CX-1, col. 10, lns. 30-54 (emphasis added).) The '338 specification also contains teachings on the number of sense amplifiers to be used, depending on whether the user desires a binary or multi-state implementation and which is contained in the specification's general description of Figure 9A. Thus, the specification states:

> In general, if each memory cell is to store K states, then at least K - 1, or preferably K reference levels need be provided. In one embodiment, the addressed cell is compared to the K reference cells using k sense amplifiers in

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[20] Application Serial No. 204,275 corresponds to U.S. Patent No. 5,095,344 entitled "Highly Compact Eprom and Flash EEprom Devices" issued to Harari on March 10, 1992. (CX-47.) The '344 patent is incorporated by reference into the '338 patent. (See CX-1, col. 4, lns. 23-30.)

> parallel. This is preferable for the 2-state cell because of speed, but may spread the available current too thin for proper sensing in the multi-state case. Thus for the multi-state case, it is preferable to compare the addressed cell with the K reference cells one at a time in sequence.

(CX-1, col. 11, lns. 56-65 (emphasis added); see id. at col. 12, lns. 39-59.) Another portion of the '338 specification clearly links read circuits (e.g., sense amplifiers) to the verifying function by stating that "[t]he read circuits and operation described are also employed in the programming and erasing of the memory cells, particularly in the verifying part of the operation." (CX-1, col. 18, lns. 19-21 (emphasis added).)

It is not disputed that the '338 patent discloses the use of current sensing sense amplifiers. (CFF 415 (undisputed).) A current sense amplifier, such as the circuit shown in Figure 9A of the '338 patent, receives two inputs: a current from the memory cell, and a reference current. The sense amplifier compares the two currents and can determine what state the memory cell is in – that is, for the binary case, whether the cell is programmed or not. (CFF 416 (undisputed).) It is further undisputed that a person of ordinary skill would understand that only one sense amplifier and only one reference level is required to sense the correct one of two storage states in a binary memory cell. (CFF 423 (undisputed).)

Based on the foregoing, the administrative law judge finds that the '338 patent specification links the read circuit (e.g., sense amplifier) to the verifying function and further finds that a person of ordinary skill in the art would understand that at least the read circuits 220 (e.g., sense amplifiers) are required to perform said verifying function in issue. In addition, the administrative law judge finds that said person of ordinary skill would interpret a single sense amplifier, such as the sense amplifier depicted in Figure 9A, per memory cell in a binary

implementation constitutes sufficient structure to perform the verifying function based on the distinction between binary and multi-state embodiments set forth in the '338 specification. (See CX-1, col. 11, lns. 56-65; see id. at col. 12, lns. 39-59.)

Respondents argued that a comparator, in addition to the disclosed sense amplifier, is a necessary structure corresponding to the means for verifying limitation in a binary implementation. In support of their position, respondents cited, inter alia, a disclosure of the '338 specification specifically relating to step 5 of the Figure 15 algorithm: "[i]n FIG. 15(5), the N*L read bits are compared bit by bit with the N*L program data bits from latches 190 by compare circuit 200." (CX-1, col. 20, lns. 4-7.) The administrative law judge has determined that the Figure 15 algorithm is not a limitation of the asserted claims. He has further found that the function of the means for verifying limitation in issue does not require any bit by bit comparison. Accordingly, the administrative law judge finds that respondents have not established that a comparator structure is required to perform the verifying function in a binary implementation.

As for multi-state implementations, the '338 patent discloses a verify circuit that includes: (1) a comparator, shown in Figure 16; and (2) a sense amplifier, such as the sense amplifier of Figure 9B.[21] (CFF 430 (undisputed).) The Figure 16 comparator compares the data read from the cells and the data that is temporarily stored in the data latches, i.e., the data to be

[21] Figure 16 of the '338 patent "is a circuit diagram for the compare circuit according to the present invention." (CX-1, col. 5, lns. 44-45.) Figure 9B "illustrates multi-state read circuits with reference cells according to the present invention." (CX-1, col. 4, lns. 63-64.)

programmed into the cells.[22] (Id.) Accordingly, the administrative law judge finds that sense amplifier and comparator structures are necessary to perform the claimed verifying function in a multi-state implementation.

Complainant and respondents dispute whether the sense amplifier structure corresponding to the verifying function includes only current sensing sense amplifiers, expressly disclosed in the '338 specification, or whether voltage sensing sense amplifiers, disclosed in the '344 patent incorporated by reference to the '338 specification, also constitute corresponding structure. Thus, complainant's CFF 425 states:

> The '344 patent, which is incorporated by reference into the '338 patent, and is prior art to the '338 patent, explains that both voltage sense amplifiers and current sense amplifiers can be used for verifying during programming. (Banerjee, Tr. 664:18-666:6; CX-47 at 26:66-27:3, 26:66-27:3).

(CFF 425.) Respondents' rebuttal to CFF 425 consisted of the following:

> Irrelevant. "[M]aterial incorporated by reference cannot provide the corresponding structure necessary to satisfy the definiteness requirement for a means-plus-function clause." Default Proof Credit Card Sys., Inc. v. Home Depot U.S.A., Inc., 412 F.3d 1291, 1302 (Fed. Cir. 2005)

(ROCFF 425.)

It is undisputed that the '338 patent specification discloses current-sensing sense amplifiers corresponding to the verifying function. (See CFF 415 (undisputed).) In its description of the disclosed sense amplifiers, the '338 specification does make reference to the

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[22] The '338 patent specification teaches that FIG. 16 depicts "one embodiment of the compare circuit 200 of FIG. 5 in more detail." (CX-1, col. 20, lns. 17-18.) The '338 specification further describes the compare circuit 200 of FIG. 16 at col. 20, lns. 18-36.

'344 patent as disclosing an alternative method for the determining memory state of a cell.[23] (See CX-1, col. 10, lns. 30-54.) FIG. 11e of the '344 patent and its accompanying description in the '344 specification discloses current-sensing sense amplifiers. (See CX-47, FIG. 11e; col. 26, lns. 8-35.[24]) The '344 specification further discloses that:

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[23] The '338 patent incorporates by reference the disclosure of the '344 patent in the following passage:

> The subject matter herein is a further development of the EEprom array read techniques described in copending patent application Ser. No. 204,175, filed Jun. 8, 1988, by Dr. Eliyahou Harari, particularly the disclosure relating to FIG. 11e thereof. Application Ser. No. 204,175 is hereby expressly incorporated herein by reference, the disclosure with respect to the disclosure with respect to the embodiments of FIGS. 11, 12, 13 and 15 being most pertinent.

(CX-1, col. 4, lns. 23-30.)

[24] With respect to the FIG. 11e disclosure of comparator and sense amplifier structures, the '344 patent teaches:

> During read, the current through the Flash EEprom transistor is compared simultaneously (i.e., in parallel) with these four reference levels (this operation can also be performed in four consecutive read cycles using a single sense amplifier with a different reference applied, if the attendant additional time required for reading is not a concern). The data output is provided from the four sense amplifiers through four Di buffers (Do, D1, D2 and D3).
>
> During programming, the four data inputs Ii (I0, I1, I2 and I3) are presented to a comparator circuit which also has presented to it the four sense amp outputs for the accessed cell. If Di match Ii, then the cell is in the correct state and no programming is required. If however all four Di do not match all four Ii, then the comparator output activates a programming control circuit. This circuit in turn controls the bit line (VPBL) and word line (VPWL) programming pulse generators. A single short programming pulse is applied to both the selected word line and the selected bit line. This is followed by a second read cycle to determine if a match between Di and Ii has been established. This sequence is repeated through multiple programming/reading pulses and is stopped only when a match is established (or earlier if no match has been established but after a preset maximum number of pulses has been reached).

> Of course, circuits other than the one shown in Fig. 11e are also possible. For example, voltage level sensing rather than conduction level sensing can be employed.

(CX-47, col. 26, ln. 68 to col. 27, ln. 3.)

In Default Proof, the Federal Circuit affirmed a determination of indefiniteness under 35 U.S.C. § 112, ¶ 2 where the patent specification did not disclose any structure corresponding to the "means for dispensing" limitation in issue. 412 F.3d at 1302. As to the asserted patent in Default Proof, "[t]he specification names U.S. Patent No. 5,696,908 to Muehlberger ('Muehlberger patent') as its 'closest reference'. . . ." 412 F.3d at 1295. The Federal Circuit found that Gafford, an expert testifying on behalf of the patentee, testified that a "kiosk" was one structure corresponding to the means for dispensing limitation in issue. Id. at 1300-01. Concluding that said kiosk was not a disclosed structure corresponding to the means for dispensing limitation, the Federal Circuit held:

> The 'kiosk identified by Gafford cannot constitute structure for the 'means for dispensing.' Indeed, even though Gafford declared that he understood the Muehlberger patent to disclose such kiosks, the term 'kiosk' does not even appear in the Muehlberger patent. Even if Muehlberger did disclose a 'kiosk,' however, material incorporated by reference cannot provide the corresponding structure necessary to satisfy the definiteness requirement for a means-plus-function clause. See Atmel, 198 F.3d 1381. The inquiry under § 112, ¶ 2, does not turn on whether a patentee has 'incorporated by reference' material into the specification relating to structure, but instead asks first 'whether structure is described in the specification, and, if so, whether one skilled in the art would identify the structure from that description.' Id.

Default Proof, 412. F.3d at 1301 (emphasis added).

It is a fact that the disclosure of the '344 patent is incorporated by reference into the '338 specification. However, "[t]he inquiry under § 112, ¶ 2, does not turn on whether a patentee has

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(CX-46, col. 26, lns. 8-35.)

'incorporated by reference' material into the specification relating to structure, but instead asks first 'whether structure is described in the specification, and, if so, whether one skilled in the art would identify the structure from that description.'" Default Proof, 412. F.3d at 1301. The administrative law judge finds that the '338 specification itself links the disclosed current sensing sense amplifiers to the verifying function and does not disclose voltage sensing sense amplifiers. Thus, the administrative law judge finds that a person of ordinary skill in the art would interpret the current sensing sense amplifier from the '338 patent's description as the disclosed structure corresponding to the verifying function. Hence, the administrative law judge finds that voltage sensing sense amplifiers are not a disclosed structure of the '338 patent corresponding to the means for verifying function.

Complainant argued that "a simplified comparator, such as those described by ... Dr. Banerjee, is disclosed to a person of ordinary skill in the art"; that Banerjee's simplified circuits, which simplification began with the circuit of Figure 16 of the '338 patent, eliminated circuitry that would not be necessary for the binary case (see CFF 441-46, 471); that a person of ordinary skill in the art would also eliminate unnecessary circuitry (CFF 470-71, 480-84); and that therefore, the "simplified circuits" are disclosed to a person of ordinary skill in the art, and are linked to the function of verifying. (CRRBr at 38 (emphasis in original).) As seen supra, the administrative law judge has determined that the '338 specification clearly links the disclosed sense amplifiers to the verifying function in the binary case and sense amplifiers and comparators in the multi-state case. It is a fact that the "simplified circuits "are not disclosed in the specification of the '338 patent. Moreover, when analyzing a patent's disclosure for corresponding structure, "[i]t is important to determine whether one of skill in the art would

understand the specification itself to disclose the structure," and not whether said person of ordinary skill could implement some structure to accomplish the claimed function. Medical Instrumentation and Diagnostics Corp. v. Electra AB, 344 F.3d 1205, 1212 (Fed. Cir 2003) (emphasis added).[25] Accordingly, the administrative law judge finds that complainant has not established that any "simplified circuits" based on the clear disclosure of structure in the '338 patent specification constitute structure corresponding to the verifying function.

G. Claim phrase "means for inhibiting further programming of correctly verified cells among the plurality of addressed cells"

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[25] In Medical Instrumentation, while the Federal Circuit found that the district court correctly construed the function of the "means for converting limitation" to be "converting acquired images into a particular selected digital format," the Federal Circuit reversed the district court's determination that the corresponding structure included software for performing the claimed digital-to-digital conversion where said district court reasoned "because techniques for performing those conversions were known to those of skill in the art at the time the [patent] application was filed, a person of skill in the art would understand software to be a corresponding structure for the converting function." 344 F.3d at 1211, 1219. In reversing the district court, with respect to determining whether the software was clearly linked to the converting function in the specification, the Federal Circuit noted that:

> The correct inquiry is to look at the disclosure of the patent and determine if one of skill in the art would have understood that disclosure to encompass software for digital-to-digital conversion and had been able to implement such program, not simply whether one of skill in the art would have been able to write such a software program. . . . It is important to determine whether one of skill in the art would understand the specification itself to disclose the structure, not simply whether that person would be capable of implementing that structure. . . . Indeed, the requirement of looking to the disclosure to find the corresponding structure comes from section 112, paragraph 6 itself. It is not proper to look to the knowledge of one skilled in the art apart from and unconnected to the disclosure of the patent.

Medical Instrumentation, 344 F.3d at1212 (emphasis in original) (citations omitted). Thus, the Federal Circuit found that the district court incorrectly focused its inquiry on whether said person of ordinary skill would be capable of implementing an alleged corresponding structure.

The claim phrase "means for inhibiting further programming of correctly verified cells among the plurality of addressed cells" appears in the body of claim 27 of the '338 patent in issue. (CX-1, col. 26, lns. 48-50.)

1. Function

Complainant argued that the function of the "means for inhibiting" claim element is to stop, permanently, programming of an individual cell after that cell has been verified. (CBr at 64.) Respondents argued that the meaning of said function is that it stops programming of individual cells temporarily, until the next verify cycle. (RBr at 57.) The staff argued that inhibition on programing is temporary, and that "a cycle comprised of programming, verifying, and inhibiting until the programming cycle ends when all of the addressed cells are verified."[26] (SBr at 50-51.)

The specification describes the function of this claim element in several places. First, the specification describes in the Summary of Invention section that "a circuit verifies the programmed state after each programming step with the intended state and selectively inhibits further programming of any cells in the chunk that have been verified to have been programmed correctly." (CX-1, col. 3, ln. 67 - col. 4, ln. 3.) The specification of the '338 patent further teaches that "[t]he parallel programming is implemented by a selective programming circuit which disables programming of those cells in the chunk whose states have already been verified correctly" (CX-1, col. 19, lns. 13-16) and "[a]s soon as the programmed state is verified correctly, programming stops." (CX-1, col. 18, lns. 24-25.)

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[26] The parties have characterized complainant's position, as to the inhibit function, as "permanent inhibit" and respondents' and staff's positions, regarding the inhibit function, as "temporary inhibit". (See, e.g., CBr at 63-64; SBr at 56-57.)

A term used in a claim may inform how that claim is defined in a different claim. As such, claim 32 states "means . . . for individually inhibiting programming of any addressed cell already verified . . . ." (CX-1, B1, col. 1, lns. 50-51.) The Examiner had the issue of "temporary" v. "permanent" inhibit before him, where complainant took the position that the '338 patent disclosed permanent inhibit, while the prior art included temporary inhibit. (CFF 2055; CFF 2057; 2058 (undisputed in relevant part).) In fact, during the reexamination, complainant argued to the Examiner that it disclaimed coverage of temporary inhibit. (CX-3 at SDITC058210-212.) The Examiner in the reexamination proceedings also had claim 27 before him. Yet he allowed the claims to issue over the prior art. The administrative law judge agrees with the Examiner and finds nothing in the plain language of the claims to contradict the Examiner's conclusion. Thereafter the administrative law judge finds that the claim phrase in issue discloses a permanent inhibit function.

Accordingly, the administrative law judge finds that a person of ordinary skill in the art at the time the '338 patent was filed would conclude that the function of "means for inhibiting" to be terminating or inhibiting any further programming of the verified cells for the remainder of the programming operation.

2. Structure

Complainant argued that the structure for the "means for inhibiting" claim element is a "'one-way' latch for each cell in the 'chunk,' followed by the 'program circuit with inhibit.'" (CBr at 69.) Respondents argued that the structure for said claim element is a "program circuit with inhibit 210 shown in Figs. 5, 14, and 17, the source multiplexer 107 and drain multiplexer 109 shown in Figs. 4 and 14, the local power control 180, and the program algorithm of Fig. 15.

(RBr at 58.) Respondents also argued that the latch 721 is a two-way latch, and therefore that the '338 patent cannot disclose permanent inhibit, as argued by complainant. (RBr at 39-40.) The staff does not specify a structure in its SBr but argued that latch 721 in Figure 16 of the '338 patent is a two-way latch. (SBr at 47.)

Figure 16 of the '338 patent shows latch 721. "When the control signal VERIFY is true, this result is latched to a latch 721 . . . ." (CX-1, col. 20, lns. 28-30.) As per Figure 16 of the '338 patent, the n cells labeled "1st Cell Verified" through "nth Cell Verified" indicate for each of the N cells whether that cell is verified or not. Figure 16 interacts with Figure 17 in that "the signal in line 731 is from the output of the cell compare module 701 shown in FIG. 16, it follows that V*pd* will be selectively passed onto those cells which are not yet verified." (CX-1, col. 20, ln. 67 - col. 21, ln. 2.) When a program/verify cycle for a chunk of data ends, "all cell compare module's outputs such as 725, 727 are reset to the 'not-verified' state of '0'. This is achieved by pulling the node 726 to V*ss* (0 V) by means of the RESET signal in line 727 to a transistor 729." (CX-1, col. 20, lns. 45-51.) This effectively resets the latch 721. (CX-1, Figure 16.) The latch 721 must also be used as a one-way latch, as the specification does not call for latch 721 to be reset until the end of the full programming cycle. Accordingly, the administrative law judge finds that the structure associated with the claim element "means for inhibiting" is the one-way latch 721 in conjunction with the program circuit with inhibit.

H. Claim phrase "means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly"

The claim element "means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of

addressed cells are verified correctly" appears in the body of claim 27 of the '338 patent in issue. (CX-1, col. 26, lns. 51-54.)

1. Function

Complainant argued that the portion of the claim term reading "means for further programing and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells. . . ." refers to the same functions as the "means for programming in parallel," "means for verifying," and "means for inhibiting" limitations. Complainant further argued that "the term 'until all the plurality of addressed cells are verified correctly' requires the programming and verifying of unverified cells, and inhibiting of verified cells, to continue until all the cells in the chunk are verified, and then stop." (CBr at 71.) Respondents agreed with complainant concerning the requirement of the functions of the means for programming in parallel, verifying, and inhibiting, but argued that the claim term "until all the plurality of addressed cells are verified correctly" means only that "programming, verifying, and inhibiting continue at least until all of the addressed cells are verified."[27] (RBr at 44.)

The administrative law judge finds nothing in the phrase in issue that would indicate a separate analysis for the portions of the claim term relating to the "means for programming," "means for verifying," and "means for inhibiting" claim elements construed supra. The '338 specification states that "[a]fter the whole chunk of cells have been verified correctly, logic on chip communicates this fact to the controller, whereby programming of the next chunk of cells may commence." (CX-1, col. 19, lns. 20-23.) Thus, the current chunk must finish the entire programming cycle before the next chunk can start. Also, the last step described in the Figure 15

[27] The staff makes no argument concerning this claim term in its SBr and SRBr.

embodiment of the '338 patent states "All Addressed Cells are Programmed and Verified," meaning that there are no further steps after that last step. The administrative law judge further finds that the plain meaning of the claim language "continue until" is that the functions in question (i.e., programming, verifying, and inhibiting) are ongoing and then stop when the condition listed after "until" is reached; in other words, such verifying, programming, and inhibiting of the cells stops when all the addressed cells are verified correctly.

Based on the foregoing, the administrative law judge finds that the function of the claim term "means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly" requires the programming and verifying of unverified cells, and inhibiting the programming of verified cells, to continue until all the addressed cells in the chunk are verified.

2. Structure

Complainant argued that the structure of the phrase in issue includes the structure listed supra for the "means for programming," "means for verifying," "means for inhibiting" limitations, as well as the AND gate of Figure 16 of the '338 patent, or its equivalent. (CBr at 72.) Respondents agreed with the complainant that the structure required by this claim term includes the structures corresponding to the "means for programming," "means for verifying," and "means for inhibiting," but that since the function does not require any stopping point, the AND gate of Figure 16 of the '338 patent cannot be required structure. The staff made no argument concerning this claim term in their post-hearing briefs.

The specification of the '338 patent, in Figure 16, shows that AND gate 733 receives the verification signals from each of the verified cells. When all of the signals indicate that the

individual cells are verified, then AND gate 733 outputs the "All Verified" signal labeled 735. The specification further explains that "the N outputs such as 725, 727 are passed through an AND gate 733 so that its single output 735 results in a '1' when all N cells are verified and a '0' when otherwise." (CX-1, col. 20, lns. 37-40.)

Based on the foregoing, the administrative law judge finds that the structure of the claim term "means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly" includes the structures for "means for programming," "means for verifying," and "means for inhibiting," described supra, and the AND gate of Figure 16 of the '338 patent.

I. Claim 28

Dependent claim 28 depends from claim 27 and reads: "[t]he system for programming the EEprom cells as in claim 27, wherein the system resides on the EEprom integrated circuit chip." (CX-1, col. 26, lns. 55-57.) Complainant and respondents agreed that the proper construction of claim 28 is the system of claim 27 residing on the same integrated circuit chip as the EEprom. (CBr at 73; RRBr at 45.) The administrative law judge finds nothing in the specification to dispute the parties' interpretation of the plain language of the claim.

Based on the foregoing, the administrative law judge finds that the proper construction of claim 28 is the system of claim 27 residing on the same integrated circuit chip as the EEprom.

J. Claim 32 - preamble

Complainant, respondents, and the staff agree, and the administrative law judge so finds, that the preamble of claim 32 contains only insignificant differences from the preamble of claim 27. Thus, the administrative law judge finds that the construction of each claim term in the

preamble of claim 32 is identical to the construction of the corresponding claim terms in the preamble of claim 27, supra.

K. Claim phrase "means for enabling further programming and verifying in parallel to one or more of the addressed cells until all the plurality of addressed cells are verified . . . "

The claim phrase "means for enabling further programming and verifying in parallel to one or more of the addressed cells until all the plurality of addressed cells are verified . . ." is found in claim 32 of the '338 patent. (CX-1, B1, col. 1, lns. 46-48.) Complainant, respondents, and staff agree, and the administrative law judge so finds, that the construction of the phrase in issue matches the previous constructions of the "means for programming," "means for verifying," and "until all the plurality of addressed cells are verified" claim terms, supra.

L. Claim phrase "means on chip for individually inhibiting programming of any addressed cell already verified until all the addressed cells are verified, while enabling further programming in parallel to all other addressed cells not yet verified"

The claim phrase "means for enabling further programming and verifying in parallel to one or more of the addressee cells until all the plurality of addressed cells are verified . . ." is found in claim 32 of the '338 patent. (CX-1, B1, col. 1, lns. 49-53.) Complainant, respondents, and staff agree, and the administrative law judge so finds, that the construction of the phrase in issue matches the previous constructions of the "means for inhibiting," "means for programming," "means for verifying," and "until all the plurality of addressed cells are verified" claim terms, supra.

VIII. Infringement

To establish literal infringement of a claim written in means-plus-function format, the

patentee must prove that the relevant structure in the accused device performs the identical function set forth in the claim. Odetics, Inc. v. Storage Tech. Corp., 185 F.3d 1259, 1267 (Fed. Cir. 1999). Means-plus-function claiming applies only to purely functional limitations that do not provide the recited structure. See Watts v. XL Systems, Inc., 232 F.3d 877, 880-81 (Fed. Cir. 2000). Once a "functional identity" has been established, the patentee must then prove that the relevant structure in the accused device is either identical or equivalent to the corresponding structure disclosed in the patent specification. Id. Thus, "[f]unctional identity and either structural identity or equivalence are both necessary" for a finding of literal infringement. Id. (emphasis in original); see Frank's Casing Crew & Rental Tools v. Weatherford Int'l, Inc., 389 F.3d 1370, 1378 (Fed. Cir. 2004) (affirming summary judgement of non-infringement where identity of function satisfied yet accused device and disclosed corresponding structure "represent two distinct structural approaches") (citation omitted).

As for determining structural equivalence under 35 U.S.C. § 112, ¶ 6:

> the statutory equivalence analysis requires a determination of whether the 'way' the assertedly substitute structure performs the claimed function, and the 'result' of that performance, is substantially different from the 'way' the claimed function is performed by the 'corresponding structure . . . described in the specification,' or its 'result.' Structural equivalence under § 112, ¶ 6 is met only if the differences are insubstantial . . .; that is, if the assertedly equivalent structure performs the claimed function in substantially the same way to achieve substantially the same result as the corresponding structure described in the specification.

Odetics, Inc., 185 F.3d at 1267 (citations omitted) (emphasis added); see Chiuminatta Concrete Concepts, Inc. v. Cardinal Indus., Inc., 145 F.3d 1303, 1309-10 (Fed. Cir. 1998) (reversing summary judgement of infringement where accused device and disclosed structure were substantially different). The Federal Circuit has cautioned, however, that "[t]he individual

components, if any, of an overall structure that corresponds to the claimed function are not claim limitations." Odetics, Inc., 185 F.3d at 1268. "Rather, the claim limitation is the overall structure corresponding to the claimed function. This is why structures with different numbers of parts may still be equivalent under § 112, ¶ 6 thereby meeting the claim limitation." Id.; see Caterpillar Inc. v. Deere & Company, 224 F.3d 1374, 1380 (Fed. Cir. 2000) (vacating district court's summary judgement of non-infringement based on an "impermissible component-by-component analysis" for structural equivalence).

A device that does not literally infringe a patent claim may nonetheless infringe under the doctrine of equivalents. The infringement analysis under the doctrine of equivalents requires a determination of whether the differences between the recited claim element and the accused device are insubstantial, i.e. if the accused device performs substantially the same function in substantially the same way to achieve substantially the same result as that required by the particular claim element.[28] Graver Tank & Mfg. Co., Inc. v. Linde Air Prods., 339 U.S. 605, 609 (1950); see Kemco Sales, Inc. v. Control Papers Co., 208 F.3d 1352, 1365 (Fed. Cir. 2000) (discussing applicability of doctrine of equivalents to means-plus-function claims). To prove infringement under the doctrine of equivalents, a patentee must prove equivalency on a limitation-by-limitation basis, which requires "particularized testimony and linking argument." Texas Instr. Inc. v. Cypress Semiconductor Corp., 90 F.3d 1558, 1566 (Fed. Cir. 1996). Thus, Federal Circuit precedent requires that:

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[28] In addition, other "objective evidence" may be relevant to determining whether the differences between the accused device and the claimed invention are insubstantial, which "may include evidence of known interchangeability to one of ordinary skill in the art, copying, and designing around." Texas Instr. Inc. v. Cypress Semiconductor Corp., 90 F.3d 1558, 1566 (Fed. Cir. 1996).

> a patentee must . . . provide particularized testimony and linking argument as to the 'insubstantiality of the differences' between the claimed invention and the accused device or process, or with respect to the function, way, result test when such evidence is presented to support a finding of infringement under the doctrine of equivalents.

Id. As for a doctrine of equivalents infringement analysis of a claim written in means-plus-function format, "[b]ecause the 'way' and 'result' prongs are the same under both 35 U.S.C. section 112, paragraph 6 and the doctrine of equivalents test, a structure failing the 35 U.S.C. section 112, paragraph 6 test under either or both prongs must fail the doctrine of equivalents test for the same reason(s)." Kemco Sales, 208 F.3d at 1364-65 (concluding that where accused structure was not a § 112, ¶ 6 equivalent because of a substantially different way and result, said accused structure "also cannot be an equivalent under the doctrine of equivalents"), citing Chiuminatta, 145 F.3d at 1309, 1311. However, in a means-plus-function limitation, corresponding structure(s) are limited to the structure(s) disclosed in the specification and their equivalent(s). See Phillips, 415 F.3d at 1311.

A. Accused Products

The accused ST NAND flash memory products can be divided into two categories, viz. single-level cell (SLC) products, which utilize "binary" EEprom cells, i.e. cells capable of storing one bit of information, and multi-level cell (MLC) products, which utilize EEprom cells capable of storing two bits of information. (See CBr at 76; RBr at 9, 29; Pathak, Tr. at 885, 946-47.)

{

} (See CBr at 76; RBr at 29.) {

} (See CBr at 76; RBr at 29.)

There is some ambiguity in the record between the private parties as to what specific

accused ST SLC NAND flash memory products are in issue.[29] (Compare CBr at 76 with RBr at 29.) Complainant, at page 76 of its CBr, accused the following 11 ST SLC NAND flash memory chips of infringing the asserted claims of the '338 patent: "128/256 Mbit F12, 512 Mbit F12, 1 Gbit F12, Embedded USB, 128 Mbit F90 (small page), 256 Mbit F90 (small page), 512 Mbit F90 (small page), 1 Gbit F90 (small page), 512 Mbit F90 (large page), 1 Gbit F90 (large page) and 2 Gbit F90 (large page)." (CBr at 76.) Respondents, at page 29 of their RBr, argued that SanDisk accuses the following 11 ST products of infringement: "F90 128 Mbit; F90 256 Mbit; F90 512 Mbit Small Page; F90 512 Mbit Large Page; F90 1 Gbit; F90 2 Gbit; F90 4 Gbit; F12 128 Mbit; F12 256 Mbit; F12 512 Mbit; and F12 1 Gbit." (RBr at 29.) Thus, complainant makes reference to a single "128/256 Mbit F 12" product, while respondents account for separate "F12 128 Mbit" and "F12 256 Mbit" products. (Compare CBr at 76 with RBr at 29.) In addition, complainant has included an "Embedded USB" product that has not been accounted for by respondents. (See RBr at 29.) Neither complainant nor respondents make reference to any STMicroelectronics "Embedded USB" product in their proposed findings of fact.

Complainant's recitation of the accused ST SLC NAND flash memory products also included one additional F90 1 Gbit product as compared to respondents' accounting, although it is unclear whether that "additional" F90 1 Gbit product is the "small page" or "large page" version. Respondents, in their RBr and rebuttal findings, acknowledge that there is an ST "F90 1 Gbit" product at issue, but do not indicate whether said F90 1 Gbit product is the "small page" or "large page" version or if complainant accuses both versions of the F90 1 Gbit product of

[29] The staff did not address the specific accused products at issue in its post-hearing submissions.

infringing the asserted claims of the '338 patent. (RBr at 29; see e.g., CFF 604 (undisputed) ("CPX-12 at ST 21418-19 accurately depicts the page buffer in STMicro's 1 Gbit F90 NAND chip."); CFF 625-26 (undisputed) (relating to page buffer circuit for the ST F90 1 Gbit NAND chip); CFF 651 (undisputed) (specifically referencing F90 1 Gbit NAND chip).)

Further compounding the ambiguity over the specific accused ST SLC products in issue, the record contains a stipulation among the parties on importation, which appears to include at least 24 separate accused ST NAND flash memory chips. (See SX-3; CFF 222; RRCFF 222.) The record also contains a stipulation regarding representative products, which includes 10 accused ST NAND flash memory chips. (SX-6.) In addition, complainant's expert Pathak identified eight accused ST SLC products at the hearing. (See Pathak, Tr. at 865; CDX-199 (including a single "1 Gbit F90 NAND" product without reference to small/large page, but not including "Embedded USB" product).)

Based on the present record, the administrative law judge finds that at least the following ST SLC NAND flash memory products should be considered in the infringement analysis: F90 128 Mbit; F90 256 Mbit; F90 512 Mbit Small Page; F90 512 Mbit Large Page; F90 1 Gbit; F90 2 Gbit; F90 4 Gbit; F12 128 Mbit; F12 256 Mbit; F12 512 Mbit; and F12 1 Gbit. Any ST "Embedded USB" product is not at issue in this investigation. Furthermore, the administrative law judge is making no determination on whether the ST F90 1 Gbit product at issue is the small page or large page version.

Regardless of any ambiguity surrounding the specific ST SLC products at issue, it is not disputed that all of the ST SLC NAND chips have the same functionality with respect to reading and programming operations. (CFF 618 (undisputed).) For example during a page program

operation in ST's SLC NAND flash memory products, there is{

}[30] (RFF 330 (undisputed).) It is not disputed that{

} all ST F12 and F90 small page SLC NAND products operates in substantially the same way in respects relevant to this investigation. (RFF 325 (undisputed).) For example,{ } of the ST 512Mbit NAND flash part is used during the read, program, erase, and verify functions. (RFF 336 (undisputed).) The{ } of said ST 512Mbit NAND flash part has{

}.[31] (RFF 331 (undisputed); see CPX-22 at 10435.24.) The{ }of all ST F90 large page SLC NAND products operates in substantially the same way in respects relevant to this investigation. (RFF 358 (undisputed).) Like ST's 512Mbit F12 product described above, each of the ST F90 large page products performs a program operation{ }(RFF 359 (undisputed).) Although minor differences exist, the administrative law judge finds that functionality of the { } in F90 large page NAND products, with respect to reading and programming memory cells, is the same as for the{ } part in all respects relevant to this investigation. (RFF 360 (undisputed); see also SX-6.)

As for the functionality of the accused ST multi-level or MLC product, it is not disputed that the ST 4Gbit MLC NAND chip can{ } memory cell. (CFF 678

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[30] Each memory cell has a corresponding{ } in the accused ST MLC products. (Subramanian, Tr. at 1770.)

[31] The{ }of the page buffer circuit of the accused ST F90 and F12 SLC products is utilized during programming operations in the accused ST chips. (See Pathak, Tr. at 976; Subramanian, Tr. at 1772, 1775-77; CX-95 at STE 23687.)

(undisputed).) Each memory cell is{

}(CFF 679

(undisputed).) {

}(CFF 686 (undisputed).) {

}(Pathak, Tr. at

977-81; CX-2025 at ST 022087-022089.164; see Subramanian, Tr. at 1770-72.)

Other than two brief references to the MLC product, none of the private parties nor the staff has argued structure with respect to a particular accused product. Hence, in view of the foregoing, the administrative law judge is not making any differentation among the accused ST SLC products or among the accused ST MLC products when analyzing the functionality and structure of all the accused ST NAND flash memory chips.

B. Claim phrase "erase electrode"

Complainant argued that{ }of the memory cell in the accused ST products is a terminal to which erase voltage conditions are applied to draw electrons off the floating gate and therefore, the accused ST NAND flash memory chips practice the erase electrode element of asserted claims 27, 28, and 32 of the '338 patent. (CBr at 85; see CFF 786, 777, 778, 781; CRRBr at 53-54.)

Respondents argued that the asserted claims require "memory cell[s] being of the type having . . . an 'erase electrode' – a conductive strip separate from the substrate that surrounds the floating gate and which attracts electrons during erasure"; and that because none of the accused

ST products{

} the accused ST products do not satisfy the erase electrode limitation. (RBr at 71; RRBr at 50.)

The staff argued that the{ } of the memory cells in the accused ST products does not satisfy the requirements of the erase electrode limitation under respondents' proposed construction of said erase electrode term. (See SBr at 57-58; SRBr at 19-20.)

As seen in Section VII, A, supra, the administrative law judge has construed the term "erase electrode" as: (1) a terminal to which erase voltage conditions are applied to draw electrons off the floating gate; (2) can include the substrate; and (3) is not limited to the erase gate structure of the preferred embodiment of the '338 patent. Thus, the claim term does not require "a conductive strip separate from the substrate" as respondents have argued with respect to their non-infringement position. In RBr, respondents have admitted that the accused "ST NAND flash products erase their memory cells{

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(RBr at 71, citing Subramanian, Tr. at 1761-62; CX-345C at ST-E 22885.) In the portion of Subramanian's testimony cited by respondents, Subramanian did testify that the accused ST NAND flash memory products erase{ } (Subramanian, Tr. at 1761-62; see RFF 659.) Accordingly, the administrative law judge finds that the accused ST products satisfy the erase electrode limitation because said products{

}

C. Claim phrase "means for temporarily storing a chunk of data for programming a plurality of addressed cells"

At issue as to whether the accused ST products infringe the asserted claims of the '338 patent is whether the accused ST products satisfy the "means for temporarily storing a chunk of data for programming a plurality of addressed cells" limitation recited in the preamble of claim 27. As for the claimed term "chunk of data" appearing within the means limitation, the administrative law judge has also found that the term means "typically several bytes of data." The administrative law judge has also found that function of the means for temporarily storing limitation requires that "the data for each of the addressed cells in the chunk to be programmed is temporarily stored for a limited period of time, but at least long enough to complete programming of that cell." In addition, the administrative law judge has found that the '338 patent discloses that the read/program latches and shift registers 190 are the structures corresponding to the means for temporarily storing limitation. The parties dispute whether the accused ST products satisfy the means for temporarily storing limitation as to function and corresponding structure. (E.g., compare CFF 849-50 with RRCFF 849-50 (function); compare CFF 856-896 with RRCFF 895-96 (corresponding structure).)

As for the function of the means for temporary storing limitation in issue, complainant argued that the ST NAND flash memory chips include{ } that perform the temporary storage function for the "page" or "chunk" of data to be programmed; that during a page program operation, the accused ST chips{

} (CBr at 86-87; see CFF 849-55.) Complainant further

argued that ST's expert Subramanian conceded that prior to programming,{

}until the memory cell is verified as having reached its intended programming state. (CBr at 87; CRRBr at 56-60; see CRRBr at 60-62 (relating to functionality of ST 4 Gbit MLC NAND product).)

With respect to the structure of the accused ST products alleged to perform the temporarily storing function in issue, complainant argued that "the evidence admitted at the hearing shows that the temporary storage{ } of the STMicro NAND flash memory chips is structurally equivalent to the Read/Program Latches and Shift Registers block 190 of the '338 patent" (CBr at 89; see CFF 856-96; cf. CRRBr at 62-63 ("STMicro asserts, without basis, that the claims require a 'shift register' to perform the claimed temporary storing function. . . . There is nothing in the specifications [sic] that suggest or require shift registers for performing the claimed temporarily storing function."); and that ST's own technical documents "flatly contradict STMicro's claims that{ }as opposed to the claimed chunk of data to be programmed." (CRRBr at 58; see id. 59-62.)

Respondents argued that the accused ST NAND flash memory chips do not perform the "temporarily storing" function because the ST chips do not{

}

{

} (RBr at 73-76; RRBr at 58-63; see RFF 665-82.)

As to whether the accused ST products have identical or equivalent structure to the "Read/Program Latches and Shift Registers 190," respondents argued that complainant's expert Pathak admitted that he could identify no structure in the ST NAND flash memory products that is identical to the '338 patent structure identified by complainant's claim construction expert Banerjee for performing the means for temporary storing function; that SanDisk has presented no evidence that ST's NAND flash memory products contain the complete structure that SanDisk itself admits the '338 patent requires for performing the temporarily storing function, i.e. read/program latches and shift registers 190; that "SanDisk's bald assertion that{

} are equivalent structure to the 'read/program latches and shift registers 190,' with no explanation of how{

} is insufficient to overcome its failure to adduce any evidence that a shift register or its equivalent exists in ST's products"; and "[h]aving admitted in its pre-hearing brief that the structure required to perform this function is the 'read/program latches and shift registers 190' (CPHS at 26 (emphasis added)), SanDisk failed to present any evidence that ST's page buffer circuit contains a 'shift register' as required by the claims." (RBr at 80-81; RRBr at 62-63 (emphasis in original).)

The staff argued that SanDisk has failed to establish that the accused ST products satisfy the means for temporarily storing limitation as to function and corresponding structure. (SBr at 58; SRBr at 20-21.)

1. Function

Complainant submitted proposed findings CFF 849-855 to support its allegation that the accused ST products satisfy the function of the means for temporarily storing limitation. Complainant relies on two excerpts of testimony from its expert Pathak in CFF 849-855. The first excerpt includes Pathak's conclusory statement that the accused ST products satisfy the claim limitation. (CFF 849, citing Pathak, Tr. at 952-53.) Thus Pathak[32], when asked by counsel for complainant if "the accused ST NAND flash memory chips perform the function of temporarily storing a chunk of data for programming a plurality of addressed cells," replied "[y]es, they do." (Pathak, Tr. at 953.) Pathak, in the second excerpt of testimony relied on in CFF 849-855 and responding to a question from the administrative law judge, testified that the accused ST products perform a "data load" function; and that{

}is the same data that "is programmed to the memory cell." (Pathak, Tr. at 954-55.) "So if you load a 1, the memory cell gets a 1." (Id. at 955.) "[I]f I have a zero to be programmed, I have a zero{

} (Id.) In its CFF 849-855, complainant also cites to ST product specifications referencing a "data loading period," without any testimony explaining such ST documentation. (See, e.g., CFF 850, citing CX-353C at ST-E59477 (product specification for ST

[32] Complainant's expert Jagdish Pathak was qualified as an expert in non-volatile memory, including EEPROM and flash memory. (Tr. at 476.) It is not disputed that in April of 1989, Pathak was a person of ordinary skill in the art of the '338 patent. (CFF 84 (undisputed).)

F90 1Gbit NAND flash product); CFF 854, citing CX-1985 at ST-E260985 (product specification for ST F90 4Gbit MLC NAND flash product).)

As for the data loading period described by Pathak above and referenced in the ST product specifications, respondents have presented evidence that the{

} (See Subramanian[33], Tr. at 1770-72, 1776-77, 2046-47; Micheloni[34], Tr. at 1405, 1415-16; RBr at 76-77.) Thus, in the ST SLC and MLC accused products, the{

} (Micheloni, Tr. at 1413-14; Subramanian, Tr. at 1772; see also JX-15, Maccarrone[35] Dep. Tr. at 153-54.) The{

} irrespective of whether that cell is in an erased or programmed state. (See Subramanian at 1769, 1772; Micheloni, Tr. at 1413-14.) For a cell in the{

} regardless of whether that cell is in an

---

[33] Respondents' expert Dr. Vivek Subramanian was qualified as an expert in the design and operation of non-volatile memories and flash memories. (Tr. at 1477.)

[34] Dr. Rino Micheloni is employed by ST in Italy. His current position is Product Development Manager for the Development of Multilevel NAND Flash Memories. (CFF 42 (undisputed).)

[35] Since June 2002, Dr. Marco Maccarrone has been the Manager of the SLC NAND Flash Development Unit for ST. (JX-15, Tr. at 12-13.)

erased or programmed state. (Micheloni, Tr. at 1414, 1415.) The{ } in the ST accused devices will have a logic value of "0" stored in it if{ } (Micheloni, Tr. at 1413.) Conversely, the{ } will have a logic value of "1" stored in it if{ } (Id. at 1414.)

For all of the accused ST NAND flash products at issue in this investigation, the logical value "0" is used for a memory cell in the programmed state, i.e., the memory cell holds a "0." (Micheloni, Tr. at 1413, 1432; see CFF 664 (undisputed).) A memory cell in an accused ST NAND flash product uses the logical value "1" to indicate that the cell is in the erased state, i.e., the memory cell holds a "1." (CFF 663 (undisputed).)

At the hearing, respondents' expert Subramanian described a scenario that included two memory cells of an ST NAND flash product where the first cell is in the programmed state and the second cell is in the erased state. (Subramanian, Tr. at 2111; RDX-80.) Thus, the logical value for the first cell is 0 and the logical value for the second cell is 1, i.e., the cells can be referred to as containing 0-1. (Id.; see Micheloni, Tr. at 1432.) In the scenario described by Subramanian, the user wants to program the two cells such that first cell remains in the programmed state and the second cell goes from the erased state to the programmed state. (Id.) At the end of the programming operation, the first and second cells will hold the logical values 0-0, indicating that the first cell is programmed and the second cell has reached the programmed state. (Subramanian, Tr. at 2111; see Micheloni, Tr. at 1432.) To program these two memory cells in the ST accused products from a 0-1 state to a 0-0 state,{

}[36]

(Subramanian, Tr. at 2111.) Thus,{

}

(See id.)

To perform the identical function of the means for temporarily storing limitation at issue, i.e., the data for each of the addressed cells in the chunk to be programmed is temporarily stored, the accused device must temporarily store the data to be programmed into the particular memory cell(s). The "data" stored in{ } corresponding to the first cell in the ST NAND flash device in the scenario described above, however,{ } To perform the identical function recited in the means for temporarily storing limitation,{ } corresponding to the first cell in the ST NAND flash device would need{ } because the first cell in the scenario is being programmed to a logical value "0." Thus, the administrative law judge finds that the accused ST devices do not

[36] This scenario can be illustrated as follows:

	First Cell	Second Cell
Initial State (prior to programming)	0	1
{ }	{ }	{ }
Target State (after programming)	0	0

(See RDX-80.)

store the data to be programmed into the particular memory cell(s) because{

} (Micheloni, Tr. at 1413, 1415-16; Subramanian, Tr. at 1768-69, 1772.) Accordingly, the administrative law judge finds that complainant has not established that the accused ST NAND flash memory products perform the identical function recited in the means for temporarily storing limitation at issue, i.e., the data for each of the addressed cells in the chunk to be programmed is temporarily stored for a limited period of time, but at least long enough to complete programming of that cell.

Complainant argued that in a scenario "where it is desired to program '1011' into the memory cells" of an accused ST NAND flash device, Subramanian "conceded that prior to programming[,]{

} (CFF 867-68, citing Subramanian, Tr. at 2045-47.) The portion of Subramanian's testimony relied on in CFF 867-68 was elicited by counsel for complainant during cross-examination and is as follows:

> Q. Now, Dr. Subramanian - - could I have CX-2050 on the screen. Dr. Subramanian, this was an exhibit that was used at your deposition. Correct?
>
> A. Yes, I believe I spoke about this for about 15 minutes when we were talking about this.
>
> Q. Okay. And, Dr. Subramanian, I want you to assume for the purpose of my question that all the memory cells are in the erased state prior to the start of the program operation.

A. I understand.

Q. And if I wanted to program 1-0-1-1 into four memory cells in the accused ST NAND flash memory chips, what would be{
} prior to the start of programming?

A. Okay. I guess I will go through the same methodology I used to come up with this in my deposition. So the goal is to program 1, we're going to go from left to right, the goal is to program 1-0-1-1 into four - - we're talking about the SLC parts now?

Q. Yes.

A. So into four memory cells. Let's call them B1, W2, B3, B4. We are starting in the erased state, which means their initial values are 1-1-1-1.

I will constantly go from left to right, so my methodology will be consistent. So immediately{
} Clearly, if we are, we're assuming we're starting from the erased state, and certainly cells B1, B3 and B4 are going to remain in the erased state.

{

}

And if you remember the analysis I went through earlier today,{

}

And if you recall from my expert report,{

}

Q. Dr. Subramanian, if I wanted to program 1-0-1-1 into four memory cells in the accused ST NAND flash memory chips, I would{
} correct?

A. I believe I just said it is{
}

Q. So the number 1-0-1-1 which you want to program is logically identical to the 1-0-1-1 that you would{ } of the accused ST NAND flash memory chips, correct?

A. Again, I believe that is exactly what I just said.

(Subramanian, Tr. at 2045-47 (emphasis added).)

As seen from the foregoing, Subramanian makes clear that the scenario referred to in complainant's CFF 867-68 assumes that each of the four memory cells in the accused ST device begins the programming operation in the erased state. (Subramanian, Tr. at 2046.) The same is true with Pathak's testimony cited in CFF 849-55. (See Tr. at 954-55.) However, the claims of the '338 patent, as construed by the administrative law judge including the function of the means for temporary storing limitation at issue, have no requirement that all cells begin a programming operation in the erased state. As the administrative law judge's claim construction of the means for programming in parallel limitation demonstrates, the algorithm of the '338 patent's Figure 15 is one embodiment disclosed in the patent, but not a limitation of the asserted claims. Thus, the asserted claims do not require, as a limitation, the Figure 15 algorithm's requirement that all cells begin a programming operation in the erased state. (CX-1, '338 patent, col. 19, lns. 60-63 ("As mentioned in an earlier section, prior to programming the sector, the whole sector must be erased and all cells in it verified to be in the 'erased' state (FIG. 15(1))."); col. 18, lns. 62-64 ("programming of an EEprom cell to a desired state is preferably programmed in small steps starting from the 'erase' state").) {

}

{ } (See Micheloni, Tr. at 1210, 1435-36.)

As for the scenario posed to Subramanian quoted above where all four cells begin the program operation in the erased state, i.e., "1-1-1-1," Subramanian explained why{ } i.e., 1-0-1-1. Thus, Subramanian explained that one of the consequences of the ST accused products employing the logic value "0" to represent both{ } when the ST accused products begin a program operation with all cells in the erased state. (Subramanian, Tr. at 2046-47; see also Micheloni, Tr. at 1413-16, 1432.) That the logical value{ }

(Subramanian, Tr. at 2110-12; RDX-80; see Micheloni, Tr. at 1412-16; see also JX-15, Maccarrone Dep. Tr. at 153-54.) Accordingly, the administrative law judge finds that complainant has not established that the accused ST products perform the identical function recited in the means for temporarily storing limitation at issue, i.e., the data for each of the addressed cells in the chunk to be programmed is temporarily stored for a limited period of time,

but at least long enough to complete programming of that cell.

Complainant has not offered any argument or testimony relating to whether{ } is equivalent to the function of the means for temporarily storing limitation under the doctrine of equivalents. (See CBr at 86-88; CRBr at 60-62.) Hence, the administrative law judge finds that complainant has not established that the accused ST NAND flash satisfy the function of the means for temporarily storing limitation under the doctrine of equivalents.

2. Structure

Assuming the accused ST products performed the function of the means for temporarily storing a chunk of data for programming a plurality of addressed cells, complainant must establish that the relevant structure in the accused ST NAND flash products is either identical or equivalent to the corresponding structure disclosed in the '338 patent specification. Odetics, 185 F.3d at 1267. Thus, complainant must prove that the accused ST products have an identical or equivalent structure to the read/program latches and shift registers 190.

Complainant, in the infringement section of its CRBr, argued that "[t]here is nothing in the specifications [sic] [of the '338 patent] that suggest[s] or require[s] shift registers for performing the claimed temporarily storing function." (CRBr at 62-63.) Consistent with this lack of shift register structure position, none of complainant's proposed findings relating to the structure in the accused ST products references any shift register structure or equivalent. (See CFF 856-96; see also ROCFF 879 ("SanDisk failed to present any evidence that ST's page buffer circuit contains a 'shift register' as required by the claims.").) While all of complainant's proposed findings attempt to demonstrate that{ } of the ST

accused products are "structurally equivalent to latch 190 in Figure 5," complainant has not addressed the structural identity or equivalency of the accused ST products as to the disclosed shift registers of block 190 in Figure 5 of the '338 patent. Moreover, complainant has not established that{ } are an equivalent structure to "latch 190 in Figure 5." Structural equivalence requires a showing that "the assertedly equivalent structure performs the claimed function in substantially the same way to achieve substantially the same result as the corresponding structure described in the specification." Odetics, Inc., 185 F.3d at 1267 (emphasis added). As seen supra, complainant has not established that the accused ST products perform the claimed function recited in the means for temporarily storing limitation at issue. Hence, the administrative law judge finds that complainant has not established that the accused ST products contain the identical or equivalent structure disclosed in the '338 patent as required by the means for temporarily storing limitation.

D. Claim phrase "means for programming in parallel the stored chunk of data into the plurality of addressed cells"

1. Function

Respondents argued that none of the accused ST NAND flash memory products satisfy the function of the programming in parallel limitation because no ST product, (SLC or MLC) stores the claimed chunk of data. (RBr at 83-84; RRBr at 64.) As to the accused MLC product, respondents also argued that the ST MLC{

}

{ } does not satisfy "the '338 patent's parallel programming technique [that] allows for programming{ } (RBr at 83.)

Complainant argued that during a page program operation, the ST accused products will { } is programmed in parallel into the addressed page of the NAND memory array." (CBr at 89; CRRBr at 64.)

The staff argued that the accused ST products do not satisfy the means for programming in parallel limitation "because it is predicated upon satisfaction of the 'means for storing element,' which the accused chips fail to satisfy"; and that the accused MLC product{ } (SBr at 58.)

The administrative law judge has construed the "means for programming in parallel the stored chunk of data into the plurality of addressed cells" to be programming data into more than one of the addressed cells at the same time during the same programming cycle. Given the plain language of the claim, he further finds that satisfaction of the programming in parallel limitation requires programming of said "stored chunk of data." Accordingly, the administrative law judge finds that the accused ST products do not satisfy the means for programming in parallel limitation for at least the same reasons that said accused products do not satisfy the "means for temporarily storing a chunk of data for programming a plurality of addressed cells" limitation.

Assuming that the accused ST products satisfied the "means for temporarily storing"

limitation, the administrative law judge further finds that the accused ST SLC products do {

} (JX-22 at 32, 163; CX-92 at ST642; JX-15 at 41; CX-353 at ST-E 59477.) With respect to the accused MLC{

} (Subramanian, Tr. at 2074, 2076; see CFF 966 (undisputed).) While respondents and the staff argued that the{

} the function of the means for programming in parallel requires that more than one addressed cell be programmed during any given programming cycle. (RBr at 83; SBr at 58.) The administrative law judge finds the fact that the{

} is irrelevant to the infringement analysis. The means for programming in parallel requires only that more than one of the addressed cells is programmed, i.e., "receives programming conditions", during a programming cycle, which functionality complainant has demonstrated in the accused MLC device. (CFF 352 (undisputed).)

2. Structure

Assuming, arguendo, that the accused ST products performed the function of the means for programming in parallel, complainant must then establish that the relevant structure in the accused ST NAND flash products is either identical or equivalent to the corresponding structure disclosed in the '338 patent specification. Odetics, 185 F.3d at 1267. Thus, complainant must prove that the accused ST products have an identical or equivalent structure to the program

circuit with inhibit 210 and multiplexers 107 and 109 disclosed in the specification of the '338 patent. As complainant has argued that the structures in the accused ST NAND flash memory products are equivalent to the structures disclosed in the specification of the '338 patent, complainant must establish that the differences between the accused and disclosed structures are insubstantial, i.e., that "the assertedly equivalent structure performs the claimed function in substantially the same way to achieve substantially the same result as the corresponding structure described in the specification." Odetics, Inc., 185 F.3d at 1267; see Kemco Sales, 208 F.3d at 1364-65 (noting that "the 'way' and 'result' prongs are the same under both 35 U.S.C. section 112, paragraph 6 and the doctrine of equivalents test").

Complainant argued that the structures in the accused ST products used to perform the programming function are equivalent to the program circuit with inhibit 210 and multiplexers 107 and 109 (CBr at 90; CFF 958-70); that each of the accused ST products includes a program circuit with inhibit that{

} (CFF 937-39, 941-42, 963); that "[l]ike the '338 patent, the accused STMicro NAND chips use multiplexers{ } for programming" (CFF 965; CX-1 at 7:37-43); that{

} (CFF 892, 893, 946); that{

} (CFF 943, 944, 947-949); and that{

}

during programming." (CFF 943, 944.) Complainant further argued that a person of ordinary

skill in the art would find the structures disclosed in the '338 patent and the accused ST NAND chips to be structurally equivalent; that the two sets of circuitry, i.e., structures disclosed in the '338 specification and structures in the accused ST products, operate in substantially the same way, viz., "the two sets of circuitry enable parallel programming{

}

(CFF 960, 962, 931-933, 943-949); that "[t]he two sets of circuitry{ } to determine whether a memory cell will be programmed or program inhibited during a programming pulse" (CFF 934, 936, 916, 922-923, 948); that "the two sets of circuits{

} during the application of a programming pulse" (CFF 943-949); and that "[t]he parallel program circuitry of the '338 patent and the accused STMicro NAND Flash memory chips achieve the same result," "[n]amely, the two sets of circuits program a chunk (page) of data in parallel into a plurality of addressed memory cells." (CFF 912-915, 966, 969.)

With respect to structural equivalence between the accused ST products and the disclosed structures of the '338 patent, complainant further argued that Pathak identified{

} "as corresponding to the [disclosed] drain mux" (CRRBr at 71); and that "Pathak further identified that{

} as a 'source' multiplexer." (Id.)

Respondents argued that none of the accused ST NAND flash chips have structure identical or equivalent to the source mux 107 and drain mux 109; that the disclosed mux or

multiplexers are a specific structure in electrical engineering, "namely it is a 'one of many' selector" (RBr at 87; RRBr at 65, 68-71); that while SanDisk "contends that{

}

ST's NAND memory cell string are equivalent to the '338 patent's source mux 107 structure" and {

} are equivalent to the drain mux 109," "no person of ordinary skill in the art would understand{ } to be a multiplexer, because{

} (RBr at 98); and that{ } in the accused ST products that SanDisk contends is equivalent structure{

} (RBr at 90.)

The staff argued that the ST accused chips, being NAND architecture, do not have any structure that is equivalent to the source and drain multiplexers ("MUX") that constitute a part of the corresponding structure (SBr at 59; SRBr at 21); that while SanDisk contends that{

} constitute the requisite source and drain multiplexers, the combination of{

}that Pathak testified constituted a "source" MUX do not satisfy the definition of a multiplexer because that combination cannot implement the function that defines a multiplexer (a selector of one of many); that similarly, a combination of a

{

}do not constitute a "drain" MUX (SBr at 60-61); and that therefore, the accused products do not have a structure that is "equivalent" to source and drain multiplexers disclosed and described in the specification of the '338 patent under § 112, ¶ 6. (SBr at 62.)

It is not disputed that in 1989, a person of ordinary skill in the art would have been familiar with hot electron injection and{ } programming techniques. (CFF 363 (undisputed).) While the means for programming in parallel function does not require a specific method for programming (e.g., hot electron injection (HEI) or{ }, complainant does not dispute that the structures disclosed in the '338 specification corresponding to the parallel programming function relate to hot electron injection programming as opposed to{ } (See, e.g., CORFF 435, 438, 439, 441.) However complainant argued that "[a] person of ordinary skill in the art in 1989 would appreciate that{ } hot-electron injection technique disclosed in the '338 patent were interchangeable." (CFF 967.) In support, complainant cited the testimony of its expert Pathak to establish the alleged "known interchangeability" between the HEI{ } techniques and their corresponding structural requirements. See Texas Instr., 90 F.3d at 1566 (recognizing that "evidence of known interchangeability to one of ordinary skill in the art" may establish that differences between accused device and the claimed invention are insubstantial). Thus, Pathak testified:

> Q. In 1989, would a person of ordinary skill in the art consider NAND{ } and NOR [e.g., HEI] architectures to be structurally equivalent?

A. The NAND{ } and NOR [e.g., HEI] architectures, the memory architectures, they were equivalent. Initially the NAND guys were trying to make the products looking like NOR products. And the NAND - - so in my mind, to make a memory, flash memory, whether you use a NAND architecture or a NOR architecture, it is ultimately what you are trying to provide the customer. So they are interchangeable.

(Pathak, Tr. at 988-89 (emphasis added); see id. at 986-87 (characterizing "well-known" HEI and { } techniques as "interchangeable").)

Respondents' expert Subramanian, however, testified that the assertedly equivalent structures in the accused ST products perform programming operations in a way that is substantially different when compared to the structures disclosed in the specification of the '338 patent. In response to a question from the administrative law judge, Subramanian testified that:

JUDGE LUCKERN: And is it such a big distinction between the two techniques [HEI versus{ } that the products would differ, the final products would differ? Do you understand what I am asking you?

A. Yes, I understand, Your Honor. Yes, there are substantial differences. And a really easy way to understand the differences is that hose analogy. If you remember, in hot electron programming, I had this huge gush of water, and only a few small number of electrons from that gush were actually going into the floating gate. So look at how much water I'm wasting. Most of the water is just going through, and it's not going towards programming. On the other hand,{ } So that water represents power consumption, which means how long your batteries last in your digital camera.

If I use, on a cell-by-cell basis, if I try to define - - to put - - let's say to put 10 electrons into my floating gate using{ } versus putting 10 electrons into my floating gate using hot electron programming. { } So it's not a small distinction.

(Subramanian, Tr. at 1586-87 (emphasis added).)

In support of its position that the "STMicro NAND chips use a structure that is structurally equivalent to the structures disclosed in the '338 patent for parallel programming,"

complainant relied on the following testimony from its expert Pathak, wherein Pathak, referring to a page buffer circuit in the accused ST products, testified that:

> Q. Mr. Pathak, do you have an opinion regarding whether the accused ST NAND flash memory chips use structures that are structurally equivalent to the structures disclosed in the '338 patent for parallel programming?
>
> A. Yes, I have.
>
> Q. And what is that?
>
> A. They are structurally equivalent.
>
> Q. Could you explain why?
>
> A. For parallel programming to work, we have{
>
> }
>
> Q. And are the{ } controlled individually?
>
> A. The{ }
>
> Q. And are the source and drain MUXes associated with each memory cell?
>
> A. The source and the drain MUXes are associated with each memory cell.

(Pathak, Tr. at 1004-1005; CDX-229, citing CX-95 at ST-E 23866); see CFF 958, 970.) Respondents' expert Subramanian, however, indicated that the structures in the accused ST products, i.e.,{ } would{ } as opposed to the structures disclosed in the '338 specification that apply voltages on the "source drain and control gate." (Subramanian, Tr. at 1598; see also id. at 1591-92, 1597 (noting that '338 specification discloses only structures for programming in parallel via HEI).) Subramanian further testified

that implementing the source mux 107 and drain mux 109 in the architecture of the accused ST chips would be "impossible" because the structure of the accused devices{

} (Id. at 1786; see id. at 1786-1793 (explaining that accused ST products do not contain equivalent structure corresponding to means for parallel programming).)

Based on the foregoing, the administrative law judge finds that complainant has not established that a person of ordinary skill in the art would have considered the HEI{ } programming techniques and their associated structural requirements "interchangeable." He further finds that the assertedly equivalent structure of the accused ST products, i.e.,{

} in the accused devices, does not perform the claimed parallel programming function in substantially the same way as the structure that corresponds to the claimed programming means, i.e., source and drain multiplexers and program circuit with inhibit 210 of the '338 specification. Hence, the administrative law judge finds that complainant has not demonstrated that the accused ST products have equivalent structure corresponding to the means for programming in parallel limitation.

In support of complainant's structural equivalence position, complainant argued that Pathak identified{

} "as corresponding to the [disclosed] drain mux" (CRRBr at 71); and that "Pathak further identified that{

} (Id.) The relevant portion of Pathak testimony that complainant relies on to support this position is as follows:

Q Now, if we could now go to Exhibit CDX-206, I would like to talk to you a little bit more about the organization of the NAND flash memory array and the accused NAND flash memory chips.

What is shown in Exhibit CDX-2006?

A Now what we have shown here or what is shown in this slide, this is the NAND string. These are the EEPROM cells with a floating gate structure from zero to N in this particular case.

{

}

{

}

* * *

Q With respect to looking at Exhibit - - Exhibit CDX-245, under what condition will the{ } control the voltage on the drain of the memory cell during programming?

A The{ } will control during the programming operation. {

}

* * *

Q Do the accused ST NAND flash memory chips use source and drain

MUXes to connect the memory cell undergoing programming to the proper voltage conditions?

A Yes, they do.

Q Could you explain how?

A In this particular example in CDX-229,{

}

{

}

(Pathak, Tr. at 1001-02, 1003-04 (emphasis added).) Referring to Pathak's structural equivalence analysis above, respondents' expert Subramanian testified that:

Q And are the source and drain MIXes associated with each memory cell?

Do ST's NAND flash memory chips contain the structure that is required for performing the function of programming in parallel the stored chunk of data to the plurality of addressed cells?

A No, they do not.

Q What are the reasons for concluding that ST's NAND flash memory chips do not contain the same structure?

A. { }

{

}

programming.

And of course they do not use the algorithm of figure 15, which I've already pointed out.

Q Do the ST NAND flash memory products use NOR memory cells?

A No, they do not. They use NAND.

Q What difference does this make for programming?

A {

}

Q If I could bring up CX-135C on the screen.

If I could specifically bring up ST-E 82317. Do you recognize this page?

A Yes, this is the schematic representation of a NAND array in an ST part.

Q Do the ST NAND flash memory chips have any structure that is either identical to or equivalent to the SOURCE MUX structure required in the '338 patent?

A {

}

There is no structure or its equivalent in the ST parts.

Q {

}

{

}

A I understand.

Q {

}

A No, I do not, for the reasons I just stated.

a MUX is an engineering shorthand for a multiplexer.

A multiplexer has very specific requirements. It is a one of many selector.

This is not a MUX.

Q What are your reasons for concluding that this is not a multiplexer?

A Again it has to implement a one of many function. It has to implement the logical requirements of a multiplexer, which it does not.

* * * *

BY MR. DOWD:

Q { }

A I see that.

Q What is it?

A { }

Q Is that a multiplexer?

A No, that is not.

Q {
}

A I see that.

Q {
}

A I do see that.

Q What is that?

A { }

Q Is it a multiplexer?

A No, it is not.

Q Is it equivalent to a multiplexer?

A No, it is not.

Q Have you ever seen in any publication { } called a multiplexer?

A No, I have not.

* * * *

Q Why is { } not a multiplexer?

A {

}

Q {

}

A No, I do not, for the same reasons we talked about the SOURCE MUX.

Q And is there any structure -- withdrawn.

Would this structure be equivalent to a DRAIN MUX?

A No, it would not, again for the same reasons I used when I talked about the SOURCE MUX.

Q Now, let's turn to programming of an ST chip. How do ST's NAND flash memory products program a memory cell?

A { }

Q And we've talked about this some in response to questions from the bench. But briefly{ }

A {

}

Q In hot electron injection, what percentage of the electrons moving between the source and drain end up on the floating gate?

A It's typically a very small percentage on --on the order of .1 to .001 percent.

Q {

}

A {

}

Q {

}

A {

}

Q What are the reasons for these differences?

A <u>They are very different processes. The physical process is extremely different. The way hot electron programming works is we are sending a stream of electrons in a lateral direction with very high energies, and counting on some small fraction of them being deflected vertically into the floating gate</u>.

{

}

and the drain.

Q. How does hot electron injection compare to { }

A {

}

Q What practical difference does this make in the context of NAND flash memory products?

A {

}

(Subramanian, Tr. at 1786-93 (emphasis added).) Thus, while Pathak identified the assertedly equivalent structures in the accused ST products, the administrative law judge finds that Subramanian confirmed that the ST products do not perform the claimed parallel programming function in substantially the same way as the structure that corresponds to the claimed parallel programming means, i.e., source and drain multiplexers and program circuit with inhibit 210 of the '338 specification.

Based on the foregoing, the administrative law judge finds that complainant has not demonstrated that the accused ST products have equivalent structure corresponding to the means for programming in parallel limitation.

E. Claim phrase "means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data"

1. Function

Complainant argued that the accused ST NAND flash memory chips perform the means

for verifying function "by determining whether the data in each of the addressed memory cells matches its desired or target programming state" (CBr at 91; CFF 971-79; CRRBr at 76-77); that "[d]uring the verify operation,{

} (CFF 1015, 1017-1018, 1020); that{

} (CFF 1042); and that

{

} (CFF 1059). (CBr at 91-92; CRRBr at 77.)

Respondents argued that no ST page buffer circuit is{

} that the accused ST products cannot perform a verification "with the chunk of stored data" because{ } (RBr at 94-96; RRBr at 78.) As to the accused MLC product, respondents argued that the{

} (RBr at 96; RRBr at 76.)

The staff argued that complainant has failed to demonstrate that ST's accused chips satisfy the means for verifying function because said verifying function is "predicated upon the satisfaction of the 'means for programming' and the 'means for [temporarily] storing' element, which the accused chips fail to do." (SBr at 62.)

In support of its argument that the accused ST NAND flash memory chips satisfy the means for verifying function, complainant argued that said accused chips determine "whether the data in each of the addressed memory cells matches its desired or target programming state." (CBr at 91 (emphasis added).) Said means for verifying function, however, does not require a determination of whether the data in the addressed cells matches a "desired or target programming state." The administrative law judge has construed the verifying function to require determining on a cell-by-cell basis for each of the addressed cells in the chunk whether the data in an individual addressed cell matches the data that is targeted to be written into the cell, i.e., the chunk of stored data, and not whether data matches any "desired" or "target" state. (See Section VII, F, supra.) Thus, the means for verifying function involves the chunk of stored data. The administrative law judge, however, has found that the accused ST products do not satisfy the means for temporarily storing the chunk of data. (See Section VIII, C, supra.) Accordingly, the administrative law judge finds that the accused ST products do not satisfy the means for verifying limitation for at least the same reasons that said accused products do not satisfy the "means for temporarily storing a chunk of data for programming a plurality of addressed cells" limitation.

As an additional basis for non-infringement specific to the accused ST MLC product, respondents argued that said accused MLC product does not satisfy the verifying function because the{

} and that{

} (RRCFF 971M.) The administrative law judge's construction of the verifying

function, however, does not require{

} (See Section VII, F, supra.) Thus, while the administrative law judge has determined that the accused MLC device does not satisfy the verifying function for at least the same reasons that the MLC device does not satisfy the means for temporarily storing limitation, the administrative law judge finds that the MLC device's alleged failure to{ } does not, by itself, render said MLC device non-infringing.

2. Structure

Complainant argued that the structures used in the accused ST NAND flash memory chips to perform the verify function are equivalent to the sense amplifier and verify transistor disclosed in the '338 patent as corresponding to the claimed means for verifying function (CFF 980-82, 986-1002, 1034-41); that a person of ordinary skill in the art would understand that { } used in the ST products are equivalent to the current sensing sense amplifiers disclosed in the '338 patent specification (CFF 403-10); and that both current sensing sense amplifiers and{ } use the level of current conduction through the memory cell to determine the programming state of the memory cell (CFF 410-426). (CBr at 92-93; CRRBr 78-80.)

Respondents argued that the read circuits disclosed in the '338 patent use a current mirror to perform the verifying function in contrast to the accused ST NAND flash memory chips that { } that "numerous substantial differences exist between the read circuit structures of the '338 patent and the ST{ } that all of the read circuits disclosed in the '338 patent utilize current mirrors to

determined the memory state of a cell; and that{

} (RBr at 97-99; see RRBr at 81-85.)

The staff argued that the accused ST chips do not have a structural equivalent to the current sensing sense amplifiers disclosed in the '338 patent specification; and that{

} in the accused ST chips, which complainant argued are structurally equivalent, are in fact substantially different from the read circuits disclosed in the '338 patent specification. (SBr at 62-64; see SRBr at 23.)

While complainant argued that the accused ST chips use structure equivalent to the "sense amplifier and verify transistor" disclosed in the '338 patent as corresponding to the claimed means for verifying function, the administrative law judge did not find that the '338 patent specification discloses a{ } structure as corresponding to the claimed verifying function. (See Section VII, F, supra.) Complainant further argued that a person of ordinary skill in the art would understand that the{ } used in the accused ST chips are structurally equivalent to the current sensing sense amplifiers disclosed in the '338 patent specification. (CBr at 93; see CFF 407.) The administrative law judge finds that complainant has established that both{ } and current sensing sense amplifiers were known to a person of ordinary skill in the art in 1989 (CFF 403-405 (undisputed)); and that said person of ordinary skill in the art would understand that the state of a memory cell could be determined by either{ } current sensing. (CFF 406, 409 (undisputed).) However, the administrative law judge finds that complainant has not established that the assertedly equivalent{ } in the accused ST products perform the claimed verifying function in substantially the same way as the current sensing sense

amplifiers disclosed in the '338 patent specification or that said assertedly equivalent structures and disclosed structures would have been considered interchangeable to a person of ordinary skill in the art. Odetics, 185 F.3d at 1267; Texan Instr., 90 F.3d at 1566.

Complainant has relied on, inter alia, a portion of testimony from respondents' expert Subramanian where Subramanian acknowledged that one of ordinary skill in the art would understand that it was a design option to{ } current sensing sense amplifiers. (Subramanian, Tr. at 1954.) Subramanian, however, on the same hearing transcript page (Tr. at 1954) cited by complainant, explained that "[i]t is not an either/or because it depends on the constraints of your circuits. If I don't have the appropriate circuitry{ } (Id.) Subramanian further explained the differences between the assertedly equivalent and disclosed structures and testified that:

Q. To a person of ordinary skill in the art, are{ }

A. No, they are entirely different.

Q. How are{ }different from current sensing circuits?

A. { } In a current sensing circuit, you just perform everything at the same time. You do not require such sequencing of operation. { }

{ }

Q. { }

A. {

}

Q. To a person of ordinary skill in the art, how substantial are those differences?

A. Those differences are extremely substantial.

(Subramanian, Tr. at 1637-38.) Moreover, in a portion of complainant's expert Pathak's testimony that complainant relied on to bolster its structural equivalence argument, Pathak admitted that there is a difference in the way{ } sense amplifiers determine the state of a memory cell. (See Pathak, Tr. at 506-07.)

Based on the foregoing, the administrative law judge finds that complainant has not established that the accused ST chips are structurally equivalent to the structure disclosed in the '338 patent specification that corresponds to the means for verifying function.

F. Claim phrase "means for inhibiting further programming of correctly verified cells among the plurality of addressed cells"

1. Function

Complainant argued that the accused ST NAND flash memory chips practice the means for inhibiting function "by preventing any additional programming pulses from being applied to those cells that have been verified correctly for the remainder of the programming operation"; that there is no dispute that the accused ST chips permanently inhibit the programming of correctly verified cells during a page program operation; and that during a page program operation in the ST products,{

} (CBr at 93-94; see CFF 1045-56.)

Respondents argued that the accused ST products do not perform the means for verifying limitation because they do not perform the "programming" and "verifying" functions and therefore do not inhibit further "programming" of correctly "verified" cells. (RBr at 105; RRBr at 87.)

The staff argued that the accused ST products do not satisfy the means for inhibiting limitation for the same reasons that said accused products do not satisfy the means for temporarily storing, means for programming in parallel, and means for verifying limitations. (SBr at 65.)

Complainant has demonstrated that the accused ST SLC NAND flash memory chips possess an inhibiting functionality. Thus,{

} and {

} (CFF 1048, 1050 (undisputed).) In the accused SLC products,{

} (JX-27, Song Dep. Tr. at 6, 48 (5/27/05); JX-18, Mastrangelo Dep. Tr. at 56, 62 (5/24/05).)

The means for inhibiting limitation, however, requires terminating or inhibiting any further programming of the verified cells for the remainder of the programming operation. (See Section VII, G, supra.) For an accused device to satisfy the means for inhibiting limitation, the

administrative law judge finds that said accused device must also satisfy the means for programming in parallel and means for verifying limitations construed in Sections VII, E and F, respectively. In Sections VIII, D and E, supra, the administrative law judge found that the accused ST products, SLC and MLC, did not satisfy the means for programming and means for verifying limitations. Hence, for at least the reasons that the accused ST products do not satisfy the means for programming and means for verifying limitations, the administrative law judge finds that said accused products do not practice the means for inhibiting limitation.

2. Structure

Complainant argued that the structures in the accused ST NAND flash memory chips that perform the inhibit function are equivalent to the corresponding structures to the inhibit means element, viz., one-way latch 721 with reset transistor 729 in Figure 16 of the '338 patent and the program circuit with inhibit labeled 210 shown in Figure 5, Figure 14, and (for one embodiment) Figure 17 (CFF 1074-1082);{

} (CFF 1057-1062);{

} (CFF 1063, 1065-1073); that an individual of ordinary skill would consider the{

} to be equivalent to the transistor associated with the PGM signal of Figure 17 of the '338 patent (CFF 1077); that an individual of ordinary skill would consider the circuitry in the STMicro NAND Flash memory chip such as{

} to be equivalent to

the logic in the '338 patent (e.g.,{ } that connects latch 721 to the memory cell being programmed (CFF 1074-1079); and that{ } like the AND gate, assures that the inhibit voltage/signal from the latch will prevent the drain of the memory cell from receiving the necessary conditions for programming (i.e., the memory cell will be inhibited) (CFF 1076). (CBr at 94-95.)

Respondents argued that the accused ST products have no identical or equivalent structure for performing the inhibiting function for the same reasons they lack the structure required by the means for programming and means for verifying limitations. (RBr at 105; RRBr at 87.)

The staff argued that the accused ST chips do not satisfy the inhibiting limitation for at least the same reasons that said accused chips do not satisfy the means for temporarily storing, means for programming in parallel, and means for verifying limitations. (SBr at 65.)

As seen in Section VII, G, supra, the administrative law judge found that the structure corresponding to the inhibit function is a one-way latch 721 in conjunction with the program circuit with inhibit 210. The '338 specification, in its sole disclosure relating to the one-way latch 721, teaches that: "[w]hen the control signal VERIFY is true, this result is latched to a latch 721. . . ." (CX-1 col. 20, lns. 28-30.) Complainant admitted that "when the 'means for verifying' determines that a cell is verified, the result is sent to the latch 721 . . ." in support of its argument that the means for inhibiting limitation requires latch 721 as corresponding structure. (CBr at 69-70.) However, the administrative law judge has determined that the accused ST chips do not satisfy the function or structure corresponding to the means for verifying limitation. (See Section

VIII, E, supra.) Thus, with respect to any alleged structural equivalent to one-way latch 721 in the accused ST products, the administrative law judge finds that{ } would not perform the inhibiting function in substantially the same way as the disclosed latch 721 of the '338 patent specification because said{ } in the accused product does not contain{ } Furthermore, the inhibiting means limitation in issue, i.e., means for inhibiting further programming of correctly verified cells among the plurality of addressed cells, requires an inhibition on "further programming . . . . " As seen in Section VIII, D, supra, the accused ST products do not satisfy the function or structure corresponding to the means for programming in parallel.

Accordingly, the administrative law judge finds that complainant has not established that the accused ST chips possess equivalent structure corresponding to the means for inhibiting limitation.

G. Claim phrase "means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly"

1. Function

Complainant argued that the accused ST NAND flash memory chips practice the function of the means for further programming and verifying limitation; that the accused chips include a means for programming in parallel the plurality of addressed cells, a means for verifying the plurality of addressed cells, and a means for inhibiting the program operation of correctly verified cells; and that once a memory cell in the accused chips has been verified, programming of the memory cell is inhibited until the page program operation is complete. (CBr at 95-96; see CRRBr at 81.)

Respondents argued that the accused ST NAND flash memory chips do not perform the function of the means for further programming and verifying limitation for the same reasons that they do not perform the means for programming in parallel and means for verifying functions. (RBr at 106; RRBr at 88.)

The staff did not address whether the accused ST NAND flash memory chips perform the means for further programming and verifying limitation.

The administrative law judge has construed the "means for further programming and verifying . . ." limitation to require the programming and verifying of unverified cells, and inhibiting the programming of verified cells to continue until all the addressed cells in the chunk are verified. (See Section VII, H, supra.) The means for further programming and verifying necessarily includes the means for programming in parallel and means for verifying limitations that the administrative law judge construed in Sections VII, E and F, supra. As the administrative law judge has determined that the accused ST NAND flash memory chips do not satisfy the means for programming in parallel and means for verifying limitations, for at least those same reasons, the administrative law judge finds that said accused chips do not practice the "means for further programming and verifying" limitation.

2. Structure

Complainant argued that respondents' accused products include the structures associated with "means for programing," "means for verifying," and "means for inhibiting" limitations; and that{

} (CBr at 96-97.) Respondents argued that their products do not have the structures associated with the "means for programming" and "means for verifying"claim

phrases, and therefore cannot have an equivalent structure for the "means for further programing." (RBr at 106.) The staff likewise argued that respondents' products lack equivalent structure for the "means for programming" and "means for verifying" claim phrases. (SB at 58-59, 62-64.)

The administrative law judge has found that the structure of the "means for further programming" includes the structures for "means for programming," "means for verifying," and "means for inhibiting," described supra, and the AND gate of Figure 16 of the '338 patent. The administrative law judge also found that the required structures for the "means for programming," "means for verifying," and "means for inhibiting" claim phrases or their equivalents are not present in the respondents' products. (See Sections VIII, D-F, supra.) The administrative law judge finds that complainant has not established that{

} perform the claimed function in issue in substantially the same way as the disclosed AND gate, as respondents' products{

} Therefore, the administrative law judge finds that respondents' products do not contain a structure equivalent to the structure required for the "means for further programming" claim phrase.

H. Claim 28

Complainant argued that the accused ST NAND flash memory chips, for the reasons that said accused chips satisfy the limitations of claim 27, practice claim 28; and that each of the accused chip resides on a single integrated circuit chip and therefore meets the additional limitation of claim 28. (CBr at 97.)

Respondents argued that the accused ST NAND flash memory chips do not practice the

function of asserted claim 28 for at least the same reasons that said accused chips do not perform the means for programming and means for verifying functions. (RBr at 106.)

Notwithstanding its infringement arguments relating to the various means limitations of claim 27, the staff did not address separately the issue of whether the accused ST NAND flash memory chips practice asserted claim 28.

The parties have agreed and the administrative law judge has so found that the proper construction of claim 28 is the system of claim 27 residing on the same integrated circuit chip as the EEprom. (See Section VII, I, supra.) Respondents do not dispute that the structure corresponding to the functionality in the ST NAND flash memory chips that complainant has accused of infringing claim 27 resides on the same integrated circuit chip as the EEprom and thus the administrative law judge finds that the accused ST chips satisfy the "on chip" limitation of claim 28. (See Pathak, Tr. at 1052.) However, for the same reasons that the accused chips do not satisfy the preamble and improvement means limitations of claim 27, i.e., means for temporarily storing, means for programming in parallel, means for verifying, means for inhibiting, and means for further programming and verifying, the administrative law judge finds that said accused chips do not practice claim 28 of the '338 patent.

I. Claim 32 - preamble

The administrative law judge has determined that the construction for each claim term contained in the preamble of claim 32 is identical to the construction of the corresponding claim terms in the preamble of claim 27. (See Section VII, J, supra.) Hence, for the same reasons that the accused ST NAND flash memory chips do not satisfy the means for temporarily storing, means for programming in parallel, and means for verifying limitations recited in the preamble of

claim 27, the administrative law judge finds that said accused chips do not practice said means limitations recited in the preamble of claim 32 of the '338 patent. (See Sections VIII, C, D, E, supra.)

J. Claim phrase "means for enabling further programming and verifying in parallel to one or more of the addressed cells until all the plurality of addressed cells are verified"

Complainant argued that the STMicro NAND Flash memory chips perform the functions of: (1) programming in parallel the plurality of addressed cells, (2) verifying the plurality of addressed cells, and (3) further programming and verifying in parallel until all the plurality of addressed cells are verified correctly; and that said chips enable further programming of one or more addressed memory cells until all the plurality of addressed cells are verified. (CBr at 98, citing CFF 1109, 897-911, 971-972, 976-979.)

Respondents argued that the accused ST products do not perform the function required by this limitation for the same reasons that they do not perform the "programming" and "verifying" functions of claim 27. (RBr at 107.)

Notwithstanding its arguments that the accused ST products do not practice the means for programming in parallel and means for verifying limitations of claim 27, the staff did not address separately the issue of whether said accused products satisfy the "means for enabling further programming and verifying in parallel to one or more of the addressed cells until all the plurality of addressed cells are verified" limitation of claim 32.

The administrative law judge has found that construction of the phrase in issue matches the constructions of the "means for programming," "means for verifying," and "until all the plurality of addressed cells are verified" limitations of claim 27 construed in each of Sections

VII, E, F, and H, respectively. (See Section VII, K, supra.) Accordingly, for the same reasons that the administrative law judge found that the accused ST products do not satisfy the means for programming, means for verifying, and means for inhibiting limitations of claim 27, the administrative law judge finds that said accused products do not practice the "means for enabling further programming and verifying in parallel to one or more of the addressed cells until all the plurality of addressed cells are verified" of claim 32.

K. Claim phrase "means on chip for individually inhibiting programming of any addressed cell already verified until all addressed cells are verified, while enabling further programming in parallel to all other addressed cells not yet verified"

Complainant argued that the accused ST NAND flash memory chips{

} that once verified, the programming of the memory cell is{ }; and that during a page program operation, the accused chips{

} (CBr at 99.)

Respondents argued that the accused ST products do not perform the function required by this limitation for the same reasons that they do not perform the "programming" and "verifying" functions of claim 27. (RBr at 108.)

Notwithstanding its arguments that the accused ST products do not practice the means for programming in parallel, means for verifying, and means for verifying limitations of claim 27, the staff did not address separately the issue of whether said accused products satisfy the "means on chip for individually inhibiting programming of any addressed cell already verified until all addressed cells are verified, while enabling further programming in parallel to all other addressed

cells not yet verified" limitation of claim 32.

The administrative law judge has found that the construction of the phrase in issue matches the constructions of the "means for inhibiting," "means for programming," "means for verifying," and "until all the plurality of addressed cells are verified" limitations of claim 27 construed in each of Sections VII, G, E, F, and H, respectively. Accordingly, for the same reasons that the administrative law judge found that the accused ST products do not satisfy the means for programming, means for verifying, and means for inhibiting limitations of claim 27, the administrative law judge finds that said accused products do not practice the "means on chip for individually inhibiting programming of any addressed cell already verified until all addressed cells are verified, while enabling further programming in parallel to all other addressed cells not yet verified" of claim 32.

IX. Validity

Respondents have argued that the claims in issue are not valid in view of prior art. It was further argued that the asserted claims are invalid under 35 U.S.C. §112.

A. Prior Art (Anticipation)

A patent issued from the Patent Office bears the presumption of validity. 35 U.S.C. § 282. The party challenging a patent's validity has the burden of overcoming this presumption by clear and convincing evidence. Advanced Display Sys., Inc. v. Kent State Univ., 212 F.3d 1272 (Fed. Cir. 2000). An analysis for anticipation under section 102 is a two-step inquiry. Power Mosfet Technologies, L.L.C. v. Siemens AG, 378 F.3d 1396, 1406 (Fed. Cir. 2004). The first step requires construing the claim, which is a question of law to be decided by the administrative law judge. Oakley, Inc. v. Sunglass Hut Int'l, 316 F.3d 1331, 1339 (Fed. Cir. 2003); Markman v.

Westview Instruments, Inc., 52 F.3d 967, 970-71 (Fed. Cir. 1995). The second step requires a comparison of the properly construed claims to the prior art, which is a question of fact. Power Mosfet, 378 F.3d at 1406; Oakley, 316 F.3d at 1339.

A patent claim is invalid for anticipation if a prior art reference discloses, either expressly or inherently, all of the limitations of a claim. EMI Group N. Am., Inc. v. Cypress Semiconductor Corp., 268 F.3d 1342, 1350 (Fed. Cir. 2001) (citation omitted). As to any inherent disclosure of a prior art reference, the Federal Circuit has stated:

> To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.

Metabolite Laboratories, Inc. v. Laboratory Corp. Of America Holdings, 370 F.3d 1354, 1367 (Fed. Cir. 2004).

Respondents argued that the asserted claims of the '338 patent are invalid as anticipated by either the SGS-Thompson M293 EEprom memory device (the M293 device) or U.S. Patent No. 4,890,259 to Simko (the Simko or '259 patent) (RX-62). (RBr at 113-14.) According to respondents, whether the asserted claims of the '338 patent are anticipated by the M293 device or the Simko patent depends on whether the "means for inhibiting programing of correctly verified cells among the plurality of addressed cells" of the '338 patent is construed as a means for "temporarily inhibiting" programing or a means for "permanently inhibiting" programing. (Id.) Thus, respondents argued that if said means is construed as "temporary inhibit," the M293 device anticipates and if said means is construed as "permanent inhibit," the '259 patent anticipates. The administrative law judge has determined that the "means for inhibiting programing of

correctly verified cells among the plurality of addressed cells" requires the function of terminating or inhibiting any further programming of the verified cells for the remainder of the programming operation, i.e., permanent inhibit. (See Section VII, G, supra.) Hence, based on the administrative law judge's construction of the means for inhibiting limitation and respondents' claim-construction-dependent arguments regarding anticipation, the administrative law judge only has to consider whether Simko, i.e., the '259 patent, anticipates the asserted claims.

With respect to the Simko patent, respondents argued that the preferred embodiment of the Simko invention discloses every element of the asserted claims of the '338 patent either expressly or inherently. (RBr at 116, citing Pashley, Tr. at 2211-12, 2225.) According to respondents, complainant admitted that the Simko patent discloses all of the elements in the Jepson preamble of the asserted claims and the first improvement limitation of claim 27, including a means for "permanently inhibiting" further programming. (Id. at 117, citing Banerjee, Tr. at 2605-06.) Thus, respondents asserted that the anticipation inquiry is reduced to the question of whether the Simko patent discloses the final means limitation of claim 27 – "means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly." (RBr at 117.)

Respondents argued that complainant incorrectly contends that the limitation requires not only that all the addressed cells be correctly verified, but that a signal must be sent to the system indicating that this condition has been met; that although any working embodiment of a digital memory system would inherently have such a feature, it is not a requirement of the claims as written (RBr at 118, citing Banerjee, Tr. at 2660; Pashley, Tr. at 2344-45); and that the Simko

patent indisputably discloses all that the asserted claims require, which is that programming continue until all the addressed cells are verified. (RBr at 118.)

Assuming that the asserted claims require further programming, verifying, and inhibiting of individual cells in a row to occur only until all the cells in the row are verified, i.e., that a signal is sent to the system indicating that all the cells in the row are verified as complainant contends, respondents argued that the Simko patent discloses both that function and the structure for its performance. (Id.) Respondents further argued that the Simko patent's disclosure of "until the columns are charged," appearing within the patent's teaching "[t]he write operation is such that the trial chargings of the column [of memory cells] will occur until the columns are charged to a level which matches the input sample signal," directly corresponds to the function of the means limitation of claim 27 of the '338 patent, i.e., "until all plurality of addressed cells are verified correctly"; that while complainant's expert Banerjee allegedly tried to "obfuscate this issue" by distinguishing the Simko patent based on its teaching of a "time-out feature," (RBr at 119, citing Banerjee, Tr. at 2610), such feature does not make the Simko patent non-anticipatory. (RBr at 118-19.)

In addition to disclosing the function of the means limitation of claim 27 of the '338 patent, respondents argued that the Simko patent inherently discloses structure to detect the logical identity of the charge status of the addressed cells, i.e., an AND gate; that the specification of the Simko patent necessarily discloses structure to indicate that all the addressed cells have been verified, without expressly illustrating such structure; that one of ordinary skill in the art would recognize that the language "until the columns are charged to a level which matches the input sample signal," (RX-62, col. 11, lns. 55-57), describes structure to detect the

logical identity of the charge status among addressed cells; that said structure could be an AND gate, a NAND gate, an OR gate, or a NOR gate; and that these structures are identical or equivalent to the AND gate 733 identified in Figure 16 of the '338 patent for performing the "until" function of the asserted claims. (RBr at 120-22, citing Pashley, Tr. at 2238-39.) Respondents further argued that claim 5 of the Simko patent discloses an AND gate or equivalent structure for stopping programming when all of the programming for a column is complete; and that the Figures 2 and 5 of the Simko patent, along with the accompanying written description, illustrate that the Simko patent must include logic circuitry (an AND gate or its equivalent) to confirm that all of the addressed cells have been correctly verified. (RBr at 122-23, citing Pashley, Tr. at 2227-28, 2239-40.)

Complainant argued that the Simko patent does not anticipate the asserted claims of the '338 patent because the claimed invention of said Simko patent does not perform any recited function of the '338 patent, viz. programming, verifying, or inhibiting, "until all the plurality of addressed cells are verified"; and that the system disclosed in the Simko patent does not require and does not include any structure or equivalent to the structure disclosed in the '338 patent for determining when "all the plurality of addressed cells are verified," i.e., the AND gate 733 of Figure 16. (CBr at 102.)

Complainant further argued that the Simko patent discloses an analog signal recording and playback system that stores analog information on a real time basis; that the entire specification of the Simko patent, except for the discussion of the prior art and the final paragraph of the written description, describes the real-time analog audio recording system; and that it is undisputed that the real-time analog recording system described in the Simko patent

does not require any circuitry that outputs an "all-verified" signal when all the cells in a row are verified." (CBr at 103-04, citing CFF 1127-32, 1135-43, 1154; RX-62, Abstract.)

While respondents relied on an allegedly disclosed "digital implementation" in Simko as the basis of their anticipation claim, complainant asserted that respondents' expert Pashley admitted that the "digital implementation" does not require an "all verified" signal (CBr at 104, citing CFF 1152, 1156-59); and that the portion of the specification that allegedly discloses a "digital implementation" and on which respondents relied for their anticipation claim, (RX-62 at col. 11:55-57, claim 5), does not expressly disclose structure for determining when all the cells being programmed are verified and providing an "all verified" signal (CBr at 104-05, citing CFF 1145-51); that the Simko reference does not inherently disclose such structure (CBr at 105-106); that in the real-time recording system described in the Simko patent, the time available for programming each row is fixed, whether all cells in the row reach their desired state or not (id. at 105, citing CFF 1126, 1144); that the system disclosed in Simko does not have any use for circuitry to determine when all cells in a row are verified and provide an "all verified" signal (id., citing CFF 1130-31); that because the Simko system has no use for such circuitry, such structure could not be inherent; and that the Simko patent merely suggests that a digital implementation is possible, but identifies no structure or provides no actual discussion of a digital implementation of the real-time analog recording system. (CBr at 105-106, citing CFF 1126, 1130-31, 1152-55, 1160-62.)

The staff argued that respondents failed to establish that the Simko patent anticipates the asserted claims of the '338 patent for two reasons. First, the staff argued that the Simko patent does not disclose any structure for determining if all the cells in a row have been verified (SBr. at

74-75); and that the fact that the Simko patent discloses a real-time system where the programming of one row stops and the programming of another row begins in a timed sequence, negates the need for a structure that terminates all programming when all of the addressed cells in a chunk have been programmed and verified. (Id. at 74.) Second, the staff argued that while the device disclosed in the Simko reference is an EEPROM, which must include a structure used for erasing, the Simko reference does not disclose any information regarding the type of terminal used in the erase process and thus cannot anticipate the asserted claims of the '338 patent.[37] (Id. at 75.)

Respondents have argued that the asserted claims of the '338 patent are anticipated by the Simko reference, i.e., the '259 patent. The '259 patent is titled "High Density Integrated Circuit Analog Signal Recording and Playback System" and names Richard Simko as the sole inventor. The '259 patent issued on December 26, 1989 based on an application filed in the United States on July 13, 1988. (RX-62.) The '338 patent issued on December 15, 1992 based on an application filed on April 11, 1990. (CX-1.) Because the '259 patent to Simko was filed in the United States before the '338 patent was filed, the '259 patent will anticipate the '338 patent if it discloses every limitation in the asserted claims of the '338 patent. 35 U.S.C. § 102(e).

Independent claims 27 and 32 of the '338 patent require, inter alia, means for further programming and verifying a plurality of addressed cells and inhibiting programming of verified

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[37] The staff's argument regarding the structure used for erasing is predicated on the administrative law judge construing the claim term "erase electrode" consistent with the staff's proposed construction of said claim term. The administrative law judge, however, rejected the staff's proposed construction and construed the term "erase electrode" as (1) a terminal to which erase voltage conditions are applied to draw electrons off the floating gate, (2) can include the substrate and (3) is not limited to the erase gate structure of the preferred embodiment of the '338 patent.

cells until all the plurality of addressed cells are verified. (CX-1, col. 26, lns. 51-54; col. B1, lns. 46-53.) The administrative law judge has construed said means limitation to require "the programming and verifying of unverified cells and inhibiting the programming of verified cells, to continue until all the addressed cells in a chunk are verified," with the structure corresponding to said means for inhibiting being "the one-way latch 721 in conjunction with the program circuit with inhibit." In addition, the administrative law judge has found that the limitation "until all the addressed cells in a chunk are verified" requires "the AND gate of Figure 16" as corresponding structure.

Respondents argued that the preferred embodiment of the Simko invention discloses every element of the asserted claims of the '338 patent either expressly or inherently; and that the claimed means for inhibiting of the '338 patent is disclosed in the Simko patent at column 11, lines 33-54 and Figure 5. (RBr at 116; RFF 850, 851.) While the Simko patent does contain a disclosure relating to the inhibiting function, stating in part that "this logical high level signal disables further charging of the columns even though high voltage pulses continue to be delivered to the individual column charging circuits," the administrative law judge finds that respondents have failed to show that the Simko patent discloses the requisite structure for performing the inhibiting function, i.e., a one-way latch in conjunction with a program circuit with inhibit. (RX-67, col. 11, lns. 51-53.) Respondents' expert Pashley testified that the structure associated with the inhibit function disclosed in the Simko patent is a positive voltage which appears on the node to which capacitor 147 is connected that turns on transistors 146 and 153, which causes transistor 152 to be turned off and transistor 149 to turn on and lock the column at

five volts.[38] (Pashley, Tr. at 2222-2225.) Significantly, Pashley's testimony does not explain how the structure disclosed in the Simko patent is structurally identical or equivalent to the disclosed one-way latch in conjunction with a program circuit and inhibit required by the '338 patent. Moreover, Pashley's anticipation testimony was based on respondents' proposed construction for the "means for inhibiting" limitation, which the administrative law judge did not adopt in construing said means for inhibiting. (See VII., G, supra; RBr at 58 (construing the means for inhibiting as program circuit with inhibit 210, source multiplexer 107, drain multiplexer 109, local power control 180 and the program algorithm of figure 15).)

The administrative law judge finds that respondents have also failed to establish that the Simko patent discloses the limitation of the '338 patent requiring means for programming, verifying and inhibiting "until all the addressed cells in a chunk are verified." Specifically, the administrative law judge finds that while respondents have shown that the Simko patent discloses the function "until all the addressed cells in a chunk are verified," respondents have failed to show that the Simko patent discloses its corresponding structure, i.e., an AND gate or equivalent. Respondent`s rely on the written description of the Simko patent at column 11, lines 55-57 and the language of claim 5 as evidence that the Simko patent discloses the function "until all the addressed cells in a chunk are verified." (RBr at 117-20.) The written description (CX-1, col. 11, lns. 55-57) states that "[t]he write operation is such that the trial chargings of the column will occur until the columns are charged to a level which matches the input sample signal."

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[38] Respondents, relying on a claim chart, argued that the selector circuit 148 acts as a latch to inhibit a verified cell from further charging. (RFF 920.) The administrative law judge finds that said claim chart amounts to nothing more than attorney argument and is therefore given no weight. Estee Lauder, Inc. v. L 'Oreal, S.A., 129 F.3d 588, 595 (Fed. Cir. 1997) ("Arguments of counsel cannot take the place of evidence lacking in the record.").

Respondents' expert, Pashley, testified that "to any engineer reading this, the right [sic] operation is such that the trial chargings of the column -- now, remember, the column is the memory cell -- will occur until the columns, plural, now, which are being done in parallel, are charged to a level which matches the input sample signal." (See Pashley, Tr. at 2228.) Complainant's expert, Banerjee, contended that this portion of the written description only means that the voltage conditions applied during the write operation should be sufficient for all the cells to attain their target state, (Banerjee, Tr. at 2603; CRFF 854), however a plain reading of this portion of the specification clearly does not support Banerjee's conclusion. The administrative law judge finds Pashley's testimony persuasive and accordingly finds that respondents have shown that the Simko patent discloses the functional requirement of the '338 patent's "until all the addressed cells in a chunk are verified" limitation.

With regard to the structure that corresponds to the function "until all the addressed cells in a chunk are verified," respondents did not argue that the Simko patent expressly discloses structure corresponding to the function "until all the addressed cells in a chunk are verified," i.e., an AND gate or equivalent structure, but rather, argued that an AND gate or its equivalent is inherently disclosed in the Simko patent. (RBr at 120-121.) The Simko patent discusses two general implementations of the disclosed invention, an analog implementation and a digital implementation. Respondents argued that both implementations inherently disclose an AND gate or equivalent structure that corresponds to the function "until all the addressed cells in a chunk are verified." (See RRBr at 91-95.) With regard to the analog implementation, respondents' expert Pashley admitted that the analog embodiment is not anticipatory. Thus, Pashley testified:

Q. Dr. Pashley, I would like a straight answer to my question because I don't want to have to go through the analog embodiment if it is not necessary. Is it your contention the analog embodiment that is described in the '259 patent is an anticipatory reference or, rather, is an anticipatory embodiment?

A. For digital applications? Because it can be used, that embodiment, without changing a thing, can be used for a digital applications. One bit per cell, I can show you how to do it, changing no circuits.

Q. Is it your testimony then the analog embodiment used as is, described as is in the body of the '259 patent is anticipatory?

A. Okay. How it is described for the application is not.

(Pashley, Tr. at 2341.)

With regard to the digital implementation of Simko, respondents argued that the written description of the Simko patent and the language of claim 5 shows that the Simko patent inherently discloses an AND gate or its structural equivalent. (See RBr at 121-23; RRBr at 92-92.) Respondents' expert Pashley further testified that claim 5 of the Simko patent discloses that programming stops "when all the programming is done to the columns." (Pashley, Tr. at 2227.) As each column in the Simko patent comprises at least one memory cell, Pashley testified that claim 5 discloses that programming stops when all the programming to a plurality of cells is completed. (See Pashley, Tr. at 2228 (stating that each column represents one memory cell).) According to Pashley, the language of claim 5 inherently discloses an AND gate or equivalent. (Pashley, Tr. at 2227.)

Claim 5 of the Simko patent states that "said write circuitry includes means for stopping the application of said write pulses to each cell of said plurality of cells when the charge on said cell is representative of said predetermined analog signal . . ." (RX-62, col. 14, lns. 7-11.) The

administrative law judge finds that claim 5 does not support Pashley's conclusion because claim 5 only discloses a means for stopping the programming of each cell when the cell is verified, not a plurality of cells, i.e., "columns," as Pashley argued. (See Banerjee, Tr. at 2600-01.) Assuming arguendo that the language of claim 5 did inherently disclose an AND gate or equivalent structure, the administrative law judge finds that said claim 5 would only disclose a structure for determining that each individual cell is verified and not the structure disclosed in the '338 patent for determining when all the cells in a chunk are verified. Accordingly, the administrative law judge finds that respondents have not established, by clear and convincing evidence, that the Simko patent discloses corresponding structure to the function "until all addressed cells in a chunk are verified" of the '338 patent.

Respondents further argued that the written description of the Simko patent (col. 11, lns. 55-57) inherently disclose structure corresponding to the function "until all addressed cells in a chunk are verified." (RBr at 121-22.) According to respondents, a person of ordinary skill in the art would recognize that the language "until the columns are charged to a level which matches the input sample signal," (RX-62 at 11:55-57), inherently describes an AND gate or its equivalent. (RRBr at 92.) Thus, Pashley testified that:

> To an engineer reading that [(column 11, lines 55-57)], that's an AND gate. In the same way that you understand the Christmas tree string that you have to screw in all the bulbs before the Christmas tree lights go on."

(Pashley, Tr. at 2228.) Pashley, however, did not provide any explanation of why one of ordinary skill in the art would interpret said language of the Simko patent to inherently disclose an AND gate or equivalent structure. Furthermore, assuming one of skill in the art would recognize that the language of column 11, lines 55-57 in the Simko patent inherently discloses an AND gate or

equivalent structure, Pashley admitted that in the digital implementation of the Simko patent, use of the "all verified" signal outputted from the AND gate is not required. (Pashley, Tr. at 2346 (testifying that "I believe to someone skilled in the art they would look at this and it is not required, but someone skilled in the art would say, oh, this is how I use this signal to load the next batch of data and they would know how to use it.") (emphasis added).) Because the "all verified" signal is not necessary, ipso facto, the corresponding structure AND gate is not necessary. Consequently, the administrative law judge finds that the Simko patent does not inherently disclose the AND gate structure. See Continental Can Co. v. Monsanto Co., 948 F.2d 1264, 1269 (Fed. Cir.1991). Accordingly, the administrative law judge finds that respondents have not established that the written description of the Simko patent at column 11, lines 55-57 teaches, expressly or inherently, the structure corresponding to the function "until all addressed cells in a chunk are verified" of the '338 patent.

Respondents argued that the written description of the Simko patent at column 12, lines 3-13 inherently discloses an AND gate or equivalent structure. (RBr at 123.) Specifically, respondents argued that

> [t]he fact that each compare circuit associate with each addressed cell outputs a stable signal on line 141 to indicate that permanent inhibit of the individual memory cell has been applied supports the conclusion that an AND gate is utilized to confirm that all of the individual cells in a row are correctly verified (inhibited).

(Id.) In support, respondents cite to the testimony of Pashley. (See Tr. at 2239-40.) The administrative law judge finds that the testimony cited by respondents does not support respondents' argument. To the contrary those pages appear to describe the prior art reference JP-100, not the Simko patent.

Based on the foregoing, the administrative law judge finds that respondents have failed to prove, by clear and convincing evidence, that the Simko patent anticipates the asserted claims of the '338 patent.

B. Prior Art (Obviousness)

Respondents argued that at the hearing, SanDisk admitted that Japanese Laid-Open Patent Application No. 62-188100 (the JP-100) (RX-232) contains all the "improvement" limitations of the asserted claims -- i.e., the "inhibiting" limitations on which SanDisk rested its patentability arguments during the Samsung investigation and on reexamination; that while SanDisk argued that the JP-100 lacks two limitations from the preamble: (1) the "means for temporarily storing a chunk of data for programming a plurality of addressed cells" limitation, and (2) the limitation requiring that the memory cells be electrically erasable, the JP-100 inherently discloses "means for temporarily storing" and both of those limitations are concededly present in innumerable other pieces of prior art; and that a combination of JP-100 with either the Simko '259 patent or the M293 product renders the asserted claims obvious under 35 U.S.C. § 103. (RBr at 123-24.)

Complainant argued that while respondents have presented several alleged obviousness combinations, those combinations reflect hindsight analysis. Moreover it is argued that "most" of the combinations are missing one or more elements, and all are unmotivated. (CRBr at 93.)

The staff argued that respondents have not "ultimately" made a showing of obviousness by relying on JP 100 in various combinations. (SBr at 82.)

Under 35 U.S.C. § 103, a patent is valid unless "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art

to which said subject matter pertains." The ultimate question of obviousness is a question of law, but "it is well understood that there are factual issues underlying the ultimate obviousness decision." Richardson-Vicks Inc. v. The Upjohn Co., 122 F.3d 1476, 1479 (Fed. Cir. 1997); Lockwood v. American Airlines, Inc., 107 F.3d 1565, 1570 (Fed. Cir. 1997). To establish obviousness, the patent challenger must demonstrate, by clear and convincing evidence, that "there is a reason, suggestion, or motivation in the prior art that would lead one of ordinary skill in the art to combine the references, and that would also suggest a reasonable likelihood of success." Ruiz v. A.B. Chance Co., 234 F.3d 654, 664-65 (Fed. Cir. 2000) (Ruiz). The Federal Circuit has rejected "broad conclusory statements regarding the teaching of multiple references" so as to guard against "the subtle but powerful attraction of a hindsight-based obviousness analysis." In re Dembiczak, 175 F.3d 994, 999 (Fed. Cir. 1999).

After construing the claims, the next "step in an obviousness inquiry is to determine whether the claimed invention would have been obvious as a legal matter, based on underlying factual inquiries including: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the claimed invention and the prior art; and (4) secondary considerations of nonobviousness, also known as 'objective indicia of nonobviousness." Ruiz, 234 F.3d at 660; Graham v. John Deere Co., 383 U.S. 1, 17 (1966). Secondary considerations, also part of the Graham factors, include commercial success, long-felt but unresolved need, failure of others, copying, and unexpected results. Id.

With respect to the scope and content of the prior art, as the Federal Circuit stated in State Contracting & Engineering Corp. v. Condotte America, Inc., 346 F.3d 1057 (Fed. Cir. 2003), citing In re Clay, 966 F.2d 656, 658 (Fed. Cir.1992): "A prerequisite to making a finding on the

scope and content of the prior art is to determine what prior art references are pertinent." References within the statutory terms of 35 U.S.C. § 102 (anticipation) can qualify as prior art for an obviousness determination only when analogous to the claimed invention. In re Clay, 966 F.2d 656, 658 (Fed. Cir. 1992). The Federal Circuit restated the test for determining the scope and content of the prior art to be considered for obviousness purposes in In re Bigio as follows:

> Two separate tests define the scope of analogous prior art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed and, (2) if the reference is not within the field of the inventor's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved. In re Deminski, 796 F.2d 436, 442 (Fed. Cir.1986); see also In re Wood, 599 F.2d 1032, 1036 (CCPA 1979).

In re Bigio, 381 F.3d 1320, 1325 (emphasis added); accord State Contracting, 346 F.3d at 1069. One of ordinary skill in the art would have known of such art because such a person is a hypothetical person who is presumed to be aware of all the pertinent prior art. Custom Accessories, Inc. v. Jeffrey-Allan Industries, Inc., 807 F.2d 955, 962 (Fed. Cir. 1992).

The JP-100, titled "Method of Writing to an Ultraviolet Radiation-Erasable Programmable ROM," was published on August 17, 1987. (RX-232 at ST 19200; Pashley, Tr. at 2183-84.) It is therefore prior art to the '338 patent under 35 U.S.C. § 102(b).

The JP 100 discloses a test circuit for EPROMs. (RX-232.) The English abstract provided with the Japanese application expressly states that the purpose of the invention is "[t]o obtain a writing method fitted for pre-processing of a storage characteristic test. . . ." (CX-82 at SDITC064469.) Various translations of JP 100 refer to the "storage characteristic test" as a "memory retention characteristic" test, and as a "memory maintenance characteristic" test. (CX-82 at SDITC329815; RX-232 at ST019203.) As JP 100 explains, conventional EPROM

writing methods did not provide a uniform threshold voltage – there is "variability in the threshold voltage." (RX-232 at ST019203.) Hence, "the conventional write method has had a problem in that it has not been suitable to writing as a preliminary process in memory maintenance characteristic testing, such as for high temperature maintenance or high temperature operation." (RX-232 at ST019203.) JP 100 does disclose programming in parallel. (RX-232 at ST019201.)

It is undisputed, however, that JP 100 does not disclose EEPROM cells or an erase electrode. Also, the administrative law judge finds that JP 100 fails to disclose "means for temporarily storing" because this element requires a latch or equivalent structure to temporarily store data to be programmed into the memory and such a structure is not expressly or inherently disclosed in JP 100. While experts for both private parties agreed that it is possible to provide the data to the circuit disclosed in JP 100 using a manual switch, it is undisputed that a manual switch is not equivalent to a latch, as the use of manual switching would be approximately 1 million (1,000,000) times slower than using a latch. (Pricer, Tr. at 2696.) Morever, both complainant's expert Banerjee and respondents' expert Pricer testified that a manual switch is not equivalent to a latch. (See CFF 1275-1277 (undisputed).)

Respondents attempt to cure the inadequacy of JP 100 by combining JP 100 with prior art such as the Simko '250 patent or the M293 product. The administrative law judge in Section IX, A, supra, has found that each of the '259 patent and the M293 lacking elements of the asserted claims. The administrative law judge finds nothing in the record to support the conclusion that one of ordinary skill in the art would take certain portions of the '259 patent and/or the M293, even though said prior art teaches away from the asserted claims, and combine said portions with

JP 100. Moreover, assuming complainant has established that its products practice the asserted claims, there is evidence of secondary considerations. For example, revenues from complainant's flash memory products have been in the millions of dollars. (Mehrotra, Tr. at 184-5; CDX-3, CDX-7; CX-243; CX-1970C.)

Based on the foregoing, the administrative law judge finds that respondents have not established, by clear and convincing evidence, that the asserted claims are obvious under 35 U.S.C. § 103.

C. 35 U.S.C. §112

ST argued that asserted claims 27, 28, and 32 are invalid for failure to meet the written description requirement and/or for indefiniteness under 35 U.S.C. § 112, ¶¶ 1 and 2. (RBr at 148.) ST, in support, argued that the algorithm of Figure 15 discloses a temporary inhibit function. (RBr 149-150.) It further argued that latch 721 from Figure 16 is a two-way latch and that if the claims are interpreted to require permanent inhibit, there is no corresponding structure to the claimed function. (RBr at 150-152, 155.)

The staff under the subheading "best mode under section 112, ¶ 1a" argued that while ST contends that the applicants failed to disclose the best mode by allegedly failing to disclose "ramped" programming, whereby each successive programming pulse is larger than the preceding pulse, and ST premises its allegations on the fact that Harari, one of the named inventors of the '338 patent, knew of ramped programming prior to filing the application that eventually issued as the '338 patent, the evidence of record demonstrates that many different methods of applying voltage during programming were known to those of ordinary skill at the time that Harari conceived the invention of the '338 patent; that the specific method chosen was

device-dependent; that therefore the evidence does not show that Harari had a preconceived way to use one method or another; and that therefore, the staff does not believe that ST has demonstrated that the applicants failed to comply with the best mode requirements. (SBr at 87-88.)

The staff also argued that while ST contends that if one accepts SanDisk's construction that the asserted claim require "permanent inhibit," and that such claims are then invalid for failing to satisfy the written description and/or definiteness requirements of §112, ¶ ¶ 1-2, the staff believes that the appropriate construction of the language of asserted claims 27 and 32 encompass "temporary" exhibit. (SBr at 86.) The staff then argued that the specification expressly describes latch 721, upon which SanDisk's argument relating to "permanent inhibit" is based, as a normal data latch that passes any signal received to the cell's compare module's output module; that the literal language of the text of the algorithm illustrated in Figure 15 and the description thereof in the specification of the '338 patent, specifically steps 4-6, demonstrates that latch 721 is a normal data latch, i.e., two-way; that therefore, the specification discloses only devices that will "temporarily" inhibit programming and thus, if the asserted claims are construed to exclude such devices, the asserted claims are invalid for failing to satisfy the requirements of § 112, ¶ 1, written description because the specification of the '338 patent does not describe a device that permanently inhibits programming; and that the asserted claims would not, satisfy the definiteness requirements of a § 112, ¶ 2 by virtue of SanDisk's express disclaimer of temporary inhibit because the disclaimer does not alter the fact that the disclosed structures cannot practice "permanent inhibit." (Id.)

Complainant argued that ST's arguments fall "well short of the clear and convincing

standard." (CBr at 124-126). It further argued that the Patent Office confirmed that the '338 patent claims are valid under section 112 and expressly "rejected Samsung's arguments" (repeated here by ST and the staff) that the '338 patent specification does not disclose permanent inhibit (CRRBr at 107-118, CRSBr at 67-70); that the '338 patent specification fully supports and provides the corresponding structure for the claimed means for inhibiting; and that the staff fails to establish, by clear and convincing evidence, that "the claims and specification do not meet the written description and definiteness requirements." (CRSBr at 70-72.)

Section 112, ¶1 provides that

> [t]he specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The purpose of this "written description requirement" is to "ensure that the scope of the right to exclude, as set forth in the claims, does not overreach the scope of the inventor's contribution to the field of art as described in the patent specification." Reiffin v. Microsoft Corp., 214 F.3d 1342, 1345 (Fed. Cir. 2000). A finding of invalidity for failure to disclose the best mode requires proof, by clear and convincing evidence, that the inventor knew of and concealed a better mode of carrying out the invention than was set forth in the specification. Scripps Clinic & Research Found. v. Genentech, Inc., 927 F.2d 1565, 1578 (Fed. Cir. 1991). The best mode inquiry focuses "on the inventor's state of mind at the time he filed his application." Glaxo Inc. v. Novopharm Ltd., 52 F.3d 1042, 1050 (Fed. Cir. 1995).

Section 112, ¶ 2 provides that "[t]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as

his invention." A patentee's failure to do so renders the patent indefinite and invalid. See Default Proof Credit Card Sys., Inc. v. Home Depot U.S.A., Inc., 412 F.3d 1291, 1298 (Fed. Cir. 2005). A determination of claim indefiniteness is a legal conclusion that is drawn from the court's performance of its duty as the construer of patent claims. Id. citing Atmel Corp. v. Information Storage Devices, 198 F.3d 1374, 1378 (Fed. Cir. 1999). If one employs means-plus-function language in a claim, "one must set forth in the specification an adequate disclosure showing what is meant by that language. If an applicant fails to set forth an adequate disclosure, the applicant has in effect failed to particularly point out and distinctly claim the invention as required." In re Donaldson Co., 116 F.3d 1189, 1195 (Fed. Cir. 1994).

Referring to Section VII, G, supra, the administrative law judge has found support in the specification of the '338 patent for the function and structure corresponding to the "means for inhibiting" limitation in issue. Thus, the administrative law judge rejects ST's argument that the asserted claims are invalid under 35 U.S.C. § 112.

Based on the foregoing, the administrative law judge finds that ST has not established, by clear and convincing evidence, that claims 27, 28, and 32 in issue are invalid under 35 U.S.C. § 112.

X. Enforceability

Respondents argued that the '338 patent is not enforceable on two independent grounds, viz., (A) inequitable conduct and (B) a failure to include an inventor.

A. Inequitable Conduct

ST argued that SanDisk in the reexamination prosecution of the '338 patent argued that "latch 721 in Figure 16 was a one-way latch that would only allow for permanent inhibit." (RBr

at 155); that while SanDisk's argument in the reexamination proceeding is contradicted by the inventors' publication, SanDisk failed to disclose said publication to the Patent Office; and that the inventors of the '338 patent failed to inform the Patent Office that the "specification for the product being designed during the weeks proceeding the reexamination was replete with identically drawn two-way latches." (Id.)

SanDisk argued, in the reexamination proceedings, that the Patent Office was provided with detailed attorney arguments "on both sides of the issue" and that the Patent Office after carefully considering all the evidence, concluded that "latch 721 in figure 16 ... is a one way resettable latch." (CBr at 131.) It is argued that the Patent Office adopted SanDisk's arguments, which were directed to the entire disclosure of the '338 patent and not just latch 721 in isolation, even though they were countered by Samsung's ITC briefing and Samsung's reexamination reply. (CRBr at 118-122.) Complainant further argued that ST failed to point to any information from a 1992 VLSI article that was not disclosed to the Patent Office and that "Mehrotra's uncontroverted testimony" established lack of any intent to deceive the Patent Office. (CRBr at 124-126.)

The staff argued that ST has not established, by clear and convincing evidence, that SanDisk committed inequitable conduct before the Patent Office. (SBr at 90.)

To establish unenforceability, due to inequitable conduct, a respondent must prove, by clear and convincing evidence, that a patentee failed to disclose material information during prosecution of a patent with an intent to mislead the Patent Office. Bristol-Myers Squibb Co. v. Rhone-Poulenc Rorer, Inc., 326 F.3d 1226, 1233 (Fed. Cir. 2003). Affirmative misrepresentation of material fact or submissions of false material information to the Patent Office can also form

the basis of an inequitable conduct defense. Id. Within the context of an inequitable conduct analysis, "[i]nformation is deemed material if there is a substantial likelihood that a reasonable examiner would consider it important in deciding whether to allow the application to issue as a part." Brasseler, U.S.A. I,L.P. v. Stryker Sales Corp., 267 F.3d 1370, 1380 (Fed. Cir. 2001); accord Baxter Int'l Inc. v. McGaw, Inc. 149 F.3d 1321, 1327, (Fed. Cir. 1998). In a case involving an omission of a material reference to the Patent Office, there must be clear and convincing evidence that the applicant made a deliberate decision to withhold a known material reference. Baxter Int'l, Inc., 149 F.3d at 1329, citing Molins PLC v Textron, Inc., 48 F.3d 1172, 1181 (Fed. Cir. 1995).

During the pendency of the Samsung investigation involving the '338 patent, SanDisk and Samsung each requested reexamination of the '338 patent. (CX-1979 at SDITC057969-57972; CX-3 at SDITC058111-58119). The Patent Office granted Samsung's and SanDisk's requests for reexamination. (CX-1979 at SDITC058034; CX-3 at SDITC058184). SanDisk submitted a Patent Owner Statement Including Proposed Amendments in each of reexamination files kept by the Patent Office. (CX-1979 at SDITC058040-58054; CX-3 at SDITC 058209-58224).

Inventors Mehrotra and Harari were authors of "Serial 9Mb Flash EEPROM for Solid State Disk Applications," 1992 Symposium on VLSI Circuits, Digest of Technical Papers at 24-25 (the VLSI article). (RX-29; CX-264; Mehrotra, Tr. at 247.) Mehrotra presented the article at a VLSI symposium. (JX-7C, Mehrotra, Dep. Tr. at 103.)

Latch number 721 has to be a one-way latch for the '338 patent to achieve permanent inhibition. (Mehrotra, Tr. at 284.) The overwhelming majority of switches drawn in the manner

of 721 are two-way latches. (Mehrotra, Tr. at 285; JX-7C, Mehrotra, Dep. at 166.)

The latch shown in Figure 5 of the VLSI article is drawn identically to latch 721 in the '338 patent with the immaterial exception of the orientation of the inverters. (RX-29 at Fig. 5; CX-1, at Fig. 16; Mehrotra, Tr. at 292; JX-7C, Mehrotra, Dep. Tr. at 104-105.) Figure 5 of the article shows a sector erase latch. The sector erase latch, as described in the paper, is a two-way latch. (Mehrotra, Tr. at 247-248; Pricer, Tr. at 2472.)

Mehrotra was the lead circuit designer involving the '338 patent. (Mehrotra, Tr. at 186.) When Mehrotra testified during the Samsung investigation, he had a substantial interest in the case. (Mehrotra, Tr. at 282; JX-7C, Mehrotra, Dep. Tr. at 117.) In 1996, Mehrotra had about 17 years of experience in circuit design for nonvolatile memory. (Mehrotra, Tr. at 197.) He has been employed with SanDisk continuously since the Samsung investigation. Since that time, he has been vice president of engineering, senior vice president of engineering, chief operating officer, and executive vice president. (JX-7C, Mehrotra, Dep. Tr. at 6.) Mehrotra now owns a { } stock options in SanDisk. (JX-7C, Mehrotra, Dep. Tr. at 116.)

In Samsung's Reexamination Reply, it argued to the Patent Office that "the 'one-way latch' interpretation postulated by SanDisk . . . fails to cover the disclosed circuitry, and in fact contradicts the express description," and thus should not be adopted. (CX-3 at SDITC059236.) Samsung also argued that the programming algorithm of Figure 15 of the '338 patent did not support SanDisk's claim construction (CX-3 at SDITC059231-59236); that latch 721 was not a one-way latch (CX-3 at SDITC059236, 59236 n.15); and that

> SanDisk's proposed claim construction and amendments . . . are simply not supported by the specification. Significantly, none of the terms now advanced by SanDisk in support of its interpretation

> – 'program terminate,' 'permanently inhibit,' or 'one-way latch' – appear anywhere in the specification or claims of the '338 patent.

(CX-3 at SDITC059231). Samsung further made the following argument to the Patent Office:

> Based on the steps shown in Figure 15 as well as the descriptive text, it is clear that the program algorithm disclosed requires that during each programming cycle, before a programming pulse is applied to any of the cells, the data in each cell must be read and compared with the corresponding program data ('Verify Read Data = Program Data For ALL Addressed Cells'). Figure 15, Step 5 (emphasis added). Moreover, it is also clear that the disclosed algorithm contemplates that the referenced inhibit circuit will selectively block programming only to those cells which are correctly verified during the immediately preceding verification step. In order for these steps to relate logically, selective blocking of the programming pulse must depend only upon the compare result determined in the immediately preceding verification step – not on the result of a verification 'permanently latched' some iterations ago.

(CX-3 at SDITC059233.) In addition, Samsung argued:

> [SanDisk's] interpretation requires that the first time a cell is verified as having been correctly programmed, the signal representing such verification be 'permanently' latched until the entire chunk of data has been programmed. SanDisk's proposed interpretation, however, fails to cover the embodiment actually disclosed in the specification. Moreover, SanDisk's proposed interpretation is in fact inconsistent with the express language (and figures) disclosed.

(CX-3 at SDITC059235.) Samsung also argued to the Patent Office:

> The interpretation proposed now by SanDisk – that verified cells be 'permanently' latched once verified – is inconsistent with the patentees' express requirement that each bit of every cell be verified as part of each programming cycle. If the patentees had contemplated such a 'permanently' latched condition, neither the reading of all cells (Figure 15, Step 4) nor the verification of all cells (Figure 15, Step 5) would be required. In addition, SanDisk's proposed interpretation is inconsistent with the patentees' usage of the present tense ('are') to describe their selective program inhibit.

Col. 20, lns. 10-13.

(CX-3 at SDITC059235-59236.) Samsung further argued in its Reexamination Reply:

> [T]he disclosed embodiment provides for reading and verifying every bit, 'bit by bit,' during each loop of the programming cycle and then inhibiting programming of any correctly verified cell(s) based only on the immediately [preceding] verification. The correctness of this interpretation is reinforced both by the disclosed programming algorithm and the disclosed circuitry. Accordingly, the 'means for . . . inhibiting . . . until' language in claim 27 should be construed to cover only a 'latched' inhibit which may change during each verify cycle . . . and not the 'permanently' latched inhibit proposed by SanDisk.

(CX-3 at SDITC059237 (emphasis in original).) Samsung in addition argued in its Reexamination Reply to the Patent Office:

> SanDisk can also not properly amend any of the claims of the '338 patent to cover its proposed permanently latched inhibit. In addition to the written description and enablement requirements of § 112, 35 USC § 305 expressly prohibits any claim additions or amendments which enlarge the scope of a patent in reexamination . . . . Because the claims of the '338 patent originally failed to cover a permanently latched inhibit, SanDisk cannot now by amendment secure such coverage.

(CX-3 at SDITC059237-59238.) Moreover, in Samsung's Reexamination Reply, it argued to the Patent Office that the permanent inhibit construction was erroneous; that "the 'one-way latch' interpretation postulated by SanDisk . . . fails to cover the disclosed circuitry, and in fact contradicts the express description," and thus should not be adopted (CX-3 at SDITC059236); that the programming algorithm of Figure 15 of the '338 patent did not support SanDisk's claim construction (CX-3 at SDITC059231-59236); and that latch 721 was not a one-way latch. (CX-3 at SDITC059236, 59236 n.15.)

SanDisk, in the reexamination proceeding, disclosed to the Patent Office that inventor

Mehrotra admitted during the Samsung investigation that a two-way latch is drawn the exact same way as latch 721 in Figure 16. (CX-3 at SDITC058353.) During said proceeding, SanDisk did not disclose the VLSI article. SanDisk, however, provided the Patent Office with Samsung's arguments for why the latch 721 of Figure 16 of the '338 patent was a two-way latch, and that a two-way latch is drawn the exact same way as latch 721 in Figure 16. Samsung's claim construction arguments against finding a "one-way latch" were provided by SanDisk to the Patent Office at the same time SanDisk's briefs were submitted. (CX-3 at SDITC058432-58433 (excerpt from Samsung's post-hearing brief that "The '338 Patent Is Not Limited To a One-Way Latch Or Two-Way Latch"), SDITC058506-58508 (excerpt from Samsung's reply post-hearing brief that "Latch 721 Cannot Be 'One-Way'"), SDITC058470-58472 (excerpt of Samsung's proposed findings of fact under the subheading "Latch 721 In Figure 16 Of The '338 Patent Is A Two-Way Latch.").) In addition, SanDisk disclosed to the Patent Office that Mehrotra admitted during the Samsung investigation that a two-way latch is drawn the exact same way as latch 721 in Figure 16 (CX-3 at SDITC038353.) SanDisk also disclosed to the Patent Office the following proposed finding of fact of Samsung: "RFF334. A two-way latch is the normal latch encountered by those in the art." (CX-3 at SDITC058351, 58470.) Moreover, SanDisk distinguished (1) the Torelli article, which appeared in a magazine called Alta Frequenza; (2) product brochures and technical notes for the SGS M206, M293 and M490/491 integrated circuits; and (3) the M293 integrated circuit device, as detailed in two test reports (a TAEUS report and a CHIPWORKS report). (CX-3 at SDITC058209-58212, 58216-58223.)

Mehrotra kept an inventor's notebook. (CX-248C; Mehrotra, Tr. at 289; JX-7C, Mehrotra Dep. Tr. at 31.) He testified that his notebook does not describe many things, and that although

the words "permanently inhibit" or "one-way latch" do not appear in his notebook prior to filing of the '338 patent, those ideas were very much a part of the concept of his invention. (JX-7C, Mehrotra Dep. at 378-38.) Moreover, Mehrotra's notebook had{

}" (JX-7C, Mehrotra Dep. at 34-35.)

On April 25, 1997, the Patent Office issued a notice of intent to issue a reexamination certificate. (CX-3 at SDITC059247-59255.) In the Reexamination Reason For Patentability/Confirmation, the Examiner concluded: "the inhibiting feature recited in claims of '388 [sic, '388] patent is enabled by latch 721 in figure 16 which is a one way resettable latch." (CX-3 at SDITC059250.) The Examiner considered and deemed the reexamined claims of the '338 patent to be patentable over each of the '344 patent (U.S. Patent No. 5,095,344) and JP 158 (Japanese Pat. Publica, 5931158). (CX-3 at SDITC059247, 59254, 59248-59250.) A conclusion the Examiner made was that the product brochures and technical notes (including M293) "fail to anticipate or render obvious the claims of present invention alone or in combination with Torelli reference and lack any structure for permanently inhibiting correctly verified cells for further programming." (CX-3 at SDITC059249.) In addition, the Examiner concluded, despite Samsung's arguments to the contrary, that the inhibiting feature of the claims of the '338 patent was fully supported by the specification, and that, specifically, latch 721 was a one-way latch. (CX-3 at SDITC059250.[39])

[39] SanDisk had distinguished between temporary and permanent inhibit in asserting that the '338 patent was patentable over the prior art. (Pricer, Tr. at 2426.)

Based on the foregoing, the administrative law judge finds that the Examiner had before him in the reexamination proceeding detailed arguments advocating for and against the "one-way latch" claim construction. The administrative law judge finds no material facts that SanDisk presented to the Patent Office that were false nor does he find that SanDisk withheld material information. Significantly, the record is devoid of any evidence that anyone involved in the reexamination proceeding of the '338 patent had any intent to deceive the Patent Office. Hence, the administrative law judge finds that respondents have not sustained their burden, by clear and convincing evidence, in establishing that the '338 patent is unenforceable due to inequitable conduct.

B. Inventorship

ST argued that Winston Lee worked with inventors Harari and Mehrotra at SanDisk at the time of the invention and designed a novel circuit for simultaneously comparing the current of a memory cell with the currents of multiple reference cells (RBr at 168); that Lee's invention is disclosed in the '338 patent application as an alternate embodiment of the "means for verifying" limitation of the asserted claims (RBr at 169); that the inventor of any disclosed means for a means-plus-function limitation is a joint inventor (RBr at 170); and that Ethicon, Inc. v. U.S., Surgical Corp., 135 F.3d 1456 (Fed. Cir. 1998) (Ethicon) is "legally indistinguishable" from the facts surrounding Lee's contribution to the '338 patent. Hence, ST argued that the '338 patent is unenforceable until the inventorship is corrected by re-adding Lee as an inventor. (RBr at 174.)

SanDisk argued that ST cannot prove, by clear and convincing evidence, that Lee conceived any part of the invention claimed in the '338 patent. (SBr at 127.)

The staff argued that "[o]n balance" ST has not established, by clear and convincing

evidence, that the asserted claims are invalid for failing to name Lee as a coinventor. (SBr at 78.)

An issued patent enjoys a presumption that the named inventors are the true inventors. Hess v. Advanced Cardiovascular Systems Inc., 106 F.3d 976, 980 (Fed. Cir. 1997), quoting Amax Fly Ash Corp. v. United States, 514 F.2d 1041, 1047 (Ct. Cl. 1975). Any challenge to inventorship, including non-joinder of a co-inventor, must be proven by clear and convincing evidence. Hess, 106 F.3d at 980.

Lee was listed as an inventor on the application for the '338 patent prior to a restriction requirement from the Patent Office. (JX-6C, Lee, Dep. at Tr. 8-9.) RX-22 is a petition under 37 C.F.R. 1.48(b) dated January 22, 1991 removing Lee as an inventor on the application that became the '338 patent. (RX-22; JX-6C, Lee, Dep. Tr. at 145-146.) Lee worked at SanDisk for about two years, beginning on or about February 1989. (JX-6C, Lee, Dep. Tr. at 22, 23.)

Prior to working at SanDisk, Lee worked on memory devices including SRAMs, EEProms, and flash memory. Thus Lee started working at Intel in 1982, as an engineer doing mostly NOR flash EEprom circuit design. He worked at Intel until about 1987, at which time he went to work at Integrated Device Technologies (IDT) with the title design engineer or senior design engineer. He worked at IDT for about a year and a half or two years, mostly on SRAM and some EEprom. (JX-6C, Lee, Dep. Tr. at 18-21, 41, 43.)

Inventor Sanjay Mehrotra hired Lee to work at SanDisk. (JX-6C, Lee, Dep. Tr. at 23.) At the time Lee worked at SanDisk, Mehrotra and inventor Harari also worked at SanDisk. (JX-6C, Lee, Dep. Tr. at 25.)

Harari was responsible for device physics during the first years of business at SanDisk. (Harari, Tr. at 58.) Lee worked at SanDisk exclusively on a circuit design of NOR flash

memories. (JX-6C, Lee, Dep. Tr. at 46.) Lee spent a substantial amount of his time at SanDisk working on a novel sensing circuit. (JX-6C, Lee, Dep. Tr. at 57.) Most likely Lee designed the circuit shown at RX-19C, SDITC 76975. (JX-6C, Lee, Dep. Tr. at 64; RX-019C at SDITC 76975.)

The application that issued as the '338 patent, viz., Serial No. 508,273 (the '273 application), is a continuation-in-part of abandoned U.S. Patent Application Serial No. 337,579 (the '579 application). (CX-4.) The '579 application was filed on April 13, 1989 with 58 claims, naming only Eli Harari and Sanjay Mehrotra as the inventors. (CX-4 at SDITC7923.) Inventor Mehrotra testified that Lee did not have any involvement nor make any contribution in the filing of the '579 application and that Mehrotra designed the circuits shown in Figure 9A and 9B of the '579 application (Tr. at 187-188.)[40] ST has argued that said testimony is irrelevant because the only relevant issue, under Ethicon, is whether Lee invented "any disclosed means" of a means-plus-function claim element; that whether Lee had involvement in other aspects of the patent application process has no bearing on that issue; that Lee must be named a joint-inventor because he contributed Figures 9D-9I of the '338 patent and the accompanying text; and that who invented other structures disclosed in the '338 patent has no bearing on the legal issue. (ROCFF1551, 1553, 1555 [41] (emphasis in original).)

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[40] It is undisputed that Figure 9A and 9B of the '579 application became Figure 9A and 9B of the '338 patent (CFF 1554 (undisputed), CFF 1556 (undisputed)).

[41] The courtesy copies of respondents' rebuttal to complainant's proposed findings as well as the filed docket copy did not have respondents' rebuttal to CFF 1550 to CFF 1586. Moreover those copies at page 576 ended with ST's rebuttal to CFF 1549 and at page 577 started with the heading "VI. The Reexamination Of The '338 Patent Issued Only After The Examiner Fully Considered Samsung's Arguments That Figure 16 Does Not Illustrate A One-Way Latch." The administrative law judge does not understand why ST's rebuttal to CFF1550 to CFF1586 is

Examination of the file wrappers relating to the '338 patent shows that the applicants eventually abandoned the '579 application and filed a continuation-in-part application which included Lee as an inventor (the '273 application). (CX-4 ('579 application) at SDITC008016 (letter requesting abandonment of '579 application), CX-4 at SDITC008017 (notice of abandonment of '579 application), CX-2 at SDITC057669 (stating that the '273 application is "a continuation-in-part of application Serial No. 337,579 filed April 13, 1989")); that the '273 application was filed on April 11, 1990 with the 58 claims from the parent '579 application and an additional 29 claims (CX-2 at SDITC057668, 57711-57733); that the specification of the '273 application included new matter, specifically Figures 9D - 9I and a corresponding description in the specification (appearing at col. 12, ln. 54, col. 15, ln. 53 in the issued '338 patent); that the Patent Office considered all of the originally-filed claims to be part of one invention, and all of the newly added claims (except application claim 64, which depended from original claim 5) to be a separate invention (See CX-2 at SDITC057728, SDITC057787-57793 and SDITC057791 ('338 patent file history); that the applicants therefore requested the Patent Office to "cancel non-elected claims 59-63 and 65-87a" (CX-2 at SDITC057800); that along with the amendment, the applicants filed a petition to change inventorship, deleting Lee as an inventor from the '273 application (CX-2 at SDITC0578033-034); and that SanDisk then filed a divisional application that contained the claims directed to Lee's contribution which application later issued as U.S. Patent No. 5,163,021 (the '021 patent). (See RX-536.)

It is unrefuted that Lee is named as an inventor on the '021 patent (JX-6C, Lee, Dep. Tr.

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missing from the filed docket and courtesy copies of ST's rebuttal findings. The administrative law judge was able to determine ST's position on CFF 1550 to CFF 1586 only from the word perfect version which has a different pagination from the filed docket and courtesy copies.

at 107; RX-536), and that Figures 9D-9I of the '021 patent (RX-536) and accompanying text found at col. 12, ln. 54 through col. 15, ln. 53 are the same figures and text that appear in the '338 patent. (RX-536; CX-1; Pricer, Tr. at 2476; JX-6C, Lee Dep. Tr. at 116-117, 118.) Moreover, there is unrefuted testimony by Lee that he contributed to the invention set forth in claim 30 of the '021 patent which claim is directed to a reading system, and is described in figures 9D through 9I of the '021 patent and the accompanying text of the patent, col. 12, ln. 54 through col. 14, ln. 53. (JX-6C, Lee Dep. Tr. at 114-117, 119.)

Figure 9A of the '338 patent shows a read circuit that compares the sense current from the memory cell which enters at node 415, and a reference current which enters at node 403. Depending on which is larger, the result is latched by the clock signal into a sampling transistor 423 and then into latch 425. (CX-1 at Fig. 9A; Pricer, Tr. at 2475.) The circuit shown in Figure 9A of the '338 patent measures the current from the memory cell relative to the current of a single reference cell. (Banerjee, Tr. at 2669.)

The circuit shown in Figure 9B of the '338 patent measures the current from the memory cell relative to the current of multiple reference cells at different instances of time. (Banerjee, Tr. at 2669-2670.) In Figure 9B, a number of comparisons are made sequentially, each time comparing the sense current against various references and the results are latched in the latches, in the upper right. (Pricer, Tr. at 2475-2476.) The circuits shown in Figures 9A and 9B of the '338 patent use a one-to-one current mirror. (Banerjee, Tr. at 2672.)

Figures 9A and 9B of the '579 application disclose the structure corresponding to the "means for verifying." Thus, a sense amplifier used for reading is part of the disclosed structure for the "means for verifying," since the '579 application discloses this sense amplifier structure

used to perform the "means for verifying claim" claim element in claims 27 and 32. (Banerjee, Tr. at 2619-2620.) ST's expert Pricer agreed that the sense amplifier shown in Figure 9B performs the "means for verifying" function, in conjunction with the structures shown in Figure 16. (Tr. at 2525.) The administrative law judge further finds that Figures 9A and 9B of the '579 application disclose the structures corresponding to the "means for comparing," the "reading means for comparing" and the "means for reading" in the unasserted claims.

The Figure 9D read circuit structure of the '338 patent relates to a current mirror that makes use of currents specifically flowing through the memory cell on the leg 920, and makes use of a current flowing through a reference, which may be 941, 942 through 945. (CX-1 at Fig. 9D; Subramanian, Tr. at 1646.) The output of the differential test in the Figure 9D read circuit structure is available on the reference leg. (CX-1 at Fig. 9D; Subramanian, Tr. at 1646.) Figures 9D-9I are all substantially the same with respect to their use of current mirror structure, their use of reference circuits, their compactness, their ability to dispense with the need to use latches, and their ability to output directly into the bit decoder 230 without latches. (CX-1 at Figs. 9D-9I; Subramanian, Tr. at 1655-1656.)

ST contends that Figures 9D-9I disclose structures corresponding to the "means for comparing," the "reading means for comparing" and the "means for reading" from claims 1, 7, 8, 13, 20, 29, 30, 35 and 38. (See RBr at 169.) However, the original '579 application, in particular Figures 9A and 9B, disclosed the corresponding structures for those means-plus-function claim elements. Moreover, ST's expert Pricer admitted that Figure 9B discloses a sense amplifier that can perform the "means for comparing" element of unasserted claims 1, 8, 13 and 35, the "reading means for comparing" element of unasserted claims 7, 20, 29 and 30, and the "means

for reading" element of unasserted claim 38. (Tr. at 2522-23, 2525-26.)

The administrative law judge also finds that Figures 9D-9I only add different inputs to the previously disclosed structures corresponding to the "means for verifying," "means for comparing," "reading means for comparing," and "means for reading." Thus, he finds that said Figures 9D-9I do not disclose any new structures corresponding to the "means for verifying," "means for comparing," "reading means for comparing," or "means for reading"; and do not broaden the scope of any claims of the '338 patent. As the Federal Circuit has stated, "[o]ne who reduces to practice the original inventor's broader concept is not an inventor." Ethicon, 135 F.3d at 1463-1464 (Fed. Cir. 1998). The administrative law judge finds that Lee's contributions are nothing more than a reduction to practice of inventors' Harari and Mehrotra's broader concept of using sense amplifiers and current mirrors to read the state of a memory cell, as originally disclosed in the '579 application.

In addition, the corresponding structure to a function set forth in a means-plus-function limitation "must actually perform the recited function . . . ." Asyst Technologies, Inc. v. Empak, Inc., 268 F.3d 1364, 1371 (Fed. Cir. 2001). The necessary structure that actually performs the recited function in each of the means-plus-function elements is identical to that disclosed in the original '579 application. (Banerjee, Tr. at 2615-19; CX-4 at SDITC 7994; CDX 618-21.) This identical structure, simply the current mirror that compares two inputs, is disclosed in Figures 9A and 9B and merely replicated in Figures 9D through I, with a variation discussed in the original '579 application.[42] Lee's contributions to Figures 9D-9I were the inputs that mirror reference

[42] The use of reference cells in parallel with multiple sense amplifiers was disclosed in the '579 application. (Mehrotra, Tr. at 320.)

current to the multiple sense amplifiers. (Mehrotra, Tr. at 294-95.) As a result, Figures 9D-9I do not add new structures that implement the "means for verifying," "means for comparing," "reading means for comparing" or "means for reading."

SanDisk has not disputed that Figures 9D-9I include novel circuits that can be used to mirror reference cell currents into multiple sense amplifiers. (See CRRFF1204A.) However, the administrative law judge finds that this mirroring of reference current into multiple sense amplifiers is not part of any claims of the '338 patent. Rather, such mirroring is relevant to the claims of the divisional patent. (RX-4 at ST 14311-17, 14360.)

Based on the foregoing. the administrative law judge finds that Lee's contributions to Figures 9D-9I do not include any new corresponding structure for the "means for verifying," "means for comparing," "reading means for comparing," and "means for reading." Thus, he finds that any distinctions between Figures 9A-9B and 9D-9I are irrelevant for the purposes of determining inventorship. He further finds, in view of the testimony of Lee and the named inventors on the '338 patent as well as the Patent Office restriction requirement and the '021 patent, that ST has not met its burden in establishing, by clear and convincing evidence, that Lee should be an inventor of the '338 patent.

Referring to Ethicon, relied on by ST, unlike inventor Choi in Ethicon, the administrative law judge finds that Lee did not invent the corresponding structure to any means-plus-function claim elements in the '338 patent. Moreover the corresponding structures for the "means for verifying," "means for comparing," "reading means for comparing" and "means for reading" were previously disclosed in the '579 application, which Lee did not contribute to.

ST has also relied on the Commission Opinion in Investigation No. 337-TA-395, where a

patent was held to be unenforceable for "failure to name the inventor of structure for performing the function of several claim elements written in means-plus-function format." (RBr at 167.) In that investigation, however, the sole named inventor on the patent application, viz., Jordan, admitted that he did not conceive any of the circuitry by which the elements of the patent claims at issue were realized. See In the Matter of Certain EPROM, EEPROM, Flash Memory, and Flash Microcontroller Semiconductor Devices, and Products Containing Same, ITC Inv. No. 337-TA-395, USITC Pub. No. 3136 (Oct. 1998).

XI. Domestic Industry

SanDisk argued that it practices claims 27, 28, and 32 of the '338 patent and thus satisfies the technical prong of the domestic industry requirement. (CBr at 137-154.) It further argued that it has made a substantial investment in the exploitation of the '338 patent through domestic engineering, research, development and licensing which are more than sufficient to satisfy the economic prong of the domestic industry requirement pursuant to section 337(a)(3)(C). (CBr at 154-62.)

ST argued that SanDisk does not satisfy the technical prong of the domestic industry requirement. It also argued that SanDisk does not satisfy the economic prong of the domestic injury requirement. (RBr at 175-188.)

The staff argued that SanDisk has not established that any of its NAND flash memory chips satisfy six elements of the asserted claims, viz., erase electrode, means for temporary storing a chunk of data, means for programming in parallel, means for verifying, means for inhibiting and means for further programming, verifying and inhibiting. (SBr at 65, 66.) With respect to the economic prong of the domestic industry requirement, the staff represented that the

parties have stipulated that SanDisk will rely "only" upon the third criterion set forth in sub-section 337(a)(3), viz., "(C) substantial investment in its exploitation, including engineering, research and development, or licensing." It then argued that SanDisk has established that it has made significant investments in research and development relating to products allegedly covered by the '338 patent and that SanDisk has also invested in licensing efforts relating to the '338 patent. (SBr at 67-69.)

There can be a violation of section 337 "only if an industry in the United States, relating to articles protected by the patent ... exists or is in the process of being established." 19 U.S.C. § 1337(a)(2) (emphasis added); see also Certain Methods of Making Carbonated Candy Products, Inv. No. 337-TA-292, USITC Pub. 2390, (Mar. 1990). The existence of a domestic industry is measured at the time the complaint is filed. See Bally/Midway Mfg. Co. v. U.S. Int'l Trade Comm'n, 714 F.2d 1117, 1121-22 (Fed. Cir. 1983).

The Commission has established a two-prong test for determining whether a complainant has satisfied the domestic industry requirement. The technical prong considers "whether the complainant is exploiting or practicing the patent in controversy," while the economic prong addresses "whether there is significant or substantial commercial exploitation." Certain Microsphere Adhesives, Process for Making Same, and Products Containing Same, Including Self-Stick Repositionable Notes, Inv. No. 337-TA-366, USITC Pub. 2949 (Jan. 1995). As the complainant, SanDisk bears the burden of proving that it has satisfied both the technical prong and the economic prong.

A. SanDisk Chips

The private parties are in dispute as to what are the SanDisk NAND chips which are

alleged to practice the asserted claims of the '338. For example, referring to certain proposed findings of ST and complainant's response, there is disclosed:

> RFF1269. In its Prehearing Statement, SanDisk identified seven NAND flash memory chip designs that it contends practice the asserted claims of the '338 patent and may be included in various SanDisk flash products. (SanDisk PHS at 172.) The seven chip designs are{
>
> } (SanDisk PHS at 172.)
>
> CORFF1269. SanDisk objects on grounds that SanDisk's Pre-hearing Statement is not evidence. The evidence presented at the hearing shows that the '338 patent is practiced by each of the chip designs listed on CDX-34C. CFF651: Over the last two years, SanDisk's CompactFlash Cards also include the following SanDisk NAND chips: {
>
> }
> (Conley, Tr. 464:6-25). SanDisk's PC Cards also include the following SanDisk NAND chips: {
>
> }
> (Conley, Tr. 464:6-465:4); SanDisk's USB Flash drives have the{
> } The USB Flash drives also include the following SanDisk NAND chips: {
> } (Conley, Tr. 465:5-14).
>
> RFF1270. SanDisk had no involvement in the development of{
> } designs identified by SanDisk as practicing the asserted claims of the '338 patent. The{ } designs with which SanDisk had no involvement in the development are the{ } (Quader, Tr. 350:12-21; CDX-34.)
>
> CORFF1270. SanDisk objects on grounds that the proposed finding of fact mischaracterizes the record. Dr. Quader testified that:{
>
> }; these were all designed in Sunnyvale [...] All the other products except the{
> }, SanDisk designers were actively involved in the design of these products. Some engineers from Sunnyvale and then our Japan designers in Japan participated in those designs." (Quader, Tr. 350:12-21; CDX-34.)

CRRFF1270A. SanDisk designers were actively involved in the design of all the products listed on CDX-34C except for the{ } SanDisk designers from both Sunnyvale (USA) and Japan participated in the design of the products listed on CDX-34C. (Quader, Tr. 350:12-21; CDX-34.)

CRRFF1270B. CDX-034C lists the following chip designs: {

}

However, the private parties and the staff did not differentiate, as to function and structure, with respect to a specific SanDisk product alleged to practice the asserted claims of the '338 patent. Hence the administrative law judge is not making any differentiation as to a specific SanDisk product when analyzing function and structure relating to the SanDisk products in issue.

B. Technical Prong

Complainant, in support of its argument, that it meets the technical prong argued that the evidence submitted at the hearing conclusively demonstrates that the memory cells of the SanDisk NAND chips include an erase electrode, i.e. a terminal to which erase voltage conditions are applied to draw electrons off the floating gate. (CBr at 140-141.) SanDisk further argued that its NAND chips, as for "means for temporarily storing a chunk of data for programming a plurality of addressed cells "element of claim 27 of the '338 patent, perform the claimed temporarily storing function and include a structure equivalent to the corresponding structure to the means for temporarily storing. (CBr at 141-143.) It is also argued that SanDisk NAND chips regarding the "means for programming is parallel the stored chunk of data into the plurality of addressed cells" element of claim 27 of the '338 patent perform the claimed programming in parallel function and include a structure for programming in parallel that is

equivalent to the corresponding structure disclosed in the '338 patent. (CBr at 143-145.)

SanDisk further argued, in support of its argument regarding the technical prong, that SanDisk NAND chips, as for the "means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data" element of claim 27 of the '338 patent, perform the claimed verifying function and include structure equivalent to the corresponding structure disclosed in the '338 patent for the claimed verifying means. (CBr at 146-148.) It also argued that SanDisk NAND chips as for the "means for inhibiting further programming of correctly verified cells among the plurality of addressed cells" element of claim 27 of the '338 patent perform the claimed inhibiting function and include structure equivalent to the corresponding structure disclosed in the '338 patent for the claimed inhibiting means. (CBr at 148-149.) In addition SanDisk argued that its SanDisk NAND chips regarding the "means and for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly" element of claim 27 of the '338 patent perform the claimed programming, verifying and inhibiting function and include structural equivalents to the corresponding structure disclosed in the '338 patent for the claimed programming, verifying, and inhibiting means. (CBr 149-151.)

SanDisk also argued that the technical prong is met by SanDisk NAND chips practicing claim 28 of the '338 patent for the reasons it stated with respect to claim 27. (CBr at 151.) SanDisk additionally argued that its NAND chips as for the "means for enabling further programming and verifying in parallel to one or more of the addressed cells until all the plurality of cells are verified" element of claim 32 of the '338 patent, perform the claimed enabling further

programming and verifying function and include structure identical or equivalent to the corresponding structure disclosed in the '338 patent. (CBr 152-153.) SanDisk further argued that its NAND chips regarding the "means on chip for individually inhibiting programming of any addressed cell already verified until all the addressed cells are verified, while enabling further programming in parallel to all other addressed cells not yet verified" element of claim 32 of the '338 patent perform the claimed individual inhibit while enabling further programming function and include structure equivalent to the corresponding structure disclosed in the '338 patent for the function of individual inhibiting while enabling further programming. (CBr at 153-154.)

1. Claim phrase "erase electrode"

Complainant argued that the{ } of the their product's memory cell is a terminal to which erase voltage conditions are applied to draw electrons off the floating gate, and is therefore an erase electrode. (CBr at 140.) Complainant further argued that even under respondents' construction, complainant's products have an erase electrode under the doctrine of equivalents, as the{ } performs substantially he same function, substantially the same way, with substantially the same result as an erase electrode. (CBr at 140.)

Respondents argued that since the{ } is a{ } it cannot be a terminal to a memory cell, and therefore cannot be an erase electrode. (RBr at 175.) Respondents further argued that, under their construction, complainant's products do not meet the limitation of an erase electrode under the doctrine of equivalents, since{

} (RRBr at 126.)

The staff argued that complainant's using{

} (SBr at 65.)

The claim phrase "erase electrode" has been construed to be a terminal to which erase voltage conditions are applied to draw electrons off the floating gate, is not limited to the erase gate structure of the preferred embodiment, and can include the substrate. (See Section VII, A, supra. In complainant's products it is undisputed that during an erase operation of the EEprom erase voltage conditions cause electrons{ }(CFF 1708 (undisputed).) The{ } (RRFF 1309 (undisputed); CX-396C.) Since the "erase electrode" is not limited to a separate structure, and{ } used by complainant's products satisfies the "erase electrode" limitation.

Accordingly, the administrative law judge finds that complainant's products do include an "erase electrode" as required by claims 27 and 32 of the '338 patent in issue. As the administrative law judge has found an erase electrode in the complainant's products, doctrine of equivalents is not reached.

2. Claim phrase "means for temporarily storing a chunk of data for programming a plurality of addressed cells"

a. Function

Complainant argued that the SanDisk NAND chips satisfy the means for temporarily storing function. (CBr at 141-43.)

Respondents argued that complainant's products do not perform the function of the "means for temporarily storing" as complainant{ } (RRBr at 127-28.)

The staff argued that complainant does not perform the function of the "means for temporarily storing" because complainant's products do not store a "chunk of data" long enough.

(SBr at 65-66.)

The administrative law judge has construed the function of the claim phrase "means for temporarily storing a chunk of data for programming a plurality of addressed cells" to be data for each of the addressed cells in the chunk to be programmed is temporarily stored for a limited period of time but at least long enough to complete the programming of that cell. (See Section VII, D, 1 supra). CX-396C is a training manual for new engineers that describes complainant's flash memory design. (CFF 1673 (undisputed).) The flow charts in CX-396C show that data is being loaded into the{ } (CX-396C, SDITC325006 - SDIC325007.) The claim phrase "chunk of data" has been interpreted by the administrative law judge to be at least several bytes of data, supra. Testimony by respondents' expert Subramanian indicates that{ } (CFF 1758, CFF 159, CFF 1760 (undisputed).) Two further flow charts in CX-396C show that the{ } is used through the programming cycle. (CX-396C, SDITC325008-SDITC325009.) Based on the foregoing, the administrative law judge finds that the complainant's products in issue, in distinct contrast as to what the administrative law judge found with respect to the accused products, perform this function, as they store at least several bytes of data temporarily, but at least long enough to complete programming of individual cells.

b. Structure

Complainant argued that its products have a corresponding structure for the "means for temporarily storing" element, as the{ } corresponds to the latches of block 190 in Fig. 5. (CBr at 143.)

Respondents argued that complainant's products have no structure corresponding to the "means for temporarily storing" element as neither a "shift register" nor its structural equivalent is present in the SanDisk NAND chips. (RRBr at 128.)

The staff presented no argument regarding structure for this element in SBr or SRBr.

The administrative law judge has construed the structure corresponding to the "means for temporarily storing" as the read/program latches and shift registers 190 shown in Fig. 5. (See Section VII, D, 2, supra). The flow charts in CX-396C show that{ } (CX-396C, SDITC325006 - SDIC325007.) Two further flow charts in CX-396C show that the{ } (CX-396C, SDITC325008-SDITC325009.) Since the{ } performs the function of a latch in the box 190 in Fig. 5 of the '338 patent, the administrative law judge finds that the{ } is an equivalent structure to the latches in the box labeled 190 in Fig. 5 of the '338 patent. (CFF 1762 (undisputed in relevant part).) The administrative law judge has, however, found that "shift registers" are also required for any corresponding structure for the "means for temporarily storing" limitation. Complainant makes no argument in CBr or CRRBr regarding what structure is equivalent to a "shift register" in complainant's products. Accordingly, the administrative law judge finds that complainant has failed to prove that its products in issue have an equivalent structure to perform the function of "means for temporarily storing."

3. Claim phrase "means for programming in parallel the stored chunk of data into the plurality of addressed cells"

a. Function

Complainant argued that during a programming operation in its products data is that is

stored in the{ } of the NAND chips are programmed in parallel into the addressed page of the NAND memory. (CBr at 143-44.)

Respondents argued that complainant's products cannot perform the function of "means for programming in parallel "because complainant's products{

} (RRBr at 128-29.)

The staff argued that complainant's parts do not satisfy the function of the element in issue, as it is "predicated upon satisfaction of the 'means for storing' element, which the accused chips fail to satisfy." (SBr at 66.)

The administrative law judge has construed the function of the "means for programming in parallel" claim phrase to be programming data into more than one of the addressed cells at the same time during the same programming cycle. (See Section VII, E, 1, supra). The administrative law judge has also found that complainant's products do perform the function of the "means for temporarily storing," meaning that actual data is stored, and that the data is not limited to N*L bits. During a programming operation, complainant's products program stored data into an addressed page of memory cells, and each page consists of{ } memory cells. (CFF 1777; CFF 1778 (undisputed in relevant part).) Moreover, respondents do not dispute that complainant's products perform programming in parallel. (CFF 1781, CFF 1784 (undisputed); CDX-271C.) Based on the foregoing, the administrative law judge finds that complaint's products do practice the function of the "means for programming in parallel" claim phrase.

b. Structure

Complainant argued that each of complainant's NAND chips include a program circuit with inhibit using a latch to permit or inhibit programming of the memory cell, and uses muxes

to select cell columns for programming, and is therefore structurally equivalent to the structures disclosed in the '338 patent. (CBr at 144-45.)

Respondents argued that the '338 patent only discloses structures capable of using Hot Electron Injection programming, while complainant's products{ } and therefore the structures cannot be equivalent. Respondents argued that "means for programming in parallel" depends on the "means for temporarily storing" phrase claim, and that complainant, in failing to prove that its products perform the "means for temporarily storing", have therefore failed to perform any "means for programming in parallel." Respondents further argued that complainant's products do not have a source and drain mux, as required by the claims. (RRBr at 128-29.)

The staff argued that complainant's products do not satisfy the "means for temporarily storing" claim phrase, and therefore cannot satisfy the requirement for a "means for programming in parallel." The staff also argued that complainant's products cannot have a source and drain mux, as no NAND product allows access to individual source and drain muxes for individual transistors, making their use as disclosed in the '338 patent impossible. (SBr at 66.)

The administrative law judge has found that the required structure of the claim term "means for programming in parallel" is source mux 107, drain mux 109, and program circuit with inhibit 210 as structure for this claim term. (See Section VII, E, 2, supra). A mux, or multiplexer, is a one of many selector, and is a distinct structure. (Subramanian, Tr. 1589; CX-1, Fig. 4.) The '338 patent discloses structures used for programming by Hot Electron Injection, while the complainant's products{ } for programming. (RFF 1355

(undisputed).) While the administrative law judge has found that the '338 patent does not limit the means for programming to just Hot Electron Injection, the administrative law judge has found that the structures required for the two methods of programming at issue are not interchangeable. In particular, the administrative law judge has found that the structure required by Hot Electron Injection does not perform programming in substantially the same way as the structure required { } Moreover, the administrative law judge has also found that complainant's products do not have the structure required by the "means for temporarily storing" claim phrase that is required by the claim phrase "means for programming in parallel." Based on the foregoing, the administrative law judge finds that the complainant's products do not have the structure required to perform the claim phrase "means for programming in parallel."

4. Claim phrase "means for verifying the programmed data in each of the plurality of addressed cells with the chunk of stored data"

a. Function

Complainant argued that its products contain a{

} (CBr at 146.) Respondents argued that complainant's parts do not store a chunk of data and do not use the value of the memory cell and the data in temporary storage. (RRBr at 130.) The staff argued that complainant's have no "means for programming in parallel" and no "means for temporarily storing," and thus cannot satisfy the "means for verifying" claim phrase. (SBr at 62.)

The administrative law judge has construed the function of the "means for verifying" to require determining on a cell-by-cell basis for each of the addressed cells in the chunk whether

the data in an individual addressed cell matches the data that is targeted to be written into the cell, i.e., the chunk of stored data. (See Section VII, F, 1, supra). Complainant's products do verify data, as described in CX-396C. (CFF 1811, CFF 1815 (undisputed).) The verify performed by complainant's products senses the condition of the memory cell. (CFF 1818 (undisputed).) The flow charts in CX-396C show that the verification process continues until all cells are verified. (CX-396C.) Based on the foregoing, the administrative law judge finds that the complainant's products do perform the function of "means for verifying."

b. Structure

Complainant argued that its products contain{ } which are equivalent structure to the current sensing sense amplifiers disclosed in the '338 patent for the structure of the "means for verifying". (CBr at 146-47.) Respondents argued that{ } are substantially different than current sensing sense amplifiers. (RRBr at 130-31.) The staff argued that the sense amplifiers disclosed in the '338 patent use a current mirror, while the transistors that complainant claims as equivalent structure{ } and work in a substantially different way. (SBr at 62-63.)

The administrative law judge has construed the structure of the "means for verifying" to be a current sensing sense amplifier and{ } (See Section VII, F, 2, supra.) The administrative law judge has also found that current sensing and{ } (See Section VIII, E, supra, which found { } not structurally equivalent to current sensing sense amplifiers disclosed in the specification of the '338 patent). Complainant admits that the sense amplifiers in its products use{ } as opposed to the current sensing disclosed in the

'338 specification. (CFF 1812.) Moreover, the administrative law judge has found that complainant's products do not have equivalent structure for either "means for temporarily storing" or "means for programming in parallel," both of which are also required for the claim phrase "means for verifying." Based on the foregoing, the administrative law judge finds that complainant's products do not contain an equivalent structure for the claim phrase "means for verifying."

5. Claim phrase "means for inhibiting further programming of correctly verified cells among the plurality of addressed cells."

a. Function

Complainant argued that its products perform the function of "means for inhibiting," as its products prevent further programing of any verified cells. (CBr at 148.) Respondents argued that complainant's products cannot perform the function of "means for inhibiting" because complainant's products do not perform the functions of "means for programming" or "means for verifying." (RRBr at 131.) The staff likewise argued that complainant's products cannot perform the function of "means for inhibiting" because complainant's products do not perform all the functions in the preamble. (SBr at 65, 66.)

The administrative law judge has found that the function of the "means for inhibiting" is terminating or inhibiting any further programming of the verified cells for the remainder of the programming operation. (See Section VII, G, 1, supra). The administrative law judge finds, based on undisputed evidence in the record, that complainant's products do perform the function of "means for inhibiting." (CFF 1850, CFF 1851, CFF 1852 (undisputed).)

b. Structure

Complainant argued that its products have a one-way latch in the sense amp/data cache for each memory cell being programmed that permanently inhibits a cell from being programmed. (CBr at 148-49.) Respondents argued that complainant's products cannot have an equivalent structure for the "means for inhibiting" because complainant's products do not have the structures for the "means for programming" or "means for verifying." (RRBr at 131.) The staff likewise argued that complainant's products cannot have a structure for "means for inhibiting" because complainant's products do not have equivalent structures for all the claim phrases in the preamble. (SBr at 65, 66.)

The administrative law judge has found that the structure associated with the claim element "means for inhibiting" is the one-way latch 721 in conjunction with the program circuit with inhibit. (See Section VII, G, 2, supra). Complainant's products include an inhibit latch that inhibits a memory cell from receiving further programing conditions. (CFF 1853 (undisputed).) Said inhibit latch consists of both the{ } (CFF 1859 (undisputed).) The inhibit latch inhibits programming of the memory cell by preventing it from receiving further programming pulses, after that cell had been verified. (CFF 1860, CFF 1863 (undisputed).) Thus, the administrative law judge finds that complainant's products have a structure that performs the "means for inhibiting" function. The complainant's products, however, do not contain equivalent structures for "means for temporarily storing," "means for programming in parallel," or "means for verifying," all of which are required for the "means for inhibiting." Therefore, the administrative law judge holds that the complainant's products do not have a structure that is equivalent to the structure required by the claim phrase "means for inhibiting."

6. Claim phrase "means for further programming and verifying in parallel the plurality of addressed cells and inhibiting programming of correctly verified cells until all the plurality of addressed cells are verified correctly"

a. Function

Complainant argued that its products include a "means for programming in parallel," "means for verifying," and "means for inhibiting," and continue the operation until the page program operation is complete. (CBr at 149-50.) Respondents argued that complainant's products do not include any of the above "means for" claim phrases, and so do not have a "means for further programming," (RRBr at 131.) The staff likewise argued that complainant's products do not contain any of said "means for" claim phrases, and therefore also fails to contain a "means for further programming." (SBr at 65, 66.)

The administrative law judge has found that the function of "means for further programming" requires the programming and verifying of unverified cells, and inhibiting the programming of verified cells, to continue until all the addressed cells in the chunk are verified. (See Section VII, H, 1, supra). The administrative law judge has found that complainant's products perform the function of "means for programming," "means for verifying," and "means for inhibiting." Complainant's products also perform an{

} (CFF 1878-79

(undisputed).) Based on the foregoing, the administrative law judge finds that the complainant's products do perform the function of "means for further programming."

b. Structure

Complainant argued that its products include the structures associated with the "means for programing," "means for verifying," and "means for inhibiting," and also that the{

} to create an equivalent structure to an AND gate. (CBr at 150-51.) Respondents argued that complainant's products do not have any of the structures associated with the "means for programming," "means for verifying," and "means for inhibiting" claim phrases, and therefore cannot have an equivalent structure for the "means for further programing." (RRBr at 131.) The staff likewise argued that complainant's products lack equivalent structure for the "means for further programming" as the equivalent structures for the "means for programming," "means for verifying," and "means for inhibiting" claim phrases are missing from SanDisk's products alleged to satisfy the domestic industry requirement. (SB at 65, 66.)

The administrative law judge has found that the structure of the "means for further programming" includes the structures for "means for programming," "means for verifying," and "means for inhibiting," and that the AND gate of Figure 16 of the '338 patent. (See Section VII, H, 2, supra). The administrative law judge finds that the{ } in the complainant's products, are equivalent to the required AND gate. (CFF 1878, 1879 (undisputed).) The administrative law judge has previously found, however, that the required structures for the "means for programming," "means for verifying," and "means for inhibiting" claim phrases or their equivalents are not present in the complainant's products. Therefore, the administrative law judge finds that complainant's products do not contain a structure equivalent to the structure required for the "means for further programming" claim phrase.

7. Claim 28

Complainant argued that its products practice claim 28 of the '338 patent because the system of claim 27 is on an integrated chip in said products. (CBr at 151.) Respondents argued

that complainant's products do not practice any part of claim 27, but that what systems do exist, exist on a single integrated chip. (RRCFF 1981, RRCFF 1891A.)

Claim 28 depends from claim 27, and the administrative law judge has found that the correct interpretation of claim 28 is that the system of claim 27 must reside on the same integrated circuit chip as the EEprom. (See Section VII, I, supra). The complainant's products include an integrated chip with the system on it. (CFF 1891, RRCFF 1891A (undisputed in relevant part).) The administrative law judge has found that complainant's products do not have many of the equivalent structures required to practice claim 27 of the '338 patent. Therefore, the administrative law judge finds that the complainant's products do not practice claim 28 of the '338 patent.

8. Claim 32 - preamble

The administrative law judge has found that the preamble of claim 32 contains only insignificant differences from the preamble of claim 27. (See Section VII, J, supra). The administrative law judge thus finds that the analysis of each claim phrase in the preamble of claim 32 is identical to the analysis of the claim phrases in the preamble of claim 27, supra.

9. Claim phrase "means for enabling further programming and verifying in parallel to one or more of the addressed cells until all the plurality of addressed cells are verified . . . "

Complainant, respondents, and staff agreed, and the administrative law judge so found, that the construction of the claim phrase in issue recited in claim 32 matches the previous constructions of the "means for programming," "means for verifying," and "until all the plurality of addressed cells are verified" claim phrases. (See Section VII, K, supra). Therefore, the administrative law judge finds that the analysis for the technical prong of domestic industry for

this claim phrase is identical to the analysis of said claim phrases in claim 27, supra.

10. Claim phrase "means on chip for individually inhibiting programming of any addressed cell already verified until all the addressed cells are verified, while enabling further programming in parallel to all other addressed cells not yet verified"

Complainant, respondents, and staff agreed, and the administrative law judge so found, that the construction of the claim phrase recited in claim 32 matches the previous constructions of the "means for inhibiting," "means for programming," "means for verifying," and "until all the plurality of addressed cells are verified" claim phrases. (See Section VII, L, supra). Therefore, the analysis of the technical prong of domestic industry for this claim phrase is identical to the analysis of those claim phrases discussed for claim 27.

11. Conclusion

Based on the foregoing, the administrative law judge finds that the complainant's products do not practice the asserted claims of the '338 patent, and thus that complainant has failed to satisfy the technical prong of domestic industry.

B. Economic Prong

SanDisk's research and development activities in the United States are conducted at its Sunnyvale, California facilities. (Mehrotra, Tr. at 147.) These activities include flash memory design, flash memory device engineering, flash memory process technology development and engineering, qualification of the flash memory products, characterization of the chips, as well as development of controllers that work in the flash memory chips in its flash card products. (Mehrotra, Tr. at 152.) SanDisk spent approximately $80 million in 2003, $120 million in 2004 and expects to spend approximately $170 million in 2005 on research and development, most of

which relates to NAND flash memories. (Mehrotra, Tr. at 157; CDX-4.) SanDisk's flash memory chip which is{ } was designed in Sunnyvale, California. (Mehrotra, Tr. at 164; CDX-6.) The vast majority of SanDisk's research and development budget is directed towards products containing NAND flash memory. (Mehrotra, Tr. at 157.)

SanDisk has approximately 700 employees currently working in the United States. (Mehrotra, Tr. at 147.) As of January 2005, SanDisk has about{ } employees working in research and development and engineering in the United States. (Mehrotra, Tr. at 150; CX-227.) SanDisk currently employs{ } designers;{ } of which are located at its Sunnyvale, California facility;{ } of which are located at its{ } and{ } of which are located at its facility in India. (Quader, Tr. at 340-41; CDX 32.) Approximately{ } of those individuals work on NAND flash design, and approximately{ } of their time is spent on the design of NAND flash memory circuits. (Quader, Tr. at 341.) SanDisk's budget for this group totaled approximately{ } from 2001 through the date of the hearing; and the 2005 budget is expected to be approximately{ } all of which relates to NAND flash design. (Quader, Tr. at 343.) Approximately{ } of that will be spent at SanDisk's Sunnyvale California facility. (Quader, Tr. at 344.)

More than 95 percent of SanDisk's products use flash memory circuits. (Mehrotra, Tr. at 153.) Most of the flash memory circuits in SanDisk's products are made by Flash Vision, SanDisk's joint-venture with Toshiba. (Mehrotra, Tr. at 153.) The joint-venture manufactures flash memory circuits, which are jointly designed and developed by SanDisk and Toshiba. Id.. The design effort is generally divided 50:50, with SanDisk designing half and Toshiba the other half of the flash memory circuits produced by Flash Vision. (Mehrotra, Tr. at 154.)

Flash Vision produces approximately 65 percent of the NAND flash circuits used by SanDisk, Samsung approximately 25-30 percent and Renesas approximately 5 percent. (Mehrotra Tr. 155-56; CX 243 at 21.) In 2004, approximately 65 percent of the NAND flash memory chips in SanDisk's products were produced by Flash Vision; and SanDisk estimates that between{ } percent of the memory chips used in 2005 will be produced by Flash Vision. (Mehrotra, Tr. at 156.)

It is a fact that SanDisk has three principal U.S. facilities, in adjacent buildings at 111 Java, 169 Java, and 140 Caspian in Sunnyvale, California. (CX-243, SanDisk Form 10-K Report, at 12; JX-31C, Wilson, Dep. Tr. at 94-95, 101, 104-105, 105.) ST argued that SanDisk does not conduct any research and development activities at its 111 Java facility. However, there is evidence that as of January 30, 2005,{ } SanDisk employees were working on engineering, research and development,{ } of whom (or approximately{ } percent) worked in the United States. (CX-227C at SDITC162365, SDITC162367-382; Mehrotra, Tr. at 150). Also, while ST argued that SanDisk cannot identify the portion of space in its 111 Java facility occupied by employees performing work relating to the SanDisk products identified in response to ST Interrogatory No. 1, SanDisk has{

} (Quader, Tr. at 341; Conley, Tr. at 457-458, 457, 460; CDX-32; CX-210C at SDITC073807, SDITC073811, SDITC073814; CX-227C at SDITC162373-SDITC162374.)

Moreover, all of the following design activities took place at SanDisk facilities located in the United States:{

} (designated{ } in the{ } version) design;{ } chip design;{ } chip design;{ } chip designs;{ } design, which is used to load data for programming, to program, to verify and to read; design manuals for the{ } the schematic for the{ } chip, which has a density of{ } in a{ } mode or a density of{ } in{ } mode; and the NAND Flash memory design training manual, which describes the structure and operation of the { } NAND. (Mehrotra, Tr. at 164; Quader, Tr. at 346; JX-3C, Flahaux Dep. at 111-112; CDX-6; CDX-34; CDX-35; CX-396; CX-1346; and RX-048C.)

ST argued that SanDisk has never entered into a license where the only patent licensed was the '338 patent. The administrative law judge finds that SanDisk has invested in licensing efforts involving the '338 patent. Thus, the record indicates that SanDisk has at least{ } different licenses. (Harari, Tr. at 94.) During his meeting with{ } inventor Harari also discussed the '338 patent. (Harari, Tr. at 102.) In the patent cross-license,{ } acknowledged the value and validity of the '338 patent. (Harari, Tr. at 105; CX-242C at SDITC143635 [¶5.1]) During license negotiations with{ }, the '338 patent was discussed. (Harari, Tr. at 106-107; CX-1456C.) During the negotiations with{ } the '338 was discussed particularly because it is pivotal to{ } implementations. (Harari, Tr. at 107-108; CX-1457C.) SanDisk executed a cross-license agreement with Hitachi in 1997. (CX-72C at SDITC162543.) At the time of the negotiations for the cross-license with Hitachi, Hitachi was a major supplier of non-volatile memory semiconductors. Hitachi was also a very large company with tens of

thousands of patents. Through the cross-license,{

}

(Harari, Tr. at 108.) The '338 patent arose during SanDisk's discussions with{ } (Harari, Tr. at 108.) The '338 patent played an important role in the negotiations between{ } and SanDisk. (Mehrotra, Tr. at 169-170.) During the negotiation with{ }, SanDisk informed { } that it believed "the{ } and flash memory" was covered by the '338 patent. (Mehrotra, Tr. at 170, 172.) Subsequently, during the negotiations for the second cross-license between{ } and SanDisk, the '338 patent was discussed because{ } wanted to use it for { } products (Harari, Tr. at 108-109), and the '338 patent played a central role in the negotiations between{ } and SanDisk for the "second license agreement." (Mehrotra, Tr. at 172-173.)

In addition, during the license negotiations with{ } which began in{ } the '338 patent played a very important role in the negotiations with{ } (Harari, Tr. at 109-110; Mehrotra, Tr. at 174; CX-1462C.) During the negotiations for the second settlement and cross-license between{ } and SanDisk, the '338 patent was discussed in connection with { } request for an{ } (Harari, Tr. at 111.) In his capacity as lead negotiator for SanDisk for the settlement and patent cross-license agreement with{ } inventor Mehrotra was never informed by{ } that they had designed out the '338 patent. (Mehrotra, Tr. at 179.) The second settlement and patent cross-license agreement between{ }and SanDisk licensed{ } to use the '338 patent for their MLC products – for NAND and NOR products. (Mehrotra, Tr. at 180.) The '338 patent played a very important role in the negotiations between{ }and SanDisk for the second

settlement and patent cross-license agreement because '338 patent has claims for both the binary and MLC NAND. (Mehrotra, Tr. at 181-182.)

Based on the foregoing, the administrative law judge finds that complainant has established that it satisfies the economic prong of the domestic industry requirement.

XII. Remedy

In the event the Commission finds respondents in violation of section 337, complainant argued that a permanent limited exclusion order and a cease and desist order are the proper remedies. It argued that ST's infringing NAND flash memory chips are imported into the United States and should be excluded and that the EPROMs factors demonstrate that the Commission should also exclude downstream products that contain ST's infringing NAND flash memory chips. (CBr at 163-176.) Complainant further argued that the Commission should issue a cease and desist order because ST maintains a commercially significant domestic inventory of infringing NAND memory chips. (CBr at 176-177.)

ST argued that, if it is determined that a violation of section 337 has occurred, only a limited exclusion order, not extending to downstream products, would be appropriate. (RBr at 189.) It further argued that no cease and desist order is warranted because ST has a very small share of the NAND flash market and its U.S. inventory is small. (RBr at 198.)

The staff argued that if a violation is found, a limited exclusion order should issue extending to certain lower priced third-party downstream products such as memory devices (CF, SD, Memory Sticks, USB flash drives, a/k/a "Jump drives," and like products), and MP3 players with internal non-volatile. To ease the enforcement burden on Customs, the staff argued that a certification provision may be appropriate. The staff further agreed with SanDisk that a cease

and desist order directed against the domestic ST entities may be appropriate, since it appears that there is inventory in the United States that could be sold. (SBr at 94, 95.)

Under Commission rules 210.36(a) and 210.42(a)(1)(ii), the administrative law judge is to consider evidence and argument on the issues of remedy and issue a recommended determination thereon. Under Section 337(d), 19 U.S.C. § 1337(d), the Commission may issue a limited exclusion order against respondents that have been determined to be in violation of section 337. Such an order directs the U.S. Customs Service to exclude from entry into the United States articles that are covered by, and thus infringe, the intellectual property rights at issue. Certain Flash Memory Circuits and Products Containing Same, Inv. No. 337-TA-382, USITC Pub. No. 3046, Comm'n Op. at 26 (June 1997).

The Commission may issue an exclusion order that covers not only articles specifically found to infringe, but also so-called "downstream products," i.e., those products that incorporate the infringing articles as components, if the Commission decides that exclusion of downstream products is necessary to give a complainant complete and effective relief. On the other hand, excluding downstream products has the potential to greatly expand the coverage of the exclusion order, thus increasing the risk of interfering with legitimate commerce. Hence, a balancing of factors may be appropriate.

To assist in any balancing, the Commission, in Certain Erasable Programmable Read-Only Memories, Components Thereof, Products Containing Such Memories, and Processes for Making Such Memories, Inv. No. 337-TA-276, USITC Pub. 2196, Comm'n Op. at 124-26, 136 (May 1989) (EPROMs), identified the following relevant factors to be considered:

(1) the value of the infringing articles compared to the value of the downstream products

in which they are incorporated;

(2) the identity of the manufacturer of the downstream products, i.e., whether it can be determined that the downstream products are manufactured by a respondent or by a third party;

(3) the incremental value to a complainant of the exclusion of downstream products;

(4) the incremental detriment to respondents from exclusion of such products;

(5) the burdens imposed on third parties resulting from exclusion of downstream products;

(6) the availability of alternative downstream products that do not contain the infringing articles;

(7) the likelihood that the downstream products actually contain the infringing articles and are thereby subject to exclusion;

(8) the opportunity for evasion of an exclusion order that does not include downstream products; and

(9) the enforceability of an order by Customs.[43]

The so-called "EPROMs factors" are not meant to be exclusive of other considerations, as "the Commission may identify and take into account any other factors which it believes bear on the question of whether to extend remedial exclusion to downstream products, and if so to what specific products." EPROMs at 125-26. Thus the Commission may exclude downstream

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[43] Id. aff'd sub nom. Hyundai v. Int'l Trade Comm'n, 899 F.2d 1204 (Fed. Cir. 1990). The Federal Circuit in Hyundai described the EPROMs factors to be "a careful and common-sense balancing of the parties' conflicting interests as well as other relevant factors." Hyundai, 899 F.2d at 1209.

products even though not all of the factors weigh in favor of doing so. See EPROMs at 127 (excluding certain downstream products even though the value of the EPROMs relative to the downstream products was small).

The Commission also has the authority to issue cease and desist orders where a respondent has a sufficient inventory of infringing goods in the United States. See Certain Plastic Encapsulated Integrated Circuits, Inv. No. 337-TA-315, Comm'n Op. at 37 (November 1992) (U.S.I.T.C. Pub. No. 2574). A "sufficient inventory" may consist of one infringing product. See, e.g., In the Matter of Certain Hardware Logic Emulation Systems & Components Thereof, Inv. No. 337-TA-383, USITC Pub. 2089, Comm'n Op. at 26 (Mar. 1998) (Hardware Logic). A cease and desist order can issue in lieu of or in addition to an exclusion order to prevent the sale, distribution or other use of infringing imported products in the United States. The scope of section 337 is broad enough to prevent every type and form of unfair practice. Hardware Logic, Comm'n Op. at 25-29; Certain Digital Satellite Systems Receivers, Inv. No. 337-TA-392, ID at 239-44 (Oct. 1997) (U.S.I.T.C. Pub. No. 3418); Certain Digital Satellite Systems Receivers, Order No. 53 at 7-11 (June 9, 1997).

ST is a worldwide company that designs, develops and produces semiconductor products for system companies. (Casagrande, Tr. at 1171-1172; RX-742, STMicroelectronics N.V. Form 20-F 2004 at ST 48241, 48253-254.) ST has incorporated ST NAND Flash memory into at least the following downstream products:{

} (CX-151C; JX-21C, Roveda Dep. at 57, 65-66, 152-54; CX-206 at SDITC326658; CX-1977C at ARR000126-87;

CX-2011C at AVT000001.)[44] {

}

(CX-91C at 3-4; RX-742 at ST 48258-48259.)

ST has acknowledged that its{

} (RPHS at 114.) Between April 2004 and May 2005, ST sold within the United States{ } units of imported NAND flash memory chips, with a value of{ } million. (SX-3C.)

ST NAND flash memory chips are{

} (CX-91C at 3-4.)[45] ST began offering for sale NAND flash memory products manufactured{ } (RX-742 at ST0000048251.) Pursuant to the{

} (CX-126C at ST0000001666-1668; JX-21C, Roveda Dep. at 117,

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[44] SanDisk does not sell NAND flash memory chips. SanDisk sells Downstream Products that contain NAND flash memory chips such as: CompactFlash, Memory Stick, Secure Digital (SD), MiniSD, MultiMedia, SmartMedia, xD-Picture Card, USB flash drive, Reduced-Size MultiMedia, TransFlash memory module, Wi-Fi CompactFlash, Wi-Fi SD, Flash Drive, P-Tag, TriFlash, TransFlash and MP3 players. (CX-1852C at 5; CX-46C; RX-630 at ST0000045453.) The majority of SanDisk's revenue is derived from the sale of NAND flash memory cards, and an additional 14 percent of SanDisk's revenue is attributable to USB flash drives. (RX-212 at ST0000020329.30.)

[45] On{

} (RX-742 at 0000048252 53; JX-25C, Golla Dep. at 198-199.)

169; CX-161C at ST-E000008046.) In their{

} (CX-126C at

ST0000001670-1671.)

An{

} (CX-1451C at SDITC083392.) Under the{

}

(CX-126C at ST 1688-1689.) {

} (SX-3C.) However,{

} (CX-1451C at SDITC083391-83394.) The

{

} (CX-1451C at SDITC083392.) The{

} (CX-1451C at SDITC083371.) {

} (CX-1451C at SDITC083371.) A{ }

share goes into USB Flash drives. (CX-1451C at SDITC083372.) { } percent of

NAND Flash bits are incorporated into NAND Flash memory cards, USB Flash drives and game

cards. (CX-1451C at SDITC083370-83372.) The{ } of NAND Flash bits are "on-board" (embedded) inside MP3 players, digital still cameras, mobile phones and other devices. (CX-1451C at SDITC083370-83373.)

ST began selling MultiMedia cards{ } and these cards are available for importation into the United States. (JX-21C, Roveda Dep. at 62.) ST distributor { } promotes ST MultiMedia cards on its Internet web site.{ } An{ } purchase summary and accompanying July 28, 2005 affidavit marked as Exhibit { } show that{ } made{ }United States purchases of ST CompactFlash cards on April 5, 2005.{ } STMicro has also offered for sale its CompactFlash cards to Cisco and its reduced-size MultiMedia cards to{ } in the United States, among others. { }

Each NAND Flash memory manufacturer identifies its parts in a unique manner which allows one to identify the manufacturer of the product.{ } at 103.) ST NAND Flash memory chips are marked with ST's logo, along with ST's part number. (CDX-6; CX-26C at SDITC056849; CFF2024.) ST labels ST Downstream Products that contain infringing chips with the ST name. (CX-1972C at ARR000027; CX-153C at ST-E 7708.) Downstream Product manufacturers can record whether a Downstream Product contains a NAND Flash memory chip from ST or from another supplier during assembly, and may share this fact with purchasers. { } testified that an email he received from{ } Inc.'s Taiwan Branch informed him that the{ } "has STMicro Flash in it." { } { } designs, manufactures, and sells products containing NAND flash memory chips.{ } Downstream Products

with clear plastic casings such as USB Flash drives may allow the NAND Flash memory chip manufacturer to be identified.{ } at 61-62; see also CRRFF 1510.)

{ } manufactures and sells products containing NAND flash memory chips.{ } at 14.) { } is Senior Director of Operations, Manufacturing for{ } Inc.{ } Tr. at 12-13.) { } was designated to testify on behalf of{ } { } Tr. at 13.) Each of{ } products contains a NAND flash memory chip.{ } Tr. at 40; CX-1922C.){ }corresponds to{ } model numbers{ } { } During the three months from February through April 2005, at least{ } containing ST NAND Flash memory chips were imported into the United States.{ } is an extract from{ } showing two approved suppliers for{ } Tr. at 48;{ } ST's{ } flash memory chip and Samsung's { }NAND flash memory chip are both{ } and approved for{ } Tr. at 48-49;{ }

During the period from April 4, 2004 to May 9, 2005,{ } ordered at least { } chips from ST.{ } These chips are purchased to manufacture{ } product line. { } at 117-118.) { } is one of ST's distributors.{ } Tr. at 22.) { } is the Technology Business Manager for Non-Volatile Memory at{ } { } Tr. at 11-12.) { } was designated by{ } to testify on its behalf.

Downstream Products with NAND Flash memory chips, such as Flash memory cards, are frequently bundled with other products and shipped into the United States. For example, a 2002 {

} (CX-1548C at SDITC175018.) According to one designer, manufacturer and seller of Downstream Products,{ } NAND Flash memory chips represent approximately{ } of the value of its MP3 players,{ } percent of the value of its USB Flash drives, and{ } percent of the value of its CompactFlash cards.{ } at 33, 144-162.) A designer, manufacturer and seller of Downstream Products, SimpleTech Inc., has represented to the United States Securities and Exchange Commission that integrated circuits such as NAND Flash memory chips "represent more than 90% of the component costs of our manufactured Flash cards and DRAM modules." (CX-1953 at SDITC331701.) Lexar Media, Inc. (Lexar), a designer, developer, manufacturer and marketer of Downstream Products, has represented to the United States Securities and Exchange Commission that NAND Flash memory chips are "the primary cost" of its NAND Flash memory cards, USB Flash drives and MP3 players. (CX-1951 at SDITC331649.)

{ } a manufacturer of networking equipment, incorporates STMicro NAND Flash memory chips into its{ } and imports these { } into the United States.{ } at 41, 42, 44.)

{ } a designer, manufacturer and seller of Downstream Products, is importing into the United States its{ } USB Flash drives containing STMicro NAND Flash memory chips. (CX-1953 at SDITC331694;{ } Dep. at 1175-118, 119-119.) { } a seller of Downstream Products, has imported into the United States Secure Digital Flash memory cards containing ST's NAND Flash memory chips.{ } Dep. at 105, 108-109, 114; CFF2034.) { } Dep. at 53.) { } promotes ST Downstream Products, including ST CompactFlash, Secure Digital, MultiMedia, miniSecureDigital and Reduced-Size MultiMedia cards, on its Internet web site.{ }

Based on the foregoing, if a violation is found by the Commission, the administrative law judge recommends that a limited exclusion order issue directed to ST. Moreover, he recommends that said order apply not only to ST but also to any of ST's affiliated companies, parents, subsidiaries, licensees, contractors, or other related business entities, or their successors or assigns, of ST. See Limited Exclusion Order which issued on February 16, 2005, in Certain Audio Digital-To-Analog Converters And Products Containing Same Inv. No. 337-TA-499 ("limited exclusion order applies to any of the affiliated companies, parents, subsidiaries, licensees, contractors, or other related business entities, or their successors or assigns, of ...[respondent]").

The administrative law judge further recommends that any limited exclusion order cover ST NAND Flash memory chips and at least the following Downstream Products: CompactFlash cards, Secure Digital cards, mini.Digital Secure Cards, MultiMedia cards and Reduced-Size

MultiMedia cards in view of the widespread use and importance of the chips in said Downstream Products. Moreover, the record indicates that there are ways in which to detect the presence of ST chips in downstream products. However, the administrative law judge also recommends the following certification provision when Customs cannot determine whether the Downstream Products fall within the limited exclusion order:

> When the U.S. Bureau of Customs and Border Protection (Customs) is unable to determine by inspection whether chips, including chips incorporated into CompactFlash cards, Secure Digital cards, mini.Digital Secure Cards, MultiMedia cards and Reduced-Size MultiMedia cards, fall within the scope of this Order, it may, in its discretion, accept a certification, pursuant to procedures specified and deemed necessary by Customs, from persons seeking to import said chips or said Downstream Products that they are familiar with the terms of this Order, that they have made appropriate inquiry, and thereupon state that, to the best of their knowledge and belief, the products being imported are not excluded from entry under paragraph 1 of this Order. At its discretion, Customs may require persons who have provided the certification described in this paragraph to furnish such records or analyses as are necessary to substantiate the certification.

The substance of the above certification provision is taken from a certification provision in the limited exclusion order the Commission issued on September 28, 2005 in Certain Optical Disk Controllers Chips And Chipsets And Products Containing Same, Including DVD Players And PC Optical Storage Devices, Inv. No. 337-TA-506. The Commission concluded in its opinion of September 28 that the certification therein gave Customs more discretion in determining whether it will allow importation based on certification from importers.

With respect to any cease and desist order,{

} This inventory included{ } in May 2004,{ } NAND Flash memory chips in November 2004 and{ } NAND Flash memory

chips in May 2005. (CX-481C at 3.) ST also uses the services of{ } New York to maintain a inventory of samples of ST products. (JX-8C, Pecoraro Dep. Tr. at 92.) As of July 5, 2005, there was a total of{ } ST NAND Flash memory chips in the{ } (CX-1949C.) Hence, the administrative law judge recommends the issuance of a cease and desist order against ST.

XIII. Bond

Section 337(j) (3) provides for the entry of infringing articles upon the payment of a bond during the 60-day Presidential review period. 19 U.S.C. § 1337(j) (3). The bond is to be set at a level sufficient to "offset any competitive advantage resulting from the unfair method of competition or unfair act enjoyed by persons benefiting from the importation." In re Certain Dynamic Random Access Memories, Components Thereof and Products Containing Same, Inv. No. 337-TA-242, Commission Opinion on Violation, Remedy, Bonding and the Public Interest, USITC Pub. No. 2034, (Sept. 21, 1987). When reliable price information is available, the Commission has set the bond by eliminating the price differential between the domestic and the imported infringing product. In re Certain Digital Satellite System (DSS) Receivers and Components Thereof, Inv. No. 337-TA-392, Final Initial and Recommended Determination on Remedy and Bonding, USITC Pub. No. 3418 (April 2001). Where reliable price information is not available, however, Commission precedent establishes that the bond should be set at 100 percent of entered value. In re Certain Flash Memory Circuits and Products Containing Same, Inv. No. 337-TA-382, USITC Pub. 3046, Commission Opinion 26-27 (June 1997).

Complainant argued that the evidence demonstrates that a bond of 100 percent of the entered value of the imported chips is appropriate and that the bond should be calculated at a rate

of{ } per chip imported by ST during the Presidential review period. (CBr at 178.)

ST argued that in the circumstances of this case, in which complainant has licensed the '338 patent at royalty rates as low as{ } a bonding rate of{ } would be more than adequate to protect complainant from injury during the 60-day Presidential review period. (RBr at 199.)

The staff argued that complainant proposed a "bond of 100% of entered value, or{ } per chip" and that the staff has no objection if a bond of 100 percent of entered value be imposed during the two-month Presidential review period. (SRBr at 25.)

Licenses provided by SanDisk that include rights to the '338 and other patents contain royalty rates ranging from a minimum of{ } to a maximum of{ } (CX-72C { }; CX-76C{ }; CX-1456C; CX-241C{ }; CX-242C { }; CX-385C { }; CX-386C{ }; CX-1457C { }; CX-1596C { }; CX-1462C{ }) However, ST invoice summaries (ST0000001807-08 and ST000015056-000015081 (CX-91C at 13)) show that the average selling price for ST's accused products is approximately{ }. (CX-150C, obtained by adding the average selling prices for each invoice summary and dividing by 15, which is the total number of invoice summaries provided by ST.) Thus, if the Commission finds a violation, the administrative law judge recommends a bond of 100 percent of entered value or{ } per chip during the two month Presidential review period.

XIV. Additional Findings Of Fact

1. SanDisk Corporation (SanDisk) of Sunnyvale, California, is a Delaware corporation. SanDisk owns, by assignment, the '338 patent at issue, and designs, develops, and sells flash memory data storage products, including NAND flash memory circuits, for various electronic applications. (Complaint, pp. 2-3, ¶¶ 5-7; Mehrotra, Tr. at 147, 152.) SanDisk's principal office and headquarters is in Sunnyvale, California. (Mehrotra, Tr. at 147.)

2. SanDisk owns approximately 300 patents, most of which relate to flash memory technology. (Mehrotra, Tr. at 158.)

3. STMicroelectronics NV (ST Europe) of Geneva, Switzerland, a corporation organized under the laws of the Netherlands, is engaged in the design, manufacture and sale of semiconductors, including NAND flash memory products. (Complaint, p. 5, ¶¶ 12-13.)

4. STMicroelectronics, Inc. (ST US) of Carrollton, Texas, a corporation organized under the laws of Delaware, is engaged in the design, manufacture and sale of semiconductors, including NAND flash memory products, manufactured abroad by ST Europe.

5. ST US is a wholly-owned subsidiary of STNV. (Complaint, p. 5,¶¶ 12-13.) ST was ranked as the 5th largest semiconductor manufacturer in the world according to sales during 2002. (ST Resp. to the Complaint, p. 5, ¶¶ 12-13.)

6. ST is an international company that develops and produces semiconductor products for system companies. (Cassagrande, Tr. at 1171-72.) ST employs{ } individuals world-wide. (Id.)

7. ST has several facilities in the United States, including two large application manufacturing facilities. One is in Carrollton, Texas and the other one is in Phoenix, Arizona.

(Cassagrande, Tr. at 1172.)

8. ST also has several research and development centers, typically placed near or sometimes even inside the facilities of its key customers in the United States. (Cassagrande, Tr. at 1172.) ST holds approximately 5,500 U.S. patents, 650 of which are in the field of nonvolatile memory. (Cassagrande, Tr. at 1174.)

CONCLUSIONS OF LAW

1. The Commission has in rem jurisdiction and in personam jurisdiction.

2. There has been an importation of certain accused NAND flash memory circuits and products containing same, which are the subject of the alleged unfair trade allegations.

3. An industry does not exist in the United States, as required by subsection (a)(2) of section 337, that exploits the certain NAND flash memory circuits and products containing same that are covered by the '338 patent.

4. Respondents' accused products do not infringe any of the asserted claims.

5. The asserted claims of the '338 patent are not invalid.

6. The '338 patent is enforceable.

7. There is no violation of section 337.

8. If the Commission should find a violation, the record supports issuance of a limited exclusion order, a cease and desist order, and a bond in the amount of 100 percent of the entered value for any importation involving infringing products during the Presidential review period.

ORDER

Based on the foregoing, and the record as a whole, it is the administrative law judge's Final Initial Determination that there is no violation of section 337 in the importation into the United States, sale for importation, and the sale within the United States after importation of certain NAND flash memory circuits and products containing same. It is also the administrative law judge's recommendation that, if the Commission should find a violation, a limited exclusion order and a cease and desist order should issue and a bond should be imposed, during the Presidential review period, in the amount of 100 percent of the entered value for any importation involving infringing products.

The administrative law judge hereby CERTIFIES to the Commission his Final Initial and Recommended Determinations together with the record consisting of the exhibits admitted into evidence. The pleadings of the parties filed with the Secretary and the transcript of the pre-hearing conference and the hearing, including closing arguments, are not certified since they are already in the Commission's possession in accordance with Commission rules.

Further it is ORDERED that:

1. In accordance with Commission rule 210.39, all material heretofore marked in camera because of business, financial and marketing data found by the administrative law judge to be cognizable as confidential business information under Commission rule 201.6(a) is to be given in camera treatment continuing after the date this investigation is terminated.

2. Counsel for the parties shall have in the hands of the administrative law judge those portions of the final initial and recommended determinations which contain bracketed confidential business information to be deleted from any public version of said determinations

no later than November 4, 2005. Any such bracketed version shall not be served by fax on the administrative law judge. If no such bracketed version is received from a party it will mean that the party has no objection to removing the confidential status, in its entirety, from these initial and recommended determinations.

3. The initial determination portion of the Final Initial and Recommended Determinations, issued pursuant to Commission rule 210.42(h)(2), shall become the determination of the Commission forty-five (45) days after the service thereof, unless the Commission within that period shall have ordered its review or certain issues therein or by order has changed the effective date of the initial determination portion. The recommended determination portion, issued pursuant to Commission rule 210.42(a)(1)(ii), will be considered by the Commission in reaching a determination on remedy and bonding pursuant to Commission rule 210.50(a).

Paul J. Luckern
Administrative Law Judge

Issued: October 19, 2005

CERTAIN NAND FLASH MEMORY CIRCUITS AND PRODUCTS CONTAINING SAME **Investigation No. 337-TA-526**

CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the attached **Public Version Final Initial and Recommended Determinations Order** was served by hand upon Commission Investigative Attorney Juan Cockburn, Esq. and upon the following parties via first class mail, and air mail where necessary, on January 17, 2006.

Marilyn R. Abbott

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CERTAIN NAND FLASH MEMORY CIRCUITS AND PRODUCTS CONTAINING SAME **Investigation No. 337-TA-526**

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