Metrology Challenges Associated With Gate Dielectric Scaling, Including the Vertical, Replacement-Gate MOSFET

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Outline

- **Drivers for scaling**
- **Scaled gate oxide**
- **High-κ gate dielectrics**
- **Replacement gate processes**
- **Vertical Replacement Gate**

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Outline

- **Drivers for scaling**
  - **Density**
  - **Performance**
  - **Recent history: hyperscaling of gate oxide and gate length**
- **Scaled gate oxide**
- **High-k gate dielectrics**
- **Replacement gate processes**
- **Vertical Replacement Gate**

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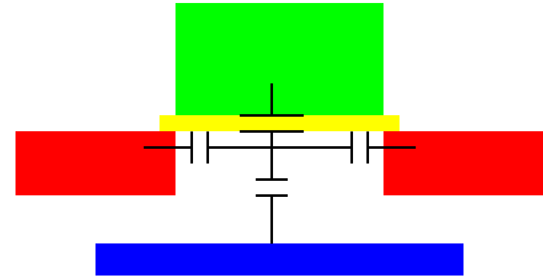
Why Scale T_{ox}?

1. Better gate control of channel

- thinner T_{ox} helps for shorter gates
- other “knobs” available



2. Increased *drive* through C'_{ox}

$$f \sim \frac{I_D}{C_{total} V_{DD}} = \frac{C'_{ox} W (V_{DD} - V_T) v_{sat}}{(C'_{ox} W L + C_{ext}) V_{DD}}$$

Improvement from increased C'_{ox} depends on:

$$\eta = \frac{C'_{ox} W L}{C'_{ox} W L + C_{ext}}$$

Gate-loaded circuits ($\eta \sim 100\%$)
no speed improvement

Interconnect-loaded circuits ($\eta << 100\%$)
big speed improvement
But we could have scaled width *W*!

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1999 ITRS*

Memory and Logic Technology Requirements -- Near Term

YEAR *TECHNOLOGY NODE*	*1999* *180 nm*	*2000*	*2001*	*2002* *130 nm*	*2003*	*2004*	*2005* *100 nm*
MPU GATE LENGTH (nm)	140	120	100	85	80	70	65
Minimum Logic Vdd (V) (desktop)	**1.5-1.8**	**1.5-1.8**	**1.2-1.5**	**1.2-1.5**	**1.2-1.5**	**0.9-1.2**	**0.9-1.2**
T_{ox} equivalent (nm)	**1.9-2.5**	**1.9-2.5**	**1.5-1.9**	**1.5-1.9**	**1.5-1.9**	**1.2-1.5**	**1.0-1.5**
Nominal I_{on} @ 25°C μA/μm) [NMOS/PMOS] high performance	**750/350**	**750/350**	**750/350**	**750/350**	**750/350**	**750/350**	**750/350**
Maximum I_{off} @ 25°C (μA/μm) [NMOS/PMOS] high performance	**5**	**7**	**8**	**10**	**13**	**16**	**20**
Percent static power reduction necessary due to innovative circuit/system design	**0**	**33**	**48**	**55**	**71**	**77**	**81**

*** International Technology Roadmap for Semiconductors**
December 1999

Difficult Challenge (before 2005): "*Production worthy high k dielectrics and compatible gate materials will not be available.*"

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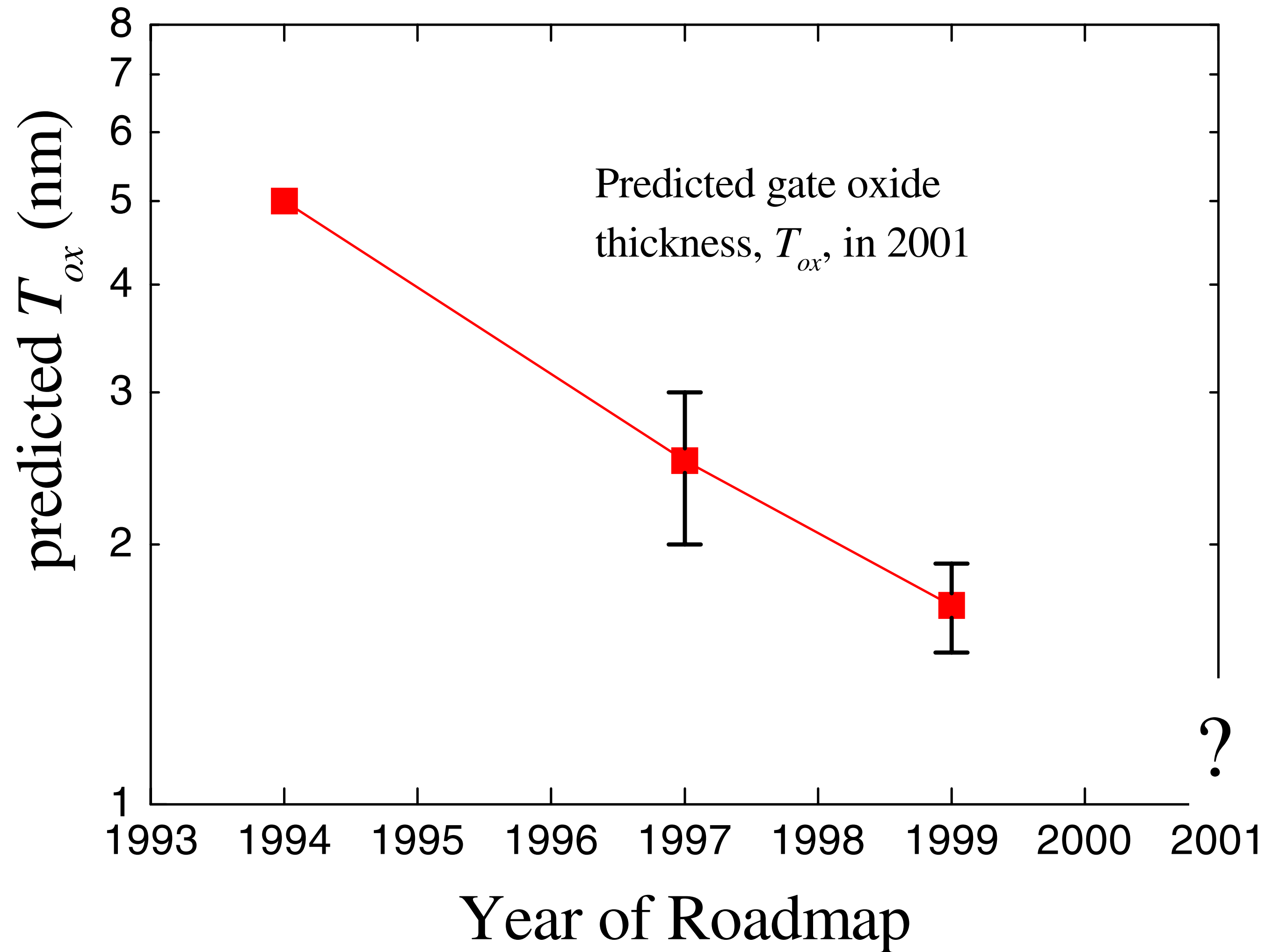
Moore Plot of Moore's Law



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Memory and Logic Technology Requirements -- Long Term

YEAR TECHNOLOGY NODE	*2008 70 nm*	*2011 50 nm*	*2014 35 nm*
MPU GATE LENGTH (nm)	***45***	***32***	***22***
Minimum Logic Vdd (V) (desktop)	**0.6-0.9**	**0.5-0.6**	**0.3-0.6**
T_{ox} equivalent (nm)	**0.8-1.2**	**0.6-0.8**	**0.5-0.6**
Nominal I_{on} @ 25°C (μA/μm) [NMOS/PMOS] high performance	**750/350**	**750/350**	**750/350**
Maximum I_{off} @ 25°C (μA/μm) [NMOS/PMOS] high performance	**40**	**80**	**100**
Percent static power reduction necessary due to innovative circuit/system design	**91**	**97**	**98**

*** International Technology Roadmap for Semiconductors**
December 1999

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Outline

- Drivers for scaling
- Scaled gate oxide
  - ~~manufacturing yield~~
  - Boron penetration
  - reliability
  - tunneling current
  - diminishing returns in capacitance
  - degraded mobility
- High-k gate dielectrics
- Replacement gate processes
- Vertical Replacement Gate

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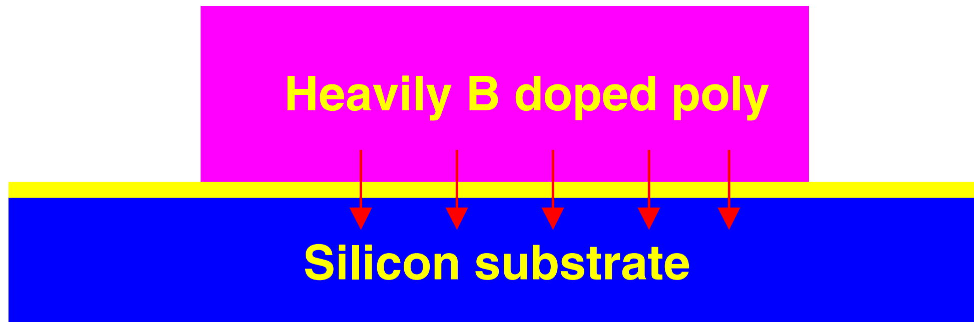
Boron Penetration



Typical dopant-activation
RTA 1000°C, 5 sec

- Boron from p-poly gate shifts pMOS threshold voltage
  - 10^{11}-10^{12} cm^{-2} is a problem
  - Only *electrical* measurement is sensitive enough
- *Repeatability* is the key issue
- Depends sensitively on thermal cycle
- Dependes sensitively on oxide thickness
- BF_2 assists boron transport
- *Nitrogen engineering can buy process margin*

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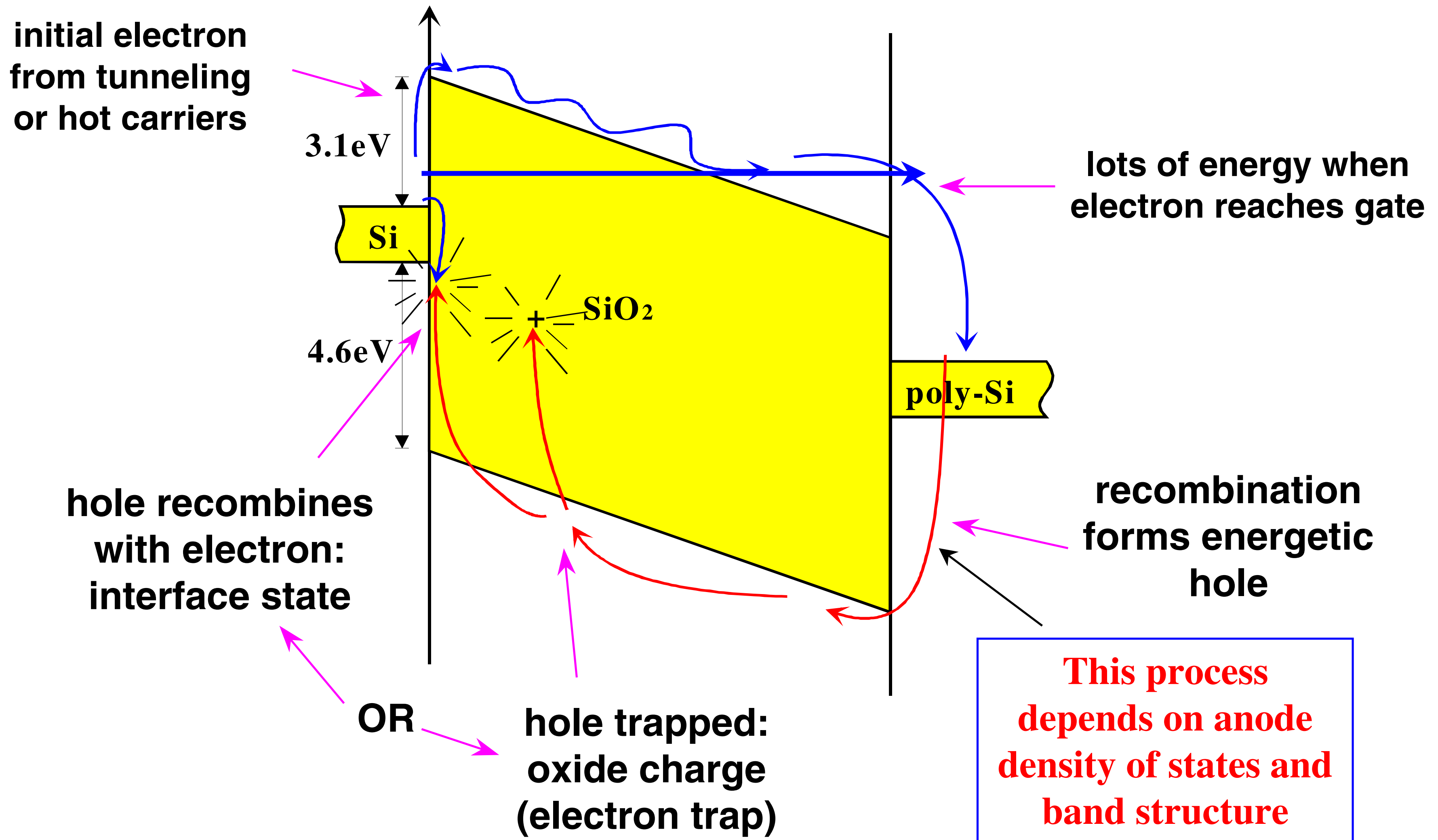
Anode Hole Injection Model



Chen et al. APL ’86
Updated Bude et al. IEDM ’98

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Percolation Model for Breakdown

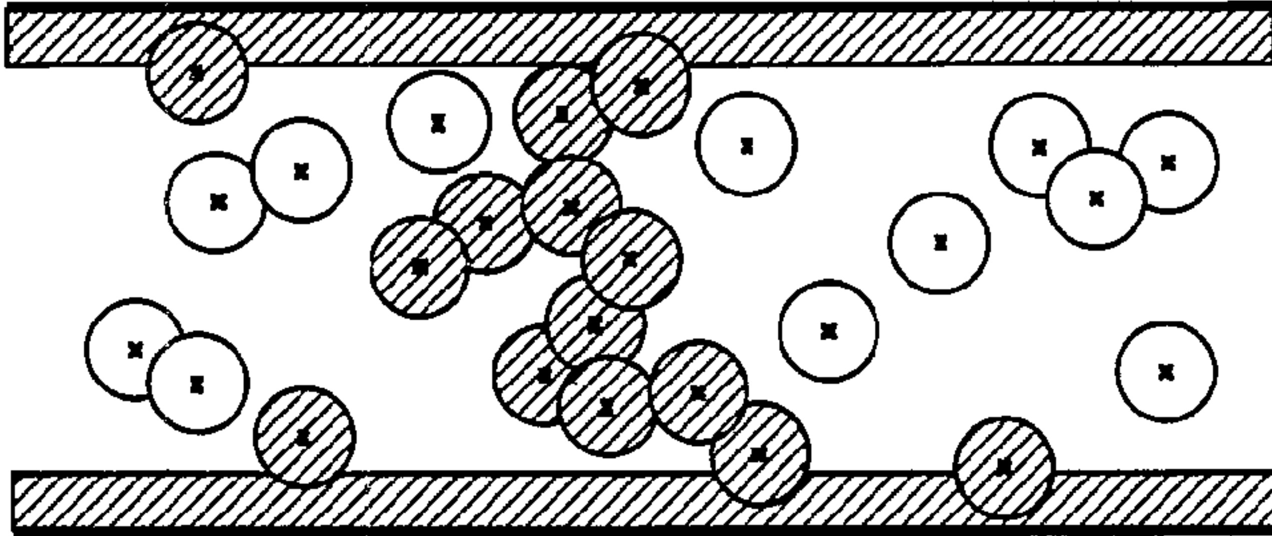

Fig. 7. Schematic illustration of the spheres model for intrinsic oxide breakdown simulation based on trap generation and conduction via traps. A breakdown path is indicated by the shaded spheres.

Degraeve et al, TED **45(4),** 904(1998) (IMEC)

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“Soft” Breakdown

- **Sudden event**
  - **increase in current or current noise**
  - ***not* a resistive shunt afterwards**
- **More prevalent:**
  - **For thin oxides**
  - **At low voltages**
  - **For small areas (like transistors)**
- **New Model (Alam *et al.* ’99 IEDM)**
  - **Explains many features**
  - **Breakdown soft if power is below a threshold**
- **Circuit Implications**
  - **Some transistors still function**
  - **What can we live with?**

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Soft Breakdown Data

Weir et al, ’97 IEDM

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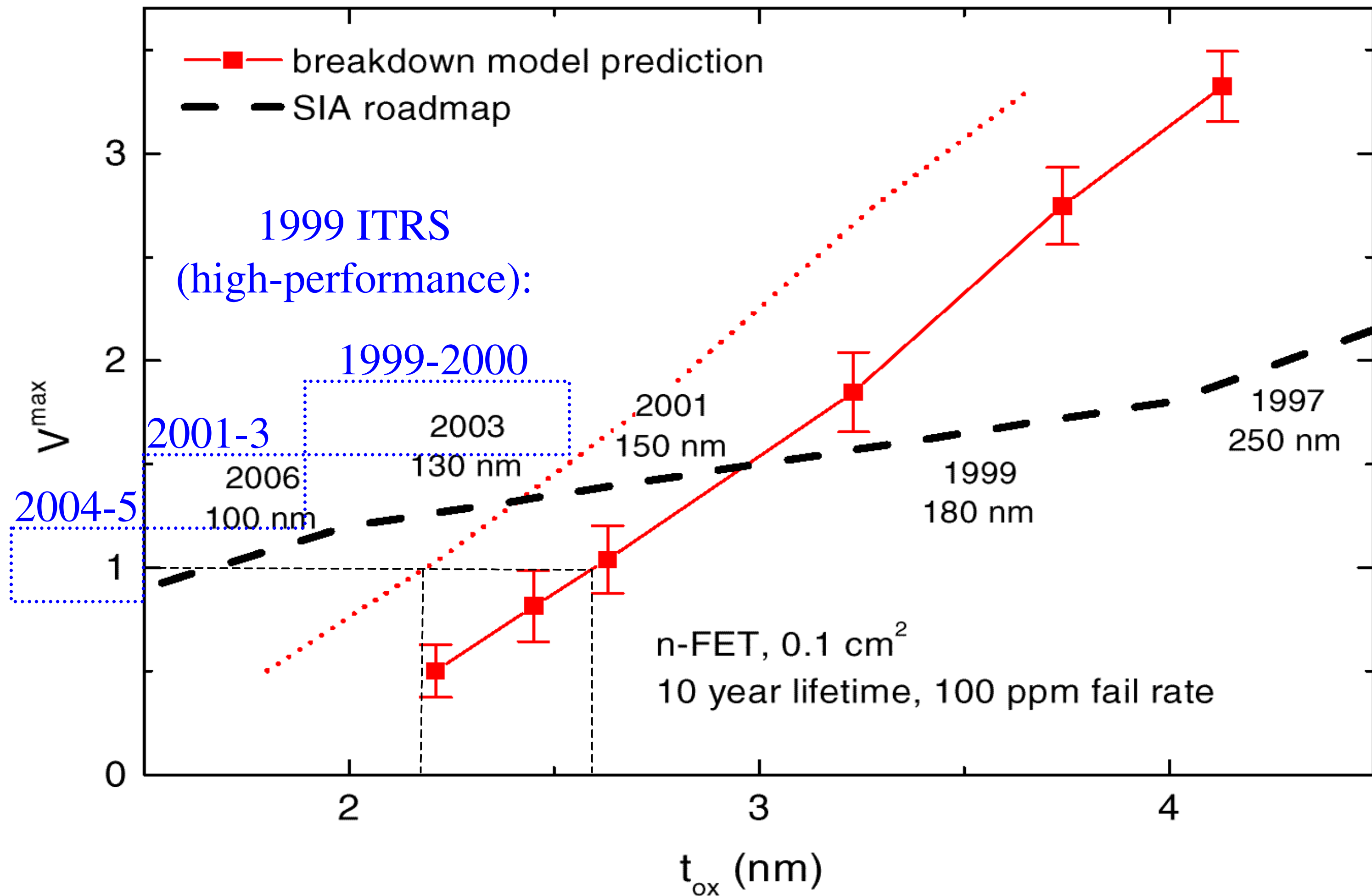
The IBM "Doomsday Scenario"



Stathis *et al.*, IEDM '98, pp167 (IBM)

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Reliability of SiO_2

- Reliability *determines* useful oxide thickness
- Time-dependent dielectric breakdown (TDDB)
  - Not voltage for instantaneous breakdown
  - Need stressing of tens of samples for days or more
  - Depends on much more than electric field: electrode type, polarity, thickness, temperature, ...
- Breakdown is getting softer
- Other reliability issues (not discussed here)
  - Process-induced damage
  - Stress-induced leakage current
  - Negative Bias-Temperature Instability
  - Hot-carrier reliability at high V_{DS}

Current estimate of limit: $T_{ox,\ physical} \sim 1.5\text{nm}$
general agreement among Lucent, IBM, IMEC (see IRPS 2000)

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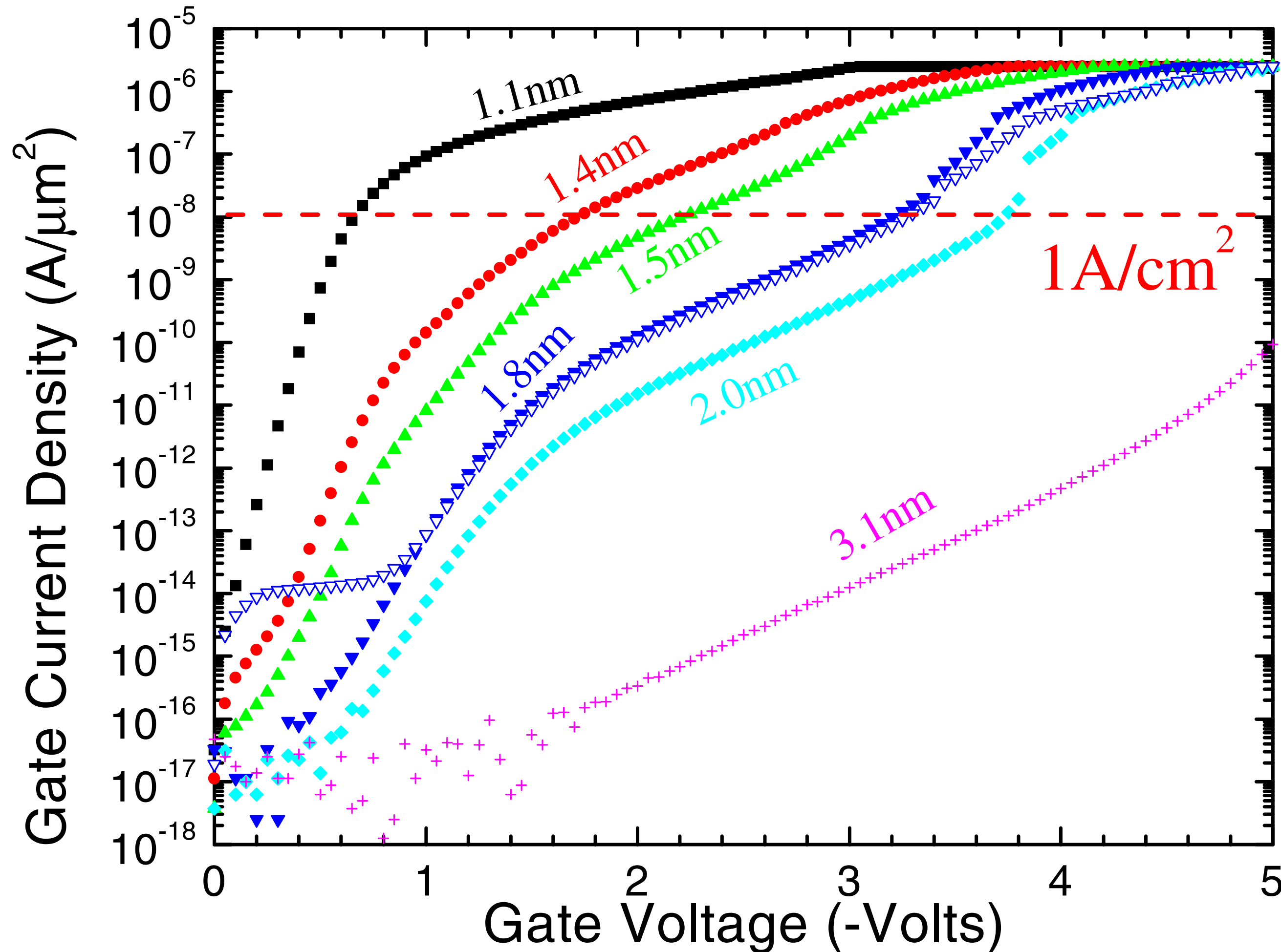
SiO_2 Tunneling Current



Sorsch et al., '98 VLSI Symposium

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What's the Tunneling Current Limit?

- **Historical:** 34Å
- **Recent Past: 1 A/cm^2** ⇒ 16Å SiO_2
- **Intel, AMD*: > 100 A/cm^2 !** ⇒ 11–12Å nitrided SiO_2
- **TSMC* ultra low power: < 10^{-3} A/cm^2 !** ⇒ 26Å

*VLSI Technology Symposium, June, 2000

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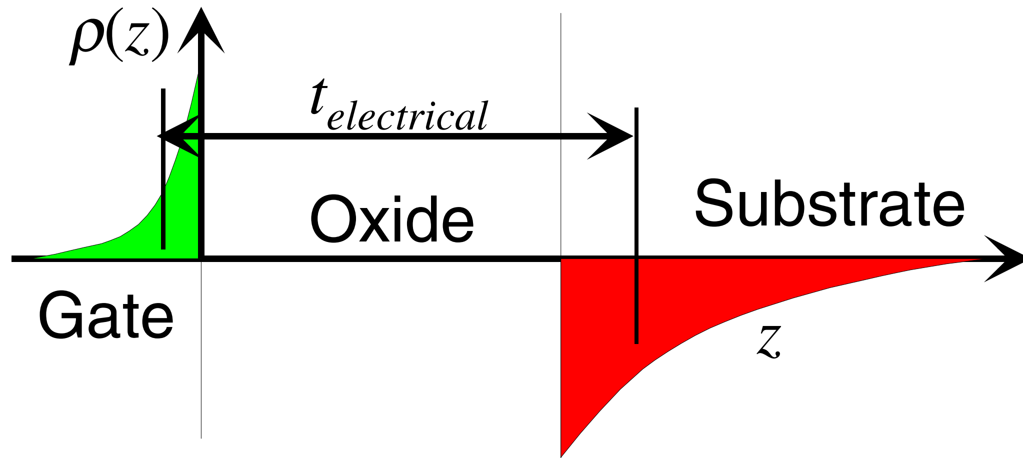
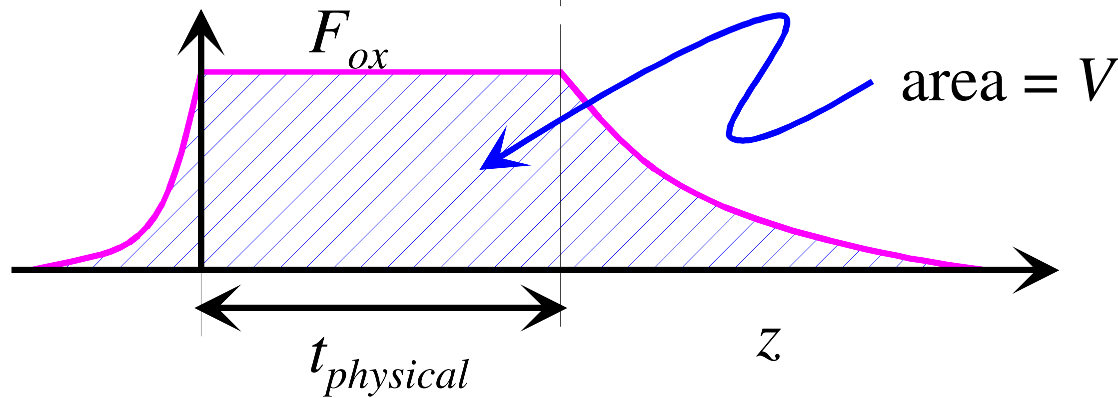
F_{ox} from CV

Charge Density



Electric Field



No charge in "bulk" of oxide: $F_{ox} = \frac{1}{\varepsilon\varepsilon_o A} Q_{gate} = \frac{1}{\varepsilon\varepsilon_o A} \int^V C(V')dV'$

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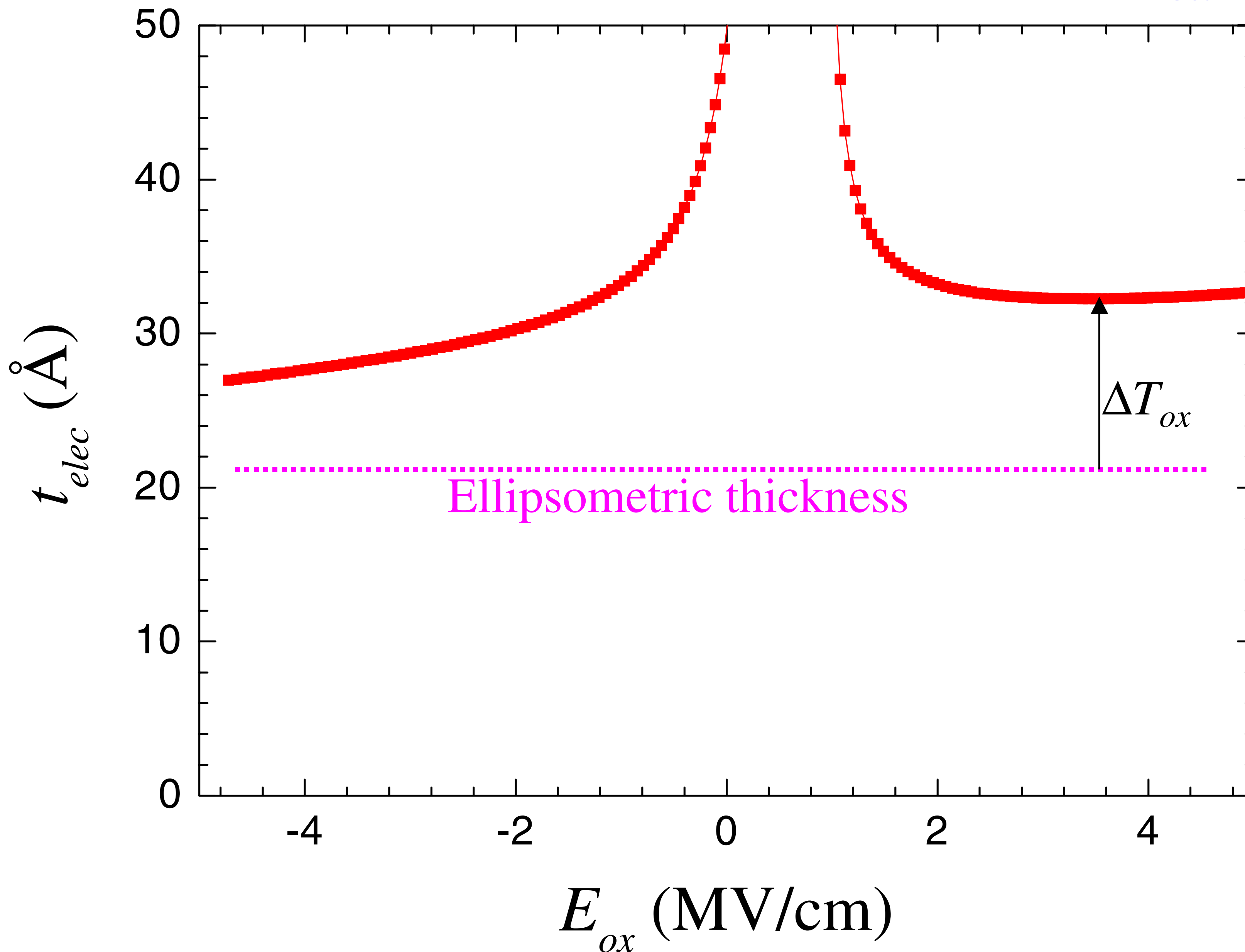
Corrections depend only on F_{ox}



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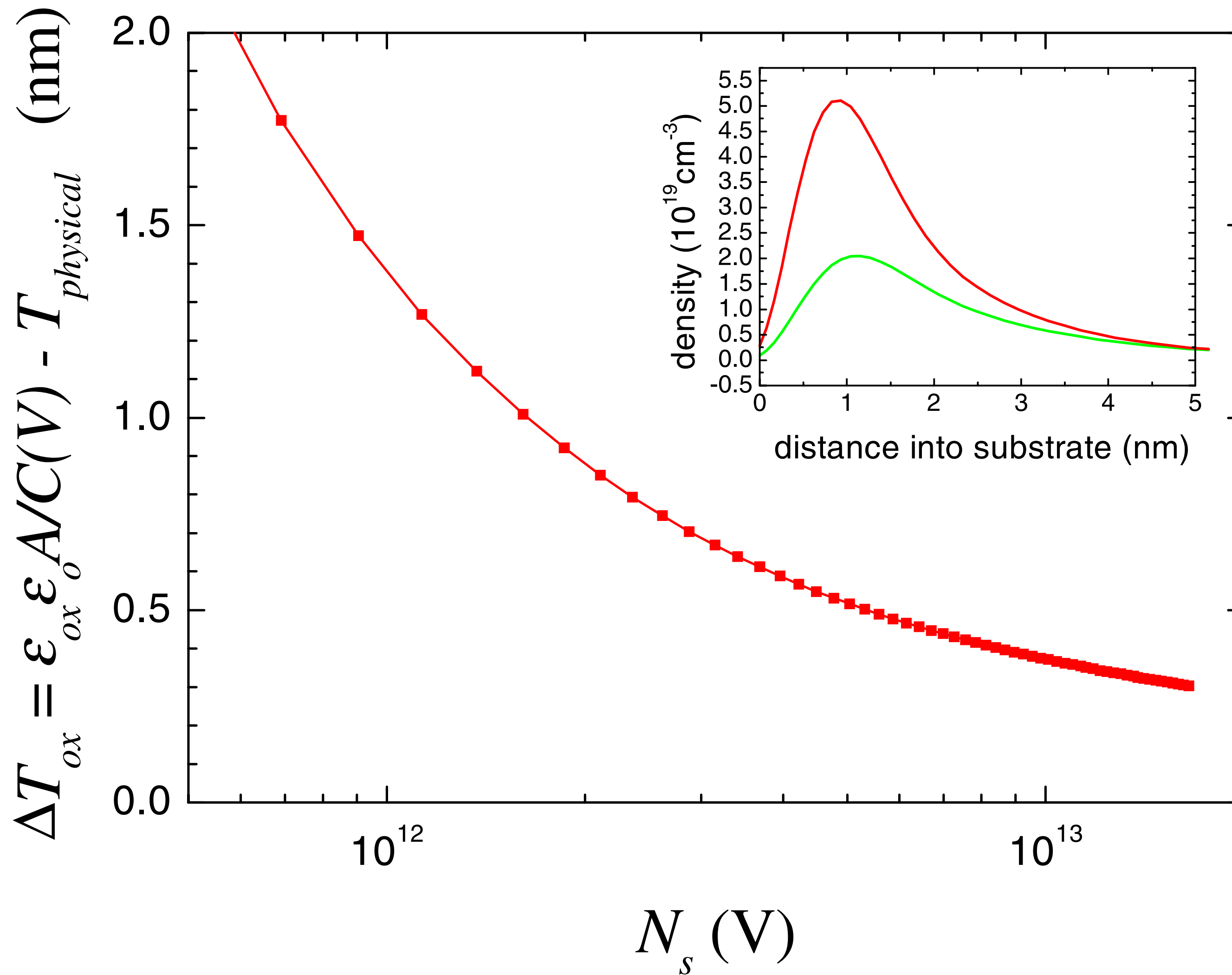
Calculated ΔT_{ox} in Substrate



Andrea Ghetti: Poisson and many-subband Schrodinger simulation

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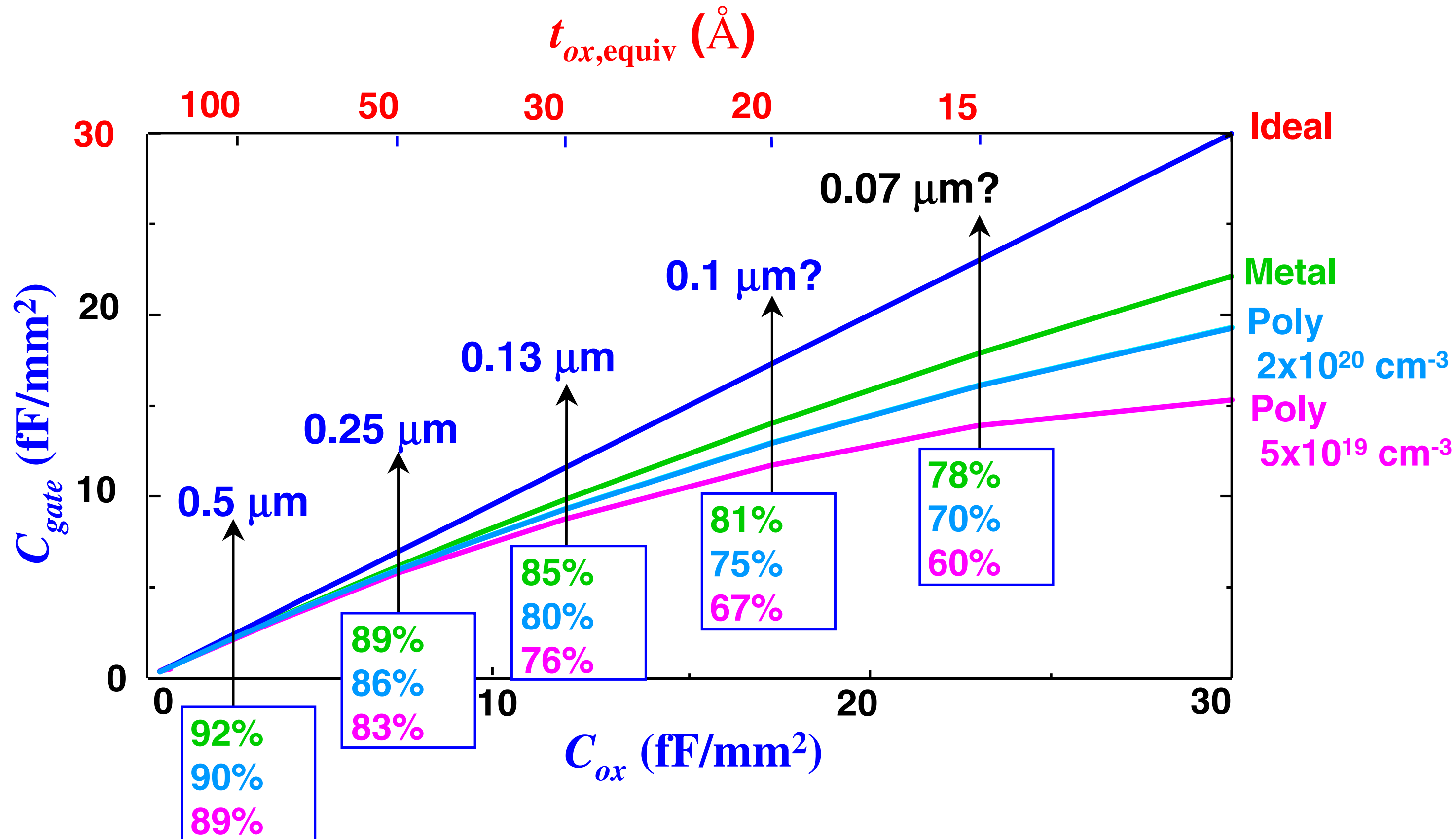
Scaling Oxide is Not Enough



- **Quantum effects become significant**
- **Must scale C_{gate}, not C_{ox}**

Kathy Krisch, 1997 VLSI Symposium

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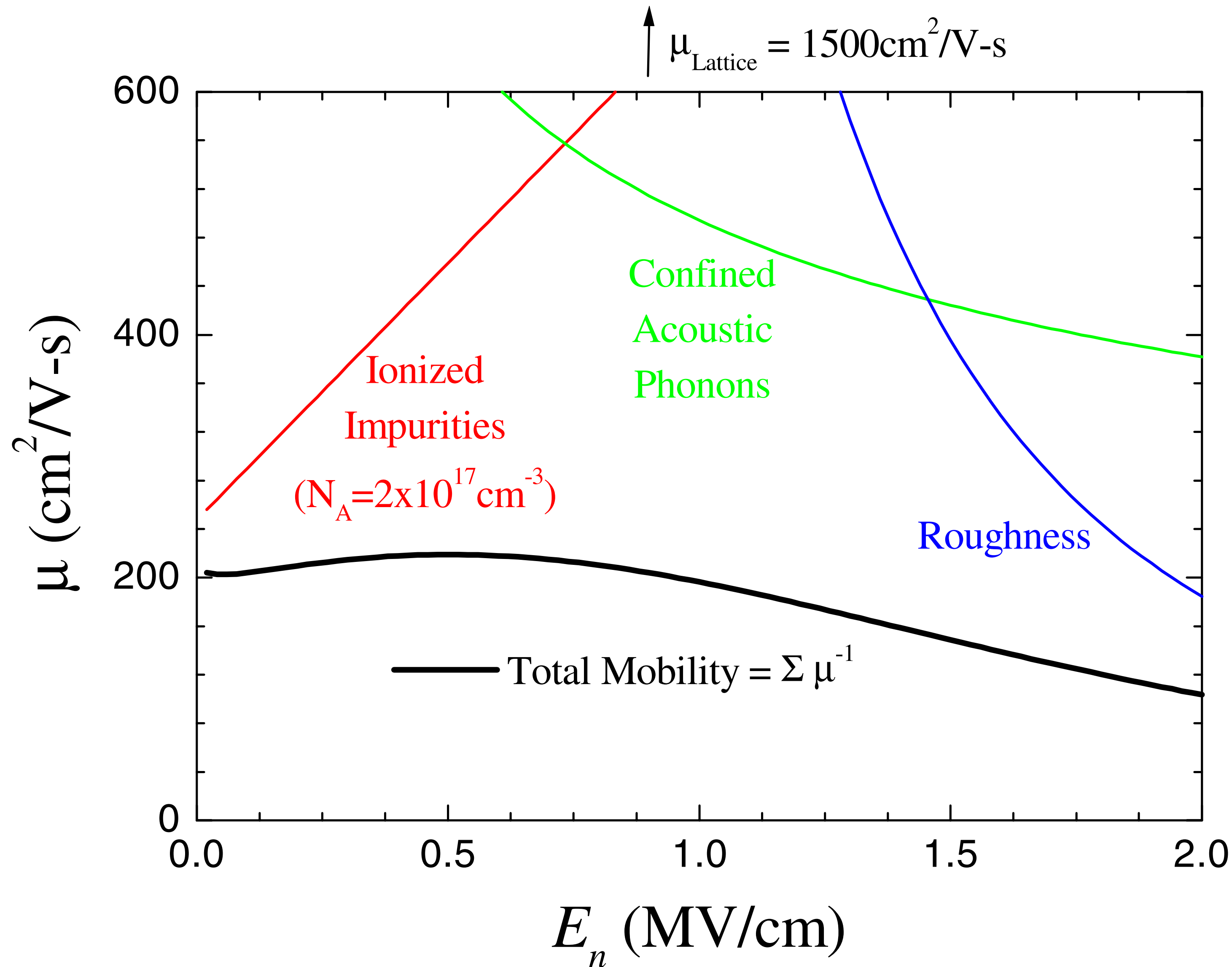
Mobility-limiting Mechanisms



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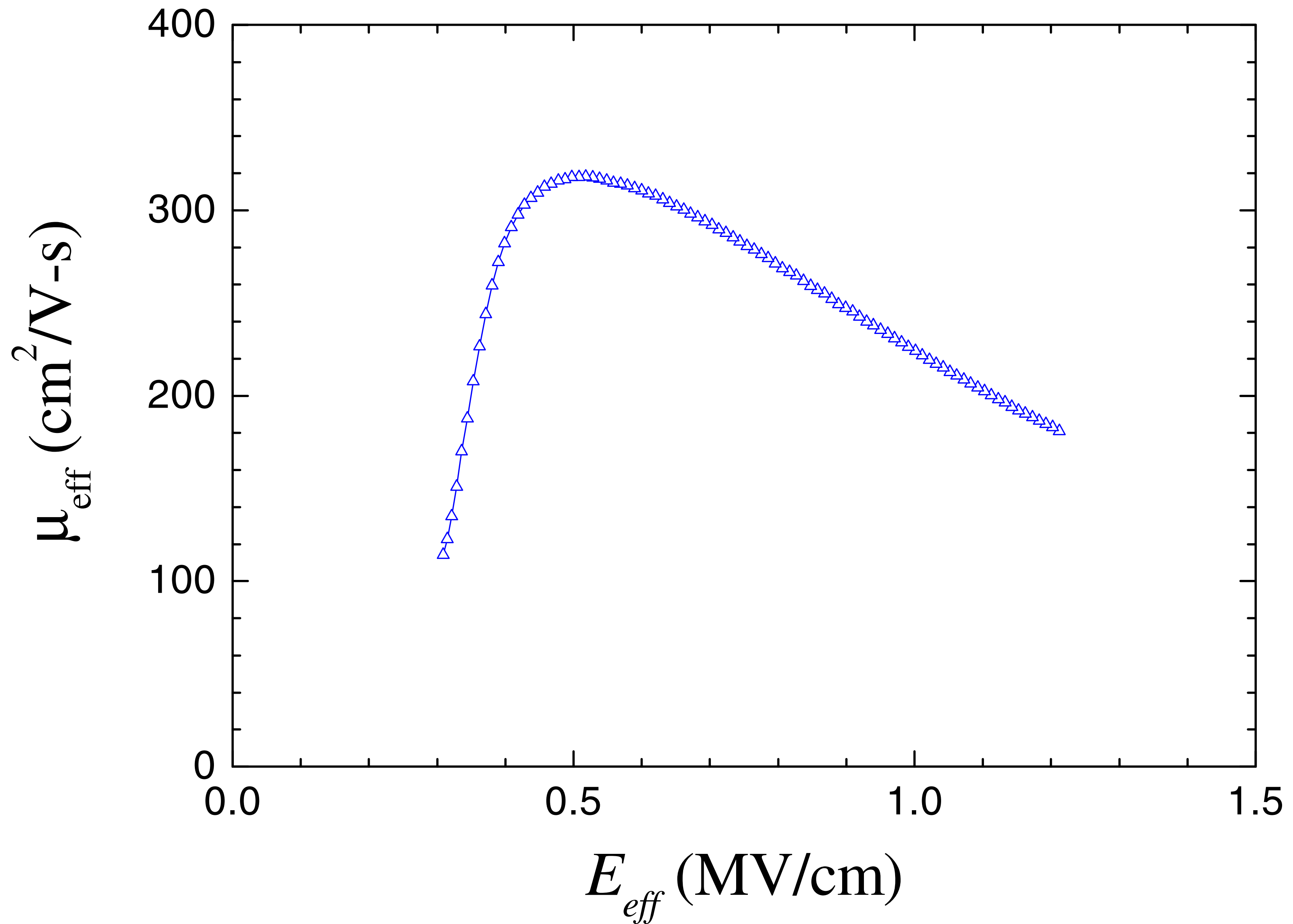
Mobility for t_{ellips} 20.7Å



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Oxide Scaling

- **Difficulties**
  - Boron penetration
  - Reliability
  - Tunneling current
- **Diminishing returns**
  - Capacitance corrections
  - Mobility degradation

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Outline

- Drivers for scaling
- Scaled gate oxide
- High-κ gate dielectrics
  - materials and processing challenges
  - characterization challenges
- Replacement gate processes
- Vertical Replacement Gate

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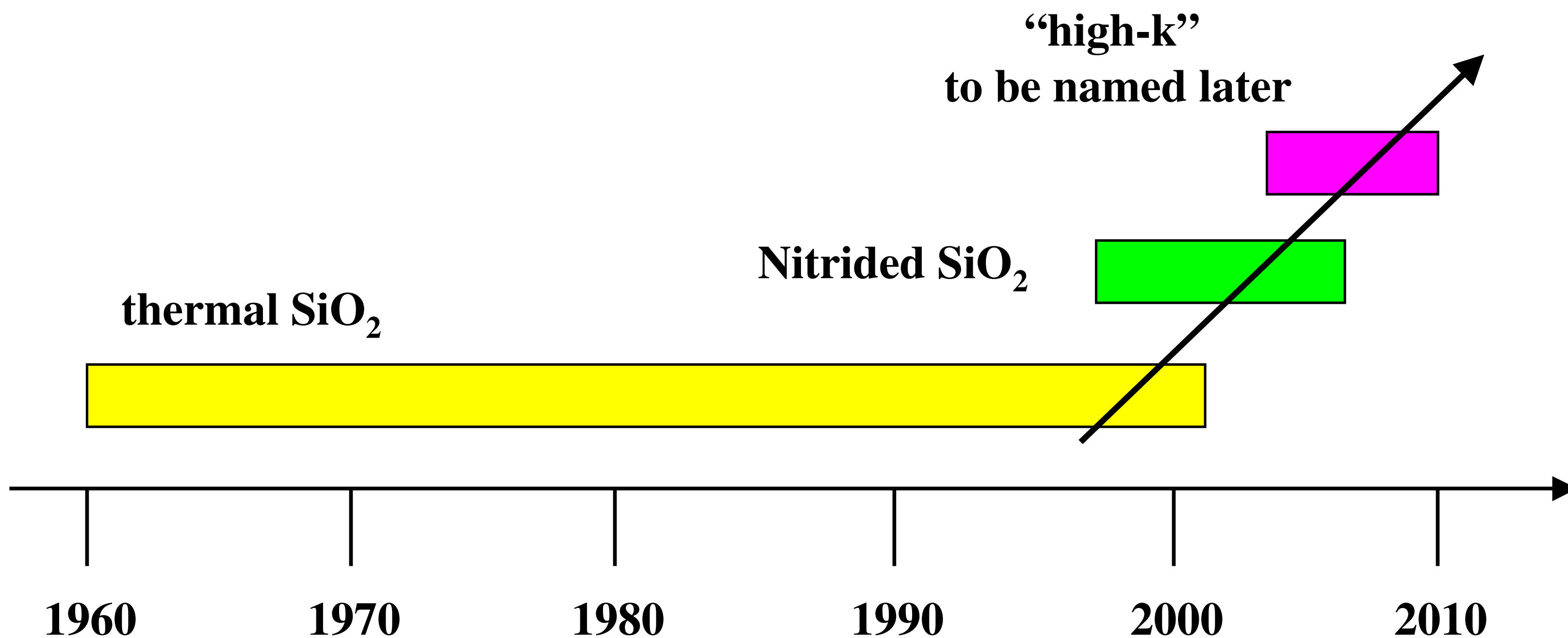
One View of Gate Dielectric Transition



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Si/SiO_2 Interface Properties

- Known preparation techniques (cleans+anneal)
- Low interface state density (<1/10,000 after H_2)
- Very low fixed charge
- No extrinsic scattering (?)
- Thermally stable
- Atomically abrupt
- Strained SiO_2 layer unless annealed above 900ºC

35 years of experience!

It’s not Si, it’s SiO_2 that makes CMOS work!
It’s not SiO_2, it’s the Si/SiO_2 interface!

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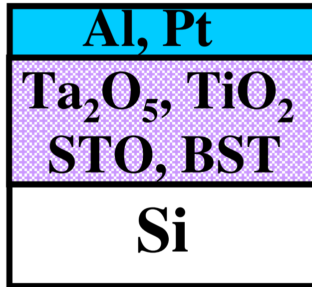
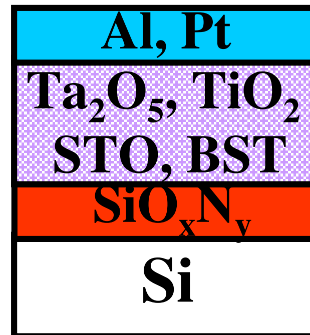
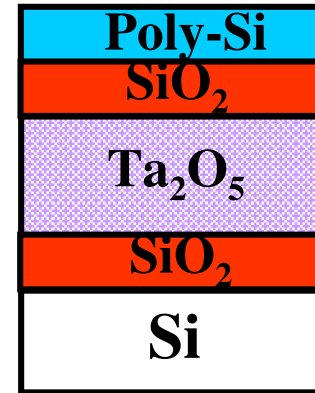
High-κ Gate Stack Approaches

High-κ on Si Metal gate	Bottom Barrier	Top and Bottom Barrier







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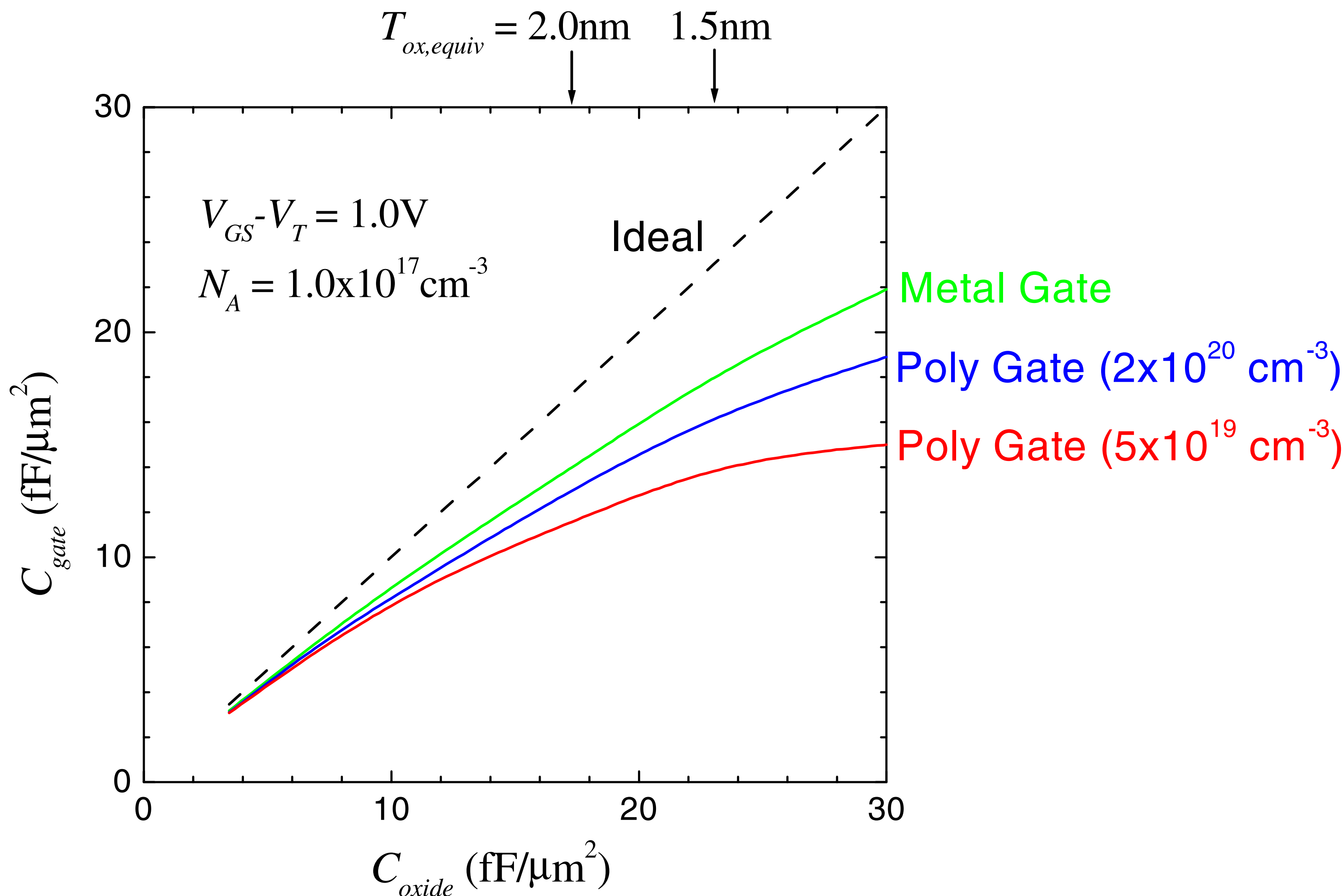
Metal-gate Improvement?



With Kathy Krisch and Jeff Bude, '97 VLSI Symp.

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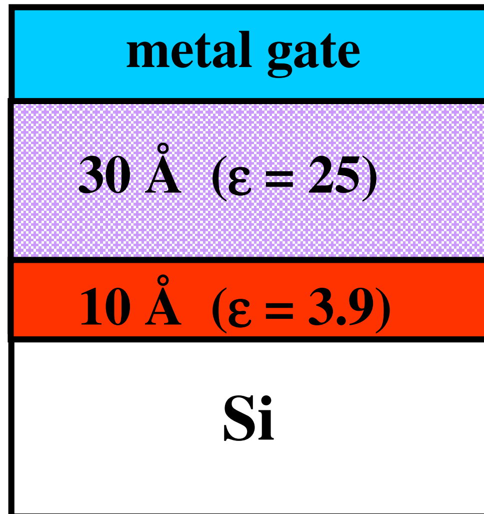
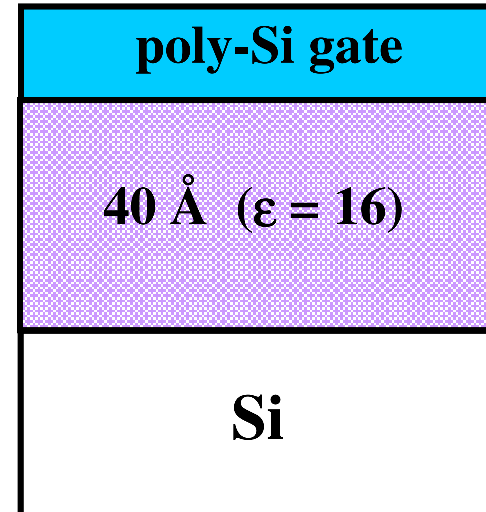
Possible High-κ Stacks





Metal gate with SiO_2 barrier.
Much of the electrical thickness "budget" is used by the SiO_2 layer.

Si-compatible dielectric
Retains compatibility with poly-Si gate

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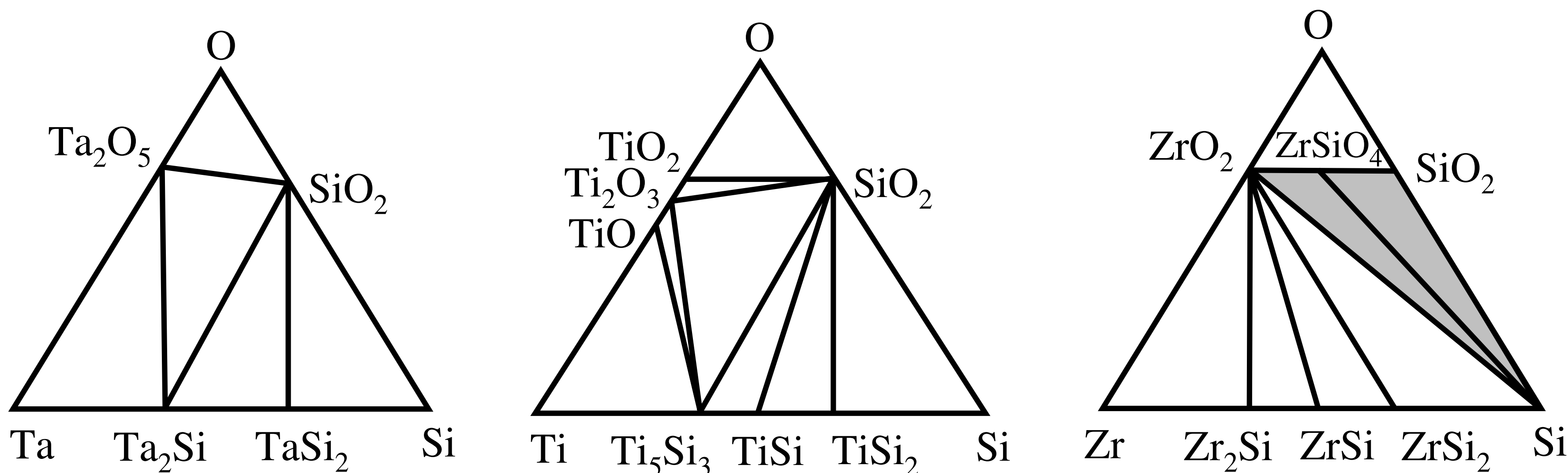
Stability of Silicates (700 - 900ºC)

After Beyers, J. Appl. Phys. **56**, 147 (1984)
and Wang and Mayer, J. Appl. Phys. **64**, 4711 (1988)



- $ZrO_2/ZrSi_xO_y$ stable next to Si; Ta and Ti oxide/silicate not stable
- Zr, Hf Silicates: no interfacial layer required AND can be used with poly-Si(Ge) gates

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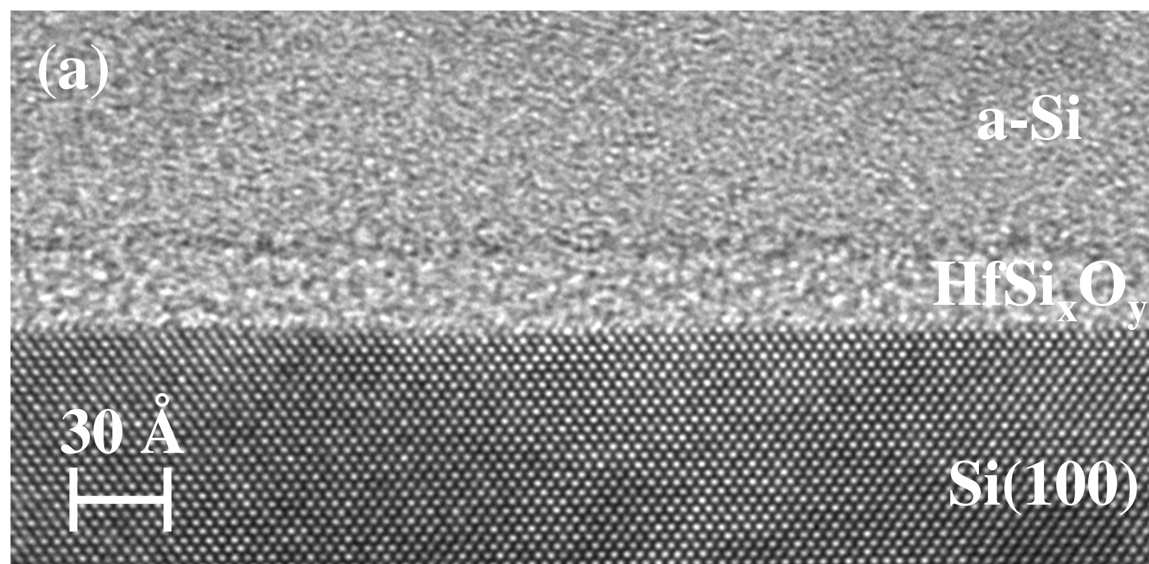
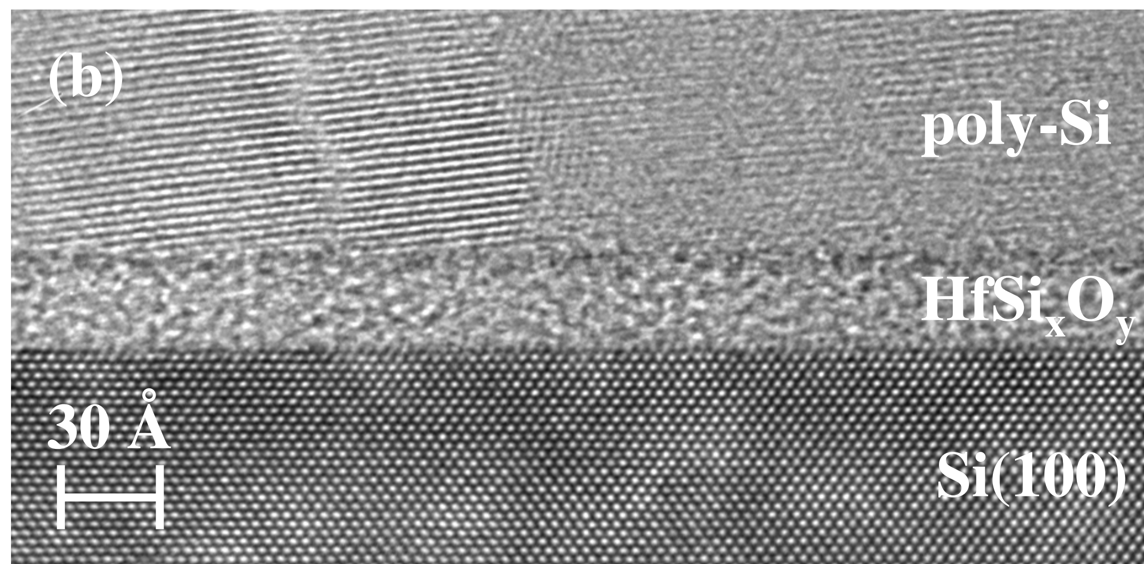
Stability of Hafnium Silicates on Si

As-Deposited
top Si at 25ºC



After Anneal
N_2/1050ºC/20 sec



Courtesy G. Wilk
formerly TI,
now Bell Labs

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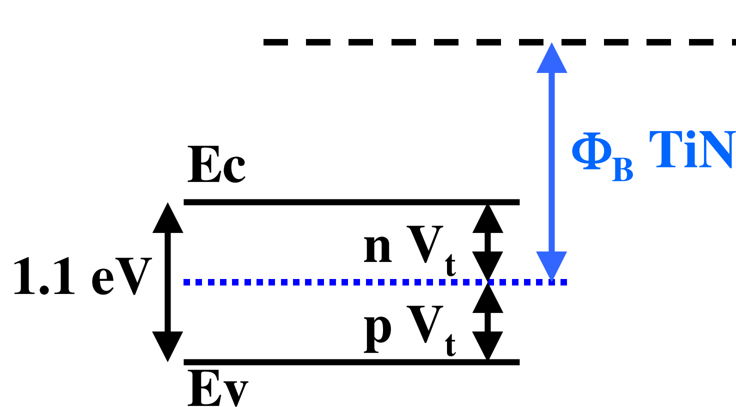
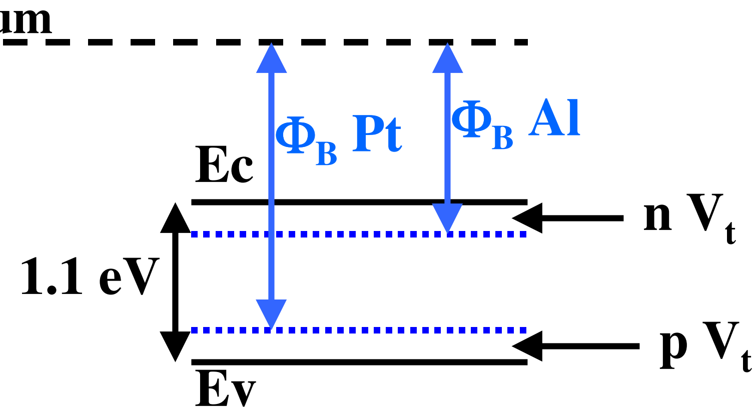
Metal-Gate Challenges





Metal Electrodes

- Metals eliminate poly depletion and B penetration
- Midgap metals force V_t ~ 0.5 eV - too high
- Dual metals achieve low V_t, but difficult & costly processing

Poly-Si Electrodes

- Poly-Si allows same gate, only alter doping
- Poly depletion and B penetration must be addressed

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Outline

- Drivers for scaling
- Scaled gate oxide
- High-k gate dielectrics
- **Replacement gate processes**
  - **Non-planar geometry**
- Vertical Replacement Gate

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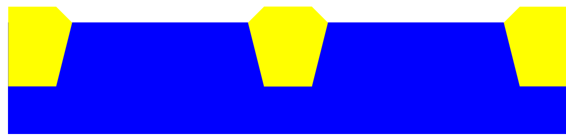
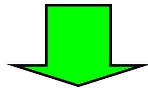
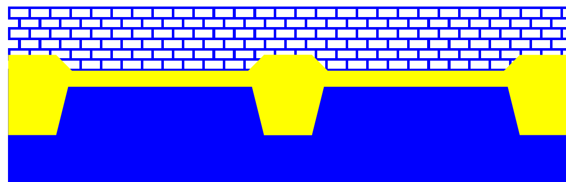
Standard *vs.* Replacement Gate*

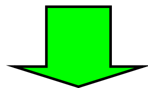


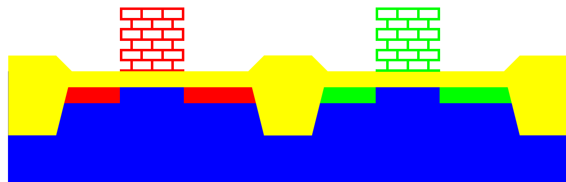
Substrate with isolation



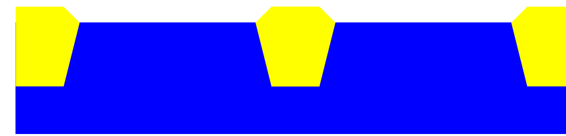


Clean; Grow gate oxide;
Deposit undoped poly

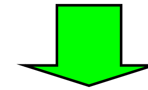


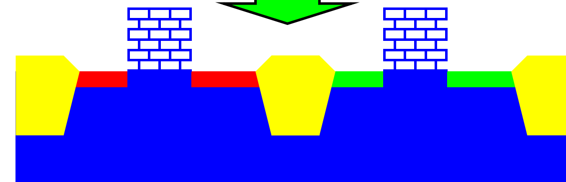


Etch Gates; implants; anneal

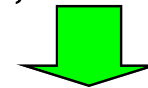


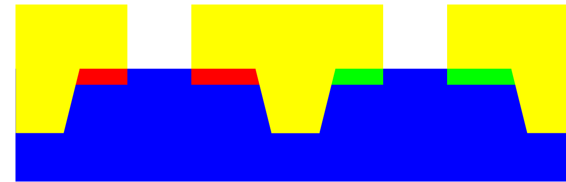
Substrate with isolation



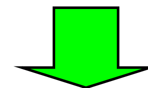


Deposit and Etch Gates;
implants; anneal





Deposit interlayer dielectric;
remove dummy gate



Deposit Gate Dielectric
and Gate Metal

*A. Chatterjee *et al.* (TI) '97 IEDM

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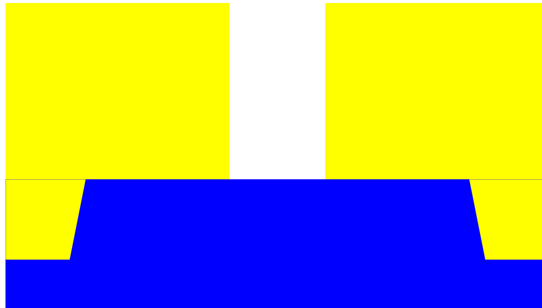
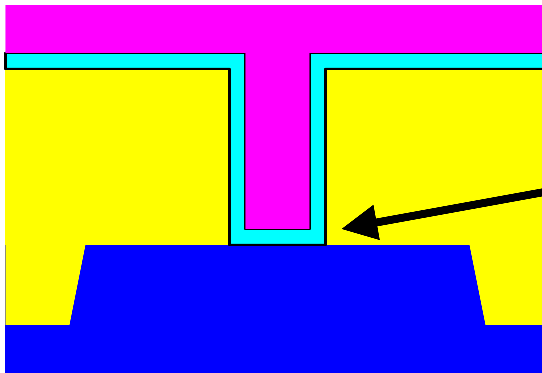
Replacement-Gate Challenges



Standard high-κ challenges



- Ultra-conformal deposition
- Properties of film in corner

Risk of new process
Critical CMP process

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Outline

- Drivers for scaling
- Scaled gate oxide
- High-k gate dielectrics
- Replacement gate processes
- **Vertical Replacement Gate**
  - **Nonlithographic gate length control**
  - **Increased drive without scaling oxide**
  - **New knobs, new challenges**

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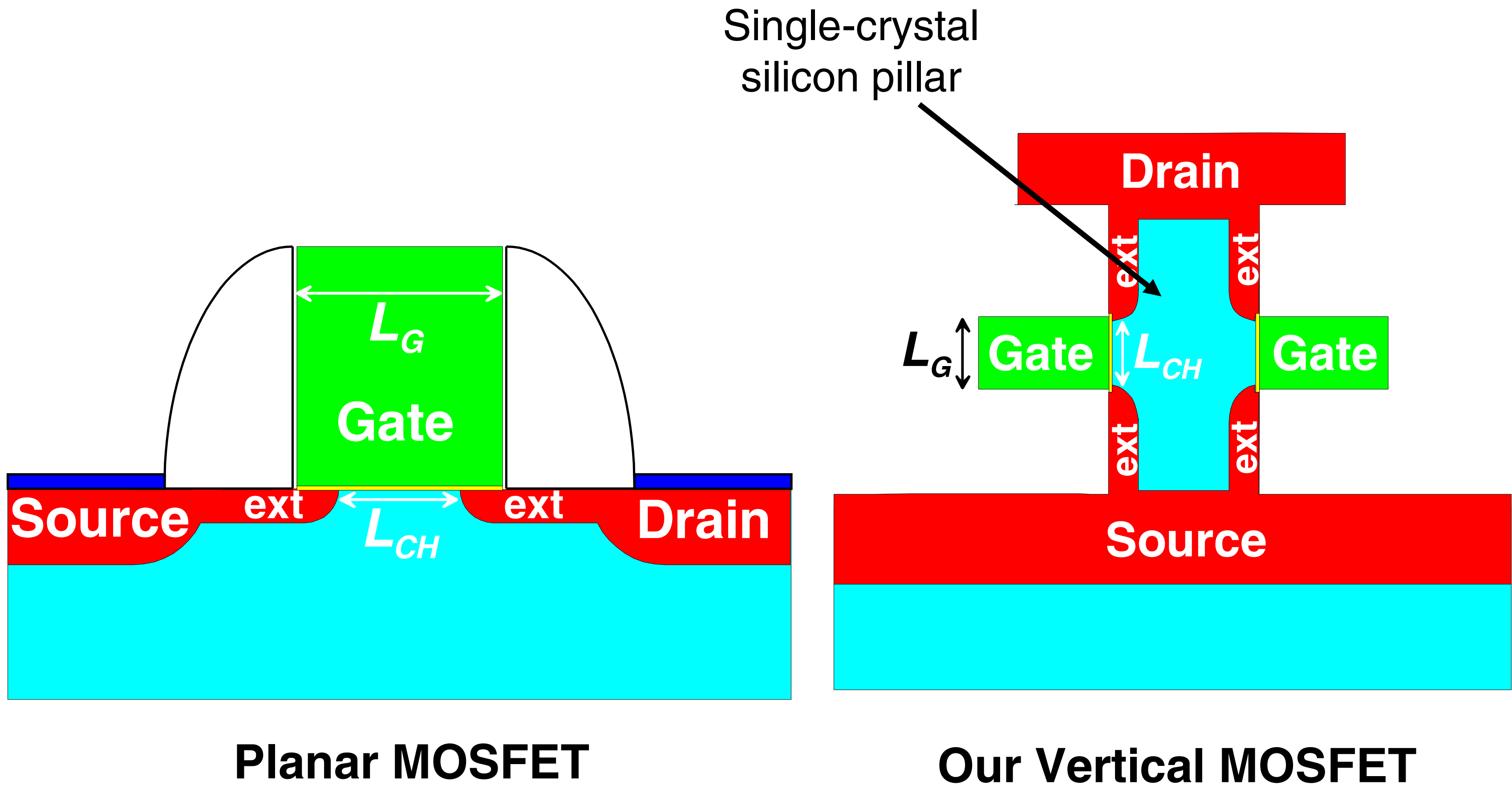
Comparison with Planar MOSFET



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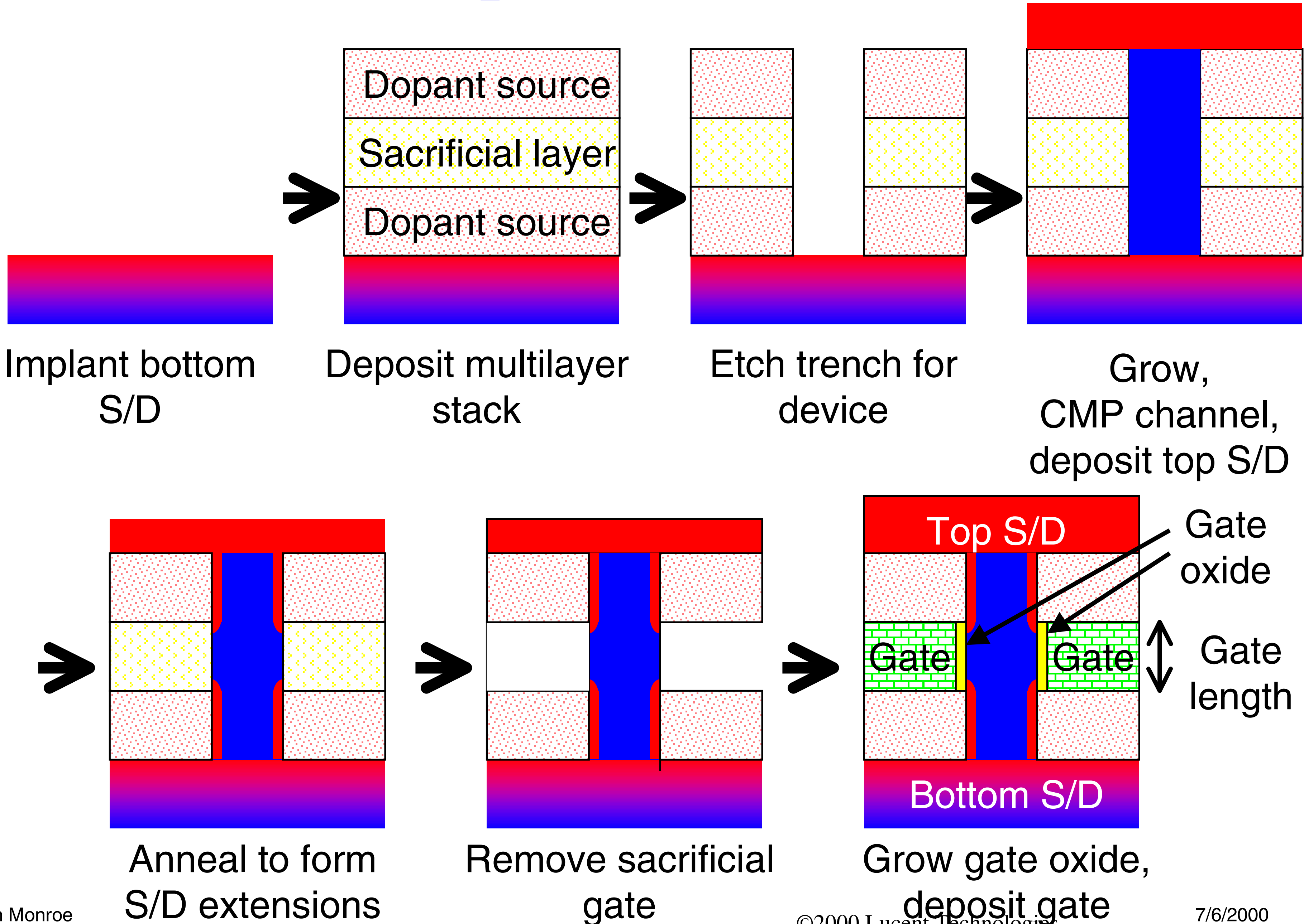
Vertical, Replacement-Gate Process



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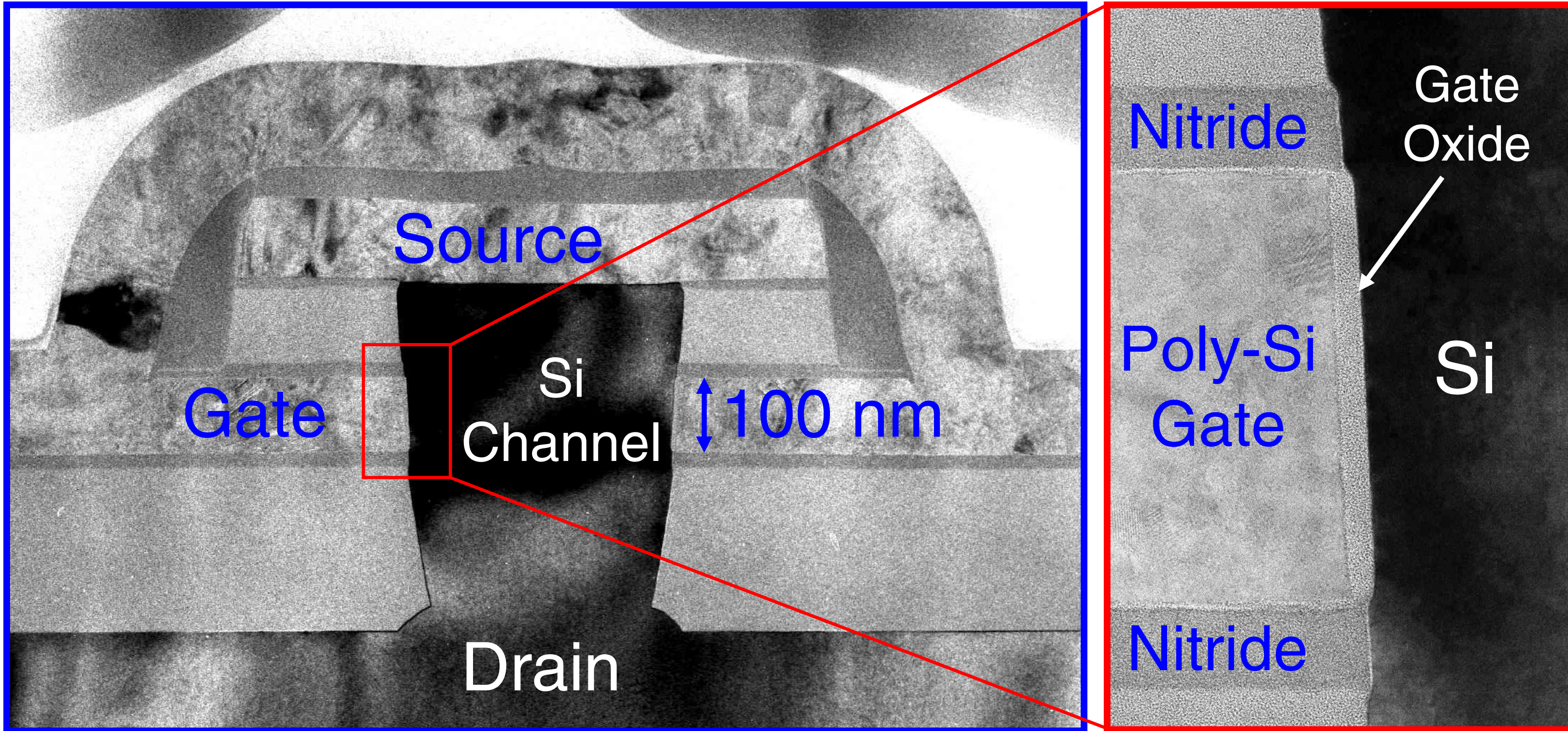
100 nm VRG MOSFET



Gate length controlled precisely through a deposited film thickness
⇒ can be scaled to sub 30 nm

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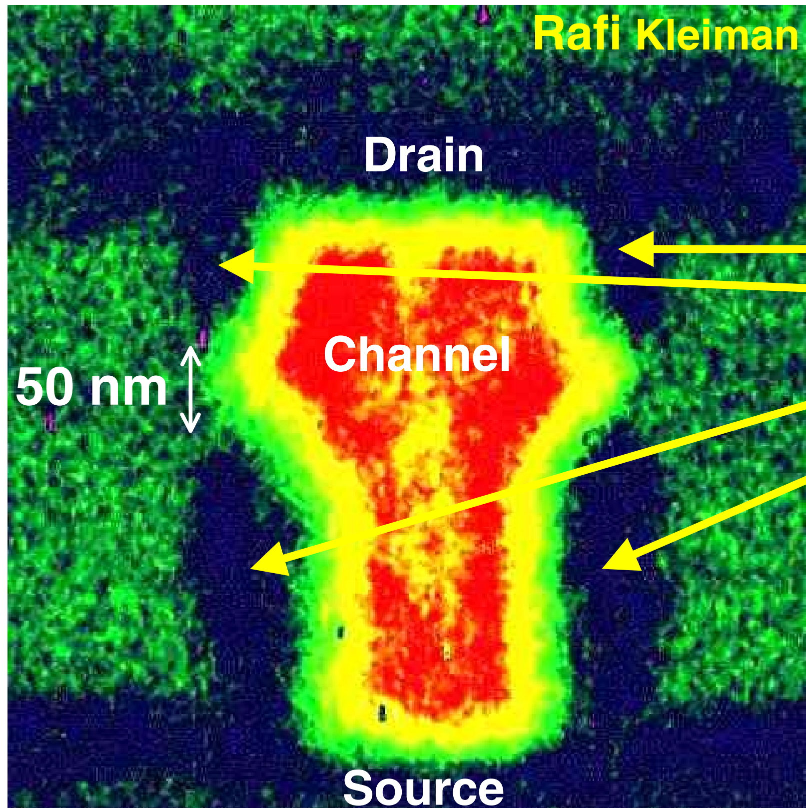
Scanning Capacitance Image



Solid source diffusion provides **self-aligned** source/drain extensions

L_G = 50 nm

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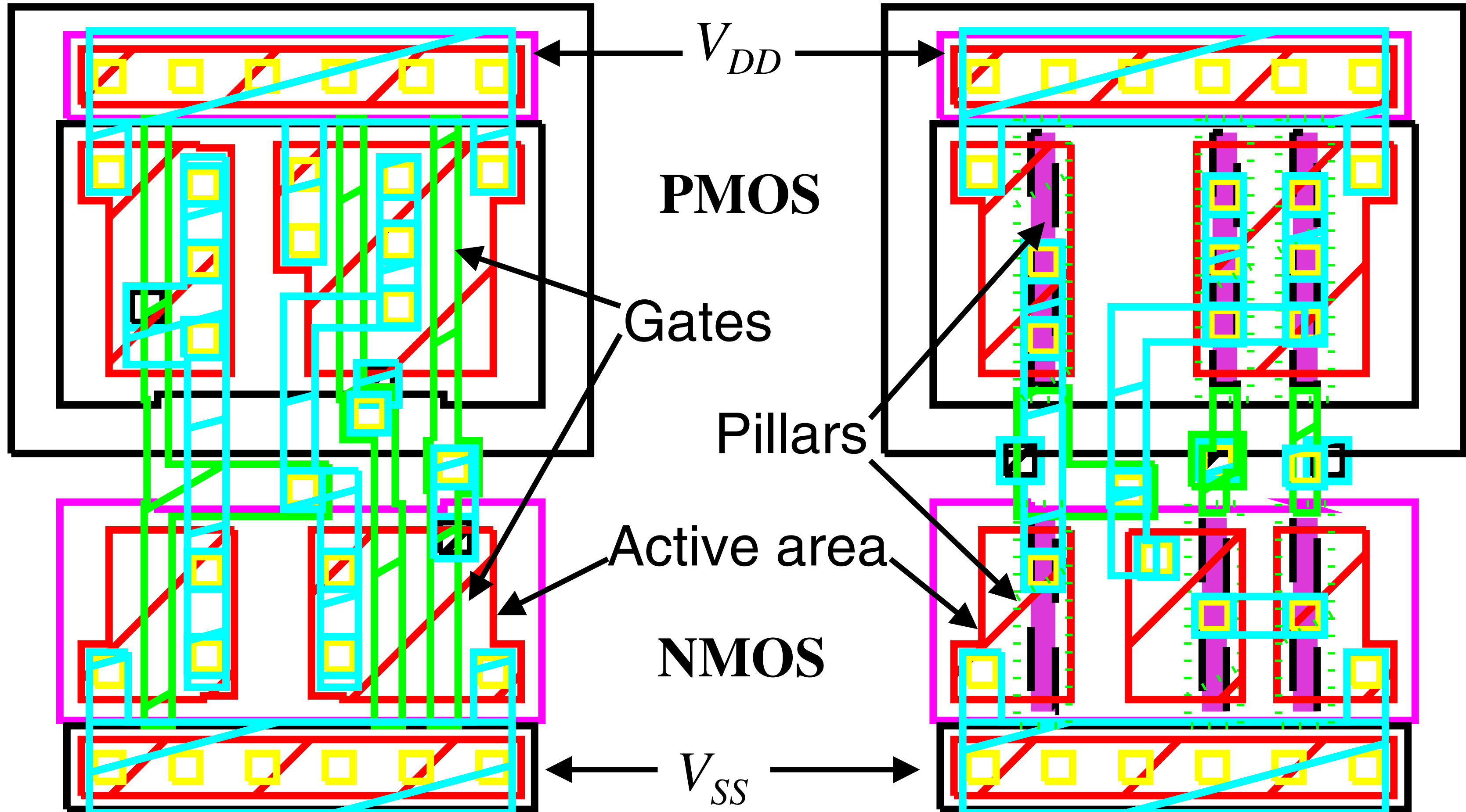
2-Input AND Comparison



Planar Layout (from 0.25µm ASIC Library)

Same Density
Double Effective Width

VRG Layout (using similar 0.25µm rules)

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Layout Density and Drive Metrics

- **Traditional Transistor Current Drive:** A/μm
  - **Useful for comparing planar transistors**
  - **Simple speed proxy if interconnect loaded**
- **VRG has (roughly) twice the width per area**
  - **Same *coded* gate width**
  - **Two sides per pillar**

Need a ***new drive current metric***

$$A/\mu m \Rightarrow A/\mu m^2$$

VRG could be *twice as good* as planar
(currently ~20-40% better)

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Can Extra Width Be Traded for T_{ox}?

- **Extra width gives more drive, but also more loading**
  - ALSO true of T_{ox} scaling! (not all circuits benefit!)
- **T_{ox} scaling needed for short devices**
  - BUT don't need to worry about length variations
- **T_{ox} scaling has driven oxide fields very high**
  - Leakage, reliability issues
  - Carrier velocity is degraded at high normal fields
- **Electrical thickness of inversion layer limimits effectiveness of T_{ox} scaling**

Some relaxation of oxide scaling should be possible!

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Special VRG Metrology Needs

- **Gate Oxide**
  - The usual replacement-gate challenges
  - No blanket film area- sidewall is vertical
  - Stress in stack may change growth
- **Dopant distribution**
  - No planar structure for SIMS profiling
  - Solid-source diffusion may be sensitive to interlayers
  - The usual problem: interstitial distribution
    - » Only indirect, post-mortem measurements
    - » Critical for all shallow doping extensions

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Summary

- Gate oxide scaling
  - Daunting challenges
  - Diminishing returns
- Alternative gate dielectrics
  - Similar diminishing returns
  - Many materials unknowns
  - New processes possible
- Vertical, Replacement-Gate MOSFET
  - Huge risks due to process and layout changes
  - No immediate materials changes
  - Provides an alternative to traditional oxide scaling
  - Non-lithographic gate-length control

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