2000 International Conference on Characterization and Metrology for ULSI Technology

NIST

The Coming & Ongoing Changes in IC Interconnect Fabrication

&

What This Has to do With Metrology

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(06/27/00)

SEMATECH • INTERNATIONAL SEMATECH

OUTLINE

Why Are We Changing

What is Changing

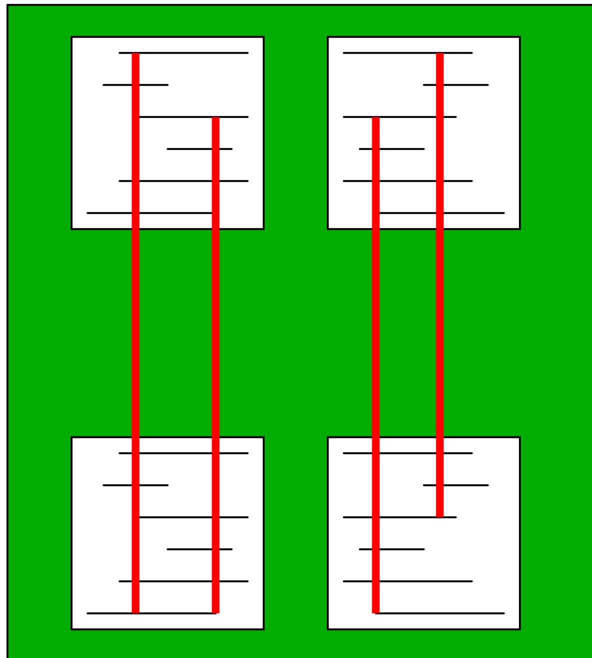
Problems Encountered

Brief Discussion on Some ‘Counter’ Forces (Money Basically)

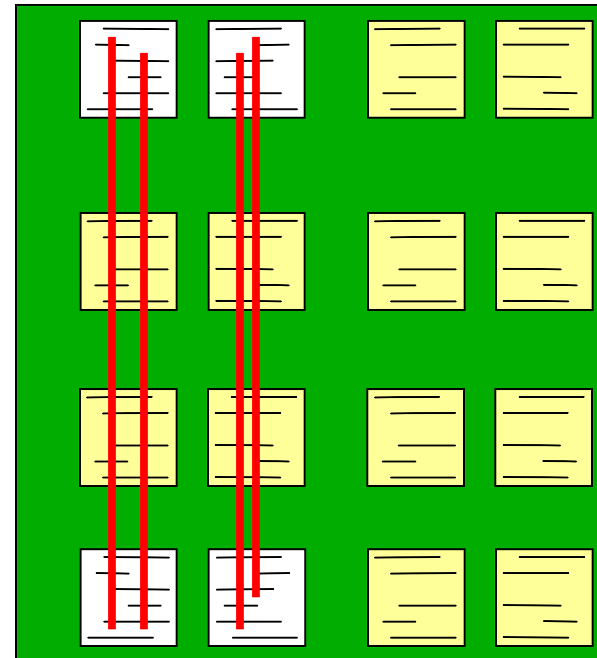
Where We Are Now

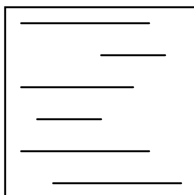
Global Wires Can't Be Scaled In Length

A Chip



A More Advanced Chip





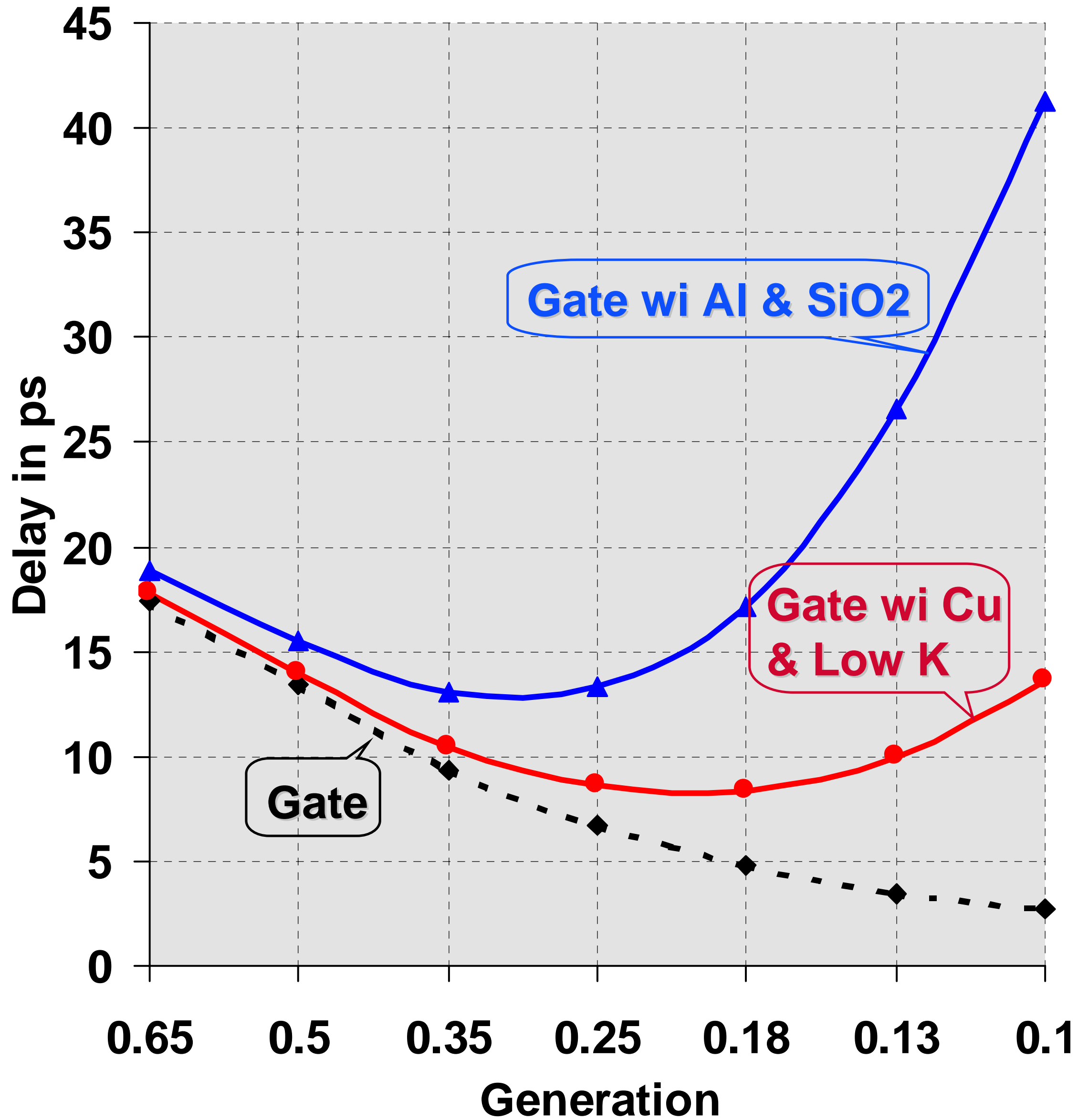
Module on a chip

Local wire in a module

Global wire between modules

SPEED / PERFORMANCE ISSUE

The Technical Problem



- ◆ - Gate Delay

Sum of Delays, Al & SiO2

Sum of Delays, Cu & Low K

Interconnect will dominate timing delay.

Cu/Low-k buys 1-2 generations.

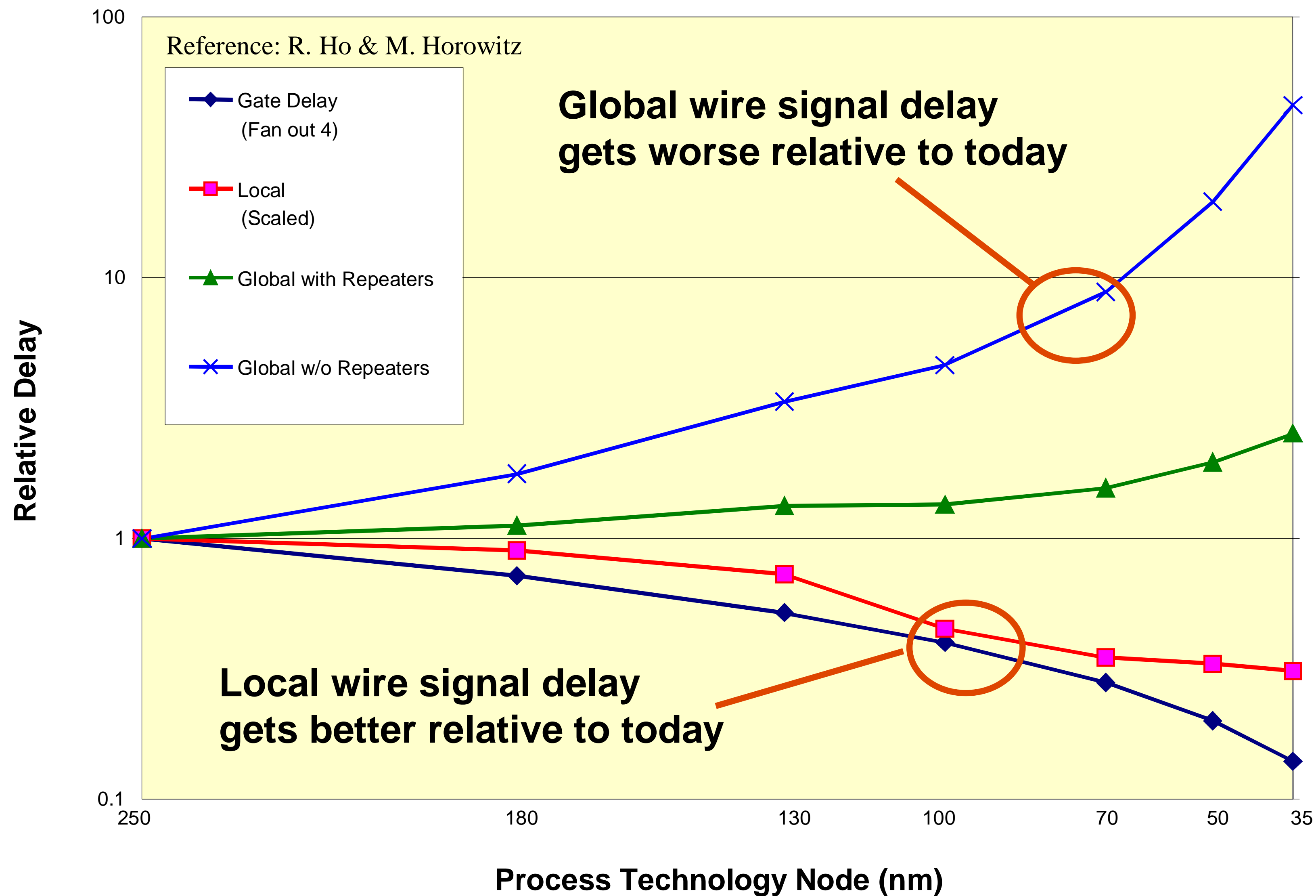
Al	*3.0 uΩ-cm*
Cu	*1.7 uΩ-cm*
SiO2,	*K=4.0*
Low K	*K=2.0*
Al & Cu	*.8u Thick*
Al & Cu Line	*436u Long*

Data From: Bohr, Mark T; "Interconnect Scaling - The Real Limiter to High Performance ULSI"; Proceedings of the 1995, IEEE International Electron Devices Meeting; pp241-242

KA Monnig 09/02/96

INTERNATIONAL SEMATECH • SEMATECH

Interconnect Delay vs. Design Rule



INTERNATIONAL SEMATECH • SEMATECH

1999 *Condensed* ITRS

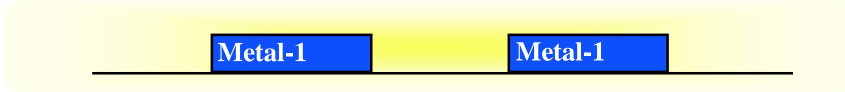
Year of First Product Shipment Technology Generation	1999 180nm	2002 130nm	2005 100nm	2008 70nm	2011 50nm	2014 35nm
Number of metal levels—DRAM	3	3–4	4	4	4	4
Number of metal levels—logic	6–7	7–8	8–9	9	9–10	10
Jmax (A/cm^2)-wire (at 105°C)	5.8E5	9.6E5	1.4E6	2.1E6	3.7E6	4.6E6
Local wiring pitch—DRAM (nm) non-contacted	360	260	200	140	100	70
Local wiring pitch—logic (nm)	450	325	230	165	120	85
Local wiring AR—logic (Cu)	1.4	1.5	1.7	1.9	2.1	2.2-2.3
Cu local wiring dishing (nm)	18	14	11	9	7	5
Intermediate wiring pitch—logic (nm)	560	405	285	210	145	110
Intrmdt wiring h/w AR-logic (Cu DD via/line)	2.0/2.1	2.2/2.1	2.4/2.2	2.5/2.3	2.7/2.4	2.9/2.5
Cu intrmdt wiring dishing (nm) 15µ wide wire	64	51	41	30	22	17
Dielctrc erosion (nm), intrmdt wrng 50% dnsty	64	51	41	0	0	0
Global wiring pitch—logic (nm)	900	650	460	330	240	170
Global wiring h/w AR-logic (Cu DD via/line)	2.2/2.4	2.5/2.7	2.7/2.8	2.8/2.9	2.9/3.0	3.0/3.1
Cu global wiring dishing (nm) 15µ wide wire	116	95	76	55	38	29
Contact aspect ratio-DRAM, stacked cap	9.3	11.4	13	14.1	16.1	23.1
Conductor effective resistivity (µΩ-cm) Cu *	2.2	2.2	2.2	1.8	<1.8	<1.8
Barrier/cladding thickness (nm)***	17	13	10	0	0	0
Interlevel metal insulator effective dielectric constant (k) logic	4.0-3.5	3.5-2.7	2.2-1.6	1.5	<1.5	<1.5
Interlevel metal insulator effective dielectric constant (k) DRAM	4.1	4.1-3.0	3.0-2.5	3.0-2.5	2.5-2.0	2.3-2.0

* Assumes a conformal barrier/nucleation layer
*** Calculated for a conformal layer in local wiring to meet effective conductor resistivity

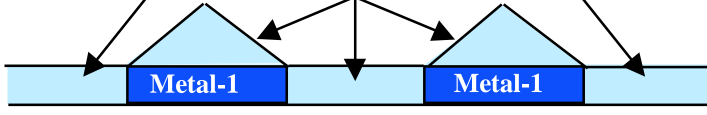
Process and Material Solutions Can't Meet Needs

INTERCONNECT PROCESS FLOWS

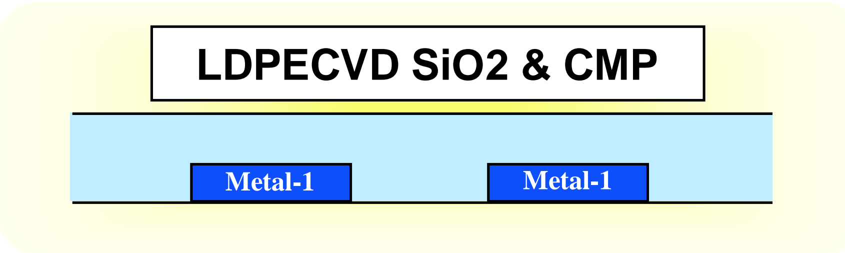
Traditional Flow VS *Dual Damascene*



GAPFILL HDPECVD SiO2

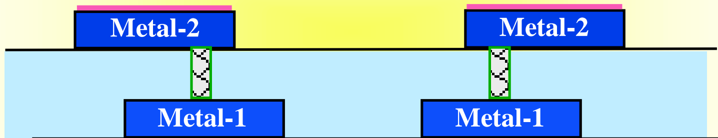


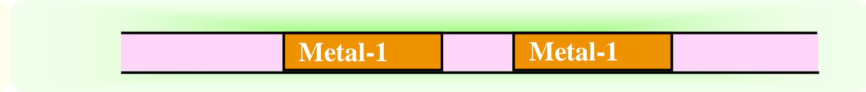
LDPECVD SiO2 & CMP



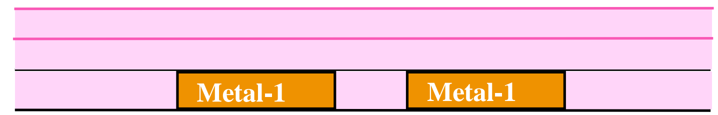
Dry Etch Via, PVD Barrier, CVD W

PVD Ti/Al-Cu/TiN, Dry Etch Metal

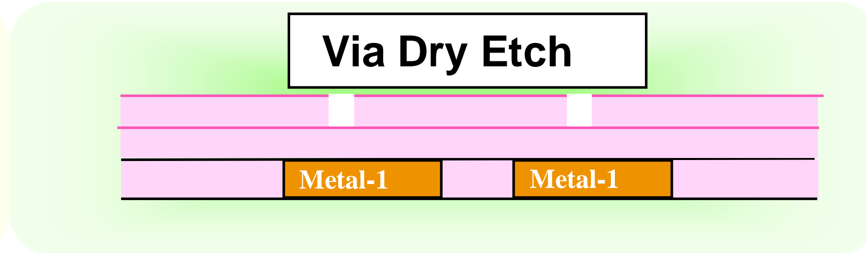




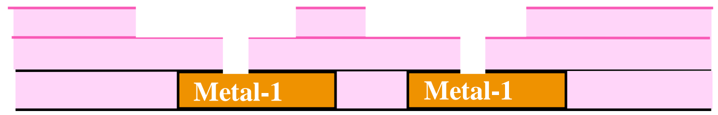
Deposit Planar Dielectrics



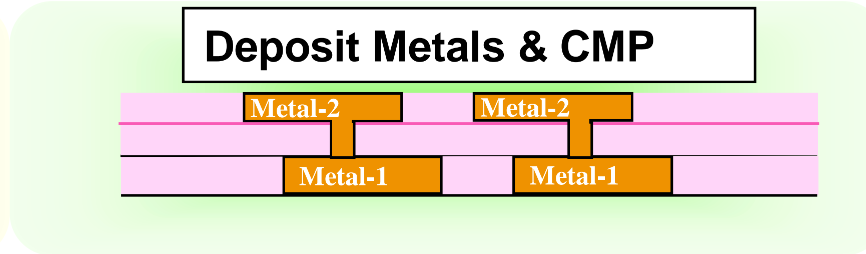
Via Dry Etch

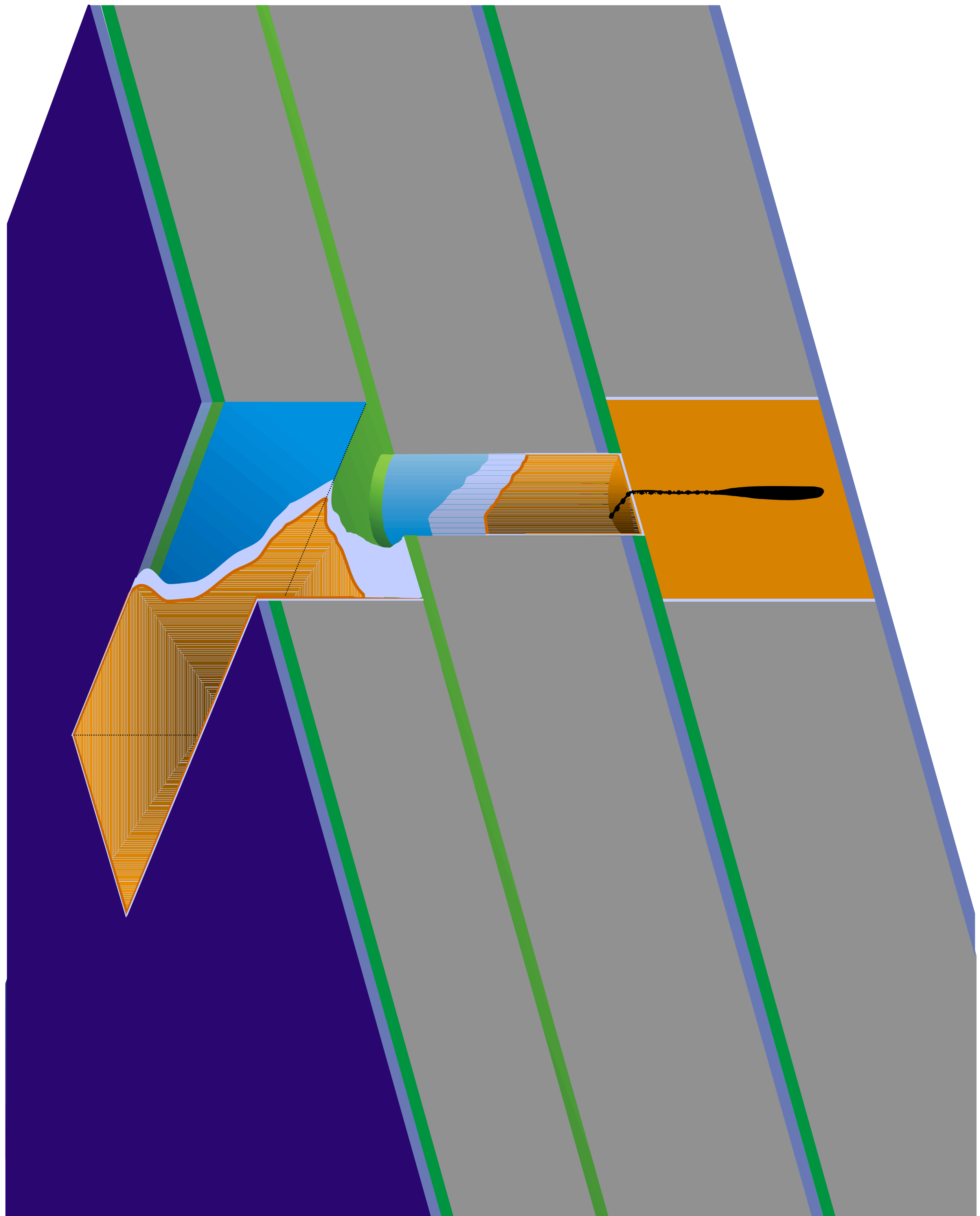


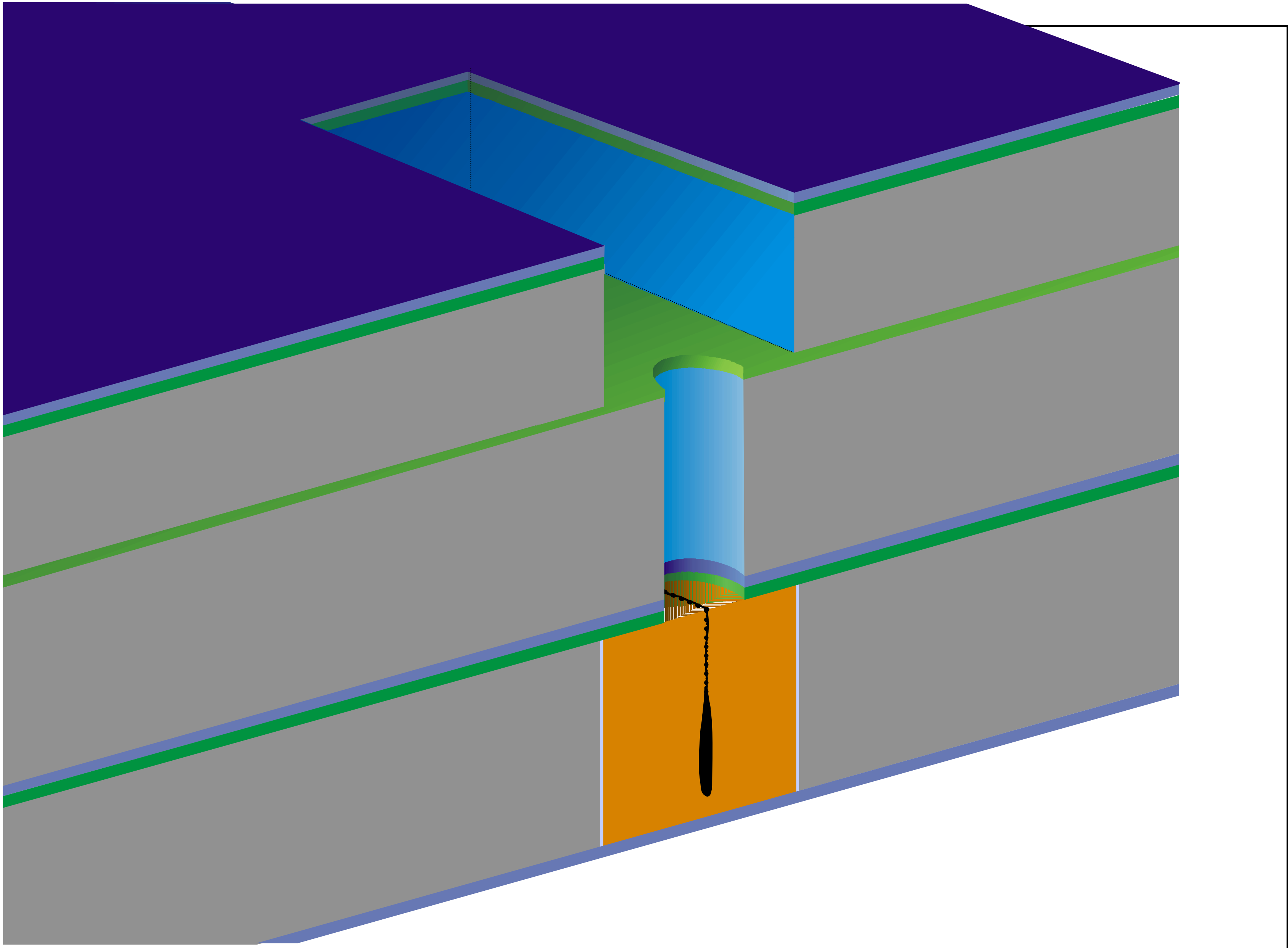
Line Dry Etch (Canals)



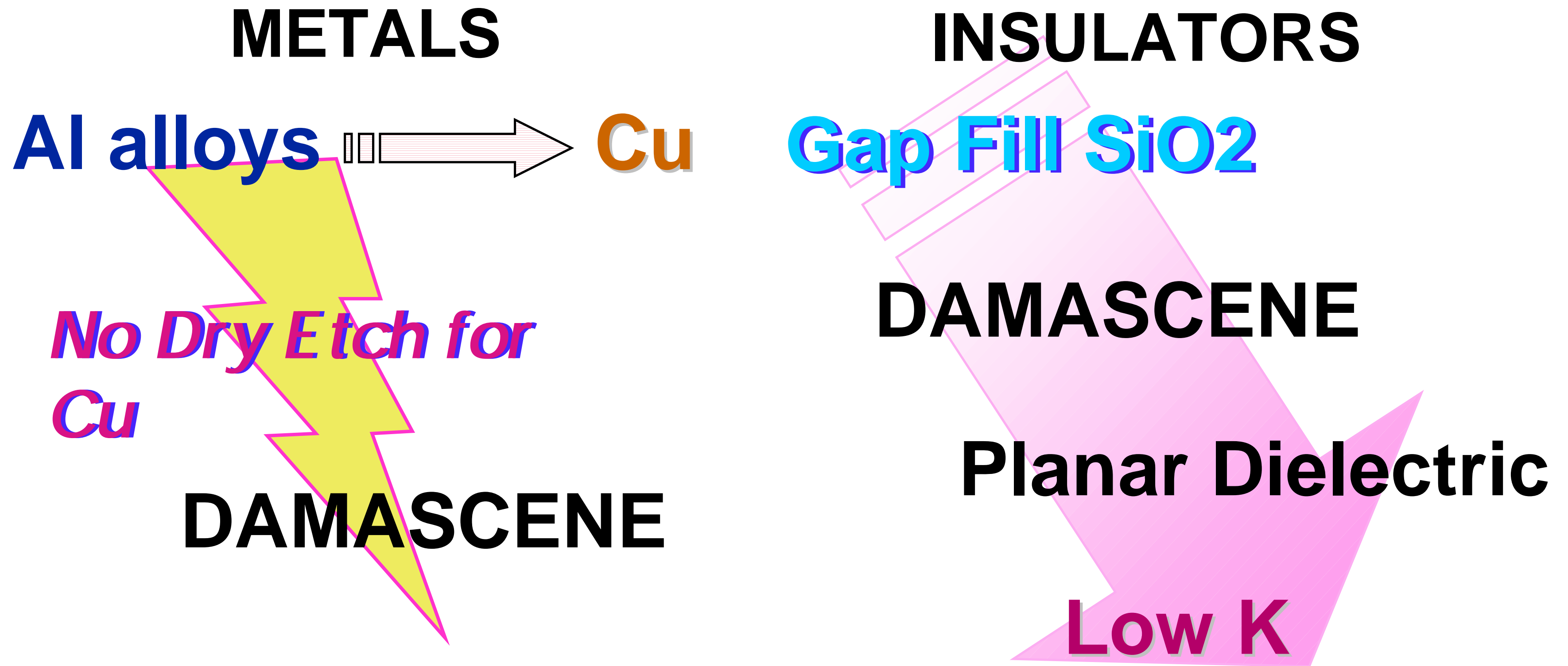
Deposit Metals & CMP







THE PROCESS FLOW CHANGES RESULT FROM MATERIAL CHANGES



The Material Changes are Catalyzed by 'New' IC Performance Needs

WHERE HIGH PERFORMANCE INTERCONNECTS ARE HEADING

“FAT” Metal

~.18*u*

The “DEVICE”

COLOR CODE

Copper on “Seed” on Barrier

Low K Dielectric

Etch Stops Polish Stops

W Plug in BPSG

Drawing to Scale Within ~10%

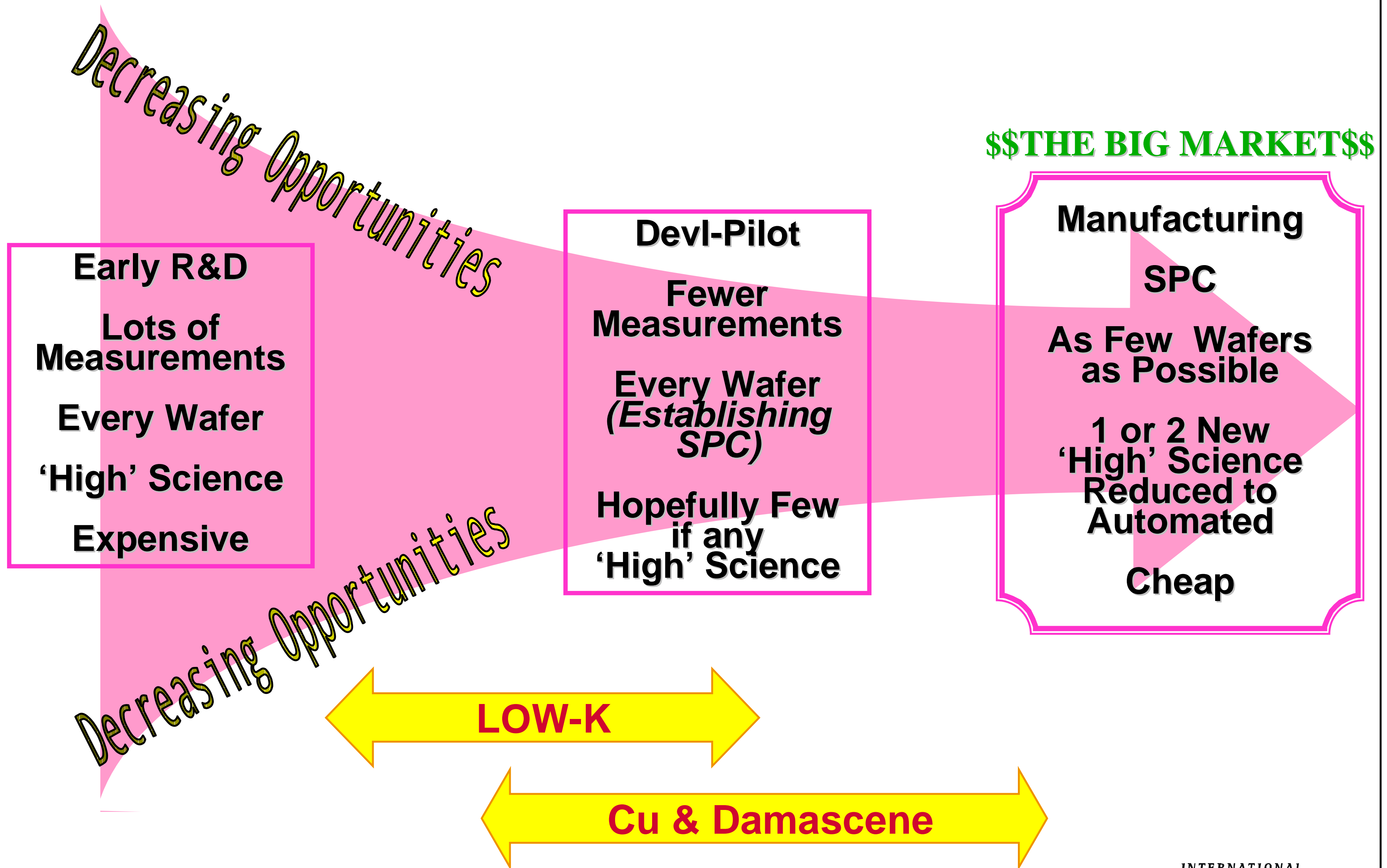
IMPACT OF CU, LOW-K, DAMASCENE ON CAPITAL EQT AND MATERIALS SUPPLIERS

- **All of the Interconnect Materials Are Being Changed**
- **Many of the Process Techniques Are Being Changed, Therefore Most of the Equipment Set Is Impacted**

BUT There Are Market and Financial Forces Against All of This Change

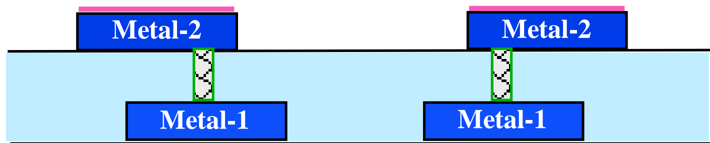
- **Interconnects Comprise 1/2 the Cost of Building an IC, There Is a Large Investment in Money, Knowledge and Experience by Both the Customers and Suppliers in the Current Equipment and Methods**
- **Suppliers of the Current Interconnect Equipment Set Are Among the Biggest and Most Successful**

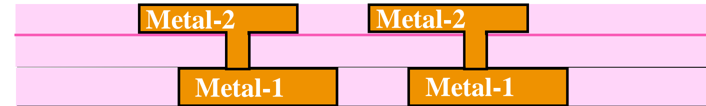
A WORD ABOUT METROLOGY



INTERCONNECT TOOL CHANGES; *Metal*

Traditional Flow VS ***Dual Damascene***





- PVD Ti Based Barrier wi PVD Al/Cu Line
- PVD TiN Barrier CVD-W Via Plug

- PVD TaN wi PVD Cu 'Seed' ElectroPlated Cu
- Via Plug and Line Metal merged into 1 operation

Projected Toward

CVD Barrier and/or CVD Cu Seed, maybe CVD Cu Fill

Precursors Likely to be Organo- Metallics wi maybe Fl, Cl, Br, I

TECHNOLOGY IMPACTS ON TOOL MARKET

TOOL/TECHNOLOGY	PLAYERS
PVD ($890M, 1998) * ($1.24B, 1999)**	AMAT / Anlv / Nvls TEL / ULVAC

TRENDs: Down

- PVD 'Slab Al" Supplanted by Cu Plate &/or CVD (ECD; 1998@ $61M, 1999@ $76M)**
- W Plug CVD Supplanted by Cu Plate &/or CVD
- PVD TiN Supplanted by PVD Cu, Ta-TaN then by CVD
- PVD Barrier and Seed wi Cu Plate will continue at upper-coarser levels

* "Semiconductor Equipment, Manufacturing, and Materials Worldwide"; Dataquest; June, 7, 1999

** "Semiconductor Equipment, Manufacturing, and Materials Worldwide"; Dataquest; June, 26, 2000

TECHNOLOGY IMPACTS ON TOOL MARKET

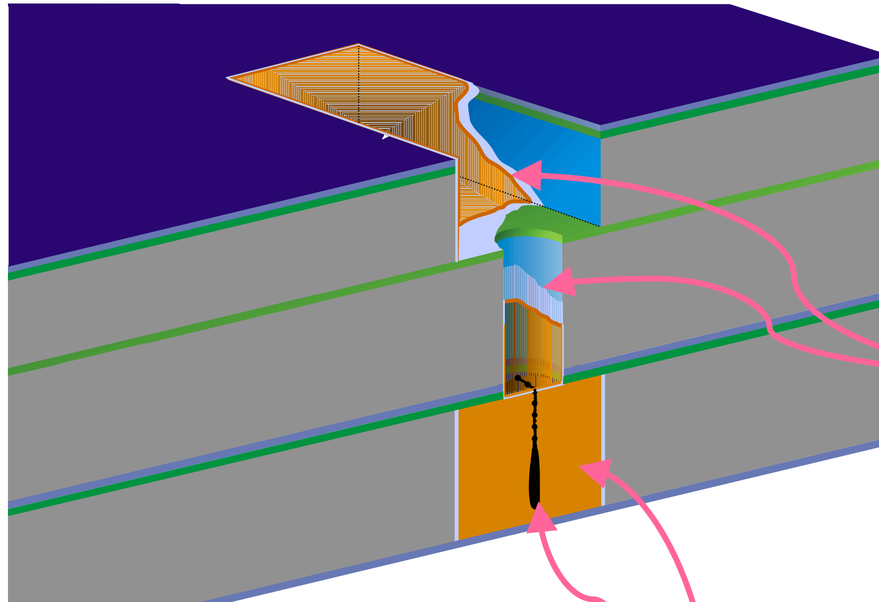
TOOL/TECHNOLOGY	PLAYERS
CVD ($??M, 1998) Metals	AMAT / Nvls / TEL

TRENDs: What People Think They Want

- CVD Barriers

- CVD Cu Seed

Metal Deposition



Want to Measure;
Thin Things on the Sidewalls of Deep Things

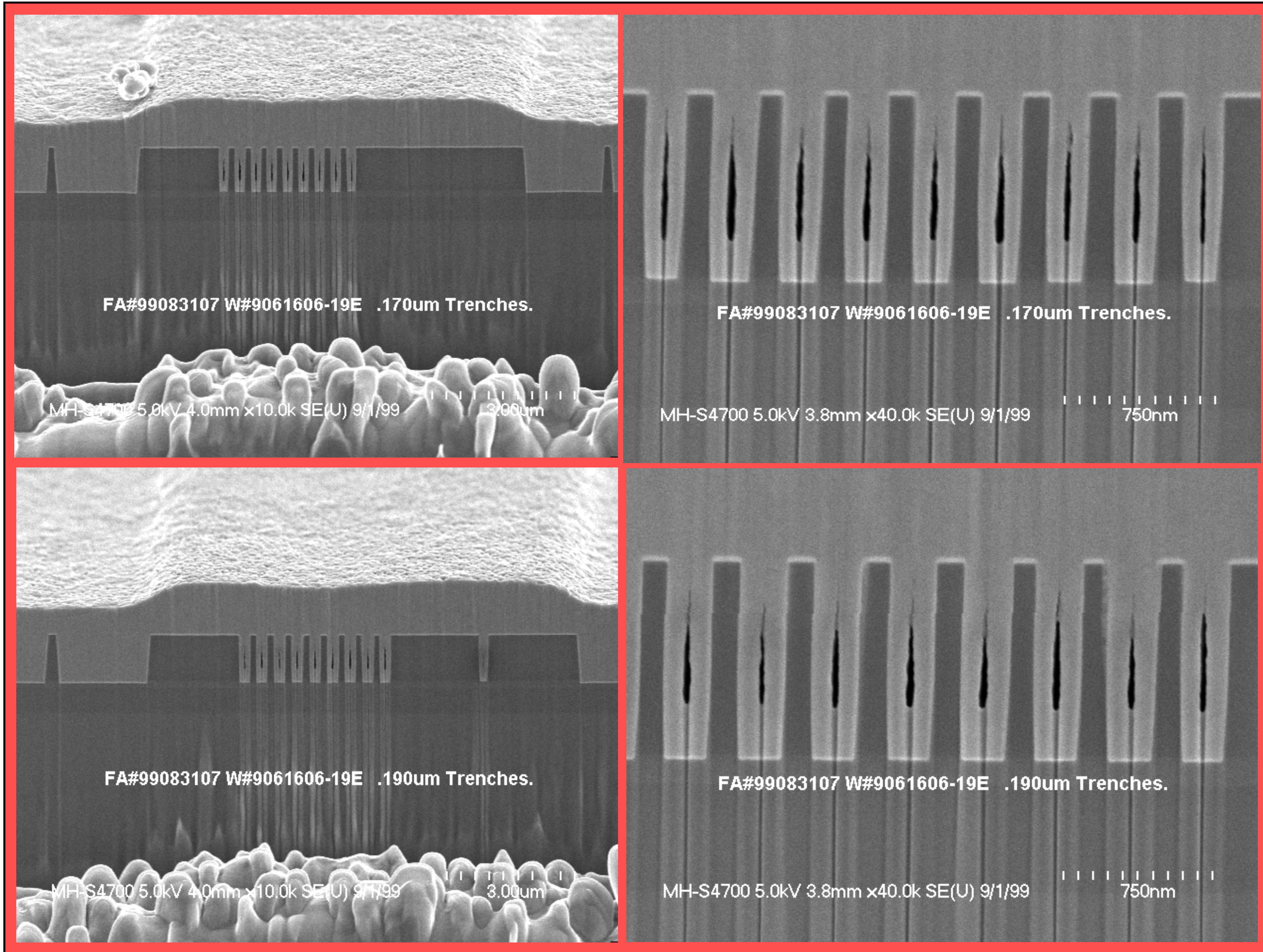
Barrier and Seed;
- Thickness (in detail)
- Resistivity
- Morphology
- Composition

Want to Measure;
Metal Properties in the "Canal"

Line;
- Resistivity
- Orientation
- Voids
- Composition

We now measure;
- Surface film properties
- Cross section
- Electrical Result

Depletion Study: 4378 Amp-min, after 750 ml Bleed/Feed



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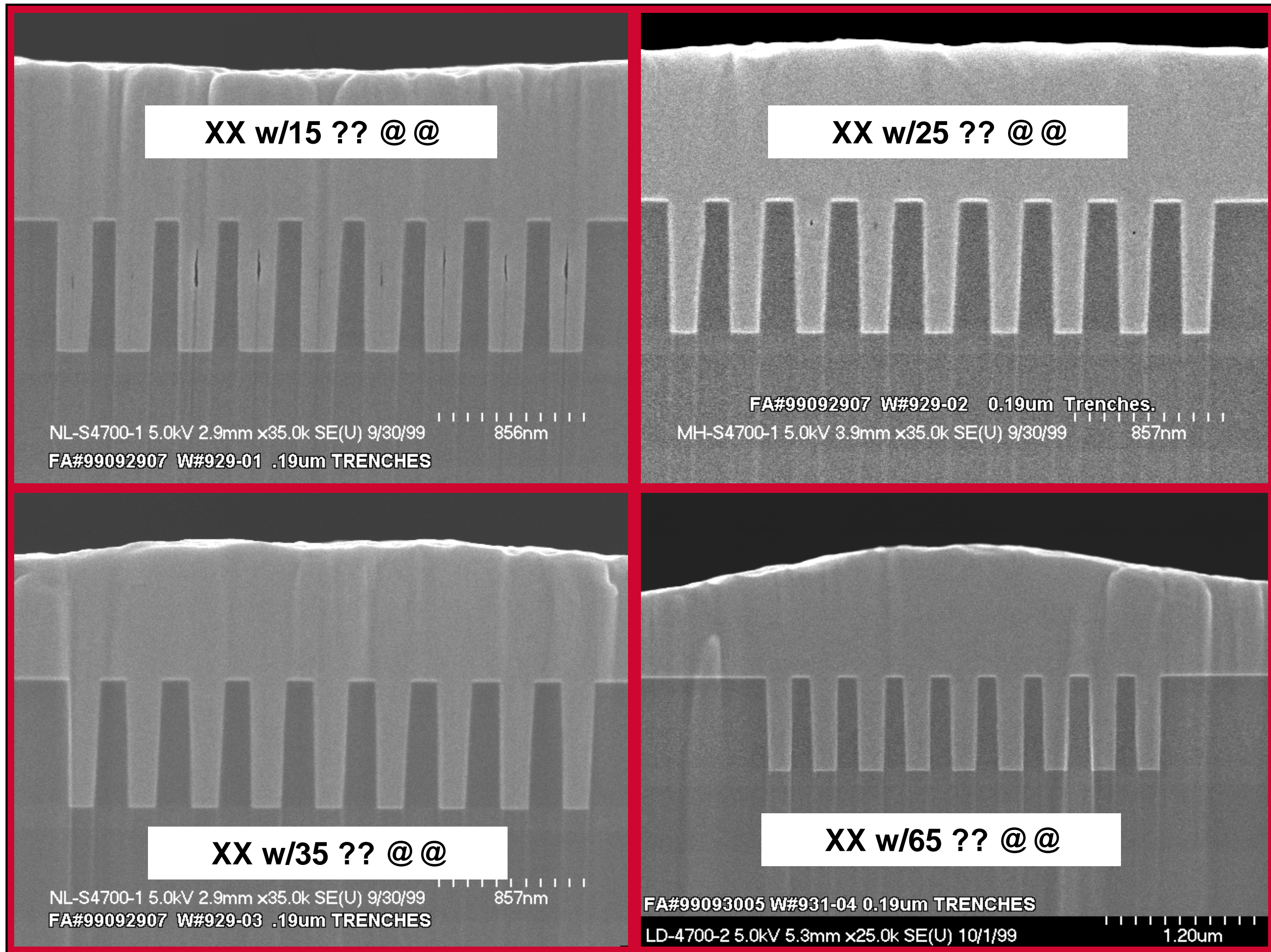
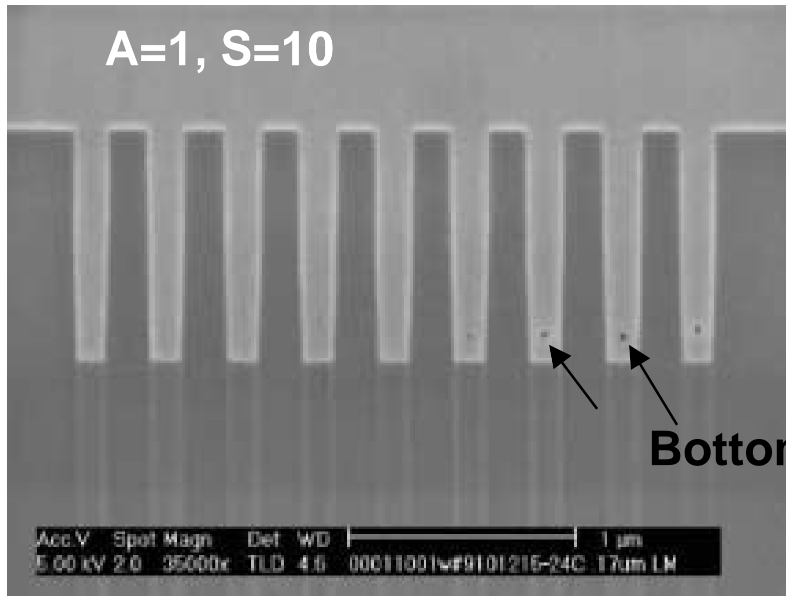
Effects of @@ Levels on Fill

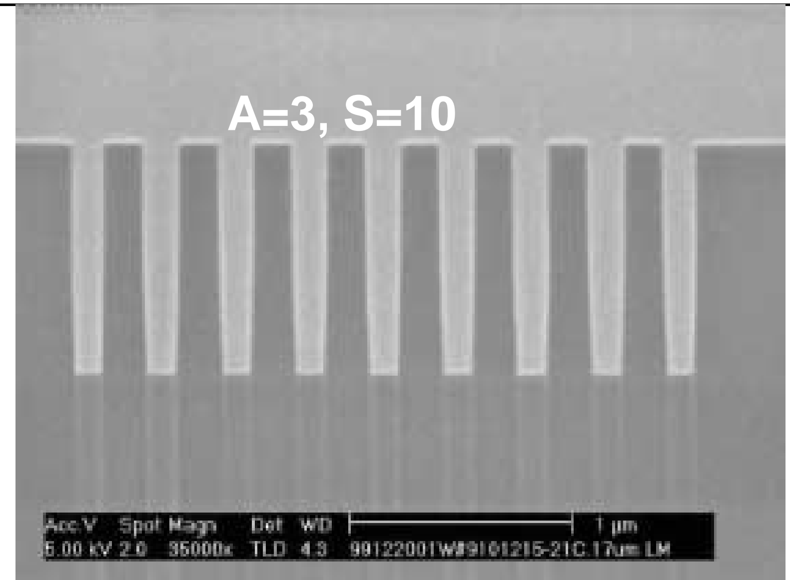


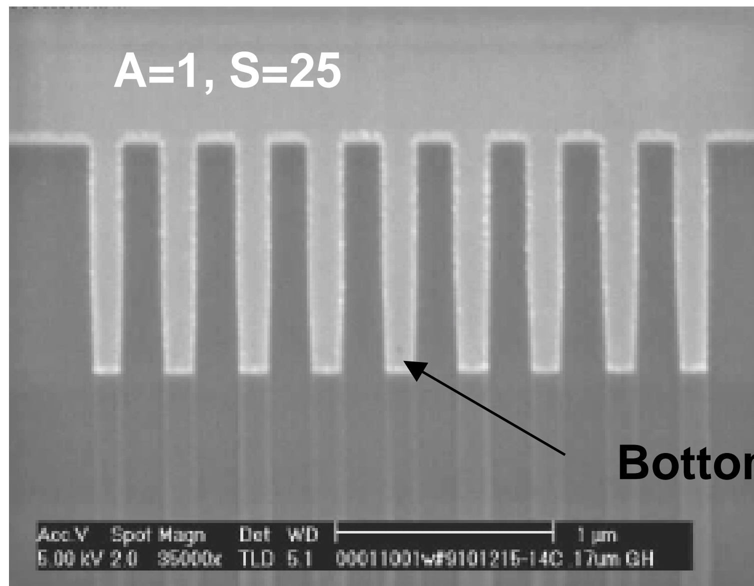
Bob Mikkola

Additive Experiment (25 ?? @@)

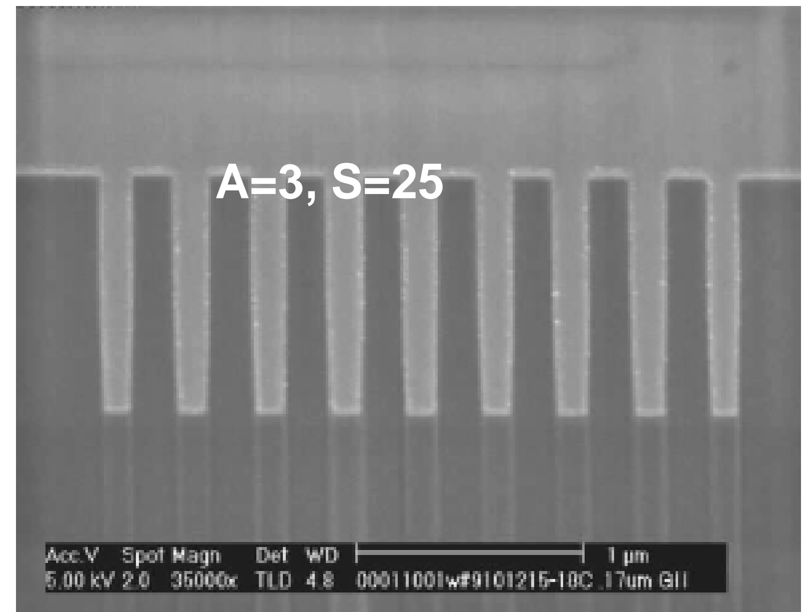


Bottom Voids

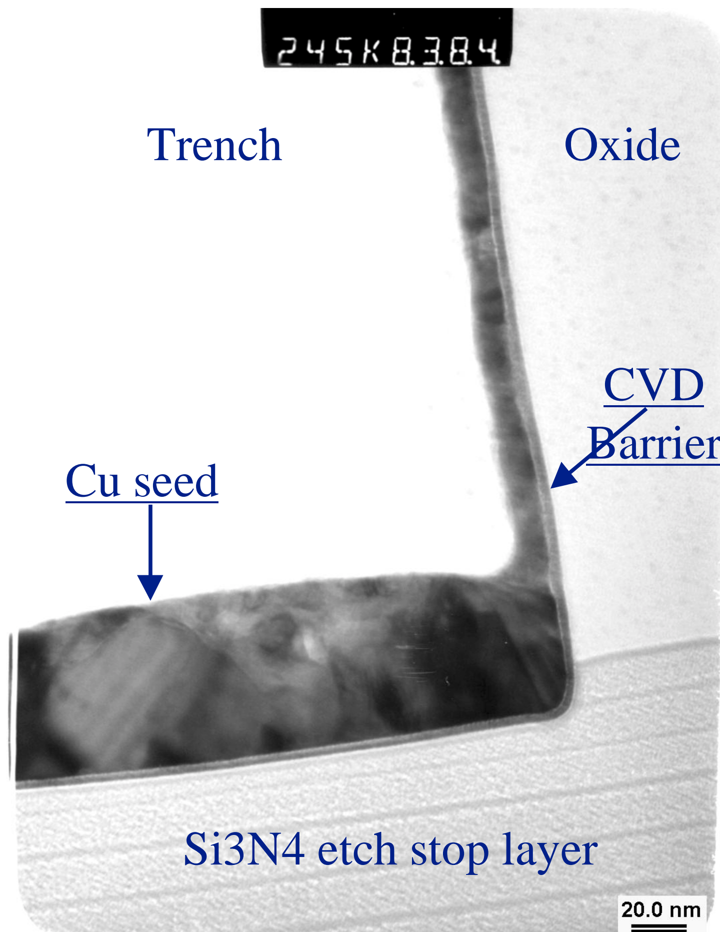




Bottom Voids



TEM Image Of CVD CVD Barrier
(100Å CVD Barrier + 1000Å 'Enhanced PVD' Cu seed)

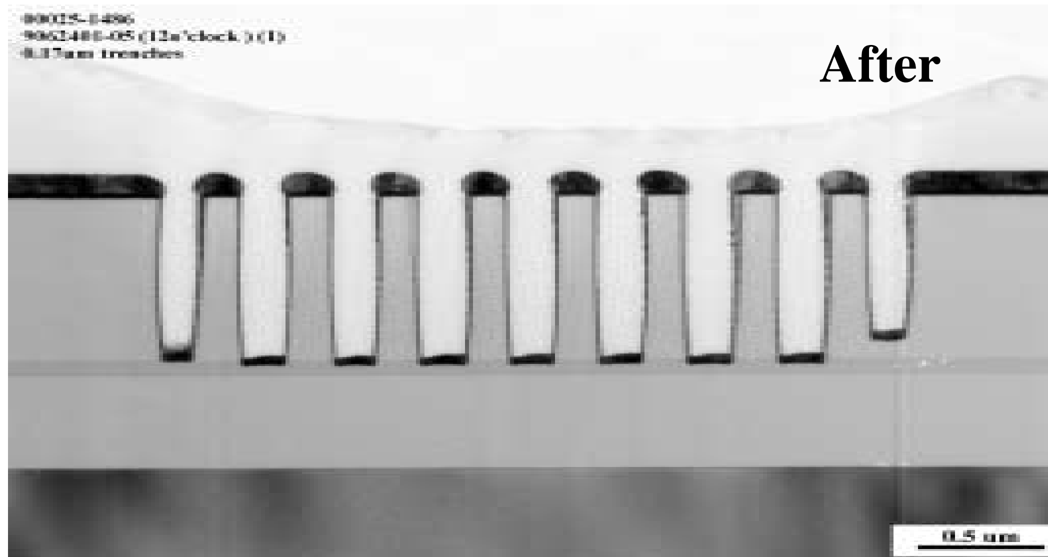


0.25µm AR ~ 3.0:1 Right edge

- Image shows good conformality of barrier (step coverage is ~69.4% on sidewall & 59.2% at bottom).
- Cu seed should be sufficient for plating (step coverage is ~ 11.0% on sidewall & 55.9% at bottom).
- Issues with sample prep at SEMATECH and Accurel.

Comparison stepcoverage “Before” & “After”

0.2 um
AR 5



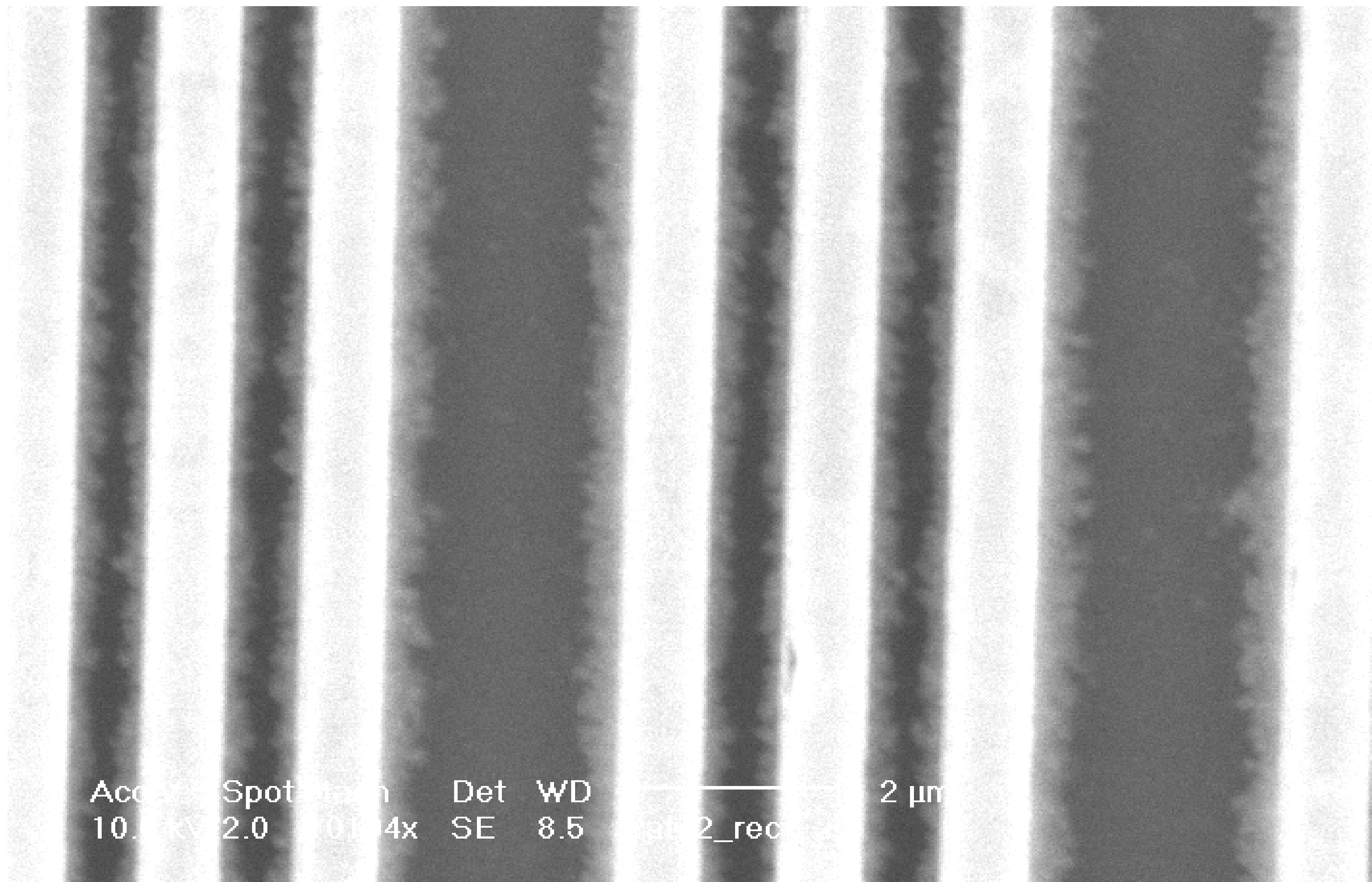
0.2 um
AR 4

8102662-08 Edge

Asymmetry after is less then before

Cu Diffusion

Cu diffuses into Low K through sidewall



Metrology Things We Can't Do

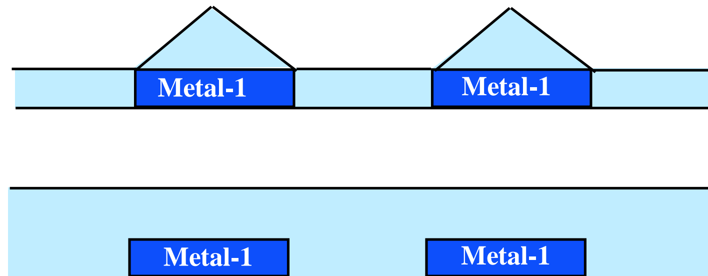
Metal Deposition

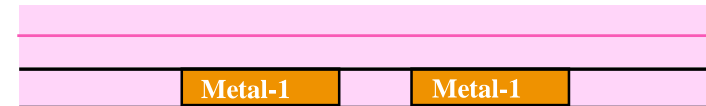
- Barrierness
- Reliability

Have to Build a Complete Device and Life Test

INTERCONNECT TOOL CHANGES; *Dielectrics*

Traditional Flow vs *Dual Damascene*





High Density Plasma CVD SiO2 wi strong 'resputter' component for Gap Fill

Capped with Low Density PECVD SiO2

Planarized with CMP

Planar CVD SiO2, wi (usually PE)CVD Stop/Mask/Arc Layers Ideally CMP not Needed

Projected Toward

Low-K Dielectrics, Either CVD or Spin On, wi (usually PE)CVD Stop/Mask/Arc Layers Ideally CMP not Needed

<u>At Least 2 Cycles</u>

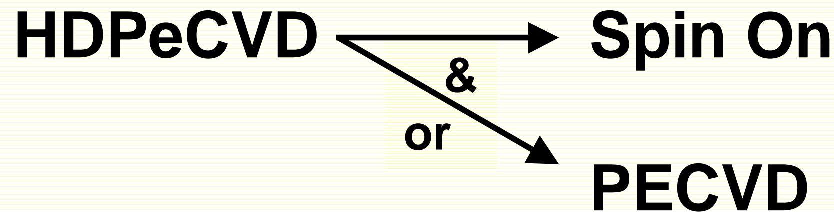
TECHNOLOGY IMPACTS ON TOOL MARKET

TOOL/TECHNOLOGY		PLAYERS
CVD	($886M, 1998)*	AMAT / ASM / Nvls
Dielectric	($1.34B, 1999)**	

TRENDs: 'Neutral' to Down but 'Easier'

•Reduced Need for High Density Plasma

•CVD Could be Supplanted in Whole or in Part by Spin on Technology (SOD; 1997@ $116M, 98@ $60M, 99@ $68M)**

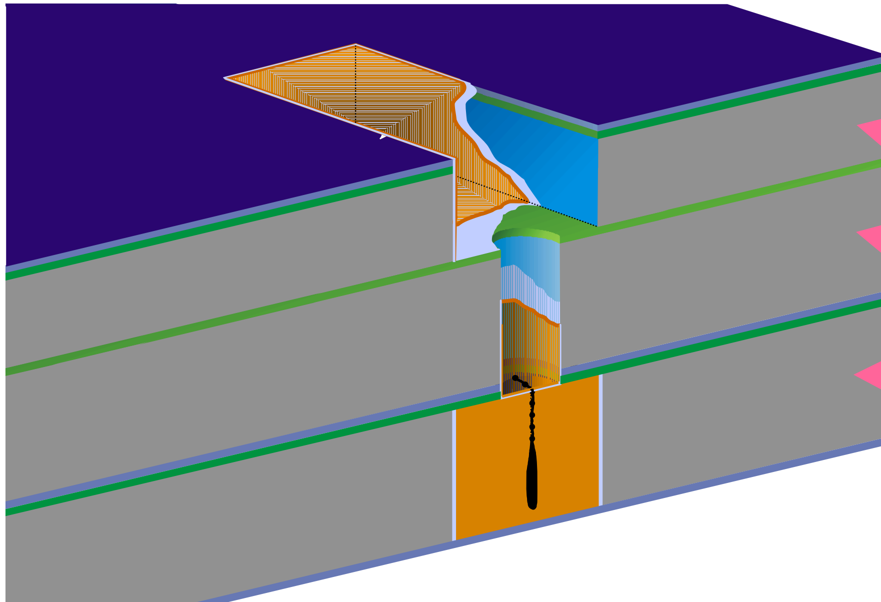


*"Semiconductor Equipment, Manufacturing, and Materials Worldwide"; Dataquest; June, 7, 1999

**"Semiconductor Equipment, Manufacturing, and Materials Worldwide"; Dataquest; June, 26, 2000

Metrology Needs

Dielectric Deposition



Now Measure;
A Whole Host of Things:

- Dielectric Constant
- CTE
- Modulus
- Adhesion
- Fracture Toughness
- Thermal "Stability"
- Moisture Uptake
- Morphology
- Composition
- etc. etc.

and as a Function of Time

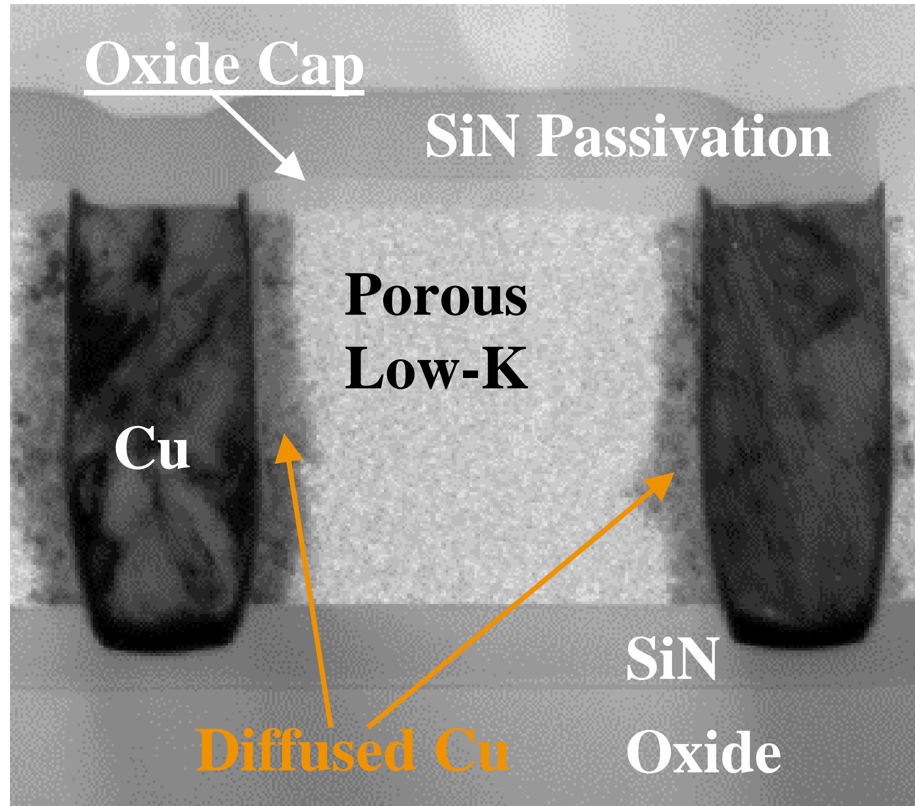
We Can Measure Some Things Pretty Well in Multiple Layers:

Planar Film:

- Thickness (Uniformity)
- Refractive Index

Don't Know How Many Will Be Carried into Production

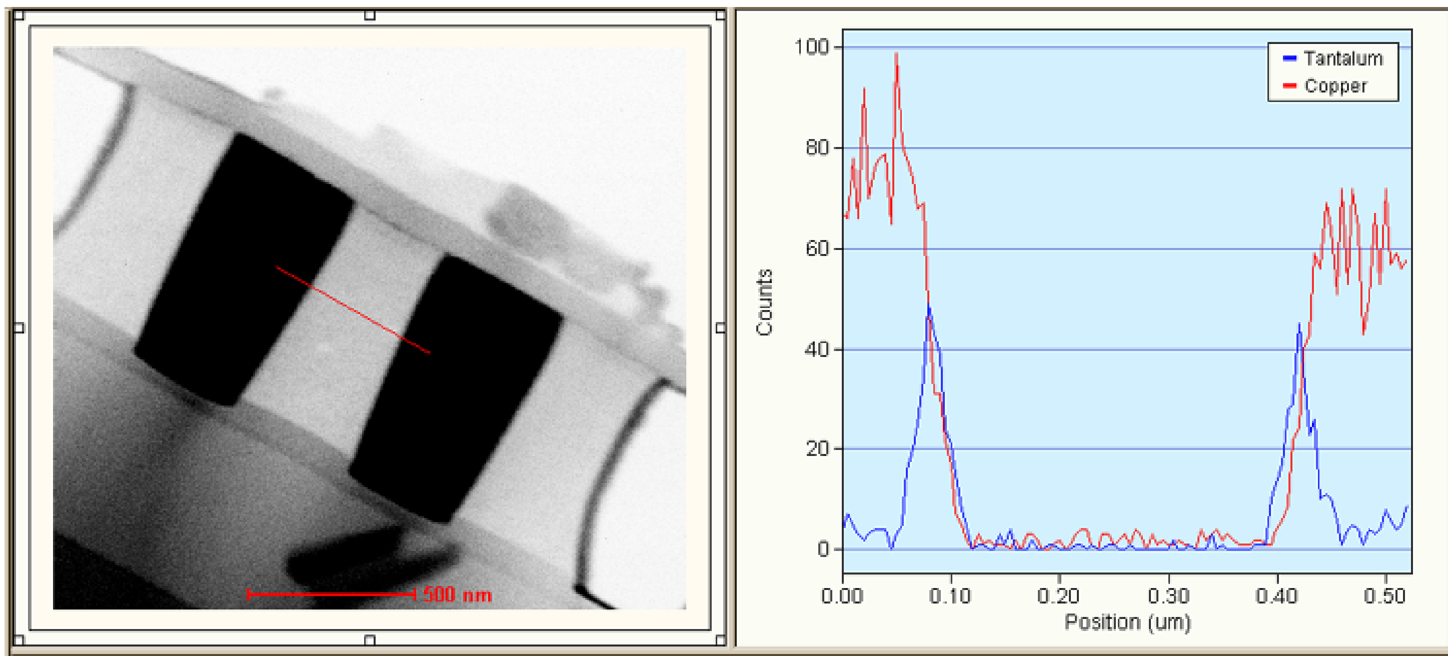
Thermal Annealing and Cu Diffusion



Bright-field TEM image of 0.35 μmL/0.40 μmS VHORG. Cu diffusion into the porous low-k was confirmed by EDX line profiles. The wafer was annealed 4 times at 400°C for 1 hour.

P 3: M1 Module Screening:

- **BF-STEM Image and EDS profile of Porous OSG**



– No Cu diffusion into low-k dielectric was detected.

Dielectric Deposition

Porosity

- Only Measure Open Cell
- Can't Measure Distribution

The Search for the "Killer Pore"

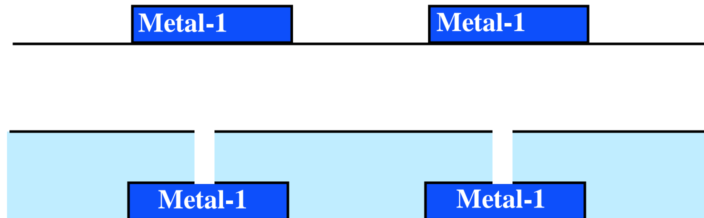
There are ~10^{13} Pores/die (and rising)

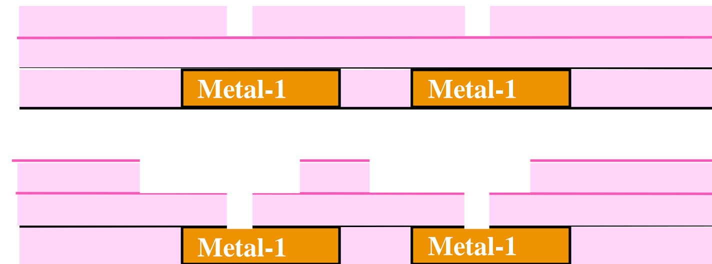
Adhesion

- A Generic Problem in Semiconductor Manufacturing
- More Problematic (now) For Dielectrics

INTERCONNECT TOOL CHANGES; *Etch & Strip*

Traditional Flow vs *Dual Damascene*





Metal Plasma Etch
- **Passivation (Dry and/or Wet)**
  - **Strip (Dry and/or Wet)**

Dielectric Plasma Etch
- **Strip (Dry and/or Wet)**

<u>No Cu Plasma Etch</u>
- **Metal CMP**

2 Dielectric Plasma Etchs
- **Tools Don't Change Much**
- **Selectivity Rqmnts Tougher**
- **Flourocarbons, O2, Ar, N2**

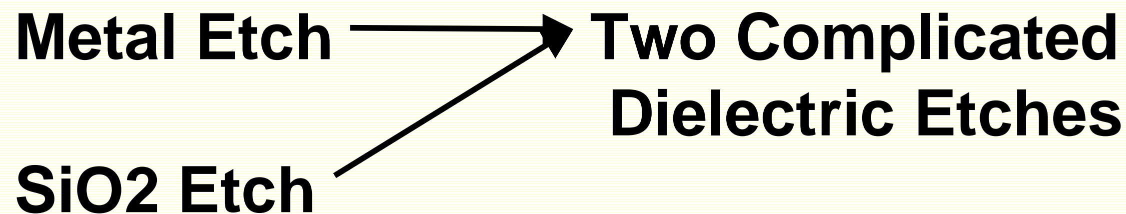
Strip (Dry and/or Wet)
- **Tough Chemistry Rqmnts**
- **May see Reducing Chemistry**

TECHNOLOGY IMPACTS TOOL ON MARKET

TOOL/TECHNOLOGY	PLAYERS
Dry Etch ($1.88B, 1998)*	AMAT / Hitachi
($2.4B, 1999)*	LAM / TEL

TRENDs: 'Neutral' to a 1st Approximation and 'Easier'

- **Metal Etch Eliminated *but***
- **Two <u>Complicated</u> Dielectric Etches per Metal Layer**
- **Still Medium to High Density Plasma**



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TECHNOLOGY IMPACTS ON TOOL MARKET

TOOL/TECHNOLOGY	PLAYERS
Dry Strip ($324M, 1997)*	Alcn / Gsnc / Etn
Strip ($162M, 1998)**	Mttsn / KEM
($227M, 1999)**	

TRENDs: "Insufficient Data Captain Kirk"

- Process (Particularly wi Low K) Not Yet Well Enough Defined

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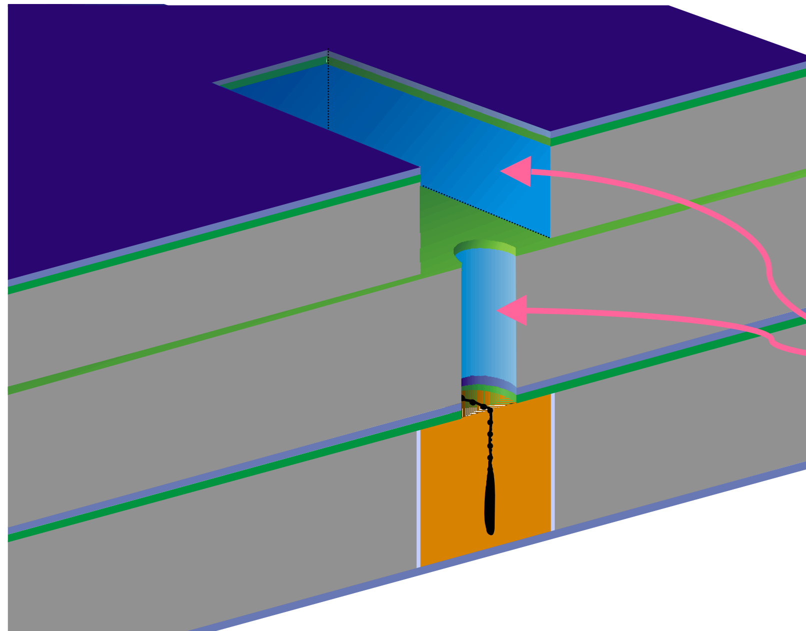
Etch & Strip



**Want to Measure;
Thin Things on the Sidewalls and Bottoms of Deep Things**

- Feature Size (in detail)
- Profile
- Residues
- Low-K 'Attack'
- Alignment
- "Depth"
- Faceting

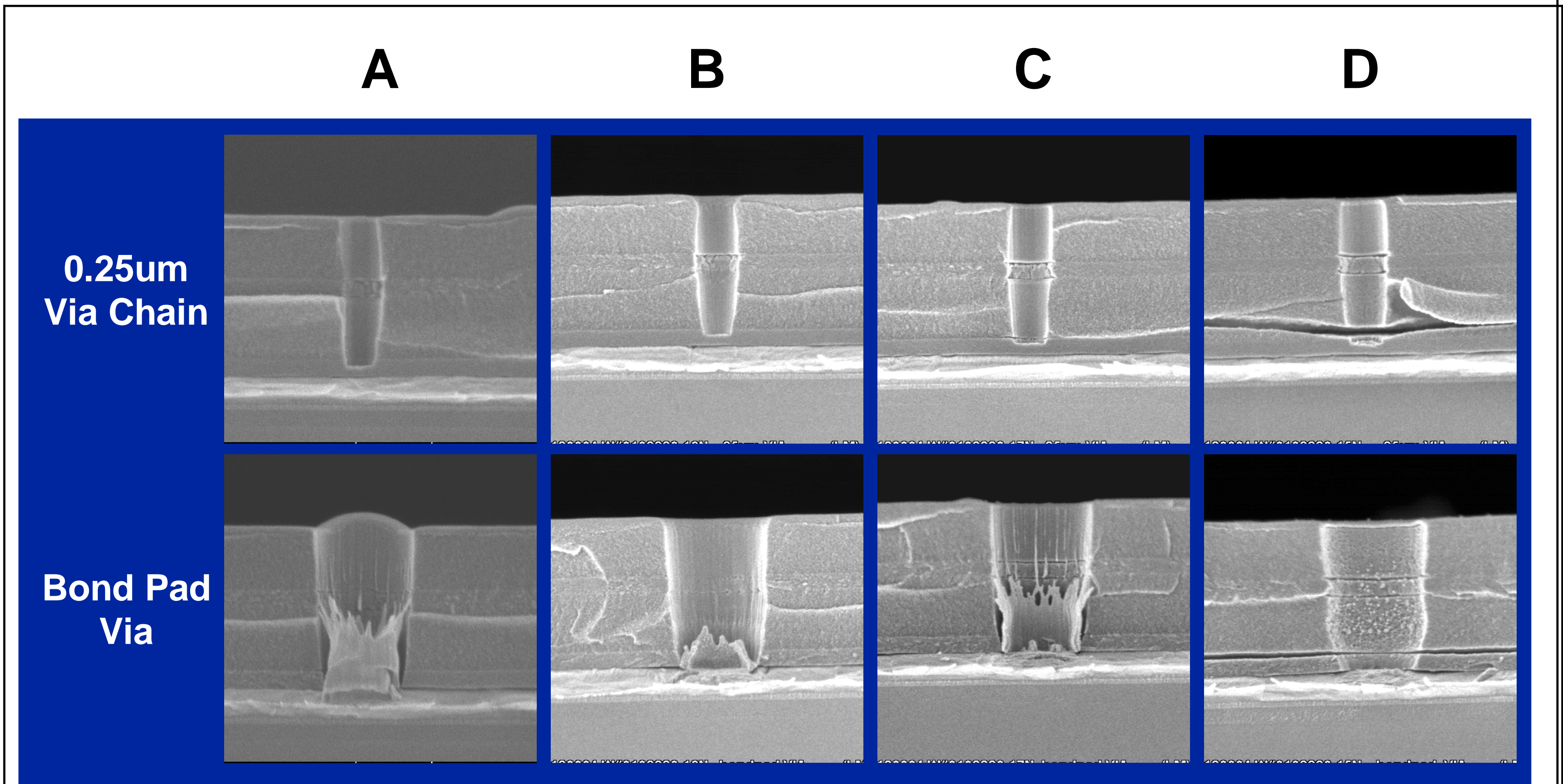
We now measure;

- Cross section
- Electrical Result

Etch Development is Paced by SEM/TEM Time

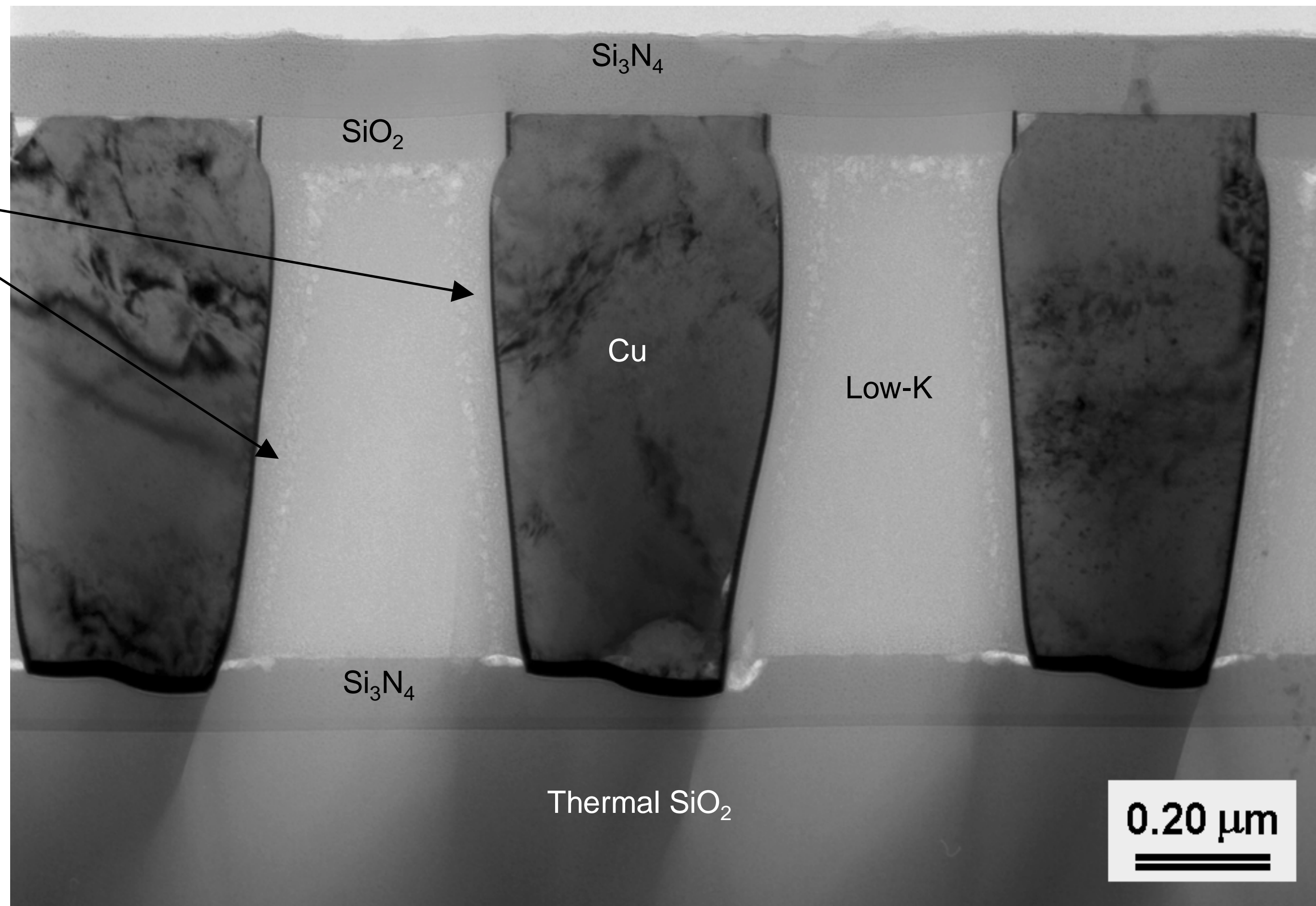
Ash of %%%% Dual Damascene Via

- **Exposed Cu presents an additional challenge for ash**



Low-K Damage

Note areas at sidewall with appearance of higher density (perhaps due to etch/ash damage).

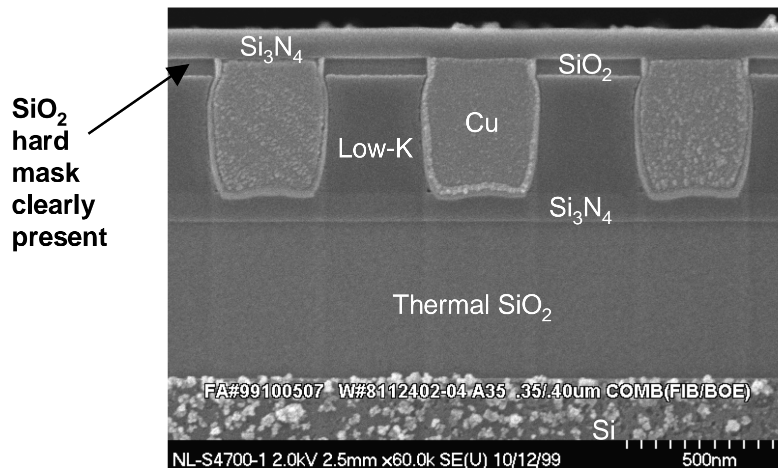


*Conventional Bright Field TEM image of completed M1 test vehicle incorporating Low-K **after TC1** (400°C, 1 hr.) anneal.*

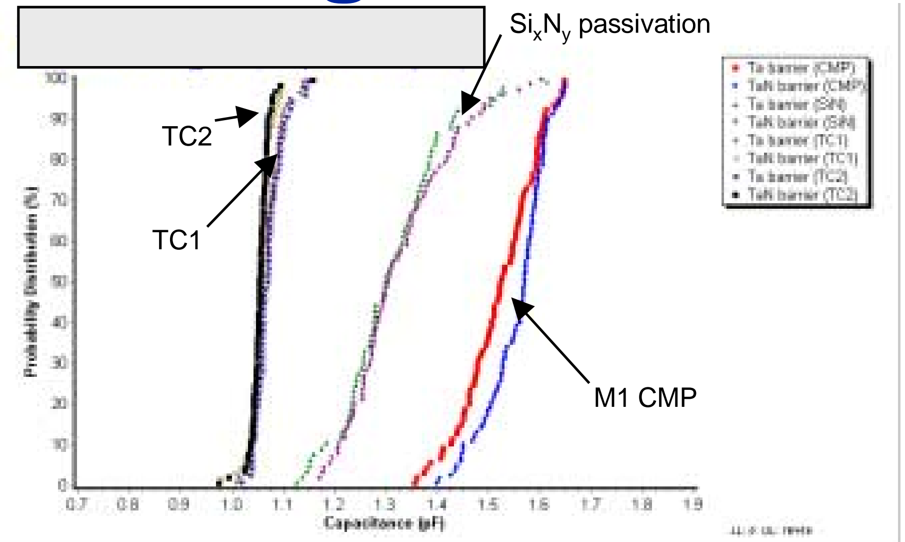
Acknowledgement: B. Foran, D. Brazeau (SEMATECH)

Another Low-K wi Damage

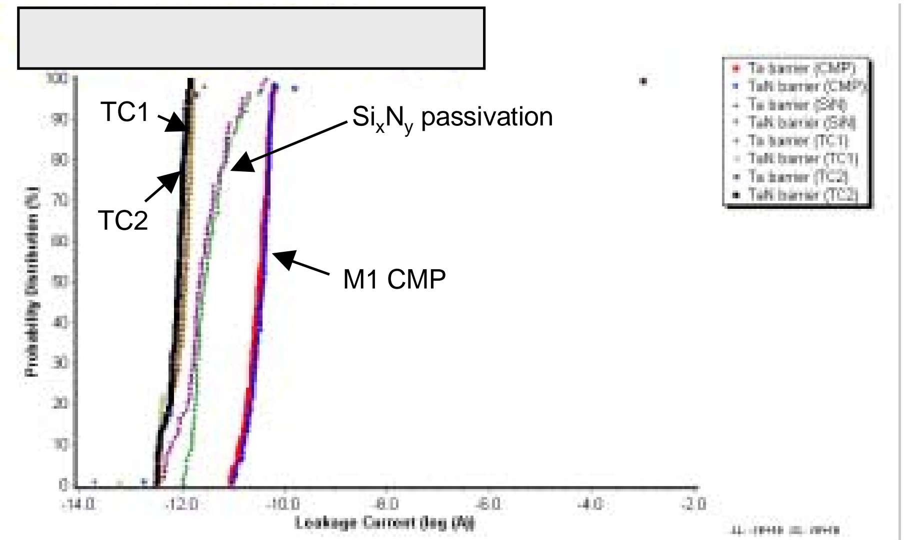
- **Electrical data**
  - Capacitance and leakage current decrease (shown in probability plots at right for 4 sequential electrical test steps) upon passivation and continued thermal cycling
  - Consistent with moisture desorption, at least through Si_xN_y passivation
  - Mechanism for capacitance decrease upon TC1, TC2 unknown



XSEM image (FIB/BOE) of completed 0.35µmL/0.40µmS COMB structure ***after TC2.***



Capacitance probability plot for 4 sequential etest steps.

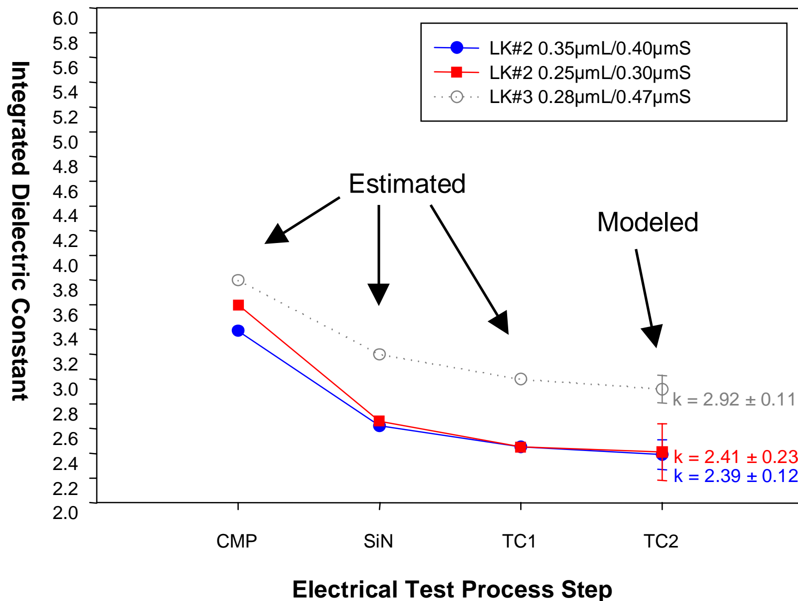


Leakage current probability plot for 4 sequential etest steps.

Integrated Dielectric Constants

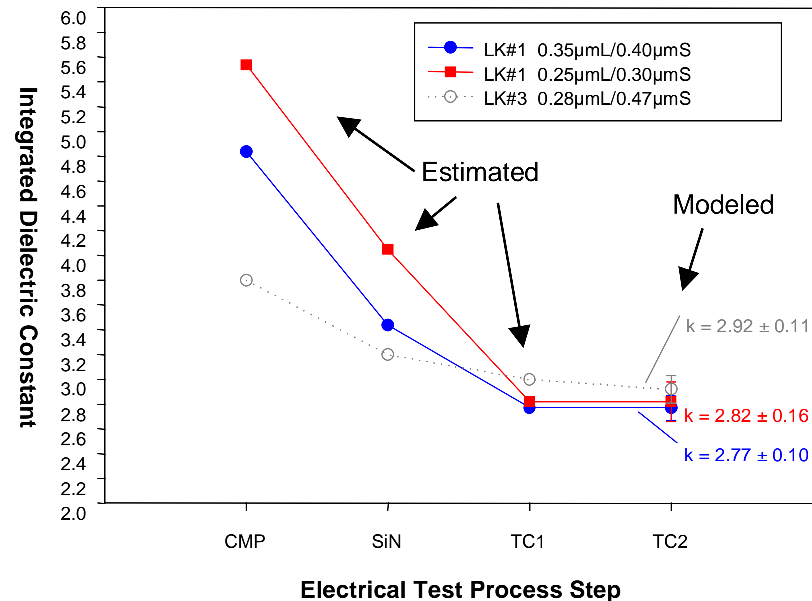
LK#2 (Rev. 8/98)

Blanket film (1 MHz) k = **2.09** ± **0.26**
15% Si, 28% O, **16% C**, 41% H
Moisture uptake (wt.%, NIST) = **12.0**
Average mass density (g/cm^3) = **1.087**
NIST measured "wall" density (g/cm^3) = **1.250**
Porosity (vol.%, assuming measured wall density) = **13.0**
Average pore size (Å) = **3.2 - 11.0**
Pore connectivity (%) = **100**
Further comments / issues: Thickness cracking threshold, "stress-corrosion" cracking



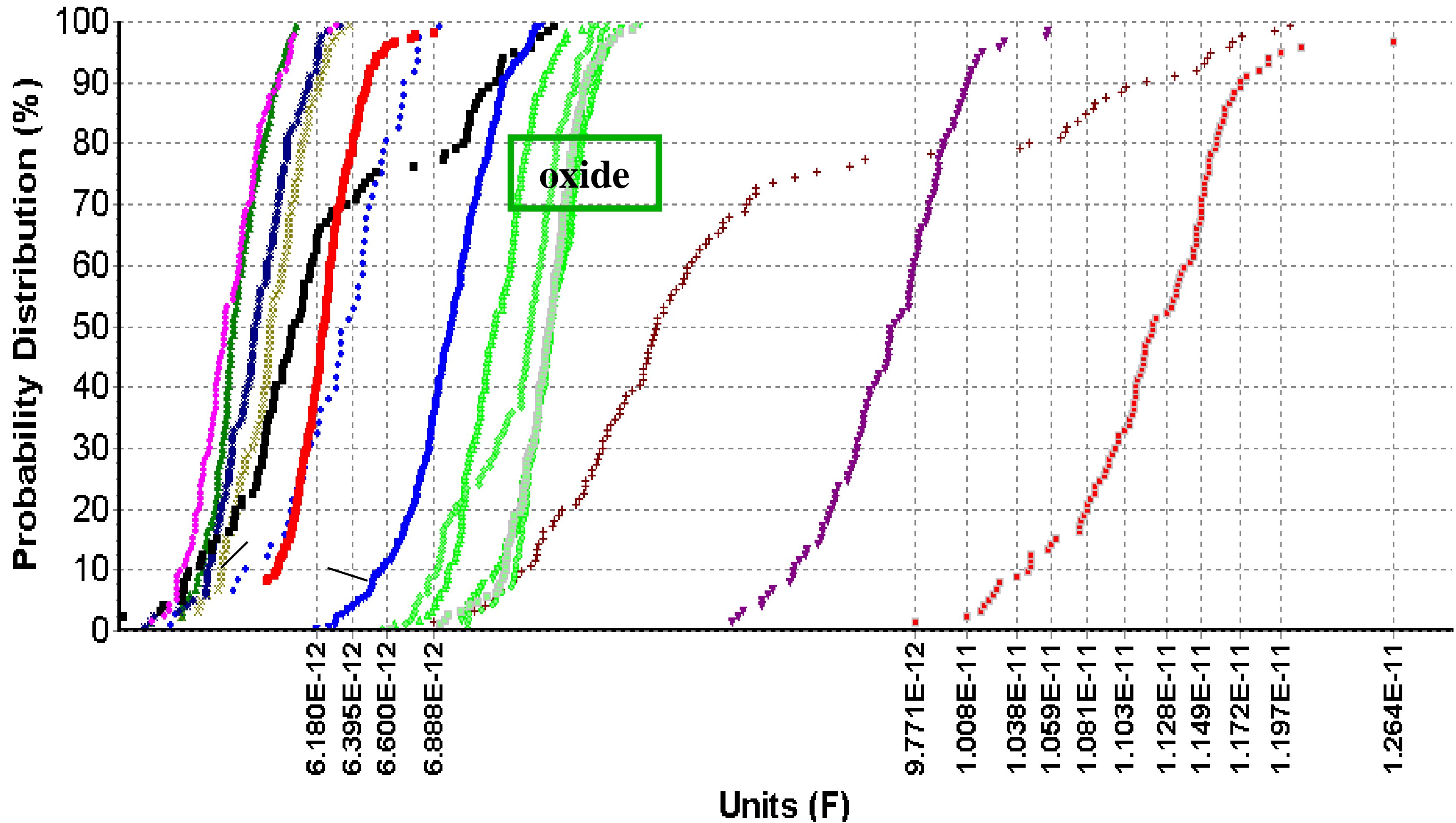
LK#1

Blanket film (1 MHz) k = **2.201** ± **0.014**
20% Si, 35% O, **11% C**, 34% H
Moisture uptake (wt.%, NIST) = **65.0**
Average mass density (g/cm^3) = **0.886**
NIST measured "wall" density (g/cm^3) = **2.103**
Porosity (vol.%, assuming measured wall density) = **57.9**
Average pore size (Å) = **11.9**
Pore connectivity (%) = **100**
Further comments / issues: Si-OH in blanket film FT-IR, trace metals



Comparison of Ash Techniques

.25-.30um Comb Line to Line Capacitance



TECHNOLOGY IMPACTS ON TOOL MARKET

TOOL/TECHNOLOGY	PLAYERS
CMP ($632M, 1998)* ($1.02B, 1999)**	AMAT / Ebara-Cybeq Speedfam-IPEC

TRENDs: 'Neutral' but Application Changing and 'Harder'

- Dielectric CMP Substituted by Cu CMP
- W Plug CMP Eliminated Except @ Contact Level
- May Still Need a 'Minor' Dielectric Planarization

*"Semiconductor Equipment, Manufacturing, and Materials Worldwide"; Dataquest; June, 7, 1999

**"Semiconductor Equipment, Manufacturing, and Materials Worldwide"; Dataquest; June, 26, 2000

SIMPLIFIED SUMMARY; Everything Could Change

- **For Circuit Performance Reasons the Materials Used to Fabricate IC Interconnects Need to Be Changed**
  - **The Change to Copper Forces a Change to Damascene**
    - **Damascene Fosters a Change Away From PVD Metal Toward Electroplate and or CVD**
      - **Damascene and the Move Toward Lower Dielectric Materials Is Creating Changes in Dielectric Deposition**
        - **As a Result of the Material and Process Technique Changes, All of the Manufacturing Tools Will Change in Some Fashion**

•Given a Choice Anybody Who Manufacturers Anything (Successfully) Would Rather Not Do This.

1999 SEMI “Copper-Critical” Survey, Results

265 industry respondents; 32% semiconductor manufacturers (merchant, captive, fabless and foundries) and consortia, majority in process development, R&D, or process engineering, 38% equipment, 11% material suppliers, 16% other.

SOME KEY FINDINGS

- *Over 40% of IC manufacturers say that volume production of Cu-based semiconductors will reach 10% of total dollar shipments by 2001.*
- *Equipment suppliers’ more enthusiastic on the readiness of the copper tool set are often inconsistent with IC manufacturers’ views.*
- *Equipment suppliers’ more conservative on the speed of copper adoption are often inconsistent with IC manufacturers’ views.*
- *Logic devices will lead the way, with the majority of respondents indicating first Cu shipments by 2000. ASIC follows in 2001; memory and system-on-a-chip are viewed as lagging beyond 2003.*
- *Over 70% of respondents still depend on tungsten as the preferred contact plug (or via) material.*