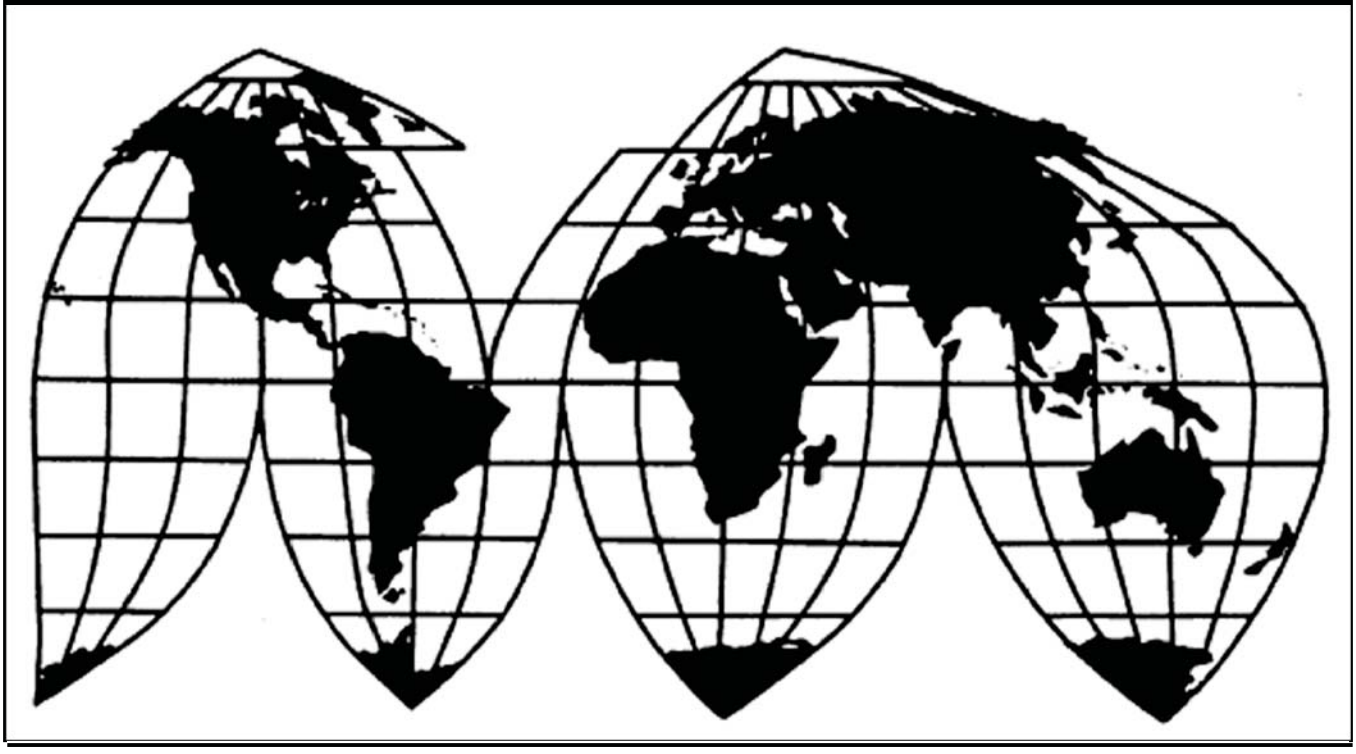
In the Matter of

Certain Semiconductor Integrated Circuits and Products Containing Same

Investigation No. 337-TA-665
Volume 2 of 2

Publication 4268 **October 2011**

U.S. International Trade Commission



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introduced as an exhibit during trial, but read aloud by Qimonda's counsel during Dr. Shanfield's cross examination. (*See* CRB at 77-78 (citing Tr. at 1739:6-1740:21, 1743:17-22).) In this testimony, Dr. Glew allegedly stated that he believed { } (Tr. at 1739:6-13.) This alleged "testimony" from Dr. Glew is not evidence, as the Glew deposition transcript was not admitted into evidence. Counsel's recitation during the cross examination of Dr. Shanfield does not suffice.

Assuming, *arguendo*, that the evidence showed { } this does not prove that the "connected to the substrate" limitation is met. As construed by me, this limitation requires a direct physical connection between the substrate and the contacts. Dr. Glew's testimony does not { } (Tr. at 1739:6-13.)

Qimonda has the burden to prove a domestic industry exists. After reviewing the expert testimony and other relevant evidence offered by the parties and admitted into the record, I find that Qimonda failed to introduce any evidence { } Thus, I find that Qimonda failed to demonstrate that { } meets the "connected to the substrate" limitation of claim 1.

V. INVALIDITY

A. Applicable Law

It is Respondents' burden to prove invalidity, and the burden of proof never shifts to the patentee to prove validity. *Scanner Techs. Corp. v. ICOS Vision Sys. Corp. N.V.*, 528 F.3d 1365, 1380 (Fed. Cir. 2008). "Under the patent statutes, a patent enjoys a presumption of validity, *see* 35 U.S.C. § 282, which can be overcome only through facts supported by clear and convincing

evidence[.]" *SRAM Corp. v. AD-II Eng'g, Inc.*, 465 F.3d 1351, 1357 (Fed. Cir. 2006).

The clear and convincing evidence standard placed on the party asserting the invalidity defense requires a level of proof beyond the preponderance of the evidence. Although not susceptible to precise definition, "clear and convincing" evidence has been described as evidence which produces in the mind of the trier of fact "an abiding conviction that the truth of a factual contention is 'highly probable.'" *Price v. Symsek*, 988 F.2d 1187, 1191 (Fed. Cir. 1993) (citing *Buildex, Inc. v. Kason Indus., Inc.*, 849 F.2d 1461, 1463 (Fed.Cir.1988).)

"A patent is invalid for anticipation if a single prior art reference discloses each and every limitation of the claimed invention. Moreover, a prior art reference may anticipate without disclosing a feature of the claimed invention if that missing characteristic is necessarily present, or inherent, in the single anticipating reference." *Schering Corp. v. Geneva Pharm., Inc.*, 339 F.3d 1373, 1377 (Fed. Cir. 2003). "When no prior art other than that which was considered by the PTO examiner is relied on by the attacker, he has the added burden of overcoming the deference that is due to a qualified government agency presumed to have properly done its job[.]" *Am. Hoist & Derrick Co. v. Sowa & Sons, Inc.*, 725 F.2d 1350, 1359 (Fed. Cir. 1984). Therefore, the challenger's "burden is especially difficult when the prior art was before the PTO examiner during prosecution of the application." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1467 (Fed.Cir.1990).

Section 103 of the Patent Act states:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35 U.S.C. § 103(a) (2008).

"Obviousness is a question of law based on underlying questions of fact." *Scanner Techs. Corp. v. ICOS Vision Sys. Corp. N.V.*, 528 F.3d 1365, 1379 (Fed. Cir. 2008). The underlying factual determinations include: "(1) the scope and content of the prior art, (2) the level of ordinary skill in the art, (3) the differences between the claimed invention and the prior art, and (4) objective indicia of non-obviousness." *Id.* (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966)). These factual determinations are often referred to as the "*Graham* factors."

"When no prior art other than that which was considered by the PTO examiner is relied on by the attacker, he has the added burden of overcoming the deference that is due to a qualified government agency presumed to have properly done its job[.]" *Am. Hoist & Derrick Co.*, 725 F.2d at 1359. Therefore, the challenger's "burden is especially difficult when the prior art was before the PTO examiner during prosecution of the application." *Hewlett-Packard Co.*, 909 F.2d at 1467.

The critical inquiry in determining the differences between the claimed invention and the prior art is whether there is a reason to combine the prior art references. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417-418 (2007). In *KSR*, the Supreme Court rejected the Federal Circuit's rigid application of the teaching-suggestion-motivation test. The Court stated that "it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." *Id.* at 418. The Court described a more flexible analysis:

> Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue…As our precedents make clear, however, the analysis need not seek out

> precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

Id.

Since *KSR* was decided, the Federal Circuit has announced that, where a patent challenger contends that a patent is invalid for obviousness based on a combination of prior art references, "the burden falls on the patent challenger to show by clear and convincing evidence that a person of ordinary skill in the art would have had reason to attempt to make the composition or device, . . . and would have had a reasonable expectation of success in doing so." *PharmaStem Therapeutics, Inc. v. Viacell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007).

B. The '670 Patent

Respondents' Position: Respondents allege that the '670 patent is anticipated by a technical article published by one of the named inventors of the '670 patent, Dr. Herbert Kabza and others entitled "Shallow Doping Profiles for High-Speed Bipolar Transistors" in the September 1988 edition of Journal de Physique. (hereinafter "the Kabza article") (RIB at 63-64 (citing RX-702).) More specifically, Respondents allege that more than one year before the filing date of the U.S. application that led to the '670 patent, the Kabza article was published disclosing the "two-step-anneal process that appears in claim 1." Respondents assert that, despite that fact, Dr. Kabza withheld the article from the U.S. Patent & Trademark Office ("USPTO"); but while withholding the Kabza article, he was arguing to the USPTO that the references cited by the examiner did not show the claimed two-step-anneal process.[44] (*Id.* at 63-64, 68.)

Respondents aver that the Kabza article was published before the earliest priority date for the '670 patent, and is thus, prior art under 35 U.S.C. § 102(a). (RIB at 64.) Respondents argue

[44] Respondents originally raised an inequitable conduct defense; but they have since abandoned that defense.

it is also prior art under § 102(b), because it was published more than one year before the earliest U.S. filing date for the application that led to the '670 patent. (*Id.*)

Respondents state that in general, the '670 patent is directed to a method for manufacturing polycrystalline silicon layers from amorphous silicon using a two-step anneal process. (RIB at 64 (citing RX-813C at Q. 39).) Respondents say that as set forth in claim 1, the first step of the two-step anneal takes place at an initial temperature below the crystallization temperature of amorphous silicon, and the second step takes place at a temperature that is above the crystallization temperature. (*Id.* (citing RX-813C at Q. 39; JX-7 at 6:45-66).) Respondents continue that by controlling heating in a reproducible manner, a polycrystalline silicon layer is formed having a defined particle size and texture. (*Id.* (citing RX-813C at Q. 39; JX-7 at 6:57-66).)

Respondents recite that Claim 1 of the '670 Patent states:

> 1. A method for the manufacture of a polycrystalline silicon layer on a substrate, comprising the steps of:
>
> [1] depositing an amorphous silicon layer on a substrate; and
>
> [2] then controlling the phase transformation of the amorphous silicon into a polycrystalline layer by the steps of:
>
> [3] heating said substrate with said amorphous silicon layer to an initial temperature that is lower than a crystalline temperature for the amorphous silicon,
>
> [4] holding the substrate with said amorphous silicon layer at the initial temperature to achieve a thermal equilibrium of the substrate with the amorphous silicon layer at said initial temperature, and then, after reaching the thermal equilibrium,
>
> [5] continuing the heating of said substrate with said amorphous silicon layer to raise the temperature at a controlled rate through a reproducible prescribed temperature profile from said initial temperature to a target temperature, said target temperature being higher than the crystallization temperature of said amorphous silicon so that said amorphous silicon

> crystallizes and becomes a polycrystalline layer having a defined grain size and texture.

(RIB at 64-65 (citing JX-7 at 6:41-66 (bracketed element numbers added by Respondents).)

Respondents assert that the Kabza article expressly discloses steps [2]-[5] of claim 1, specifically "the two-step anneal that is recited in the claim." Regarding step [1], Respondents concede that the Kabza article does not disclose "depositing an amorphous silicon layer on a substrate" as that term would be understood by a person of ordinary skill in the art. (*Id.*) They say it does describe, however, preamorphizing the silicon layer by implantation of germanium (Ge) ions at 60 keV. (RIB at 64-65 (citing RX-702 at 2).)

Respondents say Qimonda has asserted that "preamorphizing by ion bombardment" comes within the scope of "depositing an amorphous silicon layer" for purposes of infringement. (RIB at 65 (citing CX-141C at Q. 45).) Although Respondents argue that Qimonda is incorrect, they argue that if the Court were to adopt Qimonda's construction, it would necessarily have to use that claim construction for purposes of invalidity. (*Id.* (citing *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1330 (Fed. Cir. 2003) ("It is axiomatic that claims are construed the same way for both invalidity and infringement.")).) Under Qimonda's construction, Respondents allege, the Kabza article would disclose step [1] of claim 1 of the '670 patent. (*Id.*)

Respondents argue that even if the Court does not adopt Qimonda's construction for "depositing an amorphous silicon layer," the Kabza article is still material because it discloses each and every other element of claim 1. (RIB at 65-66 (citing RX-813C at Q. 47, 57).) They quote:

> To reduce the influence of the channelling effect, we preamorphized the bulk Si by Ge implantation at 60 keV prior to the B+ implant. To allow for direct comparison of the benefits of preamorphization, the B+ implantation was done at 10 keV as well. Of course perfect recrystallization of the amorphous layer is of

> crucial importance. To remove the defects we employed two step anneal. A first step (450°C, 30 min) is performed to smoothen the amorphous/crystalline interface /2/ and to create the proper conditions for defect-free recrystallization during the final high temperature step. In order to minimize the broadening of the base profile this anneal was done by rapid thermal processing (RTP) at 1075° (10 sec).

(*Id.* (citing RX-702 at 2).)

Respondents state that "Step [2] of claim 1" requires "controlling the phase transformation of the amorphous silicon into a polycrystalline layer." (RIB at 66 (citing JX-7 at 6:45-46).) They continue that the Kabza article discloses "recrystallization of the amorphous layer" using a two-step anneal. (*Id.* (citing RX-702 at 2).) Specifically, Respondents aver, the Kabza article discloses heating the substrate with amorphous silicon layer to 450°C for 30 minutes and then heating to 1075°C. (*Id.*) Therefore, they argue, the Kabza article discloses this limitation. (*Id.* (citing RX-813C at Q. 51; RX-702 at 2).)

Respondents recite that "Step [3] of claim 1" requires "heating said substrate with said amorphous silicon layer to an initial temperature that is lower than a crystalline temperature for the amorphous silicon." (RIB at 66 (citing JX-7 at 6:48-51).) Respondents argue that the Kabza article discloses using a first anneal or heat step at 450°C, which is below the crystallization temperature for amorphous silicon, thus disclosing the limitation of element 3. (*Id.* (citing RX-813C at Q. 51).)

Respondents note that "Step [4] of claim 1" requires "holding the substrate with said amorphous silicon layer at the initial temperature to achieve a thermal equilibrium of the substrate with the amorphous silicon layer at said initial temperature." (RIB at 66 (citing JX-7 at 6:52-55).) Respondents argue that the Kabza article discloses this limitation. (*Id.* (citing RX-813C at Q. 53).) Respondents say the Kabza article explains that the first part of the two-step anneal is performed at 450°C for thirty minutes. (*Id.* (citing RX-702 at 2).) Respondents reason

that because the substrate and amorphous silicon would achieve thermal equilibrium in not more than a couple of minutes, the thirty-minute first heating step in the Kabza article is sufficient to achieve thermal equilibrium. (*Id.* (citing RX-813C at Q. 53).)

Respondents say that element 5 of claim 1 requires "continuing the heating of said substrate with said amorphous silicon layer to raise the temperature at a controlled rate through a reproducible prescribed temperature profile from said initial temperature to a target temperature, said target temperature being higher than the crystallization temperature of said amorphous silicon so that said amorphous silicon crystallizes and becomes a polycrystalline layer having a defined grain size and texture." (RIB at 66-67 (citing JX-7 at 6:57-66).) Respondents argue that the Kabza article also discloses this element as it explains that after an initial heating to 450°C, the substrate is then heated to a target temperature of 1075°C. (*Id.* (citing RX-813C at Q. 54; RX-702 at 2).) Respondents add that 1075°C is above the crystallization temperature of amorphous silicon. (*Id.* (citing RX-813C at Q. 54).) They continue that the second heating step is programmed into the processing sequence of a rapid thermal processing (RTP) system. (*Id.* (citing RX-813C at Q. 54; RX-702 at 2).) Respondents say that Dr. Kabza admitted that rapid thermal processing is a controlled process that follows a reproducible temperature profile. (*Id.* (citing Deposition Stipulation, Tab 8, at 119:6-21).)

Respondents argue that in his rebuttal witness statement, Qimonda's expert, Dr. Hammond reads process steps into Kabza that are not present and are not required. (RIB at 67.) Respondents say that Dr. Hammond asserts that after the first step of the two-step anneal in the Kabza article, the substrate would be removed from a furnace, allowed to cool, and then inserted into a rapid thermal processing tool. (*Id.* (citing CX-1045C at Q. 33).) Respondents allege that the Kabza article does not mention any of these additional steps. (*Id.* (citing Tr. at 1372:24-

1373:4).) Respondents aver that nothing in the Kabza article suggests performing the two steps of the two-step anneal in separate tools or to remove the substrate from the tool after the first step. (*Id.*) They argue that it would not be unreasonable to perform both the low-temperature 450°C first step and the 1075°C second step in the same rapid thermal processing tool. (*Id.* (citing Tr. at 1374:25-1375:4).)

Respondents state that Dr. Hammond admitted that it would be possible to use the same rapid thermal anneal tool for both steps in the Kabza paper. (RIB at 67-68 (citing Tr. at 1476:25-1477:9).) Respondents argue that the test for what a prior-art reference discloses is what it discloses to a person of ordinary skill in the art. (*Id.* (citing *Motorola, Inc. v. Interdigital Tech. Corp.*, 121 F.3d 1461, 1473 (Fed. Cir. 1997) ("Although this disclosure requirement presupposes the knowledge of one skilled in the art of the claimed invention, that presumed knowledge does not grant a license to read into the prior art reference teachings that are not there.")).) Respondents reiterate that the Kabza article does not address using separate tools for the first and second heating steps in the two-step anneal. (*Id.*) They argue that it is undisputed that a single rapid thermal processing tool would work for both steps of the Kabza article's two-step anneal. (*Id.* (citing Tr. at 1374:25-1375:4, 1476:25- 1477:9).) Respondents argue that it is not necessary to use different tools for the two steps in the Kabza article, then a person of ordinary skill would not use different tools. (*Id.*)

Respondents argue that the court should not read processing steps into the Kabza article that are not there. Respondents continue that if the court were to adopt Qimonda's position that "preamorphizing by ion bombardment" is within the scope of "depositing an amorphous silicon layer," then the Kabza article discloses every element of claim 1 of the '670 patent, and that claim is invalid as anticipated by the Kabza article. (RIB at 68.)

In their reply brief, Respondents say that the only argument Qimonda raises in defense of the patent, they say, is that the Kabza article does not disclose the following limitation: "continuing the heating of said substrate with said amorphous silicon layer to raise the temperature at a controlled rate through a reproducible prescribed temperature profile from said initial temperature to a target temperature, said target temperature being higher than the crystallization temperature of said amorphous silicon." (*Id.*)

Respondents argue that the Kabza article does disclose the foregoing limitation. Respondents say, Kabza explains that after an initial heating to 450°C, the substrate is then heated to a target temperature of 1075°C, which is clearly above the crystallization temperature of amorphous silicon. (RRB at 31.) Respondents allege the second heating step is programmed into the processing sequence of a rapid thermal processing (RTP) system. (*Id.* (citing RX-813C at Q. 54; RX-702 at 2).) Dr. Kabza admitted that rapid thermal processing is a controlled process that follows a reproducible temperature profile. (*Id.* (citing Deposition Stipulation, Tab 8 at 119: 6-21).)

Qimonda's Position: Qimonda argues that the prior art reference relied upon by Respondents does not anticipate or render obvious claim 1 of the '670 patent. Respondents argue that the Kabza reference and the deposition testimony of Dr. Kabza show that Respondents' argument is meritless. (CIB at 202-203.)

Qimonda asserts that the Kabza reference does not teach element 5 of claim 1 of the '670 patent, to wit: "after reaching the thermal equilibrium, continuing the heating of said substrate with said amorphous silicon layer to raise the temperature at a controlled rate through a reproducible prescribed temperature profile from said initial temperature to a target temperature, said target temperature being higher than the crystallization temperature of said amorphous

silicon so that said amorphous silicon crystallizes and becomes a polycrystalline layer having a defined grain size and texture." (CIB at 203 (citing JX-7 at claim 1; CX-1045C at Q. 33).)

Qimonda posits that the method claimed in claim 1 of the '670 Patent controls the phase transformation of the amorphous silicon into polycrystalline silicon through a predetermined, controlled continuous heating process that begins a first heating step and continues through a second heating step, with times and temperatures specified for the duration of the continuous heating process. (CIB at 203-204 (citing CX-141C at Q. 58).) Qimonda claims it is undisputed that claim 1 of the '670 patent requires a process that does not include any interruption between the first heating step and the second heating step. (*Id.*) Qimonda asserts that once heated to a thermal equilibrium, the substrate may not be allowed to cool before it is heated through a "reproducible prescribed temperature profile." (*Id.* (citing CX-1045C at Q. 33; Tr. at 1370:8-22).) Qimonda argues that this control is necessary to achieve consistent and reliable production of polycrystalline silicon having a defined grain size and texture. (*Id.* (citing CX-141C at Q. 58; JX-7 at 2:39-56, 3:22-46).)

Qimonda contrasts the foregoing with the Kabza reference, which they say discloses a two-step annealing process where the first step is performed, then the substrate is removed from the tool, sits for an indeterminate period of time, cools an indeterminate amount, and then is subjected to the second annealing step. (CIB at 204 (citing CX-1045C at Q. 33; CX-547C at 141-144).)

Qimonda continues that the first heating step in the Kabza reference is a 450°C, 30 minute anneal. (CIB at 204.) The second anneal is a 10 second, 1075°C rapid thermal processing ("RTP") anneal. (*Id.* (citing CX-1045C at Q. 33; CX-547C at 143; RX-702 at 2).)

Qimonda points to the testimony of Dr. Kabza during his deposition, to say that one of ordinary skill in the art would recognize these two anneal steps were performed in different tools – the first in a conventional furnace, and the second in a rapid thermal processing tool – and that the wafer would be removed from the first tool and experience room temperature for an indeterminate period of time before being subject to the second step:

> Q. Do you agree that [the Kabza] reference discloses all of those steps?
>
> * * *
>
> THE WITNESS: No, it is not corresponding to Patent.
>
> * * *
>
> Q. I didn't ask you if it was corresponding to the Patent, sir, I asked you if it disclosed all of the steps that I had mentioned in the prior question?
>
> * * *
>
> THE WITNESS: There are two thermal steps which do not stay in a direct relationship to each other.
>
> Q. What do you mean?
>
> A. When you read it then it states here that you first -- that the first step would be at 450°C will be heated within 30 minutes and for sure it happens not in an RTA and not in this rapid terminal processing unit. Which means that the wafer from this first step under 450°C will be taken out, it will be cooled to any kind of temperature, for example, air temperature, normal, and then our rapid thermal processing step comes.
>
> Q. Show me the words that say that, sir?
>
> * * *
>
> THE WITNESS:
>
> "A first step (450°C at 30 minutes) is performed to smoothen the amorphous/crystalline interface and to create the proper conditions for defect-free recrystallization during the final high temperature step. In order to minimize the broadening of the base profile this anneal [so the high temperature step] is done by rapid thermal processing at 1075°C for 10 seconds."
>
> That means that the wafer is from a furnace where, just a common furnace, where it has been heated up to 450°C within 30 minutes and then, for example, a week

> later this wafer comes to rapid thermal processing unit to perform this second step.
>
> Q. Which words of this paragraph say that it is taken out of the machine used for the first step before the rapid thermal processing step is performed?
>
> * * *
>
> THE WITNESS: It is implicitly known for each who knows, who has knowledge in the field because nobody could do this 30 minute step in a rapid thermal processing equipment because it is too expensive. And here it is a clear difference to claim in Patent '670. Besides there is a total different application.

(CIB at 204-205 (citing CX-547C at 142:12-144:22).)

Qimonda states that Dr. Kabza testified that, while the Kabza paper did not explicitly state that the wafer was removed from the tool used to perform the first step, one of ordinary skill in the art would recognize that the first step would not be performed in an expensive, specialized rapid thermal processing machine, when a cheaper, common furnace could be used to perform that process:

> Q. But you will agree with me that the article in Exhibit 5 does not explicitly say that the wafer is removed from the furnace after the first temperature step, correct?
>
> * * *
>
> THE WITNESS: It doesn't state in explicit words how the transfer between the step of 450°C and 1075° takes place.
>
> Q. So the paper does not explicitly state that it is done in separate chambers, does it?
>
> * * *
>
> THE WITNESS: Everybody who has certain knowledge in the field will understand that because they will know that this 30 minutes in rapid thermal processing is not possible, not -- it is senseless.

(CIB at 205-206 (citing CX-547C at 152:12-153:4).)

Qimonda also points to the testimony of Dr. Hammond who testified:

> Kabza, it describes a first step that takes place at 450°C for 30 minutes. One of ordinary skill in the art would recognize that a rapid thermal processing and/or

> rapid thermal annealing tool was not used to complete this 30 minute step. Instead, a conventional furnace would have been used. On the same page, the Kabza reference describes the second, high-temperature step as a rapid thermal processing step. Therefore, one of ordinary skill in the art would recognize that the substrate would be removed into the air and have undergone cooling between the two steps.

(CIB at 206 (citing CX1045C at Q. 33).)

Qimonda argues that the method in use before the invention of the '670 patent used either a one-step or a two-step process to crystallize amorphous silicon. (CIB at 207-208.) For a one-step process, a furnace would be set at a specific temperature and then the wafers would be inserted into the furnace for a specified time period and removed. (*Id.*) For a two-step process, the general approach was to heat the wafer at one temperature for one period of time, remove the wafer from the tool, then at some future point, to heat the wafer at another temperature for another period of time. (*Id.*) Qimonda continues this removal of the substrate would allow the substrate to cool between the first and second heating steps. Qimonda asserts that the variable cooling associated with the removal of the wafer would affect grain size and texture of the resultant polycrystalline silicon. (*Id.* (citing CX-141C at Q. 21).) Qimonda argues that this flaw pervaded the alleged prior art, as it did the practice of those of skill in the art at the time that the application for the '670 patent was filed. (*Id.*) Qimonda asserts that no combination of references teaches the limitation of element 5 of the '670 patent, so the Kabza reference cannot render the '670 patent obvious. (*Id.* (citing CX-1045C at Q. 31-35).)

Commission Investigative Staff's Position: The Staff notes that Dr. Bruce Smith, Respondents' expert, testified that the Kabza article anticipates or would have rendered obvious all of the asserted claims of the '670 patent using Qimonda's apparent construction of the term "depositing" as set forth in claim 1 of the '670 patent. (SIB at 41 (citing RX-813C at Q. 47).) Staff asserts that Dr. Smith admitted that Kabza is not an anticipatory reference unless

Qimonda's claim construction for the term "depositing" a definition that includes ion implantation, is adopted. (*Id.* (citing RX-813C at Q. 57; Tr. at 1407).) Staff submits that under a proper claim construction, the asserted claims of the '670 patent would not be anticipated or obvious in light of Kabza. (*Id.*)

Staff restates its disagreement with Qimonda's construction that the term "depositing" as used in claim 1 of the '670 patent includes preamorphization by ion bombardment. Therefore, Staff does not believe that Kabza renders any of the asserted claims inval*id.* (SIB at 42.)

Staff opines that the evidence does not clearly and convincingly show that Kabza discloses, among other things, a continuous heating process as required by claim 1 regardless of the adopted construction of the term "depositing an amorphous silicon layer." (SIB at 42.) Staff avers that Dr. Hammond opined that Kabza discloses a "two-step annealing process where the first step is performed, then the substrate is removed from the tool, sits for an indeterminate period of time, cools an indeterminate amount, and then is subjected to the second annealing step." (*Id.* (citing CX -1045C at Q. 33).) Staff asserts that Dr. Hammond also opined that this two-step anneal process was the traditional and most cost effective method used in the industry. (*Id.* (citing Tr. at 1476).) Staff says that Dr. Hammond also pointed out that Kabza "does not specify the time or the temperature between the two [annealing] steps …" further undermining a conclusion that Kabza discloses a continuous heating process. (*Id.* (citing CX-1045C at Q. 33).) Staff's view is that Dr. Smith never effectively rebutted Dr. Hammond's opinion in this regard, let alone to the heightened level required to invalidate the claim. (*Id.*)

Discussion and Conclusion: Based upon the evidence before me, I find that Respondents have failed to meet their burden to show by clear and convincing evidence that the

Kabza article[45] anticipates claim 1 of the '670 patent.

First, to the extent that the Respondents focus on the construction of "depositing an amorphous silicon layer on a substrate" proposed by Qimonda, their argument is rendered moot by the fact that Qimonda's construction was ***not*** adopted by me in this matter.[46] I note, too, regarding element 1 of claim 1, the Kabza article does not disclose "depositing an amorphous silicon layer on a substrate" as that term would be understood by a person of ordinary skill in the art. Hence, using the construction that has been applied in this case, the Kabza article clearly does not anticipate claim 1 of the '670 patent.

Second, assuming *arguendo* that one were to apply the Kabza article to the elements of claim 1 of the '670 patent using Qimonda's definition, the record lacks clear and convincing evidence that the Kabza article would then anticipate all of the elements of claim 1.

Respondents quoted the relevant language of the Kabza article:

> To reduce the influence of the channelling effect, we preamorphized the bulk Si by Ge implantation at 60 keV prior to the B+ implant. To allow for direct comparison of the benefits of preamorphization, the B+ implantation was done at 10 keV as well. Of course perfect recrystallization of the amorphous layer is of crucial importance. To remove the defects we employed two step anneal. A first step (450°C, 30 min) is performed to smoothen the amorphous/crystalline interface /2/ and to create the proper conditions for defect-free recrystallization during the final high temperature step. In order to minimize the broadening of the base profile this anneal was done by rapid thermal processing (RTP) at 1075° (10 sec).

(RX-702 at 2.)

I have already found the clear and unambiguous language of asserted claim 1 provides for the deposit of a layer of silicon that is in amorphous form and then sets forth the step-by-step sequential process of transforming that amorphous silicon into polycrystalline form.

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[45] The Kabza article was published in September 1988.

[46] For a detailed discussion of the construction of the term "depositing an amorphous silicon layer on a substrate," see Section III.B.3 of this decision.

In claim 1, the beginning point is "depositing an amorphous silicon layer on a substrate." Immediately following that language, claim 1 continues, "and" followed by element 2, which states, "then ***controlling the phase transformation of the amorphous silicon into a polycrystalline layer by the steps of***:" Claim 1 then lists, in elements 3-5, a step-by-step process for achieving that transformation. (JX-7 at 6:43-47; 6:48-66) (emphasis added.) Element 5 of claim 1 requires "continuing the heating of said substrate with said amorphous silicon layer to raise the temperature ***at a controlled rate through a reproducible prescribed temperature profile from said initial temperature to a target temperature*** that is higher than the crystallization temperature of said amorphous silicon." (*Id.* at 6:57-63) (emphasis added.)

An example of a reproducible prescribed temperature profile is illustrated in the '670 patent specification, which describes for example:

> … then the furnace is changed from the initial temperature to a target temperature. The target temperature lies above the crystallization temperature of the silicon layer, for example at 700° C. The temperature change ensues corresponding to a predetermined temperature profile, for example having a change rate of less than or equal to 10° C. per minute.

(JX-7 at 5:41-47.)

The process described in the Kabza article does not provide clear and convincing evidence that it calls for a reproducible prescribed temperature profile from the initial temperature to a target temperature. It merely provides a first step of heating and holding the temperature at 450° C for 30 minutes, and then to use rapid thermal processing (RTP) to achieve 1075° C and to hold that temperature for 10 seconds. (RX-702 at 2.) Although Respondents say that Dr. Kabza admitted that rapid thermal processing is a controlled process that follows a reproducible temperature profile, his testimony actually was that RTP uses a prescribed temperature profile only "when the process is running in a control manner and the conditions are

okay." (Deposition Stipulation, Tab 8, at 119:6-21.) I note that the relevant language of the Kabza article, quoted *supra*, does not stipulate that the RTP is to be done "in a controlled manner."

The process described in the Kabza article calls for heating the silicon to a temperature of 450° C for 30 minutes. It does not specify the tool to be used in this step. The second step of the process, however, specifies use of an RTP to heat the silicon to 1075° C for 10 seconds. What is clear from this language is that the authors, when they so desired, were fully cognizant and capable of specifying the RTP tool for use in heating the silicon. The fact that they did not specify RTP for the initial phase leads me to conclude that a separate, unspecified, tool for that initial heating was considered appropriate.

My impression is supported by the testimony of Dr. Kabza, who said:

> Q. But you will agree with me that the article in Exhibit 5 does not explicitly say that the wafer is removed from the furnace after the first temperature step, correct?
>
> * * *
>
> THE WITNESS: It doesn't state in explicit words how the transfer between the step of 450°C and 1075° takes place.
>
> Q. So the paper does not explicitly state that it is done in separate chambers, does it?
>
> * * *
>
> THE WITNESS: Everybody who has certain knowledge in the field will understand that because they will know that this 30 minutes in rapid thermal processing is not possible, not -- it is senseless.

(CX-547C at 152:12-153:4.)

Dr. Hammond also testified on this point in his rebuttal testimony, saying in relevant part:

> One of ordinary skill in the art would recognize that the Kabza reference, like Sasaki, described a two-step annealing process where the first step is performed, then the substrate is removed from the tool, sits for an indeterminate period of time, cools an indeterminate amount, and then is subjected to the second

> annealing step. As illustrated by slide 0048A of Exhibit CDX-40, on page 2 of Kabza, it describes a first step that takes place at 450°C for 30 minutes. One of ordinary skill in the art would recognize that a rapid thermal processing and/or rapid thermal annealing tool was not used to complete this 30 minute step. Instead, a conventional furnace would have been used. On the same page, the Kabza reference describes the second, high-temperature step as a rapid thermal processing step. Therefore, one of ordinary skill in the art would recognize that the substrate would be removed into the air and have undergone cooling between the two steps … The Kabza reference does not specify the time or temperature between the two steps.

(CX1045C at Q. 33.)

Dr. Hammond also opined at trial that this two-step anneal process was the traditional method used in the industry. (Tr. at 1476:11-14.) He testified that using a rapid thermal procession or rapid thermal annealing tool to perform the initial step of heating and holding the silicon at 450° C. for 30 minutes as described in the Kabza article could not be done. He said "the temperature is quite low for any RTA apparatus" and that the time of 30 minutes was "far beyond anything one of ordinary skill would consider to use. RTA is used for tens of seconds, perhaps a hundred seconds' worth of time. Furnaces have historically been used for process times of tens of minutes to tens of hours." (*Id.* at 1477:1-9.)

The evidence supports a finding that the process contemplated by the Kabza article is a two-step process in which the silicon is heated and held at 450° C. for 30 minutes, then it is removed from the tool for an indeterminate period of time and cools an indeterminate amount, after which it is subjected to RTP to a temperature of 1075° C for a period of 10 seconds. Hence, the Kabza article does not disclose the requirement of element 5 for "***continuing*** the heating of said substrate with said amorphous silicon layer to raise the temperature ***at a controlled rate through a reproducible prescribed temperature profile from said initial temperature to a target temperature*** that is higher than the crystallization temperature of said amorphous silicon."

Based on all of the foregoing, and assuming *arguendo* that Qimonda's definition of "depositing an amorphous silicon layer on a substrate" were correct, I find that the record lacks clear and convincing evidence that the Kabza article discloses element 5 of claim 1 of the '670 patent.

C. The '434 Patent

1. Maloney

Respondents' Position: Respondents argue that the paper titled "Designing MOS Inputs and Outputs to Avoid Oxide Failure in the Charged Device Model," by Timothy J. Maloney, Electrical Overstress/Electrostatic Discharge Symposium Proceedings (Sept. 27-29, 1988), at 220-227 ("Maloney") anticipates claims 1-5 and 7 of the '434 patent. (RIB at 103-104.)

Regarding claim 1, Respondents assert that Maloney discloses every limitation. (RIB at 104 (citing RX0774C; RX-205).) They claim that one of ordinary skill in the art would know that Maloney discloses a semiconductor component. (*Id.*) Respondents state that Figure 2c of Maloney discloses a semiconductor body that has a terminal pad, a semiconductor function element, and an electrically conductive connecting line connecting the terminal to the semiconductor function element. (*Id.*) Respondents offer an annotated version of Figure 2c of Maloney with the claim elements identified. (*Id.* at 105 (citing RX-774C at Q. 145; RDX-124; RX-205 at 221-222, Fig. 2c).)

Respondents claim that Figure 2c also discloses the claimed protective element, with the protective element connected between the terminal pad and the semiconductor function element. (RIB at 105 (citing RX-774C at Q. 145, RX-205 at 221-222, Fig. 2c, RDX-124).) Respondents point to two supply lines as required by claim 1, and they assert that the supply lines are connected to a common VSS potential. (*Id.* (citing RX-744C at Q. 142; RX-205).)

Respondents state that Qimonda's only argument that Maloney does not anticipate claim 1 is that there is only one supply line disclosed, and that Respondents claim that the two supply lines are actually different portions of the same line. (RIB at 106 (citing CX-1044C, Tr. at 1529:24-1551:24; RX-774C).) Respondents rebut this assertion by pointing to a portion of Maloney that describes separate ground paths. (*Id.* (citing RX-205 at 222; RX-774C at Q. 145; RDX-124).)

Finally, Respondents claim that Figure 2c of Maloney discloses a clamp element connected to the first supply line. (RIB at 106 (citing RX-774C at Q. 145; RX-205 at 221-222, Fig. 2c; RDX-124).) Thus, Respondents claim that Maloney anticipates, because it discloses every limitation in claim 1.

Regarding claim 2, Respondents assert that Maloney also discloses that the first supply line may be connected to the second supply line by a bond connection. (RIB at 107 (citing RX-205 at 222; RX-774C at Q. 145).) Moreover, according to Respondents, one of ordinary skill in the art would have appreciated that each "Bus R" in Figure 2c represents various parasitics of ground bus paths, which typically included wire resistances, bond connections, lead frame resistances, inductances, and the like. (*Id.* (citing RX-774C at Q. 142; RX-205).)

Regarding claim 3, Respondents argue that Figure 2c of Maloney discloses that: (1) the semiconductor function element has a terminal; (2) the bond connection has a terminal; (3) the first supply line has a portion disposed between the terminal of the semiconductor function element and the terminal of the bond connection; and (4) the clamp element is connected to the portion of the first supply line. (RIB at 107-108 (citing RX-774C at Q. 149; RX-205 at 221-222, Fig. 2c; RDX-124).)

Respondents argue that claim 4 is invalid because the term "immediate spatial vicinity" is

indefinite. (RIB at 109.) If the term is not found indefinite, Respondents argue that Maloney anticipates claim 4 because Maloney calls for the clamp element to be placed at the input buffer. (*Id.* (citing RX-205 at 222; RX-774C at Q. 151; RDX-124).) Respondents state that placing the clamp element at the input buffer clearly constitutes the "immediate spatial vicinity." (*Id.* (citing RX-774C at Q. 151).)

Regarding claim 5, Respondents assert that Maloney is anticipatory. Respondents state that Figure 2 of Maloney "discloses the clamp element implemented as a MOS transistor having its main current path connected to the connecting line and to the first supply line, with its gate terminal connected to the first supply line, which is generally referred to as a ggNMOS." (RIB at 109-110 (citing RX-774C at Q. 152; RX-205 at 221-222, Fig. 2c; RDX-124).)

Respondents argue that Maloney anticipates claim 7. Respondents claim that Figure 2c of Maloney discloses that: (1) the connecting line includes a given resistance (i.e., the inherent resistance of the portion flagged by the dashed brown oval); (2) the protective element includes a resistor connected between the terminal pad and the semiconductor function element; and (3) the resistor has a resistance that has been adjusted for setting a sum of resistance of the resistor and the given resistance to a predetermined value of at least "typically a few hundred ohms." (RIB at 110 (citing RX-774C at Q. 155; RX-205 at 221-222, Fig. 2c; RDX-124).)

Qimonda's Position: Qimonda argues that Maloney fails to anticipate claim 1 because it teaches a single supply line connected to ground, instead of first and second supply lines. (CIB at 101 (citing CX-1044C at Q. 30, 31; CDX-38 at QAG-665-ITC-0233821; Tr. at 1543:9-1544:10, 1546:4-1548:7; RX-205).) Qimonda further claims that Maloney fails to teach that the supply lines are electrically conductively connected. (*Id.* at 102 (citing RX-205 at LSI-337-665-0061847; CX-1044C at Q. 30, 31; CDX-38 at QAG-665-ITC-0233821; Tr. at 1543:9-1544:10,

1546:4-1548:7).)

Qimonda states that a person with ordinary skill would have interpreted the two circuit elements labeled "BUS R" in Maloney as two internal-circuitry buses, which are connected on-chip rather than being spatially separated to decouple voltage fluctuations. (CIB at 103 (citing CX-1044C at Q. 30, 31; CDX-38 at QAG-665-ITC-0233821; Tr. at 1543:9-1544:10, 1546:4-1548:7).) Qimonda argues that it was common at the time the '434 patent was filed to connect multiple bond wires to a single bus or on-chip track. (*Id.* at 104 (citing CX-1044C at Q. 30, 31; CDX-38 at QAG-665-ITC-0233821; Tr. at 1543:9-1544:10, 1546:4-1548:7).) Qimonda claims that a person of ordinary skill in the art at the time of the '434 patent would have interpreted Maloney to refer to this configuration. (*Id.* (citing CX-1044C at Q. 30, 31; CDX-38 at QAG-665-ITC-0233821; Tr. at 1543:9-1544:10, 1546:4-1548:7).) Qimonda asserts that since ground bus (VSS) resistance is especially important for every on-chip track, the most straightforward interpretation of Fig. 2b and Fig. 2c to a person of ordinary skill in the art would have been that the two "BUS R" labels represented resistance between circuit elements on a single wiring bus or on-chip track. (*Id.* (citing CX-1044C at Q. 30, 31; CDX-38 at QAG-665-ITC-0233821; Tr. at 1543:9-1544:10, 1546:4-1548:7).) Therefore, according to Qimonda, Maloney would not have taught a person of ordinary skill in the art to spatially separate the buses from each other on the chip, so that voltage fluctuations are decoupled.

In addressing the dependent claims, Qimonda argues that because Maloney does not anticipate claim 1, it does not anticipate any of the dependent claims. (CIB at 104-106.) Regarding claim 2, Qimonda also argues that Maloney also fails to describe "at least one bond connection connecting said first and second supply lines to one another." (*Id.* at 104-105.) Qimonda asserts that a person of ordinary skill in the art would have interpreted the elements

labeled "BUS R" in Figure 2c as two internal buses connected on-chip. (*Id.* at 105 (citing CX-1044C at Q. 32).)

Regarding claim 3, Qimonda argues that Maloney does not describe that "said semiconductor function element has a terminal, said at least one bond connection has a terminal, said first supply line has a portion disposed between said terminal of said semiconductor function element and said terminal of said at least one bond connection, and said clamp element is connected to said portion of said first supply line." Qimonda states that based on the plain meaning of the claim, it is apparent that this limitation requires a specific spatial arrangement of circuit elements. (CIB at 105 (citing CX-1044C at Q. 33).) Qimonda asserts that Fig. 2c of Maloney does not show a layout, but simply provides a highly simplified sketch of a circuit schematic. (*Id.* (citing CX-1044C at Q. 33).) According to Qimonda, because Maloney provides no guidance, there would be a virtually unlimited number of physical layouts embodying the circuit of Fig. 2c, which would not include two decoupled on-chip tracks. (*Id.* (citing CX-1044C at Q. 33).)

Regarding claim 4, Qimonda claims that Maloney does not describe that "said semiconductor function element is connected to said first supply line and to said connecting line at a given location, and said clamp element has a first terminal connected to said first supply line and a second terminal connected to said connecting line, in the immediate spatial vicinity of said given location." Qimonda asserts that Maloney does not show the specific spatial arrangement required by the claim. (CIB at 106 (citing CX-1044C at Q. 34).) Qimonda points to the portion of Maloney that states that "[t]o avoid difficulties with ground bus wiring, the scheme shown in Fig. 2c is used. The pi network cell can remain undisturbed as long as TG2 is added at the input buffer [TN_{IN}, TP_{IN}], sharing a common ground connection with it." (*Id.* (citing RX-205 at LSI-

337-665-0061847-61848; CX-1044C at Q. 34).) Qimonda argues that one of ordinary skill in the art would understand this statement in light of Fig. 2c to refer to circuit topology (*i.e.*, to the schematics themselves) as opposed to spatial vicinity. (*Id.* (citing RX-205 at LSI-337-665-0061847-61848; CX-1044C at Q. 34).)

Regarding claim 7, Qimonda asserts that Maloney does not describe that "said connecting line has a given resistance, said protective element includes a resistor connected between said terminal pad and said semiconductor function element, and said resistor has a resistance being adjusted for setting a sum of the resistance of said resistor and the given resistance to a predetermined value." Qimonda notes that Maloney states that: "[t]he rest of the protection 'pi network' is a series resistor (typically a few hundred ohms) and the aforementioned grounded gate NMOS device to clamp the gate oxide voltage on TNin and TPin." (CIB at 107 (citing RX-205 at LSI-337-665-0061847-61848; CX-1044C at Q. 35).) Qimonda states that based on this passage, Maloney, at best, only teaches a *series resistor*, and not the sum of the resistances, as having a predetermined value. (*Id.* (citing CX-1044C at Q. 35).)

Commission Investigative Staff's Position: Staff argues that Maloney does not anticipate claim 1 of the '434 patent. (SIB at 87.) Staff asserts that Maloney does not clearly and convincingly disclose "a second supply line for the first supply potential…being electrically conductively connected to said first supply line" as required in claim 1. (*Id.*) Staff notes that Dr. Cottrell opined that the two circuit elements labeled "BUS R" are internal-circuitry buses which are connected on-chip rather than being spatially separated to decouple voltage fluctuations. (*Id.*) Staff asserts that given Dr. Cottrell's opinion, and the lack of clear guidance from Maloney, there is no clear and convincing evidence that Maloney discloses the claimed second supply line. (*Id.* at 87-88.)

Discussion and Conclusion: Based upon the evidence before me, I find that Respondents have clearly and convincingly demonstrated that Maloney anticipates claims 1, 2, 3, and 5 of the '434 patent.

Maloney was published in 1988, meaning that it is prior art pursuant to 35 U.S.C. § 102(a), (b). (RX-205; JX-1.) Maloney was not before the examiner during the prosecution of the '434 patent. (JX-1; JX-2.)

Respondents focus on Figure 2c of Maloney, which is reproduced below:

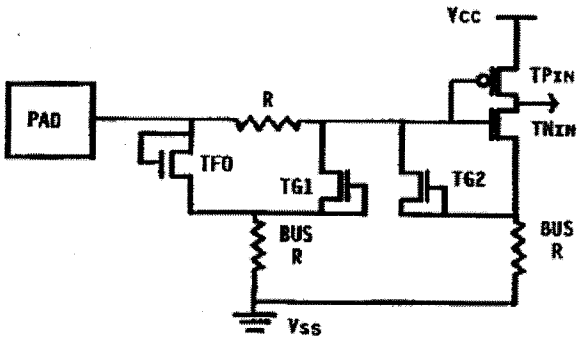


Fig. 2c. Improved input protection scheme, not affected by ground bus resistance.

(RX-205 at LSI-337-665-0061847.)

Regarding claim 1, there is no dispute that Maloney discloses a semiconductor component which includes a semiconductor body. (RX-205 at LSI-665-0061847-48; RX-774C at Q. 145; RDX-124.) Maloney discloses a terminal pad, labeled "PAD" in Figure 2c. (*Id.*) Maloney discloses a semiconductor function element, labeled as TPIN and TNIN in Figure 2c. (*Id.*) There is an electrically conductive connecting line connecting the terminal pad to the semiconductor function element in Figure 2c. (*Id.*)

Figure 2c discloses a protective element for protecting against electrostatic discharge, and the protective element is connected between the terminal pad and the semiconductor function element. (RX-205 at LSI-665-0061847-48; RX-774C at Q. 145; RDX-124.) Specifically, I find

that the protective element in Figure 2c comprises a thick field oxide device labeled "TFO," a series resistor, and a grounded gate NMOS device. (*Id.*) Maloney describes the TFO as "[t]he main protection device[.]" (RX-205 at LSI-337-665-0061848.) Maloney includes a first supply line being connected to the semiconductor function element. (RX-205 at LSI-665-0061847; RX-774C at Q. 145; RDX-124.) This is the line running from Vss (ground) to the semiconductor function element.

Maloney also includes the claimed second supply line, which is connected to the protective element and is electrically conductively connected to the first supply line, as both lines are connected to ground, Vss. (*Id.*) Finally, Maloney includes a clamp element for limiting a voltage to a clamp value. (*Id.*) The clamp element is labeled as TG2, and is connected to (1) the connecting line running between the terminal pad and the semiconductor function element; and (2) the first supply line. (*Id.*)

The only dispute between the parties is whether or not Figure 2c depicts two supply lines that are electrically conductively connected to each other, as required by claim 1. Mr. Fairbanks opines that there are two supply lines depicted in Maloney, while Dr. Cottrell opines that Figures 2b and 2c of Maloney show that the two "BUS R" labels represent resistance between circuit elements on a single wiring bus or on-chip track. (CX-1044C at Q. 31.)

Both parties focus on the following text from Maloney to support their conclusions:

> Circuit designers will often separate power and ground buses on internal circuitry from "noisy" pad driver buses, so that ***ground paths are returned to a common point (the Vss pad in this case) as shown in Fig. 2b.***

(RX-205 at LSI-337-665-0061847) (emphasis added.)

Qimonda and Dr. Cottrell state that Figure 2c of Maloney does not show a "pad driver," so there is no need for a separate ground bus. (CX-1044C at Q. 31.) Respondents argue that the

use of the plural "ground paths" demonstrates that there are two separate supply lines going to ground Vss.

I concur with Respondents. Both the figures and the text from Maloney clearly indicate that there are two separate conductive lines, one which goes from ground to the semiconductor function element, and another which goes from ground to the protective element. The above-quoted text of Maloney makes clear that there are multiple ground paths, demonstrating that there are two separate lines that connect to the ground potential Vss. While the quoted text refers to Figure 2b, Figure 2b is identical to Figure 2c, except that the clamp element TG2 is added in Figure 2c. (*Id.*) This change is not material to the above-quoted discussion, and thus I find that Maloney discloses multiple ground paths, which are the first and second supply lines.

The two lines each have their own bus resistance, which is depicted by the resistors "BUS R." (RX-205 at LSI-337-665-0061847.) Maloney makes clear that there are multiple buses (i.e. a first and second supply line) when it states that "[t]he ESD protection scheme as shown in Fig. 2a is an idelized one that does not recognize ***ground bus wiring resistances*** as shown in Fig. 2b." (*Id.*) (emphasis added).

In addition, Dr. Cottrell's analysis is based on an incorrect construction of "first supply line" and "second supply line." Dr. Cottrell states that the terms "should be properly interpreted to denote two on-chip conductor tracks being provided with the same supply potential, but spatially separated on-chip so that voltage fluctuations are decoupled." (CX-1044C at Q. 31.) As discussed *supra*, I construed "first supply line" and "second supply line" to mean "conductor track that carries a supply potential." I found that the claim did not require the additional language regarding voltage fluctuations, as this is discussed in the Background section of the specification when describing the prior art, and there is no indication that the claims should be so

limited. Thus, there is no requirement that voltage fluctuations are decoupled.

Claim 2 adds the requirement that there be at least one bond connection connecting the first and second supply lines together. I find that Maloney anticipates claim 2. Respondents identify the following language from Maloney:

> Circuit designers will often separate power and ground buses on internal circuitry from "noisy" pad driver buses, so that ground paths are returned to a common point (the Vss pad in this case) as shown in Fig. 2b. Sometimes this common point is on a lead frame and ***bond wire inductance*** also appears on each separate path.

(RX-205 at LSI-337-665-0061847) (emphasis added.)

Mr. Fairbanks testified that when Maloney mentions bond wire inductance on the path, it means that there is a bond wire connection between the supply lines. (RX-774C at Q. 147.) Otherwise, there would not be any bond wire inductance without a bond wire connection. (*Id.*) I find that the identified language in Maloney makes clear that the first and second supply lines may be connected via a bond connection. Qimonda does not address this language from Maloney, instead relying on its argument that Maloney does not disclose the claimed first and second supply lines. (CIB at 105-106; CX-1044C at Q. 32.) For the reasons discussed *supra*, I have found that Maloney discloses the claimed first and second supply lines.

Claim 3 is dependent on claim 2 and adds the following limitations: "wherein said semiconductor function element has a terminal, said at least one bond connection has a terminal, said first supply line has a portion disposed between said terminal of said semiconductor function element and said terminal of said at least one bond connection, and said clamp element is connected to said portion of said first supply line." I find that Figure 2c of Maloney discloses these additional limitations. (RX-205 at LSI-337-665-0061847; RX-774C at Q. 149; RDX-124.)

Qimonda argues that claim 3 requires a specific spatial arrangement, and that is not

shown by the simplified circuit schematic in Figure 2c of Maloney. (CIB at 105; CX-1044C at Q. 33.) Claim 3 adds limitations regarding connections between components. Contrary to Qimonda's assertion, it does not require a specific spatial arrangement. Figure 2c of Maloney clearly depicts the connections required by claim 3, and thus anticipates the claim. (RX-205 at LSI-337-665-0061847; RX-774C at Q. 149; RDX-124.)

Claim 4 depends from claim 1 and requires that the "semiconductor function element is connected to said first supply line and to said connecting line at a given location, and said clamp element has a first terminal connected to said first supply line and a second terminal connected to said connecting line, in the immediate spatial vicinity of said given location." I construed "immediate spatial vicinity" to mean "connected to the connecting line at a point in the connecting line that corresponds to the portion of the first supply line that is between (1) the connection of the first and second supply lines; and (2) the connection of the semiconductor function element to the first supply line." Respondents fail to offer evidence that Maloney discloses this limitation as properly construed based on the intrinsic evidence. I find that Maloney does not clearly disclose this limitation. (RX-205 at LSI-337-665-0061847.)

Claim 5 is dependent from claim 1 and adds the following limitation: "wherein said clamp element includes an MOS transistor having a main current path connected to said connecting line and to said first supply line and a gate terminal connected to said first supply line." Maloney clearly discloses this claim element. (RX-205 at LSI-337-665-0061847; RX-774C at Q. 152; RDX-124.) Qimonda and its expert fail to present any argument to the contrary, instead relying on their argument regarding claim 1. (CIB at 106.)

Claim 7 is dependent from claim 1 and adds the following limitation: "wherein said connecting line has a given resistance, said protective element includes a resistor connected

between said terminal pad and said semiconductor function element, and said resistor has a resistance being adjusted for setting a sum of the resistance of said resistor and the given resistance to a predetermined value." Mr. Fairbanks testifies that this is disclosed in Maloney because Maloney discloses a resistor connected between the terminal pad and the semiconductor function element, and Maloney states that the resistance of the resistor is set at "typically a few hundred ohms." (RX-774C at Q. 155; RX-205 at LSI-337-665-0061848.)

I find that Maloney fails to disclose the limitation described in claim 7. While Maloney calls for a resistor to be placed between the terminal pad and semiconductor function element, there is no discussion in Maloney about the resistor having a resistance being adjusted for setting a sum of the resistance of said resistor and the given resistance to a predetermined value. Maloney only states that the resistor is typically a few hundred ohms. (*See* CX-1044C at Q. 35.) Thus, Maloney fails to anticipate claim 7.

2. Krakauer-Mistry

Respondents' Position: Respondents contend that the paper titled "ESD Protection in a 3.3V Sub-Micron Silicided CMOS Technology," by David Krakauer and Kaizad Mistry, ELECTRICAL OVERSTRESS/ELECTROSTATIC DISCHARGE SYMPOSIUM PROCEEDINGS (Sept. 1992), at 250-257 ("Krakauer-Mistry") anticipates claims 1, 4, 5, 7, and 11 of the '434 patent. (RIB at 110.)

Respondents focus on Figure 7 from Krakauer-Mistry. Respondents assert that Krakauer-Mistry discloses a semiconductor component that includes a semiconductor body that has a terminal pad, a semiconductor function element, and an electrically conductive connecting line connecting the terminal to the semiconductor function element. (RIB at 111-112 (citing RX-774C at Q. 160; RX-188; RDX-125).) Respondents claim that Krakauer-Mistry discloses a

protective element for protecting against electrostatic discharge, with the protective element connected between the terminal pad and the semiconductor function element. (*Id.* at 112 (citing RX-774C at Q. 160; RX-188; RDX-125).)

Respondents argue that Krakauer-Mistry discloses a first supply line for the first supply potential (VSS), with first supply line connected to semiconductor function element. (RIB at 112 (citing RX-774C at Q. 160; RX-188; RDX-125).) According to Respondents, Figure 7 of Krakauer-Mistry discloses a second supply line for the first supply potential (VSS), with the second supply line connected to the protective element and electrically conductively connected to the first supply line. (*Id.* (citing RX-774C at Q. 160; RX-188; RDX-125).) Finally, Respondents claim that Figure 7 discloses a clamp element, which is connected to the connecting line and to the first supply line, for limiting a voltage applied to the clamp to a clamp value. (*Id.* (citing RX-774C at Q. 160; RX-188; RDX-125).)

Regarding claim 4, Respondents state that Krakauer-Mistry indicates that the clamp element should be connected to the first supply line close to the semiconductor function element, as the clamp element and the semiconductor function element share a common Vss symbol representing the first supply potential, whereas all other devices in Figure 7 connected by supply lines to the common supply potential have individual Vss symbols. (RIB at 113 (citing RX-774C at Q. 162; RX-188; RDX-125).) Additionally, according to Respondents, Krakauer-Mistry states that the clamp element in Figure 7 assists in protecting the semiconductor function element against Charged Device Model ("CDM") ESD events. (*Id.*) Respondents assert that one of ordinary skill in the art would appreciate that clamps that are meant to assist in CDM ESD protection must be placed close to the semiconductor function element they are meant to protect. (*Id.*)

Regarding claim 5, Respondents state that Figure 7 of Krakauer-Mistry discloses that the clamp element is a MOS device that has a main terminal connected to the first supply line and another main terminal connection to the connecting line , with the gate of the MOS device also connected to the first supply line. (RIB at 114 (citing RX-188).) Respondents claim that one of ordinary skill in the art would understand the reference to nMOST as a MOS device. (*Id.* (citing RX-774C at Q. 165; RX-188; RDX-125).)

Regarding claim 7, Respondents state that Figure 7 of Krakauer-Mistry discloses multiple resistances RI and RTC2. (RIB at 114 (citing RX-774C at Q. 166; RX-188; RDX-125).) Respondents assert that RI is part of the primary and secondary ESD protection structures, while RTC2 is part of the clamping element, including MTC2. (*Id.* (citing RX-774C at Q. 166; RX-188; RDX-125).) According to Respondents, the sum of the resistance values of RI and RTC2, and also the resistance of the connecting line is never arbitrarily chosen but always set to a predetermined value, or at least to a range of predetermined values. (*Id.* at 114-115 (citing RX-774C at Q. 166; RX-188; RDX-125).) Respondents state that if the sum of the resistance is not set appropriately, the resistors will fail. (*Id.* at 115 (citing RX-774C at Q. 166; RX-188; RDX-125).)

Regarding claim 11, Respondents state that Figure 11 of Krakauer-Mistry discloses typical bi-directional I/O [input/output] pin circuitry with ESD protection. (RIB at 115 (citing RX-774C at Q. 170; RX-188; RDX-126).) Respondents claim that Figure 11 comprises the "Input pin" configuration of Figure 7 plus two additional semiconductor function elements that form a classic CMOS output driver, which provide Input-Output or Bi-directional I/O capability at the Pin. (*Id.* (citing RX-774C at Q. 170; RX-188; RDX-126).) Respondents state that Semiconductor Function Elements MP1 and MN1 are output devices that are connected to the

terminal pad (PIN) by the connecting line and to the second supply line (flagged with the red line in the annotated figure, below). (*Id.* (citing RX-774C at Q. 170; RX-188; RDX-126).) According to Respondents, Semiconductor Function elements MP2 and MN2 are input stage devices as discussed above in regard to claim 1 and Fig. 7. (*Id.* (citing RX-774C at Q. 170; RX-188; RDX-126).)

In their reply brief, Respondents address Qimonda's arguments. Respondents argue that Qimonda attempts to improperly read limitations into claim 1 to save it from being found inval*id.* (RRB at 57.) Respondents reiterate that Krakauer-Mistry discloses two supply lines as depicted in RDX-125. (*Id.*)

In response to Qimonda's argument regarding claim 4, Respondents note that Krakauer-Mistry shows the clamp element MTC2 connected to the first supply line close to the semiconductor function element, and it states that the purpose of the clamp element is to "assist in protecting the semiconductor function element against CDM ESD events." (RRB at 58 (citing RX-188).) According to Respondents, one of ordinary skill in the art would know that clamps meant to assist in CDM ESD protection must be placed close enough to the semiconductor function element to provide effective protection. (*Id.* (citing RX-774C at Q. 162).)

Regarding claim 7, Respondents allege that Qimonda takes inconsistent positions when arguing infringement and validity. Specifically, Respondents state "when arguing invalidity, Qimonda contends that setting the value of one specific resistor does not address the sum of the resistance for the resistor and the connection line. Yet Qimonda takes a contrary position on infringement." (RRB at 59.)

Regarding claim 11, Respondents allege that Qimonda misreads the claim, as the claim requires an input switching stage, and not an output switching stage. Respondents state that

Krakauer-Mistry discloses an input stage or input buffer and an output buffer. (RRB at 59.) Respondents also claim that Qimonda is incorrect in arguing that Krakauer-Mistry does not disclose an output driver stage connected to the terminal pad and the second supply line. (*Id.* at 60 (citing RX-774C at Q. 169-170).)

Qimonda's Position: Qimonda argues that Krakauer-Mistry does not anticipate claims 1, 4, 5, 7, or 11. Regarding claim 1, Qimonda claims that Krakauer-Mistry does not describe the claim elements of "a first supply line for a first supply potential" and "a second supply line for the first supply potential . . . being electrically conductively connected to said first supply line." (CIB at 107 (citing CX-1044C at Q. 36, 37; CDX-38 at QAG-665-ITC-0233822).) According to Qimonda, a person of ordinary skill in the art at the time of filing of the '434 patent would have found no indications in Krakauer-Mistry that the various ground nodes collectively labeled "Vss" would be would be spatially arranged in any specific way, or coupled or decoupled in any specific fashion. (*Id.* (citing CX-1044C at Q. 37; CDX-38 at QAG-665-ITC-0233822. Qimonda contends that Krakauer-Mistry teaches only a single supply line, VSS, connected to ground. (*Id.* (citing RX-188 at LSI-337-665-0147597; CX-1044C at Q. 37; CDX-38 at QAG-665-ITC-0233822).)

In addressing the dependent claims, Qimonda argues that because Krakauer-Mistry does not anticipate claim 1, it does not anticipate any of the dependent claims. (CIB at 108-110).) Regarding claim 4, Qimonda argues that Krakauer-Mistry does not describe that "said semiconductor function element is connected to said first supply line and to said connecting line at a given location, and said clamp element has a first terminal connected to said first supply line and a second terminal connected to said connecting line, in the immediate spatial vicinity of said given location." (*Id.* at 108 (citing CX-1044C at Q. 38).) Qimonda asserts that the plain

meaning of the claim requires a specific spatial arrangement of circuit elements, which is not shown in Krakauer-Mistry. (*Id.* (citing CX-1044C at Q. 38).) Qimonda states that the reference in Krakauer-Mistry to Charged Device Model (CDM) ESD events does not teach any physical proximity, since physical proximity is only one of the many factors that determine the effectiveness of an ESD protection circuit. (*Id.* at 108-109 (citing CX-1044C at Q. 38).)[47]

Regarding claim 7, Qimonda argues that Krakauer-Mistry does not describe that "said connecting line has a given resistance, said protective element includes a resistor connected between said terminal pad and said semiconductor function element, and said resistor has a resistance being adjusted for setting a sum of the resistance of said resistor and the given resistance to a predetermined value." (CIB at 109 (citing CX-1044C at Q. 39).) Qimonda states that Krakauer-Mistry only teaches setting the value of the resistor R1 to a specific value (150 Ω) and does not address the sum of the resistance of the resistor and the connecting line. (*Id.* (citing CX-1044C at Q. 39).)

Regarding claim 11, Qimonda states that Krakauer-Mistry does not describe that "said semiconductor function element is an output switching stage, and including an output driver stage being connected to said terminal pad and to said second supply line." (CIB at 110 (citing CX-1044C at Q. 40).)

In its reply brief, Qimonda reiterates the argument that Krakauer-Mistry does not teach a "first supply line" and a "second supply line" as required by claim 1. (CRB at 51.) According to Qimonda, a person of ordinary skill in the art at the time of filing of the '434 patent would have found no indications in Krakauer-Mistry that the various ground nodes collectively labeled "Vss" would be would be spatially arranged in any specific way, or coupled or decoupled in any

[47] Qimonda does not raise any arguments unique to claim 5. Qimonda contends that because Krakauer-Mistry does not anticipate claim 1, it does not anticipate claim 5. (CIB at 109.)

specific fashion. (*Id.* (citing CX-1044C at Q. 37; CDX-38 at QAG-665-ITC-0233822).) Qimonda assert that Krakauer-Mistry teaches only a single supply line, VSS, connected to ground. (*Id.* (citing RX-188 at LSI-337-665-0147597; CX-1044C at Q. 37; CDX-38 at QAG-665-ITC-0233822).)

Commission Investigative Staff's Position: Staff argues that Krakauer-Mistry fails to anticipate claims 1, 4, 7, and 11 because it fails to clearly and convincingly disclose "a second supply line for the first supply potential…being electrically conductively connected to said first supply line" as required by claim 1. (SIB at 88.) Staff claims that when comparing Figure 7 of Krakauer-Mistry to Figure 3 of the '434 patent, it becomes apparent that Krakauer-Mistry does not clearly and convincingly disclose the above-quoted limitation. (*Id.* at 89.) Staff states that "Mr. Fairbanks' conclusion that this limitation is clearly and convincingly met based on Figure 7 of Krakauer-Mistry requires too big of an inferential leap and the application of impermissible hindsight to invalidate Claim 1." (*Id.*)

Discussion and Conclusion: Based upon the evidence before me, I find that Respondents have not clearly and convincingly demonstrated that Krakauer-Mistry anticipates any of the asserted claims of the '434 patent.

Krakauer-Mistry was published in 1992, meaning that it is prior art pursuant to 35 U.S.C. § 102(a), (b). (RX-188; JX-1.) Krakauer-Mistry was not before the examiner during the prosecution of the '434 patent. (JX-1; JX-2.)

Respondents focus on Figure 7 of Krakauer-Mistry, which is reproduced below:

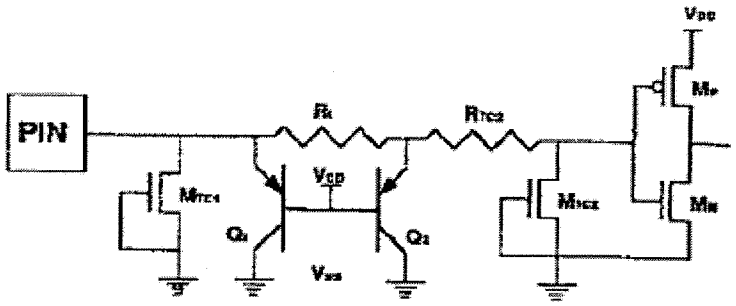


Figure 7: Typical 3.3V input pin with ESD protection.

(RX-188 at LSI-337-665-0147597.)

The only dispute between the parties is whether or not Figure 7 depicts two supply lines that are electrically conductively connected to each other, as required by claim 1. Mr. Fairbanks opines that Figure 7 depicts two supply lines that are electrically conductively connected to each other. (RX-774C at Q. 160.) Dr. Cottrell opines that this claim limitation is not met. (CX-1044C at Q. 37.) Dr. Cottrell states that the claim limitation should be interpreted to require two on-chip conductor tracks being provided with the same supply potential, but spatially separated on chip so that voltage fluctuations are decoupled. (*Id.*) Dr. Cottrell then states:

> Based on my experience, a person of ordinary skill at the time of filing of the '434 Patent would have found no indications in the Krakauer-Mistry paper reference that the various ground nodes collectively labeled "Vss" would be would be [*sic*] spatially arranged in any specific way, or coupled or decoupled in any specific fashion.

(*Id.*)

Claim 1 requires two separate supply lines: the first supply line and the second supply line. It is undisputed that because the claim calls for two separate supply lines, the supply lines must be spatially separated. (CIB at 64; RIB at 78.) Figure 7 does not clearly and convincingly disclose two separate supply lines. Figure 7 merely shows the alleged protective element, clamp element, and semiconductor function element all connected to a common ground. (RX-188 at

LSI-337-665-0147597.) Nothing demonstrates that there are separate first and second supply lines running from ground to the elements as called for in claim 1. Mr. Fairbanks' demonstrative artificially creates two separate supply lines, labeled in red and green, but this goes beyond the disclosure of Krakauer-Mistry. (RDX-125.) Thus, Respondents have failed to prove that Krakauer-Mistry anticipates the asserted claims.[48]

3. Strauss-White

Respondents' Position: Respondents contend that the paper "Protecting N-Channel Output Transistors from ESD Damage," by Mark S. Strauss and Marvin H. White, ELECTRICAL OVERSTRESS/ELECTROSTATIC DISCHARGE SYMPOSIUM PROCEEDINGS (Sept., 1991), at 110-119 ("Strauss-White") anticipates claims 1, 4, 7, and 11 of the '434 patent. (RIB at 116.)

Regarding claim 1, Respondents state that Strauss-White discloses a semiconductor component. (RIB at 116 (citing RX-774C at Q. 175; RX-187; RDX-127).) Respondents state that one of ordinary skill in the art would have understood Strauss-White to disclose a semiconductor body that has a terminal pad, a semiconductor function element, and an electrically conductive connecting line connecting the terminal to the semiconductor function element. (*Id.* at 117 (citing RX-774C at Q. 175; RX-187; RDX-127).)

Respondents point to Figure 2 of Strauss-White and state that it discloses a protective element for protecting against electrostatic discharge, with the protective element connected between the terminal pad and the semiconductor function element. (RIB at 118 (citing RX-774C at Q. 175; RX-187; RDX-127).) According to Respondents, Figure 2 of Strauss-White also discloses a first supply line for the first supply potential (VSS), with the first supply line

[48] Claim 1 is independent, and all of the other asserted claims in the '434 patent are dependent on claim 1. Thus, these claims are not anticipated by Krakauer-Mistry for the same reasons that claim 1 is not anticipated by Krakauer-Mistry. *In re Fritch,* 972 F.2d 1260, 1266 (Fed. Cir. 1992); *In re Royka,* 490 F.2d 981, 983-985 (C.C.P.A. 1974).

connected to semiconductor function element. (*Id.* (citing RX-774C at Q. 175; RX-187; RDX-127).) Respondents next state that Figure 2 of Strauss-White discloses a second supply line for the first supply potential (VSS), with the second supply line connected to the protective element and electrically conductively connected to the first supply line. (*Id.* (citing RX-774C at Q. 175; RX-187; RDX-127).) Lastly, Respondents state that Figure 2 of Strauss-White discloses a clamp element that is connected to the connecting line and to the first supply line, for limiting a voltage applied to the clamp element to a clamp value. (*Id.* at 118-119 (citing RX-774C at Q. 175; RX-187; RDX-127).)

Regarding claim 4, Respondents claim that Strauss-White expressly discloses that the clamp element should be connected to the first supply line close to the semiconductor function element, as the clamp element and the semiconductor function element are both identified as subcomponents of a greater input circuitry block. (RIB at 119 (citing RX-774C at Q. 177; RX-187; RDX-127).) Thus, according to Respondents, Strauss-White discloses that the clamp element is placed within the immediate spatial vicinity of the semiconductor function element. (*Id.*)

Regarding claim 7, Respondents state that Figure 2 of Strauss-White discloses multiple resistances, which they label R1, R2 and R3. (RIB at 120.) According to Respondents, R1 and R2 are "input resistors" that are sized to a value of 200 ohms. (*Id.* (citing RX-774C at Q. 180; RX-187; RDX-128). Respondents state that one of ordinary skill in the art would appreciate that the total sum of the resistance values of R1 and R2, and also the resistance of the connecting line should not be arbitrarily chosen but should be set to at least a minimum predetermined value to ensure that the secondary ESD devices can properly protect the input device without degrading normal circuit operation. (*Id.* (citing RX-774C at Q. 180; RX-187; RDX-128).)

Regarding claim 11, Respondents claim that Figure 2 of Strauss-White discloses a bi-directional I/O configuration. (RIB at 121 (citing RX-774C at Q. 181; RX-187; RDX-0127; RDX-0128).) According to Respondents, Figure 2 of Strauss-White clearly shows "Output Transistors" that form the output driver circuitry. (*Id.* (citing RX-774C at Q. 181; RX-187; RDX-0127; RDX-0128).) Respondents state that Figure 2 output devices that are connected to the terminal pad by a connecting line and to the said second supply line. (*Id.* (citing RX-774C at Q. 181; RX-187; RDX-0127; RDX-0128).) Respondents further assert that Figure 2 discloses input stage devices. (*Id.* (citing RX-774C at Q. 181; RX-187; RDX-0127; RDX-0128).)

Qimonda's Position: Qimonda contends that Strauss-White does not anticipate claims 1, 4, 7, or 11. With respect to claim 1, Qimonda states that Strauss-White does not teach the claim elements of "a first supply line for a first supply potential" and "a second supply line for the first supply potential . . . being electrically conductively connected to said first supply line." (CIB at 110 (citing CX-1044C at Q. 42; CDX-38 at QAG-665-ITC-0233823).) According to Qimonda, a person of ordinary skill in the art at the time of filing of the '434 patent would have found no indications in Strauss-White that the various ground nodes collectively labeled "Vss" would be spatially arranged in any specific way, or coupled or decoupled in any specific fashion. (*Id.* (citing CX-1044C at Q. 42; CDX-38 at QAG-665-ITC-0233823).) Qimonda asserts that Strauss-White describes only a single supply line, VSS, connected to ground. (*Id.* (citing CX-1044C at Q. 42; CDX-38 at QAG-665-ITC-0233823).)

In addressing the dependent claims, Qimonda argues that because Strauss-White does not anticipate claim 1, it does not anticipate any of the dependent claims. (CIB at 111-113.) Regarding claim 4, Qimonda contends that Strauss-White does not describe that "said semiconductor function element is connected to said first supply line and to said connecting line

at a given location, and said clamp element has a first terminal connected to said first supply line and a second terminal connected to said connecting line, in the immediate spatial vicinity of said given location." (CIB at 111 (citing CX-1044C at Q. 43).) Qimonda states that Mr. Fairbanks asserts that this claim element is met because the circuit elements labeled "INPUT PROTECTION CIRCUITRY" AND "INPUT BUFFER" in Fig. 2 of Strauss-White share the common word "INPUT." (*Id.* (citing CX-1044C at Q. 43).) According to Qimonda, "[i]t is unreasonable to assert that a person of ordinary skill in the art at the time of the filing of the '434 patent would conclude from mere commonality of terminology that those circuit elements are identified as sub-components of a greater input circuitry block." (*Id.* at 111-112 (citing CX-1044C at Q. 43).)

Regarding claim 7, Qimonda asserts that Strauss-White does not describe that "said connecting line has a given resistance, said protective element includes a resistor connected between said terminal pad and said semiconductor function element, and said resistor has a resistance being adjusted for setting a sum of the resistance of said resistor and the given resistance to a predetermined value." (CIB at 112 (citing CX-1044C at Q. 44).) Qimonda states that Strauss-White only teaches setting the value of an unspecified "input protection resistor" to a specific value (200 Ω), and does not address the sum of the resistance of the resistor and the connecting line. (*Id.* (citing CX-1044C at Q. 44).)

Regarding claim 11, Qimonda contends that Strauss-White does not describe that "said semiconductor function element is an output switching stage, and including an output driver stage being connected to said terminal pad and to said second supply line." (CIB at 112-113 (citing CX-1044C at Q. 45).)

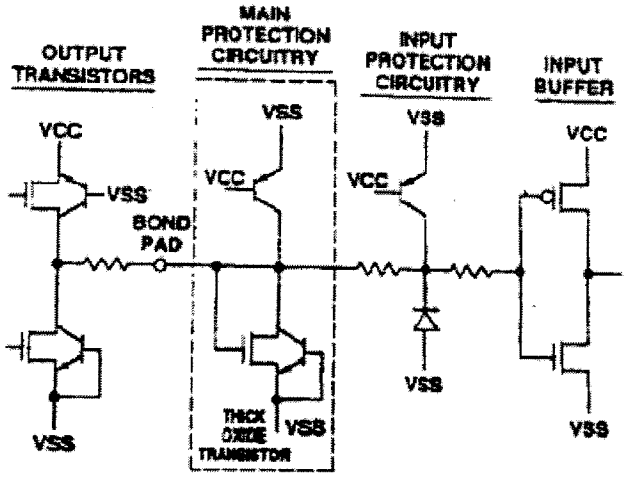
Commission Investigative Staff's Position: Staff argues that Strauss-White fails to

anticipate claims 1, 4, 6, 7, and 11 because it fails to clearly and convincingly disclose "a second supply line for the first supply potential…being electrically conductively connected to said first supply line" as required by claim 1. (SIB at 89.) Staff claims that "[f]or the reasons detailed above regarding Krakauer-Mistry, Staff does not believe that the Strauss-White [*sic*] clearly and convincingly discloses Claim 1's requirement of 'a second supply line for the first supply potential…being electrically conductively connected to said first supply line.'" (*Id.* at 90.)

Discussion and Conclusion: Based upon the evidence before me, I find that Respondents have not clearly and convincingly demonstrated that Strauss-White anticipates any of the asserted claims of the '434 patent.

Strauss-White was published in 1991, meaning that it is prior art pursuant to 35 U.S.C. § 102(a), (b). (RX-187; JX-1.) Strauss-White was not before the examiner during the prosecution of the '434 patent. (JX-1; JX-2.)

Respondents focus on Figure 2 of Strauss-White, which is reproduced below:



I/O PAD SCHEMATIC DIAGRAM
FIGURE 2

(RX-187 at LSI-337-665-0064296.)

The only dispute between the parties is whether or not Figure 2 depicts two supply lines

that are electrically conductively connected to each other, as required by claim 1. Mr. Fairbanks opines that Figure 7 depicts two supply lines that are electrically conductively connected to each other. (RX-774C at Q. 175.) Dr. Cottrell opines that this claim limitation is not met. (CX-1044C at Q. 42.) Dr. Cottrell states that the claim limitation should be interpreted to require two on-chip conductor tracks being provided with the same supply potential, but spatially separated on chip so that voltage fluctuations are decoupled. (*Id.*) Dr. Cottrell then states:

> Based on my experience, a person of ordinary skill at the time of filing of the '434 Patent would have found no indications in the Strauss-White paper that the various ground nodes collectively labeled "Vss" would be spatially arranged in any specific way or coupled or decoupled in any specific fashion.

(*Id.*)

Claim 1 requires two separate supply lines: the first supply line and the second supply line. It is undisputed that because the claim calls for two separate supply lines, the supply lines must be spatially separated. (CIB at 64; RIB at 78.) Figure 2 does not clearly and convincingly disclose two separate supply lines. Figure 2 merely shows the alleged protective element, clamp element, and semiconductor function element all connected to a common node, Vss. (RX-187 at LSI-337-665-0064296.) Nothing demonstrates that there are separate first and second supply lines running from ground to the elements as called for in claim 1. Mr. Fairbanks' demonstrative artificially creates two separate supply lines, labeled in red and green, but this goes beyond the disclosure of Strauss-White. (RDX-127.) Thus, Respondents have failed to prove that Strauss-White anticipates the asserted claims.[49]

4. Maloney In Combination With One or More Other References

Respondents' Position: Respondents contend that claims 1, 2, 3, 5, 7, 8, and 11 are

[49] Claim 1 is independent, and all of the other asserted claims in the '434 patent are dependent on claim 1. Thus, these claims are not anticipated by Strauss-White for the same reasons that claim 1 is not anticipated by Strauss-White. *In re Fritch,* 972 F.2d 1260, 1266 (Fed. Cir. 1992); *In re Royka,* 490 F.2d 981, 983-985 (C.C.P.A. 1974).

obvious in view of Maloney, alone or in combination with one or more additional references. (RIB at 121.)

Respondents first argue that Maloney, alone or in combination with U.S. Patent No. 5,394,008 to Ito et al. ("Ito") renders claim 2 obvious. Respondents note that Maloney discloses the following: "[C]ircuit designers will often separate power and ground buses on internal circuitry from 'noisy' pad driver buses, so that ground paths are retuned to a common point the VSS pad in this case . . . . Sometimes this common point is on a lead frame and bond wire inductance also appears on each separate path." (RIB at 122 (citing RX-774C at Q. 190; RX-205 at 221-222, Fig.2c; RDX-124; Tr. at 1550:10-25).) Respondents argue that while Maloney does not expressly show a bond connection, the paper explains that there can be bond wire inductances (which can only occur if there are bond wire connections) between the bus and the frame or similar package pin connections. (*Id.* (citing RX-774C at Q. 190; RX-205 at 221-222, Fig.2c; RDX-124; Tr. at 1550:10-25).)

Respondents assert that one of ordinary skill in the art would have appreciated that each "Bus R" in Figure 2c of Maloney represents various parasitics of ground bus paths, which typically included wire resistances, bond connections, lead frame resistances, and the like. (RIB at 122 (citing RX-774C at Q. 190; RX-205 at 221-222, Fig.2c; RDX-124; Tr. at 1550:10-25).) According to Respondent, before 1995, one of ordinary skill in the art would have known that a bond connection could be used between the first and second supply lines even though a bond connection is not shown in Fig. 2c. (*Id.* (citing RX-774C at Q. 190; RX-205 at 221-222, Fig.2c; RDX-124; Tr. at 1550:10-25).)

Respondents claim that Ito discloses devices, including lead frames and methods for connecting power supply lines for semiconductor circuitry, and their ESD implications. (RIB at

122 (citing RX-774C at Q. 190; RX-257).) Respondents assert that Ito describes the use of bond wire connections in many different arrangements and configurations to achieve different results, including isolating noise and power surges between different on-chip domains or supplies. (*Id.* at 122-123 (citing RX-774C at Q. 190; RX-257 at 3:50-66, 5:11-26, 7:33-68, 8:1-25, claim 22).) Respondents argue that Figure 5 of Ito shows a bond wire connection between first and second supply lines. (*Id.* at 123 (citing RX-774C at Q. 190; RX-257).)

Respondents claim that since before 1995 designers had been looking for ways to separate noise, surges, and other unwanted electrical energy between on-chip circuit blocks for many years. Respondents argue that Ito explicitly describes techniques to do this through package design and wire bonding configurations. (RIB at 123 (citing RX-774C at Q. 190; JX-1; RX-205; RX-257).) Thus, Respondents conclude that one of ordinary skill in the art would have been motivated by design choice to combine the circuitry disclosed in Figure 2c of Maloney with one of the lead frames disclosed in Ito to provide a packaged semiconductor integrated circuit including ESD protection with at least one bond connection connecting the first supply line and the second supply line. (*Id.* (citing RX-774C at Q. 190; RX-205; RX-257).)

Respondents contend that Maloney, alone or in combination with Ito and the admitted prior art renders claim 3 obvious. (RIB at 123-124.) Respondents claim that Ito discloses that at least one bond connection between a first supply line and a second supply line was well known before the '434 Patent application was filed. (*Id.* at 124 (citing RX-774C at Q. 190; RX-257 at 3:50-66, 5:11-26, 7:33-68, 8:1-25, claim 22).) Respondent argue that it would have been obvious to one of ordinary skill in the art to combine the circuitry disclosed in Maloney with one of the lead frames disclosed in Ito to provide a packaged semiconductor integrated circuit

including at least one bond connection connecting a first supply line and a second supply line as called for by claim 2. (*Id.* (citing RX-774C at Q. 190; RX-205; RX-257).)

Respondents note that the '434 patent admits that using multiple conductive paths for supplying power to semiconductor circuitry and using bond connections was well known. (RIB at 124 (citing RX-774C at Q. 133; JX-1, at 1:22-61).) Respondents argue that it would have been obvious to one of ordinary skill in the art to combine the circuitry disclosed in Maloney with the applicants' admitted prior art to provide a semiconductor body including at least one bond connection connecting a first supply line and a second supply line as called for by claim 2. (*Id.* (citing RX-774C at Q. 190; RX-205; JX-1).)

Respondents contend that the combination of Maloney and U.S. Patent No.5,034,845 to Murakami ("Murakami") renders claim 8 obvious. Respondents state that Murakami shows that replicating ESD protection circuitry as needed throughout a semiconductor integrated circuit was well known before the '434 patent. (RIB at 125 (citing RX-774C at Q. 194; RX-222 at Figs.4-6).) According to Respondents, it would have been an obvious design choice to replicate the design tactics called for by claim 7 - that is, to specially adjust total resistances between the terminal pad and a multiplicity of semiconductor function elements - to arrive at all of the elements of claim 8. (*Id.* (citing RX-774C at Q. 194; RX-222 at Figs.4-6).)

Respondents contend that claim 11 is obvious in view of Maloney and Krakauer-Mistry. As to the additional limitations of claim 11, Respondents state that Maloney discloses that "the same sort of pi network scheme [for protecting the input switching stage TPin, TNin, as shown in Fig. 2c] can be used for an I/O pin. The TFO device is simply replaced by an output buffer, for which a self-protecting NMOS pull-down is the principal ESD protection device." (RIB at 125 (citing RX-774C at Q. 196; RX-205).) Respondents aver that although Maloney teaches that the

TFO may be omitted from an I/O ESD protection configuration, this is merely one alternative way of providing ESD-protected I/O. (*Id.* (citing RX-774C at Q. 196; RX-205 at 222).) Respondents argue that simply connecting an output driver stage to an input ESD protection configuration to provide ESD-protected I/O capability without removing anything was also well known in the art before the '434 patent. (*Id.* at 125-126 (citing RX-774C at Q. 196; RX-188; RX-126; RX-129).) Respondents offer a schematic in an attempt to show that Maloney combined with the output driver stage disclosed in Krakauer-Mistry discloses all of the elements of claim 11. (*Id.* at 126 (citing RX-774C at Q. 196; RDX-129; RX-205).)

Respondents note that if a dependent claim is rendered obvious then the corresponding base claim is necessarily obvious as well. (RIB at 126 (citing *Ormco Corp. v. Allesee Orthodontic Appliances, Inc.*, 498 F.3d 1307, 1319 (Fed. Cir. 2007)).) Respondents allege that each of the asserted dependent claims 2, 3, 4, 5, 7, 8, and 11 was obvious to one of ordinary skill in the art at the time of the claimed invention. Claim 1 is the base claim from which all of claims 2, 3, 4, 5, 7, 8, and 11 depend, either directly or indirectly. Thus, Respondents assert that for the various reasons discussed in connection with each of claims 2, 3, 4, 5, 7, 8, and 11, claim 1 is also obvious. (*Id.* at 127.)

In their reply brief, Respondents dispute Qimonda's contention that the elements labeled "BUS R" in Fig. 2c of Maloney would have been interpreted as two internal buses connected on-chip. (RRB at 63.) Respondents state that a person of ordinary skill in the art would not have interpreted the separate supply lines labeled "BUS R" as two internal buses connected on-chip because Maloney expressly teaches that the two supply lines (ground paths) are returned to a common point (the VSS pad) and that "[s]ometimes this common point is on a lead frame [i.e., off-chip] and bond wire inductance appears on each separate path." (*Id.* (citing RX-205C at 222,

Fig. 2c).) Respondents argue that this indicates that the two supply lines are connected to a common point off-chip by a bond-wire connection. (*Id.* (citing RX-774C at Q. 190).)

Respondents reiterate that Ito discloses lead frames and methods for connecting power supply lines for semiconductor circuits and discusses their ESD implications. (RRB at 63 (citing RIB at 122).) Respondents claim that Ito also expressly discusses the use of bond-wire connections in the context of isolating noise and power surges between different circuit elements. (*Id.* (citing RIB at 122-23).)

Respondents conclude that because Maloney teaches connection of first and second supply lines off-chip using bonding wires, one skilled in the art, reading Maloney and searching for ways to isolate noise and power surges between different circuit elements (as the inventors of the '434 patent were doing) would be motivated to look at Ito and would find ways of connecting first and second supply lines using bond-wire connections in a lead frame or package. (RRB at 63 (citing RIB at 123).)

Respondents dispute Qimonda's contention that Murakami does not teach the equalization of signal delays across signal lines, but focuses only on the protection features of the circuitry and not on the signal delays. (RRB at 64.) Respondents aver that equalization of signal delays has nothing to do with claim 8. (*Id.* (citing JX-1).) Thus, Respondents argue that Qimonda's argument is irrelevant. According to Respondents, if one were seeking to replicate an ESD protection circuit in a semiconductor device having multiple protective elements, one would naturally be motivated to look to a reference like Murakami, which shows how to adjust the total resistance between the terminal pad and a multiplicity of semiconductor function elements to arrive at all of the element of claim 8. (*Id.* (citing RIB at 125).)

Qimonda's Position: Qimonda argues that the claims of the '434 patent are not obvious

in view of the combination of Maloney and other prior art references. (CIB at 113.)

Regarding the combination of Maloney and Ito, Qimonda states that Maloney does not disclose each and every element of claims 1, 2, or 3 of the '434 patent. (CIB at 113 (citing CX-1044 at Q. 51).) Qimonda argues that, to a person with ordinary skill in the art, the elements labeled "BUS R" in Figure 2c of Maloney would have been interpreted as two internal buses connected on-chip. (*Id.* (citing CX-1044 at Q. 51).) Therefore, according to Qimonda, a person of ordinary skill would not have had any reason to combine the teachings of Maloney with those of Ito. (*Id.* (citing CX-1044 at Q. 51).) Qimonda concludes that the combination of Maloney and Ito does not render claims 2 or 3 obvious.

Regarding the combination of Maloney and Murakami, Qimonda argues that such a combination fails to disclose every element of claim 8. (CIB at 113 (citing CX-1044 at Q. 52).) Qimonda asserts that Maloney does not disclose each and every element of claims 1 or 8 of the '434 patent. (*Id.* at 114 (citing CX-1044 at Q. 52).) Qimonda claims that the '434 patent discloses the equalization of signal propagations through design of the ESD protection circuitry. (*Id.* (citing CX-1044 at Q. 52).) According to Qimonda, Murakami does not teach the equalization of signal delays across signal lines, but rather focuses only on the protection features of the circuitry and not on the signal delays. (*Id.* (citing CX-1044 at Q. 52).) As a result, Qimonda states that claim 8 is valid in view of Maloney combined with Murakami.

Regarding the combination of Maloney and Krakauer-Mistry, Qimonda argues that such a combination fails to disclose all of the elements of claim 11. (CIB at 114 (citing CX-1044 at Q. 53).) Qimonda previously argued that Maloney and Krakauer-Mistry each do not disclose every element of claim 1 of the '434 patent. (*Id.* (citing CX-1044 at Q. 53).) Qimonda argues that Maloney expressly teaches away from the combination of the teachings of Fig. 2c with an

output driver stage. (*Id.* (citing CX-1044 at Q. 53).) Maloney states that "[t]he scheme shown in Fig. 2 is for protection of an input buffer when the pin is intended for use as an input-only." (*Id.* (citing RX-205 at LSI-337-665-0061847-61848; CX-1044 at Q. 53).) Further, Maloney states that "[t]he same sort of pi network scheme can be used for an input/output (I/O) pin. The TFO device is simply replaced by an output buffer, for which a self-protecting NMOS pulldown is the principal ESD protection device." (CIB at 114 (citing RX-205 at LSI-337-665-0061847-61848; CX-1044 at Q. 53).) Qimonda claims that such language would have strongly discouraged a person of ordinary skill in the art from combining the circuit of Fig. 2c of the Maloney paper with any output circuit, without first removing the TFO element, which Mr. Fairbanks identifies as the "protective element" required by all the claims of the '434 patent. (*Id.* at 114-115 (citing CX-1044 at Q. 53).)

Qimonda claims that Mr. Fairbanks has incorrectly asserted that although Maloney teaches that the TFO may be omitted from an I/O ESD protection configuration, this is merely one alternative way of providing ESD-protected I/O. (CIB at 115 (citing CX-1044 at Q. 53).) Qimonda argues that a person of ordinary skill in the art would have had to go against the express instructions of Maloney to keep the TFO when hypothetically adding an output driver stage to the circuit of Fig. 2c of Maloney. (*Id.* (citing CX-1044 at Q. 53).)

In its reply brief, Qimonda argues that none of the obviousness references relied on by Respondents teaches the "first supply line" and "second supply line" as required by claim 1. (CRB at 52.) In addition, Qimonda notes that Respondents have failed to assert that claim 1 is obvious. (*Id.*)

Commission Investigative Staff's Position: Staff contends that the asserted claims are not obvious in light of any of the proposed prior art combinations. (SIB at 90-91.) Staff does

not believe that claim 1 is anticipated by any of the prior art references, and Respondents do not raise an obviousness challenge with respect to claim 1. (*Id.* at 91.) Staff states that "[t]he asserted combinations also do not clearly and convincingly disclose elements of the listed dependent claims including, among other limitations, the "immediate spatial vicinity" requirement in dependents Claim 4." (*Id.*)

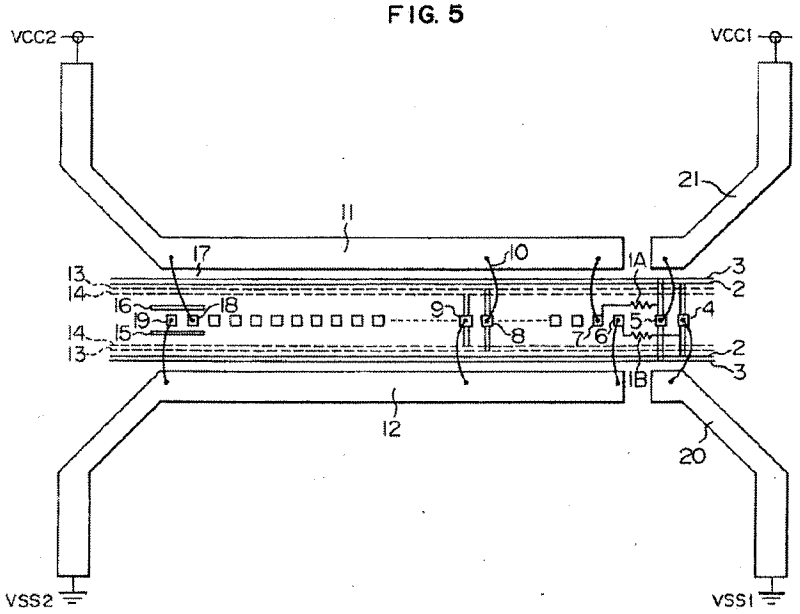
Discussion and Conclusion: Based on the evidence before me, I find that if Maloney is found not to anticipate claims 2 and 3, then the combination of Maloney and Ito renders claims 2 and 3 obvious.[50] I find that the combination of Maloney and Murakami fails to render claim 8 obvious. I find that the combination of Maloney and Krakauer-Mistry fails to render claim 11 obvious.

Respondents claim that Maloney discloses the bond connections required in claims 2 and 3. I concurred, for the reasons described *supra*. Respondents offer the alternative argument that if Maloney is not found to disclose the required bond connections, the combination of Maloney and Ito renders claims 2 and 3 obvious.

Ito is a prior art patent entitled "Semiconductor Integrated Circuit Device." (RX-257.) It was not cited during the prosecution of the '434 patent. (JX-1.) Ito discloses bond connections between buses and bonding pads through the use of bond wires. For example, this is shown in Figure 5:

[50] Based on the testimony of the experts, I find that the level of ordinary skill in the art at the time of invention was a bachelor's degree in electrical engineering and at least two years of industry experience in the field of ESD protection. (CX-1044C at Q. 9; RX-774C at Q. 186.)

FIG. 5



(RX-257 at Fig. 5.) Ito discusses how the use of bond wires, among other things, helps to suppress potential voltage fluctuations and prevent noise generated at the output circuit from entering the input circuits. (*See, e.g., Id.* at 7:41-8:11.) Thus, Ito was concerned with the same problems discussed and addressed in the '434 patent. (RX-774C at Q. 190.)

Because Ito taught the use of bond wire connections in circuits for the purpose of suppressing voltage fluctuations and preventing noise, I find that it would have been obvious to one of ordinary skill in the art to combine the teaching of Ito with the ESD design of Maloney to result in the inventions claimed in claims 2 and 3. *See KSR*, 550 U.S. at 417 ("[I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.") This conclusion is further supported by Mr. Fairbanks' testimony regarding the combination of Maloney and Ito. (RX-774C at Q. 190.)

Dr. Cottrell's opinion regarding the combination of Maloney and Ito is limited to arguing that Maloney does not disclose all of the elements of claim 1. (CX-1044C at Q. 51.) As

described *supra*, I have already found that Maloney anticipates claim 1. Thus, Dr. Cottrell fails to offer any opinion to contradict the conclusion that the combination of Maloney and Ito renders claims 2 and 3 obvious.[51]

Respondents claim that Maloney and Murakami render claim 8 obvious. Claim 8 is dependent on claim 7, which is in turn dependent on claim 1. Respondents' argument is premised on the conclusion that Maloney anticipates of claim 7, and Murakami discloses the additional limitations of claim 8. (RIB at 124-125.) Because I have found *supra* that Maloney does not anticipate claim 7, I find that Respondents cannot demonstrate that the combination of Maloney and Murakami renders claim 8 obvious.

Respondents claim that Maloney and Krakauer-Mistry render claim 11 obvious. Claim 11 requires the addition of an output driver stage being connected to the terminal pad and to the second supply line. Mr. Fairbanks opines that Maloney discloses that the circuit in Figure 2c may be reconfigured for input/output. (RX-774C at Q. 196.) Mr. Fairbanks states that Krakauer-Mistry discloses an output driver stage which could be added to the schematic in Figure 2c of Maloney to result in claim 11. (*Id.*)

Mr. Fairbanks' opinion relies on adding the output driver stage and leaving the TFO from Maloney. Maloney states:

> The same sort of pi network scheme can be used for an input/output (I/O) pin. The TFO device is simply replaced by an output buffer, for which a self-protecting NMOS pulldown is the principal ESD protection device. Special design considerations apply for p-well CMOS, where NMOS devices are in a p-well.

(RX-205 at LSI-337-665-0061847.)

Thus, Maloney clearly contemplates removal of the TFO when adding an output buffer. The TFO serves as the protective element of Maloney. Mr. Fairbanks opines that the TFO of

[51] I note that neither party raises any objective indicia of non-obviousness regarding the '434 patent.

Maloney may be left in place while the output driver stage of Krakauer-Mistry is added, but there is no support in Maloney for such a proposition. (RX-774C at Q. 196; CX-1044C at Q. 53.) Thus, I find that Respondents fail to demonstrate that claim 11 is rendered obvious by the combination of Maloney and Krakauer-Mistry.[52] I further note Dr. Cottrell's opinion that simply adding the output driver stage from Krakauer-Mistry to the circuit disclosed in Maloney is not as simple as Mr. Fairbanks makes it appear, and there is no guarantee that the combined circuit would work properly. (CX-1044C at Q. 53.)

5. Krakauer-Mistry In Combination With Maloney, Ito, or Admitted Prior Art

Respondents' Position: Respondents contend that claims 1, 2, 3, 8, and 11 are obvious in view of Krakauer-Mistry in combination with Maloney, Ito, or the admitted prior art. (RIB at 127.)

Regarding claims 2 and 3, Respondents argue that it would have been an obvious design choice for one of ordinary skill in the art to combine the ground path teachings, including bond connections, of Maloney, Ito, or the prior art admitted in the '434 patent to the ESD protection circuitry disclosed in Krakauer-Mistry to provide a semiconductor component meeting all of the claim limitations. (RIB at 127 (citing RX-774C at Q. 197).)

Regarding claim 11, Respondents claim that Dr. Cottrell admitted that, in view of Maloney, a bi-directional input/output ("I/O") circuit including "a 'pad driver' (i.e., an output buffer) . . . would necessitate a separate ground buss" for the pad driver circuitry as opposed to the ground bus (i.e., supply line) for the internal circuitry. (RIB at 127 (citing CX-1044C at Q. 31).) Respondents state that Figure 11 of Krakauer-Mistry shows the "Input pin" configuration of Figure 7 with two additional semiconductor function elements that form a classic CMOS

[52] While the above-quoted text from Maloney discusses a new principal ESD protection device when the output buffer is added, Respondents present no argument or opinion that this new device will function as the claimed protective element.

output driver, which provide Input/Output or Bi-directional I/O capability at the pin. Respondents further state that semiconductor function elements MP1 and MN1 are output devices that are connected to the terminal pad PIN by a connecting line and to the second supply line. According to Respondents, semiconductor function elements MP2 and MN2 are input stage devices. (*Id.* (citing RX-774C at Q. 170; RX-188; RDX-126).) Respondents argue that from the teachings of Krakauer-Mistry in view of the teachings of Maloney, it would have been an obvious design choice for one of ordinary skill in the art, before 1995, to provide a semiconductor integrated circuit device including ESD-protected bi-directional I/O circuitry according to Figure 11 of Krakauer-Mistry, with a first supply line for the ground supply potential for MTC2 and MN2 and with a separate, second supply line for the ground supply potential for MTC1, Q1, and MN1. (*Id.* at 127-128 (citing RX-774C at Q. 196; RX-188 at Fig.11; RX-205 at 222, Fig.2c; RDX-129; RDX-126).)

In their reply brief, Respondents address Qimonda's argument that Maloney teaches away from combining the circuit in Figure 2c with any output circuit without first removing the TFO element. (RRB at 64.) Respondents argue that although Maloney teaches that the TFO may be omitted, Figure 11 of Krakauer-Mistry teaches that the output driver can be added and the protective element can be retained. (*Id.* (citing RIB at 125-126).) According to Respondents, Figure 11 of Krakauer-Mistry teaches that you can add an output driver, connected between the terminal pad and second supply line to the Maloney circuit to get an ESD-protected I/O configuration as described in claim 11. (*Id.* at 64-65 (citing RIB at 126; RDX-129).) Respondents also reiterate that Krakauer-Mistry discloses separate supply lines, contrary to Qimonda's assertion otherwise. (*Id.* at 65 (citing RIB at 111-112).)

Qimonda's Position: Qimonda argues that Krakauer-Mistry in combination with

Maloney or Ito does not disclose every limitation of claims 2, 3, and 8. (CIB at 115 (citing CX-1044 at Q. 54).) Qimonda claims that Mr. Fairbanks appears to suggest that a person of ordinary skill in the art would have found it obvious to combine the purported ground path teachings, including bond connections, of Maloney and/or Ito with the teaching of Krakauer-Mistry to render claims 2 and 3 obvious. (*Id.* (citing CX-1044 at Q. 54).) Qimonda asserts that Mr. Fairbanks does not provide a detailed discussion of why such combination would have been obvious. (*Id.* (citing CX-1044 at Q. 54).) Qimonda states that such combination would not have been obvious, at least because Krakauer-Mistry does not discuss the use of separate supply lines, and therefore such purported "ground path teachings" would have been irrelevant to a person applying the teachings of Krakauer-Mistry. (*Id.* at 115-116 (citing CX-1044 at Q. 54).)

Qimonda asserts that Mr. Fairbanks appears to suggest that a person of ordinary skill in the art would have found it an obvious design choice to replicate the circuitry disclosed in Krakauer-Mistry to render claim 8 obvious. (CIB at 116 (citing CX-1044 at Q. 54).) Again, Qimonda states that Mr. Fairbanks does not provide a detailed discussion of why such combination would have been obvious. (*Id.* (citing CX-1044 at Q. 54).) According to Qimonda, such a combination would not have been obvious, at least because the '434 patent discloses and claims much more than mere "replication" as suggested by Mr. Fairbanks, but rather the equalization of signal propagations through design of the ESD protection circuitry. (*Id.* (citing CX-1044 at Q. 54).)

In its reply brief, Qimonda argues that none of the obviousness references relied on by Respondents teaches the "first supply line" and "second supply line" as required by claim 1. (CRB at 52.) In addition, Qimonda notes that Respondents have failed to assert that claim 1 is obvious. (*Id.*)

Commission Investigative Staff's Position: Staff contends that the asserted claims are not obvious in light of any of the proposed prior art combinations. (SIB at 90-91.) Staff does not believe that claim 1 is anticipated by any of the prior art references, and Respondents do not raise an obviousness challenge with respect to claim 1. (*Id.* at 91.) Staff states that "[t]he asserted combinations also do not clearly and convincingly disclose elements of the listed dependent claims including, among other limitations, the "immediate spatial vicinity" requirement in dependents Claim 4." (*Id.*)

Discussion and Conclusion: Based on the evidence before me, I find that Respondents have failed to demonstrate that any of the asserted claims would have been obvious in light of Krakauer-Mistry combined with Maloney, Ito, or the admitted prior art. Respondents' argument and Mr. Fairbanks' opinion is premised on the conclusion that Krakauer-Mistry discloses all of the elements of claim 1. (RIB at 127-128; RX-774C at Q. 197-199.) I have found *supra* that Krakauer-Mistry fails to disclose the claimed first and second supply lines. Thus, Respondents have failed to prove that any of the asserted claims are obvious in light of this particular combination of references.

6. Strauss-White In Combination With Maloney, Ito, or Admitted Prior Art

Respondents' Position: Respondents contend that claims 1, 2, 3, 5, and 8 are obvious in view of Strauss-White in combination with Maloney, Ito, or the admitted prior art. (RIB at 128.)

Respondents argue that it would have been an obvious design choice for one of ordinary skill in the art to combine the ground path teachings, including bond connections, of Maloney, Ito, or the prior art admitted in the '434 patent to the ESD protection circuitry disclosed in Strauss-White to provide a semiconductor component meeting all of the limitations of claims 2 and 3 of the '434 Patent. (RIB at 128 (citing RX-774C at Q. 201; RX-187 at Fig.2; RDX-127;

RDX-128; RX-0205 at 221-222, Fig.2c; RDX-124; RX-257; JX-1 at 1: 22-48).) Respondents further argue that it would have been have been an obvious design choice for one of ordinary skill in the art to replicate the circuitry disclosed in Strauss-White to provide a semiconductor component meeting all of the limitations of claim 8. (*Id.* (citing RX-774C at Q. 201; RX-187 at Fig.2; RDX-127; RDX-128; RX-222 at Figs.4-6).)

Qimonda's Position: Qimonda contends that Strauss-White combined with either Maloney or Ito fails to disclose every element of claims 2, 3, 5, and 8. (CIB at 116 (citing CX-1044 at Q. 55).) Qimonda previously argued that Strauss-White, Maloney, and Ito do not disclose each and every element of claim 1 of the '434 patent. (*Id.* (citing CX-1044 at Q. 55).) Qimonda asserts that Mr. Fairbanks does not provide a detailed discussion of why a person of ordinary skill in the art would have found it obvious to combine the purported ground path teachings, including bond connections, of Maloney and Ito with the teaching of Strauss-White to render claims 2 and 3 obvious. (*Id.* (citing CX-1044 at Q. 55).) Qimonda argues that such combination would not have been obvious, at least because Strauss-White does not discuss the use of separate supply lines, and therefore such purported "ground path teachings" would have been irrelevant to a person applying the teachings of Strauss-White. (*Id.* at 116-117 (citing CX-1044 at Q. 55).)

Qimonda further argues that Mr. Fairbanks fails to provide a sufficiently detailed explanation regarding why a person of ordinary skill in the art would have found it an obvious design choice to replace the transistor clamp disclosed in Strauss-White with a ggNMOS to render claims 5 obvious. (CIB at 117 (citing CX-1044 at Q. 55).)

Finally, Qimonda argues that Mr. Fairbanks fails to provide a sufficiently detailed explanation regarding why a person of ordinary skill in the art would have found it an obvious

design choice to replicate the circuitry disclosed in Strauss-White to render claims 8 obvious. (*Id.* (citing CX-1044 at Q. 55).) According to Qimonda, such combination would not have been obvious, at least because, the '434 patent discloses and claims much more than mere "replication" as suggested by Mr. Fairbanks, but rather the equalization of signal propagations through design of the ESD protection circuitry. (*Id.* (citing CX-1044 at Q. 55).)

In its reply brief, Qimonda argues that none of the obviousness references relied on by Respondents teaches the "first supply line" and "second supply line" as required by claim 1. (CRB at 52.) In addition, Qimonda notes that Respondents have failed to assert that claim 1 is obvious. (*Id.*)

Commission Investigative Staff's Position: Staff contends that the asserted claims are not obvious in light of any of the proposed prior art combinations. (SIB at 90-91.) Staff does not believe that claim 1 is anticipated by any of the prior art references, and Respondents do not raise an obviousness challenge with respect to claim 1. (*Id.* at 91.) Staff states that "[t]he asserted combinations also do not clearly and convincingly disclose elements of the listed dependent claims including, among other limitations, the "immediate spatial vicinity" requirement in dependents Claim 4." (*Id.*)

Discussion and Conclusion: Based on the evidence before me, I find that Respondents have failed to demonstrate that any of the asserted claims would have been obvious in light of Strauss-White combined with Maloney, Ito, or the admitted prior art. Respondents' argument and Mr. Fairbanks' opinion is premised on the conclusion that Strauss-White discloses all of the elements of claim 1. (RIB at 128; RX-774C at Q. 200-201.) I have found *supra* that Strauss-White fails to disclose the claimed first and second supply lines. Thus, Respondents have failed

to prove that any of the asserted claims are obvious in light of this particular combination of references.

7. Mr. Fairbanks' Qualifications

Qimonda argues that Mr. Fairbanks' testimony regarding the '434 patent should be given little weight because Mr. Fairbanks only has a bachelor's degree, and did not receive his degree until 2000. (CIB at 117.)[53] As a result, Qimonda claims that Mr. Fairbanks was not a person of ordinary skill in the art at the time of the filing of the '434 patent. (*Id.* (citing RX-774C at Q. 20, 185; Tr. at 1111:4-11).) Qimonda states that according to his own definition, Mr. Fairbanks was not a person of ordinary skill in the art until 2003. (*Id.* at 117-118 (citing RX-774C at Q. 186).) Qimonda further argues that Mr. Fairbanks relies on his membership in the ESD Association to prove expertise in the field, but membership in the ESD Association only requires payment of a membership fee. (*Id.* (citing Tr. at 623:10-19).)

Respondents claim that Mr. Fairbanks is qualified to serve as an expert regarding the ESD technology described in the '434 patent, as evidenced by his witness statements and curriculum vitae. (RRB at 65.) Respondents claim that Mr. Fairbanks has considerably more experience in the field of ESD circuitry than Dr. Cottrell. (*Id.*)

Mr. Fairbanks has eleven years of experience in the electronics industry, and has a bachelor's degree in electrical engineering with a minor in mathematics. (RX-774C at Q. 19-21.) Mr. Fairbanks earned 18 units towards a master's degree in electrical engineering. (*Id.* at Q. 20.) Mr. Fairbanks' work experience has focused heavily on ESD protection in circuits. (*Id.* at Q. 21.) In addition, Mr. Fairbanks has been a panel expert at the International ESD and Electrical Overstress (EOS) Symposiums in 2006-2008, presenting various workshop sessions on

[53] While this issue is addressed in the invalidity section of the Initial Determination, Qimonda's argument regarding Mr. Fairbanks' qualifications applies to his expert testimony for both invalidity and non-infringement.

topics relating to ESD. (*Id.* at Q. 22.) I find that Mr. Fairbanks' educational background and work experience qualifies him as an expert in the subject matter of the '434 patent.

Qimonda also raises the argument that Mr. Fairbanks was not one of ordinary skill in the art as of 1996, the year that the '434 patent was filed. Qimonda offers no case law to support the proposition that, in order to be a qualified expert, one must have been a person of ordinary skill in the art at the time of the patent filing. Other courts that have considered this issue have come to the opposite conclusion as Qimonda. *See, e.g., Cardiac Pacemakers, Inc. v. St. Jude Med., Inc.*, 2002 WL 1801525, at *41 (S.D. Ind. July 5, 2002), *aff'd-in-part, rev'd-in-part, & remanded by* 381 F.3d 1371 (Fed. Cir. 2004) (characterizing an identical argument as a "remarkable proposition").

D. The '899 Patent

1. Gocho

Respondents' Position: Respondents allege that U.S. Patent No. 5,498,565 to Gocho et al. ("the '565 patent" or "Gocho") anticipates claims 1, 2, 7-9, 14-16, and 21 of the '899 patent.[54] (RIB at 155.)

Respondents recite that Gocho was filed on November 25, 1992 and issued on March 12, 1996. (RIB at 155 (citing RX-598; RX-723 at Q. 148-156).) Therefore, they say, it is prior art to the '899 patent, which has an earliest possible priority date of August 8, 1996. (*Id.* (citing JX-8; RX-723 at Q. 148-156).) Respondents assert that Gocho discloses a method of manufacturing a semiconductor device. (*Id.* (citing RX-723 at Q. 157-163).) More specifically, they aver, it teaches methods of forming isolation trenches. (*Id.* (citing RX-723 at Q. 157-163).)

[54] Although Respondents assert that Gocho anticipates claims 1, 2, 7-9, 14-16 and 21 of the '899 patent, I note that of that list only claims 1, 2 and 7 are asserted. Inasmuch as, only asserted claims are relevant and material to the issues before me, this Initial Determination will only treat the anticipation issue as to claims 1, 2 and 7.

Respondents argue that those methods disclose the methods claimed in the '899 patent, which is therefore invalid under 35 U.S.C. § 102. Respondents cite *In re Crish*, 393 F.3d 1253, 1256 (Fed. Cir. 2004) to say that the procedure for determining that an invention is anticipated is to "compare the construed claim to a prior art reference and make factual findings that 'each and every limitation is found either expressly or inherently in [that] single prior art reference.'" (*Id.*)

Respondents state that claim 1 of the '899 patent requires "defining active and non-active regions on the surface of the substrate," and Gocho discloses this limitation in Figure 1(a), which shows trenches (41)-(43) in different areas on the substrate. (RIB at 155 (citing RX-598 at Fig. 1(a)).) Respondents argue that a person of ordinary skill in the art would recognize that the trenches are nonactive regions and that the regions between the trenches are active regions. (*Id.* (citing RX-723 at Q. 165).)

Respondents recite that claim 1 of the '899 patent requires "forming isolation trenches of varying widths the active regions comprising active regions of varying width in the non-active regions." They assert that this limitation is disclosed by Figure 1(a) of Gocho, which shows trenches of differing widths. (RIB at 155-156 (citing RX-598 at Fig. 1(a)).) They recite that Gocho says, at column 10, lines 63-67:

> This can provide a structure as shown in FIG. 2(a). In the drawing, are shown a burying material 5a buried in a wide trench 41, burying materials 5b, 5c buried in *narrow* trenches 41-43 [sic], burying material 5 over a wide protrusion region (1) and burying materials 5e, 5f on a narrow protrusion region.

(RIB at 155-156) (emphasis added by Respondents). Respondents argue that, a person of ordinary skill in the art would have recognized that Gocho discloses forming isolation trenches of varying widths separated by active regions of varying widths. (*Id.* (citing RX-723 at Q. 166).)

Respondents recite that claim 1 of the '899 patent requires:

> [F]orming a layer of HDP-CVD insulating material of silicon oxide, wherein the HDP-CVD silicon oxide layer is non-planar and protrudes angularly above isolation trench edges forming sloping edges that slope away from the trench on the substrate by [HDP-CVD], the HDP-CVD layer substantially filling the trenches and covering the active regions.

Respondents argue that a person of ordinary skill in the art would have recognized that Gocho discloses this limitation. (RIB at 156 (citing RX-723 at Q. 167).) Respondents state that Gocho, in describing Fig. 1(a), states: "a structure as shown in FIG. 1(a) is obtained by burying trenches 41-43 by a deposition means that conducts etching and deposition simultaneously (a bias ECR-CVD process is used in this example)." (*Id.* (citing RX-598 at 8:61-64).) Respondents add that Figures 1(a), 2(a), 6(b), 7(a), 9(b), 10(b), 10(d), 11(b), 12(a), and 14(a) of Gocho disclose the silicon oxide protruding angularly and sloping away from the trench, which the patent describes as having been deposited using ECR-CVD. (*Id.* (citing RX-723 at Q. 167).) Respondents argue that when the '899 patent application was filed, a person of ordinary skill in the art would have recognized that the ECR-CVD method is a type of HDP-CVD. (*Id.* (citing Tr. at 1452:20-1453:17; JX-8 at 5:22-24; RX-723 at Q. 167).)

Respondents say the next step in claim 1 of the '899 patent requires "removing at least a portion of the insulating material covering the active regions." Respondents allege that Gocho discloses this limitation as well, quoting:

> SiO2, which is the burying material 5, is isotropically etched by isotropic etching. For instance, this may be performed by wet etching using a solution of hydrofluoric acid diluted to 1/40.

(RIB at 156-157 (citing RX-598 at 9:23-26).)

Respondents argue that a person of ordinary skill in the art would have recognized that the etching described in this step removes the insulating material covering the active regions. (RIB at 156-157 (citing RX-723 at Q. 168).) Respondents say that Figure 2(c) of Gocho shows

the results of the described etching, in which a portion of the insulating material over the wide active region has been etched away. (*Id.* (citing RX-598 at Fig. 2(c)).) Respondents argue that a person of ordinary skill in the art would have recognized that the same technique could have been applied to the narrow active regions as well, if desired. (*Id.* (citing RX-723 at Q. 168).)

Respondents recite that the next step of Claim 1 of the '899 patent requires "planarizing the surface of said substrate to expose the active regions." They argue that Gocho discloses this limitation. (RIB at 157 (citing RX-723 at Q. 170).) Respondents refer to Figure 2(e) of Gocho, saying it shows the planarized surface of the substrate with the exposed active regions. (*Id.* (citing RX-598 at Fig. 2(e)).)

Respondents continue that claim 1 of the '899 patent clarifies that "the removal of at least a portion of insulating material from the active regions" should provide "a planar topography." Respondents point out that Figures 1(f), 2(e), 4(c), 5(d), 6(e), 7(f), 8(e), 9(f), 10(g), 11(c), 12(b), and 13(c) of Gocho show the final planar topography achieved by the Gocho process. (RIB at 157 (citing RX-598).) Respondents argue that a person of ordinary skill in the art would have recognized that these flattened substrates have planar topographies. (*Id.* (citing RX-723 at Q. 170).)

Respondents recite that claim 1 of the '899 patent then states that "removing at least a portion of the insulating material from the active regions" means first, "depositing a mask layer over the insulating material." They continue that Figures 1(b), 2(b), 5(b), 6(c), 9(c), 10(d), and 13(a) of Gocho all show a photoresist mask layer over insulating material. (RIB at 157-158 (citing RX-598; RX-723 at Q. 171).) Respondents say Figures 1(b) and 2(b) show the photoresist mask layer as layer 3 resting above insulating materials identified as 5 in Figure 1(b) and 5d in Figure 2(b). (*Id.* (citing RX-598).)

Respondents claim that the next step in "removing at least a portion of the insulating material from the active regions" requires "patterning the mask layer to expose at least a portion of the insulating material over the active regions." Respondents allege that the mask layers shown in Figures 1(b), 2(b), 6(c), 9(c), and 10(d) of Gocho each have gaps where the insulating material over the active regions is exposed. (RIB at 158 (citing RX-598; RX-723 at Q. 172).) Respondents argue that a person of ordinary skill in the art would have recognized that these gaps are due to patterning. (*Id.* (citing RX-723 at Q. 172).)

Respondents assert that the final step in "removing at least a portion of the insulating material from the active regions" requires "removing the exposed portion of the insulating material over the active regions, leaving unexposed portions of the insulating materials." Respondents point to Figure 2(c) of Gocho, which they say shows the results of removing the exposed insulating material while leaving unexposed portions (11 and 50). (RIB at 158 (citing RX-598).) Respondents argue that, although Figure 2(c) of Gocho shows that some of the unexposed oxide — the oxide below the photoresist mask — has been removed due to the use of a wet etch, claim 1 does not require leaving all of the unexposed oxide. (*Id.* (citing RX-598 at Fig. 2(c); JX-8 at 9:18-19).)

Respondents reiterate their argument from section IV.B.2 contrasting the claim language requiring removal of all the exposed oxide reasoning that the use of the definite article in "removing the exposed portion" with the language requiring leaving unexposed portions, which they say, does not use a definite article when it states "leaving unexposed insulating material." Respondents reason that claim 1 does not require leaving all the "unexposed portions of the insulating material." (RIB at 158.) Based upon that reasoning, Respondents argue that the fact that Gocho shows the removal of some of the unexposed oxide is of "no consequence." (*Id.*)

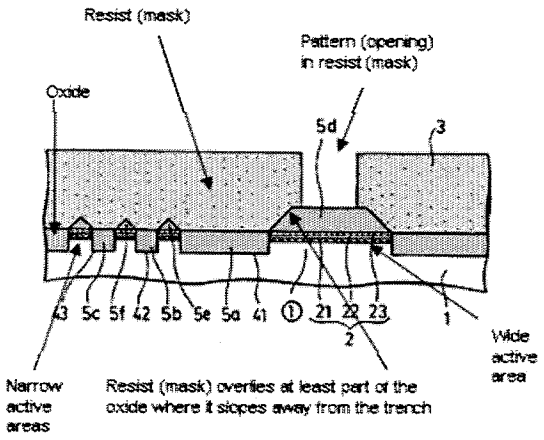
Respondents conclude that claim 1 of the '899 patent requires that "the mask layer is deposited using an inverse active area mask that is biased so that the mask layer after patterning covers the non-active regions and at least a portion of the active regions." Respondents state that the mask layers shown in Figures 1(b), 2(b), and 9(c) of Gocho are deposited using a biased inverse active area mask. (RIB at 158-159 (citing RX-723 at Q. 174-177).) Respondents say that Dr. Bravman explained, because of the bias, the photoresist covers the inactive regions (trenches) as well as a portion of the active regions. (*Id.* (citing RX-723 at Q. 174-177).) Respondents offer Figure 2(b) as an example, because of what they call the "large bias (shown by the overlap of the photoresist 3 over oxide 5d)," they say the photoresist completely covers the narrow active regions (located below oxide 5f and 5e). (*Id.* (citing RX-723 at Q. 174-177).) Respondents assert that although a simple "inverse" mask would show openings over the narrow active regions, because the mask shown in Figure 2(b) is biased by more than one-half the width of the narrow active regions, the narrow active regions (below oxide 5f and 5e) are covered by the oxide. (*Id.* (citing RX-723 at Q. 174-177).)

Respondents argue that the partial covering of the wide active regions combined with a total covering of the narrow active regions indicates the use of a biased inverse active area mask. (RIB at 159-160 (citing RX-723 at Q. 174 -177).) Respondents say that it was this same characteristic that led Qimonda's expert to conclude that {

} (*Id.* (citing CX-202C at Q. 234).) Respondents offer a side-by-side comparison of the { } that they say Dr. Gutmann found {

} and the Gocho mask, which are included below.

{ Gocho Mask



} RX598 at Fig. 2(b)

(colorized and annotated to match the annotated version of CX231C, p. 18, shown on the left)

Respondents conclude that if the { } so is the Gocho mask. (RIB at 159-160.)

Respondents recite that claim 2 of the '899 patent requires "the inverse active area mask is biased so that the mask layer after patterning covers at least a portion of the sloping edges of the insulating layer in the active regions." They argue that Gocho discloses this limitation. (RIB at 160 (citing RX-723 at Q. 179).) Respondents offer that Figures 1(b), 2(b) and 6(c) of Gocho show the photoresist mask layer covers the sloping edges of the insulating layer in the active regions. (*Id.* (citing RX-598; RX723 at Q. 178-179).)

Respondents recite that claim 7 of the '899 patent adds the step of "removing the mask layer after removing the exposed insulating material." Respondents argue that Gocho discloses this limitation as follows: "Isotropic etching is conducted to etch the buying material 5d on the wide (long) protrusion region (1) . . . . Subsequently, the resist is removed. Thus, a structure as shown in FIG. 4(c)[sic] is obtained." (RIB at 160 (citing RX-598 at 11:4-14).) Respondents

argue that a person of ordinary skill in the art would also recognize that the statement meant to refer to Figure 2(c). (*Id.* (citing RX-723 at Q. 188-189).)

Respondents argue that during prosecution of the '899 patent, the Examiner did not appreciate the type of mask disclosed in Gocho, nor was he presented with the inconsistent statements Qimonda has made about that type of mask at issue in this investigation. (RIB at 160.) So, they say, the fact that Gocho was cited during prosecution of the '899 patent carries little weight. (*Id.*)

Respondents assert that in allowing the '899 patent, the Examiner stated that the "[p]rior art of record does not teach or suggest the claimed invention in which an inverse active area mask is used to remove at least a portion of the insulating layer from the active regions as claimed." (RIB at 169-170 (citing JX-9 at 196).) They state that the Examiner's statement demonstrates a failure to grasp the breadth of the claim language — "biased so the mask layer after patterning covers the non-active regions and at least a portion of the active regions" — and a failure to appreciate the type of mask shown in the prior art. (*Id.* (citing RX-723 at Q. 148).) Respondents claim that although prior-art masks like the Gocho mask show narrow active regions covered by oxide, this does not mean they are not biased active inverse area masks. (*Id.*) They argue the scope of "at least a portion of the active regions" includes covering all of the active regions. (*Id.*) Respondents assert that Gocho discloses an inverse active area mask. Respondents offer that Figure 2(b) of Gocho shows resist layer 3 applied to the surface of the substrate. (*Id.*) This mask, they argue, is an inverse active area mask with a bias that is greater than half the width of the narrow active regions. (RIB at 169-170.) Respondents aver that because of the size of the bias, the smaller active areas are completely covered by the mask layer. (*Id.*) They argue that a person of ordinary skill in the art would have recognized at the time that

this was a biased inverse active area mask by noting how the aperture in the mask over the wide active region 5d is reduced by an amount on each side that is greater than half the width of the narrower active regions such as 5f and 5b. (*Id.* (citing RX-723 at Q. 176).)

Respondents continue that the Patent Office did not have before it the statements now being made by Qimonda that {

} (RIB at 170 (citing CX-231C; RX-598 at Fig. 2(b)).) Respondents say that if the Applicant had argued that {

}

CX-202C at Q. 234).) Respondents conclude that, in light of the applicant's failure to disclose to the Patent Office that it considered {

} Qimonda cannot now fairly argue that the Gocho patent was properly considered by the Patent Office. (*Id.*)

In their reply brief Respondents note that Qimonda argues that the prior art does not disclose a biased inverse active area mask because it does not show how to make such a mask. (RRB at 75-76 (citing CIB at 131-34).) Respondents argue that Qimonda's attack fails for at least two reasons. First, they say, a proper claim construction does not require that a mask be made in any particular fashion, and they quote the '899 patent to describe the mask as follows:

> In one embodiment, an inverse active area mask (not shown) is used to form and pattern the HDP-CVD oxide layer. **Such a mask is the negative mask of the mask used to form the active areas. Techniques for biasing the inverse mask are well known in the art.** Typically, there are overlay inaccuracies associated with the lithographic process. To compensate for the overlay inaccuracies, the inverse mask is biased. The amount of bias is sufficient to effectively shift the edges of the photoresist onto the sloping edges 55 and 56 of the HDP-CVD oxide layer.

(RRB at 75-76 (citing JX-8 at 7:6-16)) (emphasis added by Respondents). Respondents assert that the '899 patent describes an "inverse active area mask" as a "negative" of the mask used to form the active areas, and it states that techniques for "biasing" are "well known in the art." (*Id.*) Respondents say Qimonda reads a specific method of forming the mask into the claim language that is not described in the '899 patent. (*Id.*)

Second, Respondents argue, regardless of how the claim is construed, Qimonda takes inconsistent positions about biased inverse active area masks. (RRB at 76.) Respondents say that in attempting to prove the technical prong of the domestic-industry requirement, {

} Respondents assert that neither Gocho { } discloses how the masks are made. Respondents reason that if Gocho's failure to teach how the mask is made is fatal to invalidity, then Qimonda's domestic industry argument also fails. (*Id.*) They conclude that Qimonda should not be allowed to argue {

}

Qimonda's Position: Qimonda delivers its arguments regarding alleged anticipation of the '899 patent by Gocho and Sato in tandem. Qimonda asserts that the U.S. Patent Office Examiner had specifically and carefully considered both Gocho and Sato during prosecution of

the '899 patent application. (CIB at 128 (citing JX 8 at QAG-665-ITC-0189111; JX 9 at QAG-665-ITC 0189254, 0189257; CX-1046 at Q. 95; Tr. at 1212:2-1213:2, 1242:13-23, 1246:25-1247:7).) Qimonda argues that the Examiner concluded that these references, alone or in combination, did not anticipate or render obvious the claimed invention of the '899 patent, and granted the patent over both of them. (*Id.* (citing JX-9 at QAG-665-ITC-0189257, QAG-665-ITC-0189318).)

Qimonda argues that for claims 1-22[55] of the '899 patent, the only theory of invalidity presented by Respondents is anticipation. (CIB at 128-129 (citing Tr. at 1214:1-10, 1213:10-20).) Qimonda argues that the law is clear and undisputed that the claimed invention of a patent can be "anticipated" only where a single prior art reference "by itself" discloses each and every one of the claim limitations. (*Id.* (citing *Helifix Ltd. v. Blok-Lok Ltd.*, 208 F.3d 1339, 1346 (Fed. Cir. 2000)).) Qimonda says that Respondents' expert, Dr. Bravman, conceded at trial that neither of the two prior art references "by itself" discloses all of the limitations of the '899 patent claims including, *inter alia*, the "inductively coupled" and "biased inverse active area mask" limitations. (*Id.*) As a result, Qimonda argues, Respondents' invalidity position fails as a matter of law.

Qimonda argues that it is well settled and undisputed that in order for a reference to be anticipating, all of the claim limitations need to be contained in a single reference. (CIB at 129-130 (citing *Studiengesellschaft Kohle, m.b.H. v. Dart Industries, Inc.*, 726 F.2d 724, 726-727 (Fed. Cir. 1984); Tr. at 1214:1-10).) Qimonda argues that both independent claim 1 and independent claim 22 of the '899 patent require the use of inductively coupled high density plasma chemical vapor deposition. (*Id.* (citing JX-8 at 5:18-35, 8:26-31, 8:66-67, 12:1-6;

[55] I note that Qimonda has addressed claims 1-22; but that Respondents have only alleged that asserted claims 1, 2 and 7 are invalid as anticipated. Therefore, analysis and discussion of anticipation of claims other than 1, 2 and 7 is not relevant or material to this decision and will not be further considered in this part.

CX-202C at Q. 82, 159, 203; CX-1046 at Q. 57-58, 90, 118; Tr. at 1449:2-5, 1449:23-1450:1, 1450:19-1451:12, 1452:15-1453:3, 1455:11-14, 1457:19-1459:3).) Qimonda continues that the record is also clear and undisputed that Gocho discloses only one type of oxide deposition technique, electron cyclotron resonance chemical vapor deposition (ECR-CVD). (*Id.* (citing RX-598 at 4:5-12, 9:13-20, 9:60-64, 10:57-62; CX-1046 at Q. 36, 78, 91; RX-568 at 1:37-53, 2:9-19, 2:56-64, 3:23-28, 4:16-25, 5:48-6:59, 7:67-8:2; CX-1046 at Q. 36, 106-107, 120).) Qimonda argues that Gocho does not disclose a key limitation required by all claims of the '899 patent. Qimonda quotes Respondents' expert to say at the hearing:

> Q: … My question to you, sir, having analyzed that patent claim, is ECR-CVD that is disclosed in the prior art an inductively coupled plasma? Yes or no?
>
> * * *
>
> A: … Well, in my opinion, in the context of the '899 patent, with — especially with reference to that textbook, a worker of skill would understand that inductively coupled is used to differentiate from ECR. And so that answer — I believe that answers your question. ECR is not, in the way the phrase is used here, inductively coupled.
>
> * * *
>
> Q: … You gave essentially the same answer in your direct testimony for the Sato '853 patent as you did for the Gocho, that it discloses an ECR-CVD, correct?
> A: It does disclose ECR-CVD, yes.
>
> Q: Therefore, the Sato '853 patent does not disclose an inductively coupled plasma as called for in claim 22, correct?
> A: It would be the same set of answers for the same reasons. The result is the same.
>
> Q: And that is it doesn't disclose it, Dr. Bravman, correct?
> A: It discloses as a named technique ECR. Bias ECR-CVD. It does not disclose by name inductively coupled.
>
> Q: And thus, Doctor, the Sato '853 patent does not meet the inductively coupled limitation of claim 22, correct?
> A: I agree on the same basis with you.

* * *

> Q: And as we discussed earlier with respect to Gocho and Sato, I believe, but just to confirm, the '853 patent discloses only ECR plasma and thus does not describe an inductively coupled plasma, correct?
> A: That's what I said earlier today.

(CIB at 129-130 (citing Tr. at 1222:11-13, 1223:8-14, 1223:18-1224:10, 1247:8-12).) Qimonda says that "it is undisputed" that the prior art cannot anticipate the inductively coupled high density plasma limitations of the '899 patent claims. (*Id.*) Qimonda adds that Respondents "do not and cannot dispute this with respect to claims 22 and 23," which they say expressly recite "inductively coupled." (*Id.*)

Qimonda states that with respect to claim 1, Respondents are attempting to argue that the "HDP-CVD" limitation should be read more broadly to include "every conceivable deposition technique that employs a high density plasma." (CIB at 130-131.) Qimonda argues that the law requires that the claims be read in the context of the specification of the '899 patent, which clearly and expressly distinguishes between inductively coupled plasma (i.e., HDP-CVD) on one hand, and electron cyclotron plasma on the other, reciting:

> [] HDP-CVD techniques, for example, employ the use of an inductively coupled plasma source.
>
> * * *
>
> HDP-CVD techniques reduce or eliminate the formation of gaps in the shallow trenches usually associated with conventional trench filling techniques. Electron cyclotron and helicon wave excited plasma techniques are <u>*also*</u> useful for depositing the oxide layer.

(CIB at 130-131 (citing JX-8 at 5:20-21, 30-35)) (emphasis added by Qimonda). Qimonda adds that the intrinsic reference makes it clear that a person of ordinary skill would have understood the term "HDP-CVD" in claim 1 to require the use of an inductively coupled plasma source. (*Id.* (citing JX-8 at 8:26-31; CX-202C at Q. 82, 159, 203; CX-1046 at Q. 57-58, 90, 118; Tr. at 1449:23-1450:1, 1450:19-1451:12, 1452:15-1453:3, 1455:11-14, 1457:19-1459:3).)

Qimonda avers that at the hearing, Respondents' expert conceded that neither Gocho nor Sato explicitly disclose a biased inverse active area mask, "as required by all the claims of the '899 patent." (CIB at 131-133.) Qimonda refers to the testimony of Dr. Bravman, who they say admitted that the prior art does not expressly disclose (i) inverting the active area mask, or (ii) biasing such an inverse mask, quoting:

> Q: …So the record is clear, the Gocho patent itself doesn't explicitly describe biasing of an inverse active area mask to arrive at the structure shown in figure 2(b), correct?
> A: It doesn't describe how to make the inverse mask or bias it. That's correct.
>
> * * *
>
> Q: Now, the fact is, sir, that neither of the prior art references upon which you rely use the words 'inverse active area mask' or describe how to generate one; isn't that correct?
> A: I agree with you, there are -- mask making is outside the scope of both references.
>
> Q: And in your direct testimony, you didn't come forward with a single reference before the '899 patent was filed, which explicitly described the generation of an inverse active area mask, let alone a biased one, correct?
> A: The only two pieces of prior art we're discussing, that's correct.
>
> * * *
>
> Q: Okay. Just so the record is clear. The Sato '853 patent does not explicitly disclose how to generate an inverse active area mask from the original active area
> A: That's correct. It's outside the scope of the patent.
>
> * * *
>
> Q: …Now, just to clean up one point, the Sato '853 patent does not explicitly disclose a step of biasing an active area mask or its inverse mask, correct?
> A: Those words -- those phrases do not appear. I drew my conclusion based on a result.

(CIB at 131-133 (citing Tr. at 1238:20-25, 1243:11-23, 1247:19-24, 1250:11-16).) Qimonda argues that this is what the Patent Office determined when it allowed the '899 patent to issue. (*Id.*) Qimonda continues that techniques for generating the inverse active area mask directly

from the original active area mask are not specified. (*Id.*) Qimonda says Gocho generally instructs the reader to form a resist pattern to expose only the wide active area regions. (*Id.*) Qimonda contrasts RX-598 at 11:1-3 and claim 1 with JX-8 at 7:43-45, and notes that the latter provides the biased inverse active area mask of the '899 patent claimed invention "advantageously eliminates the need to randomly generate a new mask in order to expose the active areas." (*Id.* (citing Tr. at 1242:13-23; JX 8 at 9:20-24, 12:7-10; CX-202C at Q. 77; CX-1046 at Q. 60, 79-80-82, 90, 92, 118; CX-202C at Q. 77, 83-84; CX-991C at Q. 25; CX-190C at Q. 84; Tr. at 347:17-349:21; RDX-441C; CX-485C at 185:17-191:1; RX-723 at Q. 176, 280; RDX-31.59, RDX-32.60; RX-568 at 1:66-2:2, 4:55-57, 8:8-10).)

Qimonda argues that Dr. Bravman's testimony contradicts his opinion that the teaching of a biased inverse active area mask is somehow inherent in the photoresist patterns shown by the prior art, based on his "conclusory" statement that the biased inverse mask technique was so well known to persons of skill that the prior art did not need to describe it. (CIB at 133 (citing RX-723 at Q. 177).) Qimonda says that Dr. Bravman conceded both at this deposition and at the trial that there are many ways to create a photoresist pattern, and an inverse active area mask is merely one of the many possible ways. (*Id.* (citing Tr. at 1234:15-1235:1, 1249:24-1250:10, 1236:8-14).)

Qimonda argues because the result shown in the prior art relied on by Respondents and their expert can be arrived at in many different ways, and not necessarily by an inverse active area mask that has been biased, it is insufficient for purposes of anticipation. (CIB at 133 (citing RX-598 at 2:21-29, 3:29-35, 11:1-3; RX-568 at 1:66-2:2, 4:55-57, 8:8-10; CX-1046 at Q. 81-82, 89, 92-94, 121; Tr. at 1226:3-11, 1227:14-1228:3, 1234:15-1235:1, 1236:8-10, 1236:24-1237:22, 1247:19-24, 1249:24-1250:16).)

In its reply brief, Qimonda argues that Respondents' invalidity argument is based entirely on their expert's conclusory assertions, rather than on the teachings of the prior art. (CRB at 63-64.) They aver that the '899 patent explains that the use of the claimed biased inverse area mask is an improvement over prior methods of masking because it "advantageously eliminates the need to randomly generate a new mask in order to expose the active areas." (*Id.* (citing JX-8 at 7:43-45).) Qimonda says that at trial, Respondents' expert, Dr. Bravman, conceded that neither of the prior art references he relied on (Gocho and Sato) expressly taught generation of an inverse active area mask from the original active area mask, or biasing the inverse mask so generated. (*Id.* (citing Tr. at 1238:20-25, 1243:11-23, 1247:19-24, 1250:11-16; SIB at 55-57).) Qimonda alleges that Respondents have not identified a *single* prior art reference that expressly teaches this limitation.

Qimonda argues that Respondents rely solely on Dr. Bravman's assertion that inverting and biasing an active area mask "was so well known at the time that the [prior art] does not bother describing how to create it." (CRB at 64 (citing RX-723 at Q. 177 (Gocho) and Q. 280 (Sato)).) They assert that such conclusory expert testimony is legally insufficient to read teachings into the prior art where none exist. Qimonda cites *Motorola, Inc. v. Interdigital Tech. Corp.*, 121 F.3d 1461, 1473 (Fed. Cir. 1997) to say an expert's conclusory testimony, unsupported by the documentary evidence, cannot supplant the requirement of anticipatory disclosure in the prior art reference itself. (*Id.*)

Qimonda argues that Dr. Bravman's opinions are also plainly contradicted by the determination of the U.S. Patent Office in granting the '899 patent over both Gocho and Sato, based on their failure to teach the use of an inverse active area mask. (CRB at 64 (citing JX-9 at QAG-665-ITC-0189318).) Qimonda reasons that, because an "inverse active area mask that is

biased" is an element of each and every one of the claims of the '899 patent, Respondents' anticipation defense must fail as to all. (*Id.*)

Qimonda argues that all of the invalidity defenses raised by Respondents up to and at the hearing are fatally flawed, because neither of the prior art references they rely upon teaches an inductively coupled plasma "as required by the claims of the '899 patent." (CRB at 65.) Qimonda states that Respondents' expert, Dr. Bravman, conceded at the hearing that both Gocho and Sato teach only ECR-CVD, and that ECR-CVD does not meet an inductively coupled plasma claim requirement. (*Id.* (citing Tr. at 1222:8-13, 1223:2-1224:10, 1247:8-12).)

Qimonda argues that for claims 22 and 23 of the '899 patent this concession is dispositive of the anticipation defenses, because both claims expressly require "depositing a silicon oxide layer formed in an inductively coupled high density plasma chamber by chemical vapor deposition." (CRB at 65 (citing JX-8 at 12:1-3).) Qimonda continues that those defenses must also be rejected with respect to claim 1 and the remainder of the asserted claims based on the construction of the claim term "HDP-CVD" that is proposed by both Qimonda and Staff as an inductively coupled plasma, and excluding ECR-CVD. (*Id.* (citing SIB at 49-50).)

Qimonda concludes that Respondents' obviousness argument with respect to claim 23, which attempts to combine the Gocho and Sato references, must also fail based on the same logic and failure of proof, because neither reference teaches an inductively coupled plasma and Respondents' brief fails to present any argument or evidence, regarding why that limitation would be obvious in view of that combination. (CRB at 65 (citing RIB at 190-191).)

Commission Investigative Staff's Position: Staff takes the view that the evidence does not clearly and convincingly show that Gocho anticipates or renders obvious the asserted claims of the '899 patent. (SIB at 55-56.) Staff notes that Gocho was specifically considered by the

examiner during prosecution and was used as the basis for an initial rejection. (*Id.*) Staff argues that *Power Oasis, Inc. v. T-Mobile USA, Inc.*, 522 F.3d 1299, 1304 (Fed. Cir. 2008) provides that heightened deference is afforded a decision by a patent examiner which considered prior art preference. (*Id.*) Staff does not believe that the evidence clearly and convincingly shows that Gocho disclosed or taught (1) the use of a "silicon oxide layer formed in an inductively coupled high density plasma chamber by chemical vapor deposition" as required by Claim 22; or (2) an inverse active area mask that is biased. (*Id.*)

Staff asserts that Respondents' expert, Dr. Bravman, admitted during cross examination that the use of an ECR-CVD process for the formation of burying material disclosed by Gocho is not an inductively coupled plasma as used in claim 22 of the '899 patent. (SIB at 56 (citing Tr. at 1223).) Staff says that Dr. Gutmann, Qimonda's expert, opined that the ECR-CVD process disclosed in Gocho is "something entirely different from inductively coupled plasma" set forth in claim 22. (*Id.* (citing CX-1046C at Q. 91).) Staff avers that Dr. Gutmann observed that "[a]n ECR plasma chamber has a completely different configuration from an inductively coupled chamber ..." (*Id.* (citing CX-1046C at Q. 120).) Staff argues that, given the heavy burden borne by Respondents, Gocho discloses claim 22's requirement of an "inductively coupled high density plasma chamber." (*Id.*)

Staff argues that Gocho does not clearly and convincingly disclose the use of a biased inverse active area mask as required by claims 1 and 22 of the '899 patent. (SIB at 57.) Staff posits that during cross-examination, Dr. Bravman admitted that Gocho did not explicitly disclose how to make an inverse active area mask or a biased inverse active area mask; but he concluded that one of ordinary skill in the art would have implicitly understood the need for such a mask. (*Id.* (citing Tr. at 1238).) Staff contrasts this with the testimony of Dr. Gutmann, who

they say, opined that Gocho did not disclose explicitly or inherently the use of such a mask, because Gocho disclosed "a custom-designed mask that has opening in correspondence of very wide active areas ... [while] a biased inverse active area mask, on the other hand, is automatically generated ..." (*Id.* (citing CX-1046C at Q. 22).) Staff alleges that Dr. Bravman also conceded that the specification in Gocho did not explicitly disclose using an inverse active area mask that was then biased. (*Id.* (citing Tr. at 1241).) Staff says that Dr. Bravman also agreed that the patent examiner concluded that the prior art of record including Gocho did not teach or suggest an inverse active area mask that is used to remove at least a portion of the insulating material from the active area regions as claimed in the '899 patent. (*Id.* (citing Tr. at 1242).)

Staff argues that during his cross-examination, Dr. Bravman crystallized the dispute over Gocho when he said, "I believe in granting the ['899] patent over the Gocho patent ... the patent examiner misunderstood how bias would produce exactly this figure 2(b) [in the Gocho patent], because [he] did not understand that the bias would cove [sic] at least a portion of insulating layer." (SIB at 57 (citing Tr. at 1241).) Staff argues that given Dr. Gutmann's testimony and the heavy deference accorded to the examiner, Gocho does not disclose the use of a biased inverse active area mask required by claims 1 and 22 of the '899 patent. (*Id.*)

Discussion and Conclusion: Based on the evidence before me, I find that Respondents have failed to meet their burden to prove by clear and convincing evidence that Gocho anticipates claims 1, 2, or 7 of the '899 patent.

Gocho was filed on November 25, 1992, but claims priority back to November 29, 1991. (RX-598.) Gocho issued on March 12, 1996. (*Id.*)

The two disputed issues regarding whether or not Gocho anticipates the '899 patent include: (1) whether or not Gocho discloses the limit of element 3 of claim 1 which requires:

> [F]orming a layer of HDP-CVD insulating material of silicon oxide, wherein the HDP-CVD silicon oxide layer is non-planar and protrudes angularly above isolation trench edges forming sloping edges that slope away from the trench on the substrate by [HDP-CVD], the HDP-CVD layer substantially filling the trenches and covering the active regions.

and (2) whether or not Gocho discloses the "inverse active area mask" limitation of element 5 of claim 1.

First, Qimonda and Staff base their argument regarding element 3 of claim 1 on the proposed construction of the term "HDP-CVD insulating material of silicon oxide" and assert that the term requires that the material be an "inductively coupled plasma." The construction of the term applied in this case, however is "an insulating material of silicon oxide deposited using a high density plasma-enhanced chemical vapor deposition process," and the construction is not limited to require "inductively coupled plasma."[56]

Qimonda and Staff argue that Gocho discloses only one type of oxide deposition technique, electron cyclotron resonance chemical vapor deposition (ECR-CVD). Qimonda argues that since the requirement for HDP-CVD silicon oxide deposition requires "inductively coupled plasma" to be used, ECR-CVD cannot anticipate this limit of claim 1. (CIB at 129-130; SIB at 56.) Respondents agree that Gocho, discloses the use of ECR-CVD. (RIB at 156.) Thus, it is undisputed that Gocho discloses the use of ECR-CVD.

The evidence in the record clearly and convincingly supports a finding that the term "HDP-CVD insulating material of silicon oxide" includes material deposited using the ECR-CVD method. The '899 patent incorporates by reference Francombe, *Physics of Thin Film*, Academic Press (1994) ("Francombe"). (JX-8 at 5:22-24.) Dr. Bravman, Respondents' expert,

[56] The rationale for this construction is set forth in full in section III.D.1.

testified that "a person of ordinary skill would have recognized … that the bias ECR-CVD method is unequivocally a type of HDP-CVD." (RX-723 at Q. 167.) At the hearing, Qimonda's expert, Dr. Gutmann confirmed that ECR-CVD is identified in Francombe as an HDP-CVD process. (Tr. at 1452:20-1453:17.)

Based on the foregoing, I find that Gocho discloses the limitation in element 3 of claim 1 of the '899 patent.

Second, Respondents argue that Gocho discloses the limit of claim 1 of the '899 patent that teaches "the mask layer is deposited using an inverse active area mask that is biased so that the mask layer after patterning covers the non-active regions and at least a portion of the active regions." Respondents state that the mask layers shown in Figures 1(b), 2(b), and 9(c) of Gocho are deposited using a biased inverse active area mask. Respondents argue that the partial covering of the wide active regions combined with a total covering of the narrow active regions indicates the use of a biased inverse active area mask. Respondents say that it was this same characteristic that led Qimonda's expert to conclude that Qimonda's process used a biased inverse active area mask. (RIB at 158-160 (citing RX-723 at Q. 174-177; CX-202C at Q. 234).)

At the hearing, however, Respondents' expert conceded, albeit somewhat reluctantly, that neither Gocho nor Sato explicitly disclose a biased inverse active area mask. (Tr. at 1236:8-1237:22; 1243:11-16.) Dr. Bravman admitted that he had not cited any reference in his direct testimony existing before the '899 patent was filed that explicitly described the generation of an inverse active area mask. (*Id.* at 1243:17-23.)

At the hearing, Dr. Bravman admitted that the patent examiner, speaking of Gocho, had found that the prior art of record does not teach or suggest the claimed invention in which an inverse active area mask is used to remove at least a portion of the insulating layer from the

active area regions as claimed. (Tr. at 1242:13-23.) Qimonda argues persuasively that techniques for generating the inverse active area mask directly from the original active area mask are not specified in Gocho, which generally instructs the reader to form a resist pattern to expose only the wide active area regions. Qimonda contrasts RX-598 at11:1-3 and claim 1 with JX-8 at 7:43-45, and notes that the latter provides the biased inverse active area mask of the '899 patent claimed invention "advantageously eliminates the need to randomly generate a new mask in order to expose the active areas." (CIB at 131-133.)

Dr. Gutmann in his direct testimony described, *inter alia*, that an inverse active area mask is a mask that is obtained from the active area mask using an inversion step in which the clear and opaque areas of the mask are reversed. (CX-202C at Q. 83-84.) By contrast, Dr. Bravman conceded both at his deposition and at the trial that there are many ways to create a photoresist pattern, and an inverse active area mask is merely one of the many possible ways. (Tr. at 1236:8-14, 1249:24-1250:10.)

Respondents cite *In re Crish*, 393 F.3d 1253, 1256 (Fed. Cir. 2004) to say that the procedure for determining that an invention is anticipated is to "compare the construed claim to a prior art reference and make factual findings that 'each and every limitation is found either expressly or inherently in [that] single prior art reference.'" (RIB at 155.) Qimonda argues that the law is clear and undisputed that the claimed invention of a patent can be "anticipated" only where a single prior art reference "by itself" discloses each and every one of the claim limitations. (CIB at 334-335 (citing *Helifix Ltd. v. Blok-Lok Ltd.*, 208 F.3d 1339, 1346 (Fed. Cir. 2000); *Studiengesellschaft Kohle, m.b.H. v. Dart Industries, Inc.*, 726 F.2d 724 at 726-727 (Fed. Cir. 1984)).)

The court in *Helifix,* said that "to be anticipating, a prior art reference must disclose 'each and every limitation of the claimed invention[,] ... must be enabling[,] and [must] describe ... [the] claimed invention sufficiently to have placed it in possession of a person of ordinary skill in the field of the invention.'" *Helifix*, 208 F.3d at 1346 (citing *In re Paulsen*, 30 F.3d 1475, 1478-79 (Fed.Cir.1994).)

In the case at hand, the evidence indicates that an inverse active area mask is a mask that is obtained from the active area mask using an inversion step in which the clear and opaque areas of the mask are reversed. Thus, it is a specific type of mask derived from reversing its predecessor. The evidence shows that Gocho, however, does not refer to an "inverse active area mask" and does not teach or suggest making or using one. It merely instructs the reader to form a resist pattern to expose only the wide active area regions, and the evidence shows there are many ways to create a photoresist pattern.

Based upon the foregoing, I find that Respondents have failed to meet their burden to prove by clear and convincing evidence that Gocho explicitly teaches or otherwise enables a person of ordinary skill in the art to make or use an inverse active area mask as required by element 5 of claim 1 of the '899 patent. I find that Gocho does not anticipate claim 1 of the '899 patent.

Claim 2 of the '899 patent requires "the inverse active area mask is biased so that the mask layer after patterning covers at least a portion of the sloping edges of the insulating layer in the active regions." (JX-8 at 9:25-28.)

Claim 7 of the '899 patent teaches "A method according to claim 1 further including the step of removing the mask layer after removing the exposed insulating material."

Because I have found that Gocho does not anticipate independent claim 1, it follows that it does not anticipate claims 2 or 7, which depend from claim 1. If an independent claim is found not anticipated/not obvious, then the dependent claim is necessarily not anticipated/not obvious by the same reference or combination of references. *In re Fritch,* 972 F.2d 1260, 1266 (Fed. Cir. 1992); *In re Royka*, 490 F.2d 981, 983-985 (C.C.P.A. 1974).

2. Sato

Respondents' Position: Respondents aver that U.S. Patent No. 5,242,853 to Sato et al. ("the '853 Patent" or "Sato") was filed on October 25, 1990 and issued on September 7, 1993. (RIB at 170-171 (citing RX-568).) Respondents assert that it is, therefore, prior art to the '899 patent. (*Id.* (citing RX-723 at Q. 254).) Respondents argue that all elements of claims 1, 2, 7-9, 14-16, and 21 of the '899 patent were disclosed or contained in Sato. Those claims are therefore invalid as anticipated under 35 U.S.C. § 102.[57] Respondents cite *In re Crish*, 393 F.3d 1253, 1256 (Fed. Cir. 2004) to say that the procedure for determining that an invention is anticipated is to "compare the construed claim to a prior art reference and make factual findings that 'each and every limitation is found either expressly or inherently in [that] single prior art reference.'" (*Id.*)

Respondents assert that Sato discloses a method of manufacturing a semiconductor device, and that it teaches techniques for making isolation trenches in a semiconductor substrate. (RIB at 171.) Respondents argue that Sato discloses using ECR-CVD to deposit filling material into trenches, and that it discloses depositing a photoresist mask layer covering the nonactive regions and part of the active regions. (*Id.*) They conclude that the exposed material is then etched away and the remaining surface flattened. (*Id.* (citing RDX-44; RX-723 at Q. 261-267).)

[57] Although Respondents assert that Sato anticipates claims 1, 2, 7-9, 14-16 and 21 of the '899 patent, I note that of that list only claims 1, 2 and 7 are asserted. Inasmuch as, only asserted claims are relevant and material to the issues before me, this Initial Determination will only treat the anticipation issue as to claims 1, 2 and 7.

Respondents recite that claim 1 of the '899 patent requires "defining active and nonactive regions on the surface of the substrate." They argue that Sato discloses this limitation in Figures 1B, 3C, 4A, 5, 6A, 7, and 9, which show trenches 2 defining different areas on the substrate. (RIB at 171 (citing RX-568; RX-723 at Q. 258-269).) Respondents assert that a person of ordinary skill in the art would have recognized that the trenches are nonactive regions and the regions between the trenches are active regions. (*Id.* (citing RX-723 at Q. 269).)

Respondents note that claim 1 of the '899 patent requires "forming isolation trenches of varying widths the active regions comprising active regions of varying width in the non-active regions." They argue that a person of ordinary skill in the art would have recognized that Figures 1B, 3C, 4A, 5, 6A, 7, and 9 of Sato disclose isolation trenches of varying widths separated by active regions of varying widths. (RIB at 171-172 (citing RX-568; RX-723 at Q. 270).)

Respondents recite that claim 1 of the '899 patent then requires the following:

> [F]orming a layer of HDP-CVD insulating material of silicon oxide, wherein the HDP-CVD silicon oxide layer is non-planar and protrudes angularly above isolation trench edges forming sloping edges that slope away from the trench on the substrate by [HDP-CVD], the HDP-CVD layer substantially filling the trenches and covering the active regions.

Respondents argue that a person of ordinary skill in the art would have recognized that Sato discloses this limitation. (RIB at 171-172 (citing RX-723 at Q. 271).) They say Sato provides that "[a] bias ECR-CVD apparatus for carrying out the semiconductor device manufacturing process described with reference to FIGS. 1A to 1H will be described with reference to FIG. 2." (*Id.* (citing RX-568 at 5:48-51).) Respondents continue that Figures 1C, 4A, and 6A of Sato disclose the silicon oxide protruding angularly and sloping away from the trench, which the patent describes as having been deposited using ECR-CVD. (*Id.* (citing RX-723 at Q. 271).)

Respondents conclude that, when the '899 patent application was filed, a person of ordinary skill in the art would have recognized that the bias ECR-CVD method is a type of HDP-CVD. (*Id.* (citing Tr. 1452:20-1453:17 (referring to Francombe, Physics of Thin Film, which the '899 patent incorporates by reference for all purposes at JX-8 at 5:22-24); RX-723 at Q. 271).)

Respondents recite that the next step in claim 1 of the '899 patent requires "removing at least a portion of the insulating material covering the active regions." They assert that Sato discloses this limitation when it states, "[s]tep (D): As shown in FIG. 4D, the portions 3a of the insulating film which are formed in the active regions are removed by etching using the masks of the resist film 4." (RIB at 172 (citing RX-568 at 8:11-14; RX-723 at Q. 272).) Respondents argue that a person of ordinary skill in the art at the time would have recognized that the etching described in this step refers to a means of removing some of the insulating material covering the active regions. (*Id.* (citing RX-723 at Q. 272).)

Respondents say that the next step in claim 1 of the '899 patent requires "planarizing the surface of said substrate to expose the active regions." They argue that Sato discloses planarizing the substrate to expose the active regions. (RIB at 172 (citing RX-723 at Q. 273-274).) They state that Figure 6E shows the planarized surface of the substrate with the exposed active regions. (*Id.* (citing RX-568 at Fig. 6E; RX-723 at Q. 273-274).)

Respondents next assert that claim 1 of the '899 patent clarifies that "the removal of at least a portion of insulating material from the active regions" should provide "a planar topography." They say Sato discloses this claim element. (RIB at 172-173 (citing RX-723 at Q. 273-274).) They point to Figure 6E of Sato to show the planarized surface of the substrate with the exposed active regions. (*Id.* (citing RX-568 at Fig. 6E; RX-723 Q 273-74).) Respondents

argue that a person of ordinary skill in the art would have recognized that the disclosed flattened substrate has a planar topography. (*Id.* (citing RX-723 at Q. 273-274).)

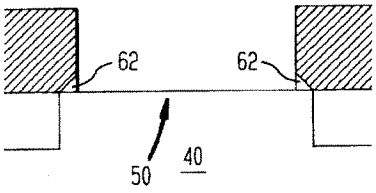
Respondents recite that claim 1 of the '899 patent further explains that "removing at least a portion of the insulating material from the active regions" means first "depositing a mask layer over the insulating material." They refer to Figures 1F, 4C, 6C, 8A, and 8B of Sato and assert they all show a photoresist mask layer above insulating materials. (RIB at 173.) Respondents say Figure 8A of Sato shows a mask layer labeled 4 over insulating material 5 and argue that Sato discloses this limitation of claim 1. (*Id.* (citing RX-568; RX-723 at Q. 275).)

Respondents aver that the next step of "removing at least a portion of the insulating material from the active regions" of claim 1 of the '899 patent is "patterning the mask layer to expose at least a portion of the insulating material over the active regions." Respondents assert that the mask layers shown in Figures 1F, 4C, 6C, 8A, and 8B of Sato each have gaps where the insulating material over the active regions is exposed. (RIB at 173.) They argue that a person of ordinary skill in the art would have recognized that these gaps are due to patterning. (*Id.* (citing RX-568; RX-723 at Q. 276).)

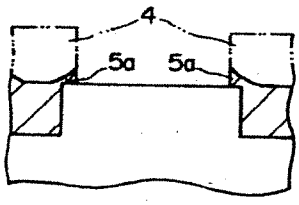
Respondents state that the final step in "removing at least a portion of the insulating material from the active regions" in claim 1 of the '899 patent requires "removing the exposed portion of the insulating material over the active regions, leaving unexposed portions of the insulating materials." Respondents say Figure 8A of Sato shows the result of removing the exposed insulating material while leaving the unexposed portions. (RIB at 173-174.) Respondents state that Figure 8A shows the removal of insulating materials over the active regions using an anisotropic etch. (*Id.*) The etch step removes the exposed portions of insulating material 5 — not shown in Figure 8A because they have been etched away — but leaves the

unexposed portions, portions 5a, of the insulating material. (*Id.* (citing RX-568 at Fig. 8A; RX-723 at Q. 277).) Respondents say that Dr. Bravman explained during the hearing that Figure 8A of Sato merely shows an alternative embodiment of the method shown in Figures 1A through 1H. (*Id.* (citing Tr. at 1265:3-18).) Respondents argue that the result of the etching step shown in Figure 8A of Sato is "virtually identical" to the result of the etching step shown in Figure 4B of the '899 patent, as shown below.

Sato, Fig. 8A (excerpt)



'899 Patent, Fig. 4B (excerpt)



(RIB at 173-174 (citing RX-568 at Fig. 8A; JX-8 at Fig. 4B; RX-723 at Q. 277).)

Respondents conclude that claim 1 of the '899 patent requires that "the mask layer is deposited using an inverse active area mask that is biased so that the mask layer after patterning covers the non-active regions and at least a portion of the active regions." They allege that the mask layers shown in Figures 1F, 4C, 6C, 8A and 8B of Sato were deposited using an inverse active area mask. (RIB at 174.) Respondents say that the resist in these figures is deposited over the isolation trenches and extends above the active regions. (*Id.* (citing RX-568; RX-723 at Q. 278-280).) They argue that a person of ordinary skill in the art would have understood that this pattern is achieved using an inverse active area mask and would have recognized that the photoresist patterns shown in these figures would have required a bias to cause the inverse mask to intrude into the active areas. (*Id.* (citing RX-723 at Q. 280).)

Respondents recite that claim 2 of the '899 patent states, "the inverse active area mask is biased so that the mask layer after patterning covers at least a portion of the sloping edges of the

insulating layer in the active regions." They argue that Sato discloses this limitation. (RIB at 174-175 (citing RX-568; RX-723 at Q. 281-282).) Respondents say that Figure 8A of Sato clearly shows that the photoresist mask layer (labeled 4) covers the sloping edges of the insulating layer (labeled 5a) in the active regions and therefore discloses this limitation. (*Id.* (citing RX-723 at Q. 282).)

Respondents add that Figures 1F, 4C, and 6C indicate that the photoresist mask covers the sloping edges. (RIB at 175.) Respondents allege that although these figures appear to show the insulating material above the active areas as having been etched away from the edge of the isolation trench, a person of ordinary skill in the art would have realized that the masking technique shown in Figure 8A could have been used instead. (*Id.*) They argue he would have known the difficulties of precisely etching away the insulating material at the edges of the active areas and would have recognized that the margin of error for mask alignment could be improved by using the Figure 8A technique. (*Id.*) Respondents argue that a person of ordinary skill in the art would have realized that biasing the mask layer to extend over at least a portion of the sloping edges of the insulating layer in the active regions would solve any precision etching difficulties or mask alignment issues that might be encountered in implementing the method disclosed by Sato. (*Id.* (citing RX-723 at Q. 282).)

Respondents recite that claim 7 of the '899 patent adds the additional step of "removing the mask layer after removing the exposed insulating material." Respondents argue that Sato discloses this limitation by stating, "[a]s shown in FIG. 6E, the resist film 4 is then removed." (RIB at 175 (citing RX-568 at 2:7-8; RX-723 at Q. 291-292).) Respondents continue that Sato also discloses this limitation by stating, "[s]tep (H): As shown in FIG. 1H, the resist film 4 is removed . . . ." (*Id.* (citing RX-568 at 4:61-62).) Respondents conclude that Sato further teaches

this step by stating, "[s]ubsequently, the resist film 4 is removed . . . ." (*Id.* (citing RX-568 at 8:15; RX-723 at Q. 291-292).)

In their reply brief, Respondents note that Qimonda criticizes Respondents' reliance on Figure 8A of Sato, because Sato describes the embodiment represented in that figure as undesirable (specifically, because small wedges of insulating material are left after an etch step). (RRB at 76-77 (citing CIB at 135).) Respondents argue that the fact that an embodiment is described as not desirable is immaterial to the anticipation analysis. (*Id.*) They say the Sato patent discloses the embodiment of Figure 8A, and that is enough for anticipation. (*Id.*)

Qimonda's Position: Qimonda's argument regarding Sato's alleged anticipation of the '899 patent was treated in tandem with its argument for Gocho, in both its initial and reply briefs, and the repetitive portions will not be repeated here.

In addition to its arguments made in tandem, Qimonda says that claim 23 of the '899 patent requires a chemical mechanical polishing (CMP) step.[58] Qimonda asserts that there is no dispute that the context of the '899 Patent is CMP, and that a key stated purpose of the invention is to shorten a final CMP planarizing step, quoting:

> Q: … And just so it's clear, there's really no dispute that a key stated purpose in the '899 invention is to shorten the time needed for CMP, correct?
> A: I agree with you.

(CIB at 134-135 (citing Tr. at 1246:13-17).) Qimonda continues that there is also no dispute that Sato fails to disclose the use of a CMP step:

> Q: … Now, Doctor, contrary to the stated purpose of the '899 patent, the Sato '853 patent doesn't even disclose the use of a CMP step; isn't that correct?
> A: CMP is not disclosed in the Sato patent, that's correct.

[58] The parties agree that the terms "chemical *metal* polishing" and "chemical *mechanical* polishing" are used synonymously in the asserted claims, and I shall treat them accordingly.

(CIB at 134-135 (citing Tr. at 1246:20-24; CX-1046 at Q. 101-102, 122-123).) Qimonda says the emphasis of Sato is on planarization without the use of CMP. (*Id.* (citing RX-568 at 2:56-64; CX-1046 at Q. 134).) Qimonda alleges that the filing of Sato predates the adoption of CMP by the semiconductor industry. (*Id.* (citing CX-1046 at Q. 101-102).)

Qimonda asserts that to obtain one of the key elements of the claim, Dr. Bravman relied on features that Sato describes as undesirable side-effects of an inferior prior art process. Qimonda states that to obtain the element "the photoresist overlies at least a portion of the angled oxide layer" as required by claim 22, Dr. Bravman relied on Figure 8A, quoting:

> Q: ...What you relied on in your anticipation opinion to show a portion of the sloping edges of the insulating layer being covered is figure 8A, correct?
> A: This figure 8A, yes.

(CIB at 135 (citing Tr. at 1257:25-1258:3).) Qimonda argues that Sato "clearly disparages the embodiment which includes Figure 8A as a problematic prior art process, which does not actually produce a planarized surface." (*Id.* (citing RX-568 at 2:25-53, 3:56-61, 4:38-41; CX-1046 at Q. 105; Tr. at 1250:17-1251:25, 1252:13-17).) Qimonda points out that claim 22 also requires a step of "planarizing the surface of the substrate," and says Dr. Bravman had to rely on the inventor's proposed solution, as shown in other embodiments of Sato, such as for example the one depicted in Figures 1A through 1E. (*Id.* (citing RX-568 at 2:25-53, 2:56-64, 3:38-41, 3:56-61; Tr. at 1253:10-17).) Qimonda states that in those embodiments, no oxide is present under a photoresist mask. (*Id.* (citing RX-568 at 3:17-22, 4:44-47, 4:65-68, 5:1-14; Tr. at 1253:18-1254:23).) Qimonda says that Dr. Bravman was "forced to cobble together the problem *and* its solution," which they argue is improper. (*Id.*) Qimonda concludes that by disparaging the prior art process of Figures 6A-6E and 8A, and teaching the elimination of all oxide under

the photoresist mask, the Sato patent clearly teaches away from the method of the '899 patent. (*Id.*)

Qimonda asserts that Sato addresses the problems of pre-CMP technology, and proposes a solution that does not involve CMP. (CIB at 136.) Qimonda argues that the inventors of the Sato patent proposed a complex process, with a sequence of two plasma etch steps, because CMP was not available. (*Id.* (citing CX-1046 at Q. 134).) Qimonda reasons that to append a CMP step to the end of the process described in Sato would have defeated the purpose of employing CMP, which rendered unnecessary "those complex plasma-etch-based processes." (*Id.* (citing CX-1046 at Q. 136-137).)

Commission Investigative Staff's Position: Staff expresses the opinion that Sato does not anticipate the asserted claims of the '899 patent by clear and convincing evidence. (SIB at 54.) Staff does not believe that the evidence clearly and convincingly discloses that Sato (1) teaches or suggests the use of a "silicon oxide layer formed in an inductively coupled high density plasma chamber by chemical vapor deposition" as required by claim 22; and (2) an inverse active area mask that is biased. (*Id.*) Staff notes that Sato was specifically considered by the patent examiner and thus, his decision is afforded a high degree of deference. (*Id.* (citing *Power Oasis, Inc.*, 522 F. 3d at 1304).)

Staff asserts that on cross-examination, Dr. Bravman admitted that Sato discloses only ECR-CVD plasma and consequently does not describe or disclose an inductively coupled plasma as required by claim 22. (SIB at 54-55 (citing Tr. at 1223, 1247).) Staff states that Dr. Bravman explained that "a worker of skill would understand that inductively coupled is used to differentiate from ECR … [and therefore] ECR is not, in the way the phrase is used here, inductively coupled." (*Id.* (citing Tr. at 1223).) Staff adds that Dr. Gutmann, Qimonda's expert,

opined that the "Sato patent teaches a manufacturing process that relies on ECR-CVD … [and that] a person of ordinary skill in the art at the time [of] [*sic*] the '899 was filed would have understood that ECR-CVD is not the same as, or even interchangeable with, HDP-CVD." (*Id.* (citing CX-1046C at Q. 120).) Staff continues that Dr. Gutmann explained , "[a]n ECR plasma chamber has a completely different configuration from an inductively coupled chamber … the ECR effect requires a strong, constant magnetic field, which is usually proved [sic] by electromagnets. Instead of using inductive coupling to feed energy to the plasma, ECR-CVD uses a microwave source to inject radio waves into the plasma … It's a completely different physical mechanism." (*Id.* (citing CX-1046C at Q. 40).)

Staff adds that they do not believe the evidence clearly and convincingly shows that Sato discloses the use of a biased inverse active area mask as required by claims 1 and 22. (SIB at 55.) Staff avers that on cross-examination Dr. Bravman admitted that Sato does not explicitly disclose how to generate a biased inverse active area mask from the original area mask. (*Id.* (citing Tr. at 1243, 1250).) Staff says Dr. Gutmann opined that a biased inverse active area mask was not disclosed in Sato and that one of ordinary skill would not consider such a mask inherent from the disclosure. (*Id.* (citing CX-1046C at Q. 121).)

Discussion and Conclusion: Based on the evidence before me, I find that Respondents have failed to meet their burden to prove by clear and convincing evidence that Sato anticipates claims 1, 2, or 7 of the '899 patent.

Sato was filed on October 25, 1990, and claims priority to an application from October 25, 1989. Sato issued on September 7, 1993, making it prior art under 35 U.S.C. § 102(b).

The two disputed issues regarding whether or not Sato anticipates the '899 patent include: (1) whether or not Sato discloses the limitation of element 3 of claim 1 which requires:

> [F]orming a layer of HDP-CVD insulating material of silicon oxide, wherein the HDP-CVD silicon oxide layer is non-planar and protrudes angularly above isolation trench edges forming sloping edges that slope away from the trench on the substrate by [HDP-CVD], the HDP-CVD layer substantially filling the trenches and covering the active regions.

and (2) whether or not Sato discloses the limit of element 5(c) of claim 1 which requires use of a biased inverse active area mask.

First, Qimonda and Staff base their argument regarding element 3 of claim 1 on the proposed construction of the term "HDP-CVD insulating material of silicon oxide" and assert that the term requires that the material be an "inductively coupled plasma." The construction of the term applied in this case, however is "an insulating material of silicon oxide deposited using a high density plasma-enhanced chemical vapor deposition process," and the construction is not limited to require "inductively coupled plasma."[59]

Qimonda and Staff argue that Sato discloses only one type of oxide deposition technique, electron cyclotron resonance chemical vapor deposition (ECR-CVD). Qimonda argues that since the requirement for HDP-CVD silicon oxide deposition requires "inductively coupled plasma" to be used, ECR-CVD cannot anticipate this limit of claim 1. (CIB at 129-130; SIB at 54-55.) Respondents agree that Sato, discloses the use of ECR-CVD. (RIB at 172.) Thus, it is undisputed that Sato discloses the use of ECR-CVD.

The evidence in the record clearly and convincingly supports a finding that the term "HDP-CVD insulating material of silicon oxide" includes material deposited using the ECR-CVD method. The '899 patent incorporates by reference Francombe, *Physics of Thin Film*, Academic Press (1994) ("Francombe"). (JX-8 at 5:22-24.) Dr. Bravman, Respondents' expert, testified that "a person of ordinary skill would have recognized … that the bias ECR-CVD method is unequivocally a type of HDP-CVD." (RX-723 at Q. 167.) At the hearing, Qimonda's

[59] The rationale for this construction is set forth in full in section III.D.1.

expert, Dr. Gutmann confirmed that ECR-CVD is identified in Francombe as an HDP-CVD process. (Tr. at 1452:20-1453:17.)

Based on the foregoing, I find that Sato discloses the limit in element 3 of claim 1 of the '899 patent.

Second, Respondents argue that Sato discloses the limit of claim 1 of the '899 patent that teaches "the mask layer is deposited using an inverse active area mask that is biased so that the mask layer after patterning covers the non-active regions and at least a portion of the active regions." Respondents state that the mask layers shown in Figures 1F, 4C, 6C, 8A and 8B of Sato were deposited using an inverse active area mask. Respondents say that the resist in these figures is deposited over the isolation trenches and extends above the active regions. (RIB at 147 (citing RX-568; RX-723 at Q. 278-280).) The resist in these figures is deposited over the isolation trenches and extends above the active regions. (*Id.* (citing RX-568; RX-723 at Q. 278-280).) A person of ordinary skill in the art would have understood that this pattern is achieved using an inverse active area mask. (*Id.* (citing RX723 at Q. 280).) The person of ordinary skill in the art would also have recognized that the photoresist patterns shown in these figures would have required a bias to cause the inverse mask to intrude into the active areas. (*Id.* (citing RX723 at Q. 280).)

At the hearing, however, Respondents' expert conceded, albeit somewhat reluctantly, that neither Gocho nor Sato explicitly disclose a biased inverse active area mask. (Tr. at 1236:8-1237:22, 1243:11-16.) Dr. Bravman admitted that he had not cited any reference in his direct testimony existing before the '899 patent was filed that explicitly described the generation of an inverse active area mask. (*Id.* at 1243:17-23.)

At the hearing, Dr. Bravman admitted that Sato does not explicitly disclose the claimed invention in which an inverse active area mask is used to remove at least a portion of the insulating layer from the active area regions as claimed. He also admitted that Sato does not explicitly teach the use of biasing an active area mask. (*Id.* at 1243:11-23, 1247:13-24, 1250:11-16.)

Dr. Gutmann in his direct testimony described, *inter alia*, that an inverse active area mask is a mask that is obtained from the active area mask using an inversion step in which the clear and opaque areas of the mask are reversed. (CX-202C at Q. 83-84.) By contrast, Dr. Bravman conceded both at his deposition and at the trial that there are many ways to create a photoresist pattern, and an inverse active area mask is merely one of the many possible ways. (Tr. at 1236:8-14,[60] 1249:24-1250:10.)

Respondents cite *In re Crish*, 393 F.3d 1253, 1256 (Fed. Cir. 2004) to say that the procedure for determining that an invention is anticipated is to "compare the construed claim to a prior art reference and make factual findings that 'each and every limitation is found either expressly or inherently in [that] single prior art reference.'" (RIB at 155.) Qimonda argues that the law is clear and undisputed that the claimed invention of a patent can be "anticipated" only where a single prior art reference "by itself" discloses each and every one of the claim limitations. (CIB at 334-335 (citing *Helifix Ltd. v. Blok-Lok Ltd.*, 208 F.3d 1339, 1346 (Fed. Cir. 2000); *Studiengesellschaft Kohle, m.b.H. v. Dart Industries, Inc.*, 726 F.2d 724 at 726-727 (Fed. Cir. 1984)).)

The court in *Helifix,* said that "to be anticipating, a prior art reference must disclose 'each and every limitation of the claimed invention[,] ... must be enabling[,] and [must] describe ... [the] claimed invention sufficiently to have placed it in possession of a person of ordinary skill in

[60] Although the question here referred to Gocho, the relevant part of the answer is not limited to Gocho.

the field of the invention.'" *Helifix*, 208 F.3d at 1346 (citing *In re Paulsen*, 30 F.3d 1475, 1478-79 (Fed.Cir.1994).)

In the case at hand, the evidence indicates that an inverse active area mask is a mask that is obtained from the active area mask using an inversion step in which the clear and opaque areas of the mask are reversed. Thus, it is a specific type of mask derived from reversing its predecessor. The evidence shows that Sato, however, does not refer to an "inverse active area mask" and does not teach or suggest making or using one. Instead Sato teaches only one step of masked etching in each of Figures 1F (RX-568 at 4:55-57), 4C (RX-568 at 8:8-10), 6C (RX-568 at 1:66-2:2). Sato does not teach a masked etching process in Figure 8A[61] which is an anisotropic etching step, and only hints at one in Figure 8B, in which case it, too, would be only a single masked etching step. (RX-568 at 2:39-52.)

Based upon the foregoing, I find that Respondents have failed to meet their burden to prove by clear and convincing evidence that Sato explicitly teaches or otherwise enables a person of ordinary skill in the art to make or use an inverse active area mask as required by element 5 of claim 1 of the '899 patent. I find that Sato does not anticipate claim 1 of the '899 patent.

Claim 2 of the '899 patent requires "the inverse active area mask is biased so that the mask layer after patterning covers at least a portion of the sloping edges of the insulating layer in the active regions." (JX-8 at 9:25-28.)

Claim 7 of the '899 patent teaches "[a] method according to claim 1 further including the step of removing the mask layer after removing the exposed insulating material."

Because I have found that Sato does not anticipate independent claim 1, it follows that it does not anticipate claims 2 or 7, which depend from claim 1. If an independent claim is found

[61] Although Qimonda criticizes Respondents' use of this example, because it discusses problems addressed by Sato, the issue here is disclosure. Disclosure, even when couched in disparaging terms, remains disclosure. Nevertheless, Figures 8A and 8B fail to disclose an inverse active area mask. (RX-568.)

not anticipated/not obvious, then the dependent claim is necessarily not anticipated/not obvious by the same reference or combination of references. *In re Fritch,* 972 F.2d 1260, 1266 (Fed. Cir. 1992); *In re Royka*, 490 F.2d 981, 983-985 (C.C.P.A. 1974).

3. Gocho In Combination With Francombe

Respondents' Position: Respondents recite that the first step in claim 22 of the '899 patent requires:

> [D]epositing a silicon oxide layer formed in an inductively coupled high density plasma chamber by chemical vapor deposition so as to fill said trenches and cover the surface of the substrate, thereby forming a non-planar layer over the surface that angles away from the edges of the trenches.

Respondents argue that a person of ordinary skill in the art would have recognized that this limitation is either disclosed by Gocho or obvious in light of Francombe, Physics of Thin Film, which is incorporated by reference into the '899 patent for all purposes. (RIB at 185-186 (citing JX-8 at 5:22-24; RX-723 at Q. 242-243; Tr. at 1452:20-1453:17).) Respondents aver that Gocho states:

> The foregoing objects are attained by the present invention, concerning a method of manufacturing a semiconductor device, wherein the burying material is silicon dioxide and a bias ECR-CVD process is used for the formation of the burying material.

(RIB at 185-186 (citing RX-598 at 5:8-12).) Respondents argue that Dr. Gutmann, Qimonda's expert, testified with reference to Francombe, that "inductively coupled" and "ECR" sources are two well-known types of high density plasma sources. (*Id.* (citing Tr. at 1452:20-1453:17).) Respondents state that a comparison of Fig. 2B of the '899 patent and Fig. 2(a) of Gocho shows the identical results achieved by these two methods of HDP-CVD. (*Id.* (citing JX-8 at Fig. 2B; RX-598 at Fig. 2(a).) Respondents reason that replacing one well-known HDP-CVD method, the ECR-CVD method of Gocho, with another well-known type of HDP-CVD, inductively-

coupled HDP-CVD, would have been obvious to a person of ordinary skill in the art in light of the teachings of Francombe. (*Id.* (citing RX-723 at Q. 242-243; Tr. at 1452:20-1453:17).)

Respondents recite that the next step in claim 22 of the '899 patent requires "depositing a photoresist layer on the oxide layer and patterning the photoresist layer with an inverse active area mask while biasing the layer so that the photoresist overlies at least a portion of the angled oxide layer." Respondents refer to Figures 1(b), 2(b), 5(b), 6(c), 9(c), 10(d), and 13(a) of Gocho, saying that all show a photoresist mask layer. Respondents say these "mask layers rest above insulating material." (RIB at 186.) Respondents argue that the mask layers shown in Figures 1(b), 2(b), and 9(c) of Gocho were deposited using an inverse active area mask, "as described in more detail in connection with claim 1, above." (*Id.* (citing RX-598; RX-723 at Q. 244-247).)

Respondents recite that the next step in claim 22 of the '899 patent requires "removing the silicon oxide in the exposed regions." They say Gocho discloses this limitation. Respondents point to Figure 2(c) of Gocho to show the result of removing the exposed insulating material while leaving the unexposed portions (11 and 50). (RIB at 186-187 (citing RX-598; RX-723 at Q. 248).) Respondents argue that although Figure 2(c) of Gocho shows that some of the unexposed oxide (i.e. the oxide below the photoresist mask) has been removed due to the use of a wet etch, claim 1 does not require leaving all of the unexposed oxide. (*Id.*) Respondents contrast this language with the claim language requiring removal of all the exposed oxide because of the use of the definite article in "removing the exposed portion." (*Id.*) They point out that the language requiring leaving unexposed portions does not use a definite article when it states "leaving unexposed insulating material." (*Id.*) They conclude that claim 1 does not require leaving all the "unexposed portions of the insulating material." (*Id.*)

Respondents recite that the next step in claim 22 of the '899 patent requires "removing the photoresist." They argue that Gocho discloses this limitation by stating, "[i]sotropic etching is conducted to etch the buying material 5d on the wide (long) protrusion region (1) . . . . Subsequently, the resist is removed. Thus, a structure as shown in FIG. 4(c)[sic] is obtained." (RIB at 187 (citing RX-598 at 11:4-14; RX-723 at Q. 249).) Respondents argue that a person of ordinary skill in the art would recognize that removing the resist is a method of removing the mask layer and would recognize that the statement refers to Figure 2(c). (*Id.* (citing RX-723 at Q. 249).)

Respondents aver that the final step in claim 22 of the '899 patent is "planarizing the surface of the substrate." They continue that Figure 2(c) of Gocho shows the results of removing the exposed insulating material while leaving unexposed portions (11 and 50). (RIB at 187 (citing RX-598; RX-723 at Q. 250).) Respondents argue that the "unexposed portions" are removed in Figure 2(d) by planarization and Gocho explains:

> Portions 50 of a protruding shape formed by isotropic etching in the step (3) above are eliminated by polishing. In this case, since flattening can be attained by flattening on the protrusion portions 50, the polishing time is shorter.

(RIB at 187 (citing RX-598 at 11:16-19).) Respondents say that a person of ordinary skill in the art would have recognized that the described flattening by polishing is planarization. (*Id.* (citing RX-723 at Q. 250).)

Respondents assert that claim 23 of the '899 patent adds the limitation that "the surface of the substrate is planarized by removing the remaining silicon oxide by chemical metal polishing." They say Figure 2(c) of Gocho shows the results of removing the exposed insulating material while leaving unexposed portions (11 and 50). (RIB at 187-188.) Respondents aver

that these unexposed portions are removed in Figure 2(d) by planarization. (*Id.* (citing RX-598; RX-723 at Q. 251-252).) They quote Gocho:

> Portions 50 of a protruding shape formed by isotropic etching in the step (3) above are eliminated by polishing. In this case, since flattening can be attained by flattening on the protrusion portions 50, the polishing time is shorter.

(RIB at 187-188 (citing RX-598 at 11:16-19).) Respondents argue that a person of ordinary skill in the art would have recognized that the standard method of polishing at the time of the '899 patent was to use CMP (i.e. chemical mechanical polishing) and would have recognized that "chemical metal polishing" is another name for chemical mechanical polishing. (*Id.*) They add that Figure 3 of Gocho shows a CMP device. (*Id.* (citing RX-598; RX-723 at Q. 251-252).)

In their reply brief, Respondents assert that claims 22 and 23 specifically require an inductively-coupled HDP-CVD plasma source: "depositing a silicon oxide layer formed in an inductively coupled high density plasma [HDP] chamber by chemical vapor deposition [CVD]." (RRB at 74 (citing JX-8 at 12:1-3).) Respondents say that Qimonda argues that Gocho (RX-598) and Sato (RX-568) do not show an inductively-coupled plasma source. (*Id.* (citing CIB at 129-131).) Respondents say that argument "ignores the fact that it would have been obvious to replace an ECR plasma source with an inductively-coupled HDP-CVD plasma source." (*Id.*)

Respondents argue that the obviousness of such a substitution is supported by the prior art cited in, and incorporated by reference into, the '899 patent, Francombe, Physics of Thin Film, Academic Press (1994). (RRB at 74-75 (citing JX-8 at 3:17-24).) Respondents say that Francombe illustrates what persons of skill in the art knew about HDP-CVD sources when the '899 patent was filed. (*Id.*) Respondents argue that Qimonda's expert acknowledged that Francombe describes "ECR" and "Inductively Coupled" as simply two types of HDP-CVD. (*Id.* (citing Tr. at 1452:20-1453:17).) Respondents conclude that although ECR was the prevalent

HDP-CVD technique when Gocho and Sato were filed, by the time the '899 patent was filed, other techniques were well known, including "inductively coupled" techniques. (*Id.*) They argue that substituting the ECR HDP-CVD technique disclosed in Gocho and Sato with an inductively-coupled HDP-CVD technique would have been obvious. (*Id.*)

Qimonda's Position: Qimonda argues generally, regarding all of the obviousness arguments presented by the Respondents herein, that in their post-trial brief Respondents attempt to introduce entirely new obviousness defenses and prior art (Francombe) for both claims. (CRB at 65-66.) Qimonda asserts that these arguments lack any basis in the record; they were never raised by Respondents, their expert or any sponsoring witness prior to or at trial; and, they violate the Administrative Law Judge's ruling on precisely this issue. (*Id.*)

Qimonda states that at trial, Respondents admitted that neither they nor their expert ever made any reference to Francombe, or to any prior art reference or combination that teaches inductively coupled plasma. Qimonda points out that following its objections at trial, the Administrative Law Judge struck the "catch-all" obviousness testimony of Respondents' expert in its entirety. (CRB at 66-67 (citing Tr. at 1276:3-10, 1277:22-24, and "generally 1272-1277"; CX-723 at Q. 357).) Qimonda states that the "Administrative Law Judge also squarely rejected Respondents' attempt to sneak these new obviousness arguments and prior art into the record at trial," quoting:

> MR. CICCARELLI: There's one more issue, Your Honor, I would like to bring to the Court's attention. That is Dr. Gutmann, which is their expert, for the first time in his rebuttal witness statement referred to the textbook [Francombe] that's referenced in the patent and used figures from that textbook to make an argument about inductively coupled plasma sources. The first time we saw it was in his rebuttal witness statement. Never saw it before. And so that might explain the reason of the specificity of some of these opinions. He had clearly placed a place holder and then he — Dr. Gutmann came back with some brand-new opinions.
>
> JUDGE ROGERS: Was this part of the prior art, the identified prior art?

MR. CICCARELLI: Yes, as described in the patent itself.

JUDGE ROGERS: Then your expert should have dealt with it.

(CRB at 66-67 (citing Tr. at 1276:12-1277:5).) Qimonda states that as a result of this ruling, Respondents were left with no evidence in the record to support their new obviousness arguments. Qimonda asserts that in their brief, Respondents cite Dr. Gutmann's testimony as support for their assertion that "replacing one well-known HDP-CVD method (the ECR-CVD method of Gocho) with another well-known type of HDP-CVD (inductively-coupled HDP-CVD) would have been obvious to a person of ordinary skill in the art in light of the teachings of Francombe." (*Id.* (citing RIB at 186).) Qimonda argues that Dr. Gutmann's testimony simply repeated the express disclosure of the '899 patent that both HDP-CVD techniques and electron cyclotron plasma are described in Francombe. (*Id.* (citing JX-8 at 5:22-24, 5:32-36).) Qimonda continues none of this rises to the level of a teaching or suggestion to modify Gocho or Sato to switch from ECR to incorporate an HDP-CVD. (*Id.*) Qimonda alleges that Respondents fail to mention or rebut Dr. Gutmann's testimony on the *non*-obviousness of claims 22 and 23. (*Id.*) Qimonda says Dr. Gutmann explained that the design of the ECR-CVD and HDP-CVD chambers is entirely different; that it would have taken a substantial effort to integrate an HDP-CVD chamber into a process using ECR-CVD; and that the substitution of ECR-CVD with HDP-CVD would have required a substantial amount of experimentation and adjustment of the entire process flow. (*Id.* (citing CX-1046 at Q. 41, 128).)

Qimonda alleges that the Francombe reference was not a reference that was "discussed in any way, shape or form" in Dr. Bravman's direct testimony or expert reports, quoting:

> [T]o the extent that the Administrative Law Judge or the Commission should find that any one of these references [Gocho or Sato] fails to show one or more elements of any of the claims, such prior art reference *could be combined with*

> *one of the other prior art references that I have discussed* to render the claim obvious. All of the *references that I discussed* deal with the formation of isolation trenches, and thus, it would have been logical for someone of ordinary skill in the art to *combine such references.*

(CRB at 66-67 (citing CX-723 at Q. 357; Tr. at 1276:3-10)) (emphasis added by Qimonda).

Commission Investigative Staff's Position: Staff did not present an argument on this issue.

Discussion and Conclusion: I find that, pursuant to Ground Rule 8.2, Respondents' arguments that claims 22 and 23 of the '899 patent are rendered obvious by Gocho and Francombe were abandoned by Respondents when they failed to include them in their pre-hearing brief and statement. Respondents' sole pre-hearing obviousness contention concerning the '899 patent and citing Gocho was in combination with Sato and is treated, *infra*. Nowhere in their pre-hearing brief did Respondents refer to claim 22 of the '899 patent.

The issue of Francombe was discussed at the hearing when Respondents admitted that neither they nor their expert ever made any reference to Francombe, or to any prior art reference or combination that teaches inductively coupled plasma. Qimonda points out that following its objections at trial, I struck the "catch-all" obviousness testimony of Respondents' expert in its entirety. (Tr. at 1272:14-1276:10, 1276:25-1277:6; 1277:17-24 (referring to RX-723 at Q. 357).) I rejected Respondents' attempt to raise new obviousness arguments. Respondents admitted that the issue related to identified prior art. Thus, their new argument does not meet the exception to the rule clearly stated in Ground Rule 8.2.

Based upon the foregoing, I find that Respondents' argument that claims 22 and 23 are obvious in light of Gocho in combination with Francombe was abandoned by Respondents and will not be considered in this Final Initial Determination.

Nevertheless, assuming *arguendo* that Respondents' argument was properly raised, I find that they have failed to prove by clear and convincing evidence that claim 22 of the'899 patent is obvious in light of Gocho in combination with Francombe.

Claim 22 of the '899 patent teaches:

> 22. A method of planarizing shallow isolation trenches in a substrate comprising:
>
> depositing a silicon oxide layer formed in an inductively coupled high density plasma chamber by chemical vapor deposition so as to fill said trenches and cover the surface of the substrate, thereby forming a non-planar layer over the surface that angles away from the edges of the trenches;
>
> depositing a photoresist layer on the oxide layer and patterning the photoresist layer with an inverse active area mask while biasing the layer so that the photoresist overlies at least a portion of the angled oxide layer;
>
> removing the silicon oxide in the exposed regions;
>
> removing the photoresist; and
>
> planarizing the surface of the substrate.

(JX-8 at 11:18-12:14.)

Respondents argue that a person of ordinary skill in the art[62] would have recognized that the limitation in element 1 of claim 22 is either disclosed by Gocho or obvious in light of Francombe. (RIB at 185-186 (citing JX-8 at 5:22-24; RX-723 at Q. 242-243; Tr. at 1452:20-1453:17).) Respondents refer to the language of Gocho that teaches a bias ECR-CVD process is used for the formation of the silicon oxide layer. (*Id.* (citing RX-598 at 5:8-12).) Respondents argue that Dr. Gutmann, Qimonda's expert, testified with reference to Francombe, that "inductively coupled" and "ECR" sources are two well-known types of high density plasma

[62] Respondents did not offer a definition of a person of ordinary skill in the art related to the '899 patent. Qimonda's expert, however, testified that a person of ordinary skill in the art would have a graduate degree in a relevant discipline (such as electrical engineering, materials science, chemical engineering, physics or mechanical engineering), and the person would have had two to four years experience in IC technology, specifically in CMP and/or IC process flows. (CX-1046 at Q. 12.)

sources. (*Id.* (citing Tr. at 1452:20-1453:17).) Respondents state that a comparison of Fig. 2B of the '899 patent and Fig. 2(a) of Gocho shows the identical results achieved by these two methods of HDP-CVD. (*Id.* (citing JX-8 at Fig. 2B; RX-598 at Fig. 2(a)).) Respondents reason that replacing one well-known HDP-CVD method, the ECR-CVD method of Gocho, with another well-known type of HDP-CVD, inductively-coupled HDP-CVD, would have been obvious to a person of ordinary skill in the art in light of the teachings of Francombe. (*Id.* (citing RX-723 at Q. 242-243; Tr. at 1452:20-1453:17).)

The evidence in the record clearly and convincingly supports a finding that the term "bias ECR-CVD" is included in Francombe as a type of HDP-CVD along with, among others, the "inductively coupled" plasma source. Dr. Bravman, Respondents' expert, testified that "a person of ordinary skill would have recognized … that the bias ECR-CVD method is unequivocally a type of HDP-CVD." (RX-723 at Q. 167.) At the hearing, Qimonda's expert, Dr. Gutmann confirmed that ECR-CVD is identified in Francombe as an HDP-CVD process. (Tr. at 1452:20-1453:17.)

While Respondents made no effort to show a reason to combine the prior art references, the evidence supports a finding that a person of ordinary skill in the art, reading Gocho's reference to "bias ECR-CVD" along with Francombe, would combine those references to arrive at the conclusion that inductively coupled high density plasma could be used to achieve the same result.

Based on the foregoing, I find that Gocho in combination with Francombe discloses element 1 of claim 22 of the '899 patent.

Second, Respondents argue that the combination of Gocho and Francombe discloses the limit of element 2 of claim 22 of the '899 patent that teaches "depositing a photoresist layer on

the oxide layer and patterning the photoresist layer with an inverse active area mask while biasing the layer so that the photoresist overlies at least a portion of the angled oxide layer." Respondents refer to Figures 1(b), 2(b), 5(b), 6(c), 9(c), 10(d), and 13(a) of Gocho, saying that all show a photoresist mask layer. (RIB at 186.) Respondents say these "mask layers rest above insulating material." (*Id.*) Respondents argue that the mask layers shown in Figures 1(b), 2(b), and 9(c) of Gocho were deposited using an inverse active area mask, "as described in more detail in connection with claim 1, above." (*Id.* (citing RX-598; RX-723 at Q. 244-247).)

As discussed in section V.D.1, *supra*, the evidence shows that Gocho does not refer to an "inverse active area mask" and does not teach or suggest making or using one. It merely instructs the reader to form a resist pattern to expose only the wide active area regions, and the evidence shows there are many ways to create a photoresist pattern. The record does not reflect that Francombe in any way teaches or suggests or otherwise mentions use of an inverse active area mask.

Based on the foregoing, I find that Respondents have failed to meet their burden to prove by clear and convincing evidence that element 2 of claim 22 of the '899 patent is disclosed in either Gocho or Francombe.

Respondents assert that claim 23 of the '899 patent, which depends from claim 22, adds the limitation that "the surface of the substrate is planarized by removing the remaining silicon oxide by chemical metal polishing." They say Figure 2(c) of Gocho shows the results of removing the exposed insulating material while leaving unexposed portions (11 and 50).

Because I have found that Gocho in combination with Francombe does not render obvious independent claim 22, it follows that it does not render obvious claim 23, which depends from claim 22. If an independent claim is found not anticipated/not obvious, then the dependent

claim is necessarily not anticipated/not obvious by the same reference or combination of references. *In re Fritch,* 972 F.2d 1260, 1266 (Fed. Cir. 1992); *In re Royka*, 490 F.2d 981, 983-985 (C.C.P.A. 1974).

Based upon the foregoing, I find that Respondents have failed to meet their burden to prove by clear and convincing evidence that Gocho in combination with Francombe renders obvious claims 22 or 23 of the '899 patent.

4. Sato In Combination With Francombe

Respondents' Position: Respondents recite that the first step in claim 22 of the '899 patent is:

> [D]epositing a silicon oxide layer formed in an inductively coupled high density plasma chamber by chemical vapor deposition so as to fill said trenches and cover the surface of the substrate, thereby forming a non-planar layer over the surface that angles away from the edges of the trenches.

Respondents argue that a person of ordinary skill in the art would have recognized that either Sato discloses this limitation or it is obvious in light of Francombe, Physics of Thin Film, which is incorporated by reference into the '899 patent for all purposes. (RIB at 188-189 (citing JX-8 at 5:22-24; RX-723 at Q. 343-344; Tr. at 1452:20-1453:17).) Respondents assert that Sato states "[a] bias ECR-CVD apparatus for carrying out the semiconductor device manufacturing process described with reference to FIGS. 1A to 1H will be described with reference to FIG. 2." (*Id.* (citing RX-568 at 5:48-51).) Respondents say Dr. Gutmann testified, "inductively coupled" and "ECR" sources are two well-known types of high density plasma (HDP) sources. (*Id.* (citing Tr. at 1452:20-1453:17).) Respondents state that a comparison of Fig. 2B of the '899 patent and Fig. 1C of Sato shows the identical results achieved by these two methods of HDP-CVD. (*Id.* (citing JX-8 at Fig. 2B; RX-568 at Fig. 1C).) Respondents reason that replacing the ECR-CVD method of Sato, which they say is one well-known type of HDP-CVD, with an inductively-

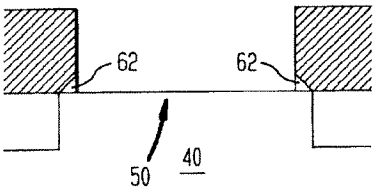
coupled method, which they characterize as "just another well-known type of HDP-CVD," would have been obvious to a person of ordinary skill in the art in light of the teachings of Francombe. (*Id.* (citing RX-723 at Q. 343-344; Tr. at 1452:20-1453:17).)

Respondents recite that the next step in claim 22 of the '899 patent requires "depositing a photoresist layer on the oxide layer and patterning the photoresist layer with an inverse active area mask while biasing the layer so that the photoresist overlies at least a portion of the angled oxide layer." Respondents allege that the mask layers shown in Figures 1F, 4C, 6C, 8A, and 8B of Sato were deposited using an inverse active area mask, as described in more detail in connection with claim 1, above. (RIB at 189 (citing RX-568 at Fig. 1F, 4C, 6C, 8A, and 8B; RX-723,[63] at Q. 345-347).)

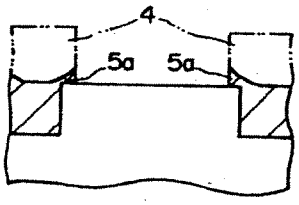
Respondents recite that the next step in claim 22 of the '899 patent requires "removing the silicon oxide in the exposed regions." They continue that Figure 8A of Sato shows the results of removing the exposed insulating material while leaving the unexposed portions. (RIB at 189-190 (citing RX-568; RX-723 at Q. 348).) Respondents indicate that Figure 8A shows the removal of insulating materials over the active regions using an anisotropic etch. (*Id.*) Respondents assert that the etch step removes exposed portions of insulating material 5, which they say is "not shown in Figure 8A because they have been etched away," but leaves the unexposed portions, portions 5a, of the insulating material. (*Id.*) Respondents say that Dr. Bravman explained during the hearing that, Figure 8A of Sato merely shows an alternative embodiment of the method shown in Figures 1A through 1H. (*Id.* (citing Tr. at 1265:3-18).) Respondents conclude that the result of the etching step shown in Figure 8A of Sato is virtually identical to the result of the etching step shown in Figure 4B of the '899 patent, as shown below.

[63] Respondents actually only cited the question numbers here; but research of RX-723 shows this to be the correct citation.

Sato, Fig. 8A (excerpt)



'899 Patent, Fig. 4B (excerpt)



(RIB at 189-190 (citing RX-568 at Fig. 8A; JX-8 at Fig. 5B; RX-723 at Q. 348).)

Respondents state that the next step in claim 22 of the '899 patent is "removing the photoresist," and Sato discloses this limitation where it states, "[a]s shown in FIG. 6E, the resist film 4 is then removed." (RIB at 190 (citing RX-568 at 2:7-8; RX-723 at Q. 349).) They say Sato also discloses this limitation by stating, "[s]tep (H): As shown in FIG. 1H, the resist film 4 is removed . . . ." (*Id.* (citing RX-568 at 4:61-62; RX-723 at Q. 349).) Respondents conclude that Sato further teaches this step by stating, "[s]ubsequently, the resist film 4 is removed . . . ." (*Id.* (citing RX-568 at 8:15; RX-723 at Q. 349).)

Respondents assert that the final step in claim 22 of the '899 Patent requires "planarizing the surface of the substrate" and that Sato discloses planarizing the substrate to expose the active regions. (RIB at 190 (citing RX-568; RX-723 at Q. 350).) Respondents cite as an example, Figure 6E to show the planarized surface of the substrate with the exposed active regions. (*Id.* (citing RX-723 at Q. 350).)

Respondents' argument in their reply brief treated both Gocho and Sato in combination with Francombe. Because the argument was made once and applies equally to the sections regarding "Gocho in Combination with Francombe" *supra* and this section (i.e. "Sato in Combination with Francombe"), I will not reiterate the argument or the discussion and conclusion.

Qimonda's Position: Qimonda's general argument regarding all of the obviousness arguments presented by the Respondents herein was stated in detail in the section, *supra*, on Gocho in Combination with Francombe, and it applies equally to all of the "obviousness" defenses. Therefore, I will not repeat the argument or the discussion and conclusion here. Qimonda did not provide a separate argument regarding the issue of Sato in Combination with Francombe.

Commission Investigative Staff's Position: Staff did not provide an argument regarding this issue.

Discussion and Conclusion: I find that, pursuant to Ground Rule 8.2, Respondents' argument that claim 22 of the '899 patent is rendered obvious by Sato in combination with Francombe was abandoned by Respondents when they failed to include it in their pre-hearing brief and statement. Respondents' pre-hearing obviousness contentions concerning the '899 patent and citing Sato included a general allegation of obviousness in light of Sato in combination with, *inter alia*, Gocho and an assertion that claim 23 was rendered obvious in light of Sato. Nowhere in their pre-hearing brief did Respondents refer to claim 22 of the '899 patent or to Francombe.

The issue of Francombe was discussed at the hearing when Respondents admitted that neither they nor their expert ever made any reference to Francombe, or to any prior art reference or combination that teaches inductively coupled plasma. Qimonda points out that following its objections at trial, I struck the "catch-all" obviousness testimony of Respondents' expert in its entirety. (Tr. at 1272:14-1276:10, 1276:25-1277:6, 1277:17-24 (referring to RX-723 at Q. 357).) I rejected Respondents attempt to raise new obviousness arguments. Respondents admitted that the issue related to identified prior art. Thus, their new argument does not meet the exception to

the rule clearly stated in Ground Rule 8.2.

Based upon the foregoing, I find that Respondents' argument that claim 22 is obvious in light of Sato in combination with Francombe was abandoned by Respondents and will not be considered in this Final Initial Determination.

Nevertheless, assuming *arguendo* that Respondents' argument was properly raised, I find that they have failed to prove by clear and convincing evidence that claim 22 of the'899 patent is obvious in light of Gocho in combination with Francombe.

Element 1 of claim 22 of the '899 patent teaches:

> depositing a silicon oxide layer formed in an inductively coupled high density plasma chamber by chemical vapor deposition so as to fill said trenches and cover the surface of the substrate, thereby forming a non-planar layer over the surface that angles away from the edges of the trenches;

Respondents argue that a person of ordinary skill in the art would have recognized that Sato in combination with Francombe, renders obvious claim 22 of the '899 patent. (RIB at 188-189 (citing JX-8 at 5:22-24; RX-723 at Q. 343-344; Tr. at 1452:20-1453:17).) Respondents assert that Sato states "[a] bias ECR-CVD apparatus for carrying out the semiconductor device manufacturing process described with reference to FIGS. 1A to 1H will be described with reference to FIG. 2." (*Id.* (citing RX-568 at 5:48-51).) Respondents say Dr. Gutmann testified, "inductively coupled" and "ECR" sources are two well-known types of high density plasma (HDP) sources. (*Id.* (citing Tr. at 1452:20-1453:17).) Respondents state that a comparison of Fig. 2B of the '899 patent and Fig. 1C of Sato shows the identical results achieved by these two methods of HDP-CVD. (*Id.* (citing JX-8 at Fig. 2B; RX-568 at Fig. 1C).) Respondents reason that replacing the ECR-CVD method of Sato, which they say is one well-known type of HDP-CVD, with an inductively-coupled method, which they characterize as "just another well-known

type of HDP-CVD," would have been obvious to a person of ordinary skill in the art in light of the teachings of Francombe. (*Id.* (citing RX-723 at Q. 343-344; Tr. at 1452:20-1453:17).)

The evidence in the record clearly and convincingly supports a finding that the term "bias ECR-CVD" is included in Francombe as a type of HDP-CVD along with, among others, the "inductively coupled" plasma source. Dr. Bravman, Respondents' expert, testified that "a person of ordinary skill would have recognized … that the bias ECR-CVD method is unequivocally a type of HDP-CVD." (RX-723 at Q. 167.) At the hearing, Qimonda's expert, Dr. Gutmann confirmed that ECR-CVD is identified in Francombe as an HDP-CVD process. (Tr. at 1452:20-1453:17.)

While Respondents made no effort to show a reason to combine the prior art references, clear and convincing evidence supports a finding that a person of ordinary skill in the art, reading Sato's reference to "bias ECR-CVD" along with Francombe, would combine those references to arrive at the conclusion that inductively coupled high density plasma could be used to achieve the same result.

Based on the foregoing, I find that Sato in combination with Francombe discloses element 1 of claim 22 of the '899 patent.

Respondents recite that the next step in claim 22 of the '899 patent requires "depositing a photoresist layer on the oxide layer and patterning the photoresist layer with an inverse active area mask while biasing the layer so that the photoresist overlies at least a portion of the angled oxide layer." Respondents allege that the mask layers shown in Figures 1F, 4C, 6C, 8A, and 8B of Sato were deposited using an inverse active area mask, as described in more detail in

connection with claim 1, above. (RIB at 189 (citing RX-568 Fig. 1F, 4C, 6C, 8A, and 8B; RX-723,[64] Q. 345-347).)

As discussed in section V.D.2, *supra*, the evidence shows that Sato does not refer to an "inverse active area mask" and does not teach or suggest making or using one. Instead Sato teaches only one step of masked etching in each of Figures 1F (RX-568 at 4:55-57), 4C (RX-568 at 8:8-10), 6C (RX-568 at 1:66-2:2). Sato does not teach a masked etching process in Figure 8A[65] which is an anisotropic etching step, and only hints at one in Figure 8B, in which case it, too, would be only a single masked etching step. (RX-568 at 2:39-52.) The record does not reflect that Francombe in any way teaches or suggests or otherwise mentions use of an inverse active area mask.

Based on the foregoing, I find that Respondents have failed to meet their burden to prove by clear and convincing evidence that Sato in combination with Francombe renders obvious claim 22 of the '899 patent.

5. Sato In Combination With Gocho

Respondents' Position: Respondents recite that claim 23 of the '899 patent requires that "the surface of the substrate is planarized by removing the remaining silicon oxide by chemical metal polishing." They argue that if Sato does not disclose planarizing the remaining silicon oxide by chemical mechanical polishing, a person of ordinary skill in the art at the time of the '899 patent would have found this step an obvious and trivial improvement over Sato in view Gocho. (RIB at 191 (citing RX-723 at Q. 352-355).) Respondents allege that Gocho discloses using a chemical mechanical polish to finalize the planarization of a surface that has remaining

[64] Respondents actually only cited the question numbers here; but research of RX-723 shows this to be the correct citation.

[65] Although Qimonda criticizes Respondents' use of this example, because it discusses problems addressed by Sato, the issue here is disclosure. Disclosure, even when couched in disparaging terms, remains disclosure. Nevertheless, Figures 8A and 8B fail to disclose an inverse active area mask. (RX-568.)

portions similar to those described by 5a in Figure 8A of Sato. (*Id.*) Respondents aver that Figure 2(c) of Gocho shows the results of removing the exposed insulating material while leaving unexposed portions 11 and 50. (*Id.* (citing RX-723 at Q. 355).) Respondents posit that these unexposed portions are removed in figure 2(d) by planarization: "(4) Portions 50 of a protruding shape formed by isotropic etching in the step (3) above are eliminated by polishing. In this case, since flattening can be attained by flattening on the protrusion portions 50, the polishing time is shorter." (*Id.* (citing RX-598 at 11:16-19).) Respondents argue that a person of ordinary skill would have recognized that the standard method of polishing at the time of the '899 patent was to use CMP — chemical mechanical polishing and would have recognized that "chemical metal polishing," as stated in claim 23 of the '899 patent, is another name for chemical mechanical polishing. (RIB at 191 (citing RX-723 at Q. 352-355).) Respondents add that Figure 3 of Gocho shows a CMP device. (*Id.* (citing RX-598 at Fig. 3).) They conclude that a person of ordinary skill would have recognized that the remaining portions indicated by 5a in figure 8A of Sato could be removed by the technique described in Gocho. (*Id.* (citing RX-723 at Q. 352-355).) Respondents quote Dr. Gutmann, "[o]ne must keep in mind that the process of Sato relies on the two etch steps to perfectly clear the active areas because there is no subsequent CMP step to finish off the oxide. If the lateral leveling etch leaves residues around the edges of the active areas those residues remain there at the end of the process and the surface is not planar." (*Id.* (citing CX-1046 at Q. 114).) Respondents say that this statement summarizes the reason a person of ordinary skill would incorporate the well-known technique of CMP planarization with the method taught by Sato, and the Gocho CMP step solves any issue with residual oxide. (*Id.*)

Respondents argue that any finding that Gocho and Sato do not anticipate a claim of the '899 patent should lead to a finding that they render that claim obvious in view of each other and "other pieces of prior art that teach methods of filling or planarizing shallow isolation trenches." (RIB at 191.) Respondents allege that any combination of these references would have been obvious to a person of ordinary skill in the art at the time of the invention of the '899 patent because of the common objectives taught by "the references." (*Id.*)

Respondents assert that Gocho and Sato are both directed to the planarization of shallow isolation trenches. (RIB at 192 (citing RX-598 at 1:9-12; RX-568 at 1:8-24).) Respondents continue that both teach planarizing insulating material deposited using HDP-CVD. (*Id.* (citing RX-598 at 4:5-13; RX-568 at 2:9-18).) Respondents say both "aim to achieve" complete filling of the trenches and a planar surface. (*Id.* (citing RX-598 at 3:29-35; RX-568 at 3:6-22).) Respondents reason that, because of the shared goals and means, combining the teachings from these patents would have been obvious to a person of ordinary skill in the art at the time of the '899 patent. (*Id.*) They add, the Gocho and Sato patents share inventors, noting Junichi Sato of Sony Corp. is a named inventor of Sato, and Tetsuo Gocho of Sony Corp. is a named inventor on both Gocho and Sato. (*Id.*)

Respondents conclude that a person of ordinary skill in the art would have found it obvious to combine any of the techniques taught by "these references" to achieve the objectives identified in those patents. (RIB at 192 (citing RX-723 at Q. 354-355).)

Respondents' argument in their reply brief treated both Gocho and Sato in combination with Francombe. Because the argument was made once and applies equally to the sections regarding "Gocho in Combination with Francombe" supra and this section (i.e. "Sato in Combination with Francombe"), I will not reiterate the argument or the discussion and

conclusion. I turn, therefore, to those portions of the Respondents' reply brief that are not already set forth, *supra*.

Respondents argue that, unlike claim 22, which specifically requires "inductively coupled" HDP-CVD, claims 1-21 have no such requirement. (RRB at 75.) They say claims 1-21 simply require HDP-CVD. Respondents state that Qimonda reads an "inductively coupled" requirement into the term HDP-CVD. Respondents argue that the inventor knew how to add such a requirement, because he included it in claim 22; but he left it out of claims 1-21. (*Id.*) Respondents assert that the inventor also explained that different types of HDP-CVD existed, quoting "HDP-CVD techniques are described in Francombe." (*Id.* (citing JX-8 at 5:22).) and that such techniques included both ECR and inductively coupled (*Id.* (citing Tr. at 1452:20-1453:17).) Respondents aver that the inventor also specifically acknowledged that ECR techniques could be used, reciting "[e]lectron cyclotron . . . techniques are also useful for depositing the oxide layer." (*Id.* (citing JX-8 at 5:33-35).) Respondents reason that because the inventor specifically required an "inductively coupled" HDP-CVD source in claim 22, but did not do so in claims 1-21, it means that HDP-CVD as used in claims 1-21 does not include the concept of "inductively coupled." (*Id.*) They conclude, because ECR is a type of HDP-CVD, Gocho and Sato teach the HDP-CVD limitation of the '899 patent. (RRB at 75 (citing Tr. at 1452:20-1453:17).)

Respondents note that Qimonda criticizes Respondents' reliance on Figure 8A of Sato because Sato describes the embodiment represented in that figure as undesirable (specifically, because small wedges of insulating material are left after an etch step). (RRB at 76-77 (citing CIB at 135).) Respondents argue that it is unimportant in the obviousness analysis. They say that although some may have considered the embodiment of Figure 8A to be undesirable when

the Sato patent was filed in 1990, this was only because CMP processes were not yet widely used. (*Id.*) Respondents allege that by the time of Gocho and the '899 patent, CMP was generally available, and the need to remove such small wedges would have no longer been undesirable. (*Id.*) Respondents assert that, Gocho, like the '899 patent, teaches removing small wedges using a CMP process. (*Id.* (citing RX-598 at 11:15-18).) Respondents conclude even if Sato teaches away from leaving the wedges, Gocho solves that problem by disclosing that they can easily be removed with CMP. (*Id.*)

Qimonda's Position: Qimonda's general argument regarding all of the obviousness arguments presented by the Respondents herein was stated in detail in the section, *supra*, on Gocho in combination with Francombe, and it applies equally to all of the "obviousness" defenses. Therefore, I will not repeat the argument or the discussion and conclusion here. Qimonda did not provide a separate argument regarding the issue of Sato in combination Gocho.

Commission Investigative Staff's Position: Staff refers to their arguments on anticipation as rationale for their position that Gocho in combination with Sato does not render claim 23 obvious. (SIB at 57.)

Discussion and Conclusion: I find that, pursuant to Ground Rule 8.2, Respondents' argument that claim 23 of the '899 patent is rendered obvious by Sato in combination with Gocho was not abandoned by Respondents, because they included that allegation in their pre-hearing brief and statement. I find, however, that Respondents' arguments in their reply brief that claims 1-21 and claim 22 of the '899 patent are rendered obvious by Sato in combination with Gocho were abandoned by Respondents when they failed to include this specific contention

in their pre-hearing brief and statement as required by Ground Rule 8.2.[66] Respondents do not mention claim 22 anywhere in their pre-hearing brief. While some fact situations might give rise to a need to make a close interpretation of the phrases in Ground Rule 8.2 that require the pre-trial brief to "set forth with particularity" a party's contentions on each of the proposed issues, the Respondents' pre-trial brief in this case is a textbook example of one that fails totally to set forth their contentions on the proposed issues with particularity. In fact, it fails to raise any specific issues on the subject of obviousness except as to claim 23.

Based upon the foregoing, I find that Respondents' argument that claim 22 is obvious in light of Sato in combination with Gocho was abandoned by Respondents and will not be considered in this Final Initial Determination.

Nevertheless, assuming *arguendo* that Respondents' argument was properly raised, I find that they have failed to prove by clear and convincing evidence that claim 22 of the'899 patent is obvious in light of Sato in combination with Gocho. In sections VI.D.1 through 4, *supra*, I examined both Gocho and Sato and determined that while both of them disclosed the teaching of element 1 of claim 22 of the '899 patent, neither of them, alone or in combination with Francombe, disclosed element 2 of claim 22. I will not repeat the detailed analyses of those prior art references here; but by this reference incorporate them in this section.

Neither Gocho, nor Sato, nor the two in combination with each other, teach, suggest or even hint at the use of an inverse active area mask, which is taught in element 2 of claim 22 of

[66] While Respondents in their reply brief argue that Sato in combination with Gocho renders claims 1-21 and claim 22 obvious, they do so in response to Qimonda's initial brief that anticipated these issues being raised by Respondents. Because those issues were abandoned by Respondents and were not included in their initial post-hearing brief, I decline to further treat them here. It is Respondents' burden to prove invalidity, and the burden of proof never shifts to the patentee to prove validity. *Scanner Techs. Corp. v. ICOS Vision Sys. Corp. N.V.*, 528 F.3d 1365, 1380 (Fed. Cir. 2008).

the '899 patent. I find that Respondents have failed to provide by clear and convincing evidence that Sato in combination with Gocho renders obvious claim 22 of the '899 patent.

Respondents assert that claim 23 of the '899 patent, which depends from claim 22, adds the limitation that "the surface of the substrate is planarized by removing the remaining silicon oxide by chemical metal polishing." They argue, persuasively, that if Sato does not disclose planarizing the remaining silicon oxide by chemical mechanical polishing, a person of ordinary skill in the art at the time of the '899 patent would have found this step an obvious and trivial improvement over Sato in view Gocho. (RIB at 191 (citing RX-723 at Q. 352-355).) Respondents allege that Gocho discloses using a chemical mechanical polish to finalize the planarization of a surface that has remaining portions similar to those described by 5a in Figure 8A of Sato. (*Id.*) Respondents aver that Figure 2(c) of Gocho shows the results of removing the exposed insulating material while leaving unexposed portions 11 and 50. (*Id.* (citing RX-723 at Q. 355).) Respondents posit that these unexposed portions are removed in figure 2(d) by planarization: "(4) Portions 50 of a protruding shape formed by isotropic etching in the step (3) above are eliminated by polishing. In this case, since flattening can be attained by flattening on the protrusion portions 50, the polishing time is shorter." (*Id.* (citing RX-598 at 11:16-19).) Respondents argue that a person of ordinary skill would have recognized that the standard method of polishing at the time of the '899 patent was to use CMP — chemical mechanical polishing and would have recognized that "chemical metal polishing," as stated in claim 23 of the '899, is another name for chemical mechanical polishing. (*Id.* (citing RX-723 at Q. 352-355).) Respondents add that Figure 3 of Gocho shows a CMP device. (*Id.* (citing RX-598 at Fig. 3).) They conclude that a person of ordinary skill would have recognized that the remaining portions indicated by 5a in figure 8A of Sato could be removed by the technique described in

Gocho. (*Id.* (citing RX-723 at Q. 352-355).) Respondents quote Dr. Gutmann, "[o]ne must keep in mind that the process of Sato relies on the two etch steps to perfectly clear the active areas because there is no subsequent CMP step to finish off the oxide. If the lateral leveling etch leaves residues around the edges of the active areas those residues remain there at the end of the process and the surface is not planar." (*Id.* (citing CX-1046 at Q. 114).) Respondents say that this statement summarizes the reason a person of ordinary skill would incorporate the well-known technique of CMP planarization with the method taught by Sato, and the Gocho CMP step solves any issue with residual oxide. (*Id.*)

I find that Respondents have shown by clear and convincing evidence that Sato in combination with Gocho discloses the CMP limitation found in claim 23 of the '899 patent.

Nevertheless, because I have found that Sato in combination with Gocho does not render obvious independent claim 22, it follows that it does not render obvious claim 23, which depends from claim 22. If an independent claim is found not anticipated/not obvious, then the dependent claim is necessarily not anticipated/not obvious by the same reference or combination of references. *In re Fritch*, 972 F.2d 1260, 1266 (Fed. Cir. 1992); *In re Royka*, 490 F.2d 981, 983-985 (C.C.P.A. 1974).

Based upon the foregoing, I find that Respondents have failed to meet their burden to prove by clear and convincing evidence that Sato in combination with Gocho renders obvious claims 22 or 23 of the '899 patent.

E. The '918 Patent

1. Nye

Respondents' Position: Respondents argue that U.S. Patent No. 6,261,945, titled "Crack stop and Oxygen Barrier for Low-K Dielectric Integrated Circuits," issued to Henry A. Nye, III,

et al. on July 17, 2001 ("Nye") anticipates the asserted claims. (RIB at 211-223.) Respondents contend that Nye is prior art under 35 U.S.C. § 102(e) due to its February 10, 2000 filing date. (*Id.* at 211.)

Regarding claim 1, Respondents assert that Nye discloses a semiconductor chip, substrate and a crack stop structure. (RIB at 212.) Respondents point to the language of claim 1 of Nye to support this, and also to various portions of the specification. (*Id.* at 212-213 (citing RX-679 at 4:17-23, 3:4-6, 2:2-4, 2:27-34; RX-772C at Q. 98-101).)

Respondents next attempt to identify all of the required elements of the crack stop structure found in claim 1 of the '918 patent. Respondents claim that Nye discloses a first conductive line disposed over the substrate. (RIB at 213 (citing RX-679 at 2:26-29, 4:44-45, Fig. 1; RX-772C at Q. 102).)

Respondents argue that Nye discloses at least two first contacts connected to the substrate and the first connective line, the at least two first contacts being spaced apart from each other and extending longitudinally along a length of the conductive line. Respondents assert that the dispute between the parties regarding this claim element is whether or not the contacts connects to the substrate. (RIB at 213.) Respondents identify the three spaced-apart first contacts 112 in Figure 1 of Nye to meet this claim limitation. (*Id.* (citing RX-772C at Q. 102).) They claim that the dashed line in Figure 1 of Nye that extends from contacts 112 to substrate 1 indicates that the repeating structure of contacts 112 and 132 and metal lines 122 and 142 extends to substrate 1. (*Id.* at 214 (citing RX-772C at Q 104).) According to Respondents, dashed lines like this are commonly used to represent repeated structures, which makes the drawing simpler and easier to understand. (*Id.* (citing RX-772C at Q 104).) Respondents state that Figure 1 shows a second optional crack stop structure, labeled number 3, that is also represented by a pair of dashed lines

running the entire vertical length of the device between the substrate and the top of the device (*Id.* (citing RX-772C at Q. 105; RX-679 at 2:43-47).)

Respondents assert that the specification makes two things very clear. First, the dotted lines representing optional crack-stop structure 3 indicate that crack-stop structure 2 — including substructures 112, 122, 132, and 142 — can be repeated in the area 3 demarked by these dotted lines. (RIB at 214 (citing RX-772C at Q. 105).) If the structure were only meant to extend half way into the device, there would be no need for the dotted box labeled 3 to extend all the way down to the substrate. (*Id.* (citing RX-772C at Q. 105).) Second, the specification states that the structure 3 is an optional secondary crack-stop structure providing redundant protection against oxygen diffusion in the event that structure 2 is compromised. (*Id.* at 215 (citing RX-772C at Q. 105; RX-679 at 2:43-47).) There would be nothing to prevent such oxygen diffusion from moving from the edge toward the active region of the device sought to be protected if the crack-stop structure ran only half way down the device. (*Id.* at 215 (citing RX-772C at Q. 105; RX-679 at 2:43-47).) Respondents claim that it necessarily follows that the dotted lines represent the same structure that appears in 2 with both structures (2 and 3) extending the length of the device from the substrate to the top of the device area 31, 20 so that each may perform the dual function of a crack stop and an oxygen diffusion barrier as taught by the patent. (*Id.* (citing RX-772C at Q. 105; RX-679 at 2:43-47).)

Respondents argue that a crack stop that did not extend all the way to the substrate would allow cracks to propagate through the insulating material below the crack stop. Respondents assert that this was clearly not intended by the patent and is inconsistent with its teachings. (RIB at 215 (citing RX-772C at Q. 110; Tr. at 647:14-22).)

Respondents state that Dr. Glew testified that the crack stop structure 2 in Nye does not extend to the substrate because Nye is concerned with protecting low-k dielectric ICs, which, according to Dr. Glew, "are usually formed at the top layers of the dielectric." (RIB at 216 (citing CX-1048C at Q. 18).) Respondents aver that Dr. Glew's testimony is contradicted by the plain language in Nye. (*Id.* (citing RX-679 at 3:16-19, 3:19-22; RX-772C at Q. 100, 106-107).) Respondents claim that Nye explains that the crack stop structure extends to the substrate because the same mask is used to form simultaneously the apertures for the crack stop and the first metal interconnects, which necessarily are connected to the substrate because they contact that source and drain regions of the active devices in the substrate. (*Id.* (citing RX-772C at Q. 106-107).) Respondents further claim that Dr. Glew's assertion that Nye's crack stop would not extend to the substrate because it is only associated with low-k dielectrics is belied by the statement in Nye that the invention applies to many materials beyond just low-k materials. (*Id.* at 216-217 (citing RX-679 at 4:1-5).)

Respondents argue that Dr. Glew's testimony that the crack stop in Nye does not touch the substrate because a dual-damascene process could be used is conclusory and contradictory. (RIB at 217.) Pointing to the specification of Nye, Respondents claim that whether dual-damascene is used is not relevant to whether the contacts touch the substrate. (*Id.* (citing RX-679 at 3:18-20; RX-772C at Q. 100, 106-107).)

Respondents argue that Dr. Glew's assertion that "[c]opper would not be connected to the substrate" is contradicted by the teachings of Nye and the '918 patent itself. According to Respondents, Nye expressly states that the crack stop structure can be formed using a dual-damascene copper process using the same mask used to form the interconnects to the transistor sources and drains in the substrate. (RIB at 217 (citing RX-679 at 3:18-21, 3:55-59).)

Respondents state that the '918 patent expressly states that copper can be used for the lowest-level contacts between the substrate and the first conductive line. (*Id.* at 217-218 (citing JX-5 at 3:53-55).) In addition, Respondents state that Nye expressly explains that a dual-damascene process is not necessary for forming the crack stop. (*Id.* at 218 (citing RX-679 at 4:5-10).) Respondents aver that one of ordinary skill in the art would recognize that Nye expressly teaches a crack stop structure built upward from the surface of the substrate, thereby explicitly connected to the substrate because the mask used for the contacts to the sources and drains is used to make simultaneously the apertures for the crack stop structures. (*Id.* at 218-219 (citing RX-772C at Q. 106).)

Respondents argue that Nye teaches the required second conductive line disposed over a portion of the first conductive line. (RIB at 219 (citing RX-679 at 2:26-2, 4:44-45).) Respondents claim that the second conductive line is labeled 142 in Figure 1. (*Id.*) Respondents claim that Nye discloses the claimed at least two second contacts. (*Id.* at 219-220 (citing RX-772C at Q. 112; RX-679 at 2:26-29).)

Respondents assert that Nye discloses the final element of claim 1, requiring the first and second contacts to be of a substantially greater longitudinal dimension than lateral dimension. Respondents explain that the crack stop in Nye is used to prevent oxygen diffusion into the active areas of the chip. (RIB at 220 (citing RX-679 at 2:43-47; RX-772C at Q. 110; Tr. at 647:14-22).) Respondents note that Nye describes the crack stop as a continuous crack stop. (*Id.* (citing RX-678 at 3:11-14).) Respondents argue that the crack stop must be a continuous wall to provide effective protection against oxygen diffusion. (*Id.* (citing RX-772C at Q. 140, 154).)

Regarding dependent claim 2, Respondents contend that Nye discloses three first contacts. (RIB at 221 (citing RX-679 at Fig. 1; RX-772C at Q. 115).) Regarding dependent

claim 4, Respondents argue that Nye discloses that the crack stop is surrounded by dielectric material. (*Id.* (citing RX-679 at 2:2-4; RX-772C at Q. 117).)

Regarding dependent claim 7, Respondents claim that while only two sets of contacts and conductive lines are illustratively represented, it is clear from the teachings of Nye that in order to form a crack stop structure at the substrate at the same time as the initial circuit elements are formed, there are more than two such structures within the device. (RIB at 221-222 (citing RX-772C at Q. 120).) Therefore, Respondents argue that Nye discloses the third conductive line and at least two third contacts described in claim 7. (*Id.* at 222.)

Regarding dependent claim 11, Respondents assert that the crack stop in Nye is used to prevent oxygen diffusion into the active areas of the chip. (RIB at 222 (citing RX-679 at 2:43-47; RX-772C at Q. 110; Tr. at 647:14-22).) Respondents note that Nye describes the crack stop as a continuous crack stop. (*Id.* (citing RX-678 at 3:11-14).) Respondents argue that the crack stop must be a continuous wall to provide effective protection against oxygen diffusion. (*Id.* (citing RX-772C at Q. 140, 154).) Respondents therefore claim that Nye discloses the additional limitation found in claim 11. (*Id.* at 223 (citing RX-772C at Q. 122).)

In their reply brief, Respondents respond to Qimonda's allegation that Nye does not disclose a solid, elongated crack stop structure. Respondents note that Nye describes the crack stop as "continuous," a term that Qimonda's expert stated is generally used and understood as a longitudinal reference. (RRB at 89-90 (citing RX-679 at 4:17-20; Tr. at 654:22-655:6).) Respondents quote a portion of the specification from Nye, stating that it unquestionably indicates that the crack stop forms a continuous circle around the chip like a wall. (*Id.* at 90-91 (citing JX-679 at 3:15-26).)

Respondents further respond to Qimonda's argument that the crack stop in Nye does not extend to the substrate because of the dotted line shown in Nye. (RRB at 91-92.) Respondents claim that Qimonda's argument about the crack stop not working due to a short circuit is unsupported by the record and should be rejected. (*Id.* at 92-93 (citing Tr. at 1331:4-6; RX-772C at Q. 104).)

Respondents claim that Qimonda's argument that the crack stop cannot touch the substrate because it is embedded within a dielectric material is incorrect. (RRB at 93-94.) Respondents claim that the terms "embed" and "surround" are synonyms in this situation, and there is no support for the proposition that there is a dielectric material separating the crack stop from the substrate in Nye. (*Id.* at 94 (citing WEBSTER'S NINTH NEW COLLEGIATE DICTIONARY, at 405).)

Respondents next address Qimonda's contention that the Nye crack stop structure does not extend to the substrate because it must be embedded in the low-k dielectric material of the device. (RRB at 94-95.) Respondents claim that Nye rebuts this argument, because it states that "those skilled in the art will appreciate that the invention applies to many dielectric materials and to many corrosive materials, not just low-k materials and oxygen and that not all the interlayer dielectric materials need to be the same." (*Id.* (citing RX-679 at 4:1-5).)

Respondents state that Qimonda similarly argues that the presence of silicon dioxide near the substrate would eliminate the need for a crack stop at that level because silicon dioxide is, itself, and effective crack stop. (RRB at 95 (citing CIB at 161-162).) Respondents claim that this argument is flawed because the'918 patent describes one embodiment as having a crack stop structure connected to the substrate and surrounded by silicon dioxide. (*Id.* (citing JX-5 at 3:47-58).) Respondents state that the invention of Nye sought to prevent cracks from occurring

regardless of the dielectric material. (*Id.*) Respondents reiterate their argument that Nye teaches a crack stop that extends to the substrate. (*Id.* at 95-96 (citing RX-679 at 3:4-6, 3:18-22, 4:22-27).)

Qimonda's Position: Qimonda argues that Nye fails to anticipate the asserted claims. (CIB at 155.)

Qimonda states that the '918 patent does not cover posts, as the claims were amended during prosecution to avoid the prior art, which consisted of posts. (CIB at 155 (citing JX-6 at QAG-665-ITC-0190124; RX-772C at Q. 88-89; Tr. at 1310:7-1312:2).)

According to Qimonda, Respondents do not (and cannot) point to any figure or passage in the specification which teaches that the crack stop in Nye contains contacts which are longer than they are wide. (CIB at 156.) Qimonda claims that Dr. Bravman's sole evidence that the elongated contact limitation of the '918 Patent is purportedly taught by Nye is a citation to the preamble of claim 1 of Nye. (*Id.* (citing CX-1048C at Q. 27; RX-772C at Q. 113; Tr. at 1317:10-19).) Qimonda argues that Dr. Bravman never explains how this language meets the claim limitation "wherein the first and second contacts are of substantially greater longitudinal dimension than lateral dimension." (*Id.* (citing CX-1048C at Q. 27; RX-772C at Q. 113; Tr. at 1317:10-19).) According to Qimonda, "[a] single citation to the preamble of Claim 1 of Nye, without any explanation, falls far short of the clear and convincing standard required to invalidate the '918 Patent." (*Id.*)

Qimonda claims that the use of the word "continuous" in Nye merely means the crack stop completely surrounds, or encircles, the circuit elements. (CIB at 156-157 (citing Tr. at 1520:12-23).) Qimonda notes Dr. Glew's testimony where he stated that continuous crack stops in the prior art contained posts, not elongated contacts. (*Id.* at 157 (citing Tr. at 1520:12-23).)

Qimonda argues that Nye teaches away from the use of elongated contacts. (*Id.*) Qimonda states that during Dr. Bravman's testimony, he acknowledged that Nye expressly teaches that the vertical members of the crack stop have the transverse dimension of vias. (CIB at 157 (citing RX-679 at 3:35-40; Tr. at 1315:21-1316:5).) Qimonda claims that this suggests the contacts are in fact typical cylindrical contacts, and not the elongated contacts expressly required by each asserted '918 patent claim. (*Id.* (citing RX-679 at 3:35-40; Tr. at 1315:21-1316:5).) Qimonda states that because the perpendicular dimension of the interconnect elements shown in Figure 1 are the same dimension of vias, Nye teaches that the interconnect members of the crack stop are not elongated. (*Id.*) Qimonda argues that in every instance, Nye refers to the vertical members of the crack stop structure as corresponding to a via, which is typically a column. (*Id.* (citing CX-1048C at Q. 14, 21, 27; RX-679 at Abstract, 1:30-36, 4:25-27).)

Qimonda next argues that Nye does not disclose first contacts that are connected to the substrate. (CIB at 158 (citing CX-1048C at Q. 20; RX-772C at Q. 103; Tr. at 1315:12-15).) Qimonda argues that since Nye does not explicitly disclose two contacts connected to the substrate, and because inherency has been disclaimed by Respondents, Respondents cannot meet the clear and convincing burden required to prove that Nye discloses this element. (*Id.* (citing CX-1048C at Q. 20; RX-772C at Q. 103; Tr. at 1315:3-15).)

Qimonda claims that Respondents do not (and cannot) point to any passage in the specification of Nye that teaches the dotted line from Figure 1 indicates a repeated structure. (CIB at 159 (citing CX-1048C at Q. 22; RX-772C; RX-679).) Qimonda assert that if the dotted line indicated a repeated structure as Respondents allege, the entire circuit would not function because the guard ring would cause all devices to be shorted out. (*Id.* (citing RX-679 at 3:48-54; RX-772 at Q. 104; Tr. at 1331:4-6).)

Qimonda argues that in drafting, a wavy line, and not a dotted line, indicates a repeated structure. (CIB at 160 (citing CX-1048 at Q. 22; RX-679 at Fig. 1).) Qimonda asserts that the dotted line is nothing more than a center line used to indicate that the crack stop structure 2 may optionally be provided in the dotted box 3. (*Id.* (citing CX-1048 at Q. 22; RX-679 at 2:42-46, Fig. 1).)

Qimonda asserts that the fact that Nye teaches that the "[c]rackstop 2 is embedded within a set of dielectric layers" means that there is a dielectric layer between the crack stop and the substrate. (CIB at 160 (citing CX-1048C at Q. 19; RX-679 at 2:2-6; Tr. at 1316:6-24).) Qimonda states that under any proposed construction, a crack stop cannot be connected to the substrate if there is a dielectric layer between the two structures. (*Id.*)

Qimonda argues that the fact that the crack stop in Nye is used with low-k or porous dielectric materials is further evidence that the contacts are not connected to the substrate. (CIB at 161 (citing CX-1048C at Q. 18; RX-679 at 3:11-14).) Qimonda notes that Dr. Glew testified that low-k dielectrics are not used on the substrate because there are no capacitance problems and using low-k near the substrate may damage the silicon. (*Id.* (citing CX-1048C at Q. 18; RX-679 at 3:11-14; Tr. at 523:16-1524:13).) According to Qimonda, since Nye teaches that the crack stop is within the low-k dielectric regions, and low-k dielectric is not used on the substrate, Nye does not teach a crack stop which extends to the substrate. (*Id.* (citing CX-1048C at Q. 18; RX-679 at 3:11-14; Tr. at 523:16-1524:13).)

Qimonda argues that the fact that a stated purpose of Nye is to protect against oxygen diffusion does not require that the crack stop touch the substrate. (CIB at 161.) Qimonda notes that the lower layers of the dielectric material in Nye would be silicon dioxide and not low-k dielectric materials. (*Id.* (citing CX-1048C at Q. 35; Tr. at 1522:17-1524:13).) Qimonda states

that Nye is only concerned with preventing oxygen diffusion in the upper, porous regions of the chip. (*Id.* at 162 (citing CX-1048C at Q. 14, 21; RX-679 at 1:6-8).) Qimonda claims that the old-style silicon dioxide is glass, and is a very good oxygen seal. (*Id.* at 161 (citing CX-1048C at Q. 35; Tr. at 1522:17-1524:13).) Thus, Qimonda states that there would be protection against oxygen diffusion in the lower layers where the crack stop does not extend to because those lower layers would be silicon dioxide and not a low-k dielectric. (*Id.* (citing CX-1048C at Q. 35; Tr. at 1522:17-1524:13).) Qimonda therefore claims that Nye does not teach a crack stop which extends to the substrate because there is no reason to provide an oxygen diffusion barrier in the lower layers of the dielectric material. (*Id.* at 162.)

Qimonda alleges that Nye contains several other citations which teach away from the crack stop being connected to the substrate. From the abstract and specification, Nye states "horizontal interconnect elements [of the circuit] have a corresponding structure in the crackstop and vias between interconnect layers have corresponding structures in the crackstop." (CIB at 163 (citing CX-1048C at Q. 14; RX-679 at Abstract, 1:30-36).) Qimonda states that from this citation, Nye is making it clear that the crack stop contains horizontal interconnect elements and vertical members which are vias between interconnect layers. (*Id.* (citing CX-1048C at Q. 14; RX-679 at Abstract, 1:30-36).) Qimonda claims that there is simply no passage in Nye which refers to the vertical elements of the crack stop being connected to the substrate and the first metal line. (*Id.* at 163-164 (citing CX-1048C at Q. 14; RX-679 at Abstract, 1:30-36).)

Additionally, Qimonda points to the claims found in Nye and state that they contain similar language which limits the vertical members of the crack stop to corresponding vias between metallization layers. (CIB at 164.) The claims provide "forming a first set of interconnect vias and a first set of solid crackstop vertical members in a first layer of porous

dielectric." (*Id.* (citing CX-1048C at Q. 21; RX-679 at 4:25-27).) Qimonda asserts that this passage supports its argument that the crack stop is not connected to the substrate. (*Id.* (citing CX-1048C at Q. 21; RX-679 at 4:25-27).)

Qimonda argues that Dr. Bravman's assertion that there would be no point in building the structure if it did not connect to the substrate, or that he has never seen a crack stop not connected to the substrate, contradicts the testimony of Respondents' other expert, Dr. Shanfield. (CIB at 164-165.) According to Qimonda, Dr. Shanfield testified that the Qimonda product does not practice the '918 patent because the crack stop is not connected to the substrate. (*Id.* at 165 (citing Tr. at 1738:15-29).) Qimonda argues that Respondents cannot have it both ways.

In its reply brief, Qimonda claims that Respondents have failed to address a number of factual issues regarding Nye, and thus have waived their right to do so. (CRB at 82-84.) Qimonda argues that Respondents make an inherency argument regarding whether the vertical crack stop members in Nye are continuous walls. (*Id.* at 85.) Qimonda argues that this inherency argument should be disregarded because Respondents disclaimed the inherency doctrine. (*Id.* (citing Tr. at 1315:3-8).)

Qimonda claims that Respondents have failed to present clear and convincing evidence that Nye discloses contacts that are longer than the are wide. (CRB at 84.) Qimonda states that Respondents cited to three places in Nye for support, but none of those three cites provides the necessary support. (*Id.* (citing RIB at 220; RX-772C at Q. 110, 113, 140, 154).) Qimonda reiterates its argument that the continuous crack stop of Nye simply means that the crack stop structure completely surrounds the circuit elements. (*Id.* at 85 (citing Tr. at 1520:12-23).) Qimonda claims that Nye is similar to the admitted prior art in the '918 patent in that it utilizes

columns as contacts. (*Id.* (citing Tr. at 1520:12-23; CX-1048C at Q. 14, 21, 27; RX-679 at Abstract, 1:30-36, 3:35-40, 4:25-27; Tr. at 1315:21-1316:5).)

Qimonda reiterates its argument that the dotted line in Figure 1 of Nye does not indicate that the crack stop extends to the substrate. (CRB at 86 (citing CX-1048 at Q. 22; RX-679 at 2:42-46, Fig. 1).) Further, Qimonda argues that if the dotted line meant that the structure extends to the substrate, the guard ring in Figure 1 would contact and short out the active devices. (*Id.* (citing RX-679 at 3:48-54; RX-772C at Q. 104; Tr. at 1331:4-6).) Qimonda argues that the crack stop does not need to extend down to the substrate to prevent oxygen diffusion because the silicon dioxide layers in Nye will prevent oxygen diffusion in the lower layers. (*Id.* at 86-87 (citing CX-1048C at Q. 35; Tr. at 1522:17-1524:13).)

Qimonda argues that Respondents misleadingly suggest that the lower interconnect structure makes contact with the transistors and that this somehow suggests that the crack stop is connected to the substrate. (CRB at 88.) Qimonda claims that Nye specifically describes that the electrical contact between the metal interconnect and the transistor is facilitated through a different metallization layer, which is not an interconnect (which, by definition and as known throughout the art, interconnects two metal layers). (*Id.* (citing Tr. at 657:10-659:24).) Qimonda states that Respondents' argument that the same mask is used for the metal interconnect and the crack stop actually teaches (as does the entire reference) that the crack stop is between metallization layers, at the interconnect level, and not connected to the substrate. (*Id.* (citing CX-1048C at Q. 8-29; RX-772C at Q. 103, 113; RX-679; CDX-41; Tr. at 1315:12-15, 1316:6-24, 1331:4-6; Tr. at 1515:1-7, 1520:12-23, 1522:17-1524:13, 1523:16-1524:13).)

Qimonda asserts that Respondents fail to address the fact that Dr. Bravman admitted that Nye does not show two contacts connected to the substrate. (CRB at 88-89 (citing CX-1048C at

Q. 20; RX-772C at Q. 103; Tr. at 1315:12-15).) According to Qimonda, Respondents thus admit Nye does not render the '918 Patent inval*id.* (*Id.*)

Commission Investigative Staff's Position: Staff contends that Nye anticipates the asserted claims. (SIB at 64.)

Pointing to Figure 1, Staff states that Nye discloses a crack stop that extends to the substrate. Staff relies on Dr. Bravman's testimony that if the crack stop did not extend to the substrate, it would not work for its intended purpose. (SIB at 65 (citing RX-772C at Q. 110).) Staff states that Nye specifically teaches that the crack stop extends to the substrate when describing the optional crack stop 3 in Figure 1. (*Id.* at 66 (citing RX-679 at 2:43-45).) Staff points to the fact that the crack stop in Nye is characterized as continuous to support its argument that Nye discloses the limitation requiring the contacts to be of substantially greater longitudinal dimension that lateral dimension. (*Id.* (citing RX-679 at claim 1).) Staff contends that Nye discloses all of the limitations found in dependent claims (*Id.* at 66-67.)

In its reply brief, Staff criticizes Qimonda's attempt to argue that the contacts in Nye are not continuous walls, but instead are posts. (SRB at 11.) Staff again notes that the crack stop in Nye is referred to as "continuous" and states that there is nothing in the intrinsic record to support the argument that the contacts are not continuous walls. (*Id.* at 11-12 (citing RX-679 at 4:16-21).)

Staff reiterates its argument that Figure 1 of Nye demonstrates that the crack stop extends to the substrate. (SRB at 13-14.) Staff states that Qimonda never explains the purpose of the dotted lines seen in Figure 1, and there is no other possible explanation for why those lines appear in Figure 1. (*Id.*) Staff claims that Nye's explanation of Figure 1 is clearer and more

credible than any of the conflicting expert testimony. (*Id.* (citing CIB at 159; RX-772C at Q. 104).)

Discussion and Conclusion: Based upon the evidence before me, I find that Respondents have demonstrated by clear and convincing evidence that Nye anticipates asserted claims 1, 2, 4, 7, and 11 of the '918 patent.[67]

Nye was filed on February 10, 2000, meaning that it qualifies as prior art under 35 U.S.C. § 102(e). This is not disputed by Qimonda. Nye is not cited on the face of the '918 patent. (JX-5.)

The parties dispute whether or not two limitations from claim 1 are disclosed in Nye: (1) "at least two first contacts connected to the substrate," and (2) "wherein said first and second contacts are of substantially greater longitudinal dimension than lateral dimension." I find that Nye clearly and convincingly discloses both limitations.

Regarding the limitation stating that the first two contacts must be connected to the substrate, both parties focus on Figure 1 of Nye, reproduced below:

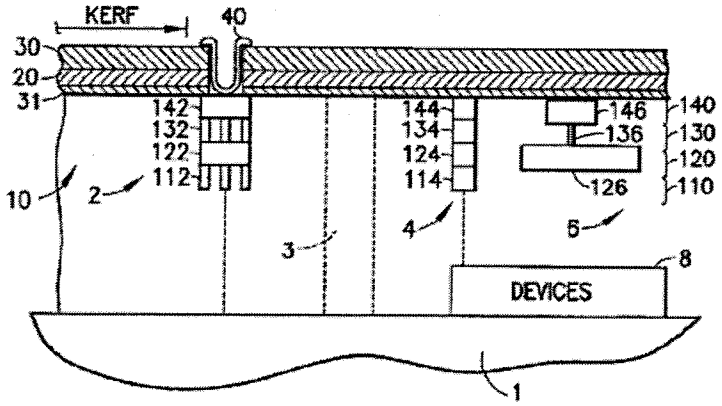


FIG. 1

[67] Based on the testimony of the parties' experts, I find that a person of ordinary skill in the art for the '918 patent would have a bachelor's degree in electrical engineering, mechanical engineering, physics, materials science, or a related field, and at least two years of work experience in the semiconductor processing field. (CX-1048C at Q. 6; RX-772C at Q. 37.)

(RX-679 at Fig. 1.)

In describing this figure, Nye identifies the crack stop as element 2. The parties and their experts vigorously dispute whether the dotted line extending from element 2 to the substrate (identified as element 1) indicates that the crack stop extends to the substrate.

I find that the crack stop disclosed in Nye extends to the substrate. Nye describes the crack stop as follows:

> Near the center of the Figure, a composite structure, denoted generally by the numeral 2 and comprising layers 112, 122, 132 and 142 serves both as the crackstop structure and also as the primary oxygen diffusion barrier.

(*Id.* at 2:26-29.) Nye then describes element 3 from Figure 1 as follows:

> Between structures 2 and 4 there is a dotted box labelled 3 that schematically represents an optional secondary structure the same as crackstop structure 2.

(*Id.* at 2:42-44.) The fact that element 3 depicts a secondary crack stop structure that is "***the same*** as crackstop structure 2" means that crack stop structure 2 also extends to the substrate as is shown by the outline of element 3. (*Id.*; RX-772C at Q. 105.)

Qimonda argues that Nye is only concerned with oxygen diffusion in the upper porous portions of the low-k dielectric, and that silicon dioxide in the lower portion provides an adequate seal. (*See* CX-1048 at Q. 35; Tr. at 1522:17-1524:13.) I find that this argument is unsupported by the evidence and contradicted by Nye.

Nye provides no description of using silicon dioxide as a diffusion barrier for oxygen. Instead, Nye describes the use of a crack stop as the "primary oxygen diffusion barrier." (RX-679 at 2: 2:26-29.) It further describes a guard ring as the "secondary oxygen barrier." (*Id.* at 2:30-32.) This provides strong evidence that the crack stop is the primary structure used to prevent oxygen diffusion, and there is no mention of not needing the crack stop in the lower portion of the dielectric. Further, Nye is not limited to use in low-k dielectrics, as it states that

"[t]hose skilled in the art will appreciate that the invention applies to many dielectric materials and to many corrosive materials, not just low-k materials and oxygen and that not all the interlayer dielectric materials need to be the same." (*Id.* at 4:1-4.) Thus, Qimonda's explanation regarding low-k dielectrics and silicon dioxide is too restrictive in light of Nye's disclosure.[68]

Regarding the claim limitation requiring that the contacts are of substantially greater longitudinal dimension than lateral dimension, I find that Nye clearly discloses such a limitation. Nye discloses the use of a continuous crack stop to prevent the propagation of cracks and act as an oxygen diffusion barrier. (*See generally* RX-679.) All of the claims in Nye require a "continuous composite crack stop structure." (*Id.* at 4:17, 5:2.) The specification explains that "[a] continuous crackstop member within the low-k or porous diesectric is required in order to avoid leaving a path for oxygen diffusion." (*Id.* at 3:11-14.) Claim 8 states that the crack stop structure is "formed from solid materials without cavities extending around said circuit elements[.]" (*Id.* at 5:5-6.) This language from the claims and specification of Nye clearly demonstrates that the crack stop requires that the contacts are longer than they are wide. (RX-772C at Q. 113.)

Qimonda argues that the fact that Nye discloses a "continuous" crack stop does not mean that the contacts extend the length of the crack stop. Qimonda claims that "continuous" merely means that the crack stop surrounds the active circuitry, and does not imply anything about the shape of the contacts. (*See* CRB at 85.)

Qimonda's argument is directly contradictory to the argument it made in asserting infringement. As support for the proposition that { } meet this claim limitation, Qimonda cited to the following language from a design rules document:

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[68] In addition, it is clear from the claims in Nye that the conductive lines are formed on top of the contacts, meaning that the contacts (and not the conductive line) will be connected to the substrate. This is described in steps (a) and (b) of the independents claims. (*See* RX-679 at claims 1 & 8.)

{ }

(CX-125C at LSI-337-665-0147060) (emphasis in original.)

In discussing this passage, Dr. Glew stated:

} (CX-110C at Q. 106.) It is logically inconsistent for Qimonda to now argue that the crack stop in Nye does not meet the limitation at issue when Nye describes the crack stop as "[a] continuous crackstop member" that is required "in order to avoid leaving a path for oxygen diffusion." (RX-679 at 3:11-14.)

Qimonda also claims that the fact that Nye refers to the contacts as "vias" means that they are columns. (*See* CRB at 85; CX-1048C at Q. 27.) This assertion is wholly unsupported, as Qimonda and Dr. Glew point to no evidence demonstrating that a "via" is necessarily a column and cannot instead refer to a continuous wall structure.

Qimonda further argues that Respondents' and Staff's position regarding the shape of the contacts relies on the doctrine of inherency, but Respondents allegedly "disclaimed" the inherency doctrine. (*See* CRB at 80-82.) The doctrine of inherency holds that a prior art reference may disclose a claim limitation even if the limitation is not explicitly disclosed in the reference, as long as one of ordinary skill in the art would necessarily know from reading the reference that the limitation was present. *Agilent Techs., Inc. v. Affymetrix, Inc.*, 567 F.3d 1366, 1383 (Fed. Cir. 2009) ("The very essence of inherency is that one of ordinary skill in the art would recognize that a reference unavoidably teaches the property in question."); *MEHL/Biophile Int'l Corp. v. Milgraum*, 192 F.3d 1362, 1365 (Fed. Cir. 1999) ("Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes, the claimed limitations, it anticipates.")

As its basis for the argument that Respondents disclaimed any use of the inherency doctrine, Qimonda cites to Dr. Bravman's testimony at the hearing that he did not "depend on the legal principle of inherency" in rendering his opinion. (Tr. at 1315:3-8.) Dr. Bravman is not an attorney, and I find that this statement regarding a legal conclusion does not constitute any disclaimer of the inherency doctrine.

Notwithstanding the foregoing, I have already found that the "substantially greater longitudinal dimension than lateral dimension" claim limitation is expressly disclosed in the specification and claims of Nye that are cited *supra*. Therefore it is unnecessary to rely on the inherency doctrine to demonstrate that Nye anticipates claim 1.[69]

Besides the two limitations discussed *supra*, Nye meets the other limitations of claim 1. Nye discloses a semiconductor chip including a substrate and a crack stop structure. (RX-679 at 1:5-50, 2:50-52; RX-772C at Q. 98-101.) Nye includes the claimed first and second conductive lines. (RX-679 at Fig. 1; RX-772C at Q. 102, 111.) Nye includes the claimed at least two second contacts. (RX-679 at Fig. 1; RX-772C at Q. 112.) Thus, I find that Respondents have offered clear and convincing evidence that claim 1 is anticipated by Nye.

Regarding the dependent claims, Qimonda offers no separate argument addressing the limitations found in these claims. Claim 2 adds the requirement that there are three contacts connected between the substrate and the first conductive line. Nye discloses this claim limitation. (RX-679 at Fig. 1; RX-772C at Q. 115.) Thus, I find that Nye anticipates claim 2.

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[69] Qimonda makes this disclaimer argument again when discussing the other prior art references asserted by Respondents. For the sake of brevity, I will not repeat my analysis. My conclusion that the inherency doctrine has not been waived is applicable with respect to all prior art references that Respondents assert anticipate the '918 patent.

Claim 4 adds the requirement that there is dielectric material surrounding the crack stop structure. Nye discloses this claim limitation. (RX-679 at 2:2-4, Fig. 1; RX-772C at Q. 117.) Thus, I find that Nye anticipates claim 4.

Claim 7 adds the requirements of a third conductive line and at least two third contacts connected to both the second and third conductive lines, wherein the contacts extend longitudinally along a length of the third conductive line. Nye discloses this claim limitation. (RX-679 at Fig. 1; RX-772C at Q. 120.) Thus, I find that Nye anticipates claim 7.

Claim 11 adds the requirement that the first and second contacts extend over the entire length of the first conductive line. Nye discloses this claim limitation. (RX-679 at 3:11-14, 4:17, 5:2-6, Fig. 1; RX-772C at Q. 122.) Thus, I find that Nye anticipates claim 11.

2. Shinogi

Respondents' Position: Respondents contend that U.S. Patent No. 6,424,051 to Shinogi, et al. ("Shinogi") anticipates the asserted claims of the '918 patent. (RIB at 223.)

Respondents claim that Shinogi discloses a semiconductor chip that includes a substrate. (RIB at 225 (citing RX-684 at 1:27-32, 4:27-34; RX-772C at Q. 226-227).) Respondents assert that Shinogi discloses the crack stop structure in claim 1. (*Id.* at 226-227 (citing RX-684 at 4:31-40).) Although it is referred to as a seal ring in Shinogi, Respondents state that Qimonda's expert acknowledged that a seal ring is a crack stop if it has the capability of stopping cracks from propagating. (*Id.* at 226 (citing Tr. at 1497:1-16).) Respondents claim that the seal ring in Shinogi acts as both a moisture seal and a crack stop. (*Id.* (citing RX-772C at Q. 228).) Respondents claim that Figure 1 of Shinogi discloses a first conductive line disposed over the substrate, as required by claim 1. (*Id.* at 227 (citing RX-772C at Q. 229; RX-684 at 5:5-7).)

Respondents state that Figure 1 of Shinogi shows at least two first contacts connected to the substrate and a first conductive line. (*Id.* (citing See RX-684, at 4:34-36, 5:54-56, 7:40-49, 8:9-17; RX-772C at Q. 230).)

Respondents aver that Figure 1 of Shinogi shows a second conductive line, labeled number 12, disposed over a portion of the first conductive line. (RIB at 228 (citing RX-772C at Q. 231; RX-684 at 5:5-7).) Respondents claim that Shinogi discloses a second pair of contacts 10M created in a manner similar to the first pair of contacts 9M. (*Id.*) According to Respondents, Figure 1 of Shinogi shows a second pair of contacts, labeled 10M, in the second story of the seal-ring structure. (*Id.* (citing RX-772C at Q. 232; RX-684, at 4:34-36, 5:54-56).)

Respondents argue that because the contacts in Shinogi are formed as rings surrounding the active circuitry, and because they are functioning as seal rings, creating a continuous wall to prevent moisture as well as cracks from reaching the active circuitry of the device, it is clear that Shinogi discloses contacts extending as walls around the perimeter of the chip. (RIB at 229.) Accordingly, Respondents state that Shinogi discloses the limitation of claim 1 requiring that the first and second contacts be of substantially greater longitudinal dimension than lateral dimension and also the limitation of claim 11 requiring that the at least two first contacts and at least two second contacts extend over the entire length of the first conductive line. (*Id.* at 229-230 (citing RX-772C at Q. 233).)

Respondents claim that the only argument that Dr. Glew presents in opposition to Dr. Bravman's opinions about Shinogi is his opinion that the contacts "are metal posts, they are not substantially greater in longitudinal dimension than lateral dimension." (RIB at 230 (citing CX-1048C at Q. 54).) Respondents argue that while Shinogi, at times, refers to structures 9M and 10M as "posts," the disclosure makes clear that their geometric configuration is not of a square

or round fence post, but rather, the structures are continuous rings of metal that surround the integrated circuit. (*Id.*)

Respondents claim that Shinogi repeatedly explains that, in reference to Figure 1, three "first seal grooves 9" are made "surrounding the IC circuit formation part 2" and two "second seal grooves 10" are also made. (RIB at 230 (citing RX-684 at 4:66-5:4).) In the next paragraph, Shinogi explains that because tungsten (chemical symbol "W") is used for interconnection, tungsten "is embedded in each seal groove 9, 10, forming a metal post 9M, 10M." (*Id.* (citing RX-684 at 5:9-12).) Respondents claim that the language used by Shinogi contradicts Dr. Glew's assertion that 9M and 10M are not substantially greater in longitudinal dimension than lateral dimension. (*Id.*)

Respondents state that the word "post" is not a term of art in the semiconductor industry. (RIB at 230 (citing Tr. at 1309:17-23, 1327:21-23).) Respondents thus claim that the configuration of the structure must be understood in light of the description. (*Id.* at 230-231.) Respondents also note that the patent is a translation of an original Japanese patent application, thus raising the possibility of translation-related language issues. (*Id.* at 231 (citing RX-684).)

Respondents assert that Shinogi also refers to the posts as "tungsten plugs," and provides a description that indicates the plugs are continuous. (RIB at 231 (citing RX-684 at 7:22-23, 7:54-57, 8:4-6, 8:47-49, 8:56-58).) Respondents claim that on cross-examination, Dr. Glew acknowledged that a tungsten plug may be continuous if used in a crack-stop structure. (*Id.* (citing Tr. at 1517:7-13).)

Regarding dependent claim 2, Respondents state that Figure 1 of Shinogi shows three contacts (9M) in the first layer of the seal ring. (RIB at 231-232 (citing RX-684 at 4:66-5-13, 8:4-6; RX-730 at 2; RDX-57.7).) Regarding dependent claim 4, Respondent state that Figure 1

of Shinogi discloses layers of insulating film (5, 7, and 8) surrounding the seal ring structure. (*Id.* at 232 (citing RX-684 at 7:31-39, 8:25-31, 9:4-6).) Respondents assert that there is no dispute that these insulating layers are dielectric materials, as Dr. Glew testified that "[a]ll integrated circuits contain dielectrics, which are insulators." (*Id.* (citing Tr. at 660:18-21; Deposition Stipulation, Tab 11 at 154:11-20).)

Regarding dependent claim 7, Respondents argue that Shinogi discloses a three level seal ring structure that satisfies the claim limitations. (RIB at 232-233 (citing RX-684 at 7:40-46, 4:33-39; RX-772C at Q. 234; RX-730 at 3; RDX-57.12).) Regarding dependent claim 11, Respondents argue that the fact that the formation in Shinogi is first "sealed" with the seal ring 4 also indicates that the seal ring is continuous in nature with no gaps or breaks - sealing off the active structure from potential contaminants from outside the seal ring in the kerf region of the device. Shinogi is explicit that a single "metal post" 9M or 10M is formed in each seal groove 9, 10, which grooves "are made surrounding the IC circuit formation part 2." (*Id.* (citing 233 (citing RX-684 at 5:11-12, 4:66-5:4).) Respondents claim that Shinogi expressly explains that the "seal ring may be made up of seal grooves formed in the interlayer insulation films of at least two layers and seal material filled in the seal grooves." (*Id.* (citing RX-684 at 2:34-37).) Respondents further state that Shinogi explains that the seal ring is made "of a plurality of rings, so that it is made possible to block moisture perfectly." (*Id.* (citing RX-684 at 2:41-43).)

Respondents claim that Dr. Glew's testimony during infringement is directly opposite to his testimony regarding Shinogi. Specifically, Respondents note that Dr. Glew testified, in connection with the accused LSI products, "if the first and second contacts were not continuous walls, then a possible path for moisture would be between the substrate and the first conductive line, or between the first conductive line and the second conductive line." (RIB at 234 (citing

CX-110C at Q. 104).) Respondents claim that Dr. Glew now testifies that Shinogi's seal ring is not continuous even though a stated purpose of Shinogi is moisture prevention. (*Id.*) Respondents reiterate their argument from claim 1 that the "tungsten plugs" disclosed in Shinogi demonstrate that the seal ring is formed from continuous walls. (*Id.*)

In their reply brief, Respondents address Qimonda's argument that Respondents failed to set out their arguments regarding Shinogi prior to trial. (RRB at 96.) Respondents state that Qimonda has been aware of this reference from almost the beginning of the investigation. (*Id.*) Respondents state that Shinogi was reclassified as an anticipatory reference, instead of an obviousness reference, because Qimonda dropped claims 3, 5, 6, and 8 shortly before the hearing. (*Id.*) Respondents claim that Qimonda has been on notice since the filing of the very first expert report of Respondents' reliance on Shinogi. (*Id.* at 97 (citing RX-730).)

Respondents state that Qimonda's only argument regarding Shinogi is that the "posts" of Shinogi are not elongated contacts, as required by the asserted claims. (RRB at 97.) Respondents claim that Qimonda's entire argument is based on the belief that "posts are posts," and cannot be elongated contacts. (*Id.* at 97-98 (citing CIB at 173).) Respondents argue that Dr. Glew's testimony is unsupported by the record. (*Id.* at 97 (citing CX-1048C at Q. 55; Tr. at 1520:12-23).) According to Respondents, the term "posts" could just as easily have been selected by a translator of the Shinogi patent from the original Japanese, given that elsewhere in the patent the same structures 9M and 10M are referred to by other terms, including "tungsten plug" - which Dr. Glew acknowledges can be a continuous structure. (*Id.* at 98 (citing Tr. at 1517:7-13).)

Respondents contend that, contrary to Qimonda's assertion, Shinogi does not consistently use the term "posts" when describing the crack stop structure. (RRB at 98.) Respondents note

that Shinogi teaches that the contacts and conductive lines in the crack-stop structure can be made as seal grooves surrounding the IC. (*Id.* (citing RX-684 at 2:34-37, 7:40-44, 7:54-57, 5:8-13).) Respondents argue that these disclosures in Shinogi make clear that the structures 9M and 10M are not cylindrical post structures, but continuous rings of metal that surround the integrated circuit. (*Id.* at 98-99.)

Qimonda's Position: Qimonda contends that Shinogi does not anticipate any of the asserted claims of the '918 patent. (CIB at 172.)

Qimonda claims that Dr. Bravman's testimony regarding Shinogi relates to obviousness, and it is incomplete. (CIB at 172 (citing CX-1048C at Q. 55; RX-772C at Q. 222-223).) According to Qimonda, Dr. Bravman's incomplete testimony fails to meet the clear and convincing standard. (*Id.*)

Qimonda argues that Shinogi teaches the use of posts, not elongated contacts. (CIB at 172 (citing CX-1048C at Q. 54; RX-684 at 5:53-55; RX-772C at Q. 225).) Qimonda claims that both experts agree about this. (*Id.* at 172-173 (citing CX-1048C at Q. 54; RX-684 at 5:53-55; RX-772C at Q. 225).)

Qimonda argues that Dr. Bravman's opinions are unsupported and incorrect. (CIB at 173 (citing RX-772C at Q. 233).) According to Qimonda, Shinogi is just like all of the other prior art references, including the prior art cited within the '918 patent itself, because it uses posts for contacts. (*Id.* (citing CX-1048C at Q. 55; Tr. at 1520:12-23).) Qimonda states that because Shinogi consistently refers to posts as one would commonly understand, Dr. Bravman's argument that a post does not have its normal meaning is against the intrinsic evidence and should be disregarded. (*Id.* at 174 (citing CX-1048C at Q. 54-55; RX-684 at 5:9-13, 5:53-55).)

Qimonda notes that Dr. Bravman has wholly failed to address any of the '918 patent's dependant claims in his direct testimony. (CIB at 174-175 (citing CX-1048C at Q. 56; RX-772C at Q. 234-237).) According to Qimonda, because Dr. Bravman provides no opinion with respect to the dependant claims of the '918 patent, Respondents cannot meet their burden in proving that Shinogi anticipates the dependent claims. (*Id.* at 175.)

In its reply brief, Qimonda claims that Respondents raised a new theory of invalidity for the first time in the post-trial briefing. (CRB at 89.) Qimonda asserts that Dr. Bravman's direct testimony only states that Shinogi renders the '918 patent obvious, and there is no anticipation testimony. (*Id.* (citing RX-772C at Q. 222).) Qimonda claims that Respondents' new anticipation argument should be disregarded. (*Id.*)

Qimonda reiterates that both parties' experts agree that Shinogi discloses posts. (CRB at 90.) Qimonda argues that there is no debate the term "post" refers to the common understanding of the word as a cylindrical object. (*Id.* at 90-91 (citing RX-772C at Q. 31; RX-772C at Q. 88, 89; CX-1048C at Q. 13; JX-5; JX-6; Tr. at 1519:7-1520:23).) Qimonda reiterates that Dr. Bravman relies on a single sentence from Shinogi, with no explanation, to support his opinion that the posts in Shinogi are elongated walls. (*Id.* at 91 (citing RX-772C at Q. 233).)

Qimonda notes that Dr. Glew testified that posts can form a ring around the active circuitry and not be longitudinally extending walls. (CRB at 91 (citing CX-1048C at Q. 55; Tr. at 1520:12-23).) Qimonda states that embedding tungsten into a groove to create a post does not teach the creation of elongated contacts. (*Id.* (citing CX-1048C at Q. 54-55; RX-684 at 1:33-36, 5:9-13, 5:53-55, Fig. 2; RX-772C at Q. 225; Tr. at 1520:12-23).) Qimonda argues that Shinogi teaches that the term "post" is used in accordance with its ordinary meaning. (*Id.* (citing RX-686 at Fig. 2, RX-684 at 1:33-36).)

Qimonda reiterates its argument that Dr. Bravman failed to offer any specific testimony regarding the dependent claims. (CRB at 92 (citing CX-1048C at Q. 56; RX-772C at Q. 234-237).) Qimonda argues that Respondents' new arguments regarding the dependent claims are untimely and should be disregarded. (*Id.*)

Qimonda states that Respondents' remark about Dr. Glew's infringement analysis was taken out of context and is misleading. Qimonda addresses Dr. Glew's infringement testimony and asserts that it is wholly consistent with his invalidity opinions. (*Id.* at 92-93 (citing CX-1048C at Q. 54; RX-684 at 5:53-55; RX-772C at Q. 225; CX-110C at Q.17-131; Tr. at 1518:21-1520:23; CX-125C; CX-126C; CX-129C; CX-130C; CX-132C; CX-133C; CX-135C; CX-451C; CX-996C; CX-997C; CDX-20C; CDX-21C; CDX-27C; CPX-9).)

Commission Investigative Staff's Position: Staff contends that Shinogi does not anticipate the asserted claims of the '918 patent. (SIB at 69-70.) Staff does not believe that the disclosure of "posts" or "pickets" such as those disclosed in Shinogi clearly and convincingly meet claim 1's limitation requiring "wherein said first and second contacts are of substantially greater longitudinal dimension than lateral dimension." (*Id.* at 70.)

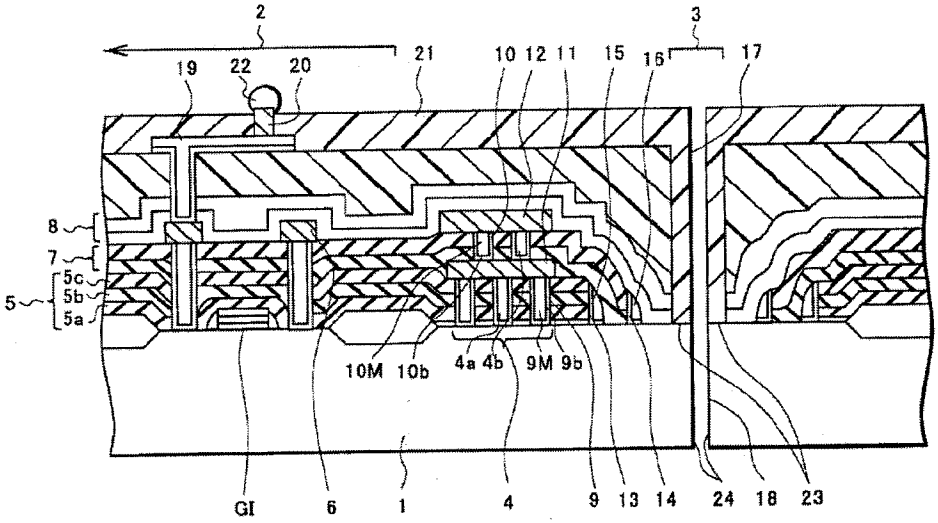
Discussion and Conclusion: Based upon the evidence before me, I find that Respondents have demonstrated by clear and convincing evidence that Shinogi anticipates asserted claims 1, 2, 4, and 11 of the '918 patent.

I first address Qimonda's argument that Respondents are precluded from arguing that Shinogi anticipates the asserted claims. Qimonda argues that Dr. Bravman relied on Shinogi as an obviousness reference, but changed his opinion before trial. Respondents argue that Dr. Bravman dropped the obviousness arguments based on Qimonda's decision to remove claims 3, 5, 6, and 8 from the investigation.

I find that Dr. Bravman's anticipation opinions find proper support in his expert report. Respondents cite to the invalidity chart from Dr. Bravman's expert report that compares the asserted claims against Shinogi. (RX-730.) While Dr. Bravman prefaces the chart with an explanation that "the reference(s) charted below render(s) obvious, alone or in combination with other prior art…the asserted claims as described below," Dr. Bravman clearly only relies on Shinogi to meet the claim limitations of asserted claims 1, 2, 4, 7, and 11. (*Id.*) Thus, I find that Qimonda had proper notice that Dr. Bravman believed that Shinogi anticipated asserted claims 1, 2, 4, 7, and 11. *Schering Corp.*, 339 F.3d at 1377.

Shinogi was filed on February 8, 2000 and claims priority to a February 9, 1999 Japanese patent application, meaning that it qualifies as prior art under 35 U.S.C. § 102(e). Qimonda has not offered any argument to the contrary. Shinogi is not cited on the face of the '918 patent. (JX-5.)

The parties' dispute focuses on a single limitation from claim 1: "wherein said first and second contacts are of substantially greater longitudinal dimension than lateral dimension." I find that Shinogi clearly and convincingly discloses this limitation. Respondents focus on Figure 1 from Shinogi:



(RX-684 at Fig. 1.)

Respondents contend that the element marked 11 is the first conductive line, the element marked 12 is the second conductive line, the element marked 1 is the substrate, the elements marked 9M are the first contacts, and the elements marked 10M are the second contacts. (*See* RDX-57.) Dr. Bravman testified that because Shinogi teaches that the structure can be made as seal grooves surrounding the IC circuit formation, Shinogi discloses contacts of substantially greater longitudinal dimension than lateral dimension. (RX-772C at Q. 233.) Dr. Glew opines that this limitation is not met because Shinogi describes elements 9M and 10M as "posts." (CX-1048C at Q. 54-55.)

I concur with Qimonda that use of the term "posts" connotes a structure of similar shape to the prior art contacts described in the '918 patent. If that was the only description of the contacts, then there would not be clear and convincing evidence that Shinogi anticipates. But Qimonda ignores the rest of the disclosure in Shinogi, which makes clear that the "posts" are actually longer than they are wide.

Shinogi describes the contacts and the crack stop structure (referred to as a "seal ring") as follows:

> According to the configuration, the seal ring is provided on the outer periphery, thus if moisture is entered from the outside, it is blocked by means of the seal ring, making it possible to prevent the internal IC circuit formation part from being degraded.

(RX-684 at 2:18-22.)

> According to the configuration, moisture is blocked by means of a plurality of rings, so that it is made possible to block moisture perfectly.

(*Id.* at 2:41-43.)

> However, here, tungsten plugs are used for the IC circuit formation part 2 for interconnection, thus W is embedded in each seal groove 9, 10, forming a metal post 9M, 10M.

(*Id.* at 5:9-12.)

> However, the seal grooves 9 and 10 are provided and metal posts 9M and 10M made of metal are embedded in the seal grooves 9 and 10. Thus, if moisture enters the chip from the flank exposed to a dicing line 24 through a dicing groove 23 via a dicing flank 17 or 18, the seal ring 4 can block the moisture.

(*Id.* at 5:54-59.)

> Subsequently, a plurality of seal grooves 9 and 10 are formed in the first interlayer insulating film 5 so as to expose the semiconductor substrate 1 by photolithography, and tungsten is embedded in the seal grooves 9 and 10. The three grooves (the number of the grooves is not limited) are formed like rings and at the same time, an opening with a first flank 13 as a component is made.

(*Id.* at 7:40-46.)

> Three tungsten plugs of the first layer are formed as rings surrounding the IC circuit formation part 2, and the first metal electrode 11 is formed as a wide ring for covering all the rings.

(*Id.* at 8:4-8.)

The specification refers to the contacts as either posts or tungsten plugs. The above-quoted passages make clear that the tungsten plugs are formed in the seal grooves, and that they extend like a ring around the circuitry. The specification further makes clear that the seal ring is intended to "block moisture perfectly," and states that the tungsten plugs function to block moisture. In addition, claims 8 and 9 of Shinogi refer to the plugs as "metal layers," providing further support that the "posts" in Shinogi are actually continuous rings of metal that surround the integrated circuit. Thus, based on these disclosures in Shinogi, I find that Shinogi discloses contacts that are of substantially greater longitudinal dimension than lateral dimension. (RX-772C at Q. 233.)

Qimonda's argument in response is limited to the fact that Shinogi uses the term "posts," and "posts" are not continuous walls. (CX-1048C at Q. 54-57.) While this argument has some superficial appeal, it ignores the full disclosure of Shinogi, which clearly explains that the contacts form rings around the circuitry.

Besides the limitation discussed *supra*, Shinogi meets the other limitations of claim 1. Shinogi discloses a semiconductor chip including a substrate and a crack stop structure. (RX-684 at 1:27-32, 4:27-40, Figs. 1-2; RX-772C at Q. 226-228.) Shinogi includes the claimed first and second conductive lines. (RX-684 at 5:5-13, Fig. 1; RX-772C at Q. 229, 231; RDX-57.) Shinogi includes the claimed at least two first and second contacts. (RX-684 at 5:5-13, 5:46-59, 7:40-57, Fig. 1; RX-772C at Q. 230, 232; RDX-57.) Thus, I find that Respondents have offered clear and convincing evidence that claim 1 is anticipated by Shinogi.

Regarding the dependent claims, Dr. Bravman does not provide testimony in his direct witness statement, but his claim chart (RX-730) provides the necessary detail. Claim 2 adds the requirement that there are three contacts connected between the substrate and the first conductive line. Shinogi discloses this claim limitation. (RX-684 at 4:66-5:2, Fig. 1; RX-730; RDX-57.) Thus, I find that Shinogi anticipates claim 2.

Claim 4 adds the requirement that there is dielectric material surrounding the crack stop structure. Shinogi discloses this claim limitation. (RX-684 at 7:31-39, 8:25-31, 9:4-6, Fig. 1; RX-730; RDX-57.) Thus, I find that Shinogi anticipates claim 4.

Claim 7 adds the requirements of a third conductive line and at least two third contacts connected to both the second and third conductive lines, wherein the contacts extend longitudinally along a length of the third conductive line. I find that Shinogi fails to disclose these claim limitations. Figure 1 of Shinogi only shows first and second conductive lines.

Respondents and Dr. Bravman point to the following passage from Shinogi to support their argument that Shinogi anticipates claim 7:

> A semiconductor device shown in FIG. 1 is a semiconductor chip just after a wafer is diced, namely, a semiconductor wafer formed with a large number of elements is cut on dicing line parts 3 and a semiconductor chip 1 comprises a first seal ring 4 disposed between an IC circuit formation part 2 and the dicing line part 3. Since the IC circuit formation part 2 itself of the semiconductor chip 1 consists of two metal layers, the seal ring 4 is of a two-story structure consisting of a first layer seal ring 4a and a second layer seal ring 4b. ***Therefore, a seal ring of a two-or-more-story structure is possible depending on the number of metal layers. For example, for three metal layers, seal rings of a one-story structure to a three-story structure are possible.***

(RX-684 at 4:27-39) (emphasis added.)

While this passage contemplates the use of a three-story seal ring structure, nothing in this passage indicates that there will be ***at least two*** third contacts between the second conductive line and the third conductive line. Thus, I find that Shinogi does not clearly and convincingly disclose all of the elements of claim 7.

Claim 11 adds the requirement that the first and second contacts extend over the entire length of the first conductive line. For all of the reasons discussed with respect to the disputed limitation in claim 1, Shinogi discloses this claim limitation. (RX-684 at 2:18-22, 2:41-43, 7:40-46, 8:4-8, Fig. 1; RX-730.) Thus, I find that Shinogi anticipates claim 11.

3. Ma

Respondents' Position: Respondents contend that U.S. Patent No. 6,509,622 to Ma, et al. ("Ma") anticipates the asserted claims in the '918 patent. (RIB at 235.)

Respondents claim that Ma discloses a semiconductor chip, as Figure 3 of Ma is a conceptual drawing of a very small portion of a semiconductor chip (die) 103. (RIB at 236 (citing RX-868 at 2:8-10; RX-772C at Q. 198).) Respondents state that Ma discloses a substrate,

as the specification explains that "[a]n integrated circuit is formed on a die, which is typically a semiconductor substrate." (*Id.* (citing RX-868 at 1:13-14, 2:34-37).)

Respondents argue that Ma discloses the claimed crack stop structure. Respondents point to Figure 3 of Ma, which shows a guard ring 105. (RIB at 237 (citing RX-772C at Q. 200; RX-686 at 3:9-12).) Respondents state that guard ring 105 is the crack stop. (*Id.* (citing RX-686 at 3:9-12, 2:55-56).) Respondent assert that Figure 3 of Ma shows a first conductive line over the substrate as first-level metal guard-ring 305 of guard-ring-structure 311. (*Id.* (citing RX-772C at Q. 201; RDX-61.2; RX-686 at 4:16-45).)

Respondents argue that Ma discloses the claimed first contacts. (RIB at 237.) Respondents explain that Figure 3 of Ma shows vertical guard-ring substructures 317-319 of guard-ring structure 311. (*Id.* (citing RX-868 at 4:45-50, Fig. 3).) Respondents assert that although the drafter of Ma did not show a line in Figure 3 indicating that these are directly connected to the substrate, they clearly are. (*Id.* (citing RX-772C at Q. 202-203).) Respondents state that to be effective, a crack-stop structure must extend all the way down to the substrate. (*Id.* at 238 (citing RX-772C at Q. 202-203).) According to Respondents, to build a crack stop that extends only partially down into the chip runs directly contrary to the logic and purpose of such a structure. (*Id.* at 238 (citing RX-772C at Q. 202-203).)

Respondents claim that Ma's specification supports this understanding. Respondents point to the passage in the specification that states: "[i]n general, the via level guard rings 307-311 are formed on die 103 at the same time that the via level metallization is formed in circuit area 107 [shown in Figure 3], so the thickness 323 of each of the one or more via level guard rings is substantially the same as the thickness of the via levels in circuit area 107." (RIB at 238 (citing RX-868 at 4:57-62).) Respondents point to additional passages in the specification that

they claim support the understanding that the guard ring extends to the substrate. (*Id.* at 238-239 (citing RX-686 at 2:8-14, 4:45-50, Fig. 1A).)

Respondents state that Dr. Glew's only argument that Ma does not anticipate is that the "connected to the substrate" limitation is not met. (RIB at 239.) Respondents assert that Dr. Glew's reading of Ma is too limited, as Dr. Glew opines that Ma only discloses via levels between metallization levels. (*Id.* (citing CX-1048C at Q. 50; RX-686 at 3:42-44).) Respondents argue that Dr. Glew's testimony on cross-examination show that his position is not reasonable. (*Id.* at 239-240 (citing Tr. at 657:10-19, 659:11-14).) Respondents claim that Dr. Glew selectively focuses on one passage from the specification but ignores others that demonstrate that the contacts 317-319 are connected to the substrate. (*Id.* at 240 (citing RX-686 at 1:13-14, 2:55-56, 4:34-37, 4:57-60, 4:64-5:4; CX-1048C at Q. 24).) Respondent thus assert that Ma teaches at least two first contacts: (1) be connected to the substrate and to the first conductive line; (2) be spaced apart from each other; and (3) and extend longitudinally along a length of the first conductive line. (*Id.* at 240-241 (citing RX-772C at Q. 202-203; RX-732).)

Respondents claim that Ma discloses the claimed second conductive line, as Figure 3 of Ma shows a second-level metal guard ring, labeled 304, of guard-ring-structure 310 and at least two second-level contacts connected to the first and second conductive lines that are spaced apart from each other and that extend longitudinally along a length of the second conductive line. (RIB at 241 (citing RX-772C at Q. 204; RX-686 at 4:33-37, Fig. 3; RX-732; RDX-61.4).) Respondents state that Figure 3 of Ma at 310 shows five second contacts connected to the first and second lines. According to Respondents, these contacts meet the requirements of the second contacts in claim 1. (*Id.* (citing RX-686 at 4:45-50, Fig. 3; RX-772C at Q. 205; RX-732; RDX-61.5).)

Finally, Respondents claim that Ma discloses that the first and second contacts are of a substantially greater longitudinal dimension than lateral dimension. (RIB at 241-242.) Respondents state that the guard ring substructures of Figure 3 are made up of concentric rings. According to Respondents, the "concentric rings would necessarily be substantially greater longitudinally than laterally[.]" (*Id.* (citing RX-686 at 3:10-12, 4:16-17, 4:19-22, 4:45-50, Fig. 3; RX-772C at Q. 206; RX-732; RDX-61.6).)

Regarding dependent claim2, Respondents state that Figure 3 of Ma shows that guard-ring substructures of guard-ring structure 311, which correspond to the first contacts of Claim 2 of the '918 patent, consist of five contacts. (RIB at 242 (citing RX-686 at 4:45-50, Fig. 3; RX-772C at Q. 209; RX-732; RDX-61.7).)

Regarding dependent claim 4, Respondents note that the specification of Ma explains that the "interconnects are embedded in a dielectric, such as an oxide or a low-K dielectric, such as xerogel." (RIB at 242 (citing RX-686 at 2:46-48).) In addition, Respondents note that Ma states that vias are formed through a dielectric material. (*Id.* (citing RX-686 at 3:40-43).) Respondents assert that Ma further states that "the one or more via level guard ring structures 307-311" are formed "at the same time that the via level metallization is formed in circuit area 107." (*Id.* (citing RX-686 at 4:57-60).) Respondents argue that one of ordinary skill in the art would thus recognize that the dielectric surrounds the guard ring substructures. (*Id.* (citing RX-772C at Q. 210; RX-732; RDX-61.9).)

Regarding dependent claim 7, Respondents state that Ma discloses a third-level metal guard ring (303) and four vertical substructures that form guard ring structure (309). Each of the substructures is connected to the third-level metal guard ring structure (303) and the second level metal guard ring (304). Thus, according to Respondents, Ma discloses the required elements of

claim 7. (RIB at 243 (citing RX-686 at 3:10-12, 4:32-34, 4:45-50, Fig. 3; RX-772C at Q. 217; RX-732; RDX-61.12).)

Regarding dependent claim 11, Respondents reiterate that Ma teaches that the guard ring substructures shown in Figure 3 are separated concentric rings, and Figure 1A shows those structures encircling the IC. (RIB at 243 (citing RX-686 at 3:10-12, 4:45-50).) Respondents argue that because the structure extends along the entire periphery of the chip, Ma discloses the additional limitation of dependent claim 11 requiring that the first and second contacts extend over the entire length of the first metal line. (*Id.* (citing RX-772C at Q. 220; RX-732; RDX-61.15).)

In their reply brief, Respondents address Qimonda's argument that Respondents failed to set out their arguments regarding Ma prior to trial. (RRB at 96.) Respondents state that Qimonda has been aware of this reference from almost the beginning of the investigation. (*Id.*) Respondents state that Ma was reclassified as an anticipatory reference, instead of an obviousness reference, because Qimonda dropped claims 3, 5, 6, and 8 shortly before the hearing. (*Id.*) Respondents claim that Qimonda has been on notice since the filing of the very first expert report of Respondents' reliance on Ma. (*Id.* at 97 (citing RX-732).)

Respondents reiterate their position that Ma shows a crack stop structure connected to the substrate. Respondents state that "although the drafter of Figure 3 did not show a line indicating that the contacts in Ma are directly connected to the substrate, they clearly are." (RRB at 99-100 (citing RX-772C at Q. 202-203).)

Respondents note Qimonda's argument that one of ordinary skill in the art would recognize that it is not desirable to connect a crack stop to the substrate because of damage that may be caused. (RRB at 100 (citing CIB at 171).) Respondents claim that this argument is

wholly unsupported by the evidence cited by Qimonda. (*Id.* (citing CX-1048C at Q. 35; Tr. at 1522:17-1524:13).)

Respondents argue that Dr. Glew's testimony on cross examination expressly contradicts Qimonda's contention. According to Respondents, Dr. Glew acknowledged that it would be particularly effective to have a crack-stop structure connected to the substrate because doing so would provide additional support for the crack stop. (RRB at 100 (citing Tr. at 648:5-9).) Respondents cite to additional testimony from Dr. Glew that they claim shows that Dr. Glew realized the benefits of connecting a crack stop to the substrate. (*Id.* at 100-101 (citing Tr. at 648:10-649:2).)

Respondents point to Dr. Bravman's testimony on this subject and claims that it also contradicts Qimonda. (RRB at 101.) Respondents state that Dr. Bravman explained that an effective crack stop must extend down to the substrate. (*Id.* (citing RX-772C at Q. 202-203).)

Respondents contend that even if Ma does not anticipate, the combination of Ma and a prior art reference that teaches a crack stop that is connected to the substrate would render the asserted claims obvious. (RRB at 101.) Respondents state that "Ma or Nye, in combination with Shinogi, admitted prior art showing crack stops connected to the substrate, or standing alone simply because of the beneficial effects of connecting the crack stop to the substrate that one of ordinary skill in the art would recognize, also render the '918 Patent invalid as obvious." (*Id.* (citing RX-772C at Q. 94, 155, 221, 230; RX-730).)

Qimonda's Position: Qimonda contends that Ma does not anticipate the asserted claims. (CIB at 170.)

As an initial matter, Qimonda argues that Dr. Bravman's opinion concerning Ma as an anticipatory reference should be disregarded. (CIB at 165-166.) Qimonda asserts that Dr.

Bravman only relied on Ma as an obviousness reference in his expert report and deposition. Qimonda claims that Dr. Bravman's anticipation argument with respect to Ma is untimely and should be rejected for that reason. (*Id.*)

Qimonda argues that Ma fails to disclose that the first contacts are connected to the substrate. (CIB at 165-166.) Qimonda points to Dr. Bravman's testimony, where he stated that Figure 3 of Ma fails to clearly show that the guard ring is connected to the substrate. (*Id.* citing CX-1048C at Q. 50-51; RX-686 at 3:29-46; RX-772C at Q. 202).) Dr. Glew agrees that Ma does not explicitly disclose a crack stop structure connected to the substrate. (*Id.* (citing CX-1048C at Q. 50-51; RX-686 at 3:29-46; RX-772C at Q. 202).) Qimonda claims that Dr. Bravman's testimony regarding what the drafter of Ma meant to disclose is unsupported and incorrect. (*Id.* at 170-171 (citing CX-1048C at Q. 50-51; RX-686 at 3:29-46, Fig. 3; RX-772C at Q. 202-203).)

Qimonda argues that Dr. Bravman's testimony is contrary to the understanding of one of ordinary skill in the art that it is not desirable to connect a crack stop to the substrate because of the damage that may be caused. (CIB at 171 (citing CX-1048C at Q. 35; Tr. at 1522:17-1524:13).) Qimonda further argues that Dr. Bravman's assertions are contrary to the express teachings of Ma. (*Id.* at 171-172 (citing CX-1048C at Q. 49-51; RX-686 at 3:29-46; RX-772C at Q. 202).)

In its reply brief, Qimonda argues that Respondents' argument relies on the inherency doctrine, which Respondents disclaimed. (CRB at 93-94.) Qimonda reiterates its argument that Ma does not disclose a crack stop connected to the substrate, a point that was conceded by Dr. Bravman. (*Id.* at 94 (citing CX-1048C at Q. 50-51; RX-686 at 3:29-46, Fig. 3; RX-772C at Q. 202).)

Commission Investigative Staff's Position: Staff contends that Ma does not anticipate the asserted claims. (SIB at 69.) After summarizing the positions of the experts regarding whether or not Ma discloses a crack stop connected to the substrate, Staff states that while the issue is very close, Staff does not believe that Ma clearly and convincingly disclose a crack stop connected to the substrate. (*Id.* (citing CX-1048C at Q. 50).)

Discussion and Conclusion: Based upon the evidence before me, I find that Respondents have not demonstrated by clear and convincing evidence that Ma anticipates asserted claims 1, 2, 4, 7, and 11 of the '918 patent.

I first address Qimonda's argument that Respondents are precluded from arguing that Ma anticipates the asserted claims. Qimonda argues that Dr. Bravman relied on Ma as an obviousness reference, but changed his opinion before trial. Respondents argue that Dr. Bravman dropped the obviousness arguments based on Qimonda's decision to remove claims 3, 5, 6, and 8 from the investigation.

I find that Dr. Bravman's anticipation opinions find proper support in his expert report. Respondents cite to the invalidity chart from Dr. Bravman's expert report that compares the asserted claims against Ma. (RX-732.) While Dr. Bravman prefaces the chart with an explanation that "the reference(s) charted below render(s) obvious, alone or in combination with other prior art…the asserted claims as described below," Dr. Bravman clearly only relies on Ma to meet the claim limitations of asserted claims 1, 2, 4, 7, and 11. (*Id.*) Thus, I find that Qimonda had proper notice that Dr. Bravman believed that Ma anticipated asserted claims 1, 2, 4, 7, and 11. *Schering Corp.*, 339 F.3d at 1377.

I find that Respondents have not demonstrated clearly and convincingly that Ma discloses at least two first contacts connected to the substrate. Respondents rely on Figure 3 from Ma, which is shown below:

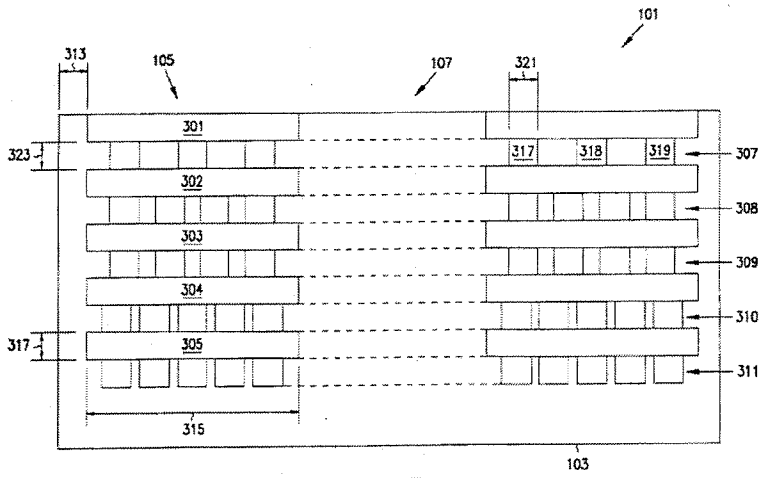


Figure 3

(RX-686 at Fig. 3.)

Respondents claim that the element marked 305 is the first conductive line, and the boxes below the first conductive line are the first contacts. (RX-772C at Q. 201-202; RDX-61.) The element labeled 103 is a die, and is described in the specification: "[d]ie 103 includes a substrate and a circuit area 107. The die is typically fabricated from a semiconductor, and integrated circuit structures, such as active devices, passive devices, and interconnects, are formed in circuit area 107." (RX-686 at 2:34-37.)

Dr. Bravman acknowledged that "[t]he drafter of Ma did not show a line in Figure 3 of Ma clearly indicating that guard ring substructures 317-319 are directly connected to the substrate." (RX-772C at Q. 202.) Nevertheless, Dr. Bravman testified that the identified first contacts are connected to the die 103, which he identified as the claimed substrate. (*Id.* at Q. 202-203.) Dr. Bravman based this opinion on his belief that all effective crack stops must extend all the way down to the substrate. (*Id.* at Q. 203.) He stated that in his career, he has never seen

a crack stop that was not formed upwards from the substrate. (*Id.*) He likened the situation to building a fence to keep out intruders, but leaving the bottom three feet of the fence open. (*Id.*)

Dr. Glew criticized Dr. Bravman's testimony, claiming that he improperly filled in gaps in the reference that are not present. (CX-1048C at Q. 50-51.) Dr. Glew opined that the teachings of Ma demonstrate that the identified contacts do not connect to the substrate. (*Id.*)

I find that the evidence does not clearly and convincingly support a finding that Ma discloses contacts connected to the substrate. Figure 3 from Ma, on which Respondents rely, does not clearly demonstrate any particular connection between the contacts and the substrate. This is admitted by Dr. Bravman when he opines that Ma fails to clearly indicate that the contacts are connected to the substrate. (RX-772C at Q. 202.) What remains is Dr. Bravman's assertion that the contacts must connect to the substrate. In light of Dr. Glew's opinion, I find that Dr. Bravman's assertion is insufficient to meet the clear and convincing evidence standard. While it may be possible that the contacts in Ma are connected to the substrate, that fact has not been proven by clear and convincing evidence. Thus, Respondents have failed to meet their burden to prove that Ma anticipates the asserted claims. *See In re Fritch,* 972 F.2d 1260, 1266 (Fed. Cir. 1992); *In re Royka*, 490 F.2d 981, 983-985 (C.C.P.A. 1974).

4. Sauber

Respondents' Position: Respondents contend that U.S. Patent No. 6,028,347 to Sauber, et al. ("Sauber") anticipates the asserted claims. (RIB at 243.)

Respondents claim that Sauber discloses a semiconductor chip. Claim 1 of Sauber recites: "A semiconductor structure, comprising: a semiconductor chip having . . . ." (RIB at 245 (citing RX-666 at 2:65, 4:59-60; RX-772C at Q. 130).) Respondents assert that Sauber discloses a substrate. (*Id.*) Respondents state that the substrate or base layer of Sauber's chip 20

is not separately numbered but is subsumed within the reference to chip 20 itself in Figure 3, it is clearly the lower portion of the chip marked with broad diagonal lines. (*Id.* (citing RX-772C at Q. 131; RX-728).)

Respondents argue that Sauber discloses a crack stop structure. Sauber calls the structure labeled 28 in Figure 3 a seal ring. (RIB at 246 (citing RX-666a t 3:4-18; RX-772C at Q. 132).) Respondents contend that this seal ring acts as a crack stop. (*Id.* (citing RX-772C at Q. 228).) Respondents state that Sauber's seal ring provides both a barrier to prevent incursion of contaminants and a crack-stop structure as required by claim 1. (*Id.* (citing RX-772C at Q. 132; RX-728).)

Respondents assert that Figure 3 clearly shows that seal ring 28 comprises three horizontal conductive lines disposed over the substrate. (RIB at 246 (citing RX-666 at 3:5-7, Fig. 3).) Respondents states that there are four first-level contacts are connected to the substrate and to the first conductive line; three contacts are connected to the first and second conductive lines; and two are connected to the second and third conductive lines. (*Id.*)

Respondents state that Sauber describes the vertical members of the seal ring (the contacts) as tungsten posts. (RIB at 246 (citing RX-666 at 3:5-7).) Respondents claim that these "posts" are actually longitudinally continuous walls that extend along the periphery of the functional circuitry of the chip. (*Id.* at 246-247 (citing RX-772C at Q. 140; RX-728).) Respondents claim that this must be so because seal-ring 28, in addition to providing crack stop protection, was created to seal off the functional circuitry of the chip against the incursion of moisture and contaminants from the dicing lines at the periphery. (*Id.* at 247 (citing RX-666 at 1:10-14).)

Respondents note that Dr. Glew testified during his infringement analysis that if the first and second contacts were not continuous walls, then there would be a possible path for moisture. (RIB at 247 (citing CX-110C at Q. 104).) Respondents argue that this position is inconsistent with Dr. Glew's invalidity opinion, where he states that the posts of Sauber are not continuous walls. (*Id.* (citing CX-1048C at Q. 33).)

Respondents claim that Dr. Glew's opinion that the seal ring in Sauber is not connected to the substrate is incorrect. (RIB at 247-248 (citing CX-1048C at Q. 32).) Respondents state that Sauber clearly shows that the seal ring is connected to the substrate. (*Id.* (citing RX-666 at 2:66-67, 3:20-21, 3:49-50).)

Respondents state that Dr. Glew's sole reason for asserting that the contacts in Sauber do not meet the claim limitations of claim 1 is that they are labeled as "posts." (RIB at 248.) According to Respondents, "post" is not a term of art in the semiconductor industry, and it can refer to a contact or plug that is formed by embedding material in a groove that extends in a ring around the periphery of an integrated circuit. (*Id.* (citing Tr. at 1309:17-23, 1327:21-23; RX-772C at Q. 140).)

Regarding dependent claim 2, Respondents states that seal ring 28 of Figure 3 of Sauber includes four first contacts, so Sauber discloses at least three first contacts, as required by the additional limitation of dependent claim 2. (RIB at 248 (citing RX-772C at Q. 143; RX-728).)

Regarding dependent claim 4, Respondents state that Figure 3 of Sauber shows the seal ring structure surrounded by a layer of dielectric, labeled number 42. (RIB at 249 (citing RX-666 at 3:28-30).) In addition, Respondents claim that it is well known to one of ordinary skill in the art that such conductive lines and contacts would be surrounded by dielectric material in order for the device to work. (*Id.* (citing CX-110C at Q. 118).)

Regarding dependent claim 7, Respondents state that Figure 3 of Sauber shows a third conductive line disposed over a portion of the second conductive line and two third contacts, connecting the second and third conductive lines. (RIB at 249 (citing RX-666 at Fig. 3).) Respondents argue that the contacts of the seal ring form continuous walls that are substantially longer than they are wide in order for the seal ring to inhibit penetration of contaminants and moisture into the active areas of the device. (*Id.* (citing RX-772C at Q. 151-152; RX-728).)

Regarding dependent claim 11, Respondents state that because the primary function of seal ring 28 is to seal off the active devices from the introduction of moisture or other contaminants, it is clear that the vertical members of seal-ring 28 are longitudinally continuous walls that extend along the periphery of the functional circuitry of the chip. (RIB at 249-250 (citing RX-772C at Q. 154; RX-728).) Respondents note that Dr. Glew testified that continuous walls were necessary to avoid providing a path for moisture to enter the active area of the chip. (*Id.* at 250 (citing CX-110C at Q. 108).)

In their reply brief, Respondents address Qimonda's argument that Respondents failed to set out their arguments regarding Sauber prior to trial. (RRB at 96.) Respondents state that Qimonda has been aware of this reference from almost the beginning of the investigation. (*Id.*) Respondents state that Sauber was reclassified as an anticipatory reference, instead of an obviousness reference, because Qimonda dropped claims 3, 5, 6, and 8 shortly before the hearing. (*Id.*) Respondents claim that Qimonda has been on notice since the filing of the very first expert report of Respondents' reliance on Sauber. (*Id.* at 97 (citing RX-728).)

Respondents again point to Dr. Glew's infringement testimony and claim that he stated that a crack stop must be a continuous structure to prevent the incursion of moisture, contaminants, and cracks into the device. (RRB at 102 (citing CX-110C at Q. 69).) Because the

seal ring in Sauber is used to prevent the incursion of moisture and contaminants, Respondents argue that following Dr. Glew's logic leads to the conclusion that the seal ring in Sauber is made up of continuous walls. (*Id.* at 102-103.)

Qimonda's Position: Qimonda contends that Sauber does not anticipate the asserted claims. (CIB at 166.)

As an initial matter, Qimonda argues that Dr. Bravman's opinion concerning Sauber as an anticipatory reference should be disregarded. (CIB at 165-166.) Qimonda asserts that Dr. Bravman only relied on Sauber as an obviousness reference in his expert report and deposition. Qimonda claims that Dr. Bravman's anticipation argument with respect to Ma is untimely and should be rejected for that reason. (*Id.*)

Qimonda argues that Sauber is nearly identical to the prior art which the applicant overcame during prosecution, and Sauber does not teach the elongated contacts required in claim 1. (CIB at 167.) Qimonda asserts that Sauber teaches the use of vertically disposed posts of tungsten. (*Id.* (citing CX-1048C at Q. 30, 33; RX-772C at Q. 138; RX-666 at 3:4-7).) Qimonda states that there is no debate between the experts that Sauber discloses the use of posts. (*Id.* (citing CX-1048C at Q. 30, 33; RX-772C at Q. 138; RX-666 at 3:4-7).) Qimonda claims that Dr. Bravman's opinion that the posts in Sauber are walls is unsupported by the evidence. (*Id.* (citing RX-772C at Q. 138-140; CX-1048C at Q. 34-37; Tr. at 1522:17-1524:13; CDX-42).)

In its reply brief, Qimonda claims that Respondents' argument relies on the inherency doctrine, which Respondents disclaimed. (CRB at 95-96.) Qimonda reiterates its position that Sauber discloses posts and not elongated contacts. (*Id.* at 96-97.) Qimonda contends that Dr. Glew's infringement and valid analyses are consistent, contrary to Respondents' argument. (*Id.* (citing CX-110C at Q. 63, 69; CDX-21; Tr. at 1518:21-1520:23).) Qimonda claims that Dr.

Glew provided testimony that the term "post" is used in the semiconductor industry in the same way it is used in the everyday world. (*Id.* at 97 (citing RX-772C at Q. 31, 88-89; CX-1048C at Q. 13; JX-5; JX-6: Tr. at 1519:7-1520:23).) Qimonda claims that silicon dioxide is an excellent seal, and it is unnecessary for Sauber to contain elongated walls. (*Id.* (citing CX-1048C at Q. 35; Tr. at 1522:17-1524:13).)

Commission Investigative Staff's Position: Staff contends that Sauber does not anticipate the asserted claims. (SIB at 67.) Staff argues that Sauber fails to disclose that the first and second contacts are of substantially greater longitudinal dimension that lateral dimension. (*Id.*) It is Staff's belief that Sauber discloses "posts" or "pickets" and thus does not meet the claim limitation. (*Id.*) Staff concludes that "the Sauber patent appears to teach that the connection between the substrate and the metal lines are posts or pickets and not a continuous wall." (*Id.* at 67-68.)

Discussion and Conclusion: Based upon the evidence before me, I find that Respondents have not demonstrated by clear and convincing evidence that Sauber anticipates asserted claims 1, 2, 4, 7, and 11 of the '918 patent.

I first address Qimonda's argument that Respondents are precluded from arguing that Sauber anticipates the asserted claims. Qimonda argues that Dr. Bravman relied on Sauber as an obviousness reference, but changed his opinion before trial. Respondents argue that Dr. Bravman dropped the obviousness arguments based on Qimonda's decision to remove claims 3, 5, 6, and 8 from the investigation.

I find that Dr. Bravman's anticipation opinions find proper support in his expert report. Respondents cite to the invalidity chart from Dr. Bravman's expert report that compares the asserted claims against Sauber. (RX-728.) While Dr. Bravman prefaces the chart with an

explanation that "the reference(s) charted below render(s) obvious, alone or in combination with other prior art…the asserted claims as described below," Dr. Bravman clearly only relies on Sauber to meet the claim limitations of asserted claims 1, 2, 4, 7, and 11. (*Id.*) Thus, I find that Qimonda had proper notice that Dr. Bravman believed that Sauber anticipated asserted claims 1, 2, 4, 7, and 11. *Schering Corp.*, 339 F.3d at 1377.

The parties dispute whether or not Sauber discloses first and second contacts that "are of substantially greater longitudinal dimension than lateral dimension." The parties focus on the following Figure from Sauber:

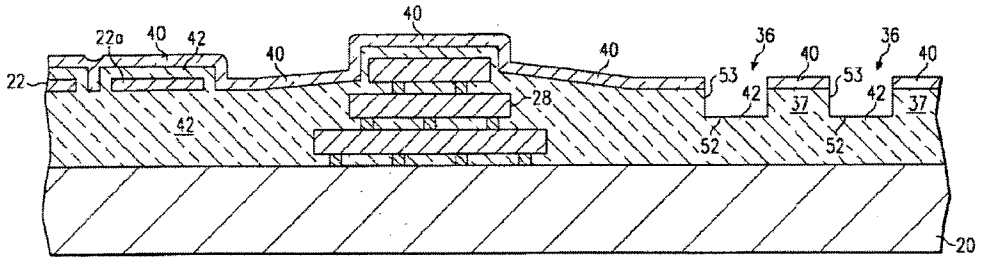


FIG. 3

(RX-666 at Fig. 3.)

The element labeled 28 is the seal ring, which the parties agree is a crack stop structure. (RX-772C at Q. 132-133; CX-1048C at Q. 30.) In explaining the composition of the seal ring, Sauber states: "[t]he seal ring 28 includes horizontally disposed layers of aluminum and vertically disposed post of tungsten." (RX-666 at 3:5-7.)

Qimonda contends that because the contacts are described as "posts," they are not longer than they are wide, as required by claim 1. (CX-1048C at Q. 32-33.) Qimonda asserts that Sauber has a similar structure to the prior art discussed in the '918 patent. (*Id.*)

Respondents contend that the "posts" are actually "longitudinally continuous walls that extend along the periphery of the functional circuitry of the chip." (RX-772C at Q. 138.) Respondents argue that because the seal ring in Sauber must prevent moisture and other

contaminants from destroying the functional circuitry, the "posts" must be continuous walls so that there are no gaps in the seal ring. (*Id.* at Q. 139-140.)

The evidence does not clearly and convincingly support a finding that Sauber discloses that the first and second contacts "are of substantially greater longitudinal dimension than lateral dimension." The use of the term "post" implies that the contacts are of a similar shape to the prior art contacts shown in Figures 1A & 1B in the '918 patent. (JX-5 at 1:24-59, Figs. 1A-1B.) Sauber does not provide any additional detail on the shape of the posts or whether they extend longitudinally along the conductive lines.[70] (*See generally* RX-666.) Neither party offers any evidence that the term "post" has a special meaning in the semiconductor field that would require the posts in Sauber to be longer than they are wide.

Dr. Bravman opines that because the seal ring in Sauber is meant to protect the circuitry from moisture and contaminants, its must be made up of a continuous wall, meaning that the posts would necessarily be longer than they are wide. I find that there is not clear and convincing evidence that supports this opinion. In the Background section of the specification, Sauber contains a very brief discussion of protecting against moisture and contaminants:

> Also, a seal ring is typically formed in the dielectric layer around the outer edge region of the chip to protect the active devices formed in the inner region of the chip from contaminants.

(RX-666 at 1:10-13.)

> As noted briefly above, the die fabrication process creates intrinsic stresses in: the dielectric layers (i.e., a silicon dioxide insulating layers used to, inter alia, electrically isolate the electrical interconnect lines); the aluminum electrical interconnect lines; and, the passivation layer on the surface of the die. When the die is encapsulated, additional stresses are generated by the expansion differential between the die and molding compound as the die cools to room temperature. To further complicate the issue, the adhesive bond between the molding compound sometimes fails (i.e., delaminates) which can concentrate forces and stresses on the die's surface. ***If the stresses are high enough, it is possible for the***

[70] In contrast, Shinogi provides sufficient additional detail to overcome the plain meaning of "posts."

> ***passivation layer and/or the dielectric layers to crack. Once this has occurred, moisture can penetrate into the aluminum lines which can cause corrosion leading to device failure.***

(*Id.* at 1:41-56) (emphasis added.)

Neither passage appears to provide any support for Dr. Bravman's assertion, and the second passage appears to contradict Dr. Bravman. Specifically, the second passage states that moisture penetration only becomes a problem if the passivation layer or dielectric layers crack. This implies that when these layers are not cracked, there is no moisture problem. Thus, this passage does not support the opinion that the seal ring needs to be a continuous wall to prevent moisture penetration. Because Sauber provides no clear evidence that the first and second contacts are of substantially greater longitudinal dimension than lateral dimension, I find that Respondents have failed to demonstrate that Sauber anticipates the asserted claims. *See In re Fritch,* 972 F.2d 1260, 1266 (Fed. Cir. 1992); *In re Royka*, 490 F.2d 981, 983-985 (C.C.P.A. 1974).

VI. INFRINGEMENT

A. Applicable Law

Complainant must prove either literal infringement or infringement under the doctrine of equivalents. Infringement must be proven by a preponderance of the evidence. *SmithKline Diagnostics, Inc. v. Helena Labs. Corp.*, 859 F.2d 878, 889 (Fed. Cir. 1988). A preponderance of the evidence standard "requires proving that infringement was more likely than not to have occurred." *Warner-Lambert Co. v. Teva Pharm. USA, Inc.*, 418 F.3d 1326, 1341 n. 15 (Fed. Cir. 2005).

Literal infringement is a question of fact. *Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1332 (Fed. Cir. 2008). Literal infringement requires the patentee to prove that the accused

device contains each and every limitation of the asserted claim(s). *Frank's Casing Crew & Rental Tools, Inc. v. Weatherford Int'l, Inc.*, 389 F.3d 1370, 1378 (Fed. Cir. 2004).

As for the doctrine of equivalents:

> Infringement under the doctrine of equivalents may be found when the accused device contains an "insubstantial" change from the claimed invention. Whether equivalency exists may be determined based on the "insubstantial differences" test or based on the "triple identity" test, namely, whether the element of the accused device "performs substantially the same function in substantially the same way to obtain the same result." The essential inquiry is whether "the accused product or process contain elements identical or equivalent to each claimed element of the patented invention[.]"

TIP Sys., LLC v. Phillips & Brooks/Gladwin, Inc., 529 F.3d 1364, 1376-77 (Fed. Cir. 2008) (citations omitted).

Thus, if an element is missing or not satisfied, infringement cannot be found under the doctrine of equivalents as a matter of law. *London v. Carson Pirie Scott & Co.*, 946 F.2d 1534, 1538-39 (Fed. Cir. 1991). Determining infringement under the doctrine of equivalents "requires an intensely factual inquiry." *Vehicular Techs. Corp. v. Titan Wheel Int'l, Inc.*, 212 F.3d 1377, 1381 (Fed. Cir. 2000).

B. The '670 Patent

1. Claim 1

Claim 1 recites:

> 1. A method for the manufacture of a polycrystalline silicon layer on a substrate, comprising the steps of:
>
> depositing an amorphous silicon layer on a substrate; and
>
> then controlling the phase transformation of the amorphous silicon into a polycrystalline layer by the steps of:
>
> heating said substrate with said amorphous silicon layer to an initial temperature that is lower than a crystalline temperature for the amorphous silicon,

holding the substrate with said amorphous silicon layer at the initial temperature to achieve a thermal equilibrium of the substrate with the amorphous silicon layer at said initial temperature, and then, after reaching the thermal equilibrium,

continuing the heating of said substrate with said amorphous silicon layer to raise the temperature at a controlled rate through a reproducible prescribed temperature profile from said initial temperature to a target temperature, said target temperature being higher than the crystallization temperature of said amorphous silicon so that said amorphous silicon crystallizes and becomes a polycrystalline layer having a defined grain size and texture.

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2. Claim 6

Claim 6 recites:

6. A method as claimed in claim 1, wherein said target temperature is in a range of approximately 700° C to 800° C.

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3. Claim 7

Claim 7 recites:

7. A method as claimed in claim 1, wherein said step of controlled heating from said initial temperature to said target temperature is carried out with a controlled rate of no more than 10° C change in temperature per minute.

Qimonda's Position: {

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C. The '434 Patent

1. Claim 1

Claim 1 recites:

1. A semiconductor component, comprising:

a semiconductor body having a terminal pad, a semiconductor function element, and an electrically conductive connecting line connecting said terminal pad to said semiconductor function element;

a protective element for protecting against electrostatic discharge, being connected between said terminal pad and said semiconductor function element;

a first supply line for a first supply potential, being connected to said semiconductor

function element;

a second supply line for the first supply potential, being connected to said protective element and being electrically conductively connected to said first supply line; and

a clamp element being connected to said connecting line and to said first supply line, for limiting a voltage applied to said clamp element to a clamp value.

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2. Claim 2

Claim 2 recites:

2. The semiconductor component according to claim 1, including at least one bond connection connecting said first and second supply lines to one another.

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3. Claim 3

Claim 3 recites:

3. The semiconductor component according to claim 2, wherein said semiconductor function element has a terminal, said at least one bond connection has a terminal, said first supply line has a portion disposed between said terminal of said semiconductor function element and said terminal of said at least one bond connection, and said clamp element is connected to said portion of said first supply line.

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4. Claim 4

Claim 4 recites:

4. The semiconductor component according to claim 1, wherein said semiconductor function element is connected to said first supply line and to said connecting line at a given location, and said clamp element has a first terminal connected to said first supply line and a second terminal connected to said connecting line, in the immediate spatial vicinity of said given location.

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5. Claim 5

Claim 5 recites:

5. The semiconductor component according to claim 1, wherein said clamp element includes an MOS transistor having a main current path connected to said connecting line and to said first supply line and a gate terminal connected to said first supply line.

Qimonda's Position: {

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6. Claim 7

Claim 7 recites:

7. The semiconductor component according to claim 1, wherein said connecting line has a given resistance, said protective element includes a resistor connected between said terminal pad and said semiconductor function element, and said resistor has a resistance being adjusted for setting a sum of the resistance of said resistor and the given resistance to a predetermined value.

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7. Claim 8

Claim 8 recites:

8. The semiconductor component according to claim 7, including additional protective elements having resistors, additional semiconductor function elements and additional connecting lines respectively connecting said semiconductor function elements to said protective elements and having a given resistance, forming a multiplicity of protective elements, semiconductor function elements and connecting lines, and a sum of the resistance of said resistors and the given resistance is substantially constant for said multiplicity of protective elements, semiconductor function elements and connecting lines.

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8. Claim 11

Claim 11 recites:

11. The semiconductor component according to claim 1, wherein said semiconductor function element is an input switching stage, and including an output driver stage being connected to said terminal pad and to said second supply line.

Qimonda's Position: {

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D. The '899 Patent

1. Claim 1

Claim 1 recites:

A method for fabricating devices including the step of forming isolation between device structures fabricated on a substrate comprising:

defining active and non-active regions on a surface of the substrate;

forming isolation trenches of varying widths the active regions comprising active regions of varying width in the non-active regions;

forming a layer of HDP-CVD insulating material of silicon oxide, wherein the HDP-CVD silicon oxide layer is non-planar and protrudes angularly above isolation trench edges forming sloping edges that slope away from the trench on the substrate by high density plasma-enhanced chemical vapor deposition (HDP-CVD), the HDP-CVD layer substantially filling the trenches and covering the active regions;

removing at least a portion of the insulating material covering the active regions; and

planarizing the surface of said substrate to expose the active regions, the removal of at least a portion of insulating material from the active regions providing a planar topography; wherein removing of at least a portion of the insulating material from the active regions includes:

depositing a mask layer over the insulating material;
patterning the mask layer to expose at least a portion of the insulating material over the active regions; and
removing the exposed portion of the insulating material over the active regions, leaving unexposed portions of the insulating materials; and wherein the mask layer is deposited using an inverse active area mask that is biased so that the mask layer after patterning covers the non-active regions and at least a portion of the active regions.

Qimonda's Position: {

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In its reply brief, Qimonda asserts that Dr. Gutmann's testimony that {

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2. Claim 2

Claim 2 recites:

2. A method according to claim 1 wherein the inverse active area mask is biased so that the mask layer after patterning covers at least a portion of the sloping edges of the insulating layer in the active regions.

Qimonda's Position: {

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3. Claim 7

Claim 7 recites:

7. A method according to claim 1 further including the step of removing the mask layer after removing the exposed insulating material.

Qimonda's Position: {

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4. Claim 22

Claim 22 recites:

22. A method of planarizing shallow isolation trenches in a substrate comprising:

depositing a silicon oxide layer formed in an inductively coupled high density plasma chamber by chemical vapor deposition so as to fill said trenches and cover the surface of the substrate, thereby forming a non-planar layer over the surface that angles away from the edges of the trenches;

depositing a photoresist layer on the oxide layer and patterning the photoresist layer with an inverse active area mask while biasing the layer so that the photoresist overlies at least a portion of the angled oxide layer;

removing the silicon oxide in the exposed regions;

removing the photoresist; and

planarizing the surface of the substrate.

Qimonda's Position: {

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5. Claim 23

Claim 23 recites:

23. A method according to claim 22 wherein the surface of the substrate is planarized by removing the remaining silicon oxide by chemical metal polishing.

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E. The '918 Patent

1. Claim 1

Claim 1 recites:

1. A semiconductor chip, comprising:

a substrate; and

a crack stop structure comprising:

> a first conductive line disposed over the substrate;
>
> at least two first contacts connected to the substrate and to the first conductive line, the at least two first contacts being spaced apart from each other and extending longitudinally along a length of the first conductive line;
>
> a second conductive line disposed over a portion of the first conductive line; and at least two second contacts connected to the first conductive line and the second conductive line, the at least two second contacts being spaced apart from each other and extending longitudinally along a length of the second conductive line; and
>
> wherein said first and second contacts are of substantially greater longitudinal dimension than lateral dimension.

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2. Claim 2[87]

Claim 2 recites:

2. The chip as recited in claim 1, wherein the at least two first contacts includes three contacts.

Discussion and Conclusion: {

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3. Claim 4

Claim 4 recites:

4. The chip as recited in claim 1, further comprising a dielectric material surrounding the crack stop structure.

Discussion and Conclusion: {

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4. Claim 7

Claim 7 recites:

7. The chip as recited in claim 1, further comprising:

a third conductive line disposed over a portion of the second conductive line; and

at least two third contacts connected to the second conductive line and the third conductive line, the at least two third contacts being spaced apart from each other and extending longitudinally along a length of the third conductive line.

Discussion and Conclusion: {

}

{

}.

5. Claim 11

Claim 11 recites:

11. The chip as recited in claim 1, wherein the at least two first contacts and the at least two second contacts extend over the entire length of the first metal line.

Discussion and Conclusion: {

}

VII. LICENSE DEFENSE

Respondents' Position: Respondents contend that two legacy Agere Systems, Inc. ("Agere") products that Qimonda accusing of infringement are licensed under the asserted patents. (RIB at 250-251.) Specifically, Respondents state that the two Agere products at issue are the { } (*Id.* at 250.)

Respondents argue that the two Agere products are covered by a { } { } (the "PLA"). (RIB at 250 (citing RX-844C at ¶ 103(c); RX-1077C at Q. 14-15).) { } { }

{

}

Respondents claim that Lucent granted a sublicense to Agere { }in February 2001 as part of various agreements providing for the separation and distribution of assets between Lucent entities and Agere Systems as part of the spin-off of Agere from Lucent that began in 2001. (RIB at 251 (citing RX-988; RX-1077C at Q. 28-29).) At that time, Lucent owned at least 50% of the shares of Agere Systems, and it continued to be the majority shareholder of Agere until June of 2002. (*Id.* (citing RX-1077C at Q. 35-37).) Respondents explain that in 2000, Agere Systems Inc. was formed as a separate legal entity, but it was still a wholly-owned subsidiary of Lucent. (*Id.* (citing RX-1077C at Q. 35).) Next, there was a partial IPO in 2001, after which Lucent continued as the majority shareholder. (*Id.* (citing RX-1077C at Q. 35).) Respondents claim that it was not until June of 2002 that Lucent no longer held a majority of the shares in Agere Systems. (*Id.* (citing RX-1077C at Q. 37).) {

}

Respondents aver that Agere currently remains a legal entity. (RIB at 251 (citing RX-1077C at Q. 38-40).) Respondents state that the patents at issue were licensed to Lucent {

} Respondents conclude

that the asserted patents are therefore covered { } and Qimonda has no right to enforce them in this action against any legacy Agere product. (*Id.*)

Qimonda's Position: Qimonda contends that LSI has failed to prove that it is licensed to practice any of the asserted patents. (CIB at 211.)

Qimonda argues that Respondents failed to cite any legal authority in support of their license defense in their pre-hearing brief. Qimonda therefore claims that the license defense should be deemed abandoned or withdrawn in accordance with Ground Rule 8.2. (CIB at 211-212.) Further, Qimonda states that Respondents failed to present evidence of their license defense in their direct case. Because a license defense is an affirmative defense for which Respondents bear the burden of proof, Qimonda argues that Respondents are required to prove such a defense in their direct case. (*Id.* at 212 (citing *Carborundum Co. v. Molten Metal Equip. Innov., Inc..*, 72 F.3d 872, 878 (Fed. Cir. 1995); *Bandag, Inc. v. Al Bolser's Tire Stores, Inc.*, 750 F.2d 903, 924 (Fed. Cir. 1984); *Lucent Techs., Inc. v. Newbridge Networks Corp.*, 168 F. Supp. 2d 181, 240 (D. Del. 2001)).) Qimonda asserts that Respondents only presented evidence related to their license defense in their rebuttal case and therefore waived the defense.

Turning to the substance of the defense, Qimonda argues that LSI failed to prove that any of the accused products are within the scope { } (CIB at 214.) {

}Qimonda states that LSI acquired Agere on April 2, 2007 through a merger of Agere and a subsidiary of LSI's named Atlas

Acquisition Corp. (*Id.* (citing CX-556C at LSI-337-665-0000274, 275, 283, 285, 292, 295, 296, 297, 298, 299, 300, 302, 303, 305, 308, 309, 314, 318, 322, 328, 332, 339, 342, 343, 344, 345, 347, 402; CX-839C at SEA665ITC0012005, 12006, 12014, 12023, 12024, 12027, 12028, 12029, 12032, 12033, 12036, 12046, 12051, 12054, 12055, 12071, 12072, 12074, 12075, 12076, 12090; CX-1051 at 1; Tr. at 1583:13-1588:17, 1592:11-15, 1592:23-1593:15; CX-481 at 103:23-105:12; Pallinti Tr. at 1606:22-1608:1).) Qimonda concludes that any sublicense to Agere that might have existed { } {

} (*Id.* at 215 (citing RX-844C at LSI-337-665-1358244-45).)

Qimonda notes that Respondents cannot point to any evidence that Agere currently sells any products. (CIB at 215 (citing Tr. at 1594:20-22).) Qimonda states that as of January 1, 2009, there are no employees of Agere and all former Agere employees are now directly employees of LSI. (*Id.* (citing Tr. at 1591:6-1592:1).) Qimonda assert that the building where Agere was formerly housed does not bear any signage identifying Agere and instead now bears signage bearing the names of LSI Corporation and Infineon. (*Id.* (citing Tr. at 1593:23-1594:1).)

Qimonda next argues that {

} Qimonda argues that there is no evidence in the record that Agere sold any products at all from the time that it was formed in 2000 until its spin-out, or divestiture, from Lucent in 2001. (*Id.* at 216 (citing RX-1077C; Tr. at 1556:20- 1598:6).) Qimonda states that there is no evidence in the record that Agere sold any { }

{ } from the time that it was formed in 2000 until its spin-out, or divestiture, from Lucent in 2001. (*Id.* (citing RX-1077C; Tr. at 1556:20-1598:6).)

Qimonda claims that Respondents are expected to argue that the reference in Article 1.03(d) of the PLA { } should be construed to mean any products sold by a business unit of Lucent that eventually became Agere. (CIB at 216.) Qimonda argues that under New York law, the language is limited to products sold during the period from the time that the divested business (Agere) was formed until the divested business (Agere) was divested. (*Id.* (citing RX-844C at LSI-337-665-1358244-45).) Qimonda claims that this construction best realizes the parties' intent because { } (*Id.* at 216-217 (citing RX-844C at LSI-337-665-1358244-45; *Greenfield v. Philles Records, Inc.*, 98 N.Y.2d 562, 569, 750 N.Y.S.2d 565, 780 N.E.2d 166 (2002)).) Qimonda reiterates its arguments in its reply brief. (See CRB at 114-115.)

Commission Investigative Staff's Position: Staff takes no position on Respondents' licensing defense.

Discussion and Conclusion: Based upon the evidence before me, I find that Respondents have failed to meet their burden to demonstrate that the { } products are licensed to practice the asserted patents.

The existence of a patent license is an affirmative defense to a claim of patent infringement. *Carborundum Co. v. Molten Metal Equip. Innov., Inc..*, 72 F.3d 872, 878 (Fed. Cir. 1995). The burden rests on the alleged infringer to prove the license defense. *Id.* The interpretation of a patent license is a matter of state law. *See Studiengesellschaft Kohle, m.b.H.*

v. Hercules, Inc., 105 F.3d 629, 632 (Fed. Cir. 1997) (interpreting a patent license agreement under Delaware law).

Qimonda has raised two procedural arguments regarding Respondents' patent license defense. First, Qimonda claims that Respondents' pre-hearing brief was not sufficiently detailed as required by Ground Rule 8.2. Ground Rule 8.2 requires that the parties' contentions be set forth "with particularity" in the pre-hearing brief, and that the parties include citations to supporting legal authorities.

Here, I find that Respondents' discussion of the license defense in the pre-hearing brief was sufficient to meet Ground Rule 8.2. Respondents identified the two Agere products at issue, and identified the relevant license agreement. While Respondents do not include any citations to legal authorities in their pre-hearing brief, they likewise do not cite any legal authorities in their post-trial brief. (*See* RIB at 250-251.) Thus, I find no merit to Qimonda's complaint regarding the lack of citations to legal authorities.

Next, Qimonda argues that because Respondents bear the burden to prove the license defense, Respondents were required to present the evidence of the license defense in their direct case. Qimonda claims that Respondents failed to do this, and instead introduced the evidence in their rebuttal case. I concur. Similar to the issue of invalidity, patent license is an affirmative defense on which Respondents bear the burden. *Carborundum Co.*, 72 F.3d at 878. Thus, Respondents were required to prove their license defense through their direct case. This would allow Qimonda the opportunity to offer rebuttal evidence. Respondents failed to do this, as they presented their license defense as part of their rebuttal case. (Tr. at 1552:22-25.)[88] Thus, I find

[88] Qimonda raised an objection to this at the hearing, and I reserved judgment until the Initial Determination. (Tr. at 1568:19-1572:21.)

that Respondents waived the opportunity to raise the license defense by failing to include it in their direct case.

Assuming, *arguendo*, that Respondents' license defense was properly part of the case, I find that Respondents have failed to meet their burden to prove the license defense.

The license agreement relied on by Respondents is a 2001 agreement between Lucent Technologies GRL Corporation ("Lucent") and Siemens Aktiengesellschaft ("Siemens"). (RX-844C.) The license is governed by New York law. (*Id.* at ¶ 4.05.) Each party granted a license to the other party under its patents for "communications products." (*Id.* at ¶ 1.01.) The term "communications products" was defined to include {

} (*Id.* at Appendix A.) The term was further defined to include { }

(*Id.*)[89]

The parties focus on the provision in paragraph 1.03(d) of the license agreement, which provides in pertinent part:

{

[89] Because of this broad definition, there is no dispute between the parties that the two Agere products in question qualify as "communications products."

}

}

According to Respondents, Agere was formed in 2000 as a separate legal entity, but it was a wholly owned subsidiary of Lucent. (RX-1077 at Q. 35.) There was a partial IPO in 2001, after which Lucent was still a majority shareholder in Agere. (*Id.*) It was not until June 2002 that Lucent no longer held a majority of the shares in Agere. (*Id.* at Q. 37.) Lucent sublicensed the patents to Agere pursuant paragraph 1.03(d) when the parties entered into a 2001 license agreement. (RX-1077C at Q. 28-34; RX-988.)

In 2007, LSI acquired Agere through the merger of Agere and an LSI subsidiary. (CX-556C.) LSI claims that Agere is now a wholly-owned subsidiary of LSI. (RX-1077C at Q. 38.)

Thus, Respondents claim that Agere is a divested business { } (RIB at 251.) Respondents further claim that Agere remains a legal entity. (RX-1077C at Q. 38.) Further, Respondents claim that the {

} are of the kind of products sold or furnished by Agere prior to the divestiture. (*Id.* at Q. 41-42.)

I find that Respondents have failed to meet their burden in demonstrating that the {

} products are currently licensed under the asserted patents. The language from {

}

Thus, the sublicense does not extend to any products sold by LSI, or any products sold by Agere after it was acquired by LSI.[90]

VIII. REMEDY & BONDING

A. General Exclusion Order

Qimonda's Position: Qimonda seeks a general exclusion order excluding from entry into the United States { } incorporating infringing LSI integrated circuits. (CIB at 302.)

Qimonda argues that there is a pattern of violation of the patents-in-suit evident both with respect to { } and with respect to non-respondent companies' { } that contain LSI ICs. (CIB at 303 (citing CX-544C at Q. 200; CX-945 at 6).) Qimonda states that manufacturers of { } in addition to LSI use LSI ICs in { } (*Id.* (citing CX-544C at Q. 195; RX-1298C at Q. 207-208).) Qimonda states that non-respondent foreign producers purchase LSI ICs and incorporate those ICs into { } for export to the United States. (*Id.* (citing CX-544C at Q. 195; RX-1298C at Q. 207-208).) Qimonda identifies the following LSI customers using LSI ICs to produce { } adapters: { } (*Id.* at 303-304 (citing CX-59C at 137:10-138:11; CX-1018C at 35:1-9; 93:3-11; RX-1298C at Q. 207-208; CX-544C at Q. 210; JX-23C, Ex. 18).) Qimonda notes that several of LSI's current customers using LSI ICs are potential sources of products similar to the { } adapters that LSI sells. (*Id.* at 304 (citing CX-544C at Q. 210; JX-23C, Ex. 18; CX-965; CX-959; CX-958; RX-1298C at Q. 207-208).)

[90] In addition, while Agere may remain a legal entity, there is evidence that it is not active at the present time. As of January 1, 2009, all Agere employees became LSI employees. (Tr. at 1591:10-1591:1592:1.) When asked whether one could buy products from Agere today, Mr. Waskiewicz responded "I do not know." (*Id.* at 1594:20-22.)

Qimonda claims that the majority of other non-respondent companies using LSI ICs in their { } are not licensees of Qimonda AG. (*Id.* (citing CX-8C; JX-23C, Exs. 21-22; RX-1298C at Q. 255-259; Tr. at 1813:19-1816:11).)

Qimonda argues that it is difficult to identify the { } of non-respondent foreign producers that contain LSI ICs. (CIB at 304 (citing CX-544C at Q. 215, 216).) In the face of a limited exclusion order, Qimonda claims that the pattern of trade in goods containing LSI ICs would likely make it difficult to identify the sources of { } containing infringing LSI ICs. (*Id.* (citing CX-544C at Q. 215).) Qimonda asserts that products containing ICs are sold through multiple supply channels by foreign manufacturers and domestic importing distributors. (*Id.* (citing CX-983, Ex. 55; CX-544C at Q. 126).) According to Qimonda, there are extensive marketing and distribution networks in the United States available to existing and potential manufacturers of products containing ICs. (*Id.* (citing CX-983, Ex. 55; CX-544C at Q. 126).)

Qimonda argues that { } would continue to enter the United States under a non-respondent brand name and would likely enter in increased volumes. (CIB at 304-305 (citing CX-544C at Q. 215).) Qimonda claims that LSI actively encourages customers such as { } to purchase LSI products and to sell them under the purchaser's own brand name. (*Id.* at 305 (citing CX-1018C at 59; CX-544C at Q. 202-204; CX-958; CX-986).)

Qimonda states that when LSI sells its { } for rebranding, the { } remains unchanged, but it bears a new brand, thereby making it difficult to identify the source of the infringing downstream product. (CIB at 305 (citing CX-544C at Q. 201; CX-945 at 6).) Qimonda argues that while the re-branded products of such

companies clearly should be covered by an exclusion order, LSI would have an economic incentive to find additional customers to sell its downstream products on a re-branded basis in order to evade a limited exclusion order. (*Id.* (citing CX-544C at Q. 215).)

Qimonda notes that Respondents argue in their prehearing brief that there is no widespread pattern of unauthorized use because "only 20 percent of all PC shipments were to the United States in the fourth quarter of 2008… [and] only 44 percent of server shipments were to North America in 2006." (CIB at 305 (citing RPHB at 339).) Qimonda claims that Respondents miss the point, as there is no requirement that a majority of worldwide sales must be to the United States. (*Id.*) Qimonda claims that the Commission evaluates the volume and value of imports into the United States; imports into other countries are irrelevant as to whether there exists a widespread pattern of unauthorized use for purposes of a general exclusion order. (*Id.* at 305-306.)

Qimonda states that Respondents also contend the potential for market entrants is diminished by the fact that existing firms that are not current LSI customers are likely to be delayed by the "design-in" process associated with some LSI products. (CIB at 306 (citing RPHB at 341).) In response, Qimonda argues that the threat of new companies entering the market with downstream products containing infringing LSI's ICs is no less real and measurable if it were to be delayed by a few months or even a year. (*Id.*)

Qimonda argues that a general exclusion order is necessary because an order limited to products of LSI and Seagate would be circumvented. (CIB at 306 (citing CX-544C at Q. 206).) Qimonda claims that if LSI is faced with a limited exclusion order, it could sell its ICs to foreign producers of the same types of downstream products that LSI would be prevented from exporting to the United States. (*Id.* (citing CX-544C at Q. 207).)

Qimonda argues that foreign producers of downstream products could use LSI ICs in the future. (CIB at 306 (citing CX-544C at Q. 211).) Qimonda states that because of the global economic recession, it appears that there is substantial unutilized capacity to produce such electronic products abroad. (*Id.* at 306-307 (citing CX-968; CX-969; CX-970; CX-544C at Q. 208).)

Qimonda claims that foreign producers of { } have the capability of incorporating LSI chips into their downstream products. (CIB at 307 (citing CX-544C at Q. 208).) Qimonda argues that in the event of an exclusion order on infringing LSI ICs, LSI would have a very strong economic incentive to set the price of its ICs to be attractive to new customers so as to permit LSI to maintain its IC production volume. (*Id.* (citing CX-544C at Q. 212).) Thus, numerous electronics assemblers might seek to assemble and sell these products if they could use LSI ICs at bargain prices. (*Id.* (citing CX-544C at Q. 211; CX-974; CX-975; CX-977).)

Qimonda asserts that in addition to foreign producers that may enter the market for downstream products incorporating LSI ICs, customers may enter the market with rebranded LSI downstream products. (CIB at 308.) According to Qimonda, LSI actively encourages customers to purchase LSI products and to sell them under the purchaser's own brand name. (*Id.* (citing CX-544C at Q. 201).) Qimonda argues that LSI would have an economic incentive to find additional customers to sell its downstream products on a re-branded basis and circumvent a limited exclusion order. (*Id.* at 309 (citing CX-544C at Q. 215).)

Qimonda states that a general exclusion order against downstream { } would not place an undue burden on legitimate commerce. (CIB at 309 (citing CX-544C at Q. 218).) Qimonda claims that LSI is able to identify and to track the sale of which

models of { } contain infringing ICs and which contain non-infringing ICs. (*Id.*) As such, Qimonda states that LSI would be capable of notifying its customers as to which LSI ICs have been determined by the Commission to be infringing and which are non-infringing. (*Id.* (citing CX-544C at Q. 220).) Qimonda avers that LSI's customers would have information as to which LSI ICs could be placed in downstream products destined for the United States and those that would need to be sold in foreign markets. (*Id.* (citing CX-544C at Q. 220).) With respect to the product-tracking abilities of these non-respondent producers of downstream products, they do, or could, identify which of their downstream products contain infringing LSI ICs. (*Id.* (citing CX-544C at Q. 220).)

According to Qimonda, many of LSI's customers are OEMs likely to have relatively sophisticated product and component tracking capabilities. (CIB at 309 (citing CX-544C at Q. 220).) Qimonda notes that {

} (*Id.* (citing CX-544C at Q. 220; CX-501C at 40:10-41:9).) Qimonda claims that other producers of downstream products containing LSI ICs would generally have a similar capability. (*Id.* at 310 (citing CX-544C at Q. 220).) Qimonda states that given the likely product tracking capabilities of the downstream product producers, the provision of certifications to U.S. Customs would not likely be an undue burden. (*Id.* (citing CX-544C at Q. 221).)

In its reply brief, Qimonda states that Respondents' contention that Qimonda should be foreclosed from receiving a GEO because it allegedly failed to name additional suppliers of { } also is unfounded. (CRB at 143 (citing RIB at 303-304).) Qimonda states that there is no requirement that Qimonda name additional parties, and a GEO is necessary to prevent new suppliers from entering the market and circumventing the LEO. (*Id.*) Qimonda

claims that in the event of an LEO on its ICs and downstream products, LSI would have an economic incentive to find a new commercial outlet for its excluded ICs, including foreign producers of downstream products that currently do not use LSI ICs but who can incorporate them into their downstream products. (*Id.* (citing CIB at 306).) According to Qimonda, LSI would have an economic incentive to find additional customers to sell its downstream products on a re-branded basis. (*Id.* (citing CX-544C at Q. 200, 203-204; CX-945 at 6.; CX-958C; CX-986).)

Qimonda states that contrary to Respondents' remaining argument, a GEO against downstream { } would not place an undue burden on legitimate commerce because LSI and Seagate are {

} (CRB at 143 (citing CX-501C at 39:21-24, 41:3-42:3; 42:22-25; CX-544C at Q. 138; CX-500C at 153:14-154:22).)

Respondents' Position: Respondents contend that Qimonda is not entitled to a general exclusion order. (RIB at 303.)

Respondents argue that Qimonda has not only fundamentally failed to define the scope of the general exclusion order that it requests, but Qimonda also fails to identify any credible evidence that would suggest that a general exclusion order is warranted in this case notwithstanding its scope. (RIB at 303.) Respondents state that to the extent that Qimonda may allege that a general exclusion order covering the downstream products of LSI's customers is warranted, Qimonda's failure to name known LSI customers, other than Seagate, should preclude any such claim. (*Id.* (citing RX1298C at Q. 158-161, 163; RDX-145C; JX23C at Ex. 16; RX-1356).)

Respondents assert that Qimonda is not entitled to a general exclusion order because LSI and Seagate have not engaged in a widespread pattern of unauthorized use, nor are the relevant business conditions such that foreign manufacturers are likely to attempt to enter the United States market with infringing { } or ICs, or products containing same. (RIB at 304 (citing RX-1298 at Q. 250, 277, 279-280).) Respondents allege that these conclusions are supported by Qimonda's choice to assert its patents against LSI and only one of its customers - Seagate. (*Id.*) Respondents argue that Qimonda has provided no evidence that it would receive any relief from a general exclusion order beyond what it would receive from a limited exclusion order, while the corresponding disruption to legitimate commerce would likely be substantial. (*Id.*)

In their reply brief, Respondents state that Staff correctly notes in its Post-trial Brief that neither Qimonda, nor its remedy expert, Dr. Button, identified the number of accused products that enter the U.S. as a percentage of world-wide LSI sales, the amount of these products that are imported into the U.S. by third parties, or the number of such products that are rebranded and imported into the U.S. (RRB at 139 (citing SIB at 104).) Respondents therefore assert that there is no evidence regarding the scope of any of this alleged widespread pattern of importation and unauthorized use. (*Id.*) Respondents argue that to the extent that any of LSI's OEM customers currently rebrand LSI's products and sell them as their own in the U.S., continuation of such practices after the issuance of a limited exclusion order does not support a finding of circumvention. (*Id.* (citing *Certain Baseband Process Chips and Chipsets, Transmitter and Receiver (Radio) Chips, Power Control Chips, and Products Containing Same, Including Cellular Telephone Handsets*, Inv. No. 337-TA-543, Comm'n Op. at 107-98 (June 19, 2007);

Certain GPS Devices and Products Containing Same, Inv. No. 337-TA-602, Comm'n Op. at 18 (January 15, 2009)).)

Respondents note that while there may indeed be underutilized capacity because of the global recession, there can be no dispute that there is no incentive to enter the semiconductor market during a recession such as this when semiconductor companies like Qimonda are failing. (RRB at 140 (citing Joint Stipulation at ¶ 3; JX-23C at 7; RX-1248 at 9; RX-1321C; Tr. at 717:2-6; RX-1321C; RX-1339 at 11534).) Respondents note that Staff agrees. (*Id.* (citing SIB at 105-106).)

Respondents claim that the evidence shows that identifying the source of infringing products is not difficult. (RRB at 140.) Respondents argue that not only are the entities that fabricate semiconductors and semiconductor components well known, but to the extent Qimonda argues that LSI's customers rebrand LSI's ICs and sell them in the U.S., LSI top-selling customers are easily identified. (*Id.* (citing RX-1298 at Q. 270-274; RDX-148C; JX-23C at 53, Exs. 21-22; RX-1299C; RX-1301C; RX-1302C; RX-1306C; RX-1331 at 12).) Respondents state that Qimonda did not adduce any evidence of any significant quantities of imports of infringing products outside of those allegedly attributable to Respondents. (*Id.* (citing *Certain Self-cleaning Litter Boxes and Components Thereof*, Inv. 337-TA-625, Comm'n Op. at 22 (April 28, 2009)).)

Commission Investigative Staff's Position: Staff contends that in the event a violation of Section 337 is found, Qimonda is not entitled to a general exclusion order. (SIB at 104.) Staff argues that there is no evidence to determine the scope of the alleged widespread importation and rebranding of LSI products by third parties. (*Id.*) Staff states that "neither Dr. Button nor Qimonda identify the number of accused products that enter the country as a percentage of

worldwide LSI sales, the amount of these products that are imported into the United States by third parties, or the number of such products that are rebranded and imported into this country." (*Id.*) Further, Staff notes that the Commission has made clear that non-respondent manufacturers that continue to import downstream products containing infringing articles after the issuance of a limited exclusion order cannot be deemed to have circumvented the exclusion order. (*Id.* at 105 (citing *Certain GPS Devices & Products Containing Same*, Inv. No. 337-TA-602, Commission Opinion at 18 (Jan. 15, 2009)).)

Staff states that the evidence shows that circumvention is unlikely because other chip makers have little incentive to enter the market due to the recent economic downturn. (SIB at 106 (citing *Certain Microsphere Adhesives, Process for Making Same, & Products Containing Same, Including Self-Stick Repositionable Notes*, Inv. No. 337-TA-366, Commission Opinion at 19, USITC Pub. 3949 (Jan. 1996)).) Staff states that "the fact that LSI may continue to sell to third-parties in unspecified quantities who may in turn rebrand the accused products is insufficient to warrant issuance of a general exclusion order." (*Id.*)

Staff does not believe the evidence demonstrates that it is difficult to identify the source of infringing products. (SIB at 106.) Staff contends that the entities that fabricate semiconductors are well known, as are the top selling customers of LSI. (*Id.*) Staff claims that Qimonda has failed to identify any significant quantities of imports of the accused products outside of those attributable to the named Respondents. (*Id.* at 107.) Staff claims that a general exclusion order should only issue in extraordinary circumstances, and those extraordinary circumstances are not present in this investigation. (*Id.*)

Discussion and Conclusion: In this Initial Determination, I have found no violation of Section 337. If, however, a violation of Section 337 is found by the Commission, I do not

recommend that the Commission issue a general exclusion order.

Pursuant to 19 U.S.C. § 1337(d), the Commission may issue either a limited or a general exclusion order. A limited exclusion order instructs the U.S. Customs and Border Protection ("CBP") to exclude from entry all articles that are covered by the patent at issue and that originate from a named respondent in the investigation. A general exclusion order instructs the CBP to exclude from entry all articles that are covered by the patent at issue, without regard to source.

A general exclusion order is permitted in certain limited situations. Specifically, the statute provides:

> (2) The authority of the Commission to order an exclusion from entry of articles shall be limited to persons determined by the Commission to be violating this section unless the Commission determines that—
>
> > (A) a general exclusion from entry of articles is necessary to prevent circumvention of an exclusion order limited to products of named persons; or
> >
> > (B) there is a pattern of violation of this section and it is difficult to identify the source of infringing products.

19 U.S.C. § 1337(d)(2) (2008); *see also Certain Hydraulic Excavators*, Inv. No. 337-TA-582, Commission Opinion (Feb. 3, 2009) (describing the standard for general exclusion orders).

Circumvention - 19 U.S.C. § 1337(d)(2)(A)

This prong of the statute requires a showing that "a general exclusion from entry of articles is necessary to prevent circumvention of an exclusion order limited to products of named persons[.]" I find that Qimonda has failed to demonstrate that a general exclusion order is necessary to prevent circumvention of an limited exclusion order.

Qimonda primarily relies on the testimony from its expert Dr. Button to assert that LSI, if faced with a limited exclusion order, would have a "clear economic incentive" to attempt to

circumvent the exclusion order by selling its ICs to foreign producers of downstream products. (CX-544C at Q. 207.) I find that Dr. Button's testimony regarding the likelihood of circumvention of a limited exclusion order is unsupported by the record and speculative. (*See Id.* at Q. 205-212.) Dr. Button provides no evidence that if a limited exclusion order was entered, it would be likely that LSI would attempt to sell their integrated circuit products to foreign downstream manufacturers (other than Seagate) so that it could circumvent the limited exclusion order. Further, Dr. Button provides no evidence that these un-named foreign downstream product manufacturers would be interested in purchasing LSI integrated circuits, and there is no evidence regarding whether or not it would be economically feasible for downstream manufacturers to switch to LSI integrated circuits if they are not currently LSI customers.

Pattern of Violation - 19 U.S.C. § 1337(d)(2)(B)

This prong requires a showing that "there is a pattern of violation of this section and it is difficult to identify the source of infringing products." The pattern of violation must be separate from the accused infringement alleged in this investigation. *See Certain Self-Cleaning Litter Boxes & Components Thereof*, Inv. No. 337-TA-625, Commission Opinion at 56 (Apr. 28, 2009) (explaining that a "pattern of violation of this section" must include acts of importation unrelated to one of the named respondents).

Qimonda focuses on LSI's practice of selling its products for re-branding. As described by Dr. Button, LSI products are sold to OEM customers, who in turn sell the products under their own brand. (CX-544C at Q. 201.) Examples of such OEM customers are { } (*Id.* at Q. 203-204.) Qimonda further identifies a number of LSI customers using the accused LSI integrated circuits in their downstream products and allegedly importing those products into the United States. (CIB at 303-304; RX-1298C at 207-208; CX-544C at Q. 210; JX-23 at Ex. 18.)

I find that Qimonda's argument lacks the necessary detail to demonstrate the necessary pattern of violation. Qimonda fails to present any evidence of the scope of the alleged unauthorized use, as it cites no documentation demonstrating the amount of products imported, the value of those products, or the number of companies importing such products. I find without any sufficient evidence regarding the scope of the alleged widespread pattern of violation, I cannot recommend the entry of a general exclusion order.

In addition, Respondents offer testimony to contradict Qimonda's assertions that there is a widespread pattern of unauthorized use. Respondents' expert testified that for LSI's top ten customers, approximately two-thirds of their product revenues are derived from sales outside of the United States. (RX-1298C at Q. 252-254; RDX-147C.) This is relevant because sales of products outside of the United States that remain outside of the United States do not constitute unauthorized use. Further, relying on Qimonda's list of licensees, Respondents' expert testifies that many of LSI's customers are potentially licensees to the patents-in-suit, making any use authorized. (*Id.* at Q. 255-261.) In addition, it appears that the re-branding activities so heavily relied upon by Qimonda are not as extensive in scope as Qimonda attempts to portray them. (*Id.* at Q. 262-266.)

Based on the lack of evidence offered by Qimonda, I cannot find that "there is a pattern of violation of" Section 337 that would warrant the entry of a general exclusion order. 19 U.S.C. § 1337(d)(2)(B).

B. Limited Exclusion Order

Qimonda's Position: Qimonda contends that the Commission should at least issue an limited exclusion order against infringing articles imported, sold for importation, or sold after importation by LSI and Seagate. (CIB at 261.) Qimonda states that the products at issue in this

investigation are LSI ICs and downstream products containing same. (*Id.* (citing CX-544C at Q. 88; RX-1298C at Q. 131).)

Qimonda argues that all LSI chips sharing the structural features, circuit designs, and/or fabrication processes relevant to the asserted patents are believed to be infringing. (CIB at 261 (citing CX-2 at QAG-665-ITC-0201290; CX-190C at Q. 60-65, 194, 266, 271, 276).) According to Qimonda, all LSI chips of the same technology node are extremely likely to share the vast majority of structural features and processing steps. (*Id.* at 261-262 (citing CX-2 at QAG-665-ITC-0201290; CX-190C at Q. 60-65, 194, 266, 271, 276).)

Qimonda argues that Respondents are incorrect that any exclusion order should be limited to the named products in this investigation. (CIB at 262.) Citing Commission precedent, Qimonda claims that exclusion orders should be directed to all products covered by the patent claims as to which a violation has been found, rather than limiting it to the products examined in the infringement analysis. (*Id.* (citing *Certain Hardware Logic Emulating Systems*, Inv. No. 337-TA-383, Comm'n Op., 1998 WL 307240 (March 1998); *Certain Electric Robots*, Inv. No. 337-TA-530, ID/RD, 2008 WL 1727624 (Dec. 19,2005); *Certain Unified Communications Systems, Prods. Used With Such Systems, and Components Thereof*, Inv. No. 337-TA-598, ID/RD (Jan. 28, 2009)).) Qimonda notes that if a limited exclusion order was limited to the accused products identified by Qimonda, Respondents could easily circumvent the order by increasing the production of infringing articles not named in this investigation. (*Id.* at 262-263 (citing *Certain Automated Mech. Transmission Sys. For Medium-Duty And Heavy-Duty Trucks*, Inv. No. 337-TA-503, ID, 2005 ITC LEXIS 241 at *303 (Jan. 7, 2005)).)

Qimonda asserts that the limited exclusion order should apply not only to LSI and Seagate, but also to their "affiliated companies, parents, subsidiaries, or other related business

entities, or their successors or assigns." (CIB at 263 (citing *Certain Light-Emitting Diodes*, Inv. No. 337-TA-512, Limited Exclusion Order (Jan. 11,2006); *Certain Pet Food Treats*, Inv. No. 337-TA-511, Limited Exclusion Order (June 1, 2005)).) Qimonda claims that a limited exclusion order should include articles that are sold under any trade name or brand name of Respondents or their affiliated companies, parents, subsidiaries, or other business entities, successors, or assigns, and any products that have been sold to third parties and that are merely rebranded ore relabeled before they are imported into the United States, sold for importation, or sold after importation into the United States. (*Id.* at 264 (citing *Certain Unified Communications Systems, Prods. Used With Such Systems, and Components Thereof*, Inv. No. 337-TA-598, ID/RD (Jan. 28, 2009); *Certain Laser Bar Code Scanners and Scan Engines, Components Thereof, and Prods. Containing Same*, Inv. No. 337-TA-551, Limited Exclusion Order, ¶ 1 (May 30, 2007)).)

Qimonda claims that, contrary to Respondents' assertions, they are still entitled to relief even though Qimonda has filed for bankruptcy. (CIB at 264.) Qimonda points to its discussion of the economic prong of domestic industry to support the assertion that Qimonda's domestic operations have not ceased. (*Id.*) In addition, Qimonda claims that Respondents provide no legal support for the position that the Commission should deny any relief because of Qimonda's financial status. (*Id.* at 264-265.) Qimonda notes that language of 19 U.S.C. § 1337(d)(1), which states that the Commission "shall direct that the articles concerned, imported by any person violating the provision of this section, be excluded from entry into the United States..." (*Id.* at 265.) Qimonda claims that a limited exclusion order is mandatory if a violation of Section 337 is found. (*Id.* (citing *Certain Unified Communications Systems, Prods. Used with Such Systems, and Components Thereof*, Inv. No. 337-TA-598, ID/RD, 2008 ITC LEXIS 319, at 378 (Jan. 28, 2008)).)

In its reply brief, Qimonda reiterates many of the same arguments described *supra*. (CRB at 131-135.) Qimonda addresses Respondents' argument that "the estate of what was

{

} (*Id.* at 133 (citing RIB at 282-283).)

{

} QAG must maintain this investigation to maximize those interests. (*Id.* at 133-134.) Qimonda states that QAG and QNA/QR collaborate in many respects. (CRB at 134.)

Qimonda claims that even if Qimonda AG's interests as an equity holder in QNA and QR are contrary to the interests of QNA's and QR's creditors, Qimonda AG is one of QNA's largest creditors. (CRB at 134.) According to June 18, 2009 filing in QNA's June 18, 2009 bankruptcy proceeding, Qimonda is QNA's largest creditor holding unsecured nonpriority claims, with a claim in the amount of $144,455,415.54. (*Id.*) Thus, Qimonda asserts that QAG's interests in the capacity as a QNA creditor are directly aligned with those of other QNA and QR creditors. (*Id.*)

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} (CRB at 134-135 (citing Tr. at 825:25-826:9, 868:21-873:17, 875:22-882:12, 889:17-890:1; Tr. at 986:1-2, 990:13-19, 1000:17-1001:4).)

Respondents' Position: Respondents contend that to the extent that the Commission finds Qimonda's prior domestic activities sufficient to establish both the economic prong and the technical prong of the domestic industry requirement, a remedy should not issue in this investigation because Qimonda has no domestic industry to warrant protection. (RIB at 279.)

Respondents claim that the following alleged facts support their argument that Qimonda is not entitled to any remedy in the event a violation is found:

- Qimonda and all of its subsidiaries relevant to this investigation, including those located in the United States, are insolvent and have filed for bankruptcy. (RIB at 279 (citing JX-23C at 7; RX-1248 at 9; RX-1282C; Tr. at 704:24-705:19, 705:20-706:8, 717:2-6; RX-1321C; RX-1322C).)

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  . } (RIB at 280 (citing RX-1298C at Q. 41, 52-57, 61-62; CX-989C at Q. 87, 88, 92, 96; Tr. at 708:25-709:5, 760:22-761:15, 762:16-20; Deposition Stipulations, Munn at Tab 10, 23:1-18, 28:12-22, 39:13-40:22, 74:22-77:3,1119:9-13, 81:21-183:11, 185:21-186:22; Tr. at 192:7-10; Tr. at 1013:16-1014:1; JX-23C at 20; RX-1248 at 4; RX-1253C at 95).)

- {

  } (RIB at 280 (citing JX-23C at 20; Button Report at 11; Deposition Stipulations, Munn at Tab 10, at 42:1-43:14, 66:4-7, 66:14-67:3, 95:21-96:3; RX-1298C at Q. 61-62; CX-989C at Q. 111; Tr. at 688:24-689:23, 763:1-5; RX-1248 at 4; Tr. at 1857:6-1858:6; RX-1253C at 95).)

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  } (RIB at 280 (citing Tr. at 763:6-17; Deposition Stipulations, Munn at Tab 10, 138:20-141:22).)

- {

  } (RIB at 281 (citing JX-23C at 20; RX-1298C at Q. 61-62, 105; RX-1248 at 4; RX-1253C, at 95; Deposition Stipulations, Munn at Tab 10, at 47:7-47:9, 47:21-48:22; 49:1-51:9, 59:15-17, 59:22-60:3, 62:4-14; Tr. at 726:6-20, 731:12-734:3, 762:21-25).)

- {

  . } (RIB at 281 (citing JX-23C at 20, 21; RX-1298C at Q. 83; Deposition Stipulations, Munn at Tab 10, 144:2-145:22, 151:3-18, 155:4-14; 159:5-10, 169:11-170:16, 171:5-14, 171:20-172:6, 175:7-11, 175:14-22, 178:7-17; CX-23C at 21; RX-1329 at F-3; Tr. at 977:22-978:2, 987:7-12).)

- {

  . } (RIB at 281 (citing RX-1298C at Q. 41, 52-54, 56; CX-989C at Q. 84, 88, 96; Tr. at 192:7-10; Deposition Stipulations, Munn at Tab 10, 23:1-18, 39:13-40:22, 119:9-13; JX-23C at 14; RX-1248 at 10; RX-1324; Tr. at 722/:5; Tr. at 1818:1-10).) {

  } (*Id.* at 282 (citing RX-1268; RX-1273C; RX-1274C; RX-1275C; RX-1276C; Tr. at 734:25-740:8; RX-1248 at 6-7).)

Respondents argue that since the Chapter 11 bankruptcy filings by Qimonda North America Corp. and Qimonda Richmond LLC on February 20, 2009, and the opening of Qimonda AG's formal insolvency proceeding on April 1, 2009, there exists a complete disconnect between the patents-in-suit and the nominal domestic activities involved in winding up Qimonda's U.S. operations. Respondents claim that the estate of what was Qimonda AG, which is being operated by Dr. Jaffe on behalf of Qimonda AG's creditors, retains the patents-in-suit. (RIB at 282 (citing Joint Stipulation; Tr. at 752:24-753:2).) They assert that the estates of Qimonda North America Corp. and Qimonda Richmond LLC, currently in Chapter 11 bankruptcy and being operated on behalf of Qimonda North America Corp.'s and Qimonda Richmond LLC's creditors, previously undertook or are undertaking the domestic activities claimed by Qimonda. (*Id.* (citing Tr. at 687:10-11, 19-20; CX-2 at 3; JX-23C, at 7; RX-1248 at 3, 9; RX-1321C; Tr. at 717:2-6; RX-1322C; RX-1298C at Q. 41; Deposition Stipulations, Munn at Tab 10, 23:1-18).)

Respondent thus claim that the estate of what was Qimonda AG does not control or influence the decisions or activities of the estates of Qimonda North America Corp. and

Qimonda Richmond LLC. (*Id.*) Respondent assert that the estate of what was Qimonda AG, {

.} (RIB at 282-283 (citing JX-23C at 7).) Thus, Respondents argue that any claim by Qimonda that the requisite nexus exists between the patents-in-suit and any nominal domestic activities involved in winding up Qimonda's U.S. operations going forward is baseless.

Respondents also note the { . } Respondents state that while Dr. Bayerl testified that any such entity would be located in the United States, the documents and materials related to the preliminary discussion clearly indicated {

. } (RIB at 283 (citing Tr. at 889:14-21, RX-1710C; RX-1711C).) Respondents claim that the proposal documents and materials also indicated that {

. } (*Id.* at 283-284 (citing RX-1710C; RX-1711C).) Respondents argue that these facts negate any finding that Qimonda has made a sufficient showing to demonstrate any domestic activities currently or going forward, much less that a "significant" or "substantial" level of such activities relating to the patents-in-suit currently exist or will exist in the future.

Respondents next argue that by reason of Order Nos. 23 and 37, and Qimonda's failure to adequately allege that any broader class of LSI products infringe, the scope of this investigation

includes only those integrated circuits produced pursuant to LSI's { } technologies, and downstream products containing such integrated circuits. (RIB at 287.) Respondents assert that any remedy may cover, at its broadest, only those integrated circuits produced pursuant to LSI's { } technologies, and downstream products containing such integrated circuits that are specifically found to infringe the patents-in-suit. (*Id.*) Respondents submit that any remedial order that issues should identify the specific products (by model number, etc.) or class of products (by the process technologies they are manufactured pursuant to, i.e., { } (*Id.*)

In their reply brief, Respondents claim that Qimonda's contention that any remedy should include products that are outside the scope of this Investigation expressly disregards the rulings in Order Nos. 23 and 37. (RRB at 135.) Respondents argue that scope of this Investigation, as narrowed by Qimonda's failure to adequately define the scope of allege infringing products, includes only those integrated circuits produced pursuant to LSI's { } technologies, and downstream products containing such integrated circuits. (*Id.* (citing Order Nos. 23 & 37).)

Commission Investigative Staff's Position: Staff contends that in the event a violation is found, the appropriate remedy is a limited exclusion order that covers all of Respondents' accused products that are manufactured abroad by or on behalf of, or imported by or on behalf of, the Respondents, or any of their affiliated companies, parents, subsidiaries, or other related business entities, or their successors or assigns. (SIB at 99.)

Discussion and Conclusion: In this Initial Determination, I have found no violation of Section 337. If, however, a violation of Section 337 is found by the Commission, I recommend that the Commission issue a limited exclusion order that applies to LSI, Seagate, and all of their

affiliated companies, parents, subsidiaries, or other related business entities, or their successors or assigns, and covers the semiconductor integrated circuits and products containing same found to infringe the asserted Qimonda patents.

Respondents first argue that Qimonda is not entitled to relief due to the fact that Qimonda has filed for bankruptcy and { } I find that such an argument is more appropriate for the economic prong analysis. If the Commission finds a violation of Section 337, then it has conclusively found that a domestic industry exists or is in the process of being established. 19 U.S.C. § 1337(a)(2) (2008). No additional domestic industry analysis should be necessary to determine whether Qimonda is entitled to any remedy. The statute clearly states that in the event of a violation, the Commission "***shall*** direct that the articles concerned, imported by any person violating the provision of this section, be excluded from entry into the United States..." 19 U.S.C. § 1337(d)(1) (2008) (emphasis added).[91] Respondents cite no support, and I find none, for the proposition that Qimonda may be denied a remedy, even after a violation is found, due to Qimonda's current business conditions.

Respondents next argue that the scope of any remedy should be limited by Order Nos. 23 and 37. Order Nos. 23 and 37 addressed the definitions of "Relevant Products" and "Seagate Downstream Goods" that Qimonda used in its discovery requests. Specifically, I found that Qimonda's definitions were overly broad, and I limited the definitions. Respondents now argue that those discovery orders should limit the scope of any exclusion order to cover only specific integrated circuits produced pursuant to LSI's { } and downstream products containing such integrated circuits.

I decline to recommend a limited exclusion order as proposed by Respondents.

[91] While 19 U.S.C. § 1337(d)(1) provides that the Commission may decline to enter an exclusion order after considering a number of public interest factors, Respondents do not raise that statutory provision here, and I find that it is inapplicable to the current situation.

Commission precedent has held that it is not appropriate to include specific product names in an exclusion order, as the exclusion order should extend to Respondents' products that are within the scope of the investigation and that are found to infringe the applicable patent or patents. *See Certain Integrated Repeaters, Switches, Transceivers & Products Containing Same*, Inv. No. 337-TA-435, Commission Opinion at 22-23, USITC Pub. 3547 (Oct. 2002); *Certain Hardware Logic Emulation Systems & Components Thereof*, Inv. No. 337-TA-383, Commission Opinion, 1998 WL 307240 (Mar. 1998) ("[T]he Commission's long-standing practice is to direct its remedial orders to all products covered by the patent claims as to which a violation has been found, rather than limiting its orders to only those specific models selected for the infringement analysis.")

C. Alleged Downstream Products

Qimonda's Position: Qimonda contends that it is entitled to a limited exclusion order on the LSI and Seagate downstream goods that incorporate the allegedly infringing LSI integrated circuits. (CIB at 267.) Citing *Certain Semiconductor Chips with Minimized Chip Package Size & Products Containing Same*, Inv. No. 337-TA-605, Initial Determination (Dec. 1, 2008), Qimonda argues that the *EPROMs* analysis is only applicable to downstream goods of non-respondents,[92] and that it is not necessary to engage in such analysis if the downstream goods are made by named respondents. (CIB at 267-268.)

Nevertheless, Qimonda argues that downstream products should be excluded under the *EPROMs*[93] analysis. Qimonda's analysis focuses on three categories of downstream products: LSI's { ,} and Seagate's { }

[92] The Federal Circuit in *Kyocera Wireless Corp. v. Int'l Trade Comm'n*, 545 F.3d 1340, 1356-1357 (Fed. Cir. 2008) held that a limited exclusion order cannot extend to third parties not named as respondents in an investigation.
[93] "*EPROMs*" refers to *Certain Erasable Programmable Read-Only Memories, Components Thereof, Products Containing Such Memories, & Processes for Making Such Memories*, Inv. No. 337-TA-276, Commission Opinion, 1989 ITC LEXIS 122 (May 1989)

Regarding the first *EPROMs* factor, Qimonda states that "[t]he role of the accused LSI ICs within { } is to provide the actual interface to the devices or networks, and thus their functionality is core to that of the downstream product." (CIB at 270-271 (citing JX-23C at 36; CDX-29C).) Qimonda cites to testimony from LSI's witness, Robert Andrews, to support its argument that the accused LSI ICs are critical components to the downstream { } (*Id.* at 271 (citing CX-1018C at 74:4-14, 119:15-17; CX-544C at Q. 107; CX-59C at 130:23-131:25; CDX-29C).) Qimonda asserts that without the LSI IC, a Seagate { } would not function. (*Id.* at 272 (citing CX-501C at 100:22-101:24; JX-23C at 37; CX-534C at 254:3-19, 257:1-4, CDX-29C; Tr. at 1773:10-13; CX-544C at Q. 110).) Qimonda thus claims that the LSI ICs are of value to the downstream products.

Turning to quantitative value, Qimonda claims that LSI ICs used in { } are approximately { } of the price of { } (CIB at 274 (citing CX-544C at Q. 99; JX-23C at ¶ 65).) Qimonda claims that LSI ICs used in { } are approximately { } of the price of { } (*Id.* at 275 (citing CX-544C at Q. 99; RX-1298 at Q. 147; JX-23C at ¶ 65).) Qimonda claims that the LSI ICs used in Seagate { } is, { } (*Id.* at276 (citing CX-544C at Q. 107).)

Regarding *EPROMs* factor 2, Qimonda claims that this factor is irrelevant in light of *Kyocera*. (CIB at 278.) If factor 2 is still relevant, Qimonda claims that it weighs in favor of an exclusion order including downstream goods, as both LSI and Seagate, named respondents in this investigation, are the manufacturers of the downstream goods. (CIB at 278-279 (citing CX-544C at Q. 114, 115; CX-2; CX-42).)

Regarding *EPROMs* factor 3, Qimonda claims that the vast majority of commercially available LSI ICs are imported in downstream products. (CIB at 281-286.) Qimonda further

claims that the LSI ICs have no commercial use other than incorporation into downstream products. (*Id.* at 280 (citing CX-59C at 90:5-25, 131:11-25; CX-534C at 266:17-267:4).) Thus, Qimonda claims that factor 3 favors exclusion of downstream products.

Regarding *EPROMs* factor 4, Qimonda argues that LSI will not lose sales of non-infringing products following the exclusion of downstream products containing the allegedly infringing ICs. (CIB at 286.) Qimonda claims that LSI has the capability to track and identify its products that do not infringe. (*Id.* at 287 (citing JX-23C at Ex. 17; CX-544C at Q. 138).) Accordingly, Qimonda states that LSI is will positioned to continue exporting products to the United States that contain non-infringing ICs. (*Id.* at 288 (citing CX-544C at Q. 138; Tr. at 1799:16-1800:5).) Qimonda asserts that Seagate failed to provide any evidence that it would be burdened with costs associated with segregating infringing and non-infringing inventory. (*Id.* at 289 (citing Tr. at 1790:2-22, 1791:3-11, 1794:6-1795:6; RX-1298C at Q. 192-193, 227, 238).) Qimonda points to testimony from Seagate witnesses who stated that an exclusion order on downstream goods would { } (*Id.* (citing CX-501C at 231:11-17; Tr. at 1791:21-1794:5; CX-498C at 87:14-20; CX-788C at SEA0006987).) Qimonda notes that for many products, Seagate has multiple suppliers for the same components. (*Id.* at 290-291.) For the products where Seagate {

} (*Id.* at 291 (citing CX-544C at Q. 146; CX-501C at 40:10-41:17).)

Regarding the fifth *EPROMs* factor, Qimonda asserts that there are alternative products for virtually every one of LSI's { } found to include infringing ICs. (CIB at 293 (citing CX-544C at Q. 153, 157; Tr. at 1801:21-1802:9; CDX-7C).) According to Qimonda, customers of LSI's infringing ICs have alternative suppliers. (*Id.* (citing CX-544C at

Q. 157; CDX-7C).) Qimonda further notes that many of {

} (*Id.* at 294 (citing CX-544C at Q. 162; CX-8C).)

With regard to Seagate, Qimonda claims that there would be no burden imposed on third parties as a result of the exclusion order. (*Id.*) Qimonda notes that Seagate's customers do not single-source from Seagate, meaning that they can purchase { } from other manufacturers. (CIB at 294 (citing CX-544 at Q. 164; CX-498C at 39:23-40:1).) Qimonda states that Seagate has many competitors in the { } market who can fill Seagate's place. (*Id.* at 295 (citing CX-501C at 45:10-46:2, 49:21-50:11; CX-544C at Q. 165; CX-498C at 17-21).) Qimonda claims that {

} (*Id.* (citing CX-544C at Q. 163; JX-23C at Ex. 19).) {

} (*Id.* (citing CX-544C at Q. 162; CX-8C).)

With regard to the sixth *EPROMs* factor, Qimonda claims that there several substitutes for LSI's { } (CIB at 296 (citing CX-544C at Q. 171; CDX-7C).) Qimonda asserts that LSI identified 12 competitors in its "Storage Systems segment." (*Id.* (citing CX-544C at Q. 171; CDX-7C; CX-945 at 9).) Qimonda alleges that Seagate has a number of significant competitors in the { } market. (*Id.* at 297 (citing CX-501C at 45:10-46:2, 49:3-19, 49:21-50:11, 120:18-121:7; CX-544C at Q. 165, 172; RX-1298C at Q. 200, 216; CX-947 at 5-6, 14).)

With regard to *EPROMs* factor 7, Qimonda argues that it is likely that the downstream { } contain the infringing LSI ICs. (CIB at 298 (citing CX-544C

at Q. 176, 177).) Qimonda reiterates that both LSI and Seagate {

} (*Id.* at 298-299 (citing CX-544C at Q. 138; Tr. at 1799:16-1800:5; CX-522 at Q. 147; CX-501C at 39:21-24, 41:3-42:3).)

Regarding *EPROMs* factor 8, Qimonda claims that an exclusion order extending only to infringing ICs would result in LSI shifting the importation of these stand-alone ICs to imports of downstream products containing the ICs. (CIB at 299-300 (citing CX-544C at Q. 180).) Qimonda argues that LSI would have the economic incentive to expand the imports of downstream products in the event that an exclusion order limited to ICs issues. (*Id.* at 300 (citing CX-544C at Q. 184).)

Regarding *EPROMs* factor 9, Qimonda reiterates that both LSI and Seagate have the { } (CIB at 300-301 (citing CX-544C at Q. 191-192; JX-23C at Exs. 17-18).) According to Qimonda, this means that LSI and Seagate {

} (*Id.*) In its reply brief, Qimonda reiterates its arguments regarding the *EPROMs* factors. (CRB at 135-142.)

Respondents' Position: Respondents contend that an analysis of the EPROMs factors demonstrates that the downstream { } should not be excluded. (RIB at 289.)

With regard to the first EPROMs factor, Respondents claim that the relative value of the accused LSI ICs is insubstantial in proportion to the value of the downstream goods. (RIB at 290 (citing RX-1298C at Q. 142-145, 151, 156).) For { } Respondents state that the LSI ICs account for { } of the value of the { } (*Id.* (citing RX-1298C at Q. 147; RDX-60C).) For { } Respondents state that the LSI ICs account for { } of the

total value of the { } (*Id.* (citing RX-1298C at Q. 147; RDX-60C).) For { } Respondents note that {

} (*Id.* at 291 (citing RX-1298C at Q. 151; RDX-60C; JX-23 at 232102-232103).)

With regard to the qualitative analysis, Respondents argue that the important components of the { } perform the core functionality of the product, which is { } (RIB at 291-292 (citing RX-1298C at Q. 135, 153; RX-1339).) Respondents argue that the incorporated LSI ICs do not provide this core functionality, but instead {

} (*Id.* at 292 (citing RX-1298C at Q. 153; RX-1339; RX-1340).) Respondents state that the role of the LSI ICs in the LSI downstream products depends greatly on the specific product under examination. (*Id.* (citing RX-1298C at Q. 149; RX-1340).) Respondents state that the ICs play a secondary role to other components in the { } (*Id.* (citing RX-1298C at Q. 149; RX-1340).)

With regard to the second EPROMs factor, Respondents claim that Qimonda knew of other downstream { } manufacturers that use LSI ICs, but only chose to include Seagate as a respondent. (RIB at 293 (citing RX-1298C at Q. 160; RDX-145C; JX-23C at 232170-3, Ex. 16; RX-1356; RX-1306C).) Respondents claim that a limited exclusion against Seagate will disadvantage it in the marketplace against these other { } manufacturers. (*Id.*) According to Respondents, "[t]hat the universe of potential downstream manufacturers is small and readily identifiable weighs against extending any limited exclusion order to encompass downstream { } products manufactured by Seagate." (*Id.*)

Regarding EPROMs factor 3, Respondents state that LSI imports a number of stand-alone ICs into the United States. The evidence shows that LSI imported approximately {

} into the U.S. from January 2006 to January 2009. (RIB at 294 (citing RX-1298C at Q. 172; RDX-146C; JX-23C at 232169).) Respondents note that these stand-alone ICs are very valuable to LSI and its customers, as these chips are used for testing, product development, and product qualification. (*Id.* (citing RX-1298C at Q. 174; Tr. at 1861:2-17, 1861:18-24).) Thus, Respondents claim that the exclusion of LSI ICs alone would afford great relief to Qimonda. (*Id.* at 295.) Respondents assert that if any downstream products are excluded, then the exclusion should be limited to { } as that would provide adequate relief to Qimonda. (*Id.* (citing RX-1298C at Q. 179; RDX-146C; JX-23 at 232169).) Finally, Respondents note that LSI's ICs and the DRAM products formerly produced by Qimonda do not compete. (*Id.* at 296 (citing Munn Deposition Tr. at 195:19-196:9; Tr. at 1010:11-14).)

With regard to the fourth EPROMs factor, Respondents argue that LSI's legitimate commerce will be affected if downstream products are excluded because Seagate may drop LSI as a supplier altogether - not just for products destined for the U.S., but for all { } worldwide. (RIB at 296-297 (citing RX-1298C at Q. 198-199; Tr. at 1853:11-14, 1853:19-23, 1854:11-18).) Respondents claim that there will negative effects on Seagate, as it will have to {

} (*Id.* at 297 (citing RX-1298C at Q. 193; JX-23C at Ex. 20; RX-1355 at 40, 43).) In addition, Respondents state that the process that Seagate would need to go through to qualify a new controller chip for its { } that use LSI ICs would be expensive and time-consuming. (*Id.* at 298 (citing RX-1298C at Q. 203; CX-501C at 121:4-11, 122:1-10).)

Regarding the fifth EPROMs factor, Respondents assert that U.S. customers of downstream products would be significantly burdened if downstream products are included in a

limited exclusion order. (RIB at 298 (citing RX-1298C at Q. 206-213; RDX-58C).) Respondents claim that LSI's market share is as high as { } (*Id.* (citing RX-1298C at Q. 217-218; RX-1524C at 21).) Respondents claim that a switch to an alternative { } would take at least 9-12 months and a switch to an alternative { } would be even more difficult. (*Id.* at 299 (citing RX-1298C at Q. 213, 219, Andrews Dep. Tr. at 126:24-127:3, 127:25-128:10).)

With regard to EPROMs factor 6, Respondents state that the availability of alternative products varies depending on the downstream product at issue. Respondents argue that the availability of alternatives to LSI's { } is limited. (RIB at 299 (citing RX-1298C at Q. 217).) Respondents claim that Seagate is the dominant supplier of { } for use in enterprise applications, with a { } in 2007. (*Id.* at 300 (citing RX-1298C at Q. 216; RX-1344 at 27).) According to Respondents, even if alternative suppliers could provide equivalent products, there would be time and cost associated with switching to a new supplier. (*Id.*)

With regard to EPROMs factor 7, Respondents state that LSI generally uses its own ICs in all of its { } however not all LSI { } imported into the U.S. contain accused ICs. (RIB at 300 (citing RX-1298C at Q. 222).) Respondents claim that {

} (*Id.* at 300-301 (citing RX-1298C at Q. 197, 226; RDX-157).) This would allegedly impose a burden on Customs and Seagate. (*Id.* at 301 (citing RX-1298C at Q. 226-227; RDX-157).)

Regarding the eighth EPROMs factor, Respondents state that their current practices

include final manufacture of the { } outside of the United States. (RIB at 301 (citing RX-1298C at Q. 230; Tr. at 1834:5-13; Andrews Dep. Tr. at 91:6-16; RX-1355 at 12).) Respondents state that "LSI and Seagate would not be able to evade the consequences of a limited exclusion order by altering their current practices." (*Id.*)

Regarding the ninth EPROMs factor, Respondents assert that it would be difficult to enforce a limited exclusion order against Seagate { } (*Id.* at 301-302.) Respondents again note that the type of IC used in the { } { } (RIB at 302 (citing RX-1355 at 12517-12519; RX-1298C at Q. 151, 226; RDX-60C; RDX-157).) Respondents dispute Qimonda's contention that Seagate { } (*Id.* (citing RX-1298C at Q. 196-197, 227).) Respondents acknowledge that the manufacturer of the chip may be determined by opening the { } and examining the actual chip, but this would be onerous and would likely destroy the { } (*Id.* (citing RX-1298C at Q. 235, 237).)

In their reply brief, Respondents assert that an EPROMs analysis should be performed to determine whether to include downstream products in a limited exclusion order. (RRB at 137.) Respondents claim that Qimonda's argument for not using the EPROMs analysis is incorrect and inconsistent with Qimonda's reliance on EPROMs through this investigation. (*Id.*) Respondents assert that any downstream relief is limited to the { } and HDDs produced by LSI and Seagate. (*Id.* at 138.)

Commission Investigative Staff's Position: Staff contends that in the event a violation is found, the appropriate remedy is a limited exclusion order that covers all of Respondents' accused products that are manufactured abroad by or on behalf of, or imported by or on behalf of, the Respondents, or any of their affiliated companies, parents, subsidiaries, or other related

business entities, or their successors or assigns. (SIB at 99.)

Discussion and Conclusion: In this Initial Determination, I have found no violation of Section 337. If, however, a violation of Section 337 is found by the Commission, I recommend that a limited exclusion order should cover all products from LSI and Seagate which contain a semiconductor integrated circuit found to infringe the asserted Qimonda patents. Specifically, I recommend that any exclusion order should apply to LSI, Seagate, and all of their affiliated companies, parents, subsidiaries, or other related business entities, or their successors or assigns, and should cover any products manufactured by or on behalf of LSI or Seagate which contain a semiconductor integrated circuit found to infringe the asserted Qimonda patents.

The Notice of Investigation makes clear that the investigation concerns "certain semiconductor integrated circuits or products containing same" that infringe one or more claims of the asserted patents. *See* 73 Fed. Reg. 79165 (Dec. 24, 2008). LSI and Seagate are the two named respondents. *Id.* Thus, the LSI and Seagate products containing the accused semiconductor integrated circuits are themselves accused in this investigation. *See Certain Semiconductor Chips with Minimized Chip Package Size & Products Containing Same*, Inv. No. 337-TA-605, Initial Determination (Dec. 1, 2008). Therefore, if the Commission does find a violation of Section 337, any limited exclusion order should reach LSI and Seagate products that contain the infringing semiconductor integrated circuits. *See* 19 U.S.C. § 1337(d)(1) ("If the Commission determines, as a result of an investigation under this section, that there is a violation of this section, it shall direct that the articles concerned, imported by any person violating the provision of this section, be excluded from entry into the United States[.]").

Assuming, *arguendo*, that notwithstanding the holding in *Kyocera*, it remains necessary to examine the *EPROMs* factors, I find that a balancing of the *EPROMs* factors support the inclusion of LSI's { } and Seagate's { } in a limited exclusion order.

In *Certain Erasable Programmable Read-Only Memories, Components Thereof, Products Containing Such Memories, & Processes for Making Such Memories*, Inv. No. 337-TA-276, Commission Opinion, 1989 ITC LEXIS 122 (May 1989), the Commission laid out a framework for analyzing whether or not to include downstream products in a limited exclusion order. The Commission explained that it "may, in issuing exclusion orders, whether general or limited, balance the complainant's interest in obtaining complete protection from all infringing imports by means of exclusion of downstream products against the inherent potential of even a limited exclusion order, when extended to downstream products, to disrupt legitimate trade in products which were not themselves the subject of a finding of violation of section 337." *Id.* The Commission provided a number of factors to analyze when balancing the competing interests. Those factors are:

1. the value of the infringing articles compared to the value of the downstream products in which they are incorporated,

2. the identity of the manufacturer of the downstream products (i.e., are the downstream products manufactured by the party found to have committed the unfair act, or by third parties),

3. the incremental value to complainant of the exclusion of downstream products,

4. the incremental detriment to respondents of such exclusion,

5. the burdens imposed on third parties resulting from exclusion of downstream products,

6. the availability of alternative downstream products which do not contain the infringing articles,

7. the likelihood that imported downstream products actually contain the infringing articles and are thereby subject to exclusion,

8. the opportunity for evasion of an exclusion order which does not include downstream products, and

9. the enforceability of an order by Customs.

Id. The Commission noted that this list of factors is not exclusive. *Id.*

EPROMS FACTOR 1

The first factor focuses on the value of the accused LSI ICs compared to the value of the products in which the ICs are incorporated. I find that this factor supports inclusion of LSI's { } and Seagate's { } in a limited exclusion order. First, I address the LSI { } Regarding the quantitative analysis, the accused LSI ICs account for between { } of the price of the { } (CX-544C at Q. 99; RX-1298C at Q. 147.) Regarding the qualitative analysis, the testimony from Robert Andrews of LSI demonstrates the importance of the LSI ICs in the { } (CX-544C at Q. 107 (pg. 17-18); CX-1018C.) Ms. Mulhern does not dispute this. She testified that in the { } the accused LSI IC "provided the majority of the functionality." (RX-1298C at Q. 149.) For the { } she only states other components also play important roles, but she never denies the assertion that the accused ICs play an important role. (*Id.*)

Next, I turn to the Seagate { } The price of the LSI ICs { } (CX-544C at. Q. 107 (pg. 19-20); RX-1298C at Q. 151.) Both experts agree that the accused LSI controller ICs perform the function of interfacing between the Seagate { } and an external device. (CX-544C at Q. 110 (pg. 20); RX-1298C at Q. 153.) The experts disagree regarding the qualitative value of this function. I find that this function is qualitatively valuable. While the controller IC may not perform { } the LSI controller IC provides crucial functioning which is of the utmost

importance for a working { } (CX-544C at Q. 110 (pg. 20); CX-501C at 100:22-101:14.)

EPROMS FACTOR 2

The second EPROMs factor focuses on the identity of the manufacturer of the downstream products, i.e., whether it can be determined that the downstream products are manufactured by the respondent or by a third party. I find that this factor is no longer relevant in light of the Federal Circuit's decision in *Kyocera Wireless Corp. v. Int'l Trade Comm'n*, 545 F.3d 1340 (Fed. Cir. 2008).

If this factor is still relevant to the analysis, I find that it favors the relief sought by Qimonda. Qimonda seeks an exclusion order only against products manufactured by and on behalf of LSI and Seagate.

EPROMS FACTOR 3

The third factor looks at the incremental value to complainant of the exclusion of downstream products. I find that this factor supports inclusion of LSI's { } and Seagate's { } in a limited exclusion order. Both experts agree that a majority of LSI's accused ICs are not imported directly into the United States. (CX-544C at Q. 124; RX-1298C at Q. 174.) Because only a small fraction of LSI's accused ICs enter the United States as stand-alone products, there is great incremental value to Qimonda in including the { } and { } in the exclusion order. Otherwise, the relief would be relatively weak, as the majority of LSI ICs that enter the country are already integrated into another device.

Ms. Mulhern opines that while the number of stand-alone LSI ICs that are imported into the U.S. is small, the value of these ICs is large because they are used for testing and qualification purposes. (RX-1298C at Q. 174.) Ms. Mulhern's opinion is unsupported by any

evidence,[94] and I decline to find that Respondents have demonstrated that these imported ICs have extraordinary value due to their purported use in the United States. (*Id.* at Q. 174-176.)

EPROMS FACTOR 4

This factor considers the extent to which Respondents' legitimate commerce would be affected by the entry of an exclusion order which extended to products containing the accused LSI ICs. I find that this factor favors the Respondents.

Respondents state that if an exclusion order is entered that covers the Seagate { } it is likely that Seagate will drop LSI as an IC supplier. (RX-1298C at Q. 199-203.) In light of the fact that there are other IC suppliers available to Seagate, Seagate would be able to stop purchasing ICs from LSI altogether to avoid infringement issues. (CX-544C at Q. 148; RX-1298C at Q. 199.) If Seagate needed to replace the LSI ICs with ICs from other suppliers, this would be a time-consuming process. (RX-1298C at Q. 203.) This would have a negative effect on the legitimate commerce of LSI and Seagate because Seagate {

} (*Id.* at Q. 194-195, 201-202.)

EPROMS FACTOR 5

This factor focuses on the burdens imposed on third parties resulting from exclusion of downstream products. I find that this factor favors Qimonda. With regard to Seagate, Ms. Mulhern conceded that EPROMs factor 5 weighs in favor of including Seagate's {HDDs} in a limited exclusion order. (Tr. at 1800:11-1801:2; RX-1298C at Q. 220.)

With regard to LSI, the parties both acknowledge that there are companies that make competing { } even though LSI holds a large market share. (CX-544C at Q. 157; Tr. at 1802:10-1803:16; RX-1298C at Q. 218.) The parties dispute the extent of the

[94] Ms. Mulhern cites to RX-1306C as support. RX-1306C appears to be a large spreadsheet document. Ms. Mulhern fails to explain how this exhibit supports her opinion, and it is not clear from the document itself.

burden that third party computer companies would face if they were required to purchase { } from companies other than LSI. (CX-544C at Q. 157-162; RX-1298C at Q. 219.) I find that the fact that companies other than LSI manufacture { } demonstrates that factor 5 supports Qimonda's position. While I understand there will be some burden to third party computer companies in switching from LSI's products to a competitor's products, I find that this burden is not significant enough to warrant this factor favoring exclusion of the LSI { } from a limited exclusion order.

EPROMS FACTOR 6

This factor focuses on the availability of alternative downstream products that do not contain the infringing articles. Due to the fact that LSI has multiple competitors for { } and Seagate has multiple competitors for { } I find that this factor favors Qimonda. (CX-544C at Q. 171-172.) Ms. Mulhern concedes that this factor supports exclusion of Seagate { } (RX-1298C at Q. 220.) While Ms. Mulhern states that LSI has a significant market share for { } there is no evidence that other competing manufacturers could not increase their market share should LSI be precluded from importing certain { } (*Id.* at Q. 218.) Further, while it make take some time for a customer to switch from an LSI or Seagate product to a product made by a different manufacturer, I find that this is not a relevant consideration with regard to the sixth factor. (*Id.* at Q. 219.)

EPROMS FACTOR 7

This factor focuses on the likelihood that the downstream products actually contain the infringing articles. The Commission has explained that "[t]he central issue with respect to Factor 7 is the effect of a downstream exclusion order on products entered under the same HTS number

that do not contain infringing chips." *Certain Baseband Processor Chips & Chipsets, Transmitter & Receiver (Radio) Chips, Power Control Chips, & Products Containing Same, Including Cellular Telephone Handsets*, Inv. No. 337-TA-543, Commission Opinion at 104 (June 19, 2007) ("*Baseband Processors*"). I find that this factor favors Qimonda. LSI uses its own accused ICs in its { } meaning that it is very likely that there would be any confusion regarding whether or not the downstream { } include the accused ICs. (RX-1298C at Q. 222.)

Regarding Seagate, {

} *See Baseband Processors* at 105 (explaining that a certification requirement in an exclusion order substantially lessens the possibility that non-infringing commerce would be impacted). While Ms. Mulhern testified that {

} she cites no evidence to support this, and instead relies on undocumented conversations that she had with Mr. Moe. (RX-1298C at Q. 196-198, 220.) I decline to rely on such conversations.

EPROMS FACTOR 8

This factor focuses on the opportunity for evasion of an exclusion order that does not include downstream products. In *Baseband Processors*, the Commission provided the following explanation regarding Factor 8:

> Where an infringing article was imported in a stand-alone form prior to an investigation, and a Commission order excludes only the infringing article itself, then the subsequent incorporation of such article into a downstream product prior to importation would constitute an evasive act for purposes of our *EPROMs* analysis. If instead, however, there is a pre-existing practice whereby virtually all infringing articles are incorporated into downstream products prior to importation,

> then the continuation of that practice would not constitute evasion for purposes of *EPROMs* Factor 8.

Baseband Processors at 108. In that investigation, the Commission found that Factor 8 was inapplicable because virtually all infringing chips were imported only after being incorporated into downstream products. *Id.*

Dr. Button and Ms. Mulhern agree that only a very small amount of accused LSI ICs are imported into the U.S. in a stand-alone form, as opposed to being imported as part of a downstream product. (CX-544C at Q. 123-124; RX-1298C at Q. 174.) Thus, consistent with the Commission's view in *Baseband Processors*, I find that Factor 8 is inapplicable.

EPROMS FACTOR 9

This factor focuses on the enforceability of an exclusion order by Customs. The Commission has explained that "[g]enerally, this assessment has not been determinative in our decision on whether to issue a downstream exclusion order but it has been used to more narrowly tailor the Commission's remedy to assist Customs in enforcement of any remedial order issued." *Baseband Processors* at 108.

I find that this factor supports Qimonda. A limited exclusion order would only extend to LSI and Seagate. The { } include the accused LSI ICs. (RX-1298C at Q. 222.) { } (CX-501C at 40:10-43:22.) Furthermore, the inclusion of a certification provision in the exclusion order will reduce the burden on Customs. *Baseband Processors* at 115.

D. Cease & Desist Order

Qimonda's Position: Qimonda contends that the Commission should issue a cease and desist order against LSI's inventory of integrated circuits and downstream goods in the United

States and Seagate's inventory of downstream goods in the United States. (CIB at 310.)

Qimonda asserts that both LSI and Seagate maintain commercially significant inventories of infringing articles in the United States. According to Qimonda, LSI maintains inventory in warehouses in the Unites States. (CIB at 310 (citing CX-499C at 21:5-16; CX-500C at 53:24-54:9).) Qimonda claims that LSI maintains distribution centers in the United States from which it delivers products to its customers. (*Id.* (citing CX-500C at 36:14-19).) Qimonda states that LSI has a database that can identify what inventory is held at each of its warehouses in the United States. (*Id.* (citing CX-500C at 142:3-6).) Qimonda avers that LSI's inventory of infringing products and downstream goods in the United States is commercially significant. (*Id.* at 310-311 (citing CX-618).)

Qimonda asserts that Seagate {

} (CIB at 311 (citing CX-497 at 127:17-25, Ex. 14; CX-501C at 87:21-90:11, Ex. 11).) Qimonda states that Seagate {

} (*Id.* (citing CX-498C at 54:1-17).) Qimonda states that Seagate also {

} (*Id.* (citing CX-498C at 53:2-6).) According to Qimonda, Seagate {

} (*Id.* (citing CX-498C at 53:7-12, 53:18-25).)

Respondents' Position: Respondents contend that a cease and desist order is not warranted. (RIB at 304.) Respondents argue that Qimonda has not and cannot meet its burden of showing that a cease and desist order should be entered in this investigation. (*Id.* at 305.) According to Respondents, there is no evidence that either LSI or Seagate maintains a

commercially significant amount of infringing product in the United States. (*Id.*) Respondents assert that even if LSI and Seagate maintain some minimal amounts of product in the United States, the amounts are simply insufficient to support a cease and desist order. (*Id.* (citing *Certain Zero-Mercury-Added Alkaline Batteries*, Inv. No. 337-TA-493, 2004 WL 1875414, Initial Det. at 294-95 (June 2, 2004)).) In their reply brief, Respondents reiterate that Qimonda has failed to introduce evidence demonstrating that LSI and Seagate maintain commercially significant levels of the accused products in the United States. (RRB at 141.)

Commission Investigative Staff's Position: Staff supports the issuance of a cease and desist order in the event that a violation of Section 337 is found. (SIB at 107.) Staff states that the evidence shows that Respondents maintain commercially significant levels of inventory in the United States sufficient to justify the issuance of a cease and desist order. (*Id.* (citing CX-618; CX-500C at 171; CX787C; CX-498C at 52).)

Discussion and Conclusion: In this Initial Determination, I have found no violation of Section 337. If, however, a violation of Section 337 is found by the Commission, I recommend that the Commission issue a cease and desist order directed to the infringing semiconductor integrated circuits and products containing same held in the United States by the Respondents. Specifically, it is recommended that the Commission issue a cease and desist order prohibiting Respondents and any of their principals, stockholders, officers, directors, employees, agents, licensees, distributors, controlled (whether by stock ownership or otherwise) and/or majority owned business entities, successors, and assigns, and to each of them from selling, distributing, advertising, promoting, marketing, storing, exhibiting, demonstrating, or testing the infringing products in the United States.

Section 337 provides that in addition to, or in lieu of, the issuance of an exclusion order, the Commission may issue a cease and desist order as a remedy for violation of section 337. *See* 19 U.S.C. § 1337(f)(1). The Commission generally issues a cease and desist order directed to a domestic respondent when there is a "commercially significant" amount of infringing, imported product in the United States that could be sold so as to undercut the remedy provided by an exclusion order. *See Certain Crystalline Cefadroxil Monohydrate*, Inv. No. 337-TA-293, USITC Pub. 2391, Comm'n Op. on Remedy, the Public Interest and Bonding at 37-42 (June 1991); *Certain Condensers, Parts Thereof and Products Containing Same, Including Air Conditioners for Automobiles*, Inv. No. 337-TA-334, Comm'n Op. at 26-28 (Aug. 27, 1997). The complainant bears the burden of proving that a respondent has a commercially significant inventory in the United States. *Certain Integrated Repeaters, Switches, Transceivers & Products Containing Same*, Inv. No. 337-TA-435, Comm'n Op., 2002 WL 31359028 (Aug. 16, 2002).

I find that Qimonda has met its burden in demonstrating that LSI has a commercially significant inventory of allegedly infringing products in the United States. LSI maintains inventory in the United States in various warehouses and distribution centers. (CX-499C at 21:5-5-16; CX-500C at 36:12-17, 53:24-54:9, 142:3-8.) I find that such inventory is "commercially significant," as demonstrated by an inventory spreadsheet produced by LSI during discovery. (CX-500C at 170:20-171:23, Ex. 22.) Thus, I recommend that any remedy issued by the Commission include a cease and desist order against LSI.

I find that Qimonda has met its burden in demonstrating that Seagate has a commercially significant inventory of allegedly infringing products in the United States. {

} I find that such inventory is "commercially significant." (CX-497C at 123:14-133:20, Ex. 2, Ex. 14; CX-498C at 52:16-

54:17.) Thus, I recommend that any remedy issued by the Commission include a cease and desist order against Seagate.

E. Bonding

Qimonda's Position: Qimonda requests that the Commission require Respondents to post a bond at 100 percent of the entered value of the infringing articles in order to enter their products and downstream goods into the United States during the presidential review period. (CIB at 311.)

Qimonda asserts that the Commission typically sets bonds at 100 percent of the entered value where the prices of the infringing articles are highly variable. (CIB at 311-312 (citing *Certain Unified Communications Systems*, Inv. No. 337-TA-598, Initial Determination, 2008 WL 683369 (Jan. 28, 2008); *Certain Neodymium-Iron-Boron Magnets*, Inv. No. 337-TA-372, Commission Opinion, 1996 WL 1056324 (Apr. 30, 1996)).) Qimonda states that the prices of the infringing articles in this investigation are highly variable. (*Id.* (citing CX-544 at15-20, 24, 50-53).) As an example, Qimonda notes that the prices of LSI integrated circuits range from { }and the prices of LSI downstream goods range from { }. (*Id.* (citing CX-544 at15-20, 24, 50-53).) Qimonda further notes that the prices of Seagate products { } (*Id.* (citing CX-928 at 47; CX-544 at15-20, 24, 50-53).)

In its reply brief, Qimonda contends that where prices of the infringing articles are highly variable, the Commission typically sets bond at 100 percent of the entered value because "it is impossible for the Commission to calculate what level of bond based on price differentials would protect a complainant from any injury." (CRB at 144 (citing *Certain Integrated Repeaters*, Inv. No. 337-TA-435, 2002 WL 31359028 (Aug. 16,2002).) Qimonda asserts that the prices of the

infringing articles are highly variable, and thus a 100 percent bond is warranted. (*Id.* (citing CIB at 312).)

Respondents' Position: Respondents contend that in the event a violation of Section 337 is found, no bond should be required. (RIB at 305.) Respondents claim that no bond is required because there can be no injury to Qimonda - having declared bankruptcy and having no manufacturing activities, there is no Qimonda domestic industry that could be injured by any patent infringement. (*Id.* at 305-306 (citing JX-23C at 7, 20; RX-1248 at 4, 9; RX-1282C; RX-1321C; Tr. at 717:2-6; RX-1322C); RX-1298C at Q. 31; RX-1253C at 95).)

Respondents claim that to the extent that the Commission disagrees, the bond should still be set at zero. Respondents assert that there are no competitive products as between Respondents and Qimonda on which to base a price differential. (RIB at 306 (citing Tr. at 772:3-12, 1010:11-14; Deposition Stipulations, Munn at Tab 10, 195:19-196:9).) Respondents further assert that {

} (*Id.* (citing RX-1298C at Q. 88, 90-94; Deposition Stipulations, Munn at Tab 10, 169:11-170:16, 171:5-14, 171:20-172:6, 175:7-11, 175:14-22, 178:7-17; Tr. at 987:7-12).)

Respondents argue that the record contains no information that could serve as a basis for determining an appropriate bond. (*Id.* at 307.) Respondents argue that Qimonda should not be permitted to benefit from its own failure to provide evidence, and thus no bond should be required. (RIB at 306.)

Finally, Respondents argue that because the level of a bond should only be sufficient to "offset any competitive advantage resulting from the unfair method of competition or unfair act enjoyed by persons benefiting by the importation," a bond is not appropriate in this Investigation. (RIB at 306 (citing *Certain Dynamic Random Access Memories, Components Thereof and*

Products Containing Same, Inv. No. 337-TA-242, USITC Pub. 2034, 1987 ITC LEXIS 170, Comm'n Op. at *133 (Nov. 1987); *Certain Rubber Antidegradants*, Inv. No. 337-TA-533, 2006 ITC LEXIS 212, at *206, Initial Det. (Feb. 17, 2006)).) Respondent assert that the record is devoid of evidence that any bond amount would offset any competitive advantage that may have resulted from the allegedly unfair acts allegedly undertaken by the Respondents. (*Id.* (citing Tr. at 772:3-12, 1010:11-14; Deposition Stipulations, Munn at Tab 10, 195:19-196:9).) Respondents reiterate their arguments in their reply brief. (RRB at 141-142.)

Commission Investigative Staff's Position: Staff contends that if a violation of Section 337 is found, no bond should be set during the Presidential review period. (SIB at 109.) Staff believes that there was insufficient evidence adduced at the hearing demonstrating variable prices of the accused products in comparison to the domestic industry products. (*Id.*) Specifically, Staff asserts that Qimonda has not offered any proof of pricing regarding its own domestic products in comparison to the accused products. (*Id.*)

Discussion and Conclusion: In this Initial Determination, I have found no violation of Section 337. If, however, a violation of Section 337 is found by the Commission, I recommend no bond during the Presidential review period.

The administrative law judge and the Commission must determine the amount of bond to be required of a respondent, pursuant to section 337(j)(3), during the 60-day Presidential review period following the issuance of permanent relief, in the event that the Commission determines to order a remedy. The purpose of the bond is to protect the complainant from any injury. 19 CFR §§ 210.42(a)(1)(ii), 210.50(a)(3).

When reliable price information is available, the Commission has often set the bond by eliminating the differential between the domestic product and the imported, infringing product.

See Certain Microsphere Adhesives, Processes for Making Same, and Products Containing Same, Including Self-Stick Repositionable Notes, Inv. No. 337-TA-366, Comm'n Op. a 24 (1995). In other cases, the Commission has turned to alternative approaches, especially when the level of a reasonable royalty rate could be ascertained. *See, e.g., Certain Integrated Circuit Telecommunication Chips and Products Containing Same, Including Dialing Apparatus*, Inv. No. 337-TA-337, Comm'n Op. at 41 (1995).

The evidence demonstrates that due to its bankruptcy, {

} (RX-1298C at Q. 41, 52; CX-989C at Q. 87, 92; Tr. at 708:25-709:5, 821:19-822:1.) Even when Qimonda was manufacturing and selling products in the U.S., Qimonda's products did not compete with Respondents' products. (Tr. at 772:3-12, 1010:11-14.) Thus, a bond would not protect Qimonda from competitive injury. I recommend no bonding during the Presidential review period.

F. Reporting Requirement

Respondents' Position: Respondents state that if the Commission finds that remedial relief is appropriate in this investigation, any remedy should be accompanied by a quarterly reporting requirement, obligating Qimonda to demonstrate the sufficiency and ongoing nature of its domestic industry. (RIB at 284.) Respondents cite *Certain Variable Speed Wind Turbines and Components Thereof*, Inv. No. 337-TA-376, USITC Pub. No. 3003, 1996 ITC LEXIS 556, Comm'n Op. at 22-26 (Nov. 1996) as support for requiring a reporting requirement after the complainant filed for bankruptcy and its domestic activities were in question. (*Id.*)

Respondents note that in *Variable Speed Wind Turbines*, the Commission imposed a quarterly reporting requirement to monitor the complainant's continuing domestic activities related to the patent-in-suit. (RIB at 284-285.) Respondent state that Commission precedent

holds that the cessation of domestic activities related to the patents-in-suit renders the continuation of any remedy inappropriate. (*Id.* at 285 (citing *Certain Variable Speed Wind Turbines and Components Thereof*, Inv. No. 337-TA-376, USITC Pub. No. 3003, 1996 ITC LEXIS 556, Comm'n Op. at 22-26 (Nov. 1996); *Certain Neodymium-Iron-Boron Magnets, Magnet Alloys, and Articles Containing Same*, Inv. No. 337-TA-372, 1997 ITC LEXIS 422, Comm'n Op. at 73 (Oct. 28, 1997)).)

Respondents argue that the complete {

} (RIB at 285.)

Respondents claim that the facts in the present situation are stronger than the facts in *Variable Speed Wind Turbines*, where a reporting requirement was imposed. (*Id.*) Respondents reiterate their argument in their reply brief. (RRB at 142.)

Qimonda's Position: Qimonda opposes Respondents' request for a reporting requirement. (CIB at 313.) Qimonda states that in other investigations where the Commission based its domestic industry finding on past domestic activities in light of stoppage of domestic operations, the Commission has not instituted a reporting requirement. (*Id.* (citing *Certain Video Graphics Display Controllers and Prods. Containing Same*, Inv. No. 337-TA-412, Initial Determination (May 14, 1999); *Certain Battery-Powered Ride-On Toy Vehicles and Components Thereof*, Inv. No. 337-TA-314, Comm'n Op., U.S.I.T.C. Publ. No. 2420 (April 9, 1991)).)

Qimonda argues that the facts are distinguishable from *Certain Variable Speed Wind Turbines*, Inv. No. 337-TA-376, Comm'n Op. (Sept. 23, 1996), cited by Respondents. Qimonda

asserts that it continues to engage domestic activities and continues to maintain inventory. (CIB at 314-315 (citing CX-72; CX-281C at Q. 71-76; CX-190C at Q. 120-138).) Qimonda further states that it has licensed the patents-in-suit, and its licensees exploit the patented technology. (*Id.* at 315 (citing CX-72; CX-281C at Q. 71-76; CX-190C at Q. 120-138).) Qimonda argues that it has already demonstrated that its domestic operations are equivalent, if not greater, than those held by the Commission in *Wind Turbines* to be sufficient to satisfy a reporting requirement and justify an exclusion order. (*Id.*)

Qimonda cites to *Neodymium-Iron-Boron Magnets, Magnet Alloys, and Articles Containing Same*, Inv. No. 337-TA-372, Commission Determination, Enforcement Proceeding, 1997 WL 857227 (Nov. 1997) ("*Magnets*") and states that the Commission denied respondents' request for a reporting requirement where there was some uncertainty as to whether the complainant would continue to engage in domestic activities related to the patents-in-suit. (CIB at 315.) Qimonda argues that as was the case in *Magnets*, Respondents have failed to prove that Qimonda will discontinue domestic activities related to the patents-at-issue. (*Id.*)

Qimonda claims that a reporting requirement is a rarity that requires special circumstances. (CIB at 315 (citing *Magnets*).) Qimonda asserts that a reporting requirement is burdensome on the Commission and the parties, and prevents the investigation from coming to a definitive end. (*Id.* at 315-316 (citing *Magnets*; *Certain Hardware Logic Emulation Systems and Components Thereof*, Inv. No. 337-TA-383, Advisory Op. 2000 WL 1468389 (Aug. 7, 2000)).) Qimonda reiterates its arguments in its reply brief. (CRB at 145-147.)

Commission Investigative Staff's Position: Staff concurs with Respondents that any remedy should include an ongoing reporting requirement. (SIB at 100.) Staff also cites to the Variable Speed Wind Turbines opinion as support for its position. (*Id.* at 100-101.) Staff notes

that Qimonda AG has filed for bankruptcy in Germany, and its subsidiaries have filed for bankruptcy in the United States. (*Id.* at 101.) Staff states that there is strong evidence that

{

.} (*Id.*

(citing Tr. at 870:14-18, 876:2-14).)

Discussion and Conclusion: Based on the evidence before me, I recommend that any remedy issued by the Commission include a quarterly reporting requirement to ensure that Qimonda still meets the domestic industry requirement of 19 U.S.C. § 1337.

The parties focus heavily on the Commission's decision in *Certain Variable Speed Wind Turbines and Components Thereof*, Inv. No. 337-TA-376, USITC Pub. No. 3003, 1996 ITC LEXIS 556, Comm'n Op. at 22-26 (Nov. 1996) ("*Wind Turbines*"). There, the ALJ did not have notice of the complainant's bankruptcy filing before issuing his Initial Determination. The Commission considered the bankruptcy filing in connection with the economic prong, and affirmed the ALJ's finding that the economic prong was satisfied. The limited exclusion order issued by the Commission included a reporting requirement:

> [W]e have issued a limited exclusion order containing a quarterly reporting requirement to monitor complainant's practice of claim 131 of the '039 patent. If it becomes clear from its reports that complainant has suspended or ceased practice of claim 131, the Commission will consider whether to suspend or revoke the exclusion order, as may be appropriate.

Wind Turbines, 1996 ITC LEXIS 556, at *39.

In contrast, the Commission did not impose a reporting requirement in *Certain Neodymium-Iron-Boron Magnets, Magnet Alloys, and Articles Containing Same*, Inv. No. 337-TA-372, 1997 ITC LEXIS 422, Comm'n Op. at 73 (Oct. 28, 1997). There, the respondents

argued that a reporting requirement was appropriate because the complainant had just sold its assets, including the patent-in-suit, to a Canadian company. The respondents claimed that there was a chance that all U.S. operations would be shut down. The respondents further argued that recent statements had been made by employees of the complainant that implied that complainant was no longer manufacturing magnets that contained oxygen in the patented range.

The Commission rejected these arguments and declined to impose a reporting requirement:

> We do not believe that such reporting is warranted in this case. We adopted the finding in the ALJ's final ID that Crucible satisfied the domestic industry requirement inasmuch as "a very substantial number" of Crucible's magnets contained oxygen in the patented range. We agree with Crucible and the IA that respondents have not put forth evidence that would indicate that these same domestic facilities no longer satisfy that requirement. Indeed, YBM has stated that it "will continue to manufacture and sell in the United States" magnets covered by the '439 patent. In this respect, this case is unlike the unique circumstances involved in *Caulking Guns, EDM,* or *Wind Turbines,* and respondents have not, in our view, provided a reasonable basis for us to impose the requested reporting requirement on the domestic industry at this time.

Magnets, 1997 ITC LEXIS 422 at *107-108.

Based on the status of Qimonda's U.S. operations and its bankruptcy proceedings (as described *supra* in connection with the economic prong analysis), I recommend the imposition of a quarterly reporting requirement as part of any remedy issued by the Commission. This reporting requirement will ensure that a domestic industry continues to exist in the future. *Magnets*, 1997 ITC LEXIS 422, at *106 (explaining that "in the event [the patent owner was] to cease domestic activities related to articles protected by the [patent-in-suit], the continued existence of Commission remedial orders would no longer be appropriate or necessary to serve the purposes of the statute.")

IX. MATTERS NOT DISCUSSED

This Initial Determination's failure to discuss any matter raised by the parties, or any portion of the record, does not indicate that it has not been considered. Rather, any such matter(s) or portion(s) of the record has/have been determined to be irrelevant, immaterial or meritless. Arguments made on brief which were otherwise unsupported by record evidence or legal precedent have been accorded no weight.

X. CONCLUSIONS OF LAW

1. The Commission has subject matter jurisdiction, *in rem* jurisdiction, and *in personam* jurisdiction.

2. Qimonda has standing to assert the patents-in-suit against Respondents.

3. There has been an importation of the accused semiconductor integrated circuits and products containing same which are the subject of the alleged unfair trade allegations.

4. An industry does not exist in the United States that exploits U.S. Pat. No. 5,213,670, as required by 19 U.S.C. § 1337(a)(2).

5. An industry does not exist in the United States that exploits U.S. Pat. No. 5,646,434, as required by 19 U.S.C. § 1337(a)(2).

6. An industry does not exist in the United States that exploits U.S. Pat. No. 5,851,899, as required by 19 U.S.C. § 1337(a)(2).

7. An industry does not exist in the United States that exploits U.S. Pat. No. 6,495,918, as required by 19 U.S.C. § 1337(a)(2).

8. U.S. Patent No. 5,213,670 is valid and enforceable.

9. Claims 1, 2, 3, and 5 of U.S. Patent No. 5,646,434 are invalid under 35 U.S.C. § 102.

10. If claims 2 and 3 of U.S. Patent No. 5,646,434 are not found to be invalid under 35 U.S.C. § 102, claims 2 and 3 of U.S. Patent No. 5,646,434 are invalid under 35 U.S.C. § 103.

11. U.S. Patent No. 5,851,899 is valid and enforceable.

12. Claims 1, 2, 4, 7, and 11 of U.S. Patent No. 6,495,918 are invalid under 35 U.S.C. § 102.

13. None of the accused products literally infringe U.S. Pat. No. 5,213,670.

14. None of the accused products literally infringe U.S. Pat. No. 5,646,434.

15. None of the accused products literally infringe U.S. Pat. No. 5,851,899.

16. All LSI semiconductor integrated circuits manufactured pursuant to the { } and products containing same literally infringe claims 1, 2, 7, and 11 of U.S. Patent No. 6,495,918.

17. The { } products are not licensed under any asserted Qimonda patents.

18. There is no violation of 19 U.S.C. § 1337(a)(1).

XI. ORDER

Based on the foregoing, and the record as a whole, it is my Final Initial Determination that there is no violation of 19 U.S.C. § 1337(a)(1) in the importation into the United States, sale for importation, and the sale within the United States after importation of certain semiconductor integrated circuits and products containing same

I hereby **CERTIFY** to the Commission my Final Initial and Recommended Determinations together with the record consisting of the exhibits admitted into evidence. The pleadings of the parties filed with the Secretary, and the transcript of the pre-hearing conference and the hearing, as well as other exhibits, are not certified, since they are already in the

Commission's possession in accordance with Commission rules.

It is further **ORDERED** that:

In accordance with Commission Rule 210.39, all material heretofore marked *in camera* because of business, financial and marketing data found by the administrative law judge to be cognizable as confidential business information under Commission Rule 201.6(a), is to be given *in camera* treatment continuing after the date this investigation is terminated.

The initial determination portion of the Final Initial and Recommended Determination, issued pursuant to Commission Rule 210.42(a)(1)(i), shall become the determination of the Commission sixty (60) days after the service thereof, unless the Commission, within that period, shall have ordered its review of certain issues therein, or by order, has changed the effective date of the initial determination portion. If the Commission determines that there is a violation of 19 U.S.C. § 1337(a)(1), the recommended determination portion, issued pursuant to Commission Rule 210.42(a)(1)(ii), will be considered by the Commission in reaching a determination on remedy and bonding pursuant to Commission Rule 210.50(a).

Within fourteen days of the date of this document, each party shall submit to the office of the Administrative Law Judge a statement as to whether or not it seeks to have any portion of this document deleted from the public version. The parties' submissions must be made by hard copy by the aforementioned date and must include a copy of this document with red brackets indicating any portion asserted to contain confidential business information to be deleted from

the public version. The parties' submission concerning the public version of this document need not be filed with the Commission Secretary.

SO ORDERED.

Issued: October 14, 2009
DATE

Robert K. Rogers, Jr.
Administrative Law Judge

IN THE MATTER OF CERTAIN SEMICONDUCTOR INTERGRATED CIRCUITS AND PRODUCTS CONTAINING SAME

Inv. No. 337-TA-665

PUBLIC CERTIFICATE OF SERVICE

I, Marilyn R. Abbott, hereby certify that the attached **ORDER** was served upon **Stephen R. Smith, Esq.**, and **Vu Q. Bui, Esq.,** Commission Investigative Attorneys, and the following parties via first class mail and air mail where necessary on FEB 25 2010

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IN THE MATTER OF CERTAIN SEMICONDUCTOR INTERGRATED CIRCUITS AND PRODUCTS CONTAINING SAME

Inv. No. 337-TA-665

PUBLIC CERTIFICATE OF SERVICE - PAGE 2

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