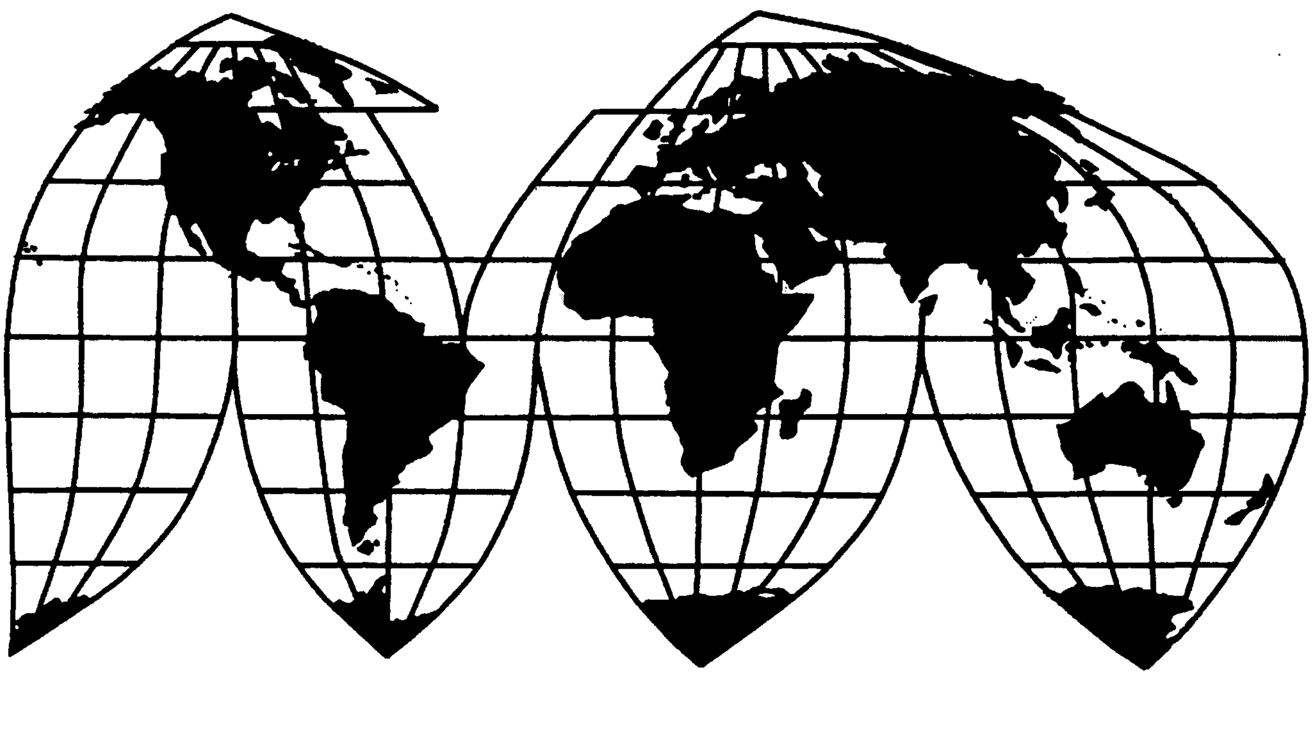
In the Matter of

Certain CD-ROM Controllers and Products Containing the Same-II

Investigation No. 337-TA-409

Publication 3251 **October 1999**

U.S. International Trade Commission



Washington, DC 20436

U.S. International Trade Commission

Address all communications to
Secretary to the Commission
United States International Trade Commission
Washington, DC 20436

U.S. International Trade Commission

Washington, DC 20436

In the Matter of

Certain CD-ROM Controllers and Products Containing the Same-II

Publication 3251

October 1999

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C. 20436

In the Matter of CERTAIN CD-ROM CONTROLLERS AND PRODUCTS CONTAINING THE SAME - II	Inv. No. 337-TA-409

NOTICE OF FINAL DETERMINATION

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has found no violation of section 337 of the Tariff Act of 1930 in the above-captioned investigation.

FOR FURTHER INFORMATION CONTACT: Timothy P. Monaghan, Esq., Office of the General Counsel, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone 202-205-3152. General information concerning the Commission may also be obtained by accessing its Internet server (*http://www.usitc.gov*). Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on 202-205-1810.

SUPPLEMENTARY INFORMATION: The Commission instituted this investigation on May 13, 1998, based on a complaint filed by Oak Technology, Inc. 63 Fed. Reg. 26625 (1998). The complaint named four respondents: MediaTek, Inc., United Microelectronics Corporation ("UMC"), Lite-On Technology Corp., and AOpen, Inc., Actima Technology Corporation, ASUSTek Computer, Incorporated, Behavior Tech Computer Corporation, Data Electronics, Inc., Momitsu Multi Media Technologies, Inc., Pan-International Industrial Corporation, and Ultima Electronics Corporation were permitted to intervene in the investigation.

In its complaint, Oak alleged that respondents violated section 337 by importing into the United States, selling for importation, and/or selling in the United States after importation electronic products and/or components that infringe claims of U.S. Letters Patent 5,581,715 (the '715 patent). The presiding administrative law judge (ALJ) held an evidentiary hearing from January 11, 1999, to January 28, 1999.

On May 10, 1999, the ALJ issued an initial determination ID (Order No. 15) granting respondent UMC's motion for a summary determination terminating UMC from the investigation on the basis of a license agreement. On May 12, 1999, the ALJ issued his final ID in which he found that there was no violation of section 337. Although the ALJ found that there was a domestic industry with respect to the '715 patent, he found that there was no infringement of any claim at issue, and that the claims in issue of the '715 patent were invalid for on-sale bar under 35 U.S.C. § 102(b), anticipation under 35 U.S.C. § 102(a), obviousness under 35 U.S.C. § 103, indefiniteness under 35 U.S.C. § 112(1), (2), and (6), and derivation under 35 U.S.C. § 102(f).

Complainant Oak filed a petition for review of Order No. 15 and respondent UMC and the Commission investigative attorneys (IAs) filed responses to Oak's petition for review of Order No. 15. Oak, respondents UMC, MediaTek, Lite-On Technology, and AOpen, and the IAs filed petitions for review of the final ID, and all parties subsequently responded to each other's petitions for review of the final ID.

On June 28, 1999, the Commission determined not to review the ALJ's findings with respect to the preamble of claim 1 and its digital signal processor (DSP) element, and determined to review the remainder of the final ID and Order No. 15.

Having examined the record in this investigation, including the briefs and the responses thereto, the Commission determined that there is no violation of section 337. More specifically, the Commission affirmed the ALJ's finding that there is a domestic industry with respect to the '715 patent; affirmed the ALJ's finding of no literal infringement and no infringement under the doctrine of equivalents; reversed the ALJ's findings of invalidity based on an on-sale bar under 35 U.S.C. § 102(b), anticipation under 35 U.S.C. § 102(a), obviousness under 35 U.S.C. § 103, indefiniteness and vagueness under 35 U.S.C. § 112(1), (2), and (6), for derivation under 35 U.S.C. § 102(f); and reversed the ALJ's finding of unenforceablity due to inequitable conduct before the PTO.[1] The Commission determined to take no position with regard to Order No. 15 terminating respondent UMC from the investigation, and with regard to the issue of equitable estoppel.

This action is taken under the authority of section 337 of the Tariff Act of 1930, 19 U.S.C. § 1337, and sections 210.45-210.51 of the Commission's Rules of Practice and Procedure, 19 C.F.R. §§ 210.45-210.51.

[1] Chairman Bragg and Commissioner Crawford take no position on the validity and enforceability of the claims at issue of the '715 patent.

Copies of the public versions of the subject IDs, and all other nonconfidential documents filed in connection with this investigation, are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone 202-205-2000.

By order of the Commission.

Donna R. Koehnke

Donna R. Koehnke
Secretary

Issued: September 27, 1999

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C. 20436

In the Matter of

CERTAIN CD-ROM CONTROLLERS AND PRODUCTS CONTAINING THE SAME - II

Inv. No. 337-TA-409

ORDER

The Commission instituted this investigation on May 13, 1998, based on a complaint filed by Oak Technology, Inc. 63 Fed. Reg. 26625 (1998). The complaint named four respondents: MediaTek, Inc., United Microelectronics Corporation ("UMC"), Lite-On Technology Corp., and AOpen, Inc., Actima Technology Corp., ASUSTek Computer, Inc., Behavior Tech Computer Corp., Data Electronics, Inc., Momitsu Multi Media Technologies, Inc., Pan-International Industrial Corp., and Ultima Electronics Corp. were permitted to intervene in the investigation.

In its complaint, Oak alleged that respondents violated section 337 of the Tarriff Act of 1930 by importing into the United States, selling for importation, and/or selling in the United States after importation electronic products and/or components that infringe claims 1-5 and 8-10 of U.S. Letters Patent 5,581,715 (the '715 patent). Oak did not assert claims 8 and 10 at the evidentiary hearing.

The presiding administrative law judge (ALJ) held an evidentiary hearing from January 11, 1999, to January 28, 1999, in which Oak, MediaTek, UMC, and Lite-On Technology participated.

On May 10, 1999, the ALJ issued an initial determination ID (Order No. 15) granting respondent UMC's motion for a summary determination terminating UMC from the investigation on the basis of a license agreement. On May 12, 1999, the ALJ issued his final ID in which he found that there was no violation of section 337. Although the ALJ found that there was a domestic industry with respect to the '715 patent, he found that there was no infringement of any claim at issue, and found that the claims in issue of the '715 patent were invalid for on-sale bar under 35 U.S.C. § 102(b), anticipation under 35 U.S.C. § 102(a), obviousness under 35 U.S.C. § 103, indefiniteness under 35 U.S.C. § 112(1), (2), and (6), and derivation under 35 U.S.C. § 102(f).

Complainant Oak filed a petition for review of Order No. 15 and respondent UMC and the Commission investigative attorneys (IAs) filed responses to Oak's petition for review of Order No. 15. Oak, respondents UMC, MediaTek, Lite-On Technology, and AOpen, and the IAs filed petitions for review of the final ID, and all parties subsequently responded to each other's petitions for review of the final ID.

On June 28, 1999, the Commission determined not to review the ALJ's findings with respect to the preamble of claim 1 and its digital signal processor (DSP) element, and determined to review the remainder of the final ID and Order No. 15.

Having examined the record in this investigation, including the briefs and the responses thereto, it is hereby ORDERED THAT:

1. The investigation is terminated with a finding of no violation of section 337 of the Tariff Act of 1930 (19 U.S.C. §1337).

2. The Commission finds that a domestic industry exists with respect to the '715 patent.

3. The claims in issue of the '715 patent are found to be not literally infringed and not infringed under the doctrine of equivalents by the accused MediaTek CD-ROM controllers.

4. The claims in issue of the '715 patent are found to be not invalid on the basis of an on-sale bar under 35 U.S.C. § 102(b), anticipation under 35 U.S.C. § 102(a), obviousness under 35 U.S.C. § 103, indefiniteness and vagueness under 35 U.S.C. § 112(1), (2), and (6), or derivation under 35 U.S.C. § 102(f).

5. The '715 patent is found to be not unenforceable due to inequitable conduct before the U.S. Patent and Trademark Office.

6. The Commission takes no position with regard to Order No. 15 terminating respondent UMC from the investigation and no position with regard to the issue of equitable estoppel.

7. The Secretary shall serve copies of this Order, and the forthcoming Commission Opinion in support thereof, on the parties of record and on the Department of Health and Human Services, the Department of Justice, and the Federal Trade Commission, and publish notice thereof in the *Federal Register*.

By order of the Commission.

Donna R. Koehnke

Donna R. Koehnke

Secretary

Issued: **September 27, 1999**

CERTAIN CD-ROM CONTROLLERS AND PRODUCTS CONTAINING SAME II **337-TA-409**

CERTIFICATE OF SERVICE

I, Donna R. Koehnke, hereby certify that the attached **NOTICE OF FINAL DETERMINATION**, was served upon the following parties via first class mail, and air mail where necessary, on September 28, 1999.

Donna R. Koehnke

Donna R. Koehnke, Secretary
U.S. International Trade Commission
500 E Street, S.W., Rm. 112
Washington, D.C. 20436

ON BEHALF OF COMPLAINANT OAK TECHNOLOGY, INC.:

Joel M. Freed, Esq.
Stephen J. Rosenman, Esq.
Howrey and Simon
1299 Pennsylvania Avenue, N.W.
Washington, D.C. 20004

ON BEHALF OF UNITED MICROELECTRONICS CORPORATION, MEDIATEK, INC., LITE-ON GROUP, LITE-ON TECHNOLOGY CORPORATION, AOPEN INC.:

Jai Rho, Esq.
Loeb and Loeb L.L.P.
10100 Santa Monica Blvd.
Suite 2200
Los Angeles, CA 90067

Mark S. McConnell, Esq.
Joanne L. Leasure, Esq.
Hogan and Hartson L.L.P
Columbia Square
555 Thirteenth Street, N.W.
Washington, D.C. 20004-1109

Michael A. Ladra, Esq.
Wilson, Sonsini, Goodrich and Rosati
650 Page Mill Road
Palo Alto, CA 94304-1050

ON BEHALF OF COMMISSION:

Timothy P. Monaghan, Esq.
International Trade Commission
Office of General Counsel
500 E Street, S.W., Rm. 707-U
Washington, D.C. 20436

T. Spence Chubb, Esq.
International Trade Commission
Office of Unfair Import Investigations
500 E Street, S.W., Rm. 401-F
Washington, D.C. 20436

<u>PUBLIC MAILING LIST</u>

Donna Wirt
LEXIS - NEXIS
1150 18th Street, NW
Suite 600
Washington, D.C. 20036

Ronnita Green
West Services, Inc.
901 Fifteenth Street, NW
Suite 1010
Washington, D.C. 20005

Charles S. Stark, Esq.
Antitrust Divison
U.S. Department of Justice
Penn. Ave., & 10th St., N.W.
Washington, D.C. 20530

Randy Tritell, Esq.
Director for Int'l Antitrust
Federal Trade Comm., Rm. 380
Penn. Ave., at 6th St., N.W.
Washington, D.C. 20580

Richard Lambert, Esq.
Nat'l Institute of Health
9000 Rockville Pike
Bldg. 31, Room 2B50
Bethesda, MD 20892-2111

Michael Smith, Acting Chief
Intellectual Property Rights Branch
U.S. Customs Service
Ronald Reagan Building, 3rd Floor
1300 Penn Ave., N.W.
Washington, D.C. 20229

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C. 20436

In the Matter of CERTAIN CD-ROM CONTROLLERS AND PRODUCTS CONTAINING THE SAME - II	Inv. No. 337-TA-409

COMMISSION OPINION

This section 337 investigation is before the Commission for final disposition of the issues under review and, if necessary, for determinations on remedy, the public interest, and bonding. We find no violation of section 337 of the Tariff Act of 1930, and therefore need not consider the issues of remedy, the public interest, and bonding.

I. BACKGROUND

The Commission instituted this investigation on May 13, 1998, based on a complaint filed by Oak Technology, Inc. (Oak), 63 Fed. Reg. 26625 (1998). The complaint named four respondents: MediaTek, Inc., United Microelectronics Corp. (UMC), Lite-On Technology Corp., and AOpen, Inc., Actima Technology Corp., ASUSTek Computer, Inc., Behavior Tech Computer Corp., Data Electronics, Inc., Momitsu Multi Media Technologies, Inc., Pan-International Industrial Corp., and Ultima Electronics Corp. were permitted to intervene in the investigation.

In its complaint, Oak alleged that respondents had violated section 337 by importing into the United States, selling for importation, and/or selling in the United States after importation electronic products and/or components that infringe certain claims of U.S. Letters Patent 5,581,715 (the '715 patent). The presiding administrative law judge (ALJ) held an evidentiary hearing from January 11, 1999, to January 28, 1999.

On May 10, 1999, the ALJ issued an initial determination (ID) (Order No. 15) granting the motion of respondent UMC for a summary determination terminating UMC from the investigation on the basis of a license agreement. On May 12, 1999, the ALJ issued his final ID in which he found that there was no violation of section 337. Specifically, the ALJ found that there was no infringement of any claim at issue, and that the claims at issue of the '715 patent were invalid for on-sale bar under 35 U.S.C. § 102(b), anticipation under 35 U.S.C. § 102(a), obviousness under 35 U.S.C. § 103, indefiniteness under 35 U.S.C. § 112(1), (2), and (6), derivation under 35 U.S.C. § 102(f), and that the '715 patent was unenforceable due to inequitable conduct before the U.S. Patent and Trademark Office (PTO). The ALJ also found that there was a domestic industry with respect to the '715 patent.

Complainant Oak filed a petition for review of Order No. 15 and respondent UMC and the Commission investigative attorneys (IAs) filed responses to Oak's petition for review of Order No. 15. Oak, respondents UMC, MediaTek, Lite-On Technology, and AOpen, and the IAs filed petitions for review of the final ID, and all parties subsequently responded to each other's petitions for review of the final ID.

On June 28, 1999, the Commission determined not to review the ID's findings with respect to the preamble of claim 1 and its digital signal processor (DSP) element, and determined to review the remainder of the final ID and Order No. 15 in its entirety.

Having considered the parties' written submissions and the evidence of record, we determined to: (1) affirm the ID's finding that there is a domestic industry with respect to the '715 patent; (2) affirm the ID's finding of no literal infringement and no infringement under the doctrine of equivalents; (3) reverse the ID's findings of invalidity based on an on-sale bar under 35 U.S.C. § 102(b), anticipation under 35 U.S.C. § 102(a), obviousness under 35 U.S.C. § 103, indefiniteness under 35 U.S.C. § 112(1), (2), and (6), and derivation under 35 U.S.C. § 102(f); (4) reverse the ID's finding of unenforceablity due to inequitable conduct before the PTO, (5) take no position with regard to Order No. 15 terminating respondent UMC from the investigation, and (6) take no position on the issue of equitable estoppel.[1] We have therefore determined that there is no violation of section 337 in this investigation.

II. VIOLATION ISSUES

A. <u>Summary of Key Issues and Determinations in this Investigation</u>

The key issues in this investigation are (i) whether the "memory means" element of claim 1 is a means-plus-function claim element with no corresponding structure in the patent

[1] Chairman Bragg and Commissioner Crawford concur in the ID's finding that there is a domestic industry with respect to the '715 patent, in the determinations to affirm the ID's claim construction of the error detection and correction means, and in the finding of no literal infringement and no infringement under the doctrine of equivalents based on that claim construction. Because they concur in the finding that the MediaTek controller does not infringe the '715 patent, they do not find it necessary to reach the other issues, and thus do not join in the discussion, analysis or conclusion related to those issues.

specification, (ii) construction of the "data error detection and correction means" element of claim 1, (iii) construction of the "host interface means,"element of claim 1, and (iv) whether the so-called "ATAPI specification"[2] is a printed publication.

The ID found that the "memory means" claim element was a means-plus-function claim element that lacked a "corresponding structure" in the specification. We agree with the ID that the "memory means" element is a means-plus-function claim element, but disagree with the finding that this element has no "corresponding structure" in the specification. We believe that a person of ordinary skill in this technological art would find an adequate disclosure of the claimed "memory means" in the specification, and would regard as an obvious error the language and drawings of the specification of the '715 patent describing the disclosed memory means as not being part of the claimed invention.

The proper construction of the "data error detection and correction means" element of claim 1 governs whether respondents' accused MediaTek CD-ROM controller infringes the claims in issue of the '715 patent. We affirm the ID's finding that there is no literal infringement or infringement under the doctrine of equivalents based on a comparison of the binary mathematics, the circuitry, the sequence of operations, the data processed, and the interrelationship with the previous error correction operation, of the accused MediaTek CD-ROM controller and the '715 patent.

[2] ATAPI is an acronym for AT Attachment Packet Interface for CD-ROM devices. A complete list of acronyms used in this opinion is attached as an appendix to the opinion

The construction of the "host interface means" largely determines the relevance of the prior art asserted by respondents against claim 1 of the '715 patent. If a "direct" connection to the IDE (integrated drive electronics) bus is optional, then the asserted prior art becomes very relevant for assessing the validity defenses of on-sale bar, anticipation, obviousness, and derivation. Construction of the host interface means also has direct implications for analyzing whether the patent applicants engaged in inequitable conduct before the PTO. We reverse the ID on several aspects of construction of the "host interface means" and find that the host interface means requires, among other things, a *direct* connection to the IDE bus. As a result we do not find the patent invalid for on-sale bar, anticipation, obviousness, and derivation, and we do not find that the patent unenforceable due to inequitable conduct before the PTO.

A fourth key issue is whether the so called "ATAPI specification" is a prior art publication. The ATAPI specification describes a detailed command set that enables communication between a CD-ROM drive and a host PC over an IDE bus. Without the ATAPI specification, none of the asserted combinations of prior art asserted by respondents for obviousness purposes discloses a host interface means with a direct connection to the IDE bus. However, if the ATAPI specification is prior art publication, then it, when combined with the Mitsumi prototype (a prior art device), would render the asserted claims of the `715 patent obvious. We reverse the ID's finding that the ATAPI specification is a prior art publication.

B. Construction of Claim 1 of the '715 Patent

Claim 1

While Oak asserts infringement of claims 1-5 and 9 of the '715 patent, the primary focus of this investigation is on claim 1. Claim 1 is an independent claim from which claims 2, 3, 4, 5, and 9 depend. Claim 1 is set forth below, with critical language highlighted in bold and italic type.

> A compact disk drive controller to control the communication of data between a compact disk in a compact disk drive and a host computer *via an IDE/ATA data bus*, said data bus for receiving and transmitting data between said controller and said host computer, said disk drive having drive electronics that include a digital signal processor and a microcontroller, said controller comprising:
>
> a digital signal processor interface for receiving data from said digital signal processor, said digital signal processor interface descrambling and assembling data received from said digital signal processor;
>
> ***memory means*** for *temporarily storing* data, said memory means temporarily storing *said assembled data*;
>
> ***data error detection and correction means*** for correcting said assembled data, said detection and correction means including *error correction circuitry* for performing error correction on said assembled data and a *cyclic redundancy checker* for detecting errors in said assembled data *after correction of said data* by said correction circuitry for providing corrected data; and
>
> ***host interface means*** for connecting said host computer to said controller, said interface means *adapted to **receive** data addresses and commands* from said host computer *and **transmit** corrected data* to said host computer to insure uninterrupted flow of data from said controller to said host computer.

We previously determined not to review the ID's construction of the preamble and digital signal processor elements of claim 1, but determined to review the "memory means," the "data error detection and correction means," and the "host interface means" elements of that claim.

2. Memory Means

The "memory means" element of claim 1 reads as follows: "memory means for temporarily storing data, said memory means temporarily storing said assembled data." The use of the term "means" raises a rebuttable presumption that the element is a means-plus-function element under 35 U.S.C. §112, ¶ 6. To rebut the presumption of § 112, ¶ 6, the element must "elaborate sufficient structure, material, or acts within the claim itself to perform entirely the recited function." *Sage Products, Inc. v. Devon Industries, Inc.*, 126 F.3d 1420, 1427 (Fed. Cir. 1997). The ID made a threshold finding that the "memory means" element is a means-plus-function element. (ID at 26). This finding was based on the testimony of respondents' expert witness (Blahut) that a CD-ROM sector of data is the amount of data typically read on each data read from a CD-ROM. Blahut Transcript (Tr.)[3] 1852-1854. Complainant Oak relied on the testimony of its expert (Wedig) that the term "memory" alone implicates sufficient structure to overcome the means-plus-function presumption. Wedig testified that the term "memory" implicates "any of the possible structures which implement memory." Wedig, Tr. 623-624. However, the ID found that most types of memory cited by Wedig have insufficient storage capacity to store a CD-ROM sector of data. Thus, the ID found that the term "memory means" has insufficient structure to support a finding that the term is *not* a means-plus-function element.

The ID found that the term "memory means" should be interpreted in light of the

---

[3] The following abbreviations are used in this opinion: Br. (brief), CX (complainant's exhibit), FF (ID's Findings of Fact), ID (Initial Determination), RX (respondents' exhibit), Tr. (hearing transcript).

specification to mean a memory device capable of storing an entire sector of CD-ROM data, *i.e.*, approximately 16,000 bits. (ID at 26-27; FF 2 at 200). This finding is the ID's interpretation of the claim phrase "said assembled data." A dynamic random access memory (DRAM) is the only device discussed in the patent specification capable of storing a sector of CD-ROM data. Since the DRAM is explicitly described in certain portions of the specification as *not* being part of the claimed controller, however, this finding laid the foundation for the ID's finding of invalidity based on a lack of the "corresponding structure" required by 35 U.S.C. § 112, ¶6.

The threshold issue in interpreting the "memory means" element is whether it is a means-plus-function element that invokes §112, ¶ 6. As noted, an inventor's use of the word "means" in a claim creates a rebutable presumption that the claim is a means-plus-function claim. Thus, the phrase "memory means" creates a rebuttable presumption that the term is a means-plus-function claim. This presumption can be rebutted if the claim recites sufficient structure to perform the claimed function.[4] The phrase "memory" is a general term which, according to testimony of record, implicates "any of the possible structures which implement memory," such as a DRAM, a register, a latch, or a flip-flop.[5] The question then is whether an open-ended term such as "memory" has sufficient structure to overcome the means-plus-function presumption.

In *Rodime PLC v. Seagate Technology Inc.*, 174 F.3d 1294 (Fed. Cir. 1999), the Federal Circuit held that the claim term "positioning means for moving said transducer means between

---

[4] *Rodime PLC v. Seagate Technology, Inc.*, 174 F.3d 1294 (Fed. Cir. 1999).

[5] Wedig Tr. at 623-624.

the concentrically adjacent tracks on said micro hard-disk" overcame the §112, ¶ 6 presumption because the claim itself had sufficient structure to perform the claimed function. However, in *Signtech USA Ltd. v. Vutek Inc.*, 174 F.3d 1352 (Fed. Cir. 1999), the term "ink delivery means" was held not to overcome the § 112, ¶ 6 presumption because the term "ink delivery" did not recite sufficient structure. The term "ink delivery" was found to be too general and did not give a "detailed recitation of structure."[6]

In our view, the term "memory means," does not explicitly recite sufficient structure to preclude the application of § 112, ¶ 6. As the ID pointed out, there are a number of memory devices that are capable of carrying out this claim function, *viz.*, a RAM, a register, a latch, or a flip flop, to name a few (ID at 25). Thus, the term "memory means' in and of itself does not recite sufficient structure to overcome the presumption that this claim is a means-plus-function claim, and the ID therefore correctly found that "memory means" is a means-plus-function element.

The ID also found that the "memory means for temporarily storing ... said assembled data" was a DRAM capable of storing a block of CD-ROM data, *i.e.*, approximately 16,000 bits of digital data. The specification of the '715 patent states that "[t]he error correction circuitry would first perform Reed-Solomon error correction *on each block of data* ... ."[7] (emphasis

---

[6] *Rodime* at 1303.

[7] Complainant's Exhibit (CX)-1/Respondent's Exhibit (RX)-1 '715 patent, col. 6, lines 30-33 (see also col. 12, lines 44-46 "E01RQ–bit5–Error Detect and Correct Request "1" enables the error correction and detection (ECC and EDC) logic to process the following *CD-ROM blocks*

(continued...)

added). The record shows that the ordinary understanding of the "memory means" element in the context of CD-ROM controllers is a memory means capable of storing an entire sector of CD-ROM data. Blahut, Tr. 1852. In particular, the term "assembled data," suggests an entire sector of CD-ROM data to one of ordinary skill in the art. Blahut, Tr. 1854. This interpretation is confirmed by the '715 patent specification's use of the term "block of data" as opposed to a few bytes of CD-ROM data. As noted, a block or sector of CD-ROM data is approximately 16,000 bits. Blahut, Tr. 1852.

We agree with the ID's claim construction of the "memory means" element and adopt its finding that the term "memory means" is a means-plus-function element, and that the "memory means" in the context of claim 1 is a DRAM capable of hold approximately 16,000 bits of CD-ROM "assembled data."

3. Data Error Detection And Correction Means

The "data error and correction means" element of claim 1 of the '715 patent reads as follows:

> *data error detection and correction means* for correcting said assembled data, said detection and correction means including *error correction circuitry* for performing error correction on said assembled data and a *cyclic redundancy checker* for detecting errors in said assembled data *after correction of said data* by said correction circuitry for providing corrected data (emphasis added).[8]

---

[7] (...continued)
... ." (emphasis added)).

[8] The threshold issue in this claim construction is whether the "data error detection and correction means" is a means-plus-function claim element. As noted above, the use of the word

(continued...)

The ID first focused on the language in this element that reads "detecting errors in said assembled data *after* correction of said data." The ID made a straightforward finding that this language requires that error correction occur first on the "said assembled data" followed by error detection. (FF 118-121). The ID further interpreted this language as requiring "that the claimed CD-ROM controller *first* perform error correction <u>on an entire sector of data</u> with error correction circuitry, and *then* perform error detection with a cyclic redundancy checker circuit *after* error correction" (ID at 30)(underlined emphasis added; italics in original). This finding goes back to the previously-mentioned finding that "said assembled data" means an entire 16,000 bit sector, and also to specific language in the specification pointing out that the error correction circuitry (ECC) and the error detection circuitry (EDC) process CD-ROM blocks of data.[9]

The ID next found that the "error correction circuitry" called for in this claim element refers to circuitry for correcting errors in Reed-Solomon code words. (FF 55). It came to that conclusion by reasoning that the claim relates to CD-ROM technology and the so-called "yellow book" specification, defining data protocols (*i.e.*, agreed upon procedures) for CD-ROMs, states that the data must be written in Reed-Solomon code words. (FF 54). The ID noted that the specification describes no specific circuitry for error correction, but simply states that these types

---

[8] (...continued)
"means" in this claim element creates a presumption that § 112, ¶ 6 applies. However, all parties agree that this claim element also recites sufficient structure (via the terms: "error correction circuitry" and "a cyclic redundancy checker") to overcome that presumption. We agree that the error detection and correction means should not be interpreted as a means-plus-function element.

[9] CX-1/RX-1, '715 patent, col. 12, lines 44-46.

of error correction code circuits are commonly available as hardware. (FF 61; '715 patent, col. 6, lines 41-43). The ID also noted that respondents' expert (Blahut) agreed that a number of circuits are available for such error correction and that Reed-Solomon is the standard error correction method and circuitry used in CD-ROMs. (FF 55, Blahut, Tr. 1812-1813).

Finally, the ID interpreted the "cyclic redundancy checker" as a "linear feedback shift register which operates on an entire sector or block of data." (ID at 34; FF 68). The ID noted that while the patent specification does not describe any particular circuitry to be used for the error detection operation, it states that "[t]hese ... EDC-CRC circuits are commonly available as hardware used in many other applications"[10] ('715 patent, col. 6, lines 41-43). The ID then went on to find that the evidence shows that, at the time the application that matured into the '715 patent was filed, the only specific type of circuit commonly available as hardware for performing a cyclic redundancy check was a linear feedback shift register (ID at 35; FF 96).

Oak asserts that the ID erred in restricting the scope of the cyclic redundancy check to linear feedback shift registers, which are mentioned neither in the claims nor elsewhere in the '715 patent. It argues that the phrase "commonly available as hardware," to the extent it is relevant, should be interpreted to mean "commonly available as literature and product art." The IAs assert that the ID erred in limiting the "cyclic redundancy checker" to devices that were "commonly available as hardware" at the time of the invention. They regard the phrase

---

[10] "CRC" and "cyclic redundancy check" will be used interchangeably in this opinion and will refer to the method of performing cyclic redundancy error detection. The term *cyclic redundancy checker* will be used to refer to a specific hardware implementation of a CRC.

"commonly available as hardware" as not directed to structure, and assert that it should not be construed to limit any available choices for implementing a CRC. The IAs argue that a cyclic redundancy checker need only be publicly available in literature and need not be reduced to hardware as of the June 1994 filing date of the patent application that matured into the '715 patent. They conclude that requiring the "cyclic redundancy checker" to be a linear feedback shift register, a circuit nowhere alluded to in the specification, is erroneous.

In construing the "data error detection and correction means," in accordance with *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576 (Fed. Cir. 1996), we first look to the claim language. We agree with the ID that the plain language of the claim requires a clear sequence, *viz.*, "error correction circuitry for performing error correction on said assembled data and a cyclic redundancy checker for detecting errors in said assembled data *after* correction of said data by said correction circuitry" ('715 patent, col. 29, lines 13-16, emphasis added). We also agree with the ID that the word "after" is "clear English," with no specialized technical meaning, and dictates a particular sequence of operations in claim 1 of the '715 patent. Thus, the claimed CD-ROM controller of the '715 patent first performs error correction on an entire sector of data with error correction circuitry, and then performs error detection with a cyclic redundancy checker circuit on that sector. The specification of the '715 patent further confirms this construction, stating that "[t]he error correction circuitry would first perform Reed-Solomon error correction *on each block of data*. ... Then, a cyclic redundancy check of the corrected data would be performed." (emphasis added).[11] The ID interpreted the phrase "assembled data" in the claim, and the phrase "block of data" in the specification, as being a 16,000 bit CD-ROM data block. We agree with the ID found that claim 1 of the '715 patent sets up a clear and straightforward sequence of first performing an error correction operation on an entire block (or sector) of CD-ROM data, followed by a cyclic redundancy check on that corrected block of data.

The final step in the claim construction of the data error detection and correction means is the construction of the terms "error correction circuitry" and "cyclic redundancy checker." We agree with the ID that the portion of claim 1 that reads "error correction circuitry for performing error correction on said assembled data" refers to a Reed-Solomon error correction circuit. The testimony of record makes clear that one of ordinary skill in the art would understand the phrase "error correction circuitry" to refer to circuitry that performs Reed-Solomon error correction on a sector of data coming from a CD-ROM disk. Blahut, Tr. 1811-1815, 1869-1870. CD-ROM data is formatted according to the so-called "yellow book" specification, and the yellow book states that the data must be written in Reed-Solomon code words. (FF 54) We adopt the ID's finding that the data error correction circuitry of the data error correction means is a Reed-Solomon error correction circuit.[12]

The parties' dispute centers on the construction of the claim term "*a cyclic redundancy*

---

[11] '715 patent, col. 6, lines 30-39.

[12] Oak has not challenged this aspect of the ID's interpretation of the data error detection and correction means.

checker for detecting errors in said assembled data after correction of said data by said correction circuitry." (emphasis added). In construing this term, the ID first looked to the language of claim 1 of the '715 patent and determined that "a cyclic redundancy checker" was a technical term. ID at 31. Thus, in accordance with *Vitronics*, the ID looked to the evidence of record to ascertain how one of ordinary skill in the art would understand this term. Based on the testimony of Dr. Blahut, Mr. Chuang, and Dr. Luby,[13] the ID determined that one of ordinary skill in the art would understand the term cyclic redundancy checker to refer to a linear feedback shift register which performs a cyclic redundancy check. A CRC is essentially a binary division operation on an entire 16,000 bit sector or block of CD-ROM data. ID at 31-34.

After the ID determined that one of ordinary skill in the art would understand the claim term "cyclic redundancy checker" as a linear feedback shift register, it turned to the specification to confirm this construction. *Vitronics* emphasized the importance of the specification in claim construction: "[t]he specification acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication. ... Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Vitronics* at 1582. Thus, although the specification provides no specific circuitry for the "cyclic redundancy checker," it is the best source for understanding how this technical term is used in the claim.[14] Although the '715 specification

[13] Dr. Blahut was respondents' expert in the area of information theory, coding theory and error control codes. Mr. Chuang is the designer of the error detection and correction circuitry for MediaTek's CD-ROM controller. Dr. Luby was complainant's expert witness in the area of information theory, coding theory, and error control codes.

[14] "The best source for understanding a technical term is the specification from which it arose

(continued...)

contains no specific description of the hardware for error detection means, it states that "[t]hese ECC and EDC-CRC circuits are commonly available in hardware used in many other applications." ('715 patent, col. 6, lines 41-43). The words "*commonly* available as hardware used in many other applications" indicate to us that this technical term refers to the standard or conventional usage of the term "cyclic redundancy checker," *viz.*, the division of a generator polynomial into a block of data to produce a cyclic redundancy check remainder. (RX-490, Encyclopedia of Computer Science, pp. 382-303).

According to respondents' experts (Blahut and Chuang) a cyclic redundancy checker is typically implemented by a linear feedback shift register (also known as a serial shift register). Blahut, Tr. 1818; RX-490; Chuang, Tr. 1585-1596, 1768-1775. Oak argues that a "cyclic redundancy check" is simply a mathematical algorithm that can be performed by any device that is designed to yield the same result, and that the portion of the specification in question does not dictate the use of a specific type of circuitry. (Complainant's Post-Hearing Brief at 46). However, as the ID pointed out, the language of claim 1 clearly refers to "error correction circuitry" and to a "cyclic redundancy checker," terms which both complainant's expert (Luby) and respondents' expert (Blahut) agreed are references to hardware. Luby, Tr. 1466, Blahut, Tr. 1831. The evidence of record shows that as of June 1994, when the application for the '715 patent was filed, only one specific type of EDC-CRC circuit was *commonly* available as hardware used in many other applications, *viz.*, a linear feedback shift register. Blahut, Tr.

---

[14] (...continued)
... ." *Multiform Desiccants, Inc. v. Medzam, Ltd.*, 133 F.3d 1473 (Fed. Cir. 1998).

1824-1825. Oak relies on the testimony of its expert (Luby) in an attempt to expand the types of circuits "commonly available as hardware used in many other applications" as of the filing date of the '715 patent. However, Dr. Luby conceded that he did not know whether the error detection methods discussed in any of the references shown to him had ever been implemented in hardware. He admitted that, although he understood the term "cyclic redundancy check" to mean a binary division problem in which one string of bits is divided into another, the usual hardware implementation of a cyclic redundancy check was a linear feedback shift register. Luby, Tr. 1488-1489, 1500-1504.

The four references used by Oak to expand the CRC beyond a linear feedback shift register are all special case applications of the CRC. The four references are all examples of updating an existing CRC remainder with a knowledge of the type and location of the corrupted data. All the cited references depend on data not normally or commonly found in a cyclic redundancy check operation. Thus, the IBM Technical Disclosure Bulletin entitled "High-Speed Cyclic Redundancy Checking Scheme For Error Correcting Codes," RX-608, discloses a method for updating an original CRC remainder using data from a previous error correction operation. As stated in the article, "[n]ormally, a linear feedback shift register ... is used to perform the division," and the "conventional way of checking CRC is to read the corrected data into the CRC shift register [a linear feedback shift register] and test if the resulting contents of the shift register are zero." However, the method described in the article is used to update the original CRC remainder with error data from an error correction operation. As the IBM Technical Disclosure Bulletin points out, this kind of update of the CRC remainder is *not* a "conventional way of checking CRC." RX-608 at p. 2. As we have noted, neither the claims nor the specification of the '715 patent disclose anything other than a cyclic redundancy checker "*commonly* available as hardware used in many other applications."

The specification of a patent must support a specialized meaning of a claim term. In *Hoover Group, Inc. v. Custom Metalcraft, Inc.*, 66 F.3d 299 (Fed. Cir. 1995), the Federal Circuit found that the ordinary meaning of a disputed term prevailed over a proffered specialized meaning because the patentee could not point to anything in the specification or prosecution history "to suggest other than the ordinary meaning" of the term. In the present investigation, Oak has pointed to nothing in the claims or specification that refers to any special case usage of the term "cyclic redundancy checker." Indeed, the only language in the specification that refers to the "cyclic redundancy checker" ("*commonly* available as hardware used in many other applications") makes clear that the patentees had in mind only the standard, conventional usage of the term "cyclic redundancy checker," *viz.*, the division of a generator polynomial into a data block to produce a CRC remainder.

Language in a specification dealing with a disputed claim term can also be used to limit the expansion of that claim term. In *Laitram Corp. v. Morehouse Industries, Inc.*, 46 U.S.P.Q.2d 1609 (Fed. Cir. 1998), the Federal Circuit found that the written description was important in limiting a potentially expansive claim interpretation. The patent at issue claimed a sprocket assembly with teeth that "extended downwardly," and the specification disclosed a sprocket with a planar surface. The accused product had sprockets with teeth that were curved. Although the plain language of the claim seemed to cover the accused device, the court noted that "nothing in the written description suggests that the driving surfaces can be anything but flat," *Laitram,* 46 U.S.P.Q.2d at 1614, and refused to expand the claim to cover the accused device. Similarly, in this investigation there is nothing in the specification that supports an interpretation that the cyclic redundancy checker is other than the standard or conventional CRC, a binary division into a block of CD-ROM data.

Patent applicants have a statutory obligation to distinctly claim the subject matter of their invention.[15] They must provide clear boundaries for their invention, and where there is ambiguity in the claim and specification, the Federal Circuit "consider[s] the notice function of the claim best served by adopting the narrower meaning ... to guard against unreasonable advantages to the patentee and disadvantages to others arising from uncertainties as to their respective rights." *Athletic Alternatives, Inc. v. Prince Mfg., Inc.*, 73 F.3d 1573 (Fed. Cir. 1996). Thus, when there is a choice between a boarder claim interpretation and a narrower one, and the specification is ambiguous, the notice function of the patent claim is best served by adopting the narrower meaning.

In our view, the ID correctly found that the only circuits commonly available for a CRC when the application for the '715 patent was filed were linear feedback shift registers. However, we also agree with the IAs that the proper focus of a CRC operation is the CRC mathematics, *i.e.*, the division of a 33-bit binary polynomial into a 16,000-bit EDC code word and any

---

[15] "The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention." 35 U.S.C. §112, ¶ 2

hardware, commonly available in June, 1994, that performs that long division operation. We construe the scope of the CRC operation as defined in respondents' exhibit RX-490, an entry in the Encyclopedia of Computer Science. In RX-490 at pp. 382-383, a cyclic redundancy check is described as an error detection operation with the following features:

> [a]ll characters in the message block are treated as a serial string of bits representing a binary number. This number is then divided modulo 2 by a predetermined binary number and the remainder is appended to the block of characters as a cyclic redundancy check (CRC) character. The CRC is compared with the check character obtained in similar fashion at the receiving end. If they agree the message is assumed to be correct.

We therefore agree with the ID that the *common* hardware implementation of a cyclic redundancy checker in June 1994 was a linear feedback shift register. However, we augment the ID's analysis by also discussing in our claim construction (and infringement analysis, below) the CRC mathematical detection operation, the interrelationship between the error correction and detection operations, the amount and type of data processed, and the sequence of steps in the error detection function.

Thus, with regard to the overall claim construction of the "data error detection and correction means" element, we agree with the ID and affirm the following claim construction for this element: a Reed-Solomon error correction is first performed on an entire sector of CD-ROM assembled data (approximately 16,000 bits), followed by a cyclic redundancy check on the entire CD-ROM sector of assembled data. The cyclic redundancy checker is hardware, commonly available in June 1994, that performs the division of a CRC generator binary polynomial into a 16,000-bit EDC code word to produce a CRC remainder.

4. <u>Host Interface Means</u>

The fourth and last element of claim 1 of the '715 patent reads as follows:

> ***host interface means*** for connecting said host computer to said controller, said interface means *adapted to* ***receive*** *data addresses and commands* from said host computer *and* ***transmit*** *corrected data* to said host computer to insure uninterrupted flow of data from said controllers to said host computer. (emphasis added).

Before discussing our construction of the host interface means, we will provide a brief overview of an IDE host interface as background. The following discussion was compiled from RX-31C (the ATA specification), Oak's Written Submission On The Issues Under Review, pp. 41-49, and Wedig, Tr. 442-495.

An IDE host interface mediates command data and CD-ROM data across the IDE databus as the data flows between the microcontroller of the CD-ROM and the host computer. On system start-up, or during an error condition that requires re-initialization, the IDE bus uses the ATA bus signals DASP/HDASP (drive active/drive 1 present) and PDIAG/HPDIAG (passed diagnostics) to allow devices to identify their presence on the bus and to perform diagnostic testing. Once diagnostic testing is completed and all devices on the IDE bus pass, the IDE bus is ready for CD-ROM data transfers.

The transfer of data across an IDE bus is initiated when the host computer writes command data into the ATA command block registers. The ATA command block registers are a collection of eight registers that are used to pass CD-ROM drive command data from the host computer to the CD-ROM drive, and to pass status and data from the CD-ROM drive to the host computer. One of the more important command parameters is the drive selector bit (DRV), located in the drive/head register. By setting the DRV bit, the host computer selects which of the two drives connected to the ATA bus it intends to have execute the command. The host computer also writes a code identifying the particular command it wants the CD-ROM controller to execute into the command register. When the host computer writes to the command register, the ATA device identified by the DRV bit commences execution of the command specified by the command code placed in the command register and the command parameters stored in the other command block registers.

Before accessing and executing the parameters in the command block registers, the selected CD-ROM drive first sets the BSY (busy) bit. The BSY bit is a flag that indicates to the host that it may not write to the ATA command block registers because the selected drive is accessing these registers. While the BSY bit is asserted, the selected CD-ROM drive must retrieve the command data from the command block registers. The microcontroller of the CD-ROM interprets the command data and directs the drive electronics of the CD-ROM drive to begin the process of retrieving the requested data ftom the CD-ROM.

When the microcontroller has retrieved the data it needs to carry out the command from the ATA command block registers, it de-asserts the BSY flag to free up the IDE bus. After retrieving CD-ROM command data from the ATA registers and the multi-byte command FIFO (a first-in first-out data queue), the microcontroller must interpret this command data and instruct the drive electronics and the CD-ROM controller to implement the requested command. When the data stored on the CD-ROM has been retrieved and corrected and is ready for transfer to the host, the microcontroller accesses the ATA status register and sets bits in the register that identify whether the command was successfully executed and the data is ready for transfer to the host.

Once the command block registers have been properly initialized, the microcontroller sets the IRQ/HIRQ (host interrupt request line) signal to interrupt the host computer.

When the host computer receives this interrupt, it sets aside the task that it was performing and reads the ATA status register located within the CD-ROM controller. Once the host computer has determined from its review of the status register that data is available for transfer, it makes repeated reads from the data register in order to retrieve the data requested. The data is transferred from the RAM, where it was stored, into a data FIFO. The data FIFO buffers the flow of data from the RAM to the host. The data FIFO ensures that there is an uninterrupted supply of data that flows to the host. Once all of the data has been transferred, the CD-ROM microcontroller accesses a flag bit stored in the ATA status register to indicate to the host computer that there is no more data available and that transfer of CD-ROM data to the host computer is complete.

Whether the host interface means requires a "direct" connection to the IDE bus is one of the key claim construction issues presented, and the features that are included and excluded in the definition of this element are crucial to the analysis of patent validity. The direct connection requirement is also critical in determining the relevance of the prior art asserted by respondents against the '715 patent for validity purposes. If a "direct" connection to the IDE bus is optional (as respondents contend and the ID found), then the asserted prior art becomes very relevant for assessing the on-sale bar, anticipation, obviousness, and derivation validity defenses, as well as for respondents' allegation of inequitable conduct. If a direct connection to the IDE bus is required (as complainant Oak and the IAs contend), then the prior art becomes much less relevant and Oak's arguments for patent validity and enforceablity are strengthened.

While the ID made no specific finding that the host interface element is a means-plus-function element, the ID clearly treats it as such, including and excluding various features from the specification on the basis of whether they are "clearly linked" to the claimed functions. In its analysis of the host interface means, the ID identified three circuit structures that were required by the host interface means: a command FIFO, a status FIFO, and a configuration register. (ID at 41). The ID identified the functional blocks in the specification that were directly linked to the host interface and found four functional blocks were necessary to the host interface means (ID at 43,44; FF 145, 146, 150), *viz.*, the host control **44,** the output buffers **54**, the control and status registers **56**, and the data path controller **64.**

The ID then examined Figures 5a and 5b of the specification, which are described in the specification as a "the pin description of the host interface of an implementation of this invention" and "an address map of the host registers of an implementation of this invention," respectively ('715 patent, col. 3, lines 57-58, 59-60), and identified various bits of assorted registers that "must be supported."[16] The ID summarized the registers as those called for in Figs. 5a, 5b, and 7 of the '715 patent, as well as the various bits as the BSY, DRV, and SRST (soft reset bits). (ID at 51).

The ID rejected six structures proposed by Oak as being part of the host interface means. The most important of these was Oak's contention that the patent requires the host interface

---

[16] *See, e.g.,* ID at 49 (specific bits of ATA register, BSY, DRV, and SRST, must be supported by the host interface means to perform its function in the invention).

means to connect *directly* to the IDE bus. The ID cited language from the specification of the '715 patent to the effect that the host interface means "can" directly drive an IDE/ATA bus, and concluded that the specification therefore did not *require* that the means directly drive the IDE/ATA bus. (ID at 52).

All parties agree that the "host interface means" is a means-plus function claim element. The dispute among the parties is over what *specific structures* in the specification are included in the host interface. All parties agree that the following structures are adequately supported by the specification and should be deemed to be part of the host interface means of claim 1:

(1) host addressing signals that control which ATA register is being addressed;

(2) data bus signals;

(3) host computer control of control and initialization signals PDIAG, DASP, RESET (drive reset trigger), DIOR (drive I/O read), DIOW (drive I/O write));

(4) some of the eight ATA (AT attachment) command block registers;

(5) a DRV bit; and

(6) a SRST bit.

The following six structures are in dispute and were not included in the ID's claim construction of the host interface means:

(1) CD-ROM controller access to all eight ATA command block registers;

(2) direct connection of the CD-ROM controller to the IDE bus;

(3) a detailed implementation of the BSY bit flag;

(4) initialization and interrupt signals (HIRQ/INTRQ and microcontroller control of control signals DASP, PDIAG, and HIRQ);

(5) a multi-byte command packet FIFO for sufficient storage for multi-byte commands; and

(6) dedicated circuits to handle IDE control signals DASP, PDIAG, and HIRQ, and to clear HIRQ.

The main claim construction issue in dispute among the parties concerns the nature of the linkage required between the "host interface means" claim language and the "corresponding structure" in the specification. Respondents argue and the ID found that a direct linkage is required; the IAs and Oak argue that a "corresponding" link is all that is required. Oak and the IAs contend that the specification must be read in light of what the entire invention discloses and that the expert testimony (*i.e.*, extrinsic evidence) may be considered where there is some ambiguity in the specification. They argue that expert testimony interpreting the specification language clarifies how one of ordinary skill in the art would interpret the claims and the specification.

The ID and respondents cite *B. Braun Medical, Inc. v. Abbott Laboratories, 124 F.3d 1419* (Fed. Cir. 1997), as requiring a direct, clear link between the specification and a means-plus-function claim. The Federal Circuit stated in *Braun* that:

> Section 112, paragraph 6 states that a means-plus-function claim "shall be construed to cover the corresponding structure ... described in the specification." We hold that, pursuant to this provision, structure disclosed in the specification is "corresponding" structure only if the specification or prosecution history clearly links or <u>associates</u> that structure to the function recited in the claim. This duty to link or <u>associate</u> structure to function is the *quid pro quo* for the convenience of employing § 112, ¶ 6.[17]

[17] *Braun* at 1424 (citing *O.I. Corp. v. Tekmar Co.*, 115 F.3d 1576, 1583 (Fed. Cir.1997))(underline emphasis added, italic emphasis in original).

Respondents argue that a structure is only deemed to be "corresponding structure" under section 112, ¶6 if the structure is clearly linked or associated with the function recited in the claim. Based on this language in *Braun* and citing language in *Vitronics,*[18] respondents take issue with Oak's reliance on extrinsic evidence for claim construction.

Respondents contend that Oak's arguments for the limitations of a direct connection to the IDE/ATA bus, use of all eight ATA registers, and the other structures in dispute, are improperly based on extrinsic evidence and these arguments do not *directly* link claim language with corresponding structures in the specification. Oak, they assert, has improperly doubled the number of limitations of the host interface means, relying on the ATA specification, not on a direct, clear link with material set forth in the `715 specification. Respondents argue that *Vitronics* emphasized that a court should only consider extrinsic evidence such as "expert testimony, inventor testimony, dictionaries, and technical treatises and articles" in the event of "some genuine ambiguity in the claims." Id. at 1584.

The verb "associate" used in the above-quoted passage from *Braun* indicates to us that an explicit linkage is not always necessary to show that a feature is a "corresponding structure." As *Vitronics* clearly states, a court should only consider extrinsic evidence, such as "expert testimony, inventor testimony, dictionaries, and technical treatises and articles" in the event of "some genuine ambiguity in the claims." Id. at 1584. In construing the host interface means

---

[18] "In those cases where the public record unambiguously describes the scope of the patented invention, reliance on any extrinsic evidence is improper." *Vitronics Corp. v. Conceptronic Inc.*, 90 F.3d 1576 (Fed. Cir. 1996).

element of claim 1, there is, in our view, a "genuine ambiguity" regarding the linkage between the "host interface means" claim term and the corresponding structure in the specification, as evidenced by the copious amount of argumentation devoted to construing the host interface means by the parties. We find the specification language discussing each of the six structures in dispute, supplemented by the testimony of complainant's expert (Wedig) and the ATA specification, instructive in construing the host interface means to include the six structures in dispute. The ATA specification is referred to frequently in the specification. The CD-ROM controller disclosed in the '715 patent is referred to "as integrated drive electronics with an AT attachment interface, or IDE/ATA." The ATA specification is an industry standard method of connecting a host computer to an IDE hard drive and it is well known to those knowledgeable in the art of designing peripheral devices for computers.[19] We thus find nothing improper in complainant's expert (Wedig) basing his claim construction on the '715 specification and reference to the ATA specification. The '715 patent is a type of patent that is often characterized as an "architecture patent," meaning that the description is in terms of a block diagram, with lower level circuit schematics and specific hardware references omitted. Such patents rely heavily upon the hypothetical person of ordinary skill in the art to supply knowledge regarding implementation that is described in the specification.

We construe the host interface means along the lines suggested by complainant's expert (Wedig) and find the following structures are part of the host interface means of the '715 patent:

---

[19] Tutorial Tr. at 19, 58 and Wedig Tr. at 438-39.

(1) *All ATA command block registers and complete access of the CD-ROM controller to the command block registers.*[20]

All eight ATA command block registers identified in the ATA specification[21] are disclosed in the '715 specification in Figure 2 ("IDE Reg. 54") and Figure 5b.[22] There is no indication anywhere in the `715 patent that the host interface means can be met by a controller having fewer than all of the disclosed ATA registers. We agree with the IAs that it is not enough that the ATA registers are available, they must also be able to communicate over the IDE bus. Only by supporting all eight registers can the CD-ROM controller be used with *any* IDE-based command set, including the ATA and ATAPI protocols.[23]

(2) *Direct connection of the '715 controller to the IDE bus.*

The '715 patent states (at col. 6, lines 60-62) that "the output buffers 54 of the invention can directly drive the IDE bus," and (at col. 7, lines 51-52) that "the drive controller can drive IDE interface signal lines directly." The ID found that the word "can" means that a direct connection to the IDE bus is optional. However, we agree with the IAs that the word "can"

---

[20] *See* `715 patent, Fig. 5(b), and col. 7, lines 58-61. *See also* CX-127, ATA Spec. at 15; Wedig Tr. at 464-68

[21] CX-2 at Fig. 5b.

[22] CX-2 at Fig. 5b, CX-127 at 1039DOC00013.

[23] A protocol is an agreed upon procedure for peripheral devices to communicate with a host computer.

means "to be able to do, make or accomplish."[24] We find that these two sections of the '715 specification, taken together with the preamble, other sections of the specification, the prosecution history, and testimony at the hearing, disclose a host interface with a *direct* connection to an IDE bus.

The preamble to claim 1 states that the invention is a "compact disk drive controller to control the communication of data between a compact disk in a compact disk drive and a host computer via an IDE/ATA data bus ... ." ('715 patent, col. 28, lines 64-66). Fig. 2 includes a block diagram that identifies a Host Controller 44 and an IDE Registers 54 and shows a direct connection to the IDE data bus with no intervening circuitry.[25] ('715 patent, col. 2, lines 66 - end and col. 3, lines 1-7). The specification further explains that "[t]he term IDE/ATA applies to a drive if and only if its interface conforms to the industry standard AT attachment specification" published by the American National Standards ('715 patent, col. 2, lines 23-31). The specification clearly identifies the purpose of the claimed controller as follows:

> Therefore, the controller **10** of the present invention communicates corrected command data, status signals, and other corrected data over the IDE bus **16** of the host computer, *eliminating the need for a host adapter card or additional ISA bus interface electronics*, to reduce the cost of the CD drive **14**. ('715 patent, col. 7, lines 28-33). (emphasis added).

The original title of the '715 patent was an "IDE/ATA CD Drive Controller," and testimony at the hearing indicated that the primary commercial motivation for developing an IDE CD-ROM

---

[24] Webster's Ninth Collegiate Dictionary at 158 (1993).
[25] Fig. 2 is the only figure in the '715 patent depicting the overall invention. This patent is an architecture patent and figure 2, depicting the overall invention, would show any intervening circuitry, if any was required or contemplated.

controller that could be directly connected to an IDE bus was to eliminate the cost and other problems associated with the indirect connection of the controller through a host adapter card to an ISA (industry standard architecture) bus. (Wedig Tr. at 463-64).

Respondents assert that the doctrine of claim differentiation lends further support to the ID's finding that the host interface means of claim 1 does not require a direct connection to the IDE. Respondents argue that claim 8 includes a direct connection limitation for the host interface means and hence claim 1 should not be construed to include a direct connection limitation. Respondents' Response to Oak's Written Submissions on Commission Review of ID pp. 44-45. However, claim 8, which depends from claim 1, adds the additional element of a "memory control means" to claim 1 and does not modify the host interface means. ("The compact disk controller of claim 1 further compromising a memory control means ... .") Additionally, the language cited by respondents at the end of this claim is found in a "whereby" clause. A "whereby" clause is a statement of result and cannot, by itself, impart patentability. *In re Boileau*, 163 F.2d 562 (C.C.P.A. 1947) When terms appearing in a whereby clause are emphasized as being effective for distinguishing over the prior art and in securing the allowance of that claim during the prosecution of the patent, then those terms may be deemed as an essential feature necessary to the establishment of infringement. *Eltech Systems Corp. v. PPG Industries Inc.*, 710 F. Supp. 622, 633, 11 USPQ2d 1174, 1183 (W.D. La. 1988), aff'd, 903 F.2d 805, 14 USPQ2d 1965 (Fed. Cir. 1990). However, we find that the whereby clause of claim 8 of the '715 patent merely states the result of the limitations and structures already recited in the claim and adds nothing to the patentability of the substance of the claim. Additionally, since claim 8 depends from claim 1, the whereby clause at the end of claim 8, which reads "said host interface means for transferring said data ... without requiring the use of additional interface electronics between said compact disk drive and said host computer," is further evidence that the intent of claim 1 was a direct connection to the IDE bus.

(3) *Oak's detailed implementation of the BSY bit flag.*[26]

Respondents argue that because the BSY bit shown in the status register of Figure 75 is shown as permanently set to a `0,' that implementation should be the only implementation allowed for the BSY bit. However, a fully functioning BSY bit is disclosed in the specification.[27] We also find that the "R/W" designation in the figures, including Figure 75, would be interpreted by one of ordinary skill in the art as meaning that the register and all its bits can be both read ("R") and written ("W").[28] Additionally, the very purpose of a "BSY" bit is to indicate a busy or not-busy state and disclosure of permanently '0' state is inconsistent with this purpose.

(4) *Initialization and interrupt signals (HIRQ/INTRQ, DASP, and PDIAG).*

The purpose of the HIRQ/INTRQ signal is to interrupt the host computer and indicate that the CD-ROM drive is ready to transmit data. Respondents argue that because software running on the host computer can disable the host interrupt request line (HIRQ/INTRQ) of an

---

[26] BSY Bit in Status Register, `715 patent at Fig. 5(b). *See also* CX-127, ATA Spec. at 19; Wedig Tr. at 470-72. Dedicated Circuitry to Set BSY Bit, `715 patent at col. 22, lines 5-9. Wedig Tr. at 492-94.

[27] `715 patent, Fig. 75, and col. 27, lines 20-25, col. 28, lines 17-20

[28] Wedig Tr. at 2484-2485.

IDE peripheral, the host interrupt request is optional and therefore not a necessary structure for transmitting data to the host computer. We find this argument unpersuasive in view of the language in the specification describing the host interrupt signal and the overall thrust of the specification that discloses an invention capable of driving the IDE bus.

The host computer may be able to disable the host interrupt signal and thereby disable communication on the IDE databus. However, when the host computer communicates over the IDE databus, the host interrupt request (HIRQ,/INTRQ) must be enabled as set forth in the ATA specification and in the '715 patent. We find the description of the host interrupt in Figure 5a, "HOST INTERRUPT - This signal is used to interrupt the host system," to be a sufficient linkage to the claimed function of communicating "data between a compact disk in a compact disk drive and a host computer via an IDE/ATA data bus ... [and] transmit[ing] corrected data to the host computer."[29] Without this capability to interrupt the host computer, the controller of the '715 patent would not be able to operate over the IDE bus.

Similarly, we find a sufficient description of the operation of the DASP and PDAIG signals in the specification (CX-2 at col. 21, lines 31-55). The DASP and PDIAG signals indicate that two drives are on the IDE databus and that both drives have passed diagnostics and are running properly. These signals are fully described in the specification, they are tied to the ATAPI and ATA specifications,[30] and they are clearly linked to the claimed function of

---

[29] `715 patent, col. 28, lines 64-66; col. 29, line 20.

[30] PDIAG is "set following the timing in ATAPI and ATA specification," '715 patent, col. 21,
(continued...)

communicating "data between a compact disk in a compact disk drive and a host computer via an IDE/ATA data bus ... [and] transmit[ing] corrected data to the host computer."

(5) *a FIFO (sufficient storage for multi-btye commands).*[31]

The ID did not include a multi-byte command packet FIFO in its construction of the host interface means. The ID based this conclusion on the following language in the specification: "[t]he command FIFO register COMIN is used to direct the host interface by the host computer."[32] The ID noted that claim 1 of the '715 patent operates only in the IDE mode and that IDE mode does not support COMIN. It therefore found that no FIFO was directly linked to the host interface. However, the specification also states that "[t]he host interface contains a 12 byte command packet FIFO and IDE regs."[33] This statement is sufficient connection between the host interface means and a 12 byte command packet FIFO to ensure the "uninterrupted flow of data from said controller to said host computer."[34]

(6) *Dedicated circuits to handle IDE control signals DASP, PDIAG, and HIRQ, and to*

---

30 (...continued)
lines 37-38, 51-51.

31 `715 patent, col. 7, lines 52-53, and Wedig Tr. at 472-75.

32 `715 patent, col. 8, lines 4-6.

33 '715 patent, col. 7, lines 51-53.

34 The quoted language is the last phrase in the host interface means element of claim 1 of the '715 patent.

clear HIRQ.[35]

We agree with the IAs that the '715 specification (at col. 21, lines 32-38) teaches that "PDIAGEN is automatically cleared to 0," by SRST. (PDIAGEN, or pin HPDIAG, is a bit in a microcontroller register that sets the HPDIAG/PDIAG signal.) The '715 specification also teaches (at col. 21, lines 44-50) that "DASPEN is automatically cleared to 0, clearing pin HDASP- to high-impedance by ... ATA Soft Reset (SRST)" and that "HINTRQ is automatically cleared to 0." (DAPSEN, or pin HDASP, is a bit in a microcontroller register that sets the HDASP/PDIAG signal. HINTRQ, host interrupt register, sets the IRQ/HIRQ signal.) Although a special dedicated circuit to implement this automatic setting is not explicitly mentioned in the '715 specification, we find credible the testimony of complainant's expert (Wedig) that the specification language would be interpreted by those knowledgeable in the art as teaching the use of "specialized hardware to perform automatic clearing of that bit."[36]

In conclusion, we find that the claims, the specification, the prosecution history of the '715 patent, and the hearing testimony, require a construction of the "host interface means" that entails a direct connection to the IDE bus, and that the "host interface means" should be constructed to include the associated ATA specification registers and signals disclosed in the '715 patent specification to carry out that direct connection.

We find that the corresponding structures of the '715 host interface means are the following:

---

[35] *See* '715 patent at col. 21, lines 34-37, 46-49; col. 26, lines 67-27:5; and Wedig Tr. at 494-96.
[36] Wedig Tr. at 495

(1) direct connection of the '715 controller to the IDE bus;

(2) all eight ATA command block registers and complete access to the command block registers by the CD-ROM controller;

(3) a fully functioning BSY bit;

4) microcontroller control of the initialization and interrupt signals (HIRQ and INTRQ, DASP, PDIAG, and HIRQ);

(5) a FIFO with sufficient storage for ATAPI multi-bye commands;

(6) dedicated circuits to handle IDE control signals DASP, PDIAG, and HIRQ, and to clear HIRQ;

(7) host addressing signals which control which ATA register is being addressed;

(8) ATA data bus signals;

(9) host computer control of control and initialization signals (PDIAG, DASP, RESET, DIOR, DIOW);

(10) a DRV bit; and

(11) a SRST bit.

C. Domestic Industry

Section 337 requires, as a condition of relief, that a domestic industry exists that exploits the patent at issue.[37] Satisfying any of the three statutory criteria establishes the requisite

---

[37] The pertinent statutory language is as follows:

> (2) [The prohibitions of the statute] apply only if an industry in the United States, relating to the articles protected by the patent, copyright, [registered] trademark, or mask work concerned, exists or is in the process of being established.
>
> (3) For purposes of paragraph (2), an industry in the United States shall be

(continued...)

domestic industry.[38]

The domestic industry requirement is written in the present tense and, therefore, requires that a domestic industry either currently exist or be in the process of being established. The date for determining whether an industry exists is the filing date of the complaint.[39]

The statutory domestic industry requirement has two prongs: the technical prong and the economic prong. The former requirement is that the patent claims cover the articles of manufacture relied on to establish the domestic industry, *i.e.*, that the complainant be practicing its own patent(s). The latter requirement is that one or more of the economic activities specified in section 337(a)(3)(A)-(C) be taking place with respect to the articles identified by the technical prong.

---

[37] (...continued)

> considered to exist if there is in the United States, with respect to the articles protected by the patent, copyright, trademark, or mask work concerned --
>
> (A) significant investment in plant and equipment;
>
> (B) significant employment of labor or capital; or
>
> (C) substantial investment in its exploitation, including engineering, research and development, or licensing.

19 U.S.C. § 1337(a)(2-3).

[38] *Certain Integrated Circuit Telecommunications Chips and Products Containing Same, Including Dialing Apparatus*, Inv. No. 337-TA-337, USITC Pub. 2670, Initial Determination at 94 (Aug. 1993).

[39] *Texas Instruments v. United States International Trade Commission*, 988 F.2d 1165, 1181 (Fed. Cir. 1993); *Bally/Midway Mfg. Co. v. United States International Trade Commission,* 714 F.2d 1117, 1121 (Fed. Cir. 1983).

The ID noted that the economic prong of the domestic industry requirement was not contested with respect to the amount of investment that Oak has made domestically, and found the economic prong satisfied.[40] We agree.

Respondents argued that the technical prong was not satisfied based on (1) their construction of claim 1 as covering only a dual mode IDE/ISA device (*i.e.*, Oak's product is not a dual mode CD-ROM controller), and (2) their contention that Oak's product does not satisfy the "memory means" element of independent claim 1.

The ID found that claim 1 reads on an IDE device, and does not require dual mode functionality. Thus, the ID found that it is not necessary for Oak's devices to have a dual mode functionality in order to practice the '715 patent. With respect to the memory means, the ID found that it was not possible to determine whether Oak's product satisfies that element in claim 1 since it found that element indefinite under 35 U.S.C. §112, ¶ 2 and ¶ 6. However, the ID found that Oak practices claim 9 of the '715 patent and therefore satisfies the domestic industry requirement of section 337 (claim 9 is a dependent claim, dependent on claim 1, and recites a DRAM for the memory means).

We agree with the ID's conclusion on the domestic industry requirement. As noted, respondents make two arguments concerning whether Oak practices the claims of the '715 patent: (1) claim 1 of the '715 patent covers a dual mode (IDE and ISA) CD-ROM controller and Oak's OTI-011 controller is not a dual mode controller, and (2) because the '715 patent specification allegedly does not disclose a structure capable of carrying out the claimed memory

---

[40] ID at 177.

means of the patent and therefore it is not possible to determine whether Oak's OTI-011 controller satisfies claim 1 of the '715 patent.

As to the first issue, we agree with the ID that the preamble of claim 1, which states that the invention is "[a] compact disk drive controller to control communication of data ... via an IDE/ATA bus," clearly refers to on an IDE-only controller. Although the ISA mode is mentioned in the specification, only the IDE/ATA mode is claimed. Therefore, the invention covered by the '715 patent is IDE-only, and since Oak's OTI-011 controller is an IDE-only CD-ROM controller, Oak practices its own patent.

As to the contention that Oak's product does not satisfy the "memory means" element of independent claim 1, we agree with the ID that Oak's product uses a random access memory as required by claim 9. Moreover, based on our claim construction of claim 1, we find the OTI-011 CD-ROM controller, which requires a RAM or DRAM "memory means," is covered by independent claim 1 as well as dependent claim 9.

In summary, we affirm the ID's finding that a domestic industry exists in this investigation. Specifically, we find that all claims at issue are valid and that Oak practices its own patent with its OTI-011 CD-ROM controller.

D. <u>Literal Infringement</u>

After the scope of the claim has been determined, the next step in an infringement analysis is to compare the claim, as properly interpreted, with the accused device to determine whether that device is within the scope of the claim, *i.e.*, whether the device infringes the claim.[41] Proof of literal infringement requires a finding that each and every claim limitation in the accused product.[42]

The only element in dispute in alleged infringement of the '715 patent by the MediaTek CD-ROM controller is the "cyclic redundancy checker for detecting errors in said assembled data after correction of said data." We have construed the "cyclic redundancy checker for detecting errors in said assembled data after correction of said data" language of claim 1 as follows: a cyclic redundancy check on the entire CD-ROM block of "assembled data" *after* the correction of that CD-ROM block by Reed-Solomon error correction.

As to the accused product, the MediaTek device first performs an error detection by a cyclic redundancy check on the entire CD-ROM block of data (generating an original CRC remainder), followed by Reed-Solomon error correction, followed by a second error detection. This second error detection is an update to the original CRC remainder with 20 bits of error location and error pattern data from the Reed-Solomon error correction operation. In this second error detection operation, the original CRC remainder is decremented until it equals zero, indicating that all errors have now been corrected.

Thus, the issue is whether the second error detection operation of the MediaTek controller is the same as the cyclic redundancy check after error correction of the '715 patent. We agree

---

[41] *Electro Medical Systems S.A. v. Cooper Life Sciences Inc.*, 34 F.3d 1048, 1053 (Fed. Cir. 1994). If the accused device is within the scope of the claim, the claim is said to "read on" the accused device.

[42] *Johnston v. IVAC Corp.*, 885 F.2d 1574, 1580 (Fed. Cir. 1989).

with the ID and find that it is not. The second MediaTek error detection operation computes the CRC of the error polynomial, formed from the Reed-Solomon error pattern, and adds that CRC to the previous CRC to arrive at the CRC of the newly corrected data. Luby, Tr. 1477-1478. The focus of the mathematics in this CRC remainder update is on the addition operation to *update* the 32 bit CRC remainder with 20 bits of Reed-Solomon error correction data.[43] This operation differs fundamentally from the '715 patent's CRC remainder generation by dividing a CRC generator polynomial into an entire block of CD-ROM data. The MediaTek controller's generation of a CRC remainder *before* error correction and the updating of that remainder *after* error correction is not the same as the '715 patent's cyclic redundancy check on the entire CD-ROM sector of data *after* error correction.

The second error detection step of the MediaTek CD-ROM controller calculates a

---

[43] The centrality of this addition operation in the CRC remainder update is demonstrated in the following testimony of complainant's expert (Luby) on cross examination:

Q So for each of these updating operations on the EDC remainder that takes place in the error detection processor, you have 20 bits of information about an error pattern and an error address that is used to update an EDC remainder that is only 32 bits long; right?

A Right. As I explained before, it's an incremental kind of rule. Each time it [the MediaTek controller] updates the CRC by taking whatever error patterns have been found, including the CRC, and adding to the previous CRC and getting new CRC for the corrected data.

Q So mathematically, that's what's happening; correct?

A It's a little more -- I described the process of what's going on and mathematically, that's an accurate description, yes.
Luby Tr. at 1480.

correction to the CRC remainder and iterates this correction to the CRC remainder until the remainder is zero:

> The present error detection processor incrementally tracks the corrections made to the error check remainder, *decrements* the remainder value by the corrections and determines when the error check remainder is reduced to zero. Thus, the remainder is fully corrected through the *subtraction* from the original error check remainder of one or more numbers, *the sum* of which are equal to the original error check remainder. (emphasis added). RX-386-C at M000188.[44]

Once the CRC remainder is determined to be zero, all Reed-Solomon error correction stops on that sector of CD-ROM data. The MediaTek patent application goes on to explain that "[b]y calculating a correction to the CRC remainder, the error detection logic does not have to divide the long binary number consisting of the bits of all the sector data protected by the EDC by the check polynomial to calculate the CRC remainder." (RX-386C at M000185). Thus, although the second error detection step of the MediaTek CD-ROM controller uses the initial CRC remainder, the mathematics of updating this remainder from the previous Reed-Solomon error correction step is very different from standard CRC calculations. The two circuits given for this CRC remainder update are given in RX-386C at page M000208, Figure 7, and at page M000209, Figure 9, and are referred to as a "correction calculation circuit" (RX-386C at M000192). The mathematics that drive the design of the "correction calculation circuit" circuit are very different from the standard, straightforward binary division operation of CRC linear feedback shift register, and the MediaTek circuitry used to update the CRC remainder is significantly more

---

[44] This is taken from respondents' patent application, RX- 386C at M000184, which fully describes the accused error detection and correction process.

complex than the standard CRC linear feedback shift register. (Blahut Tr. 1839)

The '715 patent processes an entire block or sector of CD-ROM data in a clear sequential and temporal relationship:[45]

> (1) The digital signal processor interface descrambles and assembles data from the DSP 28, then stores that CD-ROM data in RAM;
>
> (2) The error correction circuitry *first* performs a Reed-Solomon error correction on each block of CD-ROM data; and
>
> (3) *Then*, a cyclic redundancy check *of the corrected block of data* is performed.[46]

By contrast, the MediaTek CD-ROM controller performs a complicated series of simultaneous events that we believe is a significant improvement over the standard Reed-Solomon and cyclic redundancy check disclosed in the '715 patent. The MediaTek sequence is as follows:

> (1) Read a sector of CD-ROM data from the CD-ROM into external RAM and into the CD ROM controller, and as the data is read into the CD-ROM controller *do an initial and standard CRC* with linear feedback registers;[47]
>
> (2) Store the initial CRC remainder to RAM with the CD-ROM sector of data;[48]
>
> (3) Start Reed-Solomon EDC on the data in RAM and simultaneously pass the initial

---

[45] ID at 29.

[46] CX-1/RX-1 ('715 patent), col. 6, lines 25-27, 30-39 (emphasis added).

[47] Blahut Tr. at 1833-4; Luby Tr. at 1472-73, 1485; RX-387 at M000003.

[48] Blahut Tr. at 1833-4; Luby Tr. at 1841-43; RX-287C; RPX-1C/RPX-2C.

CRC remainder to the "Error Detection Processor;"[49]

(4) Each time the Reed-Solomon decoder finds and corrects errors in the data, the 32-bit CRC Remainder is updated using a 20-bit code word containing the error location and error pattern from the Reed-Solomon error correction operation;[50] and

> (A) While sending the 20-bit code word data to the Error Detection Processor to update the CRC remainder, the CD-ROM controller also retrieves the erroneous byte from RAM, corrects it, and sends it back to RAM;[51]
>
> (B) While this read/write operation is taking place, the Reed-Solomon decoder begins processing the next codeword from DRAM and begins checking for errors, but before it reads the next codeword the decoder checks to see if the updated CRC remainder is zero;[52]
>
> (C) If the CRC remainder is not equal to zero, another CRC code word is read and error correction continues and this process continues until all corrected data have a non-zero CRCs (corrects only those words flagged by the initial CRC check);[53]
>
> (D) If the CRC remainder is zero, no further Reed-Solomon error correction is performed on that sector of CD-ROM data and the sector is passed onto the host computer.

Oak asserts that the only requirement of the error detection element of the '715 patent is that the error detection be completed after error correction is completed. Oak argues that the MediaTek controller's amending the CRC remainder after error correction and checking to see if that remainder is equal to zero, is the same as the claimed error detection after correction of the

---

[49] Chuang Tr. at 1588-89, 1593-95; Blahut Tr. at 1845; RX-287C; RPX-1C/RPX-2C, Slide 4.

[50] Chuang Tr. at 1589, 1593-98; Blahut Tr. at 1834; RX-287C; RPX-27C; RPX-387C.

[51] Chuang Tr. at 1595-97; Blahut Tr. at 1843-44; RPX-27C; RPX-1C/RPX-2C, Slide 5.

[52] Chuang Tr. at 1590; Blahut Tr. at 1853; RPX-387C.

[53] Chuang Tr. at 1590; Blahut Tr. at 1835; RPX-387C.

'715 patent. The ID, Oak asserts, improperly construed claim 1 of the '715 patent to specify a particular order in which the error detection and correction operations must be initiated. Oak submits that the fact that error detection is initiated *before* correction in the MediaTek controller does not place that controller outside the scope of the claim, since error detection in the MediaTek controller also occurs *after* correction in satisfaction of the claim.

We do not find this argument persuasive in light of the clear limitation of the claim language: "a cyclic redundancy checker for detecting errors in said assembled data *after* correction of said data." The claimed cyclic redundancy checker is defined in the specification as "commonly available as hardware used in many other applications."[54] As we have noted previously, these words indicate that the technical term "cyclic redundancy checker" refers to the common or conventional usage of the term, *viz.*, to the division of a generator polynomial into a data block to produce a cyclic redundancy check remainder.[55] Oak does not dispute that the error detection and correction means of the '715 patent were not novel and were present in prior art controllers.[56]

Additionally, as the ID found, the word "after" is an express limitation of claim 1 of the '715 patent. Claim 1 and the specification nowhere indicates the generation of the CRC

---

[54] '715 patent, col. 6, lines 41-43.

[55] RX-490, Encyclopedia of Computer Science, pp. 382-303.

[56] "Oak has not disputed that the DSP interface, error detection and correction means, and memory elements of Claim 1 of the '715 patent were present in the prior art CD-ROM controllers. Rather, it is the combination of those known elements together with the host interface means of the '715 patent that is novel." Oak's Post-Hearing Brief, p. 2.

remainder *before* error correction and the updating of that remainder *after* error correction, as is performed in the MediaTek controller. The error detection element of the '715 patent claims the straightforward, sequential relationship of performing conventional CRC remainder generation on an entire block of CD-ROM data "after" error correction. The specification supports this construction:

> "The error correction circuitry *first* performs a Reed-Solomon error correction on each block of CD-ROM data. *Then*, a cyclic redundancy check *of the corrected block of data* is performed.[57] (the '715 patent, col. 6, lines 30-32). (emphasis added).

Therefore, we affirm the ID that claim 1 of the '715 patent is expressly limited to CRC remainder generation on an entire block of CD-ROM data that occurs *after* error correction, and this mode of error detection is not literally infringed by the MediaTek controller, which involves CRC remainder generation *before* error correction and the updating of that remainder *after* error correction. For this reason, and because we find that the error detection after error correction in the MediaTek CD-ROM controller involves different binary mathematics, different circuitry, different data processed, and different processing steps, we find that the MediaTek CD-ROM controller does not literally infringe the '715 patent.

E. <u>Infringement Under the Doctrine Of Equivalents</u>

To show infringement under the doctrine of equivalents, Oak must show that there are insubstantial differences between the claims at issue and the MediaTek controller, or that the MediaTek controller performs substantially the same function in substantially the same way to

---

[57] '715 patent, col. 6, lines 25-27, 30-39 (emphasis added).

obtain substantially the same result as the patented controller. Known interchangeability between the claimed and accused elements is a significant factor bearing on the similarity or differences between an accused device and a claimed invention. *Warner-Jenkinson* v. *Hilton Davis Chemical*, 117 S. Ct. at 1040, 1053 (1997).

Oak argues that even if the ID's claim interpretation and literal infringement analysis are upheld, the accused devices infringe under the doctrine of equivalents. It contends that the ID found that the two operations are mathematically equivalent and that both devices execute a cyclic redundancy check.[58] Oak also contends that a person of ordinary skill in the art would view the MediaTek error detection circuitry as interchangeable with a typical linear feedback shift register, and notes that under *Warner-Jenkinson* known interchangeability is a significant indicator of equivalence.

The doctrine of equivalents issue in this investigation is whether the CRC operation after error correction of the '715 patent is substantially different from the second error detection operation of the MediaTek CD-ROM controller. We agree with the ID and find that it is.

The MediaTek controller's updates of the CRC remainder after error correction is not an equivalent mathematical operation to the CRC remainder generation on an entire CR-ROM data block of the '715 patent. The MediaTek controller computes a CRC from the error pattern of the previous Reed-Solomon error correction operation and updates the original CRC remainder with

[58] Oak cites FF 179 of the ID: "Mathematically, one would understand the process of updating the EDC remainder in the MediaTek devices to be another method of accomplishing the same task that is mathematically equivalent to cyclic redundancy checking error detection, yet one would not understand it to be what was intended by the meaning of the words cyclic redundancy error detection as described in the '715 patent." Blahut Tr. at 1836-1837.

this CRC in a binary *addition* operation. This is substantially different from the binary *long division* operation carried out on an entire block of CD-ROM data of the '715 patent's cyclic redundancy checker. Using the output of a division in an addition operation, as is done in the MediaTek controller, is not equivalent to performing the long division on an entire block of data, as is done in the '715 patent.

Moreover, the updating of a CRC remainder is not interchangeable with the generation of a CRC remainder. The MediaTek controller performs conventional CRC remainder generation *before* error correction and updates that remainder *after* error correction. This remainder generation, the same conventional CRC remainder generation as claimed in the '715 patent, is not interchangeable with the CRC remainder updates after error correction. The second error detection operation of the MediaTek controller, the updating of the initial CRC remainder, depends on the initial CRC remainder division and is not in any way interchangeable with it.

The doctrine of equivalents does not give a patentee a license to ignore or erase structural and functional limitations on which the public is entitled to rely in avoiding infringement. *Athletic Alternatives, Inc. v. Prince Mfg., Inc.*, 73 F.3d 1573, 1582. In *Sage Products, Inc. v. Devon Industries, Inc.*, 126 F.3d 1420 (Fed. Cir. 1997), the Federal Circuit considered a simple mechanical device for disposing of hazardous medical waste, and stated as follows:

> [T]he '728 patent claims a precise arrangement of structural elements that cooperate in a particular way to achieve a certain result. Devon [the accused product] achieves a similar result–restricted entry to a medical disposal container–but it does so by a different arrangement of elements .... If *Sage* desired broad patent protection for any container that performed a function similar to its claimed container, it could have sought claims with fewer structural encumbrances. ... Instead, Sage left the PTO with manifestly limited claims that it now seeks to expand through the doctrine of equivalents. However, as

> between the patentee who had a clear opportunity to negotiate broader claims but did not do so, and the public at large, it is the patentee who must bear the cost of its failure to seek protection for this foreseeable alteration of its claimed structure.

Sage at 1425.

The '715 patent claims a precise arrangement of functional elements: a "cyclic redundancy checker for detecting errors in said assembled data *after* correction of said data." In the MediaTek controller there is a parallel relationship between error detection and correction that is not encompassed by the straightforward *"after"* of claim 1 of the '715 patent. The CRC operation in the MediaTek controller is divided into a *before, during,* and *after* error detection, with the *during* and *after* portions of the CRC operation being the updating of the original CRC remainder. In the MediaTek controller, a conventional CRC division of the entire CD-ROM data block is performed and then Reed-Solomon error correction is initiated.

In parallel with this ongoing Reed-Solomon error correction operation, the remainder from the initial CRC operation is updated with the error location and pattern data from data from the last iteration of the Reed-Solomon error correction operation. This CRC remainder is then updated during the current Reed-Solomon iteration with the error location and error pattern data obtained in the previous Reed-Solomon iteration, forming the parallel *during* and *after* portions of error detection. The MediaTek controller obtains substantially the same result as the patented controller, the detection of errors after error correction, but it does not obtain that result in substantially the same way as the '715 patent. The MediaTek controller detects errors by a substantially different arrangement of functional elements, CRC remainder generation on an entire block of CD-ROM data *before* error correction and the updating of that remainder *during* and *after* error correction.

In conclusion, we find that following features of the '715 patent and the MediaTek CD-ROM controller are substantially different: (1) the binary mathematics (the division of a generator polynomial into an entire block of CR-ROM data versus computing a CRC from a Reed-Solomon error pattern and location data and adding this to the original CRC remainder), (2) the circuitry (a linear feedback shift register versus a binary adder), (3) the data processed (an entire 16,000 bit block of CD-ROM data versus a 32 bit CRC remainder and a 20 bit Reed-Solomon error syndrome containing the error pattern and location), and (4) the interrelationship between the error correction and detection operations (conventional CRC remainder generation *after* error correction versus conventional CRC remainder generation *before* error correction and then CRC remainder updates *during* and *after* error correction). We therefore affirm the ID and find that the MediaTek CD-ROM controller does not infringe the claims at issue of the '715 patent under the doctrine of equivalents.

Complainant asserts claims 1, 2, 3, 4, 5 and 9 of the '715 patent against respondents in this investigation. Claim 1 is an independent claim from which claims 2, 3, 4, 5, and 9 depend. If the accused devices do not infringe claim 1, either literally or by equivalents, they cannot infringe claims 2-5 and 9 of the patent.[59] We therefore find no infringement of claims 1-5 and 9 of the '715 patent.

F. <u>Validity</u>

The ID found that the '715 patent was invalid for on-sale bar under 35 U.S.C. § 102(b),

---

[59] *Wahpeton Canvas Company, Inc. v. Frontier, Inc.*, 870 F.2d 1546, 1552 n. 9 (Fed. Cir. 1989).

anticipation under 35 U.S.C. § 102(a), obviousness under 35 U.S.C. § 103, for indefiniteness under 35 U.S.C. § 112(2), (6), and for derivation under 35 U.S.C. § 102(f), and we determined to review each of those findings.

1. <u>On-Sale Bar</u>

An inventor is not entitled to a patent if the claimed invention was "on sale in this country, more than one year prior to the date of the application for the patent in the United States." 35 U.S.C § 102(b). "On sale" includes an offer for sale, even if the prospective sale is never consummated. Proof by clear and convincing evidence of such a sale or offer for sale with respect to the device claimed in an issued patent invalidates the patent.

The Supreme Court has held that an on-sale bar requires proof of two facts: (1) the product must be the subject of a commercial offer for sale, and (2) the invention must be ready for patenting. *Pfaff v. Wells Elec., Inc.*, 119 S.Ct. 304, 311-312 (1998).

The latter prong can be satisfied by either evidence of reduction to practice[60] or "proof that prior to the critical date *the inventor had prepared* drawings or other descriptions ... that were sufficiently specific to enable a person skilled in the art to practice the invention." *Pfaff* at 312. (emphasis added).

The filing date of the application that matured into the '715 patent is June 22, 1994. The first known embodiment of the invention claimed in the '715 patent was an Oak CD-ROM

---

[60] *Actual* reduction to practice is the physical construction of an apparatus that works for its intended purpose. *McCarthy's Desk Encyclopedia of Intellectual Property*, p. 278. C*onstructive* reduction to practice occurs on the date a patent application is filed. *Id.*

controller designated as the OTI-011. There is no dispute that there was an offer for sale of the OTI-011 to NEC Corporation over one year prior to the application date of the '715 patent.

While the ID found that there was no clear and convincing evidence of reduction to practice before the critical date (ID at 73), it did find clear and convincing evidence that the claimed invention was "ready for patenting" before the critical date. (ID at 74). The ID listed six documents,[62] two of which were not prepared by the inventors (the ATA specification and the ATAPI standard), that in its view provided strong evidence that the claimed invention was "ready for patenting" at the time of Oak's offer for sale of the OTI-011 to NEC, as that term was defined in *Pfaff*.

Additionally, the ID made a conditional finding that the Mitsumi prototype,[63] should the Commission find that this device anticipates the claimed invention, also leads to an on-sale bar. It noted that the activities of a third party may establish an on-sale bar as well as the activities of the

[62] These are (1) the ATA specification of February 10, 1992, which was cited to the PTO and is listed on the face of the '715 patent; (2) the Sanyo LC8950/51 Application Note for the LC8950/51 CD-ROM controller, which was cited to the PTO in part, but not in its entirety; (3) information concerning Oak's OTI-012 CD-ROM controller; (4) the ATAPI specification of June 10, 1993; (5) the Mitsumi prototype; and (6) U.S. Letters Patent 5,805,921 to Kikinis *et al.*, which issued on September 8, 1998, and which is based on a continuation of a later abandoned application filed on March 19, 1993.

[63] As discussed more fully in the next section of this opinion, Oak had pursued various joint development projects with Mitsumi Corporation. One of these joint projects was the development of a prototype to assess the feasibility of a CD-ROM controller to drive directly an IDE/ATA bus. Respondents contend that the resulting hardware, referred to as "the Mitsumi prototype," was anticipatory prior art.

inventor or his agents.[64] It went on to find that Mitsumi shipped its prototype to a number of companies before the '715 patent application date in order to encourage eventual purchase of a Mitsumi CD-ROM drive incorporating the prototype. (FF 12 at 255).

The issue before us is whether respondents have established by clear and convincing evidence that the invention disclosed in the '715 patent was "ready for patenting," as that term was defined by the Supreme Court in the *Pfaff* case, one year before the June 22, 1994, the filing date of the '715 patent.

We do not find that the collection of six documents satisfies the clear and convincing evidence standard for showing readiness to patent. The ID's piecing together of the claimed invention from these documents is very different from the facts of either *Pfaff* or *Weatherchem Corp. v. J. L. Clark Inc.*, 49 USPQ 2d 1001 (Fed. Cir. 1998). At most, these documents evidence a conception of the invention, not a "readiness for patenting" as contemplated in *Pfaff*. We do not read either *Pfaff* or *Weatherchem* to trigger the on-sale bar based on the point of conception where one *might* have patented a device.[65]

---

[64] *J.A. LaPorte, Inc. v. Norfolk Dredging Co.*, 787 F.2d 1577, 1581 (Fed. Cir. 1986), *cert. denied*, 479 U.S. 884 (1986); *In re Caveney*, 761 F.2d 671, 676 (Fed. Cir. 1985).

[65] Such a use of the doctrine of readiness for patenting in the context of an on-sale bar would in our view negatively impact patent practice on a widespread scale -- especially in the electronics industry. It is not unusual for electronics manufacturers to seek customer commitments to purchase a semiconductor, even before it is developed or the manufacturer is sure whether it can be developed. Electronics firms are not given to spending research and development funds in the hope that someone may wish to buy the resulting semiconductor product. If courts and the Commission were to examine laboratory notebooks and specifications with the aid of hindsight in search of the earliest possible point in time that the eventually-claimed device is discernible

(continued...)

In *Pfaff,* detailed engineering drawings enabled the manufacturer to develop the tooling to produce the patented device, a computer chip socket. Those drawings were prepared before the critical date, although the invention was not reduced to practice until much later.[66] The key in *Pfaff* was that the engineering drawings "were sufficiently specific to enable a person skilled in the art to practice the invention" and they "fully disclosed the invention."[67] In *Weatherchem*, also cited in the ID, a co-inventor testified that one of his drawings contained all the structural limitations of the claims.[68]

In this investigation, the nearest thing to a "drawing or other description" that contained all the structural limitations of the claims and that would enable one of ordinary skill in the art to practice the invention, was the tape-out of the OTI-011 chip that took place on July 22, 1993, a month *after* the critical date. Moreover, even this tape out was flawed and another was required on July 29, 1993.[69] We agree with Oak and the IAs that there is insufficient evidence in the record to invalidate the claims in issue of the '715 patent based on an on-sale bar under section 102(b).

---

[65] (...continued)
from a piecemeal analysis, prospective inventors would be forced to file patent applications any time they had a complete conception, and before they knew whether the concept would work. This practice would work at cross purposes to the statutory requirement that the specification provide an enabling disclosure of the invention.

[66] 119 S.Ct. at 307.

[67] 119 S.Ct. at 312.

[68] *Weatherchem Corp. v. J.L. Clark Inc.*, 49 USPQ 2d at 1007.

[69] Verinsky Tr. at 1036.

For the foregoing reasons, we believe that the ID's finding of an on-sale bar is erroneous and we therefore reverse it.

We also find that the offer for sale of the Mitsumi prototype in March 1993 was not an invalidating offer for sale. To be invalidating, the product offered for sale must contain each and every element of the claimed invention. As explained below, we do not believe that the Mitusmi prototype contained each and every element of the '715 patent claims at issue.

2. Other Invalidity Issues And Unenforceability

The evidence shows that since at least 1988 Oak has had an ongoing business relationship with Mitsumi Corporation. Teams of Oak and Mitsumi engineers worked together to create semiconductor products to be manufactured by Oak for use in Mitsumi products. Oak and Mitsumi cooperated to develop a CD-ROM controller, for use in a Mitsumi CD-ROM drive system, which used a similar Sanyo controller designated the LC8950/51.[70] This CD-ROM drive system utilized a proprietary bus interface, and the Oak controller was designated as the OTI-012.

Subsequently, Oak proposed to Mitsumi that a project be launched to design a controller to drive an IDE bus directly. Mitsumi began working on a prototype to demonstrate the feasibility of the idea. The prototype utilized the existing Mitsumi drive electronics, including the OTI-012 controller, and an intermediate electronics assembly (a "daughterboard"), which plugged into an ISA slot on the motherboard of the host computer. This daughterboard operated as an

[70] In order to facilitate Oak's design efforts, Mitsumi furnished a great deal of information on its existing controller, including a Sanyo application note on the operation of the LC8950/51 controller.

interface between the Mitsumi proprietary system and the IDE bus.

a) <u>Anticipation</u>

The ID found that the Mitsumi prototype anticipated the patented invention, thereby rendering the claims in issue of the '715 patent invalid under 35 U.S.C. § 102(a). It noted testimony from a Mitsumi engineer (Sugie) to the effect that Mitsumi intended to integrate the functionality of the daughterboard into the controller chip that it expected to emerge from the feasibility study (ID at 85). The ID quoted the Mitsumi engineer to the effect that the Oak OTI-011 had "the same functionality" as the Mitsumi daughterboard,[71] and stated that the Mitsumi schematics show the ATA command block registers, and utilize the DRV, BSY, and SRST bits. The ID concluded that the circuitry in the Mitsumi daughterboard is equivalent to the circuitry disclosed in the '715 patent.

The issue before us is whether the Mitsumi prototype is anticipatory prior art because it contained each and every claim element of the claimed host interface means. More specifically,

---

[71] The relevant testimony is as follows:

> Q. . . . Did you consider the OTI-011 to be an integrated version of Mitsumi's IDE CD-ROM daughterboard?
>
> A. No. If you're talking about circuitry, no.
>
> Q. The functionality?
>
> A. Functionality, yes. We would direct the Oak chip to have the same functionality.

Sugie Tr. at 755 (quoted in ID at 86).

the issue is whether the versions of the Mitsumi prototype in existence prior to April 21, 1993, incorporated the elements of an IDE host interface means as called for in claim 1 and later reduced to practice in the OTI-011.

The memorandum of February 19, 1993 (RX-47C), which Mitsumi's Akio Tanaka sent to co-inventor Verinsky, points out significant problems with Mitsumi's prototype and highlights the differences between what Mitsumi had accomplished and what should be incorporated in the IDE CD-ROM controller chip to be designed by Oak. That memorandum identifies characteristics of the Mitsumi prototype that differed from Verinsky's conception of the IDE CD-ROM controller of the '715 patent, including (1) the Mitsumi prototype translated between an IDE PC interface and a proprietary CD-ROM controller interface and did not have a direct connection to the IDE data bus, (2) the daughterboard of the prototype was not fully ATA compatible, (3) the daughterboard was only compatible with the Mitsumi proprietary interface, (4) the Mitsumi prototype had only the registers and bits used by the device driver, not all eight ATA command registers, (5) the prototype did not monitor bit 2 of register 3F7 for issuance of PDIAG to the master drive, and (6) the host PC cleared the BSY bit, a function performed by the CD-ROM according to the ATA specification.[72] These features of the Mitsumi prototype differ from the '715 patent. As late as April 20, 1993, Mr. Sugie, an employee of Mitsumi working on the prototype, wrote a letter to another Mitsumi employee on the status of the prototype, explaining that work was still needed to eliminate problems. The prototype was still being used to test an IDE CD-ROM because Oak's

---

[72] Verinsky Tr. at 1019-20, 1124-26, 1134-35; RX-47C; RX-31C, ATA Specification at 19.

OTI-O11 was not yet available.[73]

The record shows that Verinsky conceived of the CD-ROM controller disclosed in the '715 patent on or before April 21, 1993. That controller included (1) a direct interface with the IDE data bus, (2) support for all ATA command registers and a multi-byte command FIFO, (3) microcontroller access to all ATA command registers, and (4) dedicated circuitry for responding to high speed bus activity.[74] The first tape out of the controller for this CD-ROM drive took place on July 22, 1993, with a second tape out (to correct problems with the original tape out) taking place on July 29, 1993.[75] Thus, co-inventor Verinsky conceived of an IDE CD-ROM controller in March or April 1993, and this conception was reduced to practice in the form of manufacturing specifications on July 29, 1993. (Verinsky, Tr. at 1024-38).

Based on our claim construction of the host interface means, which requires a *direct* connection to the IDE bus, we reverse the ID's conclusion that the asserted claims of the '715 patent are invalid for anticipation by the Mitsumi prototype under 35 U.S.C. § 102(a). We find that the Mitsumi prototype contained a intermediary daughterboard that was only compatible with the Mitsumi proprietary interface and did not contain a direct connection to the IDE bus. Consequently, we find that respondents have failed to present clear and convincing evidence that the Mitsumi prototype anticipated all of the limitations of claim 1.

---

[73] Sugie Tr. at 928-30; RX-407.

[74] Verinsky Tr. at 1024-25 (CPX-167C).

[75] Verinsky Tr. at 1036; Brown, Tr. at 142.

b) Obviousness

The ID began its obviousness analysis by citing a recent Federal Circuit case for the proposition that the suggestion to combine references to render a patent invalid as obvious "may flow from the nature of the problem, from the teachings of pertinent references, or from the ordinary knowledge of those skilled in the art that certain references are of special importance."[76] The references asserted against the '715 patent by respondents and analyzed in the ID are as follows:

(1) The ATA specification of February 10, 1992, which was cited to the PTO and is listed on the face of the patent;

(2) The Sanyo LC8950/51 Application Note for a CD-ROM controller, which was cited to the PTO in part, but not in its entirety;

(3) Information concerning Oak's OTI-012 CD-ROM controller;

(4) The ATAPI specification of June 10, 1993;[77]

(5) The Mitsumi prototype; and

(6) U.S. Letters Patent 5,805,921 to Kikinis *et al.*, which issued on September 8, 1998, and which is based on a continuation of a later abandoned application filed on March 19, 1993.

The ID found the '715 patent invalid as obvious in the light of three distinct combinations of these prior art references:

---

[76] *In re Rouffert*, 149 F.3d 1350, 1355 (Fed. Cir. 1998).

[77] The ID found that the distribution (approximately 10 copies) and the relative lack of restrictions on the use made of the information qualified this document as a "publication." (ID at 111). The ID also emphasized that Western Digital Company, which created the draft specification, sought to "evangelize" the industry to accept it. (ID at 111).

(1) The ID found that the Oak OTI-012 CD-ROM controller chip in combination with either the February 1992 ATA specification, or the June 1993 ATAPI specification, would teach each and every limitation of the claims in issue of the '715 patent. The ID surveyed each of the 15 limitations for which Oak contends and outlined how each of them is purportedly found in one or another reference.

(2) When the Kikinis patent is added to the foregoing combination, the ID asserted that the suggestion to combine the OTI-012 and the ATA/ATAPI specifications is strengthened because Kikinis suggests the use of a CD-ROM drive on an IDE bus.

(3) The ID stated that the combination of the Mitsumi prototype and the February 10, 1992, ATA specification renders the claims in issue of the '715 patent obvious.

The ID considered the secondary indicia of nonobviousness, mentioning only the commercial success of the Oak controller. It stated, however, that this commercial success derived largely from information provided to Oak in the prior art references, and thus gave it less weight than it would otherwise be entitled to receive (ID at 130-131).

We find that respondents have failed to prove that the ATAPI specification qualifies as prior art. Without the ATAPI specification, none of the asserted combinations of prior art discloses the inventive host interface means of claim 1, as properly interpreted.

We first consider whether the ATAPI specification is prior art to the '715 patent. The ATAPI specification is dated June 10, 1993, and describes a detailed command set that enables communication between a CD-ROM drive and a host PC over an IDE bus. It also provides detailed information for the reduction to practice of such a controller. The '715 patent discusses the ATAPI commands in considerable detail and many of those commands are essential to the functioning of the claimed host interface means.

The question of whether the ATAPI specification qualifies as prior art depends upon whether it was in fact "published" before the critical date of June 22, 1993, one year before the application for the `715 patent was filed. Respondents argue that it was a publication because ten copies were distributed by Western Digital, whose employees authored the ATAPI specification, and respondents characterize this distribution as part of Western Digital's program to "evangelize" the IDE/ATAPI CD-ROM concept to the industry.[78] The number of copies distributed on that date is not dispositive. The courts have found a publication based on fewer copies and have found no publication when more copies were in limited circulation.[79] The evidence shows that only three companies besides Oak were provided copies of the June 10, 1993, ATAPI specification.[80] Western Digital confided in these insiders in the development of the proposed CD-ROM drive in order to obtain their approval and support before taking the proposal to a wider audience.[81] Thus, the distribution of the copies of the ATAPI specification on June 10, 1993, was a restricted

---

[78] Rutledge Tr. at 1664.

[79] *See In re Hall, supra* (*single* copy of catalogued doctoral dissertation in one university library sufficiently available to those interested in the art exercising reasonable diligence so as to bar patentability of reissue claim); *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 936-37 (Fed. Cir. 1990) (distribution of nonclassified report to *fifty* persons or organizations involved in military development project did not constitute publication where report was not generally available to anyone by exercise of reasonable diligence).

[80] RX-158C.

[81] Rutledge Tr. at 1659-61.

distribution. Moreover, each copy distributed bore a restrictive watermark legend on each page[82] and was printed on red paper to discourage photocopying.[83]

In *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 937 (Fed. Cir. 1990), the Federal Circuit found that a document is a printed publication for the purposes of patent invalidity if "anyone could have had access to the documents by the exercise of reasonable diligence." We agree with the IAs that the evidence concerning the controlled distribution of the ATAPI specification and the use of the restrictive watermark legend and the red paper to discourage photocopying supports a finding that the specification was not "published." The ATAPI specification was not available to anyone using reasonable diligence in the June 1993 time frame. We therefore reverse the ID's finding that the ATAPI specification is prior art.

We will now consider the various combinations of prior art found by the ID to render the `715 patent invalid as obvious.

(1) *The OTI-012 controller chip and ATA specification combined.*

The ID contains a detailed discussion of how the OTI-012 controller chip combined with the ATA specification provides, in the ID's view, all of the elements of the `715 patent's host interface means. ID at 118-29. The February 10, 1992, ATA specification set forth the commands needed for a hard disk drive to communicate with a host PC over an IDE bus. [84]

---

[82] *See* RX-84C.

[83] Rutledge Tr. at 1742.

[84] Buscaino Tr. at 2077; Wedig Tr. at 2453-54.

However, as noted, there must be some suggestion in the prior art to combine these references. As we have found that the ATAPI specification is not prior art, it is unavailable to provide the requisite suggestion. The combination of the OTI-012 and the ATA specification alone merely exemplified the state of the art when Oak's OTI-O11 project was commenced in late 1992. At that time, there were no controller chips that could directly connect a CD-ROM drive to a host PC through an IDE bus, and that was precisely the problem that Oak set out to solve. Combining the OTI-012 with the ATA specification does not solve the problem of directly driving the IDE bus. We therefore reverse the ID's finding that the combination of the OTI-012 and the ATA specification renders the claims at issue of the '715 patent obvious.

(2) *The OTI-O12 controller chip and the ATA specification combined with the Kikinis patent.*

The ID found that the Kikinis patent provides the suggestion to use a CD-ROM drive on the IDE/ATA bus, and thus to combine the OTI-012 and the ATA specification. ID at 129. However, the Kikinis patent teaches a translation between hard disk drive address formats and CD-ROM address formats performed by the microcontroller on a CD-ROM drive,[85] but does not teach anything about a direct connection of a CD-ROM controller to a IDE bus.[86] We therefore reverse the ID's finding that the combination of the Kikinis patent with the OTI-012 and ATA specification render the claims in issue of '715 patent obvious.

(3) *The Mitsumi prototype combined with the ATA specification.*

---

[85] CX-215; Buscaino Tr. at 2346-47.

[86] Buscaino Tr. at 2347-49.

As discussed previously, the Mitsumi prototype was a CD-ROM drive prototype that was designed to test the feasibility of using an IDE bus to connect a CD-ROM drive to a host PC. The Mitsumi prototype used an OTI-012 controller chip and a translator board to connect the CD-ROM indirectly to an IDE bus. The ATA specification fails to disclose the essential features of the claimed host interface means, as that means is properly construed. Specifically, it fails to disclose the direct connection of the controller to the IDE bus. We therefore reverse the ID's finding that the Mitsumi prototype combined with the ATA specification renders the claims in issue of the '715 patent obvious.

We also find that the so-called secondary considerations of nonobviousness strengthen the case for nonobviousness. Respondents' expert (Zech) testified that a solution to the problem of connecting a CD-ROM drive directly to an IDE bus was needed in the electronics industry since 1989, and prior to the invention of the controller of the '715 patent several companies tried but failed to use the IDE bus with a CD-ROM drive. Additionally, Oak has had sales of approximately [ ] dollars for the controller covered by the '715 patent. Thus, the long felt need for an IDE-compatible CD-ROM controller with a direct connection to the IDE bus and Oak's considerable commercial success with the controller of the '715 patent are significant secondary considerations of nonobviousness.

In summary, we find that the ID's various combinations of prior art fail to disclose the key inventive features of the host interface means of the `715 patent. We therefore reverse the ID's conclusion that the claims at issue of the '715 patent are invalid for obviousness.

c) Derivation

The patent statute states that a person is not entitled to a patent if "he did not himself invent the subject matter sought to be patented ... ."[87] The ID found that neither the named inventors nor anyone else at Oak invented the CD-ROM controller disclosed in the '715 patent. (ID at 132). Rather, it concluded that the subject matter of the patent was "derived" from the Mitsumi prototype and the June 1993 ATAPI specification.

We find that respondents have not provided clear and convincing evidence that the listed co-inventors of the '715 patent, Verinsky and Case, did not themselves invent the subject matter of the `715 patent. "To show derivation, the party asserting invalidity must prove both prior *conception* by another and communication of that *conception* to the patentee."[88] Conception, in turn, requires the presence of all the claimed elements.[89] The ID concluded that the ATAPI specification was "someone else's prior conception of a substantial amount of subject matter that was communicated to Oak." However, the record establishes that Verinsky conceived of his invention no later than April 21, 1993, Verinsky Tr. 1024-25, and the date of the ATAPI specification is June 10, 1993. There is no evidence that the ATAPI specification or any earlier version of it was communicated to Oak before the April 21, 1993, conception date. The '715 patent cannot be derived, in whole or in part, from the ATAPI specification when evidence of the conception date for the claimed invention places that conception nearly two months prior to even

---

[87] 35 U.S.C. § 102(f).

[88] *Gambro Lundia,* 110 F.3d at 1576.

[89] *Coleman v. Dines*, 754 F.2d 353, 359 (Fed. Cir. 1985).

the limited distribution of the ATAPI specification.[90]

Moreover, although the ATAPI specification describes a command set and other information that contributed to the reduction to practice of the host interface means of claim 1, the ATAPI specification does not describe all of the elements of the '715 patent's IDE CD-ROM controller, such as, for example, the digital signal processor interface. The ATAPI specification was delivered to Oak well after Verinsky's April 1993 conception of the invention of the `715 patent. Although the ATAPI specification was used by Oak in reducing the invention to practice, it did not contribute to the conception of the invention.

The ID also found that because Oak was provided with information regarding the Mitsumi prototype and was given a copy of the ATAPI specification, Verinsky and Case did not invent the CD-ROM controller of the '715 patent.[91] However, as discussed above, the Mitsumi prototype does not contain all the properly construed claim elements of the claims at issue of the `715 patent. Specifically, it does not contain a host interface means capable of directly driving the IDE bus. We therefore find that respondents have failed to show by clear and convincing evidence that the inventors of the '715 patent derived their invention from the Mitsumi prototype or from the ATAPI specification, and we reverse the ID's finding that the claims in issue of the '715

---

[90] Since the ATAPI specification was a candidate to establish an industry protocol for communication between host computers and CD-ROM drivers over the IDE/ATA bus, it is not surprising that the inventors of the '715 patent altered their patent specification and design to conform to it. The copying of certain information from the ATAPI specification into the disclosure of the '715 patent does not, without more, demonstrate that someone other than the named inventors conceived the entire invention claimed in the '715 patent.

[91] ID at 132.

patent are invalid for derivation under 35 U.S.C. § 102(f).

d) Indefiniteness and Vagueness

A patent may be held invalid for indefiniteness and vagueness as a result of failure to comply with the requirements of 35 U.S.C. § 112, ¶ 1 and ¶ 2.

The ID addressed four issues under 35 U.S.C. § 112, *viz.*, (1) alleged invalidity under § 112, ¶ 2 and ¶ 6 because the specification does not specifically identify structures for performing the "host interface means;" (2) alleged invalidity under § 112, ¶ 2 and ¶ 6 because the specification does not specifically identify structures for performing the "memory means;" (3) alleged invalidity under § 112, ¶ 1 because the specification does not provide a written description of a controller that includes a "memory means for temporarily storing data;" and (4) alleged invalidity under §112, ¶ 1 for failure to include essential material necessary to describe and enable the claimed invention.

The ID found that the '715 patent was not invalid under § 112, ¶ 6 and ¶ 2 for failure to identify in the specification structures for performing the "host interface means," and not invalid under §112, ¶ 1 for failure to include essential material necessary to describe and enable the claimed invention.

The ID found that the '715 patent is invalid as indefinite under § 112, ¶ 2 and ¶ 6. Having found that the "memory means" element is a means-plus-function element, the ID referred to the specification to determine the appropriate construction of this element. As mentioned previously, means-plus-function elements are construed to cover the structure(s) disclosed in the specification and their equivalents. In the specification, the ID was confronted with the fact that the dotted lines purporting to encompass the claimed controller in both Figures 1 and 2 of the specification appear to indicate that the DRAM is not a part of the claimed controller, but rather is an external device. Certain textual passages in the specification tend to support the same conclusion.[92] Aside from the DRAM, however, the ID found that the specification discloses no memory device capable of performing the claimed storage function. It concluded that this inconsistency between the claims and specification invalidated the claims at issue as indefinite.

Based on the same facts, the ID also found that the '715 patent is invalid for failure to provide an adequate written description under § 112, ¶1. Since the "memory means" element was added by amendment during the prosecution of the patent before the PTO (because the claims initially submitted with the application claimed a controller that did *not* include a memory means), the ID concluded that the specification and prosecution history indicate that the inventors were *not* in possession of the claimed invention, including a DRAM, at the time the original application was filed.[93]

We will address the four issues raised under 35 U.S.C. § 112 in turn:

(1) *Alleged invalidity of the "host interface means" under § 112, ¶ 6 and ¶ 2.*

The ID noted that complainant Oak's interpretation of the "host interface means" element has shifted during the course of the litigation. ID at 142. Although this shifting has caused some

---

[92] '715 patent, col. 3, lines 14-18; col. 6, lines 14-16; col. 6, lines 25-32; col. 6, lines 41-4; col. 7, lines 1-19.

[93] *Ex parte Grasselli*, 231 USPQ 395 (Bd. Pat. App. & Inter. 1983)(amendment to avoid prior art rejection not supported by original specification); M.P.E.P. (Manual of Patent Examining Procedure) ¶ 2163.05 (amendments introducing elements or limitations not supported by original specification are violations of written description requirement of 35 U.S.C. § 112, ¶1).

confusion as to what structures in the specification are linked to this claim element, we agree with the ID that in view of the clear and convincing evidence required to prove patent invalidity, there is not sufficient evidence to find that the asserted claims of the '715 patent are invalid, with respect to the host interface means element, under § 112, ¶ 6 and ¶ 2. The ID correctly found that even though Oak's interpretation of the host interface means has shifted, it is possible to find numerous structures in the specification that are clearly linked to the functions claimed by the host interface means of independent claim 1. Thus, the '715 patent conveys with reasonable clarity to one of ordinary skill in the art that the inventors were in possession of the patented host interface means. We therefore affirm the ID's finding that the host interface means is not invalid under § 112, ¶ 6 and ¶ 2.

(2) *Alleged invalidity of the "memory means" under § 112, ¶ 6 and ¶ 2.*

The ID found that the '715 patent specification does not disclose a structure capable of performing the storage function required by the "memory means" element of claim 1 because the specification clearly states that the DRAM disclosed in the specification is not part of the claimed invention. The specification identifies only one structure that is linked to the "storing" function of the memory means, and that structure is a DRAM.[94] But the specification also explicitly identifies the DRAM as an *external structure* that is separate and distinct from the CD-ROM controller. The specification teaches that the external RAM that performs the "storing" function of the

---

[94] Identified in the '715 patent as 30 in Fig. 1 and 50 in Fig. 2. *See also* col. 3, lines 14-18; col. 6, lines 14-16; col. 6, lines 25-32; col. 6, lines 41-44; col. 7, lines 1-19.

memory means is not part of the claimed "drive controller 10," shown in Figure 2.[95] Thus, the required "memory means" called for in the claim, although disclosed in the patent, is described in the patent as not being part of the claimed invention.

The memory means claim element was not included in the set of claims provided with the original '715 patent application, but was added to the application later by amendment. Thus, while the original patent specification disclosed a "memory means," a DRAM, the original claims did not claim that memory means as part of the invention. Although the claims were later amended to include the memory means, the language in the specification was not amended to state that the originally-disclosed memory means were now considered part of the claimed invention.

For a patent to be valid under § 112, ¶ 2, the "claims read in light of the specification reasonably apprise those skilled in the art of the scope of the invention ... ."[96] We are presented in this investigation with the rather odd situation of a later-amended claim claiming matter that the specification clearly states is not part of the claim. The key legal issue is whether the scope of the invention thereby takes on an unreasonable degree of certainty for those of ordinary skill in

[95] '715 patent, col. 2, lines 60-66 ("The compact disk drive would generally have its own . . . random access memory . . . ."); col. 5, lines 44-47; col. 6, lines 14-16 (A DRAM **30** is coupled with the drive controller of the present invention for storing and buffering data via the drive controller."), lines 19-25; col. 9, lines 60-63 ("external RAM"); col. 10, lines 3-5, 34-49; col. 10, line 67 through col. 11, line 2; col. 11, lines 25-26, 45-55; col. 12, lines 5-13, 18-23; col. 3, lines 3-6; col. 15, lines 20-21; col. 16, lines 16-19; col. 18, lines 18-21; col. 19, lines 55-58; col. 20, lines 60-61; col. 22, lines 44-46; col. 24, lines1-26; Figures 1 and 2.

[96] *Credle v. Bond*, 25 F. 3d 1566, 1576 (Fed. Cir. 1994).

the art. The ID cited *In re Cohn*, 438 F.2d 989, 993 (C.C.P.A. 1971), stating that the court in that case invalidated claims that were inherently inconsistent when read in light of the "summary of the description, definitions and examples . . . in [the] specification." In *Cohn*, the court concluded that "[t]he result is an inexplicable inconsistency within each claim requiring" rejection under 35 U.S.C. 112, ¶ 2. *Id.*, at 1001. The specification in *Cohn* defined a critical claim term, "opaque finish," as a flat-appearing finish not obtained when alkali metal silicate is used as a sealant, and the claims specifically called for sealing a surface with alkali silicate in order to obtain an "opaque finish." The court concluded that "we are not sure that interested parties would be able to determine with adequate precision just what is the 'opaque appearance' which indicates completion of the 'corrosion treatment' step."[97] However, the conflict in terminology between the specification and the claims in *Cohn* presents a very different situation than the present one where a claimed "memory means," although fully disclosed in the specification, is also described in the specification as not being part of the claimed invention

In the prosecution of a patent application before the PTO, the claims and thus the scope of the invention are in a constant state of flux until agreement between the applicant and the PTO examiner is reached. During this process, an applicant is not allowed to introduce new matter, but is allowed to change what he originally regarded as his invention. In *In re Bower*, 433 F.2d 813 (CCPA 1970), the court allowed the applicants to later claim as part of their invention what they had not originally considered as part of the invention, but had nevertheless disclosed in the

---

[97] 438 F.2d at 991.

specification. "Considering the disclosure of the appellants' parent application ... we find that it contains an enabling disclosure of the invention now claimed. ... we have no doubt that the disclosure would still teach one having ordinary skill in this art how to make and use the claimed invention."[98] The issue in the present investigation is whether one having ordinary skill in the relevant art would be able to make and use the claimed CD-ROM controller when the patent specification fully discloses a RAM memory means that the specification indicates was not part of the claimed invention. In our view, the statements in the specification indicating that the DRAM memory means is not part of the claimed invention would be viewed as an obvious error by those skilled in the art.[99]

Respondents have failed to show by clear and convincing evidence that persons of ordinary skill in the art would not understand the scope and meaning of the "memory means" claim element. The '715 patent specification does disclose a structure capable of performing the storage function required by the "memory means" element of claim 1, *viz.*, the DRAM. The dotted lines in the figure of the '715 patent that appear to indicate that the DRAM is *not* a part of the claimed controller would be viewed as an obvious error by those skilled in the art, and the claims read in light of the specification would reasonably apprise those skilled in the art of the scope of the invention.[100] Both respondents' and complainant's experts (Buscaino and Wedig,

---

[98] *In re Bower*, 433 F.2d at 817.

[99] *In re Oda*, 433 F.2d 1200, 170 USPQ 260 (CCPA 1971). (Obvious errors are amendable if one skilled in the art would recognize the error and the appropriate amendment).

[100] Respondents cite *Process Control Corp. v. HydReclaim Corp.*, 98-1082, -1277 (Fed. Cir.

(continued...)

respectively) testified that, after reading the '715 patent, they understood that the claimed CD-ROM controller included a DRAM.[101] We therefore reverse the ID's finding that the '715 patent is invalid under § 112, ¶ 2 and ¶ 6 for failure to disclose any structure to perform the storing function of the memory means claim element.

(3) *Alleged invalidity of the '715 patent under § 112, ¶ 1 ("written description").*

The ID also held that the '715 patent was invalid under § 112, ¶ 1 because the specification and the original application do not provide a written description of a controller that includes a "memory means for temporarily storing data," and thus the written description in the specification of the '715 patent does not "convey with reasonable clarity to those skilled in the art that, as of the filing date . . . , [that applicants were] in possession *of the invention*," where "the invention is, for purposes of the 'written description' inquiry, *whatever is now claimed*."

---

[100] (...continued)
1999), for the proposition that when the claim language of a claim reasonably dictates a nonsensical result, the claim is invalid. Respondents argue that *Process Control* dictates an interpretation for the claim term "memory means" that results in a finding of invalidity under 35 U.S.C. § 112, ¶ 1 due to the apparent lack of support for that term in the specification. However, the issue in *Process Control* was whether a term recited twice in a claim could be construed to have two different meanings within that claim. It not the claim would be rendered nonsensical and, therefore, invalid. The Federal Circuit held that the plain language of the claim compelled only one reasonable construction of the claim term and therefore invalidated the claims as inoperative and failing to comply with the utility and enablement requirements of 35 U.S.C. § § 101 and 112, ¶ 1, respectively. In this investigation, the holding in *Process Control* strengthens our construction of the term "memory means." The plain language of claim 1 of the '715 patent states that the "memory means" is part of the claim CD-ROM controller. We do not agree with respondents' construction, which relies upon what we found to be an obvious error in the specification, to circumvent the plain language of the claim.

[101] Buscaino Tr. at 1996-1997; Wedig Tr. at 627.

Vas-Cath Inc. v. Mahurkar, 935 F.2d 1555, 1563-64 (Fed. Cir. 1991) (cited in ID at 147). In our view, the applicants *were* in possession of the claimed memory means as of the filing date and they fully disclosed that "memory means," *viz.*, the DRAM. They simply did not regard the "memory means" as part of their invention when they filed the original '715 patent application.

The ID also cited and quoted from *Ex parte Grasselli*, 231 USPQ 395 (Bd. Pat. App. & Inter. 1983), where it is stated that "[t]he express exclusion of certain elements not discussed in the original specification together with the implicit . . . inclusion of all other elements not originally disclosed in the original specification constitutes new matter, i.e., lacks description in the original specification and violates [§ 112, ¶ 1]." 231 USPQ at 394. However, the DRAM "memory means" was supported and fully disclosed in the original application. It simply was not part of the original *claims*, although the claims were later amended to include the memory means. The ID found that the applicants "amended their claims to add elements 'not discussed in the original specification' as being part of the claimed controller."[102] But the applicants did discuss a "memory means" in the original claim 1 of the application; they discussed a memory means sufficient for the ID to construe the "memory means" as a means-plus-function element with a DRAM as the corresponding structure disclosed in the specification. For these reasons, we reverse the ID's finding that asserted claims of the '715 patent are invalid under § 112, ¶ 1.

(4) *Alleged invalidity of the '715 patent under §112, ¶ 1 ("essential material").*

With regard to their assertion of invalidity under § 112, ¶ 1 for failure to include essential

---

[102] ID at 148.

material necessary to describe and enable the claimed invention, respondents argue that Oak's expert (Wedig) conceded that the '715 patent specification, standing alone, does not provide a basis for understanding what is encompassed within the scope of the claims. Respondents assert that the '715 patent does not completely describe or enable the claimed invention, and contend that the ATA specification is "essential material" necessary to describe and enable fully the invention claimed in the '715 patent. They note that under the PTO's rules essential material may not be incorporated in a patent by reference to a non-patent publication.[103]

However, mere reference to another document is not an incorporation by reference.[104] The ATA specification is not incorporated by reference in the '715 patent, it is merely referred to in the '715 patent, presumably on the assumption that it was a reference known to those skilled in the art of designing peripheral devices for computers.[105] We agree with the ID that the evidence shows that one of ordinary skill in the art would already be familiar with the ATA specification, or would become familiar with it if he or she planned to design a CD-ROM drive to be connected to a host computer. Thus, there was no need for the '715 patent specification to repeat information already within the knowledge of one of ordinary skill in the art. We therefore adopt the ID's finding that the claims at issue of the '715 patent are not invalid valid under §112, ¶ 1 for

---

[103] M.P.E.P. § 608.01(p) (part I.A) ("essential material" is defined as "that which is necessary to (1) describe the claimed invention, (2) provide an enabling disclosure of the claimed invention, or (3) describe the best mode.")

[104] *In re de Seversky*, 474 F.2d 671 (CCPA 1973).

[105] Wedig Tr. at 439.

failure to include "essential material" necessary to describe and enable the claimed invention.

Since we find claim 1 valid, we also find claims 2-5 and 9, claims that depend on claim 1, valid.

e) Enforceability/Inequitable Conduct

A patent may be valid yet unenforceable against infringers for a variety of reasons. One reason, which is at issue in this ID, is inequitable conduct by the patent applicants before the PTO during the process of obtaining the patent. Inequitable conduct requires proof of two elements: (1) a failure to disclose material information, or the submission of false material information, during prosecution of a patent; and (2) an intent to deceive.[106] The trier of fact is to weigh the intent of the party accused of inequitable conduct in light of all the evidence, including any evidence of good faith.[107] A prior art reference that is merely cumulative of references already before the PTO examiner is not material for purposes of determining inequitable conduct.[108] In the presence of material omissions or misrepresentations, less evidence suffices to show intent to deceive.[109]

The ID ruled that the inventors of the '715 patent (Verinsky and Case) were guilty of inequitable conduct before the PTO for failure to disclose various references and facts to the PTO

---

[106] *Kingsdown Medical Consultants Ltd. v. Hollister Inc.*, 863 F.2d 867, 872 (Fed. Cir. 1988) (en banc).

[107] *Id.* at 876.

[108] *Halliburton Co. v. Schlumberger Tech. Corp.*, 925 F.2d 1435, 1440 (Fed. Cir. 1991).

[109] *Id.* at 1439.

examiner. The ID found that those persons should have disclosed to the PTO examiner information on (1) the OTI-012 controller, (2) the full Sanyo LC8950/51 Application Note, (3) the existence of the Mitsumi prototype, (4) the June 1993 ATAPI specification, and (5) the offer for sale of the OTI-011 controller. The ID found that all of these facts and documents would have been material to the examination of the patent application that matured into the '715 patent.

As to the intent requirement for a finding of inequitable conduct, the ID made two points. First, the ID quoted from a letter from an Oak marketing manager, Brown, to his supervisor in which Brown outlined his intention to seek patent protection for the OTI-011 controller. However, Brown also stated that a patent application for the OTI-011 controller "may not pass the test of being 'non-obvious' nor the time test since we have been promoting it for more than two years." The ID viewed this statement as indicating an awareness on the part of Brown of on-sale bar difficulties that should have led to disclosure to the PTO examiner of the offer for sale of the OTI-011 product. Second, the ID drew negative inferences from the fact that none of the facts or documents that it found were material to validity were ever disclosed to the patent attorney who prosecuted the application that matured into the '715 patent. From these facts, the ID concluded that the inventors knew of the materiality of the omitted information and intentionally concealed it from the examiner.

We find that respondents have failed to present clear and convincing evidence that the information that was not disclosed to the PTO examiner was material and that the failure to disclose that information was done with an intent to deceive the PTO. First, the non-disclosed references are not material in light of our conclusions on anticipation and obviousness. Second, we find that co-inventors Verinsky and Case both offered reasonable explanations concerning why they did not consider the omitted items to be material. Each explanation will be discussed along with a discussion of the materiality of each reference.

The OTI-012 controller was Oak's starting point, or "baseline," for the IDE CD-ROM project. That controller was therefore well known to the inventors of the OTI-011 IDE CD-ROM controller (the subject of the '715 patent) and it contained many of the elements of the OTI-011. But more than this is needed to show by clear and convincing evidence that the applicants' failure to disclose the OTI-012 chip itself, or its schematics, to the examiner was inequitable conduct. We agree with the IAs that the ID appears to have shifted the burden of proof on intent to deceive to Oak, and seems to have disregarded the plausible explanations offered by the applicants for their failure to disclose the references in question. Inventor Verinsky testified as to his awareness of the duty of disclosure to the PTO and denied any intent to deceive the examiner. He testified that he believed that the OTI-012 controller was simply the state of the art at the time, and that by disclosing the state of the art to the examiner in the specification, he had satisfied his duty of candor.[110] The features of the OTI-012 controller are generally described in the portion of the specification that describes the prior art.[111]

Concerning the Sanyo LC8950/51 Application Note, the ID concluded that "Oak intentionally kept the full text of the Sanyo application note and information about the Sanyo

---

[110] Verinsky Tr. at 1044-45, 1105-06.

[111] '715 patent, col. 1, lines 19 to col. 2, line 56.

products from [Oak's patent attorney] and the PTO for the purpose of deceiving the PTO."[112] However, the Sanyo LC8950/51 Application Note simply represented the state of the art described in the '715 patent, and withholding that document from the PTO examiner does not show an intent to deceive the examiner.

The Sanyo LC8950/51 Application Note describes a proprietary interface CD-ROM controller that was functionally identical to Oak's OTI-012.[113] It was therefore no more material to the application than was the OTI-012, which is generally described in the patent as the state of the art.

The ID also found an intent to deceive from the fact that the applicants provided some pages of the Sanyo Application Note to their patent attorney, but not the entire document. The ID regarded the omitted portions as "highly material."[114] However, if the whole document was merely a description of the state of the art when Oak started the OTI-011 project, and was therefore necessarily not material to the claimed invention, then the omitted portions of the document were no more material.

The ID found that the Mitsumi prototype was material to patentability, and that there is no "exculpatory explanation for the applicants concealment of Mitsumi's work" from their patent

---

[112] ID at 166.

[113] Brown Tr. at 176; RX-4C; Sugie Tr. at 829-30.

[114] ID at 164.

attorney and the PTO.[115] However, the ID's finding that the Mitsumi prototype was material is based on what we have found to be an erroneous construction of the "host interface means" element of claim 1 of the '715 patent. A known anticipatory reference must be disclosed to the examiner, but the Mitsumi prototype is not anticipatory because it did not contain the key inventive feature of the `715 patent's "host interface means" *viz.*, a direct connection to the IDE.

Although the ID found it "incredible" (ID at 169) that inventor Verinsky believed that Mitsumi's work "was not of interest to" him, we find Verinsky's testimony credible since the Mitsumi prototype used a ISA daughterboard and a proprietary interface, which Oak was trying to design away from with the OTI-011 project and its proprietary interface. We therefore reverse the ID's finding that the '715 patent is unenforceable due to inequitable conduct before the PTO for not disclosing the Mitsumi prototype to the PTO examiner.

We also believe that the ID's conclusion that the inventors concealed the "ATAPI documents" and that such concealment was intentional (ID at 171) is erroneous. As discussed above, the ATAPI specification has not been shown to be prior art and only prior art need be disclosed to the PTO examiner. Morover, the ID itself pointed out the extent to which the '715 patent specification expressly references the ATAPI specification.[116] Thus, the ID found that Oak had committed inequitable conduct by not disclosing a reference that is repeatedly mentioned in

---

[115] ID at 169.

[116] *See* ID at 113: "In columns 8 through 28, the word `ATAPI' and the use of `ATAPI' registers are mentioned 38 times"; ID at 135-36: "the `715 specification is replete with many references to ATAPI."

the patent specification.

The ID found that the April 1993 sales agreement between NEC and Oak for the yet-to-be completed OTI-O11 controller should also have been disclosed to the PTO examiner. However, we believe that this finding is based on the ID's erroneous construction of the host interface means and on an improper shifting to Oak the burden of proof on intent to deceive. The record shows that there was evidently some confusion within Oak about what constituted a "sale" that had to be disclosed to the PTO examiner. Marketing manager Brown testified that he did not believe that the sales agreement with NEC raised an on-sale bar because Oak was not obliged to deliver a product if Oak was unable to develop the IDE CD-ROM controller.[117] Brown's understanding of what constituted a "sale" was erroneous, but he is not an attorney and his misunderstanding does not amount to an intent to deceive.

The ID also found it highly significant that Brown, in a memorandum to his supervisors, raised concerns about a possible on-sale bar and obviousness.[118] However, Brown did not believe the OTI-O11 was obvious because numerous engineers at Oak and other companies believed that an IDE CD-ROM would not work.[119] Brown's memorandum, considered in isolation, might prove some prior knowledge on Brown's part of possible material sales activity and evince an intent to deceive by not disclosing that activity to the PTO. But after writing the memorandum,

---

[117] Brown Tr. at 145-46.

[118] RX-77C.

[119] Brown Tr. at 149-53.

Brown learned that the time period for filing a patent application was not initiated by Oak's *promotion* of the *idea* of an IDE CD-ROM controller, but rather by Oak's first sale of the device or when the device was ready for patenting.[120] Moreover, although Brown initiated preparation of a patent application for the OTI-O11 controller, he was not involved in the final decision to file the application and did not review it.[121] Thus, although we agree that it would have been better prosecution practice to disclose the sales activity and file affidavits with the PTO as to why such activity did not constitute an on-sale bar, we do not believe we should attribute the sophistication of a patent attorney to a marketing person such as Brown. While his memorandum shows that Brown had some sketchy awareness of the concept of an on-sale bar, it also shows that he had an imperfect understanding of the differences between "promotion" and "sale" for the purposes of an on-sale bar. His confusion about the meaning of "sale" is understandable in view of the fact that Oak's contract with NEC relieved Oak of any obligation to deliver a product if Oak was unsuccessful in developing one. For these reasons we reverse the ID's finding that the '715 patent is unenforceable due to inequitable conduct before the PTO for not disclosing to the examiner the April 1993 sales agreement between NEC and Oak for the yet-to-be completed OTI-O11.

In summary, we reverse the ID's conclusion of law that the claims in issue of the '715 patent are unenforceable because of inequitable conduct before the PTO for failing to disclose the OTI-012 controller, the Sanyo LC8950/51 Application Note, or the ATAPI specification to the

---

[120] Brown Tr. at 153-54.

[121] Brown Tr. at 352-55.

PTO examiner.

G. ALJ Order No. 15

In Order No. 15, the ALJ granted UMC's motion for summary determination terminating UMC from the investigation on the basis of a license agreement.

The agreement between Oak and UMC licenses two major categories of CD-ROM controllers manufactured by UMC and/or its partially owned affiliates. Thus, UMC is licensed by Oak to manufacture and sell "CD-ROM controller devices" "in production lots of no more than [ ]," "for a time period ending [ ] after the date of this agreement." The first category consists of CD-ROM controllers on which UMC had already begun production as of the date of the agreement. These parts are licensed at a royalty of [ ]. The second category, denominated *"limited basis"* parts, consists of CD-ROM controllers to be manufactured "in production lots of no more than [ ], for a time period ending [ ] after the date of [the] agreement." Oak's contends that UMC's manufacture and sale of CD-ROM controllers during the [ ] "limited basis" period far exceeded that which was permitted by the agreement. In Order No. 15 the ALJ held that Oak failed to provide any facts in support of this contention and granted the summary determination.

Since we affirm the ID's finding that the MediaTek CD-ROM controller does not infringe the claims in issue of the '715 patent, we take no position with regard to Order No. 15 on the grounds that it is moot.

H. Equitable Estoppel

Respondents have argued that Oak should be equitably estopped from asserting the claims in issue of the '715 patent against them because of Oak's purported failure to disclose Oak's patent rights to the ATA/ATAPI-4 Standards Committee.[122] However, since we find that the MediaTek controller does not infringe the '715 patent, we take no position on the equitable estoppel defense on the grounds that it is moot.

I. Conclusion

In sum, we determine to: (1) affirm the ID's finding that there is a domestic industry with respect to the '715 patent; (2) affirm the ID's finding of no literal infringement and no infringement under the doctrine of equivalents; (3) reverse the ID's findings of invalidity based on an on-sale bar under 35 U.S.C. § 102(b), anticipation under 35 U.S.C. § 102(a), obviousness under 35 U.S.C. § 103, indefiniteness under 35 U.S.C. § 112(1), (2), and (6), and for derivation under 35 U.S.C. § 102(f); (4) reverse the ID's finding of unenforceablity due to inequitable conduct before the PTO, (5) take no position with regard to Order No. 15 terminating respondent UMC from the investigation, and (6) take no position on the issue of equitable estoppel. We have therefore determined that there is no violation of section 337 of the Tariff Act of 1930 in this investigation.

[122] The ATA/ATAPI-4 Standards Committee is an industry standards committee that develops uniform standard for all peripherals, including CD-ROM drives, for attachment to the IDE/ATA interface.

APPENDIX OF ACRONYMS

The ALJ's final ID in this investigation, the parties' submissions, and this memorandum contain many acronyms, the most important of which are listed below.

AT	Advanced Technology (one of the original models of the IBM personal computer)
ATA	AT Attachment
ATAPI	ATA Packet Interface
BSY	Busy
CD-ROM	Compact Disk-Read Only Memory
CRC	Cyclic Redundancy Check
DASP	Drive Active/Drive 1 Present
DIOR	Drive Input/Output Read
DIOW	Drive Input/Output Write
DRAM	Dynamic Random Access Memory
DRV	Drive
DSP	Digital Signal Processor
ECC	Error Correction Code
EDC	Error Detection Code
FIFO	First In First Out
HIRQ/INTRQ	Host Interrupt Request Line
IDE	Integrated Drive Electronics
ISA	Industry Standard Architecture
PC	Personal Computer
PDIAG	Passed Diagnostics

RAM	Random Access Memory
RESET	Drive Reset Trigger
SRST	Software Reset