

Spring 2017: EENG 5550

Hardware Design Methodologies for ASICs and FPGAs

Tu, Th – 11.30 am – 12:50 pm

Room B227

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When students design circuits, they often think only about the functionality of the circuit, not considering how their circuit will be implemented in real hardware. This course fills that gap, teaching students how to code their designs in such a way that the hardware implementation is efficient and achieves their design goals in an elegant manner. When students complete this course, they have a good control of what happens behind the scenes when a synthesis tool creates a design from a specification in a hardware description language.

This course teaches hardware design methodologies through the use of industry tools. Students use design automation tools to design, simulate, and synthesize designs for standard cell-based ASICs and FPGAs using hardware description languages (e.g. VHDL and Verilog). Students will study the synthesis concept to understand how hardware functions written in these hardware description languages are synthesized. Techniques for design optimization, simulation, and synthesis of combinatorial functions, data paths, and finite state machines are covered in depth. Students will be exposed to the differences between design flows for standard cell-based ASICs and FPGAs.

Pre-requisite: EENG 2710 (Digital Logic Design)

Required Text: J. Bhasker, *A VHDL Synthesis Primer: Second Edition*, Star Galaxy Publishing, ISBN 0-9650391-9-6

Course Material: Blackboard Learn

Grading:

- Homework / Lab Assignments: 20%
- Reading Assignments / Paper Presentations: 40%
- Final Project: 40%