EENG 4710 VLSI Design

Instructor: Gayatri Mehta
Office: Discovery Park B-262
Office Hours: (T, Th) 11:00 am-12:00 pm
Phone: 940-369-5118
Email: gayatri.mehta@unt.edu

Fall 2010
Time: (T,Th) 9:30-10:50 am
Meeting Place: NTDP B227

Course Description:

This course focuses on the design of digital systems with an emphasis on hands-on chip design. Students will use industry CAD tools to design, layout and simulate the VLSI circuits. The topics covered include MOS transistor, circuit characterization, circuit simulation, combinational and sequential circuits, static and dynamic logic circuits, and memories.

Topics:

- Introduction and Overview of VLSI systems
- CMOS logic and fabrication
- MOS transistor theory
- Layout design rules
- Circuit characterization and performance estimation
- Circuit simulation
- Combinational and sequential circuits
- Static and dynamic CMOS gates
- Memory system design
- Design methodologies and tools

Course Objectives:

By the end of the course, you will

- Understand the theory and characteristics of MOS transistor
- Understand the CMOS process and technology
- Understand combinational circuits
- Understand sequential circuits
- Understand power dissipation in CMOS circuits
- Understand memory system design
- Develop ability to use commercial CAD tools to design and simulate digital circuits
- Develop technical writing skills
- Develop project presentation skills

Prerequisites:

EENG 2710 and EENG 3510

Textbook(s) and/or required material:
CMOS VLSI Design 4th edition, Neil Weste and David Harris (Required textbook)
Digital Integrated Circuits by Rabaey, Chandrakasan, Nikolic (Reference)

Exams: There will be three exams (this includes the final exam), each worth 100 points.

Missed Exams: You will be allowed to make up a missed exam only if you have a documented university excused absence. If you know in advance that you will miss an exam, you MUST contact me before the scheduled exam.

Assignments: No late assignments will be accepted.

Rather than taking attendance, there will be pop quizzes. A quiz may be administered at the beginning, middle, or end of a class session.

Grading:

- Assignments: 30%
- Exam 1: 15%
- Exam 2: 15%
- Final: 20%
- Project: 10%
- Pop Quiz: 10%

Disabilities Accommodation:

The University of North Texas complies with Section 504 of the 1973 Rehabilitation Act and with the Americans with Disabilities Act of 1990. The University of North Texas provides academic adjustments and auxiliary aids to individuals with disabilities, as defined under the law. Among other things, this legislation requires that all students with disabilities be guaranteed a learning environment that provides for reasonable accommodation of their disabilities. If you believe you have a disability requiring accommodation, please see the instructor and/or contact the Office of Disability Accommodation at 940-565-4323 during the first week of class.

Additional Policies and Procedures:

Cell Phones: Please remember to turn off phones prior to class.

Extra Help: PLEASE DO NOT WAIT UNTIL THE LAST MINUTE. If you are having trouble with this class, please come by my office during office hours. I am also available by email at gayatri.mehta@unt.edu.

Course Outline and Tentative Schedule:

Week	Date	Day	Topics
1	08/26	Th	Introduction
2	08/31	T	Introduction to CMOS Circuits
	09/02	Th	CMOS Transistor Theory
3	09/07	T	Manufacturing and Layout
	09/09	Th	DC Response and Logical Effort
4	09/14	T	Logical Effort
	09/16	Th	Wires
5	09/21	T	*Review*
	09/23	Th	**Mid-term Exam 1**

6	09/28	T	MOS Transistor: Non-ideal IV Effects
	09/30	Th	Combinational Circuits - 1
7	10/05	T	Combinational Circuits - 2
	10/07	Th	Circuit Families -1
8	10/12	T	Circuit Families -2
	10/14	Th	Sequential Circuits - 1
9	10/19	T	Sequential Circuits - 2
	10/21	Th	Adders
10	10/26	T	Data path Functional Units
	10/28	Th	*Review*
11	11/02	T	**Mid-term Exam 2**
	11/04	Th	Static Random Access Memory
12	11/09	T	Static Random Access Memory
	11/11	Th	CAMs, ROMs and PLAs - 1
13	11/16	T	CAMs, ROMs and PLAs - 2
	11/18	Th	Non-ideal Transistors -1
14	11/23	T	Non-ideal Transistors -2
	11/25	Th	*Thanksgiving, no classes*
15	11/30	T	Design for Low Power
	12/02	Th	*Review*
16	12/07	T	*Pre-Finals Week, No Class*
	12/09	Th	
17	12/14	T	**Final Exam**