Nanoelectronics, Nanophotonics, and Nanomagnetics

Report of the National Nanotechnology Initiative Workshop
February 11–13, 2004

About this document

This document is the report of a workshop held under the auspices of the NSET Subcommittee on February 11–13, 2004, in Arlington, Virginia. The primary purpose of the workshop was to examine trends and opportunities in nanoscale science and engineering as applied to electronic, photonic, and magnetic technologies.

About the cover

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Nanoelectronics, Nanophotonics, and Nanomagnetics

Report of the National Nanotechnology Initiative Workshop
February 11–13, 2004, Arlington, VA

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PREFACE

This report on nanoelectronics, nanophotonics, and nanomagnetics is one of a series of reports resulting from topical workshops convened during 2003 and 2004 by the Nanoscale Science, Engineering, and Technology (NSET) Subcommittee of the National Science and Technology Council's Committee on Technology. The workshops were part of the NSET Subcommittee's long-range planning effort for the National Nanotechnology Initiative (NNI), the multi-agency Federal nanotechnology program. The NNI is driven by long-term goals based on broad community input, in part received through these workshops. The NNI seeks to accelerate the research, development, and deployment of nanotechnology to address national needs, enhance our Nation's economy, and improve the quality of life in the United States and around the world, through coordination of activities and programs across the Federal Government.

At each topical workshop, nanotechnology experts from industry, academia, and government were asked to develop broad, long-term (ten years or longer), visionary goals and to identify scientific and technological barriers that once overcome will enable advances toward those goals. The reports resulting from this series of workshops inform the respective professional communities, as well as various organizations that have responsibilities for coordinating, implementing, and guiding the NNI. The reports also provide direction to the researchers and program managers in specific areas of nanotechnology R&D regarding long-term goals and obstacles to reaching those goals.

This workshop was convened to solicit input from the research community on the NNI research agenda relating to the uses and impact of nanoscale science and engineering within the fields of electronics, photonics, and magnetics, and its role in integrating these technologies within the broad area of information technology. The nanotechnology experts were asked to (1) develop long-term, visionary goals within topical areas and (2) identify specific barriers (or "hard problems") inhibiting "quantum advances" toward those goals.

Electronics, photonics, and magnetics are critical areas of research and development for the information technology industry—a sector that is vital to both the economy and defense of the United States. This workshop report provides recommendations for the NNI research agenda in five major categories related to information technology: acquisition, storage and memory, information processing, transmission, and system-level integration.

The findings from this workshop were taken into consideration by the NSET Subcommittee in the preparation of the December 2004 National Nanotechnology Initiative Strategic Plan and served as input to the December 2007 update to that plan. The expert opinions voiced at the workshop have also guided managers from the Federal agencies in the development of programs that make up part of the fiscal year 2006–2009 budget requests for the NNI. The strong continuing NNI investment in the science of electronic, photonic, and magnetic devices and systems, as well as in the materials, processes, and instrumentation needed to fabricate and characterize them, reflects the consensus that the future of these fields lies at the nanoscale.

On behalf of the NSET Subcommittee, we wish to thank Drs. Gernot Pomrenke and Chagaan Baatar for their creativity and hard work in organizing and conducting an outstanding workshop that offered a glimpse at that future. We also thank all the speakers, session chairs, and participants for their time

and efforts to join the workshop, to make their individual contributions to the discussions at the workshop, and then to contribute to the drafting of this report. Their generous sharing of the results of their research and their insights ensures that this document will serve as a reference for the NNI.

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TABLE OF CONTENTS

Table of Contents

EXECUTIVE SUMMARY

Nanotechnology is coming of age in a time when society's appetite for information processing is voracious, and still growing. The proliferation of information technology (IT)—now essential to many areas of industry and commerce including health care, environmental monitoring, communication, and scientific computing—has relied on steady increases in both the flow of information and the capacity to process that information. New technologies must be developed to meet the continuing need for greater throughput and more powerful processing.

On February 11-12, 2004, scientists and engineers gathered in Arlington, Virginia, at the National Nanotechnology Initiative Workshop on Nanoelectronics, Nanophotonics, and Nanomagnetics. Their purpose was to identify groundbreaking research opportunities in electronics, photonics, and magnetics enabled by nanoscale science and engineering, and to discuss the application of such research to address tomorrow's IT needs.

The vision of electronic, photonic, and magnetic technologies twenty years from now that emerged from the workshop is quite unlike the corresponding technologies of today. Over the coming years, participants predict that the integrated circuits of today will give way, slowly at first, to devices that resemble them neither in form nor in details of function. In this vision, small-scale, lightweight, low-power systems will become ubiquitous, and will interact with their environment in real time. Some of these systems will be part of prosthetic devices, combining biomedical advances with integrated nanodevices, directly connected to or embedded within the human body to mitigate the effects of illness or injury. Others will be intelligent external assistants, new tools to further extend humankind's capabilities.

The route leading to that vision includes both revolutionary and evolutionary steps. If the future of information processing technologies lies at the nanoscale, functional devices incorporating nanostructures will have to be devised. Then affordable nanomanufacturing techniques must be developed and integrated with existing processes for fabricating electronics, photonics, and magnetics.

A central task for the workshop participants was to identify hard problems—scientific and technological obstacles to the broader adoption of nanotechnology for information processing. The identified problems can be broadly divided into two categories: those arising from performance requirements of information processing devices themselves or in systems integration, and those arising from the desire to operate devices in novel, often harsh, environments. Overcoming these obstacles will almost certainly require better integration of electronic, magnetic, and photonic phenomena into information processing devices and systems. As biological systems teach us, it will also require extension of the present largely two-dimensional chips (centimeter in width, micrometer in depth) into fully three-dimensional devices and circuits.

For problems in the first category, nanotechnology serves as a means to keep electronic, photonic, and magnetic technologies on the path of improving performance they have followed for the last forty years. The IT industry's focus on managing larger and larger bodies of information in shorter and shorter periods of time has driven it to continually develop smaller, faster, and less expensive computation, memory, and communication devices. In the near term nanotechnology will contribute to maintaining this course by resolving issues inherent to scaling silicon semiconductor technology

to its ultimate limits. In the longer term today's materials and architectures will yield to completely new nanoscale approaches scalable to densities and performance levels well beyond the ultimate limits of silicon-based technology.

For problems in the second category, nanodevices and nanomaterials offer unique methods for introducing electronic, photonic, and magnetic components into biological systems, or utilizing them in other environments with their own stringent constraints. For example, chips implanted in the human body to replace lost or damaged natural abilities must operate from ultralow input power, produce negligible thermal output, and be compatible with the *in vivo* physiological environment. These same considerations—nanotechnology's potential for exquisite control over power usage, thermal output, and materials compatibility—make nanoscale devices and systems very attractive candidates for spaceborne and defense applications.

Workshop participants made specific findings and recommendations related to five information technology functions—acquisition, storage, processing, and transmission of information, and systems integration. They also reached consensus that several crosscutting themes and topics should receive research emphasis in order to ensure that nanotechnology-enabled electronic, photonic, and magnetic devices and systems develop apace. In implementing the workshop findings and recommendations, other significant investments in these areas of nanotechnology should be considered. For greatest effect, U.S. activities should leverage investments by other nations and by the private sector.

FINDINGS BY SPECIFIC FUNCTION

Acquisition of Information

Signal acquisition, the essential first step in many information technology systems, was examined in both plenary and breakout sections of the workshop. The utilization of nanotechnology-based sensors and transducers to convert environmental variables into electromagnetic signals for processing and storage involves the creation of nanoscale probes, the development of novel device synthesis and characterization techniques, and the design of new acquisition system architectures.

Successful development of sensors and acquisition systems employing nanoelectronic, nanophotonic, and nanomagnetic technology will provide several key advantages:

- *Interaction with the environment on the molecular level* will provide new sensing schemes with improved sensitivity and specificity.
- *Extremely small transducers* will allow arrays of many sensors within a small area, which can employ statistical sampling together with adaptive processing to improve sensitivity, resolution, and accuracy.
- *Low power operation* will allow use for extended periods via batteries or energy scavenging devices, and will reduce waste heat to negligible levels.
- *Novel adaptive architectures* will successfully emulate the architectures and organizing principles of biological organisms to provide large dynamic range, high selectivity, and excellent sensitivity.

Recommended topics for major research thrusts in acquisition include:

1. Integrated handheld disease diagnostic systems
2. Integration of chip-based electrical, optical, magnetic, and mechanical sensors with "intelligence" implemented via conventional silicon technology

3. Single-molecule detection systems
4. Manipulation and imaging of structures within fluid channels
5. Probes based on quantum nanostructures in novel architectures designed to provide desired functionality (*Nanoscale acquisition demands nanoscale probes.*)

Memory and Storage

While all computing systems use memory during the processing of information and for storing data, their requirements vary widely. Supercomputers correlating complex images require rapid access to huge memory banks, while radio frequency identification tags need only small amounts of memory but must minimize power use. Most of today's IT systems use fast but volatile memory for intermediate results during processing, and persistent but slow memory for storage

Nanotechnology offers promising means for optimizing the key parameters of memory systems, including capacity; storage density; reading and writing speed; persistence of stored data; and required power, and could replace the two-memory paradigm of today's computing systems with a single unified memory. Memory elements for nanotechnology-based data storage might utilize quantum dots, single magnetic domains, molecular states, nanoscale defects, phase change materials, single electron charges, or an electronic spin.

The development of nanoscale memories must be guided by experts from multiple disciplines. Physics must be used to evaluate potential device elements; materials science and chemistry to develop fabrication technologies; engineering paradigms and computer-aided design tools to allow systematic design optimization for different applications. Addressing the individual elements of future terabit nanomemories poses difficult technical problems. Nanophotonic memories (e.g., holographic storage devices) will require development of new nonlinear, spectrally sensitive materials.

Recommended areas of emphasis for research in memory and storage include:

1. Development of a unified memory architecture featuring fast, inexpensive, high-density, nonvolatile memory
2. Development of a lookup memory with greater than 100 terabyte capacity and appropriate access times

Information Processing

Information processors manipulate and interpret gathered or sensed data. The exponential development of microelectronic integrated circuit technology throughout the last half century has driven an unprecedented revolution in information processing capacity and speed. The area of a single transistor in a commercial microprocessor shrinks by a factor of two every other year, as does its cost; the total cost of an ever-improving processor chip remains relatively constant.

With the development and commercial introduction of 65 nm complementary metal-oxide-semiconductor (CMOS) technology, the semiconductor industry has already crossed the nanoelectronics frontier. These trends are expected to continue for the next 10 to 15 years, until the feature size of silicon-based nanoelectronics reaches 22 nm or perhaps even 16 nm. Then fundamental physical limits to the size of conventional devices and the power they dissipate will prevent additional improvements. Further scaling will require the introduction of revolutionary technologies not subject to the same limits, though the first such technologies will likely be integrated with scaled CMOS.

Nanotechnologies under investigation for that role include carbon nanotubes or nanowires integrated in the channel of a metal-oxide-semiconductor transistor and molecular memory embedded on the processor chip. These will still operate within the current paradigm for information processing, which is closely tied to the representation of data by electrical charge or magnetic domains. Further in the future, substantial additional reductions in scale may be achieved by employing a completely new approach, which would use alternate physical phenomena to represent, store, process, and communicate information. New state variables that could serve as the physical manifestation of information include electron or nuclear spin, photon number or polarization, molecular or atomic energy states, and other quantum states. Molecular electronics, spintronics, and nanotube-based devices are all examples of this approach.

Implementation of these new processor technologies presents challenges including materials issues, design of architectures that best exploit the opportunities available at the nanoscale, and the development of appropriate tools for chip designers. The larger issue, however, may be producing such ultrahigh performance technologies at a viable cost.

Recommended areas of emphasis for research in information processing include:

1. Development within a decade of technologies and processes to extend silicon-based technology beyond the current scaling limits by integrating nanomaterials in the channel of the transistor
2. Exploring applications of molecular memory embedded on the processor chip
3. Exploring information processing paradigms based on alternate physical representations of data to allow scaling of processor size, speed, and power by several additional orders of magnitude

Transmission

Data transmission and interconnectivity are essential components of all information processing systems and underlie the operation of all current communication and monitoring systems. As technologies continue to advance and device densities increase, interconnecting the devices is becoming more difficult. This is especially true as device dimensions move well into the nanoscale regime. The sheer number of connections that must be made within a system is enormous. Coupling of signals into or out of processor chips requires new techniques when the physical size of the interconnects is larger than that of the connected on-chip device (e.g., for metallic interconnects), or when the device is much smaller than the relevant wavelength (e.g., for optical interconnects).

Nanoelectronics, spintronics, plasmonics, and molecular electronics all offer means for addressing these challenges. A unified approach drawing from all these areas, called nanonics, has also been proposed. Three-dimensional architectures and connection schemes, which would greatly increase system density, are under investigation. In each case, materials, design, and modeling issues must be addressed to achieve the desired functionality and to successfully integrate new interconnect methods with chip fabrication processes.

Recommended areas of emphasis for research in transmission include exploring:

1. Interconnections for three-dimensional architectures, including photonic approaches and those that emulate biological systems
2. The incorporation of ultra-high-index materials for ultra-high-density data transmission

3. Materials for nonelectronic logic or holographic routing that are multifunctional, incorporate intrinsic functionality, or have nonlinear properties

4. Techniques to couple information processing elements in the nanoscopic domain with the macroscopic world

System Level Integration

Workshop participants predicted that nanotechnology-based sensing, processing, control, communication, and actuation will lead to ubiquitous small-scale, lightweight, low-power systems. These integrated nanosystems will find application in new generations of prosthetic devices, lab-on-a-chip diagnostic systems, and self-powered, self-configuring sensor arrays. They will expand mankind's ability to sense, interact with, and ultimately control our environment.

These systems will be hybrids, combining novel nanoelectronic, nanophotonic, and nanomagnetic components with conventional electronic technology through integration on a common platform. Architecturally, many will be inspired by biological examples of nanotechnology-enabled systems. They must be able to function in situations that would challenge today's conventional technologies, such as when interfaced to biological organisms or in harsh chemical environments.

Perhaps the most difficult challenges in developing integrated nanosystems will be energy management. New architectures and new materials will be required to supply power to and remove heat from vast two- or three-dimensional arrays of active elements.

Recommended areas of emphasis for research in system level integration include:

1. Developing and validating methods, design tools, and physical parameter libraries for integrating nanoscale devices in CMOS technology

2. Developing top-down and bottom-up approaches for hierarchical assembly and cost effective fabrication of nano-micro-macrosystems

3. Learning to exploit nature's (biological) approach to integrate organic and inorganic materials and develop complex structures and architectures with encoded multifunctionality

4. Creating a design framework incorporating hierarchical representation, multilevel simulation and analysis, and verification tools

5. Exploring non-traditional silicon architectures with closely coupled sensing and processing functions, and identifying key applications for systems employing these architectures

FINDINGS IN CROSSCUTTING AREAS

Major research thrusts should also be considered in the following crosscutting areas, each of which affects several of the specific functions discussed in the preceding pages:

- Materials, Structures, and Metrology
  - discovery and characterization of new materials with unique electronic, photonic, or magnetic properties
  - design of materials with desired functionality or functionalities
  - scaling functional elements through self-assembly of functional materials or structures
  - utilization of quantum confinement and related effects to control quantum states
  - co-integration of nanomaterials, nanostructures, and the macroscopic world

- development and provisions for widespread access to modeling, simulation, and computer-aided design tools
- development of metrology, measurement, and characterization tools and techniques for the nanoscale
- controlling the interface between nanomaterials and biological systems
- Systems Function and Performance
  - improved information processing capacity and speed
  - fabricating, assembling, and interconnecting three-dimensional nanoelectronic, nanophotonic and nanomagnetic systems
  - connecting nanoscale components to the macroscopic world
  - new data representations and architectures, including biologically inspired information processing schemes
  - sensors with high sensitivity and single-molecule selectivity
  - power management and thermal management
  - hybrid nanoelectronic, nanophotonic, and nanomagnetic technologies
- Low-Cost Fabrication, Assembly, and Manufacturing
  - biologically inspired fabrication methods
  - directed or templated self-assembly of materials, structures, and devices
  - interfacing nanophotonics and nanomagnetics with nanoelectronics and with conventional electronics
  - nanoimprinting and soft lithography
  - multiprobe manufacturing

1. Introduction

BACKGROUND AND OVERALL VISION

Nanotechnology is coming of age in a time—the first decade of the 21st century—when society's appetite for gathering, transmitting, processing, and storing information is both voracious and steadily growing. Information technology (IT) is an essential component, for example, in managing human health, monitoring the environment, and communicating with our colleagues and families, as well as for transacting commercial and government business and for scientific computing.

A remarkable series of achievements in semiconductor growth, materials processing, nanoscale patterning, and device fabrication have been essential to the development of our IT infrastructure. Today's electronic, photonic, and magnetic materials are fabricated virtually atom by atom, with properties that are nearly ideal for application in the IT devices upon which we increasingly rely.

For society's dependence on the flow of information to continue to evolve on its current path, bringing new capabilities and extending the benefits of the information age to more and more of the world's citizens, new technologies must be developed. Numerous national and international programs are in place to develop materials, processing technologies, quantum and conventional devices, and device architectures for next-generation information processing systems and subsystems. These programs seek to improve speed, density, power and functionality beyond what is achievable simply by scaling silicon-based transistors.

Many have identified nanotechnology—already widely employed in today's semiconductor manufacturing processes—as an area ripe for exploration for future generations of IT hardware.

Are nanoelectronics, nanophotonics, and nanomagnetics the new technologies needed to address tomorrow's IT needs? Can they deliver sensors, devices, and systems that are smaller, less power-hungry, and closely tailored to a specific use? Will they allow makers of processors, memory devices, and magnetic recording media to extend the steep improvement curves, to which we have become accustomed, beyond the middle of the next decade? Will nonvolatile magnetic memory allow for "instant-on" computers? Will massive arrays of nanometer-scale devices lie at the heart of future information appliances? Will integrated high-density memories replace mechanical storage drives? Will nanoelectronics, nanomagnetics, and nanophotonics enable the development of ultralow-power devices, lessening or eliminating the need for batteries in portable systems? Will simpler nanodevices, embedded in nanoengineered biocompatible materials, control prosthetic devices that restore function to the injured and diseased? What obstacles must be overcome if the promise these technologies have already shown is to be translated into commercial reality?

These are the questions that scientists and engineers gathered to discuss on February 11–12, 2004 in Arlington, Virginia, at the National Nanotechnology Initiative Workshop on Nanoelectronics, Nanophotonics, and Nanomagnetics. Their purpose was to identify ground-breaking opportunities for research in nanoscale science and engineering applied to electronics, photonics, and magnetics, and specifically to identify hard problems—scientific and technological obstacles to the broader adoption of nanotechnology for information processing.

On the whole these scientists answered the above questions in the affirmative. They envisioned that completely new systems will evolve from research in nanoscale electronics, photonics, and

magnetics, which could improve throughput rates by a factor of 10 to 100 and increase device density by a factor of 5 to 100—all while operating at room temperature and reducing power consumption by one or two orders of magnitude.

Quantum effects, already important in today's electronic devices, will completely dominate the behavior of nanoelectronics; classical physics will recede into the background. Probability will replace determinism as the mechanism for representing logical operations in nanoscale physical devices. The von Neumann and Harvard architectures that dominate today's processor designs will be superseded by new architectures compatible with this new logical paradigm and capable of handling huge data flows, perhaps carried by ultrahigh frequency waves and manipulated with nanostructured nonlinear media. A quantum of information now stored as a bundle of charge will instead be encoded in the behavior of an individual particle. A host of new physical and chemical phenomena will be discovered, mastered, and then employed to manipulate these new information states. Fast nonvolatile memories will make computers available the instant they are turned on. Great reductions in required power will allow devices to operate for extended periods in remote locations. Systems will perform flawlessly in harsh environments. Multiple functions will be embedded within single chips to construct intelligent sensors for surveillance or robotic applications; these systems on a chip will detect, process, and store information, make decisions, and then adapt their own behavior to best support their mission. Nanoengineered devices will be embedded in biocompatible materials to control prosthetic devices that restore function to the injured and diseased. Intelligent external assistants will increase humankind's capabilities—as tools have throughout history—in ways we cannot yet even imagine.

ORGANIZATION OF THE REPORT

The technologies associated with information processing are highly varied, so finding an organizational structure for examining the impact of nanotechnology across the entire field is a difficult task. The organizers chose to arrange workshop discussions around several processes commonly utilized in information technology. The participants' evaluation of the impact of nanotechnology on each of these generic processes is represented by a chapter in this report. First, one must acquire data—sensing and detection functions are covered in Chapter 2, "Acquisition of Information." Raw or processed data must be retained indefinitely in some form of storage—Chapter 3 covers "Memory and Storage." Processes for converting data into useful information and analyzing that information are the focus of Chapter 4, "Information Processing." Chapter 5 , "Transmission," explores functions for moving data from place to place within a device or system or conveying information to the final user. Chapter 6, "System-Level Integration," considers how these four classes of functions can be fully integrated into an information system. The workshop began with a keynote speech by Horst Stormer, Professor of Physics and Applied Physics at Columbia University. An almost-verbatim transcription of Dr. Stormer's remarks, which ably set the stage for the workshop, forms the remainder of this chapter.

INTRODUCTORY REMARKS BY H. STORMER

I'm going to take this opportunity to give you some free flying thoughts [which will] probably [be] a bit controversial I hope and also a bit entertaining. One of the characteristics of talks on "nano anything" [is] extraordinarily jazzy viewgraphs. I have often wondered about this, and can find all sorts of cynical explanations for it. On the other hand it is one of the ways to get a handle on the

subject by creating ways to handle virtual molecules and nano objects that fly through your mind. Given the apparent power of this approach I will go further in my talk, and bypass the jazzy graphics. I will create the images directly in your head just through words, a totally new angle.

So this workshop is about nanoelectronics, nanomagnetics, and nanophotonics. If I tried to put my arms around this in a really broad way, I would say this is basically about data processing; how to create better, faster, more efficient data processing and storage. True I am neglecting some very interesting further applications of nanoelectronics, nanomagnetics, and nanophotonics such as sensing or interfacing to biology, but the great majority of the efforts are eventually geared towards building vastly more powerful calculating machines—computers that will allow us to design better space probes, predict the ocean currents, save our environment, create a virtual reality to surround us, and eventually help us think by rivaling the ability of the human brain.

We are immensely impressed with our brain and its many talents and are attempting to build intelligent machines of comparable abilities.

We're not talking about machines that can run MS Word five times faster or that can speed up our high resolution movies. To a large degree this workshop, in my opinion, is about providing the means to make a leap in creating much more powerful machines.

Operating processors have typically two ingredients. They have hardware and they have software, the machine and the program. We are largely the machine guys, the hardware people. More precisely, we are really the bricks and mortar—the ones that make the bricks and the mortar and the components. But just as importantly, we provide the scheme, how to build walls and houses from bricks and mortar, how to assemble the pieces into something bigger with a function. We're not the architects, the people that designed the building with basement floors, roofs, and the rooms. That is largely left to the computer scientists. But we have a huge impact on what edifice can be erected. We can change the preferred building material from brick and mortar to steel and glass and totally change what can be erected. We provide new opportunities, new options, to build more powerful data processors.

We have done this in the past and arrived at the silicon chip, the most complex man-made piece of machinery—almost a hundred million components, each one measuring less than one micrometer, all functioning. All [these components are] precisely interconnected according to a well-defined wiring scheme. It is an incredible result, perhaps the most incredible, of human ingenuity. It's powering our computers, our cell phones, our palm tops; it's controlling our car engines, flying our airplanes, creating our television pictures; it's running the Internet, our financial systems, and you could not enjoy Jurassic Park or the Matrix without it.

So what are the bricks and the mortars of the chip? They're basically switches and wires at its most basic conception—lots and lots of semiconductor transistors and miles and miles of metal wires. These are the components. The fact that we make the transistors out of silicon has given the name to the technology: silicon technology and the silicon chip.

So how did we arrive at today's state of the art? Scaling. Starting from the first processor with a few hundreds of components, each sized not much less than a millimeter, [we have scaled down to] today's microprocessor [,which] features millions of nanometer size components. Speaking of nanotechnology, this is it.

Smaller has always been better, in many ways. Smaller devices have smaller capacitances and inherently smaller distances for electrons to travel. Both decrease the time it takes to switch a

component. Smaller devices can be spaced more closely, decreasing the time it takes a signal to reach the next component. And as an added benefit, smaller devices require less energy to switch, reducing the power consumption of a given circuit. The additional added benefit today is turning out to be one of the most important limitations for processors. Power consumption and heat removal have become central concerns.

So, what has allowed us to arrive at today's state of the art in data processing? It's lithography. You may want to argue for silicon since it has this great oxide that allows us to grow amazingly thin gate insulators, or since it has a wide enough bandgap, or due to [its] good thermal and mechanical properties. I allege that all of these characteristics could have been met by other material combinations—maybe not as conveniently as they can be met in silicon; maybe at a higher cost; maybe somewhat later in time because of the additional research required. But we could have made gallium arsenide the semiconductor, in fact Seymour Cray did. We could have been able to work with MESFETs rather than MOSFETs. We have demonstrated that aluminum as well as copper wires work. We would have been able to avoid breakage, which has always been claimed as a major advantage of silicon. We could have avoided breakage of the wafers made from other materials. We would have been able to choose a material even with better thermal conductivity. True, in silicon we seem to be getting any of the desired characteristics just in one material. It's sort of the luck of the draw. But we would've been able to engineer around the shortcomings of other material combinations and arrive at processors that work just as well as silicon chips.

There's one thing that we would have not been able to do without, and that is lithography. In one sentence, in today's technology lithography determines the size of the components and implements into a physical structure the functional connectivity of the circuit. The first [of these roles], making small things, we can accomplish by various other means. The latter [role], connecting such things in a highly complex pattern, we do not know how to do without lithography.

Yes, we're able to make big things from small things. We can press and fire powders to make ceramics. We can mix molecules and make block copolymers. We can even grow periodic crystals from nanocrystals, from nanoparticles. But these are highly trivial structures on the scale of the layout of the microprocessor, or (if you wish) on the scale of the brain. They're either random arrangements of components or they're ordered, periodically in this case, and hence give us the expression "as boring as a crystal"—which in Fourier space is just a bunch of dots. It certainly is not a willful arrangement, that's for sure. In this case nature offers anything the architect wants as long as the architect wishes for what he gets. It's the saying that the Model T comes in any color that you want as long as it's black.

Lithography on the other hand gives us the whole spectrum of the rainbow. It allows us to create a physical relationship between any arbitrary two components by virtue of the interconnecting wire— whatever [relationship] you want. There certainly are better and worse physical implementations of a given functional map. It's a matter of optimization. But lithography can wire you anything you want, and it has been able to do this down to previously unimaginably small dimensions, from well below a micron to up to a centimeter long.

Silicon in principle is abandonable, lithography is not. Therefore we really should call it lithotechnology and not silicon technology. As we are approaching the limits of our human-made technology to create large data processors with nanosize components, we are contemplating alternatives to our present day approach. Extending the previously always successful paths of

scaling to smaller dimensions, we're pushing the limits of making components that are smaller yet than what can be projected from the ultimate silicon device.

Molecules represent an extraordinarily attractive alternative. Chemists can make molecules of a myriad of different designs. Our computer models are becoming sufficiently powerful to calculate their electronic orbitals and predict the electrical properties and how they will be affected by electric fields. Even on the scale of the less-than-1/1000th-of-a-penny silicon transistor, the cost of molecules is minuscule—typically ten dollars for 10^{23} switches. Silicon eat your heart out.

We have even created immensely impressive electrical wires which are nanometers in diameter that conduct electricity better than copper wires, and I am convinced we can make them sufficiently long for electronic applications. We have learned a lot and we're learning a lot about junctions between molecules and metals, although some of the things we learn only the second time around.

Such research is making enormously valuable links between the realm of chemistry and the realm of condensed matter physics. These disciplines are recognizing that their common future lies with molecules and molecular-sized options. We are learning to appreciate each other's abilities and learning each other's languages and lingoes. It is an enormously fruitful scientific undertaking.

However, most of the research is not addressing the lack of a suitable construction process. Either "How do molecules and wires fit into the lithography paradigm of creating the point-to-point relationship of a processor?" or "What could replace lithography to perform this task?" I allege [that] in this regard we are totally in the dark. There are attempts but none of them seems viable for large complex systems.

It may be that there's no better way to interconnect nanoscale objects in an arbitrary (as opposed to a random) way than to use lithography. After all this technology performs a sheer incredible task today and still has a few generations to go. What will this mean?

First of all, the end of scaling is not the end of performance. There are a few other tricks we can play when we reach the end of the litho growth. We can cool the stuff. We can make hybrids. We can use optics (some optics at least) on the chip, multichips, even superconductivity perhaps—but most of all, however, architecture and software. I once said in a talk, "The end of scaling is the end of the free ride for the computer scientists." They gave me a lot of grief. I was fiercely attacked. But I think it's true. At the stage when lithography has reached saturation, the computer scientists are our great hope to squeeze more out of the bricks and mortar. And they have ample opportunity to do so. Right now with 10^8 devices running at one gigahertz we have roughly 10^{17} operations per second. This is projected to reach 10^9 devices and 10 gigahertz, equal to 10^{19} operations per second. I know they may not all be running at the time; therefore give me ten percent of the 10^{19} which makes 10^{18} operations per second.

I now will do what it's always dangerous to do in such a talk, since it obviously puts one in a group of the unenlightened, and that is compare to the brain. I know, I know. I'm a moron. Let's just redo the old calculation anyway—10^{11} neurons, 10^4 synapses per neuron, at best 100 Hz, makes about 10^{17} synaptic operations per second. This is about equal to the number of operations [per second] of a Pentium chip today. It will be superseded by chips we can still project based on lithography.

I know you're going to tell me the brain works in a different way. Yes, yes, yes. But how many bits do you give me per synaptic operation? Ten? I don't give you more than ten. So [let's take] a ten bit analog depth. If you plug that in, today's microprocessors are comparable, in operations per second,

to what we think we have in our brains. It will take a few bits. So why do our Pentium chips run Excel worksheets, and [our brains] can come up with black holes and quantum mechanics? *Architecture* and *software*—the way these transistors are connected and run.

But of course why should we stop at this level of complexity? Let's see how much we can squeeze out of nature, how far we can go. And in any case data processing has many other probably even more demanding applications in limiting the brain. Maybe the brain ain't that good after all. It can't build an Airbus.

Since we are ready with a brain enhanced with biology, let's continue in a somewhat different vein. I allege there presently are only two technologies known to create large and complex systems on earth, lithography and biology—perhaps in the other order. As we're running into the limits of lithography we're often looking to our colleagues the biologists. On the things they are studying, [the work is] marvelous—extraordinarily complex. The DNA, the protein, the regulatory cycles, the cell, the motion, their channels, the organisms that build on them. And most directly, comparison to brains— no doubt the greatest unbelievably complex structure, [which] has solved the three dimension connection problem in the most amazing fashion that we do not understand yet. And it represents the most powerful data processor. However, one also needs to acknowledge the shortcomings of the design.

I know this sounds a little bit like hubris. But let's face it; the axon is a most cumbersome design for signal transmission—a long thin post filled mostly with water and some potassium and sodium, with a wall that pumps these ions periodically in and out in a bucket-brigade fashion with a transmission speed of ten meters per second. Such a signal transmitter would not get very much attention on the design screens of Intel. Our electronic signal travels at the speed of light—at least a good fraction of it. This is a difference of a factor of 10^7, hence our processors run at 1 GHz and [for] a brain (if you want to attribute a cycle time to it), it's 100 Hz.

It's often said that the reasons for the brain's ability may be its parallel design and its relatively slow transmission speed. I'm not a subscriber to the sentiment. The brain is designed from components of biological objects, which are the cells [whose] original function is chemical and not electrical. The cell had once been a single-cell organism that had no ability to think. When signal transmission became important, nature took what it had—a lovely chemical factory—and ingeniously transformed it into a lengthy signal transmitter. The axon is probably the best way you can do this out of the cell. The same is probably true for the synapse. Many different chemicals and nanosize objects are required to transmit an action potential across a synapse.

It is a big shortcoming of Mother Nature, not having discovered the metal wire and electronic switch. With the slow speed of components of biology, what do we do to increase performance? You have only one choice—parallelize. The fact that the brain is highly parallelized is a result of the slow characteristics of the components and not the other way around. The components are so slow that the brain can take advantage of parallelism.

So, is biology then a poor guide to create higher performance data processors? In my opinion, the answer is 'yes' and 'no.' Yes, biology is a poor, poor guide in terms of the implementation of electronic devices. Mother Nature is not a very experienced engineer when it comes to the handling of electricity—apart, perhaps, from the electric eel, and it ain't that impressive. In the world of data transmission the electric wire stands tall. I allege this to be true for any short distance, with a glass fiber waiting for the long haul.

In a certain sense, I regard the copper wire as the greatest invention of all of electronics. It transmits signals with the speed of light in one dimension, being only of nanometer size in the other two dimensions.

A similar statement holds, in my opinion, for the required non-linear elements in most any realistic implementation of a computation fabric. The simple electronic on/off behavior of transistors or even of individual molecules, designed for this purpose, outstrips the ability of any chemical machinery that [one] would try to manipulate.

So much for biology being a poor guide for electronics. On the other hand, biology is enormously powerful in assembling things—the wiring of the brain, and in general any kind of nervous system, being one of these immensely impressive processes in which an axon is growing from a giraffe's brain to find its receptor some meters down at the end of the spine. We don't know how to do something like this in electronics, nor do we know how to assemble anything complex in three dimensions. Biology is a master at it, no doubt. You can learn a tremendous amount [about] how to build things from biology, even if we think that the starting materials are poor for our purposes.

We may be able to translate processes and schemes to other environments. The aim is not to build a magnetic cockroach—although they may be not too bad to catch—or an electric dog. The aim is rather to learn small-scale biological processes and see whether we can translate them, to learn how molecules can be made, can be moved, can be assembled, can be copied, can be rotated, can be catalyzed, can be deposited, can walk on surfaces or along ropes. What kind of regulatory cycles exist? What feedback loops are in action?

Biologists, with the help of some people with our kind of background, are doing a very good job in deciphering these elemental steps. We kind of guys, the chemists and the physicists in the wider sense—meaning including the development engineering disciplines such as [electrical], mechanical, chemical—we ought to start looking at such things in non-biological molecules. Can we make a molecule crawl on the surface, perhaps powered by light or by other molecules in solution? Can we detect this motion? Can we have it rotate around a pivot? Can we make a molecule reproduce itself to be a template for another one? Can we have a molecule sense the presence of another one and report on it, perhaps in an electrical fashion? Can we play the game of molecular dynamics on a small scale, in analogy to biology, but with non-biological molecules that have more appropriate electrical characteristics?

I realize this is an enormous challenge. I also lay no claim to the originality of such thoughts. This should not make it less exciting. There are even some—mostly chemists—that are making small steps in this direction. I find it the most exhilarating research direction. In the long run it will enable us to create complex self-assembled non-biologic entities that may provide a new paradigm for the construction of a powerful data processing means. Probably [these will be] hybrids with lithographically constructed backbones in the short run, but all self-assembled in the long run. I also realize that this is a long path. There are ways proposed very different from basically digital electric data processing. Let's all have a shot at it.

So, after this long and wordy exposé, and without showing any viewgraphs—and hence, having everybody's brain gyrate—what [am I] saying? I think lithography is carrying us to the edge of a plateau. If you want to do better than litho, you have to teach wires and switches. You have to teach them how to smell, how to cut, and how to graft. Thank you.

2. Acquisition of Information

Participants: Steve Blair, Gail Brown, Leon Chua, Paul Evans, Anupam Madhukar, Scott Meller, Charles Paulson, Axel Scherer

VISION

Nanotechnology will play important roles in improving the performance of individual sensors and in manufacturing high-performance sensor arrays. It will facilitate integration of sensors with other information processing components and allow deployment of low-power sensor systems in previously impractical applications. Nanotechnology gives designers powerful means for tailoring the electrical, optical, and magnetic response of sensors, for modifying a sensor's external characteristics to ensure compatibility with and endurance amidst its operating environment, and for implementing advanced sensing algorithms utilizing multiple interconnected interacting devices.

Nanofabricated antennas and emitters can be designed to efficiently couple light into or out of devices across the electromagnetic spectrum. They will be utilized in transducers and to facilitate highly sensitive spectroscopies. The low-noise, low-signal performance of nanostructured magnetic sensors—successors to the giant magnetoresistance (GMR) read heads widely touted among the early commercial successes of nanotechnology—will continue to improve, and they will become critical components of spintronic systems (see Chapter 3). Nanoscale chemical or biological detectors responding to individual molecules of a given species will become commonplace; this sensitivity will be of paramount importance in designing medical interventions at the molecular level, and also in responding to biological or chemical hazards.

There are many enabling technologies for nanoscale acquisition. For nanometric light sources and nanoantennas—essential building blocks for nanophotonic sensors—researchers typically rely on semiconductor quantum dots (QDs) or plasmonic nanostructures to couple optical wavelengths to smaller (nanoscale) devices. Both approaches offer efficient, tunable coupling across much of the electromagnetic spectrum. They can be used with electro-optical transducers or to enhance spectroscopic techniques including Raman scattering, fluorescence resonant energy transfer, and surface plasmon enhanced fluorescence. Nanostructured probe tips can improve the resolution of near-field nanoscopic imaging tools.

Natural and artificial nanopores and nanotubes are additional enabling technologies, useful in a variety of nanofluidic, biosensor, and molecular electronics devices. The unique mechanisms nature has evolved for efficient recognition of molecules, including complementary pairing of DNA and antibody-antigen matching, will also be adapted for use in human-made nanosensors.

The successful development of left-handed nano-optical materials (exhibiting negative index of refraction in the optical regime) would provide another route for enhancing nanophotonic devices. A simple slab of left-handed material forms a "perfect lens" [1] that can focus light to a spot much smaller than the Rayleigh limit.

Many advanced sensors will rely on hybrid nanotechnology combining the lithography and materials modification tools of semiconductor nanomanufacturing with techniques from biotechnology and

microfluidics. New design pathways encompassing both the biological and human-engineered worlds will be broadly applied to improve traditional sensors and will enable novel sensors and sensing applications. For example, sensors merging living cells with electronic devices could serve as an artificial immune system—an ultrasensitive laboratory for rapid detection of biological pathogens or for testing pharmaceutical responses to those pathogens.

The development of nanoscale sensor arrays relies on two essential capabilities of nanomanufacturing. The minuscule size of nanosensors is more than a matter of definition; it is a feature allowing the creation of compact, inexpensive arrays containing large numbers of detectors. The potential to combine many distinct technologies and processes at the nanoscale allows designers to integrate intelligent processing into sensor arrays and to ensure compatibility with a variety of operating environments. Together, these capabilities enable the creation of nanosensor arrays that can autonomously adjust their dynamic range or spectral operating band to match changing environmental conditions. These smart, adaptive, multimodal arrays will feature sensitivity and dynamic range enhanced by several orders of magnitude over raw signal detection, perhaps using architectural organizing principles and processing schemes similar to those found in the sensory systems of biological organisms. These principles serve as enabling tools for working on a diverse range of acquisition problems. Applied *in vivo,* smart acquisition and processing could empower neural prosthetics that restore or augment damaged vision or memory.

CURRENT STATE OF THE ART

Emitters and Antennas

Nanoscale nearfield excitation sources can be constructed for controlled emission across the electromagnetic spectrum, from the ultraviolet through the visible to the infrared (IR) and beyond. Nanoantennas serve as efficient input couplers to nanoscale devices across this same spectral range.

Semiconductor quantum dots have electromagnetic properties that can be tuned via quantum size effects. Two independent classes of semiconductor quantum dots have emerged with considerable potential for advancing nanoscale processing, communication, and sensing—where they can be used as nanoantennas and as nanometric light sources. These are epitaxial island quantum dots formed on a crystalline substrate such as indium arsenide/gallium arsenide or germanium/silicon, dubbed self-assembled quantum dots (SAQDs) [2, 3]; and colloidal nanocrystal quantum dots (NCQDs) such as cadmium sulfide, cadmium selenide, core-shell cadmium selenide/zinc sulfide, or indium arsenide/zinc selenide, which form in solution [4, 5]. Self-assembled quantum dots have been incorporated in ultralow-threshold and high-speed lasers [6] and long-wavelength infrared detectors [7]. These advanced devices are already competitive with the established quantum-well-based devices, and hold promise for significantly higher performance. In contrast, colloidal nanocrystal quantum dots have primarily been utilized as improved luminescent labels for biological molecules and cells in solution or adhered to surfaces [8–10]. NCQDs with transition energies in additional spectral regimes have recently been developed. In particular, indium arsenide/zinc selenide nanocrystals and lead-salt semiconductor nanocrystals (lead sulfide, lead selenide, lead telluride) [11] have strongly size-quantized optical transitions in the near infrared. Fabrication problems have been solved with the demonstration of monodisperse colloidal synthesis [12]. Unique and novel quantum nanostructures can be created by integrating different types of semiconductor quantum dots. These hybrid structures are being investigated for information sensing and processing in ambient and solution environments, and could enable breakthroughs in information sensing, transduction, and amplification [13].

Plasmonic nanostructures can also serve as efficient couplers from the nanoscale to optical wavelengths. Using quantitative predictive methods developed over the last few years, these structures can be designed to focus micrometer-scale light into nanoscale volumes with high spatial and spectral control. For example, core-shell dielectric metal geometries—or plasmonic nanoshells (Fig. 2.1)—have been shown to have sharp, tunable plasmon resonances [14], and can be used as optical nanoantennas for efficient coupling to light at any visible or IR frequency. Plasmonic nanoantennas can be designed to focus micrometer-scale light into nanoscale volumes with high spatial and spectral control of the concentrated energy. Bow-tie nanoantennas (Fig. 2.2) can efficiently concentrate light into 10 nm gaps, with local field enhancement up to 10^4 [15]; C-shaped metallic apertures possess similar properties [16]. Bull's-eye structures (Fig. 2.3) transmit 125 times more light than an equivalent aperture with no surrounding nanostructure [17]. Periodic arrays of nanoapertures in a metal film [28, Fig. 2.4] can also exhibit enhanced light transmission properties.
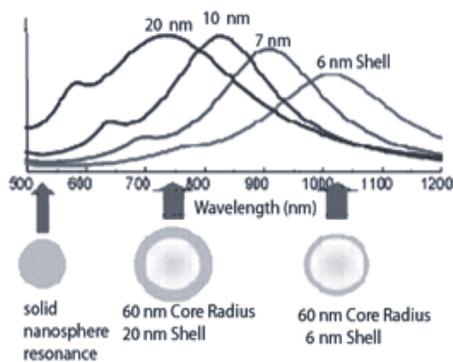
Figure 2.1. Silica core–gold shell nanoshell resonances as a function of the core–shell ratio *(*courtesy of N. Halas and J. West, Rice University).
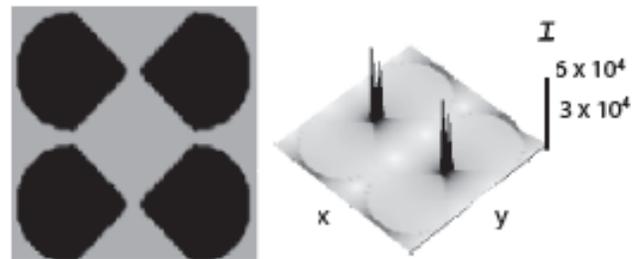
Figure 2.2. Bow-tie nanoantennas and enhanced local fields calculated for λ=0.5 and 0.8 μm (courtesy of V. Shalaev, Purdue University).

(a)

(b)
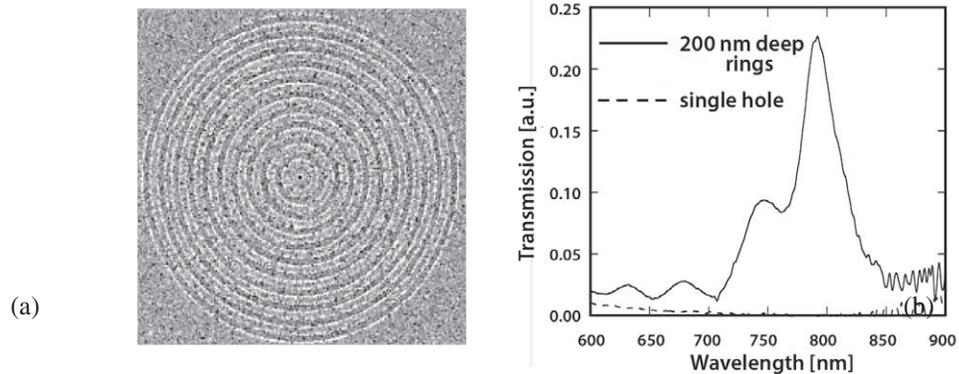
Figure 2.3. (a) Electron micrograph of a bull's-eye nanoantenna, a single sub-wavelength aperture with surrounding periodic surface corrugation. The concentric ring pattern was milled into a sapphire substrate, which was then overcoated with 300 nm of silver. As a final step, a 200 nm diameter aperture was fabricated at the center. Bull's-eye structures create a region of high electric field near their central aperture when light is incident at the resonance wavelength. A portion of the concentrated field evanescently couples through the aperture and radiates into the far field. (b) Zero-order transmission for the bull's-eye structure and an equivalent bare aperture, with normal incidence optical illumination. The traces correspond to measurements obtained using a white light source. The wavelength of peak optical transmission is determined by the groove periodicity and the effective refractive index seen by the surface plasmon wave that mediates the transmission. The geometry of the corrugation on the back side of the structure greatly affects the nearfield and farfield radiation patterns (courtesy of A. Nahata, University of Utah).
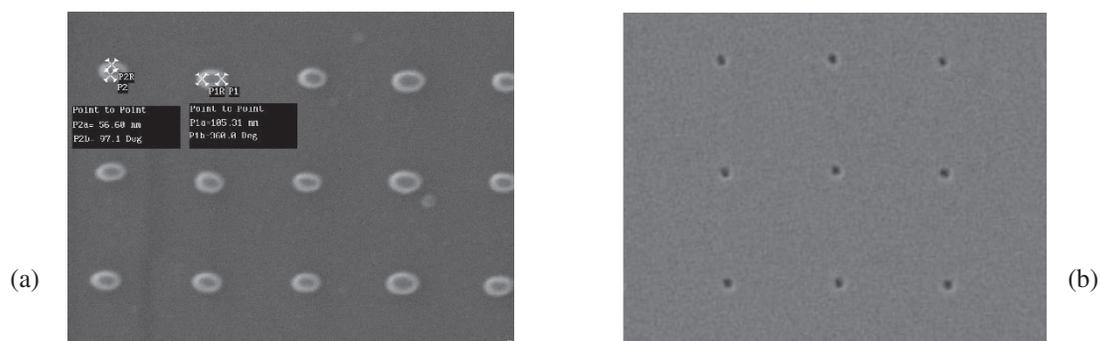
Figure 2.4. (a) Periodic array of elliptical gold nanodots, which are roughly 57 nm by 105 nm (courtesy of S. Blair, University of Utah). (b) Periodic array of metallic nanoapertures in gold with lattice spacing of 1 μm. Incident light of a frequency which excites surface plasmon modes enhances the electric field in the aperture [33]. Molecules located within the nanoapertures therefore experience enhanced optical excitation [34] and enhanced fluorescence. Their fluorescence signal is strongly isolated from that produced by molecular species lying outside the nanoapertures [35].

Molecular Detection

The development of sensors with single-molecule sensitivity and high selectivity hinges on the integration of biological molecules with other organic materials. Nucleic acids, antibody/antigen pairs, or other receptor systems provide selectivity while simpler chemistry activates or passivates the sensor. The potential of such integration has been demonstrated through construction of sensors for specific antibodies or molecules and for oligonucleotide sequences [18]. Most of these sensors have been formed as bulk devices, but their nanoscale analogs have already been shown to have high sensitivity and to offer the possibility of designed-in functionality using well-defined interfaces [19].

A variety of strategies have been developed for forming biological/inorganic interfaces. Much of the early work focused on thiol-metal driven self-assembly [20]. A common approach is to thiolate the biological system and directly attach the molecule of interest to the surface. Another approach is to coat the metal surface with a terminally functionalized organic thiol, which, in turn, binds to a biomolecule. Because of the weak nature of the metal/thiol bond and the propensity for the thiol linkage to be electrically insulating, more recent work has focused on other chemistries. These new approaches include attachment to the metal surface through nucleotides and modification of semiconductor oxides with molecules, such as biotin, that act as binding receptors for other biomolecules.

Nanoantennas have been used extensively in molecular detection. For example, metallic nanoparticles or semiconductor quantum dots attached to molecules can function as mass labels [21], fluorescence labels [22], and light scattering labels [23, 24]. Nanostructured metallic surfaces have been studied extensively for surface-enhanced fluorescence [25] and surface-enhanced Raman scattering [26], where single-molecule detection can be obtained [27]. Increased quantum yield is one benefit to placing a fluorescing molecule near a metal surface. Quantum yield is a strong function of the surface–molecule separation, reaching its maximum in the 3 to 10 nm range [25, 28]. A major drawback of surface-enhanced techniques is that if the nanostructure is random (or possesses fractal order), the enhancement factor varies spatially, leading to random hot spots on the surface [29]. The hot spot effect makes these techniques unsuitable for quantitative detection, especially in an array format, as

the average enhancement may be small and the enhancement from zone to zone may vary. This has stimulated efforts to attach molecules to lithographically defined arrays of metallic nanoparticles [30, 31] or nanoapertures [32, 34]. With these architectures, uniform nanoparticle size, shape, and spacing result in enhancement factors with well-defined magnitude and spatial location.

Natural and artificial nanopores and nanotubes have demonstrated their efficacy in nanofluidic, biosensor [35], and molecular electronics devices. Self-assembled alumina nanopores, for example, can be used directly in a variety of devices or can serve as templates for constructing metallic, semiconducting, and dielectric nanotubes [36]. Lithographically defined nanopores have been used to measure molecular conductivity [37]. Nanopores integrated with silicon MOSFET technology may allow the real-time electrical identification of molecules passing through the pore [38].

Nanoscale Imaging

Nanoantennas can enhance a number of optical and non-optical imaging modalities. Semiconductor nanocrystals have been employed as nanoscopic fluorescent sources in biological media [39]. Metallic nanoantennas, which do not suffer from photobleaching or "blinking," can provide nanoscale contrast in scanning electron microscopy [40], single- and multi-photon optical imaging methods [41, 42], surface-enhanced Raman scattering [43], and magnetic resonance imaging [44]. Nanoantennas can be functionalized to recognize a specific target, enabling intracellular imaging of specific proteins [45] and targeted phototherapy [46]; both techniques rely on strong optical absorption and subsequent heating in a nanoscale volume. In photothermal microscopy, changes in the optical properties of the absorber induced by this local heating are monitored with a probe beam [45, 47].

Several different nearfield probe configurations incorporating nanoantennas have been developed over the last decade, and have demonstrated resolution well beyond the classical Rayleigh diffraction limit. One method for overcoming the diffraction limit is nearfield scanning optical microscopy (NSOM) utilizing tapered metal-coated probes [48, Fig. 2.5]. Apertureless techniques involving localized dipole scattering of laser light from a sample have also demonstrated high spatial resolution (<30 nm) and for inhomogeneous materials further exhibit chemically specific dielectric responses [49, Figs. 2.6 & 2.7]. Tip fabrication is easier for apertureless nearfield techniques than for aperture-based NSOM. A hybrid probe, having a metallic antenna extending from the aperture of a conventional NSOM probe, has also been demonstrated. This enhances the throughput of NSOM relative to conventional probes, and produces a sharper tip [50].
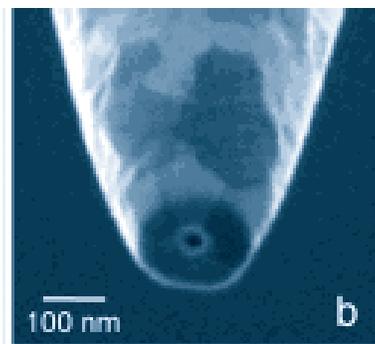
Figure 2.5. Apertured NSOM probe tip (courtesy of N. Van Hulst, Institute of Photonic Sciences).
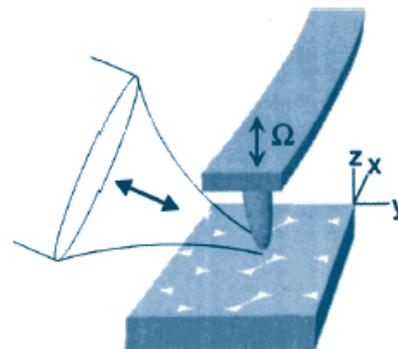
Figure 2.6. Apertureless NSOM probe (courtesy of F. Keilmann, Max Planck Institut für Biochemie).
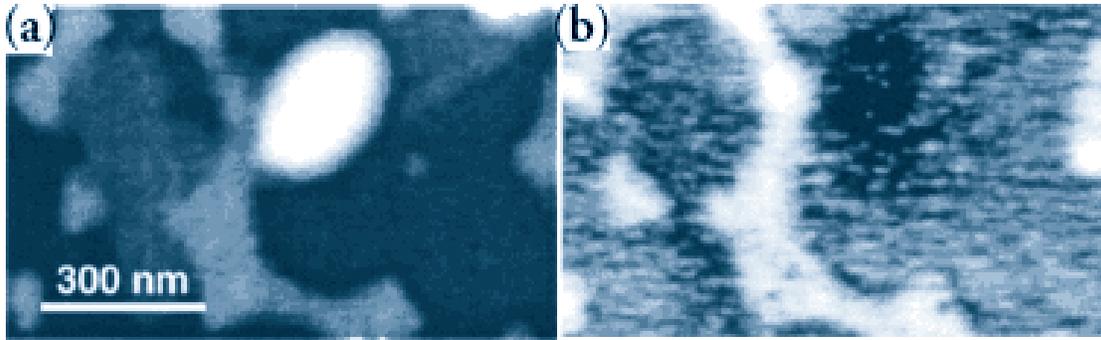
Figure 2.7. (a) Topography of gold patterned on silicon and (b) the corresponding nearfield optical image at 633 nm (courtesy of Keilmann, Max Planck Institut für Biochemie).

Proof-of-principle experiments on negative index materials—in which the negative dielectric permittivity and permeability result in a negative refractive index, implying that electromagnetic waves propagate with phase velocity in the opposite direction to energy flow [51]—have been performed in the microwave regime [52]. Efforts to extend this phenomenon to the optical regime are underway. Theory predicts that plasmonic nanostructures consisting of closely spaced pairs of nanowires [53] can act as a left-handed optical material, enabling the focusing of light to a spot size in the tens of nanometers range.

Apertured probes of metal-coated silicon have been developed for scanning microwave microscopy [54, 55]. Mechanical probes with resonant frequencies of 100 MHz and beyond have been demonstrated [56, Fig. 2.8]. Magnetic dipoles on cantilever beams demonstrate high sensitivity to 10 GHz magnetic fields, which can be monitored concurrently with topographic mapping [57]. Ultrafloppy magnetic cantilevers with unprecedented force sensitivity are capable of sensing the drag induced by a few magnetic nuclei in magnetic resonance force microscopy [58], and promise the chemical specificity associated with magnetic resonance techniques. So-called protein pulling techniques, a sort of force nanoantenna in which the force between a protein and a cantilever is monitored as the protein is pulled apart, have also emerged [59, 60].
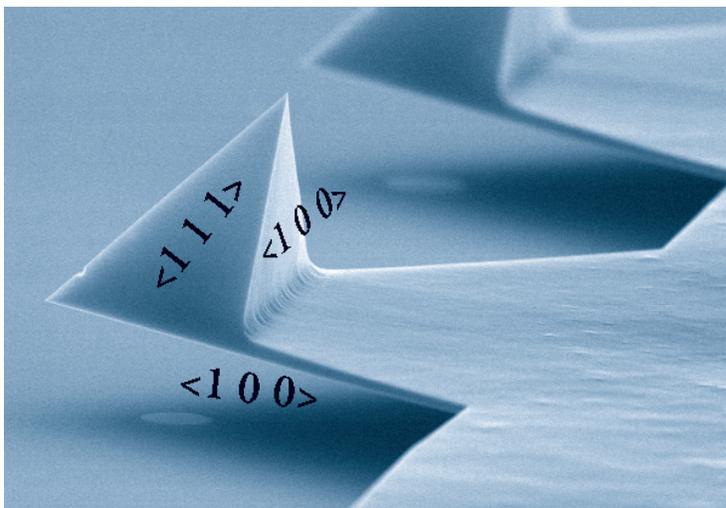
Figure 2.8. Single-crystal cantilevers with resonant frequency up to 100 MHz (courtesy of Kawakatsu, Univ. of Tokyo).

Acquisition of Multispectral Signatures

Nanostructured devices offer detector designers new combinations of selectivity and tunability, and show great potential for multispectral and hyperspectral measurements. Quantum dot infrared photodetectors with long wavelength detectivities ~10^{11} cm-Hz$^{1/2}$/W at 77 °K have recently been demonstrated, with sensitivity in a narrow spectral band which can be shifted by design. Infrared diodes utilizing superlattice materials can be tailored to detect wavelengths anywhere between 2 µm and 30 µm. Carbon nanotubes on a silicon substrate have recently been shown to have an infrared photoresponse [61], and a crystallized biological molecule has been reported with high sensitivity in the ultraviolet.

Wavelength selection and multiple wavelength detection can be achieved within a diffraction-limited spot using nanoantennas. A recent demonstration exploited the shape dependence of the spectral response of metallic nanoparticles for plasmonic nanoparticle data storage, using an arrangement of multiple nanoparticles within a single, optically addressable, spot to spectrally encode multiple data bits [62]. The ultimate spectral selectivity of this technique and its applicability to more general acquisition problems remain open issues.

Nanotransducer Design and Characterization

The theoretical description of the adsorption of molecules at inorganic surfaces has traditionally been based either on fully quantum mechanical models (often using the techniques of density functional theory) or phenomenological models such as molecular dynamics. The computationally intensive quantum mechanical descriptions are at present limited to the order of hundreds of electrons. The successes of the fully quantum mechanical approach are therefore limited to small systems (i.e., the interaction of a few molecules with metal surfaces), for which it produces highly quantitative results. Techniques such as molecular dynamics using pseudopotential interactions can scale to several million atoms. They have shown great promise in describing self-assembled monolayer systems and polymer nanostructures, both potentially useful for nanotransducers.

Traditional biological and chemical characterization techniques have been of limited use in probing designer interfaces. The development of these interfaces has instead been based on characterization via structural scattering probes and surface science techniques such as scanning microscopy, area-integrated spectroscopy, and electronic structure probes.

Intelligent Nanoarrays

Current schemes for the integration of adaptive processing with nanoscale acquisition emphasize cellular architectures with local interactions between cells. Preliminary CMOS-based cellular nonlinear network (CNN) technology allows the integration onto each pixel of up to 25 nanoantennas, spanning a spectrum from the infrared to visible light. In addition to nanoscale sensing, *on chip* CNN processing via recently developed excitatory-inhibitory twin wave computing principles can be applied to enhance sensitivity and selectivity by orders of magnitude [63]. Locally active biomaterials such as bacteriorhodopsin can be used to provide pixel-by-pixel local memory, thereby enabling smart processing in real time [64].

HARD PROBLEMS

Emitters and Antennas

SAQDs are formed on a solid substrate and are inherently compatible with the hierarchically organized component architecture that has been so successful in electronic and optoelectronic microsystems. If NCQDs are to become important enablers of advanced electronic, photonic, and magnetic devices, they too must be fabricated and their functionality preserved within this architecture. Integration of NCQD fabrication with optoelectronic and electronic processing is a hard problem involving disparate materials normally used in different environments. Progress is being made towards achieving functions such as stimulated emission from quantum dots embedded in polymeric solid matrices. Successful development of hybrid integration techniques would allow sensor designers to combine nanocrystal QDs and epitaxial QDs, enabling breakthrough concepts for truly novel acquisition devices.

Improving Sensitivity While Maintaining Selectivity

The enormous surface-to-volume ratio of nanowires, quantum dots, and other nanoantennas provide modalities for detection and identification of molecules at levels better than parts per billion. This exquisite sensitivity is, however, accompanied by an enormous burden on specificity. If nanosensors are to provide effective means for deterring or remediating chemical, biochemical, and biological threats, they must provide high sensitivity *and* selectivity in harsh environments. Inadequate specificity would result in many false positives and render the sensor ineffective. Several known approaches can deliver the required specificity in the laboratory—for example, antibody-antigen reactions or the hybridization of single-stranded DNA to form a duplex—but their effectiveness in quantitative field applications is usually limited by the thermodynamically defined affinity kinetics of competing molecules. Finding ways to create highly localized differential affinities between actual targets and competing species, while maintaining high sensitivity, is a difficult challenge.

Multimodality and Materials Integration

Many advanced nanoelectronic, nanophotonic, and nanomagnetic devices involve interfaces between different materials, often belonging to different operational classes (such as semiconductors, insulators, conductors, or magnetic materials) and chemical classes (such as inorganic, organic, or biochemical). Design and manufacture of devices utilizing several classes of materials, and control of the interfaces between them, pose difficult problems.

To combine multiple nanoscale materials or functions into compact devices, researchers must explore materials and processes, develop models, and build prototypes. This requires addressing a wide variety of issues including selective deposition of different materials in a controlled area, integration of disparate materials and processes, interconnectivity between different functions, and fusion or readout of multiple signals.

The integration of molecular sensing with electrical and optical systems depends on the chemical functionalization of inorganic surfaces. To adequately control the chemical selectivity, electronic properties, and optical response of a sensor, breakthroughs are needed in the design and fabrication of nanosystems integrating materials whose compatibility is presently limited.

New chemical and physical techniques must be developed for the formation of controlled interfaces between biological or chemical species and solid materials. The framework for understanding the

structure and electronic states of compound semiconductor–semiconductor or silicon–silicon dioxide interfaces is quite well established, and descriptions of the semiconductor–metal interface are reasonably well founded. The understanding of semiconductor–organic and inorganic–biochemical interfaces is far less mature.

In addition to the interfaces within sensors, there is an interface between a sensor and the environment in which it is to be employed. The abiotic–biotic interface between the human body and devices such as artificial retinas or implanted glucose sensors is perhaps the least examined. A device must not be recognized as foreign or it will provoke the body's inflammatory response. One fundamental approach to creating biocompatible devices is to apply surface coatings that mimic biological materials. Development of this biomimetic approach will require improved understanding of inorganic–polymer coatings and of interfaces involving novel hybrid biomaterials such as inorganic polypeptide–peptide polymer coatings, which are virtually unexamined to date.

Nanotransducer Design and Characterization

The surface analysis tools that have contributed to our current understanding of nanoscale interfaces will undoubtedly be extended to higher spatial resolution and new spectral regions. While extensions of present computational and characterization techniques will have some impact, new strategies are required to meet the challenge of materials integration over large areas, in appropriate ambient environments, and at potentially heterogeneous interfaces.

Modeling of nanotransducers will require accuracy approaching that of quantum mechanical calculations for systems of a size currently only amenable to molecular dynamics or similar phenomenological approaches. Multiscale approaches have successfully been applied to describe the dynamics of bulk structural defects [65]; these length-scale-bridging techniques should be adapted to help understand the properties of large molecules at surfaces well enough for use in accurate simulations of nanosensors.

Biological molecules are orders of magnitude larger and will require unique new tools, but could enable a new class of sensors and integrated materials. The electrical and optical properties of molecules are at the heart of their promise as sensors, but are understood only in limited circumstances.

Identifying the nature of the fundamental issues of biocompatibility is a hard problem requiring the development of techniques for nanoscale characterization in a physiological environment and the definition of figures of merit or other performance metrics. Advances in materials design, synthesis, and testing are needed to develop biocoatings combining nanoscale uniformity with other desired features such as controlled drug release.

Intelligent Arrays

Developing adaptive nanoscale acquisition arrays that autonomously adjust their dynamic range or wavelength band to match time-dependent environmental conditions presents many challenges. One approach is to mimic nature's techniques for sensitivity enhancement and dynamic range expansion by interfacing nanoscale sensor outputs with CMOS components in a cellular architecture incorporating lateral inhibition and pixelwise adaptation. Another approach is to design multifunctional materials with inherent capabilities such as sensitivity to multiple spectral bands or polarization diversity. Selectively combining different quantum engineered materials to create multifunctional capabilities within an imaging array is a challenging but important enterprise.

The degree to which noise and fluctuations influence the output of nanoacquisition systems is a key parameter in the design of devices. The scaling of noise (*1/f*, shot, chemical attachment and detachment) across large numbers of devices and throughout sensor systems will be a critical issue. Statistical methods that have evolved to describe interface chemistry must be extended to the few-molecule limit for use in sensor design.

STRATEGIES AND NEEDS

If new acquisition schemes are to achieve commercial success, several challenges must be overcome. Lack of nanotechnology manufacturing and analysis equipment is a roadblock to innovation, as is lack of modeling tools. New characterization tools are needed to analyze nanoscale interactions. Accurate models of material interactions must be developed and proven, allowing researchers to progress apace by simulating sensor behavior before investing in device fabrication. Inexpensive prototyping and low-volume production capabilities would also speed innovation.

In many applications of nanosensors, transduction will occur on the nanoscale while a macroscale result must ultimately be reported. Interfacing and packaging of nanoacquisition systems to the bulk world needs attention and should be pursued in parallel with system designs (see also Chapter 6). The history of the microelectromechanical systems (MEMS) industry reveals that volume manufacturing of lab-proven sensor designs can be difficult, and that efficient and effective device packaging is often a roadblock.

Many of the hard problems identified in the previous section involve integration of disparate materials. Interfacing organic systems with inorganic sensor elements involves problems at a range of length scales, from deposition of films a single atom thick to the conformation of large macromolecules. Developing nanosensors for harsh environments is no less difficult. Solving these problems will depend on understanding process protocols from multiple disciplines and will require colocated processing and characterization equipment. There is a critical need for centralized, user-fee-based facilities that provide researchers and educators access to and expertise in multiple fabrication processes and characterization tools.

The unprecedented analytical capabilities of nanoscale characterization tools are now typically available only in relatively large instruments optimized for specific tasks. We have only recently begun to explore compact analytical systems exploiting the miniaturization and integration options afforded by nanotechnology. Compact systems promise faster analysis, of smaller volumes, with greater sensitivity. NNI programs should encourage researchers to develop systems integrating nanoscale sensors and picoliter sample manipulation.

New materials and device structures should be explored to extend the spectral range of nanophotonic detectors. A variety of wide bandgap nanodots and nanowires should be studied to select the most promising materials for ultraviolet detection. Quantum structures for efficient terahertz detection should be explored in depth. Models for predicting the optical and electrical properties of complex quantum dot or quantum wire heterostructures need to be developed so that the materials and structures can be optimized for highest sensor performance at a given wavelength. Plasmonic nanostructures consisting of closely spaced pairs of nanowires [52] should be evaluated, along with other candidate left-handed optical materials, to enable the focusing of light with resolution in the tens of nanometers.

The continued development of quantum dot photodetectors requires improvements in several areas including control of growth processes, theoretical description of quantum states and electron transport mechanisms, and models for device design. Combinations of QDs with other nanophotonic structures should be explored to enhance optical absorption in thin or small volume devices. To perform spectroscopy on an imaging array, control of both dot size and location is essential. Similar issues should be addressed for semiconductor nanorods or quantum wires.

There are multiple directions worth pursuing to build on rapid progress in nanoantenna design, due in part to the success of first-principles computational modeling [66]. One direction is to develop inverse design methods for multifunctional mappings between the macroscale and the nanoscale, including space variance, polarization state, and spectral content. Another possibility is to design assemblies of nanoantennas for tomographic reconstruction via multispectral nanoscale imaging; each nanoantenna could be functionalized to recognize a specific molecular or chemical target. The related technique of fluorescence nanotomography, which determines molecular distributions based on the modification of fluorescence lifetime via resonant energy transfer among multiple fluors [67], has been applied to porous polymers and biomolecules. It could be extended to more general structural imaging utilizing nearfield interactions among nanoantennas.

Multiscale theoretical and computational techniques should be developed to describe the properties of interfaces including several large molecules, an area of the surface, and the surrounding environment. These may be based on extensions of present approaches or on new scaling paradigms.

Nanoscale characterization techniques such as confocal microscopy and nearfield scanning optical microscopy do not yet have adequate spatial and temporal resolution to address critical, fundamental issues underlying molecular detection. These techniques must be improved and new techniques developed to provide the quantitative information on chemical, optical, and electrical signatures of target species needed for nanosensor design. Goals should include higher resolution (~ 20 nm) and simultaneous subpicosecond time resolved detection in NSOM; multiphoton spectroscopy in the 50 nm range; and flow chambers designed for few-microsecond measurements. For biochemical and medical applications, the identification and synthesis of biocompatible intracellular probes with improved luminescent characteristics is one approach worthy of investigation. Scanning confocal arrangements (in which both incoming excitation light and outgoing fluorescence pass through a high numerical aperture objective) could be particularly interesting for improving the performance of nanoparticle-array-based sensors. Techniques involving higher order processes (such as surface-enhanced Raman scattering or multiphoton fluorescence) can have strong isolation and should also be explored in conjunction with nanoparticle arrays.

Biomimetic sensing is one promising approach for developing intelligent adaptive sensors. Nanoelectronic, nanophotonic, and nanomagnetic transducers can be leveraged with biology's organizing principles to design smart, adaptive, multimodal sensors. Nature has over eons evolved sensing architectures that greatly enhance sensitivity, selectivity, and dynamic range. Our vision and hearing both exploit array architecture and provide models of smart sensing. The human retina can process a single photon of light in a darkened room, or the flood of photons in a sunlit scene, providing over 10 decades of dynamic range by adapting its response based on the brightness of the visual scene. The human cochlea can detect weak sounds in silence, yet distinguish the voices of multiple speakers in a noisy room (the "cocktail party effect") due to a structure that provides spectral analysis of the auditory environment. Nature has also evolved unique mechanisms for efficient recognition of molecules, including complementary pairings of DNA and antibody-antigen matching. These are enabling principles for working on a diverse range of acquisition problems,

including the identification of individual molecules, real-time nanoscale imaging, and the acquisition of multispectral signatures from the terahertz to the ultraviolet. They can also be used to augment biological sensory systems; applied *in vivo*, smart acquisition and processing could be incorporated in neural prosthetics that restore or supplement damaged vision or memory. Significant enhancements to the performance of sensor arrays may be achievable by utilizing CNN technology with pointwise local adaptation and lateral inhibition [68, 69]. The cellular architecture could be combined with the local activity principle from nonlinear electronics to develop adaptive single chip sensors with orders of magnitude improvements in sensitivity, selectivity, and dynamic range.

PRIORITIES AND CONCLUSIONS

NNI programs should continue to fund basic research at university and government laboratories, initially exploring a wide variety of potential approaches to nanoscale data acquisition. Government should also provide opportunities for small businesses to further develop promising materials and devices.

Short-term programs should:

- Focus on developing nanomaterials-based acquisition schemes that do not require physical connection to the macro world
- Utilize "stand off" interrogation of sensor arrays via optical or electromagnetic means
- Emphasize development of sensing methodologies that are quantum leaps over what is available today

Long-term programs should:

- Focus on effective manufacturing approaches that fit with emerging interconnection schemes
- Develop statistical approaches to make intelligent decisions fully utilizing multiparameter sensing platforms
- Utilize high sensor counts to reduce cross sensitivities and false positives

Funds should be dedicated to building university-based laboratory infrastructure supporting multidisciplinary activities. The critical need for shared, high-availability processing and characterization equipment should be addressed at an accelerated pace. Separately, the development of major national facilities housing more highly specialized or unique equipment should continue.

The development of integrated nanobiotechnology systems and their deployment at the frontiers of biological investigations are just beginning. Timely nurturing through the NNI could enhance and accelerate these efforts. NNI programs should promote opportunities for developing common platforms that merge living cells with conventional electronic chips and for determining the ultimate size and sensitivity limits of hybrid nanobiotechnological sensing systems. These will be highly crossdisciplinary activities.

Nanoscale acquisition demands nanoscale probes. The highest priority must be given to support for synthesis and characterization of quantum nanostructures in novel architectures motivated by acquisition functionality. "If you can't make it, you can't study it!" Systems of interest include quantum dots, rods, and wires of semiconductors, metals, ceramics, and polymers.

Nanoelectronic, nanomagnetic, and nanophotonic systems will increasingly be used in hostile environments. Much greater emphasis needs to be placed on research into use–environment compatibility, particularly abiotic–biotic.

The development of integrated sensor systems should emphasize four major research thrusts, each relying on nanoscale subcomponents for critical functions:

- Integrated handheld disease diagnostic systems for the rapid detection of biological pathogens and for testing pharmaceutical responses to those pathogens
- Single devices integrating chip-based electrical, optical, magnetic, and mechanical sensors with silicon CMOS "intelligence" for the rapid identification of chemicals
- Single molecule detection systems pushing the performance limits of nanofabricated sensors
- Sensors integrated with microfluidics for intracellular nanomanipulation and measurement

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3. Memory and Storage

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VISION

The next twenty years will see enormous changes in the fabric of electronic, photonic, and magnetic technologies. As the physical size of components extends deep into the nanoscale, the influence of classical physics on device performance will continue to wane and quantum effects will become dominant. Deterministic digital information states will give way to probabilistically defined states. Wave function computation and processing will exploit strong quantum behavior in nanoscale components while collective effects will decrease. Von Neumann and Harvard architectures will be replaced by information processing designs better suited to incorporating and extracting huge amounts of information via ultrahigh frequency waves interacting with nanoscale nonlinear media. Information now represented as bundles of charge in electron-based devices will instead reside in a single or few electrons, photons, spin orientations, nanoparticles, polarization states, or phase space states. A host of new physical and chemical phenomena will emerge as researchers uncover myriad new opportunities in this fertile area of technology development. Tomorrow's functional devices will gradually lose all resemblance to today's integrated circuits, which will become obsolete as further improvements to their technology finally hit impermeable physical and financial barriers.

What Can This 21st Century Technology Deliver?

If Moore's Law were to continue to describe the evolution of semiconductor technology until 2020, it would lead to terabyte dynamic random access memory (DRAM) chips featuring devices in which the pass transistor contains, instantaneously, a single electron. It is widely accepted that this cannot happen, driving industry interest in adjuncts and alternatives to silicon-based electronics. Over the next twenty years we will learn to harness nanoelectronics, nanophotonics, and nanomagnetics to create device technologies that provide huge advances in storage and data processing. Applications that now seem impossible will become commonplace.

To accomplish such a dream, the challenge will be to develop the technology to design, build, test, and utilize a single quantum/nanoelectronic device that:

- Computes, processes and communicates at a rate > 100 terabit/s
- Stores 10^{21} bits/cm^3
- Processes 10^{15} instructions/s/cm^3
- Reduces interconnects by 99%
- Increases speed by 1000×
- Dissipates milliwatts of power
- Operates at room temperature
- Fits into a package size < 5 mm on a side

Some example applications include externally worn components that assist humans with diminished or lost senses, augmenting their sight, hearing, memory, or smell with systems integrating detection, recognition, and response.

Such a technology would allow:

- Instant recognition of faces, places, and information with direct interface to the brain
- Searching of 100 million images in 1 ms
- Production of inexpensive disposable computers and entertainment systems
- Instant downloading and permanent storage of 100 Tb of information, literally giving instantaneous access to the entire Library of Congress
- Creation of intelligent robotic pets almost indistinguishable from real animals
- Precise simulation of complex dynamics and turbulent flow, allowing prediction of earthquakes and weather

Realizing the technology that will enable these applications requires substantial and broad-based advances in numerous areas of science and engineering. New technological disciplines must be developed at the interfaces between classically distinct fields of study. Specific requirements include:

- A technology that moves beyond silicon CMOS to provide input and output to the new technology
- Control of single quantum states
- Unification of hard disk memory and chip-based memory into a single universal nonvolatile memory
- Development of >100 Tb mass storage lookup memory with massively parallel read/write capabilities
- Development of integrated cooling to allow room temperature operation of this extremely dense technology

CURRENT STATE OF THE ART

Today's information stores must trade off density, speed, and cost. Extremely low-cost, high-density devices operate at moderate speed, while more expensive technologies are used when fast access is essential. Disk drives emphasize archival needs; speed of access is modest and information retrieval is usually serial. For the interface to a computer's arithmetic logic unit, random rapid access is essential and is provided by static or dynamic semiconductor memory devices. Slower nonvolatile memories are employed to retain bootup programs and (increasingly frequently) for general file storage.

The physical representation of information is critical to storage and memory technologies. Information may be encoded in charge, spin or magnetization, resistance, polarization, index modulation, reflectivity, birefringence, or a host of other physical manifestations. The character of storage and memory, has, to date, been divergent, with different mechanisms employed to optimize each of these functions.

Archival storage emphasizes density. Ultrasensitive reading and writing are achieved through electromagnetic means employing inexpensive media. These media consist of magnetic or optical materials that can be easily deposited yet provide a very high density storage of information—encoded in the magnetization vector of domains in magnetic media, or in the reflectivity of pits at

the surface of a compact-disc read-only memory (CD-ROM). Circa 2004, the minimum bit length on magnetic disks is ~70 nm, and on optical media it is ~500 nm. The read/write head with its interface is the most complex and expensive part of the system needed to record and reproduce the weak signals from the domains or pits. For magnetic disks, the distances between heads and magnetic domains are a few tens of nanometers. The disks spin at ~5000 rpm, leading to speeds of the order of 5×10^5 cm/s. Nanoscale phenomena such as giant magnetoresistance or magnetic tunnel junction resistance are employed to detect the read signal. The read time is microseconds to milliseconds, and information is retrieved serially.

Computing memory emphasizes speed. Circa 2004, a typical static random access memory consists of a 6-transistor cell with an area of the order of 1000 nm × 1000 nm per bit. Information can be read from or written to the cell in a few nanoseconds, at least three orders of magnitude faster than comparable operations to disk. The logic operation performed at each switch of a state-of-the-art microprocessor occurs ten times faster still. More than half of the area of a modern processor is devoted to many megabits of high-speed memory. Additional hierarchical levels of memory—including several levels of standalone static-random-access and dynamic-random-access memories, or SRAMs and DRAMs—hold the large amount of information that is to be processed. The dynamic memories are the highest density memories in use today (a bit takes about 300 nm × 300 nm). A typical personal computer utilizes several thousand megabits of standalone DRAM, which is about a factor of ten slower than SRAM. When dynamic memory is manufactured in an integrated system with processor logic (a costlier process), its performance approaches that of static memory.

Nonvolatile memories are also ubiquitous. There performance falls between that of magnetic disks and DRAM. The microcodes necessary for booting up any electronic system—computer, cellphone, personal digital assistant, compact disc player—are stored in nonvolatile memory. It is also employed in systems that store information in digital cameras, voice recorders, thumb drives, and memory sticks.

Commercially available magnetic storage media now achieve storage densities of ~25 Gb/cm^2. Optical storage technologies deliver 1 Gb/cm^2, while semiconductor-based (dynamic) memories achieve 2–4 Gb/cm^2. Potential densities for these technologies are currently estimated as ~200 Gb/cm^2 for magnetic storage, 80 Gb/cm^2 for optical storage, and 100 Gb/cm^2 for transistor-mediated storage.

Several forms of improved storage and memory structures and systems are now under investigation or in small-scale use in the laboratory [1, 2]. Some of these devices fall into conventional categories:

- *SRAM:* Two inverters are connected to form static storage with two stable states. Transistors can flip between states, and are also used for accessing the information. (6 transistors/bit)
- *DRAM:* Charge is stored on a capacitor and accessed through an extremely low-leakage transistor. This storage is dynamic, requiring periodic refreshes. (1 transistor and 1 capacitor/bit)
- *Flash:* A floating gate is used to alter transistor conduction in this non-volatile form of storage. (1 transistor/bit)
- *Magnetic Hard Disk:* Data is stored in a magnetic film. The magnetization direction is sensed or changed through an electromagnetic head.
- *Optical Disks:* The reflectivity of features stores the data, which is modified and measured through a semiconductor laser and photodetector.

Beyond these are several exploratory storage media and architectures [3–5]:

- *MRAM:* a nonvolatile storage in which a transistor accesses a stack of magnetic materials. The conductivity of the stack is changed by the parallel or anti-parallel alignment of magnetic domains in adjacent layers. MRAMs have been demonstrated with a capacity of 4 Mb. (1 transistor and 1 resistor/bit)

- *Ferromagnetic FET*: A magnetic semiconductor affects the conduction of electrons due to spin effects. Individual devices have been demonstrated at low temperature. (1 transistor/bit)

- *Phase Change Memory:* Resistance of a chalcopyrite material is programmed through temperature, with access through a transistor. (1 transistor and 1 resistor/bit)

- *Macromolecular Memory:* Electrical resistance of a molecular material is programmed and read through a transistor. (1 transistor and 1 resistor/bit)

- *Single Molecule Memory:* Electrical resistance of a single molecule is programmed and read through a transistor. (1 transistor and 1 resistor/bit)

- *Nanodots and Defects:* Charge is stored on a nanoscale assembly of atoms and defects. The amount of stored charge changes the conduction of a transistor. (1 transistor/bit)

- *Volume Holographic Storage:* Information is stored as a modulation in the refractive index of an optical medium, and accessed through sensitive optical detection.

- *Spectral Hole-Burning and/or Spectral Holography:* Optical saturation of select frequency components of an inhomogeneously broadened absorption line indicates the state of each bit of information. Lasers are used to sense or change the saturation state.

These many approaches to information storage are summarized in Table 3.1. The desired characteristics of the hypothetical ultimate, ubiquitous memory and storage element are indicated in the last column.

Table 3.1
Characteristics of Storage Technologies

	Nanodot	Scaled MRAM	Ferromagnetic FET	Macromolecular	Single Molecule	Phase Change	Volume Holographic	Magnetic Disk	SRAM	DRAM	Ultimate
Write Speed	M	H	H	H	H	M	M	L	H	H	H
Read Speed	H	H	H	H	H	H	M	L	H	H	H
Power	M	M	M	L	L	M	M	M	M	L	L
Area	L	L	L	L	L	L	L	L	H	L	L
Cost	L	L	M	L	L	L	L	L	M	L	L
Nonvolatile	H	H	H	M	L	H	H	H	L	L	H
Endurance	M	H	H	H	L	L	H	M	H	H	H
Destructive Readout	N	N	Y	Y	Y	N	N	N	N	Y	N
Scalability	M	M	L	H	L	L	H	M	M	L	H

L: Low   M: Medium   H: High   N: No   Y: Yes   Good ▐   Acceptable ▐   Poor ☐

HARD PROBLEMS

As memories and storage elements become smaller and smaller, and are integrated in higher and higher numbers, their design, engineering, and production present a broad range of challenges, including:

- Power usage and power density
- Need for materials engineered by design [6]
- Interconnectivity
- Integration of function—(logic, memory, communication…)
- Achievement of adequate signal and minimization of noise in devices utilizing small numbers of electrons, photons, atoms, or spins
- Room temperature operation

Any memory and storage system technology that attempts to achieve high density, integrate processing capability, and provide suitable information access must face the following issues:

- Bandwidth to access information
- Speed and latency of information access
- Heat dissipation during massive storage in or retrieval from a small volume
- Cost and density
- Algorithms/architectures to read and write
- Detection of the information
- Validation of the read or stored information
- Self-healing/self-repairing of invalid information
- Endurance of the information at the smallest scale
- Design, growth, and processing of suitable materials
- Processing of structures
- Accessible inputs and outputs (interfaces we can work with)
- Design and modeling—systems to devices to materials
- Confining and guiding the information element—field, particle, etc.
- Optical elements as single-photon source and wave-guiding at nanometer length scale

For currently known techniques, the following key problems emerge as the size of memory and storage elements approaches the scaling limits:

- MRAM and hard disk
  - current density (MRAM)
  - super-paramagnetism and thermal energy
  - scalability
- Field effect and its use
  - reduction in collective effect
  - ensuring sufficient and reproducible signal
  - reproducibility

- Molecular memory
  - power densities and temperature
  - volatility
  - issues of field effect
- Flash/QD/back-gate/defects
  - scalability and issues of field effect
- Optical disks
  - scalability and issues related to large wavelength of used light
  - speed
- Holographic optical memory
  - materials with reduced shrinkage
  - high speed modulator
  - speed
- Spectrally addressed memory
  - formation and programming of quantum dots
  - low temperatures
  - modulators, sharp and stable lasing
  - short wavelength lasers
  - sensitivity of measurement
  - speed
- Two-photon memories
  - materials
  - modulators
  - speed
- Slow-light storage
  - materials for a large group delay
  - tunability of group velocities
  - speed
- Scattering-based storages
  - fabrication and placement of nanospheres
  - near field read-out
  - speed
- Plasmonic spectral memories
  - materials
  - modulators

STRATEGIES AND NEEDS

A focused effort in the science and engineering of materials, optics, electronics, systems architecture, characterization, and integration will be required in order to develop the theoretical and practical knowledge needed to implement new storage and memory technologies. The effort will require support across many disciplines—from traditional disciplines of condensed matter physics, optics, electronics, and electrical engineering, to mechanics, systems engineering, and computer science.

The following critical needs must be met to ensure success:

- Theoretical understanding across dimensional scales
- The ability to make structures, devices, and systems at the nanoscale
- The ability to characterize these nanostructures, nanodevices, and nanosystems

Meeting these needs requires a science and technology infrastructure that lowers barriers to exploration and development across disciplines, as discussed further in Chapter 6. The financial cost will be significant, but extensive, readily available resources are essential to a national-scale effort addressing the hard problems that must be overcome in creating and commercializing fast, high-density, unified storage devices.

PRIORITIES AND CONCLUSIONS

Nanoscale electronics, photonics, and magnetics promises to herald an era of incredible information sensing, storage, processing, and interfacing. The challenge is in making the discoveries and progressing across a large frontier spanning several disciplines so that the fruits of NNI research can serve society.

Storage and memory is a particularly attractive area for emphasis at the nanoscale because storage of information is a less power-hungry and more ordered process than other IT functions. New approaches and new materials can therefore be more easily incorporated through highly symmetric and regular techniques, taking advantage of stable states for reading and writing.

Magnetism [3, 5] offers a particularly interesting opportunity for high density storage and logic devices. Control of magnetic states in nanostructures would lead to terabit nonvolatile memory devices. Nanomagnetic devices could also be utilized for logic applications; concepts for reprogrammable functions within a universal nanomagnetic architecture should be developed. Integration of addressable, nonvolatile, high-density memory with logic operations would lead to single-chip supercomputers by avoiding separate off-chip memory systems and slow mechanical storage.

To maximize the progress in various directions required to catalyze success, workshop participants recommended the following:

- Aggressively pursue new ideas for low-power information storage that is less easily disturbed, promises to reach very high densities, and can operate at room temperature. Both fundamental research and engineering development are required.
- Focus both on research for the long-term and on small-scale laboratory demonstrations that may identify truly promising ideas.
- Provide the level of support and infrastructure necessary to conduct high-cost experimental research in the university environment.

Long-term research in the basic science and engineering underlying storage and memory is critical to success, as is focus on bringing together technical approaches from the sciences and engineering, and infrastructure resources that facilitate integration and demonstration of prototypes. To achieve the vision presented above and successfully overcome the challenges in technology implementation, we must bring together the necessary intellectual resources and ideas, means to reduce them to practice, and a management mechanism that allows disciplined pursuit of the relevant science and

engineering. The bringing together of theory and experiment, and of research and development, requires education and pursuit across traditional disciplines.

There is a risk we may encounter fundamental limits not yet understood and practical engineering barriers. It is also possible that the goals presented here are not ambitious enough, but it is too early to know if that is the case. The support process must allow pursuit of open, discovery-driven research. Fundamental understanding must be achieved; prototypes must be made and tested. We need improved mechanisms for dissemination and exchange of information. It is also critical that mechanisms are found to minimize administrative overhead, conflicts between parties over objectives and intellectual property, and other disincentives that can arise when projects are funded simultaneously by multiple sources. If goals are to be met, management must understand working at the edges of disciplines and must embrace the vision of a grand challenge, and yet single-mindedly drive researchers in promising directions. The management also should have sufficient strength and independence to maintain long-term focus in the face of short-term pressures.

ADDENDUM—S. SHAHRIAR'S STATEMENT ON NANONICS

I suggest that a subcategory called single particle nanonics be created within the global view of nanotechnology. Single particle nanonics will concentrate primarily on technologies such as single molecules. Examples include switches based on individual molecules, electrically trapped individual ions, optically trapped single atoms, single electron transistors, and single photons in high-quality-factor optical cavities. Single particle nanonics holds the promise of realizing a memory/processor system with the highest possible density (10^{21}/cm^3 or higher), designed in a way so as to suppress undesired quantum effects such as coherent superpositions and entanglements. Nanotechnology itself is likely to play a critical role in realizing the potential of single particle nanonics. In particular, technologies for confining and guiding optical fields on a few-nanometer scale—using, for example, photonic bandgaps or plasmonics—ought to be identified as a critical challenge in this context. Novel architectures and computational paradigms may also have to be developed in order to take full advantage of such a high bit/gate density.

A truly revolutionary and disruptive application of single particle nanonics would be the development of a large-scale quantum memory and computer. Briefly, a quantum memory and computer is a collection of N single particles, with controllable interaction between nearest neighbors. It would have a storage capacity of 2^N bits and an ability to operate on 2^N numbers simultaneously. There are some special tasks—such as searching a database, factoring a large number, game-theoretic optimizations, and lattice gas dynamics—for which quantum memory and computing can offer a level of performance that lies beyond the ability of conventional computing. For example, a quantum memory and computer with a modest number of bits (a few thousand) may be able to factor a number with 300 digits in a few minutes. This task requires millions of years for even the best supercomputers. Many hard problems must be solved before the dream of a quantum memory and computer may be realized. Some key technologies that have to be addressed include (a) sources of single photons; (b) high-quantum-efficiency single-photon detectors; (c) microlens arrays; and (d) photonic-band-gap-based cavities and waveguides with dimensions of a few nanometers.

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4. Information Processing

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The progress of a civilization depends upon its production and use of knowledge. The rapid progress of our civilization has relied heavily on information processing technology to produce knowledge in a timely fashion. At the time of this workshop—early 2004—information processing technology is dominated by Boolean logic circuits implemented in complementary metal oxide semiconductor (CMOS) electronic technology. This dominance will certainly continue for another 10 years. There are well-known difficulties in extending Moore's Law far beyond 10 years. The lead-time to bring radical new ideas to fruition in commercial electronics is 10 to 15 years. Therefore, there is now a call for the urgent exploration of innovative technologies and paradigms for information processing. Nanoscale materials and structures provide a unique opportunity to accomplish a revolutionary transformation, using nanoelectronic, nanophotonic, and nanomagnetic information processing technologies to enter a new realm of function and scaling.

VISION

Nanoscale physical properties of matter combined with novel architectures can accelerate and revolutionize information processing by exploiting atomic-scale physical phenomena.

Two separate research thrusts will contribute to the realization of this vision:

Evolutionary nanoelectronics research will focus on new ways to construct nanoscale devices with atomic precision that can address known problems. In this case, we can be fairly specific in stating the near-term research goals. For example, one may use nanostructures (e.g., nanotubes, nanowires, single molecules, etc.) to extend or scale silicon-based microelectronics to its ultimate limit. Nanostructures could also be used to realize devices (e.g., room-temperature single-electron transistors) that could be useful in conventional CMOS-based systems, in novel electronic architectures, or both. Research should also be performed to improve manufacturability by means such as reducing device variability and improving contacts to ultrasmall devices.

Revolutionary nanotechnology research will seek ways toward a fundamental transformation in information processing. Here the goal is to discover new concepts and paradigms, which would propel information processing several orders of magnitude beyond that attainable with CMOS-based technology extended to its ultimate limit. These concepts could include new physical phenomena, represented by unit elements, arranged to interact according to new prescriptions or architectures. This combination of new physical phenomena interacting via a new organization (i.e., architecture) could provide new functions for processing information. In this direction, it is hard to be specific, but one can ask what can be done to set the stage and increase the probability that discoveries will be made. The focus here should be on science itself, but in an environment in which unpredictable discoveries of the type needed are likely to occur.

CURRENT STATE OF THE ART

For digital information processing applications, CMOS scaling challenges include controlling leakage currents and short-channel effects, increasing saturation current while reducing the power supply voltage, and controlling device parameters (e.g., threshold voltage, leakage) across the chip and from chip to chip. For analog, mixed-signal, and radio-frequency (RF) applications, additional challenges include sustaining linearity, low noise figure, power-added-efficiency, and transistor matching.

The planar bulk devices are basically sufficient for satisfying the CMOS (I_{on}–I_{off}) requirements up to the 90 nm node of the International Technology Roadmap for Semiconductors (ITRS)[1], even for high performance applications. Figure 4.1 summarizes the expected evolution of high-performance CMOS on the I_{on}–I_{off} plane due to introduction of specific technology performance boosters.

The development of CMOS technology beyond the 90 nm node will rely on advanced metal oxide semiconductor field effect transistor structures shown in Tables 4.1 and 4.2, which may provide a path to scaling CMOS to the end of the roadmap. For a full discussion of these tables, see the ITRS [1] or Skotnicki et al. [2].

There are two avenues to meeting the scaling challenges:

1. *New transistor structures:* Create new transistor structures that improve the electrostatics of the MOSFET, provide a platform for introduction of nanoscale materials, and accommodate the integration needs of new materials [3].

2. *New materials (including nanoscale materials):* Explore new opportunities to apply functionalized nanoscale materials in the gate stack (high-κ dielectric and electrode materials), to improve carrier transport in the conducting channel, and to reduce resistance while improving carrier injection in the source/drain regions.
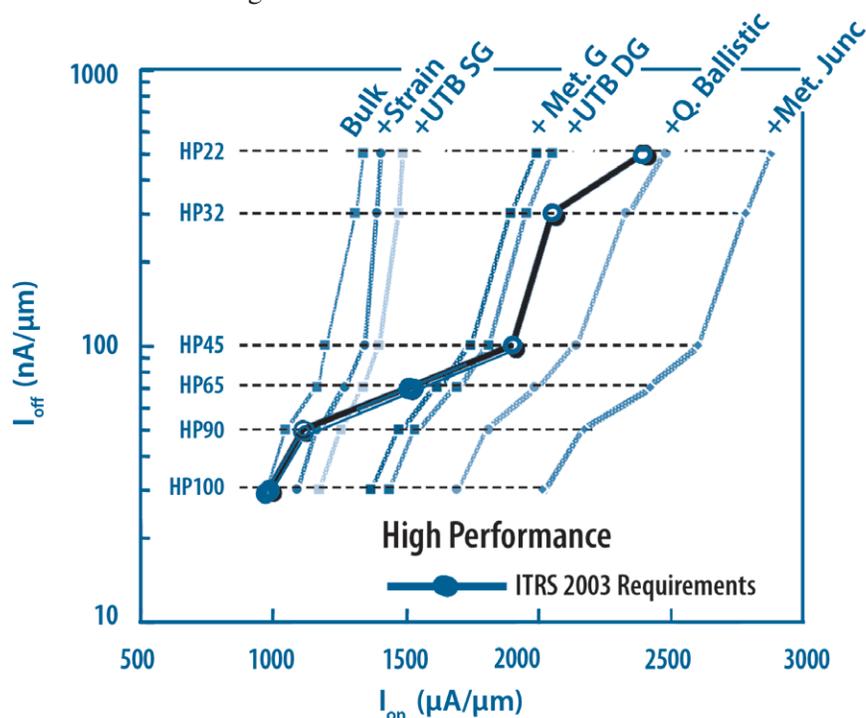
Figure 4.1. Expected impact of various CMOS technology boosters, shown on the I_{on}–I_{off} diagram for high performance integrated circuits.

Table 4.1
Single-Gate Nonclassical CMOS Technologies
(see [1, 2] for further discussion)

Device	Transport-Enhanced FETs	Ultrathin Body SOI FETs		Source/Drain Engineered FETs	
Concept	Strained Si, Ge, SiGe, SiGeC, or other semiconductor; on bulk or SOI	Fully depleted SOI with body thinner than 10 nm	Ultrathin channel and localized ultrathin BOX	Schottky source/drain	Nonoverlapped S/D extensions on bulk, SOI, or DG devices
Application/Driver	HP CMOS	HP, LOP, and LSTP CMOS	HP, LOP, and LSTP CMOS	HP CMOS	HP, LOP, and LSTP CMOS
Advantages	High mobility	Improved subthreshold slope No floating body Potentially lower E_{eff}	SOI-like structure on bulk Shallow junction by geometry Junction silicidation as on bulk Improved S-slope and SCE	Low source/drain resistance	Reduced SCE and DIBL Reduced parasitic gate capacitance
Particular Strength	High mobility without change in device architecture	Low diode leakage Low junction capacitance No significant change in design with respect to bulk	Quasi-DG operation due to ground plane effect enabled by the ultra thin BOX Bulk compatible	No need for abrupt S/D doping or activation	Very low gate capacitance
Potential Weakness	Material defects and diode leakage (only for bulk) Process compatibility and thermal budget Operating temperature	Very thin silicon required with low defect density V_{th} adjustment difficult Selective epi required for elevated S/D	Ground plane capacitance Selective epi required for channel and S/D	Ultrathin SOI required NFET silicide material not readily available Parasitic potential barrier	High source/drain resistance Reliability Advantageous only for very short devices
Gain/Loss in Layout compared to Bulk	No difference	No difference	No difference	No difference	No difference
Impact on I_{on}/I_{off} compared to Bulk	Improved by 20–30% (from MASTAR supposing μ_{eff}X2)	Improved by 15–20% (from MASTAR supposing E_{eff}/2 and S=75mV/dec)	Improved by 15–20% (from MASTAR supposing E_{eff}/2 and S=75mV/dec)	Improved by 10–15% (from MASTAR supposing R_{series}=0)	Both shifted to lower values
Impact on CV/I compared to Bulk	Lowered by 15–20% (from MASTAR supposing μ_{eff}X2)	Lowered by 10–15% (from MASTAR supposing Eeff/2 and S=75mV/dec)	Lowered by 10–15% (from MASTAR supposing E_{eff}/2 and S=75mV/dec)	Lowered by 10–15% (from MASTAR supposing R_{series}=0)	Constancy or gain due to lower gate capacitance

Table 4.2
Multiple-Gate Nonclassical CMOS Technologies
(see [1, 2] for further discussion)

Device	Multiple Gate FETs				
	N-Gate (N>2) FETs	Double gate FETs			
Concept	Tied gates (number of channels >2)	Tied gates, side-wall conduction	Tied gates, planar conduction	Independently switched gates, planar conduction	Vertical conduction
Application/ Driver	HP, LOP, and LSTP CMOS	HP, LOP, and LSTP CMOS	HP, LOP, and LSTP CMOS	LOP and LSTP CMOS	HP, LOP, and LSTP CMOS
Advantages	Higher drive current; 2× thicker fin allowed	Higher drive current; Improved subthreshold slope; Improved short channel effect	Higher drive current; Improved subthreshold slope; Improved short channel effect	Improved short channel effect	Potential for 3D integration
Particular Strength	Thicker Si body possible	Relatively easy process integration	Process compatible with bulk and on bulk wafers; Very good control of silicon film thickness	Electrically (statically or dynamically) adjustable threshold voltage	Lithography independent L_g
Potential weakness	Limited device width; Corner effect	Fin thickness less than the gate length; Fin shape and aspect ratio	Width limited to <1 μm	Difficult integration; Back-gate capacitance; Degraded subthreshold slope	Junction profiling difficult; Process integration difficult; Parasitic capacitance; Single gate length
Scaling Issues	Sublithographic fin thickness required	Sublithographic fin thickness required	Bottom gate larger than top gate	Gate alignment	Si vertical channel film thickness
Gain/Loss in Layout compared to Bulk	No difference	No difference	No difference	No difference	Up to 30% gain in layout density
Advantage in I_{on}/I_{off} compared to Bulk	Improved by 20–30% (from MASTAR assuming $E_{eff}/2$ and S=65V/decade)	Improved by 20–30% (from MASTAR assuming $E_{eff}/2$ and S=65V/decade)	Improved by 20–30% (from MASTAR assuming $E_{eff}/2$ and S=65V/decade)	Potential for improvement	Improved by 20–30% (from MASTAR assuming $E_{eff}/2$ and S=65V/decade)
Advantage in CV/I compared to Bulk	Lowered by 15–20% (from MASTAR assuming $E_{eff}/2$ and S=65V/decade)	Lowered by 15–20% (from MASTAR assuming $E_{eff}/2$ and S=65V/decade)	Lowered by 15–20% (from MASTAR assuming $E_{eff}/2$ and S=65V/decade)	Potential for improvement	Lowered by 15–20% (from MASTAR assuming $E_{eff}/2$ and S=65V/decade)
Analog Suitability G_m/G_d advantage compared to Bulk	Potential for improvement	Potential for improvement	Potential for improvement	Potential for improvement	Potential for improvement

Nanodevices

One-Dimensional Devices

Reduced or one-dimensional (1D) device structures include several device concepts, each containing a 1D structure (e.g., nanotube or nanowire) as a critical element. Several 1D devices have been demonstrated, including carbon nanotube field-effect transistors (FETs), semiconductor nanowire FETs, and semiconductor nanowire heterostructures. Two potential advantages of one-dimensional material systems over bulk material systems have made them the subject of intense research activity. These frequently cited advantages are enhanced mobility relative to bulk systems and phase-coherent transport of electrons. Enhanced mobility may lead to faster transistors and devices, although arguments vary regarding the theoretical potential of enhanced mobility in nanowires.

Carbon nanotubes are an important class of 1D structures because their electronic band structure can vary from metallic to semiconducting to insulating. The tubes can be doped both *p*- and *n*-type, so *p–n* junctions can be formed. Several groups have demonstrated *p*-FET device structures in which a gate electrode modulates the tunneling probability or conductivity of a source/channel Schottky tunnel barrier by a factor of 10^5 or more, providing an I_{on}/I_{off} ratio similar to those for silicon MOSFETs. Various simple circuits with carbon nanotube transistors have been demonstrated, such as NOT and NOR logic gates, a flip-flop, and a ring oscillator. A complimentary voltage inverter with both *p*- and *n*-channel FETs fabricated in a single carbon nanotube has also been demonstrated.

Similar to the carbon nanotube FET, a nanowire FET consists of one of two structures. The first is a device with a channel made out of a semiconductor nanowire having a diameter of 10–20 nm. The second structure consists of the cross intersection of two different nanowires consisting of a *p*-Si channel and an *n*-GaN gate separated by a thin SiO_x dielectric. These nanowire FETs have exhibited I_{on}/I_{off} ratios exceeding 10^4 or 10^5, respectively.

Even though the conductivity per unit width of a nanotube or a nanowire can be quite large, the fact that the transverse dimensions of a carbon nanotube FET or a nanowire FET are quantized in units of an individual tube diameter (1–20 nm) will cause the overall drive current produced by a single device to be quite limited unless many 1D structures can be combined in parallel. Experimental attempts to do this have not been successful. One problem is the widely varying properties of the individual tubes. Another problem associated with any 1D structure is the contact resistance between the 1D structure and the bulk material. This resistance has a minimum value associated with the quantum of resistance (~12 kΩ), so even though transport in the body of a 1D structure may be ballistic, the transport through the structure will be limited by the electrical contacts.

The potential of one-dimensional nanoscale materials to provide ballistic electron transport may enable CMOS transistors at the 22 nm and 16 nm nodes and perhaps beyond.

Quantum Dot Arrays

Quantum dot arrays can be self-assembled, for example, as hexagonal honeycomb nanoclusters, where each quantum dot is 5 nm or less in diameter. Such quantum dot arrays can be reconfigured to perform neuromorphic computation and Boolean logic functions, though at this point no successful circuit has been fabricated [4]. Ultrafast image processing with limited functionality may emerge as a useful electronic application of such structures. For example, an array of 100×100 quantum dots has been configured to detect the edge and vertical lines in an image.

Single-Molecule Diodes and Transistors

The concept of electronic components based on electronic transport through individual nanoscale molecules is based on the following observations: some molecules are stable, some specially designed molecules can be chemically self-assembled, and electron transport through some molecules displays behavior characteristic of active devices. Demonstrated examples include transport through molecules showing nonlinear current–voltage (I–V) curves (sometimes including gate-controllable bistability) and single-bit memories. Experimental demonstrations have been performed with both two-terminal devices and three-terminal devices. Several groups have successfully demonstrated single-molecular transistors (mostly operating in single-electron mode) [5, 6].

A potential advantage of specially synthesized molecules is the possibility of incorporating into their structure not only certain operational functionality but also means for chemically directed assembly on prefabricated wires. Self-assembly of these molecules may eventually be extended to integrated circuits, at low fabrication cost. These developments open the possibility of integration at unprecedented scale—ultimately, beyond 10^{12} devices per cm^2. However, both experiments and numerous theoretical studies have shown inherent limitations for single-molecule devices including limited functionality, below-unity voltage gain, and (most importantly) limited reproducibility of properties of self-assembled devices. There is substantial evidence that the last problem results mostly from difficulties in forming electrical connections.

Most molecular circuit architectures explored so far are based on the use of crossbar-type structures. In this configuration, two grids of parallel wires are laid down perpendicular to one another and molecules are used to connect the points at which the two wires intersect. Individual molecules can then be addressed by using one grid as word lines and the other grid as bit lines, as in conventional semiconductor memories. By using molecules whose current-voltage curves display nonlinear diode characteristics or a region of negative differential resistance, it is possible to perform logic operations with such an array. It is important to note that crossbar architectures may incorporate either individual molecules or groups of molecules operating in parallel at every crosspoint.

Another attractive approach is the integration of molecular memory with CMOS to form hybrid CMOS–molecular circuits where sparsely distributed CMOS components provide additional functionality as needed. An interesting twist of the generic crossbar approach is the so-called CMOL where the contacts between the molecular array and the CMOS subsystem are distributed over the chip area [7].

Spin Transistors

The phrase *spin transistor* is used to refer a three-terminal device that modulates current through spin coupling effects. A variety of spin-FETs and spin-valve transistors have been demonstrated or proposed [8, 9]. The spin-FET consists of a narrow-gap-semiconductor field effect transistor with ferromagnetic source and drain contacts, which enable injection and collection of spin-polarized electrons that are controlled by the gate voltage. The spin-valve transistor more closely resembles a bipolar transistor, consisting of a semiconductor emitter and collector separated by a base region made of a thin multilayer ferromagnetic–nonmagnetic metal sandwich. Spin-valve transistors have been experimentally demonstrated, however the spin-polarized current transfer ratios achieved to date are very low. Another concept for a spin valve uses momentum-dependent spin charge coupling to modulate the electron current flowing into the collector. At the present time, this concept has

not been demonstrated. Both the original concept for a spin valve and its variations depend on the interaction between spin orientations of individual particles and the macroscopic polarization of a ferromagnetic material, the same microscopic interaction that gives rise to the giant magnetoresistive effect. The performance of such devices is likely to be limited by low dynamic range and energy efficiency because they involve electron transport across potential barriers. Spin-based devices discussed in this section do not include the more general category of *spintronic* devices such as spin-light-emitting diodes, spin detectors, spin-resonant-tunneling diodes, optical switches, encoders, decoders, and modulators.

The prevalence and enormous economic impact of spin-based transport on magnetic storage media continues to drive the search for similar devices that can be applied to logic technology. At the time of this workshop, no viable devices have been demonstrated or proposed, but even the restricted field of spin-transistors is the subject of a great deal of research activity.[*]

Innovative Architectures

Suggested concepts that may be used in future nanoelectronic circuits include (but are not limited to) the following architectures.

CNN and Wave Processing

A cellular nonlinear network (CNN) is an array of mainly identical dynamical systems called cells that satisfy two properties. Most interactions are local, within a distance of one cell dimension; the state variables are continuous-valued analog signals (not digital) [11, 12].

A template specifies the interaction between each cell and all its neighbor cells in terms of their input, state, and output variables. Variables of one cell may depend either linearly or nonlinearly on the variables associated with its neighbor cells. A cloning function determines how the template varies spatially across the grid and determines the dynamical response of the array to boundary values and initial conditions. Since the range of interaction and the connection complexity of each cell are independent of the number of cells, the architecture is extremely scalable, reliable, and robust. Although the CNN computes via nonlinear dynamics, and hence is analog in nature, it allows communication with the digital world via high-level language programming features.

The bioinspired CNN and the related wave processing architectures offer a radical paradigm shift in computing that may offer, for a set of important image processing tasks, a nearly five order of magnitude improvement in processing speed over general purpose microprocessors, with comparable reductions in chip area and dissipated power. Operational prototypes of visual microprocessors using this architecture and 0.35 μm CMOS technology with equivalent computing power of 10 teraflops have been already implemented.

CrossNets

For some advanced information processing tasks (including image recognition, pattern classification, image feature detection, and possibly more intelligent tasks) the limited connectivity of CNN and wave processing architectures has to be extended, and the possibility of adaptation ("plasticity") of cell connection strength has to be included into the network architecture. An example of such

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[*]Some general architectures for logic have since been proposed, and are reviewed in [10].

extension is provided by the recently suggested distributed crossbar networks ("CrossNets"), including notably the InBar species. The main advantage of CrossNet circuits is that they allow one to reach arbitrary connectivity (i.e., the number of cells directly connected to a certain cell) in essentially two-dimensional circuits. Hence they can approach, to a certain extent, the expected performance of hypothetical three-dimensional networks. These circuits are also inherently compatible with CMOL technology and may allow CMOL to reach its ultimate performance (of the order of 10^{21} bits per cm^2-s, about five orders of magnitude higher than that of high performance CMOS microprocessors, at acceptable power consumption). The range of possible CrossNet applications beyond image recognition and pattern classification is not yet clear.

Reconfigurable Digital Architectures

Hybrid CMOS/nanodevice circuits—including but not limited to CMOL and nanoscale programmable logic arrays—may be also used to implement highly effective digital memories and logic architectures, to some extent similar to CMOS field-programmable gate array (FPGA) circuits. The uniformity of such circuits makes them highly defect tolerant; they can be reconfigured around 10 to 20% bad nanodevices. In contrast to their CMOS prototypes, memory functions of hybrid circuits (performed by bistable two-terminal nanoscale devices, programmable diodes) are rather similar to logic functions, making the circuits very compact. The delay-area product is 100 to 500 times smaller than purely semiconductor FPGAs fabricated with similar CMOS design rules and ITRS-specified power levels. The major challenge for these hybrid CMOS/nanodevice circuit architectures is high-yield fabrication. The development of effective CAD tools for such circuits is another urgent issue.

Quantum Computing

The core idea of quantum information processing (quantum computing) is that each individual component of an infinite superposition of wavefunctions is manipulated in parallel, thereby achieving massive speedup relative to conventional computers.

Hardware approaches to the implementation of quantum computing can be divided into three approaches:

- Bulk system implementations including nuclear magnetic resonance, linear optics, and cavity quantum electrodynamics
- Atomic implementations including trapped ions and optical lattices [13]
- Solid state quantum implementations [14] including semiconductors and superconductors

Apparently, only the last systems are potentially scalable to eventually reach the large number of elementary devices (qubits) necessary for practically valuable quantum computing.

A major challenge in any system for quantum computing is to provide sufficiently low dephasing so that quantum coherence, or entanglement, is preserved. The role of dephasing (or decoherence) may be reduced using error correction schemes, but these are only effective if the degree of decoherence per quantum operation is well below $\sim10^{-4}$. The degree of decoherence per operation is currently approximately 10^{-3} for electron charge states in semiconductors, 10^{-4} for superconductor qubits, 10^{-9} for photons, 10^{-13} for trapped ions, and 10^{-14} for nuclear spins. A lot of progress must be achieved if scalable quantum computing technologies are to become practical.

Another grand challenge to quantum computing is to address the so-called *algorithm bottleneck*. So far, a quantum computing algorithm providing a significant advantage over classical computing has been found only for integer number factoring. Though factoring is central to public-key cryptography, this field alone may not provide a sufficient customer base for the development of practical quantum computing.

HARD PROBLEMS

While suggestions for new information processing approaches are numerous, most of these will not satisfy the properties necessary for future systems beyond those attainable using ultimately scaled CMOS. These requirements include most notably:

- Functional scalability
- Manageable power
- Substantial performance advantages (e.g., increased information throughput)
- Architectural compatibility between hardware, algorithms, and applications
- Preferably, room-temperature operation
- Acceptable technology stability, reliability, and manufacturing cost

Nanostructure Fabrication and Integration with Silicon

Whatever the physical implementation of a future high performance information processor may be, it is likely to require the willful spatial positioning of a vast number of nanoscale components, as opposed to a random structure. The assembly of such a complex entity poses the biggest challenge.

At present two successful methods to assemble large complex entities are known. One is conventional photolithography, which has allowed manufacture of processors with almost one billion highly interconnected nanoscale devices following a top-down methodology. The other is the biological process, which assembles extraordinarily complex organisms with nanoscale precision employing a "bottom-up" approach. As the limits of the "top-down" lithography paradigm are approached, these two approaches could be usefully combined. For example, one could employ the lithography paradigm and special patterning techniques (such as nanoimprint) as a skeleton for the assembly of still smaller components (such as specially designed molecules or quantum dots). Nanoimprinting would prepare nanoscale sites for the formation and growth of nanodevices such as nanowires and nanodots. For the development of three-dimensional multifunctional structures, hybrid technologies must be developed to produce nanoscale registration from layer to layer. The development of such techniques would provide additional benefits by allowing fabrication of photonic nanostructures, such as optically nonlinear photonic crystal-like arrays. It is important to note that some proposed circuit architectures could use innovative nanolithography schemes tolerating imprecise layer alignment.

In addition, methods should be explored that mimic biological self-assembly processes. These methods could be based on actual biological molecules, abiotic molecules, or mixtures of both.

New Information Processing Concepts

The conventional von Neumann and Harvard architectures are expected to dominate applications for information processing as long as CMOS semiconductor technology is available. As new developments in materials, assembly, fabrication, and characterization emerge, however, it is

anticipated that device and interconnect density will increase beyond known limits. This will create a number of challenges, most notably:

- Fabrication-induced and assembly-induced device defects
- Operational functionality of devices

It will be necessary to develop new architecture types to solve these problems. As discussed in Chapter 2, some examples of possible architectures are biologically inspired: highly parallel systems with large throughput, possibly made of relatively slow devices. Alternatively, a new architecture could provide extremely small processors that are connected in large numbers or distributed over large areas. Also, such approaches to signal processing as connection-oriented and multiprocess schemes may be more adequate for future hybrid CMOS–nanodevice circuits than the conventional architectures. The advent of magnetoelectronic devices will permit the development of reprogrammable logic structures.

One of the most important requirements of any new architecture is tolerance of defects and faults. Given the scale of the components, the complexity of the processor, and the challenges for its assembly, we expect a considerable fraction of the devices to be defective. The extent of the defects may be controllable during the assembly process, but will probably turn out to be nonideal due to fundamental limitations or cost. Hence architecture and software will need to tolerate inherent nonideality of the processor.

Search for Alternative Physical Variables for Data Representation

New physical structures and the characteristics of their components and their interactions may differ considerably from those designed into today's electronic processors. They also may require the invention and adoption of totally new ways of physically representing data and variables. Possible advantages and drawbacks of devices and circuits based on using unconventional degrees of freedom or alternative physical variables for data representation (e.g., spin) should be explored in detail.

Explore New Energy Management Concepts

Independent from the huge challenge of designing and assembling highly complex information processing units described above, tremendous challenges can be expected in the operation of such processors. Systems based on today's computation paradigms necessarily dissipate heat at each operational step. If future processors perform at even greater speed, they will present huge challenges for power management and heat removal. Reversible and adiabatic computational methods may have to be explored to manage the power dissipation of such high performance processors.

Some theoretical calculations show that adiabatic computing may be used to overcome the conventional thermodynamic and quantum limits on energy dissipation. However, this prediction has not yet been confirmed experimentally. Moreover, the few published studies of adiabatic processor design indicate that this approach, taken literally, leads to a substantial increase in necessary hardware and chip real estate. There are preliminary indications that this overhead may be reduced by partial sacrifice of reversibility, while still retaining power savings compared to fully irreversible logic. Thus the issue of adiabatic computing should be intensely explored.

Multiscale Theory, Modeling, Simulation, and CAD Tools

Existing CAD tools are mostly CMOS-oriented. Nanodevice-based, and especially hybrid CMOS/molecular circuits require development of efficient multiscale modeling and simulation methods and eventually a hierarchical set of CAD tools. Such a tool set may include, e.g., the following components:

- Nanodevice modeling tools
- Circuit simulation tools based on compact nanodevice models
- Synergistic full-chip simulation and optimization tools

Atomic Level Metrology

One of the key challenges of nanoscale technology is the ability to measure the effectiveness of fabrication techniques and device operation. This problem is extreme for molecular- and atomic-scale single-electron devices. Although current metrological techniques are very sophisticated, resolution is limited by the dimensions of the available probe. Even carbon nanotube probes are an order of magnitude larger than single molecules. Research is needed to explore and develop metrologies for obtaining three-dimensional physical characteristics of materials and structures on the atomic scale. An interesting observation is that at these scales, metrology and device characterization become unified. Since it is necessary to look at the interaction of individual molecular units, measuring the operation of a device is the same as characterizing its surface properties. For larger devices such as single-electron tunneling diodes, thermal vibrations are sufficient to mask the signal unless the device is cooled to low temperatures. To make these devices useful at room temperature, it will be necessary to develop new instrumentation techniques to separate very weak signals from thermal noise.

STRATEGIES AND NEEDS

In order to effectively address and realize this vision of nanoscale information processing, new approaches to research and education will be required. In particular, there should be a closer interaction between materials, device, process, and circuit-architecture scientists and engineers throughout all stages of the research, encompassing all aspects of nanoelectronics synergistically. Rather than independent optimization of materials, devices, architectures, assembly processes, and software, the new methods of information processing will require optimization of the whole process. This may require the establishment of nanoelectronics as a new engineering discipline. Critical investigation of the advantages and disadvantages of particular directions of scientific exploration and potential solutions to technological problems should be encouraged. Investigators should ask hard questions of themselves, identify potential issues, and assess the fundamental limitations of their approaches.

PRIORITIES AND CONCLUSIONS

Nanoscale materials and structures are poised to sustain and accelerate the epoch-defining revolution in information processing technologies. Realization and exploitation of these exciting possibilities requires a simultaneous focus on two thrusts, one ("evolutionary") having a major impact on nanoelectronics from approximately 10 to 15 years from now, and the other ("revolutionary") enabling advanced information processing beyond 15 years. These approaches must be pursued simultaneously if information processing capabilities are to continue to improve at the rate to which we have become accustomed, ultimately achieving performance several orders of magnitude beyond that available today.

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5. Transmission

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VISION

From the shipping of goods that sustains our national economy to our daily commutes, many human endeavors depend on the ability to move something from one location to another. In sensing and communication systems, this ability takes the form of transmitting signals across an electronic chip, between chips, and through space. Interconnecting the elements of a system allows for the processing, storage, retrieval, and transformation of information through the exchange of data; synchronization of functionality; and performance of algorithmic operations on data sets. Interconnectivity underlies the operation of current communication and sensing systems.

As each successive generation of today's dominant CMOS technology appears, the architecture must change since transistor dimensions can be reduced in scale much more easily than the wiring networks that interconnect them. Even with the recent addition of more metal layers and the transition to copper wiring, interconnection complexity remains a challenging issue for contemporary high-performance CMOS design. As CMOS continues to advance along with even-higher-density alternatives, making the necessary interconnections becomes ever more difficult. New interconnect technologies must be pursued, and new processes developed to support the data transmission needs of future information processing systems.

In today's technology the function of an interconnect is to transfer information in the form of charge; in future generations of interconnects information will be transferred in another form that maximizes bandwidth, most likely using optical carriers. Tomorrow's interconnects may convey a change in polarization, phase, or even quantum state. Information may be transmitted directly between multifunctional, mixed-technology devices. It is time to rethink the approach to interconnects.

Nanonics, the field which is concerned with the creation, control, and transformation of information using nanoscale technologies, is poised to address this challenge. Nanonics embodies aspects of electronics, photonics, spintronics, plasmonics, and molecular electronics. Merging these seemingly disparate technologies into a unified and synergistic technology base would provide the means to interconnect next-generation sensor, processor, and information subsystems, but is itself a formidable task.

Keynote speaker Horst Stormer presented his own perspective on data transmission, noting that at current levels of CMOS integration, a state-of-the-art microprocessor chip performs switching operations at roughly the same rate (about 10^{17}/sec) as all of the synapses in the human brain (see Chapter 1). This simple comparison clearly illustrates the critical role of interconnection in the power and functionality of an information processing system. The brain takes advantage of the natural three-dimensional (3D) aspect of its architecture, while the CMOS paradigm is limited to two-dimensional (2D) architectures, or, at best, layered 2D architectures. The further development of nanoscale interconnect technologies may introduce a new paradigm where billions of devices can be incorporated into a fully 3D system design. If the challenges can be overcome, emerging

interconnect technologies will be key enablers for high-density integration of a new class of systems combining sensing, actuation, computation, and communications. Applications await in improving medical diagnostics, remote sensing, transportation, and manufacturing.

CURRENT STATE OF THE ART

Metallic Interconnects

An electronic system accepts data, processes it, and supplies a result to the outside world (which may be another electronic system). The signal path in one direction can run from a printed wiring board trace, to a package pin through a solder bump, to a global interconnect, and to a local interconnect or transistor gate. The return trip starts at a transistor drain and follows a similar path out through a pad driver, to a solder bump, and then off package. Interconnect requirements depend on the function and speed necessary at each step; these can vary considerably. The critical steps—the transmission of the signal across the chip, and then off of the package—will be reviewed here.

CMOS Metal Interconnects

On modern integrated circuits the metal interconnect layer, adjacent barrier layers, and dielectrics are combined into a high-speed, high-reliability interconnection system. Until 1997 or so, the core interconnect material was aluminum (alloyed with copper to reduce electromigration). Subsequently, pure copper interconnects replaced aluminum in most modern ICs. Since copper is harmful to CMOS circuits, care is taken to encapsulate the copper in barrier layers. These barrier layers scale with the linewidth, so reliable protection against copper diffusion will be a challenge in future generations.

The nonconductive dielectric that electrically separates the metal lines is a critical part of the interconnect system. The signal delay along a line depends on the resistance, R, and capacitance, C, and is characterized by their product (also called the RC time constant). For lower resistance copper, circuit speed is improved. Also, since lower resistances dissipate less power, overall thermal generation is reduced. The dielectric material is characterized by its dielectric constant, k, which when low reduces C and therefore also speeds up circuit operation. Historically, dielectrics were made from silicon dioxide ($k=4.5$). An active area of development is new low-k dielectrics with values forecast to go below 2.6 by 2010 and to 1.7 by 2016. These materials achieve their dielectric properties by being "fluffy." They are therefore relatively poor heat conductors and offer decreased hardness, hindering chemical mechanical polishing of the copper lines and reducing resistance to degradation via electromigration (which can lead to open or short circuits).

As of late 2004, the half-pitch dimension for DRAM is 90 nm (line and space), and characteristic dimensions are somewhat larger for microprocessors. It is anticipated that by 2018, the interconnect half-pitch will be about 18 nm. The interconnect/dielectric layers are stacked, the smallest being closest to the transistor layer. The number of layers of interconnects is currently 9, and will grow to 14 by 2018 according to the International Technology Roadmap for Semiconductors. Since resistance increases with shrinking dimensions more rapidly than capacitance decreases, RC time constants are expected to increase considerably over succeeding generations.

Packaging

Methods for transmitting signals on to and off of chips through the package vary widely, the most popular one today being the ball grid array. In this technology, solder bumps on a pitch of ~100 μm

contact the outer layer of interconnects and bond the chip to a package substrate, from which pins or other board connection methods protrude. To improve heat transfer to the package, an underfill polymer is injected to fill the space between chip and package. For complex systems, several chips can be placed on one package substrate to form a multichip module. Data transmission rates off the chip through the package are typically much slower than the on-chip clock speeds. The industry is working toward system-on-chip or system-in-package solutions to increase data rates within a full system.

Optical Interconnects

Within the Box

There has been no significant penetration or utilization of photonic transport for chip-to-chip, board-to-board, or intra-box interconnections. Existing electronic data transport links provide superior cost normalized to performance. For in-box connections, factors currently favoring electronics are reliability, power consumption, and cost (since photonic transport requires added components to convert signals between electronic and optical forms).

The main driver for future utilization of photonic connections is increasing bandwidth requirements. The necessary developments for adoption of photonic interconnects are monolithically integrated low-power electronic-to-optical-to-electronic conversion elements and an optical bus with multichip signal access.

DataLinks

One and ten gigabit per second (Gb/s) Ethernet systems employing optical fiber are widely used for local area network applications spanning distances up to a few kilometers. The driving factor favoring photonics in these cases is the distance. Electronic transport on kilometer distances at Gb/s rates is lossy. Nanotechnology could improve integration of transmitters and receivers, thereby lowering costs. It may also provide for new integrated photonic devices.

Metro and Long-Haul Telecom

Synchronous optical network single-mode fiber systems operating at 2.5 or 10 Gb/s are being used for metropolitan and long-haul applications, spanning distances from tens to thousands of kilometers, and 40 Gb/s systems are under consideration. Multichannel wavelength division multiplexing systems are widely deployed. At these distances, optical systems have rendered electronic and microwave systems obsolete. Again, nanotechnology could provide for integration of transmitters and receivers, thereby lowering costs, and may also provide for new integrated photonic devices.

HARD PROBLEMS

Interconnections for 3D Architectures

It has been widely forecast that nanotechnology will enable a new class of multifunctional systems incorporating sensing, computation, data storage, and communications in a single package (see Chapter 6). The component materials, devices, and interconnections in this new type of multitechnology system span the domains of electronics, optics, mechanics, and fluidics. In such a diverse system there will certainly be fundamental differences in the properties of the components. Incompatibilities between materials or device feature scales and differences in fabrication processes

will inevitably arise. These differences are likely to mean that nanotechnology-based systems will continue to segregate into sensor, processing, memory, and communications components in much the same way current mixed technology microscale systems are segregated. If so, onto what substrate will these components be integrated? How can we design such a substrate to preserve the benefits of nanoscale integration?

Some of the characteristics required of the integration substrate are fairly obvious, while others are more subtle. Collectively, they represent a new paradigm for reliable nanotechnology system packaging:

- The components must integrate into a 3D volumetric solid, with interconnection through a central volume and components on the outside surface. This preserves the communication density of nanodevice arrays while minimizing communication latency. This structure will allow the separation of signal propagation and thermal extraction paths.
- . The elements that provide interconnection paths must also support the structural integrity of the volume. In other words, these will not be elements in which electrical conductors or optical waveguides are embedded within a structural material (e.g., ceramic). Instead, the elements will be constructed of a multifunctional engineered material in which the waveguides, capillaries, and electrical conductors themselves define the mechanical structure of the solid.
- There must be a capability to spatially interleave mixed technology interconnections within the volume. For example, an array of optical channels must be able to share a region of the substrate with electrical signals and/or electrical supplies. Microfluidics might be integrated with optical or electrical channels to allow the signals to interact with an analyte in solution.
- The interconnection topology should be as flexible as possible but need not be completely unconstrained. For example it is likely that arrays of devices will have common and parallel interconnection requirements. Other types of communication locality can be identified and exploited.
- Thermal extraction paths must be well defined. Heat can flow into the substrate, which can then be actively or passively cooled. Preferably, thermal extraction will be done in the opposite direction of signal flow, through the outside surfaces of the volume.

The integration and packaging issue is common to all mixed technology systems, both microscale and nanoscale. As the field moves forward, from the emergence of nanotechnology-based devices to the creation of systems from these devices, it is imperative to concurrently develop new packaging technology.

Accommodating Heterogeneous Materials and Device Modalities

Monolithic integration of photonic, electronic, and magneto-optical components can increase interconnect functionality. The function of an interconnect needs to be defined when a device is first conceived in order to identify its optimal form, be it electrical, optical, or hybrid. Fabrication of large-bandwidth multifunctional interconnects will require a monolithic integration approach if low-cost implementations are to be achieved (as has occurred for silicon integrated circuits). Chip-scale integration technologies must be developed for components that operate simultaneously in the electronic, photonic, and magneto-optical domains. Development of integrable optical building blocks such as low-loss waveguides, buffers, isolators, filters, and an "optical transistor" will require substantial efforts.

Materials and process compatibility requirements will drive novel device architectures. Different technologies and devices have incompatible process requirements regarding temperature and other environmental variables. Techniques such as localized processing and wafer bonding need to be further developed to overcome this incompatibility.

Metals, semiconductors, and optical materials need to be compatible to achieve full integration. New materials and techniques need to be developed to support this goal, such as accelerated characterization of material parameters at the nanoscale under operating conditions.

Fabrication of nanoscale interconnects will also require new tools with increased resolution, allowing atom-by-atom placement or removal of material and chip-to-chip alignment with nanoscale precision.

Visualization, Measurement, and Characterization Tools

Visualization, measurement, and characterization tools for both structural and functional tests are probably the least advanced of the required developments. The fundamental difficulty is that most tools function at a wavelength larger than the geometric features of the device. At the nanoscale, it is impossible to use standard free-space imaging systems (e.g., microscopes) whose resolution is limited by diffraction. For numerous nanophotonic device applications, new tools are needed that can operate below the diffraction limit while measuring the complex amplitude of the operating optical fields over a broad spectral range. This will allow time-resolved characterization of nanomaterials, devices, and systems with femtosecond resolution, including detailed measurement of nonlinear and quantum effects.

Reliability of Novel Interconnect Systems

General reliability issues include signal integrity and materials stability. The most important reliability issues in metal wafer-level interconnects are electromigration and stress migration; for packaging, thermal stress issues are most important. Future metal interconnects will be smaller, so failures will occur with the migration of less material. As packages are subjected to higher heat densities and package interconnects shrink, thermal stresses will be a greater issue.

Future nanoscale transmitting channels must provide longevity and high reliability in the face of decreasing energy per device and deployment in increasingly harsh thermal environments. Simply creating functional electrical connections will not be enough. Nanoscale interconnects for commercially viable systems must operate for years in a thermally suitable environment; the chemistry and contacts must be robust when operating in ambient conditions unlikely to resemble the cryogenic environment often used for model systems. Thermal degradation will be an important issue.

As active photonic devices shrink, signaling energy (and the number of photons available for signaling) are reduced. Losses ignorable in the large photon number limit become significant for small photon numbers—loss is quantized. Even small average loss levels will lead to fluctuations in photon number and potentially to signal loss. Strategies for maintaining signal integrity at small photon numbers will be required. An advantage of photonic interconnects is that distributed transport structures can be immune to localized structure failure.

Manufacturing of Novel Interconnect Schemes

Nanoscience has had many successes in the last decade—among them the manipulation of individual molecules within strands of DNA, the exploitation of quantum effects in electronic and photonic devices, and the controlled self-assembly of nanoparticles into enhanced materials. But few nanotechnologies have been transitioned into large-scale systems, at least in part due to a scarcity of efforts in integration and interface technologies that function on, and preserve, the nanoscale. For example, both electronic and photonic devices can be readily fabricated on the nanoscale. The integration scale for these nanodevices, however, is typically 10–100 μm. To a large extent this negates the progress made in nanoelectronics and nanophotonics. Research to address these issues must focus on developing advanced material systems explicitly for nanoscale integration and interfaces. Many proposed applications utilize hybrid materials, so particular effort should be dedicated to the use of organic/inorganic materials for heterogeneous integration and interfaces on the nanoscale [1]. Materials need to be developed with superior thermal and electrical conductivity and other optimal properties including adhesion, transparency, and mechanical strength.

STRATEGIES AND NEEDS

Incorporate Ultrahigh Density, Ultrahigh Index Materials

The development of *transmitting systems* for integrated electronics platforms, typically optical or radio frequency (RF), is now beginning to exhibit the same scaling trends that have earlier characterized the evolution of memory and logic sections of integrated microelectronic chips. There is a growing desire to develop and place optical devices on scaled silicon for purposes such as clock distribution and signal routing. One of the more promising enablers for reduced-size optical devices is index contrast. Greater differences in refractive index lead to tighter optical confinement in the high-index region. Thus silicon-on-insulator (SOI) technology has recently been used to realize optical waveguides with dimensions that are just fractions of micrometers because of the high index contrast between silicon, the insulating layer, and air. The same contrast allows reduction in the dimensions of bends and other optical features on the silicon wafer substrate.

In future nanosystems, the optical interconnects in the transmitting backbone must be even smaller. For example, direct interconnects to biological or macromolecular species may be required to transmit light from receptors to signal processing sites in nanoelectronic systems. Reduction to this scale is a major challenge for photonic nanotechnology. It will require new materials with extremely high dielectric constants or refractive indices. Candidates include complex oxides or hitherto unexplored organics. Another direction which seems particularly intriguing is the use of high-quality-factor metal interconnects, which permit plasmonic light transmission [2]. Ultrasmall plasmonic structures— much smaller than the wavelength of the transmitted light—could provide direct connections from molecules to nanocircuits (Fig. 5.1).

Nonlinear and Multifunctional Materials for Nonelectronic Logic and Holographic Routing

The demand for interconnects to operate at shorter and shorter distances will be a challenge not only for miniaturization and integration of circuits and systems, but also for the engineering of devices that efficiently generate, regenerate, detect, switch, process, multiplex, and demultiplex information-carrying signals using direct operations. Nonlinear materials—in particular, optical nonlinear materials—are good candidates for such operations. Such an approach may significantly reduce the need for costly and somewhat cumbersome conversions between the optical and electronic
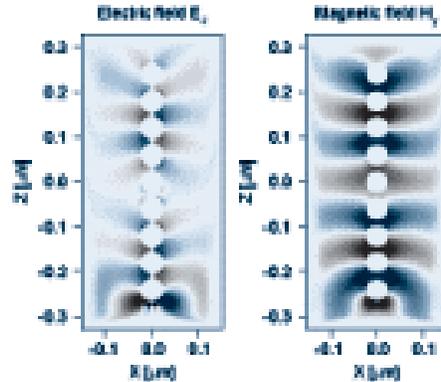
Figure 5.1. Optical fields in a plasmonic interconnect consisting of metallic spheres (courtesy of Panoiu and Osgood, Columbia University).

domains. For example, the efficiency in nonlinear optical interactions can be enhanced by increasing the peak power of interacting optical fields and by increasing the nonlinear optical coefficient of the material in which the fields interact. Existing nonlinear optical materials and devices are efficiency limited due to the relatively small effective nonlinear coefficients and the short effective interaction lengths imposed by dephasing. Each of these parameters can be enhanced by exploiting nanotechnology, leading to increased capability and broader applicability of nonlinear devices.

Using nanotechnology to engineer interactions between microwaves and optical waves may be of great importance for efficient and cost-effective interfaces between RF and optical systems. Control of light-matter interaction on a subwavelength scale using inhomogeneous composite materials will enable the design of ultracompact integrated photonic transmission subsystems. Inhomogeneous materials can be designed to localize optical fields on the nanoscale, enhancing classical as well as quantum interactions. Materials, devices, and subsystems can be engineered to control localized polarization states or dispersion properties, and to exploit quantum effects in interactions between optical fields and electronic states. Quantum effects will be a significant design parameter at the nanoscale, leading to a whole new class of highly efficient low-power low-noise all-optical signal processors, switches, detectors, and emitters. All-optical signal processing at single-photon power levels should be within the realm of nanophotonics, enabling quantum information processing and transmission. This could be achieved by combining electromagnetically induced transparency, quantum dots, or surface plasmon structures with ultrasmall volume nanocavities (e.g., photonic crystal cavities or microspheres). Alternatively, ultra-slow or stopped light concepts could be employed. Since quantum information transport will be performed in the optical domain, it may be useful to perform all-optical signal processing at network nodes to avoid loss of quantum coherence during conversion to electronic quantum states.

Appropriately designed dielectric, metallic, and metallo-dielectric nanostructures can strongly localize and manipulate light. Such engineered nanophotonic structures can guide light and can be utilized in ultracompact functional devices. These in turn can be integrated into circuits via near-field interactions and control. For example, a resonant inhomogeneous medium such as a photonic crystal lattice can serve as an integration platform for ultra-small photonic systems. Exploitation of surface plasmon effects may also allow orders of magnitude reduction in the size of optical waveguides, devices, and components. While metallo-dielectric structures support a very high level of miniaturization and optical field localization, for certain applications their losses are detrimental. Techniques to cope with, or overcome, these losses are highly desired.

Advancement of nanophotonic transmission technology will require several innovations including:

- Advancing efficient design, modeling, and simulation tools
- Developing cost-effective nanofabrication techniques
- Building accurate and reliable visualization, measurement, and characterization tools for both structural and functional testing of operating nanophotonic devices and circuits

Design and Modeling Tools

Advanced design and modeling tools must do more than provide accurate solutions of electromagnetic optics equations; they will also need to incorporate linear (e.g., dispersion, birefringence, absorption, etc.) and nonlinear materials properties and the equations of quantum physics. A number of tools for this purpose are being developed, utilizing the finite difference time domain method, the finite element method for nonperiodic structures, and the rigorous coupled wave analysis method for periodic linear and nonlinear structures. The computational complexity of an accurate analysis of nonlinear optical effects depends on the order of the nonlinearity, and has been addressed in the past under simplifying assumptions for low-order nonlinear processes. More sophisticated approaches will be needed as higher order linearities are exploited. Moreover, as the typical features of nanoscale engineered materials decrease, quantum effects need to be included into the nonlinear electromagnetic optics equations.

Nanofabrication

Using well-established microelectronics fabrication techniques, nanofabricators have already constructed actual nanophotonic materials and devices including quantum wells, superlattices, quantum wires [3], quantum dots, form-birefringent nanostructures, photonic crystal lattices (Fig. 5.2), and defected photonic crystal lattices. This approach realizes discrete optical devices and components. Novel techniques are being developed to allow integration of nanoscale inhomogeneous optical materials into operational optical devices and components, which will in turn need to be integrated into subsystems and systems. Two general classes of fabrication technologies are being investigated for nanophotonic optical subsystems: wafer-scale integration and fiber-scale integration. Both integration platforms are driven by the results of fundamental, innovative research on photonic and plasmonic materials and devices. The main goal is to construct ultracompact, tunable multifunction devices on a subwavelength scale, by using either high-refractive-index-contrast dielectrics or (even smaller) plasmonic resonant structures. Processes commonly used to fabricate wafer-scale devices are high resolution electron beam and ultraviolet (UV) lithography, reactive ion etching, chemically assisted ion beam etching, and various evaporation and growth methods. For cost-effective nanofabrication of large-area nanophotonic circuits and subsystems, novel techniques must be developed [4]. For fabrication and integration of metallic and metallo-dielectric composites, for example, one could deposit or grow a well-aligned array of carbon nanotubes and subsequently fill their cores with specific metals or oxides utilizing supercritical carbon dioxide deposition. Fiber-scale fabrication can be used to construct devices requiring variable interaction length (determined from either weak or strong coupling and field interaction effects, depending on the specific application). Fiber-chip interfaces may cause additional losses, so it may be useful to perform optical signal processing by exploiting optical nonlinearities in specially designed in-fiber devices.
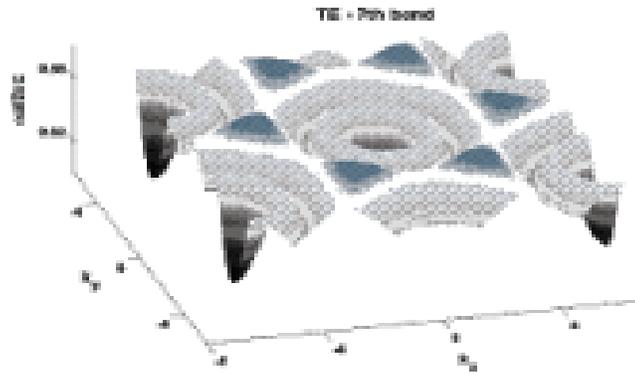
Fig. 5.2. The computed band structure of a nonlinear photonic crystal, based on Kerr nonlinearity (courtesy of Panoiu and Osgood, Columbia University).

Transmission of Signals to Nanodevices

Transmitting information to and from nanodevices at the dimensional limits poses unique problems [5]. CMOS gates may eventually be scaled down to the few nanometer range, and must still be electrically connected to other circuitry during fabrication. Another contender at this same or smaller scale is molecular nanocomputing devices [6]. While molecules can be synthesized to produce a near-infinite variety of physical, chemical, and electrical characteristics useful in devices, there is no obvious path to interconnecting many such molecular elements.

Nanometallic contacts currently under research are at a scale large compared with single molecules. The contact points to the molecules are beyond the limits of any conventional lithographic technique. Carbon nanotubes can be made less than 1 nm in diameter, and if functionalized appropriately could interconnect molecular devices. With improvements in lithography, metallic contacts smaller than 5 nm may become more common; if functionalized they, too, could serve as contacts to particular parts of molecules.

Optical means for communicating with nanostructures are equally important. In future nanoelectronics devices, signal processing will be performed at the nanoscale. A single electron confined inside an atom at Angstrom (0.1 nm) scale can undergo a transition between states and produce a photon with a wavelength at micrometer scale; in this way the scale at which information is stored is automatically "magnified" by 3 to 4 orders of magnitude. This simple process could be used to transport information between elements of vastly different sizes.

Directing Optical Signals Across Wafers or Chips

It is natural to model signal routing in photonic circuits after the wiring methods used in their eminently successful electronic cousins. In such a model, light is routed from active element to active element by channel waveguides. While effective after a fashion, such designs do not exploit one powerful aspect of photonic transport: photons in linear media can flow through one another without interaction. This ability represents a fundamental difference between photonics and electronics. Photons have no charge and thus interact only indirectly through controllable material intermediates. The absence of charge also results in low propagation loss even at high signal bandwidths—a very powerful property that has allowed fiber optic transport to dominate the world of long distance communications.

Signal lines in wire-analog (i.e., channel waveguide based) chip-scale photonic circuits must not overlap and must be routed to avoid tight, lossy bends. These constraints sharply limit the available interconnection architectures. Nanoscale fabrication technology may provide for breakthrough photonic transport designs that fully utilize the noninteractive nature of light, allowing for channel-free, distributed, and overlapping (yet fully integrated) signal transport. This will substantially broaden the available variety of photonic interconnect architectures.

Truly photonic signal control devices and circuits may incorporate volume holography and photonic bandgap structures. Advancing nanofabrication technology provides for the (heretofore unachievable) realization of computer-generated holographic structures. Volume holograms are structures extending in two or three dimensions whose interaction with optical signal modes is constrained by generalized Bragg scattering conditions. Using nanolithographic fabrication techniques, a volume hologram can transport a signal between active devices while avoiding interaction with other signals. One can envision a chip-scale planar waveguide optical transport layer, with signals flowing unconstrained in the slab waveguide like free-space beams. These signals can overlap and intersect, yet each is precisely guided by distributed mode-specific holographic structures. Extension to multiple transport layers is possible, perhaps interspaced with electronic processing layers. Modes coupled by distributed diffractive structures might reside in adjacent planes, which will be exciting to explore.

Photonic bandgap structures, computer-designed and nanofabricated or perhaps self-assembled [7], provide a powerful alternate means of steering photons (Fig. 5.2). Bandgap structures can form advanced photonic circuits including channel waveguides with sharp bends. Bandgap structures may also provide for channel-free overlapping signal beams.

The core need in order to realize transparent (non-interactive) photonic interconnects is the ability to fabricate structures and devices with nanoscale precision in optical media. Advanced concepts for fully integrated, transparent interconnects are intimately connected to the challenges of advancing fabrication capabilities.

Multidomain Integrated Design Tools

Computer-aided design tools and simulation software utilize advanced electronic systems to develop even more advanced systems. This "bootstrapping" approach, a mainstay in the evolution of scaled silicon chips, has recently been applied to the design of integrated optical devices and microsystems. Tools based on numerical techniques such as the finite-difference time-domain and beam propagation methods have been developed extensively in the last few years, and are now central to the implementation of the first wave of nanophotonic devices. These tools allow a scientist to design, simulate, and redesign a new optical device or photonic circuit without recourse to fabrication. Fabrication and further redesign are utilized later in the development process to test and more carefully examine the real structures.

Future optical nanosystems will require new advances in software tools. The first need is for a rigorous means to design three-dimensional nanosystems on personal computers. Simulation codes that run on personal computers are accessible by all designers irrespective of institutional size or resources. The second need is for device and charge transport models that treat materials structures atomistically. As smaller and smaller optical devices such as nanotube lasers or molecular emitters come into play, these models will become essential. Models needed for photonic devices are similar but must also couple to the optical properties of the molecular medium. A final need, increasingly important as microsystems are scaled down to nanosystems, is for tools that can compute across multiple

functional domains. For example, designing transmission channels on a nanosystem chip will require simulation across the boundaries of optics and electronics, sensing, and thermal management.

The field of nanotechnology is concerned with molecular-scale interactions. Conventional design and fabrication tools are largely ineffective on this scale due to increased difficulty in determining physical properties and to the coupled nature of the interactions. A good example is the calculation of the electromagnetic properties of a nanostructure. When a structure is large compared to a particular wavelength of electromagnetic waves, most interactions within the structure become decoupled. Simplified solution methods can then be used to solve for the interaction between an incident wave and the structure. When, however, the structure is small compared to the relevant wavelength, all points on the structure become coupled. Then the full electromagnetic boundary value problem must be solved. In this case analytical techniques can seldom be used, so computational approaches are necessary. Most computational platforms are severely taxed by the full boundary value problem for realistic structure sizes. Alternative approaches to meeting the computing needs of nanoscale modeling and simulation should be developed, and the resources needed to acquire and maintain them should be considered. One approach is to use large clusters of computers. Technologies such as reconfigurable computing, distributed computing, and hardware-based acceleration are also candidates to analyze previously intractable problems on the nanoscale. The development of affordable, accessible computational platforms for the creation and application of nanotechnology design tools is a near-term need.

PRIORITIES AND CONCLUSIONS

Transmission and interconnection issues must receive increased attention to keep up with the progress that has been made in nanoscale devices. The problems to be overcome are multifaceted. Their full definition and eventual solution will require input from many communities and sustained support. Approaches that bring the high bandwidth of optical interconnects to the chip level are promising, but the scale mismatch between lightwaves and nanoscale devices is difficult to overcome, and new paradigms are required. Comprehensive analytical and computational approaches must be developed, and design tools embodying them must be made widely available to device and subsystem designers. Materials issues are challenging. The full promise of multifunctional "designer" nanomaterials may need to be delivered upon to realize concepts for scalable interconnects and three-dimensional architectures at the nanoscale.

Session participants recommended the following potential foci for future research:

- Engineering materials and devices at the nanoscale for all-optical signal processing at single-photon power levels
- Designing active devices incorporating nonlinear nanophotonics (e.g., photonic crystals or surface-plasmon structures) to enable all-optical signal processing and/or buffering for on-chip or between chips optical interconnects
- Developing theoretical (numerical and analytical) tools to tractably model electromagnetic phenomena at microscale and nanoscale, including nonlinearities, material dispersion, gain, absorption, and quantum effects
- Fundamental understanding of chemical bonding for electronic transmission to molecules
- Fundamental understanding of electromigration on the nanoscale
- Mitigation of quantized photon loss as a source of error on low-photon-per-bit photonic interconnects

Since nanotechnology is still a field in its infancy, programs addressing the technical challenges presented above must first be targeted at developing suitable infrastructure to provide design tools and fabrication capabilities to serve the research and development community. Without widely available design and fabrication capabilities, the field of nanotechnology will either be restricted to a select few or remain largely speculative. Megasites represent a solution for only a subset of the community. To serve the entire community, decentralized facilities also need to be established, which may take the form of foundry-like services for nanotechnology. A stumbling block here is that the field is not mature enough to have adopted standards facilitating the provision of such services. Despite this apparent lack of maturity, it may be fruitful to initiate decentralized services so that advances and their associated standards can begin to evolve. Once these mechanisms are in place to foster creativity within the nanotechnology community, programs in subsystem-level nanotechnology integration should be supported. These programs should explore alternate technologies that may overcome current limitations and solve pressing problems. Candidate programs might focus on developing molecular-scale lithography, ultrahigh-density digital storage for archival information, metrology and inspection tools, and novel devices and systems to create, encode/decode, and process signals. As these subsystem technologies mature, they will become poised for integration into larger systems. Then new paradigms can be introduced offering unprecedented performance improvements over conventional systems.

An important issue raised during the workshop was ensuring that appropriate funding mechanisms are utilized to create and maintain a balanced effort among the industrial, Federal, and academic research institutions in the nanotechnology community. Mechanisms discussed include: at the industrial level, direct government funding and tax breaks or other incentive programs; at the Federal level, block funding of institutional charters; and at the academic level, supporting initiatives targeted at curiosity-driven research, providing both the resources necessary to foster creative thought and the longevity to see them through.

Some additional issues to consider in this regard are: providing continuity at universities by supporting permanent technical staff, balancing single investigator grants with longer-term group grants, and balancing curiosity-driven research with program-directed research. University-based efforts should be able to ensure support for several generations of students, each making small contributions in theory, simulation, materials development, device fabrication, and testing, which come together over time to complete a larger picture.

Perhaps the most important recommendation is to establish and maintain sufficient funding to foster the growth and advancement of the nanotechnology base within the United States. While funding alone will not move the field forward, it is the very fuel of progress and facilitates the pursuit of research. The growing trend in the industrial and government sectors to take a more near-term view of R&D has affected nanotechnology development. Overemphasis on short-term progress could jeopardize the nurturing of next-generation leaders in nanotechnology R&D, erode the technology base, and threaten our international economic position. The National Nanotechnology Initiative must maintain the long view, inspiring a new and committed appreciation to the development of nanotechnology. Investments in infrastructure should be paramount. Subsequent programs can then address the hard problems of the day, and support the development of new methods and processes with which to attack them. Following the natural course of research, some of these efforts will succeed; new paradigms will emerge, be embraced by the technical community, and lead to innovation on all levels.

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6. System-Level Integration

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VISION

Tomorrow's researchers will build sophisticated nanosystems combining the nanotechnology-enabled advances in sensing, storing, communicating, and processing discussed in previous chapters with appropriate actuation and control mechanisms. Hybrid systems will include disparate components, each optimized for a particular function. Initially these systems may leverage existing silicon-based manufacturing infrastructure, adding novel nanoelectronic, nanomagnetic, and nanophotonic components on a common platform. More-or-less conventional silicon circuitry will process digital information, while other device technologies provide analog sensors and actuators to interact with the real world. Future vision systems will incorporate electronic processing components combined with photonic sensors in a tightly integrated package. Labs-on-a-chip will deliver local, low-cost diagnostic capabilities by fully integrating electronic processors with electro-opto-magnetic sensors and nanofluidic sample handling.

The workshop participants' vision for how these integrated nanosystems will develop incorporates three major themes:

1. Nanosystems for sensing and interacting with the environment will become ubiquitous.
2. Biological organisms offer inspiring examples of nanotechnology-enabled systems, and are a challenging host environment for man-made nanosystems.
3. Tools and facilities for design and fabrication of nanosystems should be made available to all interested parties.

Ubiquitous nanosystems will extend mankind's ability to sense, interact with, and ultimately control our environment. Nanotechnology will allow us to make sensors for temperature, light, motion, sound, chemical agents, pathogens, and a host of other variables. These sensors will be very small, self-powered, and self-configuring, and will include at least rudimentary communication and data reduction capabilities. The sensors will communicate with each other and form *ad hoc* networks, utilizing redundancy, dense sampling, and multimodal signals to monitor their environment far more accurately than is possible with isolated sensors. Further data reduction can be performed at any level of the sensor communication fabric and will be distributed across nodes in an optimized manner to extract actionable information from massive raw datasets. This information will then be used to determine an algorithmic response, realized through communication to and actuation of appropriate control elements.

The participants envisioned systems to manage a variety of ambient conditions—heating and cooling, light and dark, noise and silence, chemical atmospheres—through either anticipatory or real-time control, without human interaction.

Bioinspired and *biointeractive nanosystems* represent a merger of biology and nanoscience with widespread application and broad implications. Many scientists and engineers are developing

nanoscale manufacturing technologies that draw inspiration from biological processes, or designing nanosystems that employ nature's paradigms for sensing and processing information. Others are focusing on how biological molecules, cells, and systems interact with more conventional materials and devices in the nanoscale regime.

Bioinspired nanosystems draw on the materials (organic and biological molecules), processes (self-assembly), structures, architectures (brain-like or nervous-system-like), device mechanisms (neuron-like), and functionality (nonlinear dynamics) of living systems.

Biointeractive systems will extend current biotechnologies to the nanoscale. Nanoscale labs-on-a-chip will analyze cells and subcellular components with great accuracy. *In vivo* diagnostic or treatment devices will be inexpensive and robust, and will utilize advances in the understanding and control of organic/inorganic interfaces at the nanoscale to ensure biocompatibility.

These approaches can be combined in application areas such as prosthetics. Consider, for example, a functional replacement eye. Nanosensors would detect light, a bioinspired nanoprocessor would mimic retinal image processing functions, and biointeractive devices would interface directly to the nervous system.

The third theme selected by the workshop participants is represented by the phrase *nano for all*, encapsulating the need to provide researchers from universities or industry throughout the United States with broad and affordable access to nanoscale tools and technologies. Current programs to build centers of excellence are a necessary first step. To meet the National Nanotechnology Initiative goals of unprecedented innovation and pervasive impact, nanotechnology resources must be available to all interested scientists and engineers for a modest investment in time and money. Emerging methodologies for nanoscale design and nanomanufacturing should be fully developed into system-level tools with well-defined interfaces to facilitate the use of nanotechnology by engineers and architects of large-scale multifunctional systems.

CURRENT STATE OF THE ART

Ubiquitous Nanosystems

There has been little work to date on how new nanoscale devices would function in a real system. Many innovative device structures have been proposed and developed in the separate realms of nanoelectronics, nanophotonics, and nanomagnetics, as described in the previous chapters of this report; comparatively little effort has gone into understanding the advantages novel nanoscale devices offer at the system level versus existing silicon technology.

In nanoelectronics, for example, there is beautiful and exciting research on current flow through single molecules and on utilizing this flow in molecular electronic devices [1, 2]. For nanophotonics, impressive strides have been made in devices that exploit photonic bandgaps and plasmon resonances. Nanomagnetics shows significant promise for new generations of nonvolatile data storage devices. It is less clear how any of these structures would be integrated in practical systems [3]. The potential for new combined magneto-electronic devices also remains largely unexplored.

Silicon-based systems continue to develop new capabilities at a rapid pace. For example, microelectromechanical and nanoelectromechanical systems (MEMS and NEMS) combine ever

more processing power with novel sensors and actuators. Sophisticated as these systems are, there is still ample room for integration of new sensor structures.

Bioinspired and Biointeractive Systems

The study of how biological nanosystems process information has already led to concepts suggesting new directions for nanoelectronics. Neurons operate through a simple integrate-and-fire mechanism and use firing time and rate to encode information. Artificial neural networks mimicking this process have been useful for specialized computations. Features such as real-time local computing, adaptive connection, and weighting have already influenced the design of artificial nanosystems.

Biological "manufacturing" uses several kinds of biorecognition to enable bottom-up self-assembly. These include receptor-acceptor binding, Watson-Crick base pairing, coulombic interactions between protein surfaces, and hydrophobic/hydrophilic interactions. Exploitation of these approaches for the design and fabrication of programmable artificial structures is in its infancy [4].

Biointeractive systems of today include DNA microarrays and various implementations of the lab-on-a-chip concept. Some primitive organism-to-hardware interfaces have been developed; their application has progressed from directional control of lab mice and insects to control of a robotic arm by a monkey and of a prosthetic arm by a human. Cochlear and deep brain stimulation implants have been widely adopted and are prime examples of the state of the art in biointeractive systems.

Nano for All

Access to state-of-the-art technology for design, simulation, and fabrication of microsystems and nanosystems is currently provided through one of three models: centralized facilities like MOSIS (the Metal Oxide Semiconductor Implementation Service originally supported by the Defense Advanced Research Projects Agency) or the Nanoscale Science Research Centers at five Department of Energy National Laboratories; centers of excellence in nanotechnology research supported through the National Science Foundation (NSF), the Department of Defense, or NASA extramural research programs; and distributed resources such as the NSF-supported National Nanotechnology Infrastructure Network and Nanoscale Computational Network.

The idea of a Nano-MOSIS has been discussed in previous reports. The fundamental definition and standardization of an appropriate set of manufacturing technologies for a Nano-MOSIS has not yet occurred; while much fundamental science remains ahead, sufficient progress has been made so that the definition of standard processes and a tool flow for the integration of nanodevices into larger systems can begin.

HARD PROBLEMS

Across all three major themes, realization of the envisioned nanosystems requires integration of multiple technologies. This presents numerous challenges in areas including system architecture, devices, assembly techniques, interfaces, power supply, data representation, state variables, algorithms, applications, and design tools. In nanomanufacturing, materials, interface, and process issues abound since these systems incorporate multiple, independently developed advanced technologies.

Ubiquitous Nanosystems

The hardest problems associated with ubiquitous nanosystems are related to power. Communication and control systems will also be challenging. These are primarily system integration issues, but a similar hierarchy of problems exists at the chip level and even at the die level.

Delivering power through a grid is prohibitively expensive simply due to the large number of elements, and would greatly inhibit reconfigurability. Replenishing local energy storage devices such as batteries or fuel cells would require human intervention. Power scavenging is viable, but ensuring that an adequate amount of scavenged power is available when and where it is needed constitutes a difficult problem; photovoltaic collectors, for example, do not work well at night or in dark places. Related issues are minimizing the power dissipated by environmental sensing and control elements and dissipating heat generated by deeply embedded elements. Low-power elements ease both the power scavenging problem and the thermal dissipation problem.

The communication and control system must be self-configuring, self-testing, self-repairing, upgradable, and ultimately controllable by human intervention when required. It must be fault tolerant and highly reliable. Every element of the environmental sensing and control system must be recoverable and will preferably be reusable. The ubiquitous nature of the elements means that no one will know exactly where they all are, so there must be some deterministic way of locating elements on demand. This could be achieved with an integrated transponder that emits a radio frequency signal on interrogation, or through something more sophisticated.

One specific chip-level hard problem is the homogeneous integration of multiple sensor technologies on a single chip. This entails process integration involving very different material systems as well as reconciling multiple time scales, spatial resolutions, and analog-to-digital or digital-to-analog conversion strategies.

A more general problem for the integration of nanoelectronic, nanophotonic, and nanomagnetic structures is the absence of a design methodology and a standard fabrication environment. The situation is reminiscent of that in the very large scale integration (VLSI) community prior to the ground-breaking work of Mead and Conway [5], who introduced a framework for VLSI design including a design methodology and design rules. This framework allowed different groups to compare their designs and have them fabricated in standardized facilities. Nanotechnology may not yet be ready for the introduction of a common framework and standardized facilities, but it is time to start thinking about them. The reconfigurable and dynamic nature of the hardware elements in these ubiquitous systems will challenge the design methodologies contemplated in *nano for all* and thus should help shape those methodologies.

Bioinspired and Biointeractive Systems

Biomimetic, bioinspired, and biointeractive systems are still in their infancy; many hard problems need to be solved. Adaptations of some biological mechanisms for information processing can be explored today, but a better understanding of the algorithms, structures, and architectures of biological information processors is needed to fully develop both bioinspired and biointeractive systems. While circuits that operate by nonlinear dynamics similar to those of the brain have been studied, their programmability must be better understood. The well-known robustness (i.e., fault tolerance) of biological systems is also poorly understood. Understanding of biocompatibility has progressed but is far from complete; further progress is essential, especially for biointeractive systems.

Close integration of sensing and processing functions in non-traditional silicon architectures like the cellular neural network has demonstrated significant performance gains, but only for specialized applications like image processing. Application of these approaches to general information processing tasks may require major advances in nonlinear mathematics.

Another hard problem for bioinspired information processing circuits is input/output (see also Chapter 5). For biological systems this is usually two dimensional (2D); thus means are needed to interface a micrometer-scale optical input pattern to a 2D array of bioinspired nanoscale devices. Various bioinspired methods for generating 2D arrays have been demonstrated but hard problems remain including:

- Controlling array periodicities and dimensions
- Implementing self-correction and self-repair techniques
- Aligning self-assembled subcomponents with conventional circuitry
- Physically and electrically interfacing semiconductor materials to molecular elements
- Combining organic and inorganic components in a common environment

A basic problem in the area of biointeractive systems relates to the wet-world-to-dry-world interface, from organism to biomolecule to organic material to inorganic material. For example, organism signaling may be done by small molecules or through conformational changes in large molecules. Converting these signals to electrical form will likely involve multiple intermediate steps using chemistry, photonics, or other means. Wet-to-dry interface issues are also intimately tied to biocompatibility.

Since many of the envisioned biomimetic and bioinspired systems will of necessity be tiny, they will require small, low-power processors for onboard control, similar to those discussed in *ubiquitous nanosystems*. These tiny systems will require advances such as nonconventional power sources and super-resolution optical imaging and sensing. Improved biocompatible materials and processes are needed for devices and for device-to-bio interface elements. For fluid analysis at smaller scales, methods for circumventing the limits imposed by stiction effects must be developed.

Nano for All

Many hard problems must be solved to enable the *nano for all* vision. These problems can be grouped in three areas: design methodologies, assembly methodologies, and inexpensive facilities access.

New technologies have historically been leveraged with existing technologies at the architectural level. The technology we now employ to build billion-device semiconductor systems was developed over the past 50 years. The design methodologies that enable systems architects to effectively utilize systems of such complexity were developed concurrently. If nanotechnology is to become pervasive and if it is to be employed in even more complex systems, we must make it accessible to designers and engineers working at the systems level.

While programs are in place to make nanoscale tools and technology available, the entry barrier is still too great for most interested researchers. Current nanomanufacturing technology is often based on expensive instrumentation available at only a few locations. Researchers must travel to those locations or ship devices around the country for multistep fabrication. The lack of standard techniques, tools, and interfaces forces users to have intimate knowledge of each fabrication process, and limits the exchange of personnel and ideas.

STRATEGIES AND NEEDS

Ubiquitous Nanosystems

- Explore new approaches for supplying or distributing power to tiny systems, including power scavenging and storage
- Explore close integration of sensing and processing functions in non-traditional silicon architectures like the cellular neural network, which may provide significant performance gains
- Develop homogeneous materials integration methods to facilitate close coupling of multiple sensor, processor, and actuator technologies
- Continue to explore nanostructured materials with exceptional thermal characteristics to alleviate heat dissipation problems

Bioinspired and Biointeractive Systems

- Introduce special bioinspired devices into information processors in a step-by-step manner, integrated with CMOS. Eventually, bioinspired components will represent a significant fraction of the chip area
- Encourage the development of nanotechnologies that will lead to special algorithm processors with break-through performance
- Encourage cooperation between the CMOS industry and nanosystems researchers to solve the problems of interfacing special algorithm processors to general purpose computers
- Fund development of microscopic, biocompatible systems integrating sensing, processing, communication, and task performance
- Encourage and support basic research in surface interactions that affect the functioning of biological molecules, structures, and systems
- Encourage and support basic research in micrometer-sized imaging systems, in which the sensing elements are subwavelength
- Encourage people to work on areas other than "nano for supercomputers", e.g., the biointerface area
- Identify a suitable mid-term applications goal (or "killer app") for cellular nonlinear networks or similar architectures to stimulate their continued development

Nano for All

Nanotechnology—more than any technology before it—spans multiple technologies, embraces multiple disciplines, and provides a broad range of functionality encompassing sensing, actuating, and control with processing power. Therefore we need new capabilities for system-level nanotechnology design. Programs should be developed to encourage creation of tools and interfaces, lower the barrier to entering the field of nanosystems design and fabrication, and thus increase both the number of researchers and their productivity.

New tools and new design methodologies must be consistent and compatible with the enormous infrastructure of current design tools and methodologies and software for our current microsystems technologies. This implies that they will be based on hierarchical functional building blocks and design rules, and methods for composing these blocks into systems. This will provide the necessary clean abstractions for system architects. Further, these tools should be developed in close cooperation with the design architects who will use them as well as the engineers who will fabricate the nanosystems.

System-level nanotechnology design should be based on the following principles:

- Tie current nanotechnology simulation tools to state-of-the-art microelectronics CAD tools
- Create a framework based on hierarchical representation and multilevel simulation, analysis, and verification tools
- Utilize parameterized libraries for synthesis from abstract models to fabrication processes
- Develop methodologies for extraction of "meaningful" parameters from physical models to behavioral models for devices that span energy domains

These tools and methodologies will greatly improve capabilities for the following essential tasks:

- Top-down approaches for design exploration
- Evaluation of mixed technology interactions, optimization, and architectural tradeoffs
- Construction of performance, reliability, tolerance, and fault models
- Incorporation of new materials, processes, chemistry, and devices in nanosystems
- Reducing the necessity for prototyping the first device
- Designing for manufacturing—the 1,000,001st device

Scientific and Technological Infrastructure Support

The three major themes comprising the vision of nanosystems presented in this chapter all involve multiple disciplines of science and engineering. The workshop participants, recognizing the importance of interactions across disciplinary boundaries, suggested several approaches to enhancing the infrastructure supporting such interactions:

- Convene NNI brainstorming panels mixing experts from biochemistry and biological sciences with those from physical sciences and electronics
- Create combined biological and semiconductor lab facilities
- Establish combined biological science and physical science programs at universities
- Create combined research groups in industry

PRIORITIES AND CONCLUSIONS

Bringing new technology to the world is a trial and error process. Consider Edison's development of the light bulb, or current methods for drug discovery. These processes take many iterative development cycles. Design and fabrication of complex systems is intrinsically difficult, and historically also involves several iterative levels of trial and error. We must leverage the lessons learned from previous heroic development efforts to speed up the introduction of nanotechnology to the mainstream. We have to "dirty a lot of paper" and we have to do it fast, going around the design iteration loops at an accelerated pace. To do so we need to develop low-cost fabrication methods, as measured in both design time and dollars.

Access to inexpensive, fast-turnaround technology by a large number of researchers will lead to many design iterations and learning cycles. With support for the appropriate infrastructure we can all learn from each others' successes and failures. We also need a lot of choices of technology. The promise of integrating both top-down and bottom-up assembly methods gives us more choices than either one provides separately. Establishing clean interfaces to the manufacturing process also increases choice since plug-and-play capabilities let the designer incorporate many related technologies.

Broad access to rapid, inexpensive fabrication processes is also essential for the education of a new generation of engineers and scientists. There must be a concerted effort to introduce a consistent view of nanosystems design and fabrication to graduate and undergraduate students in mainstream engineering programs.

Much fundamental science remains ahead. Priority should be given to providing access to low-cost top-down and bottom-up nanofabrication processes to the broadest range of researchers, while providing them with a tool flow enabling the integration of nanodevices into larger systems. The only way to create the revolution is by providing access to all.

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Appendix A. Abstracts

The Role of Nanoscience/Nanotechnology in Improving Chem/Bio Detection

Mario Ancona, Naval Research Laboratory

Chem/bio detection relies on transduction of chemical signals into electrical information, often indirectly, and then proper interpretation of this information. Nanoscience/nanotechnology (which in this context mostly means chemistry) can potentially improve this process by (1) aiding in its miniaturization; (2) improving selectivity by helping to push as much of the information processing to the front end as possible; and (3) increasing sensitivity. The latter two aspects are well illustrated by existing sensors that directly exploit highly selective biological mechanisms, e.g., sensors based on antibodies or on DNA complementarity. To achieve similar results for a broader range of analytes including materials that are gases, nonaqueous liquids or solids under ambient conditions, and to do it with efficiency, versatility and robustness, and all in, say, a butterfly-sized analyzer, presents a number of difficult challenges for nanoscience/nanotechnology. Recognizing that this is a very broad topic that cannot be properly treated within a short essay, below I give only a few idiosyncratic comments.

Identification of chem/bio agents in the laboratory with great sensitivity/selectivity (e.g., using mass spectrometry or fluorimetry) is of course highly developed. One way for nanoscience/nanotechnology to have impact is to further enhance the capabilities of the laboratory, e.g., by allowing one to work with smaller amounts of starting material or by increasing parallelism to speed an analysis (as occurs in a fiber-optic array used for differentiating huge numbers of DNA fragments). A second opportunity for nanoscience is in field applications where one wants to optimally combine good sensitivity/selectivity with ultrasmall size and power consumption. An example is a sensor array for point detection that is battery powered, remotely deployed, and designed to detect chemical warfare agents at parts-per-billion levels over many months of operation without service.

Generally speaking, assembling sensors into arrays is attractive because it can give redundancy, provide statistical enhancement (including combating false positives), yield greater dynamic range and enhance selectivity through the use of "orthogonal" sensors. With respect to the latter, the number of different sensors that can be usefully employed is limited by their selectivity. At present, the number of sensors in an array for chemical detection is kept quite small (<20) because their selectivity is low. By contrast, highly selective DNA arrays employ as many as 10^6 sensors and in nature the numbers are even higher, e.g., the rabbit's 5×10^7 olfactory receptors. Whether chemical sensor arrays will ever become this large will depend on the degree to which the selectivity of their component sensors can be improved. In any event, because these numbers are relatively small (compared with other nanoelectronic/nanophotonic/nanomagnetic applications), chem/bio detection makes a good leading application of nonevolutionary nanoscience with a fair possibility of payoff. Finally, it is important to note that while sensor scaling generally translates into reduced power consumption, lower packaging/servicing costs and higher speed, how sensor performance scales depends on the implementation.

When size/power are at a premium, e.g., in a field application, sensors that rely on direct electrical transduction, either chemiresistors or potentiometric sensors, tend to be favored, though NEMS-based sensors might also play a role. When such sensors are "large," they operate in what might be termed a continuum regime meaning that they are composed of a sufficient number of discrete

elements, e.g., polymer molecules or carbon particles, that the fluctuations associated with the underlying discreteness are negligible. This property means the sensor behavior will be much more predictable, regular, and uniform. And clearly, for maximal scaling of such sensors, they must be formed of the smallest possible elements that still display the desired chemical characteristics. Thus, for example, a sensor composed of micrometer-sized carbon particles will be far less scalable than a sensor made of 2 nm gold nanoclusters. As a result, the "optimum" sensor operating in the continuum regime would be formed of a nanostructured material and this is a key opportunity for nanoscience in the coming years. Some of the technical challenges for advancing in this direction involve the self-assembly chemistries, improvement in selectivity of the coatings, development of a broader spectrum of potentiometric coatings, minimization of contact resistances, etc.

Of course it is also possible to scale a sensor below the continuum limit and into what might be called the discrete regime. This regime has the potential for improving sensitivity because surface effects will become even more dominant and because of the possibility that new amplifying mechanisms will come into play, e.g., operating near a percolation threshold or with Coulomb blockade. Moreover, it is clear that one will need to enter the discrete regime if the goal is not to detect a concentration of analyte but rather to be sensitive to small numbers of analyte molecules even down to the limit of a single molecule. In the near term, the discrete regime presents substantial obstacles associated with collection, with nonuniformity, with nonlinear response (especially with multiple analytes) and with noise, all of which make practical detection very difficult. But with biology as an inspiration and a guide, sensor systems that operate in the discrete regime represent a major long-term goal for nanoscience/nanotechnology.

Information Processing

Dimitri A. Antoniadis, Massachusetts Institute of Technology

Fabrication of silicon-based electronic integrated circuits is today by far the most widely practiced form of nanotechnology. The success of "silicon nanotechnology" is due to the scalable nature of the core electronic devices (e.g., field-effect transistors) and to the scalable nature of subtractive lithography. The enormous leverage of this technology is due to the remarkable applicability of transistors and associated fabrication techniques not only in information processing, but also information storage, and information acquisition, transmission, and the interface to the physical world. As it is generally accepted that continuing progress in silicon nanotechnology is facing rapidly increasing challenges, both technological and economic, the focus of this workshop session is to ask what aspects of hitherto unpracticed or even undiscovered elements of nanotechnology can help continue the rapid progress of *information processing* that we have been accustomed to. Focusing then entirely on how to impact *information processing,* in my view the challenge for "new" nanotechnology is to find ways to interface with the silicon nanotechnology infrastructure. Here is my list of challenges in terms of urgency:

- Improved subtractive patterning in terms of resolution, placement and edge roughness will have the most direct impact, and of course it is the subject of enormous investments by the semiconductor industry and governments, worldwide, but still with no clear solutions for future silicon nanotechnology.
- Engineering of semiconductor materials properties in the nanoscale. The emphasis here is on improved transistor switching figure of merit impacted by channel mobility, transport velocity, and nonplanar channel structures. Examples include introduction of lattice strain and complex semiconductor/insulator heterostructures.

- Nanostructured semiconductor channel materials via additive patterning (partial self-assembly). Promising materials include single-wall semiconducting carbon nanotubes and perhaps semiconductor nanowires.
- Introduction of new "on-chip functionality," most likely in environmental information sensing but also possibly in specialized ultradense memory, via integration of molecular or organic electronic elements.
- Exploration of information representation and processing by means other than direct charging and discharging of individual circuit nodes. The basic element of this technology will have to be free of transistor-like electrostatic integrity requirements. There are no clear promising directions here for goal-driven research. Research will have to be curiosity driven with emphasis on fundamental understanding rather than early demonstrations.

Challenges and Opportunities in Nanomagnetics and Spintronics

David D. Awschalom, University of California, Santa Barbara

Control over spins and magnetic structures forms the basis for nascent spintronics that will lead to future quantum information technologies. There is a growing interest in the use of electronic and nuclear spins in solid state and molecular nanostructures as a medium for the manipulation and storage of both classical and quantum information at the atomic level. Spin-based electronics offer the unique opportunity for exploiting the robustness and parallel processing possibilities of quantum states by combining existing charge-based electronics with the spin-dependent effects that arise from interactions between electrons, nuclei, and magnetic fields. Here we discuss recent developments and challenges in creating, manipulating, and storing information in a variety of structures at the nanometer scale, including measurements that reveal an interesting interplay between the different spin degrees of freedom in devices (electronic, magnetic, and nuclear). In particular, we will review opportunities in materials synthesis, the assembly of nanostructures, the development of experimental tools, and relevant theory for the next generation of multifunctional electronics. Furthermore, we will examine different approaches that enable both "top-down" and "bottom-up" engineering efforts, including the wiring and assembly of biologically and chemically synthesized structures, to fabricate hybrid systems that will form the platform for future logic and storage. These efforts focus on investigating the underlying physics for processing quantum states at the nanometer scale, and reveal new opportunities for spin-based technologies. We will discuss several scientific and technological challenges to be addressed in order to enable significant advances in the field.

Interfacing from the Molecular to System Size Scales

Gary H. Bernstein, University of Notre Dame

In order to plan a strategy for future developments in signal transmission through an electronic system that contains nanoscale elements, certain assumptions must be made so that we can predict what it is that we must interface to:

1. **Silicon technology will scale successfully to at least the 10 nm gate length scale**, and as some predict, possibly to 1.5 nm gate length. Future "nano" technology must be distinguished from current, nanoscale silicon technology. As Intel points out, they have been doing nanotechnology for some years now. (Here I'll call that "SiNano" for simplicity.) For future nanotechnology to overtake SiNano it must make some drastic changes to the current paradigm. Single molecules (not aggregates of molecules) are possibly the only nanocomponents that can perform any reasonably useful function on a scale that beats a 1.5 nm-gate-length transistor. This could lead to

many other issues, but the discussion here is only about signal transmission. So, the assumption is that we are discussing molecules as the ultimate nanostructure.

2. **Future systems incorporating new nanotechnology will almost certainly contain SiNano technology** as well for signal restoration, input/output, etc.

3. **Applications in electronic systems are highly varied**, from portable, low-power handhelds to cryogenically cooled supercomputers. Not all solutions will apply to all problems.

4. **Signal integrity must be maintained.** Clock speeds will almost certainly attain a few tens of GHz in the not too distant future, given that power dissipation doesn't prove a showstopper. These systems will be fully microwave transmission systems, and must be designed as such at every step.

5. **Signals must originate at the molecular level and be transmitted all the way to the system level**, which is presumably off chip. Figure A.1 shows the complete system from the nanocomputing block through the SiNano system, where indicators *a* through *d* are transmission points under discussion in this panel.

Off-chip, or off-package scaling is a serious system speed bottleneck. It likely is not practical to think that thousands of interconnects can be made by either wireless or optical connections. No suitable silicon light emitters have been developed yet, and the sizes of waveguides and associated packaging might not be competitive with future electronic transmission formats. One idea being pursued at Notre Dame (Bernstein and Fay), called "Quilt Packaging," consists of thousands of nodules built on the vertical edges of chips. Butting chips together to connect the nodules will provide seamless, impedance-matched interconnects between chips. This will provide high speed and low power signal integrity between silicon or other heterogeneous materials and subsystems to create true systems-in-package.

Interconnects from the SiNano scale to the package level may be only a matter of scaling on-chip metal interconnects and adding pad drivers for gain. The number of inputs and outputs is approaching tens of thousands, but there seems to be more room for scaling in this regard.

Interconnects on the SiNano chip threaten to slow things down as resistance and capacitance increase. The move to copper has helped, and new low-*k* dielectrics will also help, but desired increases in speed will likely not keep up with the gains made in this realm. Also, layers of interconnect will go beyond 10 and become unwieldy. The quantum dot cellular automata paradigm offers as one advantage the possibility for keeping all line crossings on a single plane.

Contacts from molecules to conventional computing elements are worthy of a grand challenge since good contacts to molecules are not well understood, and there exists no acceptable solution to manufacturing contacts at the single molecule level. Without this, there is no "molecular electronics." Candidates include carbon nanotube contacts, or possibly direct contact to molecules by functionalized metals structures defined via ultrahigh resolution lithography. Bernstein's group is developing electron beam lithography technology for the 5 nm scale at which large molecules will be size compatible.
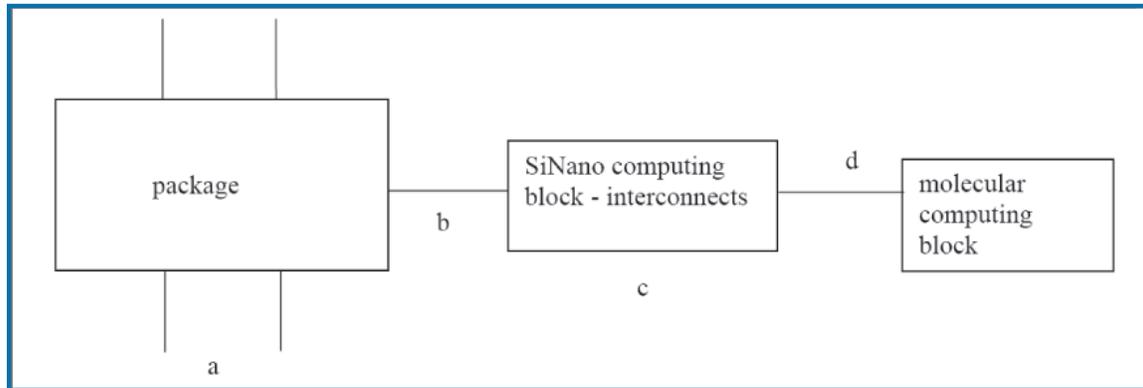
Figure A.1. Beam lithography model.

Impact of Nanotechnology on Optoelectronic Devices for Acquisition

Gail Brown, Air Force Research Laboratory

Challenges in sensing cover a wide range of issues depending on what part of the electromagnetic spectrum is being accessed and on the range at which the signatures needed to be detected. There is a continuing need for hyperspectral sensors, with high sensitivity in a large number of closely spaced wavelength bands, for chemical detection and target identification. There is a need for detectors with multifunction capabilities such as a combination of infrared and polarization sensing. There is a need for smart sensors that can process the signal real-time and provide meaningful data quickly to the warfighter. There is a need for reconfigurable sensors that can automatically adjust wavelength sensitivity and gain depending on the scene conditions. There is a need for small sensors and arrays that can be used in widely distributed systems for widespread signal detection and for sensors small enough to be embedded into structures for vehicle health monitoring applications. These are just some of the challenges for creating a future generation of sensors for acquiring data about the environment. For most of these challenges nanoscale materials and devices are a very promising solution.

Some of the nanoelectronics for acquiring will be based on nanoscale materials in micrometer-sized devices, and some will be nanoscale devices. For instance, superlattices can be used to design infrared detectors with high performance for long-range space-based sensing. Superlattices are composed of alternating layers of two different semiconductors with the layer widths (controlled at the atomic scale) on the order of 2 to 4 nm. Quantum dots are just now showing their potential for hyperspectral applications. Previously reported performance was too poor to be considered in an application. Quantum dots can be formed by molecular beam epitaxy on a semiconductor substrate or can be grown from solution and then embedded in a polymer matrix. Both forms will find niche applications depending on the device requirements. For instance, quantum dots in a polymer matrix would allow a flexible sensor that could conform to curved surfaces or mate more easily to a composite structure. New fabrication processes for heterostructure quantum wires open up new potential combinations of properties such as simultaneous infrared and polarization sensing, or even creating optical readout of the signal by taking advantage of the nonlinear optical properties of the wires. A gated nanopillar can be used to sense a single photon or to create a sensor whose wavelength range can be adjusted with a small change in bias voltage. This would be an example of a nanoscale device. There are also organic compounds that when crystallized have shown some remarkable ultraviolet sensitivity. Carbon nanotubes have even been shown to be efficient full-spectrum absorbers but are only just beginning to be tested in simple sensing devices. Besides carbon, there are other forms of tubes,

such as zinc oxide or silicon carbide, which are in early research stages and may prove to have some unique sensing properties. The types of sensors I have addressed all revolve around optical sensing so the list is by no means complete.

There are a variety of challenges to implementing the advanced sensors described above. One challenge is control of materials properties, such as composition, size, and defects at the nanoscale. Small variations have much larger effects on quantum confined materials than on their bulk counterparts typically. While many advances have been made in this area, there are still issues with size control of quantum dots for instance. A second challenge is in modeling the optical and, especially, electrical properties of small-dimensional materials. Surface effects play a much bigger role in a twenty-atom nanocluster than they do in a much larger crystal. Computational methods for simulation of transport in nanosized clusters or wires are still in their infancy and require further development to aid in designing nanoelectronic devices. A third challenge is fabrication processes for nanosized devices. Electron beam lithography or bottom-up self-assembly approaches can be used to make nanoscale patterns in a material. Making electrical connections and adding passivating layers or other dielectric layers on these patterns in order to construct a device remains a challenge, which must be met if laboratory test devices are to transition into a production environment. New processing approaches need to be encouraged such as supercritical fluid deposition of metals and dielectrics to line nanometer-size holes or to make a uniform layer, nanometers thick, with no pin holes.

Nanotechnologies for Space Sensor Systems

David A. Cardimona, Air Force Research Laboratory

Generation-after-next sensor systems for use in space should be smaller in volume and weight and have reduced power consumption requirements for both reduced launch costs and improved satellite maneuverability in orbit. At the same time, these systems should have similar, if not improved, sensing capabilities so that the user will feel comfortable taking advantage of the new technologies. In addition, on-chip data processing would be highly advantageous for increased speed and enhanced data handling. Several nanotechnologies promise to provide just such new properties.

Nanophotonic crystals are being developed that can convert sunlight into electric power, while others are being investigated for their "super lensing" abilities that will allow future imaging systems to beat the diffraction limit in resolution. Mechanical folding of nanopatterned membranes is being studied to form 3D nanophotonic structures. Thin metallic films perforated with periodic arrays of nanoholes can act as spectral bandpass filters or, if combined with nonlinear materials, as all optical switching elements. Other such nanostructured metallic films can enhance optical field transmission for weak signal detection, or act as plasmonic waveguides for on-chip optical signal processing. Biochemical processes are being pursued that can be used to pattern rows of single atoms into nanoelectronic circuits or optical waveguides for increased electrical or optical processing power and speed. Nanolayered semiconductor materials are being investigated with an eye towards on-chip cryogenic cooling of sensor focal plane arrays (FPAs). Other such semiconductor nanostructures are being grown with embedded quantum dots in the hope of obtaining tunable wavelength response. Quantum dots can also be immersed in electrostatically self-assembled organic polymers to detect optical signals. These polymer detectors can be formed into any shape, providing the possibility of developing curved FPAs for distortionless, wide-field-of-view optical imaging. Nanotubes have the ability to detect local magnetic fields, high energy particles, or optical signals. They can also be grown on curved surfaces, again yielding a possible method of producing curved FPAs.

These are just a few of the many sensor-related nanotechnologies presently under investigation in laboratories all over the world, with many of the leaders here in the United States. Funding for these research projects must continue at a substantial level so the United States can maintain its lead and bring these technologies to maturity during the next ten to fifteen years. As each new concept matures, a major challenge will be to bring these disparate technologies together and integrate them into new sensor systems of the future.

Nanotechnology System Packaging Issues

Donald M. Chiarulli, University of Pittsburgh

As with any early stage technology, devices and sensors have been the central focus of nanotechnology research to date. It has been widely forecast that these devices will enable a new class of multifunctional systems incorporating sensing, computation, data storage, and communications into a single package. This will be a new type of multitechnology system in which the component materials, devices, and interconnections span the domains of electronics, optics, mechanics, and fluidics.

In such a diverse system there will certainly be fundamental differences in the properties of the components. Incompatibilities between materials, differences in fabrication processes, and device feature scales are examples of issues that will inevitably arise. It seems likely that these differences will mean that nanotechnology-based systems will continue to segregate into sensor, processing, memory, and communications components in much the same way as current mixed technology microscale systems. If so, what is the substrate onto which these components will be integrated? How can we design such a substrate to preserve the benefits of nanoscale integration?

I suggest that such a substrate should have the characteristics below. Some are fairly obvious. Others are more subtle. Taken as whole, they represent a new paradigm for reliable nanotechnology system packaging.

1. The components must integrate into a 3D volumetric solid with interconnection through a central volume and components on the outside surface. This is the only way to preserve the communication density of nanodevice arrays (particularly if optical interconnects are used) and to minimize communication latency. This structure will also provide a means to separate signal propagation and thermal extraction paths (see item 5 below).

2. The same elements that provide interconnection paths must also support the structural integrity of the volume. In other words, this will not be a material in which electrical conductors or optical waveguides are embedded within a structural material (i.e. ceramic). Instead, this is an engineered material in which the waveguides, capillaries, and electrical conductors must themselves define the mechanical structure of the solid.

3. There must be a capability to spatially interleave mixed technology interconnections within the volume. For example, an array of optical channels must be able to share a region of the substrate with electrical signals and/or electrical supplies. Microfluidics might typically be integrated with optical or electrical channels designed such that the signals could interact with an analyte in solution.

4. The interconnection topology should be as flexible as possible but need not be completely unconstrained. For example, it is likely that arrays of devices will have common and parallel interconnection requirements. Other types of communication locality can potentially be identified and exploited.

5. Thermal extraction paths must be well defined. They can flow into the substrate (which can be actively or passively cooled). Preferably, thermal extraction can be done in the opposite direction of signal flow, through the outside surfaces of the volume.

These issues are common to all mixed technology systems at both micro and nano scale. As we move forward to creating systems from the devices that emerge from nanotechnology research it is imperative to concurrently develop new technology for packaging these systems.

Cellular Architecture, Wave Computing, and Device Characterization in Nanoelectronics

Leon O. Chua, University of California, Berkeley

In spite of the impressive advances in nanoelectronics research during the past decade, our focus so far has been directed almost exclusively at the physics and fabrication of *single* nanodevices. But what can we achieve with nanodevices? What properties must a nanodevice possess for it to be capable of information processing? Into what optimal architecture should nanodevices be imbedded to achieve orders of magnitude increase in computing power over conventional digital computers? What new computing paradigm is called for to harness this immense computing power? How do we develop circuit models of nanodevices so that future nano engineers can design a complete nanocomputer-on-a-chip in the same way that one designs a microprocessor? These important issues beg for answers in any concerted research program on nanoelectronics.

Integrated Sensing—Computing Cellular Nanoarchitecture

Even assuming that CMOS transistors can be scaled down to molecular size, the current von Neumann digital computer architecture will become impractical due to excessive power dissipation in the interconnecting wires. This problem can be overcome with a cellular architecture made of nanoscale computing units, called nanocells, which form a regular 2- or 3-dimensional array where each nanocell interacts only with neighbors located within some sphere of influence (e.g., nearest neighbors). Our recent research has proved that any such cellular array can be designed to compute or execute some functionalities (e.g., detecting edges of an image) by choosing appropriate cell interaction strengths, provided that the nanocells are *locally active* in a precise and easily tested nonlinear circuit-theoretic sense. This new computing paradigm, called *cellular nonlinear networks* (CNN), is *device independent* in the sense that *any* nano cell can be chosen provided it is locally active. A CNN can therefore be built from CMOS transistors, or any locally active nano or molecular devices.

Future molecular CNNs would be fabricated via molecular *self-assembly*, which is nature's way of producing molecular structure in reproducible manner via self organization, without recourse to lithography. Since molecular cellular structures will emerge spontaneously upon reaching their thermodynamic minimum (resulting from multiple, weak, reversible interactions such as hydrogen bonds, ionic bonds, and van der Waal forces between molecular subunits), they can be controlled with atomic precision. The information that determines the cellular architecture is coded in the structure and the dynamic properties of the nanocells.

Many operational CNN chips have been fabricated using standard CMOS technology. The latest (128 $\times$ 128 cell) CNN chip occupies 1.5 cm^2 of silicon area (via 0.35 μm CMOS technology) and dissipates only 4 watts of power. Because of its massively parallel architecture, this CNN chip can execute 10^{13} image processing operations per second (10 Tera OPs), and 10^5 video processing operations per

second. With this immense computing speed, the CNN chip has outperformed current commercially available supercomputers when tested on similar tasks. Indeed, it has provided an enabling technology to several mission-critical applications (e.g., detecting and tracking missiles, and controlling plasma instability in thermonuclear fusion reactors). This CNN chip has also provided the computing power necessary for operating an intelligent and adaptive stereographic camera (developed in Hungary), an impressive engineering feat which has recently been awarded first prize at the 2003 International Machine Vision exhibition held annually in Stuttgart, Germany.

The above CNN architecture is also being deployed in a Multidisciplinary University Research Initiative recently begun at the University of Notre Dame. Several light-sensing nanoantennas will be integrated directly onto each pixel, thereby greatly enhancing its sensitivity and processing speed. Since each nanoantenna occupies only a 2×2 μm area, it is possible to integrate at least 25 nanoantennas onto each pixel, each tuned to a different wavelength from the infrared through the visible. It is clear that the same technique will allow the integration of several sensors for different modalities (e.g., pressure, temperature, strain, toxic content, etc.) onto each pixel. Moreover, the CNN chip can be programmed to tune the parameters of each sensor to adapt to local conditions. Such pixel-by-pixel adaptation is similar to the human retina where each light sensor (rod) in the retina can independently adapt to the local brightness level over 8 decades of intensity, a situation one encounters, for example, when entering a dark movie house from a brightly lit lobby.

Active Wave Computing Nanoarray

The cellular nanoarchitecture represents a radical paradigm shift from conventional digital computing and calls for a new mindset and brain-like computing principle based on *active wave* computing via nonlinear dynamics and *non-Boolean* spatial-temporal logics. Such nonlinear waves are generated spontaneously via the device physics governing the nanocells, and their local interactions. Neither arithmetic nor mathematical operations are performed in this new paradigm. Instead, nonlinear active waves, which are entirely different from the familiar sound waves and electromagnetic waves, are generated within the chip and propagate like a forest fire. For example, one of many novel wave computing paradigms generates two competing nonlinear waves (one excitatory, the other inhibitory) *simultaneously* in such a way that the excitatory wave emanates from the desired target (e.g., a warhead), while the inhibitory waves emanates from the *nontargets* (e.g., decoys). The eventual annihilation resulting from colliding wavefronts can be decoded to yield the desired target, or the solution to some nonlinear partial differential equation (e.g., the Navier-Stokes equation) by several orders of magnitude faster computing speed than that of a supercomputer.

Nanodevice Characterization: A Serious Weak Link in Nanoelectronics Research

Not all nanodevices are useful from an information technology perspective. Certain devices are said to be inept in a precise technical sense that can be easily tested from explicit mathematical criteria. Often an inept device can be redesigned into a device capable of computing and artificial intelligence by massaging the device's parameters, such as doping, concentration, geometrical profile, chemical moiety, etc., in accordance with the *principle of local activity*. Nanodevices will remain novelty toys for nanodevice specialists unless they possess realistic nonlinear circuit models so that future nano circuit designers can simulate their exotic designs as easily and accurately as current CMOS circuit designers. A mathematically consistent theory for modeling nonlinear high frequency nanodevices, especially those endowed with exotic tunneling and entanglement quantum mechanical effects, will require training a new breed of design-oriented nanocircuit engineers. There is a dire need therefore that we address this very serious weak link in any concerted nanoelectronics research program.

Nanoelectronic Computing Architectures

Larry Cooper, Office of Naval Research

The question that has always accompanied research on nanoelectronic devices is: ***How are they going to be used?*** That is, how can nanodevices be incorporated into a circuit architecture that provides revolutionary capability compared to existing technologies? We assume that silicon MOSFETs, scaled to 5 nm gate lengths, will be developed, but will never provide the performance needed by the Navy. The Navy Grand Challenge in Multifunctional Electronics for Intelligent Naval Sensors (1998) envisions technologies providing performance far beyond what can be achieved through the downscaling developments in silicon very-large-scale integration (VLSI). The goals are to pursue nanoelectronic technologies leading to the following performance enhancements compared with current technologies: improve logic speeds by $100\times$, reduce power supply requirements by $1000\times$, and decrease sensor volume by $100\times$. Other features will be nonvolatility, radiation hardness, replacement of mechanical devices, and a realistic manufacturing technology. These technologies will affect many Navy systems, such as autonomous vehicles (land, air, and underwater), radar, robotics, satellites, portable computing and communications.

Devices that can be considered as nanoscale devices include: nanometer-gate-length silicon MOSFETs, single electron transistors, resonant tunneling diodes/transistors, quantum wire devices, quantum dots, carbon nanotubes and other molecular devices, spintronic devices, nanomagnetic devices (such as Hall effect, giant magnetoresistance, tunneling magnetoresistance, and domain-controlled logic devices), and superconducting devices. All of these have at least one measured dimension in the sub-100-nanometer range.

Based on the criteria given above, several of these devices are not viable candidates for processing. Nanoscaled silicon MOSFETs may go as far as the roadmap allows but speeds will not be great. Power dissipation will limit their applicability in dense circuits. Besides, the commercial sector will drive this to the end. Carbon nanotube transistors are not considered as candidates due to the difficulty in control of properties and in locating them in any reasonable layout. Further, their electrical properties suggest only a small improvement in capability for transistor circuits. Their most obvious application is as sensors which may be integrated with processing elements. Superconducting devices are not feasible for large-scale circuits, and the cooling requirements and manufacturing complexity indicate opportunities may exist for special niche applications. Molecular electron devices have high resistance and serious contact problems and are not considered further.

For the 10-year time frame, there are several areas for implementation of nanoscale devices in data processing.

Digital Signal Processing Using Resonant Tunneling Diodes

Current capability includes all of the required adders, analog/digital converters, latches, SRAM memory, etc., based in indium gallium arsenide with clock speeds up to 25 GHz. This technology uses resonant tunneling diodes (RTDs) coupled with high-electron-mobility transistors (HEMTs), with an RTD area of about $4\,\mu m^2$. Power dissipation is very low and device count is up to 5 times fewer than in silicon FET technology. The future path for RTDs is to shrink the area to $100\,nm^2$; to exploit the antimonide-based heterojunction materials; to devise a three-terminal RTD; to develop full RTD based circuits; to explore multivalue logic and memory using stacked RTDs; and to demonstrate terahertz digital signal processing speeds.

Cellular Nonlinear Networks

This is a special architecture adapted to image processing at extremely high speed. Current implementations use ordinary VLSI at 0.25 μm. A universal image processing computer on a single chip, with 4 million devices and 4 watts power dissipation, has been demonstrated; it has a throughput of 10,000 frames per second with a 128×128 cell array. This computer uses mixed analog and digital circuitry. The challenge for the future is to use this architecture to incorporate nanoscale devices, such as single electron transistors and RTDs, for more compact and lower power chip computers. Department-of-Defense-based special applications need to be identified so that special purpose CNN chips can be delivered. IR, visible, acoustic, and RF sensors need to be integrated with the cell array to generate smart sensors.

Magnetoelectronic Reprogrammable Logic and Memory Circuits

There have been demonstrations of magnetic elements being used for logic and memory. These include hybrid Hall effect devices and both giant magnetoresistance and tunneling magnetoresistance devices. Circuit designs have been completed. Devices are capable of 100 ps switching speeds and are nonvolatile. Future development must include better understanding and control of switching processes of nanomagnetic contacts/elements, inclusion of other materials, reduction of writing currents, and reduction of element feature size to 10 nm. The development of functioning spintronic devices is a major issue. The injection and control of electron spin currents must be achieved. Materials exhibiting ferromagnetism at room temperature are required.

Vertical Magnetic Random Access Memory

Current developments demonstrate RAM performance with critical dimensions of 100 nm. Modeling of memory architectures indicates an ultimate bit density for nonvolatile RAM of 400 Gb/in^2. Individual bit switching speed is below 100 ps. Vertical MRAM improves as dimensions shrink. Future activities include reducing feature size to 10 nm, development of high throughput lithography and processing technologies and on-chip integration with digital processors (such as central processing units and digital signal processors).

Quantum Cellular Automata

This concept makes use of coulomb interactions between trapped charges or uses interactions between magnetic elements through magnetic dipole fields. Currently, only the charge interaction model has been demonstrated using metal dots at very low temperatures. Quantum celluar automata (QCA) offer the possibility of extremely low power dissipation. Circuit models have been simulated. The future is very uncertain since a technology must be developed which can operate at much higher temperatures. New materials, such as semiconductor nanocrystals, have been suggested.

Room at the Bottom?

Alan E. Craig, Montana State University

General Commentary on Storage Attributes

What can be new for nonvolatile nanostorage? Why not engineer until its density encounters the discrete nature of atoms?

Some successful nonvolatile storage depends on cooperative phenomena. Magnetics is the chief example. Magnetic domains have already shrunk to near their feasible limits. Although substantially smaller stable domains might be devised, the derivable signal becomes steadily harder to detect. Giant magnetoresistance based detection sees limits on the horizon.

In many applications, access bandwidth can be more important than density (although with spinning disks one tracks the other). Bandwidth in nonvolatile storage was ignored for a long time, even though it contributes to latency when an entire packet delivers an instruction. Latency-hiding software controlling storage hierarchy hardware (invoking data locality, lookahead data calls, etc.) has obscured the role of bandwidth deficiencies in process delay. Recently, however, memory bus bandwidth has been pushed to improve. The time (and monetary) cost of accommodating huge but slow tertiary file storage has become excessive. Rummaging through nonvolatile storage takes too long to be useful for much more than backup. While high access bandwidth DRAM is nearly free, it is volatile.

Dissipative storage processes create heat. Heat destabilizes data. The data trap potential must exceed the average thermal energy to provide resilience against phonon and phonon-coupled perturbations. Statistics can be calculated from the density of states. A tradeoff arises that might be nonlinear, like a Laffer curve. Low barriers between initial (unwritten) and final (e.g., trap) states confer reduced energy dissipation and less heating. Even though they are less resilient as impediments to thermal erasure, the fact that accessing the data they protect releases less heat is advantageous. For quantum-scale data structures, these considerations could constrain performance.

Consider the retrieval of useful data from immense data storage repositories. Retrieving a needed subroutine is difficult when the called object is well specified. Retrieving vague but relevant references within the time window of utility, when the address is not only organizationally remote but is not precisely known, is an extraordinary challenge. (Consider the declining utility of search engines.) A high bandwidth intermediate store serving as an efficient storage interrogator and switch node for process calls can ameliorate this deficiency (nonvolatility and extended persistence optional). Solid state disk technology provides this function, for example.

A Plasmon Proposal for Dense Storage

Atoms per bit. How many? How closely packed? A signal-to-noise ratio of ~ 6 can be reasonably extended, with acceptable coding overhead, to produce a bit error rate of ~ 1 in 10^{15}. For larger files, the bit error rate must often be even smaller. Assuming the signal-to-noise ratio equals 6, 36 photons per bit must be detected in the shot noise limit. At $\sim 30\%$ participation, 125 storage atoms are needed per bit. If in each linear dimension every fourth atom records data, then $20 \times 20 \times 20$ atoms (in three dimensions) or $\sim 1000\,nm^3$ per bit are required (assuming atoms on 0.5 nm centers). $1\,cm^3 = 10^{21}\,nm^3$. So 10^{18} bits/cm^3 can be recorded, but $10 \times 10 \times 10$ nm is a small voxel, perhaps impossible to address in a volume medium without being overwhelmed by crosstalk. In an area storage format, 10^{12} bits/cm^2 represents the top end. (Present day magnetic disks have area density exceeding 15 x 10^9 bits/cm^2.) Stacking disks (say 5 per cm) could provide up to 5 x 10^{12} bits/cm^3.

Here are two related sidebar calculations:

- Disks with a rotation rate of 4000 rpm, or 66 rps, match a 266 MHz bus clock rate. So each rotation reads, on the average, 4,030,000 bits from a single track with a radius of about 1.9 cm, or about 120 mm around. Calculation shows the track holds a bit every 30 nm.

- No moving parts allow more stacked layers per cm and higher volume density. Consider an optically addressed memory using a VCSEL array on $10\,\mu m$ centers for illumination. You would need 10 layers of quarter wave stack, top and bottom, or $5 \times \lambda/n = 5 \times 850\,nm/3 = 1.4\,\mu m$ as mirror structures per VCSEL layer. Add a detector layer: $\sim 5\,\mu m$. Add the storage medium; as an example, for spectral hole burning in absorbers with modest oscillator strength, material thickness of $\sim 1\,\mu m$ suffices. (Spectral hole burning, however, is volatile.) Add drive and detection wire printed circuit boards. The total thickness could be as little as $\sim 20\,\mu m$ per layer. Double this dimension to accommodate spacing shims; you could still get 250 layers per cm. Each layer has 1,000,000 pixels with 1,000 spectral holes, giving a storage density of $250\,Gb/cm^3$. Decreasing the pixel spacing to 2 gives 25 times that capacity or $6.25\,Tb/cm^3$.

Now consider an alternative spectrally selective scheme. Metallic nanoparticles exhibit plasmon resonances. The optimal optical scattering frequency depends on the volume and morphology of each particle. An Austrian team, at Graz, has shown that particles varying in diameter from about 30 to 150 nm exhibit broad scattering resonances for incident light. The scattering wavelength range for each size distribution covers about 80 nm, so that about 5 distinct ranges could span the visible spectrum.

Here we suggest that local surface plasmon resonances occur on even smaller nanoparticles, in the $10-30$ nm range. Formed as thin shells (rather than as solid particles), they might support long-range surface plasmon modes, antisymmetrically coupled surface plasmon perturbations carried on both surfaces simultaneously and coupled by field overlap and commensurate propagation wavevectors. For example, at $\lambda = 628$ nm and with the refractive index of the bounding dielectric equal to 3, a shell of radius 33.3 nm propagates one wavelength around its periphery. (Bending losses remain to be considered.) Long-range surface plasmon modes on planar silver films have been measured to propagate over 10,000 wavelengths to 1/e absorption. This indicates a propagation linewidth of less than 20 GHz. Using 50 different size shells, one could then cover aggregate optical spectrum 1 THz in extent.

Consider using 32 shell sizes, with accompanying distinct spectral signatures. Perhaps 20 shells, each of a different size, could be placed (or synthesized) in an optically addressable spot, say 500 nm in diameter. The combinatorics for choosing 20 sizes from 32 possibilities, with no two identical, is $32! / [20! \times (32 - 20)!]$. This evaluates to 2.26×10^8, (or $> 2^{27}$) different spectral patterns from a pixel, with the spectral word always containing twenty symbols. A density of 4×10^8 pixels/cm^2 would give $10.8\,Gb/cm^2$. Each pixel conveys one of 2.26×10^8 values approximately every 100 picoseconds in a thirty-two place word.

Nanomagnetics, Semiconductor Spintronics, and Quantum Storage

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Recent advances in semiconductor spintronics, in particular the development of ferromagnetic semiconductor materials (e.g., gallium manganese arsenide, indium manganese arseninde, gallium manganese nitride, cobalt-doped tin oxide) and the nanostructure-level control of nonequilibrium spin dynamics in semiconductor hybrid structures, provide the exciting potential for seamlessly combining memory/storage and processing/logic capabilities on the same chip. The active manipulation of multifunctional carrier charge and spin dynamics in semiconductors (using external electric and magnetic fields as well as light) may lead to novel disruptive nonvolatile memory (and perhaps reprogrammable logic) technologies. The subject of semiconductor spintronics is, however,

in an early basic research stage with rapid current accumulation of fundamental knowledge. Specific applications (most likely coming first in storage and nonvolatile memory or as sensors and filters) are still several years away. The great deal of recent research activity in semiconductor spintronics is discussed in a comprehensive review article with a reference list of more than 800 research articles [1].

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Nanophotonics

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Nanoscale science and technology are playing an increasingly important role in development of various science and engineering fields. Optical and photonic technologies are recognized enablers, making a significant impact not only on engineering future information systems (e.g., computing, communications, lighting, sensing, display, and high resolution imaging), but also advancing science and technology areas in biology, chemistry, physics, and medicine. However, as optical technology develops, it is evident that there is a growing need to establish reliable photonic integration technologies. This includes the development of passive as well as active optical components and devices that can be integrated into optical circuits and systems such as filters, switching fabrics that can be controlled either electrically or optically, optical sources, detectors, amplifiers, etc. It is evident that further advances in nanophotonic technology will rely on our ability to develop (i) efficient design and modeling tools, (ii) advanced nanofabrication techniques, and (iii) visualization and imaging tools (for both structural and functional tests).

We explore the unique capabilities and advantages of nanotechnology in developing next-generation integrated photonic chips. Our long-range goal is to develop a range of photonic nanostructures—including artificially birefringent and resonant devices, photonic crystals, and defected photonic crystals to tailor spectral filters, and nanostructures for spatial field localization to enhance optical nonlinearities—to facilitate on-chip system integration through compatible materials and fabrication processes. The design of artificial nanostructured materials, photonic crystals, and integrated photonic systems is one of the most challenging tasks as it not only involves the accurate solution of electromagnetic optics equations, but also the need to incorporate the material and quantum physics equations. Near-field interactions in artificial nanostructured materials provide a variety of functionalities useful for optical systems integration. Furthermore, near-field optical devices facilitate miniaturization and simultaneously enhance multifunctionality, greatly increasing the functional complexity per unit volume of the photonic system. Finally, and most importantly, nanophotonics may enable easier integration with other technologies: electronics, magnetics, mechanics, chemistry, and biology.

Challenges for Nanophotonics: Advancing Integration Technologies

Michael. A. Fiddy, University of North Carolina, Charlotte

Lack of integrated functionality at the device level drives up the design cost of optical components and systems, as well as assembly costs. Optical devices are generally still assembled from discrete components, which is costly and results in low yields. Next generation optoelectronic components will utilize quantum effects and involve a greater integration of active and passive electronic and

optical components onto a single platform. This will necessitate alignment, finish, and feature sizes that are made with tens of nanometer precision. Candidate platforms are beginning to emerge; of particular note are photonic crystal circuits that have now been shown to demonstrate essentially all of the functionality needed in, for example, an "all optical router." Integration of this functionality into a single "data-in-the-optical" chip and then volume production of such chips plus nanotapered connectors to fiber will require a radical change in how these devices are made.

Optoelectronic integration follows two approaches: hybrid and monolithic. Hybrid is packaging-related and brings together different materials and components with great precision, as illustrated by the classic silicon optical bench. It might bring together the "best of the best" sources, detectors, micro-opto-electro-mechanical components, etc., onto a single assembled platform. Monolithic integration is equally challenging at present but may eventually be more manufacturing-friendly. Considerable research and development is required in order to achieve a diversity of functionality through a single platform. However we should be pursuing solutions that lend themselves to design and fabrication for manufacture and test. Methods for replication, e.g., via stamping or molding of nanoprecise features in a variety of materials, requires significant research and attention if we are to be able to manufacture devices based on 2D and 3D functionality, especially to surface physics and chemistry at the nanoscale.

Our longer term goals, as a country, should be to advance R&D that leads to microsystems based on chip-scale integration. The field of nanophotonics is important because it not only introduces a new way of thinking about and designing optical devices, but also offers possibilities for monolithic integration. Subwavelength optical elements are nanoscale structures with critical dimensions ranging from 10 nm to hundreds of nm. They need only be a fraction of a wavelength thick and can serve as building blocks for various optical processing functionalities. They are primarily subwavelength diffraction gratings, which can function as polarizers, waveplates, filters, photodetectors, phase modulators, microlenses, etc. They can also be fabricated directly via e-beam lithography, or e-beam lithography could eventually be used to make molds to produce these elements at low cost by nanoimprint lithography.

Nanophotonics includes fabricating photonic crystals, control of propagation (e.g., delays) and local fabrication of nanodots, nanodomains or nanocomposites which can be used for local control or sensing purposes. Nanoscale precision is required for the manipulation of light. This has primarily focused on linear operations to date with very little having been published on nonlinear operations. Recently announced results on Raman light emission from silicon light wires and the potential for fabricating a silicon optical amplifier are significant.

We need strong capabilities in integration technologies, especially in advancing CAD tools for accurate modeling and design. When integrating and interconnecting passive and active components on a chip, the need is for tools that facilitate manufacturing and testing. UNC Charlotte and its partner institutions (see Figure A.2) are using this approach to address longer-term challenges in nanophotonics.

Figure A.2. Partner institutions in the UNC photonics effort.

CNN Single-Electron Transistor Circuits and Architectures

Stephen M. Goodnick, Arizona State University

While semiconductor dimensions continue to shrink in accordance with, and sometimes in contradiction to, the International Technology Roadmap for Semiconductors [1], an eventual end to the roadmap is anticipated around 2015, precluding further scaling of CMOS technology. Alternative technologies are desired which will allow continued increase in the density of memory and logic into the terabit regime. At the same time, there is a realization that the architectures employed at ultrahigh densities may be quite different than those in, for example, current microprocessor design. New architectures may be necessary in order to accommodate new device concepts and to accommodate the increasing need for fault tolerance as device-to-device fluctuations become larger at the ultimate limits of integration. It is likely that conventional digital architectures will coexist with special purpose systems using nanoscale devices which will perform parallel analog processing at much greater speed, utilizing algorithms such as those based on quantum computation and biologically inspired cellular architectures. "Nano" integrated circuits are envisioned as a hybrid of conventional CMOS digital/mixed signal circuits, massively parallel nanoarchitectures for special purpose computation, and ultradense memory.

Single-electron tunneling (SET) transistors [2] have attractive properties which make them candidates for implementing ultradense and complex signal and image processing systems. SET devices satisfy hardware requirements for large-scale neural networks such as local interconnectivity, small device size, and low power consumption. Current fabrication technology allows the integration of 10^{11} SET transistors per cm^2 and a power consumption of 10^{-9} W per transistor [3]. Ultimately the goal is to build SET transistors capable of operation at room temperature and compatible with conventional CMOS process technology. The potential for very dense arrays of SET transistors make them attractive for the realization of cellular nonlinear network (CNN) circuits [4, 5], where locally connected cells may alleviate the necessity for individual external interconnects to every cell. The main disadvantage with SET devices is the difficulty in fabricating structures with sufficiently small capacitances to function at room temperature based on current lithographic techniques. Also, device to device variations for present structures are quite large, an issue that has to be overcome by greatly improved process technology, or some scheme of self-assembly to realize uniform arrays of structures. Analog CNN architectures offer some promise in this regard as they are less subject to process variations that are problematic for all digital-based technologies.

Various schemes have been considered for using single-electron systems to construct CNN architectures. Quantum cellular automata (QCA) [6] circuits based on few-electron cells have been shown to satisfy the local activity requirements of CNN for signal processing and similar applications [7]. CNN cells based on capacitively coupled SET inverters have been simulated, and are capable of simple image-processing-type algorithms [8]. Phase coupled single-electron circuits have also been proposed as the basis for SET CNN architectures [9]. All such schemes show the potential for the implementation of CNN algorithms with low power dissipation and reasonable speed. The building blocks of such circuits, such as simple QCA cells, silicon SET inverters, or coupled SET current mirrors, have usually been demonstrated at low temperature, although recent results from Japan and Korea have demonstrated multidevice circuits at elevated temperatures. The greatest challenge at present is the fabrication of silicon-based SETs circuits of more than just a few SET transistors. This would demonstrate experimentally the basis of functional cell building blocks that can be reproducibly manufactured and modeled for higher level design.

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Massively Parallel Optical Interconnects and Advanced System Architectures for Rapid Data Processing

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Increases in data handling capacity are being driven by growing demand for large bandwidth data transfer. For example, phased array radar systems may include video and simultaneous signal routing from multiple sensors. Computational processing speed is also constantly growing, but will approach a bottleneck due to the limitations of on-chip and chip-to-chip data transfer. The ideal approach to meet these increasing requirements is the use of optical networks to enable high data rates. Unfortunately, traditional semiconductor-based optical networks employ edge-emitting lasers that are large compared to transistors, consume large amounts of power, and are prohibitively expensive. However, the development of vertical cavity surface-emitting lasers (VCSELs) has allowed the realization of optical networks that address these shortcomings. VCSELs are small in size and have low power consumption, thus enabling highly dense, two-dimensional arrays of devices to be integrated on-chip. The manufacturing technology used for VCSELs also allows a dramatic reduction in cost, allowing their widespread use in many high bandwidth systems.

Despite the adoption of VCSEL technology, optical data capacity is still limited by the complexity of the interconnect schemes used in the system architectures. Device geometries often require costly packaging and assembly techniques to enable signal generation, routing, and detection through optical fibers. The device geometries also limit the complexity of the network topology to simple point-to-point signal links. Even with the use of wavelength division multiplexing, the performance and cost of optical systems make them unsuitable for certain applications. OptiComp Corporation

is developing a novel approach to address these challenges. Our architectural approach enables high data throughput, high switching speed, low latency, and system scalability through advanced network topologies based on an integrated optoelectronic switch. This switch consists of pairs of monolithically integrated VCSELs and resonant cavity photodetectors interconnected along a common waveguide.

Different levels of system connectivity and functionality are available by interconnecting the optoelectronic switches in various configurations. For example, a distributed crossbar switch with N access ports, referred to as an N^3 architecture (N^3 interconnect paths), can be realized by interconnecting an N element VCSEL array with an array of N photodetectors. Each VCSEL and photodetector are connected using an interconnect media such as silica-based waveguides and/or optical fibers. Using this configuration, each port can listen to all interconnect paths simultaneously. When a port senses no traffic on an interconnect path, it can transmit its signal onto that path. This implementation uses single-wavelength switches on parallel interconnect paths, but an alternative N^3 network can be realized with our optical switches operating at different wavelengths using wavelength division multiplexing. Each network port has switches operating at different wavelengths, which are routed along a common optical path.

Our integrated optoelectronic switch permits transparent optical data transport, thus allowing signal routing without the need for detection and subsequent retransmission. This optical transparency reduces the latency of the system, which dramatically improves parallel or distributed data processing. More importantly, the parallel nature of the N^3 network topology makes the system redundant and fault tolerant. If one optical path is broken, the system can route the optical signals on another parallel path, thus allowing the system to function. Further complexity in network topology allows for the realization of N^4 architectures by using parallel N^3 systems. N^4 topologies allow for increased scalability, thus dramatically increasing the data handling capacity of the network. Using OptiComp's integrated device technologies and chip-to-chip data transfer via interconnecting waveguides, massively parallel optical interconnects can be realized in a small-form factor. The combination of device integration and highly functional network topologies offers an ideal approach to solve many of the problems of current optical networks.

Future optical networks will likely employ similar approaches. Simple point-to-point interconnecting schemes are inherently limited in their data handling capacity. More complex and functional interconnect schemes are required to enable higher capacity systems. However, the interconnection schemes will be limited by items such as cost constraints, system performance requirements, and device geometries. The trend toward device integration to increase functionality, reduce chip size, and lower cost is being pursued by multiple researchers. Combinations of different kinds of devices, including both passive and active optical devices, as well as electrical devices, will likely be seen in the coming years. However, the increase in device density will be limited by issues such as power dissipation, thermal management, and signal crosstalk. Challenges in manufacturing approaches, including maintaining yields and reproducibility, will also result from the increase in device packing densities. The experience of the electronics industry, which has undergone similar development paths, will likely be of great benefit.

Nanoelectronic Technologies Coexisting with CMOS

Mark Johnson, Naval Research Laboratory

In most competitive applications, the technology that rises to success is (i) inexpensive, (ii) well established, and (iii) has performance that is adequate for the task. According to the scaling demands of the silicon roadmap, a number of key process steps have requirements demanding solutions that are not yet known. This has led to metaphorical predictions that CMOS technology will face a developmental "brick wall" around 2007. CMOS is a very successful technology. The success of Moore's law is well known and, furthermore, processor speed doubles every 1.5 years while the cost per device shrinks by 25% per year. Logic process technology is driven by 3 key areas: (1) transistor performance (gate oxide integrity, channel mobility), (2) patterning and etching of nanometer lines, and (3) fabrication of low RC interconnects. Intel will begin production of FETs with 30 nm gate length in 2005, while FETs with 20 nm gates are in development and 10 nm gate FETs exist as research prototypes. It is likely that CMOS will continue to be the dominant information processing technology for the next ten years. New, disruptive nanoelectronic paradigms may find niche applications during this time, and may eventually come to dominate some application areas in the future. The technology that will be dominant in thirty years has probably not yet been introduced. Basic research should support a wide variety of approaches, including fabrication techniques described as "bottom-up" as well as "top-down." Applied research should recognize that early generations of novel devices should be compatible with CMOS.

Terahertz Interactions with Nanophase Materials

James Kolodzey, University of Delaware

At terahertz frequencies, materials have unique absorption characteristics that are attractive for medical and cancer diagnostics, penetration imaging through objects, astronomy, standoff sensing of biological and chemical agents, materials spectroscopy, and wideband communications. These properties result from the resonances of molecular bonds and intraband energy states. Nanophase materials and nanocomposites have a high density of interfaces that are modified by quantum size effects, which makes the terahertz frequencies ideal for material analysis and for stimulating particular responses.

There is a need to investigate the response of nanostructures to incident terahertz illumination, for the purposes of nanomaterials characterization, and as a probe to induce oscillations and reactions for device and sensor applications.

Research Topics

The characteristics of materials and nanostructures are not yet well known at terahertz frequencies. The effect of terahertz illumination on nanostructure properties such as electrical conductivity and mechanical resonances needs to be measured and theoretically analyzed.

Architecture and System Integration

Philip J. Kuekes, Hewlett-Packard Laboratories

The integrated circuit, manufactured by optical lithography, has driven the computer revolution for four decades. If we are to continue to build complex systems of ever smaller components, we must find a new technology that will allow massively parallel construction of electronic circuits at the

atomic scale. To do so we must develop both the molecular electronics building blocks and CAD algorithms for such a reconfigurable technology.

Integrated circuits as currently manufactured must be perfect. They are sufficiently complex that if they weren't, they wouldn't work. This perfection comes at an increasingly high manufacturing cost, as the requirements for ever improving precision become more stringent with ever smaller feature sizes. The capital expenditures needed to achieve the mechanical precision required for such perfection may be prohibitive long before the feature sizes in integrated circuits shrink to a few nanometers. Defect tolerance, which is the ability for a circuit to perform perfectly even with broken components that result from manufacturing mistakes, will be essential in the electronics of the future.

The technical problem we face is to make extremely small electronic components (at the atomic scale), use very large numbers of these components to make very complex circuits, but manufacture these circuits at much less cost than today's integrated circuits. This requires many disciplines to work together. To make them function at the smallest scales we use quantum physics. To achieve massive complexity we use computer architecture. To keep them inexpensive we use low mechanical precision and do self-assembly with chemistry. And to deal with the inevitable defects of chemical self-assembly we use defect-tolerant design algorithms.

One potentially scalable device consists of two crossed nanowires sandwiching an electrically addressable molecular species. The approach is extremely simple and inexpensive to implement, and scales from wire dimensions of several micrometers down to nanometer-scale dimensions. This structure can be used to produce crossbar switch arrays, logic devices, memory devices, and communication and signal routing devices. The device is either partially or completely chemically assembled. The key to the scaling is that the locations of the active devices on the substrate are defined after the devices have been assembled, not prior to assembly. This architectural approach allows us to address the functions of interconnect, memory, logic and input/output.

The first function we require is interconnection, creating a physical circuit to implement any logical wiring diagram. The electronic switch is a quantum state molecular switch forming an electrically adjustable tunnel junction between two wires. The chemical state of the molecular switches determines the tunneling resistance between the two wires. Each switch consists of two crossed wires sandwiching an electrically addressable molecular device. The state of each switch is determined by applying set or reset voltages to the row and column of that specific switch.

Memory is the second function we require to reinvent the integrated circuit. The crossbar architecture is ideally suited to constructing memories. The physical advantages of the molecular wire crossbar memory are in its scalability, low power consumption, the well-defined threshold voltages of its switching elements, low sensitivity to fields and temperature, and a non-destructive read process. The molecular wire crossbar memory is basically a voltage-controlled device, and therefore the fact that it contains components with relatively large resistance is actually an advantage in terms of power consumption.

Diode logic is performed by a programmable logic array of nanometer-scale crossed-wire devices. Each crossed-wire device comprises a selectable diode junction formed by a pair of crossed wires. A vertical nanowire is configurable as an AND gate and a horizontal wire is configurable as an OR gate. The very desirable property of this invention is that a single molecular wire crossbar, having diodes pointing in one specific direction, e.g., always from the vertical to the horizontal wires, is of a form

that allows an AND programmable logic array followed by an OR programmable logic array. This permits performing any logic that can be represented as a sum of products in a single logic array.

The major roadblock to building nanoelectronic circuits based on a crossbar architecture is the interconnection between the "outside world" and the nanoscale resources. This requires a hard-wired set of connections to perform multiplexing and demultiplexing functions between a crossbar based on nanoscale wires and the driving circuitry, which will most likely be CMOS. One proposal for creating the demultiplexers needed to address a single nanowire in an array is to use a statistical chemical process that has a 50% probability of making a connection between a nanowire and a conventional CMOS wire connected to driving electronics. This process completely eliminates the necessity for precision alignment between the layer of nanowires and the CMOS drivers. Shannon demonstrated that a random code is good with very high probability, although there is a low risk that some nanowires will remain unaddressable. The number of addressing wires, and thus the amount of CMOS circuitry, is about 2.5 times that required for an ideal binary tree demultiplexer, and a fairly sophisticated discovery algorithm must be executed to identify each wire.

The key task of the architectural community in the immediate future is to develop a sense of the tradeoffs between the computational costs of CAD algorithms to repair defects and the manufacturing costs of avoiding defects in the first place. Biology has struck one balance. We need to find the appropriate balance for nanotechnology.

Nanophotonic Devices for Sensors

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Owing to the difference in optical and electronic wavelengths and the relative strengths of optical vs. electronic interaction, nanophotonics includes a range of evolving fields in science and technology at two diverging length scales. Materials and devices are patterned in a periodic fashion (in one, two, or three dimensions), with minimum feature sizes corresponding to a quarter of an optical wavelength (typically 50–250 nm for materials at visible and near-infrared wavelengths), but overall dimensions are considerably larger. These "photonic crystal" structures range from commercially deployed 1D-patterned photonic devices, such as distributed feedback lasers, distributed Bragg reflector lasers, vertical cavity surface emitting lasers (VCSELs), thin film interference filters, and fiber Bragg gratings, to 2D- or 3D-patterned structures presently under development. An important parameter for these structures is the refractive index contrast—the relative difference in index between materials—which determines how strongly the light is confined by each interface and therefore the size of the overall structure. High light intensity through strong optical confinement can also enhance nonlinear optical properties. A second important characteristic is loss, which is typically degraded in a high-contrast material system and is therefore currently a topic of intense research. Fabrication processes employ holographic, optical near-field (phase mask) holography, or electronic beam lithography followed by etching and regrowth, or else direct UV holographic patterning (fiber Bragg gratings), or mechanical reduction by drawing from a preform (photonic crystal fibers).

As sensors, these photon-confined structures transduce changes in the local environment (temperature, stress) into changes in absorption or refractive index and therefore optical response—reflectance or transmittance—at a given wavelength. Optical interrogation of the sensor can be performed using an external light source and photodetector. Spectroscopic analysis is possible, for example with a rapidly swept tunable laser or filter. Resonant enhancement of the optical interaction afforded by high-quality-factor nanophotonic structures improves sensitivity.

In contrast to these photon-confined structures, nanostructures at much smaller length scales (~1–10 nm) have altered electronic states or band structure giving rise to their optoelectronic properties. Exploitation of electron confinement along one dimension (e.g., the growth direction) has led to the quantum-confined Stark effect electroabsorption modulator and the ubiquitous quantum well laser. Semiconductor quantum dots fabricated through self-assembly have are utilized in semiconductor lasers with reduced temperature sensitivity. Future needs here include artificially structured "molecules" whose optoelectronic properties change markedly depending on whether or not they are bound to specific chemical agents in the external environment. Again, when used as sensor, the structure transduces the presence or concentration of a particular species into a change that can be interrogated optically.

One example of an application concept radically enhanced by the convergence of the technology trends discussed above is a tunable laser cavity chemical sensor integrated on a single indium phosphide chip [1]. It uses the heterodyne beat signal of tandem tunable lasers to improve sensitivity. One of two sampled grating distributed Bragg reflector lasers has a bare waveguide core within the optical cavity, leading to evanescent optical interaction with any surrounding fluid in which it is immersed. The second laser is isolated from the outside chemical environment by standard waveguide cladding layers. Changes in the environment cause a relative change in cavity phase and therefore frequency shift between the two laser outputs, which are combined and sensed as a beat signal by an on-chip photodetector. A thousandfold increase in sensitivity should be possible by incorporating tagged nanoparticles in the phase shift section of the laser, and an additional hundredfold improvement should be possible with photonic crystal guiding structures to enhance the optical overlap with the environment. Thus, the research outlook for the next 10 years in nanophotonic sensors will emphasize the union of nanostructured materials having high chemical specificity with high-quality-factor photonic crystal structures with enhanced optical interaction, to achieve impressive increases in sensitivity as well as reduction in size and power consumption.

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Nano = 1/Giga, How Will We Design These Systems?

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The continued scaling of silicon technologies as well as the promise of other nanoscale electronic devices leads to the conclusion that we will soon have available systems with billions of devices on a single substrate. In fact, to all intents and purposes, "nanotechnology" is already here.

My thesis is that continued scaling and higher levels of integration will soon be irrelevant since we are already limited by constraints which stem from our current levels of integration. These include, design time, power, signal integrity, signal delays, yield, and fabrication costs. While many of these problems stem from our current "CMOS paradigm," it is not likely that any near-term technology will circumvent the origins of these issues, for two reasons. First, near-term solutions will have to be compatible with CMOS. Second, the problems come from achieving our goal: we have lots of little devices.

This technology accomplishment means we need low-switching-energy devices, both for scale and to keep the system from self-destructing. Low switching energy, however, means we have signal integrity and delay issues at room temperatures. Small devices mean lower yields and higher

fabrication costs. Of course all of these problems are being attacked by the semiconductor industry, see, for example, the ITRS Roadmap [1].

However, the one problem which is not simply technological is the design productivity gap: the number of available devices grows faster than the ability to meaningfully design them. This occurs for two reasons. First, at these scales, the technology is more difficult to simulate, synthesize, optimize, and verify. Second, the number of devices in a design is huge. Current design tools are based on simulation and synthesis algorithms (which take polynomial time), and on optimization and verification algorithms (which take exponential time in the number of devices).

The ITRS has repeatedly documented the above-mentioned (see Figure A.3). Yet, investment in process technology has by far dominated investment in design technology. "Today, many design technology gaps [at companies] are crises." [1] Along with funding for research in new technologies, we clearly also need funding for research for new design paradigms and new design tools.
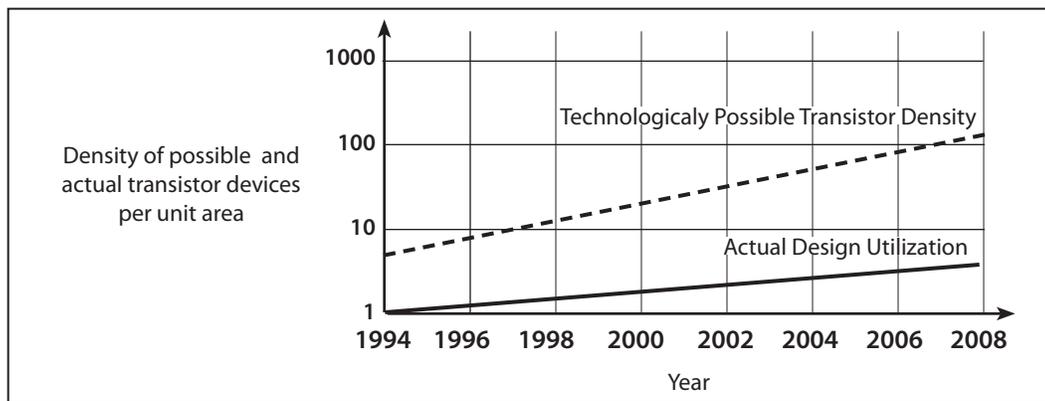
Figure A.3. The growing design productivity gap is the most dangerous problem in integrated system design. The gap is between the technologically possible circuit design density and the significantly lower actual design utilization (growing at the different rates of 58% and 21%, respectively).

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The CMOL Concept

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Ultradense integrated circuits with sub-10-nm features would provide enormous benefits for all information technologies, including computing, networking, and signal processing [1]. However, recent research results [2] indicate that the current VLSI paradigm based on CMOS technology and digital number crunching can be hardly extended into this region. Indeed, below 10 nm gate length the sensitivity of parameters of semiconductor field effect transistors to inevitable fabrication spreads grows exponentially. This sensitivity may send the fabrication facilities costs (extremely high even now) skyrocketing, and lead to the end of the CMOS Moore's Law sometime during the next decade. The main alternative nanodevice concept, single-electronics [2, 3], offers some potential advantages over CMOS; in particular, it allows a broader choice of possible materials. However, the critical dimension of single-electron devices for room temperature operation (the island size) should be below ~1 nm, far too small for currently used (and even forthcoming) lithographic techniques. This

impending crisis may be avoided by a radical paradigm shift from purely CMOS technology to hybrid *CMOL* circuits [2]. These would combine an advanced CMOS subsystem fabricated by the usual lithographic patterning, a few layers of parallel nanowires formed, e.g., by nanoimprinting, and finally a level of molecular devices that would self-assemble on the nanowires from solution. The CMOL concept enables a combination of the advantages of its components (e.g., reliability of MOSFET transistors and minuscule footprint of molecular devices), as well as those of patterning techniques: the fine layer alignment of the usual lithography and the potentially low cost of nanoimprinting and chemically directed self-assembly. This combination may allow CMOL circuits to reach an unparalleled potential density (up to 10^{12} functions per cm^2) and ultrahigh rate of information processing (up to 10^{20} operations per second per cm^2), at acceptable power dissipation (below 100 W/cm^2). The most immediate applications of CMOL technology, which may provide the initial "market pull" for its development, are embedded terabit-scale memories and standalone memory chips. There are also very interesting prospects [4, 5] for the development of mixed signal neuromorphic CMOL circuits for advanced information processing. The recent spectacular breakthroughs in molecular electronics (see, e.g., Ref. 6) give every hope that the transfer of electronic industry from CMOS to CMOL technology may happen as soon as in the next 10 to 20 years.

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Commercially Viable Processes

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Continued device miniaturization is leading us into the realm of nanoelectronics, where nanoscale structural units are set to perform the functions of computer, laser, data storage, sensor, and satellite communication. A prerequisite condition for the realization of nanoelectronics is to achieve controlled fabrication of nanoscale structural assemblies with a commercially viable process. Recently, many resources and much effort have been devoted to nanofabrication research. A host of new approaches, such as nanopatterning and self-assembly/self-organization, have been proposed. The incentive for new approaches is the fact that current silicon processing technology using photolithography will not be able to continue down to the nanometer scale. On the other hand, however, because of its technology maturity and economic value, silicon technology is unlikely to go away but will instead remain as the backbone of electronics industry. Therefore, one viable route toward nanoelectronics is by integration of new approaches of nanofabrication with the existing silicon processing technology.

Nanoelectronics of the future will demand the creation of large arrays of nanostructures with uniform size, shape, and spacing, because properties of nanostructures (unlike their bulk counterparts) display

a strong size and shape dependence. One "natural" approach to the creation of such arrays is by self-assembly and self-organization of low-dimensional nanostructures—e.g., quantum dots (QDs)—in heteroepitaxial growth of semiconductor thin films. However, most self-assembled nanostructures are created by molecular-beam epitaxy in the laboratory, while silicon wafers are processed by chemical vapor deposition in industrial factories. Although self-assembled nanostructures like QDs may exhibit good size uniformity, they are often not uniform enough for real applications and they usually have poor spatial ordering. One way to further improve their uniformity is by self-assembly on nanopatterned substrates [1]. But nanopatterning is a difficult and time consuming process, which negates many of the advantages of self-assembly. Future effort is needed not only to improve the nanostructure uniformity but also to integrate self-assembly with industrial process. For example, a recent study [2] has hinted at the feasibility of integrating nanoscale assembly with conventional silicon processing, which shows the directed QD self-assembly on patterned silicon surfaces prepared by simple photolithography. The excellent QD ordering is achieved via a new concept of guiding QDs on a curved surface by a local-strain-mediated control of surface chemical potential [2].

Besides thin films, other forms of self-assembled nanostructures, in particular molecule assemblies and carbon nanotubes, have been studied as potential functional units for nanoelectronics. They display some extraordinary properties which are very attractive, such as the electromechanical properties of carbon nanotubes [3]. But we doubt that they can replace many device applications based on silicon technology. Instead, they are more likely to be used for certain applications attuned with their special properties. Many of them may also require integration with silicon technology. Apparently, integration of these "exotic" nanostructured assemblies with silicon processing technology poses more challenges.

Nanoelectronics also requires integration of different nanoscale structural components into a device unit at the system level. Application of nanostructures in future devices, therefore, requires a fundamental understanding of *not only* the properties of nanostructures themselves *but also* their interactions with their surroundings, especially when the surrounding structures are also reduced to nanometer scale. Most studies until now, however, have focused only on the properties of nanostructures themselves. One outstanding question that needs to be answered in the near future is how the properties of nanostructures will change when they are integrated together. For example, a novel nanomechanical behavior of silicon film has been observed during growth of germanium quantum dots on a silicon-on-insulator (SOI) substrate when the silicon layer is thinned down to nanometer thickness [4, 5]. The stressful germanium QDs reshape the silicon nanofilm in a dramatic fashion, inducing a large and localized bending of the silicon film underneath the germanium QDs. Simulations [5] show that a transition from the normal extended thin film bending to such unusual localized bending occurs when local stress is applied to a film whose thickness is reduced to a few nanometers. Such a "nanoscale" mechanical transition is expected to occur generally in any solid thin film. It has significant implications on the use of SOI in semiconductor industry, because the localized stress in SOI becomes an increasingly significant issue as the device size shrinks toward the nanoscale. In fact, we may expect mechanical instability at the nanometer scale to pose serious challenges for system-level integration of nanoscale device components, because the typical characteristic length scale of elastic interaction happens to fall exactly into the nanometer range.

While we face many challenges for the integration of nanoscale structural assemblies into a real nanoelectronics device, we are also presented with many opportunities. For example, by combining the self-assembled QD growth with conventional silicon photolithography patterning, we may control

the spatial arrangement of QDs as well as improve their size uniformity. Self-assembled germanium QDs on ultrathin SOI substrates have been proposed as a *nanostressor* [5]. It might be used as a unique method for electron band engineering at the nanometer scale, as the resulting germanium QDs as well as the bent silicon layers are expected to have unique and unusual electronic, electrical and optical properties. For example, it provides a possibility to make a QD lattice with one single material of silicon, as the silicon bandgap modulates from the normal and stressed regions, while conventional QD lattices require/ one material embedded in another of different bandgap.

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Challenges for Modeling, Simulation, and Design

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The goal of the National Nanotechnology Initiative is to enable the design and manufacture of new materials, devices, and even systems atom by atom. The hope is that by learning to engineer at the length scale where nature operates, materials, devices, and systems with fundamentally new capabilities will emerge. Modeling, simulation, and design will be keys to realizing this grand challenge. My talk will review where materials, device, circuit, and system design now stand and the new challenges that must be addressed in order to contribute to success in nanotechnology. I'll argue that theory, modeling, and simulation should be an integral, not separate, part of nanoscience and technology. We must first understand materials and structures at the molecular level; theory and simulation must work alongside experiment in discovering that new science. We must be able to measure what we've built, and computation will become an integral part of new techniques for metrology. We must also learn new ways to assemble and manufacture devices at the nanoscale, and simulations can play an important role in understanding and exploring new approaches. As the science progresses and we learn to design new materials and devices at the molecular scale, a new generation of CAD tools becomes necessary. Finally, these new materials and devices will enable fundamentally new systems and require a fresh look at how we understand and design complex systems. The key messages that I want to convey in this talk are: (1) advances in theory, modeling, and design will be critical to success in nanoscience and nanotechnology, (2) grand challenges are easier to state than to achieve; we don't need a roadmap, but we do need a game plan for making progress on ambitious goals, (3) the research enterprise includes research in academic institutions, government laboratories, and R&D in industry; each has an important and somewhat different role

to play, and (4) education will be critical. When engineers are as comfortable thinking and working at the molecular scale as they now are at the continuum level, nanotechnology will have arrived.

Biomimetic Integrated Nanoelectronic Systems

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The transistor paradigm of the past 60 years, implemented in silicon technology, has seen the gate/channel length headed towards sub 50 nm with concomitant increase in density and speed, but with accompanying challenges in power consumption/dissipation. Perhaps gate lengths down to sub 20 nm would be economically viable. But even so, this push continues to derive from the need to deal with massively compute-intensive problems on rapid human time scales (say fractions of a second to minutes).

By contrast, a variety of warfighter and civilian home security needs arise not necessarily from situations demanding massive computations at ultrahigh speeds, but rather sensing entities/agents at the earliest possible stages of proliferation in environments ranging from air, to water, to soil, to animal and human bodies. Now the need for "nano" may not arise for the same reasons as conventional information processing. Rather, now, "nano" may be central for reasons such as the surface area to volume gain as one core factor in early detection of the "entity" of interest, from chemical toxins and explosives to biochemical and biological agents. And "electronics" (in the sense of participation of a minimal number of electrons, in sensing, transducing, and amplifying the detected information) may be of prime importance owing to the ultraweak detection signals, the need for use of minimal power per unit, and correspondingly minimal heat generation per operation. Additionally, and perhaps singularly, the need for compatibility with "hostile" environments may be of paramount consideration. Mostly, the need for dealing with a combination of the above-noted elements in various classes of situations or problems, faced both on the battlefield and at home, argues that the current paradigms of nanoelectronics R&D (derived as they are from traditional applications perspectives limited to computing and communication in normal environments) simply fail to cover an equally important and rapidly growing need of American and human society: use of electronics in general, but the need for nanoelectronics in particular, when operating in hostile environments that include air, soil, solution, and physiological. There is thus a critical need for major R&D investment in identifying and addressing the fundamental issues whose resolution will enable realization of nanoelectronic systems that operate reliably and efficiently in such environments. The generic science and engineering problems to be addressed, some noted below, fall indeed in a category worthy of being classified as a grand challenge over the next decade.

To enable the use of nanoelectronics in hostile environments is not simply a matter of developing suitable protective coatings, packaging, etc., and hence merely of rendering conventional materials compatible with the environment (such as physiological in the context of implanted "chips"). It is that, and more. Much more. Indeed, the very paradigm of the materials in which we carry out the "electronics" may, in certain environments, preclude inorganic semiconductor-based systems and instead require that polymeric or even biochemical polymer-based systems be examined. Understandably, massive investments in mature technologies such as silicon will not, and should not, give way to "maybe"s. But the potential of nanoelectronics applications in these emerging need areas does argue strongly in favor of investing meaningful R&D dollars in biomimetic integrated nanoelectronic systems, even if the implementation of the electronics occurs within the inner sanctums of silicon, silicon dioxide, and the like. Biomimetic integrated nanoelectronic systems, at the minimum, thus involves hybrid inorganic/polymeric/biopolymeric materials integration in an

attempt to realize nanoelectronic devices/systems that provide the desired functionality and involve mimicking nature either in a bioinspired synthesis process or function or both. Stated simply, few electron effects in new materials (particularly biochemical), assembly of hybrid nanostructures, and even new paradigms of information transfer not based on the transistor, should be investigated with some depth and longevity. Many of the biomimetic and integrative aspects of such investigations are equally relevant to nanophotonics and nanomagnetics.

Visual Computing by Mesoscopic and Nanoscale Systems

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Conventional shrinking methods to improve CMOS VLSI chip performance through dense packing of circuit elements and scaling of device and interconnect geometries in all three dimensions will presumably continue for a few more years, until the channel length of transistors approaches 50 nm or so, thus encountering the ultimate "CMOS brick wall." During the *postshrinking VLSI era*, a slew of nascent nanoelectronic technologies such as quantum barrier devices, single electron transistors, self-assembled arrays of quantum dots, molecular electronics, etc., are likely to emerge as viable candidates for extending the frontiers of the commercial VLSI chip industry. However, conventional CMOS circuit techniques, design optimization tools, and SPICE-type circuit simulation are found to be grossly inadequate for these revolutionary nanotechnologies. The objective of this talk is to introduce *next generation* innovative nanocircuits and nanoarchitectures that can perform image processing and visual computing at least two orders of magnitude faster than conventional CMOS high performance microprocessors. The talk will also discuss a suite of novel CAD tools for emerging quantum and nanoelectronic technologies.

Quantum tunneling in nanometric devices augurs a revolutionary shift of paradigm for circuit and CAD tools design, which must account for quantum effects as well as local interactions between uniform circuit elements. These circuit elements may consist of a coterie of self-organized quantum dots, an assortment of interband resonant tunneling diodes, intraband resonant tunneling diodes, and resonant tunneling transistors, or just ultralow power Coulomb barrier devices such as single electron transistors. Whereas current CMOS VLSI research primarily targets improved circuit speed and low power design through conventional tweaking methods, we have introduced (1) revolutionary circuit topologies, (2) a suite of nanoCAD simulation and circuit optimization tools, and (3) new circuit theoretic models for understanding the behavior of nanocircuits.

In this talk, we will introduce mesoscopic systems with quantum tunneling devices in order to implement nonlinear cell functions in a cellular neural/nonlinear network (CNN), which is now widely recognized as an ideal information processing model of computation for emerging self-assembled nanoelectronic and regular-structured mesoscopic systems. We will discuss the implementation of RTD-based 12 x 12 and 128 x 128 arrays to perform image algorithms such as edge detection, hole filling, noise removal, etc. The resulting RTD-based CNN can be implemented by both silicon and compound semiconductors and will perform at Tera analog operations per second rate.

Also, we will discuss nanoscale 0-dimensional RTDs confined in quantum dots, which can be self-assembled as hexagonal honeycomb nanoclusters where each quantum dot is of 5 nm or less diameter. We will demonstrate how quantum dots can be configured to perform several Boolean functions such as AND/OR/XOR gates, half-adders, 2-level logic networks, etc. We will also discuss how quantum dots can be connected through resistive and capacitive interconnect structures to perform various image processing algorithms such as edge detection, horizontal or vertical line detection, etc.

The operating principle of such nanoscale quantum dot arrays will be significantly different from mesoscopic RTD-based CNN processors.

We will also discuss the design principles for nanoCAD tools for simulation of quantum and nanoelectronic circuits. We will specifically discuss a quantum electronic circuit design optimization environment that we have utilized to synergistically optimize quantum circuits and mesoscopic structures in quantum devices. Together with an augmented quantum SPICE simulator, this allows us to accurately compute electrical parameters such as power, speed, noise margin, etc., for an entire mesoscopic system. We will also briefly discuss the design of a 3D-scattering-matrix-based device simulator to estimate tunneling current in a pyramid-shaped quantum dot. To solve the 3D time independent Schrödinger equation, a 2D Schrödinger equation with the Dirichlet boundary conditions is first solved, yielding a set of 2D lateral eigenstates and wave functions. The 1D Schrödinger equation is solved numerically with scattering boundary conditions on the wave functions, and the total transfer matrix is calculated by multiplication of the transfer matrix for each segment of the structure.

Interconnects for Nanoelectronics: Meeting Industry's Criteria

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The push to develop nanoelectronics has led to the proposal of a variety of interconnect technologies ranging from nanowires to optical interconnects. On paper, or as one-up concept devices, these proposals sound feasible. However, what will the tooling, or processing requirements, be to integrate these technologies? This is not a trivial issue that can be waived aside as something that will need to be solved down the road. The reason is the following: the cost of constructing the next generation of fab is estimated to be in the billions of dollars. Consequently, the commercial sector will not be satisfied with science fiction.

In addition to the issue of building the next generation of fab facilities, there is the issue of compatibility with silicon. The industry is so entrenched in silicon-based technology that the next generation of nanointerconnects must be compatible with silicon processing. Silicon is so well understood that it is senseless to abandon it for new, less controllable, materials. If a nanoscale interconnect technology is incompatible with silicon it will not be accepted by the commercial sector.

The next issue is process yield. In order for an interconnect process to be considered suitable from the standpoint of yield, it essentially needs to be reproducible a million times or more on a single wafer, every day, seven days a week, fifty-two weeks a year. If the yields are too low, driving the cost of a chip up, then the process is not cost effective and the jump to the next generation of nanoscale interconnects will be moot. As an example, let's consider free standing nanowires as interconnects. Assuming they have sufficient conductivity, how does one go about ordering millions of nanowires into an array? Functionalization of their ends has been proposed, but will the contact resistance be too high? Will we end up with Schottky contacts, as opposed to ohmic contacts? Contact resistances must be low and Ohmic contacts are a must. In the field of molecular electronics it has been proposed that you build it, and based on the random interconnect configuration, what you get is what you get. This could be a one transistor device or a one million transistor device. Once again, this is impractical from a manufacturing standpoint.

The last issue is reliability. Whatever technology is employed for producing nanoscale interconnects, it must be reliable. If reliability is not maintained market share will be lost. If you recall the automotive

industry in the mid to late 1970s, in particular the Big Three (General Motors, Ford, and Chrysler), during this decade the quality of cars coming out of Detroit was at an all-time low. The Big Three didn't think this would be a problem, yet it was. The poor performance of the cars opened the door for foreign automakers, in particular, the Japanese automakers. The Big Three's image is still haunted by the poor quality of that period. In the highly competitive microelectronics industry where the profit margin is narrow, reliability is a key factor in the identification of the nanoscale interconnect technology of the future.

The point of the above discussion is not to say that nanoscale interconnects are unrealistic, but to bring to the attention of researchers the ancillary issues associated with the development of nanoscale interconnects. The ideal solution to this problem would appear to be the integration of photonics and electronics, which is currently a hot topic of research in the scientific community. However, the major drawback to the development of such a hybrid device is that lithography is still the primary tool in the fabrication process. Can we walk away from lithography as a tool in the manufacturing of nanoscale interconnects? In my opinion, the answer is no. Consequently, efforts will need to continue in the area of lithography development. What about x-ray lithography? The scientific community has been working on x-ray lithography for well over 25 years with limited success. With this in mind, is x-ray lithography from an industrial standpoint feasible? Will x-ray synchrotron sources become part of the apparatus of the fabrication facilities in the next 10–20 years? Regardless of the answers, the development of new lithographic techniques is in order. While it would be desirable to move away from lithography, it is unclear if self-assembly of nanomaterials is a feasible alternative. The challenge of the next 10-20 years is the development of nonlithographic techniques for making interconnects, but with equal reliability. Both approaches—new lithographies and alternatives to lithography—need to be pursued in parallel.

Potential and Challenges for Nanotechnology-Based Sensing

Scott A. Meller, Luna Innovations

Nanotechnology will most certainly provide revolutionary changes in the sensing community. This new realm of operation in the 1–100 nm regime, in which bulk material properties are no longer valid, is ripe with new opportunities. Of particular note is the field of chemical and biological sensors for the defense industry, which is in need of revolutionary improvements in speed, specificity, and portability.

In order for these new sensing schemes to become a reality, several challenges in the industry must be overcome. Lack of nanotechnology manufacturing and analysis equipment is one roadblock to innovation. Initiatives such as the National Nanofabrication Users Network/National Nanotechnology Infrastructure Network should be promoted and continued. One of the leading roadblocks to research in the nanotechnology field is access to capital equipment required to manufacture, test, and analyze nanodevices. In particular, small businesses do not have the capital available to invest in the advanced tools required in this field. As manufacturing methods mature, access to prototype nanomanufacturing builds should be made available via collaborations similar to the MEMS Exchange that is found today for the MEMS industry. Open access to these tools will promote innovation across the country and accelerate new ideas and approaches, bringing nanotechnology to reality at a faster pace.

Sensing based on nanotechnology approaches faces many real market challenges. Cost is paramount in any successful sensor technology. Adequate high-yield processes need to be in place to realize volume manufacturing for sensors to meet the typical cost point found in the industry. Although

transducing will occur on the nanoscale, the signal must still be converted up to the macroscale and read through a typical analog or digital signal protocol. Review of the MEMs industry history will reveal that although sensor designs were successfully demonstrated early in the lab, efficient and effective packaging of the device was the main roadblock to volume manufacturing. Interfacing and packaging of nanosensors to the "bulk" world needs attention and should be pursued in parallel with sensor designs.

The nanotechnology field needs a supply of skilled researchers. Nanotechnology is multidisciplinary in nature, often requiring skills in chemistry, mechanical and electrical engineering, biology, and physics. Multidisciplinary nanotechnology-based curriculums in U.S. universities must be created and sustained if the nation hopes to remain a leader in this field.

Lastly, the nanotechnology community as a whole has a reputation that must be maintained in order to allow adoption on a wider scale. Researchers must maintain integrity and quality in their work, striving for the truth and not compromising the experimental process over business pursuits. Overselling a technology before it is mature has long-term effects on an industry that can be hard to overcome.

Nanofabricated, Macrostructured, Distributed Photonic Circuits for Chip-Scale Optical Signal Transport, Processing, and Spectral Filtering

Thomas W. Mossberg, LightSmyth Technologies, Inc.

It is natural to model photonic circuits after their eminently successful electronic cousins, wherein signals are routed from active element to active element by wire-like channel waveguides. While effective after a fashion, such an approach does not exploit the intrinsically more flexible nature of optical signal transport and processing. Optical signals, in linear media, are perfectly happy to flow through one another without interacting or interfering. Their ability to do so derives from fundamental differences between photon-mediated and electron-mediated signal transport. The absence of photonic charge provides for noninteraction as well as the perhaps more widely appreciated absence of primary radiation-based loss.

Wire-analog (i.e., channel-waveguide-based) photonic circuits do not effectively utilize photonic noninteraction. In order to do so, it is necessary to develop new routing and control devices having the ability to support overlapping, intersecting, truly photonic circuit topologies wherein the bending radii and intersection problems important in channel-waveguide-based photonic circuits become irrelevant.

The principles of such truly photonic signal control devices have been in hand for decades in the form of volume holography. Volume holograms are structures extended in two or three dimensions whose interaction with optical signal modes is constrained by generalized Bragg scattering conditions. Volume holograms can be designed to couple two specific optical signal modes that are defined in terms of their wavelength and detailed wavefront properties (including direction and curvature). One can envision a planar waveguide optical signal transport layer wherein signals simply flow unconstrained within the slab waveguide (like freespace beams overlapping and intersecting) yet with each signal precisely and specifically guided by distributed mode-specific holographic structures along desired routes between active devices. Extension to multiple transport layers, perhaps interspaced with electronic processing layers, is possible and will be exciting to explore as the modes coupled by distributed, lithographically scribed, diffractive structures may reside in adjacent planes.

What has not been available for decades is the means to create the general holographic signal control structures necessary to realize the scenarios just described. Holography of the past has typically utilized optical interferometric exposure to create distributed diffractive structures. Such a process is intrinsically difficult owing to the need for: interferometric stability during recording; circuit-compatible, robust, photosensitive recording materials; and (most importantly) optical writing beams having the precise properties of the signal beams to be controlled.

Ongoing developments in nanofabrication have opened the door to revolutionary new holographic building block circuit elements for truly photonic-style circuits where signal localization during on-chip transport becomes a thing of the past. Holographic circuit elements may technically be regarded as mode-specific photonic bandgap structures. Since they control the properties of specific signal modes only, they do not require the high refractive index contrast (and hence high out-of-plane losses) characteristic of all-mode photonic bandgap devices.

Nanofabrication is crucial to the realization of distributed photonic circuits since typical features in silicon distributed photonic circuits, for example, will have linear dimensions of approximately 100 nm and positioning control at the level of 10 nm. The nanoscale is not the only scale important in distributed photonic circuits. Building block distributed structures require spatial coherence over macroscopic (micrometer to millimeter) scales. Such resolution and coherence requirements are now or will soon reach compatibility with current state-of-the-art photolithographic fabrication and nanoprinting technologies. While electron beams have been capable of producing such structures for some time, their low writing speeds and limited working fields prevent heavy commercial interest in or widespread application of devices requiring their use.

The use of nanofabrication (in the form of photolithography or nanoimprinting) to create holographic photonic circuit elements makes it possible to computer-generate signal fields that never exist prior to device fabrication. Many coactive planar holographic structures may be overlayed while retaining full compatibility with simple binary-level etching and stamping processes through judicious sampling of computer-generated structures. Another advantage of distributed diffractive signal control structures is their relative immunity to point fabrication defects, which often limit yield in other system architectures. While computer-generated holographic structures have been utilized in the past, fabrication limitations have prevented their application to in-plane scenarios (which require the nanoscale features mentioned above).

Nanofabrication capability has crossed a threshold. New and uniquely photonic circuit concepts can now be developed and implemented. Planar holographic structures provide wavefront-specific signal control allowing for the free overlap and intersection of multiple signal streams, thereby removing bending radii and channel waveguide intersection constraints. They also provide wavelength-specific signal control enabling powerful, on-chip, spectral filtering capability useful in laser source locking, multiplexing, and correlation-based signal analysis. Planar holographic structures are mode-specific photonic bandgap structures whose low index contrast and concomitant low loss provides useful application. The growing availability of powerful nanofabrication methods enables a new photonic technology wherein distributed diffractive (holographic) structures, computer generated and tool written, provide multiple previously inaccessible functions. The field is rich in opportunity for innovation and impact on practical photonic and electrophotonic circuits.

Nanoscale Optical Technology for Advanced Data Interconnections

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As integrated circuit chips and electronic packaging becomes denser in functional elements and higher in operating speeds, optical interconnects are becoming increasingly more useful, and are now considered essential for future electronic systems. The advances in this area are best seen in two categories: evolutionary advances and revolutionary (or leapfrogging) discoveries. These are separate tracks entirely although one may drive the other. In my talk I will present several key areas in which important evolutionary advances in nanooptical technology will make a difference for optical interconnects. These include breakthroughs in nanoscale silicon-on-insulator photonics elements, continued advances in VCSEL technology (including passive mode-locking technology), the growth of CAD tools for rapid nanooptical design, and, finally, new approaches in packaging. Full realization of these advances awaits breakthroughs, but we can see the form of the change in today's research. In the case of revolutionary advances we can only dimly see the possibilities. Each of these new advances in nanoscience stems from unexpected breakthroughs in either materials, devices, or systems architecture. One example yielding intriguing results is the use of metal-based optics, which relies on the use of plasmonic excitation that couples to either light or electrons and has intriguing dielectric properties. Another is harnessing the advances in nanotubes of functional oxides and semiconductors to make ultrasmall lasers and optical cavities, including devices operating at short wavelengths.

Scanning Probes are Indispensable to Nanotechnology

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Scanning probe methodologies are indispensable to the field of nanotechnology due to their capability to image the nanoscale arrangement and properties of materials. Scanning probe microscopy is not a fully explored research area; rather, *new probes and techniques continue to be developed at a rapid pace, each yielding new insights in nanoscale phenomena*. Broadly speaking, the ultimate goal is to achieve atomic scale imaging of the arrangement of atoms, simultaneously with determining local electronic, magnetic, chemical, and mechanical properties, all in three dimensions. The quest toward this goal continues.

Consider some of the achievements. Scanning tunneling microscopy (STM) and force microscopy (AFM) have delivered atomic resolution images of surfaces. STM with ferromagnetic tips, a very slight modification to the original tunneling microscopy, has allowed for magnetic contrast, and detection of spins in paramagnets. Magnetic force microscopy has allowed for 10 nm resolution of magnetic fields. And magnetic resonance force microscopy (MRFM), has enabled detection of nuclear and electronic resonance in materials. The resonance is chemically specific, and MRFM also allows 3D imaging [1, 2]. The MRFM experiment relies on making extremely compliant probes, but is otherwise similar to conventional AFM. Nearfield scanning optical microscopy (NSOM) can achieve resolutions in the 10 nm range, with a wide variety of NSOM probes optimized for different experiments. NSOM can in principal be made to operate with any optical spectroscopic technique, thus yielding a plethora of contrast mechanisms at the nanoscale. These already include infrared, Raman, photoluminescence, and modulation spectroscopies [3–5]. High frequency probes can have highly localized sensing capabilities, while allowing entirely electronic interfaces to the scanned probe [6–8]. These probes also allow a wide range of dielectric and magnetic contrast mechanisms at the nanoscale, including magnetic resonance. Further development of scanned probes is beneficial to

nanotechnology, yielding new contrast mechanisms and higher resolution, and is inevitable as long as promising new ideas continue to emerge.

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Semiconductor Nanophotonic Devices for Optical Transmission

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Semiconductor photonic devices play a crucial role in existing fiber-optic communication systems, as sources and detectors of optical transmission signals. Many of these existing devices already incorporate practical nanophotonic technology, utilizing nanometer-scale structures that affect the properties of both electrons and photons. Multi-quantum-well (MQW) lasers confine electronic carriers in semiconductor layers only a few nanometers in thickness, enhancing device performance. Distributed feedback and distributed Bragg reflector lasers utilize built-in gratings with a pitch of a few 100s of nanometers to define the spectral characteristics of the device. As the capability to define nanometer-scale features in semiconductor materials becomes increasingly more flexible, the performance and functionality of photonic devices will be significantly enhanced. Technology trends and important areas for future research are indicated below:

- Additional degrees of quantum confinement can be achieved with quantum wire and quantum dot lasers. This will lead to lasers with lower threshold current, lower ambient temperature dependence, higher bandwidth, and narrower linewidth. Technology to grow these devices epitaxially requires significant investment.

- Improved gain-bandwidth avalanche photodiodes can be built with nanostructure layers. Single-photon-counting avalanche photodiodes with the higher efficiency needed for quantum

cryptography can also be achieved. Epitaxial growth technology is currently also a limiting factor for these devices.

- Low-loss waveguides defined by photonic crystals will find application in photonic integrated circuits. Many other functional elements are required for high-density photonic integration, such as optical delays and optical isolators. Large-scale photonic integration with many diverse elements is a key challenging task for a nanophotonic program.

- High-performance semiconductor gratings, dynamically programmable to transmit or reflect certain wavelength ranges, can be accomplished by appropriate refractive index profile tailoring. Such gratings could be a building block for improved tunable lasers, reconfigurable optical add-drop multiplexers, and many other applications.

Processing of Array Signal Flow in Nanosystems: Unconventional Devices and Non-Boolean WAVE Logic

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Unlike in the mainstream digital computing paradigm where discrete/binary values prevail, in many nanoscale chips (including below-100-nm CMOS devices as well as optical array computers) the incoming data, through the integrated sensor arrays, are image flows generated by radiation or distributed forces (e.g., tactile). The output might be a global detection of a target and its x-y-z coordinates or just the detection of a well-defined event, the presence of a target in a finite time interval. Hence, we are looking for a spatial-temporal event in a continuous flow of radiation. (For example, we might look for the onset of a predefined lightning shape on the night sky during thunderous weather.)

There is neither need nor time to digitize and/or sample these radiating image flows. The processing of the image flow could be made directly by performing fully parallel wavelike actions in an array-type wave computer. The *formal framework* is defined by a *universal machine on flows* and the *wave-logic* algorithms by *α-recursive functions*. The processing elements act on mixed analog and binary signals, with (mainly but not exclusively) local connections (plus crossbar), their connection strength being plastic. The *transient memory* is fully distributed. This new world of processing is a complete departure from classical number crunching or binary logic. The architecture is "tailor made" for nanotechnology. Interestingly, this is the way and language of (for example) the mammalian retina. Here, the arithmetic depth, a notion introduced by J. von Neumann, is very low. The most difficult task for number crunching computers—the wave action—becomes an elementary instruction, performed by our programmed physics in one single step.

One present-day practical implementation is a CMOS TeraOPs cellular visual microprocessor. Another one is a laptop-sized laser array computer with molecular-level grayscale image memory and programmable semiconductor laser array or acousto-optic modulator. As to the future development, two classes of inquiries will prevail.

What kind of "nano" and molecular devices will be useful and practical in these sensory computers? What will be the easy-to-implement multi-input functional units, the non-transistor-based elementary devices? Or, what are the *nano-friendly* devices and interconnections that are optimally suited to this new computing paradigm? What are the convenient computing architectures? What if the input flow is really continuous in time, like in the retina, with no snapshots? We do not want to force a preconceived architecture; on the contrary, we start from nano-friendly units and interconnections (not forgetting the microelectromechanical and nanoelectromechanical systems, as well as the integration of activation

and communication). The resulting nanosystem will then be symbiotic with the environment via sensing, acting, and communication (e.g., using optical RF MEMS transceivers).

Once we have an architecture with a feasible physical implementation, what will be the best and most efficient wave algorithms? What are the complexity and spatial-temporal properties of these algorithms for spatial-temporal logic? This is a non-Boolean logic—what are the necessary skills and tools to develop this new kind of software?

Next, we summarize the tasks to be solved for the two classes of questions we have just posed.

Unconventional Nanodevices for the Universal Machine on Flows

In very deep submicron, two-digit nanometer CMOS technology, the effect of parasitics could be significant. Why not circumvent this problem by using *amoeba-like* multi-leg nonlinear locally active devices to form a cellular wave computer architecture? The characteristics of the devices are inherently coupled to preserve some necessary properties (like local activity or monotonicity, and stored programmability for the whole architecture) but otherwise there will not be any "parasitics." There are no parasitics in a mammalian retina, "it works as it is."

Instead of forcing the implementation of a rigid, strictly Boolean digital circuit and system, let us turn the design strategy upside down. Why do we not start with well-defined successful nano-friendly devices, like the binary-controlled-weight-analog-signal, single-electron-transistor-based units, then start building a complex non-Boolean architecture based on easy to implement physical properties, and finally introduce wave-programmability and plasticity? Analog valued, continuous time and binary signals are the natural signal models in this field.

Much is to be done to make small optical computers operating on image flows, taking advantage of the fully parallel nature of optical lens processing and the speed of light processing of millions of pixels. Molecular 2D holographic transient memories, optical feedback on million pixel flows, and programmable picosecond semiconductor laser arrays will bring unprecedented computing power.

One major challenge to building nanosystems is input and output from the tiny devices. The integration of the MEMS and NEMS in a hybrid nanosystem provides for the inclusion of actuation and communication. For example, by adding optical RF MEMS to a hybrid nanosystem, a self-contained device could serve as a nanosupercomputer, sensing and communicating exclusively via radiation.

Unconventional Wave Algorithms for Nanosystems

Once a stored programmable nanotechnology-friendly sensing-computing non-Boolean architecture is available, the new world of wave algorithms and software technology will start to emerge. Today we see only the tip of the iceberg. Some principles can be taken from neuroscience models of sensory modalities, including retinal, tactile, and auditory processing, as well as some immune system responses. Experimental skills are being developed by many algorithm and software designers, but a firm basis, theoretical models, and standard software tools are yet to be developed. Eventually this will lead to a genuinely different, non-Boolean computer science and software practice. Moreover, the integration of spatial-temporal sensing and communication instructions, as well as embedded semantics, will make the resulting algorithms and software distinct entities in the realm of software technology.

Limits of Miniaturization of Sensors

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The field of nanofabrication, clearly led by the microelectronics revolution over the past 40 to 50 years, has been applied towards the miniaturization of mechanical (MEMS), optical (integrated optoelectronic, plasmonic), magnetic (magnetic storage media), and fluidic (microfluidic) systems. A wide range of materials, from silicone elastomers to epitaxially grown compound semiconductors, has been developed for these purposes. Fabrication methods ranging from replication molding and stamping to high resolution electron beam lithography are needed for the construction of nanostructures in these different fields. Much of this technology has been developed by researchers in the separate disciplines of biology, chemistry, physics, and engineering. Here we discuss the opportunities to combine these efforts and to explore the limits of miniaturization of sensors. These integrated nanosensors will be used for applications ranging from bioassays and disease diagnostics to quantum optics.

In 1965, Gordon Moore predicted the geometric progression with time of the number of electronic devices integrated on a chip, with corresponding reductions in the cost per individual device. Moore's Law has since then correctly predicted the development of electronic circuits with ever-increasing complexity, functionality, and speed. The underpinning for Moore's Law was the development of lithographic fabrication techniques ideally suited for rapid miniaturization of planar structures, along with the careful selection of silicon electronics that lends itself to such miniaturization and integration. Similar opportunities are available for the miniaturization of fluidic, mechanical, and optical devices, which can now be fabricated by lithography rather than by the traditional process of laborious machining and assembly of individual parts. We believe that it is possible to also bring Moore's Law scaling to sensors and to integrate these sensors into interactive arrays through miniaturization.

One of the key components of a sensor system is the delivery and concentration of analyte to the sensor elements. This becomes more challenging as sensors sizes are reduced. Fortunately, lithographically defined nanofluidic systems have recently been developed to manipulate picoliter volumes through valves and pumps and to concentrate, mix, and react small sample volumes. It is also possible to precisely manipulate nanoparticles with magnetic and optical tweezers. Here we propose to apply microfluidic integrated circuits and magnetic manipulators to deliver, analyze, and deliberately react small samples for a better understanding of chemical and biological systems. During the presentation, we will:

- Explore the fundamental limits of miniaturization and integration of chemical, biological, optical, and magnetic sensors on compact and robust platforms.
- Describe nanoscale sample delivery systems that can be used for the concentration, reaction, and analysis of subnanoliter quantities of material and can be fully integrated with microsensors. Rather than developing delivery and sensing devices side by side on a chip, we intend to integrate them intimately to obtain additional synergy and functionality.
- Discuss opportunities for bringing Moore's Law scaling to sensor technologies by combining lithographic and self-assembly methods with tolerant device designs, thus enabling large-scale integration of sensors which can yield complementary information about samples.

With the recent development of microfluidic tools for the manipulation of biological materials in microfluidic chips—with thousands of valves and hundreds of reaction chambers—miniaturization of sensor technology now holds the promise of realizing the "laboratory on a chip" concept. Disease

diagnostics, DNA sequencing, cell sorting, and single molecule sensing can be undertaken in these laboratories. Much the same way as the functioning of an analytical chemistry or biology laboratory requires several instruments (optical spectroscopy, chromatography, and microprobe analysis, for example) to identify unknown samples, we discuss the possibilities of integrating different sensors on the same chip to improve the specificity of the analysis system. As it is often difficult to integrate different systems into compact and miniaturized systems, we believe that it is necessary to capture the opportunities of combining sample delivery techniques with sensor applications, by forming interactive multidisciplinary teams of researchers. For example, by integrating selective surface treatments developed by chemists, new fluorescent molecular tagging techniques developed by biologists, and high-quality-factor mechanical or optical resonators developed by physicists and engineers, it may be possible to accurately identify single molecules. We intend to explore the opportunities for miniaturization of sensors through the integration of nanophotonic, nanoelectronic, nanomagnetic, and nanomechanical devices, with applications in biotechnology and chemical detection. We intend to apply this technology for the manipulation of single cells, imaging of their structure and detection of molecular processes within them. Moreover, we could even deliberately trigger reactions by delivering biofunctionalized material within the cell, performing intracellular *nanosurgery* and imaging with miniature systems that combine mechanical, optical, and magnetic manipulation and imaging techniques.

To date, intriguing discoveries have been made through research towards the development of high resolution sensing and imaging tools. But these advances have for the most part been achieved using relatively large individual instruments. We have only recently begun to embark on the opportunities of integration of sensing technologies at the nanoscale, but typically limit integration to the assembly of large numbers of devices with identical functionality. Here we propose to integrate sensors with different functionality to improve the resolution and selectivity of the identification process. Integrated nanosensors require not only the ability to control and, ultimately, manufacture components with features of molecular dimensions—but also the ability to evaluate sensing information from large assemblages of sensors. We propose that nanotechnology can be applied for the miniaturization and integration of sensors with the purpose of measuring and manipulating samples at the nanoscale, such as:

- Massive integration of biologically and chemically functionalized resistors and optical resonators for chip-based electronic (resistive) or optical (refractive index) detection of chemicals
- Highly integrated optical spectroscopy systems integrated with chemical and biological functionalization tools for specific analysis of femtoliter volumes
- Manipulation of magnetic nanoparticles for intracellular nanosurgery to deliberately trigger cell responses
- High-resolution magnetic resonance imaging and spin detection through fabrication of nanomagnets, nanocantilevers, and nanocoils
- Mass spectroscopy and nanomechanical detection of pressure and flow using MEMS devices
- Biological and chemical analysis using optical interrogation of engineered molecules with quantum dots, plasmonic nanoparticles, and fluorophores
- Ultrasensitive atom/molecule detection with high-Q optical nanocavities for environmental monitoring

From these examples, it becomes readily apparent that integrated sensor systems spanning such hierarchies are realizable only through innovative, crossdisciplinary approaches and through the development of nontraditional research. For all of the examples listed above, the nanoscale

subcomponents possess some critical function or characteristic that is attainable only through miniaturization.

There have been many driving forces to exploit the potential benefits of miniaturized apparatus relative to systems of conventional size, including reduced consumption of samples and reagents, shorter analysis times, greater sensitivity, portability that allows *in situ* and real-time analysis, and disposability. A unifying vision for the field has been the notion that, in the same way that integrated circuits use miniaturized transistors to automate computation, microfluidic chips could accomplish large-scale automation of biological processing using nanoliter volumes. Although the first microfabricated, miniaturized gas chromatograph was described in 1975, the introduction of miniaturized formats for analytical chemistry and biology using liquids in microfabricated chips did not begin in earnest until the early 1990s. The past decade was a period of furious technological development, and many individual microfluidic components with the ability to perform biological manipulations on nanoliter volumes were demonstrated. However, the actual impact of microfluidics on the life sciences and biotechnology thus far has been limited—very few academic biology laboratories use microfluidic devices on a routine basis, and when faced with a decision on how to automate, most companies still choose macroscopic robots.

One reason for this disconnect has been the difficulty of making the transition from simple microfluidic components to highly integrated systems. Individual microfluidic components, even if they are capable of analyzing nanoliters of material, are often of little use unless they can be integrated together in a functional system. An exception is when a component takes advantage of novel fluid physics only available at the microscale. There have been several scientific demonstrations that take advantage of these effects and some of them find their way to commercialization. Today, we are seeing the emergence of truly integrated microfluidic systems for biotechnology that operate on nanoliters of material, which can be termed "nanofluidic systems." The main technology platforms for micro- and nanofluidic research are based on microfabrication techniques, such as photolithography, that were originally developed for the semiconductor industry. The initial motivation was the idea that fabrication technologies used for manipulating electrons in ever more complicated ways could also be used to make devices that would manipulate fluids. Common substrates used in these devices are glass and silicon, but such hard materials are not ideally suited for implementing robust liquid control systems such as valves and pumps. Thus, alternative fabrication methods and materials such as soft lithography with silicone rubber became popular, resulting in the emergence of a wide variety of techniques and materials to make fluidic devices. Nevertheless, there are many interesting analogies between integrated nanofluidic system design and the development of integrated circuits, and conceptual comparisons between the two fields remain instructive.

Gradually, it has become apparent that the true potential of microfabricated devices lies in the ability to integrate a complete analysis system "on chip." Such a complete analysis system in a microfabricated device will need to perform more than just separation and detection. This "lab-on-a-chip" will have to integrate functionalities such as sample handling, mixing, incubation, sorting, transportation, recovery, and automation. Due to limitations of capillary electrophoresis, other means for controlling fluid flow within microfabricated devices were studied. Dielectrophoresis and pressure switching were used to create valveless switches for separation of particles and cells within microchannels. Spatially fixed temperature zones were developed that allowed for incubation at various regions in the microchannels. Multiple ports and plugs were used to dispense and dilute reagents for enzymatic reactions. Advances in developing integrated analysis systems have led to the emergence of chips that can perform enzymatic assays, immunoassays, polymerase chain reaction, and cell sorting, However,

realizing the *lab-on-a-chip* vision requires a high degree of integration of these individual elements. A major obstacle hampering progress has been the lack of scalable plumbing. While electrokinetic flow and direct pressure manipulation are suitable for simple devices, they do not scale well to more complicated systems. We have recently solved this problem through the development of active integrated microfluidic valves and pumps using multilayer soft lithography, a new micromachining technique that exploits the elasticity and the surface chemistry of silicone elastomers in order to create monolithic valves within microfluidic devices. A monolithic chip can be made of multiple layers of elastomeric channels, each layer cast from a microfabricated mold. In a typical two layer system, the bottom layer consists of fluidic channels where the sample will be introduced and manipulated, whereas the top layer has control channels by which the valves will be pneumatically actuated. When pressurized air or nitrogen is introduced into a control channel, the thin membrane between the two channels is deflected downward, sealing off the fluidic channel. In this way, a leakproof active valve with moving parts is created. The simplicity and flexibility of multilayer soft lithography allow for a high degree of integration of these plumbing units. Multiplexing schemes have been developed to allow individual addressing of thousands of valves on a chip by relatively few external pressure valves. Quake, Scherer, and collaborators [1, 2] used these valves and pumps to make a variety of chips, including integrated fluorescence-activated cell sorters, rotary pumps, and 12-nanoliter polymerase chain reaction machines.

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Nanoelectronics—Evolutionary

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Grand challenges in nanoelectronics which emerge from the downscaling of electron device technology are well documented in the 2003 International Technology Roadmap for Semiconductors [1]. Power dissipation is one of the key grand challenges facing electronic systems. "Power consumption is perhaps the major engineering concern in the design of mobile wireless devices [2]." Tunneling devices [3, 4] and molecular quantum dot cellular systems [5] offer solutions to the power dissipation challenge. In addition, low-power nanoelectronic technology should enable autonomous vehicles and sensor networks, and enhance the capabilities of radio frequency identification and portable wireless applications.

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Volume Holographic Nonvolatile Memory for Applications to Database Search and Unmanned Aerial Vehicle Navigation

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Optical data storage in volume holograms is quite promising in some ways. For example, using technologies currently at hand, it may be possible to produce a 5 mm thick, CD-sized disk with a storage capacity exceeding 1 terabyte. This corresponds to an areal density of about 1 bit per $30\,nm^2$. However, addressing individual bits in such a storage system is potentially very slow. Furthermore, the materials that offer nonvolatile holographic storage of such a high capacity are typically of the write-once, read-many type. It is questionable whether volume holographic memory (VHM) will be used as a standard digital memory device in the near future, barring significant development in materials and architecture.

However, there are some important, niche applications for which VHM offers unmatched promise, due to the inherent parallelism of optics. One such application is the search of a database containing a large number of images. Recent developments in the so-called super-parallel architecture have opened up the possibility of searching through 10 million images in a few milliseconds. The super-parallel architecture can also be employed to realize a holographic random access memory (HRAM) that may achieve a data retrieval rate exceeding a gigabyte per second. Again, it is unlikely that the high speed of such a data retrieval system will have any immediate impact in conventional computing, given the parallel nature of the data retrieved. However, an HRAM of this type may serve as a data feeder for a translation-invariant correlator (which employs thin holography) in realizing a robust system for landmark-identification-based navigation for an unmanned aerial vehicle, for example. Other applications of super-parallel-architecture-based volume holographic memory include computer vision, face recognition, and automatic target recognition.

Several challenges are slowing down the speed of progress in the area of VHM, including the development of more robust materials; high speed spatial light modulators; and high power, short wavelength diode lasers. Currently, there are a few university laboratories as well as several companies in the United States (Aprilis, InPhase, Call-Recall, Digital Optics Technologies, Laser Photonics Technologies, Displaytech, and Boulder Nonlinear Systems, for example) that are actively pursuing the development of VHM and related technologies. A comprehensive review of VHM can be found in Reference 1, and the latest developments in Reference 2.

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Fabrication and Manufacturing for Nanoelectronics, Nanophotonics, and Nanomagnetics

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With the demise of the industrial research laboratories (e.g., Bell Labs), the tasks of inventing and developing the nanoelectronic, nanophotonic, and nanomagnetic elements of the future will fall upon universities and small companies; the task of manufacturing them will remain with industry. It is therefore important that universities and small companies have the necessary tools, personnel,

and organizational structure. My talk addresses the issue of enabling the research community to realize and test their innovative ideas by fabricating them. Fabrication has always been the pacing element, not the generation of ideas. Optimal development occurs when there is synergy between the generation of ideas and fabrication.

I propose the terminology "nanostructured assembly" to encompass all the many configurations that nanoelectronic, nanophotonic, and nanomagnetic elements of the future might take. An integrated circuit is a nanostructured assembly, as is a chlorophyll-based artificial photon sensor. Materials for future nanostructured assemblies include semiconductors from several columns of the periodic chart, insulators, metals, organic materials, macromolecules, and various nanoparticles.

Focusing on the assembly of materials, the planar fabrication process (i.e., lithography plus pattern transfer) will continue to play the key role. The highly successful use of this process in the semiconductor industry has lulled many into believing that research in nanostructured assemblies will require adopting the tools and methods of that industry. This is a simplistic and seriously misguided view, as I will illustrate with examples. Rather, a wide variety of tools need to be developed that will take us from where we are now to an ability to manipulate and assemble macromolecules and nanoparticles at the 1 nm level.

In 1950, every university researcher in the country had easy access to a fabrication shop (e.g., machine shop, optical and electronic assembly). The nanofabrication shop of the future era, based on planar processing and other elements, must likewise be readily available to university researchers. This will mean that funding agencies must allocate some of their resources to the development of low-cost, highly flexible fabrication tools for nanostructured assemblies, and to making them readily available. At the present time this need is not recognized. I will illustrate with specific examples developments that should be undertaken.

Electronic Applications of Nanomaterials

Eric S. Snow, Naval Research Laboratory

Over the last two decades, the major theme of nanoelectronics research has been the search for a revolutionary device technology that could one day surpass the performance of fully scaled silicon microelectronics. Despite this effort silicon device technology remains clearly superior to any candidate nanoelectronic devices, and it is unlikely that any alternative nanoelectronics technology can provide solutions to the full spectrum of problems currently facing ultrahigh density computing such as interconnect delays, power dissipation, and economic limitations. For this reason I think that nanoscience investment strategies should place a greater emphasis on other areas of electronics that offer a higher probability of success.

Electronic applications of self-assembled nanostructures is one such area of research that I believe has a significant probability of technological payoff within the next 10 years. Various nanomaterials such as carbon nanotubes possess electronic and optical properties that far surpass the performance of currently available materials. Thus, there is a clear incentive to incorporate such nanomaterials into commercial and defense applications.

Researchers in nanoscience have developed self-assembly techniques that can inexpensively produce bulk quantities of various nanomaterials such as carbon nanotubes, semiconductor nanowires, and quantum dots. These self-assembled nanostructures are single crystalline with dimensions as small as 1 nm and often possess unique properties not found in conventional electronic materials. For

example, carbon nanotubes can have a room temperature mobility of ~100,000 cm^2/Vs and, because they are grown from small grains of catalyst, do not require a lattice-matched crystalline substrate. Thus, carbon nanotubes and other semiconducting nanowires can be used as a high mobility semiconductor on polymeric substrates. Because the organic semiconductors that are currently used on such substrates have poor electronic quality, nanomaterials offer the potential for higher performance levels that may greatly expand the range of applications for this type of electronics.

Another unique property of nanomaterials is that they possess a large surface-to-volume ratio, which means that their electronic and optical properties are often strongly affected by the ambient environment. This intrinsically high sensitivity can be used to realize new nanomaterial-based sensors. For example, the electrical resistance of single-walled carbon nanotubes is extremely sensitive to the presence of certain chemical vapors. This feature can be used to construct chemiresistors that can detect extremely small concentrations of certain chemical warfare agents and toxic industrial chemicals.

The above examples illustrate how investments in nanoscience can benefit areas of electronics technology other than traditional ultrahigh density computing. The challenge for establishing a productive investment strategy is to recognize and to support those areas of research where nanotechnology offers truly unique capabilities beyond the current state of the art. In this effort it is critical to distinguish hype, which is all too common in this field, from substance. A failure to do so risks producing nothing more than a series of impressive laboratory demonstrations with no tangible impact on commercial or defense electronics.

All-Optical Signal Processing for Nano-Photonics

Marin Soljačić, Massachusetts Institute of Technology

For a long time, there was a widespread belief in the optics community that all-optical signal processing is not feasible because of the weakness of ultrafast nonlinear effects. The weakness of these effects required making highly undesirable compromises in at least some of the characteristics of any all-optical device: its size, operational power, bandwidth, etc. This view has been changing over the past few years mostly due to the recent theoretical breakthroughs in the new and emerging field of nonlinear photonic crystals (PhCs) [1–4]. PhC-enabled designs seem to offer feasibility of any kind of signal processing, with bandwidths that are very difficult to implement electronically, at only a few milliwatt power levels. Nevertheless, for nanotechnology applications, it would be desirable to improve on performance characteristics of even those devices. PhC microcavities that use electromagnetically induced transparency (EIT) materials [5] as the nonlinear medium might enable all-optical signal processing at single-photon power levels.

There are two most commonly used approaches to enhance nonlinear effects. One is to use a material that has as large a nonlinear response as possible. The other approach involves finding a structure whose geometrical properties optimize nonlinear response.

As far as materials go, EIT materials have by far the strongest nonlinear response in nature; in a recent experiment [6], Hau et al. observed Kerr nonlinearities 12 orders of magnitude larger than in AlGaAs this way, thus making EIT materials the most nonlinear materials in nature.

For the structural enhancement of nonlinearities, PhC microcavities are superior to all other proposed systems. Our group has shown [2–4] how one can design tiny ($O(\lambda^3)$), low operational power (e.g., few tens of mW, which is compatible with single-channel power levels used in telecomm today),

ultrafast (bit rate$>=40$ Gb/s) devices suitable for any kind of all-optical signal processing. These devices can be implemented in common optical materials such as AlGaAs or As_2Se_3. One such system is illustrated in Figure A.4.

One can combine the unparalleled nonlinear properties of EIT materials with the superb opportunities of PhC microcavities for structural enhancement of nonlinear effects, producing an all-optical switch that can be operated at extraordinarily low power levels [7]. One would start with a PhC microcavity similar to the one shown in Figure A.4, and dope it with a single EIT atom. Alternatively, one could use solid state EIT materials [8], or else a single-gas-atom photonic crystal microcavity [9]. The density of one atom per modal volume of a PhC microcavity ($\approx (\lambda/3)^3$) turns out to be roughly the same as the atom density in the EIT experiment from Reference 6, so approximately the same Kerr nonlinearity would apply. Using this fact, our preliminary calculations indicate that one should be able to obtain operational bandwidth of order 1 GHz, while still operating at single-photon power levels [7]. So, the systems of this kind promise to be very natural for exploration of nonlinearities at single-photon power levels as studied by Werner and Imamoglu [10].

Devices that could perform all-optical signal processing at such low power levels could have many important applications in nanotechnology. One of the major problems in nanoelectronics is transfer of information between the nanoelements and our macroscopic world. In a way, photons provide one natural way of doing this: electronic transition inside of an atom (Ängstrom scale) can produce a micrometer-scale photon, so the scale at which information is "stored" is thereby magnified by more than 3 orders of magnitude. Nevertheless, the signals created this way will have very low power levels associated with them. In order to process them, one would need devices that can operate at such low power levels. Furthermore, all-optical signal processing at single-photon power levels could enable all-optical quantum information processing. Photons are a very suitable quantum information medium; because of the weak interactions with the surroundings, their decoherence rates are low. But also because of their weak interactions, it is difficult to perform signal processing on them. Devices that exhibit optical nonlinearities at single-photon power levels could therefore potentially have important applications for all-optical quantum information processing. Of course, an efficient quantum computer would be a very useful tool for simulating nanoelectronic systems in which quantum effects cannot be treated classically.
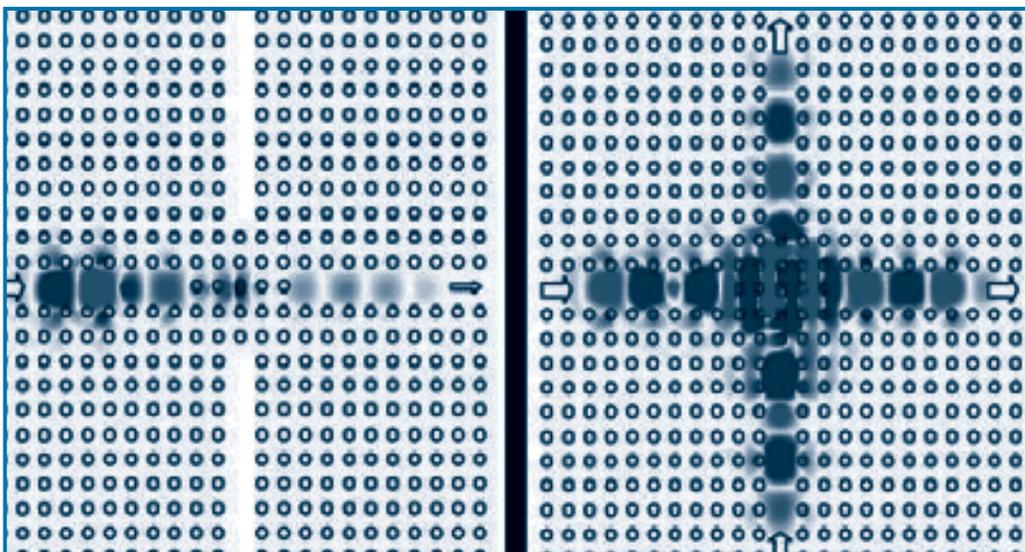

Figure A.4. Photonic crystal microcavity all-optical cross-switch from Ref. 4. The device is designed so that high transmission through the device is triggered only if both signals are present at the same (plot on the right). Thus the device performs the logical *AND* operation.

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Nonvolatile and Volatile Memories at the Nanoscale

Sandip Tiwari, Cornell University

Nearly all integrated forms of memories, volatile or nonvolatile, depend on the use of field effect for reading and access. The ultimate size limit of useful field effect is of the order of 10 nm, essentially the dimensional limit of the field effect transistor. For memories, there is another practical aspect to this limit, the signal strength. This is usually related to how many carriers can be moved per unit time (i.e., the current that is detectable and the speed with which this detection can take place), the ability to distinguish between states of storage (which is related to the detectable signal strength), the multitudes of ways by which errors can be introduced and signal lost, and finally the practicality of integration. Strong statistical control due to collective phenomena has provided the reproducibility at large dimensions, and becomes an issue at the smaller dimensions. Also, if one were to really succeed in building memories at the smallest dimensions, one would then have to find ways by which trillions of them could be packed together without power dissipation and current carrying capabilities becoming an issue. Silicon at the nanoscale does afford a way by which highly integrated memory and logic systems can be built together using novel storage approaches—in nanocrystals, in defects, and where this storage media is placed, while keeping the storage cell as a gain cell. Also, since the transistor is reducible to near 10 nm dimensions, there are approaches based on significant changes in implementation that can address density, reproducibility, and power density. Strong scientific understanding of device phenomena at the nanoscale, new technologies for implementation with reproducibility, and an open-minded approach with long-term perspective are essential in surmounting the barriers that range across the science and engineering disciplines. A general discussion of the emerging directions is included in a number of presentations in References 1 and 2. For single-electron implementations, see Reference 3.

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Nanophotonics, From a Systems Viewpoint

Alan E. Willner, University of Southern California

Nanotechnology holds the promise for producing revolutionary changes in the way we perceive systems, in which certain functions can be significantly enhanced whereas other functions are simply not possible with conventional means. In particular, nanophotonics has a special role to play due to the unique properties of photons as well as the entrenched use of optics for data transmission and storage. Seemingly, the ultimate goal is to develop a functional single-chip system composed of densely integrated nanophotonic components.

Several impressive research results have been reported in nanophotonics. These results tend to be very device oriented, for which simply getting a particular nanophotonic element to function is a significant task. However, few systems level studies have been performed for nanophotonics, leaving many unanswered questions as to the hoped-for migration of devices into systems.

I believe that nanophotonics may take a lesson from nanoelectronics, for which truly useful electronic systems can adapt to dynamic environments and functionalities. Reconfigurable and tunable nanophotonic elements will go a long way towards enabling revolutionary systems functionality.

Systems Advantages

Small size does have several advantages to an optical system. The first may be obvious, but integration on a single chip and array fabrication is vital to combining photonics alongside electronics. Other examples include: (i) a nanocavity that can produce an extremely high-quality-factor filtering function and ultralow threshold lasing, (ii) tailorable dispersion properties for dispersion management of signals and production of very slow speed light, and (iii) single-photon sources for quantum processing and communications.

Applications

Nanophotonics may have novel utility for the following applications:

- A unique feature of optics is the ability to use the wavelength domain for communication and processing. Nanophotonics may be able to produce spectrally tunable elements for high speed parallel processing of optical signals.
- At present, there is little in the way of good optical buffers, and almost nothing exists for true random access memories (RAM). It is possible, based on slow light or bistability, to create functional optical buffers and RAMs. Such modules are crucial for achieving efficient optical packet-switched networking and all-optical data processing.

- The bulk of normal optical elements has always made optical logic gates quite undesirable. Nanophotonics may fix this problem. Moreover, a reconfigurable optical element could produce the optical equivalent of a field-programmable gate arrray. Reconfigurable logic may be implemented by electronic/optical biasing of photonic crystal elements, for which a collection of elements which operate as an AND gate under certain bias conditions can be turned into an OR gate by applying appropriate control signals.
- Nanophotonics, especially in the form of carbon nanotubes, may produce saturable absorbers and highly nonlinear elements that are beyond what can be made by conventional means. These characteristics may enable ultrafast switching, ultrashort optical pulses, and data regeneration.

Systems Challenges

On a systems level, there are several key challenges when considering nanophotonics:

1. A collection of nanophotonic elements must be combined in a reasonable and efficient architecture. Can nanophotonic elements be a one-to-one substitute for nanoelectronic elements of similar function, or is there a more fundamental difference? Can nanophotonic elements be simply assumed to be a one-to-one swap with bulk optical elements of similar function? Can nanophotonic elements be combined in a new architecture that takes advantage of their unique properties and provides new functionalities? The answers are unclear.

2. It would be highly desirable to have nanophotonic elements that are rapidly tunable. However, what are the systems problems that would require reconfigurability? How do these problems manifest themselves into specifications (i.e., tuning range, tuning speed, etc.) for the device fabricator?

3. Basic nanophotonic elements have been reported. However, at present, there is little modeling and simulation of a true ensemble of nanophotonic devices. The effects on optical signals are hardly known for a single element, much less a system of elements.

4. Photonics can do few things very fast. Electronics can do many things, but individual electronic elements are typically not as fast as photonic elements. Is there a way to achieve "optically assisted" electronic systems, for which optics can do what it does best and electronics does what it does best?

A Novel Vertical MRAM Design

Jian-Gang (Jimmy) Zhu, Carnegie Mellon University

Write addressing disturbances in the crosspoint addressing scheme employed in today's magnetic random access memory (MRAM) designs presents serious practical limitations in memory element downsizing. In Reference 1, we present a new vertical MRAM design with no write addressing disturbance. The memory element is of a ring shape and can be either a current-perpendicular-to-plane giant magnetoresistive trilayer or a magnetic tunnel junction. Sending a pulsed vertical current through the memory element performs (at different amplitudes) either a write or a read operation. The low switching current threshold between the two memory states enables the use of a magnetic tunnel junction. This design eliminates the half-select problem and significantly relaxes requirements on the switching threshold distribution of the memory element array.

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APPENDIX B. AGENDA

National Nanotechnology Initiative
Workshop on Grand Challenges in Nanoelectronics, Nanophotonics, and Nanomagnetics
February 11–13, 2004
Holiday Inn Arlington at Ballston, 4610 N. Fairfax Dr., Arlington, VA 22203

WEDNESDAY, FEBRUARY 11, 2004

Opening Plenary Session, Ballston Room

- 8:30–8:40 a.m. Welcome—Gernot Pomrenke (Air Force Office of Scientific Research)
- 8:40–9:00 a.m. Purpose of the Workshop—Mike Roco (NNI/National Science Foundation)
- 9:00–9:30 a.m. Keynote Address—Horst Störmer (Columbia/Lucent)
- 9:30–9:40 a.m. Discussion
- 9:40–10:25 a.m. Outbriefs from Previous NNI Workshops
  - Grand Challenge Workshop on Nanomaterials-—Robert Hull (UVA)
  - Silicon Nanoelectronics and Beyond Workshop—Ralph Cavin (SRC)
  - Grand Challenge Workshop on Nanometrology—Mike Postek (NIST)
- 10:25–10:45 a.m. Coffee break.

     Each of the remaining Plenary presentations is followed by 5 minutes of discussion.
- 10:45–11:10 a.m. Plenary I: Nanomagnetics & Spintronics—David Awschalom (UC Santa Barbara)
- 11:15–11:40 a.m. Plenary II: Nanophotonics—Shaya Fainman (UC San Diego)
- 11:45–12:10 a.m. Plenary III: Nanoelectronics—Evolutionary—Alan Seabaugh (Notre Dame)
- 12:15–1:30 p.m. Lunch
- 1:30–1:55 p.m. Plenary IV: Nanoelectronics—Revolutionary—Mark Reed (Yale)
- 2:00–2:25 p.m. Plenary V: Architecture and Systems Integration—Philip Kuekes (HP Labs)
- 2:30–2:55 p.m. Plenary VI: Fabrication and Manufacturing—Hank Smith (MIT)

First Breakout Sessions 3:20–5:30 P.M.

Session 1, Ballston Room

Acquiring—sense the environment in real time and transduce the status into processable signals

- Extend range and robustness of chem/bio sensors
- Diversity for reduction of false positive/negative
- Compact arrays
- Increased sensitivity
- Higher frequency EM response
- Close-to-zero consumed power

Session 2, Arlington Room

Storing—memory to store data in nonvolatile, compact media

- Bit density
- Radiation hardness
- Read/write speed

Session 3, Fairfax Room

Processing—logic circuitry to transform rapidly data into information

- Device density
- Interconnections (parallel processing)
- Speed
- Multilevel logic

Session 4, Wilson Room

Transmitting—interconnections to send data rapidly across chip, between chips and through space

- Higher frequency
- Lesser delay
- Wider bandwidth
- Lower consumed power

Session 5, Glebe Room

Systems Level integration

- Mixed signal
- Architectures for the 'Billion Transistor' chip
- Computing algorithms and circuits with potentially defective devices

Breakout Session Leaders Conference 5:30–6:00 P.M, Arlington Room

THURSDAY, FEBRUARY 12, 2004

Plenary Session, Ballston Room

- 8:30–8:55 a.m. Plenary VII: Modeling, Simulation, and Design - Mark Lundstrom (Purdue)
- 9:00–9:25 a.m. Plenary VIII: NEMS, Nanosensors, and Nanofluidics - Axel Scherer (Cal Tech)
- 9:30–9:55 a.m. Plenary IX: Power and Thermal Management in Nanosystems - Rama Venkatasubramanian (RTI)
- 10:00–10:20 a.m. Coffee Break
- 10:20–12:00 a.m. Report Back from First Breakout Sessions, Groups 1–5
- 11:10–12:00 p.m. Discussion: Preliminary Identification of Grand Challenges
- 12:00–1:00 p.m. Lunch
- 1:00 p.m.–3:00 noon Second Breakout Sessions, Groups 1–5
- 3:00–3:15 p.m. Coffee Break
- 3:15–4:05 p.m. Report Back from 2nd Breakout Sessions, Ballston Room
- 4:05–5:30 p.m. Discussion and Refinement of Grand Challenges
- 5:30–6:00 p.m. Plenary Session for Writing Subgroups, Arlington Room

FRIDAY, FEBRUARY 13, 2004

Report Writing Session, NSF Room II-595

- 8:30–10:00 a.m. Drafting report
- 10:00–10:15 a.m. Coffee Break
- 10:15–11: 30 a.m. Writing groups reconvene as needed
- 12:00 p.m. Draft Report completed. Workshop adjourns.

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APPENDIX D. GLOSSARY

AFM	atomic force microscopy
CAD	computer-aided design
CMOL	a proposed technology for nanoelectronics, combining CMOS with molecular-scale electronic devices
CMOS	complementary metal oxide semiconductor, the dominant technology for microelectronic devices
CNN	cellular nonlinear network
CNT	carbon nanotube
CVD	chemical vapor disposition
DRAM	dynamic random-access memory
EIT	electromagnetically induced transparency
FPA	focal plane arrays
FET	field effect transistor
FPGA	field-programmable gate array
Gb	gigabit, unit of information storage equal to 10^9 bits
GHz	gigahertz, SI unit of frequency equal to 10^9 cycles per second
GMR	giant magnetoresistance
HEMT	high-electron-mobility transistor
HRAM	holographic random-access memory
IR	infrared
IT	information technology
ITRS	International Technology Roadmap for Semiconductors
MESFET	metal-semiconductor field effect transistor
MEMS	microelectromechanical systems
MHz	megahertz, SI unit of frequency equal to 10^6 cycles per second
MOSFET	metal-oxide-semiconductor field effect transistor

MOSIS	Metal-Oxide-Semiconductor Implementation Service, an integrated circuit foundry operated by the University of Southern California and specializing in low-volume prototyping
MRAM	magnetic random-access memory
MRFM	magnetic resonance force microscopy
NCQD	nanocrystal quantum dots, esp. colloidal QDs, see also SAQD
NEMS	nanoelectromechanical systems
NIST	National Institute for Standards and Technology
nm	nanometer, SI unit of length equal to 10^{-9} meters
NNI	National Nanotechnology Initiative
NSOM	nearfield scanning optical microscopy
QCA	quantum cellular automata
QD	quantum dot
RAM	random-access memory
R&D	research and development
RF	radio frequency
RTD	resonant tunneling diode
SAQD	self-assembled quantum dot
SET	single-electron tunneling
SOI	silicon-on-insulator
SRAM	static random-access memory
STM	scanning tunneling microscopy
Tb	Terabit, unit of information storage equal to 10^{12} bits
UV	ultraviolet
VCSEL	vertical-cavity surface-emitting laser
VHM	volume holographic memory
VLSI	very large scale integration

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