NATIONAL SCIENCE FOUNDATION
4201 WILSON BOULEVARD
ARLINGTON, VIRGINIA 22230

NSF-SIA Graduate Student and Postdoctoral Fellow Supplements to NSF Centers in Nanoelectronics

Dear Colleague:

The National Science Foundation wishes to support mechanisms that advance long-term research in nanoelectronics. For this purpose, a joint activity has been initiated with the Semiconductor Industry Association (SIA). New approaches in emerging areas of electronics at the nanoscale need to be explored, as the ultimate limits to scaling of CMOS (Complementary Metal Oxide Semiconductor) technology are neared. Such efforts in developing the fundamental research base and creation of new knowledge are critical to sustaining the U.S. leadership and competitiveness in the global semiconductor industry.

The SIA, through the Nanoelectronics Research Initiative (NRI), a consortium of participating SIA member companies, has recently endorsed support of a nanoelectronic research initiative whose goal is to work with government and universities to pursue fundamental long-term research to develop new devices and technology beyond CMOS.

At the same time, NSF wishes to leverage its own significant fundamental research investments in nanoelectronics that have been made through both its priority area for Nanoscale Science and Engineering as well as its core programs.

NRI participants have recently visited a number of NSF Centers that address future directions in nanoelectronics. We have encouraged these industry participants to consider participating actively in these NSF Centers, when there is strong overlap of research interests, through both provision of supplementary support and assignment of industry researchers. Such linkages will benefit both the industry and the Center faculty participants in providing a common perspective in guiding the research agenda, sharing of the reporting outcomes, and improving education and training.

NSF is therefore establishing a cooperative effort with SIA through the NRI to enhance these linkages to Nanoscale Science and Engineering Centers (NSEC), Materials Research Science and Engineering Centers (MRSEC), or other appropriate NSF Centers involved in nanoelectronics research. We are jointly offering the opportunity for such NSF Centers to apply for supplemental funding that will support Research Assistantships for an additional cadre of Graduate Students and Postdoctoral Fellows who will work in collaboration with NRI participant mentors or assignees on exploratory Beyond CMOS research topics within the overall scope of the Center. The Center infrastructure and related research projects will provide a good environment and critical mass for collaborations. Our view is that this type of cooperative effort can have a large impact in accelerating advancement of new concepts in Beyond CMOS research and in developing future cadres of industry and faculty researchers to help drive the field.

NSF and NRI are making a joint investment of $2,000,000 in this opportunity, of which NSF will fund $1,000,000 and NRI will fund an additional $1,000,000. This $2,000,000

investment will allow us to fund up to four supplemental awards respectively to four NSF Centers, in the range of $400,000 to $600,000 total, for duration of three years. All references to investments are subject to the availability of funds. NSF and NRI will use their own award mechanisms in jointly funding these supplements. The NRI funds will be awarded as unrestrictive gifts, with no overhead or intellectual property requirements, on topics of interest to NRI participants consistent with the mission of the respective NSF Centers. Annual progress reports on work conducted under the supplemental funding will be submitted jointly to NSF and NRI. A process of joint oversight for the supplemental awards will be established by NSF and NRI.

NSF Centers interested in competing for these additional funds should submit to NSF supplemental proposals describing their planned research efforts. The proposal should be prepared in accordance with the NSF Grant Proposal Guide (GPG) and submitted via FastLane (see GPG Section II.D.2.b. for Supplemental Funding Requests; http://www.nsf.gov/publications/pub_summ.jsp?ods_key=gpg). The proposal should summarize the Center's current research in the area of nanoelectronics and describe the proposed new work on exploratory Beyond CMOS research in which the additional Graduate Students and Postdoctoral Fellows would be involved. The proposal must be accompanied by supporting letter(s) of collaboration from NRI participant(s).

Please contact the following officials should you need additional information:

- Directorate for Engineering:
  - Lawrence S. Goldberg, E-mail: lgoldber@nsf.gov
- Directorate for Mathematical and Physical Sciences
  - Ulrich Strom, E-mail: ustrom@nsf.gov
- Directorate for Computer and Information Science and Engineering
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NRI is administered by the Nanoelectronics Research Corporation (NERC), attn: Hans Coufal, 1101 Slater Road, Suite 120, Brighton Hall, Durham, NC 27703; (E-mail: nerc-nri@src.org). Six SIA member companies have signed the agreement with NERC to participate in NRI, and hence in this supplement opportunity: AMD, Freescale, IBM, Intel, Micron, and Texas Instruments.

The deadline for submission of supplement proposals via FastLane is September 30, 2005. All proposals will be reviewed internally by program officers from the participating NSF Directorates. This opportunity may be repeated in subsequent years.

Sincerely,

John A. Brighton
Assistant Director for Engineering

Michael S. Turner
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Peter A. Freeman
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