1 **PROCESSING ARCHITECTURE**
2 .Vector processor
3 ..Scalar/vector processor interface
4 ..Distributing of vector data to vector registers
5 ...Masking to control an access to data in vector register
6 ..Controlling access to external vector data
7 ..Vector processor operation
8 ...Sequential
9 ...Concurrent
10 .Array processor
11 ..Array processor element interconnection
12 ...Cube or hypercube
13 ...Partitioning
14 ...Processing element memory
15 ...Reconfiguring
16 ..Array processor operation
17 ...Application specific
18 ...Data flow array processor
19 ...Systolic array processor
20 ...Multimode (e.g., MIMD to SIMD, etc.)
21 ...Multiple instruction, Multiple data (MIMD)
22 ...Single instruction, multiple data (SIMD)
23 .Superscalar
24 .Long instruction word
25 .Data driven or demand driven processor
26 ..Detection/pairing based on destination, ID tag, or data
27 ..Particular data driven memory structure
28 .Distributed processing system
29 ..Interface
30 ..Operation
31 ...Master/slave
32 .Microprocessor or multichip or multimodule processor having sequential program control
33 ..Having multiple internal buses
34 ..Including coprocessor
35 ...Digital Signal processor
36 ..Application specific
37 ..Programmable (e.g., EPROM)
38 ..Offchip interface
39 ...Externally controlled internal mode switching via pin
40 ...External sync or interrupt signal
41 ..RISC
42 ..Operation
43 ...Mode switching
200 **ARCHITECTURE BASED INSTRUCTION PROCESSING**
201 .Data flow based system
202 .Stack based computer
203 .Multiprocessor instruction
204 **INSTRUCTION ALIGNMENT**
205 **INSTRUCTION FETCHING**
206 .Of multiple instructions simultaneously
207 .Prefetching
208 **INSTRUCTION DECODING (E.G., BY MICROINSTRUCTION, START ADDRESS GENERATOR, HARDWIRED)**
209 .Decoding instruction to accommodate plural instruction interpretations (e.g., different dialects, languages, emulation, etc.)
210 .Decoding instruction to accommodate variable length instruction or operand
211 .Decoding instruction to generate an address of a microroutine
212 .Decoding by plural parallel decoders
213 .Predecoding of instruction component
214 **INSTRUCTION ISSUING**
215 .Simultaneous issuance of multiple instructions
216 **DYNAMIC INSTRUCTION DEPENDENCY CHECKING, MONITORING OR CONFLICT RESOLUTION**
217 .Scoreboarding, reservation station, or aliasing
218 .Commitment control or register bypass
219 .Reducing an impact of a stall or pipeline bubble
220 **PROCESSING CONTROL**
221 .Arithmetic operation instruction processing
222 ..Floating point or vector
223 .Logic operation instruction processing
224 ..Masking
225 .Processing control for data transfer

226 .Instruction modification based on condition
227 .Specialized instruction processing in support of testing, debugging, emulation
228 .Context preserving (e.g., context swapping, checkpointing, register windowing
229 .Mode switch or change
230 .Generating next microinstruction address
231 .Detecting end or completion of microprogram
232 .Hardwired controller
233 .Branching (e.g., delayed branch, loop control, branch predict, interrupt)
234 ..Conditional branching
235 ...Simultaneous parallel fetching or executing of both branch and fall-through path
236 ...Evaluation of multiple conditions or multiway branching
237 ...Prefetching a branch target (i.e., look ahead)
238 ....Branch target buffer
239 ...Branch prediction
240 ....History table
241 ..Loop execution
242 ..To macro-instruction routine
243 ..To microinstruction subroutine
244 ..Exeception processing (e.g., interrupts and traps)
245 .Processing sequence control (i.e., microsequencing)
246 ..Plural microsequencers (e.g., dual microsequencers)
247 ..Multilevel microcontroller (e.g., dual-level control store)
248 ..Writable/changeable control store architecture
300 **BYTE-WORD REARRANGING, BIT-FIELD INSERTION OR EXTRACTION, STRING LENGTH DETECTING, OR SEQUENCE DETECTING**

E-SUBCLASSES

The following subclasses beginning with the letter E are E-subclasses. Each E-subclass corresponds in scope to a classification in a foreign classification system, for example, the European Classification system (ECLA). The foreign classification equivalent to an E-subclass is identified in the subclass definition. In addition to US documents classified in E-subclasses by US examiners, documents are regularly classified in E-subclasses according to the classification practices of any foreign Offices identified in parentheses at the end of the title. For example, "(EPO)" at the end of a title indicates both European and US patent documents, as classified by the EPO, are regularly added to the subclass. E-subclasses may contain subject matter outside the scope of this class.Consult their definitions, or the documents themselves to clarify or interpret titles.

E9.001 **ARRANGEMENTS FOR PROGRAM CONTROL, E.G., CONTROL UNIT (EPO)**
E9.002 .Using wired connections, e.g.,
E9.003 .Using stored program, i.e., using internal store of processing (EPO)
E9.004 ..Micro-control or micro-program arrangements (EPO)
E9.005 ...Execution means for micro-instructions irrespective of the micro-instruction function, e.g., decoding of micro-instructions and nano-instructions; timing of micro instructions; programmable logic arrays; delays and fan-out problems (EPO)
E9.006 ...Micro instruction function e.g., input/output micro-instruction; diagnostic micro-instruction; micro-instruction format (EPO)
E9.007 ...Loading of the micro-program (EPO)
E9.008 ...Enhancement of operational speed, e.g., by using several micro-control devices operating in parallel (EPO)
E9.009 ...Address formation of the next micro-instruction (EPO)

E9.01 ....Micro-instruction address formation(EPO)
E9.011 ....Arrangements for next micro-instruction selection (EPO)
E9.012 .....Micro-instruction selection based on results of processing (EPO)
E9.013 ......By address selection on input of storage (EPO)
E9.014 ......By instruction selection on output of storage (EPO)
E9.015 .....Micro-instruction selection not based on processing results, e.g., interrupt, patch, first cycle store, diagnostic programs (EPO)
E9.016 ..Arrangements for executing machine-instructions, e.g., instruction decode (EPO)
E9.017 ...Controlling the executing of arithmetic operations (EPO)
E9.018 ...Controlling the executing of logical operations (EPO)
E9.019 ...Controlling single bit operations (EPO)
E9.02 ...For comparing (EPO)
E9.021 ...For format conversion (EPO)
E9.022 ...Using storage based on relative movement between record carrier and transducer (EPO)
E9.023 ...Register arrangements, e.g., register files, special registers (EPO)
E9.024 ....Special purpose registers, e.g., segment register, profile register (EPO)
E9.025 ....Register structure, e.g., multigauged registers (EPO)
E9.026 .....Implementation provisions thereof, e.g., ports, bypass paths (EPO)
E9.027 .....Organization of register space, e.g., distributed register files, register banks (EPO)
E9.028 ...Instruction analysis, e.g., decoding, instruction word fields (EPO)
E9.029 ....Variable length instructions or constant length instructions whereby the relative length of operation and operand part is variable (EPO)
E9.03 ....Decoding the operand specifier, e.g., specifier format (EPO)Speech classification or search (EPO)
E9.031 ....With implied specifier, e.g., top of stack (EPO)
E9.032 ...For specific instructions not covered by the preceding groups, e.g., halt, synchronize (EPO)
E9.033 ...Controlling loading, storing, or clearing operations (EPO)
E9.034 ...Controlling moving, shifting, or rotation operations (EPO)
E9.035 ...With operation extension or modification (EPO)
E9.036 ....Using data descriptors, e.g.,
E9.037 ....Using run time instruction translation (EPO)
E9.038 ...Addressing or accessing the instruction operand or the result (EPO)
E9.039 ....Of multiple operands or results(EPO)
E9.04 ....Indirect addressing (EPO)
E9.041 ....Indexed addressing (EPO)
E9.042 .....Using index register, e.g., adding index to base address (EPO)
E9.043 ......Using wraparound, e.g.,
E9.044 ......Using scaling, e.g., multiplication of index (EPO)
E9.045 ...Concurrent instruction execution, e.g., pipeline, look ahead (EPO)
E9.046 ....Data or operand accessing, e.g., operand prefetch, operand bypass (EPO)
E9.047 .....Operand prefetch, e.g., prefetch instruction, address prediction (EPO)
E9.048 .....Maintaining memory consistency (EPO)
E9.049 ....Instruction issuing, e.g., dynamic instruction scheduling, out of order instruction execution (EPO)
E9.05 .....Speculative instruction execution, e.g., conditional execution, procedural dependencies, instruction invalidation (EPO)
E9.051 ......Using dynamic prediction, e.g., branch history table (EPO)

E9.052 ......Using static prediction, e.g., branch taken strategy (EPO)
E9.053 .....From multiple instruction streams, e.g., multistreaming (EPO)
E9.054 .....Of compound instructions (EPO)
E9.055 ....Instruction prefetch, e.g., instruction buffer (EPO)
E9.056 .....For branches, e.g., hedging branch folding (EPO)
E9.057 ......Using address buffers, e.g., return stack (EPO)
E9.058 .....For loops, e.g., loop buffer (EPO)
E9.059 .....With instruction modification, e.g. store into instruction stream (EPO)
E9.06 ....Recovery, e.g., branch miss-prediction, exception handling (EPO)
E9.061 .....Using multiple copies of the architectural state, e.g., shadow registers (EPO)
E9.062 ....Using instruction pipelines (EPO)
E9.063 .....Synchronization, e.g., clock skew (EPO)
E9.064 .....Technology-related problems thereof, e.g., GaAs pipelines (EPO)
E9.065 .....Pipelining a single stage, e.g., superpipelining (EPO)
E9.066 ....Using a slave processor, e.g., coprocessor (EPO)
E9.067 .....Which is not visible to the instruction set architecture, e.g., using memory mapping, illegal opcodes (EPO)
E9.068 ......For non-native instruction set architecture (EPO)
E9.069 .....Which is visible to the instruction set architecture (EPO)
E9.07 ......Having access to instruction memory (EPO)
E9.071 ....Using a plurality of independent parallel functional units (EPO)
E9.072 .....Decoding (EPO)
E9.073 ...Address formation of the next instruction, e.g., incrementing the instruction counter, jump (EPO)
E9.074 ....Program or instruction counter, e.g., incrementing (EPO)
E9.075 ....Branch or jump to non-sequential address (EPO)
E9.076 .....Unconditional, e.g., indirect jump (EPO)
E9.077 .....Conditional (EPO)
E9.078 .....For cyclically repeating instructions, e.g., iterative operation, loop counter (EPO)
E9.079 ....Condition code generation, e.g., status register (EPO)
E9.08 ....Selective instruction skip or conditional execution, e.g., dummy cycle (EPO)
E9.081 ....Sequential commutation, e.g., ring counter, cyclical pulse distribution (EPO)
E9.082 ..Arrangements for executing sub-programs, i.e., combinations of several instructions (EPO)
E9.083 ...Formation of sub-program jump address or of return address (EPO)
E9.084 ....Object Oriented Method Invocation (EPO)
E9.085 .....Optimizing for Receiver Type (EPO)
E9.086 .Using record carriers containing only program instructions (EPO)

FOREIGN ART COLLECTIONS

FOR 000 **CLASS-RELATED FOREIGN DOCUMENTS**