PUBLIC

UNITED STATES OF AMERICA
BEFORE FEDERAL TRADE COMMISSION

COMMISSIONERS:	**Deborah Platt Majoras, Chairman** **Orson Swindle** **Thomas B. Leary** **Pamela Jones Harbour** **Jon Leibowitz**

In the Matter of **RAMBUS INCORPORATED,** **a corporation.**	)	**Docket No. 9302**

APPENDIX TO BRIEF OF APPELLEE AND CROSS-APPELLANT RAMBUS INC.

Pursuant to the Commission's October 4, 2004 Order granting Rambus leave to file an appendix, Rambus submits this appendix to its appeal brief containing a glossary of terms.

Glossary of Terms

Auto precharge: DRAMs store information as minute quantities of electrical charge in memory cells – no charge is interpreted as "0" and positive charge as a "1." Sense amplifiers are circuits on the DRAM that sense the charge in a memory cell and amplify it when information is to be read from the DRAM. Before the sense amplifiers can perform this function, they must be "precharged" to an intermediate charged state. "Auto precharge" is a feature that was originally found in RDRAMs and later adopted by SDRAMs and DDR SDRAMs that allows the controller to determine whether the sense amplifiers are to be automatically precharged – that is, precharged without the need for a separate precharge command – at the end of a read or write operation.

Bit/Byte: A bit or "binary digit" is the unit of information used by digital computers that takes on only two values – "0" or "1." Each memory cell in a DRAM stores a single bit. A "byte" usually refers to eight bits. Since each bit in a byte can take on two values, a byte can take on 2^8, or 256, possible values.

Bus: As the Federal Circuit has found, the ordinary meaning of "bus" is "a set of signal lines to which a number of devices are connected, and over which information is transferred between devices." *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1095 (Fed. Cir. 2003).

Chipset / controller: "Chipset" generally refers to multiple computer chips known as "controllers" because they control the function of certain computer components and serve as interfaces between those components and the computer's main processor, the CPU ("central processing unit"). In PCs, the chipset generally includes a memory controller that controls the computer's main memory, although there are systems in which there is no memory controller and the CPU controls the memory directly.

DDR SDRAM Standard: Double Data Rate SDRAM Standard. The DDR SDRAM standard was adopted by JEDEC after the SDRAM standard and added some features to that standard while removing and/or modifying others. JEDEC began working on the DDR SDRAM standard in December 1996 and the standard was first published in late 1999.

DDR II SDRAM Standard: The JEDEC DDR II SDRAM Standard had not yet been published at the time of trial. It was known that the standard would add some features to the DDR SDRAM Standard while removing and/or modifying. In particular, the DDR II Standard was to retain the DDR SDRAM features of variable burst length, dual edge clocking and on-chip DLL, while expanding the use of programmable latency.

DRAM: Dynamic Random Access Memory. DRAM is a form of computer memory that makes up the main memory of most computers and is also used in other products. When one sees a computer advertised as having, say, 128 megabytes or 256 megabytes of RAM, this is referring to the main memory that the CPU uses for temporary storage when executing programs as opposed to, for example, the hard drive that is used for more permanent storage. "Random Access" means that any location in the DRAM can be accessed in about the same amount of time as any other, as opposed to, for example, a tape storage system in which data can only be accessed sequentially. "Dynamic" means that the information stored in the memory cells must be refreshed, that is read from and written back into the memory cells, thousands of times every second in order to retain the information.

Dual bank design / multibank design: The memory cells in a DRAM may be organized into one or more banks. The advantage of a dual or multibank design is that one bank may be accessed while others are precharging or performing other operations. RDRAM originally used a multibank architecture. Later, SDRAM and DDR SDRAM also adopted multibank architectures, generally using four banks, although some earlier chips used only two banks.

Dual edge clocking: A clock in a computer system refers to an electrical signal that transitions between low and high voltages at a regular rate – the "rising edge" is the transition from a low to high voltage while the "falling edge" is the transition from a high to low voltage – and is used to time operations. RDRAMs have always used both the rising and falling edges of the system clock to read and write data so as to double the data transmission rate. The SDRAM standard contemplates using only the rising edge of the clock, but the DDR SDRAM standard later adopted the dual edge clocking feature.

Externally supplied reference voltage: Computer systems determine whether a signal is meant to represent a "0" (low voltage) or a "1" (high voltage) by comparing the voltage of the signal to a reference voltage which is set to a value intermediate between the low and high values. RDRAMs have always received this reference voltage from an external source, that is, they used an "externally supplied reference voltage," in order to have a more accurate reference than an internally generated reference voltage could supply. An externally supplied reference voltage was not part of the SDRAM standard but was later adopted in the DDR SDRAM standard.

IEEE: The Institute of Electrical and Electronics Engineers. An association of the computer and electronics industry that engages in standard-setting and other activities.

Megabit: A megabit is roughly one million bits. Since it is simpler in binary arithmetic to deal with powers of 2, a megabit is actually defined as 2^{20} or 1,048,576 bits. Thus a 64 megabit DRAM would have the capacity to store somewhat more than 64 million bits of information.

Megahertz: One million cycles per second.

Memory module: A small circuit board that holds multiple memory chips and can be plugged into the motherboard of a computer. The main memory of most PCs consists of DRAM modules, but, in other applications, DRAM chips are sometimes used singly.

MOST / Mosys: Mosys was a company founded by a former Rambus engineer that developed the MOST DRAM in the mid-1990s. The MOST DRAM never achieved significant market penetration.

Multiplexed bus: As the Federal Circuit has noted, "multiplexing" simply refers to the "sharing of a single set of lines to send multiple types of information." *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094 (Fed. Cir. 2003). RDRAMs, SDRAMs and DDR SDRAMs all use multiplexing. Early RDRAMs multiplexed address, data and control on the same set of bus lines, although later RDRAMs did not do so. SDRAMs and DDR SDRAMs also use multiplexed busses: the lines used to transmit address information are also used to transmit control information (such as autoprecharge information and the data to be loaded into the mode register at system initialization).

Nanosecond: One billionth of a second. Light travels approximately one foot in one nanosecond. A frequency of 1 gigahertz corresponds to 1 nanosecond per cycle, while a frequency of 100 megahertz corresponds to 10 nanoseconds per cycle.

Narrow / wide bus: Although much used during the hearing, the terms "narrow bus" and "wide bus" are not well-defined and cannot be used to distinguish among the memory technologies at issue. Some RDRAMs, for example, have approximately the same number of bus lines as some SDRAMs.

Packetized / packet-based operation: "Packetized" operation is a vague term that has no clearly defined meaning. If "packet" is defined as broadly as Complaint Counsel suggest ("a set of related signals carried on a bus over multiple clock cycles that has a distinguishable beginning and ending point"), then RDRAMs, SDRAMs and DDR SDRAMs would all use packetized operation.

Phase locked loops / Delay locked loops: Phase locked loops (PLLs) and delay locked loops (DLLs) are circuits that can be used to align signals to other signals, such as system clocks. RDRAMs, including the earliest RDRAM design, use DLLs to align output data to the system clock. The bus speeds contemplated to be used with SDRAMs were not sufficiently high to require this technology, but DLLs were added to the DDR SDRAM standard for the same purpose as in RDRAMs. The Synclink Consortium endeavored to design a DRAM to be used with a high speed bus that did not require a PLL or DLL, but was unsuccessful and ultimately did add a DLL to its design.

Programmable CAS latency: Programmable latency refers to a feature used in RDRAMs that allows the delay between the receipt of a read (write) request and the output (input) of data in response to that request to be programmed into a register. Programmable read latency was subsequently adopted in the SDRAM and DDR SDRAM standards, where it is sometimes referred to as "programmable CAS latency" because a signal known as "CAS" is used, along with certain other signals, to signify a read operation. The DDR II SDRAM standard not only expands the use of programmable read latency, but also uses programmable write latency.

RamLink: RamLink was a specification for a memory technology, developed at an IEEE working group in the early 1990s after Rambus filed its patent application, that was never manufactured. After the failure of RamLink, the members of the working group tried to develop a memory technology, known as Synclink, that incorporated more features of RDRAM into their design.

RDRAM: Rambus Dynamic Random Access Memory. A type of DRAM designed by Rambus founders Michael Farmwald and Mark Horowitz in 1988 through the early 1990s with the goal of achieving 500 megabyte per second data rates, 50 to 100 times more than the DRAMs in use when they began their work. Many of the inventions implemented in RDRAM to achieve such high rates were described in Rambus's original April 1990 patent application. As the Federal Circuit has found, that original application disclosed "many inventions," *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094 (Fed. Cir. 2003); indeed, over 50 patents have issued to Rambus based on that original application. Among the features described in that original application, used in the first RDRAMs, and later incorporated into JEDEC's SDRAM and/or DDR SDRAM standard are programmable latency, variable burst, dual edge clocking and on-chip DLL. There have been a number of different versions of RDRAM using varying numbers of bus lines and varying degrees of multiplexing. Some RDRAMs have approximately the same number of bus lines as some SDRAMs.

SDRAM Lite: SDRAM Lite was a proposal for a simpler, cheaper version of the SDRAM Standard that was discussed at JEDEC during the mid-1990s and rejected. Even though SDRAM Lite did not contain all the features of SDRAM, the proposals for it retained the programmable burst length feature.

SDRAM Standard: SDRAM (Synchronous DRAM) was discussed at various JEDEC and non-JEDEC meetings in the early 1990s and was ultimately standardized at JEDEC to be a synchronous memory; that is, SDRAM, like the earlier RDRAM, received the system clock and used it to coordinate the timing of memory operations. The SDRAM standard also adopted the programmable latency and variable burst length features that had previously been used in RDRAM designs.

SyncLink: A specification for a memory technology that began at IEEE in the mid 1990s and was later developed in the private Synclink Consortium. Synclink, which was similar to RDRAM designs in numerous respects, was never commercialized.

System clock: A clock in a computer system refers to an electrical signal that transitions between low and high voltages at a regular rate. A "system clock" is a central clock that is used to coordinate the timing of various parts of the system.

Variable burst length: "Variable burst length or block size" refers to a feature used in RDRAMs that allows the amount of data to be transmitted by the DRAM in response to a read request (or written into the DRAM in response to a write request) to be varied. This feature was subsequently adopted in the SDRAM and DDR SDRAM standards. In SDRAMs and DDR SDRAMs, a value representative of this amount of data is programmed into a register called the mode register.

DATED: October 18, 2004

Gregory P. Stone
Steven M. Perry
Peter A. Detre
MUNGER, TOLLES & OLSON LLP
355 South Grand Avenue, 35th Floor
Los Angeles, California 90071-1560
(213) 683-9100

A. Douglas Melamed
Kenneth A. Bamberger
WILMER CUTLER PICKERING
HALE AND DORR LLP
2445 M Street, N.W.
Washington, D.C. 20037
(202) 663-6000

John M. Guaragna
GRAY, CARY, WARE & FREIDENRICH LLP
1221 S. MoPac Expressway, Suite 400
Austin, Texas 78746
(512) 457-7000

Attorneys for Appellee and Cross-Appellant Rambus Inc.

UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

In the Matter of	)	
	)	Docket No. 9302
RAMBUS INCORPORATED, a corporation.	)	

CERTIFICATE OF SERVICE

I, Kenneth A. Bamberger, hereby certify that on October 18, 2004, I caused a true and correct copy of the *Appendix To Brief Of Appellee And Cross-Appellant Rambus Inc.* to be served on the following persons by hand delivery:

Hon. Stephen J. McGuire
Chief Administrative Law Judge
Federal Trade Commission
Room H-112
600 Pennsylvania Avenue, N.W.
Washington, D.C. 20580

Richard B. Dagen, Esq.
Assistant Director
Bureau of Competition
Federal Trade Commission
601 New Jersey Avenue, N.W.
Washington, D.C. 20001

Donald S. Clark, Secretary
Federal Trade Commission
Room H-159
600 Pennsylvania Avenue, N.W.
Washington, D.C. 20580

Malcolm L. Catt, Esq.
Attorney
Federal Trade Commission
601 New Jersey Avenue, N.W.
Washington, D.C. 20001

Kenneth A. Bamberger

UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

In the Matter of	)	
	)	Docket No. 9302
RAMBUS INC.,	)	
a corporation,	)	
	)	

CERTIFICATION

I, Kenneth A. Bamberger, hereby certify that the electronic copy of *Appendix To Brief Of Appellee And Cross-Appellant Rambus Inc.* accompanying this certification is a true and correct copy of the paper version that is being filed with the Secretary of the Commission on October 18, 2004 by other means.

Kenneth A. Bamberger
October 18, 2004