Annex to the summons to attend oral proceedings

Communication
of the Technical Board of Appeal 3.5.1
pursuant to Article 11 (1) of the rules
of procedure of the Boards of Appeal

concerning case **T 0081/03 - 351** (please quote on all correspondence)

Munich, 14. 11. 03

S. Wibergh (Rapporteur)

(Enclosures: 7 pages)

1. The Board has made a preliminary study of the present appeal. The following observations are made without prejudice to the final decision.

2. The following abbreviations will be used:

O1: Micron Europe Ltd; Micron Technology Italia S.R.L.
O2: Infineon Technologies AG
O3: Hynix Semiconductor Deutschland GmbH
O4: Micron Semiconductor Deutschland GmbH

WO: WO-A-91/16680, ie the patent application on which the patent-in-suit EP-B-0 525 068 is based

Prior art (using and continuing the enumeration in the decision, "Anlage P6"):
D29: US-A-4 480 307
D30: D. K. Morgan, "The CVAX CMCTL - A CMOS Memory Controller Chip", Digital Technical Journal, No. 7, August 1988, p. 139-143
D17: B. R. Rau et al, "The Cydra 5 Departmental Supercomputer", IEEE Computer, Volume 22, Issue 1, January 1989, p. 12-35.
D25: US-A-4 481 572.

3. In accordance with the present requests of the patent proprietor the patent specification consists of the following documents:

Claims:

1	as granted (*main request);* or, alternatively as submitted with the grounds of appeal dated 7/4/2003 (*auxiliary requests I-VI*);
2 - 18	as granted;
Description:	as granted;
Drawings:	as granted.

4. Submissions from the parties received on or before 7 November 2003 have been considered for this opinion, the latest being the two letters dated 7 November 2003 by O4.

5. In the following, issues are indicated which are expected to be addressed at the oral proceedings.

The patent proprietor's main request

6. Added subject-matter (Art. 100(c) EPC)

6.1. The opposition division decided that claim 1 as granted contravened Art. 123(2) EPC (cf Art. 100(c) EPC). The discussion has concentrated on the issue of whether all the features of claim 103 as originally filed should be included in the claim. It has been argued that features 2a, 2b, M1, M2, 3 and 3a (cf the feature listing annexed to the present communication) should be present in claim 1. The opposition division accepted a claim containing M1, M2 and 3.

6.2. The Board shares the doubts as to whether the subject-matter of claim 1 as granted is supported by the original disclosure. Although claim 1 is directed to a "semiconductor memory device" and not to a bus, the claimed device may in principle be defined (indirectly) by the features in claim 103 of WO stating that it is "capable" of use with a certain bus. Furthermore, against the background of the original disclosure the combination register - multiplexed bus may be understood as a natural entity.

The opponents have argued that the description as a whole emphasises the bus features rather strongly and that, if the skilled person nevertheless understood that these features were not essential for obtaining the advantages of the claimed semiconductor device, this would be his technical contribution. Moreover, they have suggested that the features deleted from claim 103 of WO have been abandoned before grant and therefore cannot be reinstated. The Board tends to disagree since these features appear to be consistent with - and according to the opponents, even closely related to - the claimed device.

7. Novelty and inventive step - claim 1

7.1. Notwithstanding the above issues concerning Art. 123(2) EPC, the Board would like to make the following comments on the patentability of the claimed subject-matter.

7.2. In the appeal proceedings the opponents have concentrated on two newly filed documents, D29 and D30.

7.3. D29

Reference is here made to the arguments by the patent proprietor in the letter dated 25/9/2003, p.15 onwards. The following questions have been raised among others:

a) Does the expression "a semiconductor memory device" in claim 1 cover separate chips, and in particular four "64 K RAM parts" and an MCU (D29, col. 4, l. 10-16)?

Even if claim 1 did not cover this, it is not clear to the Board why it would be inventive, in spite of constantly increasing levels of integration, to combine such elements in one "device".

b) Does D29 disclose "a programmable access-time register for storing a value which is representative of a number of clock cycles of the external clock signal to transpire after which the memory device responds to a read request", and the feature that data are output "onto the external bus after the number of clock cycles of the external clock transpire"?

All parties seem to agree that the "memory access time" in D29 (col. 11, l 6) refers to communication between the MCU and the memory unit. The opponents' argument seems to be that this time will always be smaller than the time it takes for the MCU to respond to the read request (coming from a BIU, cf col. 12, l. 35) by outputting data on the MACD bus. If so, it does not matter that it is not known in advance - as the patent proprietor points out - exactly when data are output on the bus: whatever the delay, it will always exceed the "memory access time".

It therefore appears relevant that claim 1 does not define the point in time at which data are output but an (infinite) interval, as indicated by the words "after which". The original disclosure supports this interpretation: see eg WO p. 39, l. 9 and 10: "*at least* two cycles after" (italics added). It is true that the more limited

reading has also been disclosed in the initial application: "A request packet and the corresponding bus access are *separated by* a selected number of bus cycles" (WO, p. 15, bottom); or "/i/n most cases, a slave will respond *at* the selected access time by reading or writing data from or to the bus" (WO, p. 28, l. 15,16) (italics added). But there is no reason why claim 1 should only be interpreted in accordance with the latter particular passages in the description.

7.4. D30

The patent proprietor has not yet commented on D30. For the time being the Board finds the opponents' arguments convincing (see eg the discussion by O3 in the letter dated 19/9/2003, p. 47 onwards). One important point seems to be the meaning of the word "responds" on p. 142, right column, 2nd paragraph of D30.

7.5. D17 and D25

These documents - in particular - might also be of relevance.

7.6. To conclude, the Board is at present not convinced that the device of claim 1 is new and involves an inventive step.

8. Claim 5

The opposition division decided (points 25-28) that claim 5 complied with Art. 123(2) EPC. Since this is not self-evident, the question may have to be discussed.

The patent proprietor's first auxiliary request

9. Additional subject-matter

See above under main request. It may also be necessary to review the various objections made under Art. 123(3) EPC.

10. Inventive step

The connection means seems to be present in D29 and D30 as well.

The patent proprietor's second auxiliary request

11. Additional subject-matter

See above under main request.

12. Inventive step

12.1. Compared with D29

Claim 1 specifies that the value in the access-time register is established by data sent over the external bus. If this bus is taken to correspond to the MACD bus in D29 a difference can be seen in that, in D29, the "memory access time" is set over the SLAD bus, not over the MACD bus. O3 argues (letter dated 19/9/2003, paragraph bridging p. 51 and 52) that it would have been easy to transfer these data over the MACD bus instead. That may be, but it remains to be shown *why* the skilled person would do so. The known circuit may even have certain advantages. For example, the various processors do not have to know the "memory access time" for the different memory modules.

In this context it may be helpful to examine what problem is being solved according to the opposed patent. It is explained at p. 20 of WO that if a slave responds to a request in a specified time known to all devices on the bus then it never needs to arbitrate for the bus. If this idea is not recognised in D29 then it could not have led the skilled person to the feature that the "memory access time" should be set over the MACD bus. Whether or not another (obvious) problem with respect to D29 could suggest the feature has yet to be shown.

12.2. Compared with D30

As O3 points out (letter dated 19/9/03, p. 50, 51), the additional features seem to be known from D30.

The patent proprietor's third to sixth auxiliary requests

13. Additional subject-matter

It is noted that claim 1 of request IV and claim 1 of request VI both relate to subject-matter very similar to that of original claim 103.

14. Inventive step

The additional features in these requests primarily specify the bus to which the semiconductor memory device is connected. Since D29 describes a bus to which a plurality of semiconductor devices are connected in parallel, the bus having a plurality of bus lines for carrying substantially all address, data and control information, there being substantially fewer bus lines than the number of bits in a single address, these additional features are not expected to add anything new or inventive.

Miscellaneous

15. In view of the very large number of documents cited in the opposition proceedings, parties wishing to discuss in depth documents previously submitted, but neither referred to in the contested decision, nor in the appeal proceedings, are recommended to inform the Board and the other parties accordingly before the oral proceedings. The parties are asked to use the numbering referred to in point 2 above. The Board may disregard evidence which is not submitted in good time prior to the oral proceedings.

16. The same applies to amendments to the patent documents, which should be filed as early as possible (at least one month before the date set for the oral proceedings). At the same time an amended description and, if necessary, amended drawings should be filed.

Claim 103 of WO (as annexed to the minutes of the oral proceedings before the opposition division):

1 A semiconductor device,

2 capable of use in a semiconductor bus architecture including

2a a plurality of semiconductor devices

2b connected in parallel to a bus

M1 wherein said bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said semiconductor device for communication with substantially every other semiconductor device connected to the bus,

M2 and has substantially fewer bus lines than the number of bits in a single address,

3 said semiconductor device comprising connection means

3a adapted to connect said semiconductor device to said bus, and

4 at least one modifiable access-time register

4a accessible to said bus through connection means,

4b whereby data may be transmitted to said register via said bus

4b aa which establishes a predetermined amount of time that said semiconductor device thereafter must wait before using said bus in response to a request.