Complaint Counsel's Proposed List Of Rambus Expert Testimony To Be Covered In Rebuttal	Pages In Professor Jacob's Trial Testimony Where He Testified On The Topics In Question
LEE/RYAN/JACOBS TOPICS	
1. it is reasonable to assume that a first-tier manufacturer would run only 20 million units of a product iteration (Geilhufe, Tr. 9562:10-9563:4; 9725:1-9726:23)	This issue was not addressed in Professor Jacob's trial testimony. However, because it was not addressed in his initial or rebuttal report, he may not now testify regarding the issue.
2. use of fixed CAS latency parts is difficult and costly because (a) based on all options contained in the JEDEC standard as adopted (and not on industry usage or practice), 3 separate parts would be required (Geilhufe, Tr. 9578:10-23, Tr. 9682:20-9683:2)	See below at pp. 12-13 (Jacob point 1) for Professor Jacob's testimony on the fixed CAS latency alternative.
(b) it would cost approximately $100,000 more than programmable CAS latency in design costs (Geilhufe, Tr. 9575:9-21)	Professor Jacob did not address Mr. Geilhufe's specific cost figures in his trial testimony. However, because the issue was not addressed in his initial or rebuttal report, he may not now address the specific cost figures in his testimony.
(c) it would require assumptions about the speed grade of the parts (Soderman, Tr. 9347:8-9348:11)	
(d) it would interfere with a manufacturer's ability to speed grade parts (Soderman, Tr, 9348:12-9349:15)	

EXHIBIT C

Complaint Counsel's Proposed List Of Rambus Expert Testimony To Be Covered In Rebuttal	**Pages In Professor Jacob's Trial Testimony Where He Testified On The Topics In Question**
(e) it would add expense due to decreased die yield (Geilhufe, Tr. 9577:1-9578:9)	
3. use of fixed burst length parts is difficult and costly because (a) based on all options in the JEDEC standard as adopted (and not on industry usage or practice), it would require 4 separate parts (Geilhufe, Tr. 9594:25-9595:3)	Professor Jacob testified extensively about the alternatives of using fixed CAS latency and/or burst length extensively in his direct examination (Tr. 5371:2 – 5378:16, 5398:25 – 5403:1). In this testimony he attempted to respond to various of the disadvantages raised by Dr. Soderman and Mr. Geilhufe. For example, with respect to the added expense of fixed CAS latency, Professor Jacob testified as follows: <u>Tr. 5376:5 – 5377:11 (Jacob):</u> Q. Now, in comparison with use of a mode register to program CAS latency, what advantages, if any, would have been realized by using fixed CAS latency in the 1991 to 1996 time period? A. It would be potentially a simpler design. Certainly you don't have a mode register, so that's a simpler mechanism. You potentially would have fewer testing stages, and again, that depends on where you decide to fix the CAS latency. For example, if you fix it earlier in the design stage, you don't actually have to test the fabricated part for multiple CAS latencies. So the test costs and design costs can go down. Q. You referred to a simpler design. Why do you include that as among the advantages? A. Well, because you don't have to build and test a mode register. Q. Are you familiar with the term "die size"? A. Yes, I am. Q. And what does "die size" mean? A. Thank you. It's the size of the semiconductor die. And the cost of manufacturing goes roughly with the area to the third power, the area of this semiconductor part, so if you have a part that is 1 percent larger, it's approximately 3 percent more expensive to manufacture. So for example, if you eliminate a mode register, you eliminate some of the size

Complaint Counsel's Proposed List Of Rambus Expert Testimony To Be Covered In Rebuttal	Pages In Professor Jacob's Trial Testimony Where He Testified On The Topics In Question
	of the part and it can make it smaller and therefore cheaper.
(b) it would involve extra photo tool costs of $50,000	Professor Jacob did not address Mr. Geilhufe's specific cost figures in his trial testimony. However, because the issue was not addressed in his initial or rebuttal report, he may not now address the specific cost figures in his testimony.
(c) it would cost approximately $100,000 more than programmable burst length in design costs (Geilhufe, Tr. 9594:5-12)	Professor Jacob did not address Mr. Geilhufe's specific cost figures in his trial testimony. However, because the issue was not addressed in his initial or rebuttal report, he may not now address the specific cost figures in his testimony.
4. based on all options in the JEDEC standard as adopted (and not on industry usage or practice), use of both fixed CAS latency and fixed burst length would require 12-15 separate parts (Geilhufe, Tr. 9601:7-16)	
5. use of fixed CAS latency would not permit the mode register to be removed from the DRAM (Geilhufe, Tr. 9736:24-9737:19)	This precise issue was raised in Professor Jacob's cross-examination. Complaint Counsel could have followed up to the extent necessary on re-direct. <u>Tr. 5593:25 – 5595:9 (Jacob – cross)</u> Q. As one of the advantages of going to a fixed latency part, yesterday you testified that if you did that, you could eliminate the mode register in SDRAMs; right? A. Correct. Q. Now, the mode register in SDRAMs is used for purposes other than to store CAS latency, isn't it? A. Yes, it is.

Complaint Counsel's Proposed List Of Rambus Expert Testimony To Be Covered In Rebuttal	**Pages In Professor Jacob's Trial Testimony Where He Testified On The Topics In Question**
	Q. In particular, it stores the burst length; is that right? A. Yes. Q. And it stores the burst type; right? A. Yes. Q. And in DDR SDRAMs they expand the use of the mode register and they store other things in the mode register; right? A. I believe so. Q. And in DDR-II SDRAMs they're expanding the use of the mode register yet further again, storing even more things in the mode register; right? A. I'm not certain about that. Q. You don't know one way or the other? A. I don't have the DDR-II spec in front of me and I have not consulted it recently, so I don't know offhand. Q. If you just remove the programmable CAS latency feature and went to fixed latency, you would still need the mode register for these various other purposes; correct? A. If you were to retain those features, you would require the portion of the mode register used to implement those features and you could eliminate the portion of the mode register and the portion of the control logic that would be used to implement the CAS latency feature.
6. (a) electrically blown fuses and anti-fuses are not reliable (Soderman, Tr. 9356:18-9357:2)	This precise issue was raised in Professor Jacob's cross-examination. Complaint Counsel could have followed up to the extent necessary on re-direct. <u>Tr. 5596:23-25 (Jacob cross):</u> Q. Now, you know that electrical fuses are not as reliable as laser-blown fuses; right? A. No, I do not know that.
(b) based on a survey of "maybe 50" out of "hundreds" of data sheets, only about 2 out of 50 SDRAMs appear to incorporate electrically blown fuses (Soderman, Tr.	

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9357:3-9358:1)	
(c) anti-fuse technology is not generally available in DRAMs (Geilhufe, Tr. 9582:20-9583:19; Tr. 9732:11-9734:21)	This issue was raised during Professor Jacob's direct examination and was followed up during cross-examination. Complaint Counsel could have followed up further during re-direct to the extent necessary. <u>Tr. 5381:21 – 5382:1 (Jacob):</u> Q. Now, the fuses that are used in synchronous DRAMs today, are they laser blown or electrically blown or both or other? A. They are both. They are – some manufacturers use laser-blown fuses; other manufacturers use electrically blown fuses. <u>Tr. 5595:21 – 5596:22 (Jacob – cross):</u> Q. And you also mentioned that another type of fuse is an electrical fuse; right? A. An electrically blown fuse, correct. Q. And you said that some DRAM manufacturers are using electrically blown fuses; right? A. Yes, I did. Q. What DRAM manufacturers are those? A. I believe Infineon and Micron and possibly Hynix. Q. And do you know what parts they're using those electrical fuses in? A. I don't know the part numbers. Q. Do you know how many parts Micron is using electrical fuses in? A. I believe a substantial number. Q. Is Micron using the electrical fuses in all of its DRAM products? A. I don't know if it's all, but I believe it's a substantial number. That's my understanding. Q. Do you know how many? A. A substantial number of the parts that they create. Q. Do you know what percentage? A. No. Q. Do you know what percentage of Infineon's parts use electrical fuses?

Complaint Counsel's Proposed List Of Rambus Expert Testimony To Be Covered In Rebuttal	**Pages In Professor Jacob's Trial Testimony Where He Testified On The Topics In Question**
	A. No, I do not.
(d) the use of laser blown fuses would lead to reduced yield due to speed distribution (Geilhufe, Tr. 9585:21-9586:9)	
7. (a) based on the number of bits provided for in the JEDEC standard as adopted (and not on industry usage or practice), setting CAS latency and burst length via pins each would require three bits of information (Geilhufe, Tr. 9589:22-9590:6; 9599:8-9600:1)	
(b) it would be necessary to add pins (Geilhufe, Tr. 9724:16-21;9741:8-974 2:1; Soderman, T	See below at pp. 13-14 (Jacob point 2) for Professor Jacob's testimony about adding pins.
8. running a single edge clock at a higher frequency (a) would cause significant clock distribution problems (Soderman, Tr. 9393:20-9394:8)	See below at pp. 16-17 (Jacob point 5) for Professor Jacob's testimony about the advantages and disadvantages of running a single edge clock at a higher frequency.
(b) would require on-DIMM clock circuitry and possibly an on-DIMM PLL/DLL, which would cost $3.80 (Geilhufe,	Complaint Counsel has already introduced evidence anticipating and attempting to rebut Mr. Geilhufe's cost figure relating to an on-DIMM PLL/DLL: <u>Tr. 6049:6 – 6050:19 (Goodman):</u>

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Tr. 9609:17-9610:5)	Q. Do you know how much a standard PLL costs? A. I believe it's generally around $1. Q. And in light of these modifications, would the PLL for Kentron be cheaper or more expensive? A. It's going to be more expensive, slightly more expensive, because it has more features. Q. Are these features complicated? A. No. Q. And the volume relationship that we described earlier would also be applicable to this situation? A. Yes. Q. Are you aware of what determines the cost of the PLL? A. No. Q. And who manufactures PLLs? A. There's several companies. The one that we're working with is called ICS. Q. So, that's the sole source for your PLL? A. Currently. Q. Are you currently in discussions with other companies? A. Yes. Q. What is the purpose of the PLL in the QBM module? A. Again, it's a -- it provides the various clocks that are required in the technology, at 1x, 1x90 and 2x. Q. Is the $2 the initial cost? A. No, it will be slightly higher at launch, but we expect it to come down pretty rapidly in cost. Q. Do you have an expectation for at what volume that would occur? A. No, again, just we expect QBM to be in high volume fairly rapidly. Q. What do you mean by "high volume"? A. Again, the marketplace is very large, and we're looking at, you know, getting some type of market share that would immediately put us into a high-volume category.
9. moving the DLL to the module would cost $3.80 for the DLL (Geilhufe, Tr. 9613:13-25)	This is covered in point 8, above.

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10. SLDRAM was unable to design a high speed DRAM using Vernier circuitry, without an on-chip DLL (Soderman, Tr. 9412:22-9415:9)	This precise issue was raised in Professor Jacob's cross-examination. Complaint Counsel could have followed up to the extent necessary on re-direct. Since Professor Jacob's testimony preceded that of Terry Lee, Complaint Counsel could have also questioned Mr. Lee about this issue once it had been raised. <u>Tr. 5618:3 – 5621:18 (Jacob – cross):</u> Q. Now, one of the alternatives that you mentioned yesterday to this idea of using an on-chip DLL was a vernier circuit; right? A. Yes. Q. And you're aware, correct, that the SLDRAM chip designed by SyncLink used a vernier? A. Yes, I am. Q. And isn't it also true that the SLDRAM chip used an on-chip DLL in addition to the vernier in order to make the timing more accurate? A. I'm not sure what you mean by making the timing more accurate. The DLL was not used to capture data. That's not the timing that it was making more accurate. So I don't know what you're getting at. Q. Well, you testified in your deposition that the purpose of that DLL on top of the vernier in SyncLink SLDRAMs was to make the timing more accurate, didn't you? A. I didn't say it was on top of the vernier. Q. Could we turn to your deposition, at page 167. And on that page, we're discussing a conversation that you had with Mr. Terry Lee of Micron about the use of verniers and DLLs and SLDRAMs. Do you see that? A. Yes, I do. Q. And you're describing what Mr. Lee told you in your response there; right? A. I am describing my understanding of the way the vernier and the DLL are used in the SLDRAM work. Q. And in the sentence of your response, lengthy response that begins at line 17, you state, "And so this static calculation was done, and the vernier was set in each of the DRAMs, and that the DLL was used to make that timing a little bit more accurate"; correct?

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	MR. OLIVER: Objection, Your Honor. Counsel has read a half of a sentence here. I believe if the entire answer is read you'll see that the answer is completely consistent with his testimony this morning. JUDGE McGUIRE: I'll give you that opportunity to do that either on your questioning or I'll let you interject at this time after he's done with that half question and I guess complete, you know, the statement. MR. OLIVER: I'd like to do that at this time if I could, please, Your Honor. JUDGE McGUIRE: All right. BY MR. DETRE: Q. Do you have the question in mind, Professor Jacob? A. No, I do not. Q. If we could begin reading at line 17 of your response, you state, "And so this static calculation was done, and the vernier was set in each of the DRAMs, and that the DLL was used to make that timing a little bit more accurate." That's what you stated; correct? A. That's what I state there. MR. OLIVER: Your Honor, may I read the entire question? JUDGE McGUIRE: Yes, Mr. Oliver. MR. OLIVER: Thanks, Your Honor. Beginning on page 167, line 1, reading through page 167, line 25: "QUESTION: And what did Mr. Lee tell you about the use of verniers in DLLs and SLDRAMs? "ANSWER: He said that contrary to what Soderman had said, that the SLDRAM part that was built did use verniers. Soderman had said that they abandoned the use of a vernier in favor of a DLL and therefore that the vernier is a useless mechanism. Lee said that the verniers were used at both the controller side and the DRAM side to capture data. "They were used to, quote-unquote, level the bus so that all DRAMs responded to transactions at nominally the same time so that even though a nearby

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	DRAM would receive a request sooner than a faraway DRAM, the nearby DRAM would delay its response so that it appeared -- so that it would write things out onto the bus at the same time that the further-away DRAM would. "And so this static calculation was done, and the vernier was set in each of the DRAMs, and that the DLL was used to make that timing a little bit more accurate, and that the verniers were used to delay the data with respect to the strobe so that the strobe captured the data. "So the verniers, according to Mr. Lee, were used in the capture of data and not the DLL. That's my recollection."
11. because the proposed alternatives didn't include circuit designs, they were poorly thought out (Geilhufe, Tr. 9673:17-9674:5)	The inadequacy of Professor Jacob's investigation of the proposed alternatives was raised on cross-examination. Complaint Counsel could have followed up on redirect to the extent necessary. <u>Tr. 5591:9-17 (Jacob – cross):</u> Q. Now, other than with respect to those three alternatives that I just mentioned now that you discussed yesterday, increasing the number of pins on the DRAM, increasing the number of pins on the module and using the burst terminate command for burst length, you did no simulation or modeling of any kind with respect to the other alternatives you testified about; correct? A. Not that I can recall.
12. DDR II (a) expands the use of programmable CAS latency (Soderman, Tr. 9351:7-9353:3)	
(b) initially planned to use a single burst length,	As set out below, Complaint Counsel's witnesses testified to this exact point on cross examination (prior to the testimony of

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but subsequently reverted to programmable burst length (Soderman, Tr. 9369:12-23)	both Professor Jacob and Mr. Lee). Complaint Counsel could have asked these witnesses to address the issue. <u>Tr. 4633:11-13 (Macri):</u> A. Is programmable burst length using the mode register part of the proposed DDR2 standard? A. Yes. <u>Tr. 4675:17 – 4676:9 (Macri – cross):</u> A. What was the change that related to burst length that occurred during the time period June through September 2001? A. The committee had received a presentation by both Intel and AMD that showed there were performance gains for adding back burst eight and also showing performance gains by adding a very simple burst interrupt so that you could interrupt a burst eight and turn it into a burst four. Those presentations were justified on performance, but they were also justified on the fact that they would be nondisruptive changes to the design. A. But it hadn't been disruptive to have in the design a fixed burst length up until that point, had it? A. Our goal was simplicity, and since previously no one was able to come up with a performance justification, that's why we simplified it. <u>Tr. 2833:25 – 2834:21 (Krashinsky –cross):</u> Did JEDEC, in connection with the DDR-II specification, also consider eliminating programmable latency for burst length or programmable -- I'm sorry -- did JEDEC also consider eliminating programmable burst length? A. At the time we were set for one programmable burst length. JUDGE McGUIRE: All right. Now, again, so that I understand it in context, you're talking about in the period of time that he attended these meetings; is that

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	correct? MR. STONE: Yes, I am, Your Honor. JUDGE McGUIRE: All right. BY MR. STONE: Q. At the time 2000 and 2001, isn't it correct that JEDEC was considering using a single burst length for DDR-II? A. Correct. Q. And they had developed their preliminary specification on the basis of a single burst length for DDR-II; correct? A. Correct.
(c) limits the use of the burst terminate command because of timing difficulties (Soderman, Tr. 9376:19-9377:20)	

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JACOB TOPICS	
1. The proposed alternatives of using fixed CAS latency and/or burst length would not have involved the disadvantages or expense claimed by Dr. Soderman and Mr. Geilhufe.	Professor Jacob testified extensively about the alternatives of using fixed CAS latency and/or burst length extensively in his direct examination (Tr. 5371:2 – 5378:16, 5398:25 – 5403:1). In this testimony he attempted to respond to various of the disadvantages raised by Dr. Soderman and Mr. Geilhufe. For example, with respect to the added expense of fixed CAS latency, Professor Jacob testified as follows: <u>Tr. 5376:5 – 5377:11 (Jacob):</u> Q. Now, in comparison with use of a mode register to program CAS latency, what advantages, if any, would have been realized by using fixed CAS latency in the 1991 to 1996 time period? A. It would be potentially a simpler design. Certainly you don't have a mode register, so that's a simpler mechanism. You potentially would have fewer testing stages, and again, that depends on where you decide to fix the CAS latency. For example, if you fix it earlier in the design stage, you don't actually have to test the fabricated part for multiple CAS latencies. So the test costs and design costs can go down. Q. You referred to a simpler design. Why do you include that as among the advantages? A. Well, because you don't have to build and test a mode register. Q. Are you familiar with the term "die size"? A. Yes, I am. Q. And what does "die size" mean? A. Thank you. It's the size of the semiconductor die. And the cost of manufacturing goes roughly with the area to the third power, the area of this semiconductor part, so if you have a part that is 1 percent larger, it's approximately 3 percent more expensive to manufacture. So for example, if you eliminate a mode register, you eliminate some of the size of the part and it can make it smaller and therefore cheaper.

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2. Setting CAS latency and/or burst length in the read/write command or by means of pins would not involve adding the number of pins, the increased board or controller complexity, or the increased cost projected by Mr. Geilhufe.	Professor Jacob testified extensively about the alternatives of setting CAS latency and/or burst length in the read/write command or by means of pins in his direct examination (Tr. 55385:22 –5393:20, 5405:13 – 5408:19). In this testimony he responded specifically to the disadvantages raised by Mr. Geilhufe about requiring additional pins and increasing complexity. For example, with respect to these alternatives to programmable CAS latency, Professor Jacob's testimony included the following: <u>Tr. 5387:1-7 (Jacob):</u> Q. Now, would this option have required that additional pins be included in the DRAM? A Not in all cases. In many examples there are no-connect pins on DRAMs. There are pins left over after the specification is made that have no function assigned to them, and so these could have been used to transmit this information. <u>Tr. 5388:10 – 5389:10 (Jacob):</u> Q. Now, in your opinion, what would the advantages of using a dedicated pin to determine CAS latency have been as opposed to using a mode register to determine CAS latency? A. Well, it would be a simpler design because you would eliminate the mode register as well as the interface required to put information into the mode register, and it would be a smaller design and therefore a cheaper design to manufacture, so it would be simpler and cheaper. Q. Now, in your opinion, what would have been the disadvantages, if any, had JEDEC chosen to use a dedicated pin to determine CAS latency as opposed to using a mode register? A. If they had no-connect pins available, there would be no disadvantage. If there were no no-connect pins available or not enough no-connect pins available, then you would have to add new pins to the package, and that would increase cost. But it would be relatively insignificant. Q. Why do you say it would be relatively insignificant? A. Because, again, as I said, these -- this type of interface, a

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	DC-type interface, is much less expensive than adding, for instance, what they call a high-speed pin, a data-type pin. Tr. 5391:12 - 5392:25 (Jacob): Q. Now, what, if any, would have been the advantages had JEDEC chosen to explicitly identify CAS latency in the read command rather than using a mode register to program CAS latency? A. The advantage would be that you would eliminate the mode register and the circuitry required to decode special commands and put that information into the mode register, so it would make the part potentially smaller and simpler. Q. And would that have had any implication for cost? A. Yes. That potentially would reduce the cost of the part. Q. What, if any, would have been the disadvantages had JEDEC chose to explicitly identify CAS latency in the read command rather than using a mode register? A. The disadvantage would be that it would make the decoding logic on the DRAM more complex because you would have these additional commands that would need to be decoded, so that would make the part more complex, so you'd have a trade-off there. And if, for example, there were certain combinations that you had to support and you didn't want to redefine, for example, the DQ mask pins in the way I've described, it might require an additional pin. Q. Focusing on the use of existing pins for the moment, you mentioned that it might require more complex decode circuitry? A. Yes. Q. How significant would that be? A. Not very significant. It would be on the order of the complexity that you're removing by not having to decode the initialization commands. Q. In other words, on the order of the complexity that would be removed by taking off the mode register? A. Absolutely.

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3. Design of a burst terminate command is fully viable.	Professor Jacob testified extensively about the viability of suing a burst terminate command to set burst length in his direct testimony. (Tr. 5408:20 – 5411:12) In this testimony, he specifically responded to Dr. Soderman's criticism that this alternative would have led to inefficiencies: <u>Tr. 5411:1-12 (Jacob):</u> Q. Now, what, if any, would have been the disadvantages had JEDEC chosen to use a long burst length with a burst terminate command rather than programming burst length through the mode register? A. You potentially could run into inefficiencies on the bus depending upon how you -- depending upon how the memory controller handles those situations where you want to terminate the burst down to 4 from 8. Q. How significant a disadvantage would that have been? A. I don't believe it would have been very significant.
4. Using a faster single-edge clock does not require conducting other operations at a faster speed.	Professor Jacob testified extensively about the alternative os using a faster single-edge clock as an alternative to dual-edge clocking in his direct testimony. (Tr. 5433:8 – 5435:3) In this testimony, he specifically addressed whether, in his opinion, this would require conducting other operations at a faster speed: <u>Tr. 5434:21 – 5435:7 (Jacob):</u> Q. This example, would this require any increase in the speed or frequency of command signals? A. No, it would not. You would still send your command and addresses at the same rates that you send them now. The only thing that would change would be the data rate and it would be similar to or, rather -- I'm sorry. The only thing that would change would be the clock frequency that accompanies your data transmission. Your data rates would be the same as in DDR parts of today, but your clock frequency would be twice what it is.
5. Using a faster	In his testimony about using a faster single-edged clock,

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single-edged clock would not involve significant engineering difficulties (including use of on-DIMM clock circuitry or an on-DIMM PLL/DLL).	Professor Jacob also addressed the engineering difficulties involved: <u>Tr. 5434:8 – 5435:3 (Jacob):</u> Q. Now, what, if any, would have been the advantages of running a single-edged clock at twice the frequency rather than using a dual-edged clock? A. The advantages include the fact that you have the single-edged clock versus a dual-edged clock, meaning that the edge rates need not be symmetric, the duty cycle need not be 50 percent, and it gives you those extra edges per data packet that are not present in a dual-edged clocking scheme, you have an edge to transmit data as well as another edge to receive data, whereas in a dual-edged clocking scheme you only have an edge to drive data or you have an edge to receive data, but you don't have both. Q. Now, what, if any, would have been the disadvantages had JEDEC chosen to double the frequency of a single-edged clock rather than using a dual-edged clock? A. You have a clock signal that is transitioning at twice the rate of present, of present systems, which means it would be burning twice as much power as present systems.
6. The proposed alternatives to dual-edge clocking do not involve using both edges of the clock.	Professor Jacob testified generally that his proposed alternatives were, in fact, *alternatives* to dual-edge clocking – i.e. that they do not involve using both edges of the clock.